Description

The P9235A-R is a 3W, magnetic induction, wireless power transmitter for low power applications. The system-on-chip operates with an input voltage range of 4.5 – 5.5V while integrating micro-controller, voltage regulation, over-current protection, full bridge power stage drivers and on-chip simultaneous voltage and current demodulation.

The transmitter includes industry-leading 32bit ARM® Cortex®-M0 processor offering a high level of programmability, while consuming extremely low standby power. The device features two LED outputs with pre-defined user programmable blinking patterns, buzzer and programmable over-current protection supporting wide range of applications. The I²C serial communication allows the user to read back information such as voltage, current, frequency and fault conditions. Together with the P9027LP-R receiver, the P9235A-R is a complete wireless power system solution.

The P9235A-R is available in a Pb-free, space-saving VFQFN 5 mm X 5 mm, 40 pin package. The product is rated over an operating temperature range of -40ºC to +85ºC.

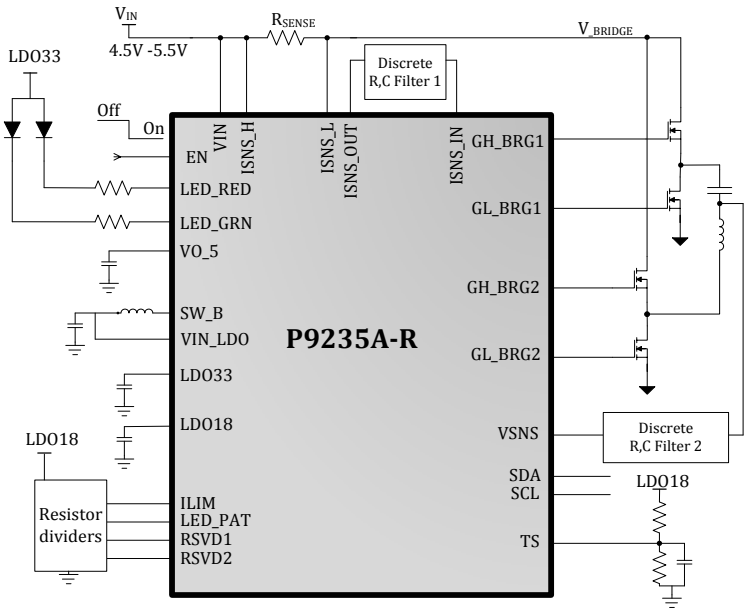
Features

- V_{IN} range: 4.5 - 5.5 V
- Supports receiver for up to 3W of power transfer
- 80% peak efficiency (when coupled with P9027LP receiver)
- Integrated power stage drivers
- Low standby power
- Simultaneous voltage and current demodulation
- Integrated 32 bit ARM® Cortex®-M0 Processor
- Supports I²C interface for field programmability
- Programmable current limit
- Over-Current and Over-Temperature protection
- Active low enable pin for electrical on/off
- Pre-defined programmable LED patterns
- Dedicated remote temperature sensing
- -40ºC to +85ºC ambient operating temperature range
- VFQFN 5mm X 5mm, 40 pin package

Typical Applications

- Smart Watches
- Headsets
- Health and Fitness monitors
- Portable Medical applications

Figure 1. Application Diagram



Absolute Maximum Ratings

These absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 3, 4 and 5 may cause permanent damage to the device. Functional operation of the P9235A-R at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect long-term reliability.

Table 1. Absolute Maximum Ratings Summary (All voltages are referred to ground.)

Pins	Rating	Units
$\overline{EN}$, VIN, SW_B, VBRG_IN, SW_BRG1, SW_BRG2, ISNS_H, ISNS_L, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
VO_5, VO_33, VIN_LDO, LED_GRN, LED_RED, VDDIO, GPIO_A4, GPIO_B2, GPIO_B3, RSVD1, RSVD2, SCL, SDA, ILIM, LED_PAT, TS, BUZ, GL_BRG1, GL_BRG2, VSNS_IN, ISNS_IN, ISNS_OUT, VDRV_IN	-0.3 to 6	V
GND_S, GND_BRG, VSNS_GND, GND_B, EPGND	±0.3	V
LDO18	-0.3 to 2	V

Thermal Characteristics

Table 2[1,2,3]. Package Thermal Characteristics

Symbol	Description	QFN Rating	Units
Θ_{JA}	Thermal Resistance Junction to Ambient	28.5	°C/W
Θ_{JC}	Thermal Resistance Junction to Case	21.87	°C/W
Θ_{JB}	Thermal Resistance Junction to Board	1.27	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Notes:

1. The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 85°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
2. This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3” x 4.5” in still air conditions.
3. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins	+/- 2000	V
CDM	All pins.	+/- 500	V

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Electrical Characteristics

Table 4. Device Characteristics

V_{IN} = 5 V, VDDIO = 3.3 V, $\overline{EN}$ = 0V, L_P= 6.5 µH, C_P = 400 nF T_A = -40°C to +85°C. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies and UVLO						
V_{IN}	Input Operating Range		4.5	5.0	5.5	V
$V_{IN_UVLO_FW}$	Firmware Controlled Under-Voltage Lockout.	V_{IN} Rising		4.3		V
I_{STD_BY}[2]	Standby Mode Current	Periodic ping		12		mA
I_{SHD}	Shutdown Current	ENB = V_{IN}		25	80	µA
Enable - $\overline{EN}$						
V_{OH_ENB}	Output logic high		2.0			V
V_{OL_ENB}	Output logic low				0.25	V
Buck Converter[1,2] - C_{OUT}=10µF; L=4.7µH						
V_{OUT}	Buck Output Voltage	V_{IN}>5.5V		5		V
I_{OUT}	Output Current			50		mA
N-Channel MOSFET Drivers						
$T_{LS_ON_OFF}$	Low Side Gate Drive Rise & Fall times	C_L= 3nF; 10 – 90%, 90 – 10%		50	150	ns
$T_{HS_ON_OFF}$	High Side Gate Drive rise & Fall times	C_L= 3nF; 10 – 90%, 90 – 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier offset voltage	Measured at ISNS_OUT pin; ISNS_H=ISNS_L		0.6		V
$ISEN_{ACC_TYP}$	Measured Current sense accuracy	V_{R_ISEN}=25mV, I=1.25A		±3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of channels			10		
$V_{IN,FS}$	Full scale Input voltage			2.4		V
LDO18[1,2] - C_{OUT}=1µF;						
V_{OUT18}	Output voltage		1.71	1.8	1.89	V
$\Delta V_{OUT}/V_{OUT}$	Output voltage accuracy			±5		%
I_{OUT18_MAX}	Maximum load current			10		mA
LDO33[1,2] - C_{OUT}=1µF;						
V_{OUT33}	Output voltage		3.15	3.3	3.45	V
$\Delta V_{OUT}/V_{OUT}$	Output voltage accuracy			±5		%
I_{OUT33_MAX}	Maximum Output Current			20		mA
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		°C
		Threshold Falling		120		°C

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Table 5. Device Characteristic (Continued)

V_{IN} = 5 V, VDDIO = 3.3 V, $\overline{EN}$ = 0V, L_P = 6.5 µH, C_P = 400 nF T_A = -40°C to +85°C. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Clock Oscillators						
F_{LSOSC}	Low speed clock			50		kHz
F_{CLOCK}	OSC clock frequency			6		MHz
F_{CENTER}[2]	PLL VCO frequency			120		MHz
General Purpose Inputs/Outputs (GPIO)						
V_{IH}	Input high voltage		0.7*VDDIO			V
V_{IL}	Input low voltage				0.3*VDDIO	V
I_{LKG}	Leakage Current		-1.0		1 .0	µA
V_{OH}	Output logic high	I=8mA	2.4			V
V_{OL}	Output logic low	I=8mA			0.5	V
SCL, SDA (I²C Interface)						
f_{SCL_MSTR}	Clock Frequency	As I²C master		400		kHz
f_{SCL_SLV}	Clock Frequency	As I²C slave		400		kHz
C_B	Capacitive load	For each bus line			100	pF
C_{BIN}	SCL, SDA Input Capacitance			5.0		pF
I_{LKG}	Leakage Current		1.0		1.0	µA

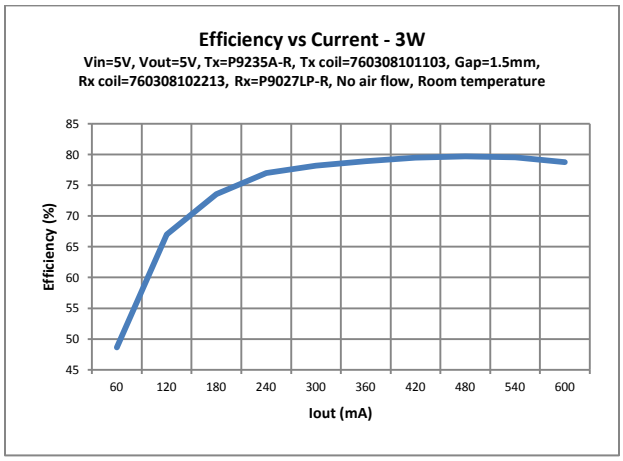
NOTES:

1. Do not externally load. For internal biasing only.
2. Guaranteed by design and not subject to 100% production testing

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Typical Performance Characteristics

Figure 2. Typical Performance Characteristics – 3W



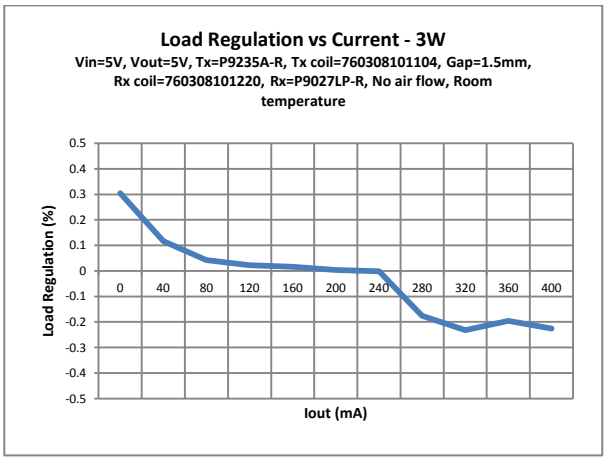
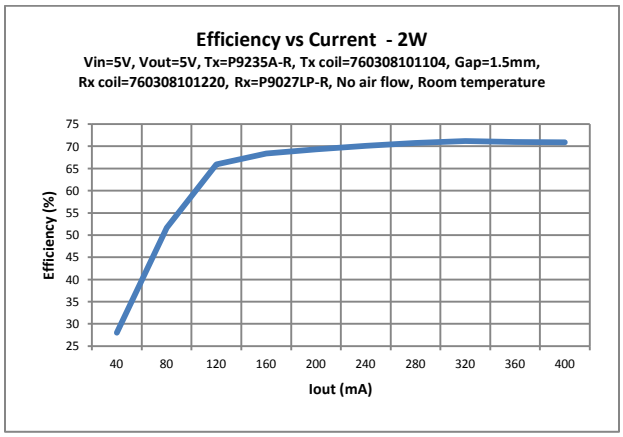


Figure 3. Typical Performance Characteristics – 2W



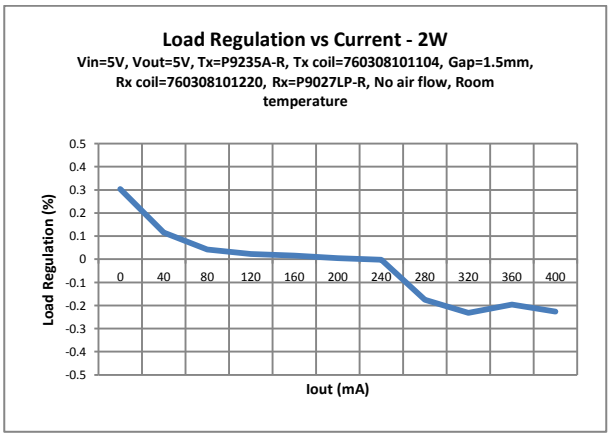
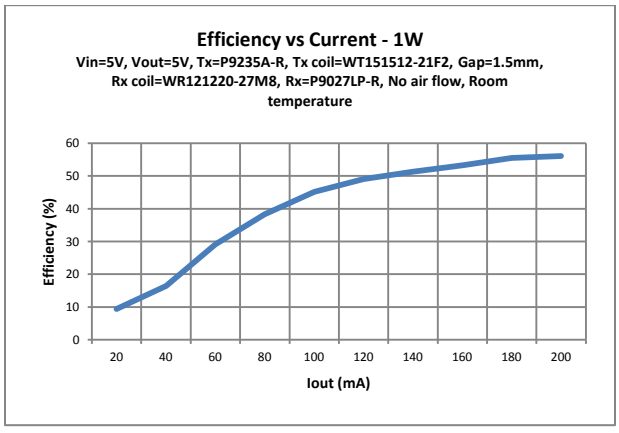
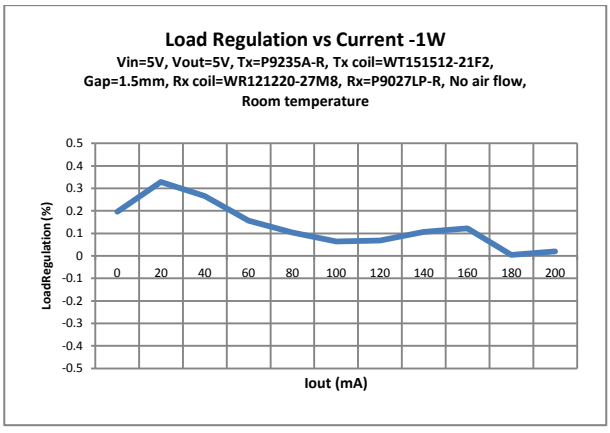


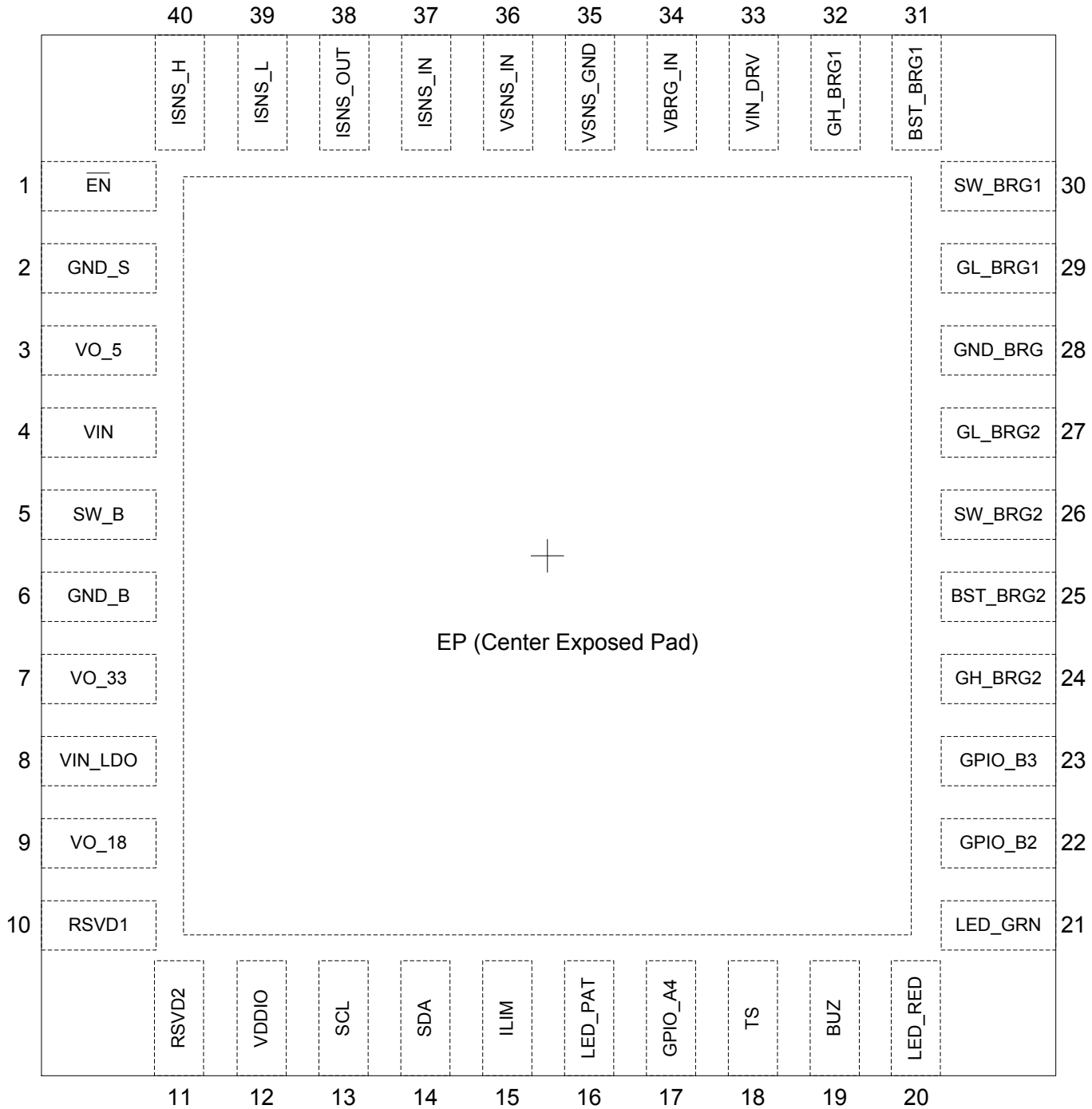
Figure 4. Typical Performance Characteristics – 1W





Pin Configuration

Figure 5. QFN-40 5 mm x 5 mm – Top View



Pin Description

Table 6. Pin Descriptions

Pin(s)	Name	Type	Description
1	$\overline{EN}$	I	Active low enable pin. When connected to logic high, the device shuts down and consumes less than 25 µA of current. When connected to logic low, the device is in normal operation.
2	GND_S	-	Ground connection.
3	VO_5	O	Regulated output voltage used for the internal device biasing. Connect a 1 µF capacitor from this pin to ground. This pin should not be externally loaded.
4	VIN	I	Input power supply. Connect a 10 µF capacitor from this pin to ground.
5	SW_B	O	Step-down regulator switch node. Connect one of the terminals of a 4.7 µH inductor to this pin.
6	GND_B	-	Ground connection.
7	VO_33	O	Regulated 3.3 V output voltage used for internal device biasing. Connect a 1 µF capacitor from this pin to ground. This pin should not be externally loaded.
8	VIN_LDO	I	Low Dropout input power supply. Connect this pin to a 5 V source, either to the output of the 5 V output step-down regulator or to the input power supply pin, VIN.
9	VO_18	O	Regulated 1.8 V output voltage used for internal device biasing. Connect a 1 µF capacitor from this pin to ground. This pin should not be externally loaded.
10	RSVD1	I	This pin is reserved for internal use only. Pull down to ground with an external 47 kΩ resistor.
11	RSVD2	I	This pin is reserved for internal use only. Pull down to ground with an external 47 kΩ resistor.
12	VDDIO	I	Input power supply for all GPIOs. Can be connected to a power supply ranging from 1.8 – 5.0 V.
13	SCL	I	Clock for I²C communication. Connect a 5.1 K resistor from this pin to VO_5
14	SDA	I/O	Data for I²C communication. Connect a 5.1 K resistor from this pin to VO_5
15	ILIM	I	Programmable over-current limit pin. Connect a resistor from this pin to GND to set the current-limit threshold. To disable the current-limit, connect the pin directly to GND. For more information, see current limit application section.
16	LED_PAT	I	Programmable LED pattern selection. Connect the center tap of the resistor divider to this pin. For more information on various LED blinking pattern, see LED pattern application section.
17	GPIO_A4	I/O	General purpose input/output. The GPIO's power is supplied from the VDDIO pin. This pin is configured as an output. If it is not used then it may be left floating.
18	TS	I	Remote temperature sensing. Connect a 10 k NTC via a voltage divider to this pin.
19	BUZ	O	Buzzer pin output.

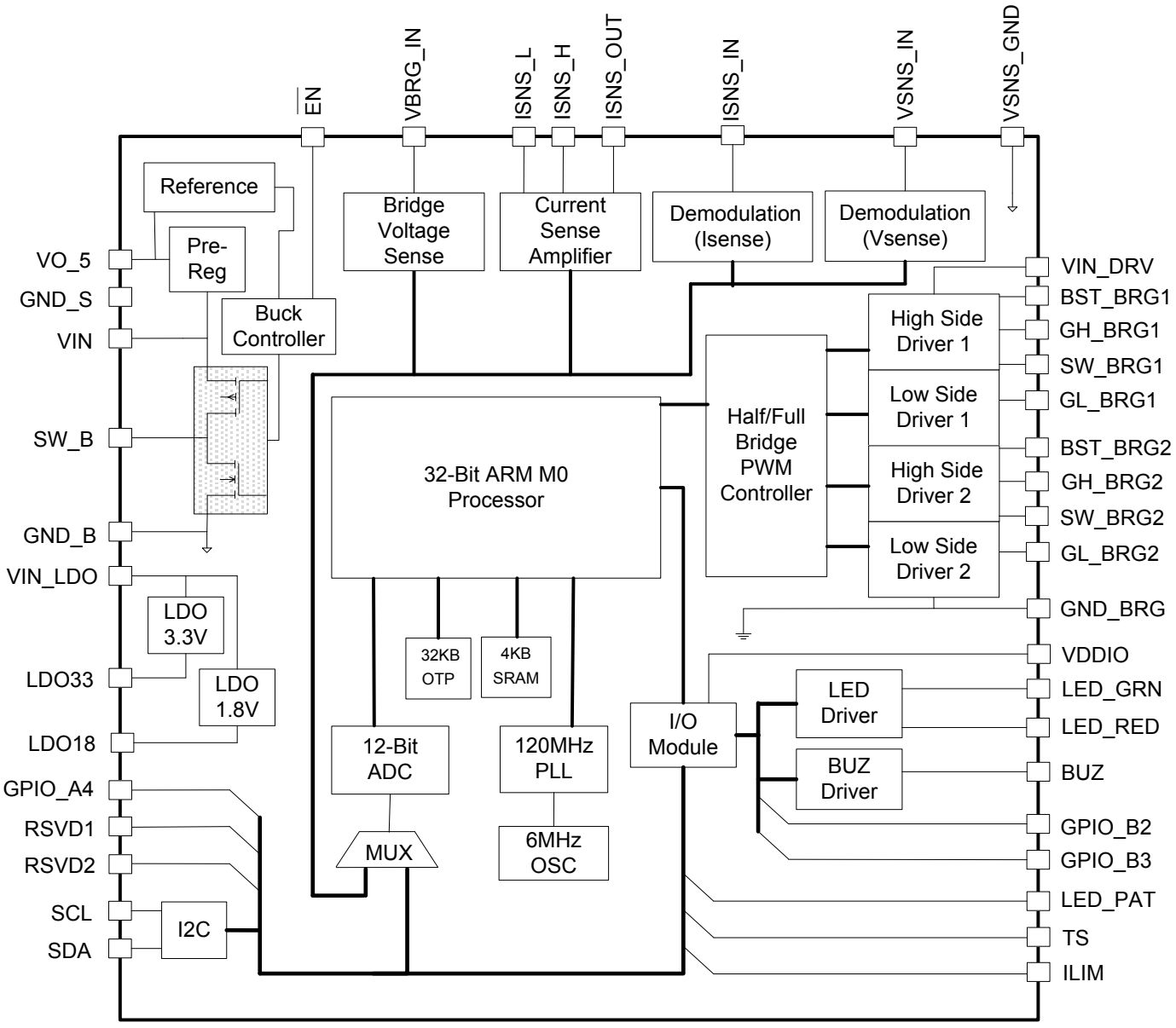
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Table 7. Pin Descriptions (continued)

Pin(s)	Name	Type	Description
20	LED_RED	O	Open drain output. Connect a red LED to this pin. This pin can sink a maximum current of 25 mA (typical)
21	LED_GRN	O	Open drain output. Connect a green LED to this pin. This pin can sink a maximum current of 25 mA (typical)
22	GPIO_B2	I/O	General purpose input/output. The GPIO's power is supplied from the VDDIO pin. This pin is configured as an output. If it is not used then it may be left floating.
23	GPIO_B3	I/O	General purpose input/output. The GPIO's power is supplied from the VDDIO pin. This pin is configured as an output. If it is not used then it may be left floating.
24	GH_BRG2	O	Gate driver output for the high-side half bridge 2.
25	BST_BRG2	I	Bootstrap pin for the half bridge 2. Tie an external capacitor from this pin to the SW_BRG2 to generate a drive voltage, which is higher than the input voltage.
26	SW_BRG2	O	Switch node for half bridge 2.
27	GL_BRG2	O	Gate driver output for the low-side half bridge 2.
28	GND_BRG	-	Ground return connection for half bridge 1 and half bridge 2 external FETs and associated components.
29	GL_BRG1	O	Gate driver output for the low-side half bridge 1.
30	SW_BRG1	O	Switch node for half bridge 1.
31	BST_BRG1	I	Bootstrap pin for half bridge 1. Tie an external capacitor from this pin to the SW_BRG1 to generate a drive voltage higher than the input voltage.
32	GH_BRG1	O	Gate driver output for the high-side half bridge 1.
33	VIN_DRV	I	Input power supply for the internal gate drivers. Connect a 10 µF capacitor from this pin to ground.
34	VBRG_IN	I	Bridge voltage input voltage sense.
35	VSNS_GND	-	Ground connection for voltage sense signals.
36	VSNS_IN	I	Voltage modulation signal input.
37	ISNS_IN	I	Current modulation signal input. ISNS_OUT is fed into this pin after external conditioning
38	ISNS_OUT	O	Differential (ISNS_H - ISNS_L) current sense buffered output.
39	ISNS_L	I	Input current sense negative input
40	ISNS_H	I	Input current sense positive input
	EPGND	-	Expose pad. Thermal pad for heat sinking purposes. Connect EPGND to GND plane.

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Figure 6. P9235A-R Block Diagram



Theory of Operation

General System Architecture

A wireless power transfer system has two sub-systems: the wireless power transmitter (Tx) and the wireless power receiver (Rx). The transmitter makes power available through a full bridge/half bridge driven LC resonant tank. It transmits power through the generation of an AC magnetic field. Once the receiver coil is placed near the magnetic field, the field will induce an AC current through the receiving coil where it is converted into a DC current.

High Level Control Scheme

Wireless power systems adopt a set of pre-defined in-band communication commands as the close loop control strategy. The amount of power transferred is controlled by the receiver. The receiver sends out Control Error Packets (CEP) to the transmitter to increase power, decrease power, or maintain the power level. The transmitter responds by adjusting the switching frequency and/or duty ratio. The receiver requests more power by sending out a CEP, which includes a positive numerical value. The communication is digital. The communication 1's and 0's ride on top of the power link that exists between the two coils.

Wireless Power Communication

When the transmitter is not transferring power to the receiver, it is in the low power Standby Mode. While in this mode, in order to detect a receiver, the transmitter sends out periodic analog and digital pings.

Analog pings are very short AC detection pulses. These short pulses do not transmit enough energy to wake up the receiver, only to detect its presence. Digital pings, on the other hand, do transmit enough power to enable the receiver to wake up and begin communication. The transmitter uses digital pings to listen for a response from a receiver. After the transmitter detects a receiver, it may extend the digital ping. This causes the system to proceed to the Identification and Configuration phase.

Once the receiver is detected and powered up, it will send out communications packets to handshake with the transmitter. The first communication packet the receiver sends out is the Signal Strength packet, followed by Identification packets and Configuration packets. Once the handshake process is done, the receiver will send out periodic Control Error packets and Received Power packets to adjust the power.

If the receiver needs to stop the power transfer, it will send out an End of Power Transfer (EPT) communication packet. The transmitter stops transmitting power immediately, and starts pre-defined routines according to the information decoded from the EPT packet.

System Fault Protection

The wireless power transfer system implements system level protection. These include over voltage, under voltage, over current, and over temperature protection. On the transmitter side, whenever a fault condition is detected, it shuts down the whole system immediately and protects itself. If the receiver detects a fault condition, it will send the End of Power Transfer packets to shut down the system. The transmitter will continue to transmit power from the time of the receiver fault detection to the reception of the End of Power Transfer packet.

Over voltage protection: If the transmitter V_{IN} is greater than 5.5 V, and the system is not in the Power Transfer mode, then the transmitter will shut down until the V_{IN} is in the range of 4.5 V to 5.5 V. If the system is already in the Power Transfer mode, then the transmitter takes no action.

Under voltage protection: If the transmitter V_{IN} is less than 4.5 V, the transmitter will shut down for five minutes, or until the V_{IN} is cycled. off/on.

Over current protection: The transmitter uses a 20 mΩ sense resistor ($R_{SENSE,}$ R6) to monitor the current. If the transmitter detects a current greater than the programmed current limit, it will shut down for five minutes, or until V_{IN} is cycled off/on.

Over temperature protection: If the TS pin (pin 18) voltage falls below 600 mV (typical) then the transmitter will shut down. It will restart once the TS voltage rises above 800 mV (200 mV hysteresis).

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Applications Information

LDOs

There are three internal LDOs, which supply the P9235A-R internal voltage rails. Do not externally load any of the LDOs. VO_5 is the output of a high voltage LDO, which serves as the pre-regulator. VO_5 initially supplies the input voltage to the other two LDOs until the buck regulator output voltage powers up.

The other two LDOs, VO_33 and VO_18, have output voltages of 3.3 V and 1.8 V, respectively. The analog circuitry is power by the 3.3 V LDO. The digital circuitry is powered by the 1.8 V LDO.

LDO Input and Output Capacitors

For proper load voltage regulation and operational stability, low ESR ceramic capacitors are required on the input and output of each LDO. A 10 µF low ESR ceramic cap is recommended for both the input (C19) and output (C14, C27, C29) capacitors. The capacitor's connection to the ground pin should be as short as possible for optimal device performance.

Buck Regulator

The buck regulator is the power supply for the 3.3 V and 1.8 V LDOs, and thus for all the internal analog and digital circuitry, excluding the pre-regulator only. Do not externally load any of the LDOs. The current sourcing capability of this internal buck regulator is 50 mA maximum. The two half bridge gate driver circuits are directly power by the buck regulator.

The P9235A-R buck regulator operates in hysteretic pulse mode to set the output voltage and will regulate the output voltage at 5 V (typical) when VIN is greater than 5.5 VDC. For operation with VIN less than 5.5 V, the buck output will decrease below 5 V. When the VIN is less than 5 V, the regulator will switch to a linear mode that is similar to a LDO.

The input (C18, C19) and output (C20, C21) capacitors must be connected directly between each power rail pins and power GND pin (and placed as close as possible to the respective IC pins). The output capacitors should be selected based on the typical reference schematic to guarantee control loop stability. A 10 µF low ESR ceramic cap is recommended for both the bulk input (C19) and bulk output (C21) capacitor.

The buck regulator output voltage is connected to the VIN_LDO pin; therefore, the connection from the buck output to the VIN_LDO pin should be made as wide and short as possible to minimize output voltage errors.

Buck Inductor Selection

A 4.7 µH inductor (L1) is used for the P9235A-R buck regulator. Select the inductor saturation current rating to exceed the value of peak inductor current (during normal operation and start up). The inductor included in the Bill of Materials is recommended. Keep the inductor DCR to a minimum to improve the efficiency of the regulator.

Decoupling Capacitors

As with any high-performance mixed-signal IC, P9235A-R must be isolated from the system power supply noise. A decoupling capacitor of 0.1 µF should be connected between each power supply pin (includes VIN, the buck regulator, LDOs, VBRG_IN, V_BRIDGE: C18, C20, C28, C9, C12, C31) and the PCB ground plane. It must be placed as close as possible to these pins. The decoupling capacitor must be mounted on the component side of the PCB.

Note: The VO_33 does not need this decoupling capacitor if the user follows the IDT recommended, optimized layout.

Full Bridge Input Capacitor

At least one 10 µF capacitor (C19) must be placed at the VIN pin. At least three 10 µF capacitors (C10, C11, C30) must be placed across the full bridge voltage source (the V_BRIDGE node in the schematic) to minimize voltage ripple and voltage drop due to the large current requirements. The full-bridge is used to convert DC voltage to AC voltage for power transfer. These 10 µF capacitors must be placed as close as possible to the respective pins.

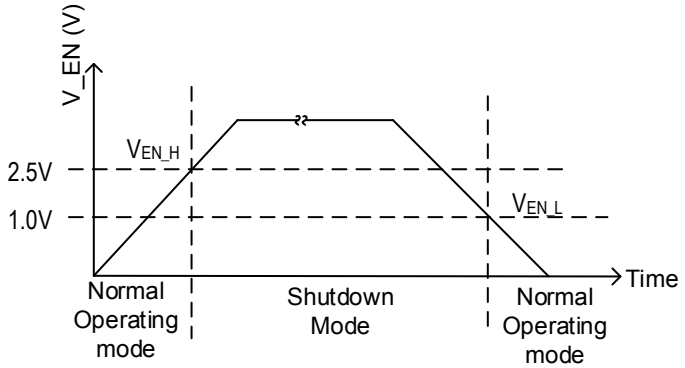
Note: If the half bridge FETs are not physically close together then two 10 µF capacitors per half bridge are needed. Follow the IDT optimized layout in order to minimize these capacitors

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Enable Function (EN Pin)

When voltage on the $\overline{EN}$ pin is greater than 2.5 V, the P9235A-R shuts down the buck regulator. It goes onto Shutdown Mode, which disables all the analog and digital modules. Current consumption in Shutdown Mode is less than 25 µA. When $\overline{EN}$ is less than 1.0 V, the P9235A-R is fully functional, and all the blocks are enabled. Figure 7 shows EN thresholds.

Figure 7. EN pin threshold



When $\overline{EN}$ is less than 1.0 V and a receiver is not yet detected, the P9235A-R is in the low power Standby Mode. The P9235A-R periodically comes out of Standby Mode to generate digital and analog pings to detect the presence of a receiver. Between these pings, the P9235A-R continues in the Standby Mode to maintain low power consumption.

Input Current Sense

The P9235A-R monitors its input current by using an external sense resistor (R6), in series with the input voltage rail of the full bridge LC tank driver circuit (Q2, Q3). The voltage across the sense resistor is fed into the ISNS_H and ISNS_L pin via an RC filter (R4,R5,C2). The differential signal of ISNS_H and ISNS_L is processed by the internal ADC and associated firmware.

The current sense resistor is sensitive to noise, as well as to circuit board conditions. On the layout of PCB, it is necessary to use Kelvin sensing when routing the ISNS_H and ISNS_L connections. Incorrect current reporting may also occur when a re-worked board has residue (e.g. flux) around the sense resistor. More details are available in the P9235A-R layout guide, AN936.

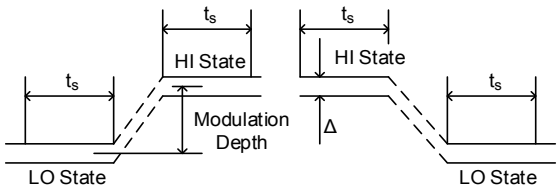
For 2W/3W applications, use a 20mΩ sense resistor (R6). For 1W applications use a 50 mΩ sense resistor. Adjust the resistor divider (R27, R31) value on the LED_PAT pin according to the sense resistor used.

Communication and Modulation

The wireless power system uses an in-band communication, such that the current and voltage on the transmitter's power coil assume two states, namely a HI state and a LO state. For a valid state, the amplitude is constant, within a certain variation Δ, for at least t_s ms. If the wireless power receiver is properly aligned to the transmitter's power coil, and for all appropriate loads, at least one of the following two conditions shall apply, as shown in Figure 8.

Difference of the amplitude of the transmitter current in the HI and LO state: ≥ 15 mA.
Difference of the amplitude of the transmitter voltage in the HI and LO state: ≥ 200 mV.
The minimum hold time for a valid HI or LO state: ≥ 0.15 ms

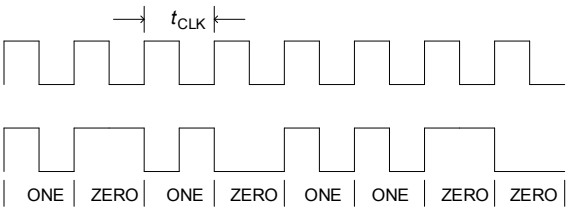
Figure 8. Modulation



The receiver uses a 2 kHz, differential, bi-phase encoding scheme to modulate data bits onto the power signal. A logic ONE bit is encoded

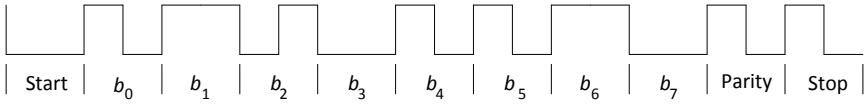
using two narrow transitions. A logic ZERO bit is encoded using two wider transitions as shown in Figure 9.

Figure 9. Bit encoding scheme.



Each byte in the communication packet comprises 11 bits in an asynchronous serial format. The start bit is always LO. This is followed by 8 bits of data. The final two bits are parity and stop, as shown in Figure 10.

Figure 10. Byte encoding scheme.



The wireless power receiver communicates with the wireless power transmitter via communication packets. Each communication packet has the following structure:

Figure 11. Communication packet structure

Preamble	Header	Message	Checksum

LED Pattern Selection

A green LED and a red LED indicate status. The LED Patterns depend on the selected LED mode. The voltage applied through resistor divider to the LED_PAT pin selects the desired LED mode. Table 8 shows the available selections. Note that the LED pin selection is combined with the input current sense resistor. Pulling the LED_PAT pin to GND via a 47 kΩ resistor will set the LED pattern to the default Mode 1.

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Table 8. LEDs indication table pattern

Current Sense Resistor	Option Number	Voltage on LED_PAT pin[V]	Resistor Divider Values (Input voltage: LDO18)		LED #/Color	Operational Status			
			R_{TOP} [R27]	R_{BOTTOM} [R31]		Standby	Transfer	Complete	Fault
20 mΩ	1	Pull down <0.037 V	NP	47 kΩ,1%	LED1-Green	Off	On	Off	Off
					LED2-Red	Off	Off	Off	Blink 4 Hz
20 mΩ	2	0.11 V	715 kΩ,1%	47 kΩ,1%	LED1-Green	On	Off	Off	Off
					LED2-Red	On	Off	Off	Blink 4 Hz
20 mΩ	3	0.18 V	422 kΩ,1%	47 kΩ,1%	LED1-Green	Off	Blink 1 Hz	On	Blink 4Hz
					LED2-Red	-	-	-	-
20 mΩ	4	0.26 V	280 kΩ,1%	47 kΩ,1%	LED1-Green	Off	On	Off	Blink 4 Hz
					LED2-Red	-	-	-	-
20 mΩ	5	0.33 V	210 kΩ,1%	47 kΩ,1%	LED1-Green	On	Blink 1Hz	On	Off
					LED2-Red	On	Off	Off	Blink 4 Hz
20 mΩ	6	0.41 V	160 kΩ,1%	47 kΩ,1%	LED1-Green	Off	Off	On	Off
					LED2-Red	Off	On	Off	Blink 4 Hz
50 mΩ	7	0.63 V	86.6 kΩ,1%	47 kΩ,1%	LED1-Green	Off	On	Off	Off
					LED2-Red	Off	Off	Off	Blink 4 Hz
50 mΩ	8	0.71 V	71.5 kΩ,1%	47 kΩ,1%	LED1-Green	On	Off	Off	Off
					LED2-Red	On	Off	Off	Blink 4 Hz
50 mΩ	9	0.78 V	61. kΩ,1%	47 kΩ,1%	LED1-Green	Off	Blink 1 Hz	On	Blink 4 Hz
					LED2-Red	-	-	-	-
50 mΩ	10	0.86 V	51.1 kΩ,1%	47 kΩ,1%	LED1-Green	Off	On	Off	Blink 4 Hz
					LED2-Red	-	-	-	-
50 mΩ	11	0.93 V	44.2 kΩ,1%	47 kΩ,1%	LED1-Green	On	Blink 1Hz	On	Off
					LED2-Red	On	Off	Off	Blink 4 Hz
50 mΩ	12	1.01 V	36.5 kΩ,1%	47 kΩ,1%	LED1-Green	Off	Off	On	Off
					LED2-Red	Off	On	Off	Blink 4 Hz

Input Over Current Protection

Input over current protection protects the transmitter half-bridge and receiver from exposure to conditions that may cause damage or unexpected behavior from the system. While the P9235A-R is in the power transfer stage, it monitors the input current, through the voltage across the input current sense resistor. If the input current goes above the programmed threshold, the P9235A-R will shut down for 5 minutes, and then re-try through digital pings. If the receiver condition remains the same for 5 more minutes, the P9235A-R will continue the periodic analog pings only (no digital pings). If the receiver is removed, or the input power is cycled, the P9235A-R will restart digital pings immediately.

The ILIM pin voltage selects the input current limit through a voltage divider connected to LDO18. Table 9 shows options for 1, 2, and 3W systems, given minimum expected efficiencies. The default value input current limit is 1.25A. The default value occurs when ILIM pin is connected to GND via a 47 kΩ resistor.

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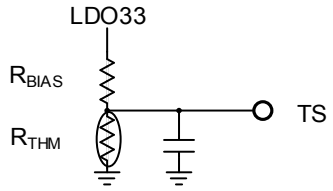
Table 9. ILIM programmable thresholds

Max Power	Vout /Max Iout	Input current Limit threshold	Voltage on ILIM pin	Resistor Divider Values (Input voltage: LDO18)	
				R_{TOP} [R26]	R_{BOTTOM} [R30]
1W	5 V/200 mA	0.75 A	0.48 V	130 kΩ,1%	47 kΩ,1%
2W	5 V/400 mA	1.25 A	0.78 V	NP	47 kΩ,1%
3W	5 V/600 mA	2.0 A	1.23 V	22 kΩ,1%	47 kΩ,1%

Remote Temperature Sensing and Over Temperature Protection

The P9235A-R uses a NTC thermistor connected to the TS pin to monitor the remote temperature during the power transfer phase. Connect the NTC thermistor to a voltage divider as shown in Figure 15. If the voltage on the TS pin decreases below 0.6 V, the transmitter shuts off the power, and will resume the wireless power transfer once the TS pin voltage rises above 0.8 V.

Figure 12. NTC connection



$$V_{TS} = \frac{LDO33 \times R_{THM,TRIP}}{(R_{THM,TRIP} + R_{BIAS})} = 600mV$$

Where:

- V_{TS} (V) = Trip voltage at the desired trip temperature
- $R_{THM,TRIP}$ (kΩ) = Resistance of the thermistor at the desired trip temperature

Given LDO33 = 3.3V and R_{BIAS}=10kΩ, then $R_{THM,TRIP}$ = 2.22 kΩ at the trip temperature

The basic characteristic of an NTC thermistor is:

$$R = R_0 \exp\left\{B \times \left(\frac{1}{T} - \frac{1}{T_0}\right)\right\}$$

Where:

- T (Kelvin) = The trip temperature.
- R_0 (kΩ) = The known resistance at calibration temperature T_0 (Kelvin).
- B (beta, Kelvin) = The material constant .

With R_{BIAS}=10kΩ, R_{THM} =2.2kΩ, and V_{TS}=600mV at a trip temperature T, the desired R_0 and B can be calculated, and the appropriate thermistor chosen.

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Buzzer Function

The BUZ pin is able to drive a piezoelectric type transducer without amplification. As shown on the reference schematic, a series current limiting resistor (R20) must be included if a buzzer is used. The buzzer signal is a 2 kHz square wave. It is recommended to use a buzzer with a 2 kHz resonant frequency for best results.

End of Power Transfer Response

The P9235A-R will shut down and stop the power transfer once it receives an End of Power Transfer (EPT) packet. The P9235A-R will behave differently based on the reason for the EPT request. Table 10 shows the different EPT behaviors.

Table 10. End of Power Transfer Response

EPT Reason	P9235A-R Behavior
End of Power Transfer: Over-Current	The P9235A-R will shut down the system, keeping the analog ping and digital ping. If the over-current condition is not removed, the system will enter into a hiccup mode. In hiccup mode the following sequence is repeated while the over current condition exists: the system starts up and applies the receiver voltage to the load, the receiver detects an over current condition and reports it to the transmitter, the transmitter shuts down.
End of Power Transfer: Over-Temperature	The P9235A-R will shut down the system, keeping the analog ping but muting the digital ping for 5 minutes. If the P9027LP-R is removed within 5 minutes, the P9235A-R will restart the digital ping. After 5 minutes, the P9235A-R will send out one digital ping to check if the fault condition has been removed.
End of Power Transfer: Charge Complete.	The P9235A-R will shut down the system, keeping the analog ping but muting the digital ping for 5 minutes. If the P9027LP-R is removed within 5 minutes, the P9235A-R will restart the digital ping. After 5 minutes, the P9235A-R will send out one digital ping to check if the battery needs to start charging again.
End of Power Transfer: Internal Fault	The P9235A-R will shut down the system, keeping the analog ping and digital ping.

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Transmitter Resonant Tank Capacitors

For optimum performance, and to keep the characteristics of the resonant tank constant, the resonant frequency and quality factor must not change due to variations in the associated capacitors or inductors. The capacitors of the resonant tank (C15, C17, C23, C25) must be COG/NPO type only. COG/NPO capacitors have no temperature variation, less voltage related de-rating, and better accuracy than other types of capacitors such at the X7R. Do not mix capacitor types when populating the resonant capacitors, use COG/NPO types only. All the resonant capacitors must be rated for 50V. See the Bill of Materials for the recommended values.

Transmitter Resonant Tank Coils

Each half-bridge output connects to a series-resonance LC tank. The inductor serves as the primary coil of a loosely-coupled transformer; the secondary is the receiver coil connected to the P9027LP-R.

The transmitter coils are mounted on a ferrite base acting as a shield to concentrate the field on the top side of the coil and to reduce EMI. The coil assembly can be mounted next to the P9235A-R PCB or on the back of PCB. Either a ground plane or grounded metal shielding (preferably copper) can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the ground plane by a single trace leading back independently to the board input power connector.

For optimum performance, the following coils are recommended for use with the P9235A-R transmitter for 1, 2 and 3 W applications. The recommended coil vendors have been tested and verified to guarantee their performance.

Table 11. Coils Recommended with receiver for 1, 2 and 3 W Applications

Output Power	Vendor	Part number	Inductance	DCR	Dimension
1W	TDK	WT151512-22F2-ID	6.49 uH	0.17 Ω	Ø15 mm
	SunLord	SWA15T15H20C01B	6.30 uH	0.12 Ω	Ø15 mm
2W	TDK	WT202012-15F2-ID	6.20 uH	0.10 Ω	Ø20 mm
	Wurth Electronics	760308101104	6.30 uH	0.11 Ω	Ø20 mm
	SunLord	SWA20N20H20C01B	6.30 uH	0.15 Ω	Ø20 mm
3W	TDK	WT303012-13F2-ID	6.30 uH	0.12 Ω	Ø30 mm
	Wurth Electronics	760308101103	6.50 uH	0.15 Ω	Ø30 mm
	SunLord	SWA30N30H20C01B	6.25 uH	0.14 Ω	Ø30 mm

PCB Layout Considerations

Layout and PCB design have a significant influence on the system performance. The power dissipation capabilities of the P9235A-R surface mount packaged power management IC rely heavily on thermally conductive traces and pads to transfer heat away from the package. The regulator or full bridge inverter could show instability, as well as cause EMI problems, if the PCB layout is not designed properly. The following general guidelines will be helpful in designing a board layout for low noise and EMI, as well as, the lowest thermal resistance:

1. PC board traces with large cross-sectional areas remove more heat. For optimal results, use large-area PCB patterns with wide copper traces, placed on the component side of the PCB.
2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
3. Thermal vias provide a thermal path from the bridge FETs to inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

For more details, please refer to the application note AN936, “P9235A-R Layout Guidelines” for the layout details.

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Power Dissipation and Thermal Requirements

The P9235A-R is offered in a QFN-40 package which has a maximum power dissipation capability of approximately 1.2W. The number of thermal vias between the package and the printed circuit board determines the maximum power dissipation. The maximum power dissipation of the package is limited by the die's specified maximum operating junction temperature, $T_{J(MAX),}$ of 125℃, the maximum ambient operating temperature, T_A, of 85℃,and the package thermal resistance, Θ_{JA}. The junction temperature rises when the heat generated by the device's power dissipation flows through the package thermal resistance. The QFN package offers a typical thermal resistance, junction to ambient (Θ_{JA}), of 28.5°C/W when the PCB layout guideline and surrounding devices are optimized.

The techniques as noted in the PCB layout section must be followed when designing the printed circuit board layout. Attention to the placement of the P9235A-R IC and bridge FET packages, in proximity to other heat-generating devices in a given application design, should also be considered. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing Θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size (QFN) and thermal vias, and final system hardware construction. Board designers should keep in mind that the package thermal metric Θ_{JA} is impacted by the characteristics of the PCB itself upon which the IC is mounted. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

The use of integrated circuits in low-profile and fine-pitch surface-mount packages requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks, convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

In summary, the three basic approaches for enhancing thermal performance are:

1. Improve the power dissipation capability of the PCB design
2. Improve the thermal coupling of the component to the PCB
3. Introduce airflow into the system

First, the maximum power dissipation for a given situation should be calculated:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

In which

- $P_{D(MAX)}$ = Maximum Power Dissipation
- θ_{JA} = Package Thermal Resistance (°C/W)
- $T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)
- T_A = Ambient Temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9235A-R device is 120°C. The thermal resistance of the 40-pin QFN package is optimally θ_{JA}=28.5°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$P_{D(Max)} = (120°C - 85°C) / 28.5°C/W \cong 1.2$ Watt.

Thermal Protection

To allow the maximum load current, and to prevent thermal overload, he heat generated by the P9235A-R solution must be dissipated into the PCB. All the available pins must be soldered to the PCB. GND pins (exposed paddle, EP) and bridge FET GND pins should be soldered to the PCB ground plane to improve thermal performance, with multiple vias connected to all layers of the PCB.

Special Notes

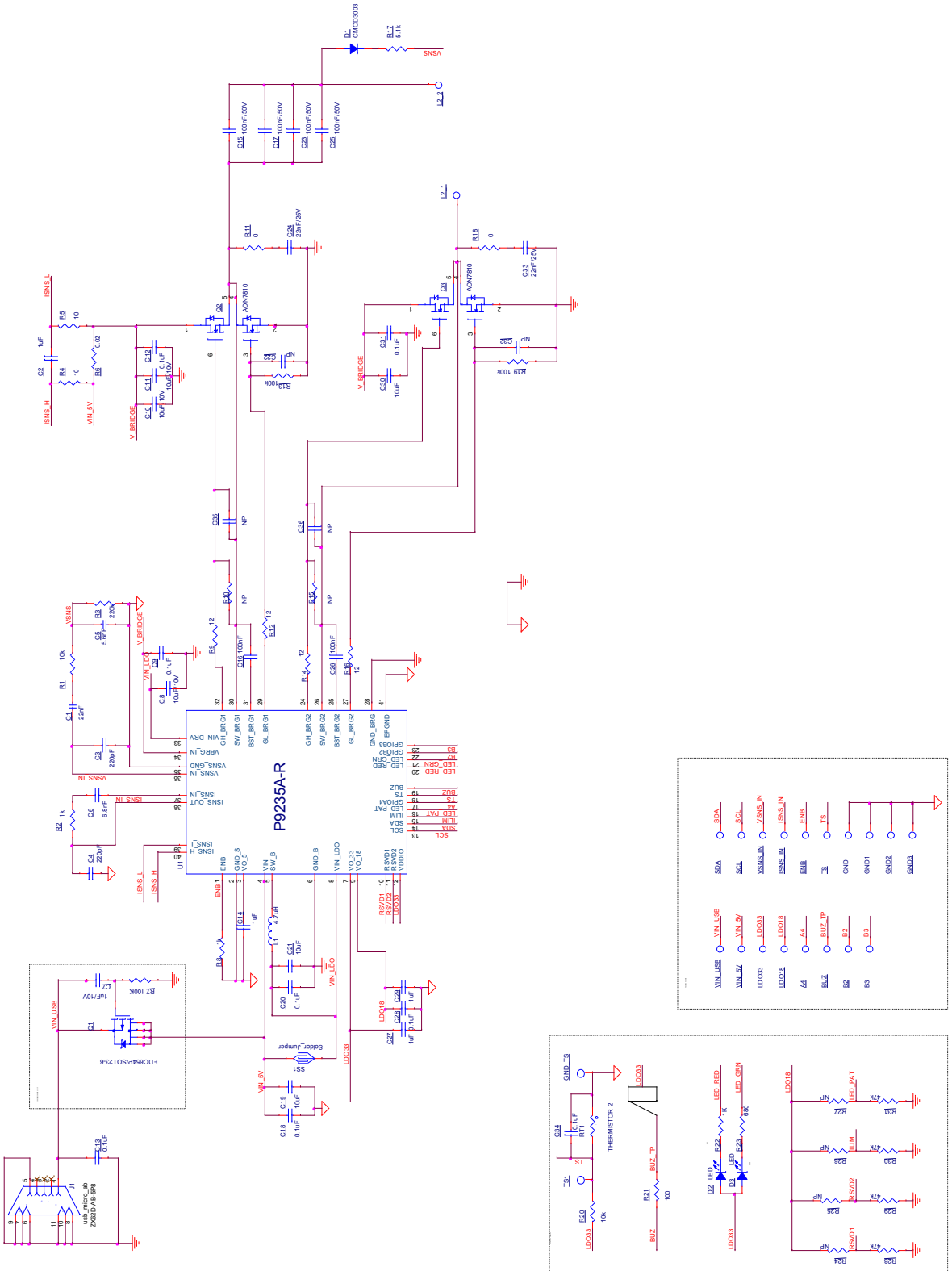
NDG QFN-40 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one-year shelf life.
Note 2: The HIC indicator card for newly-opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours prior to the assembly reflow process.

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Detailed System Diagram

Table 12. P9235A-R Schematic



Components Selection

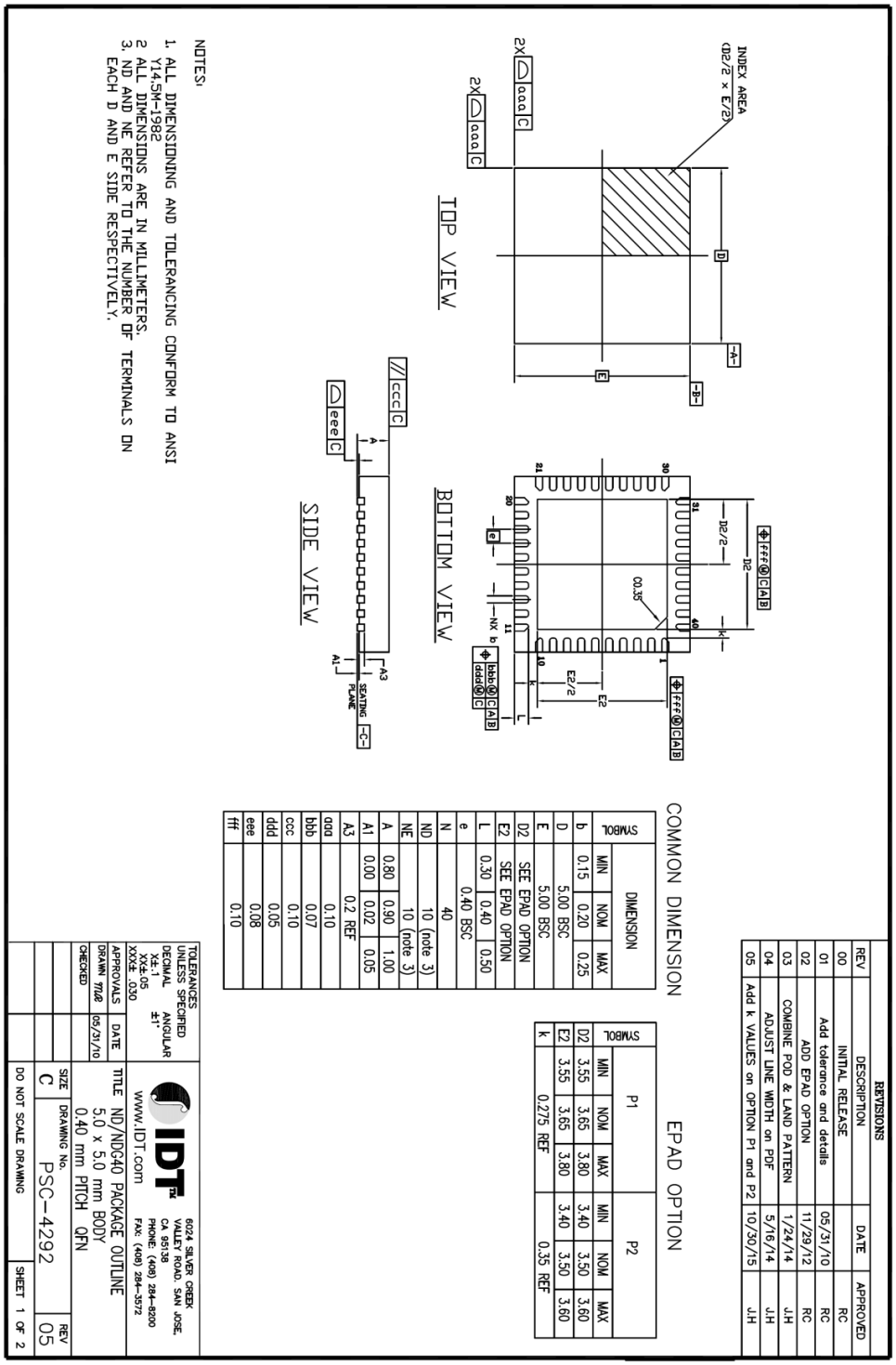
Table 13. Component List

Item	Qty	Reference	Description	PCB Footprint	MFG Part Number
1	3	C1,C24,C33	22 nF/50 V	0402	C0402C223K5RACTU
2	1	C2	1 uF/10 V	0402	C0402C105M8PACTU
3	2	C3,C4	220 pF/50 V	0402	CL05B221KB5NNNC
4	1	C5	5.6 nF/50 V	0402	CL05B562KB5NNNC
5	1	C6	6.8 nF/50 V	0402	CL05B682JB5NNNC
6	5	C9,C12,C13,C18,C31	0.1 uF/25 V	0402	TMK105BJ104KV-F
7	1	C8	10 uF/10 V	0402	CL05A106MP5NUNC
8	5	C10,C11,C19,C21,C30	10 uF/25 V	0603	CL10A106MA8NRNC
9	4	C7,C14,C27,C29	1 uF/10 V	0402	CL05A105KP5NNNC
10	4	C15,C17,C23,C25	100 nF/50 V	1206	C3216C0G1H104J160AA
11	2	C16,C26	100 nF	0402	C1005X6S1V104K050BB
12	3	C20,C34,C28	0.1 uF/10 V	0402	C0402C104K8RACTU
13	4	C22,C32,C35,C36	NP	0402	
14	1	D1	DIODE	SOD523PD	CMOD3003
15	1	D2	Red LED	0603	150 060 RS7 500 0
16	1	D3	Green LED	060	150 060 GS7 500 0
17	1	J1	5 P	usb_micro_ab	10104111-0001LF
18	1	L1	4.7 uH	0603	CIG10W4R7MNC
19	1	L2	Transmitter coil		7650308101104
20	1	Q1	80 mOhm/4.5 V	SOT23-6	FDC654P
21	2	Q2,Q3	N-Channel MOSFETs	DFN 3 mm X 3 mm	AON7810
22	1	R1	10 K/%1	402	RCG040210K0FKED
23	3	R2,R8,R22	1 k	0402	RC0402FR-071KL
24	1	R3	220 k	0402	RC0402FR-07220KL
25	2	R4,R5	10	0402	RT0402DRE0710RL
26	1	R6	0.02	0603	WSL0805R0200FEA
27	3	R7,R13,R19	100 k	0402	ERJ-2GEJ104X
28	4	R9,R12,R14,R16	12	0402	ERJ-2GEJ120X
29	6	R10,R15,R24.R25,R26,R27	NP	0402	
30	2	R11,R18	0 OHMS RESISTOR	0402	RC0402JR-070RL
31	1	R17	5.1 k	0402	MCR01MRTJ512
32	1	R20	10 k	0402	CRCW040210K0JNED
33	1	R21	100	0402	RC0402JR-07100RL
34	1	R23	680	0402	RC0402JR-07680RL
35	4	R28,R29,R30,R31	47 k	0402	ERJ-2GEJ473X
36	1	RT1	THERMISTOR	0603	ERT-J1VG103FA
37	1	U1	IDTP9235	QFN_5 x 5 mm	P9235A-R

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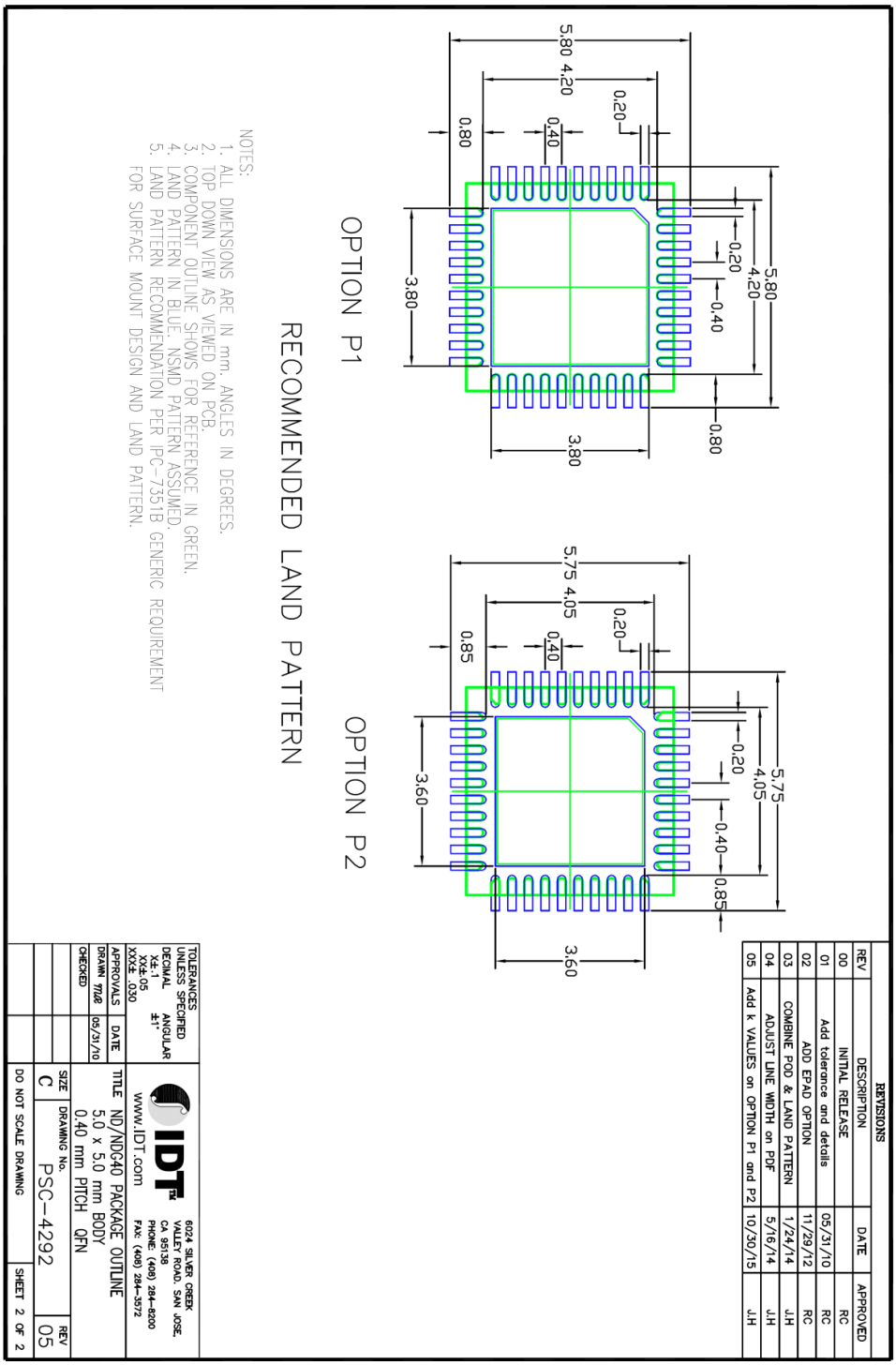
Package Drawing

Figure 13. QFN-40 NDG40 Package Outline Drawing



Landing Pattern Drawing

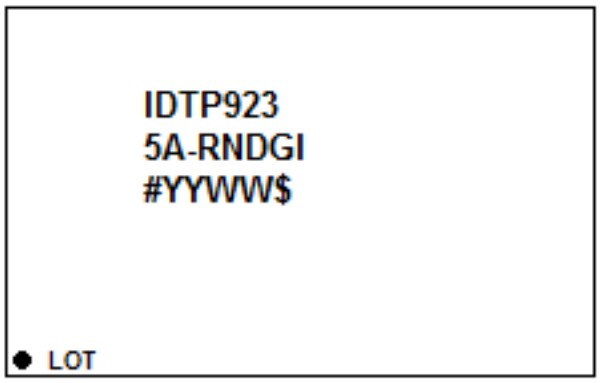
Figure 14. QFN-40 NDG40 Landing Pattern Drawing



Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
P9235A-RNDGI	NDG40 - QFN-40 5x5x0.40	3	Tray	-40° to +85°C
P9235A-RNDGI8	NDG40 - QFN-40 5x5x0.40	3	Tape and Reel	-40° to +85°C

Marking Diagram



1. “IDT” Company code, “P9235A-R” Part number.
2. “NDG” Package type: QFN, “I” Industrial
3. “#” Device stepping, “YY” Last 2 digits of the year, “WW” Work week that the part was assembled, “$” Assembly location code

Revision History

[Insert the revision history entries in reverse chronological order.]

Revision Date	Description of Change
May 16, 2016	Final
May 2, 2016	This is the first preliminary release of this datasheet..