Description

The P9242-R is a highly integrated, magnetic induction, wireless power transmitter supporting up to 15W. The system-on-chip operates with an input voltage range of 4.25V to 21V.

The transmitter includes an industry-leading 32-bit ARM® Cortex®-M0 processor offering a high level of programmability while consuming extremely low standby power. The P9242-R features two LED outputs with pre-defined user-programmable blinking patterns, buzzer, and programmable over-current protection supporting a wide range of applications. The I2C serial communication allows the user to read information such as voltage, current, frequency, and fault conditions. The P9242-R includes an under-voltage lockout and thermal management circuit to safe guard the device under fault conditions. Together with the P9221-R receiver (R_X), the P9242-R is a complete wireless power system solution.

The P9242-R is available in a lead-free, space-saving 48-VFQFN package. The product is rated for a -40ºC to +85ºC operating temperature range.

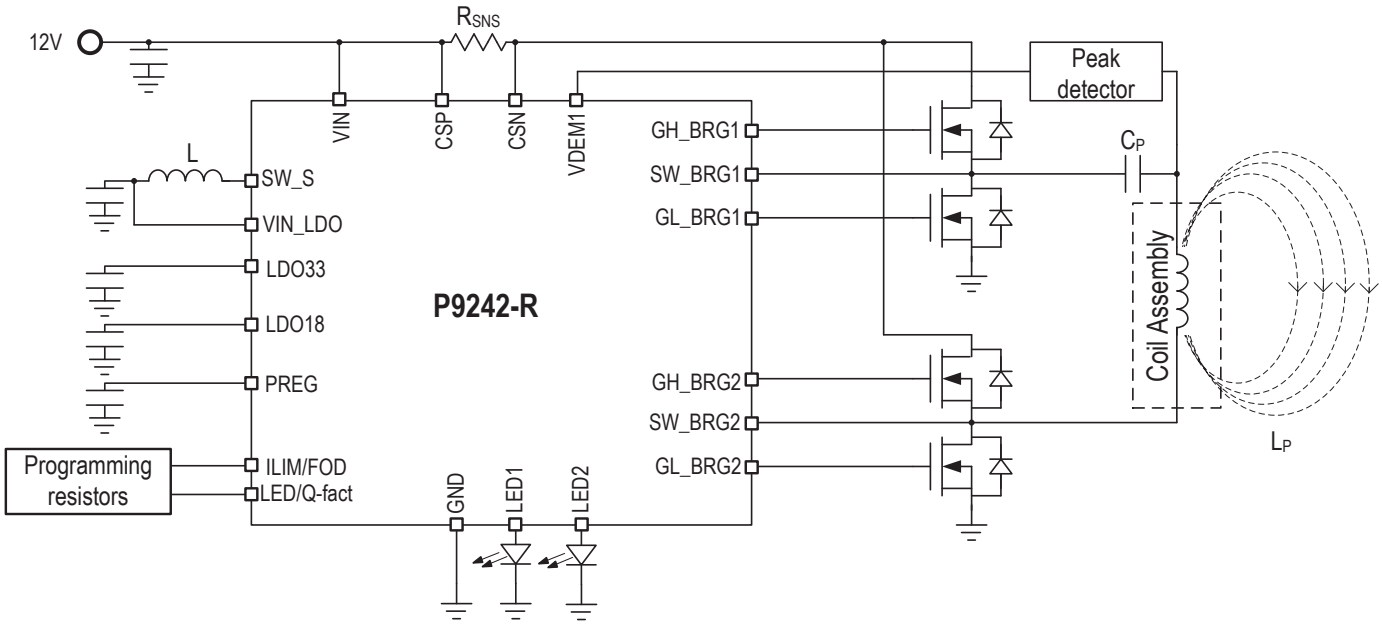
Typical Applications

- Charging pad
- Accessories
- Cradle
- Tablets

Features

- Power transfer up to 15W
- Wide input voltage range: 4.25V to 21V
- WPC-1.2 compliant, MP-A2 coil configuration
- Integrated step-down switching regulator
- Embedded 32-bit ARM® Cortex®-M0 processor
- Integrated drivers for external power FETs
- Simultaneous voltage and current demodulation scheme for communication
- Integrated current sense amplifier
- Low standby power
- Dedicated remote temperature sensing
- Programmable current limit
- Power transfer LED indicator
- User programmable foreign objects detection (FOD)
- Pre-defined user-programmable LED pattern
- Active-LOW enable pin for electrical on/off
- Over-current and over-temperature protection
- Supports I2C interface
- -40 to +85°C ambient operating temperature range
- 48-VFQFN (6 × 6 mm) RoHS-compliant package

Basic Application Circuit



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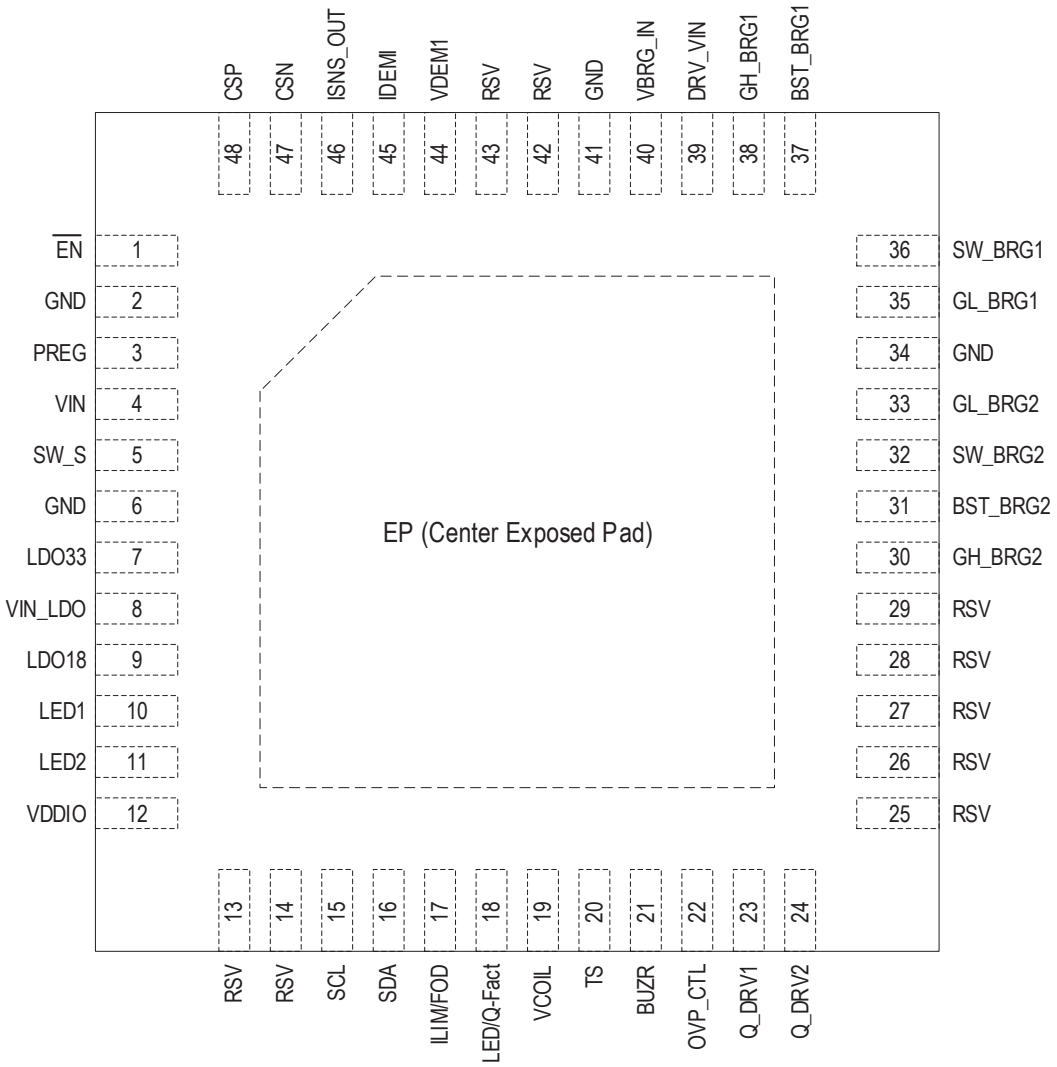
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1. Pin Assignments

Figure 1. Pin Assignments



2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
1	$\overline{EN}$	Input	Active-LOW enable pin. When connected to logic HIGH, the P9242-R enters the Shut Down Mode, which has a typical current consumption of 25µA. When connected to logic LOW, the device is in normal operation.
2, 6, 34, 41, EP	GND	–	Ground connection.
3	PREG	Output	Regulated 5V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin must not be externally loaded.
4	VIN	Input	Input power supply. Connect a 10µF capacitor from this pin to ground.
5	SW_S	Output	Step-down regulator`s switch node. Connect one of the terminals of the 4.7µH inductor to this pin.
7	LDO33	Output	Regulated 3.3V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
8	VIN_LDO	Input	Linear regulator input power supply. Connected this pin to the 5V output of the step-down regulator.
9	LDO18	Output	Regulated 1.8V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
10	LED1	Input	Open-drain output. Connect an LED to this pin
11	LED2		Open-drain output. Connect an LED to this pin.
12	VDDIO	Input	Input power supply for internal biasing. This pin must be connected to LDO33.
15	SCL	Input	I2C interface clock input. Connect a 5.1kΩ pull-up resistor to LDO33 rail.
16	SDA	I/O	I2C interface data input and data output, connect a 5.1kΩ pull-up resistor to LDO33 rail.
17	ILIM/FOD	Input	Programmable over-current limit and foreign object detection pin. Connect the center tap of the resistor divider to this pin to set the current-limit threshold and FOD threshold. For more information on setting the current limit and FOD, see section 7.2.
18	LED/Q-Fact	Input	Programmable LED pattern selection and Q-factor enable/disable. Connect the center tap of a resistor divider to this pin. For more information on setting the LED pattern and Q-factor enable/disable, see section 7.9.
19	VCOIL	Input	Input for coil voltage sensing.
20	TS	Input	Remote temperature sensor for over-temperature shutdown. Connect to the NTC thermistor network. If not used, connect to the LDO33 pin through the 10kΩ resistor.
21	BUZR	Output	Buzzer output. Connect a buzzer to this pin.
22	OVP_CTL	I/O	Logic HIGH during power transfer phase used to scale down the voltage to detect over-voltage for VCOIL pin.
23	Q_DRV1	I/O	Control signal for Q factor measurement circuit.
24	Q_DRV2	I/O	Control signal for Q factor measurement circuit.
13, 14, 25, 26, 27, 28, 29, 42, 43	RSV	–	Reserved for internal use. Do not connect.

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Pins	Name	Type	Function
30	GH_BRG2	Output	Gate driver output for the high-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
31	BST_BRG2	Input	Bootstrap pin for half bridge 2. Tie an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage higher than the input voltage.
32	SW_BRG2	Output	Switch node for half bridge 2.
33	GL_BRG2	Output	Gate driver output for the low-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
35	GL_BRG1	Output	Gate driver output for the low-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
36	SW_BRG1	Output	Switch node for half bridge 1.
37	BST_BRG1	Output	Bootstrap pin for half bridge 1. Tie an external capacitor from this pin to the SW_BRG1 to generate a drive voltage higher than the input voltage.
38	GH_BRG1	Output	Gate driver output for the high-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
39	DRV_VIN	Input	Input power supply for the internal gate drivers. Connect a 10µF capacitor from this pin to ground.
40	VBRG_IN	Input	Bridge voltage input sense.
44	VDEM1	Input	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by power receiver.
45	IDEMI	Input	High-pass filter input. Current demodulation pin for data packets based on coil current variation; transmitted by power receiver.
46	ISNS_OUT	Output	Input current sense output.
47	CSN	Input	Low-side input current sense (VBRIDGE).
48	CSP	Input	High-side input current sense (VIN).

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3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond those listed under "Absolute Maximum Ratings" might cause permanent damage to the P9242-R. Functional operation of the P9242-R at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods could affect long-term reliability.

Table 2. Absolute Maximum Ratings

Pins [a]	Rating [b]	Units
$\overline{EN}$, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, SCL, SDA, ILIM/FOD, LED/Q-Fact, VCOIL, TS, BUZR, OVP_CTL, Q_DRV1, Q_DRV2, GL_BRG1, GL_BRG2, VDEM1, IDEMI, ISNS_OUT, DRV_VIN	-0.3 to 6	V
LDO18	-0.3 to 2	V

[a] Absolute maximum ratings are not provided for reserved pins (RSV). These pins are not used in the application.

[b] All voltages are referred to ground unless otherwise noted. All GND pins and the exposed pad (EP) connected together.

Table 3. Package Thermal Information

Symbol	Description	VFQFN Rating	Units
θ_{JA}	Thermal Resistance Junction to Ambient [a], [b], [c]	27.2	°C/W
θ_{JC}	Thermal Resistance Junction to Case [b], [c]	18.8	°C/W
θ_{JB}	Thermal Resistance Junction to Board [b], [c]	1.36	°C/W
T_J	Operating Junction Temperature [a], [b]	-40 to +125	°C
T_A	Ambient Operating Temperature [a], [b]	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51-standard 4-layer board with the dimensions 76.2 x 114.3 mm in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins	±2000	V
CDM	All pins	±500	V

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4. Electrical Characteristics

Table 5. Electrical Characteristics

Note: V_{IN} = 5V, $\overline{EN}$ = LOW, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies and UVLO						
V_{IN}	Input Operating Range[a]		4.25		21	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} rising		4.0		V
V_{IN_UVHYS}	Under-Voltage Hysteresis	V_{IN} falling		0.5		V
I_{IN}	Operating Mode Input Current	Power transfer phase, Vin = 12V		10		mA
I_{STD_BY}	Standby Mode Current	Periodic ping		1		mA
I_{SHD}	Shut Down Current	$\overline{EN}$ = V_{IN} = 21V		25	80	µA
Enable Pin Threshold ($\overline{EN}$)						
V_{IH}	Input Threshold HIGH		2.5			V
V_{IL}	Input Threshold LOW				0.5	V
I_{EN_LKG}	$\overline{EN}$ Pin Input Leakage Current	$V_{\overline{EN}}$ = 0V	-1		1	µA
		$V_{\overline{EN}}$ = 5V		2.5		µA
Step-Down Regulator[b] with C_{OUT} = 33µF; L = 4.7µH						
V_{OUT}	Step-Down Output Voltage	Vin = 12V	4.5	5	5.5	V
N-Channel MOSFET Drivers						
$t_{LS_ON_OFF}$	Low-Side Gate Driver Rise and Fall Times	C_{LOAD}= 3nF; 10% to 90%, 90% to 10%		50	150	ns
$t_{HS_ON_OFF}$	High-Side Gate Driver Rise and Fall Times	C_{LOAD} = 3nF; 10% to 90%, 90% to 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier Output Offset Voltage	Measured at the ISNS_OUT pin; V_{CSP} = V_{CSN}		0.6		V
$ISEN_{ACC_TYP}$[c]	Measured Current Sense Accuracy	V_{R_ISEN} = 25mV, I = 1.25A		±3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			10		
$V_{IN,FS}$	Full Scale Input Voltage			2.4		V
LDO18[b]						
V_{LDO18}	1.8V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	1.71	1.8	1.89	V

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Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
LDO33 [b]						
V_{LDO33}	3.3V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	3.15	3.3	3.45	V
PREG						
V_{PREG}	5V LDO Regulator			5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold rising		140		˚C
		Threshold falling		120		˚C
Analog Input Pins Input Current Leakage (TS, VCOIL)						
I_{LKG}	Leakage Current		-1		1	µA
Open-Drain Pins Output Logic Levels (LED1, LED2, SCL, SDA)						
V_{OH}	Output Logic HIGH		4			V
V_{OL}	Output Logic LOW	I = 8mA			0.5	V
Digital Input/Output Pins Logic Levels						
V_{IH}	Input Voltage HIGH Level		0.7∗VDDIO			V
V_{IL}	Input Voltage LOW Level				0.3∗VDDIO	V
I_{LKG}	Leakage Current				1	µA
V_{OH}	Output Logic HIGH	I = 8mA, VDDIO = 3.3V	2.4			V
V_{OL}	Output Logic LOW	I = 8mA, VDDIO = 3.3V			0.5	V
I2C Interface (SCL, SDA)						
f_{SCL_SLV}	Clock Frequency	As I2C slave			400	kHz
C_B	Capacitive Load	For each bus line			100	pF
C_{BIN}	SCL, SDA Input Capacitance			5		pF
I_{LKG}	Input Leakage Current	V = GND and 3.3V	-1		1	µA

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and a 4.7Ω, 1% input filter resistor are required to meet the FOD specification.

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5. Typical Performance Characteristics

V_{IN} = 12.0V; $\overline{EN}$ = LOW. The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at T_A = +25°C unless otherwise noted.

Figure 2. Efficiency vs. Output Load: V_{OUT_RX} = 12V

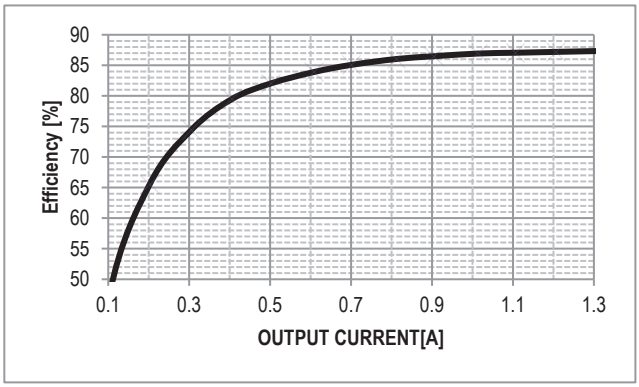


Figure 3. Efficiency vs. Output Load: V_{OUT_RX} = 9V

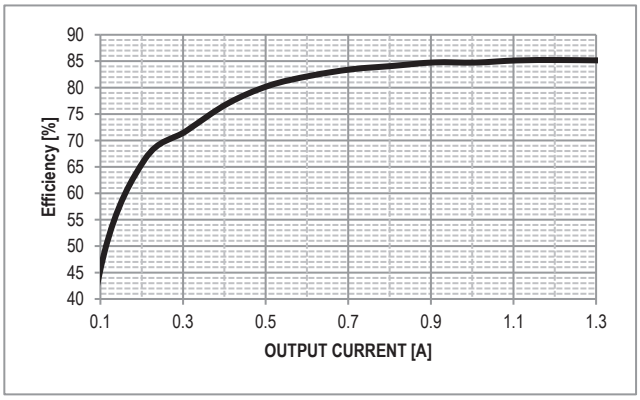


Figure 4. Efficiency vs. Output Load: V_{OUT_RX} = 5V

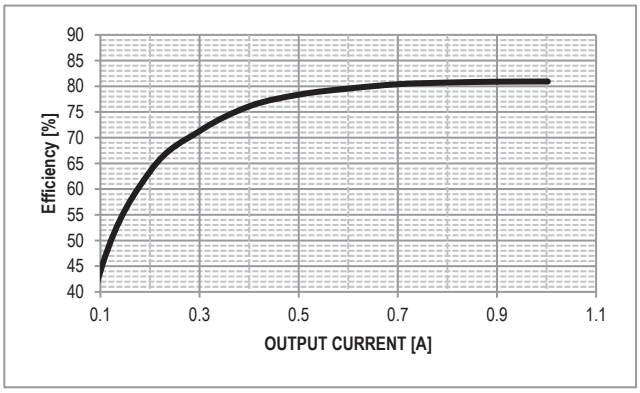


Figure 5. Load Regulation vs. Output Load: VCC_5V in Schematic Figure 25

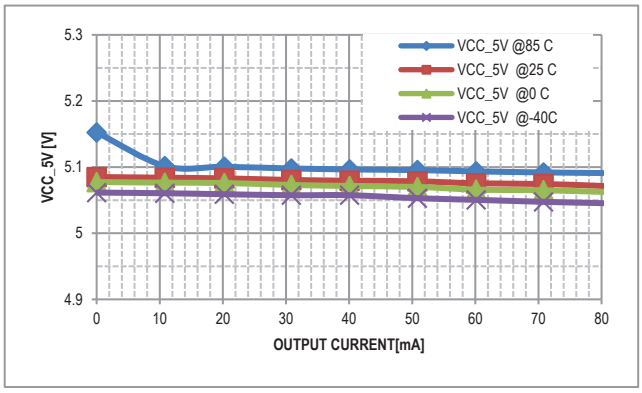


Figure 6. Load Regulation vs. Output Load: LDO33

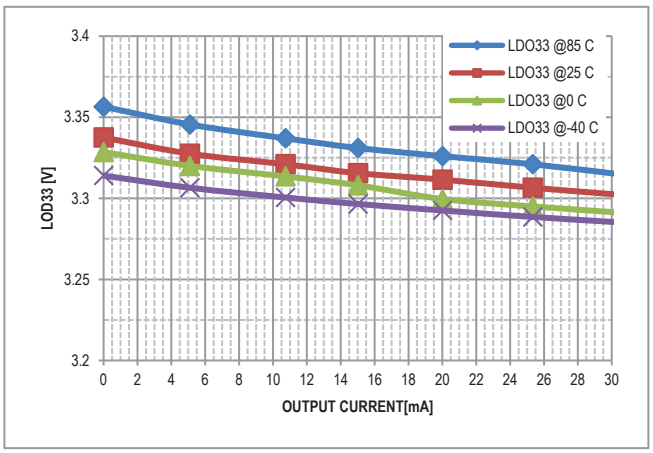
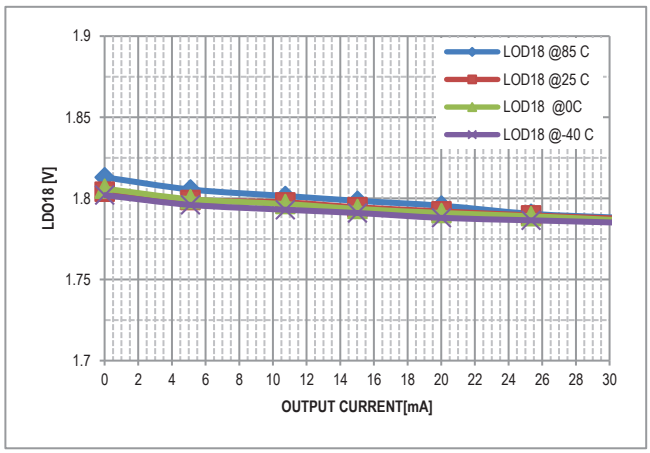


Figure 7. Load Regulation vs. Output Load: LDO18



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Figure 8. Over-Current Limit vs. V_{ILIM}

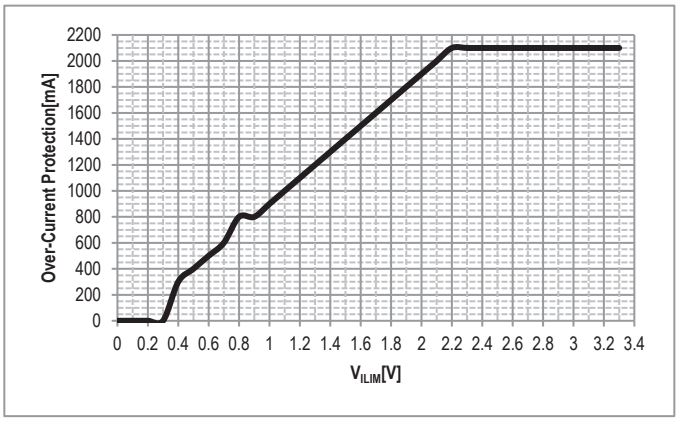


Figure 9. Voltage and Current Signal for Demodulation

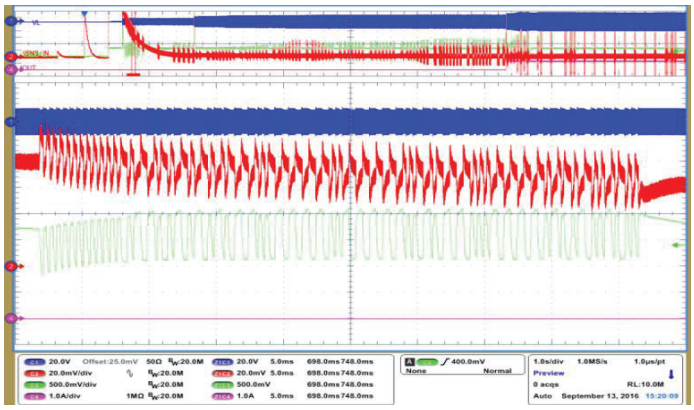


Figure 10. Enable Startup

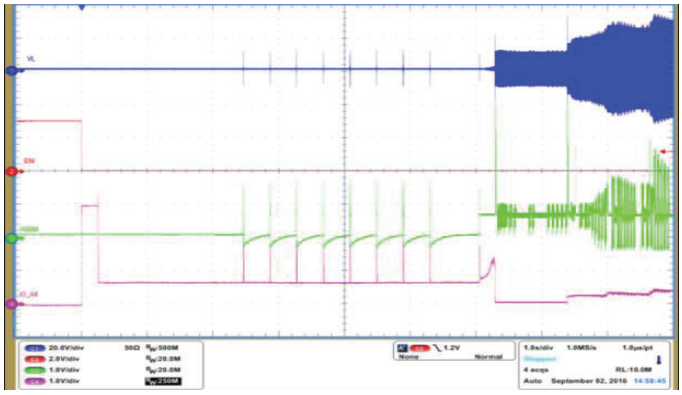


Figure 11. Communication Packet during R_X Load Step from 0 to 1.3A

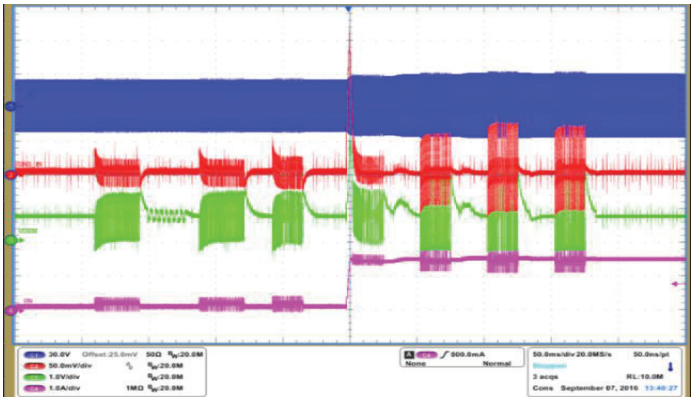
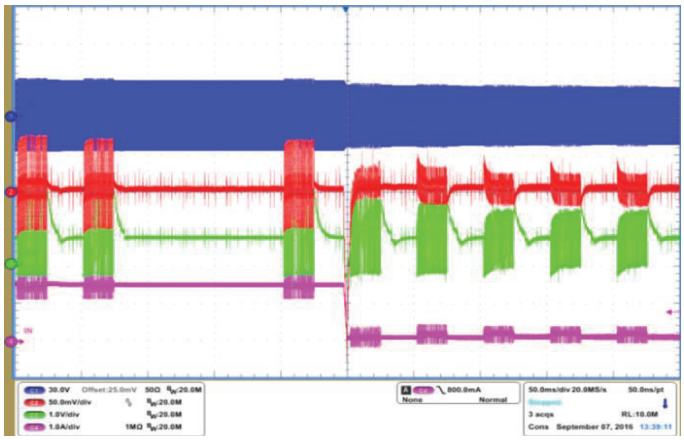
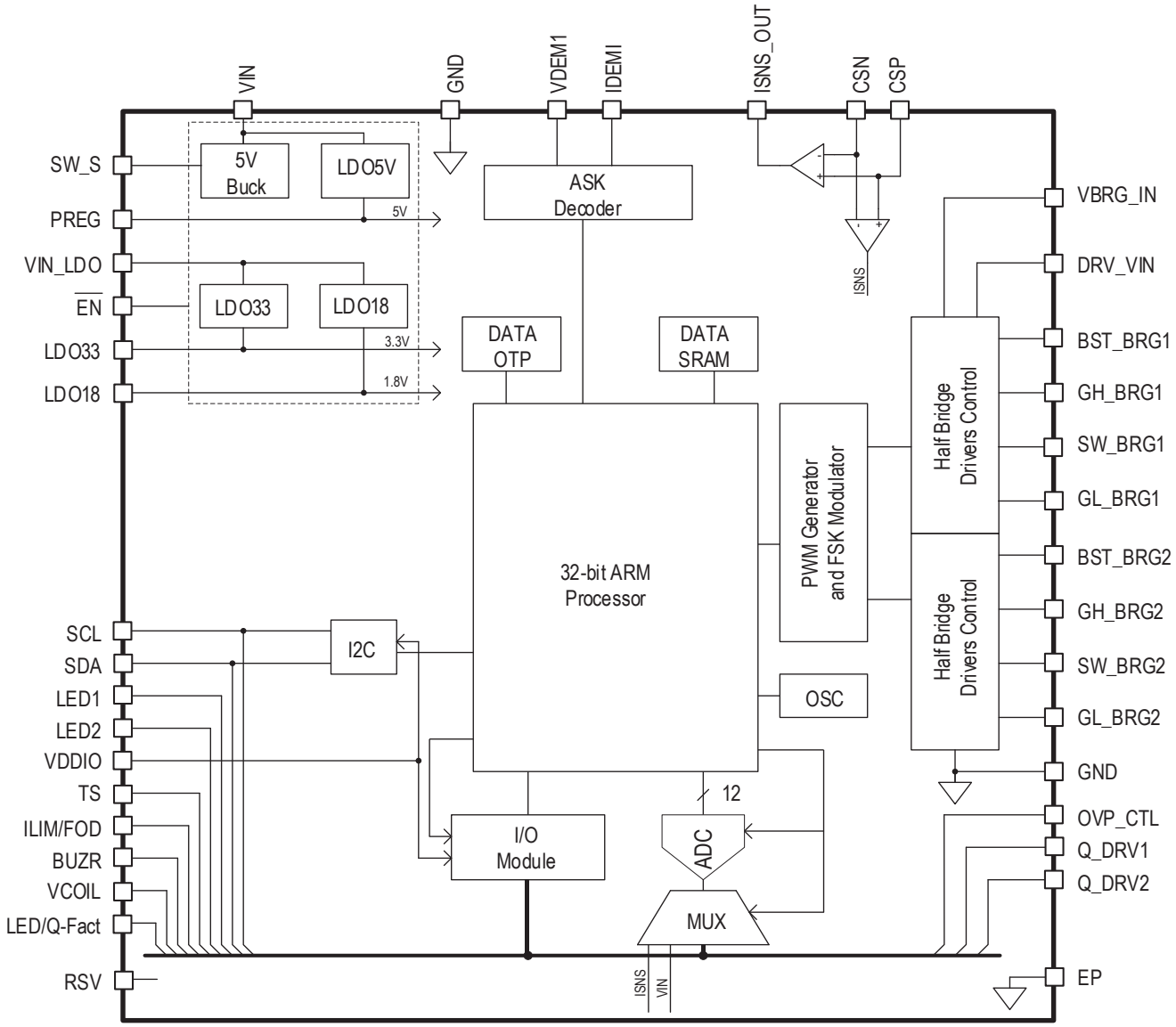


Figure 12. Communication Packet during R_X Load Step from 1.3A to 0



6. Function Block Diagram

Figure 13. Functional Block Diagram



7. Theory of Operation

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. The amount of power transferred to the mobile device is controlled by the wireless power receiver by sending communication packets to the transmitter to increase, decrease, or maintain the power level. The communication from receiver to transmitter is purely digital and consists of 1's and 0's that ride on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. Communication from transmitter to receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency and amplitude shift keying (ASK) is used for the communication protocol from receiver to transmitter.

A feature of the wireless charging system is the fact that when it is not delivering power, the transmitter is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once an Extended Power Profile Receiver is detected, such as the P9221-R or equivalent, the transmitter will provide with up to 15W of output power. If a Baseline Power Profile Receiver is present, the transmitter will deliver only up to 5W of output power.

The P9242-R contains features that ensure a high level of functionality and compliance with the WPC requirements, such as a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

7.1 Foreign Object Detection

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through the object will heat up. The amount of heat generated is a function of the amplitude and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In any wireless power system, the heat generated by the eddy current manifests itself as a power loss reducing the overall system efficiency. If appropriate measures are not taken, the heating could lead to unsafe situations.

In the Extended Power Profile, there are two stages of foreign object detection (FOD). One is by measuring the system quality factor prior to entering the power-transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power-transfer phase. Prior to entering the power-transfer phase, the P9242-R detects a change in the coil's quality factor (the Q-factor) when a wireless power receiver or metal object has been placed on its surface. The transmitter measures the Q-factor and compares it with the reference Q-factor provided by the receiver. If the difference is higher than the reference Q-factor, the P9242-R will identify it as an FOD and shut down the system. See section 7.9 for details for enabling Q-factor detection.

The second stage of the foreign object detection is during the power transfer where the power loss difference between the received power and transmitted power is constantly measured and compared to the WPC-1.2-specified threshold. If the difference is higher than the threshold set by the WPC specification, the system will shut down to avoid over-heating.

See Table 6, Table 7, and Table 8 in section 7.2 for details for configuring the FOD threshold via external resistors.

7.2 Configuring Foreign Object Detection and Over-Current Limit – ILIM/FOD Pin

The over-current protection (OCP) is designed to protect the half-bridge and wireless receiver unit from becoming exposed to operating conditions that could potentially cause damage or unexpected behavior from the system. The input current is continuously monitored during the power transfer stage. If the input current goes above the OCP threshold of 2.5A (typical), the P9242-R will increase the switching frequency or reduce the duty cycle in order to keep the input current below the OCP value.

External resistors can be used to select a different OCP threshold (ILIM). The same resistors are used to set the FOD threshold (refer to section 7.1 for FOD details). See Table 6, Table 7, and Table 8 for the resistor values. See the typical application schematic in Figure 25 for the location of the resistors.

Note: The default current limit setting on the P9242-R-EVK is set to 2.5A. It is highly recommended that the current limit to be set at 2.5A for 15W applications.

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Table 6. External Resistor Values for Setting Current Limiting (ILIM) to 2.5A and FOD Threshold

ILIM[mA]	R48[KΩ]	R40[KΩ]	Tuned FOD Threshold [%]
2500	10	6.98	-40
	10	7.68	-30
	10	8.25	-20
	10	9.09	-10
	10	Open	0
	10	11	10
	10	12.1	20
	10	13.3	30
	10	14.3	40

Table 7. External Resistor Values for Setting Current Limiting (ILIM) to 2.0A and FOD Threshold

ILIM [mA]	R48 [KΩ]	R40 [KΩ]	Tuned FOD Threshold [%]
2000	10	2.55	-40
	10	2.94	-30
	10	3.32	-20
	10	3.74	-10
	10	4.12	0
	10	4.64	10
	10	5.11	20
	10	5.76	30
	10	6.34	40

Table 8. External Resistor Values for Setting Current Limiting (ILIM) to 1.5A and FOD Threshold

ILIM [mA]	R48 [KΩ]	R40 [KΩ]	Tuned FOD Threshold [%]
1500	Open	10	-40
	10	0.232	-30
	10	0.487	-20
	10	0.732	-10
	10	1	0
	10	1.27	10
	10	1.58	20
	10	1.87	30
	10	2.21	40

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7.3 Enable Pin – $\overline{EN}$

The P9242-R can be disabled by applying a logic HIGH to the $\overline{EN}$ pin. When the voltage on the $\overline{EN}$ pin is pulled high, operation is suspended and the P9242-R is placed in the low-current Shut Down Mode. If pulled low, the P9242-R is active.

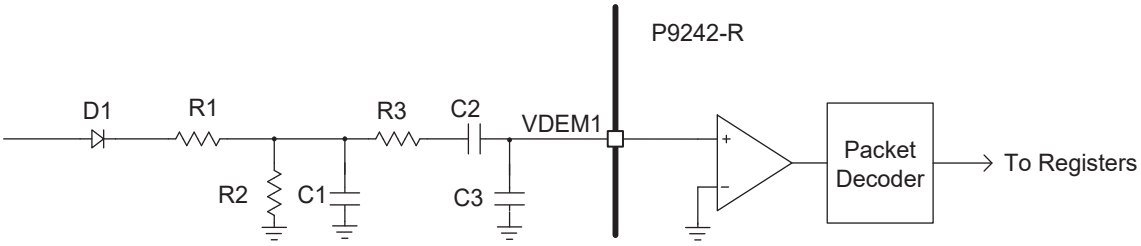
7.4 Buzzer – BUZR Pin

An optional AC-type ceramic buzzer can be connected between the BUZR pin to GND through a current limiting resistor. A short 4kHz “chirp” sound will indicate when the object is detected. Do not connect this pin if the buzzer function is not desired.

7.5 Voltage Demodulation – VDEM1 Pin

In order to increase the communication reliability in any load condition, the P9242-R has integrated two demodulation schemes, one based on coil current information and the other based on coil voltage modulation. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 14. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

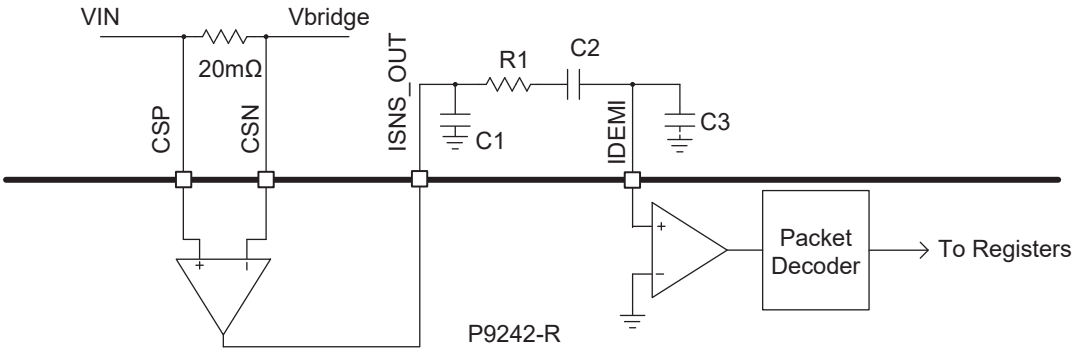
Figure 14. Voltage Mode Envelope Detector



7.6 Current Demodulation – IDEMI

The current-mode detector takes the modulation information from the current sense resistor, which carries the coil current modulation information in addition to the averaged input current. There is an additional discrete low-pass filter and DC filter between the ISNS_OUT and IDEMI pins. The packet decoder block is shared between the voltage-mode and current-mode detectors. The packet decoder selects either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Figure 15. Current Mode Envelope Detector



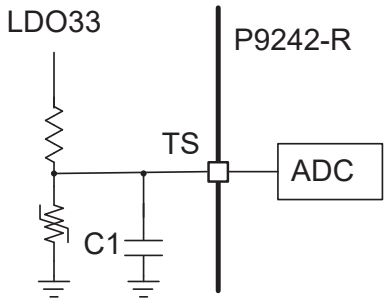
7.7 Thermal Protection

The P9242-R integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the P9242-R if the die temperature exceeds a threshold to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. An internal temperature protection block is enabled in the P9242-R that monitors the temperature inside the chip. If the die temperature exceeds 140°C, the chip shuts down and resumes when the internal temperature drops below 120°C.

7.8 External Temperature Sensing – TS

The P9242-R has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage was chosen to be 0.6V in the P9242-R, and it is used for monitoring the voltage level on the TS pin.

Figure 16. NTC Thermistor Connection to TS Pin



To disable the thermistor, the TS pin should be connected to the LDO33 pin. Do not leave the TS pin floating.

7.9 Q-Factor and LED Pattern Selection – LED/Q-Fact Pin

The P9242-R uses two LEDs to indicate the power transfer status, faults, and operating modes depending on the voltage level at the LED/Q-Fact pin. In addition, this pin enables or disables the Q-factor used for FOD (see section 7.1). The LEDs are connected to the LED1 and LED2 pins as shown in the typical application schematic in Figure 25. The LED pattern can be selected and the Q-factor can be enabled or disabled by the voltage on the LED/Q-Fact pin as determined by the resistor divider R43 and R44 as shown in Figure 25.

Table 9. Resistors for Setting the LED Pattern and Enabling/Disabling the Q-factor Detection for FOD

Q-Factor Detection	Option	LED/Q-Fact Pin Voltage	R43 [kΩ]	R44 [kΩ]	LED1/LED2 Pin	Status			
						Standby	Transfer	Complete	Fault
Enabled	1	Pull-Down	Open	10	LED2	Off	On	Off	Off
					LED1	Off	Off	Off	Blink 4Hz
	2	0.225V	10	0.732	LED2	On	On	Off	Off
					LED1	On	Off	Off	Blink 4Hz
	3	0.375V	10	1.27	LED2	Off	Blink 1Hz	On	Blink 4Hz
					LED1	Off	Off	Off	Off
	4	0.525V	10	1.87	LED2	Off	On	Off	Blink 4Hz
					LED1	Off	Off	Off	Off
	5	0.675V	10	2.55	LED2	On	Blink 1Hz	On	Off
					LED1	On	Off	Off	Blink 4Hz
	6	0.825V	10	3.32	LED2	Off	Off	On	Off
					LED1	Off	On	Off	Blink 4Hz
	7	Pull-Up	10	Open	LED2	Off	Blink 1Hz	On	Off
					LED1	Off	Off	Off	Blink 4Hz
Disabled	1	1.125	10	5.11	LED2	Off	On	Off	Off
					LED1	Off	Off	Off	Blink 4Hz
	2	1.275	10	6.34	LED2	On	On	Off	Off
					LED1	On	Off	Off	Blink 4Hz
	3	1.425	10	7.68	LED2	Off	Blink 1Hz	On	Blink 4Hz
					LED1	Off	Off	Off	Off
	4	1.575	10	9.09	LED2	Off	On	Off	Blink 4Hz
					LED1	Off	Off	Off	Off
	5	1.725	10	11	LED2	On	Blink 1Hz	On	Off
					LED1	On	Off	Off	Blink 4Hz
	6	1.875	10	13	LED2	Off	Off	On	Off
					LED1	Off	On	Off	Blink 4Hz
	7	2.025	10	15.8	LED2	Off	Blink 1Hz	On	Off
					LED1	Off	Off	Off	Blink 4Hz

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7.10 Input Voltage Requirement

The P9242-R can support an input voltage ranging from 4.5V to 21V. However, since the transmitter is compliant with WPC's MP-A2 coil configuration, the input voltage is restricted to 10V to 14V with a nominal voltage of 12V.

7.11 Integrated Step-Down Regulator

The input capacitors (C14 and C15 in Figure 25) must be connected as close as possible between the VIN pin and GND pin. Similarly, the output capacitor (C4 and C5 in Figure 25) must be placed close to the inductor and GND. The output voltage is sensed by the VIN_LDO pin; therefore, the connection from the step-down output (VCC_5V; see Figure 25) to the VIN_LDO pin should be made as wide and short as possible to minimize output voltage errors. The step-down regulator is the input voltage to the LDO18 and LDO33 linear regulators and is not recommended for powering an external load.

7.12 Integrated Linear Regulators – PREG, LDO33, and LDO18

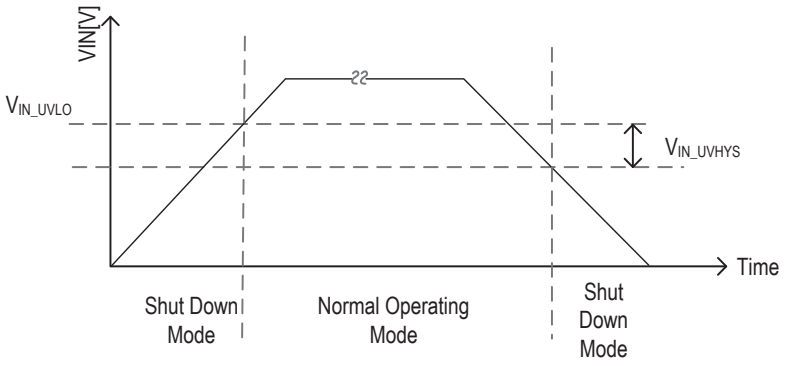
The P9242 has three low-dropout (LDO) regulators used to bias the internal circuitry. The 5V pre-regulator (PREG) provides bias for the entire internal power management. The PREG requires a 1µF ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1µF ceramic capacitor from the pin to GND. The voltage regulators must not be externally loaded.

7.13 Under-Voltage Lock-Out (UVLO) Protection

The P9242-R has 4V (typical, rising) under-voltage lockout circuit on the VIN pin. To guarantee proper functionality, the voltage on the VIN pin must rise above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9242-R is in Shut Down Mode.

Figure 17. UVLO Threshold Definition



7.14 LC Resonant Circuit

The LC resonant circuit comprises the series primary resonant coil (L_P) and series capacitance (C_P). The transmitter coil assembly is vendor specific, and it must comply with the WPC recommendation. The WPC recommendations include the self-inductance value, DC resistance (DCR), Q-factor, size, and number of turns.

The P9242-R is designed for an MP-A2 coil configuration using half-bridge and full-bridge inverter topologies to drive the primary coil (L_P) and a series capacitance (C_P). Within the operating frequency range from 110kHz to 145kHz, the assembly of the primary coil and shielding has a self-inductance of L_P = 10.0µH ±10%, and the value of the series capacitance on the P9242-R-EVK is C_P = 215nF ±5%. Near resonance, the voltage developed across the C_P series capacitance could reach 70V peak. High-voltage (100V) COG-type ceramic capacitors are highly recommended for their AC and DC characteristics and temperature stability. The recommended parts are listed on the bill of materials (BOM) in Table 22.

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8. Wireless Communication Interface

8.1 Modulation/Communication

The WPC-1.2 extended power profile specification uses two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's coil; the communication is purely digital and symbols 1's and 0's carried on the power signal. Modulation is done with amplitude-shift keying (ASK) modulation using with a bit-rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The power transmitter demodulates this variation of the coil current or voltage to receive the packets.

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power transmitter P9242-R has the means to modulate FSK data from the power signal frequency and use it in order to establish the handshaking protocol with the power receiver.

The P9242-R implements FSK communication when used in conjunction with WPC-compliant receivers, such as the P9221-R. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles. Equation 1 should be used to compute the modulated frequency based on any given operating frequency.

Communication packets are transmitted from transmitter to receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation is calculated using Equation 1.

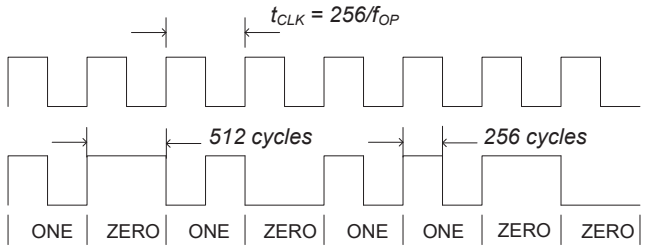
$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \text{ [KHz]}$$

Equation 1

Where f_{MOD} is the change in frequency in the power signal frequency; f_{OP} is the base operating frequency of power transfer; and 60,000kHz is the frequency of the internal oscillator responsible for counting the period of the power transfer signal.

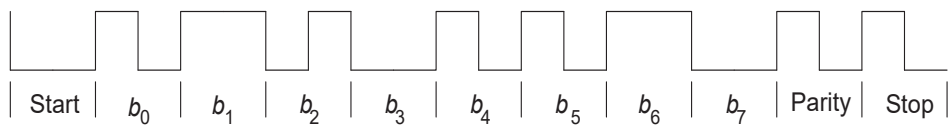
The FSK byte-encoding scheme and packet structure complies with the WPC specification revision 1.2. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit will consist of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 18. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 19:

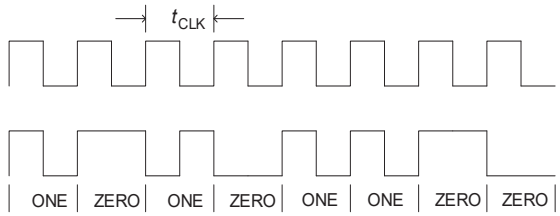
Figure 19. Example of Asynchronous Serial Byte Format for FSK



8.2 Bit Decoding Scheme for ASK

As required by the WPC, the P9242-R uses a differential bi-phase coding scheme to demodulate data bits onto the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is coded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown below:

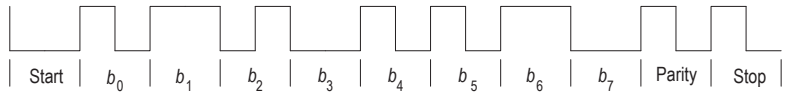
Figure 20. Bit Decoding Scheme



8.3 Byte Decoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 21.

Figure 21. Byte Decoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

8.4 Packet Structure

The P9242-R communicates with the base station via communication packets. Each communication packet has the following structure:

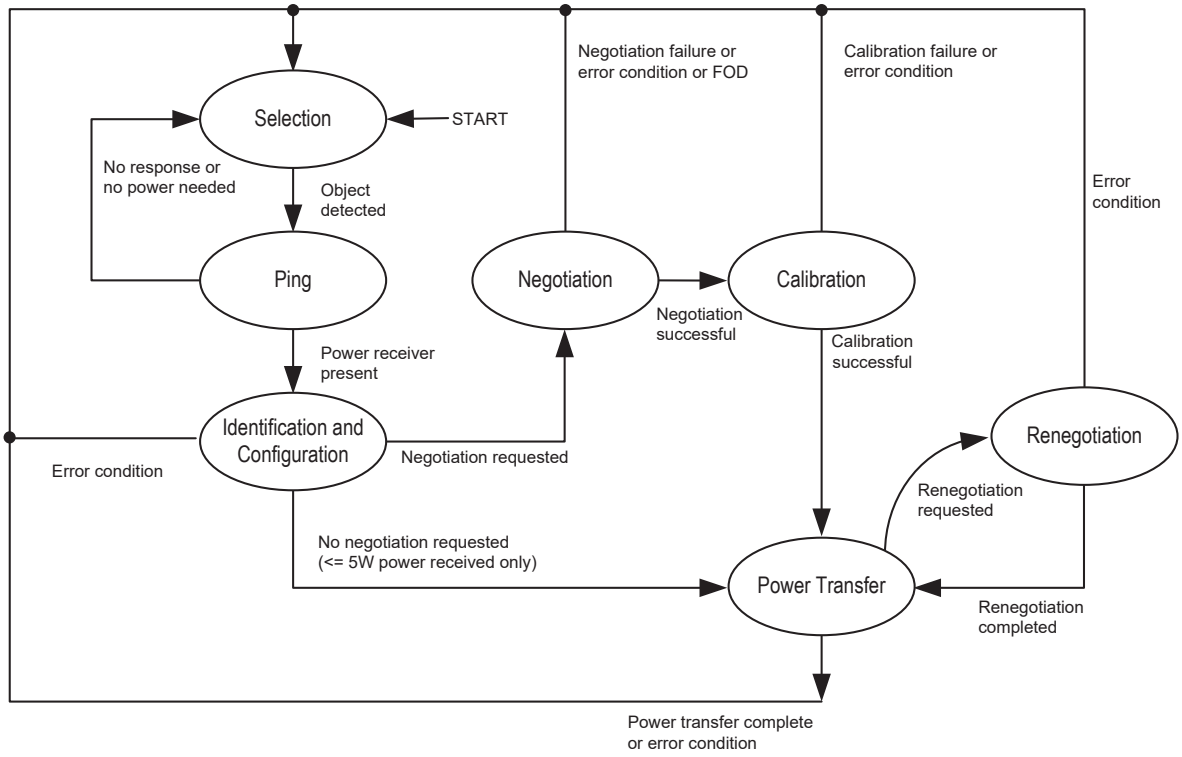
Figure 22. Communication Packet Structure

Preamble	Header	Message	Checksum

9. WPC Mode Characteristics

The WPC-1.2 extended power profile wireless power specification has a negotiation phase, calibration phase, and renegotiation phase, as shown in Figure 23.

Figure 23. WPC Power Transfer Phases Flow Chart



9.1 Selection Phase

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

9.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response ensures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a power receiver is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the internal bias voltage is greater than a specific threshold level, then receiver is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

9.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power transmitter identifies itself and receives information for a default power transfer contract as follows:

- It receives the configuration packet.
- If the *Neg* bit in the received configuration packet is set to ZERO, the power transmitter should proceed to the power transfer phase without sending a response for baseline power profile.
- If the *Neg* bit in the received configuration packet is set to ONE, subsequently the power transmitter should proceed to the negotiation phase for the extended power profile.

9.4 Negotiation Phase

In the negotiation phase, the power receiver negotiates with the power transmitter to fine-tune the power transfer contract. The power receiver sends negotiation requests to the power transmitter, which the power transmitter can grant or deny. In addition, to improve its initial assessment of whether foreign objects are present, the power transmitter can compare the quality factor reported by the power receiver with its own measurement. If the power transmitter detects a foreign object, it should return the selection phase.

9.5 Calibration Phase

In the calibration phase, the power receiver provides information that the power transmitter can use to improve its ability to detect foreign objects during power transfer.

9.6 Power Transfer Phase

In this phase, the P9242-R controls the power transfer by means of the following control data packets:

- Control Error Packets
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer mode. The receiver`s control circuit sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the actual received power packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, when the receiver sends EPT packets, the transmitter terminates the power transfer.

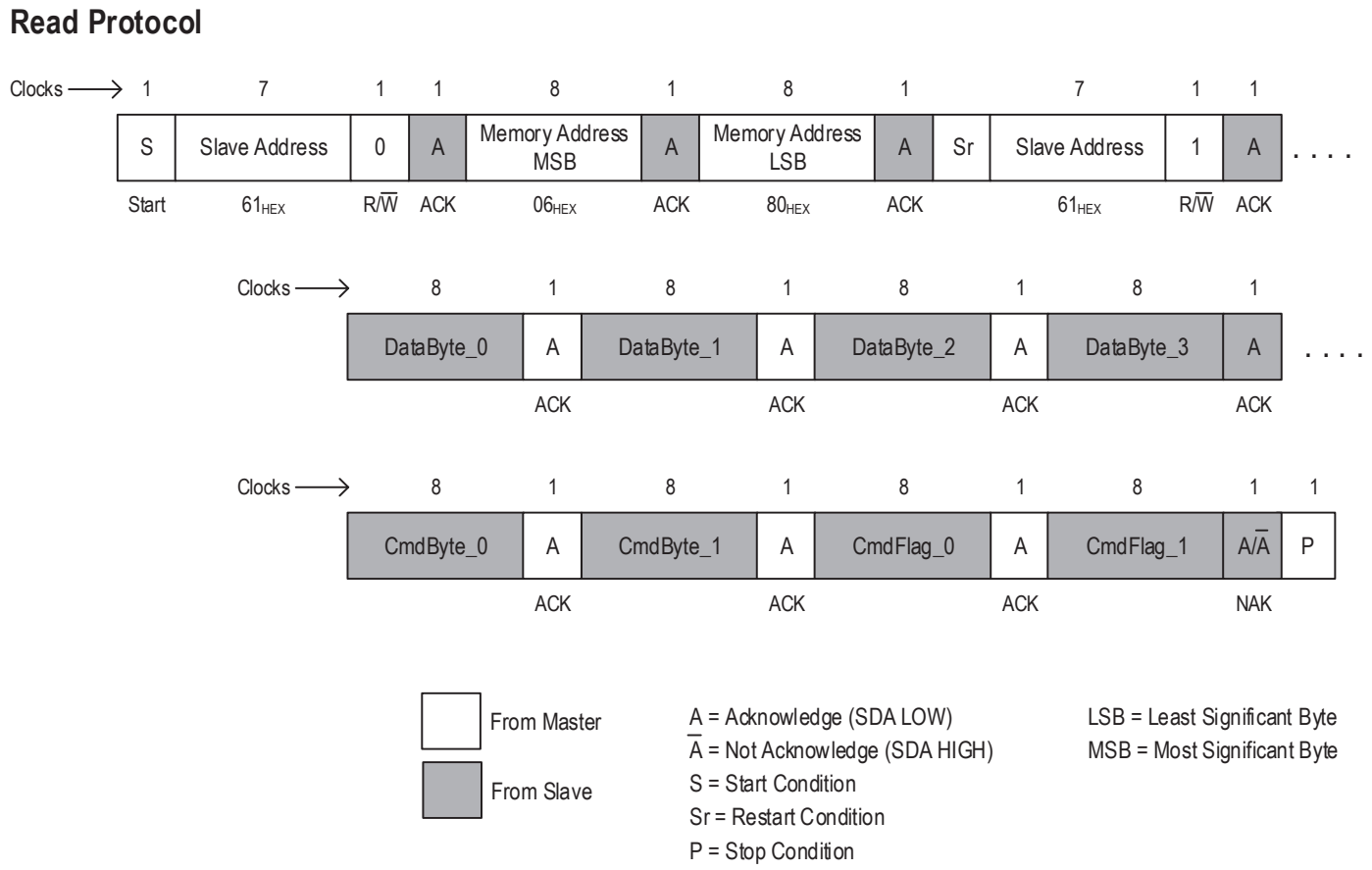
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10. Functional Registers

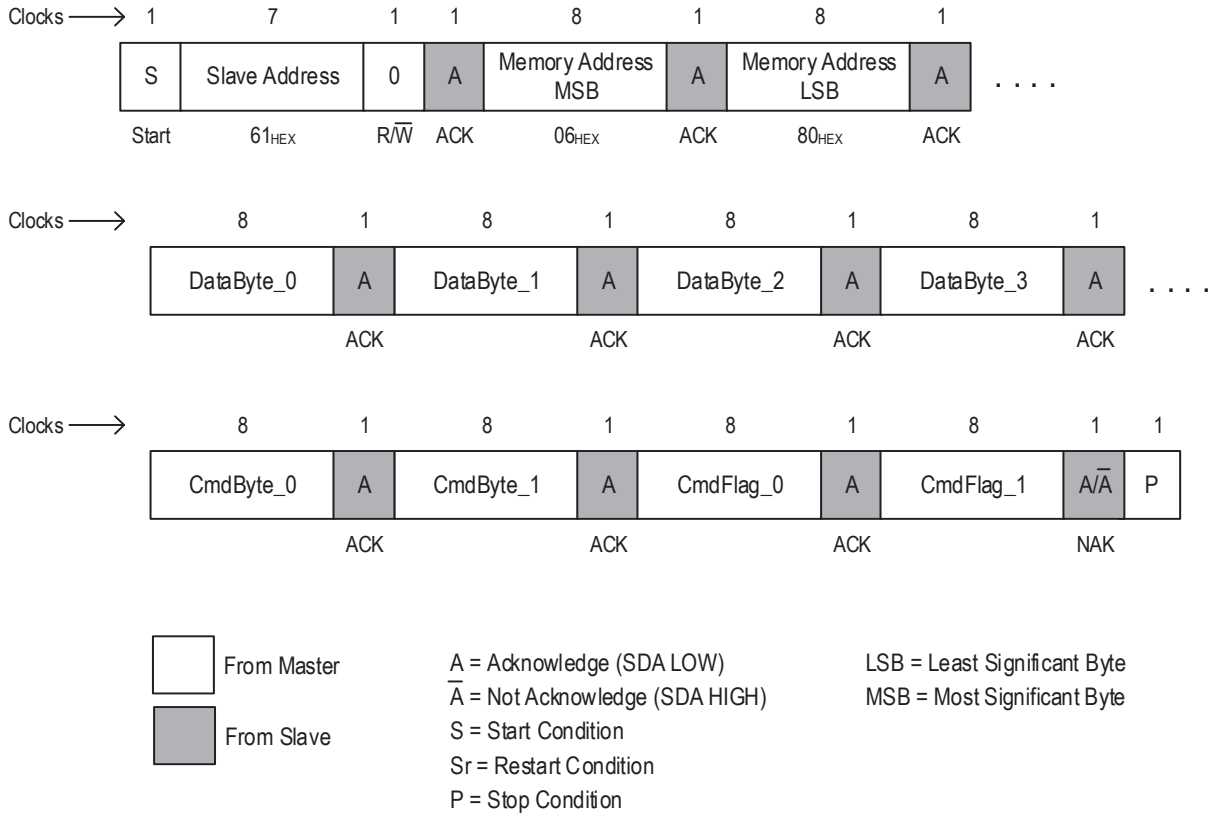
The P9242-R registers can be read and written to via the P9242-R's I2C interface on the SCL and SDA pins. Section 10.1 defines the protocol for reading and writing via this interface. Section 10.2 gives the details for the register definitions.

10.1 I2C Interface

Figure 24. I2C Access Read Protocol and Write Protocol



Write Protocol



10.2 Register Addresses and Definitions

The tables in this section provide a comprehensive list of address locations, field names, available operations (R or RW), default values, and functional descriptions of all internally accessible registers contained within the P9242-R. The default I^2C slave address is 61_{HEX}. The address of each register has a two-byte structure. For example, the address of the device ID high byte is 01_{HEX} and 05_{HEX}.

Table 10. Device ID Register

Address and Bit	Register Field Name	R/W	Default	Function and Description
0104_{HEX} [7:0]	Device_ID_L	R	42_{HEX}	Device ID low byte
0105_{HEX} [7:0]	Device_ID_H	R	92_{HEX}	Device ID high byte

Table 11. Firmware Major Revision

Address and Bit	Register Field Name		R/W	Default	Function and Description
$010C_{HEX}$ [7:0]	FW_Major_Rev_L		R	06_{HEX}	Major firmware revision low byte
$010D_{HEX}$ [7:0]	FW_Major_Rev_H		R	00_{HEX}	Major firmware revision high byte

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Table 12. Firmware Minor Revision

Address and Bit	Register Field Name	R/W	Default	Function and Description
$010E_{HEX}$ [7:0]	FW_Minor_Rev_L	R	16_{HEX}	Minor firmware revision low byte
$010F_{HEX}$ [7:0]	FW_Minor_Rev_H	R	00_{HEX}	Minor firmware revision high byte

Table 13. State Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E0_{HEX}$	System State	R	00_{HEX}	0_{DEC} = Startup 1_{DEC} = Idle 2_{DEC} = Analog Ping Phase 4_{DEC} = Digital Ping Phase 5_{DEC} = WPC Identification 7_{DEC} = WPC Configuration 8_{DEC} = Power Transfer Initialization 9_{DEC} = Power Transfer State 11_{DEC} = Remove Power 12_{DEC} = Restart 13_{DEC} = WPC Negotiation

Table 14. Status Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E1_{HEX}$	System Status	R	00_{HEX}	0_{DEC} = System Normal 1_{DEC} = FOD Alarm 2_{DEC} = EPT Charge Complete 4_{DEC} = EPT No Response 5_{DEC} = EPT Internal Fault 6_{DEC} = Over-Temperature Alarm 7_{DEC} = Over-Current 9_{DEC} = EPT Other Rx Fault 10_{DEC} = Negotiation Fail

Table 15. Read Register – Input Current

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E2_{HEX}$ [7:0]	Coil_current [7:0]	R	–	8 LSB of coil current value in mA.
$06E3_{HEX}$ [7:0]	Coil_current [15:8]	R	–	8 MSB of coil current value in mA.

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Table 16. Read Register – Input Voltage

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E4_{HEX}$ [7:0]	Coil_voltage [7:0]	R	–	8 LSB of coil voltage value in mV.
$06E5_{HEX}$ [7:0]	Coil_voltage [15:8]	R	–	8 MSB of coil voltage value in mV.

Table 17. Read Register – Remote Temperature Sensing Voltage

$$Sensing\ Voltage = \frac{Thermistor\ ADC\ Value[15:0]}{4095} * 2.4V$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E8_{HEX}$ [7:0]	Thermistor ADC Value [7:0]	R	–	8 LSB of thermistor ADC value.
$06E9_{HEX}$ [7:0]	Thermistor ADC Value [15:8]	R	–	8 MSB of thermistor ADC value.

Table 18. Read Register – Operating Frequency

$$f_{OP} = \frac{60MHz}{FRE_CNT[15:0]}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EA_{HEX}$ [7:0]	FRE_CNT [7:0]	R	–	8 LSB of operating frequency count.
$06EB_{HEX}$ [7:0]	FRQ_CNT [15:8]	R	–	8 MSB of operating frequency count.

Table 19. Read Register – Operating Duty Cycle

$$DUTY\ CYCLE = \frac{DUTY_CNT * 50\%}{255}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EC_{HEX}$ [7:0]	DUTY_CNT [7:0]	R	–	8 LSB of operating duty count.
$06ED_{HEX}$ [7:0]	DUTY_CNT [15:8]	R	–	8 MSB of operating duty count.

Table 20. Read Register – Full/Half Bridge Status

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EE_{HEX}$ [7:0]	Full/half bridge status [7:0]	R	–	1 = Half bridge. 0 = Full bridge.

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11. Application Information

11.1 Power Dissipation and Thermal Requirements

The P9242-R is offered in a 48-VFQFN package that has a maximum power dissipation capability of about 1.47W. The maximum power dissipation of the package is determined by the number of thermal vias between the package and the printed circuit board (PCB). The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C. The junction temperature rises when the heat generated by the device's power dissipation flow is impeded by the package-to-PCB thermal resistance.

The VFQFN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 27.2°C/W when the PCB layout design is optimized as described in the *P9242-R Layout Guide* document. The techniques noted in the PCB layout section must be followed when designing the printed circuit board layout. Attention to the placement of the P9242-R and bridge FET packages in proximity to other heat-generating devices in a given application design should also be considered. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attached thermal pad size (VFQFN) and thermal vias, and the final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

First, the maximum power dissipation for a given situation should be calculated using Equation 2:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}} \qquad \textbf{Equation 2}$$

Where

$P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_A = Ambient temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9242-R is 125°C. The thermal resistance of the 48-pin VFQFN package (NDG48) is optimally θ_{JA}=27.2°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is given by the following equation:

$P_{D(Max)}$ = (125°C - 85°C) / 27.2°C/W ≅ 1.47 Watt

All the previously mentioned thermal resistances are the values found when the P9242-R is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

11.2 Recommended Coils

Table 21. Recommended Coil Manufactures

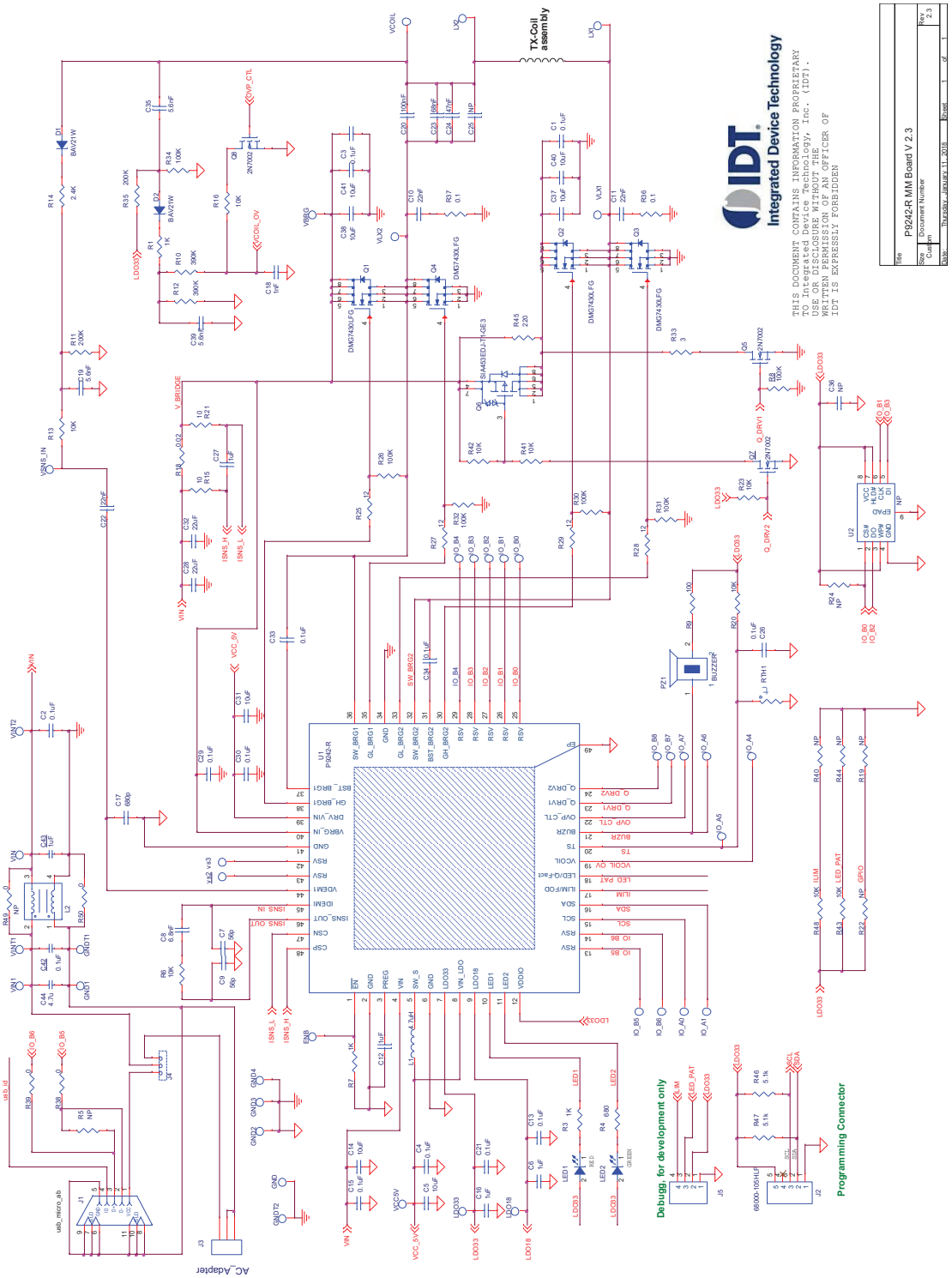
Output Power	Vendor	Part number	Inductance at 100kHz	DCR at 20°C
15W	SUNLORD	SWA53N53H30C11B	10µH	50mΩ
15W	TDK	WT525225-12F2-MA2-G	10.6µH	40mΩ

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11.3 Typical Application Schematic

The typical application schematic provides a basic guideline to understanding and building a functional medium-power wireless power transmitter type MP-A2 as described in the WPC specifications. Other components, not shown on the typical application schematic, might be needed in order to comply with other requirements, such as EMC or thermal specifications.

Figure 25. P9242-R Typical Application Schematic V2.3



11.4 Bill of Materials (BOM)

Table 22. P9242-R MM Evaluation Kit V2.3 Bill of Materials

Item	Reference	Quantity	Value	Description	Part Number	PCB Footprint
1	C1, C2, C3, C4, C13, C15, C21, C26, C29, C30, C33, C34	12	0.1µF	CAP CER 0.1µF 25V 10% X7R 0402	C1005X7R1E104K050BB	0402
2	C5, C14, C31, C37, C38, C40, C41	7	10µF	CAP CER 10µF 25V 20% X5R 0603	C1608X5R1E106M080AC	0603
3	C6, C12, C16, C27	4	1µF	CAP CER 1µF 25V 20% X5R 0402	C1005X5R1E105M050BC	0402
4	C7, C9	2	56pF	CAP CER 56PF 50V NP0 0402	CL05C560JB5NNNC	0402
5	C8	1	6.8nF	CAP CER 6800PF 25V X7R 0402	GRM155R71E682KA01D	0402
6	C10, C11	2	22nF	0.022µF 50V Ceramic Capacitor X7R 0603	GCM188R71H223KA37D	0603
7	C17	1	680pF	CAP CER 680PF 50V X7R 0402	CL05B681KB5NNNC	0402
8	C18	1	1nF	CAP CER 1000pF ±10% 50V X7R 0402	GRM155R71H102KA01D	0402
9	C19, C35, C39	3	5.6nF	5600pF 100V Ceramic Capacitor C0G, NP0 0603	C1608C0G2A562J080AC	0603
10	C20	1	100nF	CAP CER 0.1µF 100V C0G 1206	C3216C0G2A104K160AC	1206
11	C22	1	22nF	CAP CER 0.022µF 50V 10% X7R 0402	GRM155R71H223KA12D	0402
12	C23	1	68nF	CAP CER 0.068µF 100V NP0 1206	C3216C0G2A683K160AC	1206
13	C24	1	47nF	CAP CER 0.047µF 100V NP0 1206	C3216C0G2A473J115AC	1206
14	C25	1	NP	CAP CER 10000PF 100V C0G 1206	C3216C0G2A103J115AA	1206
15	C28, C32	2	22µF	CAP CER 22µF 25V 20% X5R 1206	GRM31CR61E226KE15L	1206
16	C36	1	NP	CAP CER 0.1µF 25V 10% X7R 0402	C1005X7R1E104K050BB	0402
17	C42	1	0.1µF	0.10µF 50V Ceramic Capacitor X7R 0603	GRM188R71H104KA93D	0603
18	C43	1	1µF	1µF 25V Ceramic Capacitor X5R 0603	GRM188R61E105KA12D	0603
19	C44	1	4.7µF	4.7µF 25V Ceramic Capacitor X5R 0603	GRM188R61E475KE11D	0603
20	D1, D2	2	BAV21W	DIODE GEN PURP 80V 125MA DFN	BAV21W-7-F	sod123
21	VLX1, VINT1, IO_B1, IO_A1, GNDT1, vs2, VLX2, VINT2, IO_B2, GNDT2, vs3, IO_B3, IO_B4, IO_A4, VCC5V, IO_B5, IO_A5, IO_B6, IO_A6, IO_B7, IO_A7, IO_B8, LDO18, LDO33, VSNS_IN, VCOIL, VBRG, IO_B0, IO_A0, ENB	30	PTH_TP	30 GAUGE WIRE PAD	NP	TEST_PT30D PAD
22	VIN1, GND1, GND2, GND3, GND4, VIN, GND	7	TP	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_1 35x70
23	J1	1	5P	CONN RCPT MCR USB AB SMD TH SHLL	ZX62D-AB-5P8	usb_micro_ab
24	J2	1	68000-105HLF	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sip5

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Item	Reference	Quantity	Value	Description	Part Number	PCB Footprint
25	J3	1	AC_Adapter	CONN POWER JACK 2.5X5.5MM HI CUR	PJ-002AH	CONN_POWER_JACK5_5MM
26	J4	1	TP	CONN HEADER 3POS .100" STR GOLD	901200763	sip3
27	J5	1	SIP con	4 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold or Gold, GXT™	961104-6404-AR	sip-4
28	LED1	1	LED	LED RED CLEAR 0603 SMD	150060RS75000	0603_diode
29	LED2	1	LED	LED GREEN CLEAR 0603 SMD	150060GS75000	0603_diode
30	LX1, LX2	2	NP	Tx Coil assemble through hole	NA	TP_TXCoil
31	L1	1	4.7µH	FIXED IND 4.7µH 620MA 500 MOHM	CIG10W4R7MNC	L0603
32	L2	1	NP	Common mode EMI choke	ACM4520-901-2P-T-000	EMI_TDK_ACM4520L
33	PZ1	1	BUZZER	BUZZER PIEZO 4KHZ 12.2MM PC MNT	PS1240P02CT3	9235_buzzer
34	Q1, Q2, Q3, Q4	4	DMG7430LFG	MOSFET N-CH 30V 10.5A PWRDI3333	DMG7430LFG-7	powerdi3333_8ld_fet
35	Q5, Q7, Q8	3	2N7002	N-Channel 60-V (D-S) MOSFET	2N7002KT1G	SOT23_3
36	Q6	1	SIA453EDJ-T1-GE3	MOSFET P-CH 30V 24A PPAK SC-70-6	SIA453EDJ-T1-GE3	sc70_6ld_fet
37	RTH1	1	NP	NTC Thermistor 10k Bead	NTCLE203E3103JB0	805
38	R1, R3, R7	3	1K	RES SMD 1K OHM 5% 1/16W 0402	RC0402JR-071KL	0402
39	R4	1	680	RES SMD 680 OHM 5% 1/16W 0402	RC0402JR-07680RL	0402
40	R5	1	NP	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	0402
41	R6, R13, , R16, R20, R23, R41, R42, R43, R48	9	10K	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	0402
42	R8, R26, R30, R31, R32	5	100K	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	0402
43	R24	1	NP	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	0402
44	R9	1	100	RES SMD 100 OHM 5% 1/10W 0603	RC0603JR-07100RL	0603
45	R10, R12	2	390K	RES SMD 390K OHM 5% 1/10W 0603	ERJ-3GEYJ394V	0603
46	R14	1	2.4K	RES SMD 2.4K OHM 5% 1/10W 0402	ERJ-2GEJ242X	0402
47	R11, R35	2	200K	RES SMD 200K OHM 1% 1/10W 0603	RC1608F204CS	0603
48	R15, R21	2	10	RES SMD 10 OHM 1% 1/10W 0402	ERJ-2RKF10R0X	0402
49	R18	1	0.02	RES SMD 0.02 OHM 1% 1/8W 0805	WSL0805R0200FEA	0805
50	R19, R22, R40, R44	4	NP	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	0402
51	R25, R27, R28, R29	4	12	RES SMD 12 OHM 5% 1/10W 0402	ERJ-2GEJ120X	0402
52	R33	1	3	RES SMD 3 OHM 1% 1/8W 0805	RC0805FR-073RL	0805
53	R34	1	100K	RES SMD 100K OHM 1% 1/10W 0603	ERJ-3EKF1003V	0603
54	R36, R37	2	0.1	RES SMD 0.1 OHM 5% 1/6W 0402	ERJ-2BSJR10X	0402
55	R38, R39	2	0	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	0402

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Item	Reference	Quantity	Value	Description	Part Number	PCB Footprint
56	R45	1	220	RES SMD 220 OHM 1% 0.4W 0805	RC1206FR-07220RL	1206
57	R46, R47	2	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	0402
58	R49, R50	2	0	RES SMD 0 OHM JUMPER 1/8W 0805	RC0805FR-070RL	0805
59	U1	1	P9242-R	Medium Power Transmitter	P9242-R	socketqfn_48_6x6_0p4
60	U2	1	NP	SPIFLASH 2M-BIT 4KB UNIFORM SECT	W25X20CLUXIG TR	uson_2x3_8LD

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12. Package Outline Drawings

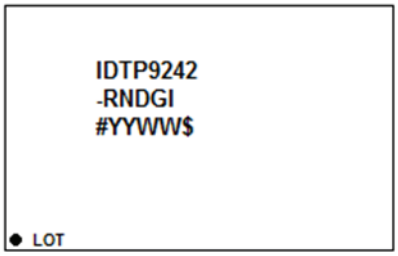
The package outline drawings and land pattern are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

13. Special Notes: NDG 48-VFQFN Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours prior to the assembly reflow process.

14. Marking Diagram



1. Line 1: Company name and part number.
2. Line 2: -R is part of the part number, which is followed by the package code.
3. Line 3: “YYWW” is the last two digits of the year and two digits for the week that the part was assembled. # is the device step.“$” denotes the mark code.

15. Ordering Information

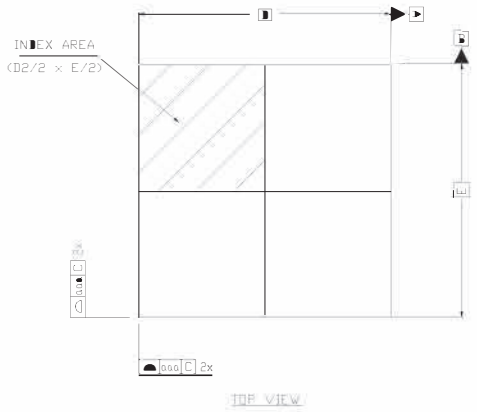
Orderable Part Number	Description and Package	MSL Rating	Shipping Package	Ambient Temperature
P9242-RNDGI8	P9242-R Wireless Power Receiver for 15W Applications, 48-VFQFN (6 x 6 mm) package (NDG48P2)	MSL3	Reel	0°C to +85°C

16. Revision History

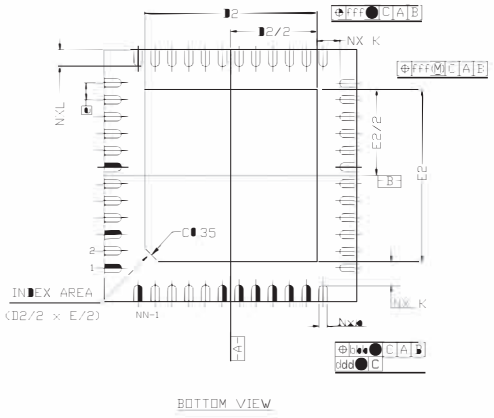
Revision Date	Description of Change
January 16, 2018	▪ Revision of D+ and D- pins (13 and 14) to RSV (reserved) ▪ Revision of GPIO pin 29 to RSV (reserved). ▪ Update for pin names for ILIM/FOD and LED/Q-Fact. ▪ Updates for descriptions of FOD, Q-Fact, and LED. ▪ Correction for color description for LED1 and LED2 in Table 9. ▪ Addition of register tables for Device ID and firmware revision. ▪ Updated application schematic and BOM ▪ Correction of MSL rating ▪ Template update. The package outline drawings are now appended to the end of the document.
March 30, 2017	▪ Update for manufacturer information in Table 21 ▪ Update for disclaimer
December 16, 2016	Initial release.

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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/06/16	JH
01	ADD CHAMFER	09/14/16	JH







SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	4.10	4.20	4.30
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
K		0.50 REF.	
D		6.00 BSC.	
E		6.00 BSC.	
e		0.40 BSC.	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 REF	---
N		48	
ND		12	
NE		12	
b	0.15	0.20	0.25
TOLERANCE of FORM & POSITION			
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

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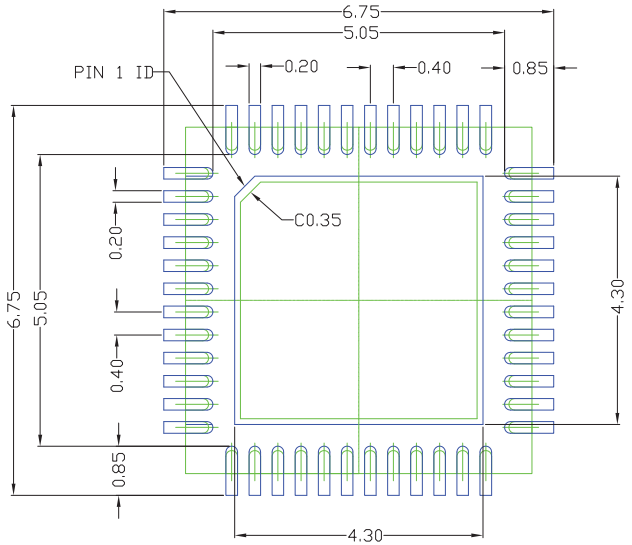
APPROVALS	DATE
DRAWN CALC	01/06/16
CHECKED	

TITLE: ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY
0.40 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4212-02	01

DO NOT SCALE DRAWING | SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	01/06/16	JH
01	ADD CHAMFER	09/14/16	JH



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°		IDT™ www.IDT.com	6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591
APPROVALS	DATE	TITLE	ND/NDG 48 PACKAGE OUTLINE 6.0 x 6.0 mm BODY 0.40 mm PITCH QFN
DRAWN RAC	01/06/16		
CHECKED			
		SIZE C	DRAWING No. PSC-4212-02 REV 01
DO NOT SCALE DRAWING		SHEET 2 OF 2	