Description

The P9243-GB is a highly integrated, magnetic induction, wireless power transmitter that supports up to 15W in compliance with the WPC-1.2.4 specification or proprietary applications. It is compatible with all popular wireless charging protocols including the WPC Baseline Power Profile (BPP), Extended Power Profile (EPP), up to 7.5W charging for iPhones, and Samsung Fast Charge. This system-on-chip solution (SoC) operates with an input voltage range of 5V to 19V.

The P9243-GB transmitter IC includes an industry-leading 32-bit ARM® Cortex®-M0 processor, offering a high level of programmability and extremely low standby power consumption. The P9243-GB has only pre-programmed bootloader firmware in the internal memory, and must be used in conjunction with an external flash memory that contains application firmware. This architecture gives the user the flexibility to change the firmware in the external flash to meet application-specific requirements.

The P9243-GB transmitter generates power through the power coil, detects the presence of a wireless power receiver, decodes the communication packets from the receiver, and adjusts the transmitted power by controlling the voltage based on feedback from the receiver. The device is specially designed to support fixed-frequency operation as described in the WPC MP-A11 coil configuration with an external input step-down buck regulator. It uses an external oscillator for very accurate 127.7kHz fixed frequency operation.

The transmitter detects if a foreign metal object is placed on the transmitter pad via advanced Q detection. The microcontroller empowers the user to customize foreign object detection (FOD) threshold settings. The I2C serial communication allows the user to read the transmitter's basic information, such as voltage, current, frequency, and fault conditions.

The P9243-GB is available in a lead-free, space-saving 48-VFQFPN package. The product is rated for a -40ºC to +85ºC operating temperature range.

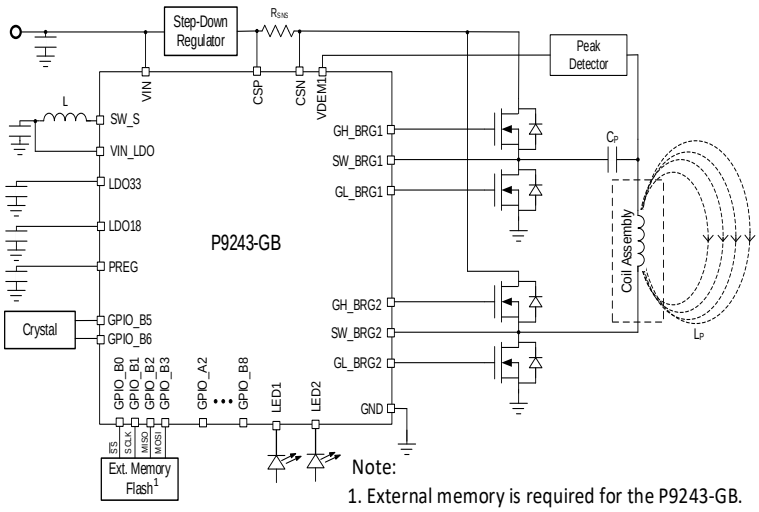
Typical Applications

- BPP and EPP Wireless Charging Pads
- Up to 7.5W charging for iPhones
- Samsung Fast Charging Pads
- After-Market Automotive Wireless Charging Pads

Features

- Power transfer up to 15W at receiver side
- Wide input voltage range: 5V to 19V
- WPC-1.2.4 compatible, MP-A11 coil configuration
- Supports system parameters configuration using a GUI
- Integrated drivers for external power MOSFETs
- Embedded 32-bit ARM® Cortex®-M0 processor (trademark of ARM, Ltd.)
- Simultaneous voltage and current demodulation scheme for WPC communication
- Integrated current sense amplifier
- Supports accurate 127.7kHz frequency operation
- Feedback control for external input step-down regulator
- Dedicated remote temperature sensing
- User-programmable power transfer LED indicators
- User-programmable foreign objects detection (FOD)
- WPC EPP-based Q-factor detection
- Active-LOW enable pin for electrical on/off
- Over-current and over-temperature protection
- Supports I2C interface
- -40°C to +85°C ambient operating temperature range
- 48-VFQFPN (6 × 6 mm) RoHS-compliant package

Typical Application Circuit



Note:
1. External memory is required for the P9243-GB.

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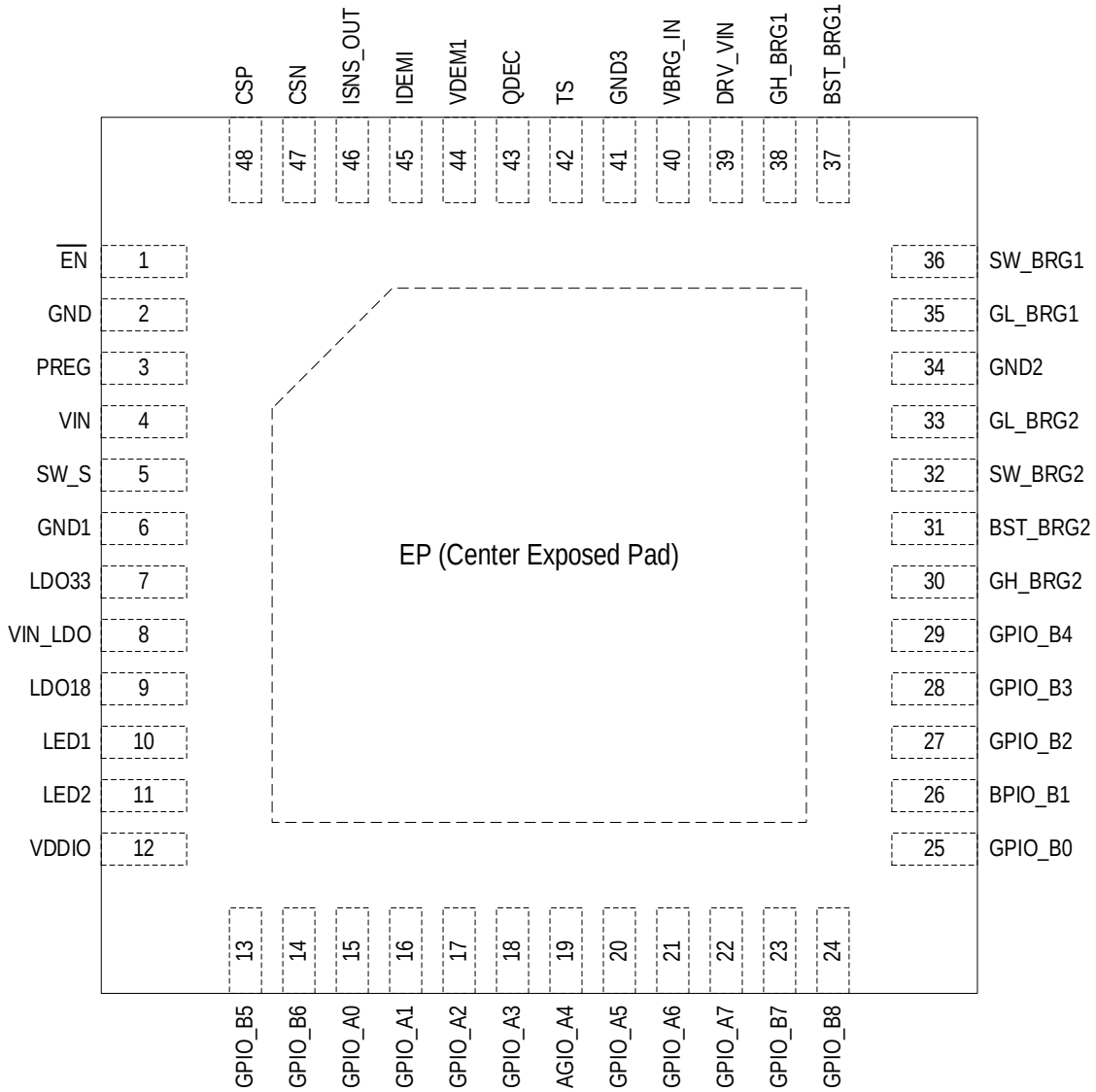
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1. Pin Assignments

Figure 1. Pin Assignments



2. Pin Descriptions

Table 1. Pin Descriptions

Note: See important table notes at the end of the table.

Pins	Name	Type	Function
1	$\overline{EN}$	Input	Active-LOW enable pin. When connected to logic HIGH, the P9243-GB enters the Shut Down Mode, which has a typical current consumption of 25µA. When connected to logic LOW, the device is in normal operation.
2	GND	–	Ground connection.
3	PREG	Output	Regulated 5V output used for internal device biasing. Connect a 1µF X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded.
4	VIN	Input	Input power supply. Connect a 10µF X5R or X7R ceramic capacitor from this pin to ground.
5	SW_S	Output	Internal step-down regulator`s switch node. Connect one of the terminals of a 4.7µH inductor to this pin.
6	GND1	-	Ground connection.
7	LDO33	Output	Regulated 3.3V output used for internal device biasing. Connect a 1µF X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded.
8	VIN_LDO	Input	Linear regulator input power supply. Connected this pin to the 5V output of the step-down regulator. This pin MUST NOT be externally loaded.
9	LDO18	Output	Regulated 1.8V output used for internal device biasing. Connect a 1µF X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded.
10	LED1	Output	Open-drain output. Connect an LED to this pin.
11	LED2	Output	Open-drain output. Connect an LED to this pin.
12	VDDIO	Input	Input power supply for internal biasing. This pin must be connected to LDO33.
13	GPIO_B5	Input	8MHz crystal input pin.
14	GPIO_B6	Input	8MHz crystal input pin.
15	GPIO_A0	Input	I2C interface clock input (SCL). Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
16	GPIO_A1	I/O	I2C interface data input and data output (SDA). Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
17	GPIO_A2 [a]	Input	General purpose input and output pin.
18	GPIO_A3 [a]	Input	General purpose input and output pin.
19	GPIO_A4 [a]	Output	Logic signal to bypass external buck regulator used to support Travel Adapters that support only 5V output power.
20	GPIO_A5 [a]	I/O	Connected to USB D- pin.
21	GPIO_A6 [a]	I/O	General purpose input and output pin.
22	GPIO_A7 [a]	I/O	Connected to USB D- pin.
23	GPIO_B7	I/O	PWM control signal for regulating buck converter output voltage.
24	GPIO_B8	I/O	Connected to USB D+ pin.

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Pins	Name	Type	Function
25	GPIO_B0	Output	Enable signal for external flash memory.
26	GPIO_B1	I/O	Clock signal for external flash memory.
27	GPIO_B2	I/O	Data output signal for external flash memory.
28	GPIO_B3	I/O	Data input signal for external flash memory.
29	GPIO_B4	Output	Enable signal for buck converter.
30	GH_BRG2	Output	Gate driver output for the high-side FET of half bridge group 2. Connect this pin to a series 22Ω resistor to the respective bridge FET gate.
31	BST_BRG2	Input	Bootstrap pin for half bridge group 2. Tie an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage higher than the input voltage.
32	SW_BRG2	Output	Switch node for half bridge group 2.
33	GL_BRG2	Output	Gate driver output for the low-side FET of half bridge group 2. Connect this pin to a series 22Ω resistor to the respective bridge FET gate.
34	GND2	–	Ground connection.
35	GL_BRG1	Output	Gate driver output for the low-side FET of half bridge group 1. Connect this pin to a series 22Ω resistor to the respective bridge FET gate.
36	SW_BRG1	Output	Switch node for half bridge group 1.
37	BST_BRG1	Output	Bootstrap pin for half bridge group 1. Tie an external capacitor from this pin to the SW_BRG1 to generate a drive voltage higher than the input voltage.
38	GH_BRG1	Output	Gate driver output for the high-side FET of half bridge group 1. Connect this pin to a series 22Ω resistor to the respective bridge FET gate.
39	DRV_VIN	Input	Input power supply for the internal gate drivers. Connect a 10µF capacitor from this pin to ground. This pin MUST NOT be externally loaded.
40	VBRG_IN	Input	Bridge voltage input sense pin.
41	GND3	–	Ground connection.
42	TS	Input	Remote temperature sensor for over-temperature shutdown. Connect this pin to the thermistor network.
43	QDEC	Input	Input signal for Q-factor measurement circuit.
44	VDEM1	Input	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by power receiver.
45	IDEMI	Input	High-pass filter input. Current demodulation pin for data packets based on coil current variation; transmitted by power receiver.
46	ISNS_OUT	Output	Input current sense output.
47	CSN	Input	Low-side input current sense.
48	CSP	Input	High-side input current sense.
–	EP	–	Ground connection.

[a] GPIO_A2 to GPIO_A7 are multi-function pins. With a firmware (FW) change, GPIO_A5 can be set to ADC inputs.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond those listed under "Absolute Maximum Ratings" might cause permanent damage to P9243-GB. Functional operation of P9243-GB at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods could affect long-term reliability.

Table 2. Absolute Maximum Ratings

Pins [a]	Rating [b]	Units
$\overline{EN}$, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2 [c]	-0.3 to 28	V
PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, GL_BRG1, GL_BRG2, VDEM1, IDEMI, ISNS_OUT, DRV_VIN, TS, GPIO_A0, GPIO_A1, GPIO_A2, GPIO_A3, GPIO_A4, GPIO_A5, GPIO_A6, GPIO_A7, GPIO_B0, GPIO_B1, GPIO_B2, GPIO_B3, GPIO_B4,GPIO_B5, GPIO_B6, GPIO_B7, GPIO_B8	-0.3 to 6	V
LDO18	-0.3 to 2	V

[a] All voltages are referred to ground unless otherwise noted. All GND pins and the exposed pad (EP) are connected internally and must also be connected together.

[b] During system application operation, pins SW_S, SW_BRG1, SW_BRG2, GH_BRG1, GH_BRG2, GL_BRG1, GL_BRG2 can momentarily go below ground by as much as -6.0V for no longer than 100ns.

[c] When measuring the GL_BRG1 and GL_BRG2 pins' absolute maximum voltage, the current must be limited to within the "Absolute Peak" and "DC Drive" current specifications.

Table 3. Package Thermal Information

Symbol	Description	VFQFPN Rating	Units
θ_{JA}	Thermal Resistance Junction to Ambient [a], [b], [c]	27.2	°C/W
θ_{JC}	Thermal Resistance Junction to Case [b], [c]	18.8	°C/W
θ_{JB}	Thermal Resistance Junction to Board [b], [c]	1.36	°C/W
T_J	Operating Junction Temperature [a], [b]	-40 to +125	°C
T_A	Ambient Operating Temperature [a], [b]	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51-standard 4-layer board with the dimensions 76.2 × 114.3 mm in still air conditions.

[c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

Test Model	Pins	Ratings	Units
Human Body Model (HBM)	All pins	±2000	V
Charged-Device Model (CDM)	All pins	±500	V

4. Electrical Characteristics

Table 5 Electrical Characteristics

Note: V_{IN} = 5V, $\overline{EN}$ = LOW, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies and UVLO						
V_{IN}	Input Operating Range [a]		4.25		19	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} rising		3.4	3.6	V
		V_{IN} falling		3.0		V
I_{IN}	Operating Mode Input Current	Power Transfer Phase, Vin = 12V		10		mA
I_{STD_BY}	Standby Mode Current	Periodic ping		1		mA
I_{SHD}	Shut-Down Mode Current			25	80	µA
Enable Pin Threshold ($\overline{EN}$)						
V_{IH}	Input Threshold HIGH		2.5			V
V_{IL}	Input Threshold LOW				0.5	V
I_{EN_LKG}	$\overline{EN}$ Pin Input Leakage Current	$V_{\overline{EN}}$ = 0V	-1		1	µA
		$V_{\overline{EN}}$ = 5V		2.5		µA
Step-Down Regulator [b] with C_{OUT} = 33µF; L = 4.7µH						
V_{OUT}	Step-Down Output Voltage	Vin > 5.5V		5.1		V
I_{OUT}	Output Current			50		mA
N-Channel MOSFET Drivers						
$t_{LS_ON_OFF}$	Low-Side Gate Driver Rise and Fall Times	C_{LOAD} = 3nF; 10% to 90%, 90% to 10%		50	150	ns
$t_{HS_ON_OFF}$	High-Side Gate Driver Rise and Fall Times	C_{LOAD} = 3nF; 10% to 90%, 90% to 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier Output Offset Voltage	Measured at the ISNS_OUT pin; V_{CSP} = V_{CSN}		0.6		V
$ISEN_{ACC_TYP}$	Measured Current Sense Accuracy [c]	V_{R_ISEN} = 25mV, I = 1.25A		±3.5		%
Analog to Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			10		
$V_{IN,FS}$	Full Scale Input Voltage			2.4		V

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
LDO18[b] (C_{OUT} = 1µF, VIN_LDO = 5.5V)						
V_{LDO18}	Output Voltage			1.8		V
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Accuracy		-5		+5	%
I_{OUT18_MAX}	Maximum Output Current			20	25	mA
LDO33[b] (C_{OUT} = 1µF, VIN_LDO = 5.5V)						
V_{LDO33}		C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	3.15	3.3	3.45	V
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Accuracy		-5		+5	%
I_{OUT18_MAX}	Maximum Output Current			10	25	mA
PREG						
V_{PREG}	5V LDO Regulator			5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold rising		140		˚C
		Threshold falling		120		˚C
Analog Input Pins Input Current Leakage (TS, QDEC)						
I_{LKG}	Leakage Current		-1		1	µA
Open-Drain Pins Output Logic Levels (LED1, LED2, GPIO_A0, GPIO_A1)						
V_{OH}	Output Logic HIGH		4			V
V_{OL}	Output Logic LOW	I = 8mA			0.5	V
General Purpose Inputs/Outputs Pins Logic Levels						
V_{IH}	Input Voltage HIGH Level		0.7 × VDDIO			V
V_{IL}	Input Voltage LOW Level				0.3 × VDDIO	V
I_{LKG}	Leakage Current				1	µA
V_{OH}	Output Logic HIGH	I = 8mA, VDDIO = 3.3V	2.4			V
V_{OL}	Output Logic LOW	I = 8mA, VDDIO = 3.3V			0.5	V
I2C Interface (GPIO_A0, GPIO_A1)						
f_{SCL_SLV}	Clock Frequency	As I2C slave			400	kHz
C_B	Capacitive Load	For each bus line			100	pF
C_{BIN}	GPIO_A0, GPIO_A1 Input Capacitance			5		pF
I_{LKG}	Input Leakage Current	V = GND and 3.3V	-1		1	µA

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and 10Ω, 1% input filter resistors are required to meet the FOD specification.

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5. Typical Performance Characteristics

The following performance characteristics are measured with a P9221-R-EVK 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted.

Figure 2. Efficiency vs. Output Load: V_{OUT_RX} = 12V

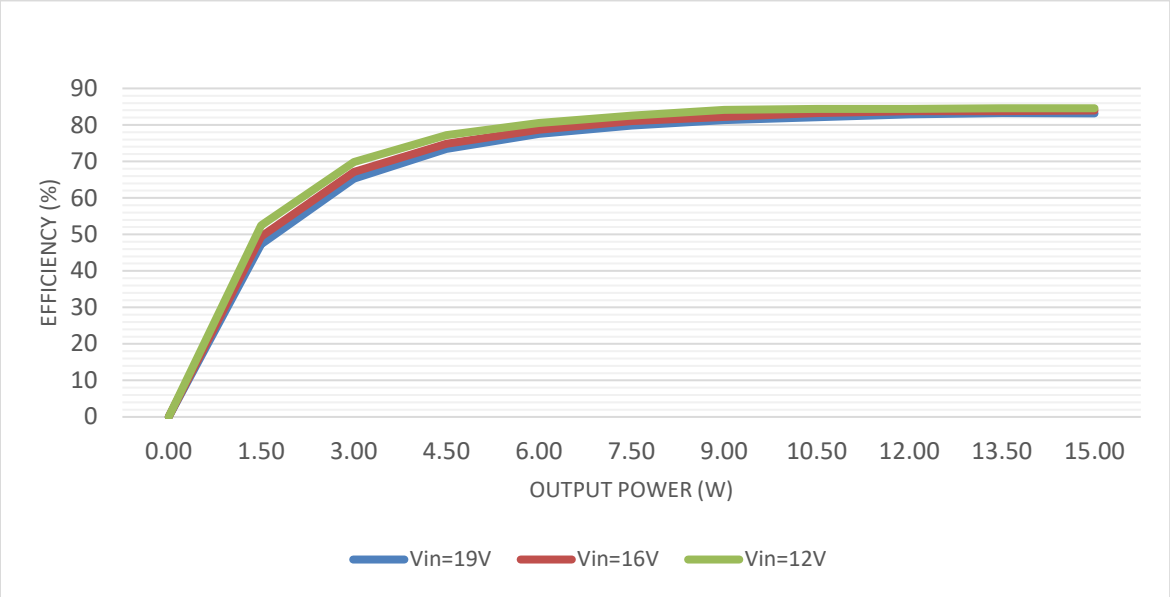


Figure 3. Full Load Efficiency and Charging Map vs. XY Positions (in mm scale): Vin = 19V, Vout = 12V, Spacer = 2.5mm

	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
12																					
11																					
10								77	75	75	75	75	75								
9								76	77	77	77	77	77	76	75						
8						75	77	78	78	79	79	79	78	78	77	76					
7					75	77	78	79	79	80	80	80	80	79	78	78	76				
6				75	77	78	79	80	80	81	81	81	80	80	80	79	77	75			
5				76	78	79	80	81	81	81	81	81	81	81	80	80	78	77			
4			75	77	79	80	81	81	81	81	81	81	81	81	81	80	79	78	75		
3			76	78	79	81	81	81	81	81	82	82	81	81	81	81	80	78	76		
2			77	79	80	81	81	81	81	82	82	82	82	81	81	81	80	79	77		
1			77	79	80	81	81	81	82	82	82	82	82	81	81	81	80	79	77	75	
0		75	77	79	80	81	81	82	82	82	82	82	82	82	81	81	80	79	78	75	
-1			77	79	80	81	81	82	82	82	82	82	82	82	81	81	80	79	77	75	
-2			77	79	80	81	81	82	82	82	82	82	82	81	81	81	80	79	77	75	
-3			76	78	79	81	81	81	81	82	82	82	82	81	81	80	80	79	77		
-4			75	78	79	80	81	81	81	81	81	81	81	81	81	80	79	78	76		
-5				76	78	79	80	81	81	81	81	81	81	81	80	80	79	77	75		
-6				77	77	78	79	80	80	81	81	81	81	80	80	79	78	76			
-7					75	77	78	79	80	80	80	80	80	79	79	78	76				
-8						75	77	78	78	79	79	79	79	78	78	76	75				
-9							75	76	77	77	78	78	77	77	76						
-10									75	75	76	76	75	75							
-11																					
-12																					
-13																					

The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted.

Figure 4. Efficiency vs. Output Load: V_{OUT_RX} = 9V

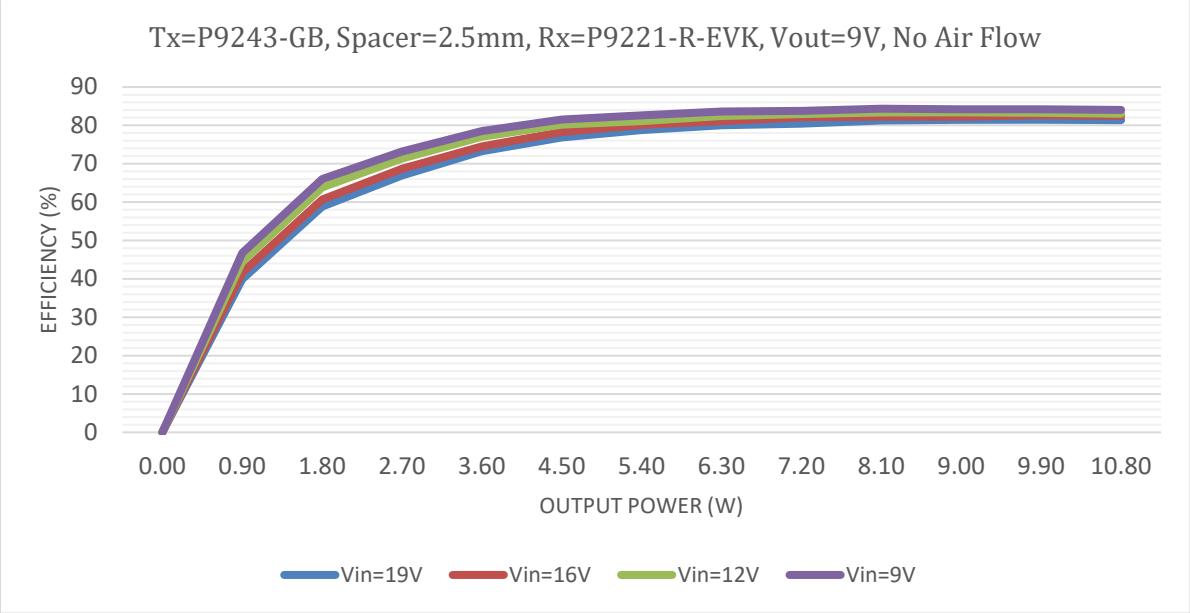


Figure 5. Full Load Efficiency and Charging Map vs. XY Positions (in mm scale): Vin = 12V, Vout = 9V, Spacer = 2.5mm

	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10
13																					
12																					
11										75	75	75									
10							75	76	77	78	78	78	77	76	75						
9						75	77	79	79	79	80	79	79	79	77	75					
8					76	78	79	80	80	80	80	80	80	80	79	78	75				
7				75	78	79	80	80	81	81	81	81	81	80	80	79	77	75			
6				77	79	80	80	81	81	81	81	81	81	81	81	80	79	76			
5			76	78	80	80	81	81	81	81	81	81	81	81	81	80	80	78	75		
4			77	79	80	81	81	81	81	81	82	81	81	81	81	81	80	79	76		
3			78	80	81	81	81	81	81	81	81	82	81	81	81	81	80	79	77		
2			77	79	80	80	80	81	81	82	82	82	82	81	81	81	81	80	78		
1		75	79	80	81	81	81	81	81	82	82	82	82	82	81	81	81	80	78		
0		75	79	80	81	81	81	81	81	82	82	82	81	81	81	81	81	80	78	75	
-1		75	78	80	81	81	81	81	81	82	82	82	81	81	81	81	81	80	78		
-2			78	80	80	81	81	81	81	81	81	81	81	81	81	81	81	79	77		
-3			77	79	80	81	81	81	81	81	81	81	81	81	81	81	80	79	76		
-4			76	78	80	80	81	81	81	81	81	81	81	81	81	80	80	78	75		
-5				77	79	80	80	81	81	81	81	81	81	81	81	80	79	77			
-6				75	78	79	80	80	80	81	81	81	81	80	80	79	78	75			
-7					75	78	79	80	80	80	80	80	80	80	79	78	76				
-8						75	77	78	79	79	79	79	79	78	78	76					
-9								76	77	78	78	78	77	77	75						
-10										75	75	75	75								
-11																					
-12																					

The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted.

Figure 6. Efficiency vs. Output Load: V_{OUT_RX} = 5V

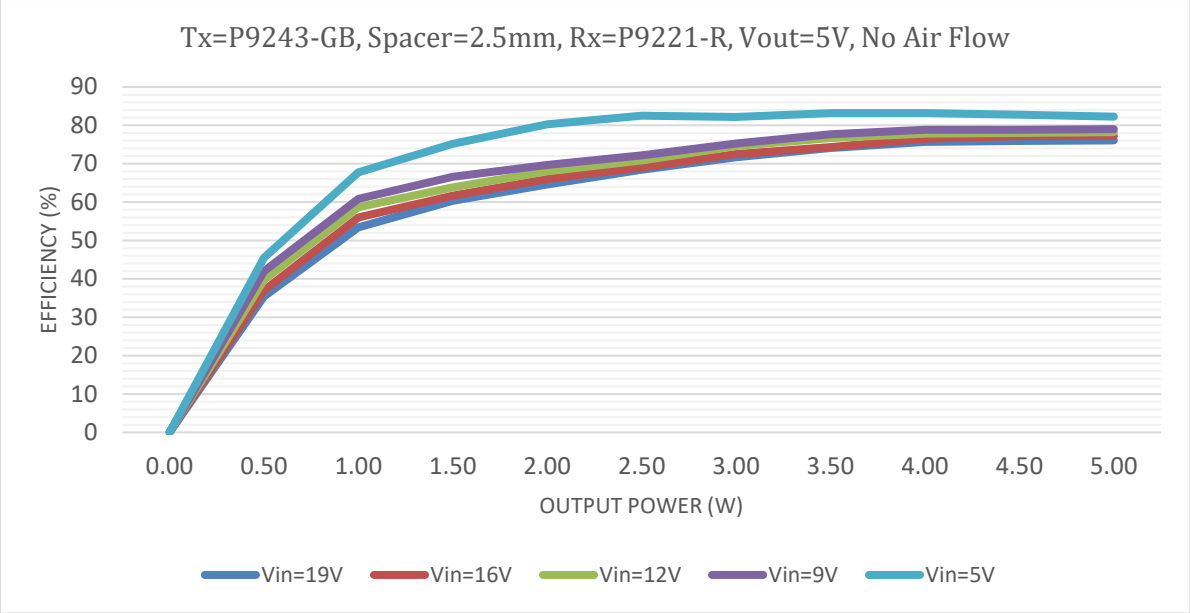


Figure 7. Full Load Efficiency and Charging Map vs. XY Positions (in mm scale): Vin = 12V, Vout = 5V, Spacer = 2.5mm

	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8	9	10	11
13																						
12																						
11																						
10																						
9																						
8										70	71	70	70	70								
7								70	71	72	72	73	72	72	71	70						
6							71	72	73	74	74	74	74	73	73	71	70					
5						70	72	73	74	75	75	75	75	75	74	73	71					
4						72	73	74	75	76	76	76	76	76	75	74	73	71				
3					70	72	74	76	76	76	77	77	77	76	76	75	73	72				
2					72	73	75	76	77	77	78	78	77	77	76	75	74	72	70			
1					72	74	75	76	77	77	78	78	78	77	76	76	75	73	71			
0				70	72	74	75	76	77	78	78	78	78	78	77	76	75	73	71			
-1				70	72	74	76	76	77	78	78	78	78	78	77	76	75	73	71			
-2				70	71	74	75	76	77	78	78	78	78	77	77	76	75	73	71			
-3					71	74	75	76	77	77	78	78	77	77	76	75	75	73	71			
-4					71	73	74	75	76	77	77	77	77	77	76	75	74	72				
-5					70	71	73	75	76	76	76	76	76	76	75	74	73	71				
-6						71	72	73	75	75	76	75	76	75	74	73	72	70				
-7							71	72	73	74	74	74	74	74	73	72	70					
-8								70	71	72	73	73	73	72	72	71						
-9									70	71	71	71	71	70	70							
-10																						
-11																						
-12																						
-13																						
-14																						

The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted.

Figure 8. Internal Buck Load Regulation

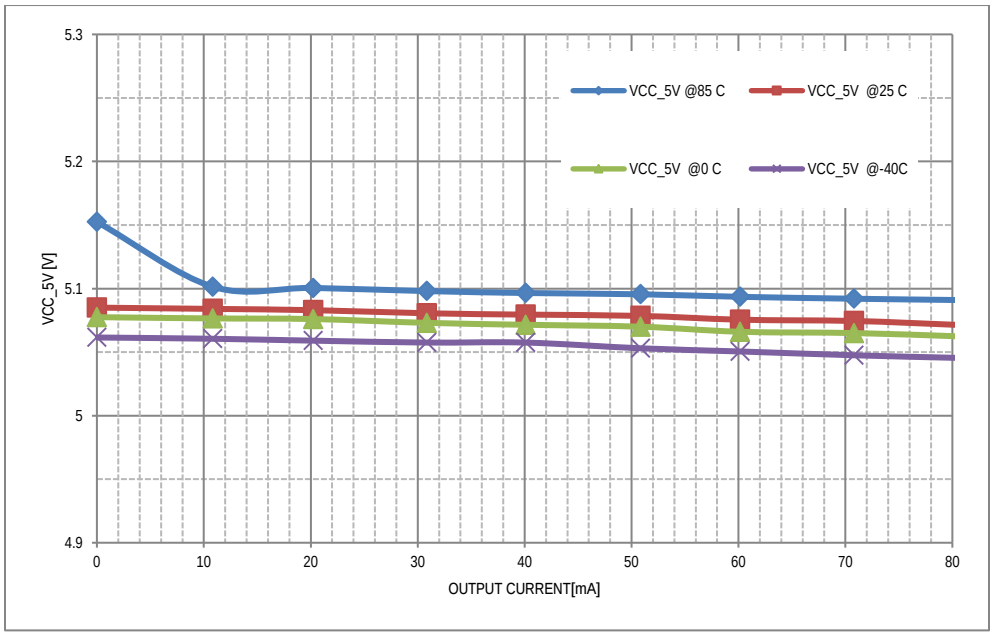
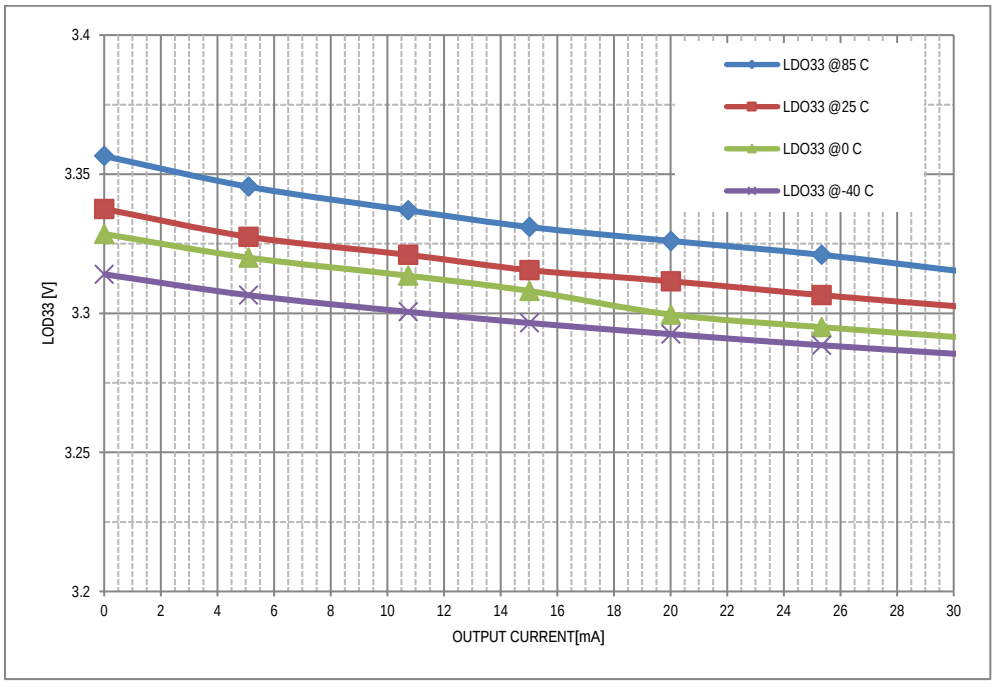


Figure 9. Load Regulation vs. Output Load: LDO33



The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted.

Figure 10. Load Regulation vs. Output Load: LDO18

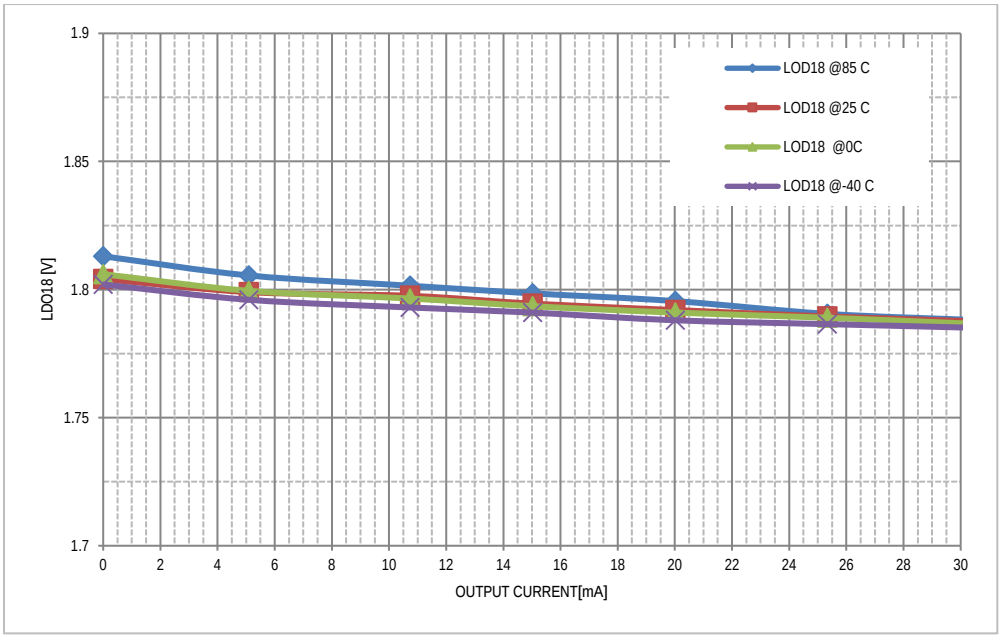
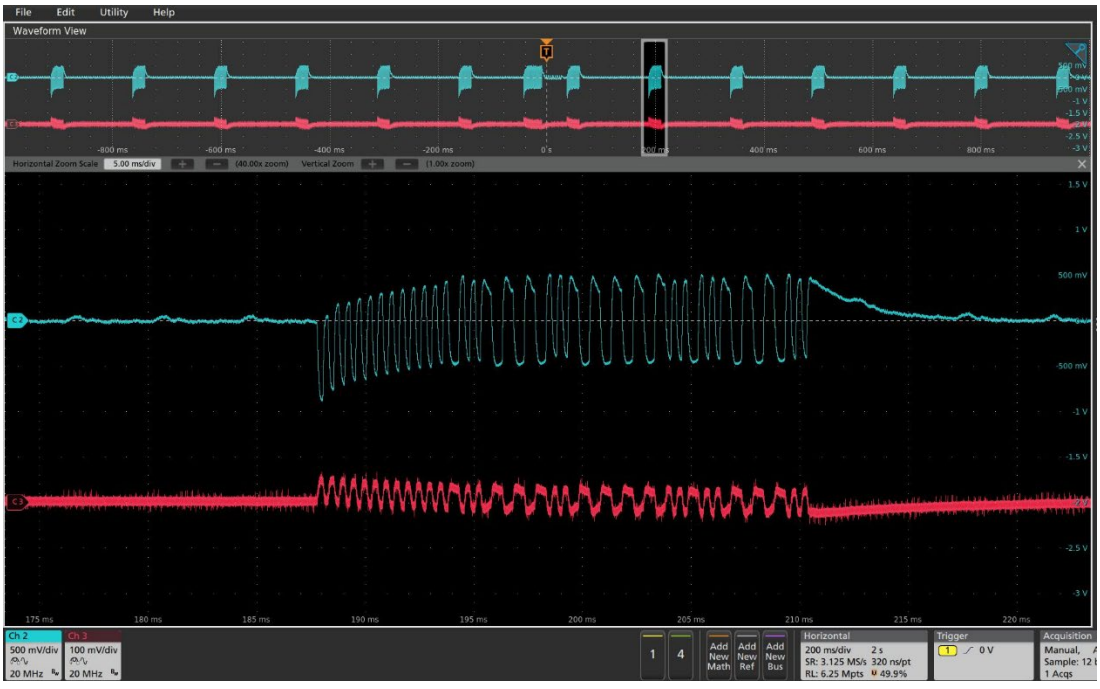


Figure 11. Voltage and Current Signal for Demodulation: Ch2 = VSNS, Ch3 = ISNS_IN



The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C, V_{IN} = 5V to 19V, and $\overline{EN}$ = LOW unless otherwise noted. Note: See the schematic in Figure 28 for the location of the signals in these figures.

Figure 12. USB Adaptor Start-up: Ch1 = VBRIDGE, Ch2 = Vin, Ch3 = D-, Ch4 = D+

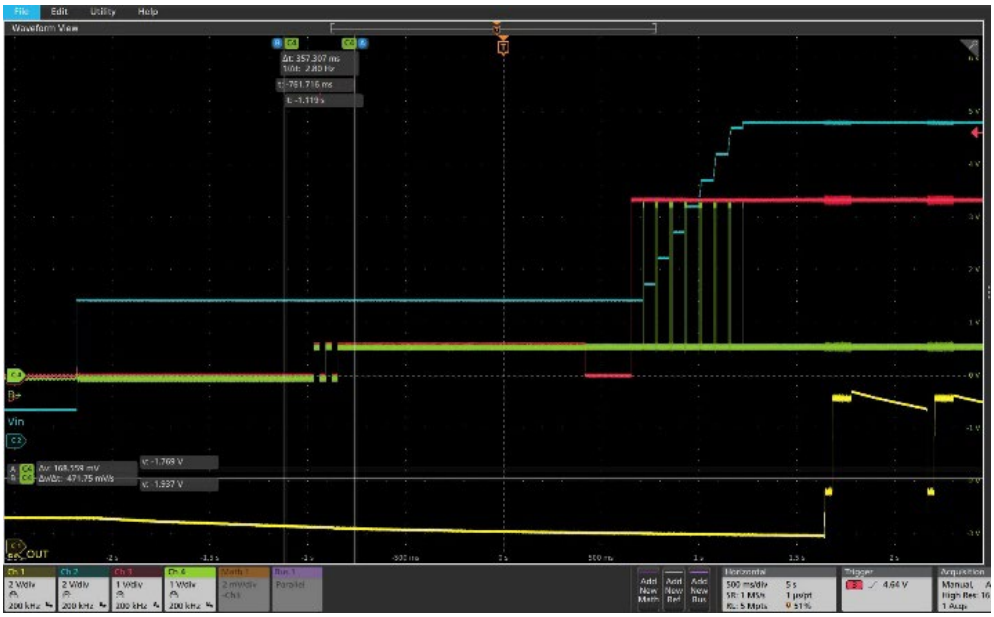
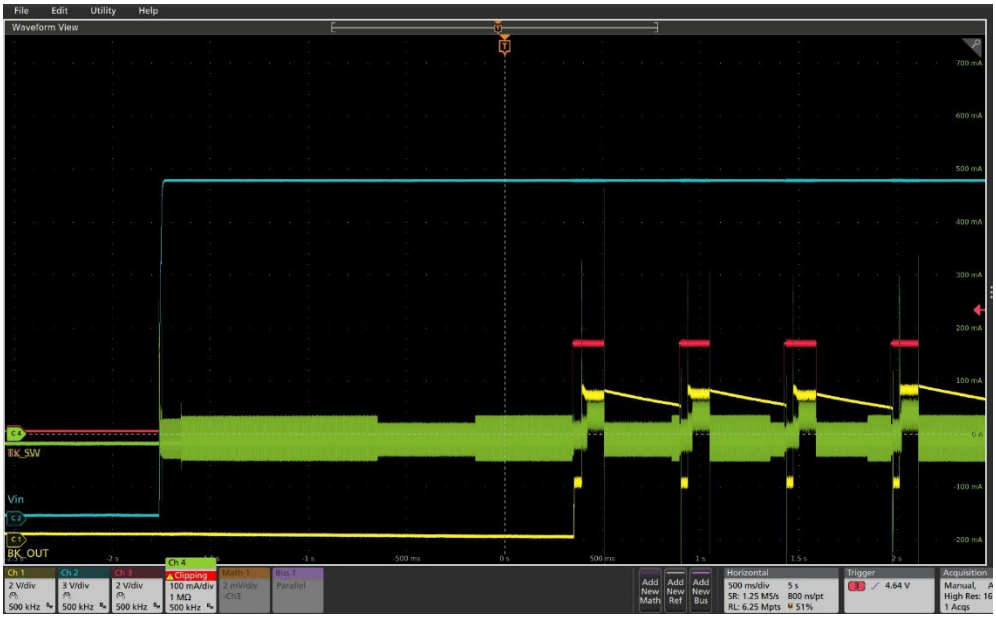
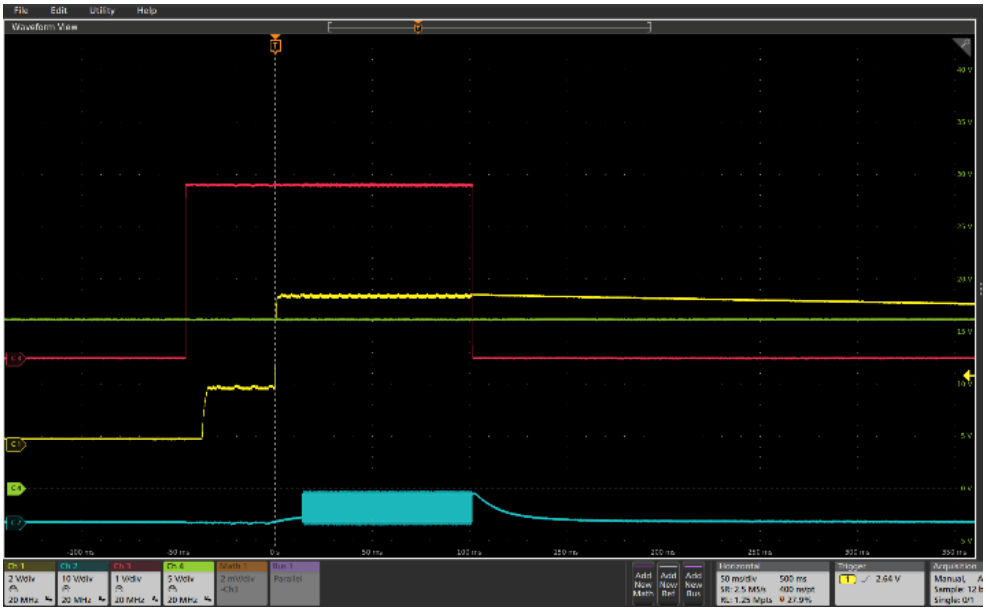


Figure 13. 19V Fixed Voltage Adaptor Start-up: Ch1 = VBRIDGE, Ch2 = Vin, Ch3 = GPIO_B4, Ch4 = iIn



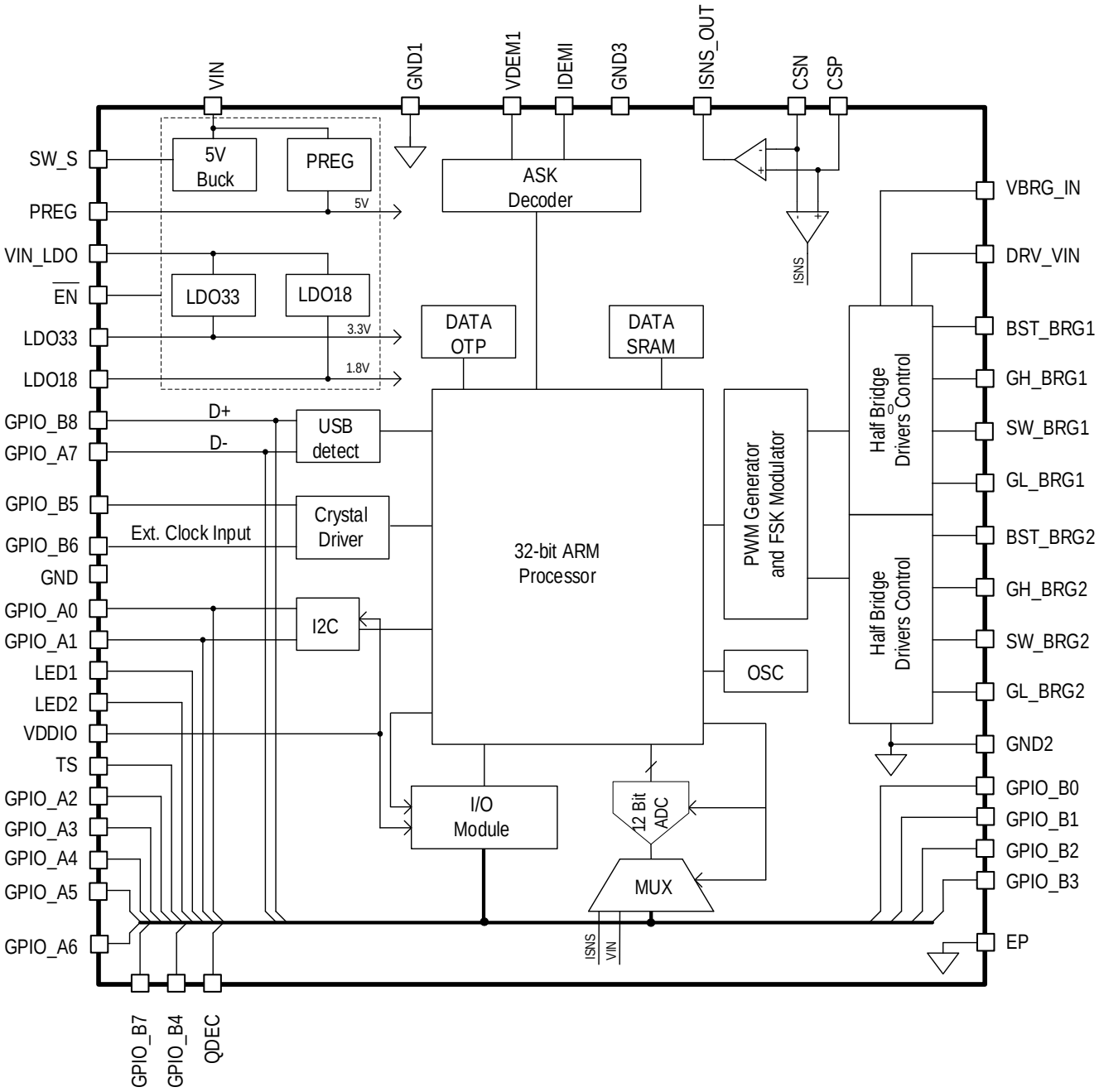
V_{IN} = 5V to 19V; $\overline{EN}$ = LOW. The following performance characteristics are measured with a P9221-R-EVK, 15W Wireless Power Receiver (RX) at T_A = +25°C unless otherwise noted. Note: See the schematic in Figure 28 for the location of the signals in these figures.

Figure 14. Enable and Disable of External Buck Regulator: Ch1 = VBRIDGE, Ch2 = Tx_SW, Ch3 = GPIO_B4



6. Function Block Diagram

Figure 15. Functional Block Diagram



7. General Description

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a loosely-coupled inductor pair to a receiver in a mobile device. Before each transmitter and receiver pair starts transferring power, a power contract will be agreed upon and created by the RX and TX. The amount of power transferred to the mobile device is controlled by the wireless power receiver via sending communication packets to the transmitter to increase, decrease, or maintain the power level. If a fault is detected, the transmitter can also stop power transfer to protect the system. A receiver can also initiate a stop power transfer command by sending an EPT Packet. The communication packet from receiver to transmitter is purely digital and consists of logic 1s and 0s, which are added on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. Amplitude shift keying (ASK) is used for the communication from receiver to transmitter; while communication from transmitter to receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency.

When the transmitter is not delivering power, it is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once an Extended Power Profile (EPP) receiver is detected, such as the P9221-R-EVK or equivalent, the transmitter may provide up to 15W of output power depending on the power contract between the transmitter and receiver. If a Baseline Power Profile (BPP) receiver is present, the transmitter can deliver up to 5W of output power.

The P9243-GB has features that ensure a high level of functionality and compliance with the WPC V1.2.4 specification requirements as illustrated in Figure 16, including a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

The P9243-GB converges all popular wireless charging protocols including WPC Baseline Power Profile (BPP), Extended Power Profile (EPP), up to 7.5W charging for iPhones, and Android proprietary fast charging modes. Depending on the type and capability of the power supply, the P9243-GB may operate in different modes. A USB adaptor detection circuit is also implemented in P9243-GB by firmware. The P9243-GB can detect input ports such as USB Standard Downstream Port (SDP), USB Charger Downstream Port (CDP), USB Dedicated Charging Port (DCP), and other AC/DC adaptors. When the connected power supply is limited at 5V, the P9243-GB functions as a BPP transmitter and can deliver up to 5W at the Rx output.

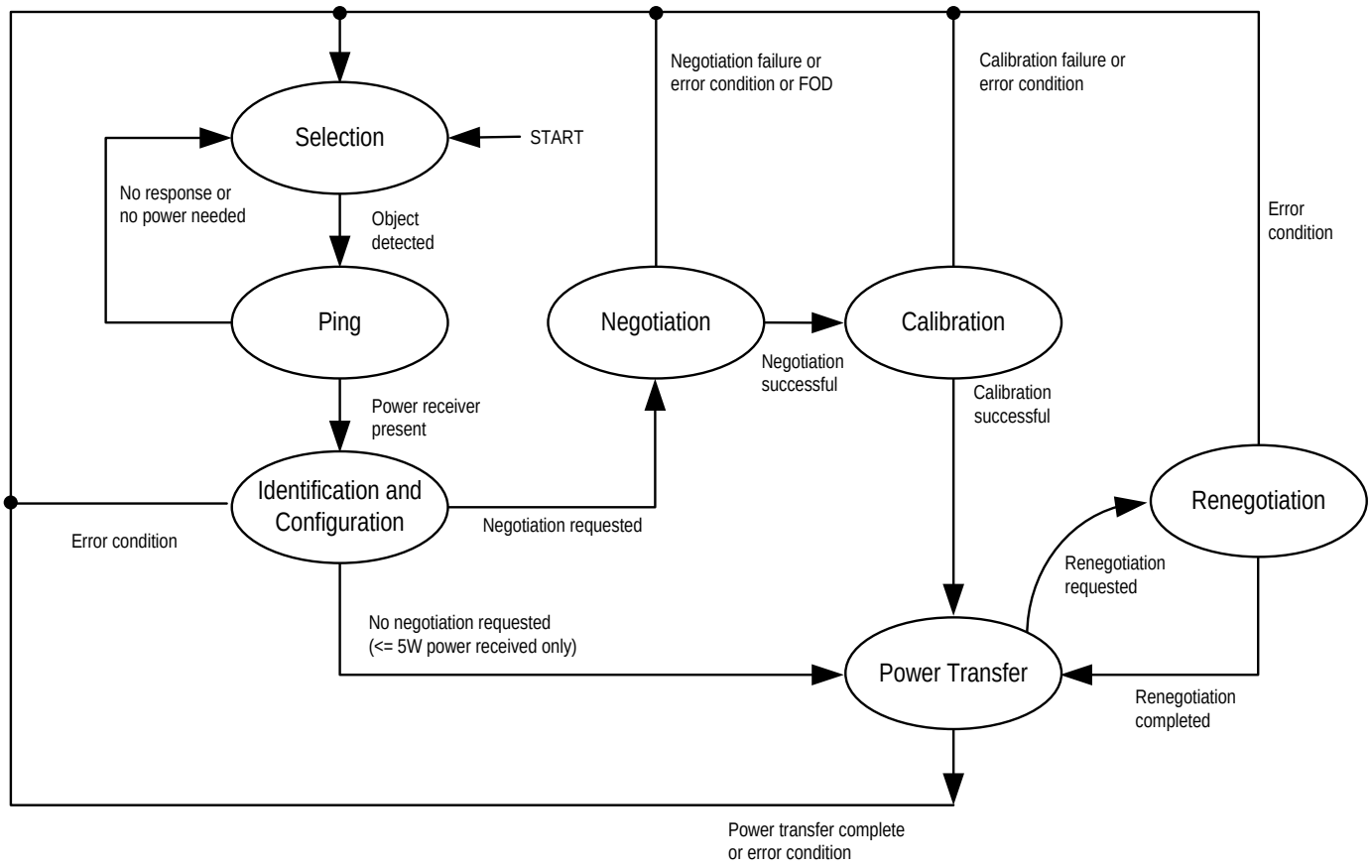
The P9243-GB supports constant and fixed frequency operation during power transfer. Under such application scenarios, the full-bridge input voltage is adjusted to control the P9243-GB transmitted power, while its operating frequency is fixed at 127.7 kHz. The accuracy depends on that of the external clock or oscillator. When using the Fixed-Frequency Operation Mode, an external step-down converter is employed in the P9243-GB reference design to control the input voltage of the full-bridge inverter. Thus, the output of the step-down buck regulator is connected to the input of the P9243-GB full-bridge inverter. A PWM signal from the P9243-GB is employed to control the output of the buck regulator by adjusting its duty ratio. To respond to an increase or decrease in the power request from receiver, the P9243-GB regulates the duty ratio of the PWM signal accordingly.

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8. WPC Mode Characteristics

The WPC-1.2.4 extended power profile wireless power specification has a Selection Phase, Ping Phase, Identification and Configuration Phase, Negotiation Phase, Calibration Phase, Power Transfer Phase, and Renegotiation Phase, as shown in Figure 16.

Figure 16. WPC Power-Transfer Phases Flow Chart



8.1 Selection Phase

In the Selection Phase, the power transmitter determines if it will proceed to the Ping Phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a measurement signal. This measurement signal is low level in order to not wake up a power receiver if it is positioned on the interface surface.

8.2 Ping Phase (Digital Ping)

In the Ping Phase, the power transmitter will start transmitting a power signal and will also detect the response from a possible power receiver. This response ensures that the power transmitter is linking to a power receiver rather than to some unknown object. When a WPC-compatible power receiver is placed on a WPC-compatible charging pad, it responds to the power signal by rectifying the power signal. When the receiver's internal bias voltage is greater than a specific threshold level, then the receiver is initiated, enabling the WPC communication protocol. If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the Identification and Configuration Phase, maintaining the power signal output to the receiver.

8.3 Identification and Configuration Phase

This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information in the Identification and Configuration Phase. The Identification and Configuration Phase is part of the WPC protocol so that the power transmitter and power receiver establish an initial default power transfer contract.

In the Configuration Phase, the power transmitter and receiver exchange information for a default power transfer contract as follows:

- The power transmitter receives the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), power receiver will assume a BPP transmitter is present.

8.4 Negotiation Phase

Under the scenario that both transmitter and receiver support the EPP, the Negotiation Phase will be initiated by the receiver to further fine-tune the default power contract established in the Configuration Phase. The power receiver sends negotiation requests to the power transmitter, such as general requests and specific requests, which the power transmitter can grant or deny. In addition, to improve its initial assessment of whether foreign objects are present, the power transmitter compares the quality factor reported by the power receiver with its own measurement. If the power transmitter detects a foreign object, it will return to the Selection Phase.

8.5 Calibration Phase

During the Calibration Phase, the power receiver provides information that the power transmitter can use to improve its accuracy to detect foreign objects during power transfer. The calibration can be divided into two different modes. Mode 1 is defined as light load calibration of the transmitted power and received power difference; Mode 2 is defined as the heavy load calibration of the power difference. If the transmitter does not send an ACK to the receiver in either Mode 1 or Mode 2, the receiver remains in the same mode and will not move on to the next stage.

8.6 Power-Transfer Phase

In this phase, the power transmitter and power receiver control the power transfer by means of the following packets:

- Control Error Packets (CEP)
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once a power contract is established, the transmitter initiates the Power Transfer Phase. The receiver`s control and communication circuit sends control error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator, and to send to the transmitter the actual received power packet for foreign-object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the receiving device, the receiver will send an EPT packet to the transmitter and the transmitter can terminate the existing power transfer.

9. Application Information

9.1 Internal Power Supply and Internal Bias

The P9243-GB has integrated internal buck regulators and internal LDOs to provide internal power.

9.1.1 Integrated Step-Down Regulator

To provide a power supply for the P9243-GB internal circuitry as well as to reduce the power loss from a wide input voltage range, a step down buck regulator is integrated. It is internally compensated for the convenience of design. It takes the power from the input voltage to the P9243-GB and regulates the DC voltage to 5V for use as an internal VCC_5V supply.

The internal step-down regulator supplies the power to the integrated MOSFET driver circuits, the internal LDO18, and the LDO33 linear regulators. It must not be used to power any external load.

9.1.2 Linear Regulators – PREG, LDO33, and LDO18

The P9243-GB has three low-dropout (LDO) regulators. The 5V pre-regulator (PREG) provides voltage for the internal bias. The PREG requires a 1µF ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The PREG voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal analog and digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1µF ceramic capacitor from the pin to GND. Both the LDO18 and LDO33 regulators must not be externally loaded.

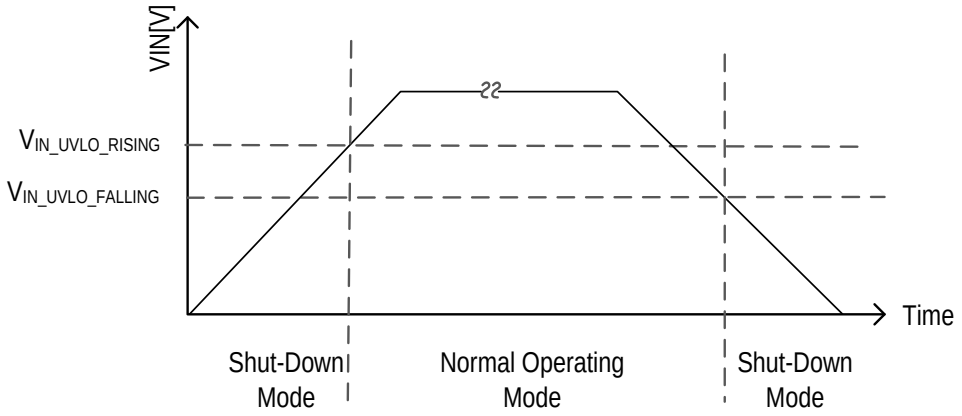
9.2 Enable Pin

The P9243-GB device can be disabled by applying a logic HIGH to the $\overline{EN}$ pin. When the voltage on the $\overline{EN}$ pin is pulled HIGH, operation is suspended and the P9243-GB is placed into the low-current Shut-Down Mode. If $\overline{EN}$ is pulled LOW, the P9243-GB is enabled and active. The rising and falling threshold for the $\overline{EN}$ is specified in Table 5.

9.3 Software Under-Voltage Lock-Out (UVLO) Protection

The P9243-GB has software UVLO features that protect the adaptor input port from being overloaded. For different adaptor voltages that are established, different UVLO levels are implemented. To guarantee proper functionality, the voltage on the VIN pin must be above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9243-GB shuts down the system. The thresholds can be configured using the P9243-GB Wireless Power Pro GUI.

Figure 17. UVLO Threshold Definition



9.4 Die Temperature Protection

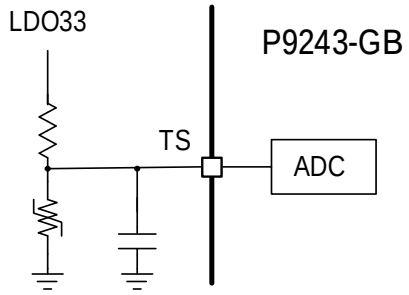
The P9243-GB integrates die thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds the threshold to prevent damage resulting from excessive thermal stress. An internal temperature protection block is enabled in the P9243-GB that monitors the temperature inside the chip.

If the die temperature exceeds 140°C, the P9243-GB shuts down and resumes when the internal temperature drops below 120°C.

9.5 External Temperature Sensing – TS

The P9243-GB has a remote temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. Figure 18 shows the temperature sensor circuits. Specific values for the thermistor and associated components are shown in Figure 28. Specific thermistor characteristics are included in the thermistor manufacturer's datasheet. The internal ADC compares the TS pin voltage to the threshold value, once the value goes below the threshold value, the P9243-GB will halt power transfer and the system will be notified in the system error register. The default threshold can be configured using the P9243-GB Wireless Power Pro GUI.

Figure 18. NTC Thermistor Connection to the TS Pin



To disable the thermistor, connect the TS pin to the LDO33 pin with a resistor. Do not leave the TS pin floating.

9.6 Full-Bridge Driver

The transmitter switching frequency and duty cycle are controlled by the two groups of half-bridge drivers with bootstrap diodes that have been integrated into the P9243-GB. Each driver is capable of driving a half bridge of two N-channel MOSFETs. The dead-time of each half-bridge can be set in the firmware to guarantee zero voltage switching as well as no risk of shoot-through. Each half-bridge driver can be controlled separately in the firmware, and thus the phase-shifted full-bridge or half-bridge can be enabled through the firmware.

The internal buck regulator provides 5V to both groups of half bridge driver circuits through the DRV_VIN pin. Applying any extra load on the internal buck regulator output is not recommended, since any extra load will compromise its loading capability and noise might be coupled into the half-bridge drivers.

9.7 LC Resonant Circuits

The LC resonant tank comprises a primary resonant coil (L_P) and series resonant capacitance (C_P). The LC resonant tank provides a resonant frequency at which it offers the minimum series resistance across the LC tank. The WPC-based transmitter is not specified to operate at the resonant frequency at any time.

The P9243-GB is designed to support various Baseline Power Profile (BPP) and Extended Power Profile (EPP) coil configurations using full-bridge inverter topologies to drive the primary coil (L_P) and series resonant capacitors (C_P). Depending on the WPC coil configuration and specification, the coil inductance and series capacitance value can vary in a wide range. The transmitter coil specification must comply with the WPC definition. The WPC specification defines the transmitter coil self-inductance value, DC resistance (DCR), Q-factor, form factor, size, and number of turns. For the EPP coil configurations, MP-A11 are supported by the P9243-GB. For each WPC-specified transmitter coil configuration, the required resonant capacitance is also defined. High-voltage-rated, multi-layer ceramic capacitors that feature stable AC and DC characteristics (such as the C0G type) and stable temperature characteristics are highly recommended for this application. For the WPC MP- A11 reference design, the Primary Coil and Shielding has a self-inductance is 6.3±10% µH. The value of the series capacitance is 500±5% nF.

9.8 WPC Communication Interface

9.8.1 Modulation/Communication

The WPC specification uses two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load applied to the receiver's coil; the communication is purely digital and logic 0s and 1s are modulated onto the power transfer signal waveform. Modulation is done with amplitude-shift keying (ASK) modulation with a bit-rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The power transmitter demodulates this variation of the coil voltage to receive the packets.

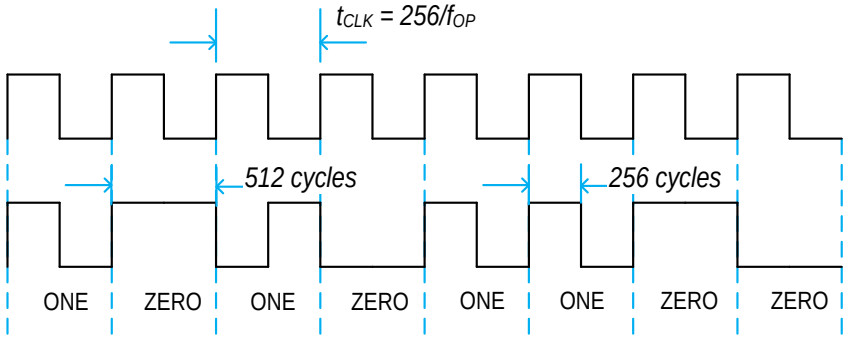
Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power transmitter P9243-GB has the capability to modulate FSK data onto the power transfer signal frequency and use it in order to establish the handshaking protocol with the power receiver.

9.8.2 Bit Decoding Scheme for FSK

The P9243-GB implements FSK communication when used in conjunction with WPC-compliant receivers, such as the P9221-R-EVK. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) of the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles.

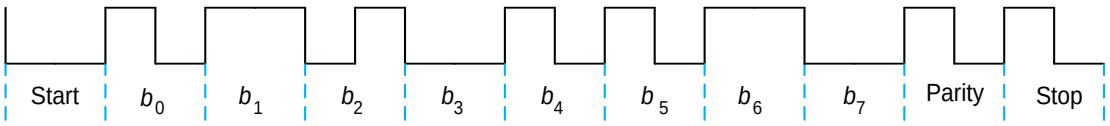
The FSK byte-encoding scheme and packet structure complies with the WPC specification revision 1.2.4. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit consists of 512 consecutive f_{MOD} cycles (or logic '0'). A logic 'ONE' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic 'ZERO' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 19. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 20:

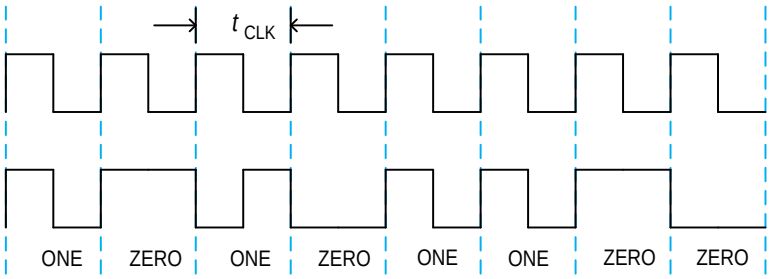
Figure 20. Example of Asynchronous Serial Byte Format for FSK



9.8.3 Bit Decoding Scheme for ASK

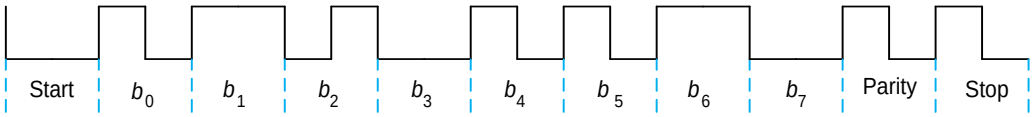
As required by the WPC specification, the P9243-GB uses a differential bi-phase coding scheme to demodulate the data bits from the power transfer signal. A frequency of 2kHz is used for this purpose. A logic ONE bit is coded using two narrow transitions; a logic ZERO bit is encoded using one wider transition as shown below in Figure 21.

Figure 21. Bit Decoding Scheme



Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 22.

Figure 22. Byte Decoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

Each ASK communication packet has the following structure as shown in Figure 23.

Figure 23. Communication Packet Structure

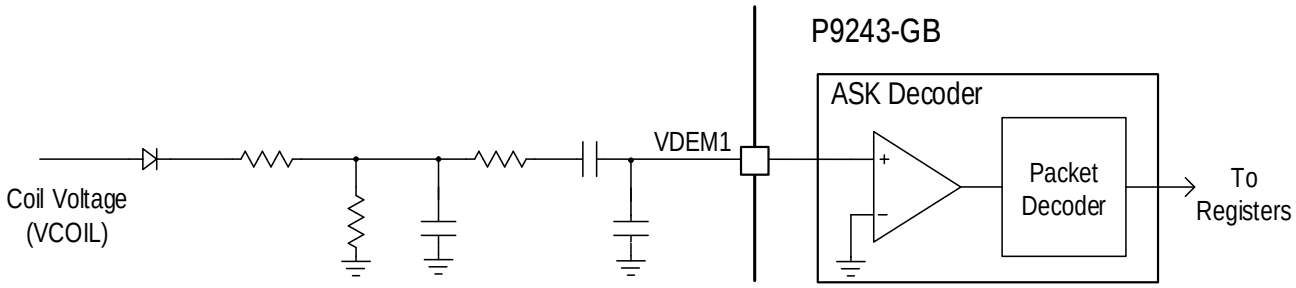
Preamble	Header	Message	Checksum

9.8.4 ASK Voltage Demodulation – VDEM1 Pin

In order to improve WPC ASK communication reliability under all loading conditions, the P9243-GB has integrated two demodulation schemes: one based on input current information and the other based on coil voltage information. During the ASK communication initialed by the receiver, the envelope of the transmitter coil voltage reflects the ASK communication packet. The communication packet can be received by tracking the envelope of the coil voltage.

The voltage mode envelope detector is implemented using a combination of an RC-based filter as depicted on Figure 24 below. This simple implementation achieves the envelope detector function by combining a low-pass filter.

Figure 24. Voltage Mode Envelope Detector



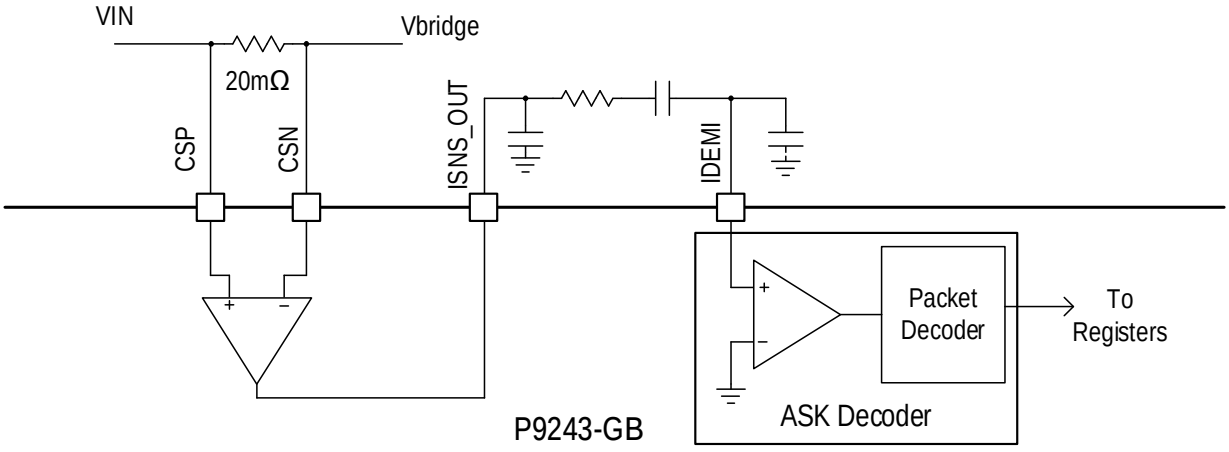
The filtered signal from the transmitter coil voltage will be processed by the P9243-GB internal ASK decoder circuit, which includes an operational amplifier to automatically condition the filtered signals, and then a digital packet decoder to translate the signal into communication packets.

9.8.5 ASK Current Demodulation – IDEMI Pin

The ASK current demodulation scheme receives input current information from the current sense resistor, which carries the coil current modulation information on top of the input current as shown in Figure 25. Similar to voltage demodulation circuits, an external discrete low-pass filter and DC filter between the ISNS_OUT and IDEMI pins provide additional filtering.

The packet decoder block is shared between the voltage and current detectors. The packet decoder selects either voltage information or current information from the filtered signals, depending upon which produces the better demodulated signal.

Figure 25. Current Mode Envelope Detector



9.9 General Purpose Input/output – GPIO Pins

The default GPIOs configuration is described in this section. The firmware can be used to repurpose some of the GPIOs to perform different functions.

9.9.1 Input Port Detection and Receiver Support – GPIO_A5, GPIO_A7, and GPIO_B8

The P9243-GB supports input voltages in a wide range, such as a 5V, 9V, 12V, and 16V to 19V fixed DC power supply. Depending on the reference design and WPC coil configuration selection, the device can support a variety of receivers based on the input voltage as shown in Table 6.

When an AC/DC adaptor is connected to the P9243-GB, it will detect if this is a USB port, based on the D+ and D- signals. In the case that a USB port is detected, the P9243-GB will identify the type of USB port by executing the USB Battery Charging (BC 1.2) protocol on the D+ and D- signals. The P9243-GB will assert a maximum of 12V when BC1.2 is detected. The device can adjust the input voltage to the highest level possible that enables as many receiver types as possible, as shown in Table 6. The GPIO_A5 and GPIO_A7 pins are used for D- detection and communication; GPIO_B8 is used for D+ detection and communication.

If the AC/DC adaptor is connected through a DC barrel jack or a fixed DC voltage, the P9243-GB will set up the operation mode and support the corresponding receivers listed in Table 6.

When the DC source is 5V fixed, the P9243-GB operates in the BPP Mode only and supports up to 5W. In this operation mode, the device disables the external power-stage buck regulator and enables an external MOSFET to bypass the buck regulator.

Table 6. Input Voltage vs. Receiver Supported with MPA11 Coil Configuration

Input Voltage/Current Rating	Receiver Supported
5V/2A	BPP (Bypass External Buck Regulator)
9V/1.67A	BPP 5W
	EPP, up to 8W
	Up to 7.5W charging for iPhones
12V/2A	BPP 5W
	EPP, up to 10W
	Samsung AFC
	Up to 7.5W charging for iPhones
15V to 19V/1.8A	BPP 5W
	EPP, up to 15W
	Samsung AFC
	Up to 7.5W charging for iPhones

9.9.2 Control of External Power Stage DC/DC Buck Regulator – GPIO_B4 and GPIO_B7

To regulate the receiver output voltage, as well as to regulate the system's delivered power, the transmitter adjusts the DC/AC inverter switching frequency, duty cycle, or DC/AC inverter input voltage. For the WPC coil configurations that operate at a fixed frequency and require adjusting the inverter bridge input voltage, the P9243-GB supports these coil configurations by employing an external front-end DC/DC stage. The external DC/DC is part of the power stage, which connects between the input voltage and the DC/AC inverter.

For Apple 7.5W charging mode, the P9243-GB supports fixed and precise switching frequency at 127.7kHz, and thus its bridge input voltage must be adjusted. Another stage of the external buck regulator is added to regulate the input voltage of the full bridge LC circuits. GPIO_B4 is employed to enable/disable this external DC/DC buck regulator. GPIO_B7 generates a PWM signal that is applied on top of the feedback pin of the buck regulator through a low-pass filter to fine-tune the output voltage of the buck regulator. The resolution of the buck regulator output depends on the buck IC's internal reference voltage, output voltage range, buck regulator compensation design, and resolution of the PWM signal from GPIO_B7.

9.9.3 Bypass External DC/DC Buck Regulator – GPIO_A4

When the input voltage is 5V only, the P9243-GB operates in the BPP Mode to support legacy adaptors, as shown in Table 6. However, enabling the external power stage buck regulator at this time compromises the efficiency, thermal performance, and maximum power that can be delivered to the receiver. Under such an application scenario, the P9243-GB will disable the external power stage buck regulator and enable another power path for the input voltage (5V) to be directly applied to the DC/AC inverter. GPIO_A4 is used to bypass the external power stage buck regulator. In this mode, the device operates in a mode for a fixed input voltage with variable frequency. The operating frequency range depends on the WPC coil configuration specification.

9.9.4 External Oscillator – GPIO_B5 and GPIO_B6

To guarantee that the operating frequency is precisely at 127.7kHz under different temperature conditions, the P9243-GB requires an external oscillator to provide accurate frequency operation. The PLL and crystal driver circuits inside the P9243-GB guarantee that the internal clock for the ARM® Cortex®-M0 core is synchronized with the external oscillator frequency.

An external 8MHz crystal needs to be connected between GPIO_B5 and GPIO_B6.

9.9.5 External Memory – GPIO_B0, GPIO_B1, GPIO_B2, and GPIO_B3

The P9243-GB has only a bootloader firmware function pre-programmed into the internal OTP memory. Therefore, the device must be used in conjunction with an external flash memory. Application firmware is loaded into the external flash for specific system requirements.

The P9243-GB fetches the application firmware from the external flash memory using an SPI interface and executes the code. Users can customize the firmware in external flash and load the new firmware in the flash via the P9243-GB I2C port. The Winbond W25X20CLUXIG is the recommended external flash memory to be used with the P9243-GB.

The P9243-GB application firmware provides extensive flexibility to customize operating parameters, such as Digital Ping Frequency, FOD parameters, coil over-temperature sensing, and over current limit. Based on the end application, the P9243-GB operating parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by creating a new user configuration HEX file that can be generated within the P9243-GB Wireless Power Pro GUI. Once the new user configuration HEX file is generated, the Flash memory can be erased and reprogramed using the P9243-GB Wireless Power Pro GUI.

9.9.6 Reserved – GPIO_A2 and GPIO_A3

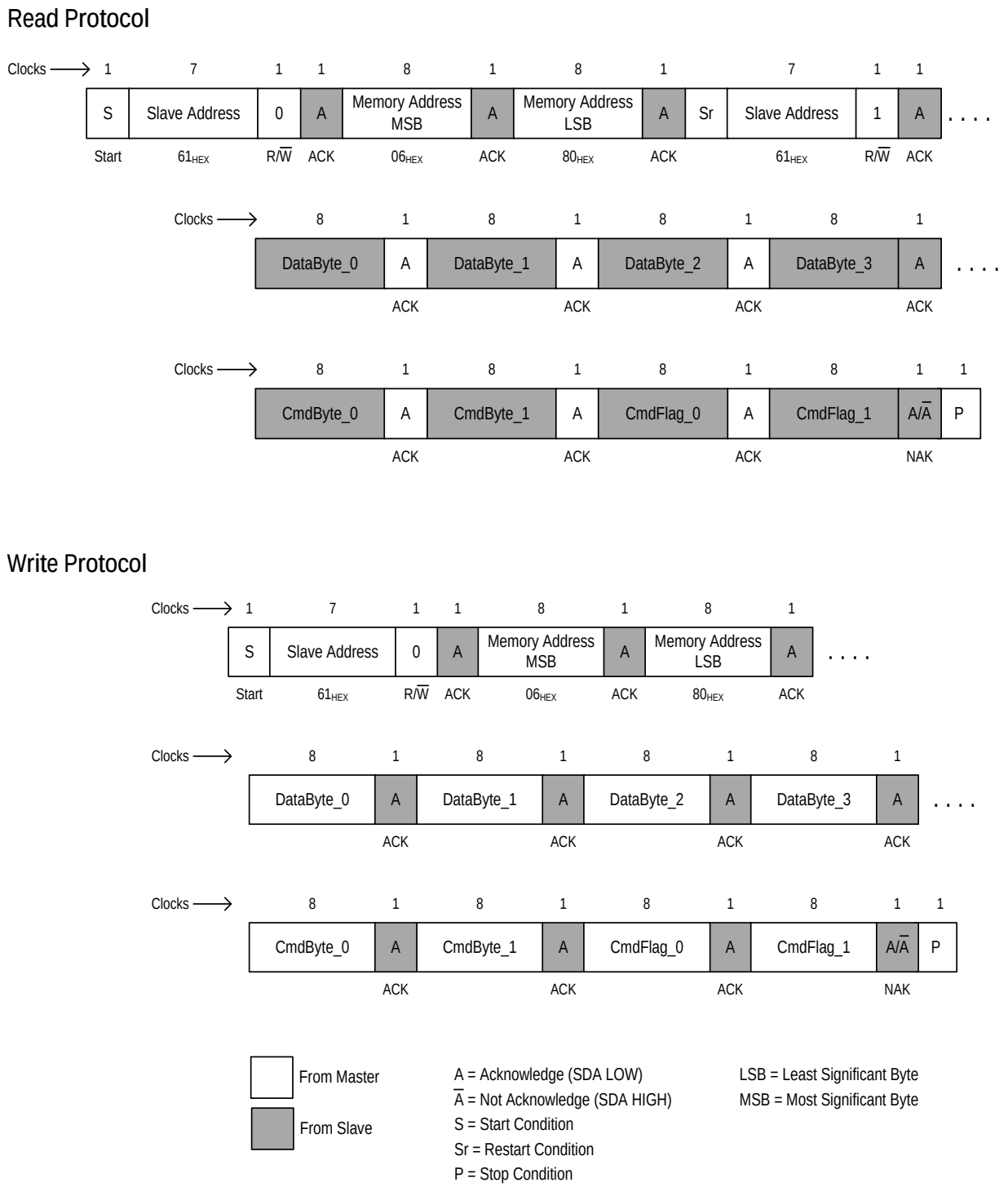
The GPIO_A2 (FOD_ADJ) and GPIO_A3 (LED_PATT) pin function is removed in the P9243-GB. Do not populate. Use the P9243-GB Wireless Power Pro GUI to adjust FOD parameters and LED pattern.

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9.9.7 I2C Communication Interface – GPIO_A0 and GPIO_A1

The P9243-GB supports the standard I2C interface. The default I2C slave address is 61_{HEX}. GPIO_A0 serves as the I2C clock line, and GPIO_A1 serves as the I2C data line. Figure 26 shows the READ and WRITE protocol structure that the external I2C master must use to communicate with the P9243-GB.

Figure 26. I2C Access Read Protocol and Write Protocol



9.10 LED Pattern Selection – LED1 and LED2

The P9243-GB uses two LED outputs to indicate the power transfer status, faults, and operating modes. The LEDs are connected to the LED1 and LED2 pins as shown in the typical application schematic in Figure 28. The LED pattern can be modified using the P9243-G Wireless Power Pro GUI.

9.11 Foreign Object Detection

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through such objects will cause a power loss and the metallic object will exhibit a temperature increase. The amount of heat generated is a function of the strength and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In a WPC-based wireless power system, the heat generated by the eddy current manifests itself as a power loss reducing the overall system efficiency. If appropriate actions are not taken, the heating could lead to unsafe conditions.

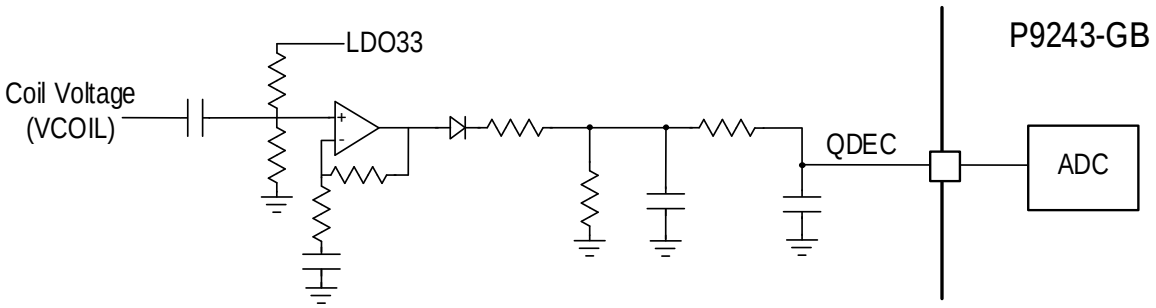
In the Extended Power Profile, there are two stages of foreign object detection (FOD). One stage is the measurement of the transmitter coil quality factor (Q-factor) prior to entering the Digital Ping Phase, and the other is a measurement of the power loss between the received power and the transmitted power during the Power Transfer Phase.

9.11.1 Quality Factor in the Digital Ping Phase

Prior to each digital ping, the P9243-GB detects and measures the coil's quality factor (Q-factor). If an EPP receiver is present, the transmitter compares its own measured Q-factor with the reference Q-factor provided by EPP receiver. If the measured Q-factor is lower than the calculated threshold based on the Receiver's reference Q-factor value, the P9243-GB will identify this situation as a WPC-defined FOD being present and cannot continue on to the Power Transfer Phase for the purpose of system protection. The default Q factor detection threshold can be adjusted using the P9243-GB Wireless Power Pro GUI.

The method implemented by P9243-GB to detect the Q-factor is completely based on the nature of the LC resonant circuit. The transmitter LC resonant tank is first charged by a low voltage DC source to ensure that the Rx will not be powered up by using a small amount of energy. Until there is no AC current flowing from the DC source to the LC tank, the DC source voltage will be removed and the LC tank will be shorted. The energy previously stored in the LC resonant tank circulates between the coil and capacitors and generates resonant ringing naturally. The frequency and envelope of the resonant ringing are directly related to the Q-factor. Thus, the Q-factor can be calculated by detecting the envelope of the ringing with the circuit in Figure 28. The default Q factor detection threshold can be changed using the P9243-GB Wireless Power Pro GUI.

Figure 27. Q-Factor Detection



9.11.2 Power Difference in the Power Transfer Phase

The second stage of the foreign object detection is achieved during the Power Transfer Phase. The power loss is calculated between the reported received power and the transmitted power, which is constantly measured and compared with the WPC-specified thresholds. In normal power transfers, the power difference between received power and transmitted power (power loss) is constantly lower than the pre-set threshold. However, if a foreign object has been placed on its surface and is able to be coupled with the magnetic flux, this can generate additional power loss, which can become significantly large. If the loss is higher than the threshold set by the WPC-specification, the power loss FOD protection mechanism will be triggered and the transmitter will shut down the whole system to avoid over-heating and a potentially unsafe situation.

The power loss can be different based on the component selection, PCB layout, and end-product casing. Therefore, it must be adjusted according to each design. The P9243-GB has a set of default power-loss FOD thresholds loaded in the firmware. It can be modified using P9243-GB Wireless Power Pro GUI.

10. Power Dissipation and Thermal Requirements

The P9243-GB is offered in a 48-pin VFQFPN package that has a maximum power dissipation capability of approximately 1.47W. The maximum power dissipation of the package is determined by the number of thermal vias between the package and the printed circuit board (PCB). The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C. The junction temperature rises when the heat generated by the device's power dissipation flow is impeded by the package-to-PCB thermal resistance.

The VFQFPN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 27.2°C/W when the PCB layout design is optimized as described in the *P9243-GB Layout Guide* document. The techniques noted in the PCB layout section must be followed when designing the printed circuit board layout. Take into consideration possible proximity to other heat-generating devices when placing the P9243-GB and the bridge FET packages in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, the size of the thermal pad attached to the die/package (VFQFPN), the thermal vias, and the final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

First, the maximum power dissipation for a given situation should be calculated using Equation 1:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{AMB})}{\theta_{JA}} \quad \text{Equation 1}$$

Where: $P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_{AMB} = Ambient temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9243-GB is 125°C. The thermal resistance of the 48-pin VFQFPN package is optimally θ_{JA} = 27.2°C/W. Operation is specified to a maximum steady-state ambient temperature (T_{AMB}) of 85°C. Therefore, the maximum recommended power dissipation is given by Equation 2.

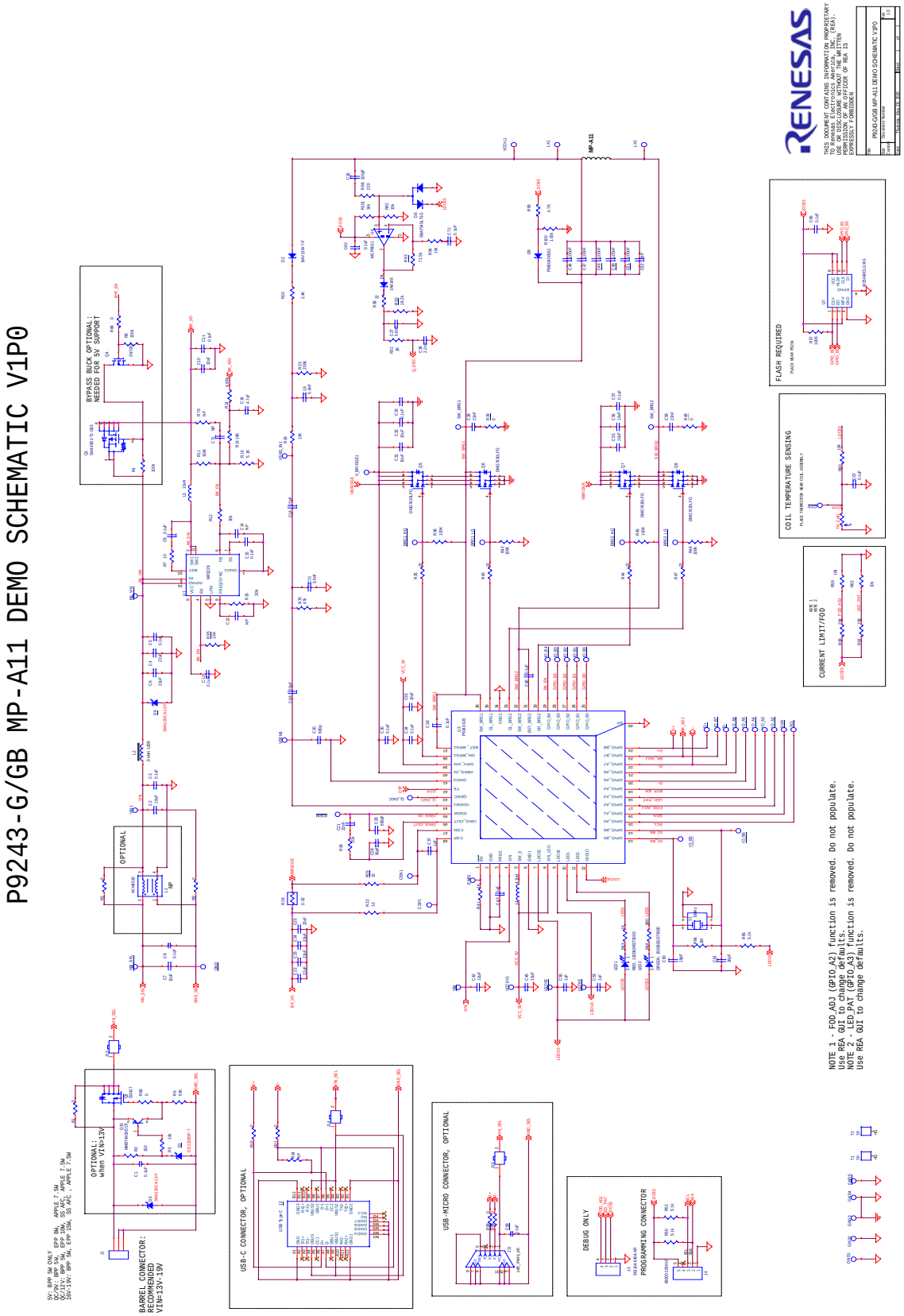
$$P_{D(MAX)} = \frac{(125℃ - 85℃)}{27.2℃/W} \cong 1.47W \quad \text{Equation 2}$$

All the previously mentioned thermal resistances are the values found when the P9243-GB is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

11. Typical Application Schematic

The typical application schematic provides a basic guideline for understanding and building a functional medium-power wireless power transmitter type MP-A11 as described in the WPC specifications. Other components, not shown on the typical application schematic might be needed in order to comply with other requirements, such as EMC/EMI or thermal specifications.

Figure 28. P9243-GB Typical Application Schematic v1.0



12. Bill of Materials (BOM)

Table 7. P9243-G-GB EVK BOM

Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
1	8	VIN1,GND1,GND2,GND3,GND4,VIN_SEL,GND,BK_VIN	TEST POINT PC MINIATURE SMT	TP	test_pt_sm_135x70	5015
2	38	V_BRIDGE1,VSNS_IN1,VDEM1,VCOIL1,SW_BRG1,IO_B1,ENB1,CSP1,CSN1,BRG1_LG,BRG1_HG,SW_BRG2,IO_B2,IO_A2,BRG2_LG,BRG2_HG,IO_B3,IO_A3,IO_B4,IO_A4,IO_B5,IO_A5,GND5,IO_B6,IO_A6,IO_B7,LDO18,LDO33,VCC5V1,VIN,SDA,SCL,Q_DEC,OTP,IO_B0,IDEM,D-,D+	30 GAUGE WIRE PAD	PTH_TP	TEST_PT30DPAD	NP
3	1	C1	CAP CER 0.1UF 25V X7R 0603	0.1uF	603	CC0603KRX7R8BB104
4	9	C2,C7,C31,C32,C35,C42,C45,C55,C56	CAP CER 10UF 25V X5R 0603	10uF	603	C1608X5R1E106M080AC
5	18	C3,C5,C8,C9,C11,C12,C15,C30,C33,C34,C38,C40,C46,C57,C66,C67,C68,C72	CAP CER 0.1UF 25V X7R 0402	0.1uF	402	CC0402KRX7R8BB104
6	7	C4,C6,C10,C22,C23,C24,C25	CAP CER 22UF 25V X5R 0805	22uF	805	GRM21BR61E226ME44L
7	4	C13,C14,R24,C71	NP	NP	402	NP
8	1	C16	CAP CER 4.7UF 16V X5R 0402	4.7uF	402	CL05A475MO5NUNC
9	2	C18,C69	CAP CER 0.022UF 50V X7R 0603	22nF	603	GCJ188R71H223KA01D
10	2	C19,C70	CAP CER 5600PF 50V X7R 0603	5.6nF	603	CC0603KRX7R9BB562
11	1	C20	CAP CER 680PF 50V X7R 0402	680p	402	CL05B681KB5NNNC
12	1	C21	CAP CER 0.022UF 25V X7R 0402	22nF	402	GRM155R71E223JA61D
13	1	C26	CAP CER 220PF 50V X7R 0603	220pF	603	CC0603JRX7R9BB221
14	1	C27	CAP CER 5600PF 16V X7R 0402	5.6nF	402	CC0402KRX7R7BB562
15	1	C28	CAP CER 56PF 50V C0G/NP0 0402	56pF	402	CL05C560JB5NNNC
16	1	C29	CAP CER 680PF 50V X7R 0402	680pF	402	CL05B681KB5NNNC
17	1	C36	CAP CER 2200PF 10V X7R 0402	2.2nF	402	CC0402KRX7R6BB222
18	4	C37,C43,C50,C53	CAP CER 1UF 25V X5R 0402	1uF	402	CGB2A1X5R1E105M033BC
19	2	C39,C59	CAP CER 0.022UF 50V X7R 0603	22nF	603	CL10B223KB8NNNC

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Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
20	5	C44,C47,C48,C49,C51	CAP CER 100nF 100V C0G 1206	100nF	1206	C3216C0G2A104K160AC
21	1	C52	NP	NP	1206	NP
22	2	C60,C61	CAP CER 18pF 50V 5% C0G/NP0 0402	18pF	402	GRM1555C1H180JA01D
23	1	D1	DIODE ZENER 20V 500MW SOD323F	DDZ20BSF-7	sod123	DDZ20BSF-7
24	1	D2	DIODE GEN PURP 200V 200MA SOD123	BAV21W-7-F	sod123	BAV21W-7-F
25	1	D4	DIODE GEN PURP 75V 150MA SOD323	1N4148	sod-323	1N4148WX-TP
26	2	D5,D6	TVS DIODE 20V 32.4V SMA	SMAJ20CA-13-F	SMAJ20CA	SMAJ20CA-13-F
27	1	D8	DIODE ARRAY SCHOTTKY 30V SOT23-3	SBAT54SLT1G	SOT-23	SBAT54SLT1G
28	1	D9	SHTKY DIODE PURP 200V 500MA	PMEG4005EJ	SOD323F	PMEG4005EJ
29	1	J1	CONN PWR JACK 2.5X5.5MM SOLDER	AC_Adapter	CONN_POWER_JACK5_5MM	PJ-002AH
30	1	J2	CONN RCP USB3.1 TYPEC 24P SMD RA	USB Type C	USB-C12401610E4	12401610E4#2A
31	1	J3	4 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold or Gold, GXT™	961104-6404-AR	sip-4	961104-6404-AR
32	1	J4	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sip5	68000-105HLF
33	1	J11	CONN RCPT USB2.0 MICRO AB SMD RA	ZX62D-AB-5P8(30)	usb_micro_ab	ZX62D-AB-5P8(30)
34	3	J13,J14,J15	CONN HEADER VERT 2POS 2.54MM	JMP	sip2	68000-102HLF
35	1	LED1	LED RED CLEAR 0603 SMD	RED, 150060RS75000	0603_diode	150060RS75000
36	1	LED2	LED GREEN CLEAR 0603 SMD	GREEN, 150060GS75000	0603_diode	150060GS75000
37	2	LX1,LX2	30 GAUGE WIRE PAD	PTH_TP	TP_TXCoil	NP
38	1	L1	Common mode EMI choke	ACM4520	EMI_TDK_ACM4520L	ACM4520-901-2P-T-000
39	1	L2	RES SMD 0 OHM JUMPER 1/4W 1206	Zero ohm	0 ohm 1206	RC1206JR-070RL
40	1	L3	29mOhm, 3.6A inductor	10uH	5x5-10x10	SWPA8040S100MT
41	1	L4	FIXED IND 4.7UH 620MA 550 MOHM	4.7uH	L0603	LQM18PN4R7MFRL

Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
42	1	Q1	MOSFET P-CH 30V 12A SC70-6	SIA449DJ-T1-GE3	sc70_6ld_fet	SIA449DJ-T1-GE3
43	1	Q2	P-Channel 30 V , 35mOhm, 15nC MOSFET	Si3417	SOT-23-6	Si3417DV-T1-GE3
44	1	Q4	N-Channel 60-V (D-S) MOSFET	2N7002	SOT23_3	2N7002KT1G
45	4	Q5,Q6,Q7,Q8	MOSFET N-CH 30V 10.5A PWRDI3333	DMG7430LFG	powerdi3333_8ld_fet	DMG7430LFG-7
46	1	Q10	TRANS PNP 40V 0.6A SOT-23	MMBT4403/SOT	SOT-23	MMBT4403LT3G
47	3	R1,R2,R9	RES SMD 0.0 OHM JUMPER 1/4W 1206	0	1206	RC1206JR-070R
48	1	R3	RES SMD 150 OHM 1% 1/10W 0603	150	603	RC0603FR-07150RL
49	2	R4,R8	RES SMD 100K OHM 1% 1/16W 0402	100k	402	RC0402FR-07100KL
50	7	R5,R19,R59,R60,R61,R82,R94	RES SMD 10K OHM 1% 1/16W 0402	10k	402	RC0402FR-0710KL
51	1	R6	RES SMD 91K OHM 1% 1/16W 0402	91K	402	RC0402FR-0791K
52	2	R7,R25	RES SMD 10 OHM 1% 1/16W 0402	10	402	RC0402FR-0710RL
53	1	R11	RES SMD 150K OHM 1% 1/16W 0402	150K	402	RC0402FR-07150K
54	2	R12,R15	RES SMD 30K OHM 1% 1/16W 0402	30k	402	RC0402FR-0730KL
55	1	R13	RES SMD 18K OHM 1% 1/10W 0402	18K	402	ERJ-2RKF1802X
56	1	R14	RES SMD 4.99K OHM 1% 1/16W 0402	4.99k	402	RC0402FR-074K99L
57	4	R16,R50,R52,R85	RES SMD 5.1K OHM 1% 1/16W 0402	5.1k	402	RC1005F512CS
58	8	R18,R21,R39,R49,R68,R69,R80,R88	RES SMD 0 OHM JUMPER 1/16W 0402	0	402	RC0402JR-070RL
59	1	R20	RES SMD 2.4K OHM 1% 1/10W 0603	2.4K	603	RC0603FR-072K4L
60	1	R22	RES SMD 10 OHM 1% 1/16W 0402	10	402	RC0402FR-0710RL
61	1	R23	RES SMD 200K OHM 1% 1/10W 0603	200K	603	RC1608F204CS
62	1	R26	RES SMD 0.02 OHM 1% 1/3W 0805	0.02	805	UCR10EVHFSR020
63	2	R28,R62	RES SMD 10K OHM 1% 1/16W 0402	10k	402	RC0402FR-0710KP
64	1	R30	RES SMD 18.2K OHM 1% 1/16W 0402	18.2k	402	RC0402FR-0718K2L
65	1	R31	RES SMD 2K OHM 1% 1/16W 0402	2K	402	RC0402FR-072KL
66	4	R35,R40,R44,R47	RES SMD 22 OHM 5% 1/10W 0402	22	402	ERJ-2GEJ220X
67	5	R36,R42,R45,R48,R57	RES SMD 100K OHM 5% 1/10W 0402	100K	402	ERJ-2GEJ104X

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Item	QTY	Reference	Description	Value	PCB Footprint	Part Number
68	1	R38	RES SMD 22 OHM 1% 1/16W 0402	22	402	RC0402FR-0722RL
69	2	R41,R43	RES SMD 1K OHM 5% 1/16W 0402	1K	402	RC0402JR-071KL
70	1	R46	RES SMD 680 OHM 5% 1/16W 0402	680	402	RC0402JR-07680RL
71	1	R58	RES SMD 20K OHM 0.1% 1/16W 0402	20K	402	RT0402BRD0720KL
72	1	R70	RES SMD 47K OHM 1% 1/10W 0603	47k	603	RC0603FR-0747KL
73	1	R79	RES SMD 51k 1% 1/16W 0402	NP	402	RC0402FR-0751KL
74	1	R84	RES SMD 1M OHM 1% 1/16W 0402	1M	402	RC0402FR-071ML
75	1	R93	RES SMD 71.5K OHM 1% 1/16W 0402	71.5k	402	RC0402FR-0771K5L
76	1	R95	RES SMD 10K OHM 1% 1/10W 0402	10K	402	RC0402FR-0710KL
77	1	R98	RES SMD 220 OHM 1% 1/16W 0402	220	402	AC0402FR-07220RL
78	1	R99	RES SMD 4.7K OHM 1% 1/16W 0402	4.7K	402	RC0402FR-074K7L
79	1	R100	RES SMD 1.05K OHM 1% 1/16W 0402	1.05k	402	RC0402FR-071K05L
80	1	R101	RES SMD 34K OHM 1% 1/16W 0402	34k	402	RC0402FR-0734KL
81	1	TH_Coil1	NTC Thermistor 10k Bead	NP	805	NTCLE203E3103JB0
82	1	T1		TP	8x250unplated	
83	1	T2		TP	8x320unplated	
84	1	U1	Buck Converter Chip, QFN-14 (3X3)	MP2229	MP_2229	MP2229GQ
85	1	U3	Medium Power Transmitter	P9243-GB	socketqfn_48_6x6_0p4	P9243-GB
86	1	U4	1.7~5.5V input, 10MHz R2R OPA	MCP6021	SOT23-5	MCP6021T-E/OT
87	1	U7	SPIFLASH 4M-BIT 4KB UNIFORM SECT	W25X40CLUXIG	uson_2x3_8LD	W25X40CLUXIG
88	1	Y1	8MHz Crystal Oscillator	8MHz	ECX-53B	ECS-80-18-30B-AGN-TR

13. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

13.1 Special Notes: P9243-GB 48-VFQFPN Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours prior to the assembly reflow process.

14. Marking Diagram



- Line 1: Company name and part number.
- Line 2: -GB is part of the part number, which is followed by the package code.
- Line 3: “YYWW” is the last two digits of the year and two digits for the week that the part was assembled; # is the device step; “$” denotes the mark code.

15. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Ambient Temperature
P9243-GBNDGI[a]	P9243-GB Wireless Power Transmitter for 15W Applications with only bootloader pre-programmed, 48-VFQFPN (6 × 6 mm) package	MSL3	Tray	-40°C to +85°C
P9243-GBNDGI8[a]	P9243-GB Wireless Power Transmitter for 15W Applications with only bootloader pre-programmed, 48-VFQFPN (6 × 6 mm) package	MSL3	Reel	-40°C to +85°C

[a] The P9243-GB has only the bootloader firmware pre-programmed into the internal one-time programmable (OTP) memory. The device must be used in conjunction with an external Winbond W25X20CLUXIG flash. For a sizeable business opportunity, the application firmware can also be loaded into the internal one-time programmable (OTP) memory and external flash memory can be removed. For more information, contact the Renesas sales team or your distributor.

16. Revision History

Revision Date	Description of Change
July 7, 2020	Initial release.