NX5P2924C

Logic controlled high-side power switch

Rev. 1 — 7 July 2015 Product data sheet

1. General description

The NX5P2924C is a high-side load switch which features a low ON resistance N-channel MOSFET with controlled slew rate that supports 2.5 A of continuous current. Designed for operation from 0.8 V to 5.5 V, it is used in power domain isolation applications to reduce power dissipation and extend battery life. An output pull-down transistor has been integrated for fast discharge of capacitive load. The enable logic includes integrated logic level translation making the device compatible with lower voltage processors and controllers. The NX5P2924C is ideal for portable, battery operated applications due to low ground current.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 5.5 V
- Very low ON resistance:
  - 18 mΩ (typical) at a supply voltage of 1.2 V
  - 18 mΩ (typical) at a supply voltage of 1.8 V
- High noise immunity
- High current handling capability (2.5 A continuous current)
- Reverse current protection
- Turn-on slew rate limiting
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5000 V
  - CDM AEC-Q100-011 revision B exceeds 1000 V
- Specified from −40 °C to +85 °C

3. Applications

- Cell phone
- Digital cameras and audio devices
- Portable and battery-powered equipment

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5P2924CUK	–40 °C to +85 °C	WLCSP6	wafer level chip-scale package; 6 bumps; 0.87 × 1.37 × 0.5 mm	NX5P2924C

5. Marking

Table 2. Marking codes

Type number	Marking code
NX5P2924CUK	4C

6. Functional diagram

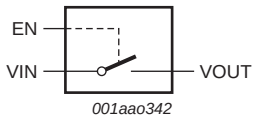


Fig 1. Logic symbol

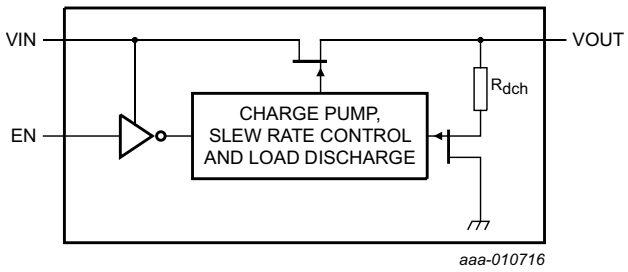


Fig 2. Logic diagram

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7. Pinning information

7.1 Pinning

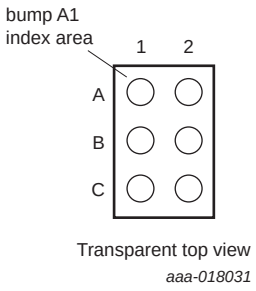


Fig 3. Pin configuration for WLCSP6

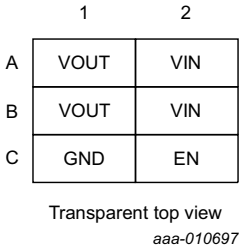


Fig 4. Ball mapping for WLCSP6

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VIN	A2, B2	input voltage
GND	C1	ground (0 V)
EN	C2	enable input (active HIGH)
VOUT	A1, B1	output voltage

8. Functional description

Table 4. Function table[1]

Input EN	Switch
L	switch OFF
H	switch ON

[1] H = HIGH voltage level; L = LOW voltage level.

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9. Application diagram

The NX5P2924C is typically used in portable, battery operated device. Pin EN enables the NX5P2924C. Slew rate controlled in-rush current reduction circuits function during switching.

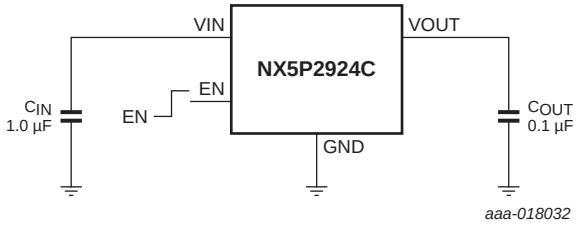


Fig 5. NX5P2924C application diagram

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10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	input EN [1]	−0.5	+6.0	V
		input VIN [2]	−0.5	+6.0	V
V_{SW}	switch voltage	output VOUT [2]	−0.5	$V_{I(VIN)}$	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V	−50	-	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V	−50	-	mA
		output VOUT: $V_{O(VOUT)} < -0.5$ V	−50	-	mA
		output VOUT: $V_{O(VOUT)} > V_{I(VIN)} + 0.5$ V	-	50	mA
I_{SW}	switch current	$V_{SW} > -0.5$ V	-	±2500	mA
		pulsed, 100 ms pulse, 2 % duty cycle	-	±5000	mA
$T_{j(max)}$	maximum junction temperature		−40	+125	°C
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	[3]	-	470	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	input EN	0	5.5	V
		input VIN	0.8	5.5	V
T_{amb}	ambient temperature		−40	+85	°C

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12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	139	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure that all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13. Static characteristics

Table 8. Static characteristics

$V_{I(VIN)}$ = 1.0 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	EN input; $V_{I(VIN)}$ = 0.8 V	0.6	-	-	0.6	-	V
		EN input; $V_{I(VIN)}$ = 1.0 V to 1.2 V	0.9	-	-	0.9	-	V
		EN input; $V_{I(VIN)}$ = 1.2 V to 2.5 V	1.2	-	-	1.2	-	V
		EN input; $V_{I(VIN)}$ = 2.5 V to 5.5 V	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	EN input; $V_{I(VIN)}$ = 0.8 V	-	-	0.25	-	0.25	V
		EN input; $V_{I(VIN)}$ = 1.0 V to 1.2 V	-	-	0.3	-	0.3	V
		EN input; $V_{I(VIN)}$ = 1.2 V to 2.5 V	-	-	0.4	-	0.4	V
		EN input; $V_{I(VIN)}$ = 2.5 V to 5.5 V	-	-	0.6	-	0.6	V
I_I	input leakage current	EN input; $V_{I(EN)}$ = 0.9 V to 5.5 V	-	-	-	-	0.1	µA
R_{dch}	discharge resistance	VOUT output; $V_{I(VIN)}$ = 0.8 V	-	4.00	-	-	-	kΩ
		VOUT output; $V_{I(VIN)}$ = 1.0 V	-	1.40	-	-	-	kΩ
		VOUT output; $V_{I(VIN)}$ = 1.2 V	-	1.30	-	-	-	kΩ
		VOUT output; $V_{I(VIN)}$ = 1.8 V	-	1.27	1.50	-	-	kΩ
		VOUT output; $V_{I(VIN)}$ = 3.3 V	-	1.25	1.50	-	-	kΩ
		VOUT output; $V_{I(VIN)}$ = 5.5 V	-	1.25	1.50	-	-	kΩ
I_{DD}	supply current	VOUT open						
		EN = HIGH; $V_{I(VIN)}$ = 1.0 V; see Figure 6 and Figure 7	-	35	-	-	50	µA
		EN = HIGH; $V_{I(VIN)}$ = 1.8 V; see Figure 6 and Figure 7	-	35	-	-	50	µA
		EN = HIGH; $V_{I(VIN)}$ = 3.6 V; see Figure 6 and Figure 7	-	50	-	-	70	µA
		EN = HIGH; $V_{I(VIN)}$ = 5.5 V; see Figure 6 and Figure 7	-	85	-	-	110	µA
		EN = LOW; see Figure 8 and Figure 9	-	0.1	-	-	1.5	µA

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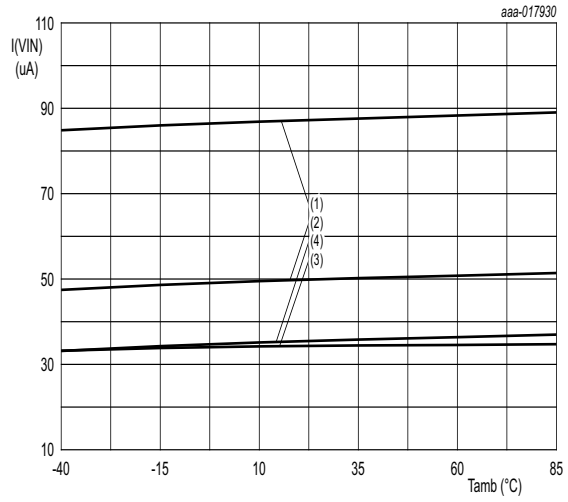
Table 8. Static characteristics *…continued*

$V_{I(VIN)}$ = 1.0 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V). …continued

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	EN = LOW; $V_{I(VIN)}$ = 1.8 V; $V_{I(VOUT)}$ = 0 V; see Figure 10 and Figure 11	-	–0.5	-	–3.5	-	µA
		EN = LOW; $V_{I(VIN)}$ = 3.6 V; $V_{I(VOUT)}$ = 0 V; see Figure 10 and Figure 11	-	–0.5	-	–5.0	-	µA
		EN = LOW; $V_{I(VIN)}$ = 5.5 V; $V_{I(VOUT)}$ = 0 V; see Figure 10 and Figure 11	-	–0.5	-	–7.5	-	µA
C_I	input capacitance	EN	-	3	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	VIN; VOUT	-	-	0.5	-	0.5	nF

[1] All typical values are measured at $V_{I(VIN)}$ = 3.6 V and T_{amb} = 25 °C unless otherwise specified.

13.1 Graphs



$V_{I(EN)}$ = $V_{I(VIN)}$.

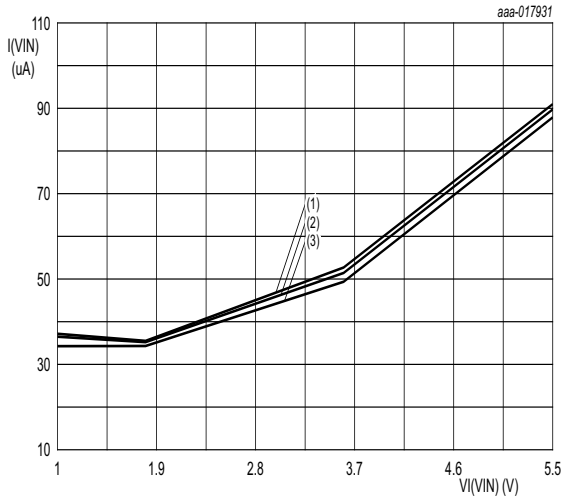
(1) $V_{I(VIN)}$ = 5.5 V.

(2) $V_{I(VIN)}$ = 3.6 V.

(3) $V_{I(VIN)}$ = 1.8 V.

(4) $V_{I(VIN)}$ = 1.0 V.

Fig 6. Typical supply current versus temperature



$V_{I(EN)}$ = $V_{I(VIN)}$.

(1) T_{amb} = +85 °C.

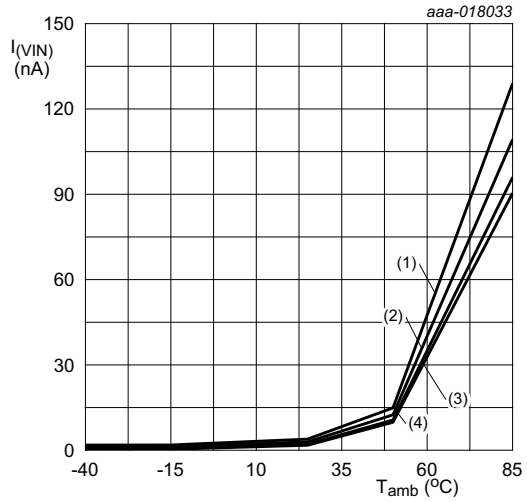
(2) T_{amb} = +25 °C.

(3) T_{amb} = –40 °C.

Fig 7. Typical supply current versus input voltage on pin VIN

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$V_{I(EN)}$ = GND.

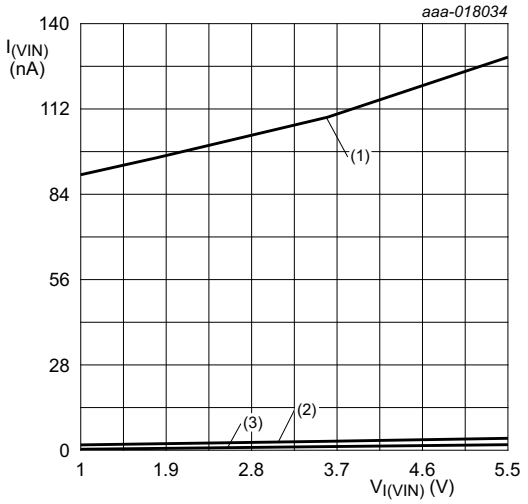
(1) $V_{I(VIN)}$ = 5.5 V.

(2) $V_{I(VIN)}$ = 3.6 V.

(3) $V_{I(VIN)}$ = 1.8 V.

(4) $V_{I(VIN)}$ = 1.0 V.

Fig 8. Typical supply current versus temperature



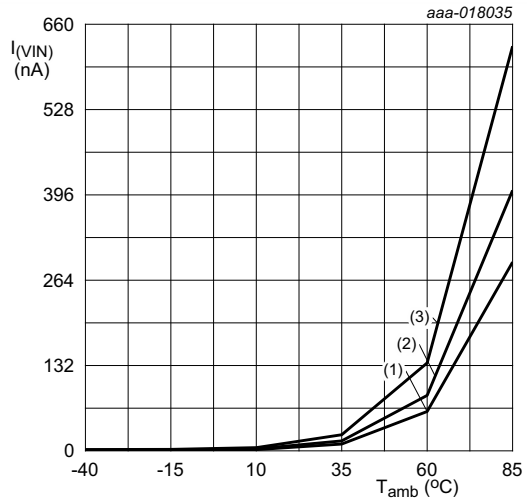
$V_{I(EN)}$ = GND.

(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = −40 °C.

Fig 9. Typical supply current versus input voltage on pin VIN

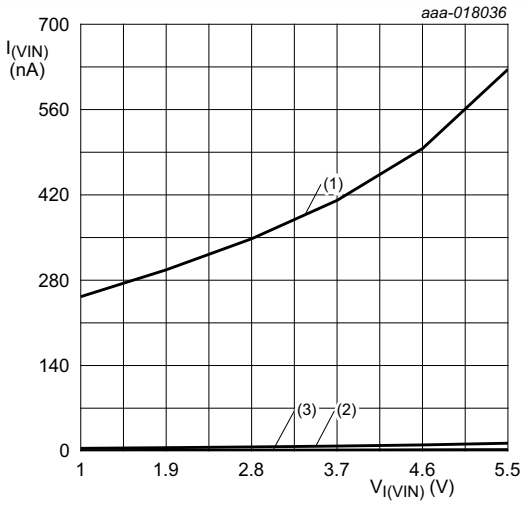


(1) $V_{I(VIN)}$ = 1.8 V.

(2) $V_{I(VIN)}$ = 3.6 V.

(3) $V_{I(VIN)}$ = 5.5 V.

Fig 10. Typical OFF-state leakage current versus temperature



(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = −40 °C.

Fig 11. Typical OFF-state leakage current versus input voltage on pin VIN

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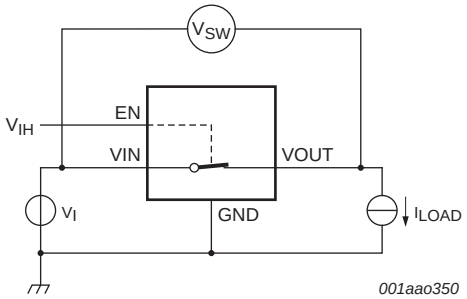
13.2 ON resistance

Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

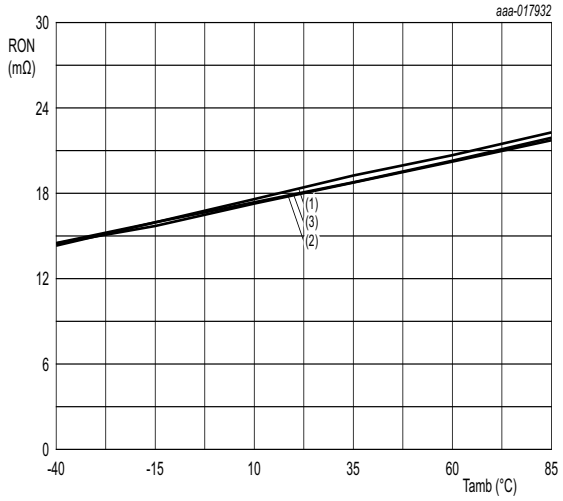
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	$V_{I(EN)}$ = 1.5 V; I_{LOAD} = 200 mA; see Figure 12, 13 and 14						
		$V_{I(VIN)}$ = 0.8 V	-	21	-	-	26	mΩ
		$V_{I(VIN)}$ = 0.9 V	-	19	-	-	24	mΩ
		$V_{I(VIN)}$ = 1.0 V to 5.5 V	-	18	-	-	23	mΩ

13.3 ON resistance test circuit and graphs



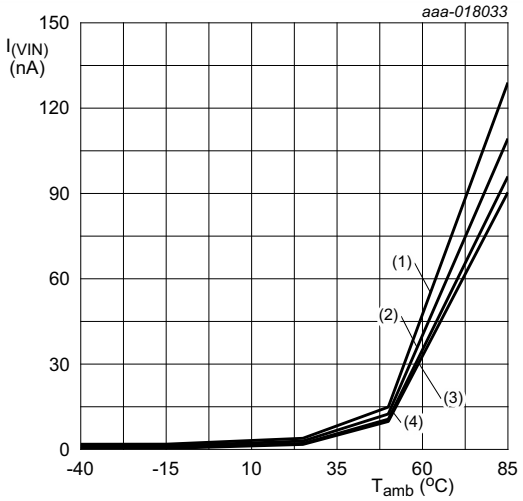
$R_{ON} = V_{SW} / I_{LOAD}$.

Fig 12. Test circuit for measuring ON resistance



(1) $V_{I(VIN)}$ = 1.0 V.
(2) $V_{I(VIN)}$ = 3.6 V.
(3) $V_{I(VIN)}$ = 5.5 V.

Fig 13. ON resistance versus temperature



(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig 14. ON resistance versus input voltage

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14. Dynamic characteristics

Table 10. Dynamic characteristics

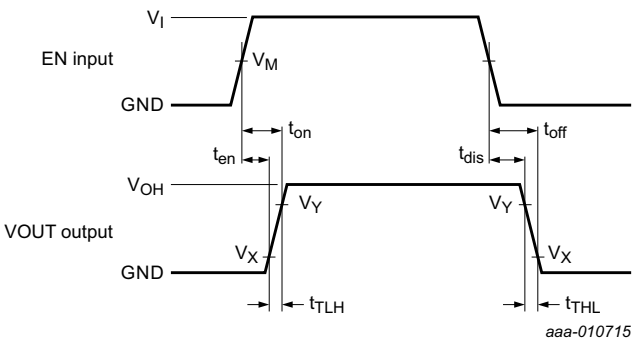
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 16.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	EN to VOUT; see Figure 15, 17, 18 and 19						
		$V_{I(VIN)}$ = 0.8 V	-	630	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	530	-	270	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	510	-	330	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	510	-	350	-	µs
t_{dis}	disable time	EN to VOUT; see Figure 15 and 20						
		$V_{I(VIN)}$ = 0.8 V	-	90	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	18	-	-	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	4	-	-	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	3	-	-	-	µs
t_{on}	turn-on time	EN to VOUT; see Figure 15, 17, 18 and 19						
		$V_{I(VIN)}$ = 0.8 V	-	990	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	940	-	520	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	1290	-	830	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	1480	-	1020	-	µs
t_{off}	turn-off time	EN to VOUT; see Figure 15 and 20						µs
		$V_{I(VIN)}$ = 0.8 V	-	100	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	20	-	-	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	6	-	-	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	5	-	-	-	µs
t_{TLH}	LOW to HIGH output transition time	VOUT; see Figure 15						
		$V_{I(VIN)}$ = 0.8 V	-	360	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	410	-	160	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	780	-	430	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	970	-	590	-	µs
t_{THL}	HIGH to LOW output transition time	VOUT; see Figure 15						
		$V_{I(VIN)}$ = 0.8 V	-	5	-	-	-	µs
		$V_{I(VIN)}$ = 1.0 V	-	2.2	-	-	-	µs
		$V_{I(VIN)}$ = 3.6 V	-	2.2	-	-	-	µs
		$V_{I(VIN)}$ = 5.5 V	-	2.2	-	-	-	µs

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14.1 Waveforms, graphs and test circuit



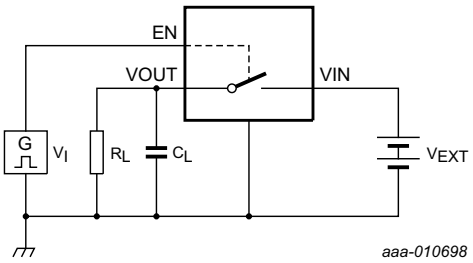
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 15. Switching times

Table 11. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
1.0 V to 5.5 V	$0.5 \times V_{I(EN)}$	$0.1 \times V_{OH}$	$0.9 \times V_{OH}$



Test data is given in Table 12.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

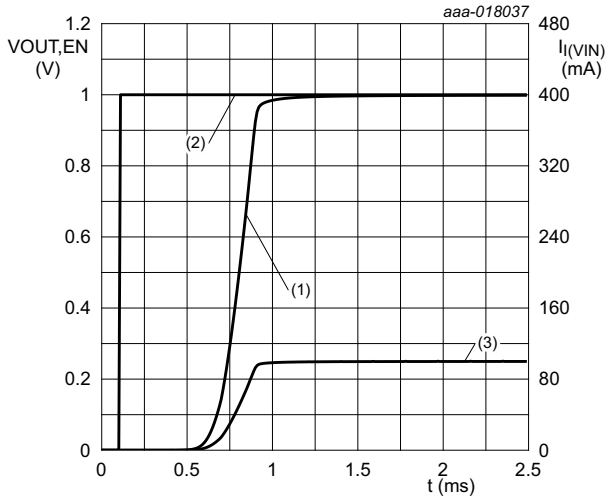
Fig 16. Test circuit for measuring switching times

Table 12. Test data

Supply voltage	Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
1.0 V to 5.5 V	1.5 V	0.1 µF	10 Ω

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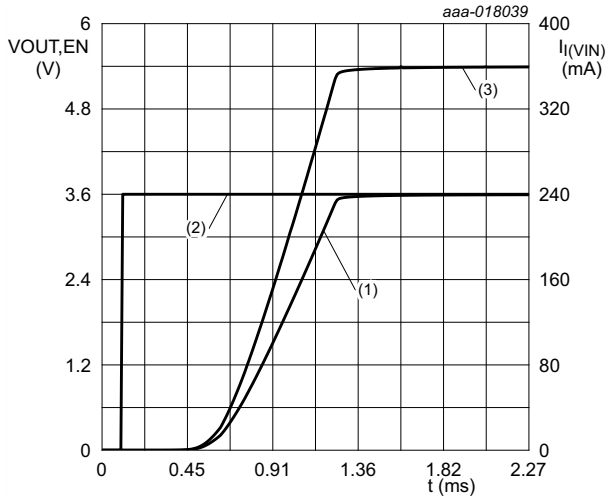
$V_{I(VIN)}$ = 1 V; R_L = 10 Ω; C_L = 0.1 µF; T_{amb} = 25 °C.

(1) VOUT

(2) EN

(3) $I_{I(VIN)}$

Fig 17. Typical enable time at $V_{I(VIN)}$ = 1 V; C_L = 0.1 µF



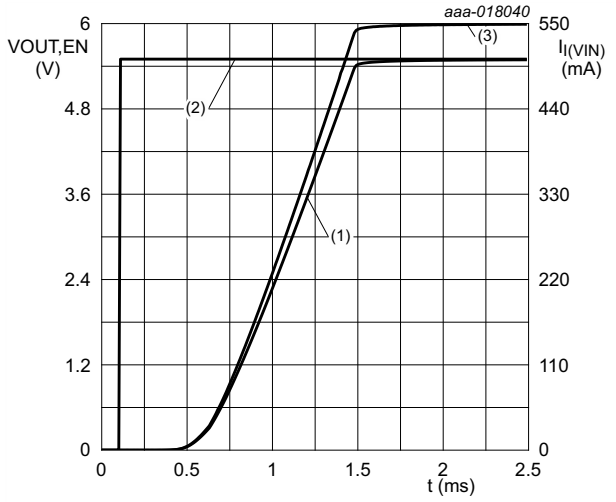
$V_{I(VIN)}$ = 3.6 V; R_L = 10 Ω; C_L = 0.1 µF; T_{amb} = 25 °C.

(1) VOUT

(2) EN

(3) $I_{I(VIN)}$

Fig 18. Typical enable time at $V_{I(VIN)}$ = 3.6 V; C_L = 0.1 µF



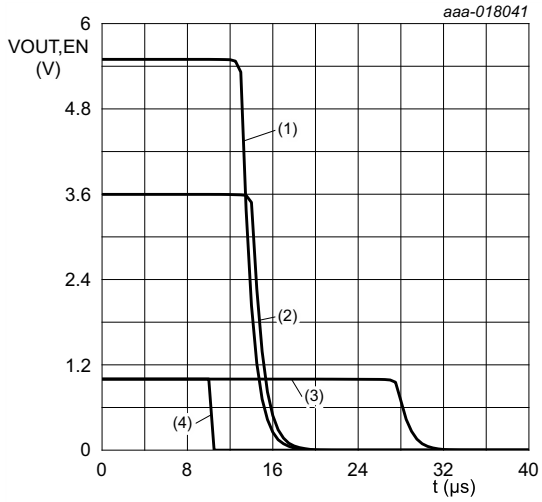
$V_{I(VIN)}$ = 5.5 V; R_L = 10 Ω; C_L = 0.1 µF; T_{amb} = 25 °C.

(1) VOUT

(2) EN

(3) $I_{I(VIN)}$

Fig 19. Typical enable time at $V_{I(VIN)}$ = 5.5 V; C_L = 0.1 µF



R_L = 10 Ω; C_L = 0.1 µF; T_{amb} = 25 °C

(1) $V_{I(VIN)}$ = 5.5 V

(2) $V_{I(VIN)}$ = 3.6 V

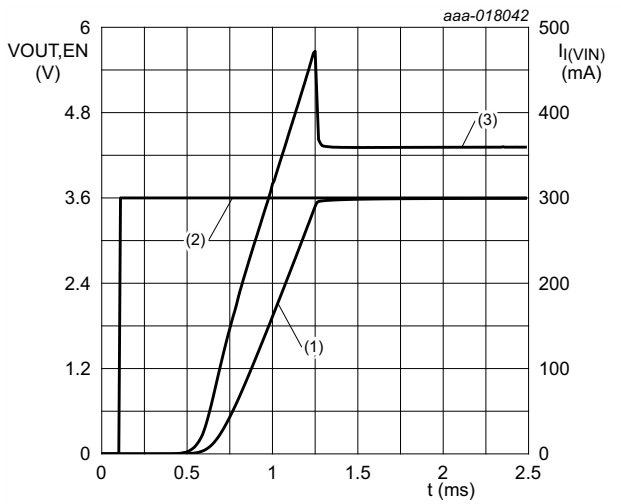
(3) $V_{I(VIN)}$ = 1.0 V

(4) EN

Fig 20. Typical disable time

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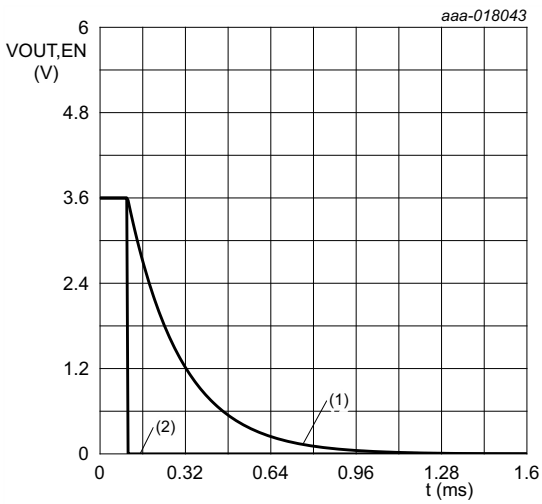
$V_{I(VIN)}$ = 3.6 V; R_L = 10 Ω; C_L = 20 µF; T_{amb} = 25 °C.

(1) VOUT

(2) EN

(3) $I_{I(VIN)}$

Fig 21. Typical enable time at $V_{I(VIN)}$ = 3.6 V; C_L = 20 µF



$V_{I(VIN)}$ = 3.6 V; R_L = 10 Ω; C_L = 20 µF; T_{amb} = 25 °C

(1) VOUT

(2) EN

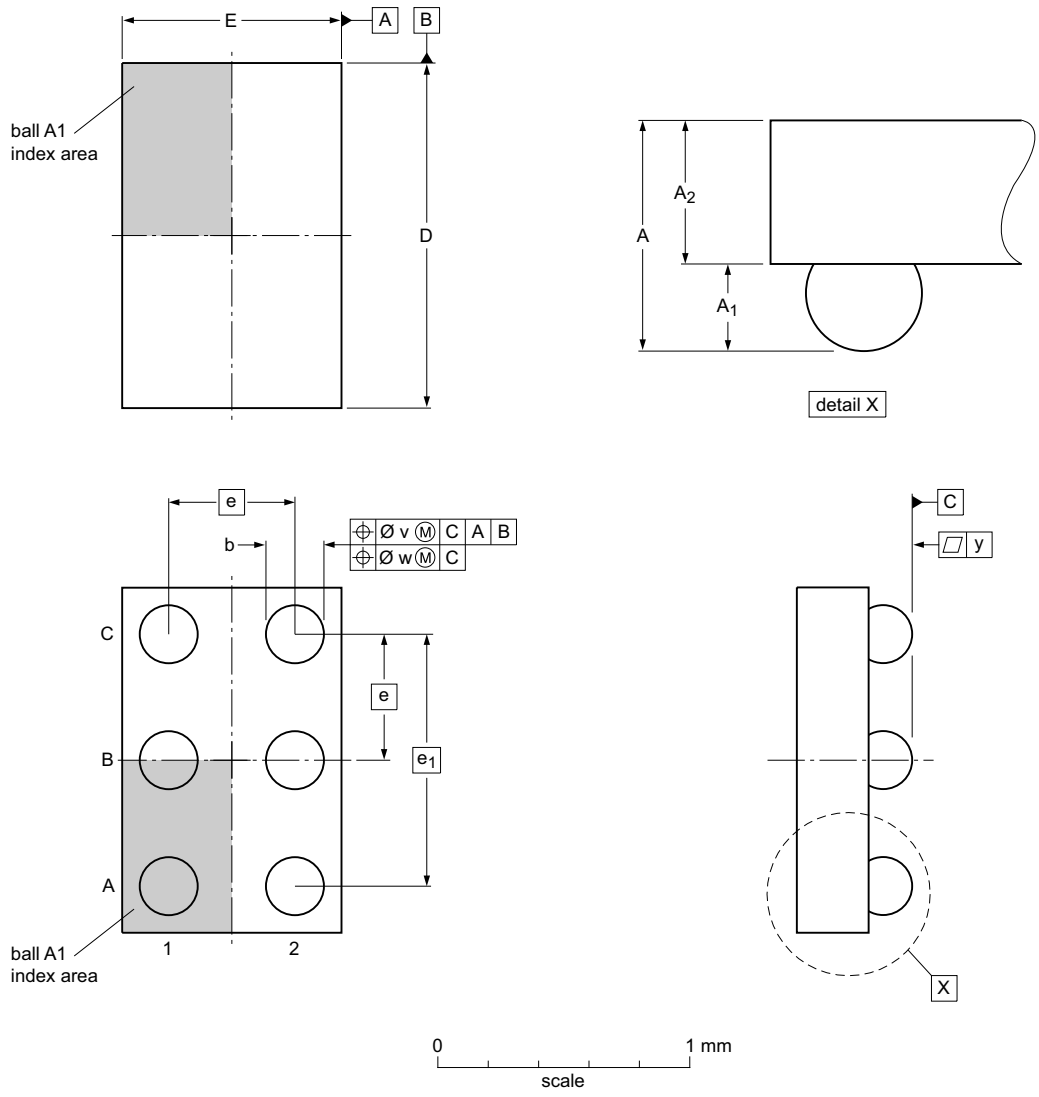
Fig 22. Typical disable time at $V_{I(VIN)}$ = 3.6 V; C_L = 20 µF

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15. Package outline

WLCSP6: wafer level chip-scale package, 6 bumps; 0.87 x 1.37 x 0.50 mm **NX5P2924C**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	v	w	y
mm	max	0.50	0.19	0.315	0.25	1.40	0.90					
	nom		0.17	0.285	0.23	1.37	0.87	0.5	1.0	0.05	0.015	0.03
	min		0.15	0.255	0.21	1.34	0.84					

wlcsp6_nx5p2924c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NX5P2924C						~~15-04-13~~ 15-04-21

Fig 23. Package outline NX5P2924C

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16. Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13.

Table 13. Lead-free process (from J-STD-020D)

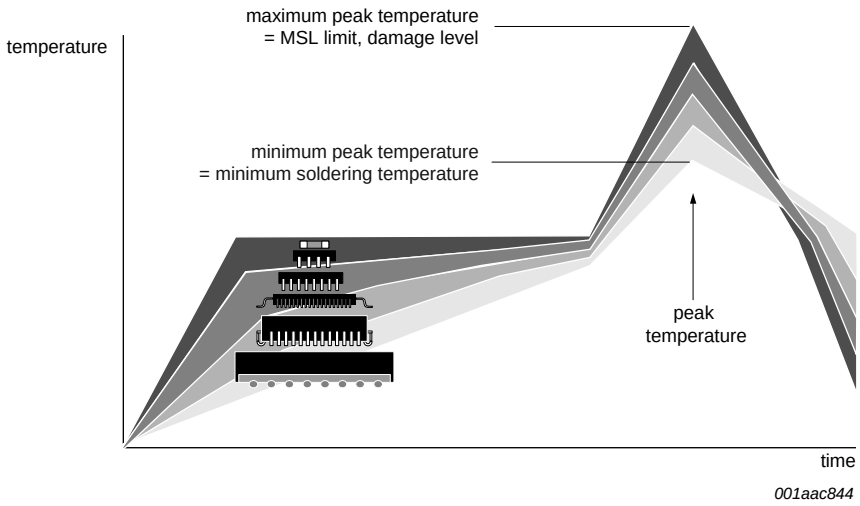
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.

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MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

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Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IEC	International Electrotechnical Commission
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor

18. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P2924C v.1	20150707	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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