RAA220002

Dual Synchronous Rectified Buck MOSFET Driver

The RAA220002 is a dual high frequency MOSFET driver designed to drive upper and lower power N-channel MOSFETs in a synchronous rectified buck converter topology.

The RAA220002's upper and lower gates are both driven to an externally applied voltage, which provides the ability to optimize applications involving trade-offs between gate charge and conduction losses.

An advanced adaptive shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The RAA220002 has a 10kΩ integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt.

The RAA220002's overvoltage protection feature is operational while V_{CC} is below the POR threshold. The PHASE node is connected to the gate of the low-side MOSFET (LGATE) through a 30kΩ resistor, limiting the output voltage of the converter close to the gate threshold of the low-side MOSFET. This is dependent on the current being shunted, which provides some protection to the load if the upper MOSFET(s) becomes shorted.

Applications

- High light-load efficiency voltage regulators
- Core regulators for advanced microprocessors
- High current DC/DC converters

Features

- Dual independent MOSFET driver suitable for multi-phase DC/DC applications
- Dual MOSFET drives for synchronous rectified bridge
- Advanced adaptive zero shoot-through protection
  - PHASE detection
  - LGATE detection
  - Auto-zero of $r_{DS(ON)}$ conduction offset effect
- Low standby bias current
- 36V internal bootstrap switcher
- Bootstrap capacitor overcharging prevention
- Integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt
- Pre-POR overvoltage protection for start-up and shutdown
- Power rail undervoltage protection
- Expandable bottom copper pad for enhanced heat sinking
- Thin Dual Flat No-lead (TDFN) package
- Near chip-scale package footprint; improves PCB efficiency and thinner in profile
- Pb-free (RoHS compliant)

Related Literature

For a full list of related documents, visit our website:

- RAA220002 device page

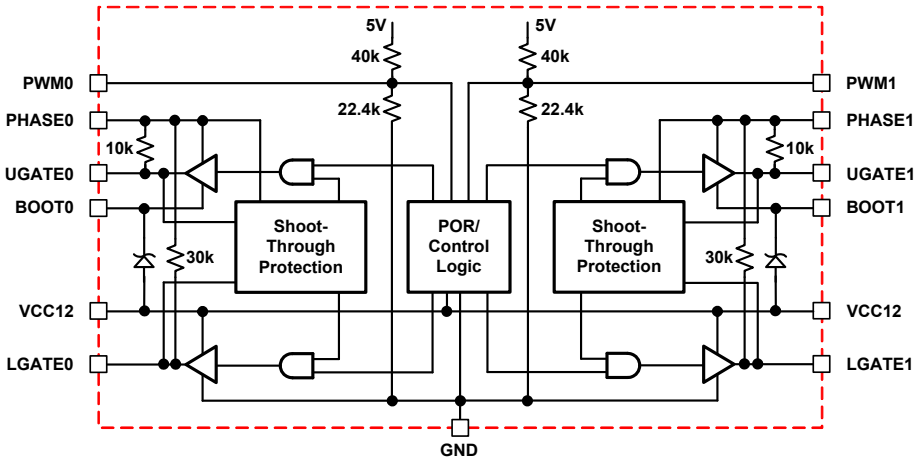


Figure 1. Block Diagram

1. Overview

1.1 Typical Applications

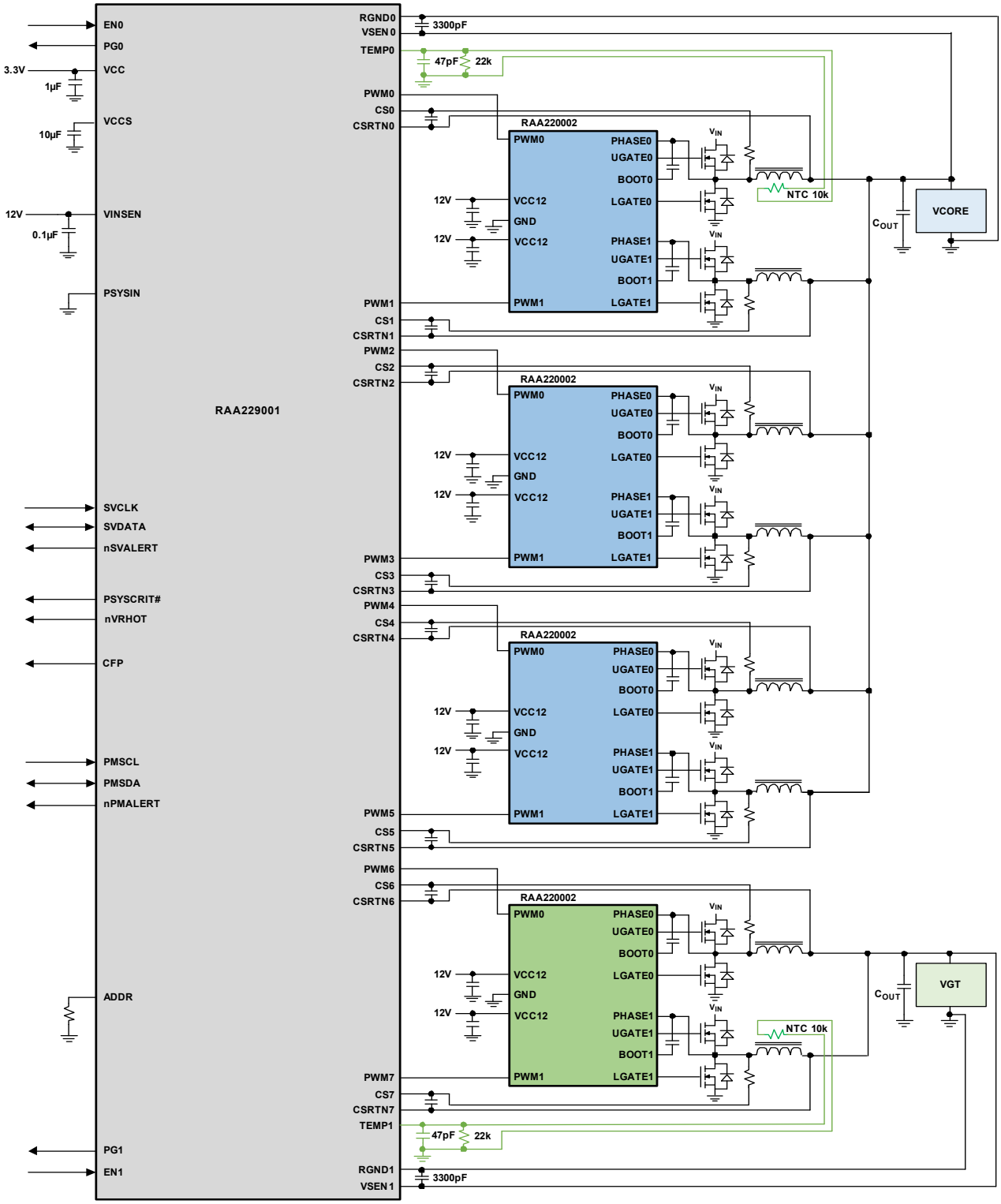


Figure 2. Intel Application 6+2 with Dual Driver

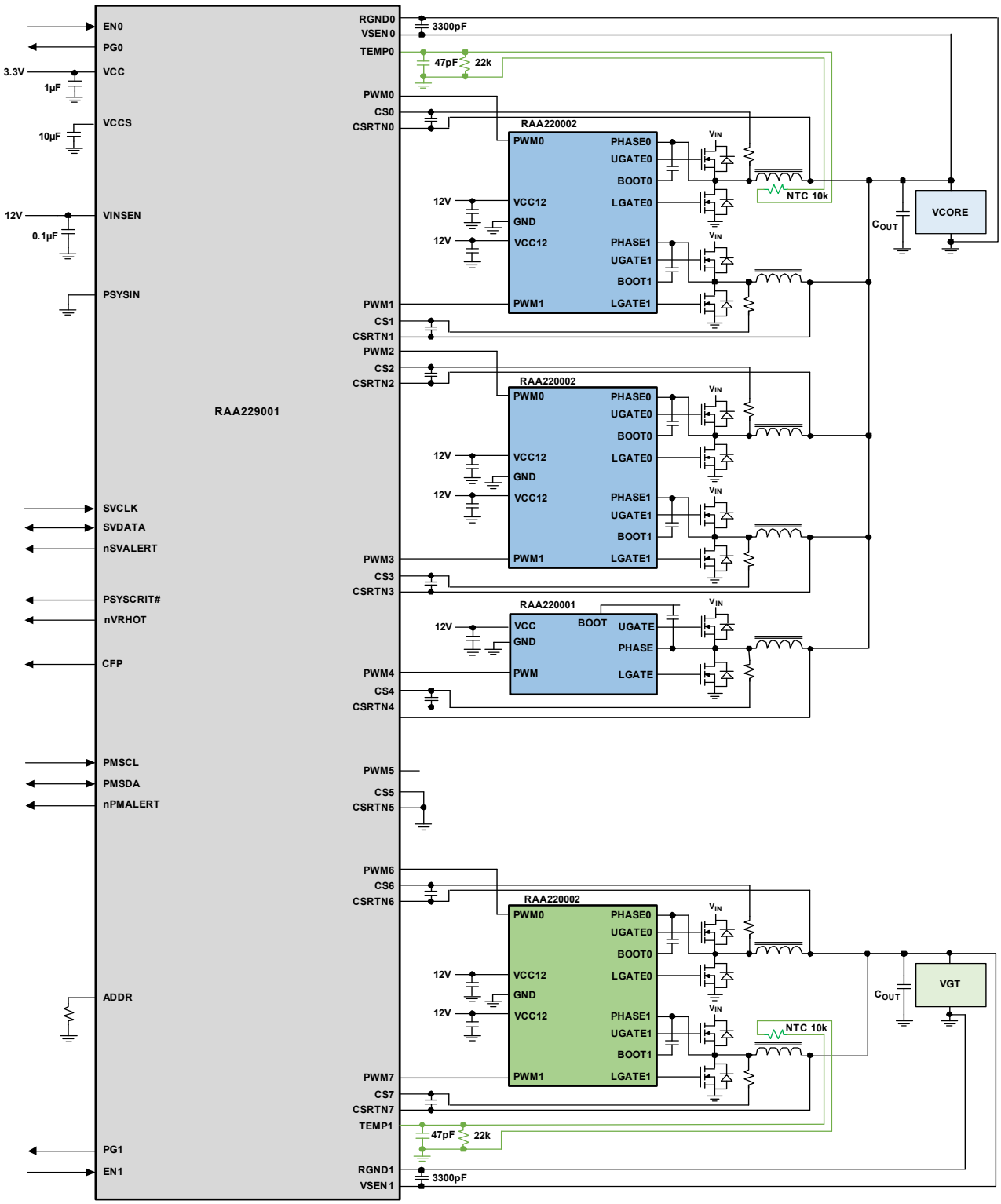


Figure 3. Intel Application 5+2 with Single-Dual Driver

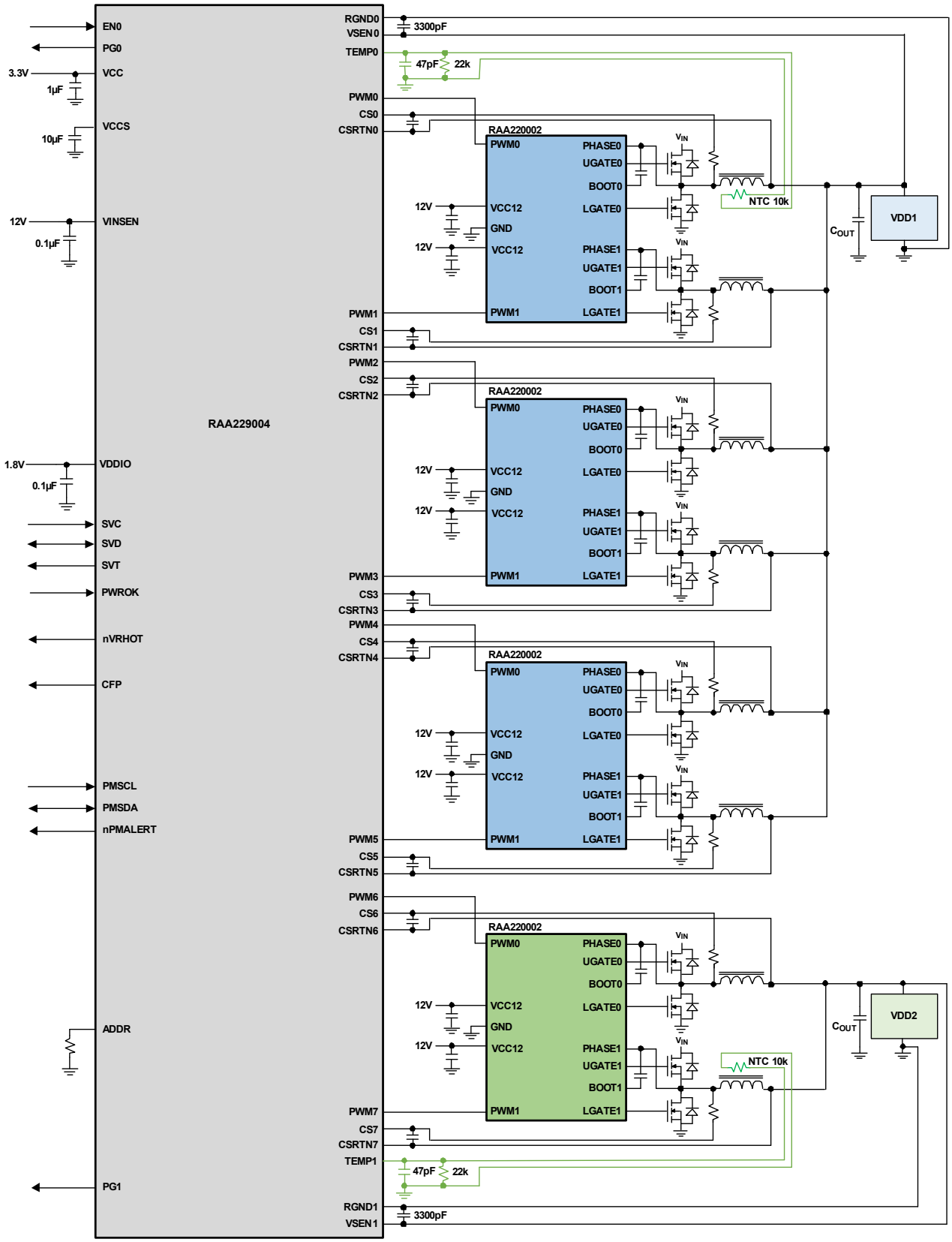


Figure 4. AMD Application 6+2 with Dual Driver

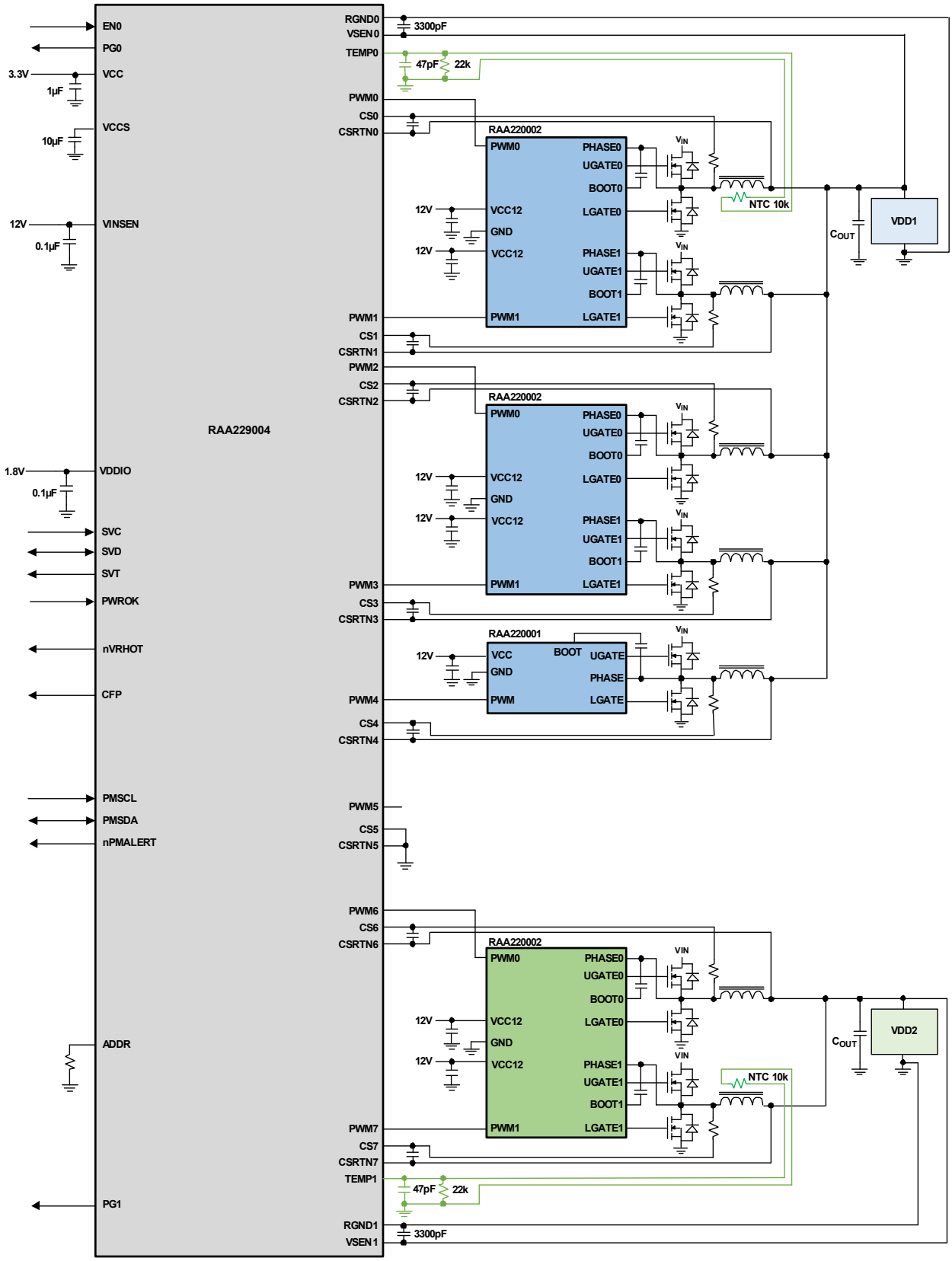


Figure 5. AMD Application 5+2 with Single-Dual Driver

1.2 Ordering Information

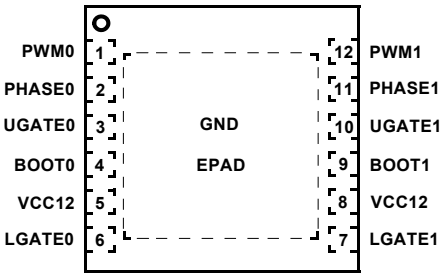
Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA220002GNP#HA0	0002	-40 to +85	6k	12 Ld 3x3 TDFN	L12.3x3C

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the RAA220002 device page. For more information about MSL, see TB363.

1.3 Pin Configuration

12 Ld 3x3 TDFN
Top View



1.4 Functional Pin Descriptions

Pin #	Pin Symbol	Function
1, 12	PWM[0:1]	Control input for the driver. The PWM signal can enter three distinct states during operation; see "Three-State PWM Input" on page 10 for more details. Connect to the PWM output of the controller.
2, 11	PHASE[0: 1]	Provides a return path for the upper gate drive. Connect to the source of the upper MOSFET and the drain of the lower MOSFET.
3, 10	UGATE[0:1]	Upper gate drive output. Connect to the gate of the high-side power N-channel MOSFET.
4, 9	BOOT[0:1]	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See "Internal Bootstrap Device" on page 10 for information about choosing the capacitor value.
5, 8	VCC12	These two pins must tie to each other. Connect them to a 12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
6, 7	LGATE[0:1]	Lower gate drive output. Connect to the gate of the low-side power N-channel MOSFET.
PAD	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver. Connect this pad to the power ground plane (GND) using a thermally enhanced connection.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage (V_{CC})		15	V
BOOT Voltage ($V_{BOOT - GND}$)		36	V
Input Voltage (V_{PWM})	GND - 0.3	7	V
UGATE	V_{PHASE} - 0.3V_{DC}	V_{BOOT} + 0.3	V
	V_{PHASE} - 3.5 (<100ns Pulse Width, 2µJ)	V_{BOOT} + 0.3	V
LGATE	GND - 0.3V_{DC}	V_{VCC} + 0.3	V
	GND - 5 (<100ns Pulse Width, 2µJ)	V_{VCC} + 0.3	V
PHASE	GND - 0.3	25	V_{DC}
	GND - 8 (<400ns, 20µJ)	30 (<200ns, $V_{BOOT - GND}$ <36V)	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	3000		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
3x3 DFN Package (Notes 4, 5)	48	10

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+85	°C
Maximum Operating Junction Temperature		+125	°C
Supply Voltage, V_{CC}	6.0	13.2	V

2.4 Electrical Specifications

Recommended operating conditions, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
V_{CC} Supply Current						
No Load Switching Supply Current (Dual)	I_{VCC}	V_{VCC} = 12V, f_{PWM} = 300kHz		12.5		mA
	I_{VCC}	V_{VCC} = 12V, PWM = 1.65V		1.4		mA
Power-On Reset						
V_{CC} Rising Threshold			4.5	4.7	4.95	V
V_{CC} Falling Threshold			4.0	4.27	4.5	V
V_{CC} POR hysteresis			0.4			V
PWM Input (See "Timing Diagram" on page 9)						
Input Current	I_{PWM}	V_{PWM} = 3.3V, V_{CC} = 12V		90		µA
		V_{PWM} = 0V, V_{CC} = 12V		-110		µA
Three-State Upper Gate Rising Threshold		V_{CC} = 12V		2.64		V
Three-State Upper Gate Falling Threshold		V_{CC} = 12V		2.17		V
Three-State Lower Gate Rising Threshold		V_{CC} = 12V		0.90		V
Three-State Lower Gate Falling Threshold		V_{CC} = 12V		1.07		V
UGATE Rise Time	t_{RU}	V_{VCC} = 12V, 3nF load, 10% to 90%		31		ns
LGATE Rise Time	t_{RL}	V_{VCC} = 12V, 3nF load, 10% to 90%		28		ns
UGATE Fall Time	t_{FU}	V_{VCC} = 12V, 3nF load, 90% to 10%		18		ns
LGATE Fall Time	t_{FL}	V_{VCC} = 12V, 3nF load, 90% to 10%		16		ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 12V, 3nF load, adaptive		16		ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 12V, 3nF load, adaptive		38		ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 12V, 3nF load		21		ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 12V, 3nF load		23		ns
Output						
Upper Drive Source Impedance	R_{U_SOURCE}	20mA source current		3.9		Ω
Upper Drive Sink Impedance	R_{U_SINK}	20mA sink current		1.4		Ω
Lower Drive Source Impedance	R_{L_SOURCE}	20mA source current		2.7		Ω
Lower Drive Sink Impedance	R_{L_SINK}	20mA sink current		0.9		Ω

Note:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

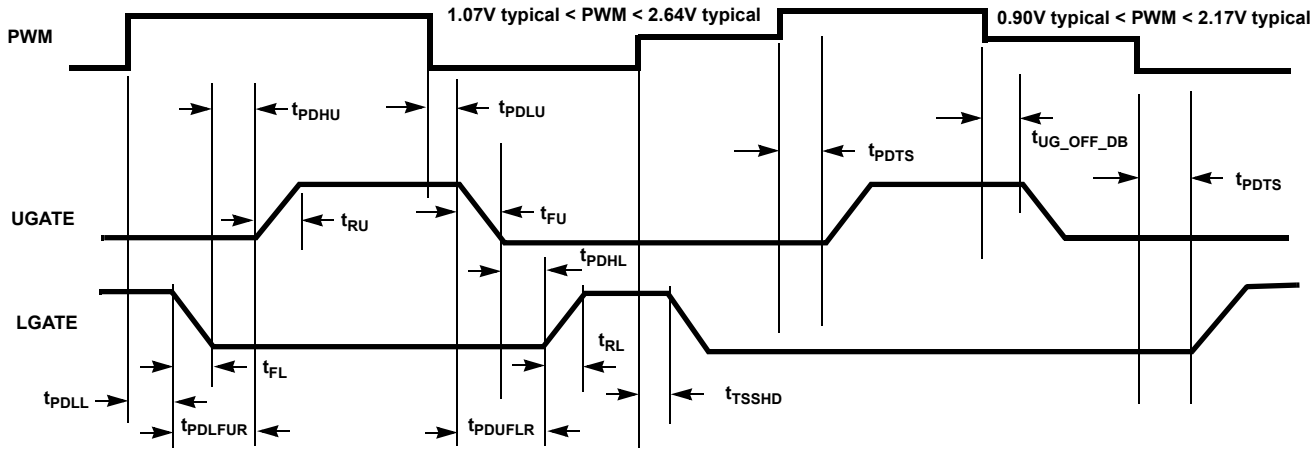


Figure 6. Timing Diagram

3. Operating the Device

3.1 Operation and Adaptive Shoot-Through Protection

The RAA220002 MOSFET driver is designed for high-speed switching and controls both high-side and low-side N-channel FETs from one externally provided PWM signal.

A rising transition on the PWM signal initiates the turn-off of the lower MOSFET (see Figure 6 on page 9). After a short propagation delay (t_{PDLL}), the lower gate begins to fall. Typical fall time (t_{FL}) is provided in the Electrical Specifications on page 8. After a 25ns blanking period, adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time (t_{PDHU}) after the LGATE voltage drops below ~1.75V. The upper gate drive then begins to rise (t_{RU}) and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay (t_{PDLU}) occurs before the upper gate begins to fall (t_{FU}). The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET following a short delay time (t_{PDHL}) after the upper MOSFET's PHASE voltage drops below +0.8V or 40ns after the upper MOSFET's gate voltage (UGATE-PHASE) drops below ~1.75V. The lower gate then rises (t_{RL}) and turns on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

The RAA220002 is optimized for voltage regulators with a large step down ratio. The lower MOSFET is usually sized larger than the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. Therefore, the lower gate driver is sized much larger to meet this application requirement. The 0.8Ω ON-resistance and 3A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

3.2 Three-State PWM Input

The RAA220002 and other Renesas drivers feature a unique three-state shutdown window to the PWM input. If the PWM signal enters the shutdown window and remains there for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the Electrical Specifications on page 8 determine when the lower and upper gates are enabled. This feature helps prevent a negative transient on the output voltage when the output is shut down, which eliminates the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

3.3 Power-On Reset (POR) Function

The V_{CC} voltage rise is monitored during initial start-up. When the rising V_{CC} voltage exceeds the rising POR threshold, driver operation is enabled and the PWM input signal takes control of the gate drives. If V_{CC} drops below the POR falling threshold, driver operation is disabled.

3.4 Pre-POR Overvoltage Protection

While V_{CC} is below its POR level, the upper gate is held low and LGATE is connected to the PHASE pin through an internal 30kΩ (typical) resistor. By connecting the PHASE node to the gate of the low-side MOSFET, the driver offers some passive protection to the load if the upper MOSFET(s) becomes shorted. If the PHASE node goes higher than the gate threshold of the lower MOSFET, this results in the progressive turn-on of the device and the effective clamping of the PHASE node's rise. The actual PHASE node clamping level depends on the lower MOSFET's electrical characteristics and the characteristics of the input supply and the path connecting it to the respective PHASE node.

3.5 Internal Bootstrap Device

The RAA220002 has an internal bootstrap Schottky diode equivalent circuit implemented by switchers with typical on-resistance of 40Ω and no typical diode forward voltage drop. Adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is designed to prevent the bootstrap

capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node and reduces the voltage stress on the BOOT to PHASE pins.

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for UVCC. Its minimum capacitance value can be estimated from Equation 1:

(EQ. 1)
$$C_{BOOT_CAP} \geq \frac{Q_{UGATE}}{\Delta V_{BOOT_CAP}}$$
$$Q_{UGATE} = \frac{Q_{G1} x UVCC}{V_{GS1}} x N_{Q1}$$

where:

- Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage
- N_{Q1} is the number of control MOSFETs
- ΔV_{BOOT_CAP} is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 7.

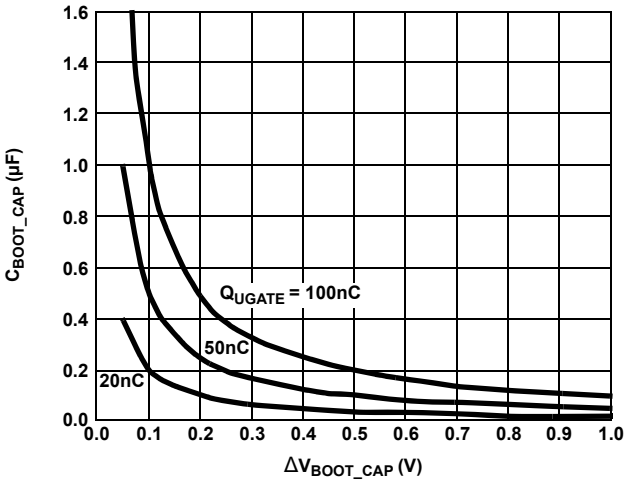


Figure 7. Bootstrap Capacitance vs Boot Ripple Voltage

3.6 Power Dissipation

Package power dissipation is mainly a function of the switching frequency (f_{SW}), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge (Q_G). Calculating the power dissipation in the driver for an application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level can push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 13 for thermal impedance improvement suggestions. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated using Equations 2 and 3, respectively.

$$P_{Qg_TOT} = P_{Qg_Q1} + P_{Qg_Q2} + I_Q x VCC$$

(EQ. 2)
$$P_{Qg_Q1} = \frac{Q_{G1} x UVCC^2}{V_{GS1}} x f_{SW} x N_{Q1}$$
$$P_{Qg_Q2} = \frac{Q_{G2} x LVCC^2}{V_{GS2}} x f_{SW} x N_{Q2}$$

(EQ. 3) $$I_{DR} = \left(\frac{Q_{G1}xUVCCxN_{Q1}}{V_{GS1}} + \frac{Q_{G2}xLVCCxN_{Q2}}{V_{GS2}}\right)xf_{SW} + I_Q$$

where:

- Gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet.
- I_Q is the driver's total quiescent current with no load at both drive outputs.
- N_{Q1} is the number of upper MOSFETs and N_{Q2} is the number of lower MOSFETs.
- UVCC is the drive voltage for the upper FETs and LVCC is the drive voltages for the lower FETs.
- I_Q x VCC product is the quiescent power of the driver without a load.

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses and the remainder are dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 8 and 9 show the typical upper and lower gate drives' turn-on current paths.

(EQ. 4)

$$P_{DR} = P_{DR_UP} + P_{DR_LOW} + I_Q xVCC$$

$$P_{DR_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right)x\frac{P_{Qg_Q1}}{2}$$

$$P_{DR_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right)x\frac{P_{Qg_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \quad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

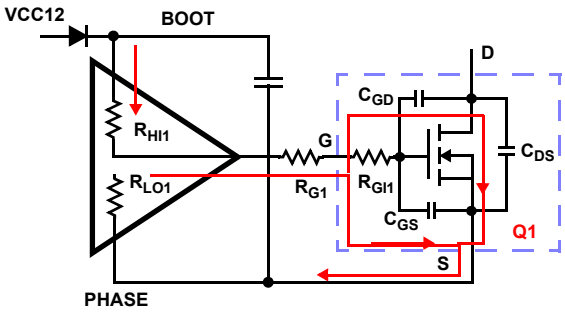


Figure 8. Typical Upper-Gate Drive Turn-On Path

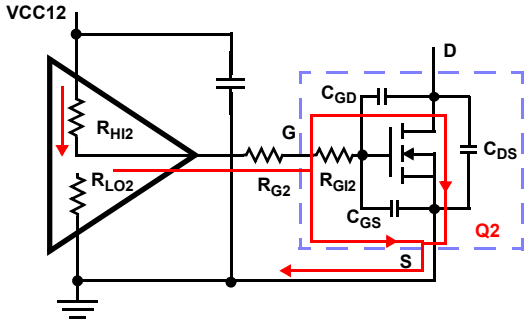


Figure 9. Typical Lower-Gate Drive Turn-On Path

4. Application Information

4.1 Layout Considerations

During device switching, the parasitic inductances of the PCB and the power devices' packaging (both upper and lower MOSFETs) lead to ringing, possibly in excess of the absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following guidelines lead to an optimized layout:

- Keep decoupling loops (VCC12-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND) should be as short and wide as possible.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper MOSFET and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the input current loop. Connect the source of the lower MOSFET to ground as close to the transistor pin as possible; place input capacitors (especially ceramic decoupling) as close as possible to the drain of the upper MOSFET and the source of lower MOSFET.

For improved heat dissipation, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended surface copper islands, and buried planes allows the IC and the power switches to achieve their full thermal potential.

4.2 Upper MOSFET Self Turn-On Effect at Start-Up

If the driver has insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating (due to self-coupling through the internal C_{GD} of the MOSFET), the gate of the upper MOSFET can momentarily rise up to a level greater than the threshold voltage of the device and potentially turn on the upper switch. In this situation, place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rise rate, the C_{GD}/C_{GS} ratio, and the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET requires a smaller resistor to reduce the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient and does not affect normal performance and efficiency.

(EQ. 5)
$$V_{GS_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right)$$

$$R = R_{UGPH} + R_{GI}$$

$$C_{rss} = C_{GD}$$

$$C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. Figure 10 on page 14 provides a visual reference for this phenomenon and its potential solution.

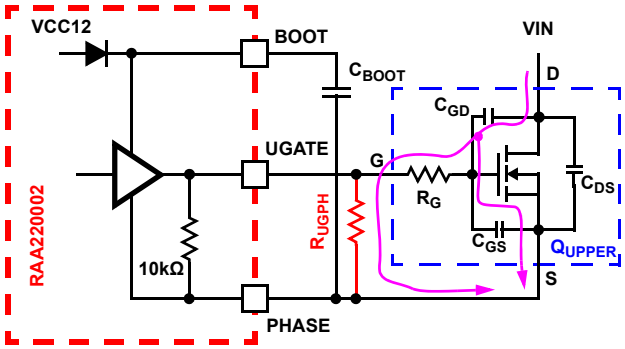


Figure 10. Gate-to-Source Resistor to Reduce Upper MOSFET Miller Coupling

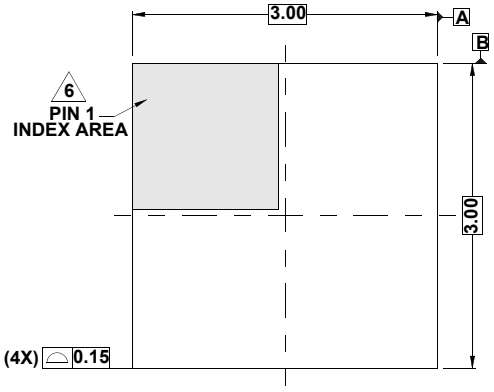
5. Revision History

Rev.	Date	Description
1.00	Jul.8.19	Initial release.

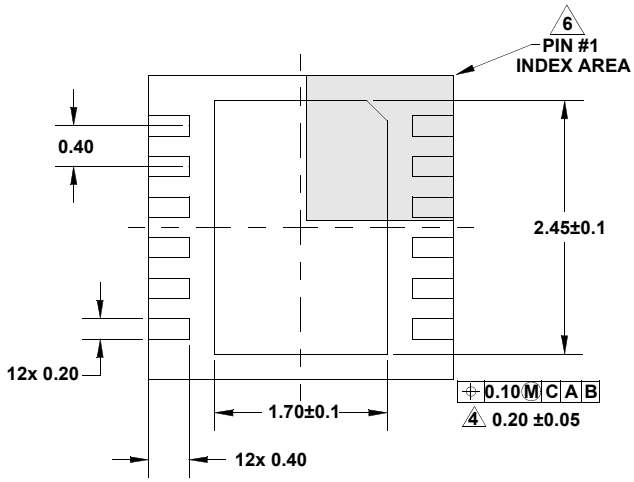
6. Package Outline Drawing

For the most recent package outline drawing, see L12.3x3C.

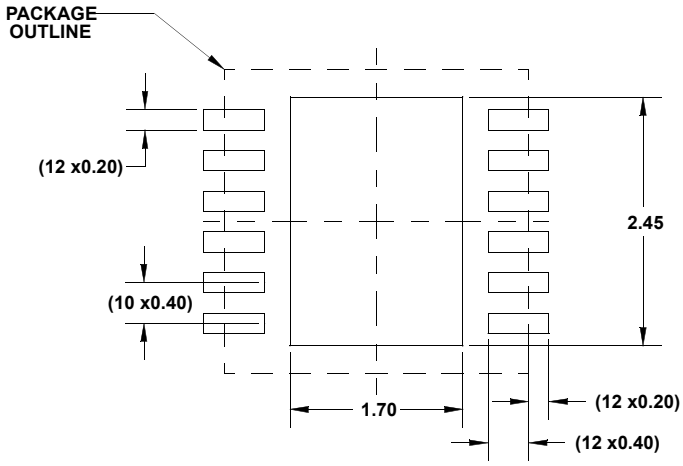
L12.3x3C
12 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (0.4mm PITCH)
Rev 1, 4/15



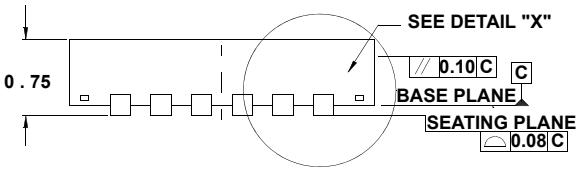
TOP VIEW



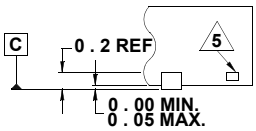
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Notice

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