GreenPAK Programmable Mixed-Signal Matrix with ASM and Dual 44 mΩ/2 A P-FET

General Description

The SLG46517 provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46517. This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Key Features

- Four Analog Comparators
- Voltage Reference
- Seventeen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Continuous DFF/LATCH or 3-bit LUT
  - Four Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Five 8-bit Delays/Counters or 3-bit LUTs
  - Two 16-bit Delays/Counters or 4-bit LUTs
- Asynchronous State Machine
  - Eight States
  - Flexible Input Logic from State Transitions
- Serial Communications
  - I^2C Protocol Interface
- Pipe Delay – 16 Stage/3 Output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Deglitch Filters with Edge Detectors
- Two Oscillators
  - Configurable 25 kHz/2 MHz
  - 25 MHz RC Oscillator
- Crystal Oscillator
- Power-On Reset
- Eight Byte RAM + OTP User Memory
  - RAM Memory Space that is Readable and Writable via I^2C
  - User Defined Initial Values Transferred from OTP
- P-FET Power Switch
  - Power Switch IDS: 2 A
  - VIN: 1.71 V to 5.5 V
  - Low RDSON
    - 44 mΩ @ 5.5 V
    - 58 mΩ @ 3.3 V
    - 110 mΩ @ 1.71 V
- Read Back Protection (Read Lock)
- Power Supply
  - 1.8 V (±5%) to 5 V (±10%) Supply
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 28-pin MSTQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Power Management Switches
- Power Sequencing with Complex Analog Control
- Power Plane Component Size Reduction Project
- LED Driver
- Haptic Motor Driver

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1 Block Diagram

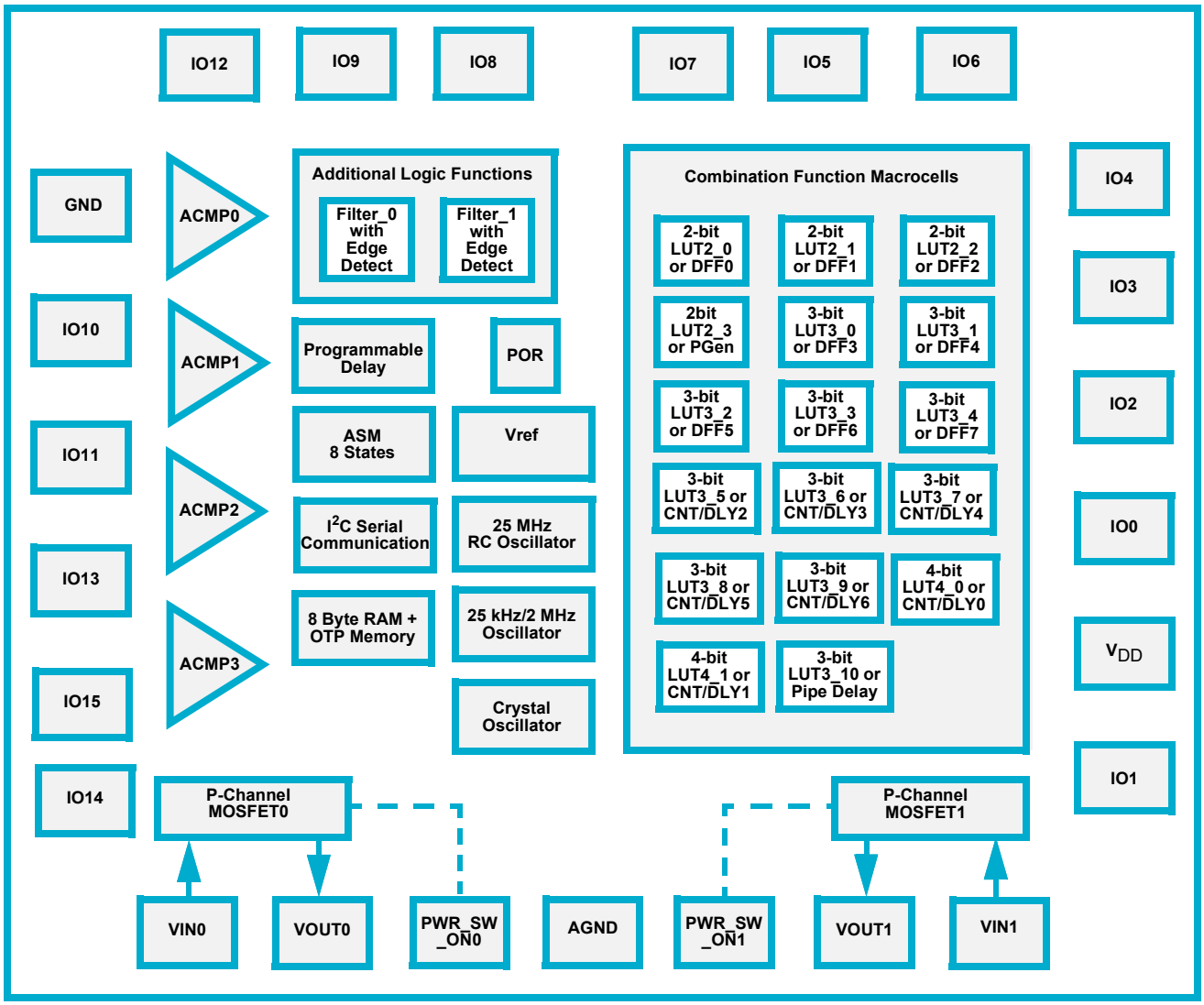
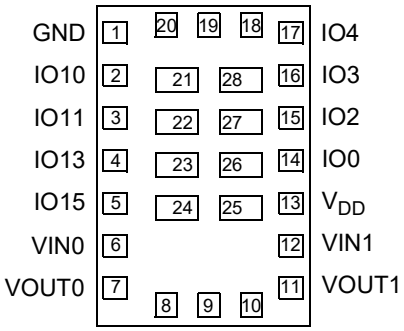


Figure 1: Block Diagram

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2 Pinout

2.1 PIN CONFIGURATION - MSTQFN- 28L



MSTQFN-28
(Top View)

8	NC	22	IO12
9	NC	23	IO14
10	AGND	24	PWR_SW_ON0
18	IO5	25	PWR_SW_ON1
19	IO7	26	IO1
20	IO8	27	NC
21	IO9	28	IO6

Pin #	Signal Name	Pin Functions
1	GND	GND
2	IO10	GPIO10/ACMP2+/ACMP3+
3	IO11	GPIO11/ACMP2-/ACMP3-
4	IO13	GPIO13/XTAL0
5	IO15	GPIO15/EXT_CLK1
6	VIN0	Power Switch 0 VIN
7	VOUT0	Power Switch 0 VOUT
8	NC	Not Connected
9	NC	Not Connected
10	AGND	Power Switch Ground
11	VOUT1	Power Switch 1 VOUT
12	VIN1	Power Switch 1 VIN
13	V_{DD}	V_{DD}
14	IO0	GPIO0
15	IO2	GPIO2
16	IO3	GPIO3
17	IO4	GPIO4/ACMP0+
18	IO5	GPIO5/ACMP0-
19	IO7	GPIO7/SDA
20	IO8	GPIO8/ACMP1+
21	IO9	GPIO/ACMP0-/ACMP1-/ACMP2-/ACMP3-
22	IO12	GPIO12/ACMP3+
23	IO14	GPIO14/XTAL1/EXT_CLK0
24	PWR_SW_ON0	Power Switch ON0
25	PWR_SW_ON1	Power Switch ON1
26	IO1	GPIO1
27	NC	Not Connected
28	IO6	GPIO6/SCL

Table 1: Functional Pin Description

MSTQFN 28L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	GND	GND	Ground	--	--
2	IO10	IO10	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP2+	Analog Comparator 2 Positive Input	Analog	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--

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Table 1: Functional Pin Description(Continued)

MSTQFN 28L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
3	IO11	IO11	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP2-	Analog Comparator 2 Negative Input	Analog	--
		ACMP3-	Analog Comparator 3 Negative Input	Analog	--
4	IO13	IO13	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		XTAL0	External Crystal Connection 0	--	Analog
5	IO15	IO15	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Vref	Voltage Reference 1 Output	--	Analog
		EXT_CLK1	External Clock Connection 1	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
6	VIN0	VIN0	Input and source terminal of Power Switch 0. Bypass the VIN0 pin to GND with a 1 µF (or larger), low-ESR capacitor.	--	--
7	VOUT0	VOUT0	Output and drain terminal of Power Switch 0.	--	
8	NC	NC	No Connection	--	--
9	NC	NC	No Connection	--	--
10	AGND	AGND	Power switch ground connection. Connect this pin to system analog or power ground plane.	--	--
11	VOUT1	VOUT1	Output and drain terminal of Power Switch 1	--	

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Table 1: Functional Pin Description(Continued)

MSTQFN 28L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
12	VIN1	VIN1	Input and source terminal of Power Switch 1. Bypass the VIN1 pin to GND with a 1 µF (or larger), low-ESR capacitor.		--
13	V_{DD}	V_{DD}	Power Supply	--	--
14	IO0	IO0	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
15	IO2	IO2	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
16	IO3	IO3	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
17	IO4	IO4	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
18	IO5	IO5	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP0-	Analog Comparator 0 Negative Input	Analog	--
19	IO7	IO7	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open-Drain NMOS
				Digital Input with Schmitt Trigger	Open-Drain NMOS
				Low Voltage Digital Input	Open-Drain NMOS

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Table 1: Functional Pin Description(Continued)

MSTQFN 28L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
20	IO8	IO8	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
21	IO9	IO9	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	--
		EXT_Vref	Analog Comparator Negative Input	Analog	--
23	IO14	IO14	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
		XTAL1	External Crystal Connection 1	Analog	--
		EXT_CLK0	External Clock Connection 0	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
24	PWR_SW_ON0	PWR_SW_ON0	ON0 turns Power Switch 0 ON	P-FET gate with 200 Ω resistor	--
25	PWR_SW_ON1	PWR_SW_ON1	ON1 turns Power Switch 1 ON	P-FET gate with 200 Ω resistor	--
26	IO1	IO1	General Purpose IO with OE **(Note 1)**	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
27	NC	NC	No connection	--	--
28	IO6	IO6	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	Open-Drain NMOS
				Digital Input with Schmitt Trigger	Open-Drain NMOS
				Low Voltage Digital Input	Open-Drain NMOS

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Table 1: Functional Pin Description(Continued)

MSTQFN 28L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
Note 1 General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.					

Table 2: Pin Type Definitions

Pin Type	Description
GND	Ground
AGND	P-FET Power Switch Ground
IO	Input/Output
VIN	P-FET Power Switch Input
VOUT	P-FET Power Switch Output
NC	No Connection
V_{DD}	Power Supply
PWR_SW_ON	Power Switch ON

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3 Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Condition	Min	Max	Unit
Supply voltage on V_{DD} relative to GND		-0.5	7	V
DC Input voltage		GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current Through V_{DD} Pin (Per chip side) **(Note 1)**	T_J = 85 °C	--	45	mA
	T_J = 110 °C	--	22	mA
Maximum Average or DC Current Through GND Pin (Per chip side) **(Note 1)**	T_J = 85 °C	--	86	mA
	T_J = 110 °C	--	41	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitivity Level		1		
V_{IN}	P-FET	0.3	V_{DD}	V
Θ_{JA}	Thermal Resistance **(Note 2)**	--	99	°C/W
P_D	Maximum Power Dissipation, T_A = +25 °C	--	1.25	W
$T_{J,MAX}$	Maximum Junction Temperature		150	°C
P-FET Power Switch IDS_{CONT}	Total, T_J < 150 °C	--	2	A
P-FET Power Switch IDS_{PK}	For no more than 1 ms with 1% duty cycle	--	2.5	A

Note 1 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7, and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14, and 15 to another.
Note 2 Mounted on 27.4 mm x 30.1 mm PCB (1.6 mm thick, 1 oz copper, FR-4 material).

3.2 ELECTROSTATIC DISCHARGE RATINGS

Table 4: Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

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3.3 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		1.8	5	V
Operating Temperature		-40	85	°C
Programming Voltage		7.25	7.75	V
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 ELECTRICAL CHARACTERISTICS

Table 6: EC at V_{DD} = 1.8 V ±5%, T = -40 °C to +85 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.06	--	V_{DD}	V
		Logic Input with Schmitt Trigger	1.28	--	V_{DD}	V
		Low-Level Logic Input	0.94	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	0.76	V
		Logic Input with Schmitt Trigger	0	--	0.49	V
		Low-Level Logic Input	0	--	0.52	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.10	0.41	0.66	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 100 µA, 1x Driver	1.69	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 1x Driver	1.69	1.79	--	V
		Push-Pull, I_{OH} = 100 µA, 2x Driver	1.70	1.79	--	V
		PMOS OD, I_{OH} = 100 µA, 2x Driver	1.70	1.79	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 100 µA, 1x Driver	--	0.009	0.013	V
		Push-Pull, I_{OL} = 100 µA, 2x Driver	--	0.004	0.006	V
		Open-Drain, I_{OL} = 100 µA, 1x Driver	--	0.006	0.009	V
		Open-Drain, I_{OL} = 100 µA, 2x Driver	--	0.003	0.004	V
		Open-Drain NMOS 4x, I_{OL} = 100 µA	--	0.001	0.002	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OH} = V_{DD} - 0.2, 1x Driver	1.07	1.70	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 1x Driver	1.07	1.70	--	mA
		Push-Pull, V_{OH} = V_{DD} - 0.2, 2x Driver	2.22	3.41	--	mA
		PMOS OD, V_{OH} = V_{DD} - 0.2, 2x Driver	2.22	3.41	--	mA
I_{OL}	LOW-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OL} = 0.15 V, 1x Driver	0.92	1.69	--	mA
		Push-Pull, V_{OL} = 0.15 V, 2x Driver	1.83	3.38	--	mA
		Open-Drain, V_{OL} = 0.15 V, 1x Driver	1.38	2.53	--	mA
		Open-Drain, V_{OL} = 0.15 V, 2x Driver	2.75	5.07	--	mA
		Open-Drain NMOS 4x, V_{OL} = 0.15 V	7.21	9.00	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	0.63	1.36	1.87	ms

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Table 6: EC at V_{DD} = 1.8 V ±5%, T = -40 °C to +85 °C, Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull-up Resistance	1 M Pull-up	--	1000	--	kΩ
		100 k Pull-up	--	100	--	kΩ
		10 k Pull-up	--	10	--	kΩ
R_{PDWN}	Pull-down Resistance	1 M Pull-down	--	1000	--	kΩ
		100 k Pull-down	--	100	--	kΩ
		10 k Pull-down	--	10	--	kΩ

Note 1 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14 to 15 another.

Table 7: EC at V_{DD} = 3.3 V ±10%, T = -40 °C to +85 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.81	--	V_{DD}	V
		Logic Input with Schmitt Trigger	2.14	--	V_{DD}	V
		Low-Level Logic Input	1.06	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.31	V
		Logic Input with Schmitt Trigger	0	--	0.97	V
		Low-Level Logic Input	0	--	0.67	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.29	0.62	0.94	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 3 mA, 1x Driver	2.70	3.12	--	V
		PMOS OD, I_{OH} = 3 mA, 1x Driver	2.70	3.12	--	V
		Push-Pull, I_{OH} = 3 mA, 2x Driver	2.85	3.21	--	V
		PMOS OD, I_{OH} = 3 mA, 2x Driver	2.86	3.21	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 3 mA, 1x Driver	--	0.13	0.23	V
		Push-Pull, I_{OL} = 3 mA, 2x Driver	--	0.06	0.11	V
		Open-Drain, I_{OL} = 3 mA, 1x Driver	--	0.08	0.15	V
		Open-Drain, I_{OL} = 3 mA, 2x Driver	--	0.04	0.08	V
		Open-Drain NMOS 4x, I_{OL} = 3 mA	--	0.02	0.04	V
I_{OH}	HIGH-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OH} = 2.4 V, 1x Driver	6.05	12.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1x Driver	6.05	12.08	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2x Driver	11.54	24.16	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2x Driver	11.52	24.16	--	mA

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Table 7: EC at V_{DD} = 3.3 V ±10%, T = -40 °C to +85 °C, Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OL} = 0.4 V, 1x Driver	4.88	8.24	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2x Driver	9.75	16.49	--	mA
		Open-Drain, V_{OL} = 0.4 V, 1x Driver	7.31	12.37	--	mA
		Open-Drain, V_{OL} = 0.4 V, 2x Driver	14.54	24.74	--	mA
		Open-Drain NMOS 4x, V_{OL} = 0.4 V	31.32	41.06	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull-up Resistance	1 M Pull-up	--	1000	--	kΩ
		100 k Pull-up	--	100	--	kΩ
		10 k Pull-up	--	10	--	kΩ
R_{PDWN}	Pull-down Resistance	1 M Pull-down	--	1000	--	kΩ
		100 k Pull-down	--	100	--	kΩ
		10 k Pull-down	--	10	--	kΩ

Note 1 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14 to 15 another.

Table 8: EC at V_{DD} = 5 V ±10%, T = -40 °C to +85 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.68	--	V_{DD}	V
		Logic Input with Schmitt Trigger	3.34	--	V_{DD}	V
		Low-Level Logic Input	1.15	--	V_{DD}	V
V_{IL}	LOW-Level Input Voltage	Logic Input	0	--	1.96	V
		Logic Input with Schmitt Trigger	0	--	1.41	V
		Low-Level Logic Input	0	--	0.77	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger	0.44	0.90	1.38	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull, I_{OH} = 5 mA, 1x Driver	4.15	4.76	--	V
		PMOS OD, I_{OH} = 5 mA, 1x Driver	4.16	4.76	--	V
		Push-Pull, I_{OH} = 5 mA, 2x Driver	4.32	4.89	--	V
		PMOS OD, I_{OH} = 5 mA, 2x Driver	4.33	4.89	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL}= 5 mA, 1x Driver	--	0.19	0.24	V
		Push-Pull, I_{OL} = 5 mA, 2x Driver	--	0.09	0.12	V
		Open-Drain, I_{OL} = 5 mA, 1x Driver	--	0.12	0.16	V
		Open-Drain, I_{OL} = 5 mA, 2x Driver	--	0.07	0.08	V
		Open-Drain NMOS 4x, I_{OL} = 5 mA	--	0.03	0.05	V

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Table 8: EC at V_{DD} = 5 V ±10%, T = -40 °C to +85 °C, Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	HIGH-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OH} = 2.4 V, 1x Driver	22.08	34.04	--	mA
		PMOS OD, V_{OH} = 2.4 V, 1x Driver	22.08	34.04	--	mA
		Push-Pull, V_{OH} = 2.4 V, 2x Driver	41.76	68.08	--	mA
		PMOS OD, V_{OH} = 2.4 V, 2x Driver	41.69	68.08	--	mA
I_{OL}	LOW-Level Output Pulse Current **(Note 1)**	Push-Pull, V_{OL} = 0.4 V, 1x Driver	7.22	11.58	--	mA
		Push-Pull, V_{OL} = 0.4 V, 2x Driver	13.83	23.16	--	mA
		Open-Drain, V_{OL} = 0.4 V, 1x Driver	10.82	17.38	--	mA
		Open-Drain, V_{OL} = 0.4 V, 2x Driver	17.34	34.76	--	mA
		Open-Drain NMOS 4x, V_{OL} = 0.4 V	41.06	55.18	--	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	0.60	1.23	1.61	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V
R_{PUP}	Pull-up Resistance	1 M Pull-up	--	1000	--	kΩ
		100 k Pull-up	--	100	--	kΩ
		10 k Pull-up	--	10	--	kΩ
R_{PDWN}	Pull-down Resistance	1 M Pull-down	--	1000	--	kΩ
		100 k Pull-down	--	100	--	kΩ
		10 k Pull-down	--	10	--	kΩ

Note 1 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2 The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7 and 8 are connected to one side, IOs 9, 10, 11, 12, 13, 14 to 15 another.

Table 9: I^2C Pins Timing Characteristics T = -40 °C to +85 °C, Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = 1.71 to 5.5 V	--	--	400	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = 1.71 to 5.5 V	1300	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = 1.71 to 5.5 V	600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 1.8 V ± 5%	--	--	95	ns
		V_{DD} = 3.3 V ± 10%	--	--	95	
		V_{DD} = 5.0 V ± 10%	--	--	111	
t_{AA}	Clock Low to Data Out Valid	V_{DD} = 1.71 to 5.5 V	--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = 1.71 to 5.5 V	1300	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = 1.71 to 5.5 V	600	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = 1.71 to 5.5 V	600	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = 1.71 to 5.5 V	0	--	--	ns
t_{SU_DAT}	Data Set-up Time	V_{DD} = 1.71 to 5.5 V	100	--	--	ns
t_R	Inputs Rise Time	V_{DD} = 1.71 to 5.5 V	--	--	300	ns
t_F	Inputs Fall Time	V_{DD} = 1.71 to 5.5 V	--	--	300	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = 1.71 to 5.5 V	600	--	--	ns

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Table 9: I²C Pins Timing Characteristics T = -40 °C to +85 °C, Unless Otherwise Noted(Continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
t_{DH}	Data Out Hold Time	V_{DD} = 1.71 to 5.5 V	50	--	--	ns

Table 10: Asynchronous State Machine Specifications at T = 25 °C

Parameter	Description	Note	Min	Typ	Max	Unit
$t_{st_out_delay}$	Asynchronous State Machine Output Delay Time	V_{DD} = 1.8 V ± 5%	225	--	275	ns
		V_{DD} = 3.3 V ± 10%	95		118	
		V_{DD} = 5.0 V ± 10%	67	--	77	
t_{st_out}	Asynchronous State Machine Output Transition Time	V_{DD} = 1.8 V ± 5%	--	--	165	ns
		V_{DD} = 3.3 V ± 10%	--		70	
		V_{DD} = 5.0 V ± 10%	--	--	46	
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 1.8 V ± 5%	29	--	--	ns
		V_{DD} = 3.3 V ± 10%	14	--	--	
		V_{DD} = 5.0 V ± 10%	9.2	--	--	
t_{st_comp}	Asynchronous State Machine Input Compete Time	V_{DD} = 1.8 V ± 5%	--	--	29	ns
		V_{DD} = 3.3 V ± 10%	--	--	14	
		V_{DD} = 5.0 V ± 10%	--	--	10	

Table 11: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C

Parameter	Description	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.45	0.75	1.12	µA
		OSC 2 MHz, pre-divider = 1	41.48	64.00	94.89	µA
		OSC 2 MHz, pre-divider = 8	25.68	32.41	43.22	µA
		OSC 25 kHz, pre-divider = 1	7.16	7.94	9.25	µA
		OSC 25 kHz, pre-divider = 8	6.97	7.60	8.68	µA
		OSC 25 MHz, pre-divider = 1	87.25	238.27	428.66	µA
		OSC 25 MHz, pre-divider = 1, Force On	87.25	238.27	428.67	µA
		OSC 25 MHz, pre-divider = 8	78.01	212.45	390.17	µA
		ACMP (each)	54.96	52.64	60.81	µA
		ACMP with buffer (each)	75.06	72.74	81.25	µA
		Vref	49.70	47.32	55.60	µA
		Vref with buffer	71.93	71.27	79.62	µA

3.5 TIMING CHARACTERISTICS

Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C

Parameter	Description	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	45	50	19	21	14	15	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	44	49	19	21	14	15	ns
tpd	Delay	Low Voltage Digital input to PP 1x	46	447	19	195	14	134	ns

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Table 12: Typical Delay Estimated for Each Macrocell at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 1.8 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital input to PMOS output	44	-	19	-	14	-	ns
tpd	Delay	Digital input to NMOS output	-	81	-	30	-	20	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	48	-	20	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	-	46	-	20	-	14	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LATCH	33	35	14	14	11	10	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bit	31	31	14	13	10	9	ns
tpd	Delay	LUT3bit	35	33	15	13	11	10	ns
tpd	Delay	CNT/DLY Logic	62	68	27	29	19	20	ns
tpd	Delay	DFF	32	28	14	12	11	9	ns
tpd	Delay	P_DLY1C	367	356	165	160	123	119	ns
tpd	Delay	P_DLY2C	667	656	303	297	225	221	ns
tpd	Delay	P_DLY3C	968	956	440	434	327	322	ns
tpd	Delay	P_DLY4C	1265	1252	576	570	428	423	ns
tpd	Delay	Filter	213	210	84	83	55	55	ns
tpd	Delay	ACMP (5mV overdrive)	1600	1900	1500	1800	1600	1800	ns
tw	Pulse Width	IO with 1x Push-Pull (min transmitted)	20	20	20	20	20	20	ns
tw	Pulse Width	filter (min transmitted)	150	150	55	55	35	35	ns

Table 13: Typical Propagations Delays and Pulse Widths at T = 25 °C

Parameter	Description	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
tw	Pulse Width, 1 cell	mode: (any)edge detect, edge detect output	296	135	101	ns
tw	Pulse Width, 2 cell	mode: (any)edge detect, edge detect output	597	272	203	ns
tw	Pulse Width, 3 cell	mode: (any)edge detect, edge detect output	898	410	305	ns
tw	Pulse Width, 4 cell	mode: (any)edge detect, edge detect output	1195	546	407	ns
time1	Delay, 1 cell	mode: (any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 2 cell	mode: (any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 3 cell	mode: (any)edge detect, edge detect output	55	24	18	ns
time1	Delay, 4 cell	mode: (any)edge detect, edge detect output	55	24	18	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	367	165	106	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	667	300	193	ns

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Table 13: Typical Propagations Delays and Pulse Widths at T = 25 °C(Continued)

Parameter	Description	Note	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
time2	Delay, 3 cell	mode: both edge delay, edge detect output	968	440	279	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1265	575	365	ns

Table 14: Typical Deglitch Filter Pulse Width Performance at T = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width for Filter 0	< 114	< 47	< 30	ns
Filtered Pulse Width for Filter 1	<75	<30	<19	ns

Table 15: Typical Counter/Delay Offset Measurements at T = 25 °C

Description	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Offset (start time)	25 kHz	auto	1.6	1.6	1.6	µs
Offset (start time), fast start	25 kHz	auto	2.1	2.1	2.1	µs
Offset (start time)	2 MHz	auto	0.4	0.2	0.2	µs
Offset (start time), fast start	2 MHz	auto	0.7	0.5	0.4	µs
Offset (start time)	25 MHz	auto	0.01	0.05	0.04	µs
Frequency settling time	25 kHz	auto	19	14	12	µs
Frequency settling time	2 MHz	auto	14	14	14	µs
Variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
Variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
Variable (CLK period)	25 MHz	--	0-0.04	0-0.04	0-0.04	µs
Tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

3.6 OSC CHARACTERISTICS

Table 16: 25 kHz RC OSC0 Frequency Limits V_{DD} = 2.3 V to 5.5 V

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5%	23.792	26.288	23.275	27.089	21.728	29.173
3.3 V ±10%	24.473	25.526	23.357	26.028	23.357	27.002
5 V ±10%	24.316	25.939	23.309	26.177	23.309	27.181
2.5 V to 4.5 V	24.438	25.559	23.336	26.051	23.336	27.038
1.71 V to 5.5 V	23.354	26.670	22.828	27.483	21.301	29.545

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Table 17: 25 kHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.83%	5.15%	-6.90%	8.36%	-13.09%	16.69%
3.3 V ±10%	-2.11%	2.10%	-6.57%	4.11%	-6.57%	8.01%
5 V ±10%	-2.73%	3.76%	-6.76%	4.71%	-6.76%	8.72%
2.5 V to 4.5 V	-2.25%	2.24%	-6.66%	4.21%	-6.66%	8.15%
1.71 V to 5.5 V	-6.58%	6.68%	-8.69%	9.93%	-14.80%	18.18%

Table 18: 2 MHz RC OSC0 Frequency Limits V_{DD} = 2.3 V to 5.5 V

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5%	1.915	2.062	1.832	2.103	1.810	2.144
3.3 V ±10%	1.937	2.070	1.858	2.132	1.813	2.145
5 V ±10%	1.894	2.233	1.853	2.270	1.767	2.270
2.5 V to 4.5 V	1.907	2.124	1.836	2.171	1.784	2.171
1.71 V to 5.5 V	1.760	2.274	1.706	2.305	1.629	2.305

Table 19: 2 MHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5%	-4.26%	3.12%	-8.38%	5.17%	-9.50%	7.20%
3.3 V ±10%	-3.14%	3.49%	-7.10%	6.58%	-9.33%	7.24%
5 V ±10%	-5.31%	11.66%	-7.37%	13.50%	-11.67%	13.50%
2.5 V to 4.5 V	-4.65%	6.18%	-8.22%	8.57%	-10.81%	8.57%
1.71 V to 5.5 V	-12.01%	13.72%	-14.69%	15.23%	-18.57%	15.23%

Table 20: 25 MHz RC OSC1 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±10%	22.316	27.220	21.771	27.572	21.771	27.912

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Table 20: 25 MHz RC OSC1 Frequency Limits(Continued)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
3.3 V ±10%	23.430	26.220	22.389	26.679	22.389	27.014
5 V ±10%	23.289	26.651	22.500	27.305	22.500	27.486
2.5 V to 4.5 V	23.383	26.220	20.725	26.679	20.725	27.014
1.71 V to 5.5 V	12.643	26.220	12.203	26.679	11.317	27.014

Table 21: 25 MHz RC OSC1 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±10%	-10.73%	8.88%	-12.92%	10.29%	-12.92%	11.65%
3.3 V ±10%	-6.28%	4.88%	-10.44%	6.72%	-10.44%	8.06%
5 V ±10%	-6.84%	6.61%	-10.00%	9.22%	-10.00%	9.95%
2.5 V to 4.5 V	-14.47%	4.88%	-17.10%	6.72%	-17.10%	8.06%
1.71 V to 5.5 V	-49.43%	4.88%	-51.19%	6.72%	-54.73%	8.06%

Note: 25 MHz RC OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

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3.6.1 OSC Power-On Delay

Note: DLY/CNT Counter Data = 100, RC OSC Power Setting: "Auto Power-On", RC OSC Clock to Matrix Input: "Enable".

Table 22: OSC Power-On Delay, T = 25 °C

Power Supply Range (V_{DD}) V	RC OSC0 2 MHz		RC OSC0 25 kHz		RC OSC1	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	372.7	407.3	0.40	0.57	71.2	87.3
1.80	349.2	379.5	0.38	0.41	65.0	78.7
1.89	330.3	358.0	0.35	0.41	59.7	71.3
2.30	277.2	298.1	0.29	0.31	43.0	54.0
2.50	262.0	281.9	0.28	0.30	39.6	48.1
2.70	250.2	269.8	0.26	0.30	36.7	43.5
3.00	236.6	256.7	0.25	0.44	33.2	39.8
3.30	226.7	247.4	0.23	0.47	30.4	36.8
3.60	219.0	239.9	0.22	0.46	28.2	34.3
4.20	207.4	229.2	0.37	0.50	25.8	30.6
4.50	202.8	224.5	1.63	1.92	25.0	29.2
5.00	196.3	218.7	1.67	2.05	24.3	27.5
5.50	190.8	213.3	1.69	1.99	23.7	26.8

Table 23: OSC Power-On Delay, T = 25 °C, Fast Start-Up Time Mode

Power Supply Range (V_{DD}) V	RC OSC0 2 MHz		RC OSC1 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
1.71	327.9	360.0	0.68	0.76
1.80	309.9	338.3	0.64	0.64
1.89	295.5	323.1	0.61	0.70
2.30	254.9	278.1	0.53	21.93
2.50	243.1	266.1	3.23	21.88
2.70	234.1	257.1	16.68	21.94
3.00	223.7	246.8	19.25	21.90
3.30	215.7	239.1	19.22	21.77
3.60	209.4	232.9	19.21	21.74
4.20	199.5	223.4	19.17	21.78
4.50	195.5	219.8	19.15	21.69
5.00	189.8	214.6	19.12	21.71
5.50	184.9	209.8	19.05	21.75

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3.7 ACMP CHARACTERISTICS

Table 24: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, Unless Otherwise Noted

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	V_{DD} = 1.8 V ± 5%	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	V_{DD} = 3.3 V ± 10%	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	V_{DD} = 5.0 V ± 10%	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = 50 mV to 1200 mV, V_{DD} = 1.71 V to 5.5 V	T = 25 °C	-9.1	--	8.4	mV
			T = -40 °C to 85 °C	-10.9	--	10.9	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = 50 mV to 1200 mV, V_{DD} = 1.71 V to 5.5 V	T = 25 °C	-7.5	--	7.2	mV
			T = -40 °C to 85 °C	-10.7	--	10.5	mV
t_{start}	ACMP Start Time	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump set to automatic ON/OFF	BG = 550 µs, T = 25 °C V_{DD} = 1.71 V to 5.5 V	--	609.7	862.2	µS
			BG = 550 µs, T = -40 °C to 85 °C V_{DD} = 1.71 V to 5.5 V	--	675.0	1028.8	µS
			BG = 100 µs, T = 25 °C V_{DD} = 2.7 V to 5.5 V	--	132.4	176.2	µS
			BG = 100 µs, T = -40 °C to 85 °C V_{DD} = 2.7 V to 5.5 V	--	149.4	213.5	µS
		ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", Regulator and Charge Pump always OFF	BG = 550 µs, T = 25 °C V_{DD} = 3V to 5.5 V	--	609.5	862.0	µS
			BG = 550 µs, T = -40 °C to 85°C V_{DD} = 3 V to 5.5 V	--	674.6	1027.5	µS
			BG = 100 µs, T = 25 °C V_{DD} = 3 V to 5.5 V	--	131.6	176.0	µS
			BG = 100 µs, T = -40 °C to 85°C V_{DD} = 3 V to 5.5 V	--	149.2	213.3	µS

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Table 24: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25 °C	7.32	--	35.5	mV
			LB - Disabled, T = 25 °C	10.0	--	38.5	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	42.9	--	57.8	mV
			LB - Disabled, T = 25 °C	44.2	--	54.3	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	192.7	--	208.7	mV
			LB - Disabled, T = 25 °C	193.3	--	204.8	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled	0.0	--	58.0	mV
			LB - Disabled	0.0	--	52.9	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	22.5	--	86.9	mV
			LB - Disabled	29.2	--	76.5	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	157.1	--	251.6	mV
			LB - Disabled	160.2	--	245.3	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time	Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 50 mV	Low to High, T = (-40…+85)°C	--	35.99	216.56	µs
			High to Low, T = (-40…+85)°C	--	39.36	208.81	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 50 mV	Low to High, T = (-40…+85)°C	--	1.85	3.04	µs
			High to Low, T = (-40…+85)°C	--	2.17	4.10	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 50 mV	Low to High, T = (-40…+85)°C	--	25.22	129.31	µs
			High to Low, T = (-40…+85)°C	--	28.31	145.47	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 50 mV	Low to High, T = (-40…+85)°C	--	1.55	2.63	µs
			High to Low, T = (-40…+85)°C	--	1.93	3.83	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 250 mV	Low to High, T = (-40…+85)°C	--	36.46	216.78	µs
			High to Low, T = (-40…+85)°C	--	39.79	216.05	µs

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Table 24: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time	Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 250 mV	Low to High, T = (-40…+85)°C	--	2.04	3.37	µs
			High to Low, T = (-40…+85)°C	--	2.21	4.12	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 250 mV	Low to High, T = (-40…+85)°C	--	25.81	132.94	µs
			High to Low, T = (-40…+85)°C	--	28.65	142.43	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 250 mV	Low to High, T = (-40…+85)°C	--	1.74	2.93	µs
			High to Low, T = (-40…+85)°C	--	1.97	3.96	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 600 mV	Low to High, T = (-40…+85)°C	--	37.36	222.82	µs
			High to Low, T = (-40…+85)°C	--	40.67	219.61	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 600 mV	Low to High, T = (-40…+85)°C	--	2.23	4.02	µs
			High to Low, T = (-40…+85)°C	--	2.23	4.33	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 600 mV	Low to High, T = (-40…+85)°C	--	26.41	135.47	µs
			High to Low, T = (-40…+85)°C	--	29.32	149.01	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 600 mV	Low to High, T = (-40…+85)°C	--	1.92	3.53	µs
			High to Low, T = (-40…+85)°C	--	2.00	4.25	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 850 mV	Low to High, T = (-40…+85)°C	--	38.36	232.64	µs
			High to Low, T = (-40…+85)°C	--	41.67	232.78	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 850 mV	Low to High, T = (-40…+85)°C	--	2.26	4.20	µs
			High to Low, T = (-40…+85)°C	--	2.25	4.60	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 850 mV	Low to High, T = (-40…+85)°C	--	27.08	137.02	µs
			High to Low, T = (-40…+85)°C	--	29.89	146.92	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 850 mV	Low to High, T = (-40…+85)°C	--	1.91	3.57	µs
			High to Low, T = (-40…+85)°C	--	1.98	4.34	µs

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Table 24: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time	Low Bandwidth - Enable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 1200 mV	Low to High, T = (-40…+85)°C	--	103.93	1853.68	µs
			High to Low, T = (-40…+85)°C	--	101.06	1656.70	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(1.71..3.3)V, Overdrive=5 mV, Vref = 1200 mV	Low to High, T = (-40…+85)°C	--	68.29	1753.33	µs
			High to Low, T = (-40…+85)°C	--	63.06	1568.55	µs
		Low Bandwidth - Enable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 1200 mV	Low to High, T = (-40…+85)°C	--	30.62	167.56	µs
			High to Low, T = (-40…+85)°C	--	33.54	181.40	µs
		Low Bandwidth - Disable, Gain = 1, VDD=(3.3..5.5)V, Overdrive=5 mV, Vref = 1200 mV	Low to High, T = (-40…+85)°C	--	5.00	32.61	µs
			High to Low, T = (-40…+85)°C	--	5.24	33.88	µs
G	Gain error (including threshold and internal Vref error), T = -40 °C to +85 °C	G = 1, V_{DD} = 1.71 V	Vref = 50 mV to 1200 mV	--	1	--	
		G = 1, V_{DD} = 3.3 V		--	1	--	
		G = 1, V_{DD} = 5.5 V		--	1	--	
		G = 0.5, V_{DD} = 1.71 V		-1.00%	--	0.93%	
		G = 0.5, V_{DD} = 3.3 V		-0.96%	--	0.82%	
		G = 0.5, V_{DD} = 5.5 V		-1.04%	--	0.90%	
		G = 0.33, V_{DD} = 1.71V		-1.75%	--	2.10%	
		G = 0.33, V_{DD} = 3.3 V		-1.95%	--	1.69%	
		G = 0.33, V_{DD} = 5.5 V		-2.03%	--	1.77%	
		G = 0.25, V_{DD} = 1.71V		-1.91%	--	2.13%	
		G = 0.25, V_{DD} = 3.3 V		-1.98%	--	1.80%	
		G = 0.25, V_{DD} = 5.5 V		-2.12%	--	1.90%	

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Table 24: ACMP Specifications at T = -40 °C to +85 °C, V_{DD} = 2.3 V to 5.5 V, Unless Otherwise Noted(Continued)

Parameter	Description	Note	Conditions	Min	Typ	Max	Unit
Vref	Internal Vref error, Vref = 1200 mV	V_{DD} = 1.8 V ± 5%	T = 25 °C	-0.58%	--	0.56%	
				-1.01%	--	0.70%	
		V_{DD} = 3.3 V ± 10%	T = 25 °C	-0.59%	--	0.58%	
				-1.06%	--	0.72%	
		V_{DD} = 5.0 V ± 10%	T = 25 °C	-0.64%	--	0.60%	
				-1.16%	--	0.74%	
	Internal Vref error, Vref = 1000 mV	V_{DD} = 1.8 V ± 5%	T = 25 °C	-0.57%	--	0.58%	
				-1.14%	--	0.76%	
		V_{DD} = 3.3 V ± 10%	T = 25 °C	-0.59%	--	0.58%	
				-1.04%	--	0.73%	
		V_{DD} = 5.0 V ± 10%	T = 25 °C	-0.67%	--	0.64%	
				-1.15%	--	0.73%	
	Internal Vref error, Vref = 500 mV	V_{DD} = 1.8 V ± 5%	T = 25 °C	-0.64%	--	0.64%	
				-1.11%	--	0.75%	
		V_{DD} = 3.3 V ± 10%	T = 25 °C	-0.63%	--	0.63%	
				-1.10%	--	0.78%	
		V_{DD} = 5.0 V ± 10%	T = 25 °C	-0.72%	--	0.70%	
				-1.15%	--	0.80%	

3.8 POWER SWITCH EC (EACH P-FET)

Table 25: Power Switch EC, T_A = -40 °C to +85 °C (Typ Values at T_A = +25 °C), V_{DD} = 5.5 V, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	T_A = +25 °C, V_{GS} = -5.5 V, I_D = -100 mA **(Note 1)**	--	44	50	mΩ
		T_A = +25 °C, V_{GS} = -3.3 V, I_D = -100 mA **(Note 1)**	--	58	65	
		T_A = +25 °C, V_{GS} = -1.71 V, I_D = -100 mA **(Note 1)**	--	110	119	
		T_A = +85 °C, V_{GS} = -5.5 V, I_D = -100 mA **(Note 1)**	--	51	58	
		T_A = +85 °C, V_{GS} = -3.3 V, I_D = -100 mA **(Note 1)**	--	69	77	
		T_A = +85 °C, V_{GS} = -1.71 V, I_D = -100 mA **(Note 1)**	--	129	138	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -1 mA	-0.48	-0.61	-0.72	V
I_{DSS}	Zero Gate Voltage Drain Current	T_A = +25 °C, V_{DS} = -4.0 V, V_{GS} = 0 V **(Note 2)**	--	--	0.4	µA
		T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 V	--	--	1.0	
		T_A = +85 °C, V_{DS} = -5.5 V, V_{GS} = 0 V	--	--	3.4	
I_{GSS}	Gate-Body Leakage	T_A = +25 °C, V_{GS} = ±5.5 V	--	±5	±100	nA
		T_A = +85 °C, V_{GS} = ±5.5 V	--	±400	±2000	

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Table 25: Power Switch EC, T_A = -40 °C to +85 °C (Typ Values at T_A = +25 °C), V_{DD} = 5.5 V, Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
G_m	Forward Transconductance	V_{DS} = -5.5 V, V_{GS} = -1.8 V, I_D = -2 A **(Note 1)**	4.5	5.4	--	S
Dynamic						
R_G	Internal Gate Resistance		--	200	--	Ω
C_{iss}	Input Capacitance	T_A = +25 °C V_{DS} = -5.5 V V_{GS} = 0 V f = 1.0 MHz **(Note 3)**	--	207	--	pF
C_{oss}	Output Capacitance		--	122	--	
C_{rss}	Reverse Transfer Capacitance		--	57	--	
Q_g	Total Gate Charge	T_A = +25 °C V_{DS} = -5.5 V V_{GS} = -5.5 V I_D = -2 A **(Note 1)**	--	1.45	1.55	nC
Q_{gs}	Gate-to-Source Charge		--	0.24	--	
Q_{gd}	Gate-to-Drain Charge		--	0.24	--	
t_{on}	Turn-On Time	T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 to -5.5 V, ID = -1 A, Internal Drive	--	63	--	ns
t_{off}	Turn-Off Delay Time	T_A = +25 °C, V_{DS} = -5.5 V, V_{GS} = 0 to -5.5 V, ID = -1 A, Internal Drive	--	287	--	ns
Drain-Source Body Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current	T_A = +25 °C, single channel operation	--	--	-2	A
V_{DSF}	Diode Forward Voltage	V_{GS} = 0 V, I_S = 100 mA **(Note 1)**	0.63	0.75	0.87	V

Note 1 Pulse test: f = 100 Hz, Duty cycle < 2%.
Note 2 Measured to be less than 0.4 µA during production test.
Note 3 R_G influence has been excluded.

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4 User Programmability

The SLG46517 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

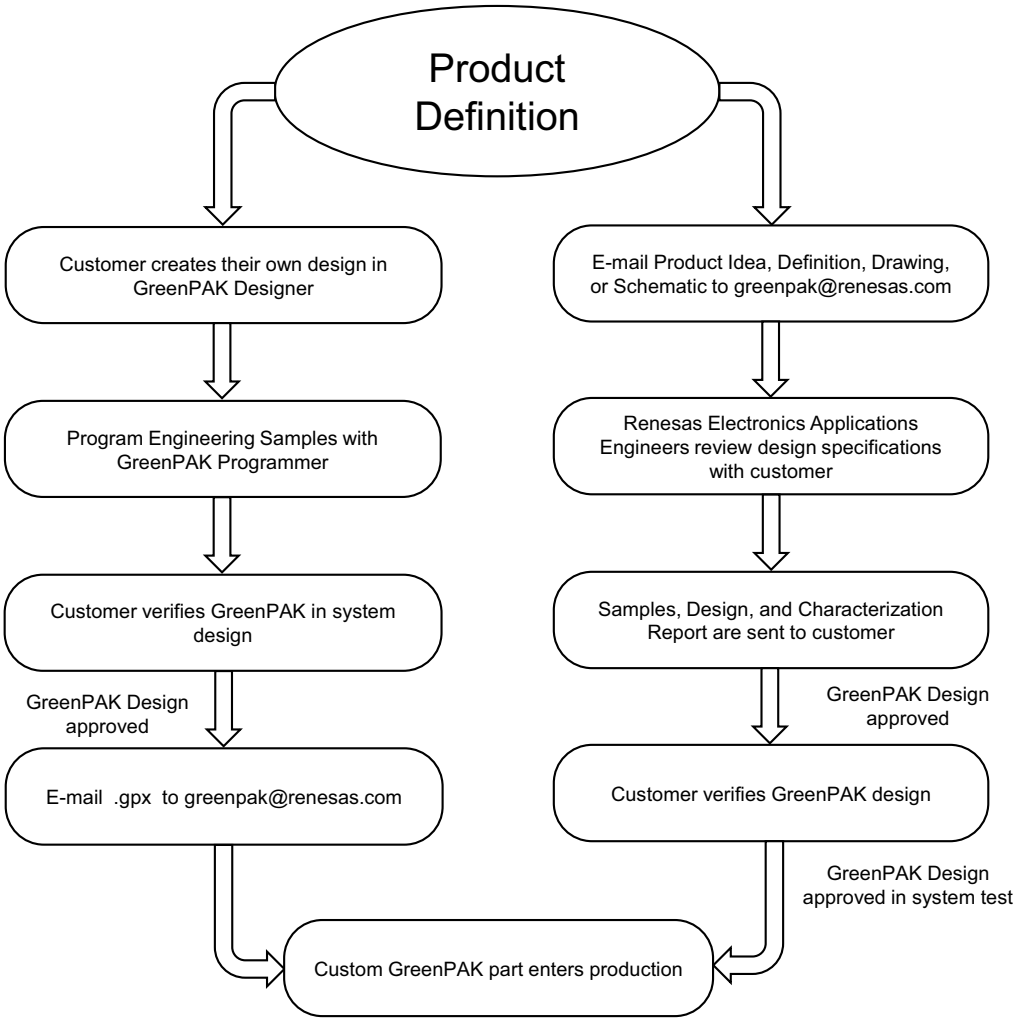


Figure 2: Steps to Create a Custom GreenPAK Device

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5 IO Pins

The SLG46517 has a total of 18 multi-function IO pins which can function as either a user defined Input or Output, as well as serving as a special function (such as voltage reference output), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Refer to Section 2 for normal and programming modepin definitions.

Normal Mode pin definitions are as follows:

- V_{DD}: V_{DD} power supply
- IO0: general purpose input
- IO1: general purpose input or output with OE
- IO2: general purpose input or output
- IO3: general purpose input or output with OE
- IO4: general purpose input or output or analog comparator 0(+)
- IO5: general purpose input or output with OE or analog comparator 0(-)
- IO6: general purpose input or OD output I^2C SCL
- IO7: general purpose input or OD output I^2C SDA
- IO8: general purpose input or output with OE, or analog comparator 1(+)
- GND: ground
- IO9: general purpose input or output, or analog comparator 1(-)
- IO10: general purpose input or output with OE, or analog comparator 2(+)
- IO11: general purpose input or output with OE, or analog comparator 2(-)
- IO12: general purpose input or output, or analog comparator 3(+)
- IO13: general purpose input or output with OE
- IO14: general purpose input or output
- IO15: general purpose input or output with OE and Vref output (Vref)
- VIN0: Power Switch 0 VIN
- VOUT0: Power Switch 0 VOUT
- AGND: Power Switch Ground
- VOUT1: Power Switch 1 VOUT
- VIN1: Power Switch 1 VIN
- ON0: Power Switch 0 ON
- ON1: Power Switch 1 ON

Programming Mode pin definitions are as follows:

- V_{DD}: V_{DD} power supply
- IO0: V_{PP} programming voltage
- IO6: Programming SCL
- IO7: Programming SDA
- GND: ground
- IO13: programming mode control

Of the 18 user defined IO pins on the SLG46517, all but one of the pins (IO0) can serve as both digital input and digital output. IO0 can only serve as a digital input pin.

5.1 INPUT MODES

Each IO pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. IOs 4, 5, 8, 9, 10, 11, and 12 can also be configured to serve as analog inputs to the on-chip comparators. IOs 15 and 16 can also be configured as analog reference voltage inputs.

5.2 OUTPUT MODES

IOs 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, and 17 can all be configured as digital output pins.

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5.3 PULL-UP/DOWN RESISTORS

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. In the case of IO0, the resistors are fixed to a Pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either Pull-up or Pull-downs.

5.4 IO REGISTER SETTINGS

Table 26: IO0 Register Settings

Signal Function	Register Bit Address	Register Definition
IO0 Pull-down Resistor Value Selection	[1028:1029]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO0 Mode Control	[1030:1031]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

Table 27: IO1 Register Settings

Signal Function	Register Bit Address	Register Definition
IO1 Pull-up/down Resistor Selection	[1033]	0: Pull-down Resistor 1: Pull-up Resistor
IO1 Pull-up/down Resistor Value Selection	[1035:1034]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO1 Mode Control (sig_IO1_oe = 0)	[1037:1036]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO1 Mode Control (sig_IO1_oe = 1)	[1039:1038]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 28: IO2 Register Settings

Signal Function	Register Bit Address	Register Definition
IO2 Driver Strength Selection	[1041]	0: 1x 1: 2x
IO2 Pull-up/down Resistor Selection	[1042]	0: Pull-down Resistor 1: Pull-up Resistor
IO2 Pull-up/down Resistor Value Selection	[1044:1043]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

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Table 28: IO2 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO2 Mode Control	[1047:1045]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved

Table 29: IO3 Register Settings

Signal Function	Register Bit Address	Register Definition
IO3 Pull-up/down Resistor Selection	[1049]	0: Pull-down Resistor 1: Pull-up Resistor
IO3 Pull-up/down Resistor Value Selection	[1051:1050]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO3 Mode Control (sig_IO3_oe = 0)	[1053:1052]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO3 Mode Control (sig_IO3_oe = 1)	[1055:1054]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 30: IO4 Register Settings

Signal Function	Register Bit Address	Register Definition
IO4 Driver Strength Selection	[1057]	0: 1x 1: 2x
IO4 Pull-up/down Resistor Selection	[1058]	0: Pull-down Resistor 1: Pull-up Resistor
IO4 Pull-up/down Resistor Value Selection	[1060:1059]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO4 Mode Control	[1063:1061]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain

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Table 31: IO5 Register Settings

Signal Function	Register Bit Address	Register Definition
IO5 Pull-up/down Resistor Selection	[1065]	0: Pull-down Resistor 1: Pull-up Resistor
IO5 Pull-up/down Resistor Value Selection	[1067:1066]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO5 Mode Control (sig_IO5_oe = 0)	[1069:1068]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO5 Mode Control (sig_IO5_oe = 1)	[1071:1070]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 32: IO6 Register Settings

Signal Function	Register Bit Address	Register Definition
IO6 Driver Strength Selection	[1073]	0: 1x 1: 2x
Select SCL & Virtual Input 0 or IO6	[1074]	0: SCL & Virtual Input 0 1: IO6
IO6 Pull-down Resistor Value Selection	[1076:1075]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO6 Mode Control	[1079:1077]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved

Table 33: IO7 Register Settings

Signal Function	Register Bit Address	Register Definition
IO7 (or SDA) Driver Strength Selection	[1081]	0: 1x 1: 2x
Select SDA & Virtual Input 1 or IO7	[1082]	0: SDA & Virtual Input 1 1: IO7
IO7 Pull-down Resistor Value Selection	[1084:1083]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

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Table 33: IO7 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO7 (or SDA) Mode Control	[1087:1085]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved

Table 34: IO8 Register Settings

Signal Function	Register Bit Address	Register Definition
IO8 4x Drive (4x, NMOS Open-Drain) Selection	[1088]	0: 4x Drive Off 1: 4x Drive On (if [884:882] = '101') (IO8 OE = 1 and PIN Mode is OD NMOS 1x)
IO8 Pull-up/down Resistor Selection	[1089]	0: Pull-down Resistor 1: Pull-up Resistor
IO8 Pull-up/down Resistor Value Selection	[1091:1090]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO8 Mode Control (sig_IO8_oe = 0)	[1093:1092]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO8 Mode Control (sig_IO8_oe = 1)	[1095:1094]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 35: IO9 Register Settings

Signal Function	Register Bit Address	Register Definition
IO9 4x Drive (4x, NMOS Open-Drain) Selection	[1096]	0: 4x Drive Off 1: 4x Drive On (if [892:890] = '101') (IO9 OE = 1 and PIN Mode is OD NMOS 1x)
IO9 Driver Strength Selection	[1097]	0: 1x 1: 2x
IO9 Pull-up/down Resistor Selection	[1098]	0: Pull-down Resistor 1: Pull-up Resistor
IO9 Pull-up/down Resistor Value Selection	[1100:1099]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

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Table 35: IO9 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO9 Mode Control	[1103:1101]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain

Table 36: IO10 Register Settings

Signal Function	Register Bit Address	Register Definition
IO10 Pull-up/down Resistor Selection	[1105]	0: Pull-down Resistor 1: Pull-up Resistor
IO10 Pull-up/down Resistor Value Selection	[1107:1106]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO10 Mode Control (sig_IO10_oe = 0)	[1109:1108]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO10 Mode Control (sig_IO10_oe = 1)	[1111:1110]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

Table 37: IO11 Register Settings

Signal Function	Register Bit Address	Register Definition
IO11 Pull-up/down Resistor Selection	[1113]	0: Pull-down Resistor 1: Pull-up Resistor
IO11 Pull-up/down Resistor Value Selection	[1115:1114]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO11 Mode Control (sig_IO11_oe = 0)	[1117:1116]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO11 Mode Control (sig_IO11_oe = 1)	[1119:1118]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

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Table 38: IO12 Register Settings

Signal Function	Register Bit Address	Register Definition
IO12 Driver Strength Selection	[1121]	0: 1x 1: 2x
IO12 Pull-up/down Resistor Selection	[1122]	0: Pull-down Resistor 1: Pull-up Resistor
IO12 Pull-up/down Resistor Value Selection	[1124:1123]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO12 Mode Control	[1127:1125]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain

Table 39: IO13 Register Settings

Signal Function	Register Bit Address	Register Definition
IO13 Pull-up/down Resistor Selection	[1129]	0: Pull-down Resistor 1: Pull-up Resistor
IO13 Pull-up/down Resistor Value Selection	[1131:1130]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO13 Mode Control (sig_IO13_oe = 1)	[1135:1134]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x
IO13 Mode Control (sig_IO13_oe = 0)	[1133:1132]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

Table 40: IO14 Register Settings

Signal Function	Register Bit Address	Register Definition
IO14 Driver Strength Selection	[1137]	0: 1x 1: 2x
IO14 Pull-up/down Resistor Selection	[1138]	0: Pull-down Resistor 1: Pull-up Resistor
IO14 Pull-up/down Resistor Value Selection	[1140:1139]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

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Table 40: IO14 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
IO14 Mode Control	[1143:1141]	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved

Table 41: IO15 Register Settings

Signal Function	Register Bit Address	Register Definition
IO15 Pull-up/down Resistor Selection	[1145]	0: Pull-down Resistor 1: Pull-up Resistor
IO15 Pull-up/down Resistor Value Selection	[1147:1146]	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO15 Mode Control (sig_io15_oe = 0)	[1149:1148]	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO15 Mode Control (sig_io15_oe = 1)	[1151:1150]	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x

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5.5 GPI STRUCTURE

5.5.1 GPI Structure (for IO0)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

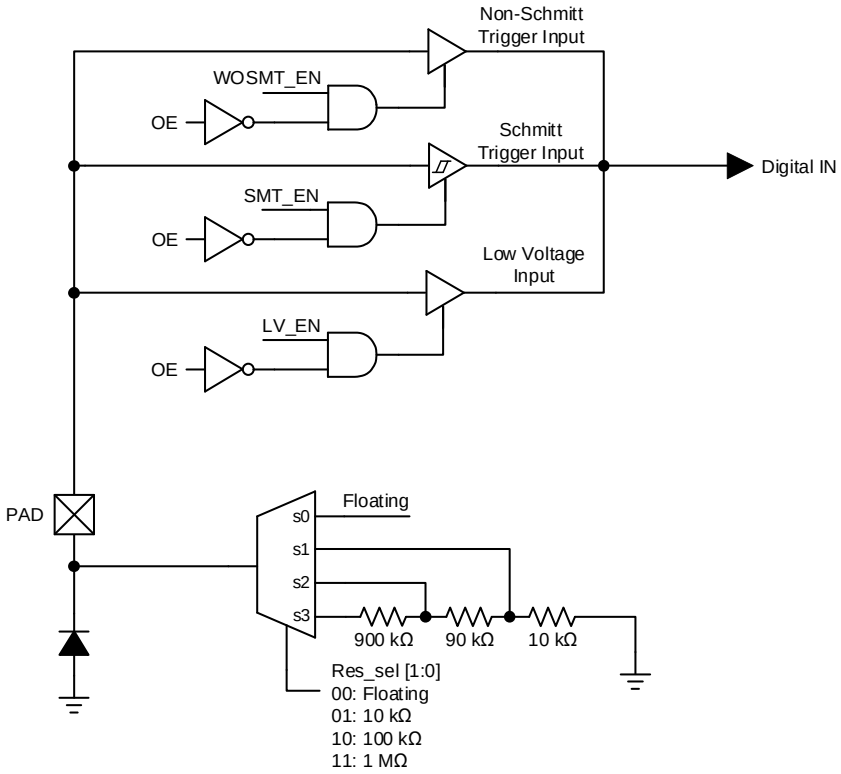


Figure 3: IO0 GPI Structure Diagram

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5.6 MATRIX OE IO STRUCTURE

5.6.1 Matrix OE IO Structure (for IOs 1, 3, 5, 10, 11, 13, 15)

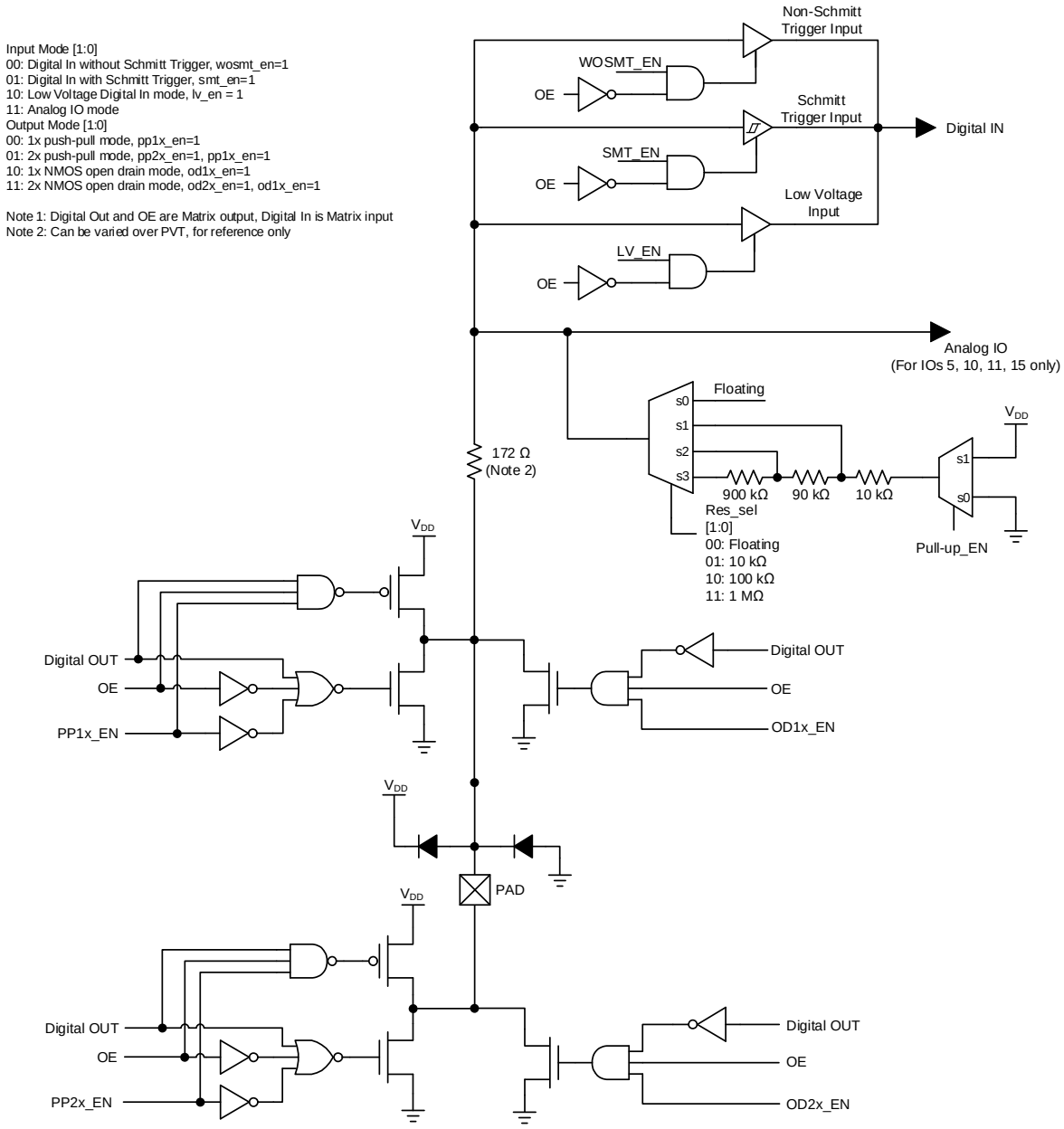


Figure 4: Matrix OE IO Structure Diagram

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5.6.2 Matrix OE IO Structure (for IOs 6 and 7)

IO6, IO7 Mode [2:0]
000: Digital Input without Schmitt Trigger
001: Digital Input with Schmitt Trigger
010: Low Voltage Digital Input
011: Reserved
100: Reserved
101: Open Drain NMOS
110: Reserved
111: Reserved

Note: Digital Out and OE are Matrix output, Digital In is Matrix input

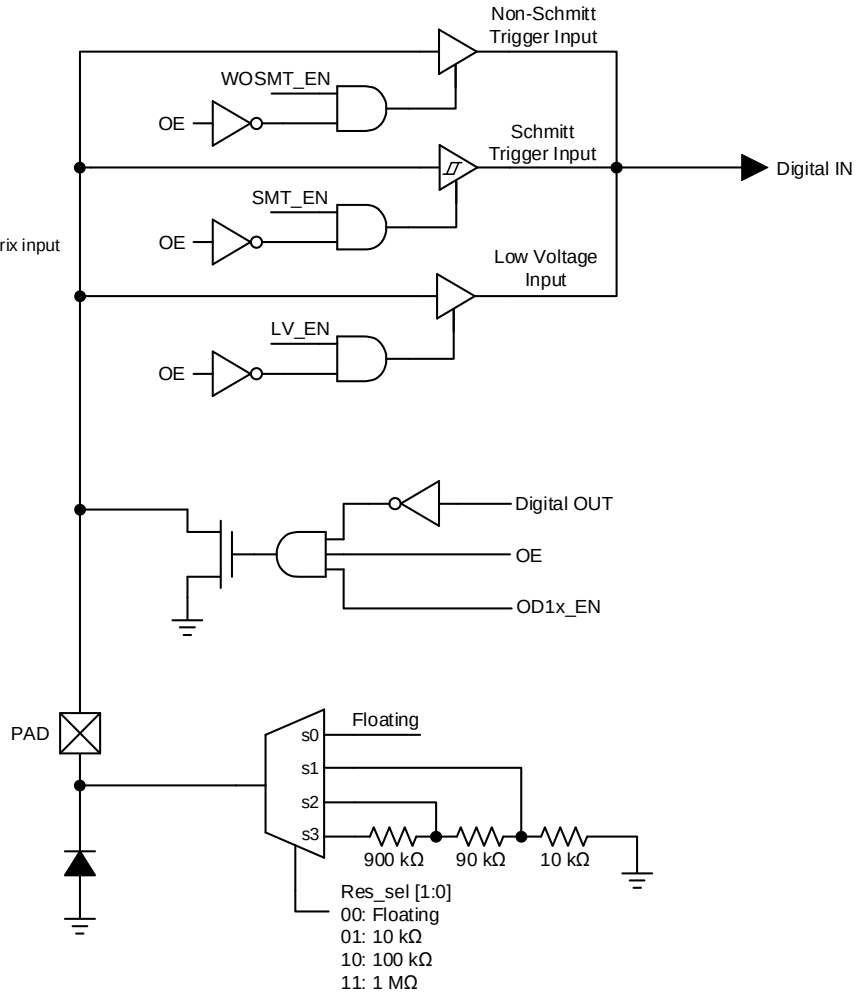


Figure 5: Matrix OE IO Structure Diagram

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5.6.3 Matrix OE 4x Drive Structure (for IO8)

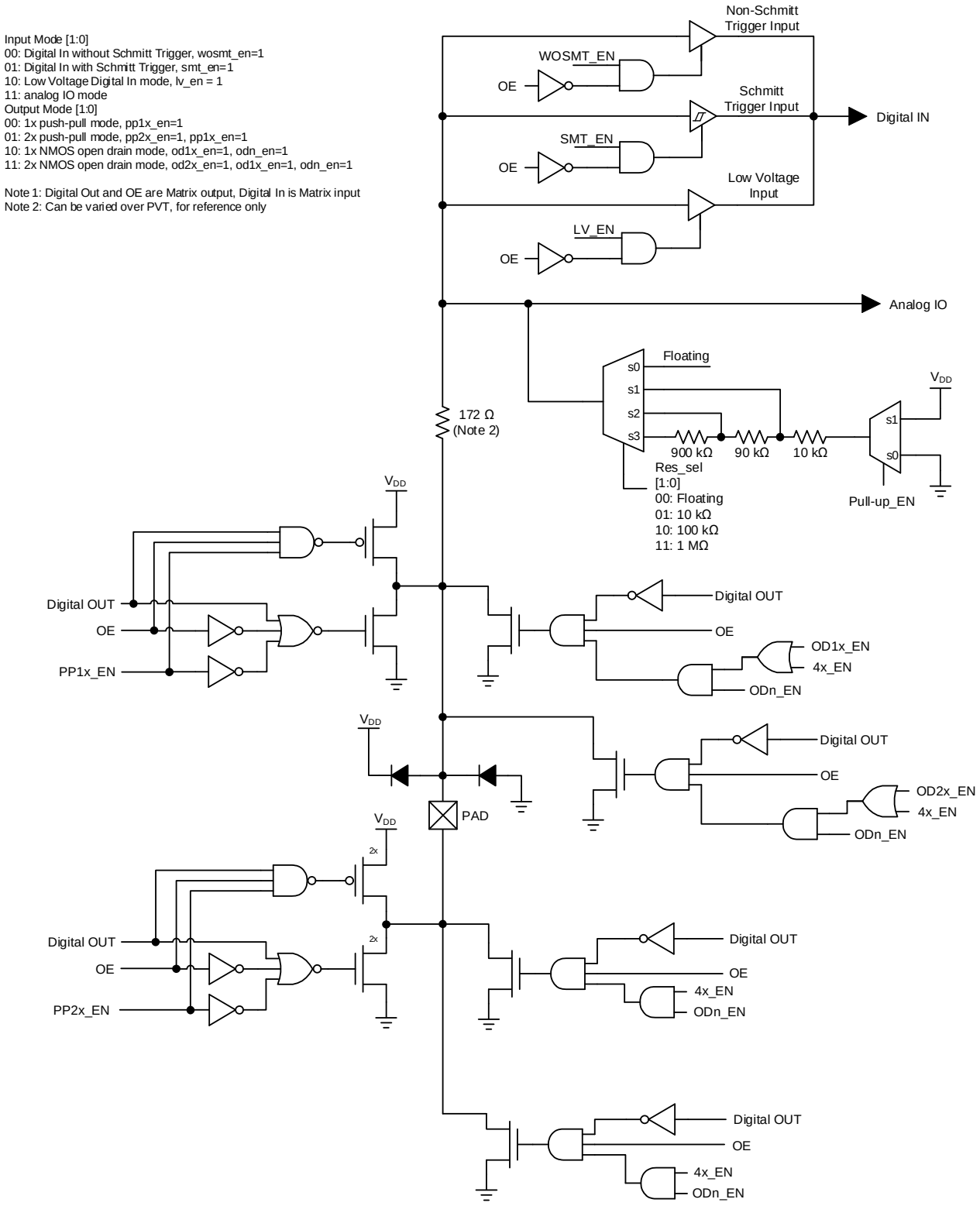


Figure 6: Matrix OE IO 4X Drive Structure Diagram

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5.7 IO STRUCTURE

5.7.1 IO Structure (for IOs 2, 4, 12, 14)

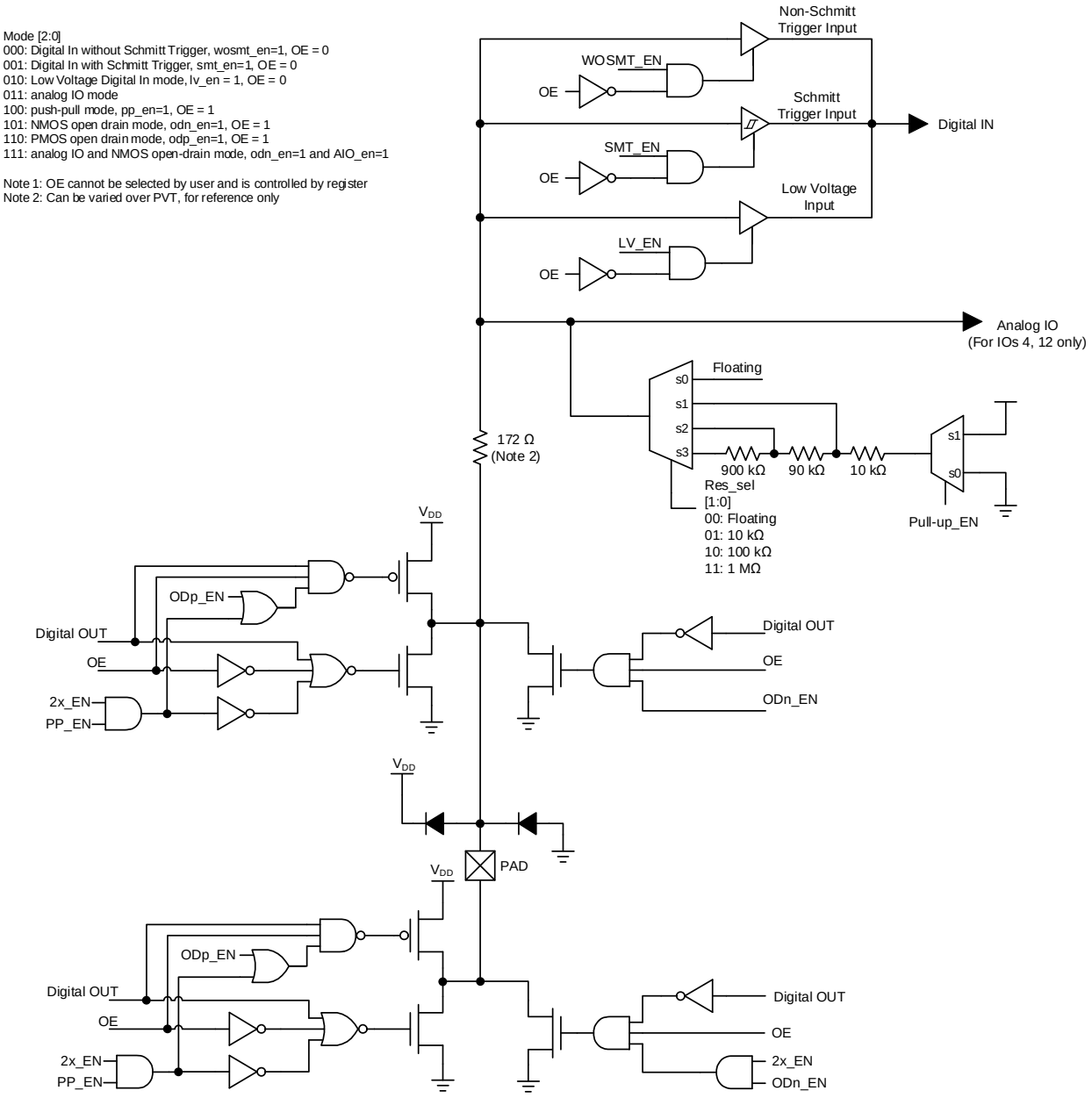


Figure 7: IO Structure Diagram

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5.7.2 4x Drive Structure (for IO9)

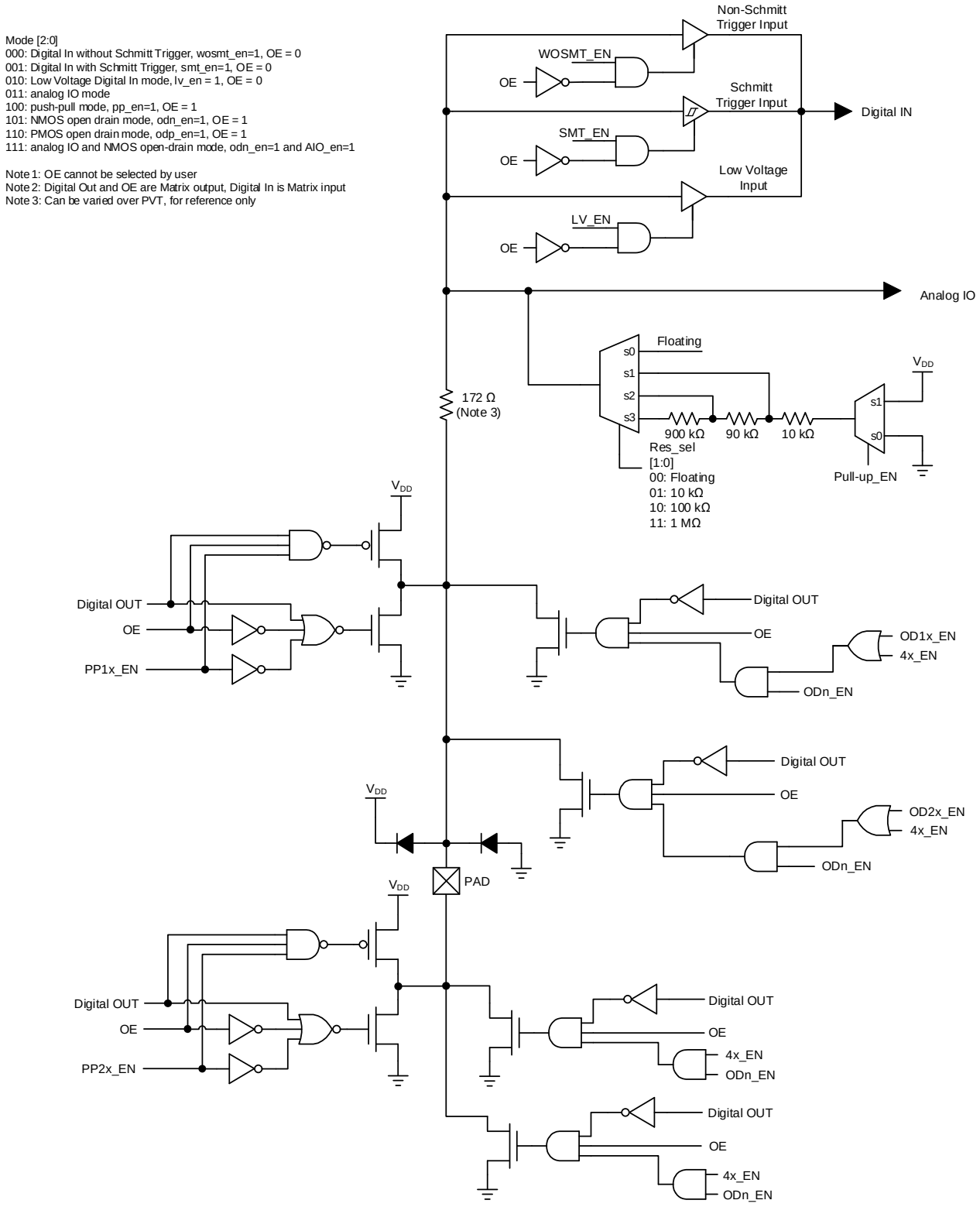


Figure 8: IO 4X Drive Structure Diagram

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6 Connection Matrix

The Connection Matrix in the SLG46517 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46517 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low”, based on the design that is created. Once the 2048 register bits within the SLG46517 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 110 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46517’s register table, see Section 20.

Matrix Input Signal Functions	N
Ground	0
IO0 Digital In	1
IO1 Digital In	2
IO2 Digital In	3
⋮	⋮
Resetb_core	62
V_{DD}	63

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	109
Registers	[5:0]	[13:8]	[21:16]	⋯	[877:872]
Function	Matrix OUT: ASM-state0-EN0	Matrix OUT: ASM-state0-EN1	Matrix OUT: ASM-state0-EN2	⋯	Matrix OUT: PD of either Temp out or XTAL Osc

Figure 9: Connection Matrix

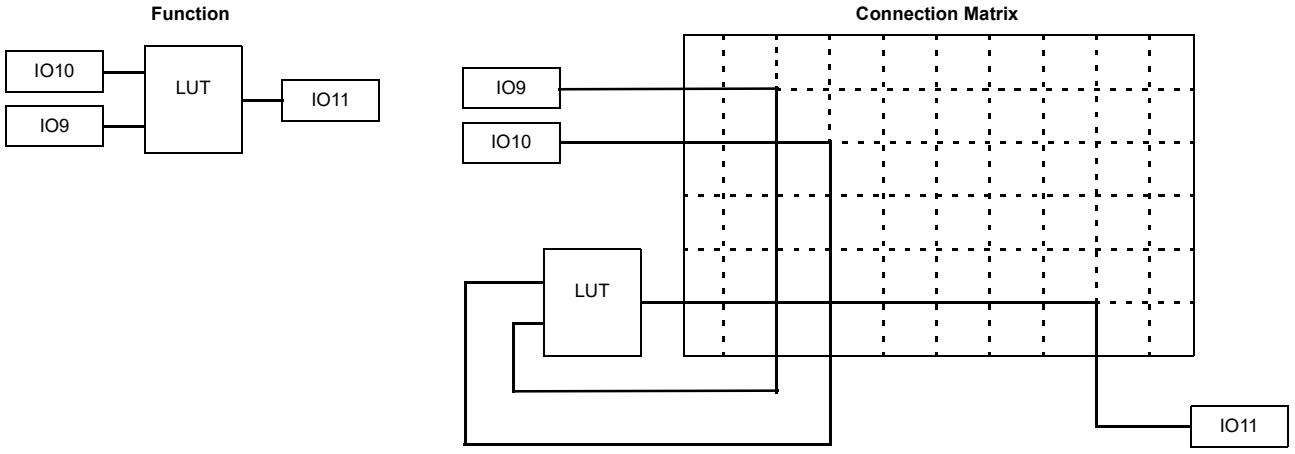


Figure 10: Connection Matrix Example

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6.1 MATRIX INPUT TABLE

Table 42: Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	IO2 Digital Input	0	0	0	0	1	1
4	IO3 Digital Input	0	0	0	1	0	0
5	IO4 Digital Input	0	0	0	1	0	1
6	IO5 Digital Input	0	0	0	1	1	0
7	IO8 Digital Input	0	0	0	1	1	1
8	LUT2_0/DFF0 Output	0	0	1	0	0	0
9	LUT2_1/DFF1 Output	0	0	1	0	0	1
10	LUT2_2/DFF2 Output	0	0	1	0	1	0
11	LUT2_3/PGen Output	0	0	1	0	1	1
12	LUT3_0/DFF3 Output	0	0	1	1	0	0
13	LUT3_1/DFF4 Output	0	0	1	1	0	1
14	LUT3_2/DFF5 Output	0	0	1	1	1	0
15	LUT3_3/DFF6 Output	0	0	1	1	1	1
16	LUT3_4/DFF7 Output	0	1	0	0	0	0
17	LUT3_5/CNT_DLY2(8bit) Output	0	1	0	0	0	1
18	LUT3_6/CNT_DLY3(8bit) Output	0	1	0	0	1	0
19	LUT3_7/CNT_DLY4(8bit) Output	0	1	0	0	1	1
20	LUT3_8/CNT_DLY5(8bit) Output	0	1	0	1	0	0
21	LUT3_9/CNT_DLY6(8bit) Output	0	1	0	1	0	1
22	LUT4_0/CNT_DLY0(16bit) Output	0	1	0	1	1	0
23	LUT4_1/CNT_DLY1(16bit) Output	0	1	0	1	1	1
24	LUT3_10/Pipe Delay (1st stage) Output	0	1	1	0	0	0
25	Pipe Delay Output0	0	1	1	0	0	1
26	Pipe Delay Output1	0	1	1	0	1	0
27	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25kHz/2MHz)	0	1	1	0	1	1
28	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output (25kHz/2MHz)	0	1	1	1	0	0
29	Internal OSC Pre-Divided by 1/2/4/8 Output (25MHz)	0	1	1	1	0	1
30	Filter0/Edge Detect0 Output	0	1	1	1	1	0
31	Filter1/Edge Detect1 Output	0	1	1	1	1	1
32	IO6 Digital or I^2C_virtual_0 Input	1	0	0	0	0	0
33	IO7 Digital or I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0

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Table 42: Matrix Input Table(Continued)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	ASM-stateX-dout0	1	0	1	0	0	0
41	ASM-stateX-dout1	1	0	1	0	0	1
42	ASM-stateX-dout2	1	0	1	0	1	0
43	ASM-stateX-dout3	1	0	1	0	1	1
44	ASM-stateX-dout4	1	0	1	1	0	0
45	ASM-stateX-dout5	1	0	1	1	0	1
46	ASM-stateX-dout6	1	0	1	1	1	0
47	ASM-stateX-dout7	1	0	1	1	1	1
48	IO9 Digital Input	1	1	0	0	0	0
49	IO10 Digital Input	1	1	0	0	0	1
50	IO11 Digital Input	1	1	0	0	1	0
51	IO12 Digital Input	1	1	0	0	1	1
52	IO13 Digital Input	1	1	0	1	0	0
53	IO14 Digital Input	1	1	0	1	0	1
54	IO15 Digital Input	1	1	0	1	1	0
55	Power Switch ON0, Digital Input	1	1	0	1	1	1
56	Power Switch ON1, Digital Input	1	1	1	0	0	0
57	ACMP_0 Output	1	1	1	0	0	1
58	ACMP_1 Output	1	1	1	0	1	0
59	ACMP_2 Output	1	1	1	0	1	1
60	ACMP_3 Output	1	1	1	1	0	0
61	Programmable Delay with Edge Detector Output	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

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6.2 MATRIX OUTPUT TABLE

Table 43: Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
7:0	Matrix OUT: ASM-state0-EN0	0
15:8	Matrix OUT: ASM-state0-EN1	1
23:16	Matrix OUT: ASM-state0-EN2	2
31:24	Matrix OUT: ASM-state1-EN0	3
39:32	Matrix OUT: ASM-state1-EN1	4
47:40	Matrix OUT: ASM-state1-EN2	5
55:48	Matrix OUT: ASM-state2-EN0	6
63:56	Matrix OUT: ASM-state2-EN1	7
71:64	Matrix OUT: ASM-state2-EN2	8
79:72	Matrix OUT: ASM-state3-EN0	9
87:80	Matrix OUT: ASM-state3-EN1	10
95:88	Matrix OUT: ASM-state3-EN2	11
103:96	Matrix OUT: ASM-state4-EN0	12
111:104	Matrix OUT: ASM-state4-EN1	13
119:112	Matrix OUT: ASM-state4-EN2	14
127:120	Matrix OUT: ASM-state5-EN0	15
135:128	Matrix OUT: ASM-state5-EN1	16
143:136	Matrix OUT: ASM-state5-EN2	17
151:144	Matrix OUT: ASM-state6-EN0	18
159:152	Matrix OUT: ASM-state6-EN1	19
167:160	Matrix OUT: ASM-state6-EN2	20
175:168	Matrix OUT: ASM-state7-EN0	21
183:176	Matrix OUT: ASM-state7-EN1	22
191:184	Matrix OUT: ASM-state7-EN2	23
199:192	Matrix OUT: ASM-state-nRST	24
207:200	Matrix OUT: IO1 Digital Output Source	25
215:208	Matrix OUT: IO1 Output Enable	26
223:216	Matrix OUT: IO2 Digital Output Source	27
231:224	Matrix OUT: IO3 Digital Output Source	28
239:232	Matrix OUT: IO3 Output Enable	29
247:240	Matrix OUT: IO4 Digital Output Source	30
255:248	Matrix OUT: IO5 Digital Output Source	31
263:256	Matrix OUT: IO5 Output Enable	32
271:264	Matrix OUT: IO6 Digital Output Source (SCL with VI/Input & NMOS Open-Drain)	33
279:272	Matrix OUT: IO7 Digital Output Source (SDA with VI/Input & NMOS Open-Drain)	34
287:280	Matrix OUT: IO8 Digital Output Source	35
295:288	Matrix OUT: IO8 Output Enable	36
303:296	Matrix OUT: IO9 Digital Output Source	37

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Table 43: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
311:304	Matrix OUT: IO10 Digital Output Source	38
319:312	Matrix OUT: IO10 Output Enable	39
327:320	Matrix OUT: IO11 Digital Output Source	40
335:328	Matrix OUT: IO11 Output Enable	41
343:336	Matrix OUT: IO12 Digital Output Source	42
351:344	Matrix OUT: IO13 Digital Output Source	43
359:352	Matrix OUT: IO13 Output Enable	44
367:360	Matrix OUT: IO14 Digital Output Source	45
375:368	Matrix OUT: IO15 Digital Output Source	46
383:376	Matrix OUT: IO15 Output Enable	47
391:384	Matrix OUT: Power Switch ON0, Digital Output Source	48
399:392	Matrix OUT: Reserved	49
407:400	Matrix OUT: Power Switch ON1, Digital Output Source	50
415:408	Matrix OUT: ACMP0 PWR UP	51
423:416	Matrix OUT: ACMP1 PWR UP	52
431:424	Matrix OUT: ACMP2 PWR UP	53
439:432	Matrix OUT: ACMP3 PWR UP	54
447:440	Matrix OUT: Input of Filter_0 with fixed time edge detector	55
455:448	Matrix OUT: Input of Filter_1 with fixed time edge detector	56
463:456	Matrix OUT: Input of Programmable Delay & Edge Detector	57
471:464	Matrix OUT: OSC 25kHz/2MHz PDB (Power-Down)	58
479:472	Matrix OUT: OSC 25MHz PDB (Power-Down)	59
487:480	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0	60
495:488	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0	61
503:496	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1	62
511:504	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1	63
519:512	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2	64
527:520	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2	65
535:528	Matrix OUT: IN0 of LUT2_3 or Clock Input of PGen	66
543:536	Matrix OUT: IN1 of LUT2_3 or nRST of PGen	67
551:544	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3	68
559:552	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3	69
567:560	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3	70
575:568	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4	71
583:576	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4	72
591:584	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4	73
599:592	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5	74
607:600	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5	75
615:608	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5	76

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Table 43: Matrix Output Table(Continued)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
623:616	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6	77
631:624	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6	78
639:632	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6	79
647:640	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7	80
655:648	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7	81
663:656	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7	82
671:664	Matrix OUT: IN0 of LUT3_5 or Delay2 Input (or Counter2 RST Input)	83
679:672	Matrix OUT: IN1 of LUT3_5 or External Clock Input of Delay2 (or Counter2)	84
687:680	Matrix OUT: IN2 of LUT3_5	85
695:688	Matrix OUT: IN0 of LUT3_6 or Delay3 Input (or Counter3 RST Input)	86
703:696	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay3 (or Counter3)	87
711:704	Matrix OUT: IN2 of LUT3_6	88
719:712	Matrix OUT: IN0 of LUT3_7 or Delay4 Input (or Counter4 RST Input)	89
727:720	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay4 (or Counter4)	90
735:728	Matrix OUT: IN2 of LUT3_7	91
743:736	Matrix OUT: IN0 of LUT3_8 or Delay5 Input (or Counter5 RST Input)	92
751:744	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay5 (or Counter5)	93
759:752	Matrix OUT: IN2 of LUT3_8	94
767:760	Matrix OUT: IN0 of LUT3_9 or Delay6 Input (or Counter6 RST Input)	95
775:768	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay6 (or Counter6)	96
783:776	Matrix OUT: IN2 of LUT3_9	97
791:784	Matrix OUT: IN0 of LUT3_10 or Input of Pipe Delay	98
799:792	Matrix OUT: IN1 of LUT3_10 or nRST of Pipe Delay	99
807:800	Matrix OUT: IN2 of LUT3_10 or Clock of Pipe Delay	100
815:808	Matrix OUT: IN0 of LUT4_0 or Delay0 Input (or Counter0 RST/SET Input)	101
823:816	Matrix OUT: IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0)	102
831:824	Matrix OUT: IN2 of LUT4_0 or UP Input of FSM0	103
839:832	Matrix OUT: IN3 of LUT4_0 or KEEP Input of FSM0	104
847:840	Matrix OUT: IN0 of LUT4_1 or Delay1 Input (or Counter1 RST/SET Input)	105
855:848	Matrix OUT: IN1 of LUT4_1 or External Clock Input of Delay1 (or Counter1)	106
863:856	Matrix OUT: IN2 of LUT4_1 or UP Input of FSM1	107
871:864	Matrix OUT: IN3 of LUT4_1 or KEEP Input of FSM1	108
879:872	Matrix OUT: crystal oscillator by register [1268]	109
Note 1 For each Address, the two most significant bits are unused.		

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6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0244.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs,(IO6 Digital or I^2C_virtual_0 Input) and (IO7 Digital or I^2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. Two register bits select whether the Connection Matrix input comes from the pin input or from the virtual register:

- register [1074] Select SCL & Virtual Input 0 or IO6
- register [1082] Select SDA & Virtual Input 1 or IO7

See Table 44 for Connection Matrix Virtual Inputs.

Table 44: Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[1952]
33	I^2C_virtual_1 Input	[1953]
34	I^2C_virtual_2 Input	[1954]
35	I^2C_virtual_3 Input	[1955]
36	I^2C_virtual_4 Input	[1956]
37	I^2C_virtual_5 Input	[1957]
38	I^2C_virtual_6 Input	[1958]
39	I^2C_virtual_7 Input	[1959]

6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are at bytes 0240 to 0247. Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0244).

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7 Combination Function Macrocells

The SLG46517 has seventeen combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops
- Five macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays
- Two macrocells that can serve as either 4-bit LUTs or as 16-Bit Counter/Delays

Inputs/Outputs for the 17 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There are three macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change
- LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

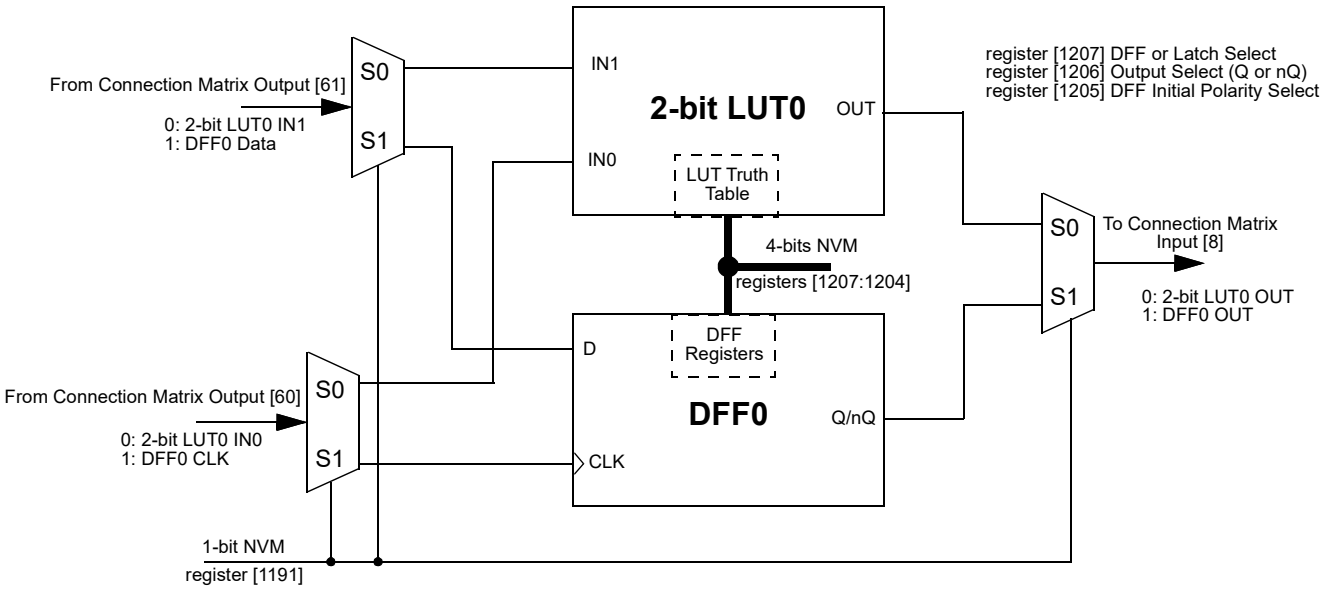


Figure 11: 2-bit LUT0 or DFF0

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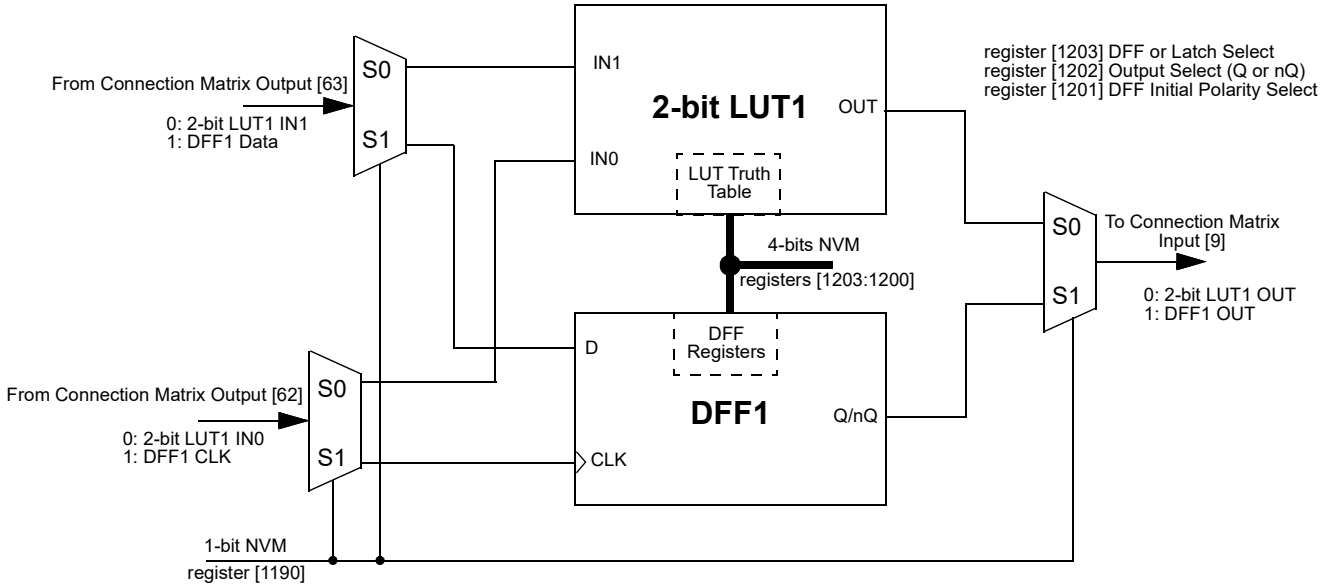


Figure 12: 2-bit LUT1 or DFF1

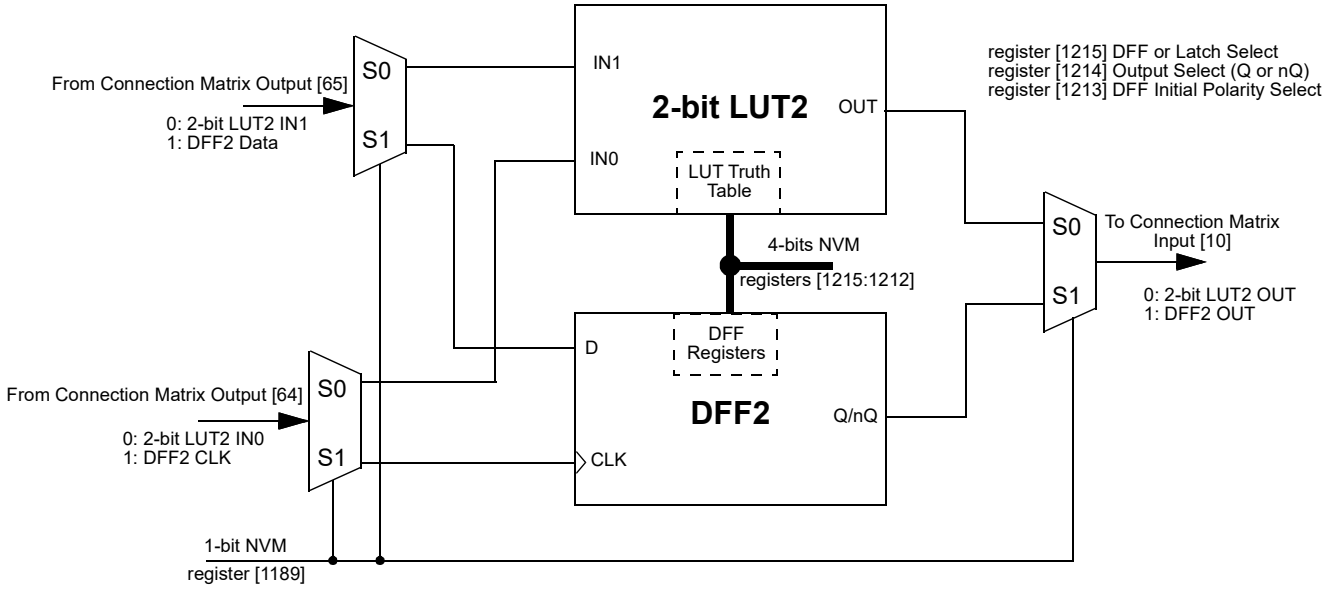


Figure 13: 2-bit LUT2 or DFF2

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7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUTs

Table 45: 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1204]	LSB
0	1	register [1205]	
1	0	register [1206]	
1	1	register [1207]	MSB

Table 46: 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1200]	LSB
0	1	register [1201]	
1	0	register [1202]	
1	1	register [1203]	MSB

Table 47: 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1212]	LSB
0	1	register [1213]	
1	0	register [1214]	
1	1	register [1215]	MSB

Each macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by registers [1207:1204]

2-Bit LUT1 is defined by registers [1203:1200]

2-Bit LUT2 is defined by registers [1215:1212]

Table 48 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 48: 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

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7.1.2 2-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 49: DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_0 or DFF0 Select	[1191]	0: LUT2_0 1: DFF0
DFF0 Initial Polarity Select	[1205]	0: Low 1: High
DFF0 Output Select	[1206]	0: Q output 1: nQ output
DFF0 or LATCH Select	[1207]	0: DFF function 1: LATCH function

Table 50: DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_1 or DFF1 Select	[1190]	0: LUT2_1 1: DFF1
DFF1 Initial Polarity Select	[1201]	0: Low 1: High
DFF1 Output Select	[1202]	0: Q output 1: nQ output
Select or LATCH select	[1203]	0: DFF function 1: LATCH function

Table 51: DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_2 or DFF2 Select	[1189]	0: LUT2_2 1: DFF2
DFF2 Initial Polarity Select	[1213]	0: Low 1: High
DFF2 Output Select	[1214]	0: Q output 1: nQ output
DFF2 or LATCH Select	[1215]	0: DFF function 1: LATCH function

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7.1.3 Initial Polarity Operations

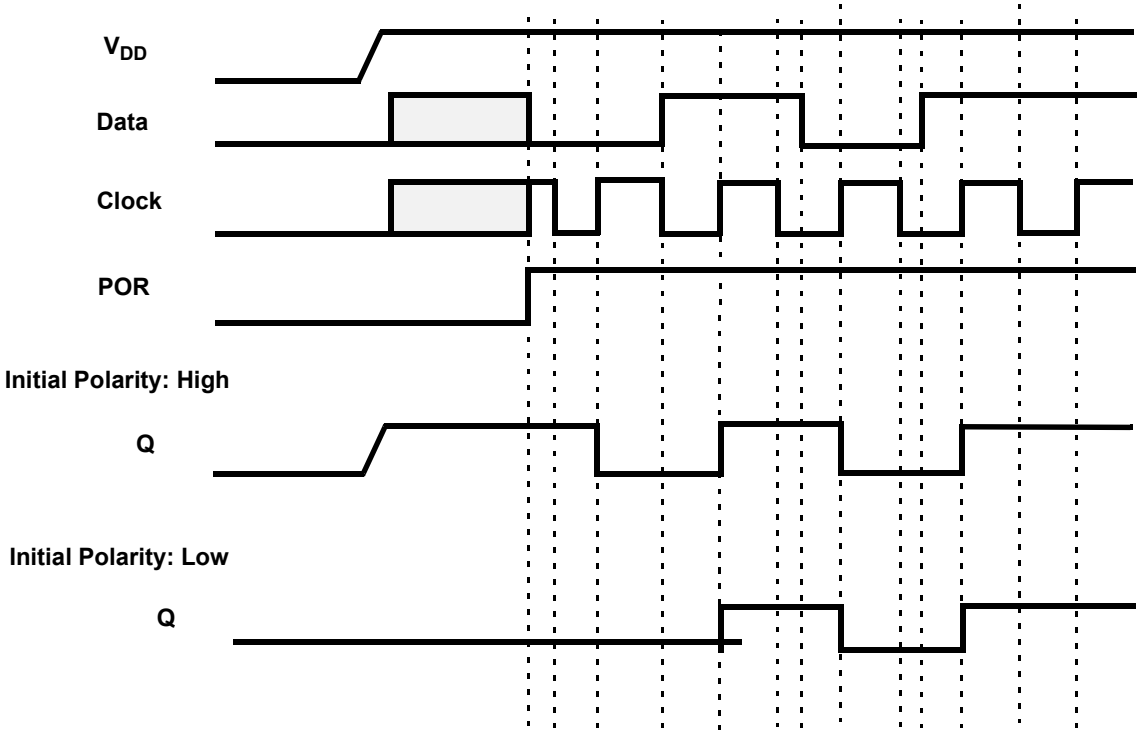


Figure 14: DFF Polarity Operations

7.2 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are five macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip-Flop, or two D Flip-Flops in series, with the first D Flip-Flop triggering on the rising clock edge, and the second D Flip-Flop triggering on the falling clock edge.

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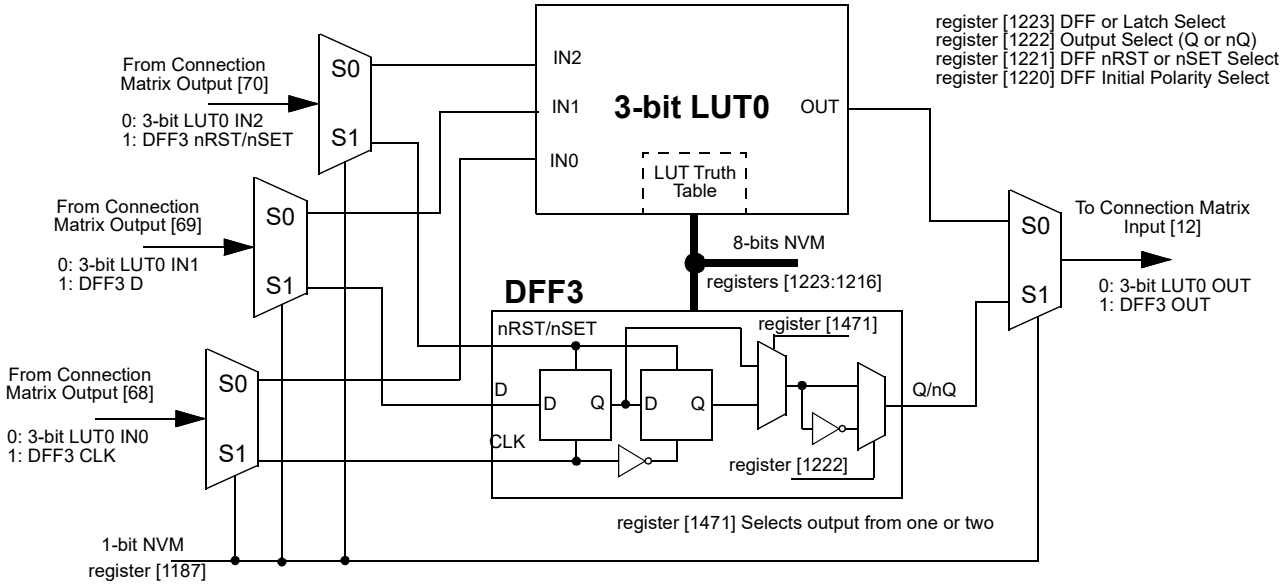


Figure 15: 3-bit LUT0 or DFF3 with RST/SET

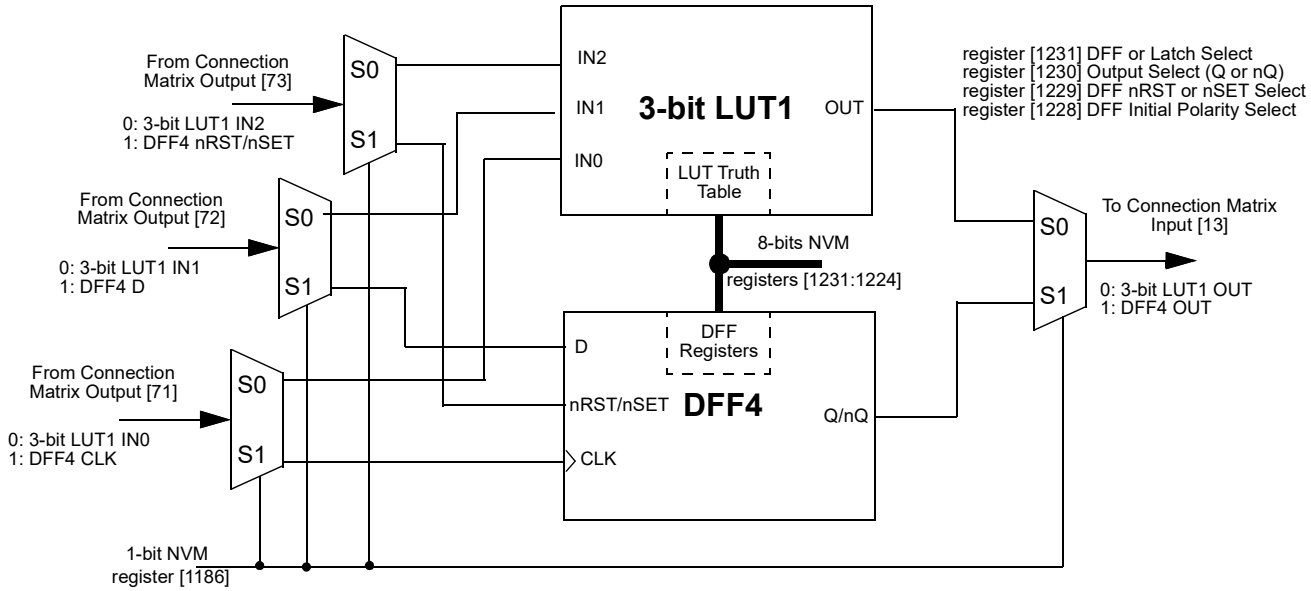


Figure 16: 3-bit LUT1 or DFF4 with RST/SET

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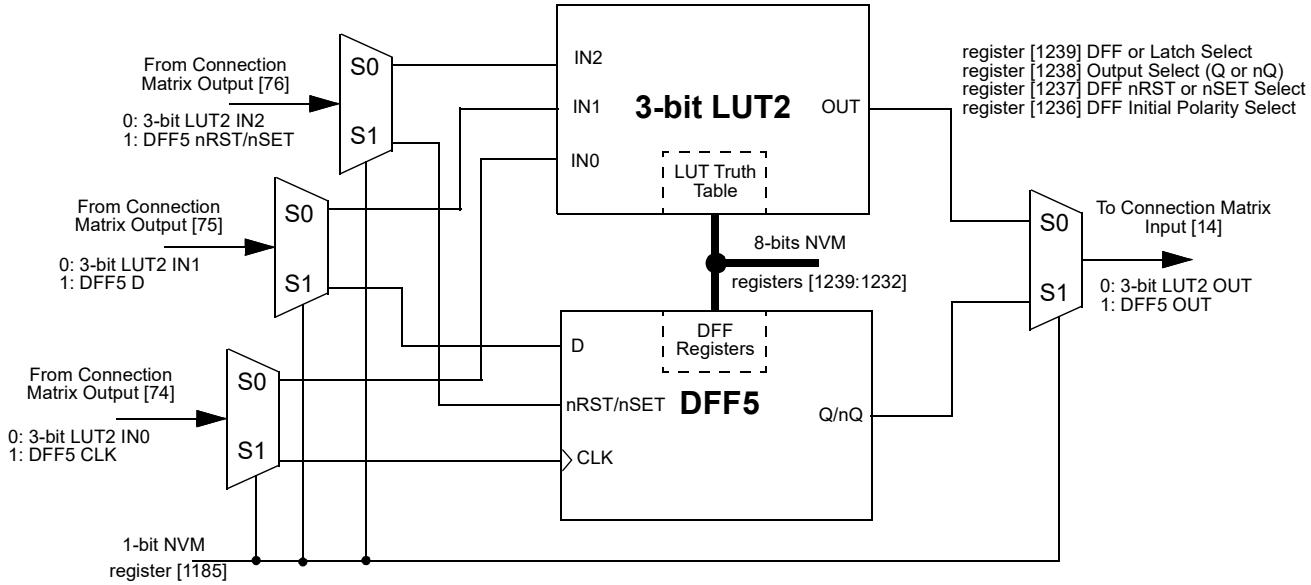


Figure 17: 3-bit LUT2 or DFF5 with RST/SET

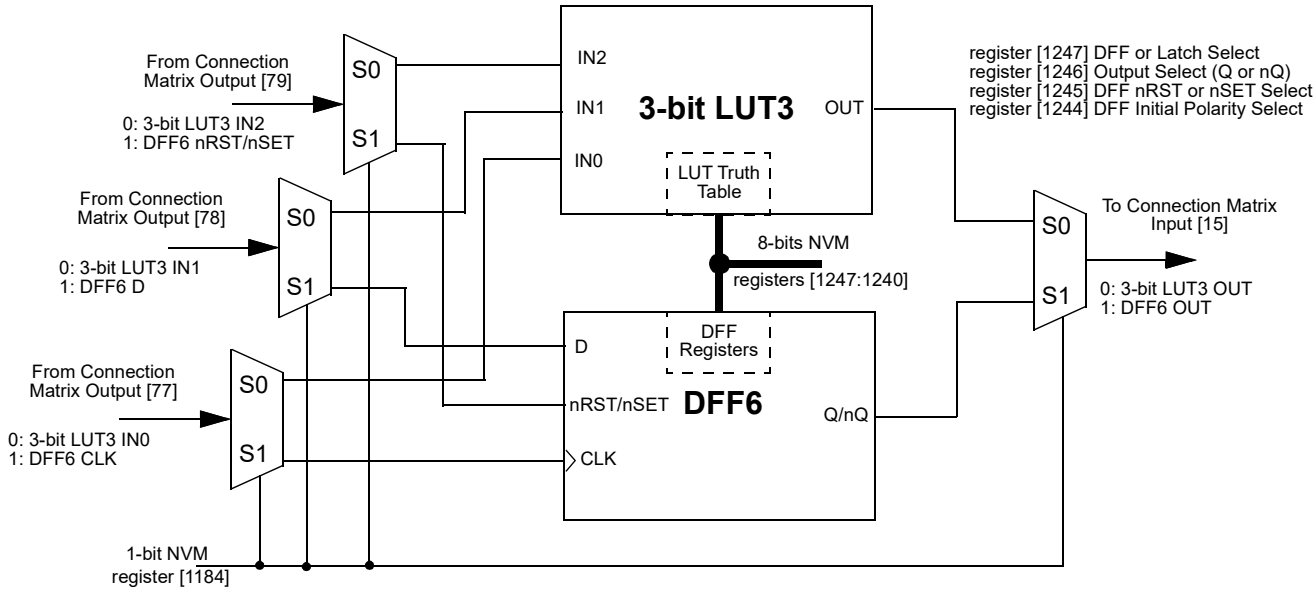


Figure 18: 3-bit LUT3 or DFF6 with RST/SET

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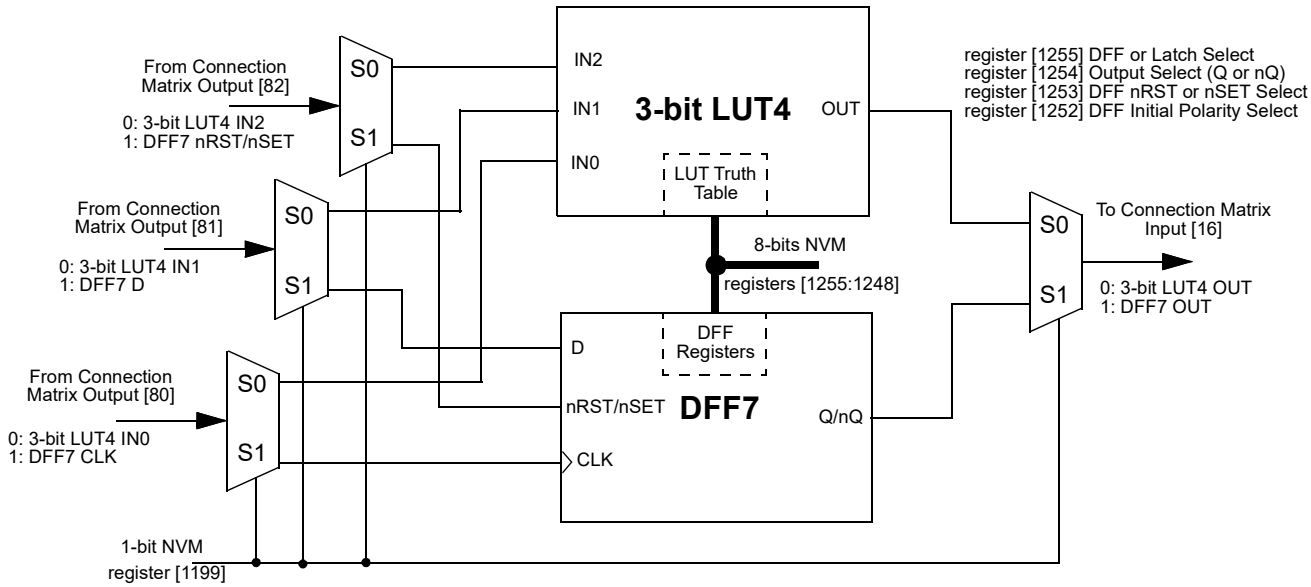


Figure 19: 3-bit LUT4 or DFF7 with RST/SET

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7.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 52: 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1216]	LSB
0	0	1	register [1217]	
0	1	0	register [1218]	
0	1	1	register [1219]	
1	0	0	register [1220]	
1	0	1	register [1221]	
1	1	0	register [1222]	
1	1	1	register [1223]	MSB

Table 53: 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 54: 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1232]	LSB
0	0	1	register [1233]	
0	1	0	register [1234]	
0	1	1	register [1235]	
1	0	0	register [1236]	
1	0	1	register [1237]	
1	1	0	register [1238]	
1	1	1	register [1239]	MSB

Table 55: 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Table 56: 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1248]	LSB
0	0	1	register [1249]	
0	1	0	register [1250]	
0	1	1	register [1251]	
1	0	0	register [1252]	
1	0	1	register [1253]	
1	1	0	register [1254]	
1	1	1	register [1255]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by registers [1223:1216]

3-Bit LUT1 is defined by registers [1231:1224]

3-Bit LUT2 is defined by registers [1239:1232]

3-Bit LUT3 is defined by registers [1247:1240]

3-Bit LUT5 is defined by registers [1255:1248]

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Table 57 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 57: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.2.2 3-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 58: DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_0 or DFF3 Select	[1187]	0: LUT3_0 1: DFF3
DFF3 Initial Polarity Select	[1220]	0: Low 1: High
DFF3 nRST/nSET Select	[1221]	1: nSET from matrix out 0: nRST from matrix out
DFF3 Output Select	[1222]	0: Q output 1: nQ output
DFF3 or LATCH Select	[1223]	0: DFF function 1: LATCH function

Table 59: DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_1 or DFF4 Select	[1186]	0: LUT3_1 1: DFF4
DFF4 Initial Polarity Select	[1128]	0: Low 1: High
DFF4 nRST/nSET Select	[1129]	1: nSET from matrix out 0: nRST from matrix out
DFF4 Output Select	[1130]	0: Q output 1: nQ output
DFF4 or LATCH Select	[1131]	0: DFF function 1: LATCH function

Table 60: DFF5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_2 or DFF5 Select	[1185]	0: LUT3_2 1: DFF5
DFF5 Initial Polarity Select	[1236]	0: Low 1: High

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Table 60: DFF5 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
DFF5 nRST/nSET Select	[1237]	1: nSET from matrix out 0: nRST from matrix out
DFF5 Output Select	[1238]	0: Q output 1: nQ output
DFF5 or LATCH Select	[1239]	0: DFF function 1: LATCH function

Table 61: DFF6 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_3 or DFF6 Select	[1184]	0: LUT3_3 1: DFF6
DFF6 Initial Polarity Select	[1244]	0: Low 1: High
DFF6 nRST/nSET Select	[1245]	1: nSET from matrix out 0: nRST from matrix out
DFF6 Output Select	[1246]	0: Q output 1: nQ output
DFF6 or LATCH Select	[1247]	0: DFF function 1: LATCH function

Table 62: DFF7 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_4 or DFF7 Select	[1199]	0: LUT3_4 1: DFF7
DFF7 Initial Polarity Select	[1252]	0: Low 1: High
DFF7 nRST/nSET Select	[1253]	1: nSET from matrix out 0: nRST from matrix out
DFF7 Output Select	[1254]	0: Q output 1: nQ output
DFF7 or LATCH Select	[1255]	0: DFF function 1: LATCH function

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7.2.3 Initial Polarity Operations

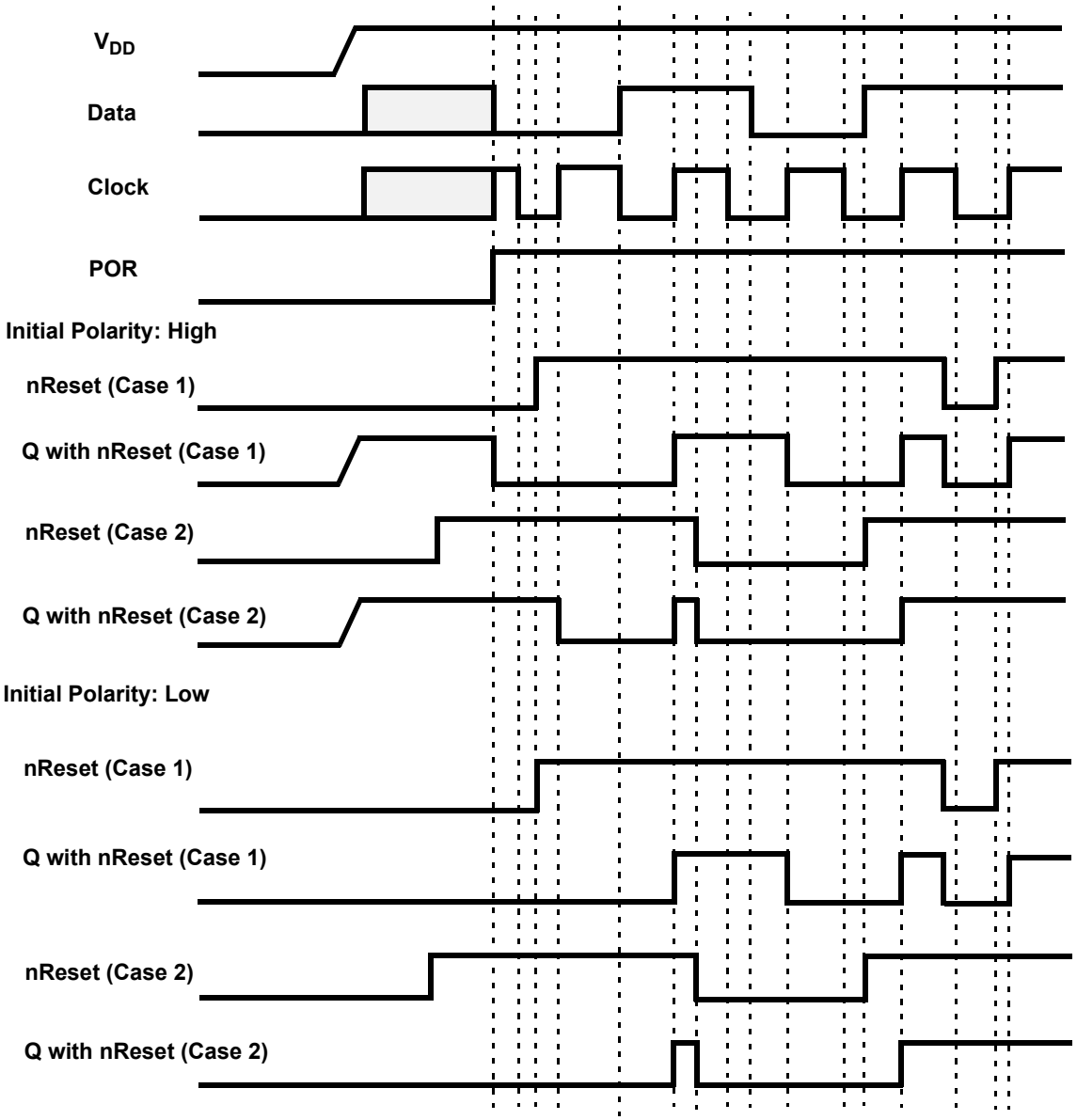


Figure 20: DFF Polarity Operations with nReset

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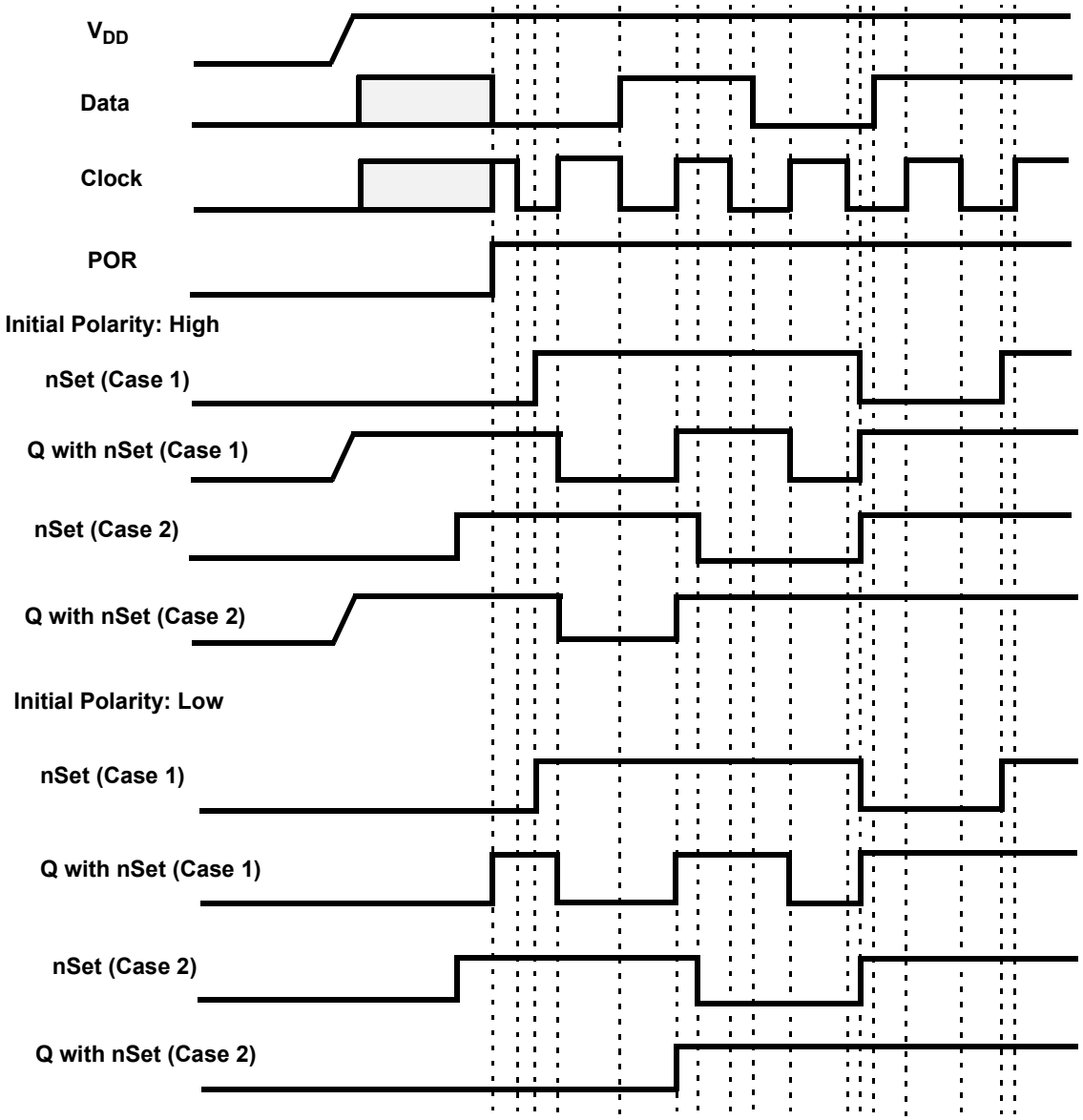


Figure 21: DFF Polarity Operations with nSet

7.3 3-BIT LUT OR PIPE DELAY MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix: Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first Flip-Flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input mux that is controlled by registers [1259:1256] for OUT0 and registers [1263:1260] for OUT1. The 16-input mux is used to select the amount of delay.

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The overall time of the delay is based on the clock used in the SLG46517 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46517). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

Note: CLK is rising edge triggered.

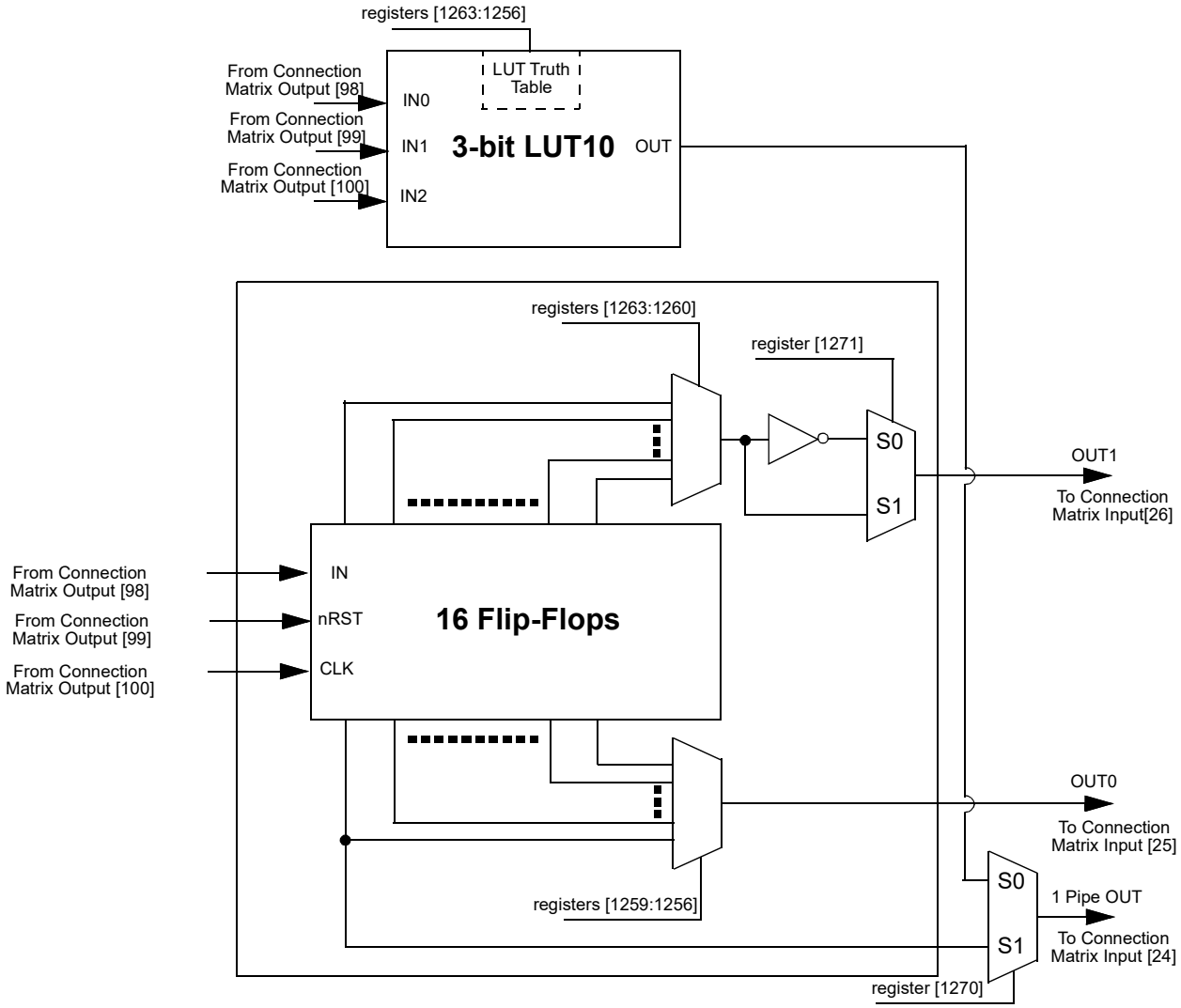


Figure 22: 3-bit LUT10 or Pipe Delay

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7.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 63: 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1256]	LSB
0	0	1	register [1257]	
0	1	0	register [1258]	
0	1	1	register [1259]	
1	0	0	register [1260]	
1	0	1	register [1261]	
1	1	0	register [1262]	
1	1	1	register [1263]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT10 is defined by registers [1263:1256]

7.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 64: Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_10 or Pipe Delay Output Select	[1270]	0: LUT3_10 1: 1 Pipe Delay Output
OUT0 select	[1259:1256]	
OUT1 select	[1263:1260]	
Pipe delay OUT1 Polarity Select Bit	[1271]	0: Non-inverted 1: Inverted

7.4 3-BIT LUT OR 8-BIT COUNTER/DELAY MACROCELLS

There are five macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the three input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the counter/delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

For timing diagrams refer to Section 7.6

Note Counters initialize with counter data after POR.

Two of the five macrocells can have their active count value read via I^2C (CNT4 and CNT6). See Section 17.6.1 for further details.

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7.4.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

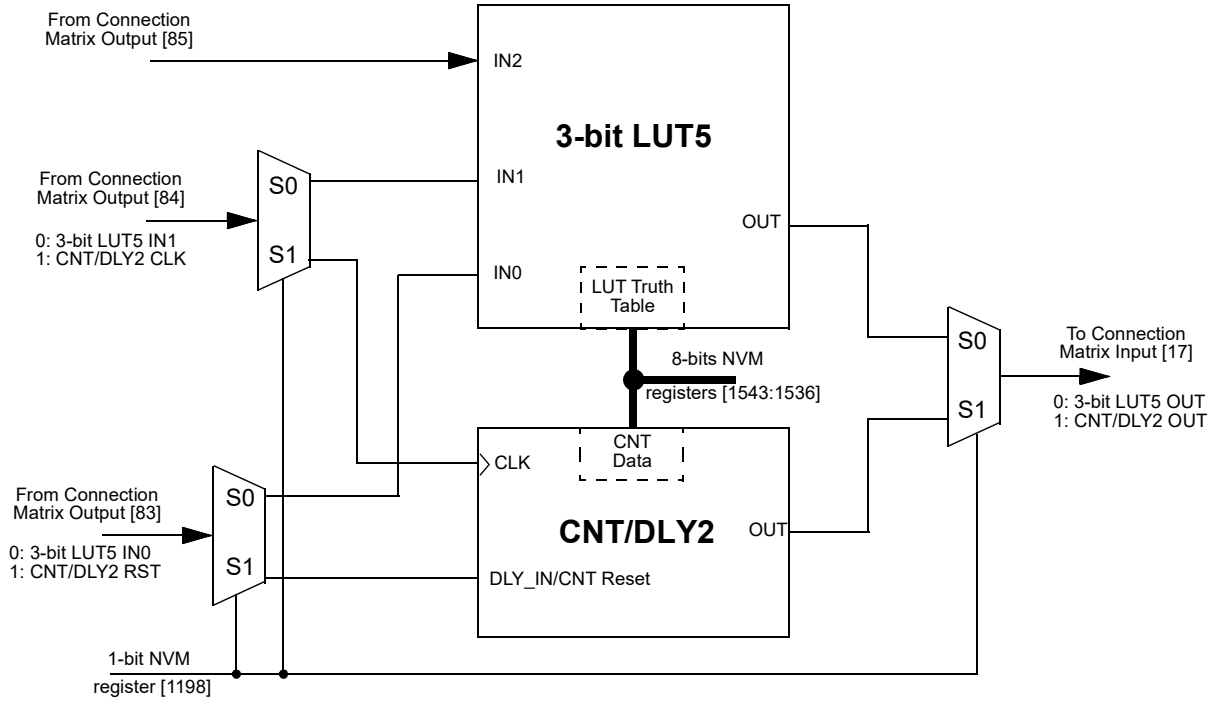


Figure 23: 3-bit LUT5 or CNT/DLY2

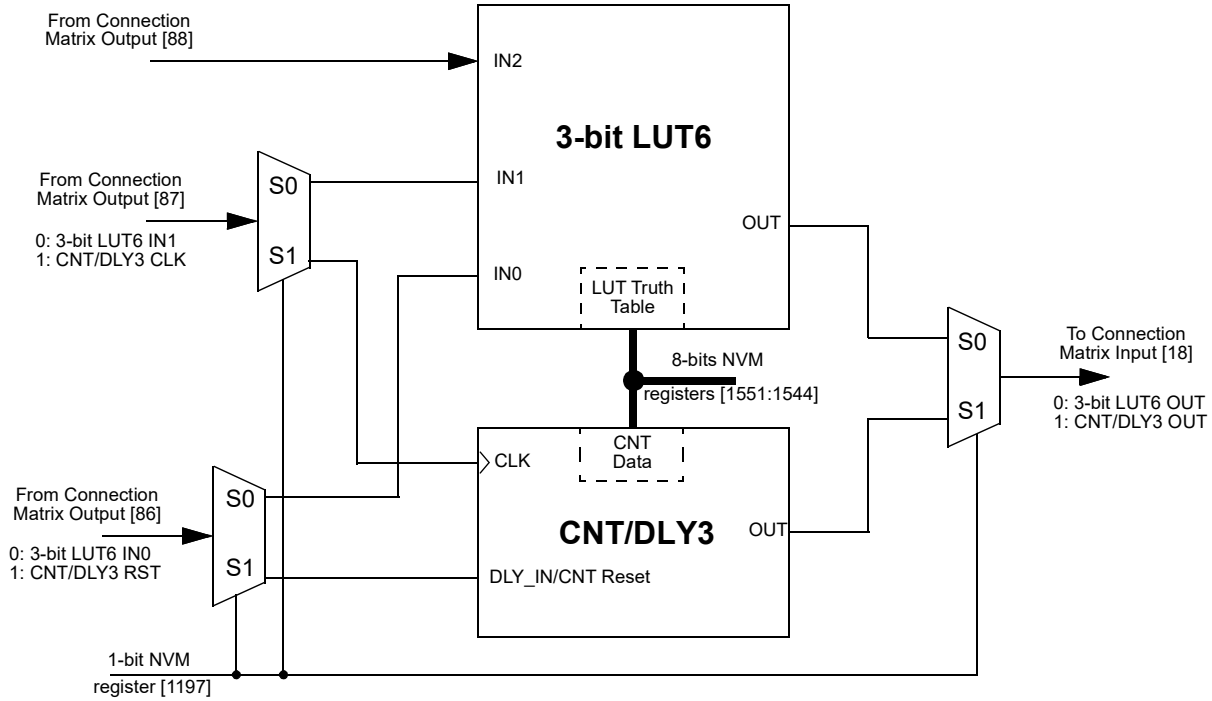


Figure 24: 3-bit LUT6 or CNT/DLY3

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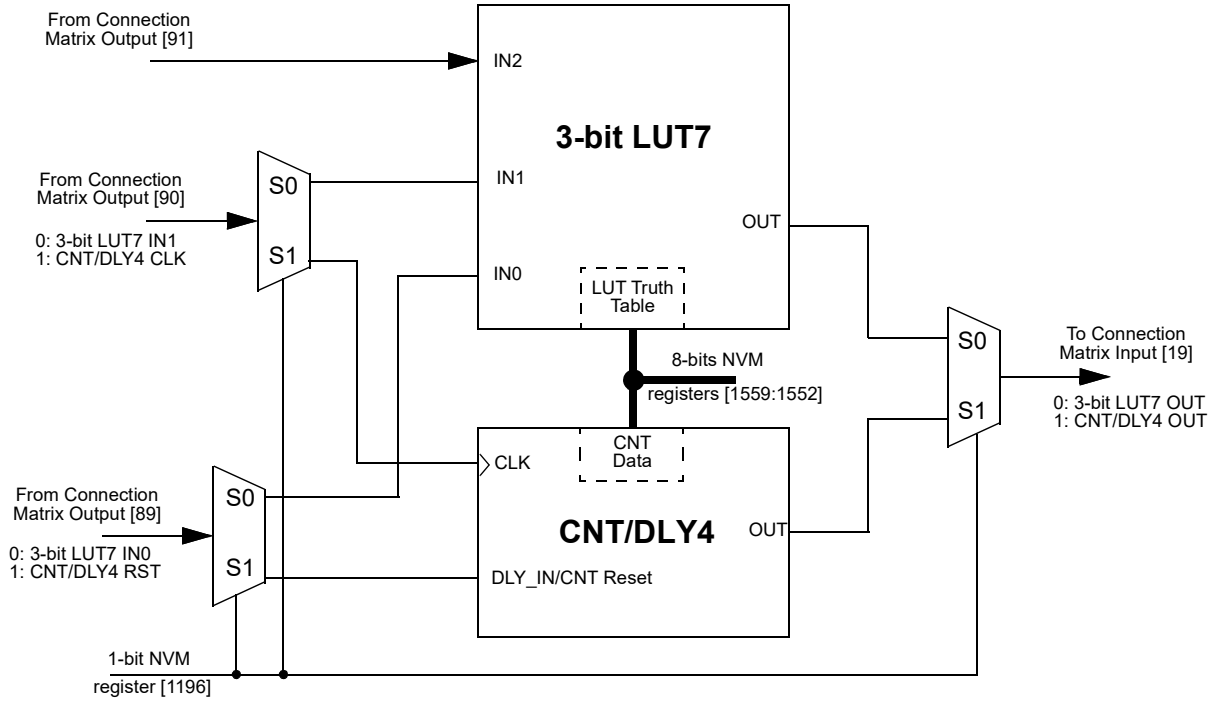


Figure 25: 3-bit LUT7 or CNT/DLY4

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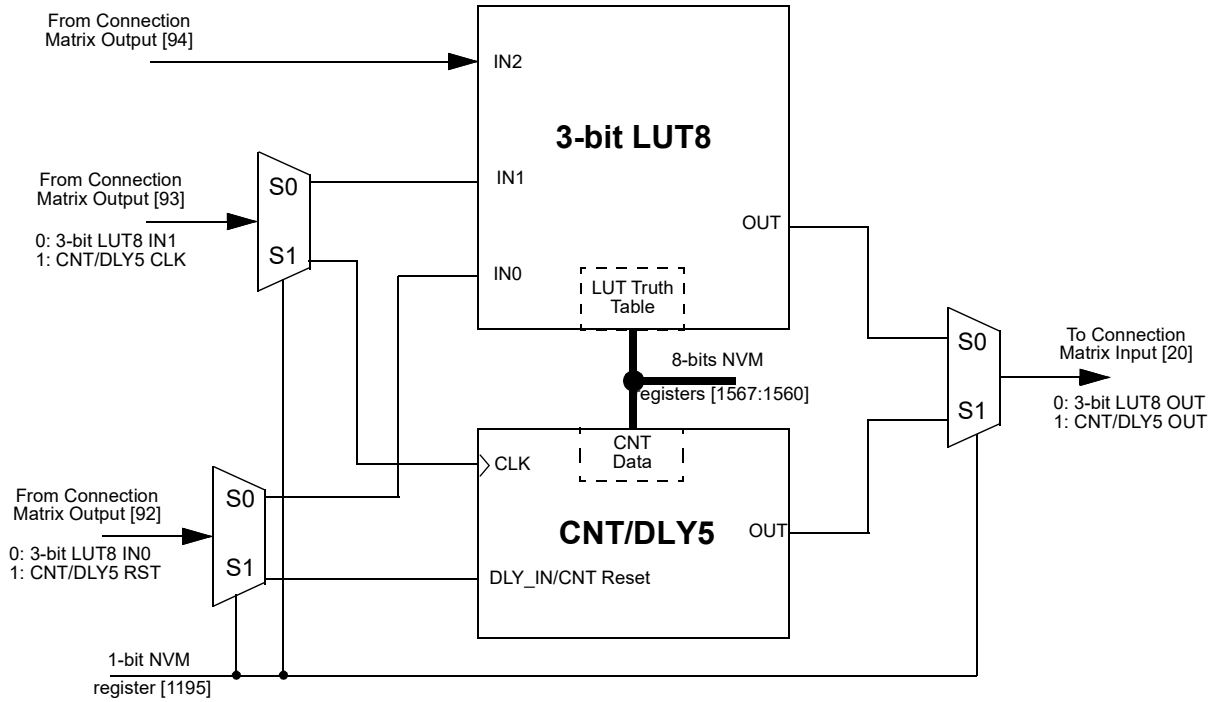


Figure 26: 3-bit LUT8 or CNT/DLY5

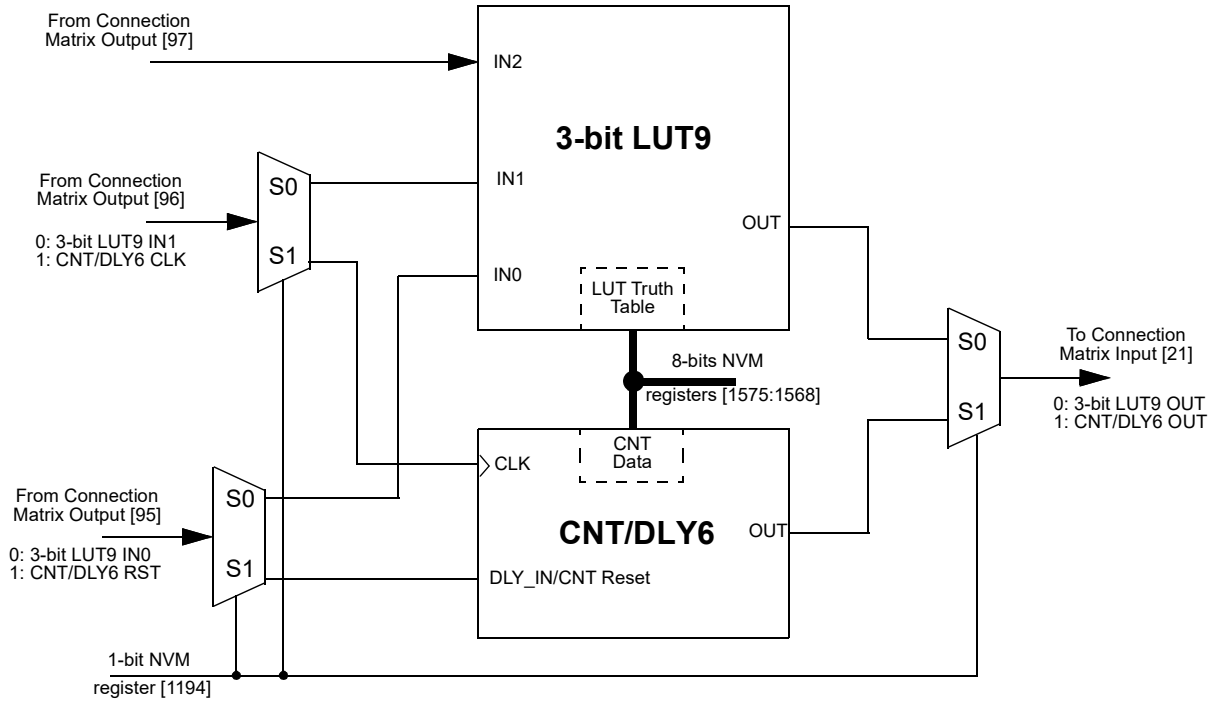


Figure 27: 3-bit LUT9 or CNT/DLY6

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7.4.2 3-Bit LUT or Counter/Delay Macrocells Used as 3-Bit LUTs

Table 65: 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1536]	LSB
0	0	1	register [1537]	
0	1	0	register [1538]	
0	1	1	register [1539]	
1	0	0	register [1540]	
1	0	1	register [1541]	
1	1	0	register [1542]	
1	1	1	register [1543]	MSB

Table 66: 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1544]	LSB
0	0	1	register [1545]	
0	1	0	register [1546]	
0	1	1	register [1547]	
1	0	0	register [1548]	
1	0	1	register [1549]	
1	1	0	register [1550]	
1	1	1	register [1551]	MSB

Table 67: 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1552]	LSB
0	0	1	register [1553]	
0	1	0	register [1554]	
0	1	1	register [1555]	
1	0	0	register [1556]	
1	0	1	register [1557]	
1	1	0	register [1558]	
1	1	1	register [1559]	MSB

Table 68: 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1560]	LSB
0	0	1	register [1561]	
0	1	0	register [1562]	
0	1	1	register [1563]	
1	0	0	register [1564]	
1	0	1	register [1565]	
1	1	0	register [1566]	
1	1	1	register [1567]	MSB

Table 69: 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1568]	LSB
0	0	1	register [1569]	
0	1	0	register [1570]	
0	1	1	register [1571]	
1	0	0	register [1572]	
1	0	1	register [1573]	
1	1	0	register [1574]	
1	1	1	register [1575]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT5 is defined by registers [1543:1536]

3-Bit LUT6 is defined by registers [1551:1544]

3-Bit LUT7 is defined by registers [1559:1552]

3-Bit LUT8 is defined by registers [1567:1560]

3-Bit LUT9 is defined by registers [1575:1568]

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Table 70 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 70: 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.4.3 3-Bit LUT or 8-Bit Counter/Delay Macrocells Used as 8-Bit Counter/Delay Register Settings

Table 71: CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_5 or Counter2 Select	[1198]	0: LUT3_5 1: Counter2
Delay2 Mode Select or asynchronous Counter Reset	[1273:1272]	00: on both falling and rising edges (for Delay & Counter Reset) 01: on falling edge only (for Delay & Counter Reset) 10: on rising edge only (for Delay & Counter Reset) 11: no Delay on either falling or rising edges/counter high level reset
Counter/Delay2 Clock Source Select	[1276:1274]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter1 Overflow
Counter/Delay2 Output Selection for Counter mode	[1277]	0: Default Output 1: Edge Detector Output
Counter/Delay2 Mode Selection	[1279:1278]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/Delay2 Control Data	[1543:1536]	1 - 255

Table 72: CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_6 or Counter3 Select	[1197]	0: LUT3_6 1: Counter3
Delay3 Mode Select or asynchronous Counter Reset	[1281:1280]	00: on both falling and rising edges (for Delay & Counter Reset) 01: on falling edge only (for Delay & Counter Reset) 10: on rising edge only (for Delay & Counter Reset) 11: no Delay on either falling or rising edges/counter high level reset

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Table 72: CNT/DLY3 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Clock Source Select	[1284:1282]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter2 Overflow
Counter/Delay3 Output Selection for Counter mode	[1285]	0: Default Output 1: Edge Detector Output
Counter/Delay2 Mode Selection	[1287:1286]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/Delay3 Control Data	[1551:1544]	1 - 255

Table 73: CNT/DLY4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_7 or Counter4 Select	[1196]	0: LUT3_7 1: Counter4
Delay4 Mode Select or asynchronous Counter Reset	[1289:1288]	00: on both falling and rising edges (for Delay & Counter Reset) 01: on falling edge only (for Delay & Counter Reset) 10: on rising edge only (for Delay & Counter Reset) 11: no Delay on either falling or rising edges/counter high level reset
Counter/Delay4 Clock Source Select	[1292:1290]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter3 Overflow
Counter/Delay4 Output Selection for Counter mode	[1293]	0: Default Output 1: Edge Detector Output
Counter/Delay4 Mode Selection	[1295:1294]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/Delay4 Control Data	[1559:1552]	1 - 255

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Table 74: CNT/DLY5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_8 or Counter5 Select	[1195]	0: LUT3_8 1: Counter5
Delay5 Mode Select or asynchronous Counter Reset	[1297:1296]	00: on both falling and rising edges (for Delay & Counter Reset) 01: on falling edge only (for Delay & Counter Reset) 10: on rising edge only (for Delay & Counter Reset) 11: no Delay on either falling or rising edges/counter high level reset
Counter/Delay5 Clock Source Select	[1300:1298]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter4 Overflow
Counter/Delay5 Output Selection for Counter mode	[1301]	0: Default Output 1: Edge Detector Output
Counter/Delay5 Mode Selection	[1303:1302]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/Delay5 Control Data	[1567:1560]	1 - 255

Table 75: CNT/DLY6 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_9 or Counter5 Select	[1194]	0: LUT3_9 1: Counter6
Delay6 Mode Select or asynchronous Counter Reset	[1305:1304]	00: on both falling and rising edges (for Delay & Counter Reset) 01: on falling edge only (for Delay & Counter Reset) 10: on rising edge only (for Delay & Counter Reset) 11: no Delay on either falling or rising edges/counter high level reset
Counter/Delay6 Clock Source Select	[1308:1306]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter5 Overflow
Counter/Delay6 Output Selection for Counter mode	[1309]	0: Default Output 1: Edge Detector Output
Counter/Delay6 Mode Selection	[1311:1310]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode

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Table 75: CNT/DLY6 Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
Counter/Delay6 Control Data	[1575:1568]	1 - 255

7.5 4-BIT LUT OR 16-BIT COUNTER/DELAY MACROCELLS

There are two macrocells that can serve as either 4-bit LUTs or as 16-bit Counter/Delays. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, four input signals from the connection matrix go to the external clock (EXT_CLK) and Reset (DLY_IN/CNT Reset), Keep and Up for the counter/delay, with the output going back to the connection matrix.

These two macrocells have an optional Finite State Machine (FSM) function. There are two matrix inputs for Up and Keep to support FSM functionality. Any counter within Green PAK is counting down by default. In FSM mode (CNT/DLY0 and CNT/DLY1) it is possible to reverse counting by applying High level to Up input. Also, there is a possibility to pause counting by applying High level to Keep input, after the level goes Low, the counter will proceed counting.These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection.

Delay time and Output Period can be calculated using the following formulas:

- Delay time: [(Counter data + 2)/CLK input frequency – Offset*];
- Output Period: [(Counter data + 1)/CLK input frequency – Offset*].

One Shot pulse width can be calculated using formula:

- Pulse width = [(Counter Data + 2)/CLK input frequency – Offset*];

*Offset is the asynchronous time offset between the input signal and the first clock pulse.

Note Counters initialize with counter data after POR

For timing diagrams refer to Section 7.6.

Both of these macrocells can have their active count value read via I^2C. See Section 17.6.1 for further details.

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7.5.1 4-Bit LUT or 16-Bit CNT/DLY Block Diagram

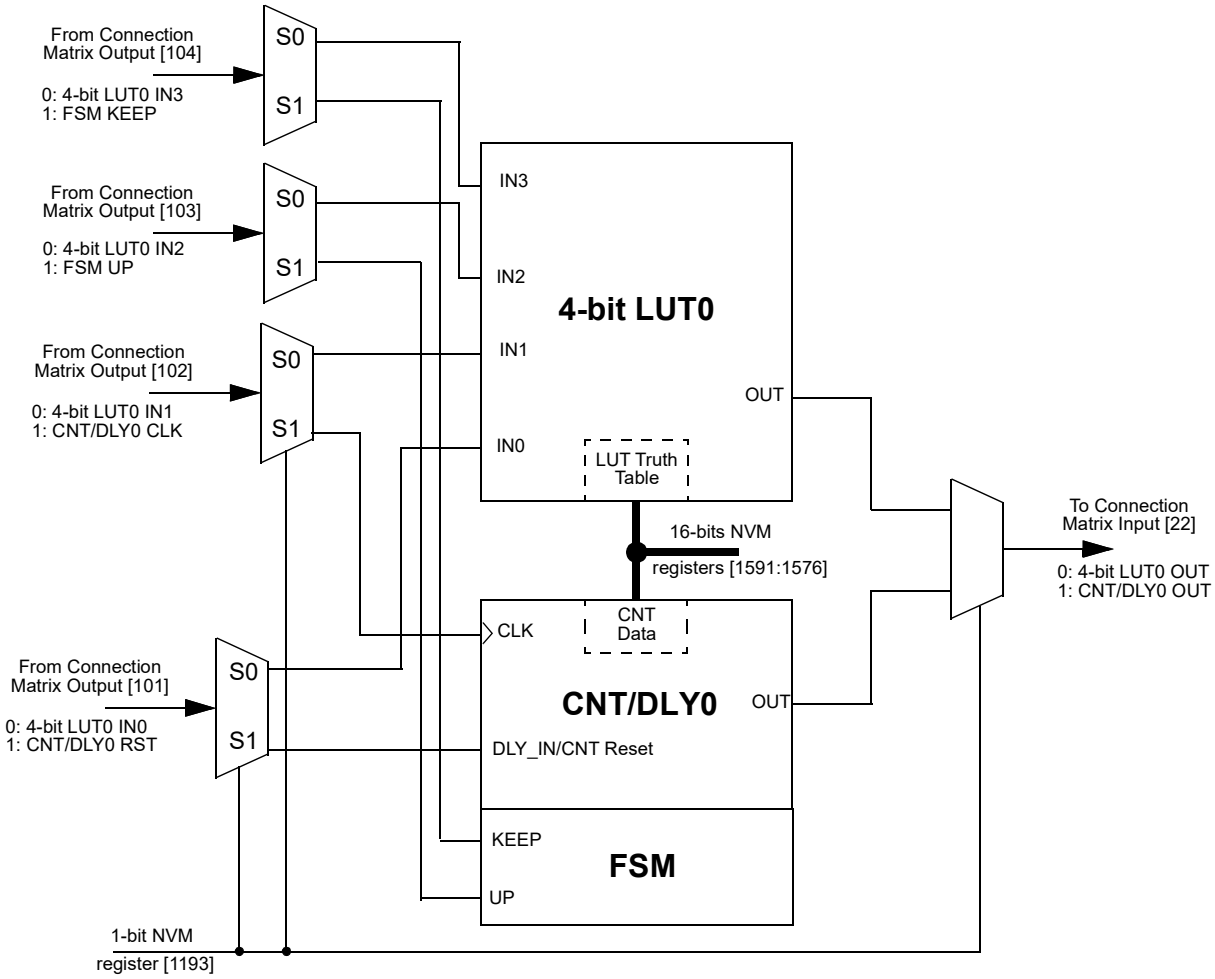


Figure 28: 4-bit LUT0 or CNT/DLY0

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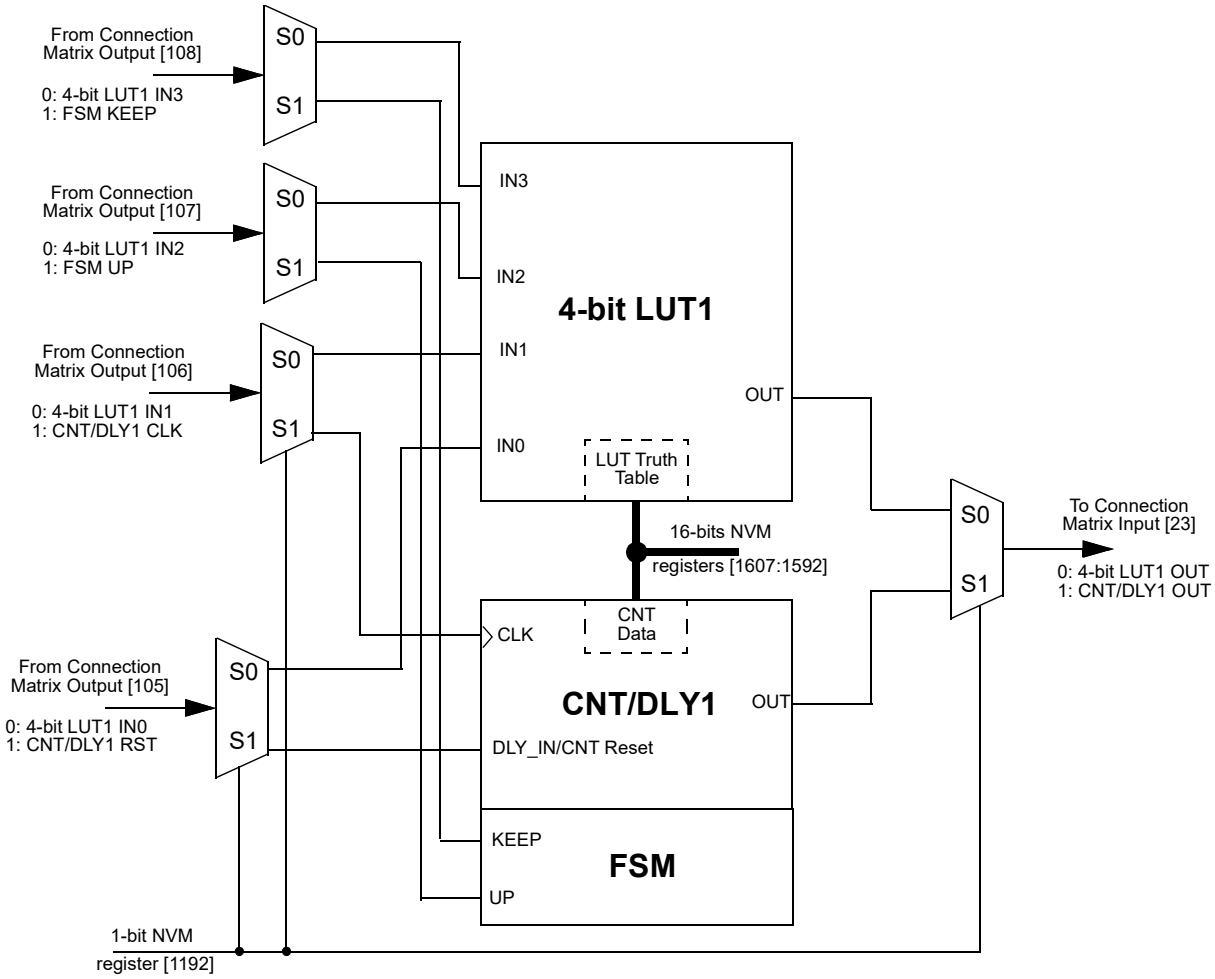


Figure 29: 4-bit LUT1 or CNT/DLY1

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7.5.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 76: 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1576]	LSB
0	0	0	1	register [1577]	
0	0	1	0	register [1578]	
0	0	1	1	register [1579]	
0	1	0	0	register [1580]	
0	1	0	1	register [1581]	
0	1	1	0	register [1582]	
0	1	1	1	register [1583]	
1	0	0	0	register [1584]	
1	0	0	1	register [1585]	
1	0	1	0	register [1586]	
1	0	1	1	register [1587]	
1	1	0	0	register [1588]	
1	1	0	1	register [1589]	
1	1	1	0	register [1590]	
1	1	1	1	register [1591]	MSB

Table 77: 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1592]	LSB
0	0	0	1	register [1593]	
0	0	1	0	register [1594]	
0	0	1	1	register [1595]	
0	1	0	0	register [1596]	
0	1	0	1	register [1597]	
0	1	1	0	register [1598]	
0	1	1	1	register [1599]	
1	0	0	0	register [1600]	
1	0	0	1	register [1601]	
1	0	1	0	register [1602]	
1	0	1	1	register [1603]	
1	1	0	0	register [1604]	
1	1	0	1	register [1605]	
1	1	1	0	register [1606]	
1	1	1	1	register [1607]	MSB

Each macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by registers [1591:1576]

4-Bit LUT1 is defined by registers [1607:1592]

Table 78: 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

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7.5.3 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 16-Bit Counter/Delay Register Setting

Table 79: CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_0 or Counter0 Select	[1193]	0: LUT4_0 1: Counter0
Delay0 Mode Select or asynchronous Counter Reset	[1313:1312]	00: on both falling and rising edges (for delay & Counter Reset) 01: on falling edge only (for delay & Counter Reset) 10: on rising edge only (for delay & Counter Reset) 11: no delay on either falling or rising edges/counter high level reset
Counter/delay0 Clock Source Select	[1316:1314]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter6 Overflow
CNT0/FSM0's Q are Set to data or Reset to 0s Selection	[1317]	0: Reset to 0s 1: Set to control data (Registers [1583:1576, 1591:1584])
Counter/delay0 Mode Selection	[1319:1318]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay0 Control Data	[1591:1576]	1 - 65535 (Delay Time = [Counter Control Data + 1]/Freq)

Table 80: CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_1 or Counter1 Select	[1192]	0: LUT4_1 1: Counter1
Delay1 Mode Select or asynchronous Counter Reset	[1321:1320]	00: on both falling and rising edges (for delay & Counter Reset) 01: on falling edge only (for delay & Counter Reset) 10: on rising edge only (for delay & Counter Reset) 11: no delay on either falling or rising edges/counter high level reset
Counter/delay1 Clock Source Select	[1324:1322]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter0 Overflow
CNT0/FSM0's Q are Set to data or Reset to 0s Selection	[1325]	0: Reset to 0s 1: Set to counter data (Registers [1599:1592, 1607:1600])
Counter/delay1 Mode Selection	[1327:1326]	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay1 Control Data	[1607:1592]	1 - 65535 (Delay Time = [Counter Control Data + 1]/Freq)

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7.6 CNT/DLY/FSM TIMING DIAGRAMS

7.6.1 Delay Mode (Edge Select: Both, Counter Data: 3) CNT/DLY2 to CNT/DLY6

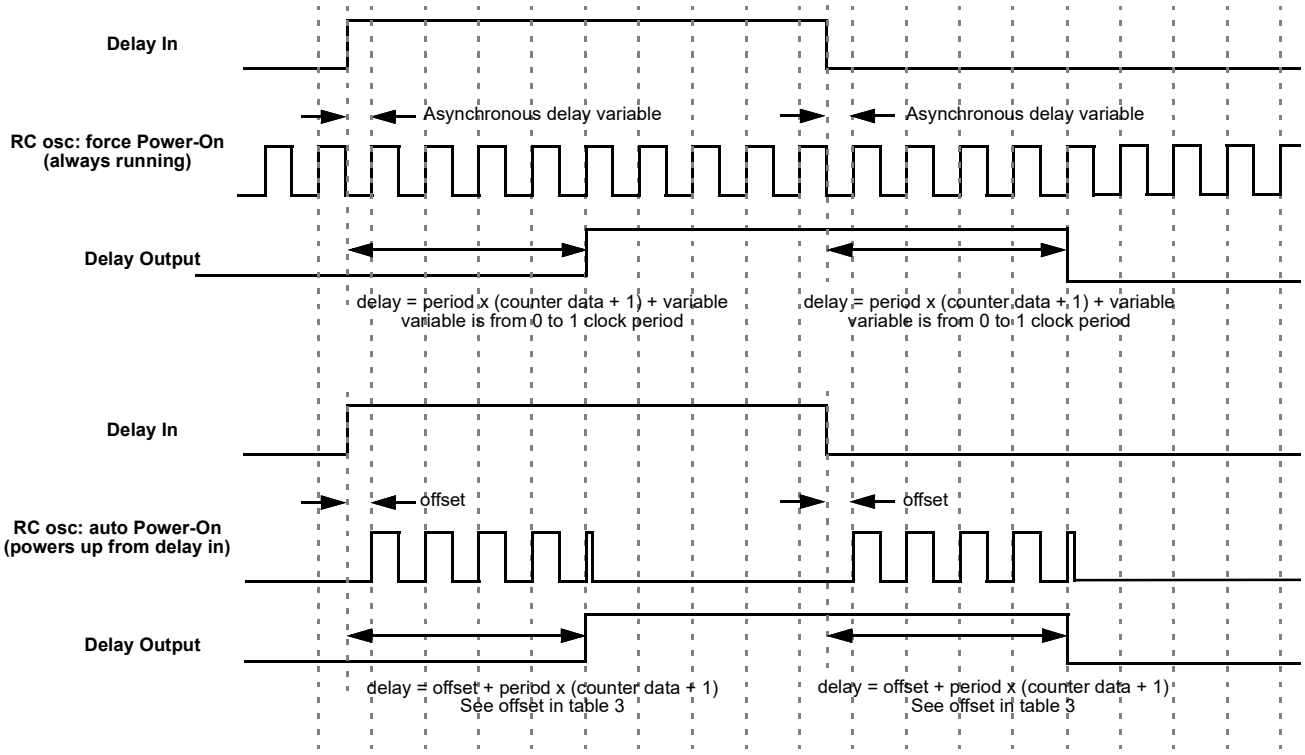


Figure 30: Delay Mode Timing Diagram

7.6.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2 to CNT/DLY6

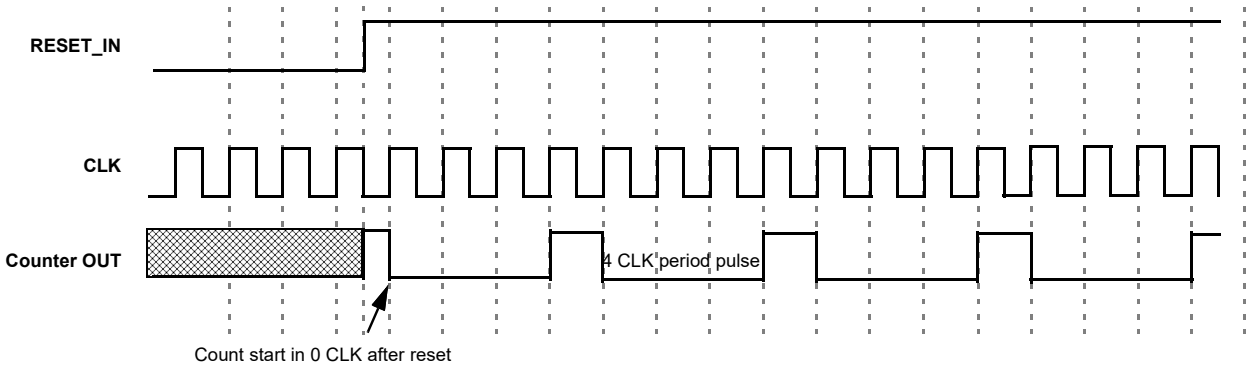


Figure 31: Counter Mode Timing Diagram

7.6.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is

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selected by register bit. See Figure 81. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

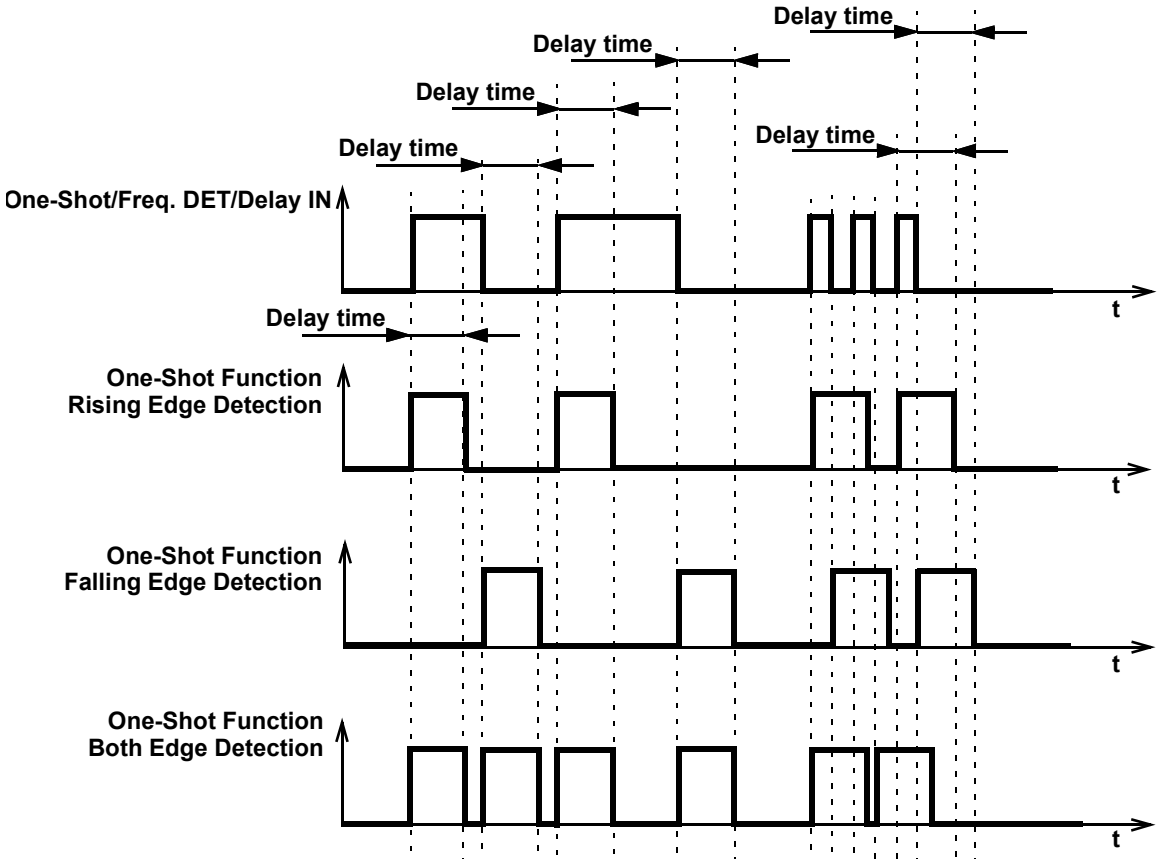


Figure 32: One-Shot Function Timing Diagram

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Table 81: DLY/CNTx One-Shot/Freq. Detect Output Polarity

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
A6	[1329]	Select the Polarity of DLY/CNT6's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1330]	Select the Polarity of DLY/CNT5's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1331]	Select the Polarity of DLY/CNT4's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1332]	Select the Polarity of DLY/CNT3's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1333]	Select the Polarity of DLY/CNT2's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1334]	Select the Polarity of DLY/CNT1's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	[1335]	Select the Polarity of DLY/CNT0's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

7.6.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

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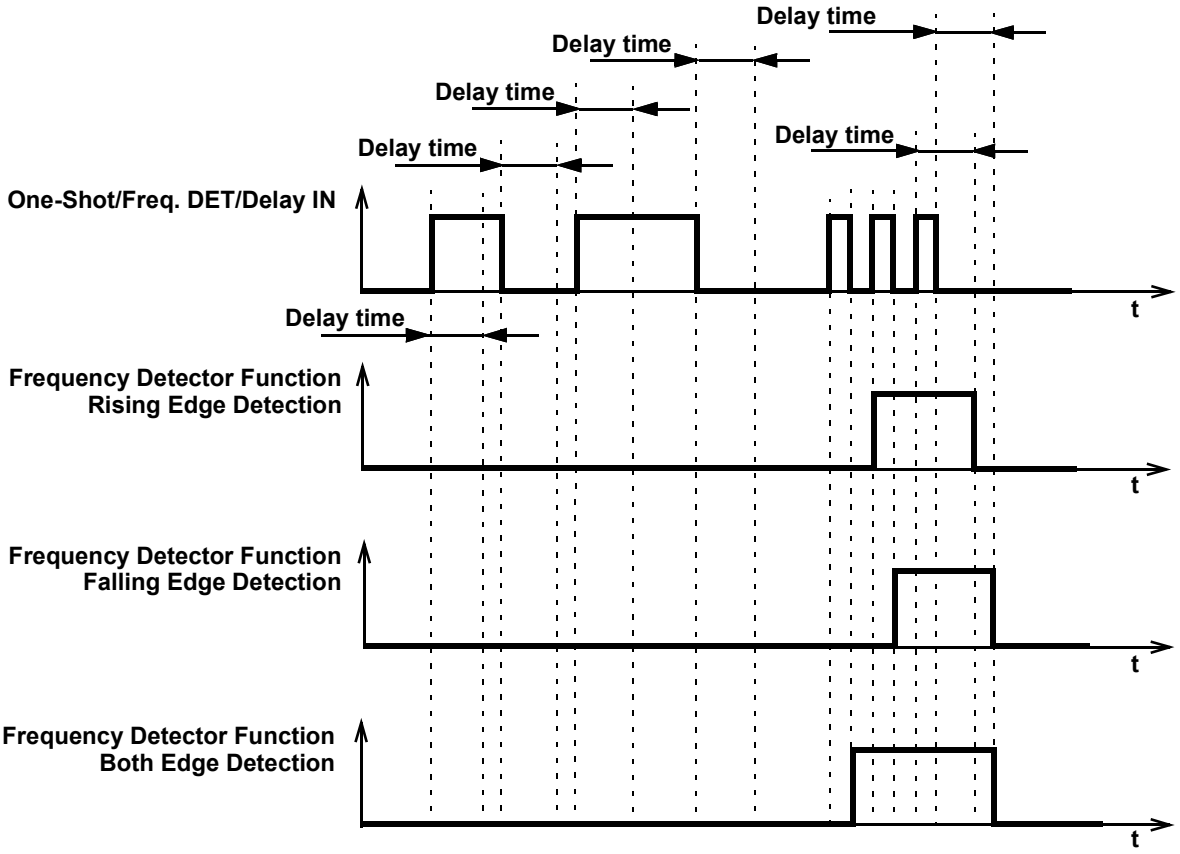


Figure 33: Frequency Detection Mode Timing Diagram

7.6.5 Edge Detection Mode CNT/DLY2 to CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge. See Table 13.

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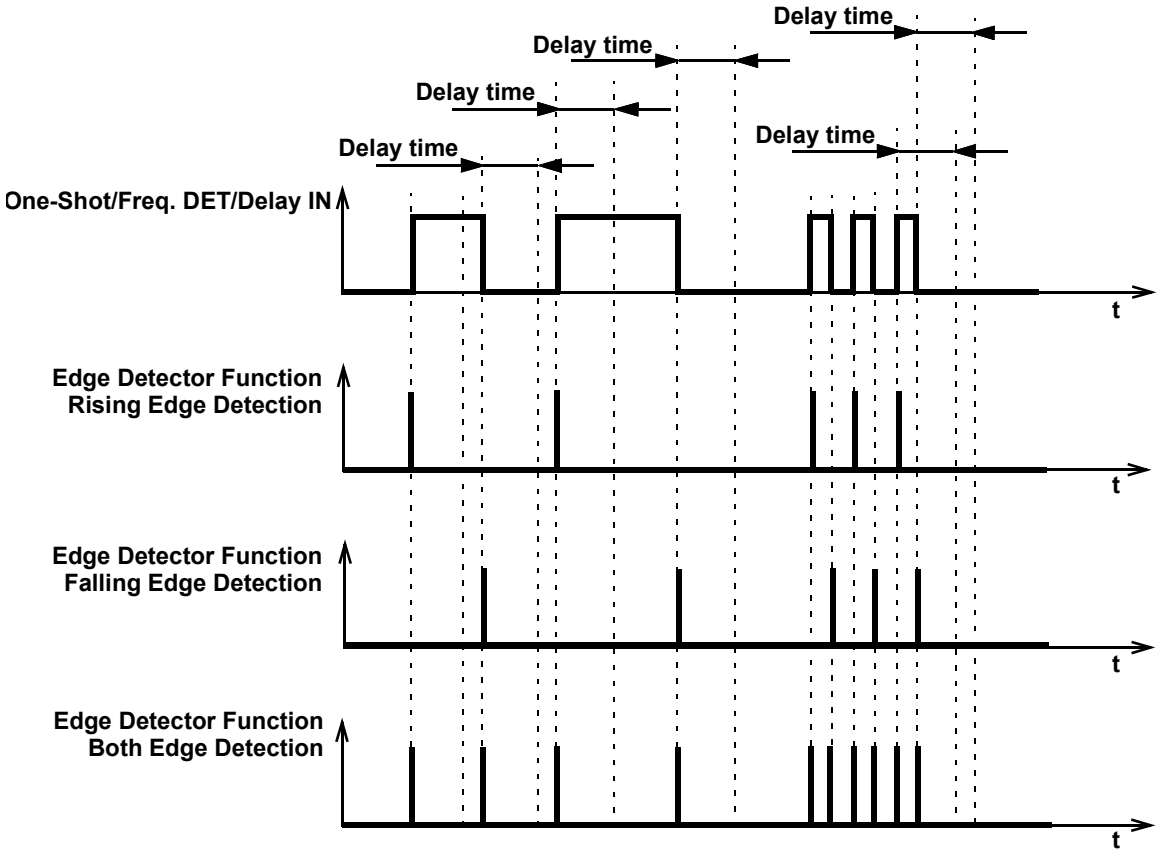


Figure 34: Edge Detection Mode Timing Diagram

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7.6.6 Delay Mode CNT/DLY0 to CNT/DLY6

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

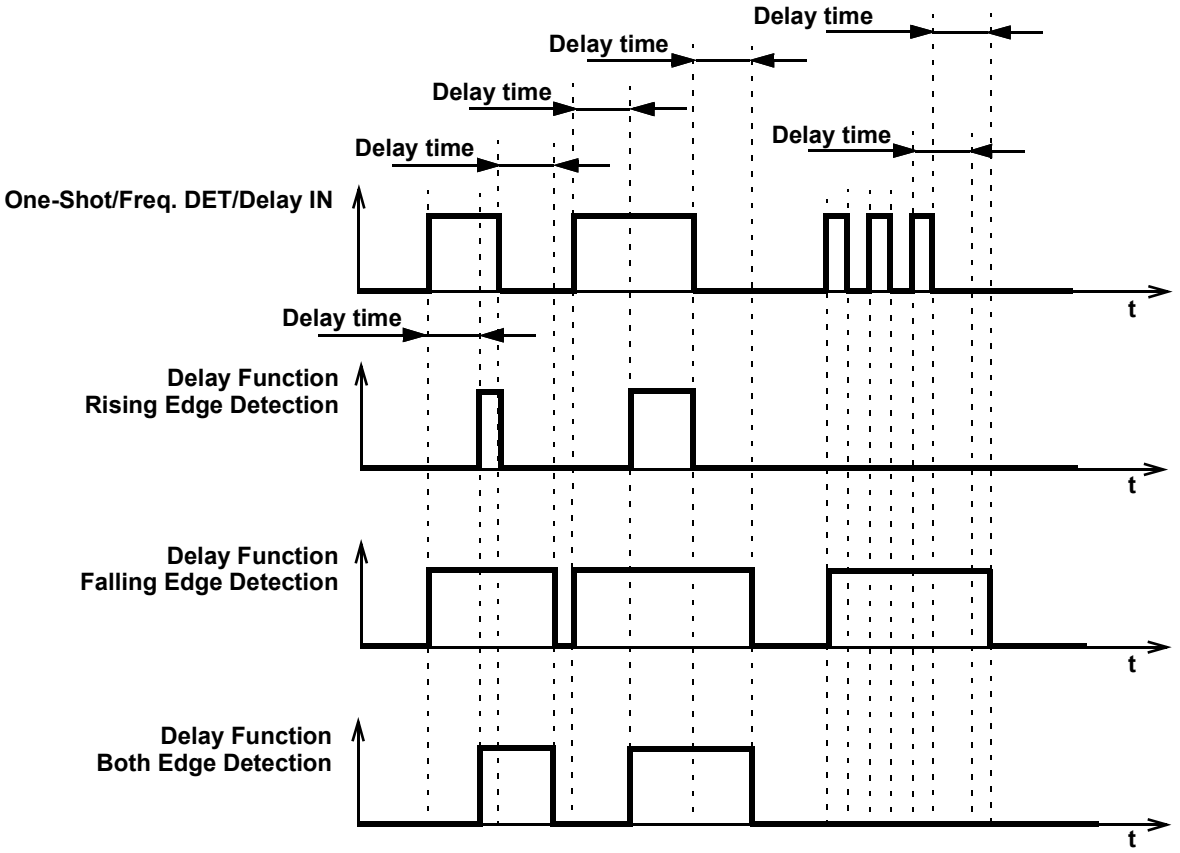


Figure 35: Delay Mode Timing Diagram

7.6.7 CNT/FSM Mode CNT/DLY0, CNT/DLY1

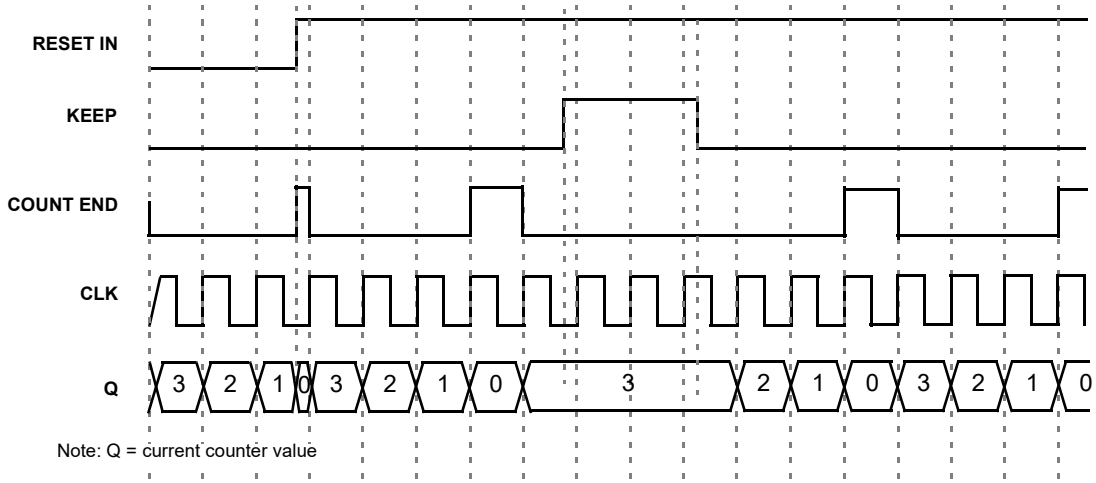


Figure 36: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

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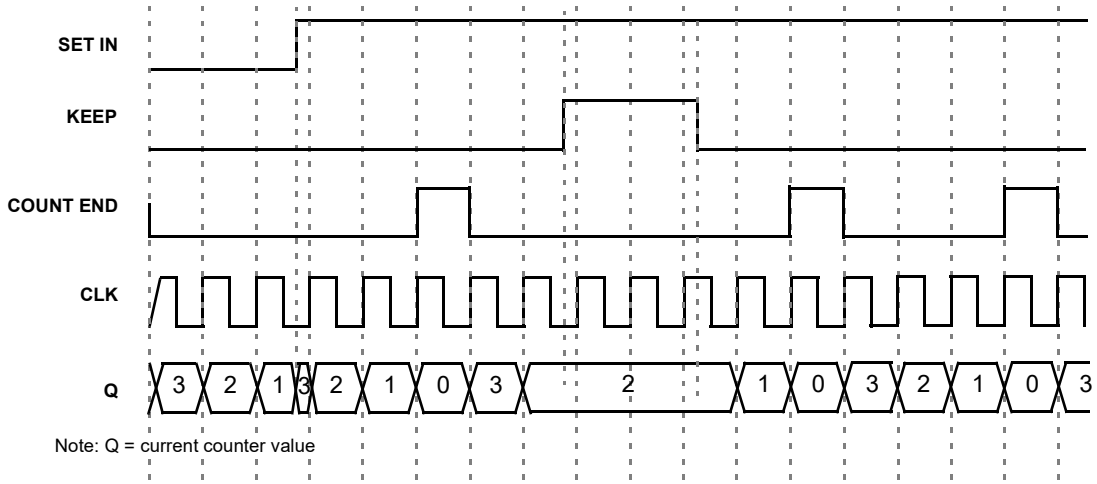


Figure 37: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0) for Counter Data = 3

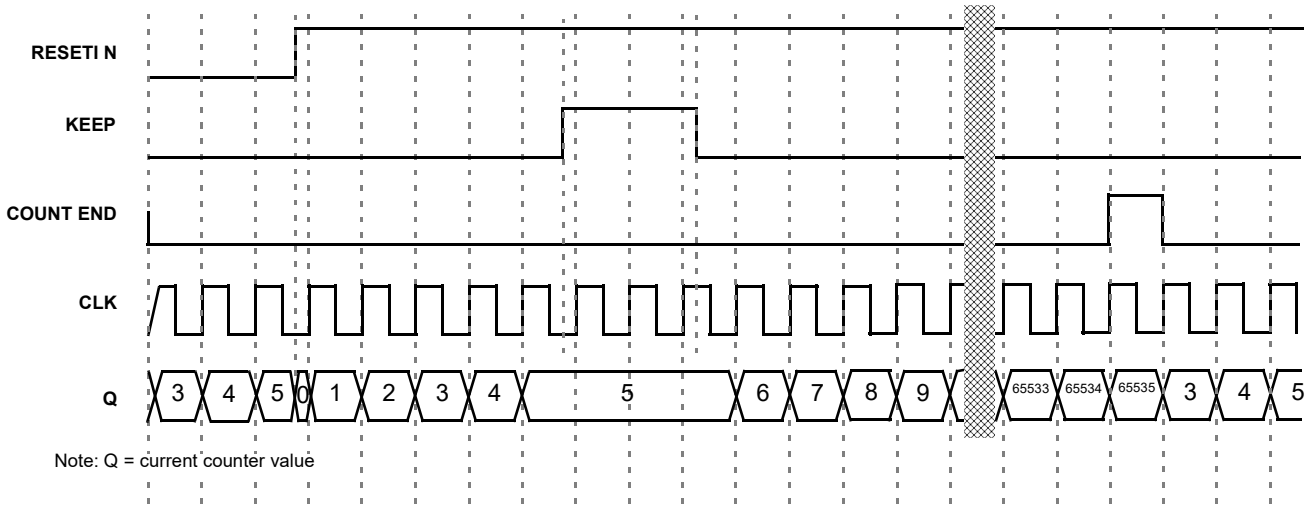


Figure 38: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

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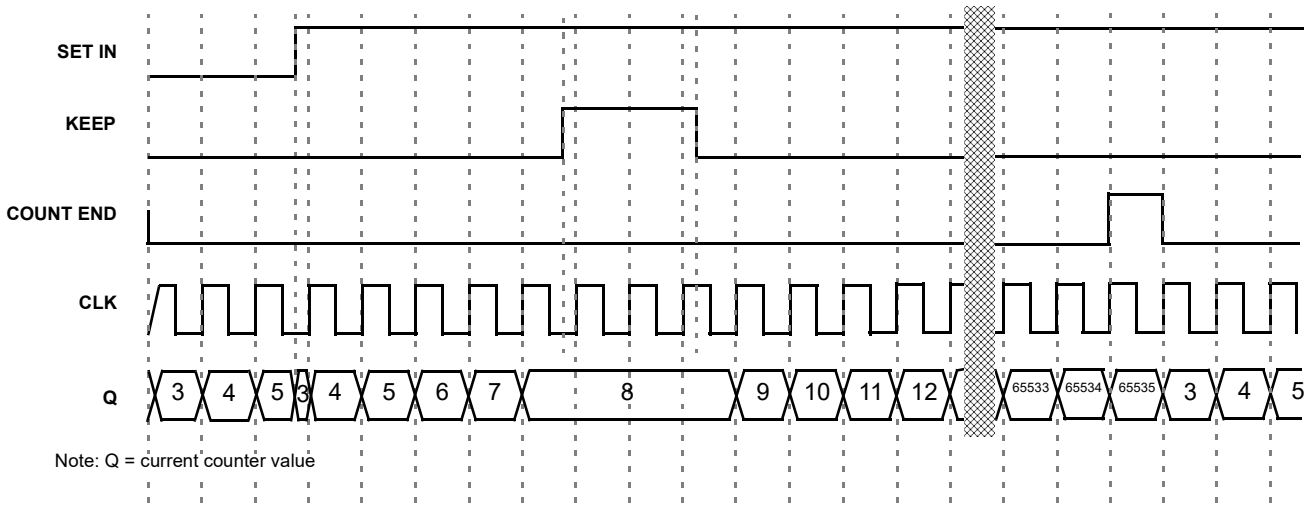


Figure 39: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for Counter Data = 3

7.7 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46517 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats. See Figure 40.

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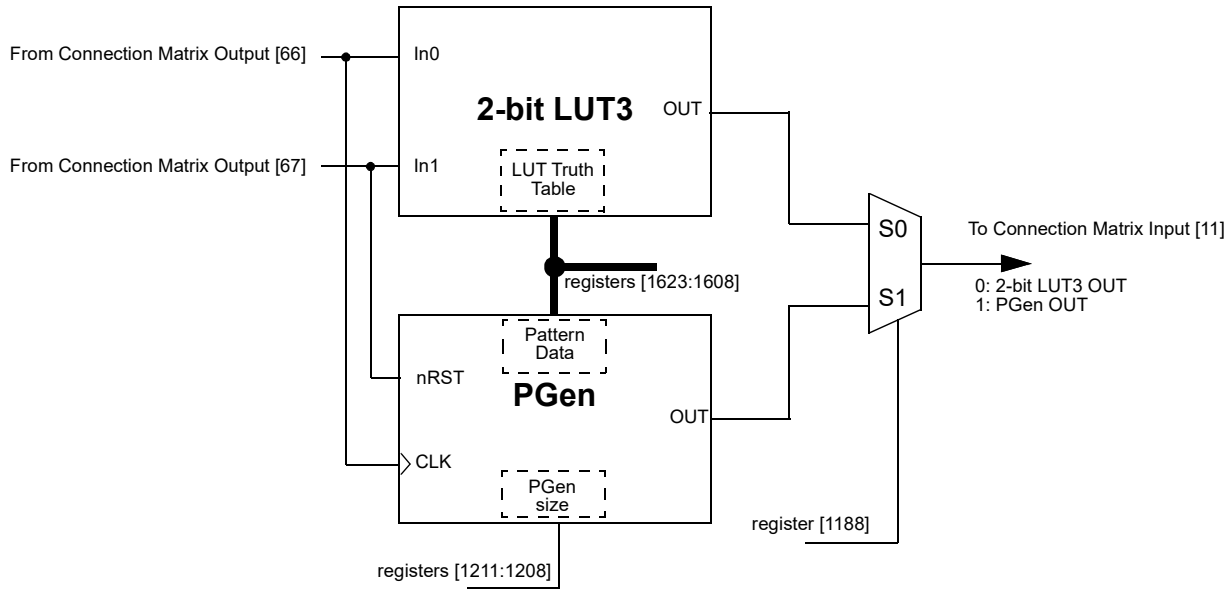


Figure 40: 2-bit LUT2 or PGen

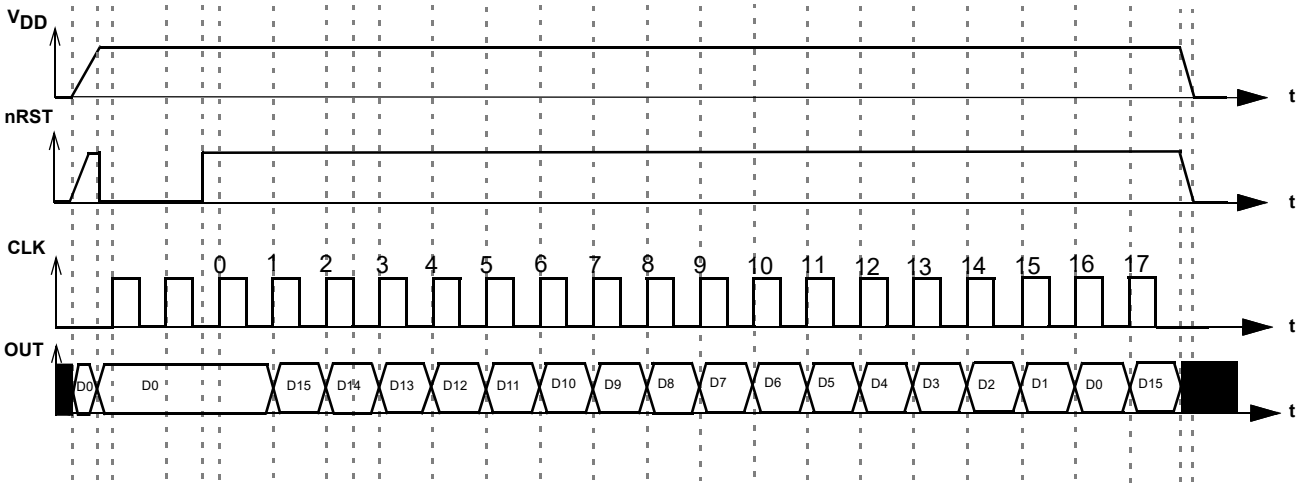


Figure 41: PGen Timing Diagram

7.8 WAKE AND SLEEP CONTROLLER

The SLG46517 has a Wake and Sleep (WS) function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1319:1318] = 11 and registers [1495] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

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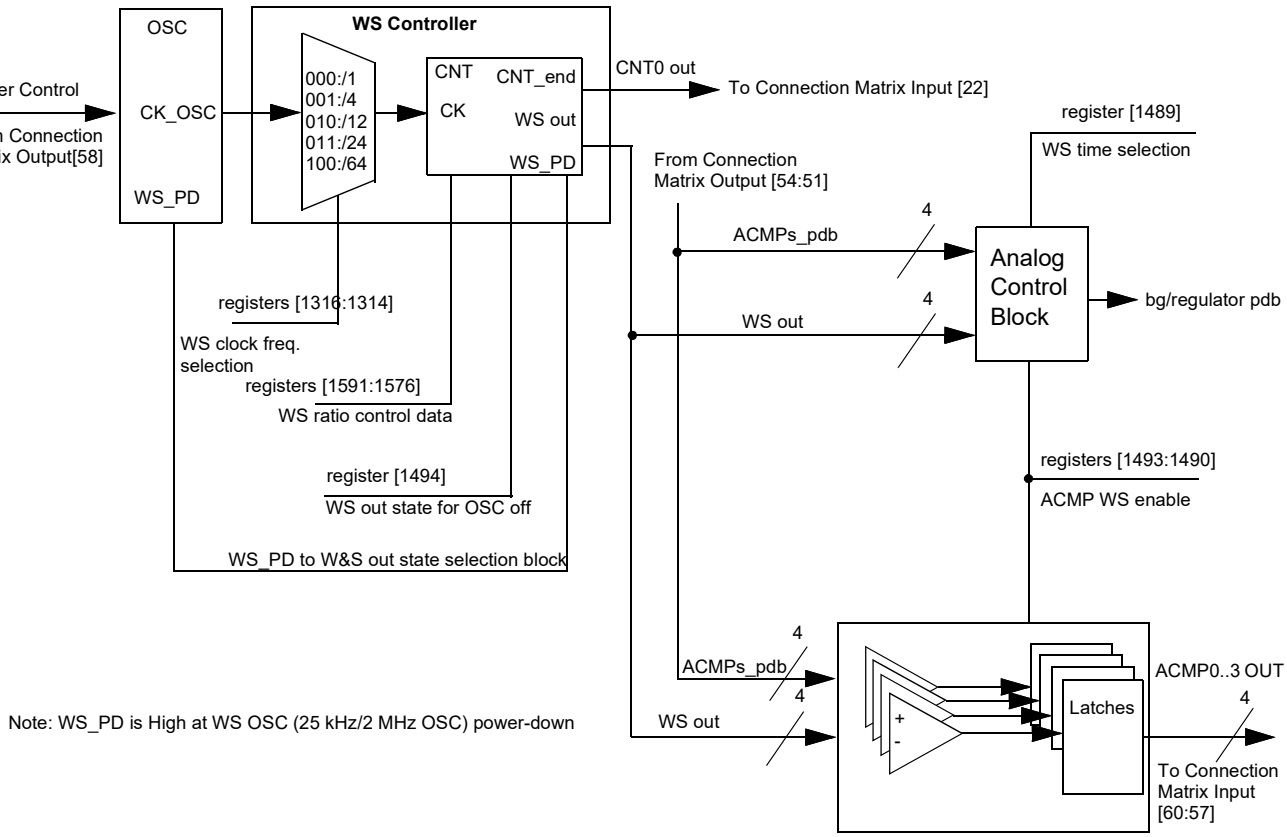
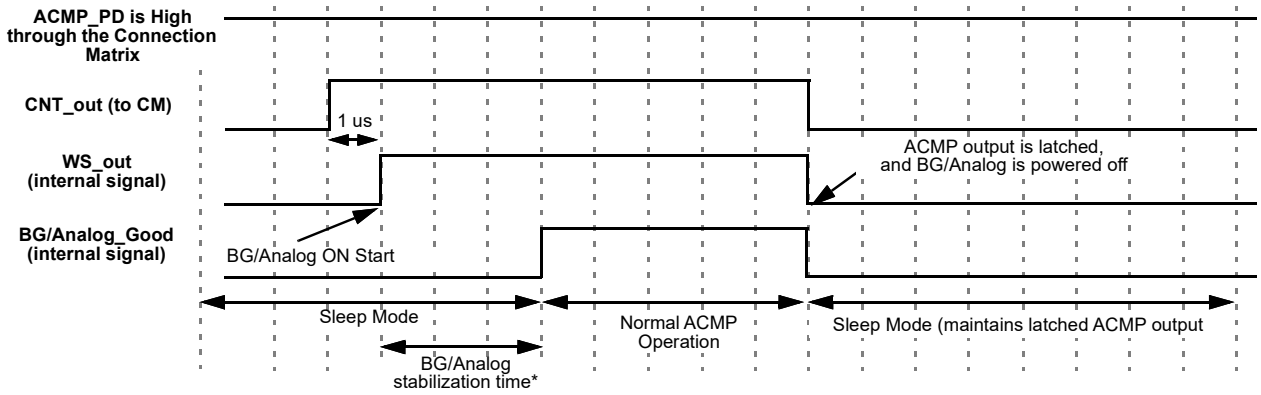


Figure 42: Wake/Sleep Controller



Note: * Refer to Electrical Spec (ACMP Start Time)

Figure 43: Wake/Sleep Timing Diagram

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs);

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- Register WS => enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMPs);
- In case of using OSC1 (25 MHz), OSC0 must be set to Force Power-On.

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.
  If OSC is powered off (Power-Down option is selected; power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears
  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end
  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

  Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPs on
  Normal Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.
  Short Wake Time - when WS signal is High, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 1.

Table 82: WS Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay0 Clock Source Select	[1316:1314]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25 MHz OSC clock 110: External Clock 111: Counter6 Overflow

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Table 82: WS Register Settings(Continued)

Signal Function	Register Bit Address	Register Definition
WS time selection	[1489]	0: Short Wake Time 1: Normal Wake Time
ACMP0 Wake & Sleep function Enable	[1490]	0: Disable 1: Enable
ACMP1 Wake & Sleep function Enable	[1491]	0: Disable 1: Enable
ACMP2 Wake & Sleep function Enable	[1492]	0: Disable 1: Enable
ACMP3 Wake & Sleep function Enable	[1493]	0: Disable 1: Enable
Wake Sleep Output State When WS Oscillator is Power-down own if DLY/CNT0 Mode Selection is "11"	[1494]	0: Low 1: High
Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"	[1495]	0: Default Mode 1: Wake Sleep Ratio Control Mode
DLY/CNT0 (16bits, [15:0] = [1591:1576]) Control Data	[1591:1576]	1 - 65535

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8 Analog Comparators

There are four Analog Comparator (ACMP) macrocells in the SLG46517. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMPx PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always on, always off, or power cycled based on a digital signal coming from the Connection Matrix. Also, all ACMPs have Wake and Sleep function (WS), see Section 7.8. When ACMP is powered down, output is low.

PWR UP = 1 => ACMP is powered up.
PWR UP = 0 => ACMP is powered down.

During ACMP power up, its output will remain low, and then becomes valid 1.03 ms (max) after ACMP power up signal goes high, see Figure 45. If V_{DD} is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG ok delay to 100 µs, see Figure 46. The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the V_{DD} signal.

Note: Regulator and Charge Pump set to automatic ON/OFF.

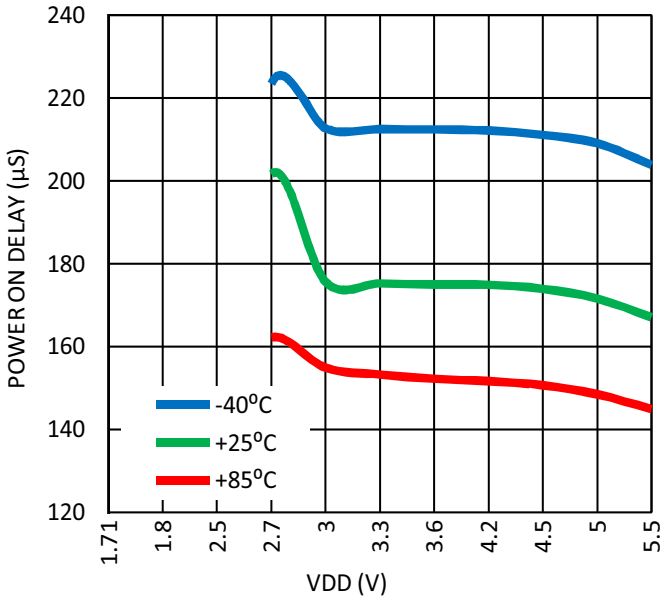


Figure 44: Maximum Power-On Delay vs. V_{DD}, BG = Auto-delay.

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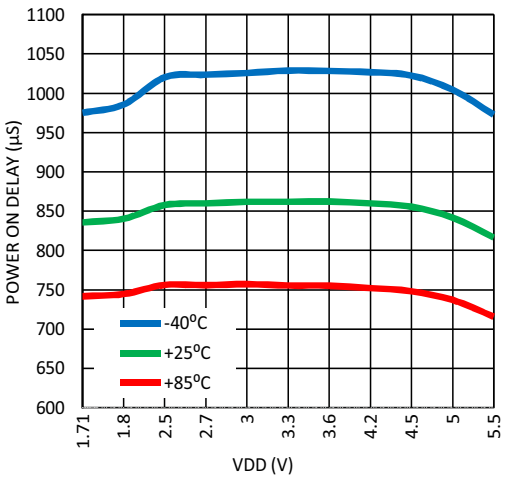


Figure 45: Max. Power-On Delay vs. V_{DD}, BG = 550 µs

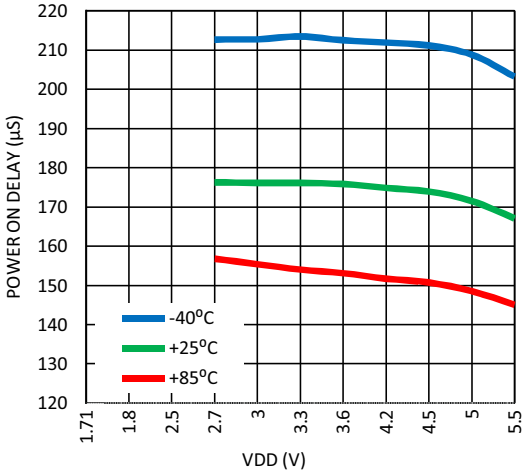


Figure 46: Max. Power-On Delay vs. V_{DD}, BG = 100 µs

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 KΩ (typ) resistors, see Table 83. For gain divider accuracy refer to Table 84. IN- voltage range: 0 - 1.2 V. Can use Vref selection $V_{DD}/4$ and $V_{DD}/3$ to maintain this input range.

Input bias current < 1 nA (typ).

Table 83: Gain Divider Input Resistance

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 MΩ	1 MΩ	0.75 MΩ	1 MΩ

Table 84: Gain Divider Accuracy

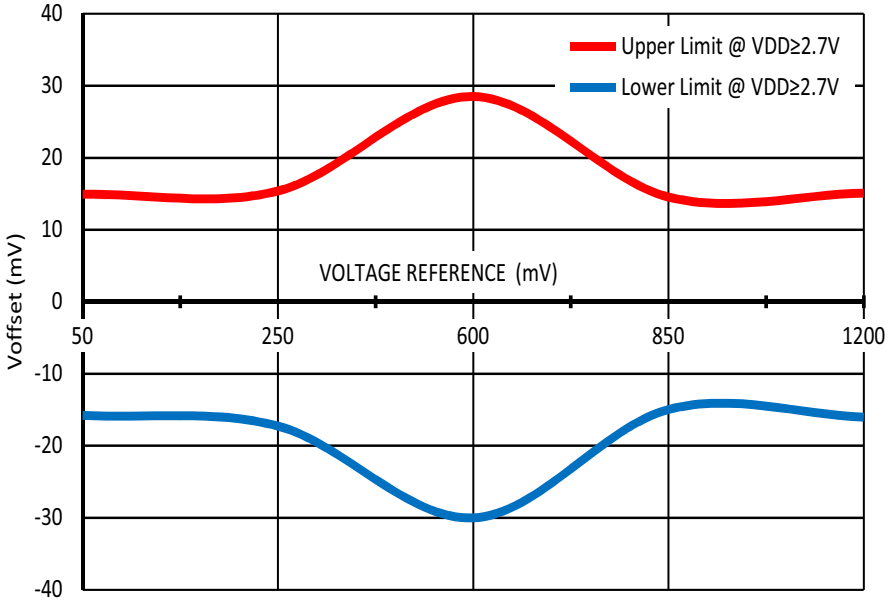
Gain	x0.5	x0.33	x0.25
Accuracy	±0.51%	±0.34%	±0.25%

Each cell also has a hysteresis selection, to offer hysteresis of (0, 25, 50, 200) mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its previous value, if the input voltage is within threshold window (between Vref and Vref - hysteresis). Please note: for the 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the BandGap internal circuit as well. An analog voltage will appear on Vref even when the Force BandGap option is set as Disabled.

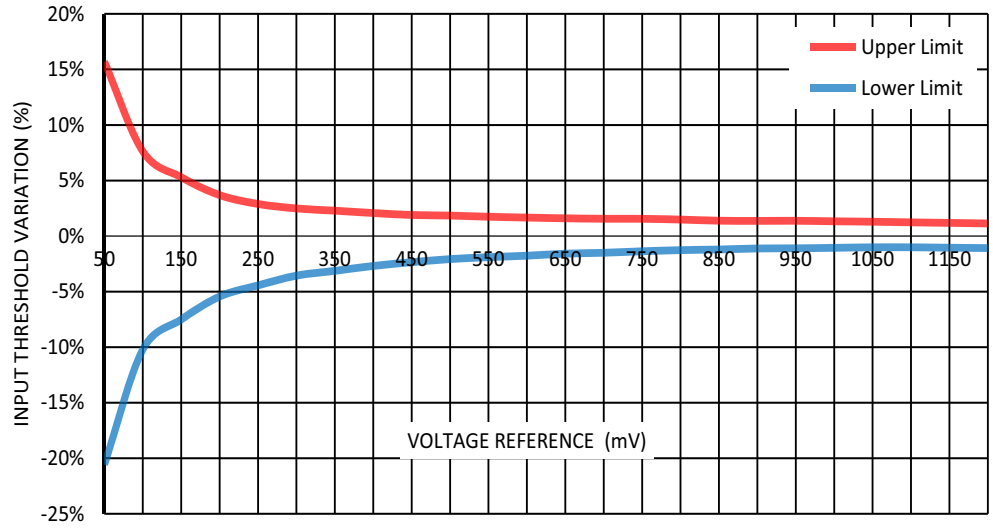
For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will add some offset, see Figure 47 to Figure 48. It is not recommended to use ACMP buffer when V_{DD} < 2.5 V.

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Note: Buffer Bandwidth = 1 kHz, Vhys = 0 mV, Gain = 1, T = -40 °C to +85 °C

Figure 47: Typical Buffer Input Voltage Offset vs. Voltage Reference



Note: LMB Mode - Disable, Vhys = 0 mV, T = -40 °C to +85 °C

Figure 48: Typical Input Threshold Variation (Including Vref Variation, ACMP Offset) vs. Voltage Reference

Note: When V_{DD} < 1.8 V voltage reference should not exceed 1100 mV.

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Table 85: Built-In Hysteresis Tolerance at T = 25 °C

Vhys (mV)	V_{DD}= 1.7 V to 1.8 V						V_{DD} = 1.89 V to 5.5 V					
	Vref = 50 mV to 500)mV		Vref = 550 V to 1000 mV		Vref = 1050 V to 1200 mV		Vref = 50 V to 500 mV		Vref = 550 V to 1000 mV		Vref = 1050 V to 1200 mV	
	min	max	min	max	min	max	min	max	min	max	min	max
25	8.6	32.2	8.6	32.3	7.0	32.5	8.5	32.3	8.5	32.3	7.8	34.0
50	44.8	56.5	43.9	56.7	42.7	56.4	44.2	56.8	43.6	57.3	43.1	56.0
200	192.8	207.9	194.0	208.0	192.7	205.4	192.0	208.6	193.0	209.5	190.8	207.7

8.1 ACMP0 BLOCK DIAGRAM AND REGISTER SETTINGS

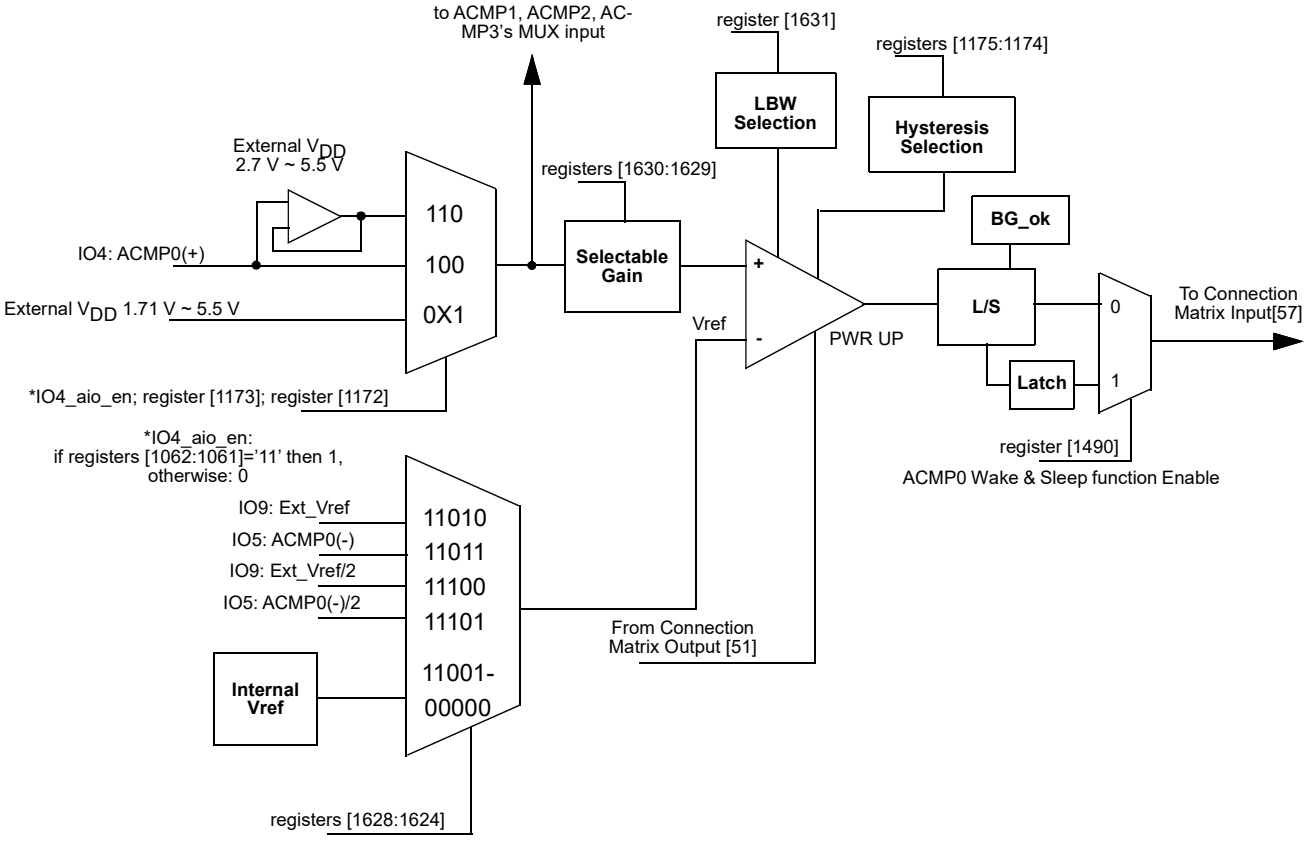


Figure 49: ACMP0 Block Diagram

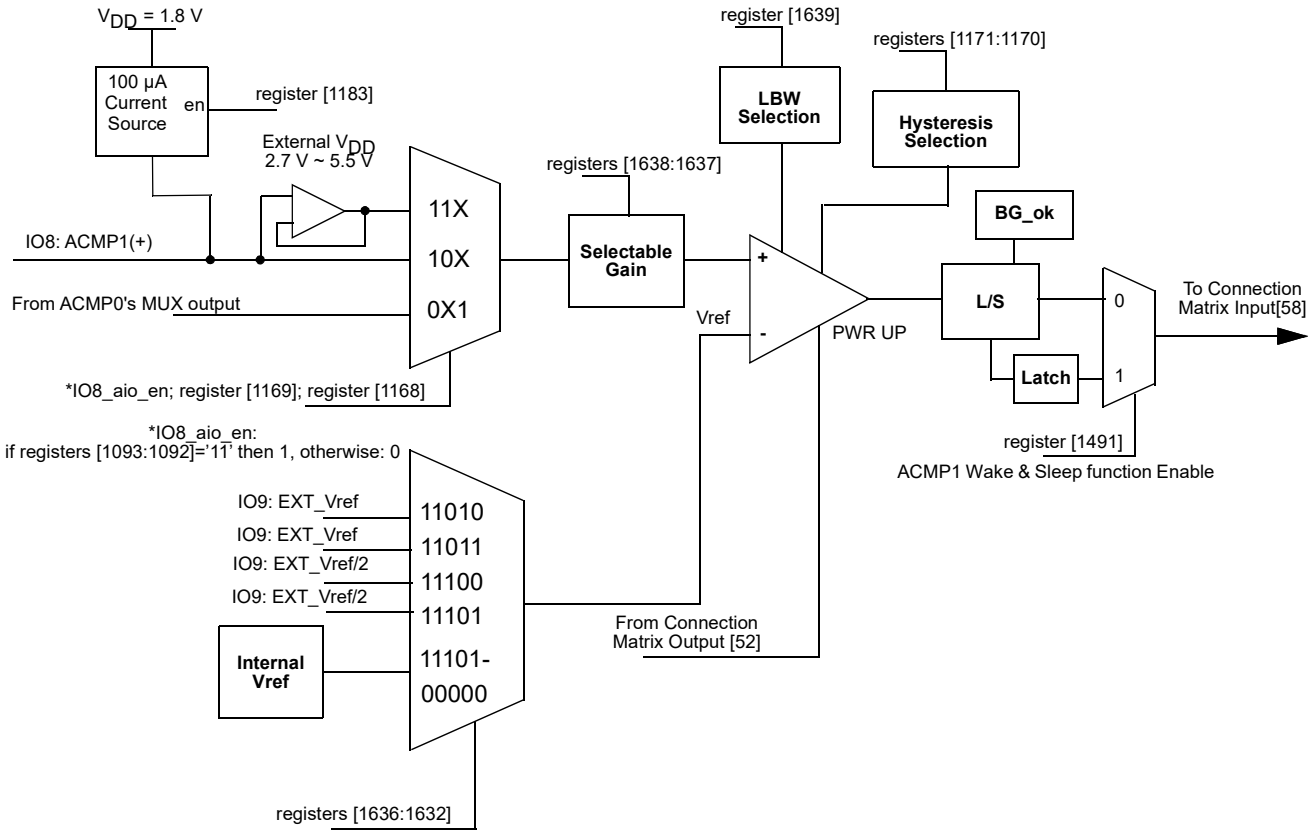
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Table 86: ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 Positive Input Source Select	[1172]	0: IO4 1: V_{DD}
ACMP0 Analog Buffer Enable	[1173]	0: Disable analog buffer 1: Enable analog buffer
ACMP0 Hysteresis Enable	[1175:1174]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50 mV & 200 mV hysteresis.)
ACMP0 Wake & Sleep function Enable	[1490]	0: Disable 1: Enable
ACMP0 In Voltage Select	[1628:1624]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO5: ACMP0- 11100: IO9: EXT_Vref/2 11101: IO5: ACMP0-/2 11110: Reserved 11111: Reserved
ACMP0 Positive Input Divider	[1630:1629]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	[1631]	0: Off 1: On

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8.2 ACMP1 BLOCK DIAGRAM AND REGISTER SETTINGS



Note: when 100 µA Current Source is enabled input voltage on IO8 should not exceed 1.8 V.

Figure 50: ACMP1 Block Diagram

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Table 87: ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 100 µA Current Source Enable	[1183]	0: Disable 1: Enable
ACMP1 Positive Input Source Select	[1168]	0: IO8 1: ACMP0 IN+ source
ACMP1 Analog Buffer Enable (max. band width 1 MHz)	[1169]	0: Disable analog buffer 1: Enable analog buffer
ACMP1 Hysteresis Enable	[1171:1170]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50 mV & 200 mV hysteresis.)
ACMP1 Wake & Sleep function Enable	[1491]	0: Disable 1: Enable
ACMP1 In Voltage Select	[1636:1632]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: Reserved 11100: IO9: EXT_Vref/2 11101: Reserved 11110: Reserved 11111: Reserved
ACMP1 Positive Input Divider	[1638:1637]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	[1639]	0: Off 1: On

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8.3 ACMP2 BLOCK DIAGRAM AND REGISTER SETTINGS

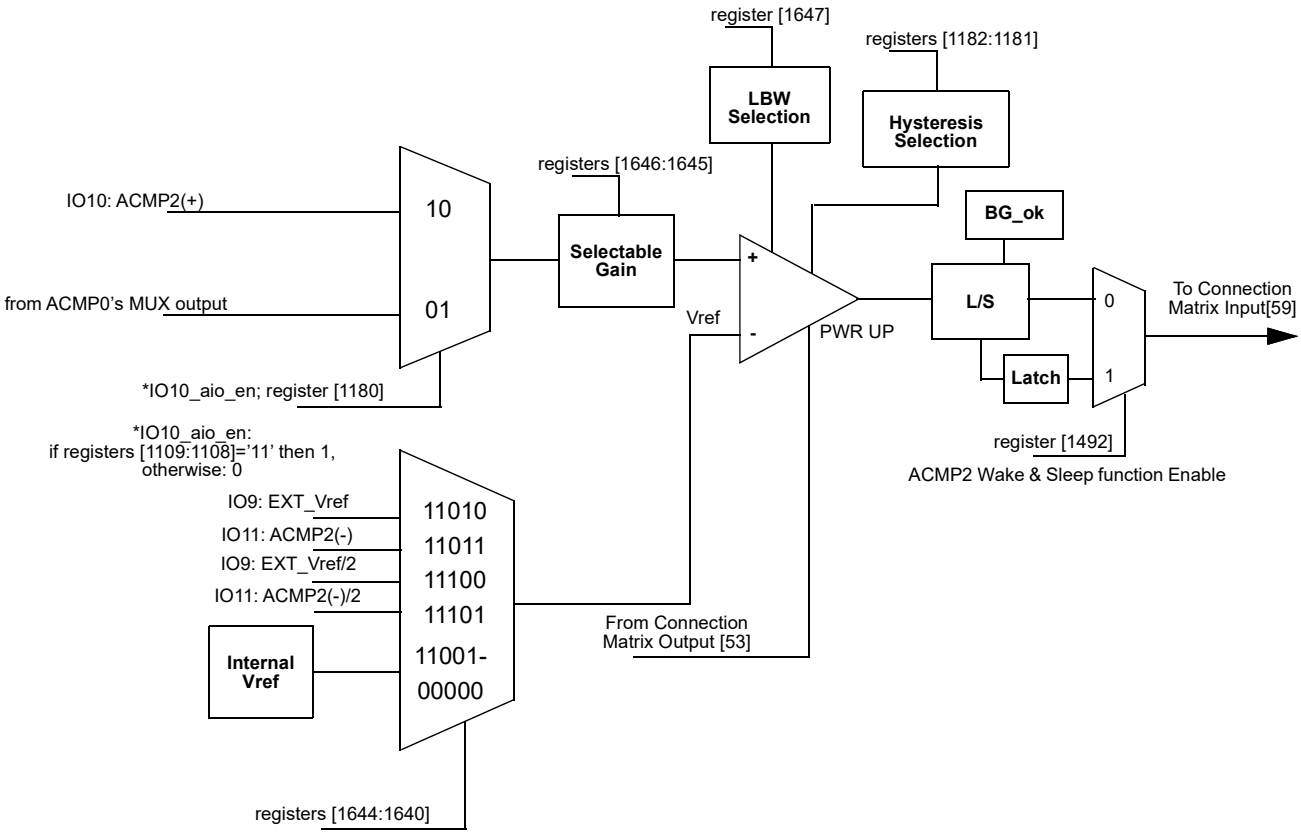


Figure 51: ACMP2 Block Diagram

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Table 88: ACMP2 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP2 Positive Input Source Select	[1180]	0: IO10 1: ACMP0 IN+ source
ACMP2 Hysteresis Enable	[1182:1181]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50mV & 200mV hysteresis.)
ACMP2 Wake & Sleep function Enable	[1492]	0: Disable 1: Enable
ACMP2 In Voltage Select	[1644:1640]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO11: ACMP2- 11100: IO9: EXT_Vref /2 11101: IO11: ACMP2-/2 11110: Reserved 11111: Reserved
ACMP2 Positive Input Divider	[1646:1645]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP2 Low Bandwidth (Max: 1 MHz) Enable	[1647]	0: Off 1: On

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8.4 ACMP3 BLOCK DIAGRAM AND REGISTER SETTINGS

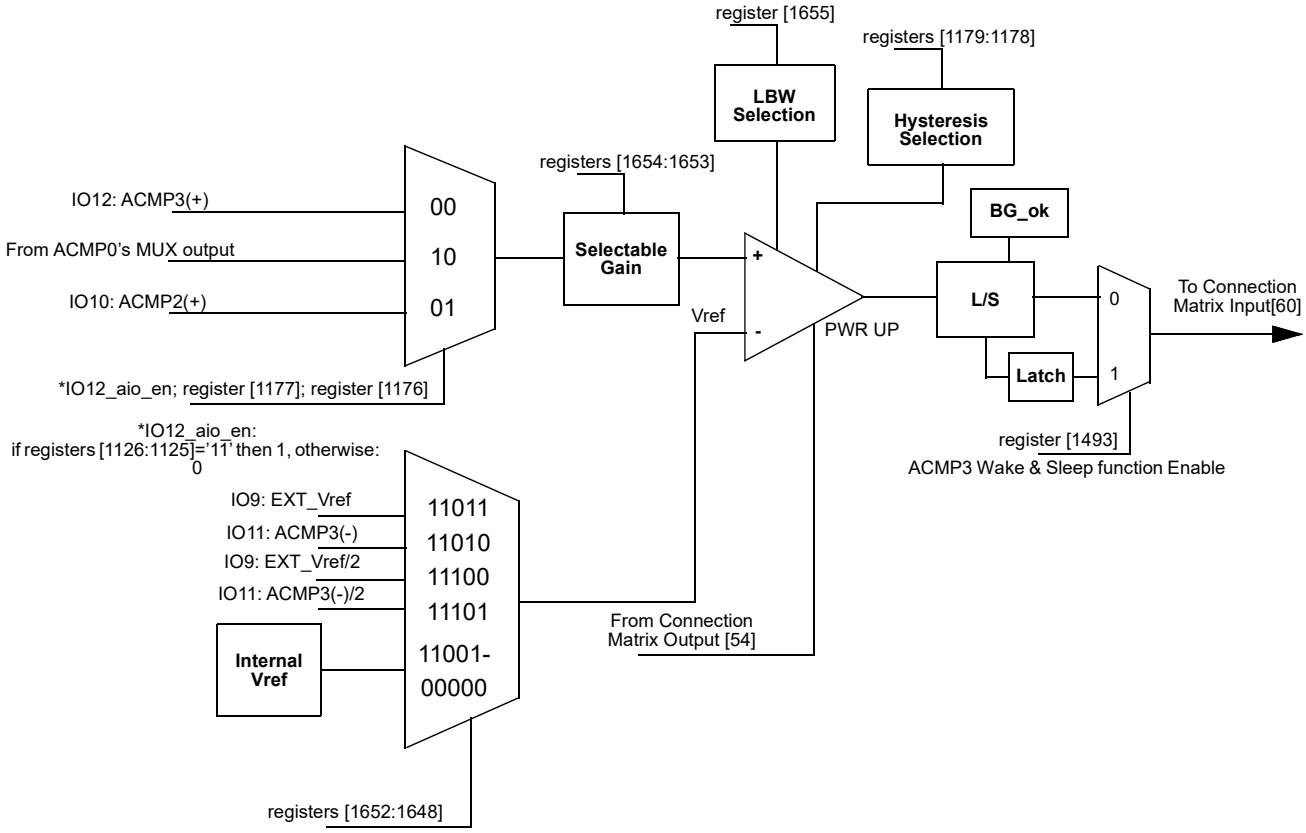


Figure 52: ACMP3 Block Diagram

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Table 89: ACMP3 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP3 Positive Input Source Select	[1177:1176]	00: IO12 01: ACMP2 IN+ source 10: ACMP0 IN+ source 11: Reserved
ACMP3 Hysteresis Enable	[1179:1178]	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50 mV & 200 mV hysteresis.)
ACMP3 Wake & Sleep function Enable	[1493]	0: Disable 1: Enable
ACMP3 In Voltage Select	[1652:1648]	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO11: ACMP3- 11100: IO9: EXT_Vref/2 11101: IO11: ACMP3-/2 11110: Reserved 11111: Reserved
ACMP3 Positive Input Divider	[1654:1653]	00: 1.00x 01: 0.50x 10: 0.33x 11: 0.25x
ACMP3 Low Bandwidth (Max: 1 MHz) Enable	[1655]	0: Off 1: On

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9 Pipe Delay

The SLG46517 has a pipe delay logic cell that is shared with the LUT3_10 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section 7.3 for the description of this Combination Function macrocell.

10 Programmable Delay/Edge Detector

The SLG46517 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. See the timing diagrams below for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

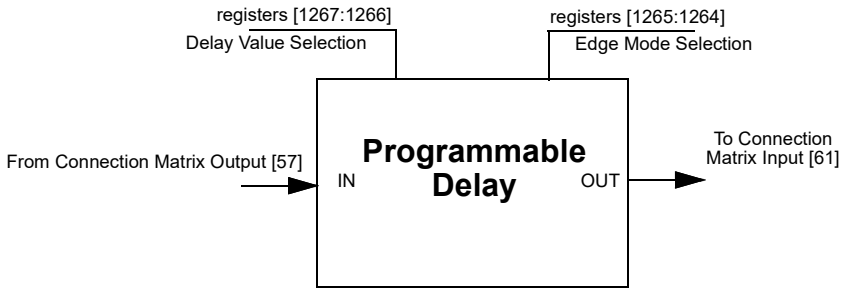


Figure 53: Programmable Delay

10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

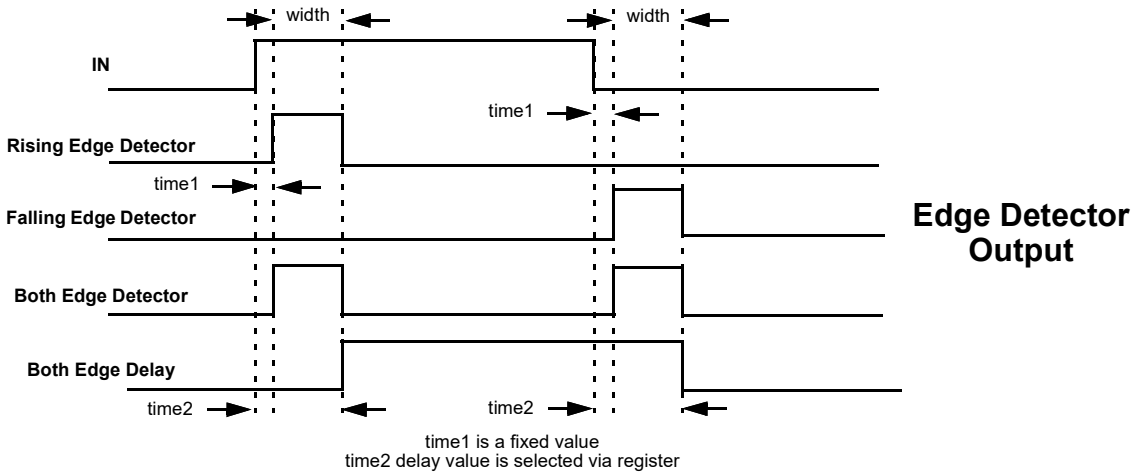


Figure 54: Edge Detector Output

Please refer to Table 13.

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Table 90: Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Select the edge mode of programmable delay & edge detector	[1265:1264]	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (V_{DD} = 3.3V, typical condition)	[1267:1266]	00: 165 ns 01: 300 ns 10: 440 ns 11: 575 ns

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11 Additional Logic Function. Deglitch Filter

The SLG46517 has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions. See Section 3.5.

11.1 DEGLITCH FILTER/EDGE DETECTOR

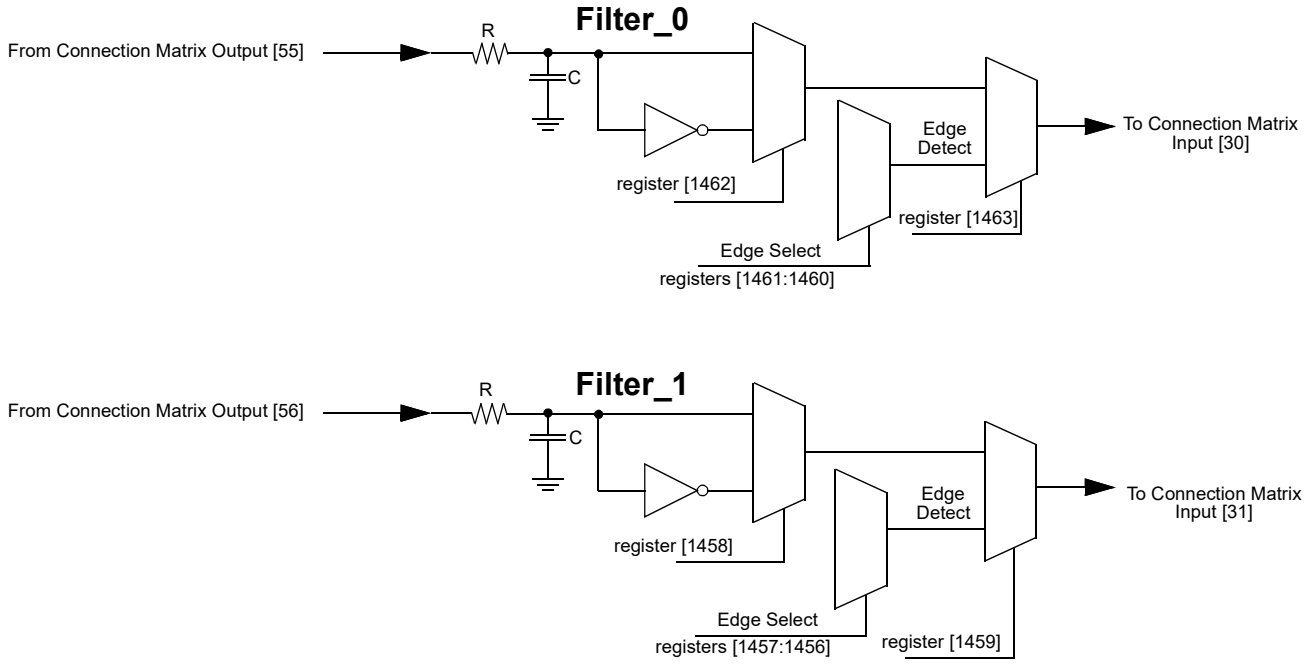


Figure 55: Deglitch Filter/Edge Detector

Table 91: Deglitch Filter Register Settings

Signal Function	Register Bit Address	Register Definition
Filter_1/Edge Detector_1 output Polarity Select	[1458]	0: Filter_1 output 1: Filter_1 output inverted
Filter_1 or Edge Detector_1 Select (Typ. 30 nS @V_{DD}=3.3 V)	[1459]	0: Filter_1 1: Edge Detector_1
Filter_0/Edge Detector_0 output Polarity Select	[1462]	0: Filter_0 output 1: Filter_0 output inverted
Filter_0 or Edge Detector_0 Select (Typ. 47 nS @V_{DD}=3.3 V)	[1463]	0: Filter_0 1: Edge Detector_0

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12 Voltage Reference

12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46517 has a Voltage Reference (Vref) Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from IOs 5, 9, and 11. The macrocell also has the option to output reference voltages on IO 15. See Table 92 for the available selections for each analog comparator. Also, see Figure 56, which shows the reference output structure.

12.2 VREF SELECTION TABLE

Table 92: Vref Selection Table

SEL[4:0]	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF
11101	vref_ext_acmp0/2	vref_ext_acmp1/2	vref_ext_acmp2/2	vref_ext_acmp2/2
11100	vref_ext_acmp1/2	vref_ext_acmp1/2	vref_ext_acmp1/2	vref_ext_acmp1/2
11011	vref_ext_acmp0	vref_ext_acmp1	vref_ext_acmp2	vref_ext_acmp2
11010	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1
11001	V_{DD}/4	V_{DD}/4	V_{DD}/4	V_{DD}/4
11000	V_{DD}/3	V_{DD}/3	V_{DD}/3	V_{DD}/3
10111	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20
00010	0.15	0.15	0.15	0.15
00001	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05

V_{DD}	Practical Vref Range	Note
2.0 V - 5.5 V	50 mV ~ 1.2 V	
1.7 V - 2.0V	50 mV ~ 1.0 V	Do not operate above 1.0 V

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12.3 VREF BLOCK DIAGRAM

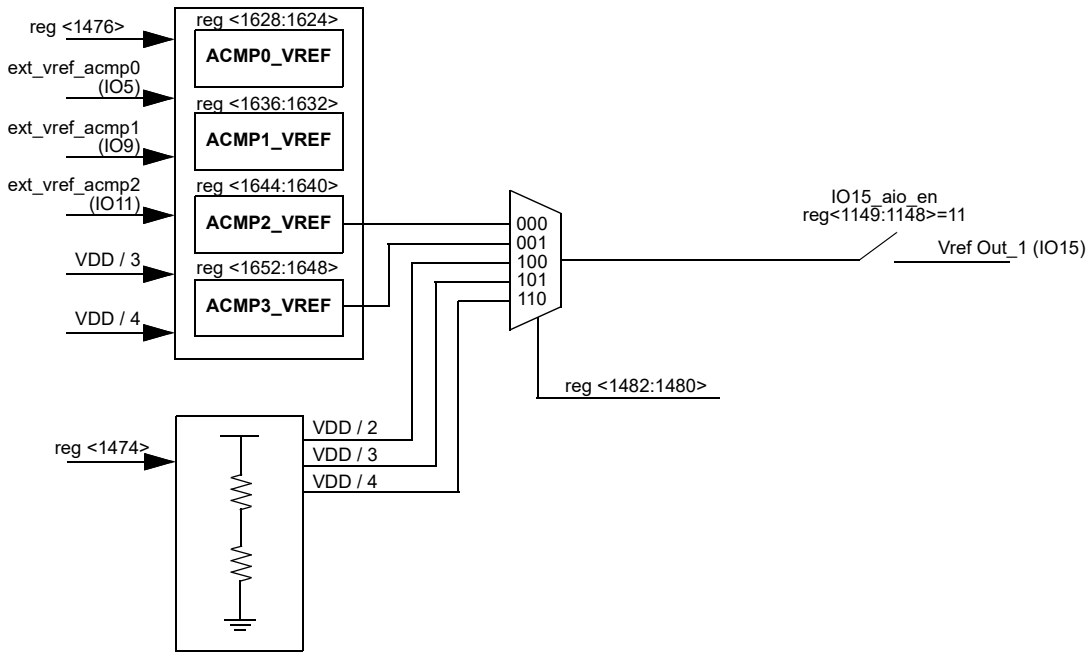


Figure 56: Voltage Reference Block Diagram

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12.4 VREF LOAD REGULATION

Note 1: Vref buffer performance is not guaranteed at V_{DD} < 2.7 V.

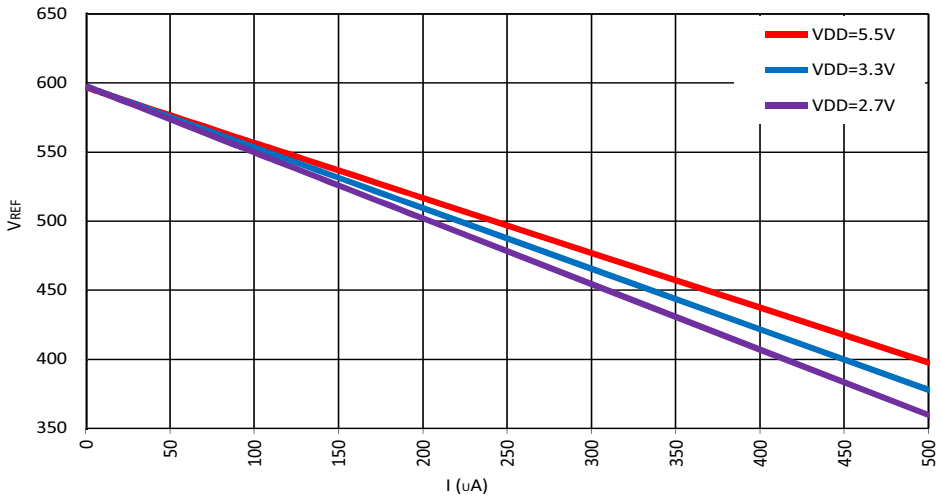


Figure 57: Typical Load Regulation, Vref = 600 mV, T = -40 °C to +85 °C, Buffer - Enable

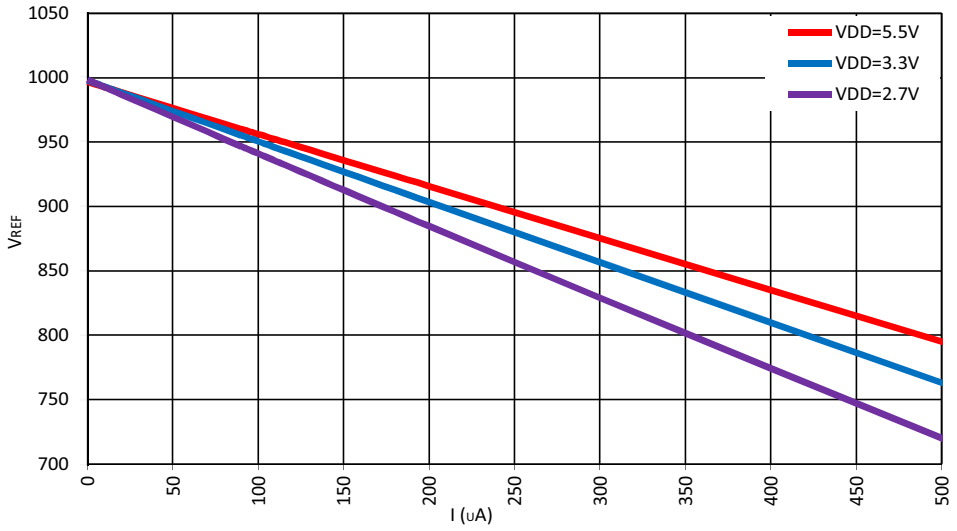


Figure 58: Typical Load Regulation, Vref = 1000 mV, T = -40 °C to +85 °C, Buffer - Enable

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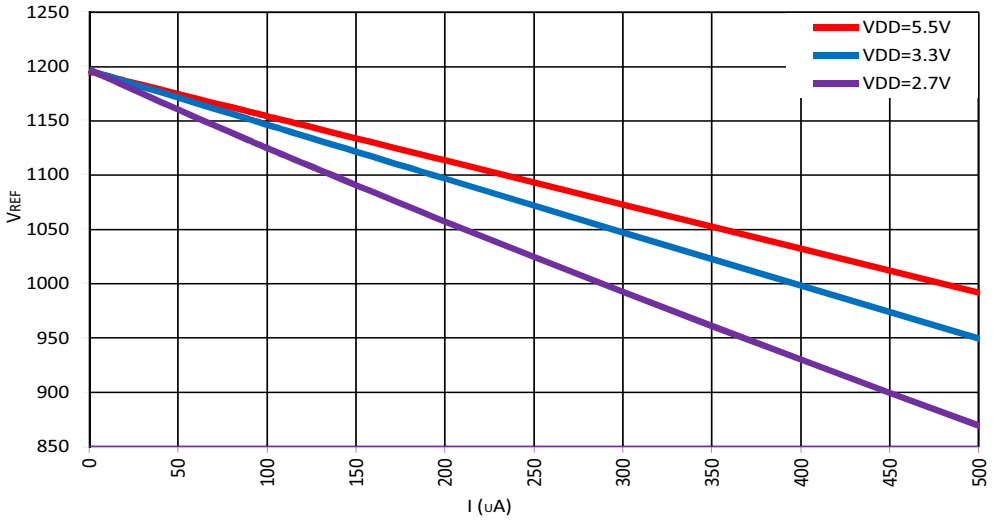


Figure 59: Typical Load Regulation, Vref = 1200 mV, T = -40 °C to +85 °C, Buffer - Enable

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13 Clocking

13.1 OSC GENERAL DESCRIPTION

The SLG46517 has three internal oscillators. RC Oscillator that runs at 25 kHz/2 MHz (OSC0), Oscillator that runs at 25 MHz (OSC1) and Crystal Oscillator. It is possible to use all three oscillators simultaneously. The fundamental frequency can also come from clock input (IO15 or IO17 for 25 kHz/2 MHz and IO14 for 25 MHz or Crystal OSC), see Section 18.

13.2 25 KHZ/2 MHZ AND 25 MHZ RC OSCILLATORS

There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The pre-divider allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. The second stage divider (only for 25 kHz/2 MHz Oscillator) has an input of frequency from the pre-divider, and outputs one of seven different frequencies on Connection Matrix Input lines [27] (OUT0) and [28] (OUT1). See Figure 60 and Figure 61 for details.

There are two modes of the POWER CONTROL pin, (register [1658] for 25 kHz/2 MHz OSC and register [1657] for 25 MHz OSC):

- **POWER-DOWN [0]**. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned on. If PWR CONTROL input of oscillator is HIGH the oscillator will be turned off and OSC divider will reset.
- **FORCE ON [1]**. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned on. If PWR CONTROL input of oscillator is LOW the oscillator will be turned off.

The PWR CONTROL signal has the highest priority.

The SLG46517 has a 25 kHz/2 MHz OSC FAST START-UP function register [1338] (1 – on, 0 – off). It allows the OSC to run immediately after power-up this decreases the settling time. Note that when OSC FAST START-UP is on, the current consumption will rise.

The user can select two OSC POWER MODEs (register [1343] for 25 kHz/2 MHz OSC and register [1341] for 25 MHz OSC):

- If **AUTO POWER-ON [0]** is selected, the OSC will run when any macrocell that uses OSC is powered on.
- If **FORCE POWER-ON [1]** is selected, the OSC will run when the SLG46517 is powered on.

OSC can be turned on by:

- Register control (force Power-On)
- Delay mode, when delay requires OSC
- CNT/FSM

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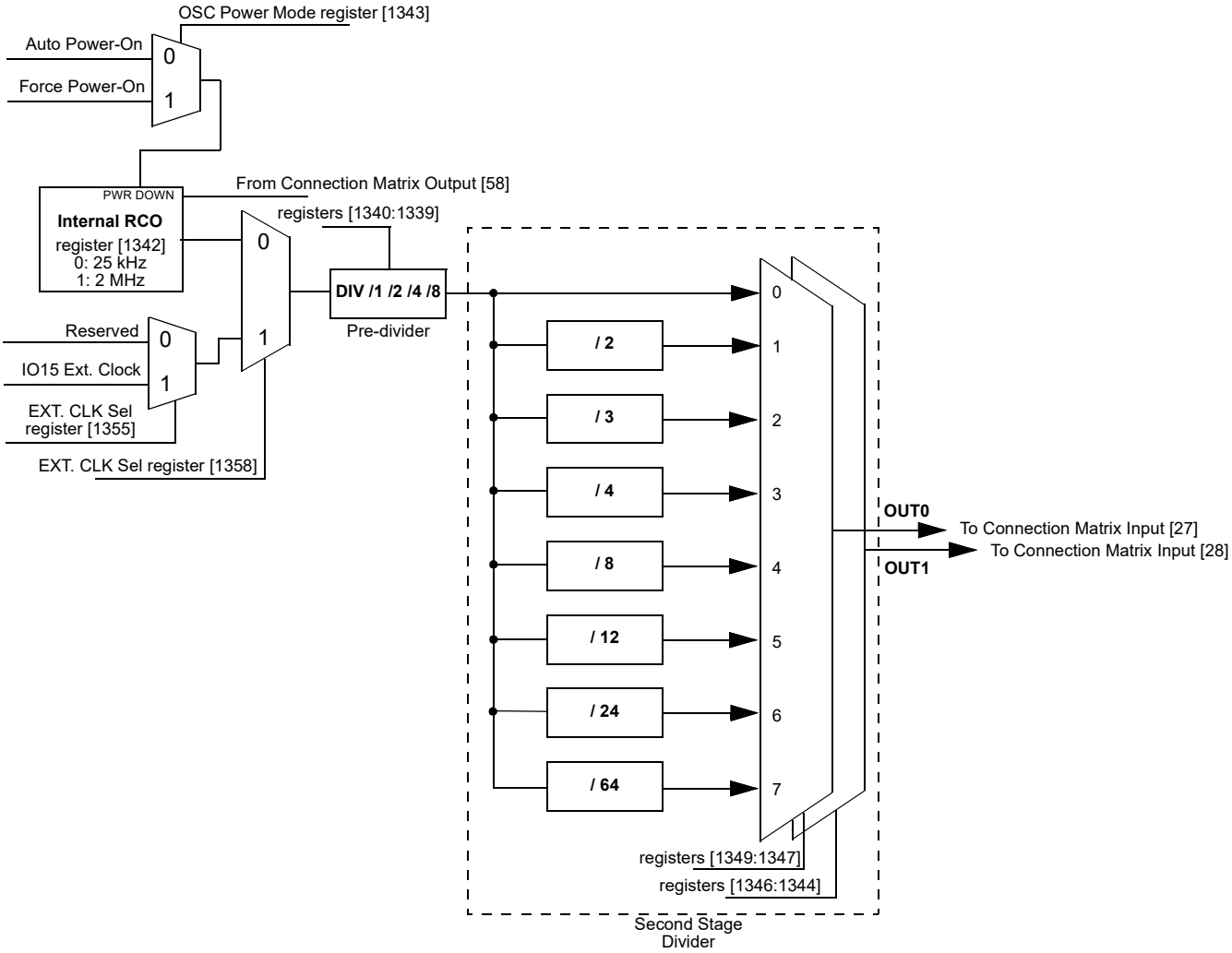


Figure 60: 25 kHz/2 MHz RC OSC Block Diagram

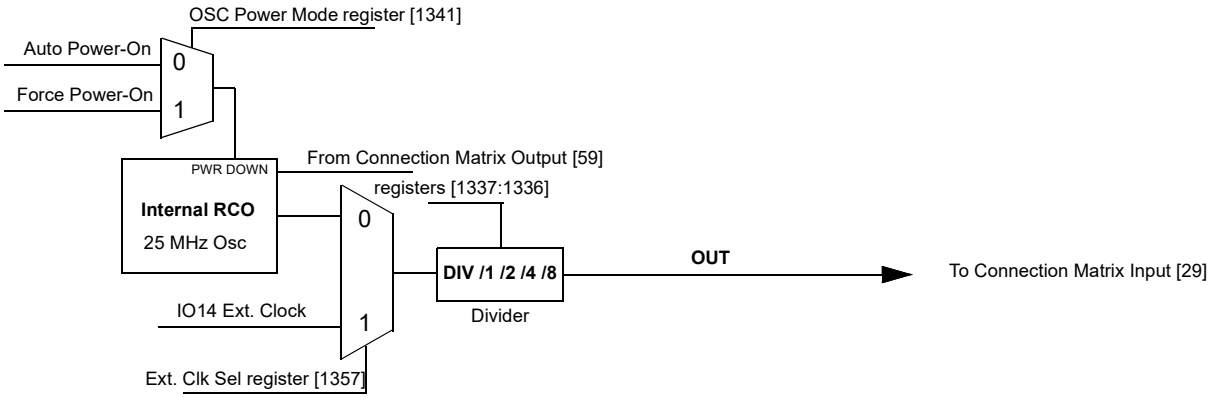


Figure 61: 25 MHz RC OSC Block Diagram

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13.3 OSCILLATORS POWER-ON DELAY

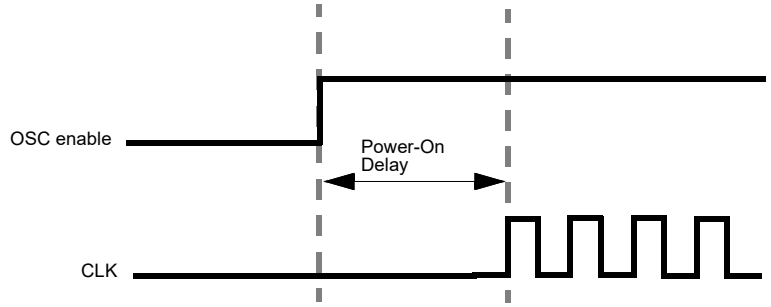


Figure 62: Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.

Note 2: “OSC enable” signal appears when any macrocell that uses OSC is powered on.

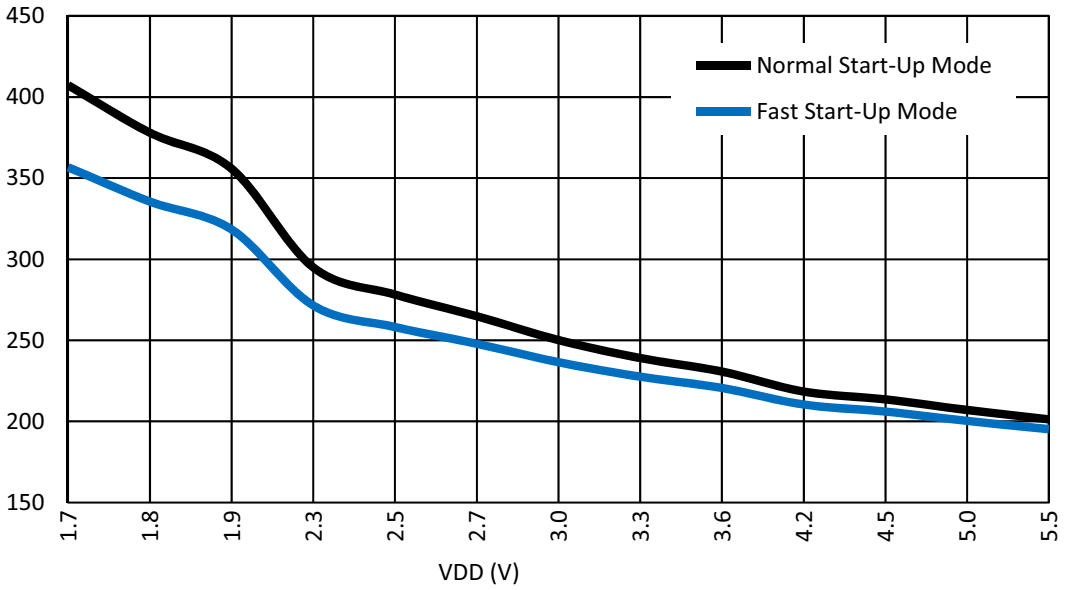


Figure 63: Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 2 MHz

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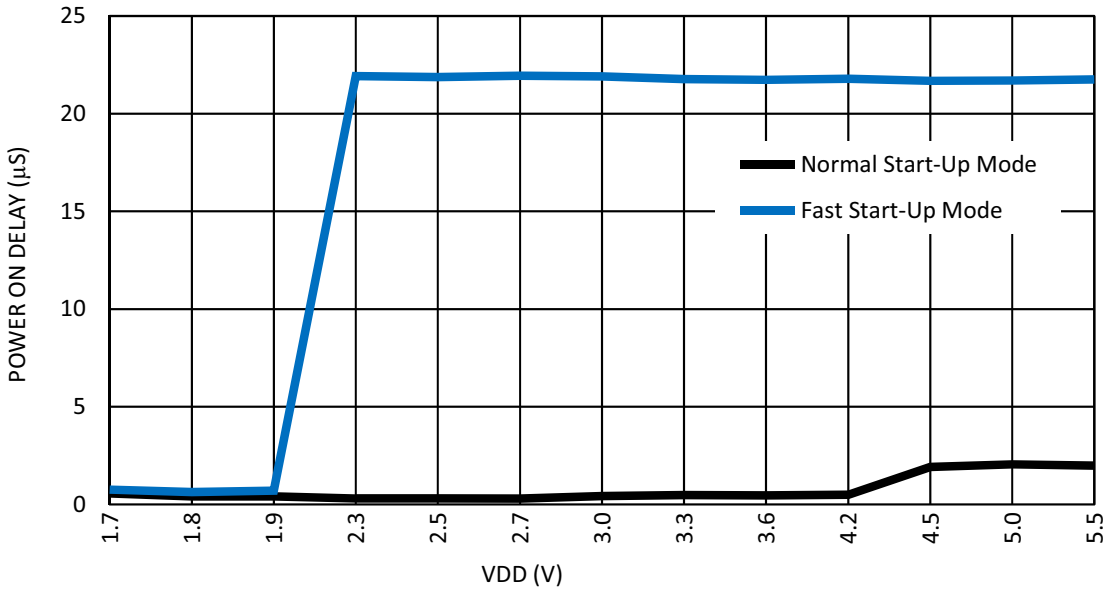


Figure 64: Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC0 = 25 kHz

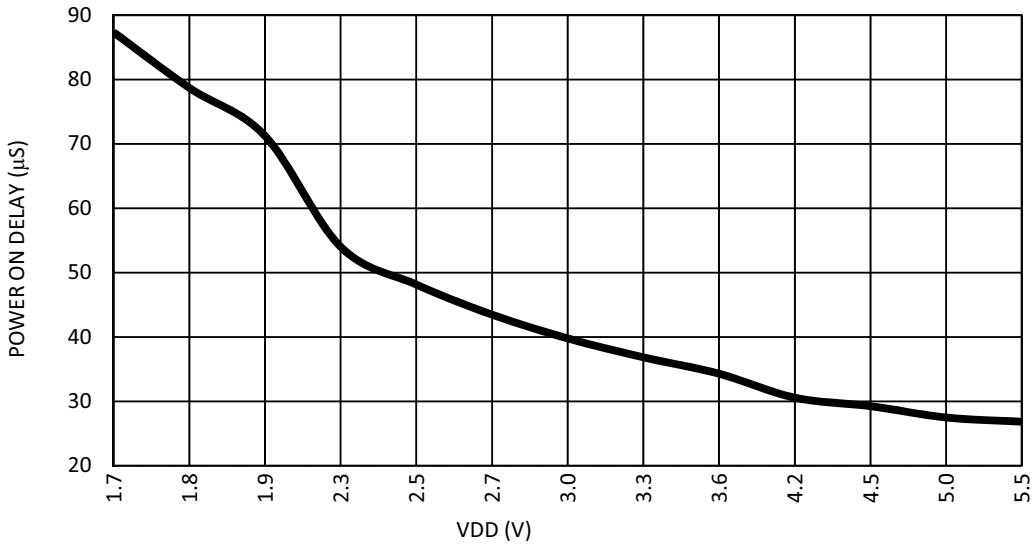


Figure 65: Oscillator Maximum Power-On Delay vs. V_{DD} at T = 25 °C, OSC1 = 25 MHz

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13.4 OSCILLATORS ACCURACY

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

Note: For more information see Section 3.6.

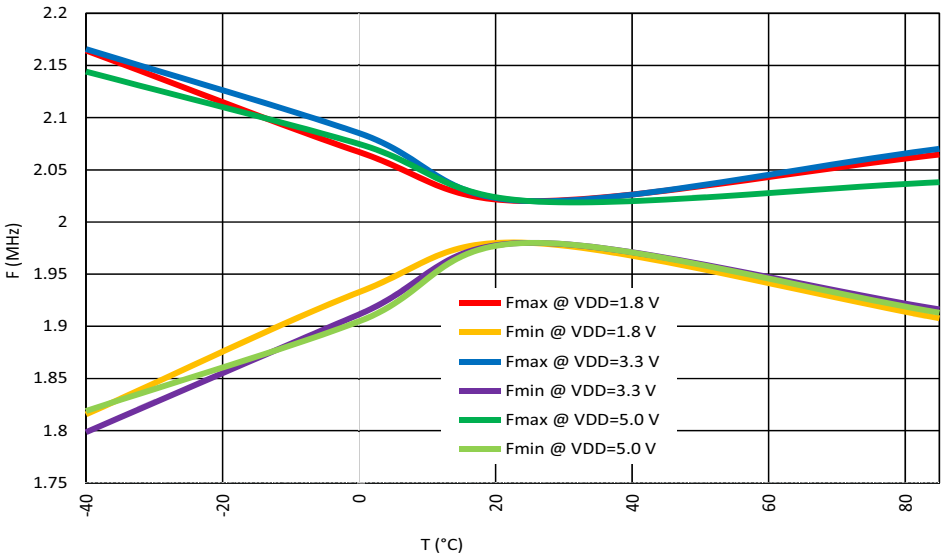


Figure 66: Oscillator Frequency vs. Temperature, OSC0 = 2 MHz

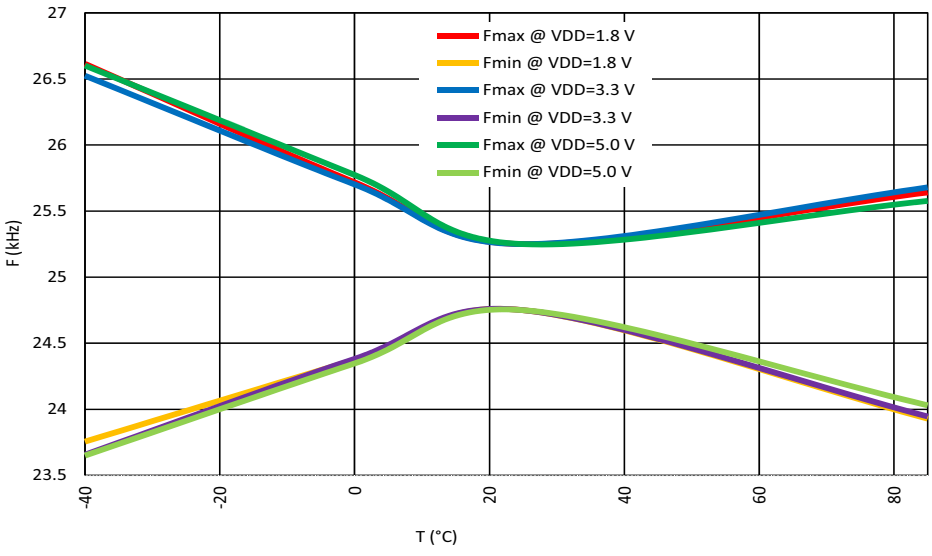


Figure 67: Oscillator Frequency vs. Temperature, OSC0 = 25 kHz

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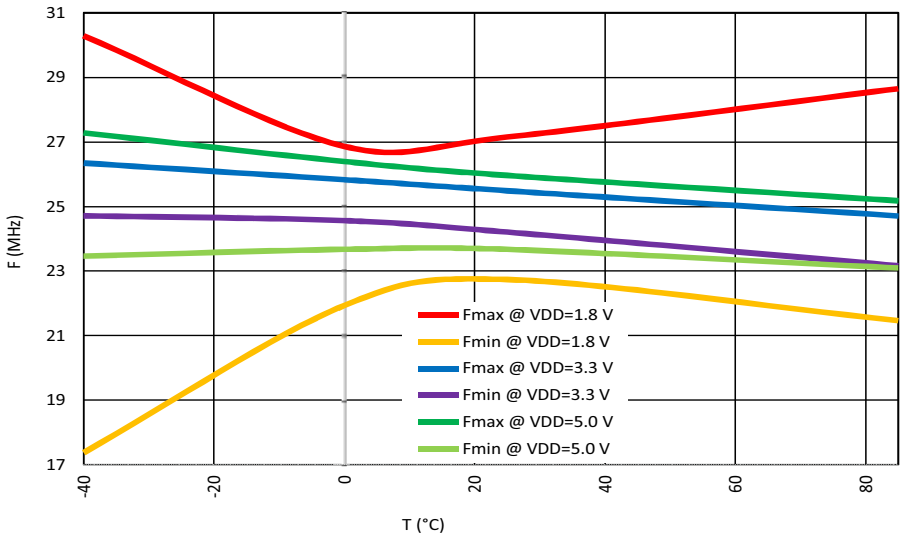


Figure 68: Oscillator Frequency vs. Temperature, OSC1 = 25 MHz

Note: 25 MHz RC OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

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14 Crystal Oscillator

The Crystal OSC provides high precision and stability of the output frequency. IO14 and IO13 are input and output, respectively, of an inverting amplifier which is configured for use as an On-chip Oscillator, as shown in Figure 70. Either a quartz crystal or a ceramic resonator may be used. The optimal value of the capacitors depends on the crystal or resonator in use, the amount of stray capacitance, and the electromagnetic noise of the environment. Refer to Table 93. For ceramic resonators, the capacitor values given by the manufacturer should be used. It is possible to use an external clock source, it must be connected to IO14. In this case no external components are required.

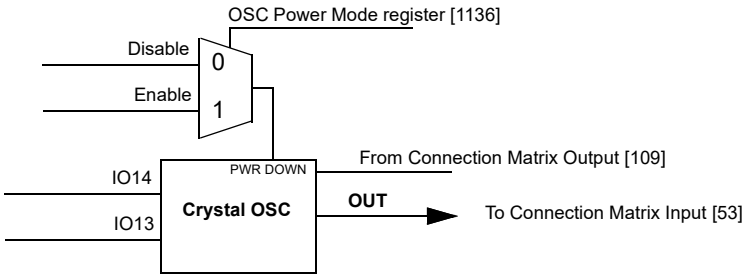


Figure 69: Crystal OSC Block Diagram

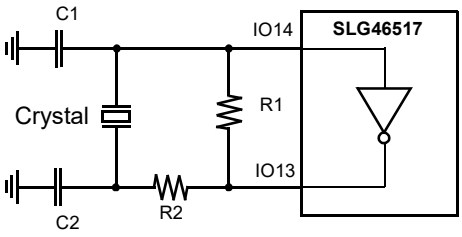


Figure 70: External Crystal Connection

Table 93: External Components Selection

f	C1	C2	R1	R2
32.768 kHz	10 pF	330 pF	20 MΩ	20 kΩ
4 - 40 MHz	12 pF	12 pF	1 MΩ	0 Ω

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15 Power-On Reset

The SLG46517 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

15.1 GENERAL OPERATION

To start the POR sequence in the SLG46517, the voltage applied on the V_{DD} should be higher than the Power-On threshold (Note). The full operational V_{DD} range for the SLG46517 is 1.71 V to 5.5 V (1.8 V ±5% to 5 V±10%). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG46517 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On threshold can vary by PVT, but typically it is 1.6 V.

The SLG46517 is guaranteed to be powered down and nonoperational when the V_{DD} voltage (voltage on V_{DD}) is less than 0.6V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To power-down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

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15.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 71.

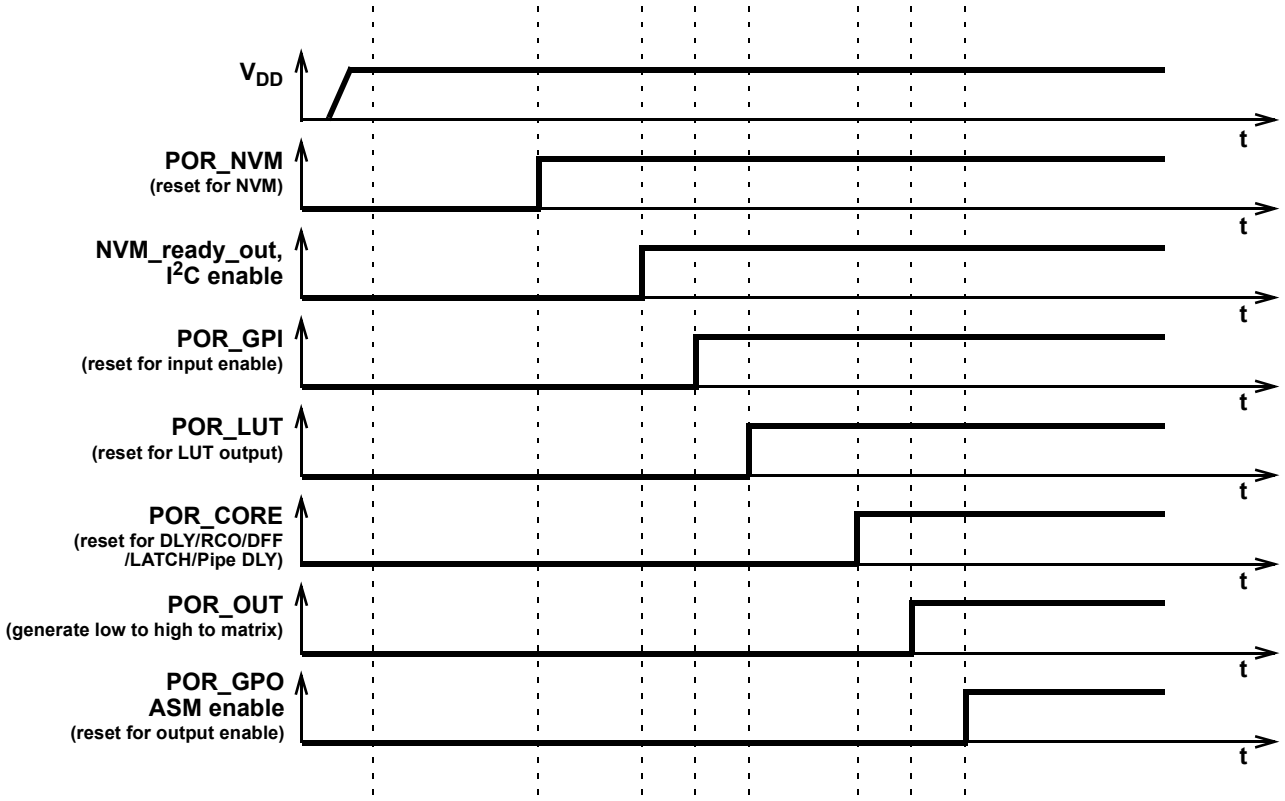


Figure 71: POR Sequence

As can be seen from Figure 71 after the V_{DD} has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

15.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46517 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 72 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P_DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next,

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all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

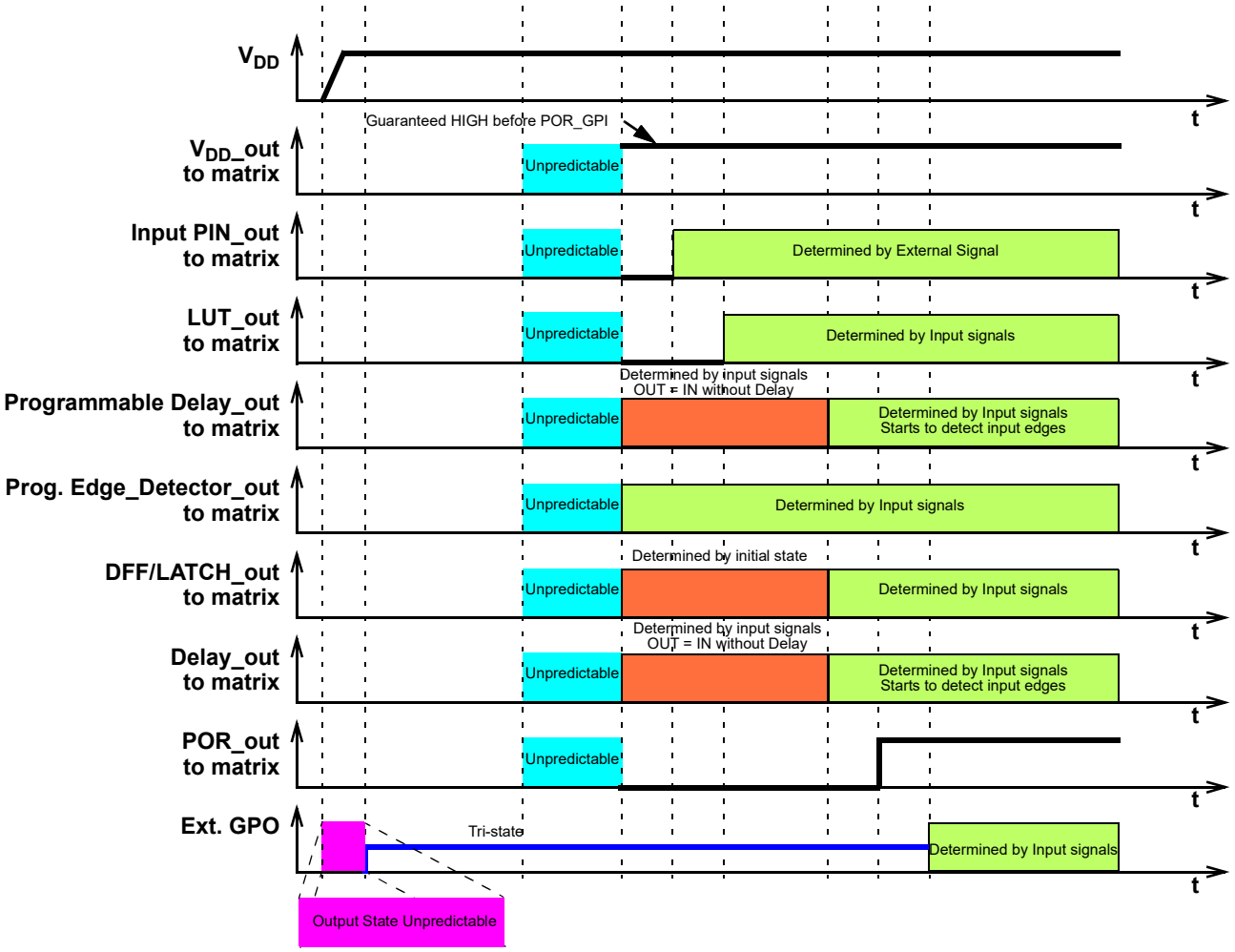


Figure 72: Internal Macrocell States during POR Sequence

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15.3.1 Initialization

All internal macrocells by default have initial LOW level. Starting from indicated power-up time of 1.15 V to1.6 V, macrocells in GPAK are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. I^2C.
2. Input PINs, ACMP, Pull-up/down.
3. LUTs.
4. DFFs, Delays/Counters, Pipe Delay.
5. POR output to matrix.
6. Output PIN corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs - 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the V_{DD} level. There are ESD Diodes between PIN → V_{DD} and PIN → GND on each PIN. So, if the input signal applied to PIN is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input PIN, and V_{DD} will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

15.3.2 Power-Down

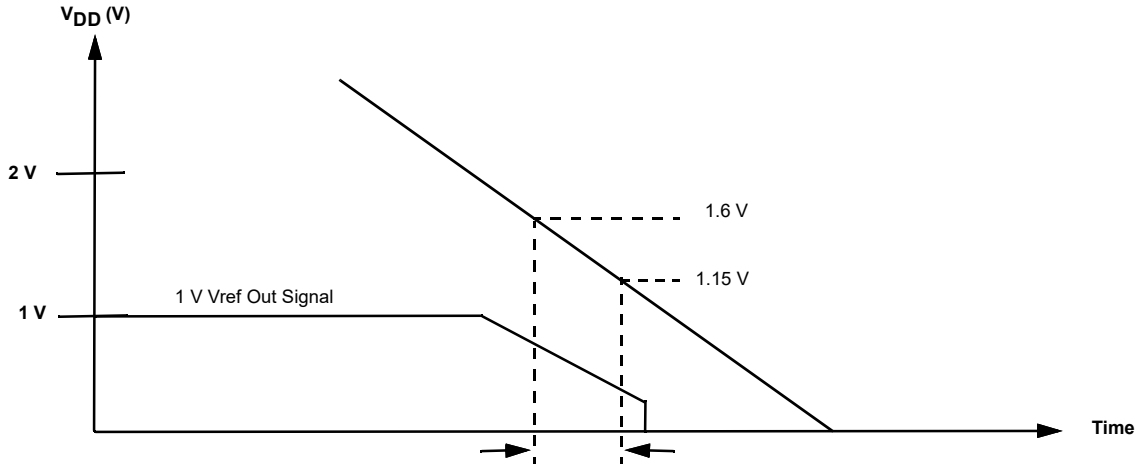


Figure 73: Power-Down

During power-down, macrocells in SLG46517 are powered off and logic macrocells may switch states after falling below 1.4 V. The IO buffers are disabled when POR goes low at V_{DD} ~1 V. Please note that during a slow rampdown, outputs can possibly switch state during this time.

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16 Asynchronous State Machine Macrocell

16.1 ASM MACROCELL OVERVIEW

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in Figure 74.

This macrocell has a total of 25 inputs, as shown in Figure 75, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state. Each of the 24 inputs is level sensitive and active high, meaning that a high level input will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user defined state machine design. There is on nReset input which will drive an immediate state transition to the user-defined Initial/Reset state when active, shown in red, in the Figure 74. For more details refer to Section 16.2.

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM. For more details refer to Section 16.3.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to ensure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. Figure 74 is a representation of the user design at the logical level, and Figure 75 shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

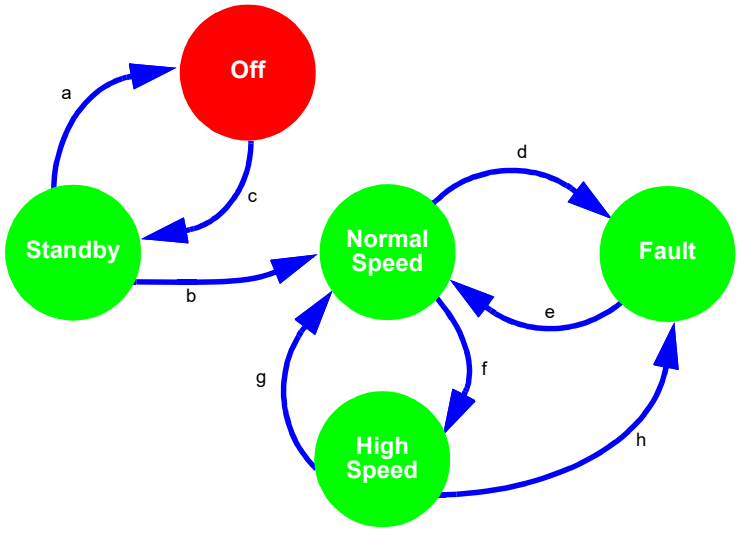


Figure 74: Asynchronous State Machine State Transitions

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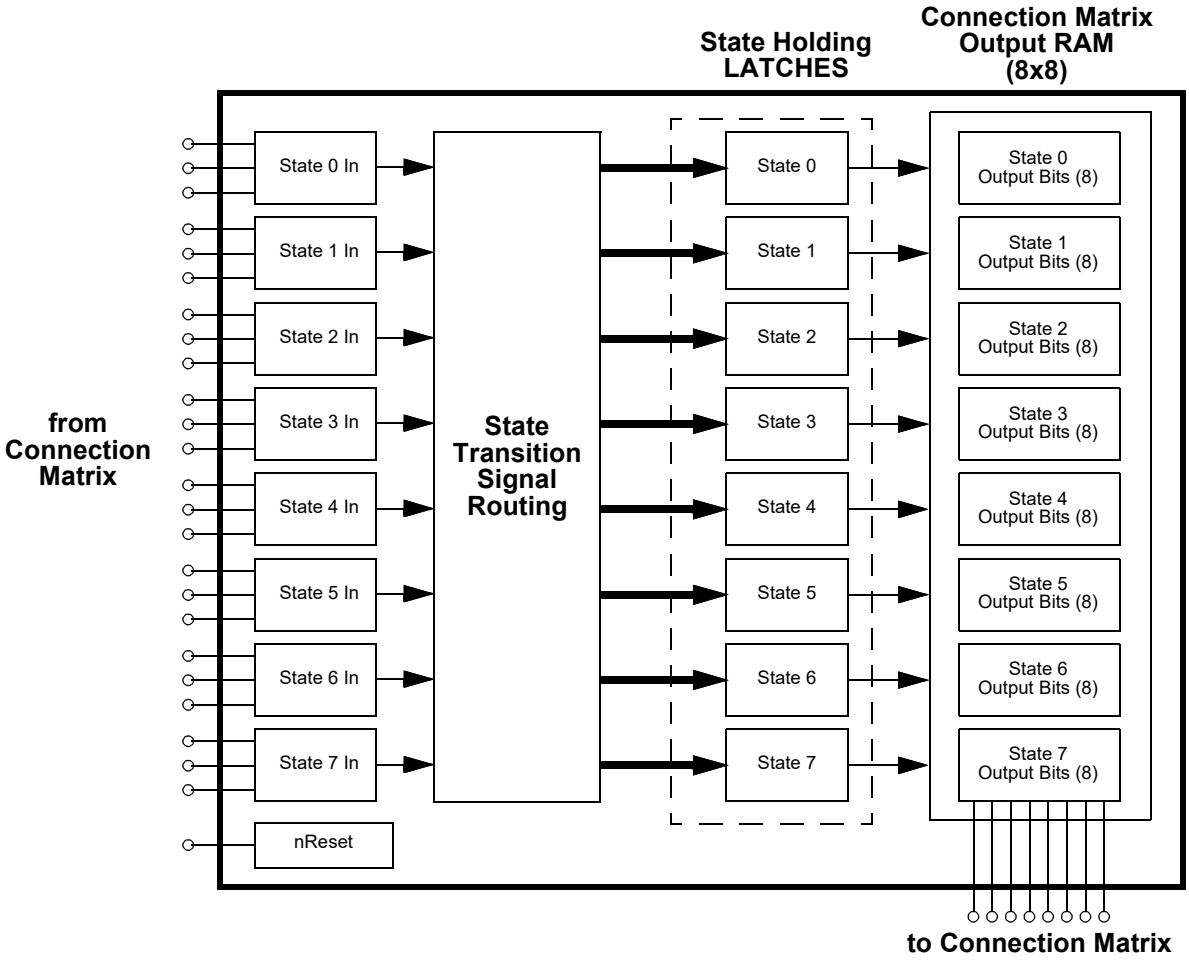


Figure 75: Asynchronous State Machine

16.2 ASM INPUTS

The ASM macrocell has a total of 25 inputs which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in Figure 76. Each of these inputs is level sensitive, and active high. A high level input will trigger a state transition.

These inputs are grouped so that each set of 3 inputs can drive a state transition **going into** a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in Figure 77.

There is no limitation on the number of transitions that can be supported coming out of a particular state, the user can select to have transitions going from a state to all other states, shown in Figure 78.

The ASM macrocell also has a nReset input highlighted in blue in Figure 76. This input is level sensitive and active low. An active signal on this input will drive an immediate state transition to the user-defined Initial/Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

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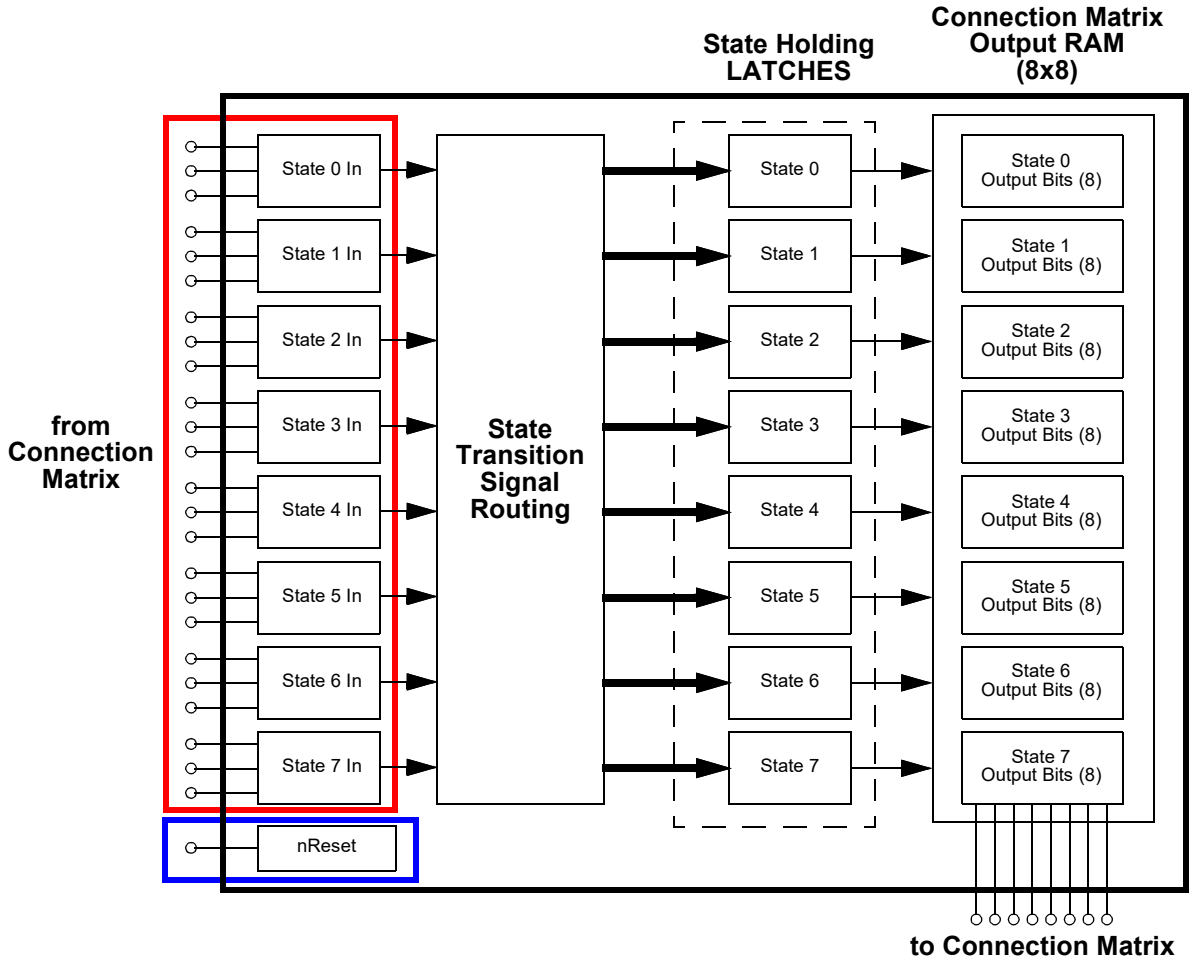


Figure 76: Asynchronous State Machine Inputs

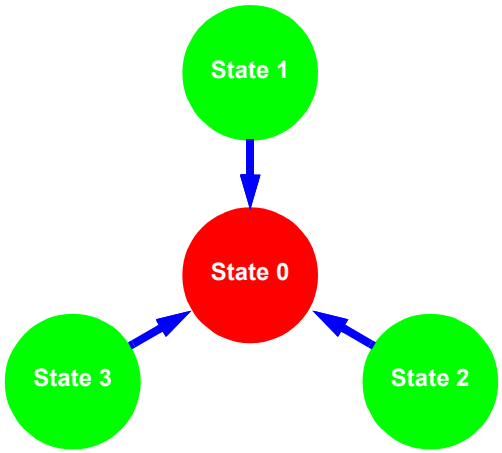


Figure 77: Maximum 3 State Transitions into Given State

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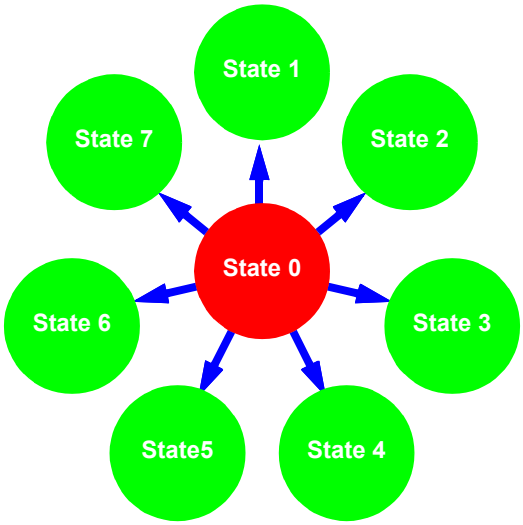


Figure 78: Maximum 7 State Transitions out of a Given State

16.3 ASM OUTPUTS

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in Figure 79. The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM macrocell, as shown in Figure 78.

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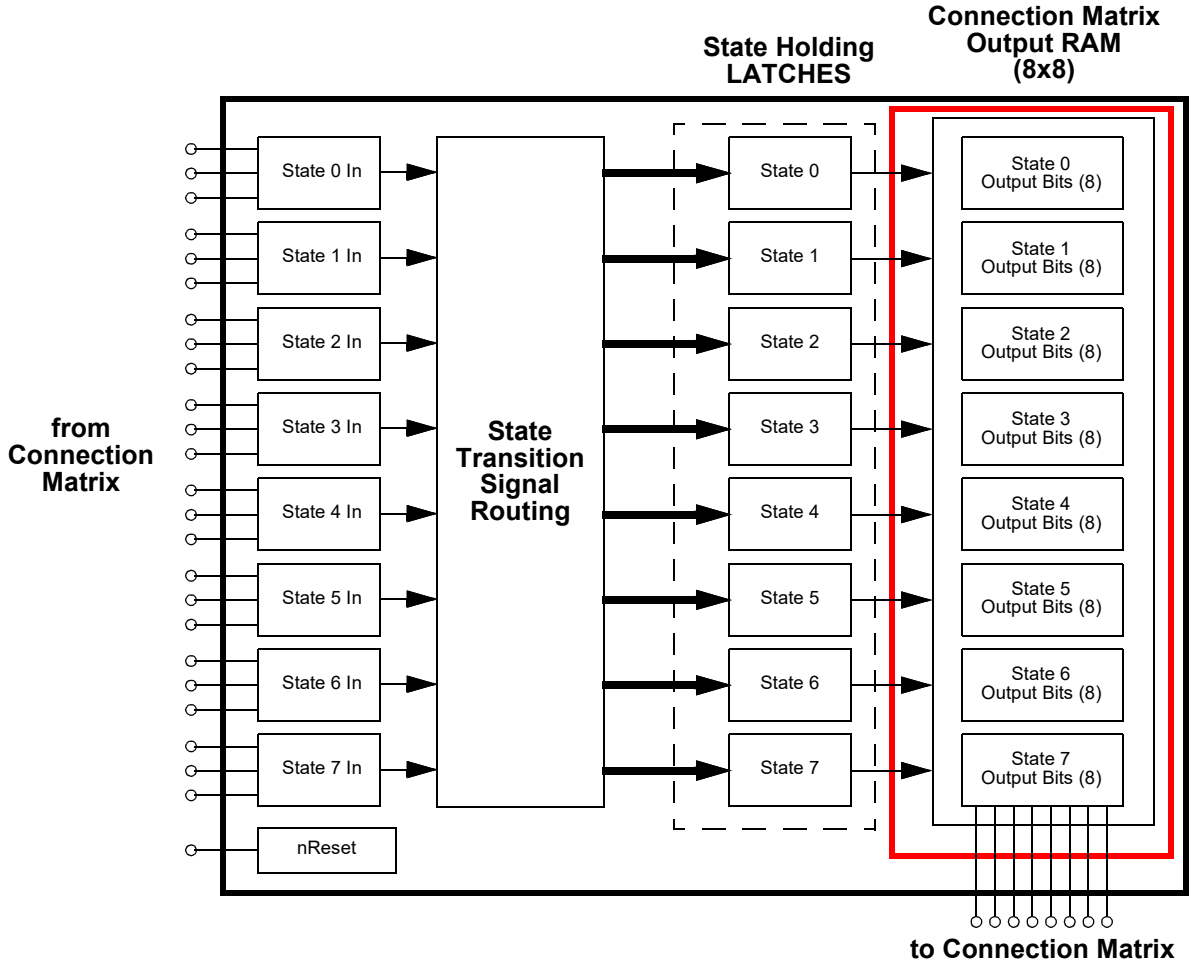


Figure 79: Connection Matrix Output RAM

Table 94: ASM Editor - Connection Matrix Output RAM

RAM								
State name	**Connection Matrix Output RAM**							
	OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0	0	1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

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There is a possibility to configure ASM (it's settings and transitions) via I^2C. Registers (registers [197:0]) correspond for ASM inputs, registers (registers [1727:1664]) correspond for ASM outputs configuration. Using I^2C commands (see Section 17.4) it is possible to read ASM settings and connections, as well as change them. Additionally, user can change Connection Matrix Output RAM bit configuration (bytes 0xD0 to 0xD7).

Note: After Connection Matrix Output RAM was updated via I^2C, ASM outputs to Connection Matrix can be changed only after ASM changes its state or after reset event. To change ASM outputs to Connection Matrix instantly after I^2C write command, ASM must be in reset all the time.

16.4 BASIC ASM TIMING

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in Figure 80 and Figure 81. The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time ($T_{st_out_delay}$). The minimum and maximum values of $T_{st_out_delay}$ define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

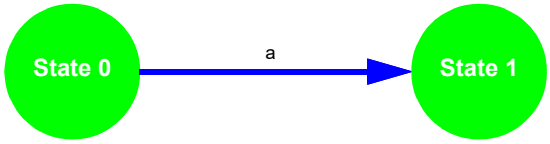


Figure 80: State Transition

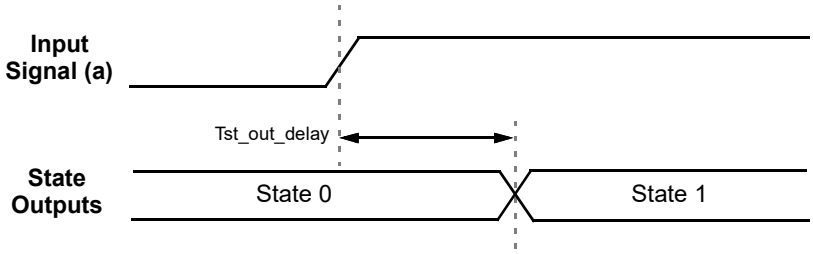


Figure 81: State Transition Timing

16.5 ASYNCHRONOUS STATE MACHINES VS. SYNCHRONOUS STATE MACHINES

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals.
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This macrocell does not have traditional set-up and hold time specifications which are related to incoming clock, as this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

16.6 ASM POWER CONSIDERATIONS

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in Figure 80 and Figure 82 below, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See Section 3.4 to find average current during state transitions.

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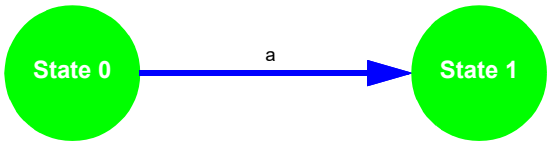


Figure 82: State Transition

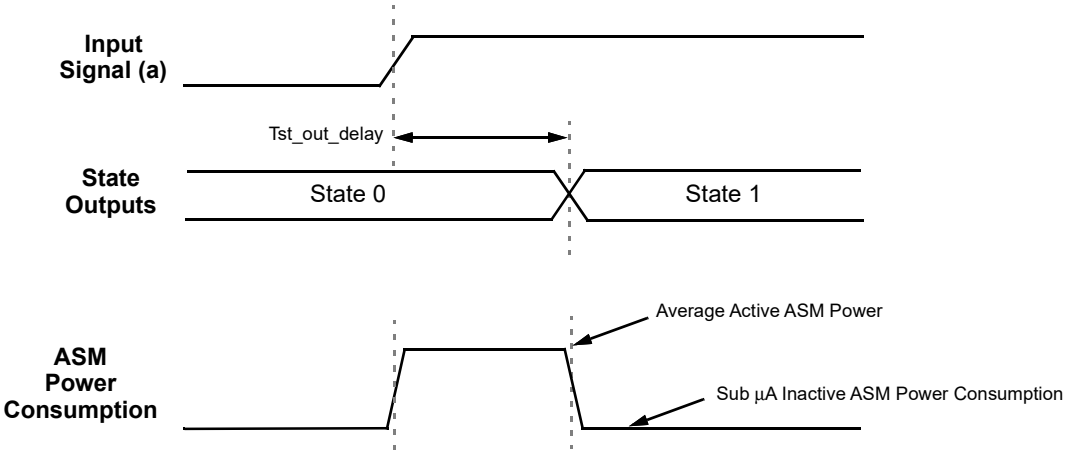


Figure 83: State Transition Timing and Power Consumption

16.7 ASM LOGICAL VS. PHYSICAL DESIGN

A successful design with the ASM macrocell must include both the logic level design, as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial/Reset state, and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

16.8 ASM SPECIAL CASE TIMING CONSIDERATIONS

16.8.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell) which is guaranteed to result in a state transition shown in Figure 84 and Figure 85. This pulse width is defined by the State Machine Input Pulse Acceptance Time (T_{st_pulse}). If a pulse width that is shorter than T_{st_pulse} is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of T_{st_pulse}), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

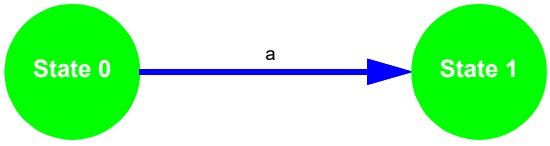


Figure 84: State Transition

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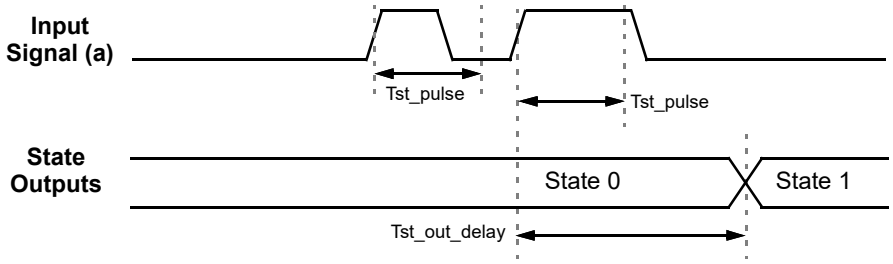


Figure 85: State Transition Pulse Input Timing

16.8.2 State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in Figure 86), and the signal that arrives sooner should drive the state transition that will “win”, or drive the state transition. If one signal arrives T_{st_comp} before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in Figure 87. If the two signals arrive within T_{st_comp} of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in Figure 88.

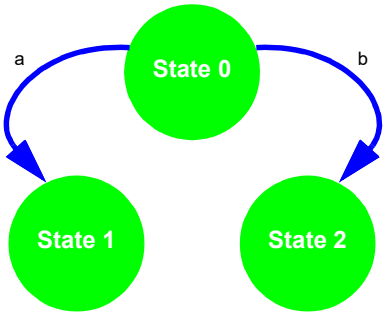


Figure 86: State Transition - Competing Inputs

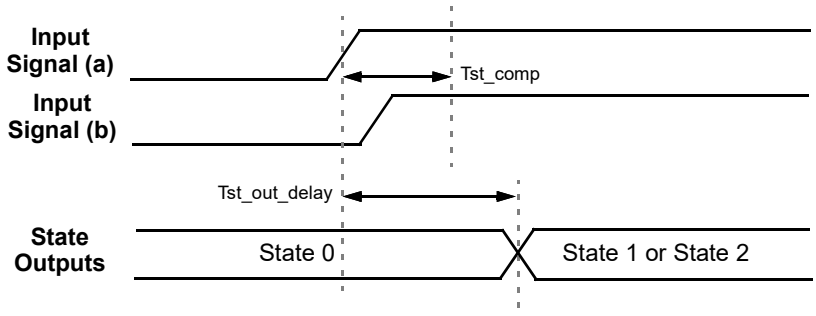


Figure 87: State Transition Timing - Competing Inputs Indeterminate

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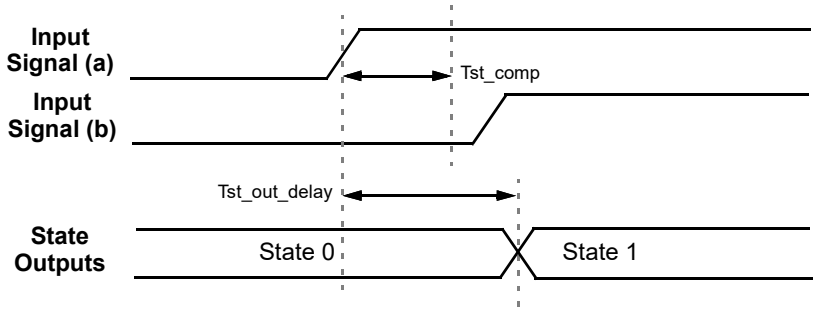


Figure 88: State Transition Timing - Competing Inputs Determinable

16.8.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for $T_{st_out_delay}$ time before making the transition to the next state. An example of this sequential behavior is shown in Figure 89 and the associated timing is shown in Figure 90.

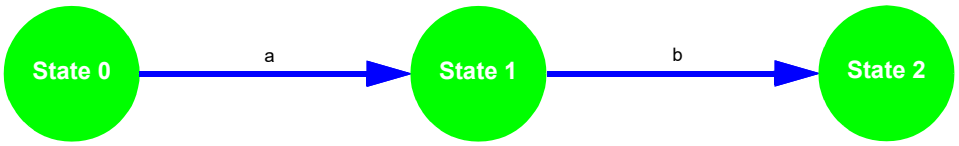


Figure 89: State Transition - Sequential

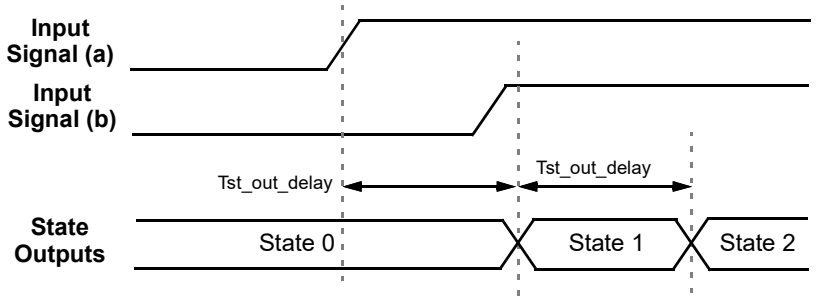


Figure 90: State Transition - Sequential Timing

16.8.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by $T_{st_out_delay}$. The example shown here in Figure 91 involves cycling between two states, but any number of two – eight states can be included in state transition closed cycling of this nature. Figure 92 shows the associated timing for closed cycling.

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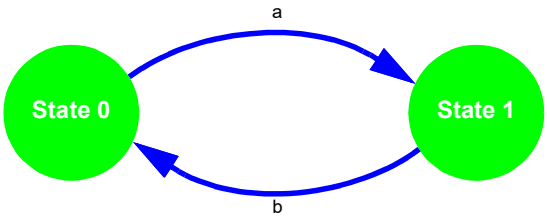


Figure 91: State Transition - Closed Cycling

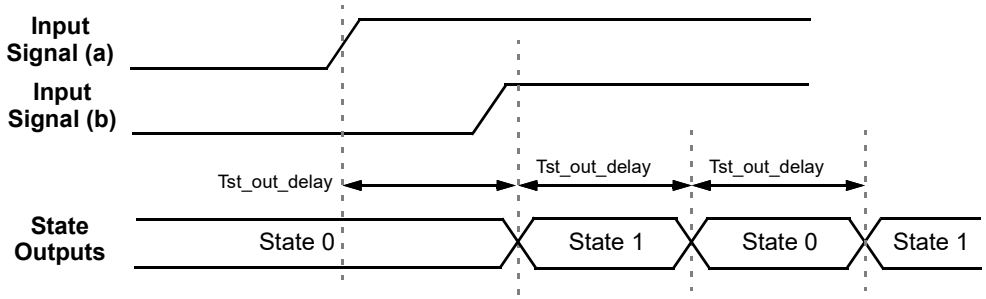


Figure 92: State Transition - Closed Cycling Timing

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17 I²C Serial Communications Macrocell

17.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits register [1832], register [1870], and register [1871]. See Section 17.5 for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

17.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 93. After the Start bit, the first four bits are a control code, which can be set by the user in registers [1867:1864]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46517 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46517.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 93 shows this basic command structure.

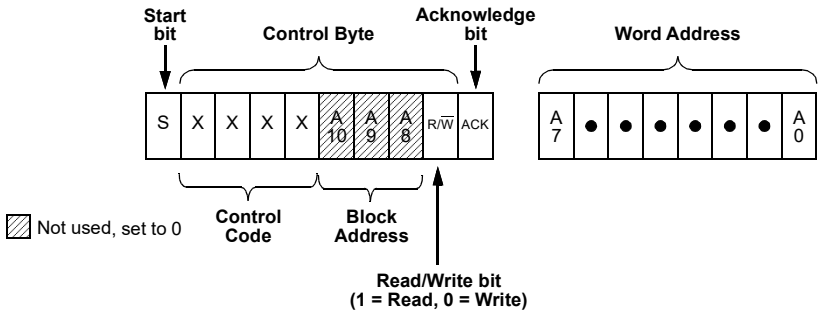


Figure 93: Basic Command Structure

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17.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 94. Timing specifications can be found in the Section 3.4.

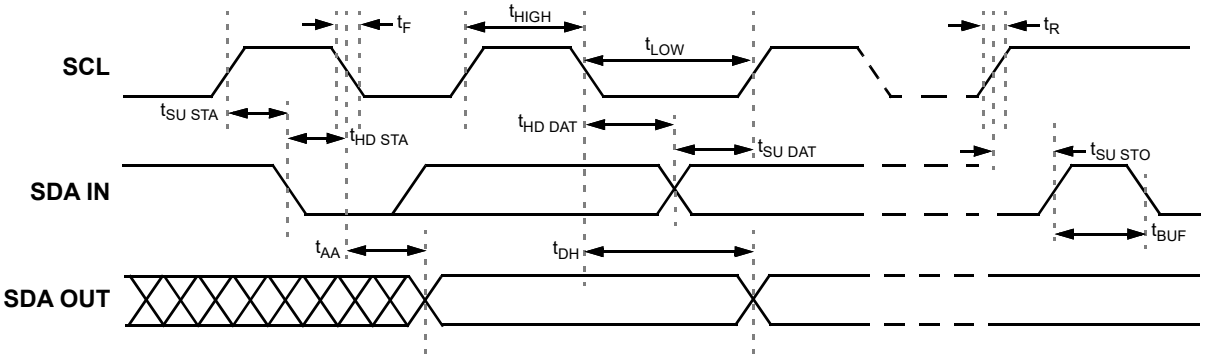


Figure 94: I²C General Timing Characteristics

17.4 I²C SERIAL COMMUNICATIONS COMMANDS

17.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46517 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46517, where the data byte is to be written. After the SLG46517 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46517 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46517 generates the Acknowledge bit.

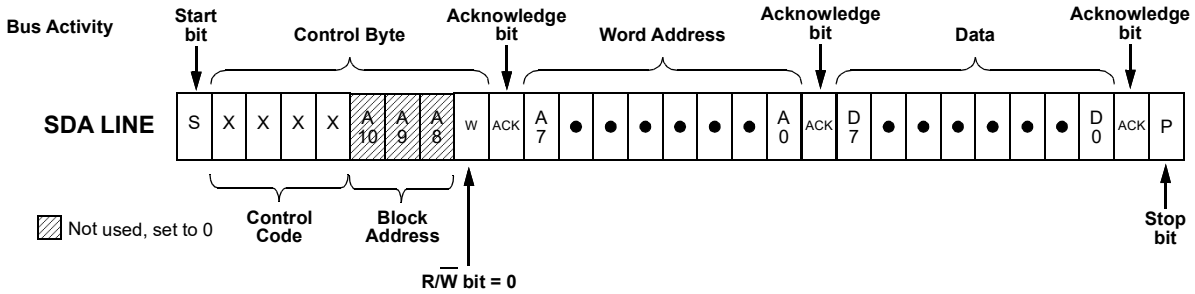


Figure 95: Byte Write Command, R/$\overline{W}$ = 0

17.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46517 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46517. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46517 generates the Acknowledge bit.

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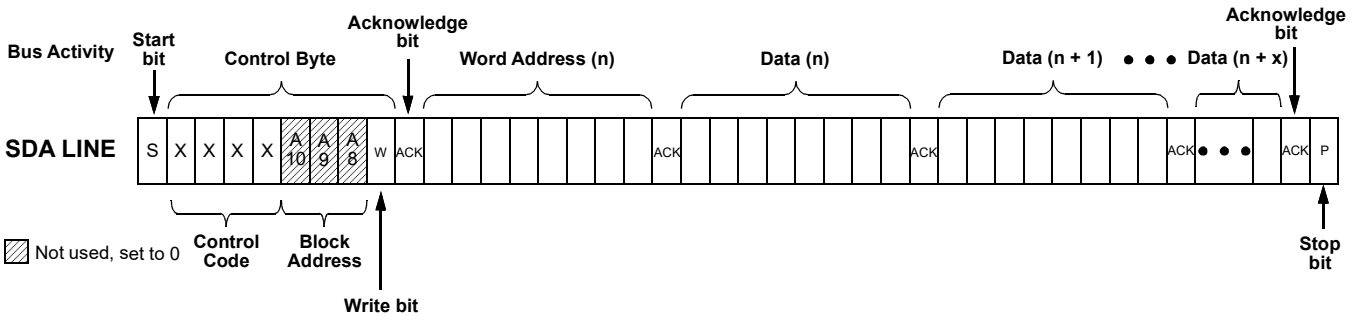


Figure 96: Sequential Write Command

17.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46517 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

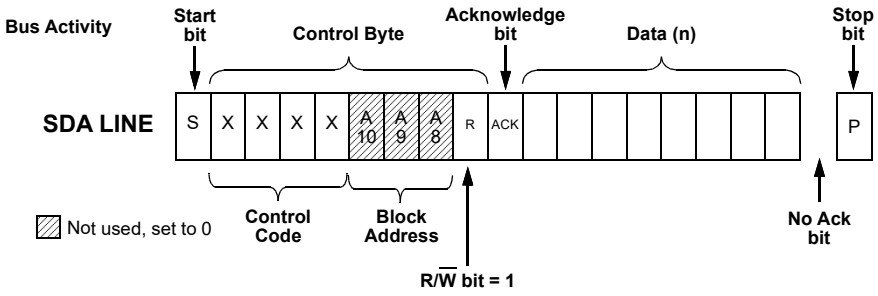


Figure 97: Current Address Read Command, R/$\overline{W}$ = 1

17.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46517 issues an Acknowledge bit, followed by the requested eight data bits.

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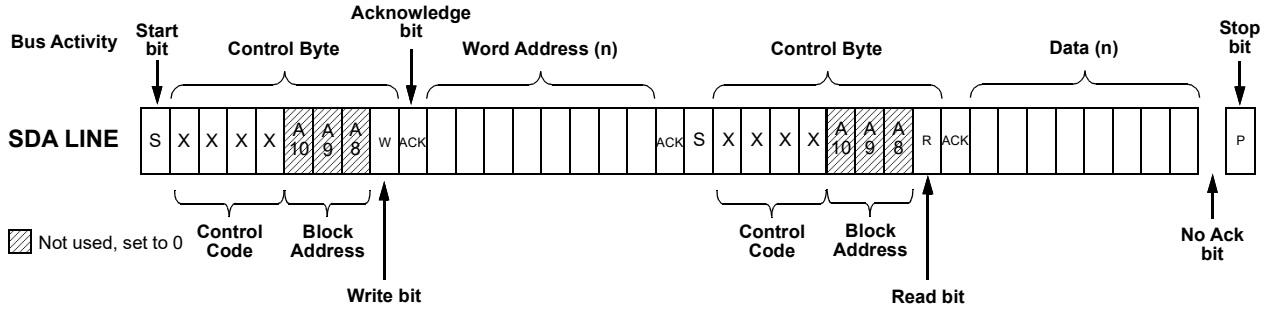


Figure 98: Random Read Command

17.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46517 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

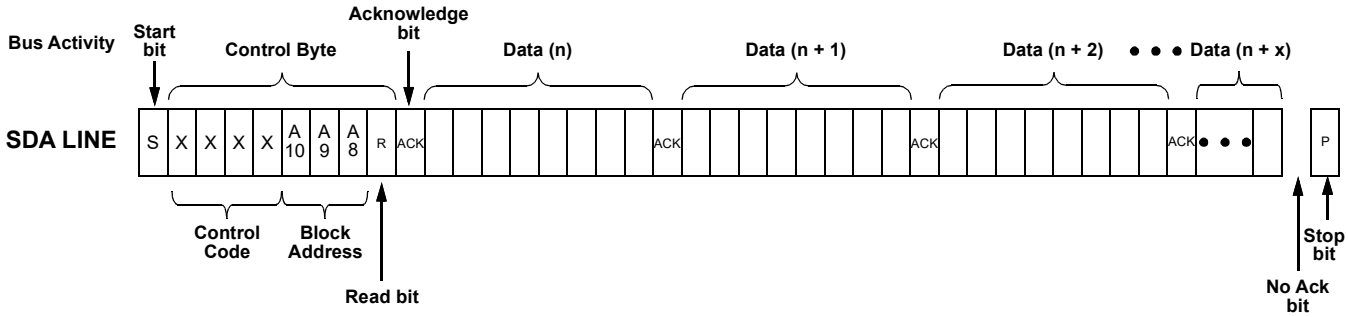


Figure 99: Sequential Read Command

17.4.6 I²C Serial Command Address Space

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46517 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46517.

17.4.7 I²C Serial Command Register Map

These register addresses are broken down into four Banks to give the user greater control on access to reading and writing information in each bank. Each of the four banks is 512 bits (64 bytes) in length. Writing information to register bits in these Banks will change the configuration of the device, resulting in either a change in the interconnection options provided by the Connection Matrix, or by changing the configuration of individual macrocells. During device use, all register bits can be read or written via I²C, unless protection bits are set to prevent this.

See Section 20 for detailed information on all register bits.

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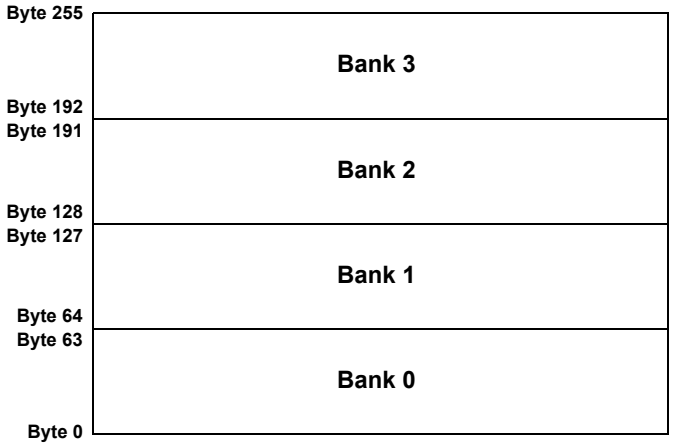


Figure 100: Register Bank Map

17.5 I²C SERIAL COMMAND REGISTER PROTECTION

The memory space is divided into four banks, each of which has 512bits (64bytes). There are three bits that allow the user to define rules for reading and writing bits in each of these banks via I²C:

- register [1832] I²C lock for read bits [1535:0] (Bank 0/1/2). If the system provides any read commands to the addresses in these three banks, the device will respond with 'FFH' in data field.
- register [1871] I²C lock for write bits [1535:0] (Bank 0/1/2). If the system provides any write commands to the addresses in these three banks, the device will acknowledge these commands, but will not do internal writes to the register space.
- register [1870] I²C lock for write all bits (Bank 0/1/2/3). If the system provides any write commands to the addresses in these four banks, the device will acknowledge these commands, but will not do internal writes to the register space.

Note: register [1870] is higher priority than register [1871], and if register [1870] is set, than register [1871] does not have any effect.

Note: If the user sets IOs 6 and 7 function to a selection other than SDA and SCL, all access via I²C will be disabled.

If register [1870] is not set, register bits in Bank 3 are open to read and write commands via I²C with the following exceptions:

- register [1871] Bank 0/1/2 I²C-write protection bit is always protected from I²C write
- registers [1867:1864] I²C Control Code Bit [3:0] is always protected from I²C write

Note: Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 20 for detailed information on all registers.

17.5.1 Register Read/Write Protection

There are six read/write protect modes for the design sequence from being corrupted or copied. See Table 95 for details.

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Table 95: Read/Write Protection Options

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits <1535:0>	Locked for write bits <1535:0>	Locked for write all bits	Locked for read and write bits <1535:0>	Locked for read bits <1535:0> and write all bits
				reg <1832>=0, <1871>=0, <1870>=0	reg <1832>=1, <1871>=0, <1870>=0	reg <1832>=0, <1871>=1, <1870>=0	reg <1832>=0, <1871>=x, <1870>=1	reg <1832>=1, <1871>=1, <1870>=0	reg <1832>=1, <1871>=x, <1870>=1
0	0-63	511-0	Connection Matrix Outputs Configuration	R/W	W	R	R	-	-
1	64-109	879-512		R/W	W	R	R	-	-
	110-127	880-1023	Reserved	-	-	-	-	-	-
2	128-186	1495-1024	Function Configuration for PINs, LUTs/DFFs, OSC, ASM and some configuration for DLYs, ACMP	R/W	W	R	R	-	-
	187-191	1535-1496	Reserved	-	-	-	-	-	-
3	192-206	1655-1536	CNT/DLY counter data and some LUTs truth table, ACMP Vref	R/W	R/W	R/W	R	R/W	R
	207	1662	I^2C reset bit with reloading NVM into Data register	R/W	R/W	R/W	R	R/W	R
		1661-1659, 1663	Reserved	R	R	R	R	R	R
		1658-1656	OSC Power Control	R/W	R/W	R/W	R	R/W	R

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Table 95: Read/Write Protection Options (Continued)

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits <1535:0>	Locked for write bits <1535:0>	Locked for write all bits	Locked for read and write bits <1535:0>	Locked for read bits <1535:0> and write all bits
				reg <1832>=0, <1871>=0, <1870>=0	reg <1832>=1, <1871>=0, <1870>=0	reg <1832>=0, <1871>=1, <1870>=0	reg <1832>=0, <1871>=x, <1870>=1	reg <1832>=1, <1871>=1, <1870>=0	reg <1832>=1, <1871>=x, <1870>=1
3	208-223	1791-1664	ASM output RAM and User configurable RAM / OTP	R/W	R/W	R/W	R	R/W	R
	224-227	1823-1792	Reserved	-	-	-	-	-	-
	228	1831-1824	Reserved	R/W	R/W	R/W	R	R/W	R
	229	1839-1836	Product Family ID	R	R	R	R	R	R
		1835-1834	Reserved	-	-	-	-	-	-
		1833	Reserved	R	R	R	R	R	R
		1832	I^2C Lock for read bits<1535:0>	R	R	R	R	R	R
	230	1847-1840	Pattern ID	R/W	R/W	R/W	R	R/W	R
	231	1855-1848	Reserved	R	R	R	R	R	R
	232	1863-1856	Reserved	R	R	R	R	R	R
	233	1871	I^2C Lock for write bits<1535:0>	R	R	R	R	R	R
		1870	I^2C Lock for write all bits	R	R	R	R	R	R
		1869-1868	Reserved	-	-	-	-	-	-
		1867-1864	I^2C Control Code	R	R	R	R	R	R
	234-239	1919-1872	Counter Current Value	R	R	R	R	R	R
	240-243	1951-1920	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	244	1959-1952	Connection Matrix Virtual Inputs	R/W	R/W	R/W	R	R/W	R
	245-247	1983-1960	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	248-250	2007-1984	Reserved	R	R	R	R	R	R

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Table 95: Read/Write Protection Options (Continued)

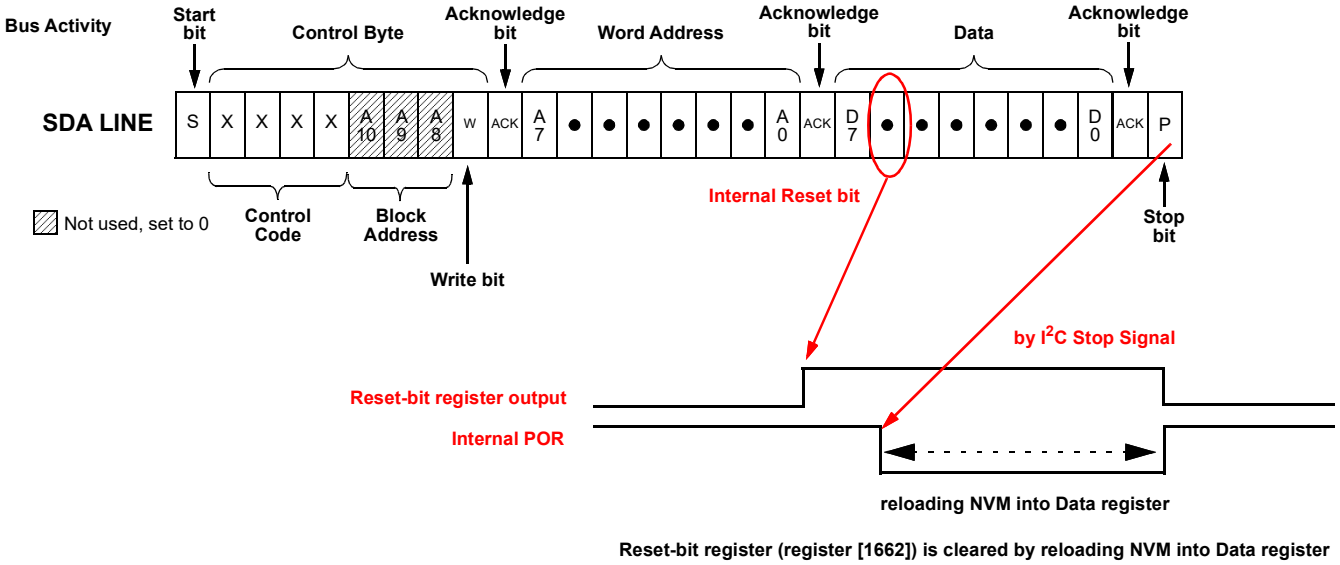
Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits <1535:0>	Locked for write bits <1535:0>	Locked for write all bits	Locked for read and write bits <1535:0>	Locked for read bits <1535:0> and write all bits
				reg <1832>=0, <1871>=0, <1870>=0	reg <1832>=1, <1871>=0, <1870>=0	reg <1832>=0, <1871>=1, <1870>=0	reg <1832>=0, <1871>=x, <1870>=1	reg <1832>=1, <1871>=1, <1870>=0	reg <1832>=1, <1871>=x, <1870>=1
3	251	2015-2008	Reserved	R/W	R/W	R/W	R	R/W	R
	252-253	2031-2016	Reserved	R	R	R	R	R	R
	254	2039-2032	Reserved	R/W	R/W	R/W	R	R/W	R
	255	2047-2040	Reserved	R/W	R/W	R/W	R	R/W	R

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

17.5.2 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1662] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1662] will be set to “0” automatically. The timing diagram shown below illustrates the sequence of events for this reset function.

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1) I²C write with register [1662] = 1 (I²C reset bit with reloading NVM into Data register)
2) POR go to LOW and reloading NVM into Data register start after "STOP" of I²C
3) POR go to HIGH after reloading NVM into Data register

Figure 101: Reset Command Timing

17.6 I²C ADDITIONAL OPTIONS

17.6.1 Reading Counter Data via I²C

The current count value in three counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

17.6.2 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

Table 96: RAM Array Table

I²C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
D8	1735	1728	User Configurable RAM/OTP Byte 0
D9	1743	1736	User Configurable RAM/OTP Byte 1
DA	1751	1744	User Configurable RAM/OTP Byte 2
DB	1759	1752	User Configurable RAM/OTP Byte 3
DC	1767	1760	User Configurable RAM/OTP Byte 4
DD	1775	1768	User Configurable RAM/OTP Byte 5
DE	1783	1776	User Configurable RAM/OTP Byte 6

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Table 96: RAM Array Table(Continued)

I^2C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
DF	1791	1784	User Configurable RAM/OTP Byte 7

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18 External Clocking

The SLG46517 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

18.1 CRYSTAL MODE

When register [1136] is set to 1, an external crystal can be connected to IOs 13 and 14 for supplying an accurate clock source. See Section 14. An external clocking signal on IO14 can be used in place of the crystal. The high and low limits for crystal frequency that can be selected are 32.768 kHz and 40 MHz.

18.2 IO17 OR IO15 SOURCE FOR 25 KHZ/2 MHZ CLOCK

When register [1358] is set to 1, an external clocking signal on IO15 will be routed in place of the internal RC oscillator derived 25 kHz/2 MHz clock source. See Figure 60. The high and low limits for external frequency that can be selected are 0 MHz and 77 MHz.

18.3 IO14 SOURCE FOR 25 MHZ CLOCK

When register [1357] is set to 1, an external clocking signal on IO14 will be routed in place of the internal RC oscillator derived 25 MHz clock source. See Figure 61. The high and low limits for external frequency that can be selected are 0 MHz and 84 MHz.

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19 Dual, 2A P-FET Power Switches

19.1 POWER SWITCHES OVERVIEW

The SLG46517 has a dual-channel, 44 mΩ PMOS power switch designed to switch 1.71 to 5.5 V power rails up to 2 A per channel.

Each P-FET Power Switch can be controlled internally via the ONx digital input of the P-FET Power Switch component in GreenPAK Designer, allowing the user to generate integrated Mixed-Signal control circuits, or externally via PWR_SW_ONx.

Whether controlled externally or internally, a low signal on either ONx or PWR_SW_ONx will close the P-FET Power Switch.

Each P-FET Power Switch need not be used in the same voltage domain as V_{DD}. However, when VIN is not tied to V_{DD}, using a large pull-up resistor on PWR_SW_ON0 and PWR_SW_ON1 is recommended to prevent current from flowing through the P-FET Power Switch while the device is not powered.

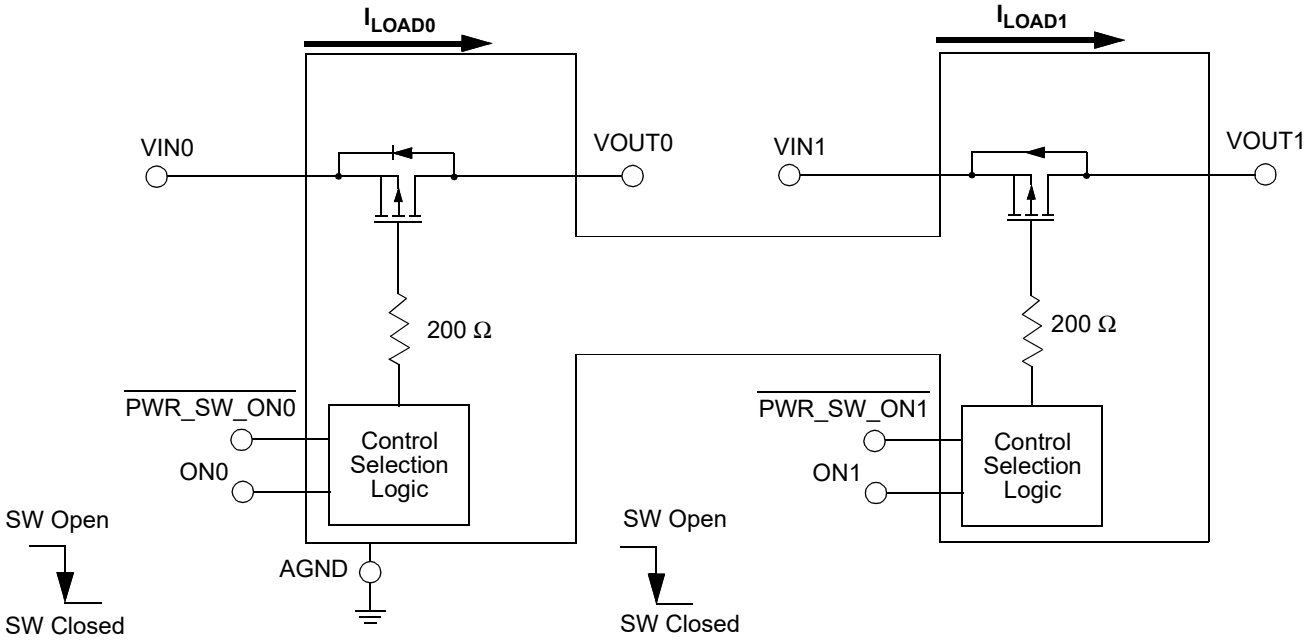


Figure 102: Dual P-FET Power Switch

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19.2 DRIVING THE P-FET SWITCH

Gate of P-FET power switch can be driven by either internally generated signal or directly by external source connected to corresponding PWR_SW_ONx pin. Simplified circuit topologies are illustrated on Figure 103.

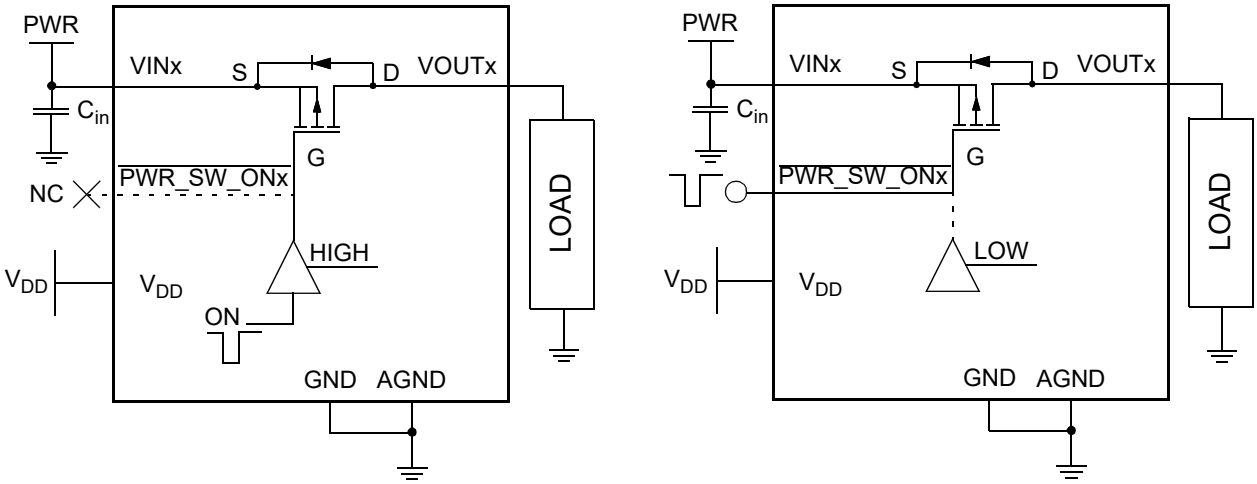


Figure 103: Typical Circuit Topology for Internal (Left) and External (Right) Drive Modes

Datasheet values for switching times are given for driving the resistive loads. The definitions of rise (t_r), fall (t_f), and delay times ($t_{d(on)}$ and $t_{d(off)}$) are given on Figure 104. To achieve highest switching performance circuit should be laid off using high speed PCB layout techniques.

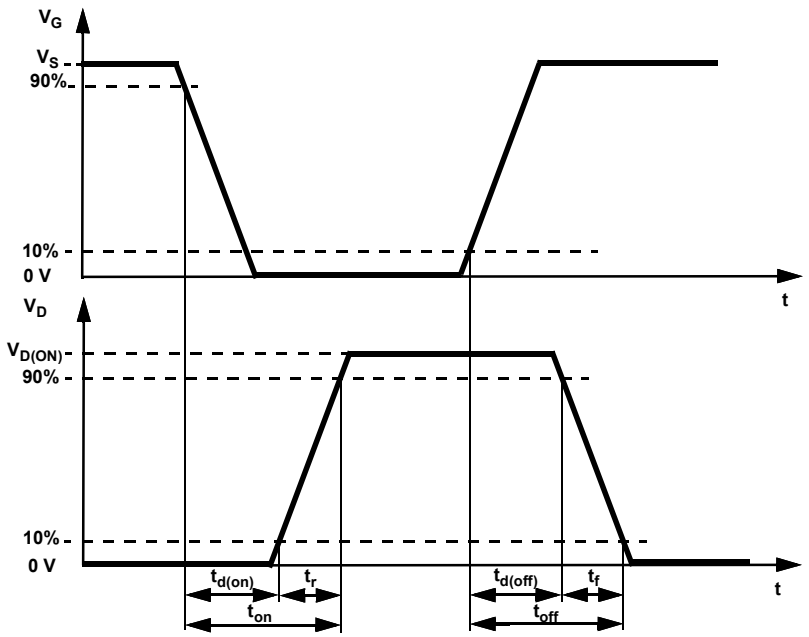


Figure 104: Definitions for Rise, Fall and Switching Delay Times

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Typical resistive switching waveforms are given on Figure 106 and Figure 107. Note that fall time is dependent on load current (see Section 19.4). At low loads turn off process can be delayed, therefore discharge circuit should be provided to reduce load turn off time in that case.

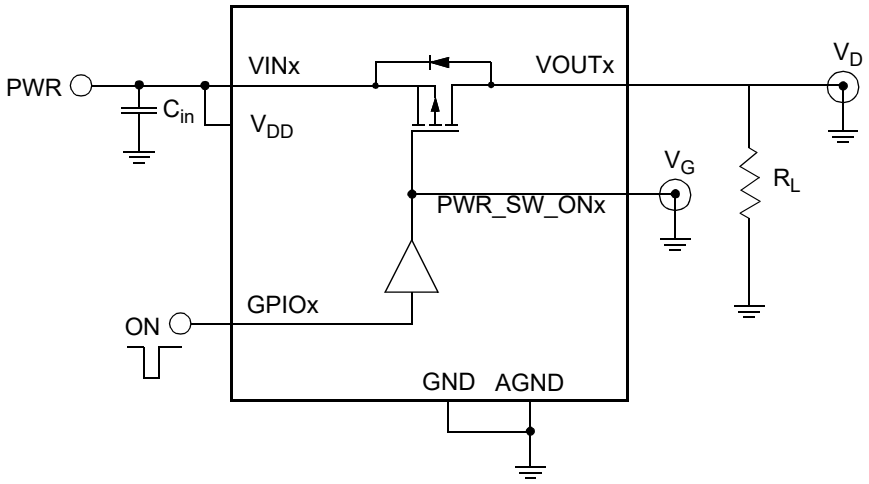


Figure 105: Test Circuit for Typical Switching Waveforms

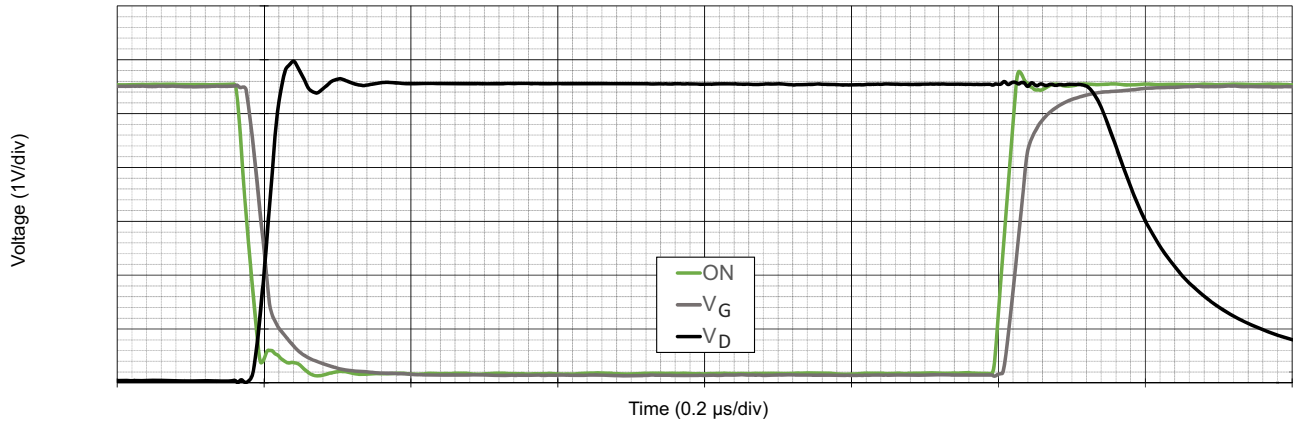


Figure 106: Typical Switching Waveforms (Internal Drive, Resistive Load, R_L = 100 Ω, V_{DD} = VIN = 5.5 V)

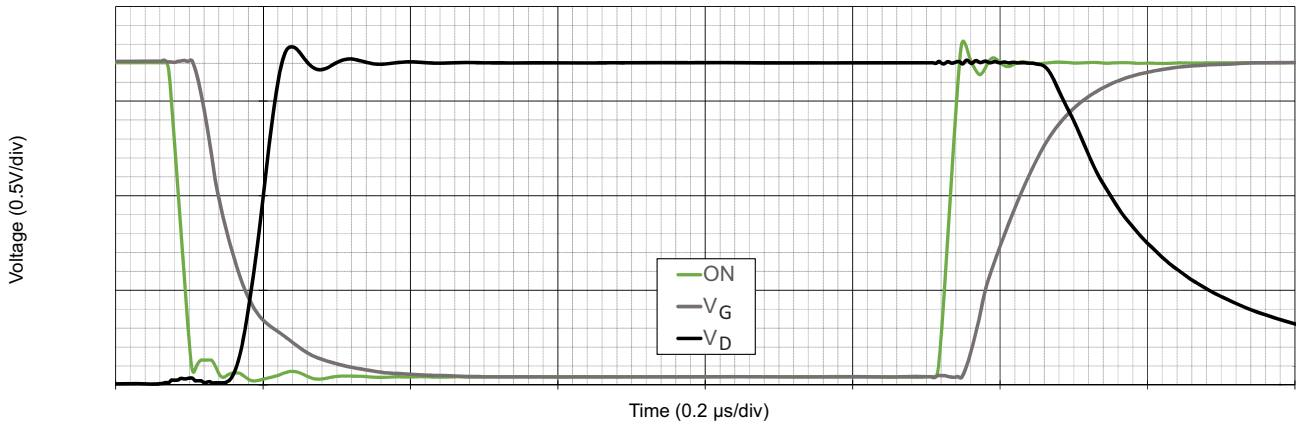


Figure 107: Typical Switching Waveforms (Internal Drive, Resistive Load, R_L = 100 Ω, V_{DD} = VIN = 1.71 V)

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19.3 POWER DISSIPATION

The junction temperature of the Power Switch depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the Power Switch is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON0} \times I_{OUT0}^2) + (RDS_{ON1} \times I_{OUT1}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON} = Channel 0 and Channel 1 Power MOSFET ON resistance, in Ohms (Ω), respectively

I_{OUT} = Channel 0 and Channel 1 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \Theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

Θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the Power Switch power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{INx}-V_{OUTx}) and the magnitude of that channel's output current (I_{OUTx}):

$$PD_{TOTAL} = [(V_{IN0}\text{-}V_{OUT0}) \times I_{OUT0}] + [(V_{IN1}\text{-}V_{OUT1}) \times I_{OUT1}] \text{ or}$$

$$PD_{TOTAL} = [(V_{IN0} - (R_{LOAD0} \times I_{OUT0})) \times I_{OUT0}] + [(V_{IN1} - (R_{LOAD1} \times I_{OU1})) \times I_{OUT1}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

V_{IN} = Channel 0 and Channel 1 Input Voltage, in Volts (V), respectively

R_{LOAD} = Channel 0 and Channel 1 Output Load Resistance, in Ohms (Ω), respectively

I_{OUT} = Channel 0 and Channel 1 output current, in Amps (A), respectively

V_{OUT} = Channel 0 and Channel 1 output voltage, or $R_{LOAD} \times I_{OUT}$, respectively

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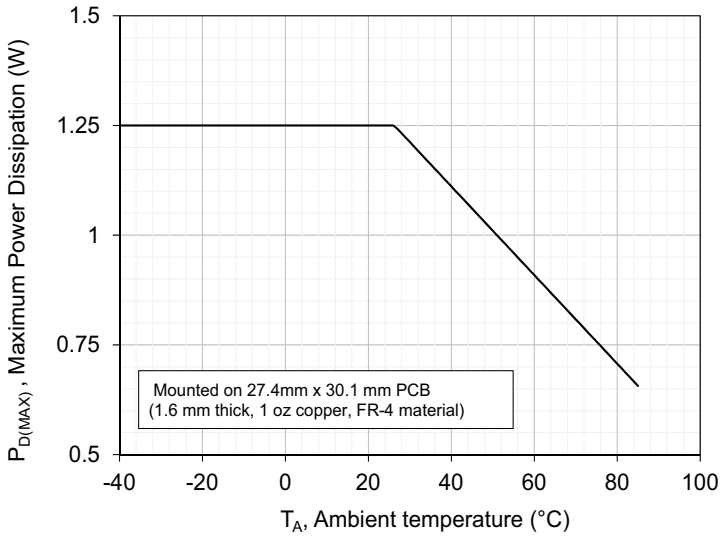


Figure 108: Power Dissipation Derating Curve

19.4 POWER SWITCH TYPICAL PERFORMANCE

T_A = 25 °C, V_{DD} = 5.5 V, unless otherwise noted.

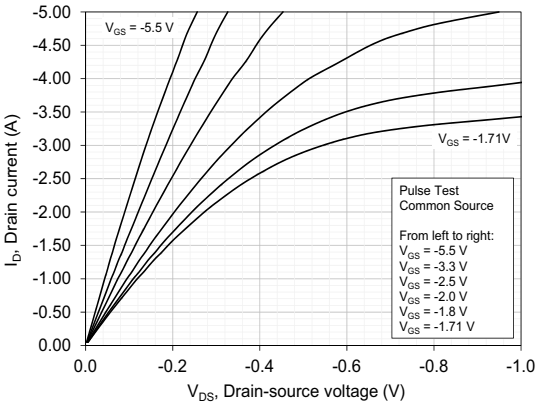


Figure 109: Typical Output Characteristics

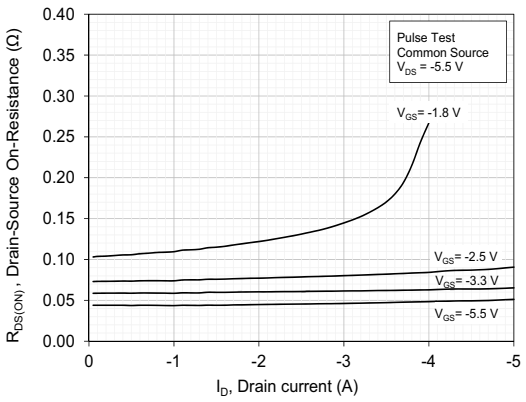


Figure 110: Drain-Source On-Resistance vs. Drain Current

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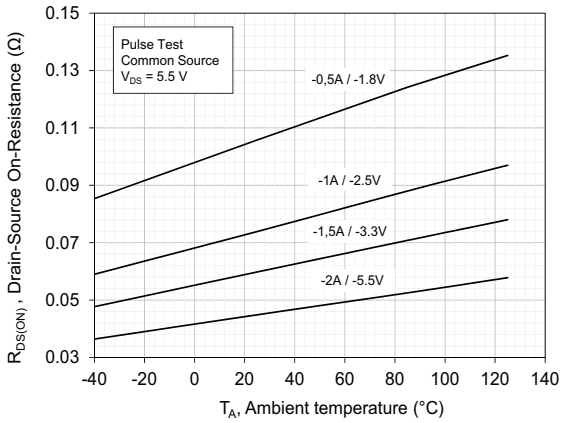


Figure 111: Typical Drain-Source On-Resistance vs. Ambient Temperature

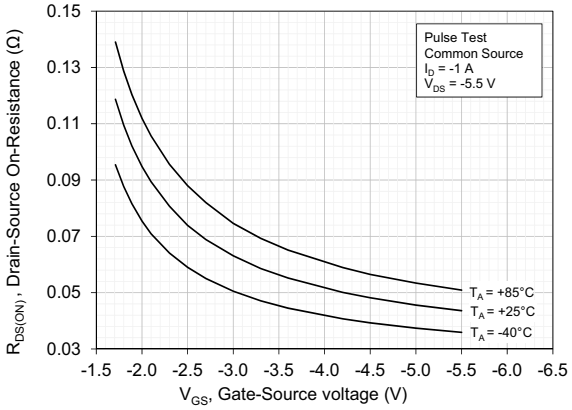


Figure 112: Gate-Source On-Resistance Gate-Source Voltage

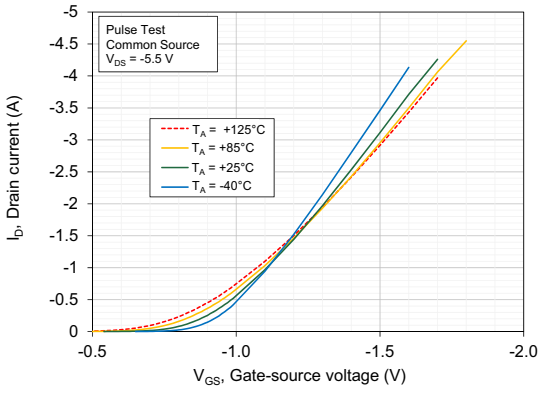


Figure 113: Drain Current vs. Gate-Source Voltage

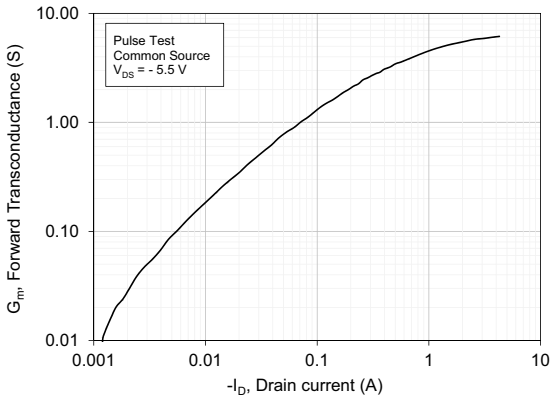


Figure 114: Typical Forward Transconductance

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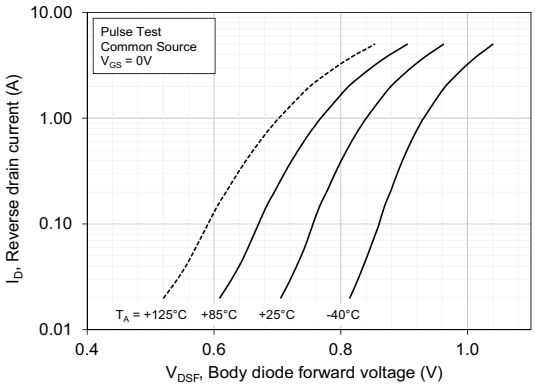


Figure 115: Typical Drain-Source Diode Forward Voltage

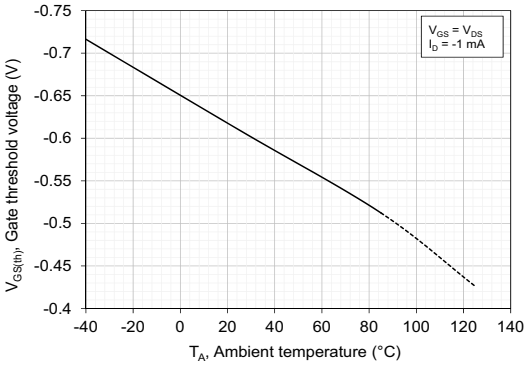


Figure 116: Gate Threshold Voltage vs Ambient Temperature

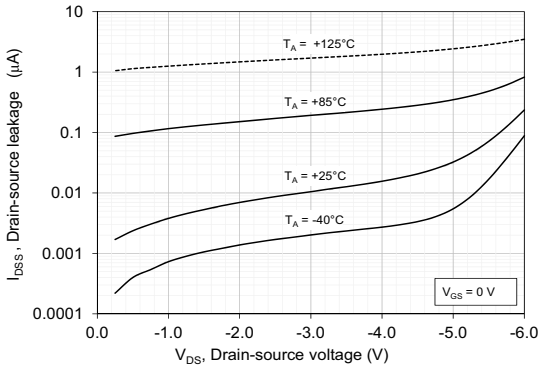


Figure 117: Zero Gate Voltage Drain Current

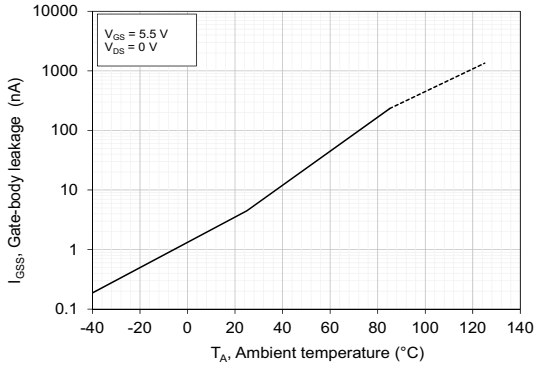


Figure 118: Gate-Body Leakage vs. Ambient Temperature

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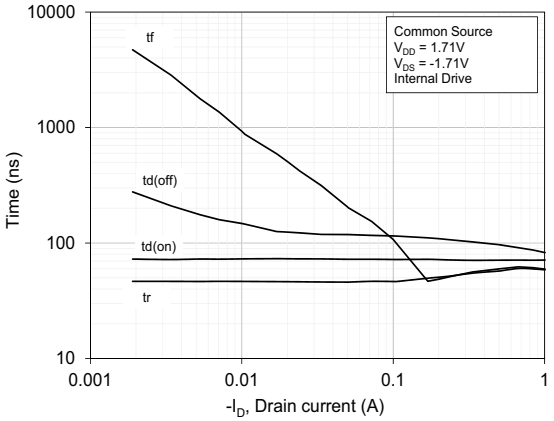


Figure 119: Typical Switching Time (Internal Gate Drive) at V_{DS} = 1.71 V

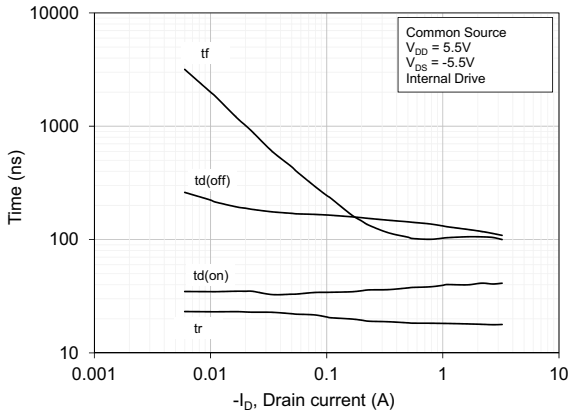


Figure 120: Typical Switching Time (Internal Gate Drive) at V_{DS} = 5.5 V

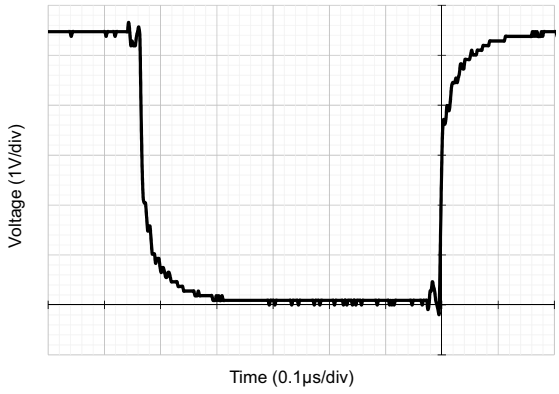


Figure 121: Typical Gate Input Waveform, Internal Gate Drive Source (Switching Time Test)

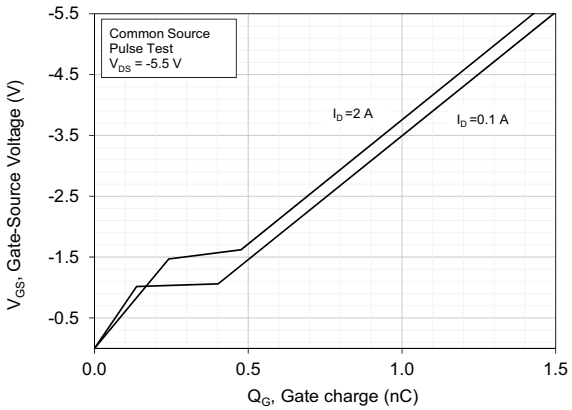


Figure 122: Typical Gate Charge vs. Gate-Source Voltage

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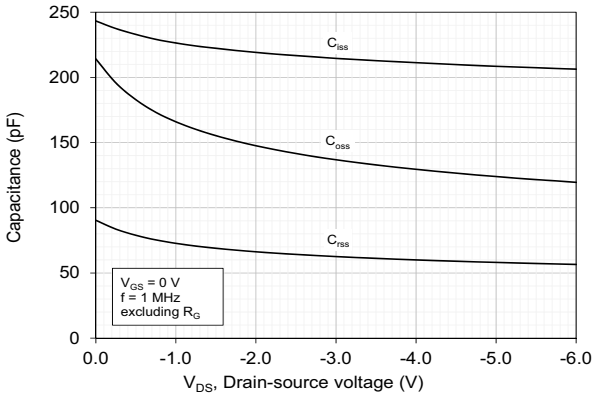


Figure 123: Typical Capacitance vs. Drain-Source Voltage

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20 Register Definitions

20.1 REGISTER MAP

Table 97: Register Map

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Note: For register [0] to register [1495], I²C Read is valid (assuming register [1832] = 0), I²C Write is valid (assuming register [1871] = 0)					
Matrix 64-to-1 MUX's 6 selection bits					
00	5:0	Matrix OUT	ASM-state0-EN0	Valid	Valid
	7:6	Reserved		Valid	Valid
01	13:8	Matrix OUT	ASM-state0-EN1	Valid	Valid
	15:14	Reserved		Valid	Valid
02	21:16	Matrix OUT	ASM-state0-EN2	Valid	Valid
	23:22	Reserved		Valid	Valid
03	29:24	Matrix OUT	ASM-state1-EN0	Valid	Valid
	31:30	Reserved		Valid	Valid
04	37:32	Matrix OUT	ASM-state1-EN1	Valid	Valid
	39:38	Reserved		Valid	Valid
05	45:40	Matrix OUT	ASM-state1-EN2	Valid	Valid
	47:46	Reserved		Valid	Valid
06	53:48	Matrix OUT	ASM-state2-EN0	Valid	Valid
	55:54	Reserved		Valid	Valid
07	61:56	Matrix OUT	ASM-state2-EN1	Valid	Valid
	63:62	Reserved		Valid	Valid
08	69:64	Matrix OUT	ASM-state2-EN2	Valid	Valid
	71:70	Reserved		Valid	Valid
09	77:72	Matrix OUT	ASM-state3-EN0	Valid	Valid
	79:78	Reserved		Valid	Valid
0A	85:80	Matrix OUT	ASM-state3-EN1	Valid	Valid
	87:86	Reserved		Valid	Valid
0B	93:88	Matrix OUT	ASM-state3-EN2	Valid	Valid
	95:94	Reserved		Valid	Valid
0C	101:96	Matrix OUT	ASM-state4-EN0	Valid	Valid
	103:102	Reserved		Valid	Valid
0D	109:104	Matrix OUT	ASM-state4-EN1	Valid	Valid
	111:110	Reserved		Valid	Valid
0E	117:112	Matrix OUT	ASM-state4-EN2	Valid	Valid
	119:118	Reserved		Valid	Valid
0F	125:120	Matrix OUT	ASM-state5-EN0	Valid	Valid
	127:126	Reserved		Valid	Valid
10	133:128	Matrix OUT	ASM-state5-EN1	Valid	Valid
	135:134	Reserved		Valid	Valid
11	141:136	Matrix OUT	ASM-state5-EN2	Valid	Valid
	143:142	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
12	149:144	Matrix OUT	ASM-state6-EN0	Valid	Valid
	151:150	Reserved		Valid	Valid
13	157:152	Matrix OUT	ASM-state6-EN1	Valid	Valid
	159:158	Reserved		Valid	Valid
14	165:160	Matrix OUT	ASM-state6-EN2	Valid	Valid
	167:166	Reserved		Valid	Valid
15	173:168	Matrix OUT	ASM-state7-EN0	Valid	Valid
	175:174	Reserved		Valid	Valid
16	181:176	Matrix OUT	ASM-state7-EN1	Valid	Valid
	183:182	Reserved		Valid	Valid
17	189:184	Matrix OUT	ASM-state7-EN2	Valid	Valid
	191:190	Reserved		Valid	Valid
18	197:192	Matrix OUT	ASM-state-nRST	Valid	Valid
	199:198	Reserved		Valid	Valid
19	205:200	Matrix OUT	IO1 Digital Output Source	Valid	Valid
	207:206	Reserved		Valid	Valid
1A	213:208	Matrix OUT	IO1 Output Enable	Valid	Valid
	215:214	Reserved		Valid	Valid
1B	221:216	Matrix OUT	IO2 Digital Output Source	Valid	Valid
	223:222	Reserved		Valid	Valid
1C	229:224	Matrix OUT	IO3 Digital Output Source	Valid	Valid
	231:230	Reserved		Valid	Valid
1D	237:232	Matrix OUT	IO3 Output Enable	Valid	Valid
	239:238	Reserved		Valid	Valid
1E	245:240	Matrix OUT	IO4 Digital Output Source	Valid	Valid
	247:246	Reserved		Valid	Valid
1F	253:248	Matrix OUT	IO5 Digital Output Source	Valid	Valid
	255:254	Reserved		Valid	Valid
20	261:256	Matrix OUT	IO5 Output Enable	Valid	Valid
	263:262	Reserved		Valid	Valid
21	269:264	Matrix OUT	IO6 Digital Output Source (SCL with VI/Input & NMOS Open-Drain)	Valid	Valid
	271:270	Reserved		Valid	Valid
22	277:272	Matrix OUT	IO7 Digital Output Source (SDA with VI/Input & NMOS Open-Drain)	Valid	Valid
	279:278	Reserved		Valid	Valid
23	285:280	Matrix OUT	IO8 Digital Output Source	Valid	Valid
	287:286	Reserved		Valid	Valid
24	293:288	Matrix OUT	IO8 Output Enable	Valid	Valid
	295:294	Reserved		Valid	Valid
25	301:296	Matrix OUT	IO9 Digital Output Source	Valid	Valid
	303:302	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
26	309:304	Matrix OUT	IO10 Digital Output Source	Valid	Valid
	311:310	Reserved		Valid	Valid
27	317:312	Matrix OUT	IO10 Output Enable	Valid	Valid
	319:318	Reserved		Valid	Valid
28	325:320	Matrix OUT	IO11 Digital Output Source	Valid	Valid
	327:326	Reserved		Valid	Valid
29	333:328	Matrix OUT	IO11 Output Enable	Valid	Valid
	335:334	Reserved		Valid	Valid
2A	341:336	Matrix OUT	IO12 Digital Output Source	Valid	Valid
	343:342	Reserved		Valid	Valid
2B	349:344	Matrix OUT	IO13 Digital Output Source	Valid	Valid
	351:350	Reserved		Valid	Valid
2C	357:352	Matrix OUT	IO13 Output Enable	Valid	Valid
	359:358	Reserved		Valid	Valid
2D	365:360	Matrix OUT	IO14 Digital Output Source	Valid	Valid
	367:366	Reserved		Valid	Valid
2E	373:368	Matrix OUT	IO15 Digital Output Source	Valid	Valid
	375:374	Reserved		Valid	Valid
2F	381:376	Matrix OUT	IO15 Output Enable	Valid	Valid
	383:382	Reserved		Valid	Valid
30	389:384	Matrix OUT	Power Switch ON0, Digital Output Source	Valid	Valid
	391:390	Reserved		Valid	Valid
31	397:392	Matrix OUT	Reserved	Valid	Valid
	399:398	Reserved		Valid	Valid
32	405:400	Matrix OUT	Power Switch ON1, Digital Output Source	Valid	Valid
	407:406	Reserved		Valid	Valid
33	413:408	Matrix OUT	ACMP0 PWR UP	Valid	Valid
	415:414	Reserved		Valid	Valid
34	421:416	Matrix OUT	ACMP1 PWR UP	Valid	Valid
	423:422	Reserved		Valid	Valid
35	429:424	Matrix OUT	ACMP2 PWR UP	Valid	Valid
	431:430	Reserved		Valid	Valid
36	437:432	Matrix OUT	ACMP3 PWR UP	Valid	Valid
	439:438	Reserved		Valid	Valid
37	445:440	Matrix OUT	Input of Filter_0 with fixed time edge detector	Valid	Valid
	447:446	Reserved		Valid	Valid
38	453:448	Matrix OUT	Input of Filter_1 with fixed time edge detector	Valid	Valid
	455:454	Reserved		Valid	Valid
39	461:456	Matrix OUT	Input of Programmable Delay & Edge Detector	Valid	Valid
	463:462	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
3A	469:464	Matrix OUT	OSC 25 kHz/2MHz PDB (Power-Down)	Valid	Valid
	471:470	Reserved		Valid	Valid
3B	477:472	Matrix OUT	OSC 25 MHz PDB (Power-Down)	Valid	Valid
	479:478	Reserved		Valid	Valid
3C	485:480	Matrix OUT	IN0 of LUT2_0 or Clock Input of DFF0	Valid	Valid
	487:486	Reserved		Valid	Valid
3D	493:488	Matrix OUT	IN1 of LUT2_0 or Data Input of DFF0	Valid	Valid
	495:494	Reserved		Valid	Valid
3E	501:496	Matrix OUT	IN0 of LUT2_1 or Clock Input of DFF1	Valid	Valid
	503:502	Reserved		Valid	Valid
3F	509:504	Matrix OUT	IN1 of LUT2_1 or Data Input of DFF1	Valid	Valid
	511:510	Reserved		Valid	Valid
40	517:512	Matrix OUT	IN0 of LUT2_2 or Clock Input of DFF2	Valid	Valid
	519:518	Reserved		Valid	Valid
41	525:520	Matrix OUT	IN1 of LUT2_2 or Data Input of DFF2	Valid	Valid
	527:526	Reserved		Valid	Valid
42	533:528	Matrix OUT	IN0 of LUT2_3 or Clock Input of PGen	Valid	Valid
	535:534	Reserved		Valid	Valid
43	541:536	Matrix OUT	IN1 of LUT2_3 or nRST of PGen	Valid	Valid
	543:542	Reserved		Valid	Valid
44	549:544	Matrix OUT	IN0 of LUT3_0 or Clock Input of DFF3	Valid	Valid
	551:550	Reserved		Valid	Valid
45	557:552	Matrix OUT	IN1 of LUT3_0 or Data Input of DFF3	Valid	Valid
	559:558	Reserved		Valid	Valid
46	565:560	Matrix OUT	IN2 of LUT3_0 or nRST (nSET) of DFF3	Valid	Valid
	567:566	Reserved		Valid	Valid
47	573:568	Matrix OUT	IN0 of LUT3_1 or Clock Input of DFF4	Valid	Valid
	575:574	Reserved		Valid	Valid
48	581:576	Matrix OUT	IN1 of LUT3_1 or Data Input of DFF4	Valid	Valid
	583:582	Reserved		Valid	Valid
49	589:584	Matrix OUT	IN2 of LUT3_1 or nRST (nSET) of DFF4	Valid	Valid
	591:590	Reserved		Valid	Valid
4A	597:592	Matrix OUT	IN0 of LUT3_2 or Clock Input of DFF5	Valid	Valid
	599:598	Reserved		Valid	Valid
4B	605:600	Matrix OUT	IN1 of LUT3_2 or Data Input of DFF5	Valid	Valid
	607:606	Reserved		Valid	Valid
4C	613:608	Matrix OUT	IN2 of LUT3_2 or nRST (nSET) of DFF5	Valid	Valid
	615:614	Reserved		Valid	Valid
4D	621:616	Matrix OUT	IN0 of LUT3_3 or Clock Input of DFF6	Valid	Valid
	623:622	Reserved		Valid	Valid
4E	629:624	Matrix OUT	IN1 of LUT3_3 or Data Input of DFF6	Valid	Valid
	631:630	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
4F	637:632	Matrix OUT	IN2 of LUT3_3 or nRST (nSET) of DFF6	Valid	Valid
	639:638	Reserved		Valid	Valid
50	645:640	Matrix OUT	IN0 of LUT3_4 or Clock Input of DFF7	Valid	Valid
	647:646	Reserved		Valid	Valid
51	653:648	Matrix OUT	IN1 of LUT3_4 or Data Input of DFF7	Valid	Valid
	655:654	Reserved		Valid	Valid
52	661:656	Matrix OUT	IN2 of LUT3_4 or nRST (nSET) of DFF7	Valid	Valid
	663:662	Reserved		Valid	Valid
53	669:664	Matrix OUT	IN0 of LUT3_5 or Delay2 Input (or Counter2 RST Input)	Valid	Valid
	671:670	Reserved		Valid	Valid
54	677:672	Matrix OUT	IN1 of LUT3_5 or External Clock Input of Delay2 (or Counter2)	Valid	Valid
	679:678	Reserved		Valid	Valid
55	685:680	Matrix OUT	IN2 of LUT3_5	Valid	Valid
	687:686	Reserved		Valid	Valid
56	693:688	Matrix OUT	IN0 of LUT3_6 or Delay3 Input (or Counter3 RST Input)	Valid	Valid
	695:694	Reserved		Valid	Valid
57	701:696	Matrix OUT	IN1 of LUT3_6 or External Clock Input of Delay3 (or Counter3)	Valid	Valid
	703:702	Reserved		Valid	Valid
58	709:704	Matrix OUT	IN2 of LUT3_6	Valid	Valid
	711:710	Reserved		Valid	Valid
59	717:712	Matrix OUT	IN0 of LUT3_7 or Delay4 Input (or Counter4 RST Input)	Valid	Valid
	719:718	Reserved		Valid	Valid
5A	725:720	Matrix OUT	IN1 of LUT3_7 or External Clock Input of Delay4 (or Counter4)	Valid	Valid
	727:726	Reserved		Valid	Valid
5B	733:728	Matrix OUT	IN2 of LUT3_7	Valid	Valid
	735:734	Reserved		Valid	Valid
5C	741:736	Matrix OUT	IN0 of LUT3_8 or Delay5 Input (or Counter5 RST Input)	Valid	Valid
	743:742	Reserved		Valid	Valid
5D	749:744	Matrix OUT	IN1 of LUT3_8 or External Clock Input of Delay5 (or Counter5)	Valid	Valid
	751:750	Reserved		Valid	Valid
5E	757:752	Matrix OUT	IN2 of LUT3_8	Valid	Valid
	759:758	Reserved		Valid	Valid
5F	765:760	Matrix OUT	IN0 of LUT3_9 or Delay6 Input (or Counter6 RST Input)	Valid	Valid
	767:766	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
60	773:768	Matrix OUT	IN1 of LUT3_9 or External Clock Input of Delay6 (or Counter6)	Valid	Valid
	775:774	Reserved		Valid	Valid
61	781:776	Matrix OUT	IN2 of LUT3_9	Valid	Valid
	783:782	Reserved		Valid	Valid
62	789:784	Matrix OUT	IN0 of LUT3_10 or Input of Pipe Delay	Valid	Valid
	791:790	Reserved		Valid	Valid
63	797:792	Matrix OUT	IN1 of LUT3_10 or nRST of Pipe Delay	Valid	Valid
	799:798	Reserved		Valid	Valid
64	805:800	Matrix OUT	IN2 of LUT3_10 or Clock of Pipe Delay	Valid	Valid
	807:806	Reserved		Valid	Valid
65	813:808	Matrix OUT	IN0 of LUT4_0 or Delay0 Input (or Counter0 RST/SET Input)	Valid	Valid
	815:814	Reserved		Valid	Valid
66	821:816	Matrix OUT	IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0)	Valid	Valid
	823:822	Reserved		Valid	Valid
67	829:824	Matrix OUT	IN2 of LUT4_0 or UP Input of FSM0	Valid	Valid
	831:830	Reserved		Valid	Valid
68	837:832	Matrix OUT	IN3 of LUT4_0 or KEEP Input of FSM0	Valid	Valid
	839:838	Reserved		Valid	Valid
69	845:840	Matrix OUT	IN0 of LUT4_1 or Delay1 Input (or Counter1 RST/SET Input)	Valid	Valid
	847:846	Reserved		Valid	Valid
6A	853:848	Matrix OUT	IN1 of LUT4_1 or External Clock Input of Delay1 (or Counter1)	Valid	Valid
	855:854	Reserved		Valid	Valid
6B	861:856	Matrix OUT	IN2 of LUT4_1 or UP Input of FSM1	Valid	Valid
	863:862	Reserved		Valid	Valid
6C	869:864	Matrix OUT	IN3 of LUT4_1 or KEEP Input of FSM1	Valid	Valid
	871:870	Reserved		Valid	Valid
6D	877:872	Matrix OUT	PD of either Temp-output with BG AND/OR crystal oscillator by register [1268]	Valid	Valid
	879:878	Reserved		Valid	Valid
6E	887:880	Reserved		Valid	Valid
6F	895:888	Reserved		Valid	Valid
70	903:896	Reserved		Valid	Valid
71	911:904	Reserved		Valid	Valid
72	919:912	Reserved		Valid	Valid
73	927:920	Reserved		Valid	Valid
74	935:928	Reserved		Valid	Valid
75	943:936	Reserved		Valid	Valid
76	951:944	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
77	959:952	Reserved		Valid	Valid
78	967:960	Reserved		Valid	Valid
79	975:968	Reserved		Valid	Valid
7A	983:976	Reserved		Valid	Valid
7B	991:984	Reserved		Valid	Valid
7C	999:992	Reserved		Valid	Valid
7D	1007:1000	Reserved		Valid	Valid
7E	1015:1008	Reserved		Valid	Valid
7F	1023:1016	Reserved		Valid	Valid
IO0					
80	1024	Reserved		Valid	Valid
	1025	Reserved		Valid	Valid
	1027:1026	Reserved		Valid	Valid
	1029:1028	IO0 Pull-down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1031:1030	IO0 Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
IO1					
80	1032	Reserved		Valid	Valid
81	1033	IO1 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1035:1034	IO1 Pull-up/down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1037:1036	IO1 Mode Control (sig_io1_oe = 0)	00: Digital Input without Schmitt Trigger, 01: Digital Input with Schmitt Trigger, 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
	1039:1038	IO1 Mode Control (sig_io1_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
IO2					
82	1040	Reserved		Valid	Valid
	1041	IO2 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1042	IO2 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1044:1043	IO2 Pull-up/down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1047:1045	IO2 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved	Valid	Valid
IO3					
83	1048	Reserved		Valid	Valid
	1049	IO3 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1051:1050	IO3 Pull-up/down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1053:1052	IO3 Mode Control (sig_io3_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
	1055:1054	IO3 Mode Control (sig_io3_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO4					
84	1056	Reserved		Valid	Valid
	1057	IO4 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1058	IO4 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1060:1059	IO4 Pull-up/down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1063:1061	IO4 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
IO5					
85	1064	Reserved		Valid	Valid
	1065	IO5 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1067:1066	IO5 Pull-up/down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1069:1068	IO5 Mode Control (sig_io5_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1071:1070	IO5 Mode Control (sig_io5_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO6					
86	1072	Reserved		Valid	Valid
	1073	IO6 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1074	Select SCL & Virtual Input 0 or IO6	0: SCL & Virtual Input 0 1: IO6	Valid	Valid
	1076:1075	IO6 Pull-down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1079:1077	IO6 (or SCL) Mode Control (input mode is selected by register at SCL)	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved	Valid	Valid
IO7					
87	1080	Reserved		Valid	Valid
	1081	IO7 (or SDA) Driver Strength Selection	0: 1x (I²C up to 400 kHz) 1: 2x (I²C up to 1 MHz)	Valid	Valid
	1082	Select SDA & Virtual Input 1 or IO7	0: SDA & Virtual Input 1 1: IO7	Valid	Valid
	1084:1083	IO7 Pull-down Resistor Value Selection	00: Floating 01: 10 K 10: 100 K 11: 1 M	Valid	Valid
	1087:1085	IO7 (or SDA) Mode Control (input mode is selected by register at SDA, output mode is fixed as OD at SDA)	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Re served 100: Reserved 101: Open-Drain NMOS 110: Reserved 111: Reserved	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
IO8					
88	1088	IO8 Super Drive (4x, NMOS Open-Drain) Selection	0: Super Drive OFF 1: Super Drive ON (if sig_IO8_oe = '1' & IO8 Mode Control = '1x')	Valid	Valid
	1089	IO8 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1091:1090	IO8 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1093:1092	IO8 Mode Control (sig_io8_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1095:1094	IO8 Mode Control (sig_io8_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO9					
89	1096	IO9 Super Drive (4x, NMOS Open-Drain) Selection	0: Super Drive OFF 1: Super Drive ON (if IO9 Mode Control = '101')	Valid	Valid
	1097	IO9 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1098	IO9 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1100:1099	IO9 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1103:1101	IO9 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
IO10					
8A	1104	Reserved		Valid	Valid
	1105	IO10 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1107:1106	IO10 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1109:1108	IO10 Mode Control (sig_io10_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1111:1110	IO10 Mode Control (sig_io10_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO11					
8B	1112	Reserved		Valid	Valid
	1113	IO11 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1115:1114	IO11 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1117:1116	IO11 Mode Control (sig_IO11_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1119:1118	IO11 Mode Control (sig_IO11_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO12					
8C	1120	Reserved		Valid	Valid
	1121	IO12 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1122	IO12 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1124:1123	IO12 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1127:1125	IO12 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Analog Input & Open-Drain	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
IO13					
8D	1128	Reserved		Valid	Valid
	1129	IO13 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1131:1130	IO13 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1133:1132	IO13 Mode Control (sig_io13_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Sel for XOSC (X2)	Valid	Valid
	1135:1134	IO13 Mode Control (sig_io13_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid
IO14					
8E	1136	X1 & X2 for crystal OSC enable	0: Disable 1: Enable	Valid	Valid
	1137	IO14 Driver Strength Selection	0: 1x 1: 2x	Valid	Valid
	1138	IO14 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1140:1139	IO14 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1143:1141	IO14 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Sel for XOSC (X1) 100: Push-Pull 101: Open-Drain NMOS 110: Open-Drain PMOS 111: Reserved	Valid	Valid
IO15					
8F	1144	Reserved		Valid	Valid
	1145	IO15 Pull-up/down Resistor Selection	0: Pull-down Resistor 1: Pull-up Resistor	Valid	Valid
	1147:1146	IO15 Pull-up/down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
	1149:1148	IO15 Mode Control (sig_io15_oe = 0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
	1151:1150	IO15 Mode Control (sig_io15_oe = 1)	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain NMOS 1x 11: Open-Drain NMOS 2x	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
PWR_SW_ON0					
90	1152	Reserved		Valid	Valid
	1153	PWR_SW_ON0 Pull-up/down Resistor Selection	0: Reserved 1: Reserved	Valid	Valid
	1155:1154	PWR_SW_ON0 Pull-up/down Resistor Value Selection	00: Reserved 01: Reserved 10: Reserved 11: Reserved	Valid	Valid
	1157:1156	PWR_SW_ON0 Mode Control (sig_io16_oe = 0)	00: Digital Input without Schmitt Trigger 01: Reserved 10: Reserved 11: Reserved	Valid	Valid
	1159:1158	PWR_SW_ON0 Mode Control (sig_io16_oe = 1)	00: Reserved 01: 2x 10: Reserved 11: Reserved	Valid	Valid
PWR_SW_ON1					
91	1160	Reserved		Valid	Valid
	1161	PWR_SW_ON1 Driver Strength Selection	0: Reserved 1: 2x	Valid	Valid
	1162	PWR_SW_ON1 Pull-up/down Resistor Selection	0: Reserved 1: Reserved	Valid	Valid
	1164:1163	PWR_SW_ON1 Pull-up/down Resistor Value Selection	00: Reserved 01: Reserved 10: Reserved 11: Reserved	Valid	Valid
	1167:1165	PWR_SW_ON1 Mode Control	000: Digital Input without Schmitt Trigger 001: Reserved 010: Reserved 011: Reserved 100: Push-Pull 101: Reserved 110: Reserved 111: Reserved	Valid	Valid
ACMP1					
92	1168	ACMP1 Positive Input Source Select	0: IO8 1: ACMP0 IN+ source	Valid	Valid
	1169	ACMP1 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
	1171:1170	ACMP1 Hysteresis Enable	00: 0mV 01: 25mV 10: 50mV 11: 200mV (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50mV & 200mV hysteresis.)	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
ACMP0					
92	1172	ACMP0 Positive Input Source Select	0: IO4 1: V_{DD}	Valid	Valid
	1173	ACMP0 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
	1175:1174	ACMP0 Hysteresis Enable	00: 0mV 01: 25mV 10: 50mV 11: 200mV (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50mV & 200mV hysteresis.)	Valid	Valid
ACMP3					
93	1177:1176	ACMP3 Positive Input Source Select	00: IO12 01: ACMP2 IN+ source 10: ACMP0 IN+ source 11: Reserved	Valid	Valid
	1179:1178	ACMP3 Hysteresis Enable	00: 0mV 01: 25mV 10: 50mV 11: 200mV (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50mV & 200mV hysteresis.)	Valid	Valid
ACMP2					
93	1180	ACMP2 Positive Input Source Select	0: IO10 1: ACMP0 IN+ source	Valid	Valid
	1182:1181	ACMP2 Hysteresis Enable	00: 0mV 01: 25mV 10: 50mV 11: 200mV (01: for both external & internal Vref; 10 & 11: for only internal Vref; External Vref will not have 50mV & 200mV hysteresis.)	Valid	Valid
ACMP1 100 uA Current Source Enable					
93	1183	ACMP1 100 uA Current Source Enable	0: Disable 1: Enable	Valid	Valid
LUT3_x Function Select					
94	1184	LUT3_3 or DFF6 with nRST/nSET Select	0: LUT3_3 1: DFF6 with nRST/nSET	Valid	Valid
	1185	LUT3_2 or DFF5 with nRST/nSET Select	0: LUT3_2 1: DFF5 with nRST/nSET	Valid	Valid
	1186	LUT3_1 or DFF4 with nRST/nSET Select	0: LUT3_1 1: DFF4 with nRST/nSET	Valid	Valid
	1187	LUT3_0 or DFF3 with nRST/nSET Select (Two consecutive DFFs if register [1471] = 1 for SM)	0: LUT3_0 1: DFF3 with nRST/nSET	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
LUT2_x Function Select					
94	1188	LUT2_3 or PGen Select	0: LUT2_3 1: PGen	Valid	Valid
	1189	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2	Valid	Valid
	1190	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1	Valid	Valid
	1191	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0	Valid	Valid
LUT4_x Function Select					
95	1192	LUT4_1 or DLY/CNT1(16bits) Select	0: LUT4_1 1: DLY/CNT1(16bits)	Valid	Valid
	1193	LUT4_0 or DLY/CNT0(16bits) Select	0: LUT4_0 1: DLY/CNT0(16bits)	Valid	Valid
LUT3_x Function Select					
95	1194	LUT3_9 or DLY/CNT6(8bits) Select	0: LUT3_9 1: DLY/CNT6(8bits)	Valid	Valid
	1195	LUT3_8 or DLY/CNT5(8bits) Select	0: LUT3_8 1: DLY/CNT5(8bits)	Valid	Valid
	1196	LUT3_7 or DLY/CNT4(8bits) Select	0: LUT3_7 1: DLY/CNT4(8bits)	Valid	Valid
	1197	LUT3_6 or DLY/CNT3(8bits) Select	0: LUT3_6 1: DLY/CNT3(8bits)	Valid	Valid
	1198	LUT3_5 or DLY/CNT2(8bits) Select	0: LUT3_5 1: DLY/CNT2(8bits)	Valid	Valid
	1199	LUT3_4 or DFF7 with nRST/nSET Select	0: LUT3_4 1: DFF7 with nRST/nSET	Valid	Valid
LUT2_1/DFF1					
96	1200	LUT2_1 [0]		Valid	Valid
	1201	LUT2_1 [1]/DFF1 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1202	LUT2_1 [2]/DFF1 Output Select	0: Q output 1: QB output	Valid	Valid
	1203	LUT2_1 [3]/DFF1 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT2_0/DFF0					
96	1204	LUT2_0 [0]		Valid	Valid
	1205	LUT2_0 [1]/DFF0 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1206	LUT2_0 [2]/DFF0 Output Select	0: Q output 1: QB output	Valid	Valid
	1207	LUT2_0 [3]/DFF0 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT2_3/PGen					
97	1211:1208	LUT2_3 [3:0] or PGen 4bit counter data[3:0]		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
LUT2_2/DFF2					
97	1212	LUT2_2 [0]		Valid	Valid
	1213	LUT2_2 [1]/DFF2 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1214	LUT2_2 [2]/DFF2 Output Select	0: Q output 1: QB output	Valid	Valid
	1215	LUT2_2 [3]/DFF2 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3_0/DFF3					
98	1219:1216	LUT3_0 [3:0]		Valid	Valid
	1220	LUT3_0 [4]/DFF3 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1221	LUT3_0 [5]/DFF3 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1222	LUT3_0 [6]/DFF3 Output Select	0: Q output 1: QB output	Valid	Valid
	1223	LUT3_0 [7]/DFF3 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3_1/DFF4					
99	1227:1224	LUT3_1 [3:0]		Valid	Valid
	1228	LUT3_1 [4]/DFF4 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1229	LUT3_1 [5]/DFF4 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1230	LUT3_1 [6]/DFF4 Output Select	0: Q output 1: QB output	Valid	Valid
	1231	LUT3_1 [7]/DFF4 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3_2/DFF5					
9A	1235:1232	LUT3_2 [3:0]		Valid	Valid
	1236	LUT3_2 [4]/DFF5 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1237	LUT3_2 [5]/DFF5 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1238	LUT3_2 [6]/DFF5 Output Select	0: Q output 1: QB output	Valid	Valid
	1239	LUT3_2 [7]/DFF5 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
LUT3_3/DFF6					
9B	1243:1240	LUT3_3 [3:0]		Valid	Valid
	1244	LUT3_3 [4]/DFF6 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1245	LUT3_3 [5]/DFF6 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1246	LUT3_3 [6]/DFF6 Output Select	0: Q output 1: QB output	Valid	Valid
	1247	LUT3_3 [7]/DFF6 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3_4/DFF7					
9C	1251:1248	LUT3_4 [3:0]		Valid	Valid
	1252	LUT3_4 [4]/DFF7 Initial Polarity Select	0: Low 1: High	Valid	Valid
	1253	LUT3_4 [5]/DFF7 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
	1254	LUT3_4 [6]/DFF7 Output Select	0: Q output 1: QB output	Valid	Valid
	1255	LUT3_4 [7]/DFF7 or LATCH Select	0: DFF function 1: LATCH function	Valid	Valid
LUT3_10/Pipe Delay					
9D	1259:1256	LUT3_10 [3:0]/Pipe Delay OUT0 Select		Valid	Valid
	1263:1260	LUT3_10 [7:4]/Pipe Delay OUT1 Select		Valid	Valid
9E	1265:1264	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay	Valid	Valid
	1267:1266	Delay Value Select for Programmable Delay & Edge Detector (V_{DD} = 3.3V, typical)	00: 125ns 01: 250ns 10: 375ns 11: 500ns	Valid	Valid
	1269:1268	Crystal oscillator Power-down enable	00: No matrix PD 01: matrix PD for crystal oscillator 10: Reserved 11: Reserved	Valid	Valid
	1270	LUT3_10 or Pipe Delay Select	0: LUT3_10 1: Pipe Delay	Valid	Valid
	1271	Pipe Delay OUT1 Polarity Select	0: Non-inverted 1: Inverted	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT2					
9F	1273:1272	DLY2 Mode Select or Asynchronous CNT2 Reset	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1276:1274	DLY/CNT2 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter1 Overflow	Valid	Valid
	1277	DLY/CNT2 Output Selection if DLY/CNT2 Mode Selection is "11".	0: Default Output 1: Edge Detector Output	Valid	Valid
	1279:1278	DLY/CNT2 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT3					
A0	1281:1280	DLY3 Mode Select or Asynchronous CNT3 Reset	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1284:1282	DLY/CNT3 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter2 Overflow	Valid	Valid
	1285	DLY/CNT3 Output Selection if DLY/CNT3 Mode Selection is "11".	0: Default Output 1: Edge Detector Output	Valid	Valid
	1287:1286	DLY/CNT3 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT4					
A1	1289:1288	DLY4 Mode Select or Asynchronous CNT4 Reset	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1292:1290	DLY/CNT4 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter3 Overflow	Valid	Valid
	1293	DLY/CNT4 Output Selection if DLY/CNT4 Mode Selection is "11".	0: Default Output 1: Edge Detector Output	Valid	Valid
	1295:1294	DLY/CNT4 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT5					
A2	1297:1296	DLY5 Mode Select or Asynchronous CNT5 Reset	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1300:1298	DLY/CNT5 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter4 Overflow	Valid	Valid
	1301	DLY/CNT5 Output Selection if DLY/CNT5 Mode Selection is "11".	0: Default Output 1: Edge Detector Output	Valid	Valid
	1303:1302	DLY/CNT5 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT6					
A3	1305:1304	DLY6 Mode Select or Asynchronous CNT6 Reset	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1308:1306	DLY/CNT6 Clock Source Select	000: Internal OSC clock 001: OSC/4 010: OSC/12, 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter5 Overflow	Valid	Valid
	1309	DLY/CNT6 Output Selection if DLY/CNT6 Mode Selection is "11".	0: Default Output 1: Edge Detector Output	Valid	Valid
	1311:1310	DLY/CNT6 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT0					
A4	1313:1312	DLY0 Mode Select or Asynchronous CNT0 Reset (16bits)	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1316:1314	DLY/CNT0 Clock Source Select (16bits)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter6 Overflow	Valid	Valid
	1317	CNT0/FSM0's Q are Set to data or Reset to 0s Selection (16bits)	0: Reset to 0s 1: Set to data (registers [1583:1576, 1591:1584])	Valid	Valid
	1319:1318	DLY/CNT0 Mode Selection (16bits)	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DLY/CNT1					
A5	1321:1320	DLY1 Mode Select or Asynchronous CNT1 Reset (16bits)	00: On both Falling and Rising Edges (for Delay & Counter Reset) 01: on Falling Edge only (for Delay & Counter Reset) 10: on Rising Edge only (for Delay & Counter Reset) 11: No Delay on either Falling or Rising Edges/High Level Reset	Valid	Valid
	1324:1322	DLY/CNT1 Clock Source Select (16bits)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: 25MHz OSC clock 110: External Clock 111: Counter0 Overflow	Valid	Valid
	1325	CNT1/FSM1's Q are Set to data or Reset to 0s Selection (16bits)	0: Reset to 0s 1: Set to data (registers [1599:1592, 1607:1600])	Valid	Valid
	1327:1326	DLY/CNT1 Mode Selection (16bits)	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNTx One-Shot/Freq. Detect Output Polarity					
A6	1328	DLY/CNT0 stop & restarting enable in CNT mode when new data is loaded	0: Disable 1: Enable	Valid	Valid
	1329	Select the Polarity of DLY/CNT6's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1330	Select the Polarity of DLY/CNT5's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1331	Select the Polarity of DLY/CNT4's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1332	Select the Polarity of DLY/CNT3's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1333	Select the Polarity of DLY/CNT2's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1334	Select the Polarity of DLY/CNT1's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid
	1335	Select the Polarity of DLY/CNT0's One Shot/ Freq. Detect Output	0: Default Output 1: Inverted Output	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Oscillator					
A7	1337:1336	OSC Clock Pre-divider for 25MHz	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
	1338	OSC Fast Start-Up Enable for 25kHz/2MHz	0: Disable 1: Enable	Valid	Valid
	1340:1339	OSC Clock Pre-divider for 25kHz/2MHz	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
A7	1341	Force 25MHz Oscillator ON	0: Auto Power-On (If any CNT/DLY use 25MHz source) 1: Force Power-On	Valid	Valid
	1342	Oscillator (25kHz: Ring OSC, 2M: RC-OSC) Select	0: 25kHz Ring OSC 1: 2MHz RC-OSC	Valid	Valid
	1343	Force 25kHz/2MHz Oscillator ON	0: Auto Power-On (if any CNT/DLY use 25K/2MHz source) 1: Force Power-On	Valid	Valid
A8	1346:1344	Internal OSC 25kHz/2MHz Frequency Divider Control for matrix input [28]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
	1349:1347	Internal OSC 25kHz/2MHz Frequency Divider Control for matrix input [27]	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
	1350	OSC Clock 25kHz/2MHz to matrix input [28] enable	0: Disable 1: Enable	Valid	Valid
	1351	OSC Clock 25kHz/2MHz to matrix input [27] enable	0: Disable 1: Enable	Valid	Valid
A9	1354:1352	ASM_reg_init[2:0] for ASM state default set-up bits		Valid	Valid
	1355	External oscillator pin selection for 25kHz/2MHz	0: IO17 1: IO15	Valid	Valid
	1356	OSC Clock 25 MHz to matrix input [29] enable	0: Disable 1: Enable	Valid	Valid
	1357	External Clock Source Select instead of 25MHz	0: Internal Oscillator 1: External Clock from IO14	Valid	Valid
	1358	External Clock Source Select instead of 25kHz/2MHz	0: Internal Oscillator 1: External Clock from IO15 or IO17	Valid	Valid
	1359	DLY/CNT1 stop & restarting enable in CNT mode when new data is loaded	0: Disable 1: Enable	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
ASM 8-to-1 MUX's 3 selection bits					
AA	1362:1360	ASM_state0_dec8x1_EN1		Valid	Valid
	1363	Reserved		Valid	Valid
	1366:1364	ASM_state0_dec8x1_EN0		Valid	Valid
	1367	Reserved		Valid	Valid
AB	1370:1368	ASM_state1_dec8x1_EN0		Valid	Valid
	1371	Reserved		Valid	Valid
	1374:1372	ASM_state0_dec8x1_EN2		Valid	Valid
	1375	Reserved		Valid	Valid
AC	1378:1376	ASM_state1_dec8x1_EN2		Valid	Valid
	1379	Reserved		Valid	Valid
AC	1382:1380	ASM_state1_dec8x1_EN1		Valid	Valid
	1383	Reserved		Valid	Valid
AD	1386:1384	ASM_state2_dec8x1_EN1		Valid	Valid
	1387	Reserved		Valid	Valid
	1390:1388	ASM_state2_dec8x1_EN0		Valid	Valid
	1391	Reserved		Valid	Valid
AE	1394:1392	ASM_state3_dec8x1_EN0		Valid	Valid
	1395	Reserved		Valid	Valid
	1398:1396	ASM_state2_dec8x1_EN2		Valid	Valid
	1399	Reserved		Valid	Valid
AF	1402:1400	ASM_state3_dec8x1_EN2		Valid	Valid
	1403	Reserved		Valid	Valid
	1406:1404	ASM_state3_dec8x1_EN1		Valid	Valid
	1407	Reserved		Valid	Valid
B0	1410:1408	ASM_state4_dec8x1_EN1		Valid	Valid
	1411	Reserved		Valid	Valid
	1414:1412	ASM_state4_dec8x1_EN0		Valid	Valid
	1415	Reserved		Valid	Valid
B1	1418:1416	ASM_state5_dec8x1_EN0		Valid	Valid
	1419	Reserved		Valid	Valid
	1422:1420	ASM_state4_dec8x1_EN2		Valid	Valid
	1423	Reserved		Valid	Valid
B2	1426:1424	ASM_state5_dec8x1_EN2		Valid	Valid
	1427	Reserved		Valid	Valid
	1430:1428	ASM_state5_dec8x1_EN1		Valid	Valid
	1431	Reserved		Valid	Valid
B3	1434:1432	ASM_state6_dec8x1_EN1		Valid	Valid
	1435	Reserved		Valid	Valid
	1438:1436	ASM_state6_dec8x1_EN0		Valid	Valid
	1439	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B4	1442:1440	ASM_state7_dec8x1_EN0		Valid	Valid
	1443	Reserved		Valid	Valid
	1446:1444	ASM_state6_dec8x1_EN2		Valid	Valid
	1447	Reserved		Valid	Valid
B5	1450:1448	ASM_state7_dec8x1_EN2		Valid	Valid
	1451	Reserved		Valid	Valid
	1454:1452	ASM_state7_dec8x1_EN1		Valid	Valid
	1455	Reserved		Valid	Valid
Filter/Edge Detector					
B6	1457:1456	Select the edge mode of Edge Detector_1	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
	1458	Filter_1/Edge Detector_1 output Polarity Select	0: Filter_1 output 1: Filter_1 output inverted	Valid	Valid
	1459	Filter_1or Edge Detector_1 Select (Typ. 30 ns @V_{DD} = 3.3 V)	0: Filter_1 1: Edge Detector_1	Valid	Valid
	1461:1460	Select the edge mode of Edge Detector_0	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
	1462	Filter_0/Edge Detector_0 output Polarity Select	0: Filter_0 output 1: Filter_0 output inverted	Valid	Valid
	1463	Filter_0 or Edge Detector_0 Select (Typ. 47 ns @V_{DD} = 3.3 V)	0: Filter_0 1: Edge Detector_0	Valid	Valid
Vref/Bandgap					
B7	1464	Reserved		Valid	Valid
	1466:1465	Bandgap OK for ACMP Output Delay Time Select, the start Time is "nRST_core go to High"	00 or 10 with registers [1474:1472] = 100 (WideV_{DD} range,1.7V~5.5V): Auto-delay mode, 550 uS for V_{DD} < 2.7V & 100 uS for 2.7 V < V_{DD} 00 or 10 with registers [1474:1472] = X10: Always 100 uS delay for 2.7 V < V_{DD} 00 or 10 with registers [1474:1472] = XX1: Always 550uS delay for V_{DD} < 2.7 V, 01: Always 550us delay regardless of registers [1474:1472] & V_{DD}, 11: Always 100 us delay with 2.7V < V_{DD} regardless of registers [1474:1472]	Valid	Valid
	1467	Reserved		Valid	Valid
	1468	Reserved		Valid	Valid
	1469	Reserved		Valid	Valid
	1470	Reserved		Valid	Valid
	1471	Two consecutive DFFs enable for SM	0: Disable 1: Enable	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
B8	1474:1472	Power divider (V_{DD}/3, V_{DD}/4) ON/OFF	0XX: Power divider off (if there is no use of V_{DD}/3, V_{DD}/4 @ ACMP negative in) 100: Reserved X10: Reserved XX1:Reserved	Valid	Valid
	1475	V_{DD} Bypass Enable when device power is 1.8 V	0: Regulator Auto ON 1: Regulator OFF (V_{DD} Bypass)	Valid	Valid
	1476	Force Bandgap ON	0: Auto-Mode 1: Enable (if chip is Power-down, the Bandgap will Power-down even if it is Set to 1).	Valid	Valid
	1477	NVM Power-down	0: None (Or Programming Enable) 1: Power-down (Or Programming Disable)	Valid	Valid
	1478	Reserved		Valid	Valid
	1479	GPIO Quick Charge Enable	0: Disable 1: Enable	Valid	Valid
B9	1482:1480	Vref Output Source Select	000: ACMP2 Vref 001: ACMP3 Vref 100: V_{DD}/2 101: V_{DD}/3 110: V_{DD}/4 111: Hi-Z	Valid	Valid
	1483	Reserved		Valid	Valid
	1486:1484	Reserved		Valid	Valid
	1487	Reserved		Valid	Valid
BA	1488	Reserved		Valid	Valid
	1489	Wake time Selection in Wake Sleep Mode	0: short wake time 1: normal wake time	Valid	Valid
	1490	ACMP0 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1491	ACMP1 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1492	ACMP2 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1493	ACMP3 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
	1494	Wake Sleep Output State When WS Oscillator is Power-down if DLY/CNT0 Mode Selection is "11"	0: Low 1: High	Valid	Valid
	1495	Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"	0: Default Mode 1: Wake Sleep Ratio Control Mode	Valid	Valid
BB	1503:1496	Reserved		Valid	Valid
BC	1511:1504	Reserved		Valid	Valid
BD	1519:1512	Reserved		Valid	Valid
BE	1527:1520	Reserved		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
BF	1535:1528	Reserved		Valid	Valid
LUT/DLY/CNT Control Data					
C0	1543:1536	LUT3_5 [7:0] or DLY/CNT2 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C1	1551:1544	LUT3_6 [7:0] or DLY/CNT3 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C2	1559:1552	LUT3_7 [7:0] or DLY/CNT4 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C3	1567:1560	LUT3_8 [7:0] or DLY/CNT5 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C4	1575:1568	LUT3_9 [7:0] or DLY/CNT6 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1]/Freq)	Valid	Valid
C5	1583:1576	LUT4_0 [15:0] or DLY/CNT0 (16bits, [15:0] = [1591:1576]) Control Data	1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq)	Valid	Valid
C6	1591:1584			Valid	Valid
C7	1599:1592	LUT4_1 [15:0] or DLY/CNT1 (16bits, [15:0] = [1607:1592]) Control Data	1 - 65535 (Delay Time = [Counter Control Data + 2]/Freq)	Valid	Valid
C8	1607:1600			Valid	Valid
C9	1615:1608	PGen pattern data [15:0] = [1623:1608]		Valid	Valid
CA	1623:1616			Valid	Valid
ACMP0					
CB	1628:1624	ACMP0-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO5: ACMP0- 11100: IO9: EXT_Vref/2 11101: IO5: ACMP0-/2 11110: Reserved 11111: Reserved	Valid	Valid
	1630:1629	ACMP0 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1631	ACMP0 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1:ON	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I^2C Interface	
Byte	Register Bit			Read	Write
ACMP1					
CC	1636:1632	ACMP1-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: Reserved 11100: IO9: EXT_Vref/2 11101: Reserved 11110: Reserved 11111: Reserved	Valid	Valid
	1638:1637	ACMP1 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1639	ACMP1 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid
ACMP2					
CD	1644:1640	ACMP2-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO11: ACMP2- 11100: IO9: EXT_Vref /2 11101: IO11: ACMP2-/2 11110: Reserved 11111: Reserved	Valid	Valid
	1646:1645	ACMP2 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1647	ACMP2 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
ACMP3					
CE	1652:1648	ACMP3-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: IO9: EXT_Vref 11011: IO11: ACMP3- 11100: IO9: EXT_Vref/2 11101: IO11: ACMP3-/2 11110: Reserved 11111: Reserved	Valid	Valid
	1654:1653	ACMP3 Positive Input Divider	00: 1.0x 01: 0.5x 10: 0.33x 11: 0.25x	Valid	Valid
	1655	ACMP3 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid
Misc.					
CF	1656	Reserved		Valid	Valid
	1657	Switch from “Matrix OUT: OSC 25MHz PD” to “Matrix OUT: OSC 25MHz Force On”	0: OSC PD 1: OSC Force On (Matrix Output [59])	Valid	Valid
	1658	Switch from “Matrix OUT: OSC 25kHz/2MHz PD” to “Matrix OUT: OSC 25kHz/2MHz Force On”	0: OSC PD 1: OSC Force On (Matrix Output [58])	Valid	Valid
	1659	Reserved Reserved		Valid	Valid
CF	1660	Reserved Reserved		Valid	Valid
	1661	Reserved Reserved		Valid	Valid
	1662	I²C reset bit with reloading NVM into Data register (TBD)	0: Keep existing condition 1: Reset execution	Valid	Valid
	1663	Reserved		Valid	Valid
D0	1671:1664	RAM 8 outputs for ASM-state0		Valid	Valid
D1	1679:1672	RAM 8 outputs for ASM-state1		Valid	Valid
D2	1687:1680	RAM 8 outputs for ASM-state2		Valid	Valid
D3	1695:1688	RAM 8 outputs for ASM-state3		Valid	Valid
D4	1703:1696	RAM 8 outputs for ASM-state4		Valid	Valid
D5	1711:1704	RAM 8 outputs for ASM-state5		Valid	Valid
D6	1719:1712	RAM 8 outputs for ASM-state6		Valid	Valid
D7	1727:1720	RAM 8 outputs for ASM-state7		Valid	Valid
D8	1735:1728	User configurable RAM/OTP Byte 0		Valid	Valid
D9	1743:1736	User configurable RAM/OTP Byte 1		Valid	Valid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
DA	1751:1744	User configurable RAM/OTP Byte 2		Valid	Valid
DB	1759:1752	User configurable RAM/OTP Byte 3		Valid	Valid
DC	1767:1760	User configurable RAM/OTP Byte 4		Valid	Valid
DD	1775:1768	User configurable RAM/OTP Byte 5		Valid	Valid
DE	1783:1776	User configurable RAM/OTP Byte 6		Valid	Valid
DF	1791:1784	User configurable RAM/OTP Byte 7		Valid	Valid
E0	1799:1792	Reserved		Invalid	Invalid
E1	1807:1800	Reserved		Invalid	Invalid
E2	1815:1808	Reserved		Invalid	Invalid
E3	1823:1816	Reserved		Invalid	Invalid
E4	1831:1824	Reserved		Valid	Valid
E5	1832	I²C lock for read bits [1535:0] (Bank 0/1/2)	0: Disable (Programmed data can be read.), 1: Enable (Programmed data can't be read.)	Valid	Invalid
	1833	Reserved		Valid	Invalid
	1835:1834	Reserved		Valid	Invalid
	1839:1836	Reserved		Valid	Invalid
E6	1847:1840	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]		Valid	Valid
E7	1855:1848	Reserved		Valid	Invalid
E8	1863:1856	Reserved		Valid	Invalid
E9	1867:1864	I²C Control Code Bit [3:0]	Value for slave address	Valid	Invalid
	1868	Reserved		Valid	Valid
	1869	Reserved		Valid	Valid
	1870	I²C lock for write all bits (Bank 0/1/2/3)	0: writable 1: Non-writable	Valid	Valid
	1871	I²C lock for write bits [1535:0] (Bank 0/1/2)	0: writable 1: Non-writable	Valid	Invalid
EA	1879:1872	CNT4 Counted Value		Valid	Invalid
EB	1887:1880	CNT0 (16bits) = [1895:1880] Counted Value		Valid	Invalid
EC	1895:1888			Valid	Invalid
ED	1903:1896	CNT6 Counted Value		Valid	Invalid
EE	1911:1904	CNT1 (16bits) = [1919:1904] Counted Value		Valid	Invalid
EF	1919:1912			Valid	Invalid

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Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
Matrix Input					
F0	1920	Matrix Input 0	GND	Valid	Invalid
	1921	Matrix Input 1	IO0 Digital Input	Valid	Invalid
	1922	Matrix Input 2	IO1 Digital Input	Valid	Invalid
	1923	Matrix Input 3	IO2 Digital Input	Valid	Invalid
	1924	Matrix Input 4	IO3 Digital Input	Valid	Invalid
	1925	Matrix Input 5	IO4 Digital Input	Valid	Invalid
	1926	Matrix Input 6	IO5 Digital Input	Valid	Invalid
	1927	Matrix Input 7	IO8 Digital Input	Valid	Invalid
F1	1928	Matrix Input 8	LUT2_0/DFF0 Output	Valid	Invalid
	1929	Matrix Input 9	LUT2_1/DFF1 Output	Valid	Invalid
	1930	Matrix Input 10	LUT2_2/DFF2 Output	Valid	Invalid
	1931	Matrix Input 11	LUT2_3/PGen Output	Valid	Invalid
	1932	Matrix Input 12	LUT3_0/DFF3 Output	Valid	Invalid
	1933	Matrix Input 13	LUT3_1/DFF4 Output	Valid	Invalid
	1934	Matrix Input 14	LUT3_2/DFF5 Output	Valid	Invalid
	1935	Matrix Input 15	LUT3_3/DFF6 Output	Valid	Invalid
F2	1936	Matrix Input 16	LUT3_4/DFF7 Output	Valid	Invalid
	1937	Matrix Input 17	LUT3_5/CNT_DLY2(8bit) Output	Valid	Invalid
	1938	Matrix Input 18	LUT3_6/CNT_DLY3(8bit) Output	Valid	Invalid
	1939	Matrix Input 19	LUT3_7/CNT_DLY4(8bit) Output	Valid	Invalid
	1940	Matrix Input 20	LUT3_8/CNT_DLY5(8bit) Output	Valid	Invalid
	1941	Matrix Input 21	LUT3_9/CNT_DLY6(8bit) Output	Valid	Invalid
	1942	Matrix Input 22	LUT4_0/CNT_DLY0(16bit) Output	Valid	Invalid
	1943	Matrix Input 23	LUT4_1/CNT_DLY1(16bit) Output	Valid	Invalid
F3	1944	Matrix Input 24	LUT3_10/Pipe Delay (1st stage) Output	Valid	Invalid
	1945	Matrix Input 25	Pipe Delay Output0	Valid	Invalid
	1946	Matrix Input 26	Pipe Delay Output1	Valid	Invalid
	1947	Matrix Input 27	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1948	Matrix Input 28	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1949	Matrix Input 29	Fixed "L" output because it is OSC clock.	Valid	Invalid
	1950	Matrix Input 30	Filter0/Edge Detect0 Output	Valid	Invalid
	1951	Matrix Input 31	Filter1/Edge Detect1 Output	Valid	Invalid
F4	1952	Matrix Input 32	Virtual Input [0]	Valid	Valid
	1953	Matrix Input 33	Virtual Input [1]	Valid	Valid
	1954	Matrix Input 34	Virtual Input [2]	Valid	Valid
F4	1955	Matrix Input 35	Virtual Input [3]	Valid	Valid
	1956	Matrix Input 36	Virtual Input [4]	Valid	Valid
	1957	Matrix Input 37	Virtual Input [5]	Valid	Valid
	1958	Matrix Input 38	Virtual Input [6]	Valid	Valid
	1959	Matrix Input 39	Virtual Input [7]	Valid	Valid

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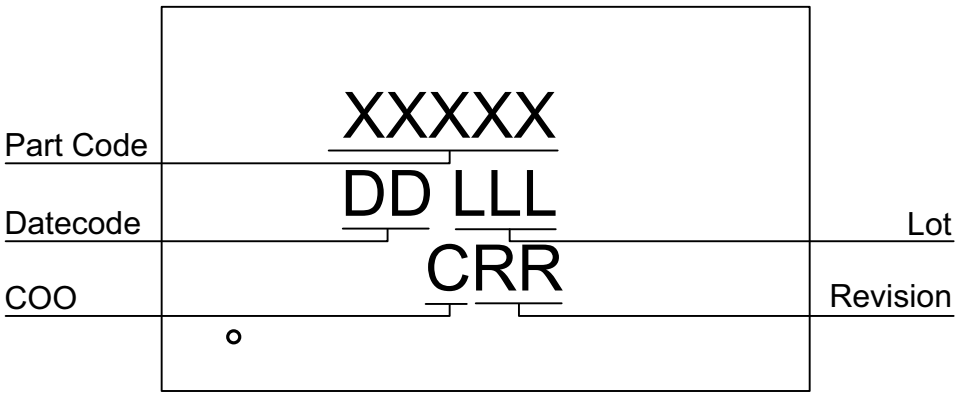
Table 97: Register Map (Continued)

Address		Signal Function	Register Bit Definition	I²C Interface	
Byte	Register Bit			Read	Write
F5	1960	Matrix Input 40	RAM_0 Output for ASM-state	Valid	Invalid
	1961	Matrix Input 41	RAM_1 Output for ASM-state	Valid	Invalid
	1962	Matrix Input 42	RAM_2 Output for ASM-state	Valid	Invalid
	1963	Matrix Input 43	RAM_3 Output for ASM-state	Valid	Invalid
	1964	Matrix Input 44	RAM_4 Output for ASM-state	Valid	Invalid
	1965	Matrix Input 45	RAM_5 Output for ASM-state	Valid	Invalid
	1966	Matrix Input 46	RAM_6 Output for ASM-state	Valid	Invalid
	1967	Matrix Input 47	RAM_7 Output for ASM-state	Valid	Invalid
F6	1968]	Matrix Input 48	IO9 Digital Input	Valid	Invalid
	1969]	Matrix Input 49	IO10 Digital Input	Valid	Invalid
	1970]	Matrix Input 50	IO11 Digital Input	Valid	Invalid
	1971]	Matrix Input 51	IO12 Digital Input	Valid	Invalid
	1972]	Matrix Input 52	IO13 Digital Input	Valid	Invalid
	1973]	Matrix Input 53	IO14 Digital Input	Valid	Invalid
	1974]	Matrix Input 54	IO15 Digital Input	Valid	Invalid
	1975]	Matrix Input 55	IO16 Digital Input	Valid	Invalid
F7	1976]	Matrix Input 56	IO17 Digital Input	Valid	Invalid
	1977]	Matrix Input 57	ACMP_0 Output	Valid	Invalid
	1978]	Matrix Input 58	ACMP_1 Output	Valid	Invalid
	1979]	Matrix Input 59	ACMP_2 Output	Valid	Invalid
	1980]	Matrix Input 60	ACMP_3 Output	Valid	Invalid
	1981]	Matrix Input 61	Programmable Delay with Edge Detector Output	Valid	Invalid
	1982]	Matrix Input 62	Resetb_core	Valid	Invalid
	1983]	Matrix Input 63	V_{DD}	Valid	Invalid
Reserved					
F8	1991:1984]	Reserved		Valid	Invalid
F9	1999:1992]	Reserved		Valid	Invalid
FA	2007:2000]	Reserved		Valid	Invalid
FB	2015:2008]	Reserved		Valid	Valid
FC	2023:2016]	Reserved		Valid	Invalid
FD	2031:2024]	Reserved		Valid	Invalid
FE	2039:2032]	Reserved		Valid	Valid
FF	2047:2040]	Reserved		Valid	Valid

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21 Package Top Marking Definitions

21.1 MSTQFN 28L 2 MM X 3 MM 0.4P PACKAGE



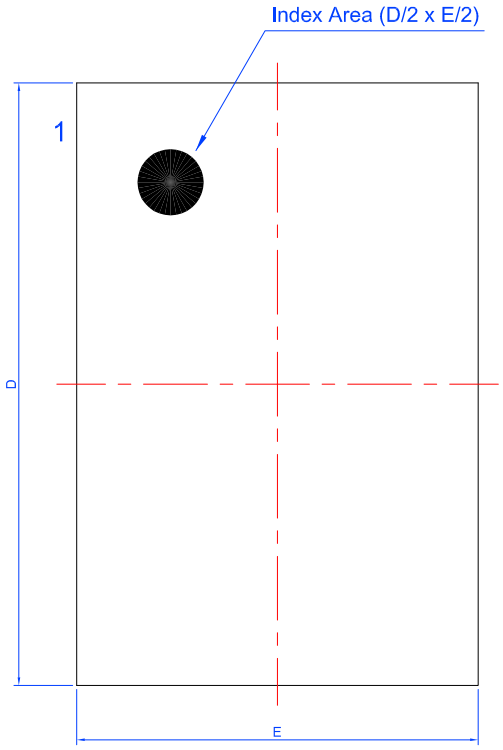
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

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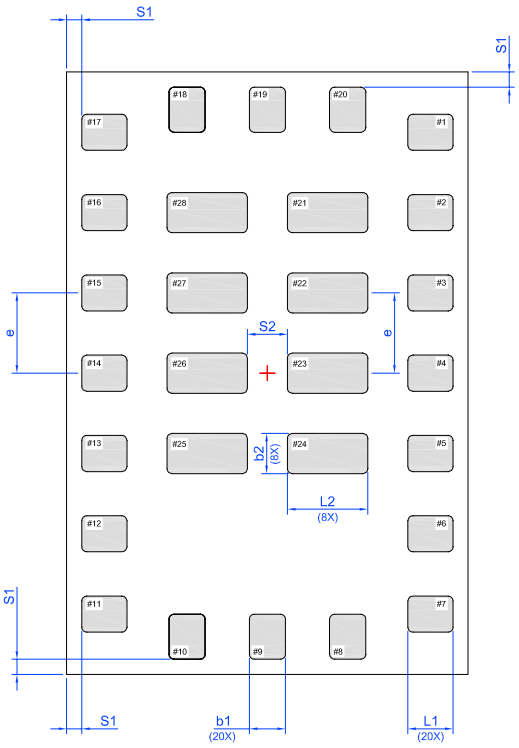
22 Package Information

22.1 PACKAGE OUTLINES FOR MSTQFN 28L 2 MM X 3 MM 0.4P PACKAGE

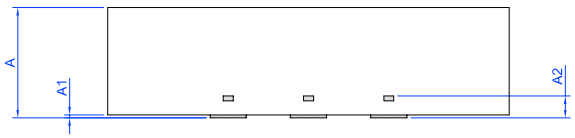
JEDEC MO-220
IC Net Weight: TBD g



Marking View



BTM View



Side View

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.00	-	0.01	E	1.95	2.00	2.05
A2	0.11 REF			e	0.40 BSC		
b1	0.13	0.18	0.23	L1	0.175	0.225	0.275
b2	0.15	0.20	0.25	L2	0.35	0.40	0.45
S1	0.075 REF			S2	0.20 REF		

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22.2 MSTQFN HANDLING

Be sure to handle MSTQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle MSTQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

22.3 SOLDERING INFORMATION

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal) for MSTQFN 28L Package. More information can be found at www.jedec.org.

23 Ordering Information

Part Number	Type
SLG46517M	28-pin MSTQFN
SLG46517MTR	28-pin MSTQFN - Tape and Reel (3k units)

Note 1 Use SLG46517M to order. Shipments are automatically in Tape and Reel.
Note 2 "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

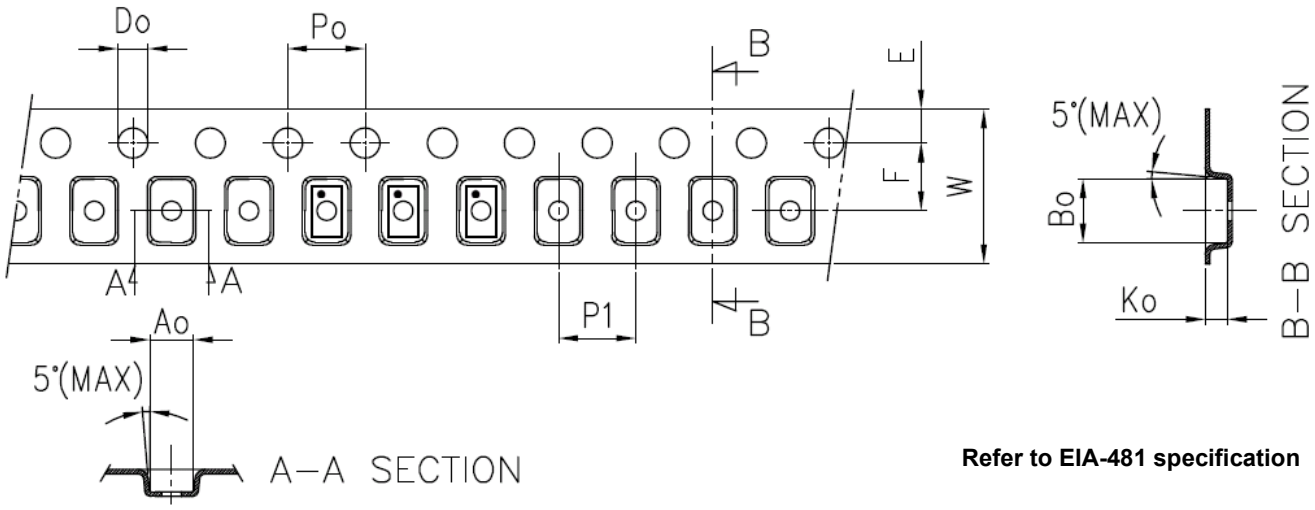
23.1 TAPE AND REEL SPECIFICATIONS

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
MSTQFN 28L 2 mm x3 mm 0.4P Green	28	2 x 3 x 0.55	3,000	3,000	178/60	100	400	100	400	8	4

23.2 CARRIER TAPE DRAWING AND DIMENSIONS

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
MSTQFN 28L 2 mm x 3 mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

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Refer to EIA-481 specification

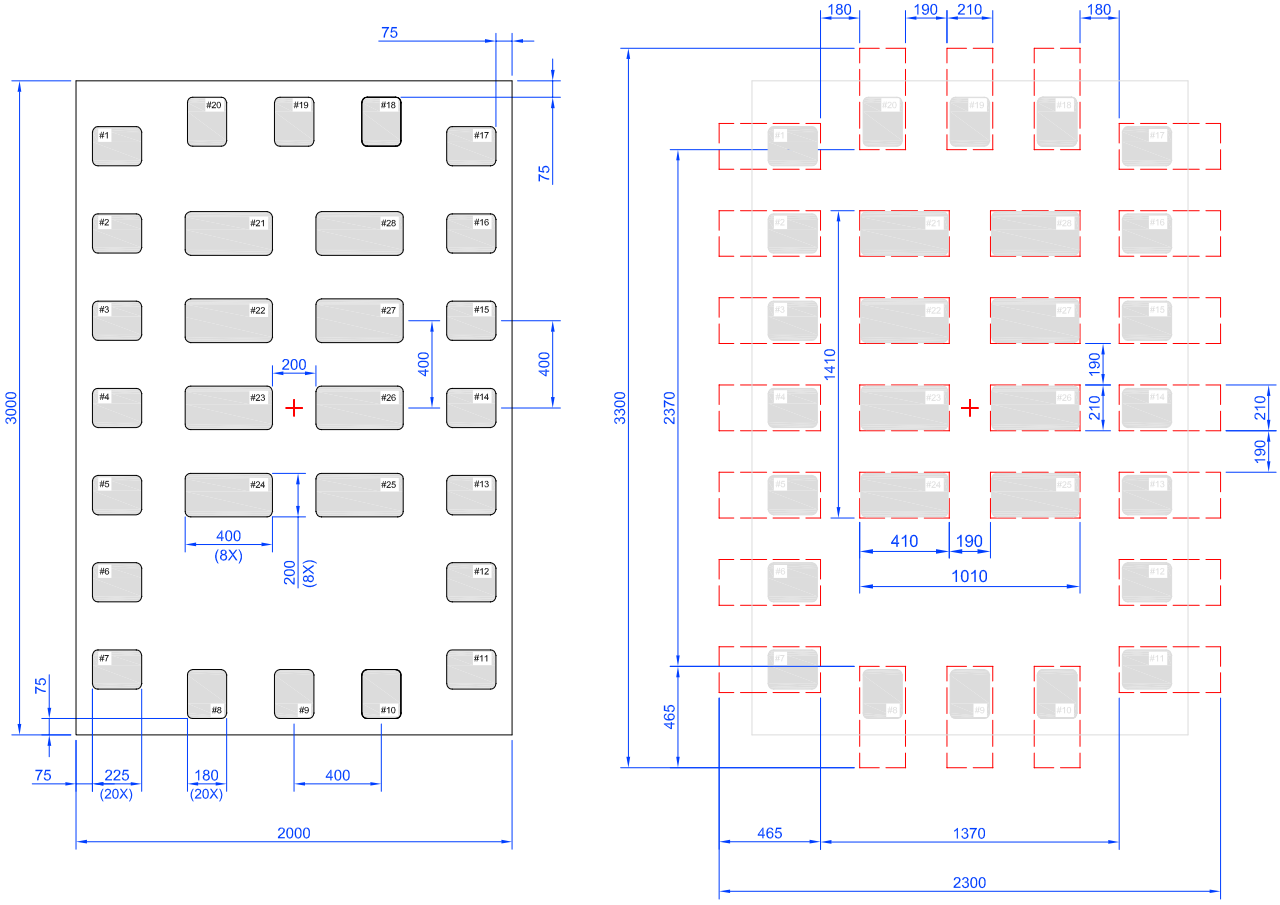
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24 Layout Guidelines

24.1 MSTQFN 28L 2 MM X 3 MM 0.4P PACKAGE

Exposed Pad
(PKG face down)

Recommended Land Pattern
(PKG face down)



Marking View

Unit: µm

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Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ASM	Asynchronous State Machine

B

BG	Bandgap

C

CLK	Clock
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

EC	Electrical Characteristics
ESD	Electrostatic discharge

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LSB	Least Significant Bit
LB	Low Bandwidth
LUT	Look Up Table

M

MSB	Most Significant Bit
MUX	Multiplexer

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N

nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-Pull
PVT	Process Voltage Temperature
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address

V

Vref	Voltage Reference

W

WS	Wake and Sleep Controller

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Revision History

Revision	Date	Description
3.9	2-Mar-2023	Added notes to section Ordering Information
3.8	26-Jan-2023	Corrected figure POR Sequence
3.7	7-Mar-2022	Updated Pull-up or Pull-down Resistance Parameter in EC table Renesas rebranding
3.6	22-Jul-2021	Removed note from section Vref Load Regulation Corrected registers [1076:1075], [1084:1083], [1087:1085]
3.5	17-Aug-2020	Updated ACMP Spec Added note for CNTs Updated Pins Structure Diagrams Corrected Reset Command Timing figure
3.4	29-Aug-2019	Updated register <1328> and register <1359> Figure Wake/Sleep Timing Diagram added to section Wake and Sleep Controller Updated section 3-Bit LUT or 8-Bit Counter/Delay Macrocells Updated section 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells Fixed typo in Package Outline Drawing
3.3	2-Jul-2019	Updated according to new template Updated I_{DSS} and I_{GSS} Fixed typos Corrected registers <1466:1464> Fixed statement regarding C1 and C2 in OSC section
3.2	22-May-2018	Corrected Dual P-FET Power Switch Block Diagram Fixed typos Updated according to Dialog's Writing Guideline Corrected 2-bit LUT2 or PGen figure Added new subsection Electrostatic Discharge Ratings Updated registers [1047:1045], [1143:1141], [1177:1176], [1636:1632] Corrected Table Read/Write Protection Options Updated Oscillator Startup Diagram
3.1	13-Aug-2018	Updated registers [1079:1077], registers [1087:1085] in Appendix A
3.0	12-Jul-2018	Final version

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Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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