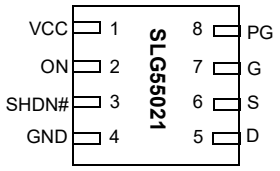
Features

- 5 V ±5% Power supply
- SLG55021 Drain Voltage Range 1.0 V to 20 V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- Stable Slew Rate (±2% typ) over Temperature Range
- TDFN-8 Package
- Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

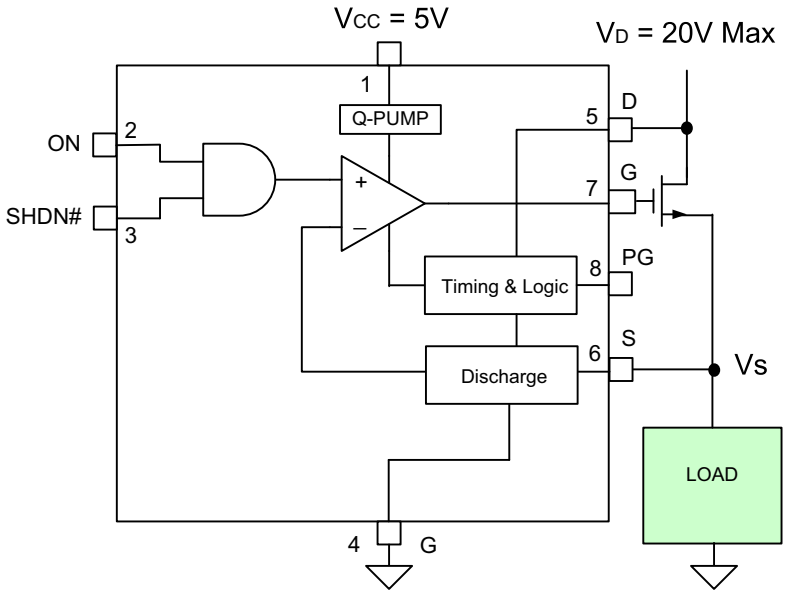


TDFN-8
(Top View)

Applications

- Power Rail Switches
- Hot Plugging Applications
- Soft Switching
- Personal computers and Servers
- Data Communications Equipment

Block Diagram



SLG55021
For N-MOSFETS with V_{GS} < 20V

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Pin Description

Pin #	Pin Name	Type	Pin Description
VCC	1	Power	Supply Voltage
ON	2	Input	CMOS Logic Level. High True
SHDN#	3	Input	Shut Down# - Low True Signal which immediately turns FET off
GND	4	GND	Ground
D	5	Input	FET Drain Connection
S	6	Input	Source Connection
G	7	Output	FET Gate Drive
PG	8	Output	Output CMOS Open Drain - Power Good, indicates external FET fully on

Overview

The SLG55021 N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the SLG55021 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80 V/ms up to 4 V/ms which, depending on load supplying source voltages in the range of 1.0 V to 20 V results in ramp times from 200 µs up to over 20 ms (see Application Section). Delays until the ramp begins are source voltage independent and range from 250 µs to 5 ms. A power good condition is output to indicate that the ramp-up slew of the source voltage is finished. Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The SLG55021 gate drive is packaged in an 8 pin DFN package.

When used with external N-Channel FETs, the SLG55021 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0 V to 20 V.

Ordering Information

Part Number	Ramp Slew Rate (Volts/ms)	Delay Time (ms)	Discharge Resistor (ohms)	Package Type
SLG55021-200010V	2.0	0.15	200	TDFN-8
SLG55021-200010VTR	2.0	0.15	200	TDFN-8 - Tape and Reel (3k units)

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Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V_D or V_S to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Operating temperature range	-55	125	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V
Moisture Sensitivity Level	1		

Electrical Characteristics

T_A = -10 °C to 75 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.75	5.0	5.25	V
I_q	Quiescent Current	V_G not ramping FET = ON	--	<7	10	µA
		V_G not ramping FET = OFF	--	0.1	1	µA
V_D	FET Drain Voltage	SLG55021	1.0	--	20	V
V_{GS}	Gate-Source Voltage	SLG55021	8.0	11.5	13	V
C_G	FET Gate Capacitance		500	--	8000	pF
T_{DELAY}	Ramp Delay Range	1.5ms Default, 500µs step	0.105	0.15	0.195	ms
T_{SLEW}	FET Turn on Slew Rate		1.4	2.0	2.6	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor	Nominal discharge time of ~100ms 10mA max rate	100	200	300	Ω
V_{IH}	HIGH-level input voltage	ON, SHDN# (200mV Hysteresis)	2.4	--	5.5	V
V_{IL}	LOW-level Input voltage	ON, SHDN# (200mV Hysteresis)	--	--	0.4	V
V_{OH}	HIGH-level output voltage	PG Open Drain	--	--	5.5	V
I_{OL_LOGIC}	Logic LOW level output	PG Sink Current	1	2	3	mA
I_{IH}*	SHDN#	V_{IH} = 3.3V	--	--	<1.0	µA
I_{G_OL}	Gate Drive Sink Current		400	--	--	µA
I_{G_OH}	Gate Drive Source Current		32	--	--	µA
I_{D_IH}	Drain Pin Current	V_D = 20V in Standby	--	--	<1.0	µA
I_{S_IH}	Source Pin Current Quiesent	V_S = 20V	--	--	<1.0	µA

Notes:
1. If using an open drain to drive SHDN#; pull up with 10 kΩ to V_{CC}

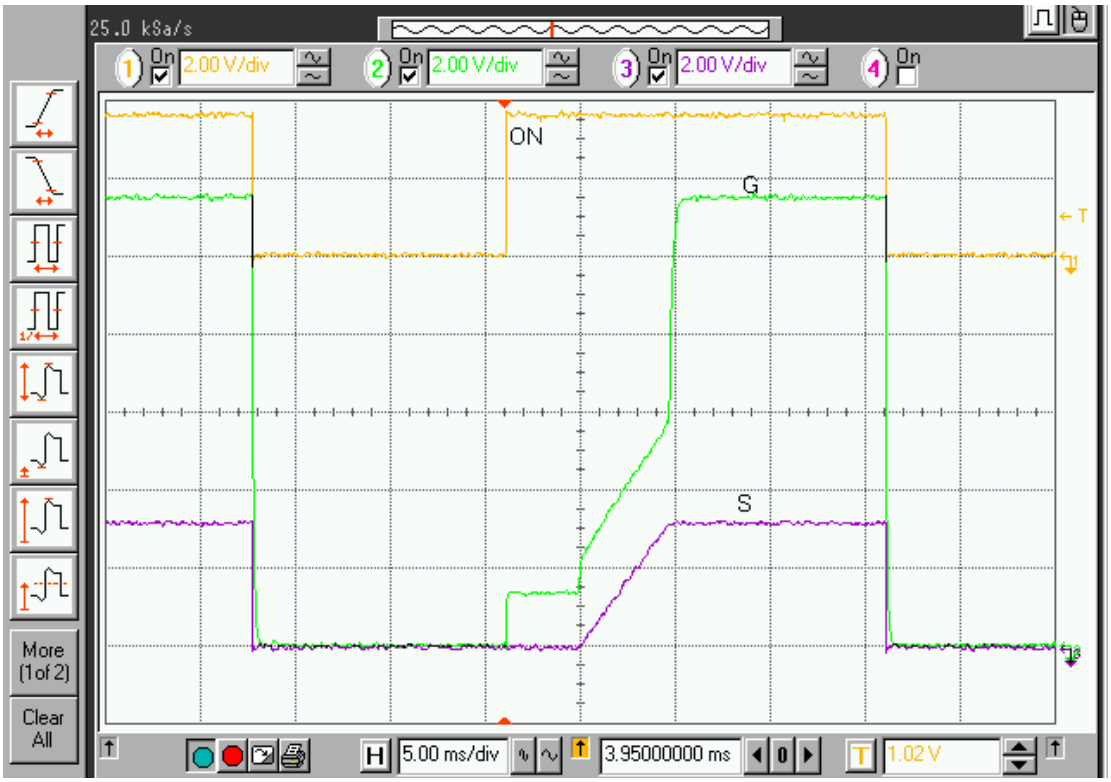
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Application Example

In a typical application, de-asserting ON (low) or asserting the low true Shut Down signal (SHDN#) turns off the external power N-FET. SHDN# is provided as an asynchronous override to the ON signal. When the FET is turned off, the voltage at the load is discharged through a resistor (typically 200 ohms) internal to the SLG55021 with the discharge current limited to a maximum of 10mA. When ON is asserted (high), gate voltage is not applied to the gate of the external power N-FET until after T_{DELAY} then the gate source (Vgs) voltage is ramped up to 11.5 V above the source voltage V_S at a slew rate determined by the internal slew rate control element internal to the SLG55021. Monotonic rise of Vs is maintained even as ID increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second SLG55021 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

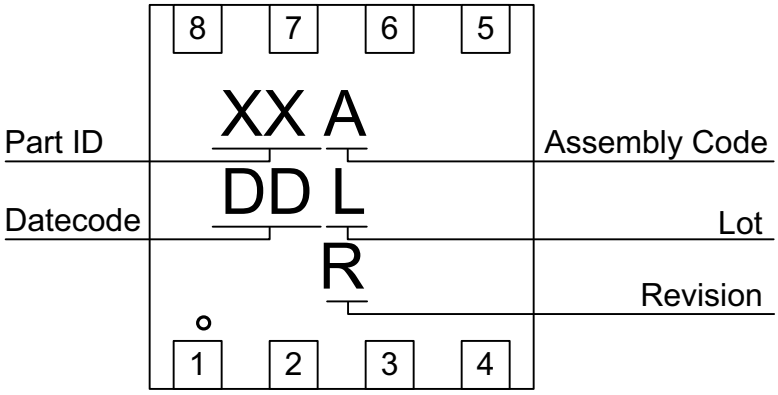
The devices will not operate if Vcc is below 3.5 V.

The waveforms shown illustrate the monotonic rise of the source voltage of a FET as gate voltage is controlled to accommodate for variations in load current as the voltage is applied.



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Package Top Marking System Definition

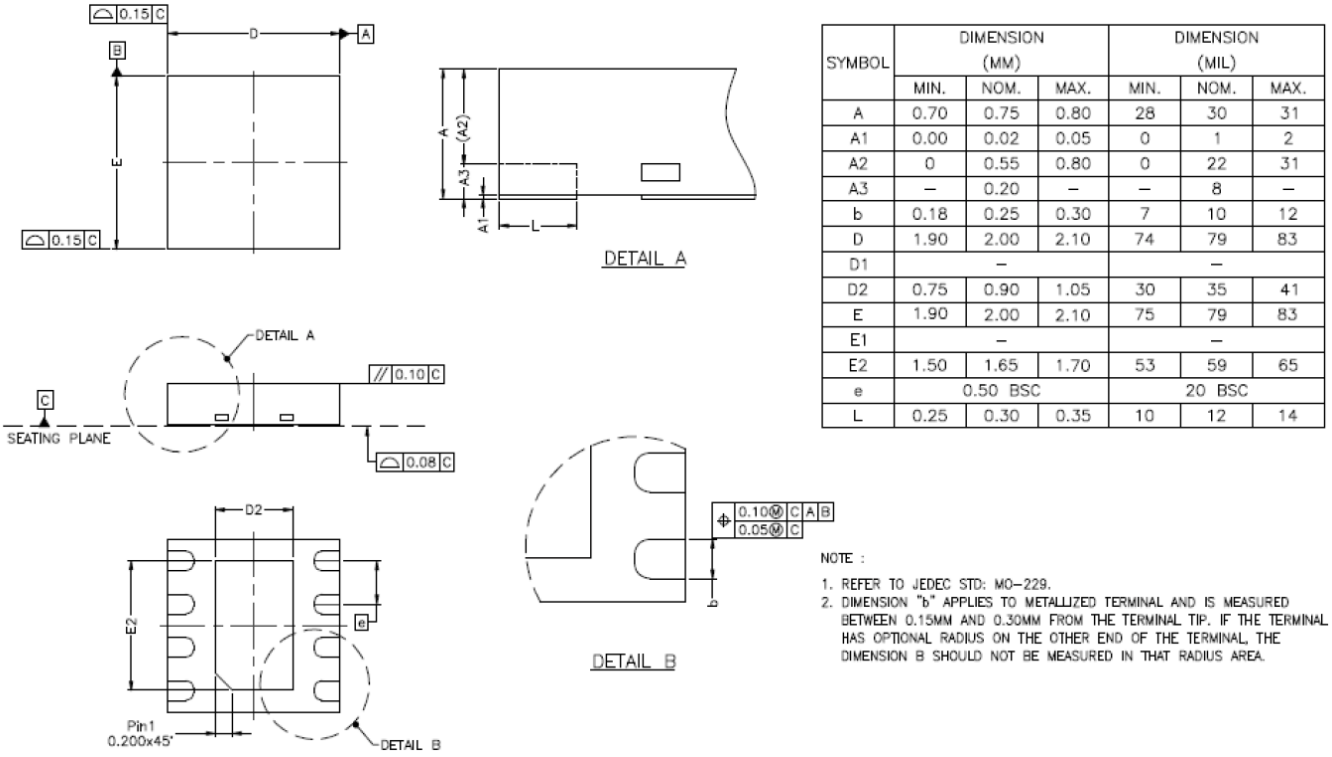


XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

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Package Drawing and Dimensions

8 Lead TDFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :
1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

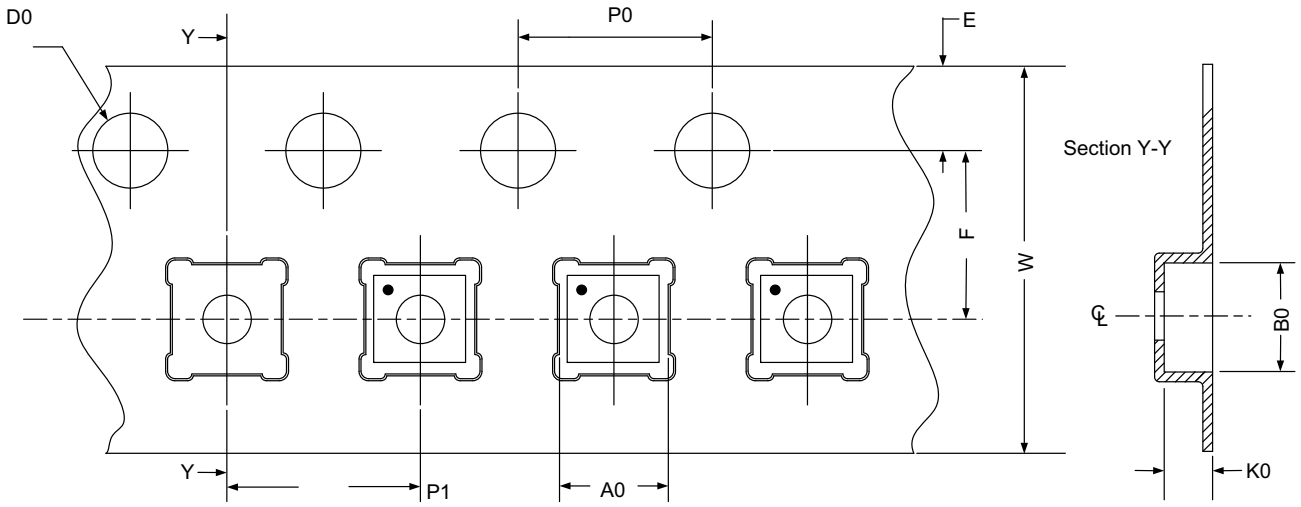
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Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.75	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm^3 (nominal). More information can be found at www.jedec.org.

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Revision History

Date	Version	Change
2/9/2022	1.05	Updated Company name and logo Fixed typos
7/10/2018	1.04	Updated style and formatting
7/27/2017	1.03	Added Pb-Free/Halogen Free/RoHS compliance Added MSL
9/26/2016	1.02	Removed TBD values Fixed typos

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