1.25V/1.35V/1.5V REGISTERING CLOCK DRIVER WITH PARITY TEST AND QUAD CHIP SELECT

SSTE32882KB1

Description

This 28-bit 1:2, or 26-bit 1:2 and 4-bit 1:1, registering clock driver with parity is designed for 1.25V, 1.35V and 1.5V V_{DD} operation.

All inputs are 1.25,1.35V and 1.5V CMOS compatible, except the reset ($\overline{RESET}$) and MIRROR inputs which are LVCMOS. All outputs are 1.25V,1.35V and 1.5V CMOS edge-controlled drivers optimized to drive single terminated 25Ω to 50Ω traces in DDR3 RDIMM applications, except the open-drain error ($\overline{ERROUT}$) output. The clock outputs (Yn and $\overline{Yn}$) and control net outputs QnCKEn, $\overline{QnCSn}$ and QnODTn are designed with a different strength and skew to compensate for different loading and equalize signal travel speed.

The SSTE32882KB1 has two basic modes of operation associated with the Quad Chip Select Enable ($\overline{QCSEN}$) input. When the $\overline{QCSEN}$ input pin is open (or pulled high), the component has two chip select inputs, $\overline{DCS0}$ and $\overline{DCS1}$, and two copies of each chip select output, $\overline{QACS0}$, $\overline{QACS1}$, $\overline{QBCS0}$ and $\overline{QBCS1}$. This is the "QuadCS disabled" mode. When the $\overline{QCSEN}$ input pin is pulled low, the component has four chip select inputs $\overline{DCS[3:0]}$, and four chip select outputs, $\overline{QCS[3:0]}$. This is the "QuadCS enabled" mode. Through the remainder of this specification, $\overline{DCS[n:0]}$ will indicate all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{QxCS[n:0]}$ will indicate all of the chip select outputs.

The SSTE32882KB1 includes a high-performance, low-jitter, low-skew buffer that distributes a differential clock input (CK and $\overline{CK}$) to four differential pairs of clock outputs (Yn and $\overline{Yn}$), and to one differential pair of feedback clock outputs (FBOUT and $\overline{FBOUT}$). The clock outputs are controlled by the input clocks (CK and $\overline{CK}$), the feedback clocks (FBIN and $\overline{FBIN}$), and the analog power inputs (AV_{DD} and AV_{SS}). When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

The SSTE32882KB1 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low. The data is either driven to the corresponding device outputs if exactly one of the $\overline{DCS[n:0]}$ input signals is driven low.

Based on the control register settings, the device can change its output characterisitics to match different DIMM net topologies. The timing can be changed to compensate for different flight time of signals within the target application. By disabling unused outputs the power consumption is reduced.

The SSTE32882KB1 accepts a parity bit from the memory controller on the parity (PAR_IN) input, compares it with the data received on the DIMM-independent data inputs (DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, and $\overline{DWE}$), and indicates whether a parity error has occurred on the open-drain $\overline{ERROUT}$ pin (active low). The convention is even parity; i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

The DIMM-dependent signals (DCKEn, DODTn, and $\overline{DCSn}$) are not included in the parity check computation.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power-up.

The SSTE32882KB1 is available in a 176-ball BGA with 0.65mm ball pitch in a 11 x 20 grid. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a-way that two devices can be placed back-to-back for four Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.

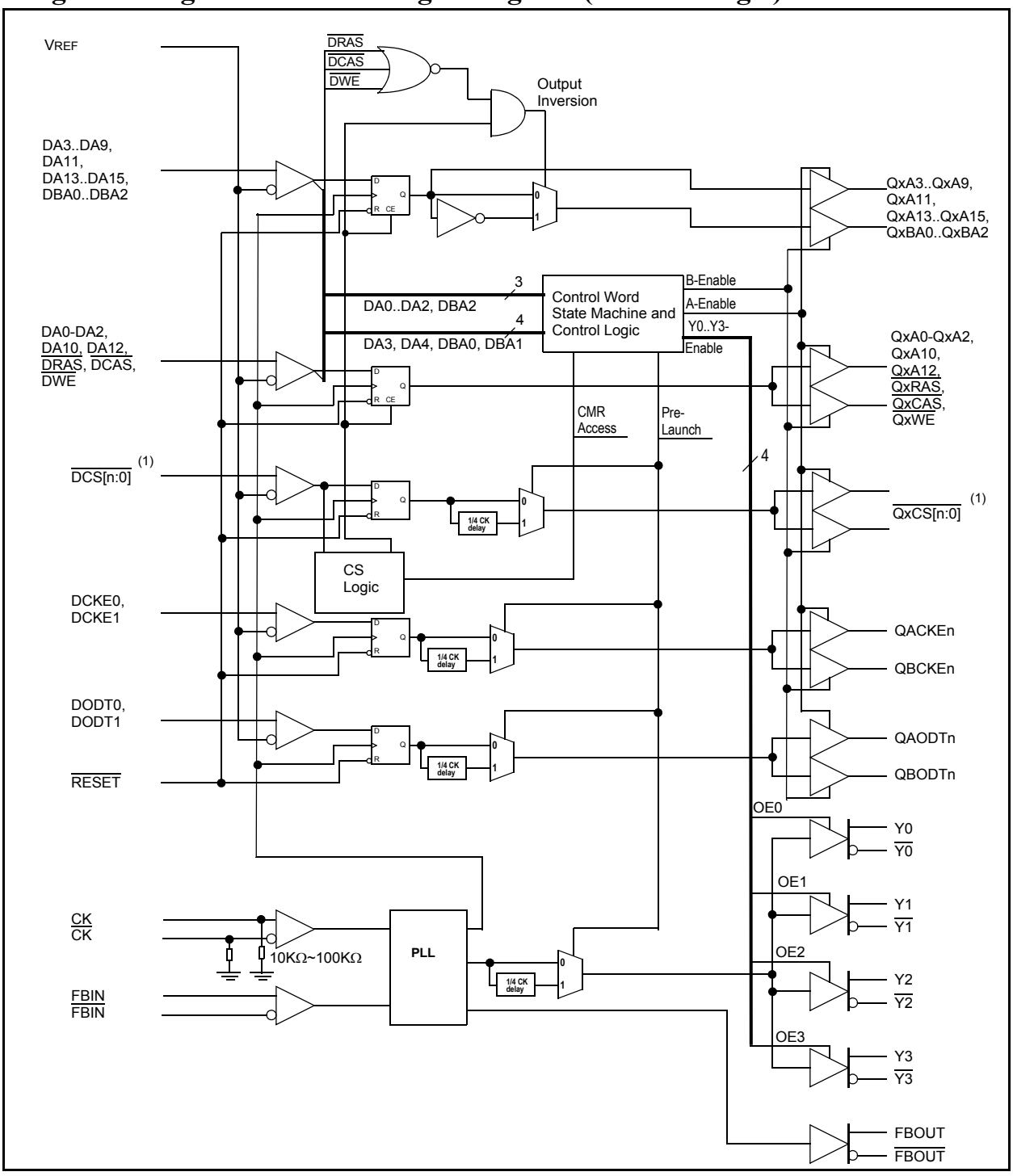
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Features

- Pinout optimizes DDR3 RDIMM PCB layout
- DDR3-800/1066/1333/1600/1866/2133 rate
- 1-to-2 Register Outputs and 1-to-4 Clock Pair Outputs support stacked DDR3 RDIMMs
- Phase Lock Loop clock driver for buffering one differential clock pair (CK and $\overline{CK}$) and distributing to four differential outputs
- Supports LVCMOS switching levels on the $\overline{RESET}$ and MIRROR inputs
- Checks priority on DIMM-independent data inputs
- Supports dynamic 1T/3T timing transaction and output inversion feature for improved timing performance during normal operations and MRS command pass-through
- Supports CKE Power Down operation modes
- Supports Quad Chip Select operation features
- $\overline{RESET}$ input disables differential input recievers, resets all registers, and disables all output drivers except $\overline{ERROUT}$ and QnCKEn
- Provides access to internal control words for configuring the device features and adapting in different RDIMM and system applications
- Latch-up performance exceeds 100mA
- ESD > 2000V per MIL-STD883, Method 3015; ESD > 200V using machine model (c = 200pF, R = 0)
- Available in 176 Ball Grid Array package

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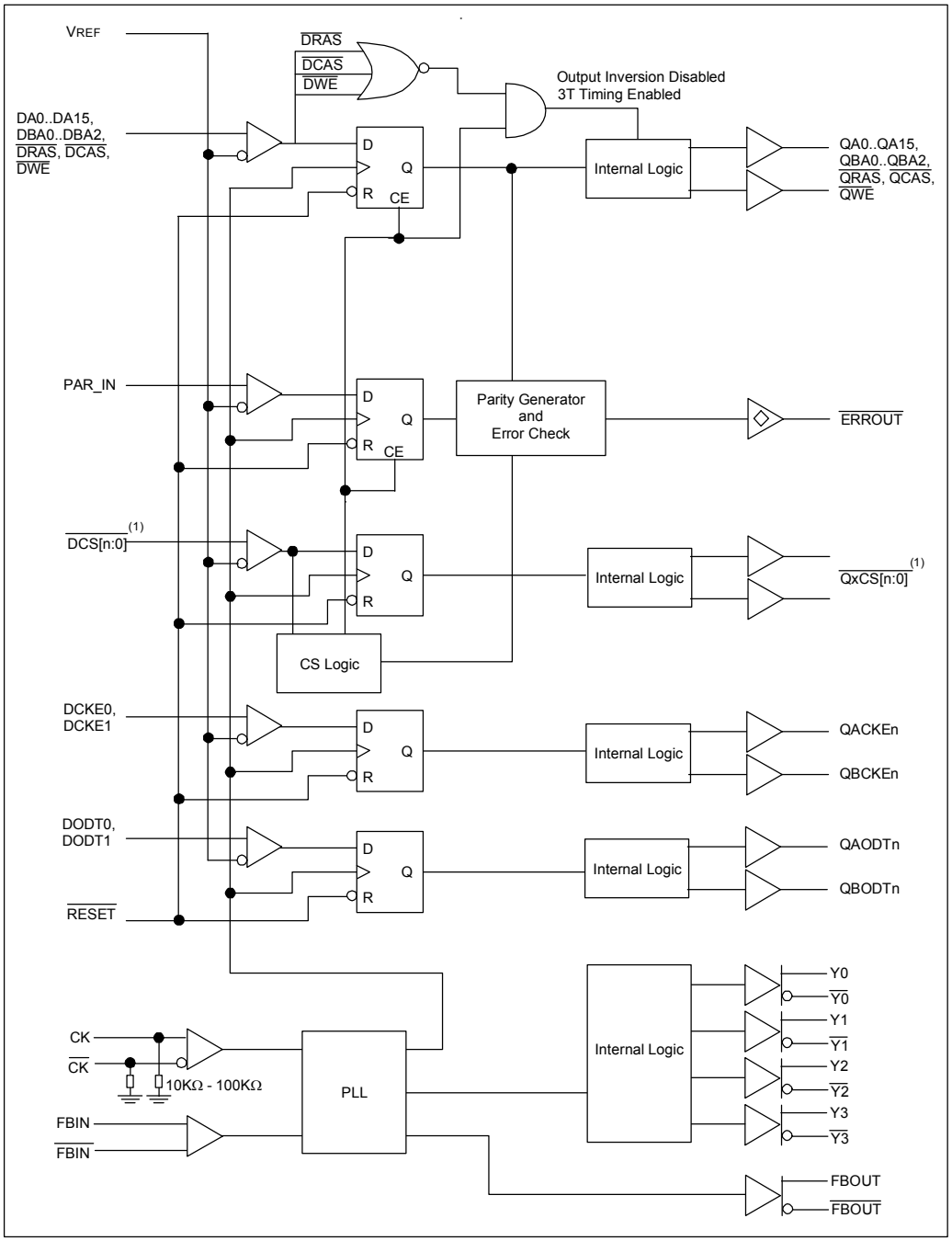
Block Diagram - Register and PLL Logic Diagram (Positive Logic)



1 $\overline{\text{DCS}}$[n:0] indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{\text{QxCS}}$[n:0] indicates all of the chip select outputs.

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Block Diagram - Parity Logic Diagram (Positive Logic)

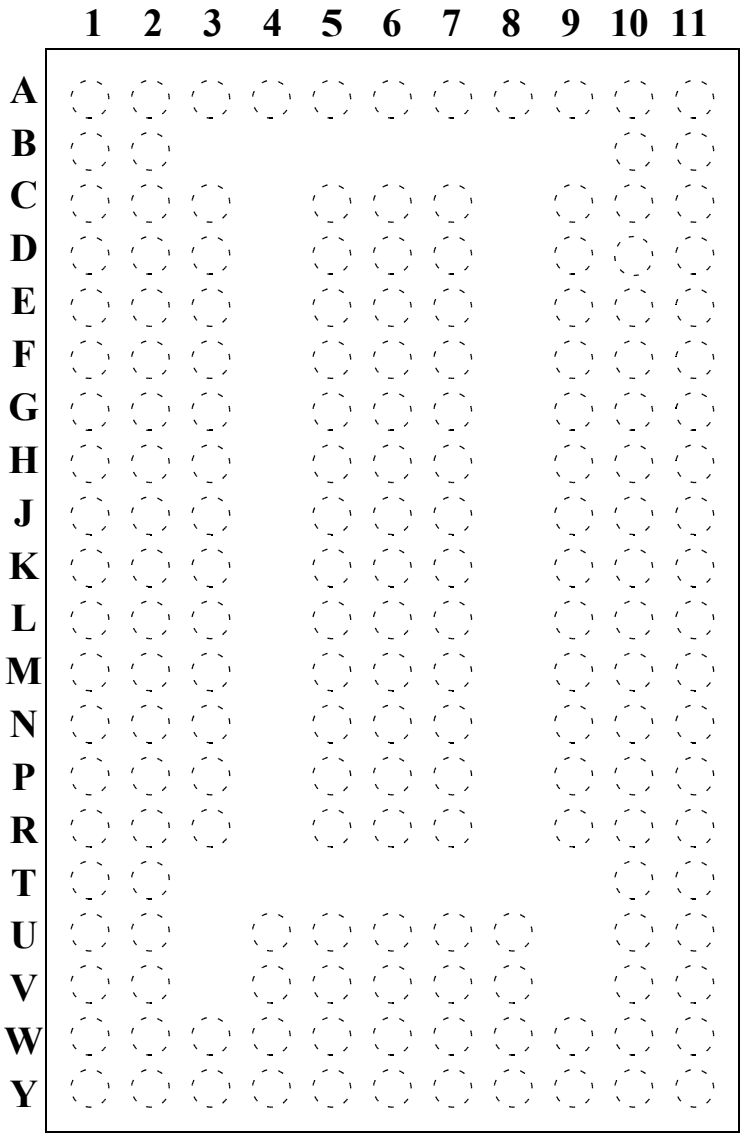


1 $\overline{\text{DCS[n:0]}}$ indicates all of the chip select inputs, where n=1 for QuadCS disabled, and n=3 for QuadCS enabled. $\overline{\text{QxCS[n:0]}}$ indicates all of the chip select outputs.

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Pinout Configuration

Package options include a 176-ball Thin-Profile Fine-Pitch BGA (TFBGA) with 0.65mm ball pitch, 11 x 20 grid, 8.0mm x 13.5mm. It uses the mechanical outline MO-246 variation F. The device pinout supports outputs on the outer two left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way that two devices can be placed back to back for 4 Rank modules while the data inputs share the same vias. Each input and output is located close to an associated no-ball position or on the outer two rows to allow low cost via technology combined with the small 0.65mm ball pitch.



176-ball Thin Profile Fine Pitch BGA (TFBGA) 11x20 Grid

Top View

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Pin Descriptions

The device has symmetric pinout with the inputs on the south side and the outputs on the east and west sides. This allows back-to-back mounting on both sides of the PCB if more than one device is needed.

Ball Assignment: MIRROR = LOW, $\overline{\text{QCSEN}}$ = HIGH or float

This table specifies the pinout for the SSTE32882KB1 in the front configuration (QuadCS mode disabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Also, balls Y2 and R6 are "do not use" balls reserved for $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ in the QuadCS mode, and must not be connected on the system. The device is designed to tolerate floating on these pins. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	RSVD	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	RSVD	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

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Ball Assignment: MIRROR = HIGH, $\overline{\text{QCSEN}}$ = HIGH or float

This table specifies the pinout for the SSTE32882KB1 in the back configuration (QuadCS mode disabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Also, balls Y10 and R6 are "do not use" balls reserved for $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ in the QuadCS mode, and must not be connected on the system. The device is designed to tolerate floating on these pins. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QACS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS1}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QACS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QBCS0}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	RSVD	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	RSVD	DA7

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Ball Assignment: MIRROR = LOW, $\overline{\text{QCSEN}}$ = LOW

This table specifies the pinout for the SSTE32882KB1 in the front configuration (QuadCS mode enabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA3		VSS	VSS	VSS		DA4	QBODT1	$\overline{\text{QBRAS}}$
R	DCKE1	DA14	DA15		DA5	$\overline{\text{DCS3}}$	DA2		DA1	DA10	DODT1
T	DCKE0	$\overline{\text{DCS0}}$								$\overline{\text{DCS1}}$	DODT0
U	DA12	DBA2		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DA13	$\overline{\text{DCAS}}$
V	DA9	DA11		Y1	PVSS	VSS	PVDD	Y0		$\overline{\text{DRAS}}$	$\overline{\text{DWE}}$
W	DA8	DA6	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA0	DBA0
Y	DA7	$\overline{\text{DCS2}}$	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	PAR_IN	DBA1

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Ball Assignment: MIRROR = HIGH, $\overline{\text{QCSEN}}$ = LOW

This table specifies the pinout for the SSTE32882KB1 in the back configuration (QuadCS mode enabled).

Balls A9 and W7 are reserved for future functions and must not be connected on the system. However, a ball on the device and connecting pad on the module are required in these locations. Blank spaces indicate no ball is populated at that gridpoint, and vias on the module may be located in these areas.

	1	2	3	4	5	6	7	8	9	10	11
A	QAA13	QAA8	$\overline{\text{QCSEN}}$	VSS	$\overline{\text{RESET}}$	MIRROR	$\overline{\text{ERROUT}}$	VSS	RSVD	QBA8	QBA13
B	QAA14	QAA7								QBA7	QBA14
C	QAA9	QAA6	VDD		VDD	VDD	VDD		VDD	QBA6	QBA9
D	QAA11	QAA5	VSS		VSS	VSS	VSS		VSS	QBA5	QBA11
E	QAA2	QAA4	VDD		VDD	VDD	VDD		VDD	QBA4	QBA2
F	QAA1	QAA3	VSS		VSS	VSS	VSS		VSS	QBA3	QBA1
G	QAA0	QABA1	VDD		VDD	VDD	VDD		VDD	QBBA1	QBA0
H	QAA12	QABA0	VSS		VSS	VSS	VSS		VSS	QBBA0	QBA12
J	QABA2	$\overline{\text{QCS1}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS3}}$	QBBA2
K	QAA15	QACKE0	VSS		VSS	VSS	VSS		VSS	QBCKE0	QBA15
L	$\overline{\text{QAWE}}$	$\overline{\text{QCS0}}$	VDD		VDD	VDD	VDD		VDD	$\overline{\text{QCS2}}$	$\overline{\text{QBWE}}$
M	QAA10	QACKE1	VSS		VSS	VSS	VSS		VSS	QBCKE1	QBA10
N	$\overline{\text{QACAS}}$	QAODT0	VDD		VDD	VDD	VDD		VDD	QBODT0	$\overline{\text{QBCAS}}$
P	$\overline{\text{QARAS}}$	QAODT1	DA4		VSS	VSS	VSS		DA3	QBODT1	$\overline{\text{QBRAS}}$
R	DODT1	DA10	DA1		DA2	$\overline{\text{DCS3}}$	DA5		DA15	DA14	DCKE1
T	DODT0	$\overline{\text{DCS1}}$								$\overline{\text{DCS0}}$	DCKE0
U	$\overline{\text{DCAS}}$	DA13		$\overline{\text{Y1}}$	PVSS	VDD	PVDD	$\overline{\text{Y0}}$		DBA2	DA12
V	$\overline{\text{DWE}}$	$\overline{\text{DRAS}}$		Y1	PVSS	VSS	PVDD	Y0		DA11	DA9
W	DBA0	DA0	$\overline{\text{FBIN}}$	$\overline{\text{Y3}}$	AVSS	$\overline{\text{CK}}$	RSVD	$\overline{\text{Y2}}$	$\overline{\text{FBOUT}}$	DA6	DA8
Y	DBA1	PAR_IN	FBIN	Y3	AVDD	CK	VREFCA	Y2	FBOUT	$\overline{\text{DCS2}}$	DA7

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Terminal Functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKEn, DODTn	1.25V/1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register function pins not associated with Chip Select.
Chip Select gated inputs	DAn, DBAn, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$	1.25V/1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register inputs, re-driven only when either chip select is LOW. If both chip selects are low the register maintains the state of the previous input clock cycle at its outputs
Chip Select inputs	$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	1.25V/1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes, and as such exactly one will be low when a valid address/command is present which should be re-driven.
	$\overline{\text{DCS2}}$, $\overline{\text{DCS3}}$	1.25V/1.35V/1.5V CMOS Inputs[1]	DRAM corresponding register Chip Select signals when QuadCS mode is enabled. $\overline{\text{DCS2}}$ and $\overline{\text{DCS3}}$ inputs are disabled when QuadCS mode is disabled.
Re-driven outputs	QxAn, QxBAn, $\overline{\text{QxCSn}}$, QxCKEn, QxODTn, $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, $\overline{\text{QxWE}}$	1.25V/1.35V/1.5V CMOS Outputs[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. x is A or B; outputs are grouped as A or B and may be enabled or disabled via RC0.
Parity input	PAR_IN	1.25V/1.35V/1.5V CMOS Inputs[1]	Input parity is received on pin PAR_IN and should maintain parity across the Chip Select Gated inputs (see above), at the rising edge of the input clock, one input clock cycle after corresponding data and one or both chip selects are LOW.
Parity error output	$\overline{\text{ERROUT}}$	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{\text{ERROUT}}$ will be active for two clock cycles, and delayed by 3 clock cycles to the corresponding input data
Clock inputs	CK, $\overline{\text{CK}}$	1.25V/1.35V/1.5V CMOS Inputs[1]	Differential master clock input pair to the PLL; has weak internal pull-down resistors (10KΩ~100KΩ) .
Feedback	FBIN, $\overline{\text{FBIN}}$	1.25V/1.35V/1.5V CMOS Inputs[1]	Feedback clock input
Clock	FBOUT, $\overline{\text{FBOUT}}$	1.25V/1.35V/1.5V CMOS Outputs[2]	Feedback clock output
Clock Outputs	Yn, $\overline{\text{Yn}}$	1.25V/1.35V/1.5V CMOS Outputs[2]	Re-driven Clock
Miscellaneous inputs	$\overline{\text{RESET}}$	CMOS[3]	Active low asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float. Once $\overline{\text{RESET}}$ becomes high the Q outputs get enabled and are driven LOW ($\overline{\text{ERROUT}}$ is driven high) until the first access has been performed. $\overline{\text{RESET}}$ also resets the $\overline{\text{ERROUT}}$ signal.
	MIRROR	CMOS[3]	Selects between two different ballouts for front or back operation. When the MIRROR input is high, the device Input Bus Termination (IBT) is turned off on all inputs, except the $\overline{\text{DCSn}}$ and DODTn inputs.
	$\overline{\text{QSCEN}}$	CMOS[3]	Enables the QuadCS mode. The $\overline{\text{QSCEN}}$ input has a weak internal pullup resistor (10KΩ - 100KΩ).

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Signal Group	Signal Name	Type	Description
Power	Vrefca[1]	Reference Voltage	Input reference voltage for the differential data inputs, VDD/2 (0.75V) nominal.
	Vdd	Register Power	Power supply voltage (Register)
	Vss	Register Ground	Ground (Register)
	AVdd	Analog Power	Analog supply voltage (PLL)
	AVss	Analog Ground	Analog ground (PLL)
	PVdd	PLL Power	Clock logic and clock output driver power supply (PLL)
	PVss	PLL Ground	Clock logic and clock output driver ground (PLL)
	RSVD	I/O	Reserved pins, must be left floating (PLL)

1 1.25V/1.35V/1.5V CMOS inputs use VREFCA as the switching point reference for these receivers.
2 These outputs are optimized for memory applications to drive DRAM inputs to 1.25V/1.35V/1.5V signaling levels.
3 Voltage levels according standard JESD8-11A, wide range, non terminated logic.

Function Table (Each Flip Flop) with QuadCS Mode Disabled

Inputs								Outputs[1]				
$\overline{RESET}$	DCS0	$\overline{DCS1}$	CK[2]	$\overline{CK}$[2]	ADDR[3]	CMD[4]	CTRL[5]	Qn[6]	QxCS0	$\overline{QxCS1}$	QxODTn	QxCKEn
H	L	L	↑	↓	Control Word	Control Word	Control Word	Q_0	H	H	Q_0	Q_0
H	X	X	L or H	H or L	X	X	X	Q_0	Q_0	Q_0	Q_0	Q_0
H	L	H	↑	↓	X	X	X	Follows Input	L	H	Follows Input	Follows Input
H	X	X	L	L	X	X	X	float	float	float	float	L
H	H	L	↑	↓	X	X	X	Follows Input	H	L	Follows Input	Follows Input
H	H	H	↑	↓	X or float	X or float	X	Q_0 or float[7]	H	H	Follows Input	Follows Input
L	X or float	X or float	X or float	X or float	X or float	X or float	X or float	float	float	float	float	L

1 Q_0 means the output does not change state.
2 It is illegal to hold both the CK and $\overline{CK}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{RESET}$ is driven HIGH.
3 ADDR = DA[15:0], DBA[2:0]
4 CMD = $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$.
5 CTRL = DODTn, DCKEn.
6 Qn = QxAn, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$, and QxBAn.
7 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state (Q_0) is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated.

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Function Table (Each Flip Flop) with QuadCS Mode Enabled

Inputs					Outputs			
$\overline{\text{RESET}}$	DCS[3:0]	CK[1]	$\overline{\text{CK}}$[1]	A/C/E[2]	Qn	QCS[3:0]	QxODTn	QxCKEn
H	LLHH	↑	↓	Control Word	No change	HHHH	No change	No change
H	HHLL							
H	LLLL							
H	XXXX	L or H	H or L	X	No change	No change	No change	No change
H	LHHH	↑	↓	Dn	Dn	LHHH	DODTn	DCKEn
H	HLHH	↑	↓	Dn	Dn	HLHH	DODTn	DCKEn
H	HHLH	↑	↓	Dn	Dn	HHLH	DODTn	DCKEn
H	HHHL	↑	↓	Dn	Dn	HHHL	DODTn	DCKEn
H	LHLH	↑	↓	Dn	Dn	LHLH	DODTn	DCKEn
H	HLLH	↑	↓	Dn	Dn	HLLH	DODTn	DCKEn
H	LHHL	↑	↓	Dn	Dn	LHHL	DODTn	DCKEn
H	HLHL	↑	↓	Dn	Dn	HLHL	DODTn	DCKEn
H	XXXX	L	L	X	float	float	float	L
H	HHHH	↑	↓	X	No change or float[3]	HHHH	DODTn	DCKEn
H	LLLH	↑	↓	X	Ilegal Input States			
H	LLHL							
H	LHLL							
H	HLLL							
L	X or float	X or float	X or float	X or float	float	float	float	L

1 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic high levels or static complementary logic levels (low and high) when $\overline{\text{RESET}}$ is driven high.

2 A/C/E = DA0..DA15, DBA0..DBA2, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, DODTn, DCKEn

3 Depending on Control Word RC0 Bit DA4. If RC0 DA4 is cleared, previous state is maintained. Address floating is disabled independent of control word RC0 once 3T timing is activated

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Parity, Low Power and Standby with QuadCS Mode Disabled

Inputs							Output
RESET	**DCS0**	**DCS1**	**CK[1]**	**$\overline{CK}$[1]**	**Σ of C/A[2]**	**PAR_IN[3]**	**ERROUT[4]**
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	H[5]
H	X	X	L or H	H or L	X	X	$\overline{ERROUT}_0$
H	X	X	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

1 It is illegal to hold both the CK and $\overline{CK}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{RESET}$ is driven HIGH.

2 C/A= DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$. Inputs DCKEn, DODTn, and $\overline{DCSn}$ are not included in this range. This column represents the sum of the number of C/A signals that are electrically HIGH.

3 PAR_IN arrives one clock cycle after the data to which it applies, $\overline{ERROUT}$ is issued three clock cycles after the failing data.

4 This transition assumes $\overline{ERROUT}$ is high at the crossing of CK going high and $\overline{CK}$ going low. If $\overline{ERROUT}$ is low, it stays latched low for exactly two clock cycles or until $\overline{RESET}$ is driven low.

5 Same three cycle delay for $\overline{ERROUT}$ is valid for the de-select phase (see diagram)

6 The system is not allowed to pull CK and $\overline{CK}$ low while $\overline{ERROUT}$ is asserted.

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Parity, Low Power and Standby with QuadCS Mode Enabled

Inputs						Output
$\overline{\text{RESET}}$	DCS[3:0]	CK[1]	$\overline{\text{CK}}$[1]	Σ of A/C[2]	PAR_IN[3]	$\overline{\text{ERROUT}}$[4]
H	LXXX XLXX XXLX XXXL	↑	↓	Even	L	H
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	L	L
H	LXXX XLXX XXLX XXXL	↑	↓	Even	H	L
H	LXXX XLXX XXLX XXXL	↑	↓	Odd	H	H
H	HHHH	↑	↓	X	X	H[5]
H	XXXX	L or H	H or L	X	X	$\overline{\text{ERROUT}}n_0$
H	XXXX	L	L	X	X	H[6]
L	X or floating	X or floating	X or floating	X or floating	X or floating	H

1 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic high levels or static complementary logic levels (low and high) when $\overline{\text{RESET}}$ is driven high.

2 A/C = DA0..DA15, DBA0..DBA2, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$. Inputs DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are not included in this range. This column represents the sum of the number of A/C signals that are electrically high.

3 PAR_IN arrivesone clock cycle afterdata to which it applies, $\overline{\text{ERROUT}}$ is issued three clock cycles after the failing data.

4 This transition assumes $\overline{\text{ERROUT}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{ERROUT}}$ is low, it stays latched low for exactly two clock cycles or until $\overline{\text{RESET}}$ is driven low.

5 Same three-cycle delay for $\overline{\text{ERROUT}}$ is valid for the de-select phase (see diagram)

6 The system is not allowed to pull CK and $\overline{\text{CK}}$ low while $\overline{\text{ERROUT}}$ is asserted.

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PLL Function Table

Inputs					Outputs				PLL
$\overline{\text{RESET}}$	AVDD	OEn[1]	CK[2]	$\overline{\text{CK}}$[2]	Yn	$\overline{\text{Yn}}$	FBOUT	$\overline{\text{FBOUT}}$	
L	X	X	X	X	Float	Float	Float	Float	Off
H	VDD nominal	L	L	H	L	H	L	H	On
H	VDD nominal	L	H	L	H	L	H	L	On
H	VDD nominal	H	L	H	Float	Float	L	H	On
H	VDD nominal	H	H	L	Float	Float	H	L	On
H	VDD nominal	X	L	L	Float	Float	Float	Float	Off
H	GND[3]	L	L	H	L	H	L	H	Bypassed/Off
H	GND[3]	L	H	L	H	L	H	L	Bypassed/Off
H	GND[3]	H	L	H	Float	Float	L	H	Bypassed/Off
H	GND[3]	H	H	L	Float	Float	H	L	Bypassed/Off
H	GND[3]	X	L	L	Float	Float	Float	Float	Bypassed/Off
H	X	X	H	H	Reserved				

1 The Output Enable (OEn) to disable the output buffer is not an input signal to the SSTE32882KB1, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver mode register.

2 It is illegal to hold both the CK and $\overline{\text{CK}}$ inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when $\overline{\text{RESET}}$ is driven HIGH.

3 This is a device test mode and all register timing parameters are not guaranteed.

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Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Symbol	Parameter	Conditions	Min	Max	Unit
AV_{DD}, PV_{DD}, V_{DD}	Supply voltage		–0.4	+1.975	V
V_I	Receiver input voltage[1]		–0.4	V_{DD} + 0.5	V
V_{REF}	Reference voltage		–0.4	V_{DD} + 0.5	V
V_O	Driver output voltage[1]		–0.4	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$		±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$		±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin			±100	mA
T_{STG}	Storage temperature		–65	+150	°C
$R\theta_{JA}$	Package Thermal Impedance, Junction-to-Ambient[2]	0m/s Airflow		43.8	°C/W
		1m/s Airflow		35.5	
$R\theta_{JB}$	Package Thermal Impedance, Junction-to-Board[2]			22	°C/W
$R\theta_{JC}$	Package Thermal Impedance, Junction-to-Case[2]			16.2	°C/W

1 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 1.975 V maximum.

2 The package thermal impedance is calculated in accordance with JESD51-2.

DC and AC Specifications

The SSTE32882KB1 parametric values are specified for the device default control word settings, unless otherwise stated. Note that RC10 setting does not affect any of the paramteric values.

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DC Specifications - Voltage

The SSTE32882KB1 parametric values are specified for the device default control word settings, unless otherwise stated. Note that the RC10 setting does not affect any of the parametric values.

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (1.5V Operation)		1.425	1.5	1.575	V
	DC Supply voltage (1.35V Operation)		1.282	1.35	1.451	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	V_{REF} + 175 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.5V Operation, DDR3-1866)	Data inputs[1]	V_{REF} + 135 mV	–	V_{DD} + 0.4	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	V_{REF} + 150 mV	–	V_{DD} + 0.2	V
	AC HIGH-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	V_{REF} + 135 mV	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (1.5V Operation, DDR3-800/1066/1333)	Data inputs[1]	–0.4	–	V_{REF} – 175 mV	V
	AC LOW-level input voltage (1.5V Operation, DDR3-1600)	Data inputs[1]	–0.4	–	V_{REF} – 150 mV	V
	AC LOW-level input voltage (1.5V Operation, DDR3-1866)	Data inputs[1]	–0.4	–	V_{REF} – 135 mV	V
	AC LOW-level input voltage(1.35V Operation, DDR3L-800/1066/1333)	Data inputs[1]	–0.2	–	V_{REF} – 150 mV	V
	AC LOW-level input voltage (1.35V Operation, DDR3L-1600)	Data inputs[1]	–0.2	–	V_{REF} – 135 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage(1.5V Operation)	Data inputs[1]	V_{REF} + 100 mV	–	V_{DD} + 0.4	V
	DC HIGH-level input voltage(1.35V Operation)	Data inputs[1]	V_{REF} + 90 mV	–	V_{DD} + 0.2	V
$V_{IL(DC)}$	DC LOW-level input voltage(1.5V Operation)	Data inputs[1]	–0.4	–	V_{REF} – 100 mV	V
	DC LOW-level input voltage(1.35V Operation)	Data inputs[1]	–0.2	–	V_{REF} – 90 mV	V
$V_{IH(CMOS)}$	HIGH-level input voltage	CMOS inputs[2]	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	CMOS inputs[2]	0	–	0.35 x VDD	V
$V_{IL\ (Static)}$	Static LOW-level input voltage[3]	CK, $\overline{CK}$,	-	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range(1.5V Operation, DDR3-800/1066/1333/1600)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 175 mV	0.5 x V_{DD}	0.5xV_{DD} + 175 mV	V
			0.5xV_{DD} - 200 mV[4]	0.5 x V_{DD}	0.5xV_{DD} + 200 mV[4]	V
	Differential input crosspoint voltage range(1.5V Operation, DDR3-1866)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180mV[5]	0.5 x V_{DD}	0.5xV_{DD} + 180mV[4]	V
	Differential input crosspoint voltage range(1.35V Operation, DDR3L-800/1066/1333/1600)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180 mV[6]	0.5 x V_{DD}	0.5xV_{DD} + 180 mV[5]	V
$V_{ID(AC)}$	Differential input voltage[7] (1.5V Operation, DDR3-800/1066/1333)	CK, $\overline{CK}$	350	–	V_{DD}	mV
	Differential input voltage[6](1.5V Operation, DDR3-1600)	CK, $\overline{CK}$	300	–	V_{DD}	mV
	Differential input voltage[6](1.5V Operation, DDR3-1866)	CK, $\overline{CK}$	270	–	V_{DD}	mV
	Differential input voltage[6](1.35V Operation, DDR3-800/1066/1333)	CK, $\overline{CK}$	300	–	V_{DD}	mV
	Differential input voltage[6] (1.35V Operation, DDR3-1600)	CK, $\overline{CK}$	270	–	V_{DD}	mV
I_{OH}	HIGH-level output current[8]	All outputs except $\overline{ERROUT}$	-11	–	–	mA
I_{OL}	LOW-level output current[8]	All outputs except $\overline{ERROUT}$	11	–	––	mA
I_{OL}	LOW-level output current	$\overline{ERROUT}$	25	–	–	mA
V_{OD}	Differential re-driven clock swing (1.5V Operation)	Yn, $\overline{Yn}$	500	–	V_{DD}	mV
	Differential re-driven clock swing (1.35V Operation)	Yn, $\overline{Yn}$	450	–	V_{DD}	mV

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Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{OX}	Differential Output Crosspoint Voltage (1.5V Operation)	Yn, $\overline{Yn}$	$0.5xV_{DD}$ – 100 mV	–	$0.5xV_{DD}$ + 100 mV	V
	Differential Output Crosspoint Voltage (1.35V Operation)	Yn, $\overline{Yn}$	$0.5xV_{DD}$ – 90 mV	–	$0.5xV_{DD}$ + 90 mV	V

1 $\overline{DCKE0/1}$, DODT0/1, DA0..DA15, DBA0..DBA2, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, PAR_IN, $\overline{DCS[1:0]}$ when $\overline{QCSEN}$ = HIGH, $\overline{DCS[3:0]}$ when $\overline{QCSEN}$ = LOW.
2 $\overline{RESET}$, MIRROR
3 This spec applies only when both CK and $\overline{CK}$ are actively driven LOW. It does not apply when $\overline{CK/CK}$ are floating.
4 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-275 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 4 V/ns.
5 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 4 V/ns.
6 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3.6 V/ns
7 VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$ See Diagram (Voltage waveforms; input clock)
8 Default settings

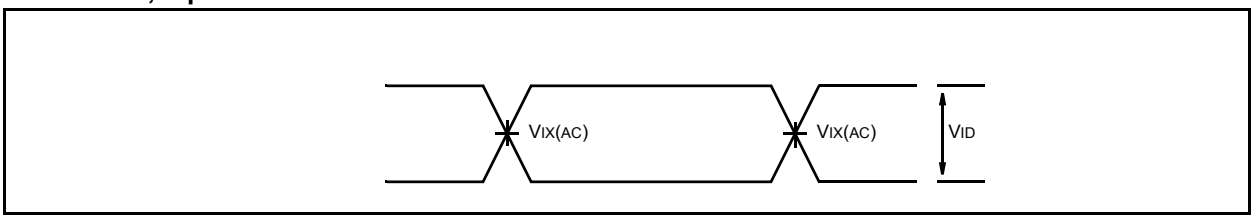
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DC Specifications - Voltage (DDR3U 1.25V)

Symbol	Parameter	Signals	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage (1.25V Operation)		1.19	1.25	1.31	V
V_{REF}	DC Reference voltage		0.49 x V_{DD}	0.50 x V_{DD}	0.51 x V_{DD}	V
V_{TT}	DC Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
$V_{IH(AC)}$	AC HIGH-level input voltage (1.25V Operation, DDR3U-800/1066/1333/1600)	Data inputs[1]	V_{REF} + 125 mV	–	V_{DD} + 0.2	V
$V_{IL(AC)}$	AC LOW-level input voltage (1.25V Operation, DDR3U-800/1066/1333/1600)	Data inputs[1]	–0.2	–	V_{REF} – 125 mV	V
$V_{IH(DC)}$	DC HIGH-level input voltage(1.25V Operation)	Data inputs[1]	V_{REF} + 90 mV	–	V_{DD} + 0.2	V
$V_{IL(DC)}$	DC LOW-level input voltage(1.25V Operation)	Data inputs[1]	–0.2	–	V_{REF} – 90 mV	V
$V_{IH(CMOS)}$	HIGH-level input voltage	CMOS inputs[2]	0.65 x VDD	–	V_{DD}	V
$V_{IL(CMOS)}$	LOW-level input voltage	CMOS inputs[2]	0	–	0.35 x VDD	V
$V_{IL\ (Static)}$	Static LOW-level input voltage[3]	CK, $\overline{CK}$,	-	–	0.35 x VDD	V
$V_{IX(AC)}$	Differential input crosspoint voltage range(1.25V Operation, DDR3U-800/1066/1333/1600)	CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	0.5xV_{DD} - 150 mV	0.5 x V_{DD}	0.5xV_{DD} + 150 mV	V
			0.5xV_{DD} - 180mV[4]	0.5 x V_{DD}	0.5xV_{DD} + 180 mV[4]	V
$V_{ID(AC)}$	Differential input voltage[5] (1.25V Operation, DDR3U-800/1066/1333/1600)	CK, $\overline{CK}$	250	–	V_{DD}	mV
I_{OH}	HIGH-level output current[6]	All outputs except $\overline{ERROUT}$	-11	–	–	mA
I_{OL}	LOW-level output current[6]	All outputs except $\overline{ERROUT}$	11	–	––	mA
I_{OL}	LOW-level output current	$\overline{ERROUT}$	25	–	–	mA
V_{OD}	Differential re-driven clock swing (1.25V Operation)	Yn, $\overline{Yn}$	400	–	V_{DD}	mV
V_{OX}	Differential Output Crosspoint Voltage (1.25V Operation)	Yn, $\overline{Yn}$	0.5xV_{DD} – 90 mV	–	0.5xV_{DD} + 90 mV	V

1 $\overline{DCKE}$0/1, DODT0/1, DA0..DA15, DBA0..DBA2, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, PAR_IN, $\overline{DCS}$[1:0] when $\overline{QCSEN}$ = HIGH, $\overline{DCS}$[3:0] when $\overline{QCSEN}$ = LOW.
2 $\overline{RESET}$, MIRROR
3 This spec applies only when both CK and $\overline{CK}$ are actively driven LOW. It does not apply when $\overline{CK}$/$\overline{CK}$ are floating.
4 Extended range for Vix is only allowed for clock (CK and $\overline{CK}$) and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-243 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3.6 V/ns.
5 VID is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$ See Diagram (Voltage waveforms; input clock)
6 Default settings

Voltage waveforms; input clock



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Thermal

Symbol	Parameter	DDR3/DDR3L/ DDR3U -800	DDR3/DDR3L /DDR3U -1066	DDR3/DDR3L/ DDR3U-1333	DDR3/DDR3L /DDR3U -1600	DDR3-1866	
$T_{case\ (max)}$	Case temperature[1]	109[2]	108[2]	106[2]	103[2]	101[2]	°C

1 Measurement procedure JESD51-2

2 This spec is meant to guarantee a Tj of 125C by the SSTE32882KB1 device. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a SSTE32882KB1 device shall not be higher than 125 °C.

DC Current Specifications

Operating Electrical Characteristics

Symbol	Parameter[1]	Conditions	Min	Typ[2]	Max	Unit
I_I	Input current	$\overline{RESET}$, MIRROR, V_I = V_{DD} or GND			±5	µA
	$\overline{QCSEN}$ input current	$\overline{QCSEN}$, V_I = V_{DD} or GND	-150		5	
I_{ID}	Input current	Data inputs[3], V_I = V_{DD} or GND			±5	µA
		CK, $\overline{CK}$[4]; V_I = V_{DD} or GND	-5		150	µA
I_{OH}	HIGH-level output current	Qn[5]	-11			mA
		Yn, $\overline{Yn}$, FBOUT, $\overline{FBOUT}$	-11			mA
I_{OL}	LOW-level output current	Qn[5]	11			mA
		Yn, $\overline{Yn}$, FBOUT, $\overline{FBOUT}$	11			mA
		$\overline{ERROUT}$	25			mA
I_{DD}[6]	Static standby current	$\overline{RESET}$ = GND and CK = $\overline{CK}$ = $V_{IL(AC)}$			5	mA
	Low-Power Static Operating	$\overline{RESET}$ = V_{DD} and CK = $\overline{CK}$ = $V_{IL(AC)}$, MIRROR = V_{DD}, RC8=x111,IBT OFF			15	mA
I_{CCD}	Dynamic operating -- input clock only; active outputs	$\overline{RESET}$ = V_{DD}, MIRROR = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, RC0[DBA0]=0, RC0[DBA1]=0, CK and $\overline{CK}$ switching 50% duty cycle, I_O = 0, $\overline{DCS0}$ = L, $\overline{DCS1}$ = H. V_{DD} = V_{DDMAX}		--		µA/MHz
	Dynamic operating -- per each data input	$\overline{RESET}$ = V_{DD}, MIRROR = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at one half clock frequency, 50% duty cycle; RC0[DBA0]=0, RC0[DBA1]=0, I_O = 0, $\overline{DCS0}$ = L, $\overline{DCS1}$ = H. V_{DD} = V_{DDMAX}		--		µA/Clock MHz/ D Input

1 The $\overline{RESET}$ and MIRROR inputs of the device must be held at valid voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{RESET}$ is LOW.

2 All typical values are at V_{DD} = 1.5V, T_A = 25°C.

3 DCKEn, DODTn, DAn, DBAn, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, DCSn, PAR_IN are measured while $\overline{RESET}$ is pulled LOW.

4 The CK and $\overline{CK}$ inputs have pull-down resistors in the range of 10KΩ to 100KΩ.

5 Qn = QxAn, $\overline{QxCSn}$, QxCKEn, QxODTn, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$, and QxBAn.

6 The supply current is measured as the total current consumptoion on the AV_{DD}, PV_{DD}, and V_{DD} supply current pins. Io= 0.

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Capacitance Values

Symbol	Parameter	Conditions	DDR3/DDR3L/DDR3U 800/1066/1333/1600			DDR3-1866			Unit
			Min	Typ	Max	Min	Typ	Max	
C_I	Input capacitance, Data inputs	see footnote[1,2]	1.5	-	2.5	1.5	-	2.2	pF
	Input capacitance, CK, $\overline{CK}$, FBIN, $\overline{FBIN}$	see footnote[1]	1.5	-	2.5	1.5	-	2.2	pF
C_O	Output capacitance, Re-driven and Clock Outputs	QxA0..QxA15, QxBA0..QxBA2, $\overline{QxCS0/1}$, $\overline{QxCKE0/1}$, $\overline{QxODT0/1}$, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$, Y0, $\overline{Y0}$.. Y3, $\overline{Y3}$	1	-	2				pF
$C_{I\Delta}$	Delta capacitance over all inputs		-	-	0.5		-	0.5	pF
C_{IR}	Input capacitance, $\overline{RESET}$, MIRROR, $\overline{QCSEN}$	$V_I = V_{DD}$ or GND; V_{DD} = 1.5 V	-	-	3		-	3	pF

1 This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147 ("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA)") with VDD, VSS, AVDD, AVSS, PVDD, PVSS, V_{REF} applied and all other pins (except the pin under test) floating. Input capacitance are measured with the device default settings when MIRROR=Low.

2. Data Inputs are DCKE0/1, DODT0/1, DA0..DA15, DBA0..DBA2, $\overline{DRAS}$, $\overline{DWE}$, PAR_IN, $\overline{DCS}$[1:0], when $\overline{QCSEN}$ = HIGH, $\overline{DCS}$[3:0] when $\overline{QCSEN}$ =LO

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Timing Requirements

Symbol	Parameter	Conditions	DDR3/DDR3L-800/ 1066/1333		DDR3/DDR3L-1600		DDR3-1866		Unit
			Min	Max	Min	Max	Min	Max	
f_{CLOCK}	Input Clock Frequency	Application Frequency[1]	300	670	300	810	300	945	MHz
f_{TEST}	Input Clock Frequency	Test Frequency[2]	70	300	70	300	70	300	MHz
t_{CH}/t_{CL}	Pulse Duration, CK, $\overline{CK}$ HIGH or LOW		0.4		0.4		0.4		t_{CK}[3]
t_{ACT}	Inputs active time before $\overline{RESET}$ is taken HIGH[4]	DCKE0/1 = LOW and $\overline{DCS[n:0]}$ = HIGH	8		8		8		t_{CK}[3]
t_{MRD}	Command word to command word programming delay	Number of clock cycles between two command programming accesses	8		8		8		t_{CK}[3]
t_{INDIS}	Input Buffers disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling; RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1	4	1	4	1	4	t_{CK}[3]
t_{QDIS}	Output Buffers Hi-Z after QxCKEn is driven LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling; RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1.5	1.5	1.5	1.5	1.5	1.5	t_{CK}[3]
t_{CKOFF}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/$\overline{CK}$ are driven low	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling	5		5		5		t_{CK}[3]
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK/$\overline{CK}$ = LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = LOW	2		2		2		t_{CK}[3]
tFixedoutputs	Static Register Output after DCKE0 or DCKE1 is HIGH at the input (exit from Power Saving state)	RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1	3	1	4	1	4	t_{CK}[3]
t_{SU}	Setup Time[5]	Input valid before CK/$\overline{CK}$	100		50		40		ps
t_{H}	Hold Time[6]	Input to remain valid after CK/$\overline{CK}$	175		125		75		ps

1 All specified timing parameters apply.
2 Timing parameters specified for frequency band 2 apply.
3 Clock cycle time.
4 This parameter is not necessarily production tested (see the “Voltage Waveforms for Setup and Hold Times–Hold Time Calculation”figure below).

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5 Setup (t_{SU}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and first crossing of $V_{IH(AC)}$ min. Setup (t_{SU}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value .

6 Hold (t_H) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)MAX}$ and the first crossing of $V_{REF(DC)}$. Hold (t_H) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)MIN}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(DC)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(DC)}$ level is used for derating value.

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Timing Requirements (DDR3U 1.25V)

Symbol	Parameter	Conditions	DDR3U-800/ 1066/1333		DDR3U-1600		Unit
			Min	Max	Min	Max	
f_{CLOCK}	Input Clock Frequency	Application Frequency[1]	300	670	300	810	MHz
f_{TEST}	Input Clock Frequency	Test Frequency[2]	70	300	70	300	MHz
t_{CH}/t_{CL}	Pulse Duration, CK, $\overline{CK}$ HIGH or LOW		0.4		0.4		t_{CK}[3]
t_{ACT}	Inputs active time before $\overline{RESET}$ is taken HIGH[4]	DCKE0/1 = LOW and $\overline{DCS[n:0]}$ = HIGH	8		8		t_{CK}[3]
t_{MRD}	Command word to command word programming delay	Number of clock cycles between two command programming accesses	8		8		t_{CK}[3]
t_{INDIS}	Input Buffers disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling; RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1	4	1	4	t_{CK}[3]
t_{QDIS}	Output Buffers Hi-Z after QxCKEn is driven LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling; RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1.5	1.5	1.5	1.5	t_{CK}[3]
t_{CKOFF}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK/$\overline{CK}$ are driven low	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = Toggling	5		5		t_{CK}[3]
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK/$\overline{CK}$ = LOW	DCKE[1:0] = LOW; $\overline{RESET}$ = HIGH; CK/$\overline{CK}$ = LOW	2		2		t_{CK}[3]
tFixedoutputs	Static Register Output after DCKE0 or DCKE1 is HIGH at the input (exit from Power Saving state)	RC9[DBA1] = 1 and RC9[DBA0] = 0 or 1	1	3	1	3	t_{CK}[3]
t_{SU}	Setup Time[5]	Input valid before CK/$\overline{CK}$	100		50		ps
t_H	Hold Time[6]	Input to remain valid after CK/$\overline{CK}$	175		125		ps

1 All specified timing parameters apply.
2 Timing parameters specified for frequency band 2 apply.
3 Clock cycle time.
4 This parameter is not necessarily production tested (see the “Voltage Waveforms for Setup and Hold Times–Hold Time Calculation” figure below).

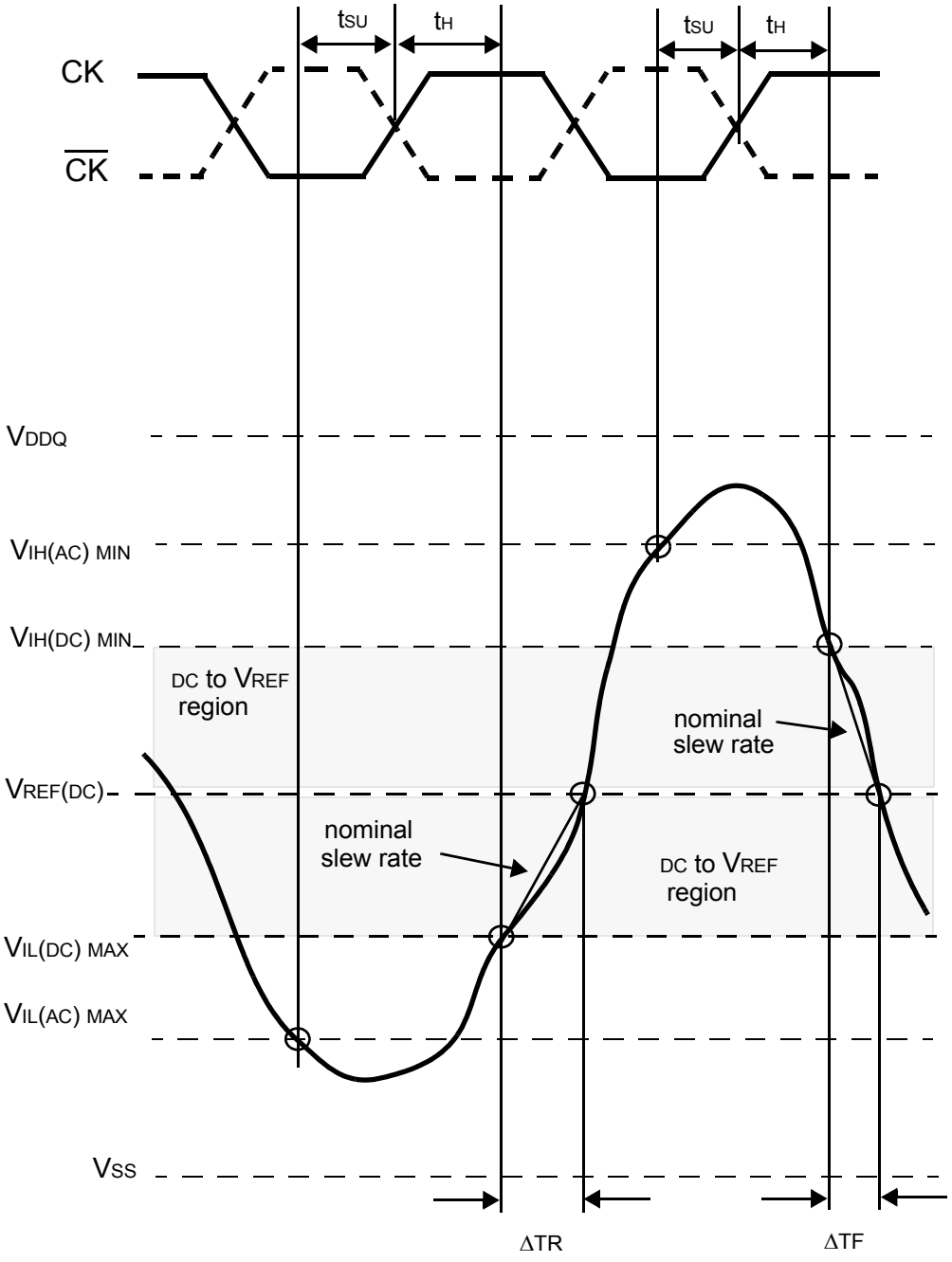
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5 Setup (t_{SU}) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and first crossing of $V_{IH(AC)}$ min. Setup (t_{SU}) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value .

6 Hold (t_H) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(DC)MAX}$ and the first crossing of $V_{REF(DC)}$. Hold (t_H) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(DC)MIN}$ and the first crossing of $V_{REF(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(DC)}$ region' use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(DC)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(DC)}$ level is used for derating value.

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Voltage Waveforms for Setup and Hold Times–Hold Time Calculation

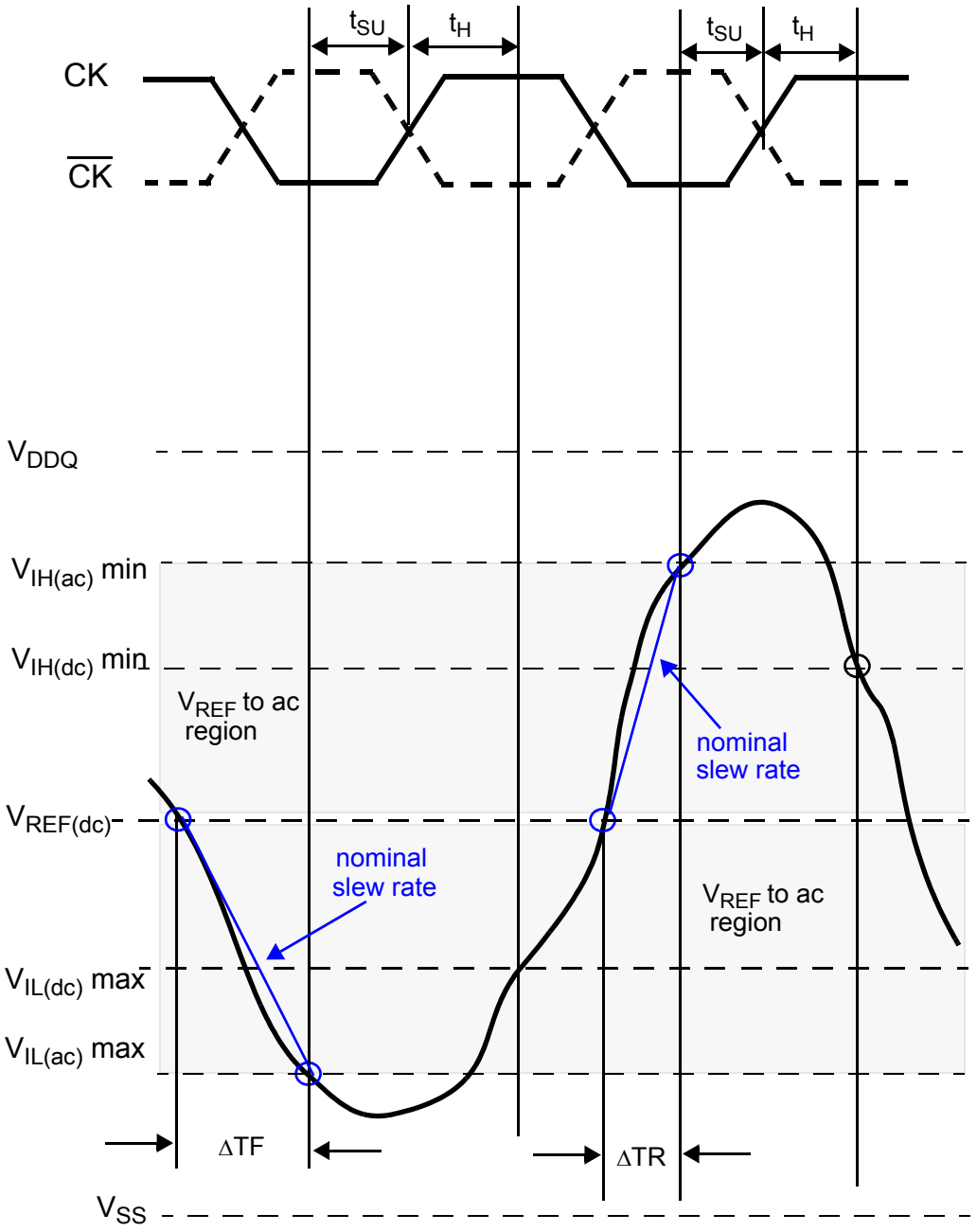


$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(DC)} - V_{IL(DC)\ MAX}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(DC)\ MIN} - V_{REF(DC)}}{\Delta TF}$$

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Voltage Waveforms for Setup and Hold Times–Setup Time Calculation



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

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AC Specifications - Output Timing Requirements

Symbol	Parameter[1]	Conditions	DDR3/DDR3L -800/ 1066/1333		DDR3/DDR3L -1600		DDR3-1866		Unit
			Min	Max	Min	Max	Min	Max	
t_{PDM}	Propagation delay, single-bit switching (1.5V operation)	CK/$\overline{CK}$ to output[2]	0.65	1.0	0.65	1.0	0.65	1.0	ns
	Propagation delay, single-bit switching (1.35V operation)[3]		0.65	1.2	0.65	1.2			
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn/$\overline{Yn}$ (falling edge) to output float[4]	0.5+ tQSK1(min)		0.5+ tQSK1(min)		0.5+ tQSK1(min)		ps
	Output disable time (3/4-Clock pre-launch)		0.25+ tQSK2(min)		0.25+ tQSK2(min)		0.25+ tQSK2(min)		
t_{EN}	Output enable time (1/2-Clock pre-launch)	Yn/$\overline{Yn}$ (falling edge) output driving	0.5- tQSK1(max)		0.5- tQSK1(max)		0.5- tQSK1(max)		ps
	Output enable time (3/4-Clock pre-launch)		0.75- tQSK2(max)		0.75- tQSK2(max)		0.75- tQSK2(max)		

1 See “Qn and Yn Load Circuit” diagram.

2 See “Propagation Delay Timing” diagram below.

3 t_{PDM} range (t_{PDM_max} - t_{PDM_min}) must remain as 350 ps. For example, if t_{PDM_min} for a device is 0.65 ns, it’s t_{PDM_max} cannot be more than 1.0 ns, If t_{PDM_max} for a device is 1.2 ns, it’s t_{PDM_min} cannot be less than 0.85 ns.

4 See “Voltage Waveforms Address Floating” diagram.

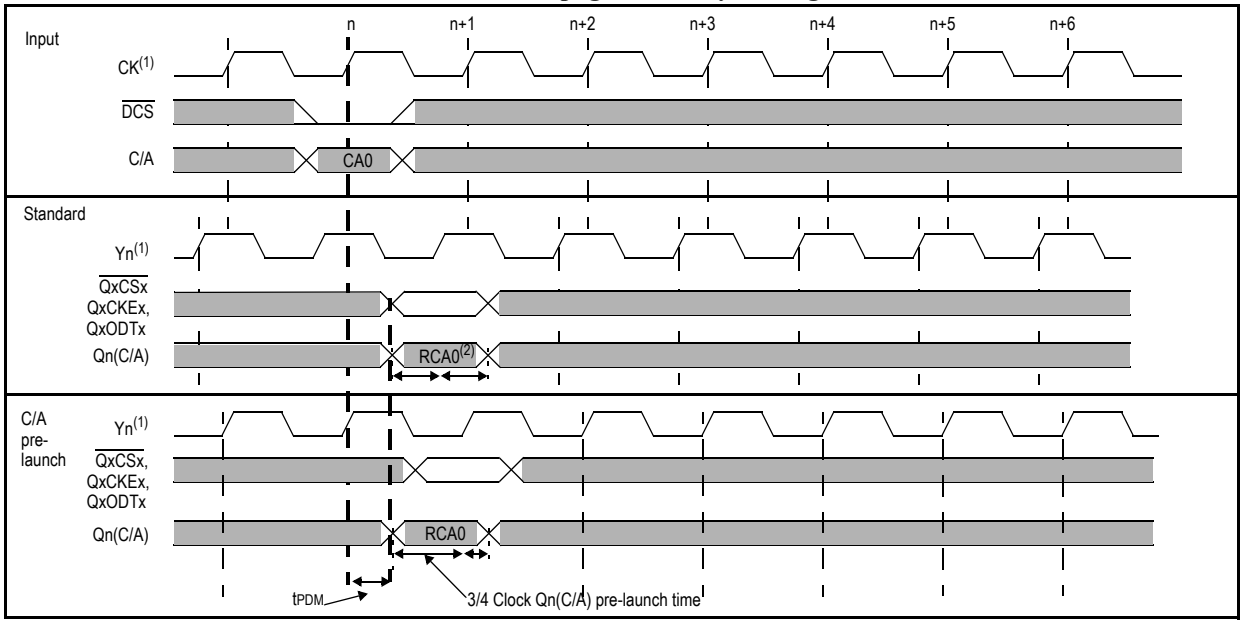
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AC Specifications - Output Timing Requirements (DDR3U 1.25V)

Symbol	Parameter[1]	Conditions	DDR3U-800/ 1066		DDR3U -1333/1600		Unit
			Min	Max	Min	Max	
t_{PDM}	Propagation delay, single-bit switching (1.25V operation)	CK/$\overline{CK}$ to output[2]	0.65	1.35	0.65	1.35	ns
t_{DIS}	Output disable time (1/2-Clock pre-launch)	Yn/$\overline{Yn}$ (falling edge) to output float[3]	0.5+ tQSK1(min)		0.5+ tQSK1(min)		ps
t_{EN}	Output enable time (1/2-Clock pre-launch)	Yn/$\overline{Yn}$ (falling edge) output driving	0.5- tQSK1(max)		0.5- tQSK1(max)		ps

1 See "Qn and Yn Load Circuit" diagram.
2 See "Propagation Delay Timing" diagram below.
3 See "Voltage Waveforms Address Floating" diagram.

Propagation Delay Timing



1 $\overline{CK}$ and $\overline{Yn}$ left out for better visibility.
2 RCA0 is re-driven command address signal based on input CA0.

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Output Buffer Characteristics - edge rates over specified operating free-air temperature range

Symbol	Parameter	Conditions	DDR3DDR3L-800/1066/1333		DDR3/DDR3L-1600		DDR3-1866		Unit
			Min	Max	Min	Max	Min	Max	
dV/dt_r	rising edge slew rate [1] (1.5V operation)		2	7	2.0	5.5	2.0	5.0	V/ns
	rising edge slew rate [1] (1.35V operation)		1.8	5.0	1.8	5.0	-	-	
dV/dt_f	falling edge slew rate [1] (1.5V operation)		2	7	2.0	5.5	2.0	5.0	V/ns
	falling edge slew rate [1] (1.35V operation)		1.8	5.0	1.8	5.0	-	-	
dV/dt_D[2]	absolute difference between dV/dt_r and dV/dt_f[1]		–	1	–	1	-	1	V/ns

1 Measured into test load at default register setting except RC3, RC4 and RC5 which are set according to the drive strength to be measured.

2 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

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Clock Driver Characteristics at Application Frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR3/ DDR3-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		DDR3-1866		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{JIT(CC+)}$	Cycle-to-cycle period jitter		0	40	0	40	0	40	0	30	0	25	ps
$t_{JIT(CC-)}$	Cycle-to-cycle period jitter		-40	0	-40	0	-40	0	-30	0	-25	0	ps
t_{STAB}	Stabilization time		-	6	-	6	-	6	-	6	-	5	µs
t_{FDYN}	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	-30	30	ps
t_{CKSK}	Fractional Clock Output skew[1]		-	15	-	15	-	15	-	10	-	10	ps
$t_{JIT(PER)}$	Yn Clock Period jitter		-40	40	-40	40	-40	40	-30	30	-25	25	ps
$t_{JIT(HPER)}$	Half period jitter		-50	50	-50	50	-50	50	-40	40	-35	35	ps
$t_{PWH/PWL}$	Yn pulse width HIG/LOW duration[3]	$t_{PW} = 1/2t_{CK} - It_{JIT}(hper)minI$ to $1/2t_{CK} - It_{JIT}(hper)maxI$	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	0.501	0.571	ns
t_{QSK1}[2]	Qn Output to Yn clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion enabled	-150	250	-150	250	-150	250	-140	140	-135	125	ps
		Output Inversion disabled	-150	350	-150	350	-150	350	-140	240	-135	225	
t_{QSK2}[4]	Qn Output to Yn clock tolerance (3/4 Clock Pre-Launch)	Output Inversion enabled	-150	250	-150	250	-150	250	-140	140	-135	125	ps
		Output Inversion disabled	-150	350	-150	350	-150	350	-140	240	-135	225	
t_{STAOFF}	Average delay through the register beween the input clock and output clock over *"n"* cycles[5]. (1.5V operation)	Standard 1/2-Clock Pre-Launch $t_{STAOFF} = t_{PDM} + 1/2\ t_{CK}$	1.9	2.25	1.59	1.94	1.40	1.75	1.28	1.63	1.19	1.54	ns
		3/4 Clock Pre-Launch $t_{STAOFF} = t_{PDM} + 3/4\ t_{CK}$	2.53	2.88	2.06	2.41	1.77	2.12	1.59	1.94	1.45	1.80	ns
	Average delay through the register beween the input clock and output clock[5]. (1.35V operation)	Standard 1/2-Clock Pre-Launch $t_{STAOFF} = t_{PDM} + 1/2\ t_{CK}$	1.90	2.45	1.59	2.14	1.40	1.95	1.28	1.83	-	-	ns
		3/4 Clock Pre-Launch $t_{STAOFF} = t_{PDM} + 3/4\ t_{CK}$	2.53	3.08	2.06	2.61	1.77	2.32	1.59	2.14	-	-	ns

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Symbol	Parameter	Conditions	DDR3/ DDR3-800		DDR3/ DDR3L-1066		DDR3/ DDR3L-1333		DDR3/ DDR3L-1600		DDR3-1866		Unit
t_{DYNOFF}[6]	Maximum variation in delay between the input & output clock		-	160	-	130	-	110	-	90	-	70	ps
	SSC modulation frequency		30	33	30	33	30	33	30	33	30	33	kHz
	SSC clock input frequency deviation		0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
t_{BAND}	PLL Loop bandwidth (-3 dB from unity gain)		25[7]		30[7]		35[7]		40[7]	-	45[7]	-	MHz

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between Y0/$\overline{Y0}$ and Y2/$\overline{Y2}$, as well as right side of the clock pairs between Y1/$\overline{Y1}$ and Y3/$\overline{Y3}$. This is not a tested parameter and has to be considered as a design goal only.
2. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See "Qn Output Skew for Standard 1/2-Clock Pre-Launch"). The output clock jitter is not included in this skew. The Qn output can either be early or late. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO).
3. The parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on t_{PW}.
4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See "Qn Output Skew for Standard 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. The Qn output can either be early or late. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO).
5. This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. t_{STAOFF} may vary by the amount of t_{DYNOFF} based on voltage and temperature drift as well as tracking error and jitter. Including this variation t_{STAOFF} may not exceed the limits set by $t_{STAOFF(MIN)}$ and $t_{STAOFF(MAX)}$.
6. See "Measurement Requirement for t_{STAOFF} and t_{DYNOFF}".
7. Implies a -3 dB bandwidth and jitter peaking of 3 dB.

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Clock Driver Characteristics at Application Frequency (frequency band 1)(DDR3U 1.25V)

Symbol	Parameter	Conditions	DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{JIT(CC+)}$	Cycle-to-cycle period jitter		0	40	0	40	0	40	0	30	ps
$t_{JIT(CC-)}$	Cycle-to-cycle period jitter		-40	0	-40	0	-40	0	-30	0	ps
t_{STAB}	Stabilization time		-	6	-	6	-	6	-	6	µs
t_{FDYN}	Dynamic phase offset		-50	50	-50	50	-50	50	-40	40	ps
t_{CKSK}	Fractional Clock Output skew[1]		-	15	-	15	-	15	-	10	ps
$t_{JIT(PER)}$	Yn Clock Period jitter		-40	40	-40	40	-40	40	-30	30	ps
$t_{JIT(HPER)}$	Half period jitter		-50	50	-50	50	-50	50	-40	40	ps
$t_{PWH/PWL}$	Yn pulse width HIG/LOW duration[2]	$t_{PW} = 1/2t_{CK} - It_{JIT}(hper)minI$ to $1/2t_{CK} - It_{JIT}(hper)maxI$	1.200	1.300	0.888	0.988	0.700	0.800	0.585	0.665	ns
t_{QSK1}[2]	Qn Output to Yn clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion enabled	-100	200	-100	200	-100	200	-100	100	ps
		Output Inversion disabled	-100	300	-100	300	-100	300	-100	200	
t_{STAOFF}	Average delay through the register beween the input clock and output clock.[5]. (1.25V operation)	Standard 1/2-Clock Pre-Launch $t_{STAOFF} = t_{PDM} + 1/2\ t_{CK}$	1.9	2.60	1.59	1.29	1.40	2.10	1.28	1.98	ns
t_{DYNOFF}[6]	Maximum variation in delay between the input & output clock		-	160	-	130	-	110	-	90	ps
	SSC modulation frequency		30	33	30	33	30	333	30	33	kHz
	SSC clock input frequency deviation		0.00	-0.5	0.00	-0.5	0.00	-0.5	0.00	-0.5	%
t_{BAND}	PLL Loop bandwidth (-3 dB from unity gain)		25[7]		30[7]		35[7]		40[7]	-	MHz

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See “Clock Output (Yn) Skew”). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to left side clock pairs between Y0/$\overline{Y0}$ and Y2/$\overline{Y2}$, as well as right side of the clock pairs between Y1/$\overline{Y1}$ and Y3/$\overline{Y3}$. This is not a tested parameter and has to be considered as a design goal only.

2. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See “Qn Output Skew for Standard 1/2-Clock Pre-Launch”). The output clock jitter is not included in this skew. The Qn output can either be early or late. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO).

3. The parameter is a measure of the output clock pulse width HIGH/LOW. The output clock duty cycle can be calculated based on t_{PW}.

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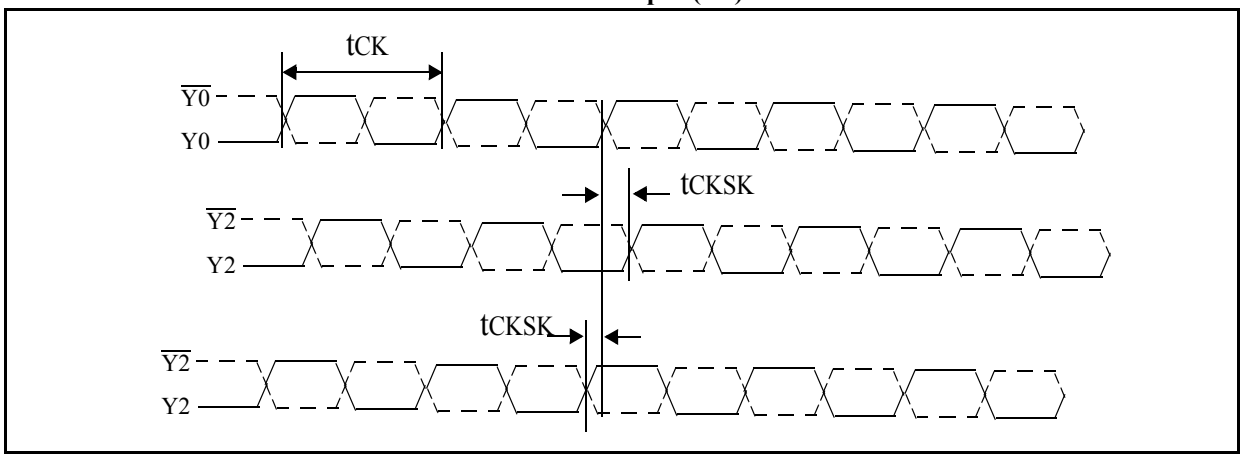
4. This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See "Qn Output Skew for Standard 3/4-Clock Pre-Launch"). The output clock jitter is not included in this skew. The Qn output can either be early or late. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO).

5. This parameter measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. t_{STAOFF} may vary by the amount of t_{DYNOFF} based on voltage and temperature drift as well as tracking error and jitter. Including this variation t_{STAOFF} may not exceed the limits set by $t_{STAOFF(MIN)}$ and $t_{STAOFF(MAX)}$.

6. See "Measurement Requirement for tSTAOFF and tDYNOFF".

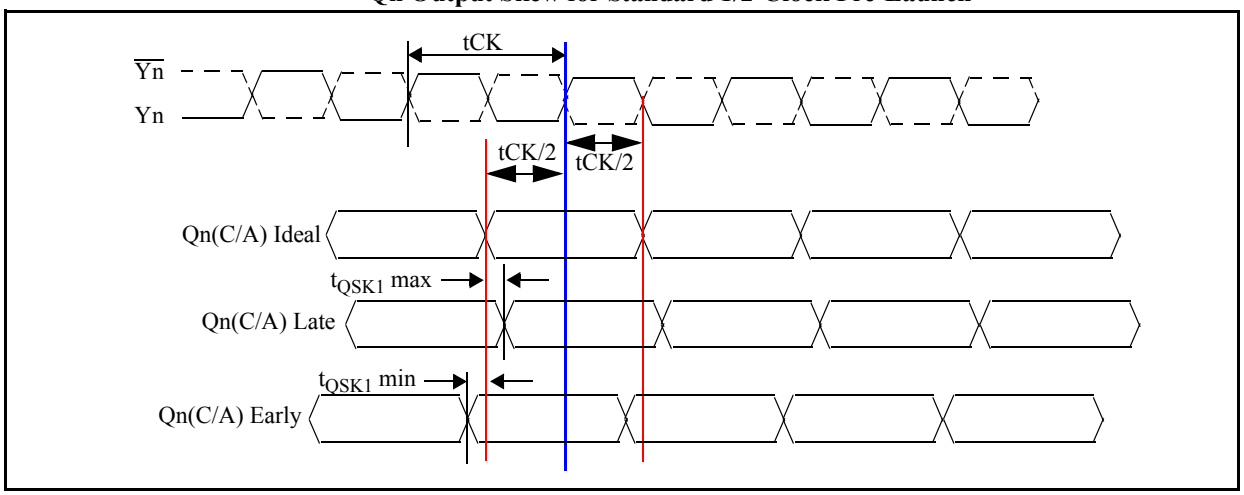
7. Implies a -3 dB bandwidth and jitter peaking of 3 dB.

Clock Output (Yn) Skew

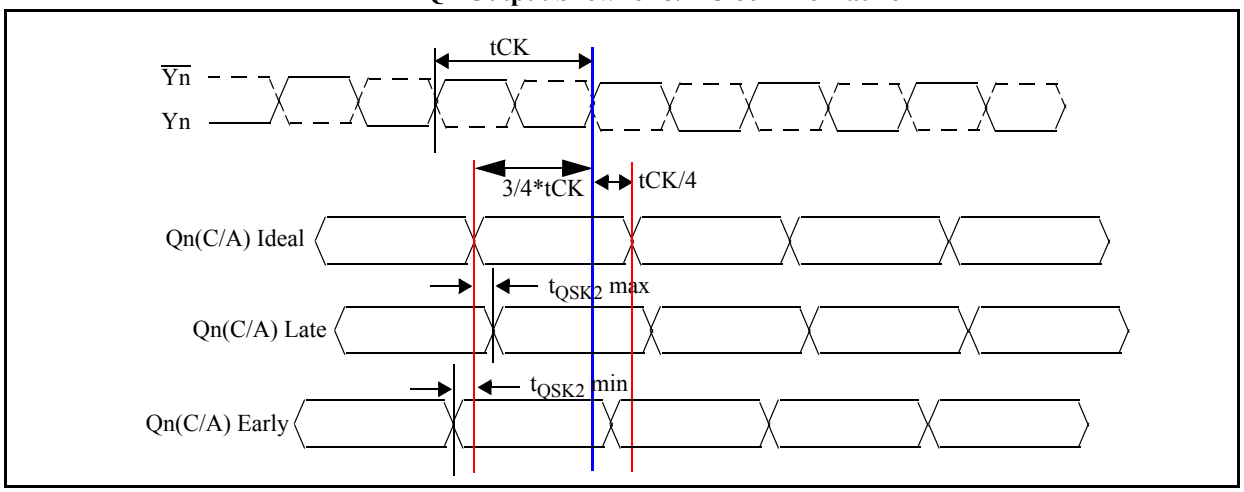


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Qn Output Skew for Standard 1/2-Clock Pre-Launch



Qn Output Skew for 3/4-Clock Pre-Launch



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Clock Driver Characteristics at Test Frequency (frequency band 2)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{JIT(CC)}$	Cycle-to-cycle period jitter		0	160	ps
t_{STAB}	Stabilization time		–	15	us
t_{CKSK}	Total Clock Output skew[1]			100	ps
	Fractional Clock Output skew[2]			TBD	
$t_{JIT(PER)}$	Yn Clock Period jitter		-160	160	ps
$t_{JIT(HPER)}$	Half period jitter		-200	200	ps
$t_{QSK}1$[3]	Qn Output to clock tolerance (Standard 1/2-Clock Pre-Launch)	Output Inversion Enabled	-100	TBD	ps
$t_{QSK1SSO}$[4]		Output Inversion Disabled	-100	TBD	
$t_{QSK}2$[5]	Output clock tolerance (3/4 Clock Pre-Launch)	Output Inversion Enabled	-100	TBD	ps
$t_{QSK2SSO}$[6]		Output Inversion Disabled	-100	TBD	
t_{DYNOFF}	Maximum re-driven dynamic clock offset[7]		-500	500	ps

1 This skew represents the absolute output clock skew and contains the pad skew and package skew.

2 This skew represents the absolute output clock skew and contains the pad skew and package skew (see "Clock Output (Yn) Skew"). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to the left side of the clock pair between Y0/$\overline{Y0}$ and Y2/$\overline{Y2}$, as well as the right side of the clock pair between Y1/$\overline{Y1}$ and Y3/$\overline{Y3}$.

3 This skew represents the absolute Qn skew compared to the output clock Yn, and contains the register pad skew, clock skew, and package routing skew (see "Qn Output Skew for Standard 1/2 Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The Qn output can either be early or late.

4 This skew represents the absolute Qn skew compared to the output clock Yn, and contains the register pad skew, clock skew, and package routing skew. The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. This parameter includes the skew related to Simultaneous Switching Noise (SSO). The Qn output can either be early or late.

5 This skew represents the absolute Qn skew compared to the output clock Yn, and contains the register pad skew, clock skew, and package routing skew (see "Qn Output Skew for Standard 3/4 Clock Pre-Launch"). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The Qn output can either be early or late.

6 This skew represents the absolute Qn skew compared to the output clock Yn, and contains the register pad skew, clock skew, and package routing skew. The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. This parameter includes the skew related to Simultaneous Switching Noise (SSO). The Qn output can either be early or late.

7 The re-driven clock signal is ideally centered in the address/control signal eye. This parameter describes the dynamic deviation from this ideal position including jitter and dynamic phase offset.

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Initialization

The SSTE32882KB1 can be powered-on at 1.5V, 1.35V or 1.25V. After the voltage transition, stable power is provided for a minimum of 200 µs with $\overline{\text{RESET}}$ asserted.

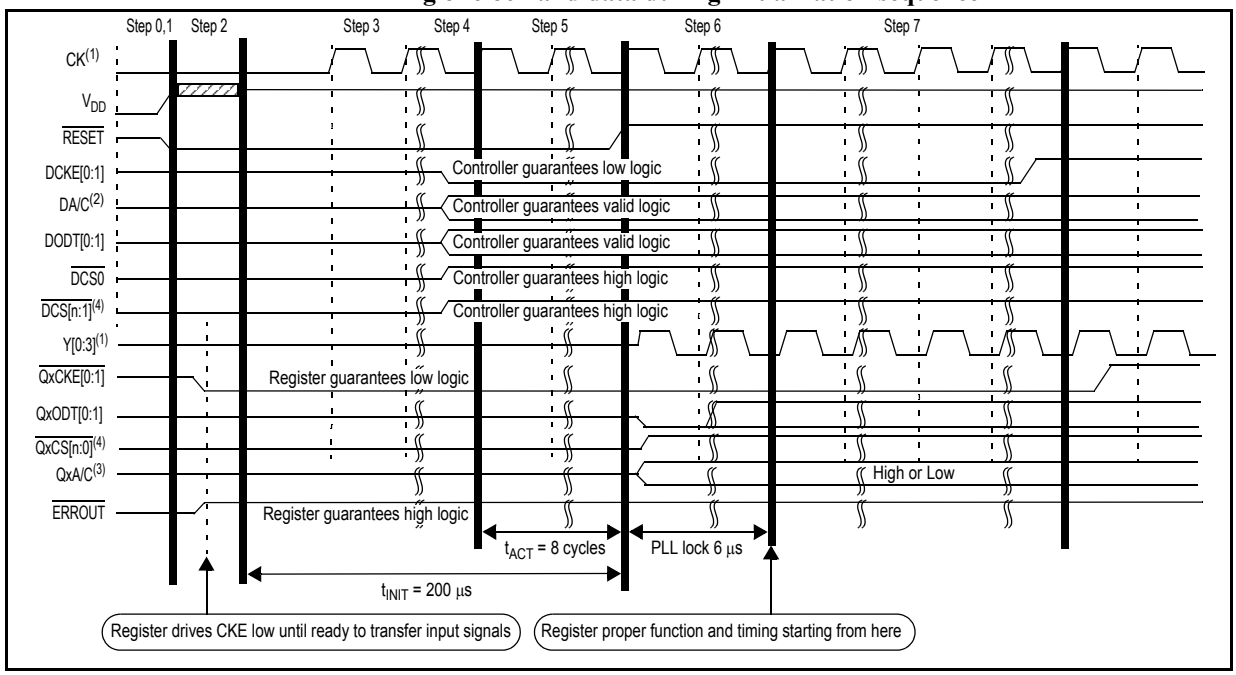
When the reset input ($\overline{\text{RESET}}$) is low, all input receivers are disabled, and can be left floating. The $\overline{\text{RESET}}$ input is referenced to $V_{DD}/2$, therefore the reference voltage (V_{REF}) is not required to be stable during reset. In addition, when $\overline{\text{RESET}}$ is low, all control registers are restored to their default states. The QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs must drive low during reset, and all other outputs must float. As long as the $\overline{\text{RESET}}$ input is pulled low the register is in low power state and input termination is not present.

A certain period of time (t_{ACT}) before the $\overline{\text{RESET}}$ input is pulled high the reference voltage needs to be stable within specification, the clock input signal must be stable, the register inputs $\overline{\text{DCS}}[n:0]$ must be pulled high to prevent any accidental access to the control registers. Also, DCKE0 and DCKE1 inputs must be pulled low for the complete stabilization time (t_{STAB}). After reset and after the stabilization time (t_{STAB}), the register must meet the input setup and hold specification before accepting and transfering data from the register inputs to the register outputs. The $\overline{\text{RESET}}$ input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a low to high transition on $\overline{\text{RESET}}$ while a stable clock signal is present on CK and $\overline{\text{CK}}$.

In the DDR3 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will float quickly (except for QACKE0, QACKE1, QBCKE0 and QBCKE1, which are driven low), relative to the time to disable the differential input receivers. The figure below shows the system timing of clock and data during the initialization sequence.

Timing of clock and data during initialization sequence



1 $\overline{\text{CK}}$ is left out for better visibility.

2 DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are not included in this range.

3 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

4 QxCKEn, QxODTn, $\overline{\text{QxCSn}}$ are not included in this range.

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From a device perspective, the initialization sequence must be as shown in the following Device Initialization table.

SSTE32882KB1 Device Initialization Sequence[1].

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	$\overline{\text{RESET}}$	Vref	$\overline{\text{DCS}}$ [n:0][2]	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK,$\overline{\text{CK}}$	$\overline{\text{QCS}}$ [n:0][2]	QODT [0:1]	QCKE [0:1]	QxA/C	$\overline{\text{ERROUT}}$	Y[0:3] $\overline{\text{Y}}$[0:3]	FB OUT[3]
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2[4]	V_{DD} 1.5V-->1.35V 1.35V-->1.5V	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	L	Z	Z	L[5]	Z	H[5]	Z	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[6]	L	X	H	running	running
7[7]	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables.						

1. x=Logic low or lolgic high. Z=floating.

2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

3. The feedback clock (FBOUT and $\overline{\text{FBOUT}}$) pins may or may not be actively driven by the device.

4. The system may power up using either 1.5V, 1.35V or 1.25V. The BIOS reads the SPD and adjusts the voltage if needed. After the voltage transition, stable power is provided for a minimum of 200 uS with $\overline{\text{RESET}}$ asserted.

5. QxCKEn and $\overline{\text{ERROUT}}$ will be driven to these logic states by the register after $\overline{\text{RESET}}$ is driven low and VDD is 1.5V, 1.35V or 1.25V (nominal).

6. This indicates the state of QxODTx after $\overline{\text{RESET}}$ switches from low-to-high and before the rising CK edge (falling $\overline{\text{CK}}$ edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) us, the state of QxODTx is a function of DODTx (high or low).

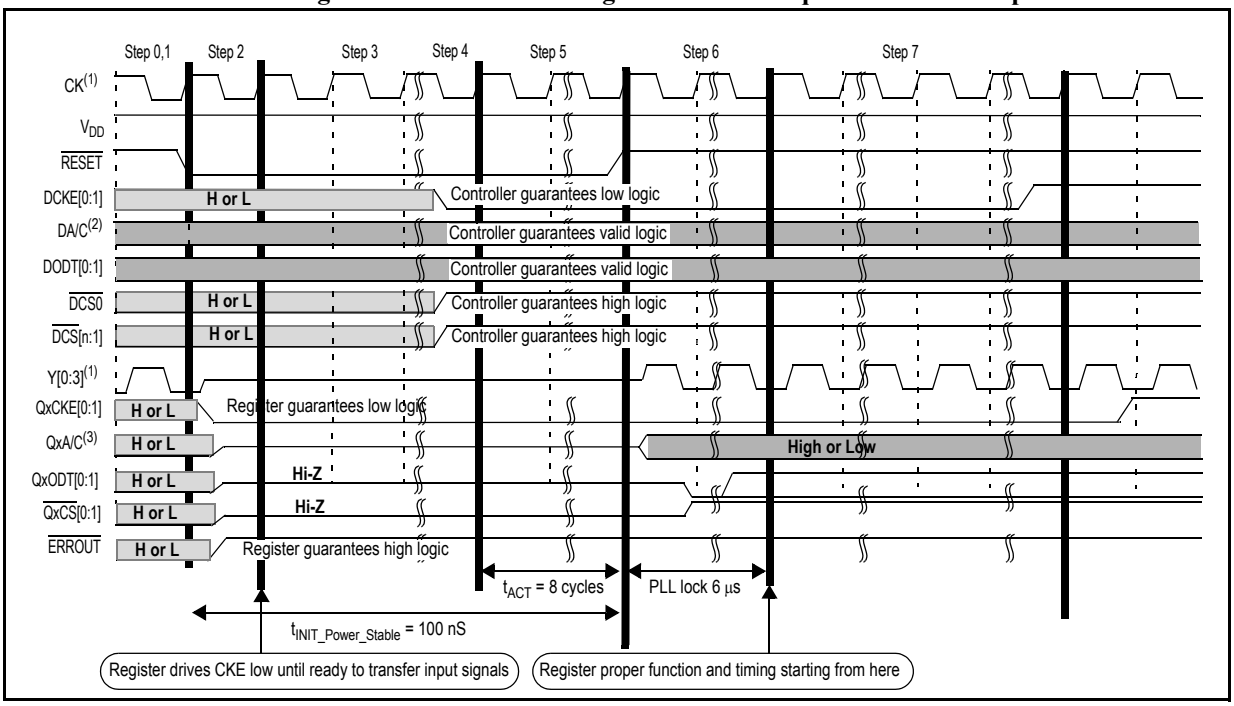
7. Step 7 is a typical usage example and is not a register requirement.

Reset Initialization with Stable Power

The timing diagram in the following diagram depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. $\overline{\text{RESET}}$ will be asserted for minimum 100ns. This $\overline{\text{RESET}}$ timing is based on DDR3 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual $\overline{\text{RESET}}$ timing can vary base on specific system requirement, but it cannot be less than 100ns as required by JESD79-3 Specification.

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Timing of clock and data during initialization sequence with stable power



1 $\overline{CK}$ is left out for better visibility.

2 DCKE0, DCKE1, DODT0, DODT1, $\overline{DCS0}$ and $\overline{DCS1}$ are not included in this range.

3 QxCKEn, QxODTn, $\overline{QxCSn}$ are not included in this range.

4 n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.

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SSTE32882KB1 Device Initialization Sequence[1] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device						
	VDD, AVDD, PVDD	$\overline{RESET}$	Vref	$\overline{DCS}$ [n:1][2]	DODT [0:1]	DCKE [0:1]	DA/C	PAR_IN	CK, $\overline{CK}$	$\overline{QCS}$ [0:1]	QODT [0:1]	QCKE [0:1]	QxA/C	$\overline{ERROUT}$	Y[0:3] $\overline{Y}$[0:3]	FB OUT[3]
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[4]	Z	H[4]	Z	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[5]	L	X	H	running	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables.						

1. x=Logic low or lolgic high. Z=floating.
2. n = 1 for QuadCS disabled mode, n = 3 for QuadCS enabled mode.
3. The feedback clock (FBOUT and $\overline{FBOUT}$) pins may or may not be actively driven by the device.
4. QxCKEn and $\overline{ERROUT}$ will be driven to these logic states by the register after $\overline{RESET}$ is driven low and VDD is nominal.
5. This indicates the state of QxODTx after $\overline{RESET}$ switches from low-to-high and before the rising CK edge (falling $\overline{CK}$ edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}) us, the state of QxODTx is a function of DODTx (high or low)

Parity

The SSTE32882KB1 includes a parity checking function. The SSTE32882KB1 accepts a parity bit from the memory controller at its input pin PAR_IN one cycle after the corresponding data input, compares it with the data received on the D-inputs and indicates on its open-drain $\overline{ERROUT}$ pin (active low) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the $\overline{DCS[n:0]}$ signals being LOW.

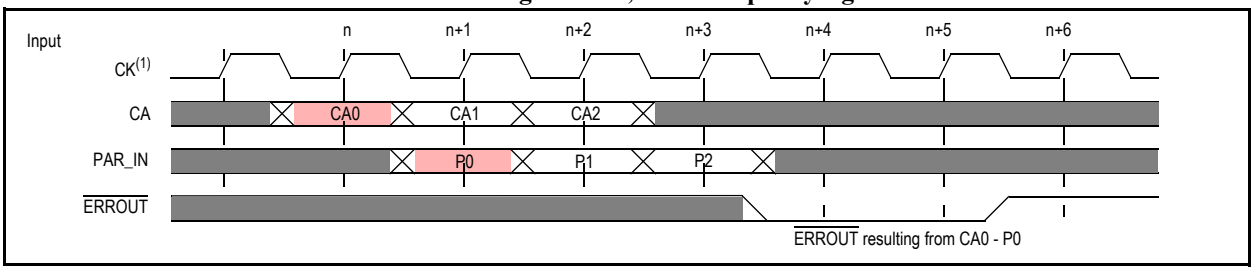
If an error occurs, and $\overline{ERROUT}$ is driven low with the third input clock edge after the corresponding data on the D-inputs. It becomes high impedance with the 5th input clock cycle after the data corresponding with a parity error. In case of consecutive errors $\overline{ERROUT}$ becomes high impedance with the 5th input clock cycle after the last data corresponding with a parity error. The DIMM-dependent signals (DCKE0, DCKE1, $\overline{DCS0}$, $\overline{DCS1}$, DODT0 and DODT1) are not included in the parity check computations.

Parity Timing Scheme Waveforms

The PAR_IN signal arrives one input clock cycle after the corresponding data input signals. $\overline{ERROUT}$ is generated three input clock cycles after the corresponding data is registered. If $\overline{ERROUT}$goes low, it stays low for a minimum of two input clock cycles or until $\overline{RESET}$ is driven low. The following figure shows the parity diagram with single parity-error occurrence and assumes the occurrence of only one parity error when data is clocked in at the n input clock cycle (PAR_IN clocked in on the n+1 input clock cycle).

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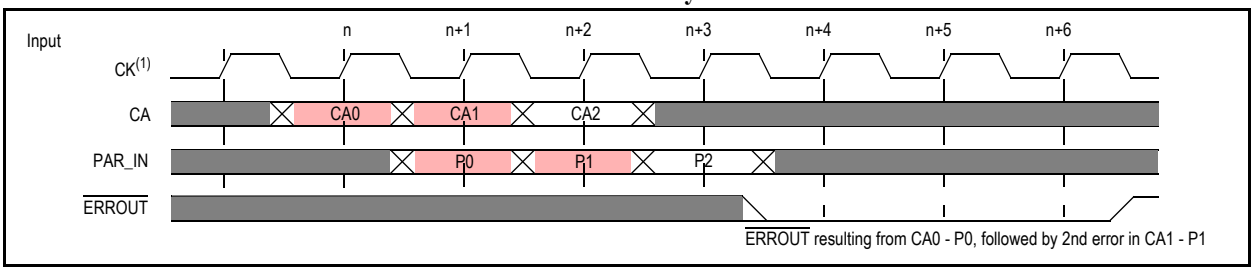
Timing of clock, data and parity signals



1 $\overline{CK}$ left out for better visibility.

The next figure shows the parity diagram with two consecutive parity-error occurrences and assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles).

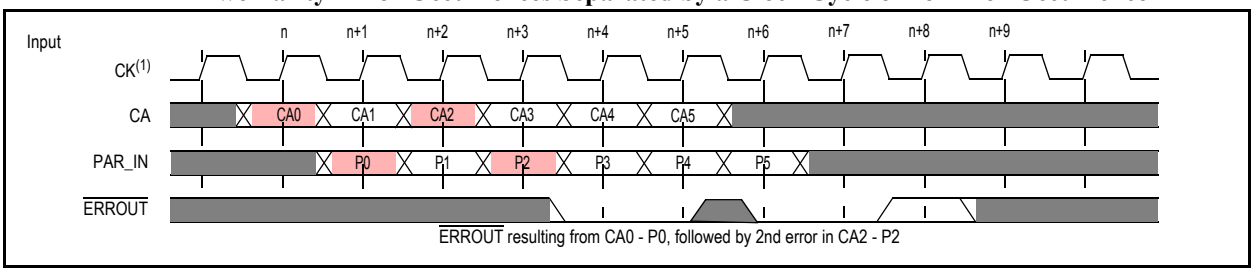
Two Consecutive Parity-Error Occurrences



1 $\overline{CK}$ left out for better visibility.

The next figure shows the parity diagram with two parity-error occurrences separated by a clock cycle with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+2 input clock cycles (PAR_IN clocked in on the n+1 and n+3 input clock cycles).

Two Parity-Error Occurrences Separated by a Clock Cycle of no Error Occurrence

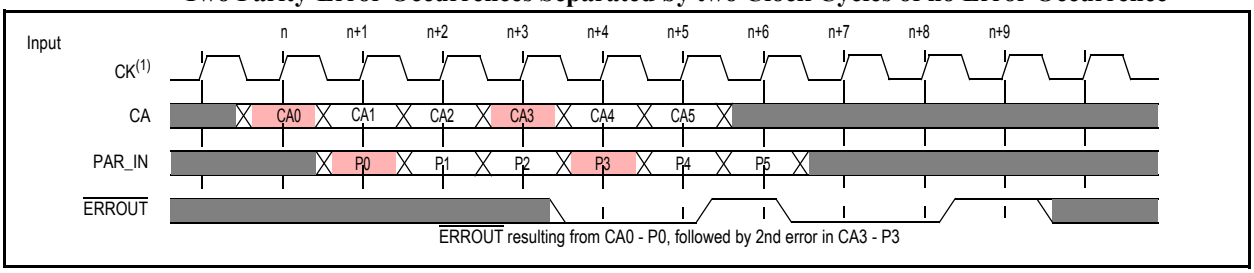


1 $\overline{CK}$ left out for better visibility.

The next figure shows the parity diagram with two parity-error occurrences separated by two input clock cycles with no error occurrence. The diagram assumes the occurrence of two parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles).

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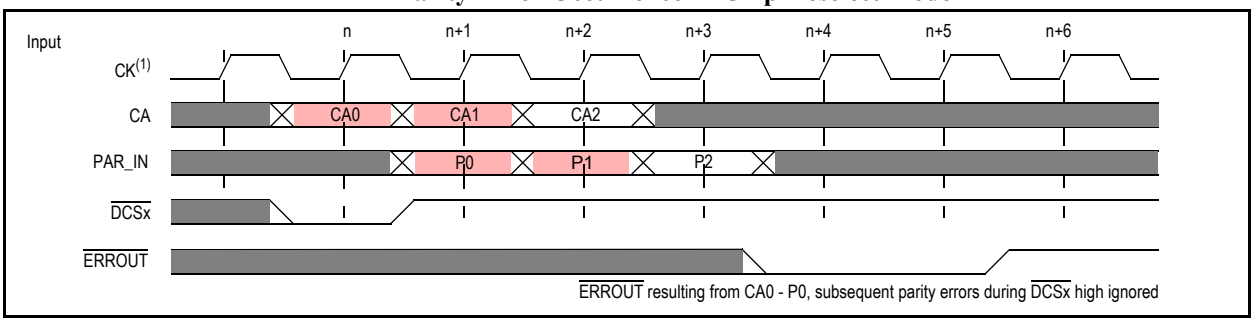
Two Parity-Error Occurrences Separated by two Clock Cycles of no Error Occurrence



1 $\overline{CK}$ left out for better visibility.

The next figure shows the parity diagram with two parity-error occurrences; during chip-select and chip-deselect modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+1 input clock cycles (PAR_IN clocked in on the n+1 and n+2 input clock cycles). Parity error in the chip-select mod is detected, but parity error in the chip-deselect mode is ignored.

Parity-Error Occurrence In Chip-Deselect Mode

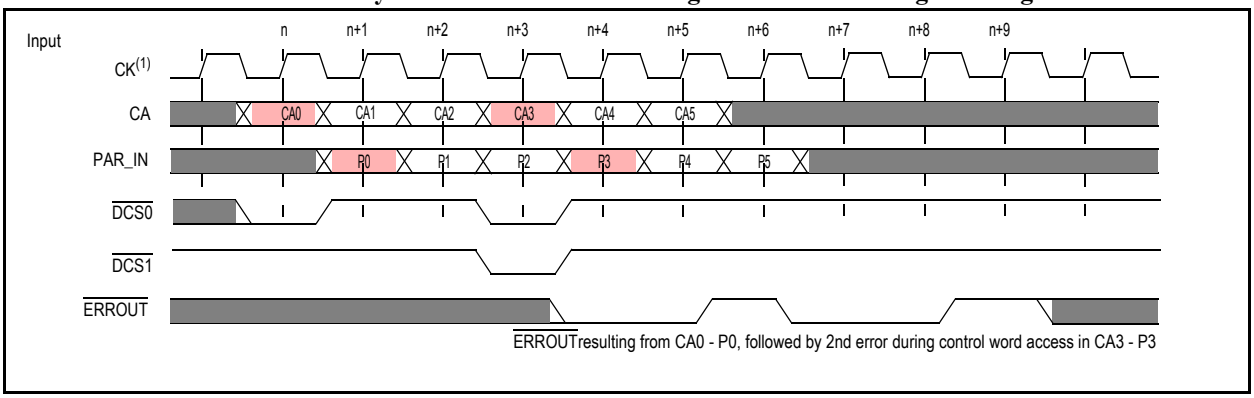


1 $\overline{CK}$ left out for better visibility.

The next figure shows the parity diagram with two parity-error occurrences; during normal operation and during control register programming. The diagram assumes the occurrence of both parity errors when data is clocked in at the n and n+3 input clock cycles (PAR_IN clocked in on the n+1 and n+4 input clock cycles). The data on the n+3 input clock pulse is intended for the control mode register. Parity error during control mode register programming is detected and the parity functionality is the same as during normal operation. If a parity error occurs, the command is ignored.

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Parity-Error Occurrences During Control Word Programming



1 $\overline{CK}$ left out for better visibility.

POWER SAVING MODES

The device supports different power saving mechanisms.

When both inputs CK and $\overline{CK}$ are being held low the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven low. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs $\overline{DCS[n:0]}$ must be pulled high to prevent accidential access to the control registers and DCKE0 as well as DCKE1 must be pulled low for a certain period of time (tACT). The input clock must be stable for a time (tSTAB) before any access to the device takes place. Stopping the clocks (CK = $\overline{CK}$ = low) will only put the SSTE32882KB1 in low-power mode and will not clear the content of the control words. The control words will reset only when $\overline{RESET}$ is diven low.

A float feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the $\overline{DCS[n:0]}$ inputs and to float all outputs corresponding with the chip select gated inputs when all the $\overline{DCS[n:0]}$ inputs are high. If any one of the $\overline{DCS[n:0]}$ inputs are low, the Qn outputs will function normally.

Once all the $\overline{DCS[n;0]}$ inputs are high, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The $\overline{RESET}$ input has priority over all other power saving mechanisms. When $\overline{RESET}$ is driven low, it will force the Qn outputs to float, the $\overline{ERROUT}$ output high, the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs low, and disables Input Bus Termination (IBT).

REGISTER CKE POWER DOWN

If RC9[DBA1] is set to “1”, the SSTE32882KB1 monitors both DCKEn input signals and enters into power saving state when it latches Low on both DCKEn inputs and at least one of the DCKEn input has transitioned from High to Low. If any input Chip Select signal ($\overline{DCS[n:0]}$) is asserted together with DCKEn, the SSTE32882KB1 transfers the corresponding command to its outputs together with QxCKEn Low.

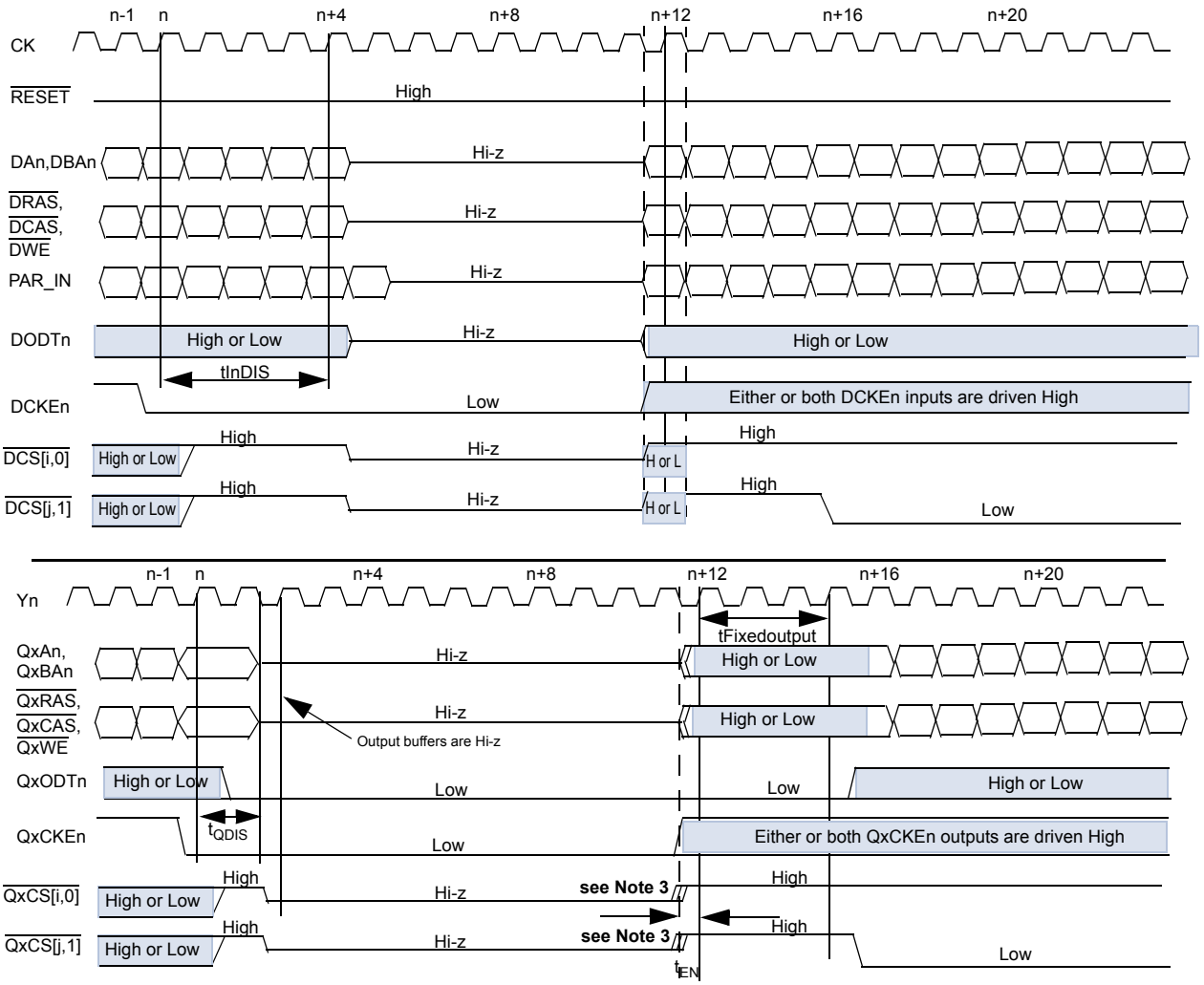
There are two modes of CKE Power Down selected by RC9. Bit DBA0 in RC9 indicates whether the register turns off IBT or keeps IBT on.

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REGISTER CKE POWER DOWN WITH IBT OFF

Upon entry into CKE Power Down mode with IBT off, all register input buffers including IBT are disabled except for CK/$\overline{CK}$, DCKEn, FBIN/$\overline{FBIN}$, and $\overline{RESET}$. The SSTE32882KB1 disables input buffers within tInDIS clocks after latching both DCKEn Low. In order to eliminate and false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after Address and Command input buffers disabled. After tInDIS, the register can tolerate floating input except for CK/$\overline{CK}$, DCKEn and $\overline{RESET}$. The SSTE32882KB1 also disables all its output buffers except for Yn/$\overline{Yn}$, QxODTn, QxCKEn and FBOUT/$\overline{FBOUT}$. The Yn/$\overline{Yn}$ and FBOUT/$\overline{FBOUT}$ outputs continue to drive a valid phase accurate clock signal. The QxODTn and QxCKEn outputs are driven Low. The register output buffers are Hi-Z t_{QDIS} clock after QxCKEn is driven Low. This is shown in the next figure.

Power Down Mode Entry and Exit with IBT Off



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3.

(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving $\overline{DCS[1,0]}$ LOW is illegal as it will force SSTE32882KB1 into Register Control Word access mode.

(3)Upon CKE Power Down exit, $\overline{QxCSn}$ will be held HIGH for maximum of 1 tCK regardless of what $\overline{DCSn}$ input level is. For all other operation $\overline{QxCSn}$ outputs will follow $\overline{DCSn}$ inputs.

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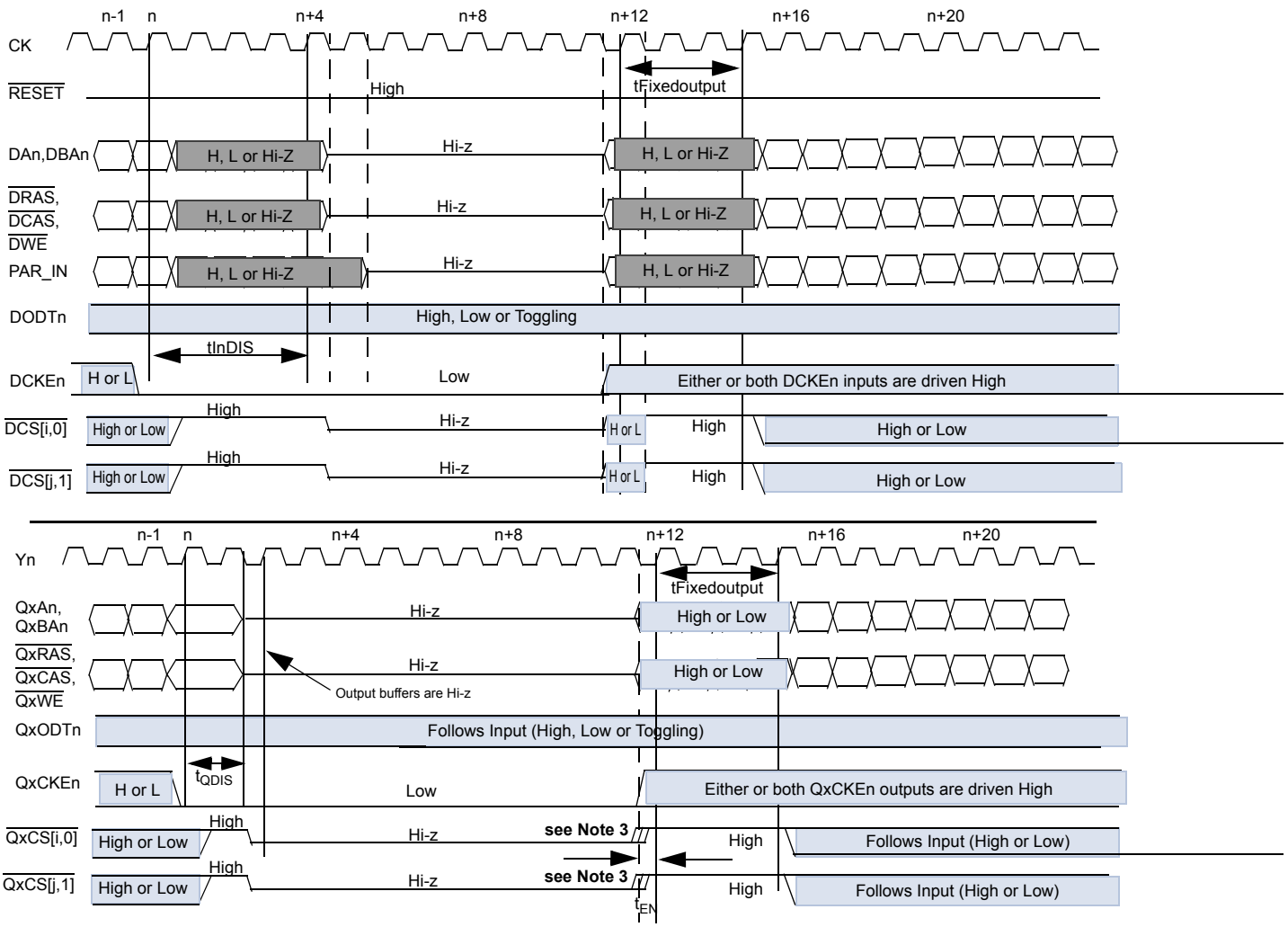
To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn inputs are driven high. Upon either DCKE0 or DCKE1 input going High, the register immediately starts driving High on the appropriate QxCKEn signal. The $\overline{\text{QxCSn}}$ signals are driven High and QxODTn signals are driven Low. Other output signals $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, $\overline{\text{QxWE}}$, and QxAddr are driven either high or low to ensure stable valid logic an all register outputs when QxCKEn goes High. The register drives output signals to these levels for $t_{FIXEDOUTPUT}$ to allow input receivers to be stabilized. After the input recievers are stabilized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip Select register inputs $\overline{\text{DCSn}}$ can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip Select register inputs $\overline{\text{DCSn}}$ can be asserted for 1 tCK. The register guarantees that input receivers are stabilized within $t_{FIXEDOUTPUT}$ clocks after DCKEn input is driven High. This is shown in the previous diagram.

REGISTER CKE POWER DOWN WITH IBT ON

Upon entry into CKE Power Down Mode with IBT on, all register input buffers excluding IBT are disabled except for CK/$\overline{\text{CK}}$, DCKEn, DODTn, FBIN/$\overline{\text{FBIN}}$, and $\overline{\text{RESET}}$. The SSTE32882KB1 disables input buffers within tInDIS clocks after latching both DCKEn Low. In order to eliminate any false parity check error, the PAR_IN input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After tInDIS, the register can tolerate floating input except for CK/$\overline{\text{CK}}$, DCKEn, DODTn and $\overline{\text{RESET}}$. The SSTE32882KB1 also disables all its output buffers except for Yn/$\overline{\text{Yn}}$, QxODTn, QxCKEn and FBOUT/$\overline{\text{FBOUT}}$. The Yn/$\overline{\text{Yn}}$ and FBOUT/$\overline{\text{FBOUT}}$ outputs continue to drive a valid phase accurate clock signal. The QxCKEn outputs are driven Low. The register output buffers are Hi-Z t_{QDIS} clock after QxCKEn is driven Low. This is shown below.

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Power Down Mode Entry and Exit with IBT On



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3.

(2) QuadCS disabled: During CKE Power Down Entry/Exit, driving $\overline{DCS[1,0]}$ LOW is illegal as it will force SSTE32882KB1 into Register Control Word access mode.

(3) UPon CKE Power Down exit, $\overline{QxCSn}$ will be held HIGH for a maximum of 1 tCK regardless of what $\overline{DCSn}$ input level is. For all other operation, $\overline{QxCSn}$ outputs will follow $\overline{DCSn}$ inputs.

To re-enable the SSTE32882KB1 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven High. Upon either DCKE0 or DCKE1 input going High, the SSTE32882KB1 immediately starts driving High on the appropriate QxCKEn signals. The $\overline{QxCSn}$ signals are driven high and the QxODTn signals follow the inputs. Other output signals $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$ and QxAddr are driven either high or low to ensure stable valid logic on all device outputs when QxCKEn goes High. The device drives output signals to these levels for tFIXEDOUTPUT to allow input receivers to be stablized. After the input receivers are stablized, the register output follow their corresponding input levels. When exiting CKE power down mode, either one of the Chip Select register inputs $\overline{DCSn}$ can be asserted for 1 tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip Select register inputs $\overline{DCSn}$ can be asserted for 1 tCK. The device guarantees that input receivers are stablized within tFIXEDOUTPUT clocks after DCKEn input is driven High. This is shown in the previous diagram.

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CLOCK STOPPED POWER DOWN MODE

To support S3 Power Management mode or any other operation that allows Yn clocks to float, the SSTE32882KB1 supports a Clock Stopped power down mode. When both inputs CK and $\overline{CK}$ are being held LOW, ($V_{IL(static)}$) or float (will eventually settle at LOW because of the (10K-100K Ohm) pulldown resistor in the CK/$\overline{CK}$ input buffer, the device stops operation and enters low-power static and standby operation. The corresponding timing are shown in "Clock Stopped Power Down Entry and Exit with IBT On" and "Clock Stopped Power Down Entry and Exit with IBT Off". The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1, which must be kept driven LOW.

The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0 and QxCKE1 can be disabled.

Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, the register will first enter CKE power down mode. Once in CKE power down mode, the host will deasserts DCKEn for a minimum of one tCKoff before pulling CK and $\overline{CK}$ LOW. After holding CK and $\overline{CK}$ LOW ($V_{IL(static)}$) for at least one tCKEV, both CK and $\overline{CK}$ can be floated (because of the (10K-100K Ohm) pulldown resistor in the CK/$\overline{CK}$ input buffer, CK/$\overline{CK}$ will stay at LOW even though they are not being driven).The register is now in Clock Stopped Power Down mode.

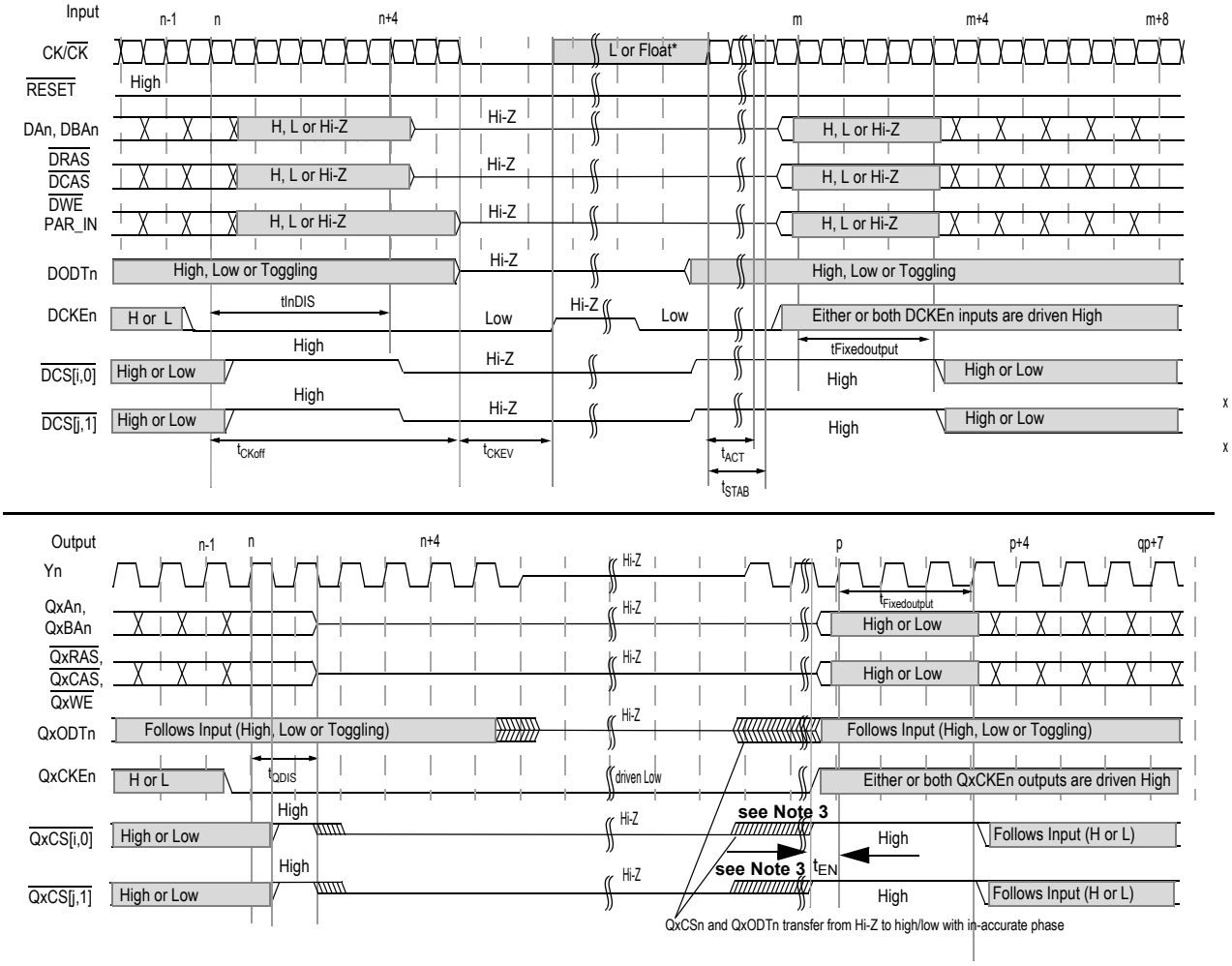
After CK and $\overline{CK}$ are pulled LOW, the host has to keep DCKEn stable for at least one t_{CKEV} before it can float DCKEn. At this point, all input receivers and input termination of the SSTE32882KB1 are disabled. The only active input circuits are CK and $\overline{CK}$, which are required to detect the wake up request from the host.

Clock Stopped Power Down Mode Exit

To wake up the register after Clock Stopped power down, the host must drive the register inputs $\overline{DCS[n:0]}$ must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, the host can apply a frequency and phase accurate input clock signal. Within t_{ACT} after CK and $\overline{CK}$ resumed normal operation, the SSTE32882KB1 outputs start becoming a function of their corresponding inputs. The state of the $\overline{DCS[n:0]}$ inputs must not be changed before the end of t_{STAB}. The input clock CK and $\overline{CK}$ must be stable for a time equal or greater than t_{STAB} before any access to the SSTE32882KB1 can takes place.

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Clock Stopped Power Down Entry and Exit with IBT On



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3.

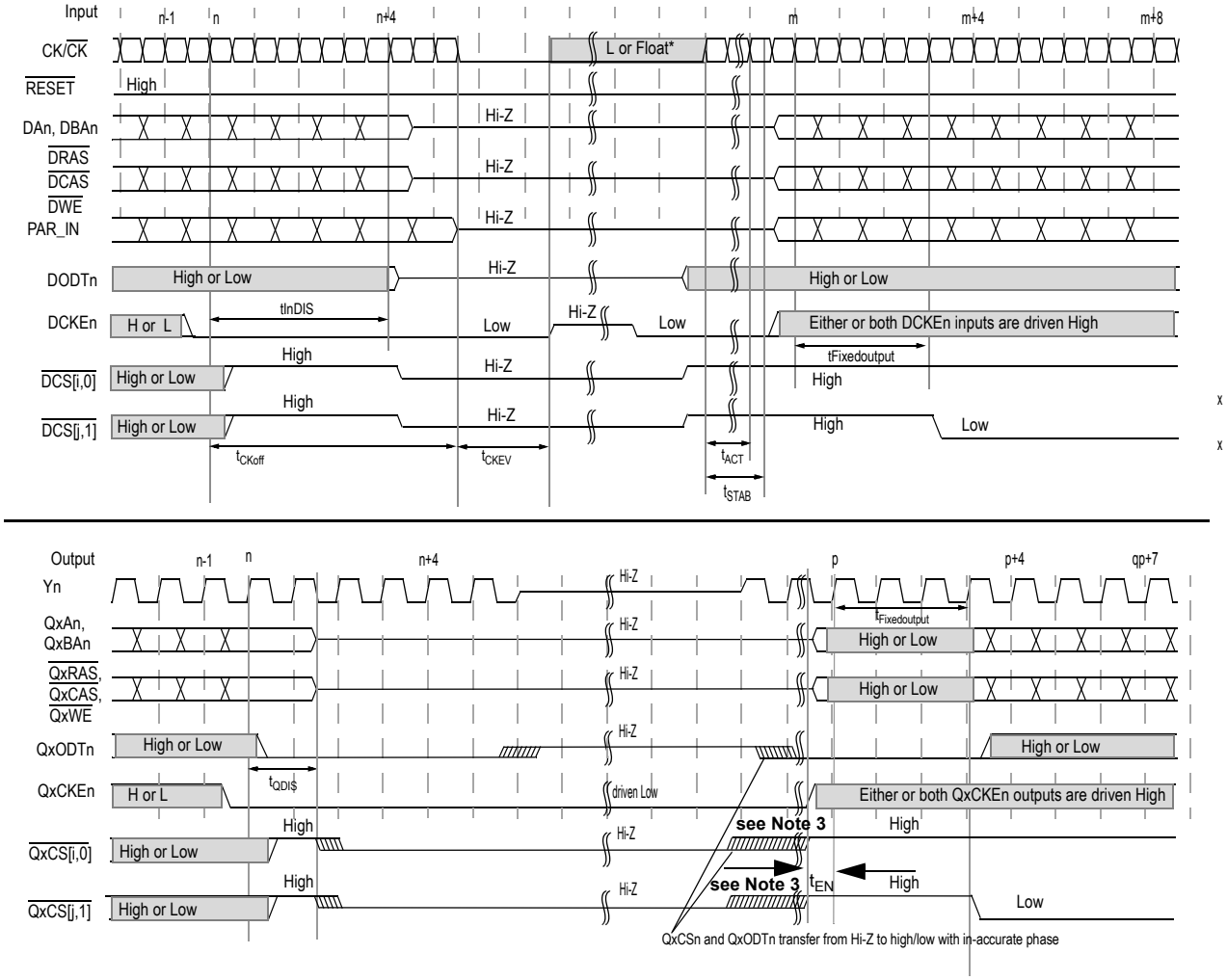
(2) With RC9 DBA0=’0’.

(3) When CK/$\overline{CK}$ inputs are floated, CK/$\overline{CK}$ inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/$\overline{CK}$ input buffer.

(4) Upon CKE Power Down exit, $\overline{QxCSn}$ will be held HIGH for maximum of 1 tCK regardless of what $\overline{DCSn}$ input level is. For all other operation $\overline{QxCSn}$ outputs will follow $\overline{DCSn}$ inputs.

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Clock Stopped Power Down Entry and Exit with IBT Off



(1) i, j only apply for QuadCS capable register. When QuadCS is enabled, i = 2, j = 3.

(2) With RC9 DBA0=’1’.

(3) When CK/$\overline{CK}$ inputs are floated, CK/$\overline{CK}$ inputs are pulled LOW by the (10K-100K Ohm) pulldown resistor in the CK/$\overline{CK}$ input buffer.

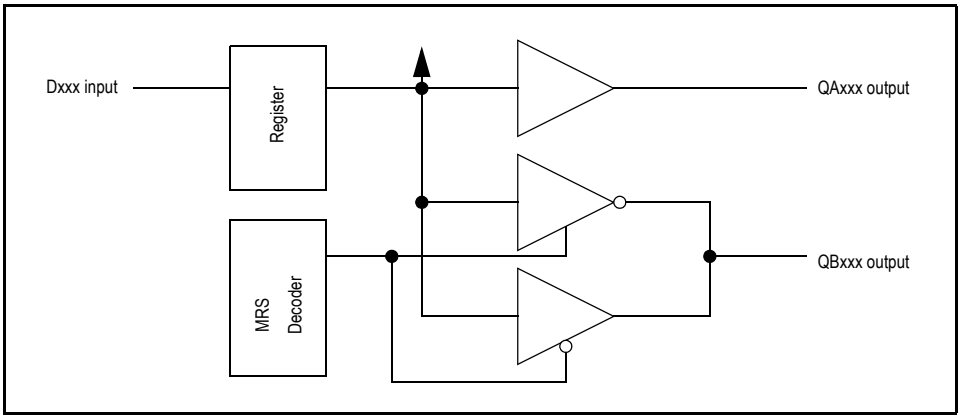
(4) Upon CKE Power Down exit, $\overline{QxCSn}$ will be held HIGH for maximum of 1 tCK regardless of what $\overline{DCSn}$ input level is. For all other operation $\overline{QxCSn}$ outputs will follow $\overline{DCSn}$ inputs.

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DYNAMIC 1T/3T TIMING TRANSACTION AND OUTPUT INVERSION ENABLING/DISABLING

Output Inversion is always enabled by default, after $\overline{\text{RESET}}$ is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs, however the following B-outputs will be driven to the complement of the matching A-outputs: QBA3 - QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2.

Output Inversion Functional Diagram



The Output Inversion feature is not used during DRAM MRS command access. When Output Inversion is disabled, all corresponding A and B output drivers of the SSTE32882KB1 are driven to the same logic levels. Output Inversion must be disabled when the MRS and EMRS commands must be issued to the DRAMs, for example, to assure that the same programming is issued to all DRAMs in a rank.

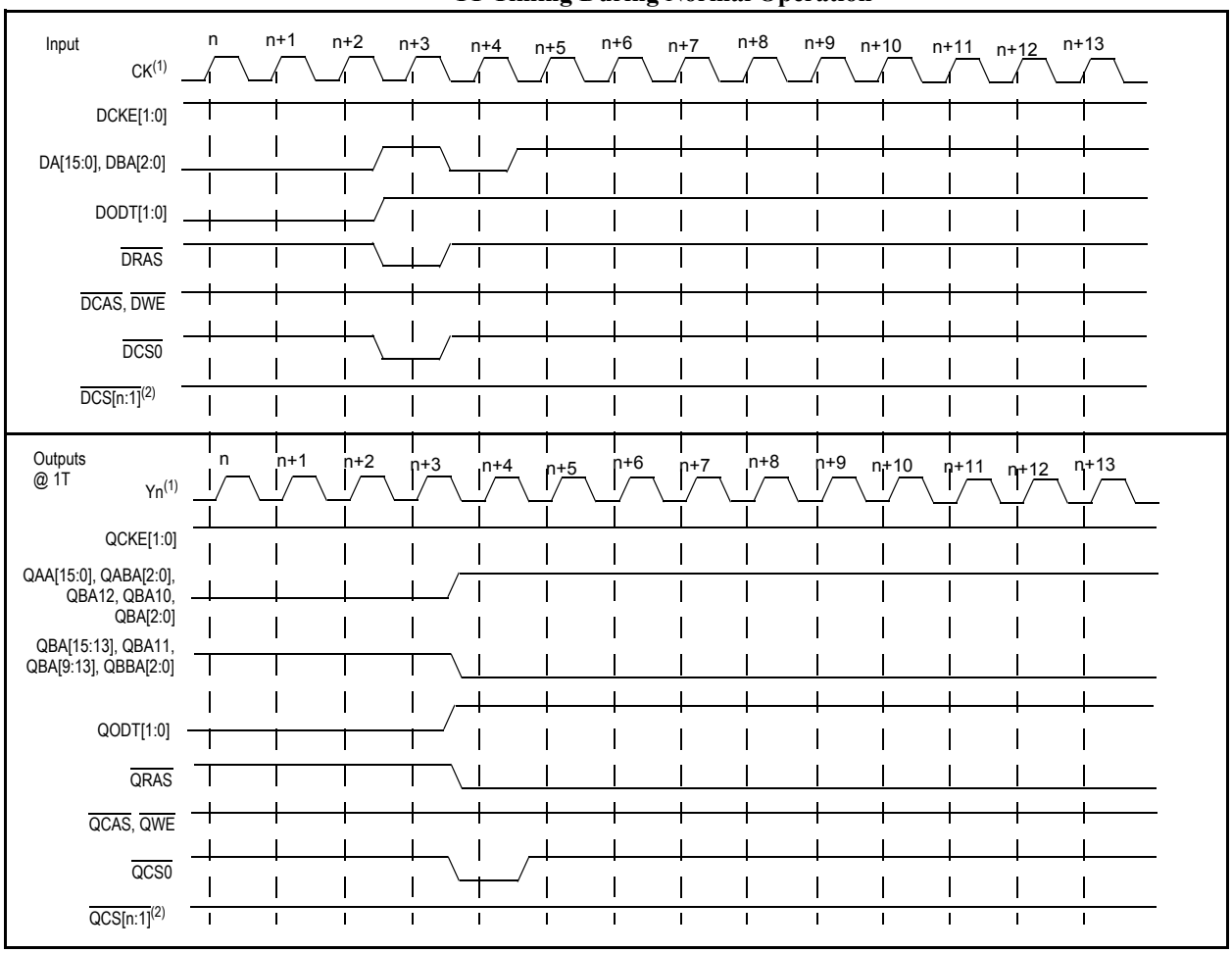
With Output Inversion disabled during MRS access, in order to allow correct DRAM accesses with the consequently increased simultaneous switching propagation delay the devices supports 3T timing. If this feature is invoked the device drives the received data on its outputs for thee cycles instead of one. The only exceptions are the $\overline{\text{QxCS[n:0]}}$ outputs, which are the $\overline{\text{QACS0}}$, $\overline{\text{QACS1}}$, $\overline{\text{QBCS0}}$, and $\overline{\text{QBCS1}}$ outputs in the QuadCS disabled mode and are $\overline{\text{QCS[3:0]}}$ in the QuadCS enabled mode.

When the device decodes the MRS command ($\overline{\text{DRAS}}$=0, $\overline{\text{DCAS}}$=0, $\overline{\text{DWE}}$=0 and only one $\overline{\text{DCSn}}$=0), it will disable the Output Inversion function and pass the DRAM MRS command with an additional (one) clock delay on the appropriate $\overline{\text{QnCSx}}$ signal to the DRAM. Back-to-back MRS command via the SSTE32882KB1 must have a minimum of three clock delays. The SSTE32882KB1 will automatically enable Output Inversion if there is no DRAM MRS command three clocks after the previous MRS command.

The inputs and outputs relationships for 1T timing and 3T timing are shown in the following three diagrams.

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1T Timing During Normal Operation

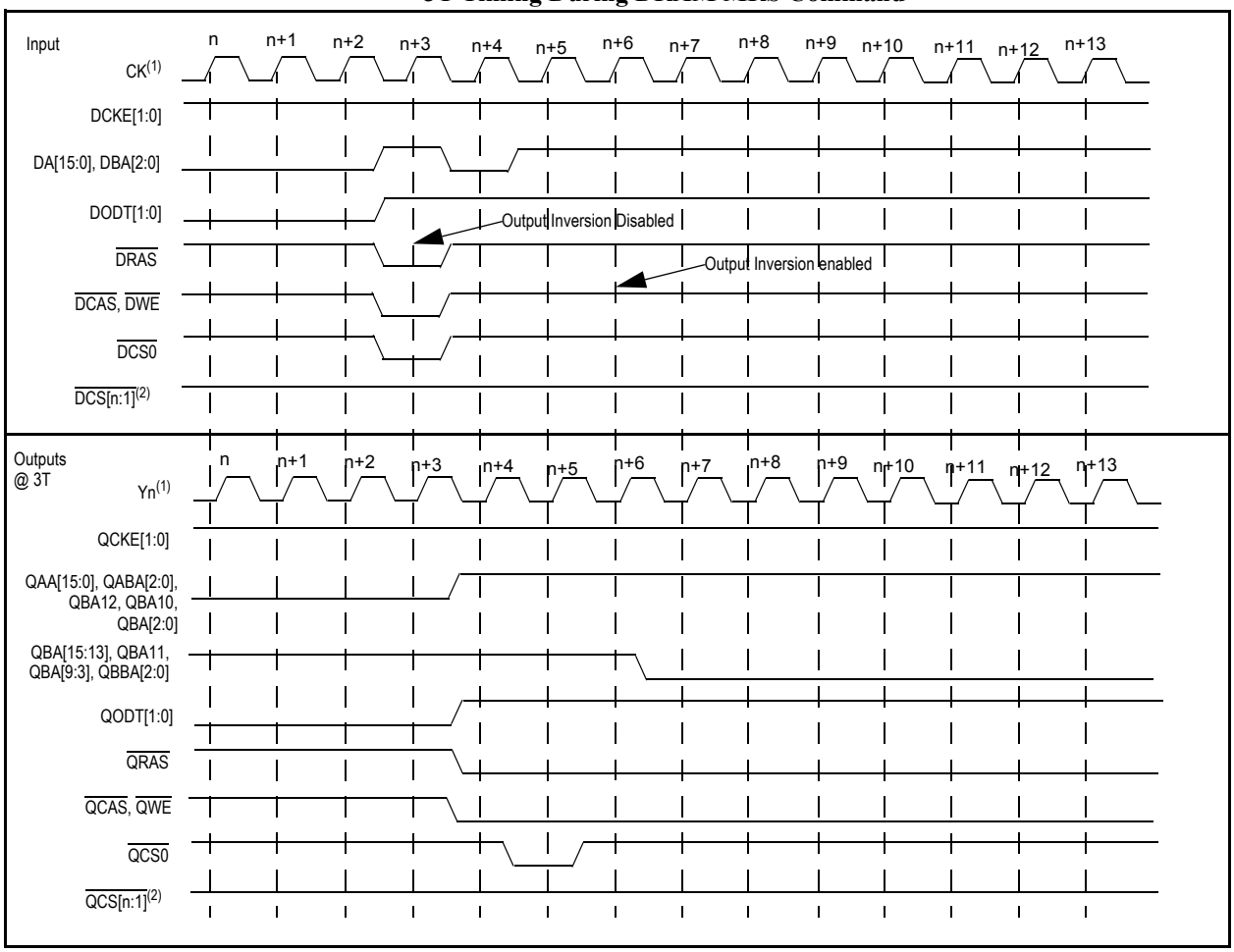


1 $\overline{CK}$ and $\overline{Yn}$ left out for better visibility.

2 n = 1 for QuadCS disabled, n = 3 for QuadCS enabled.

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3T Timing During DRAM MRS Command

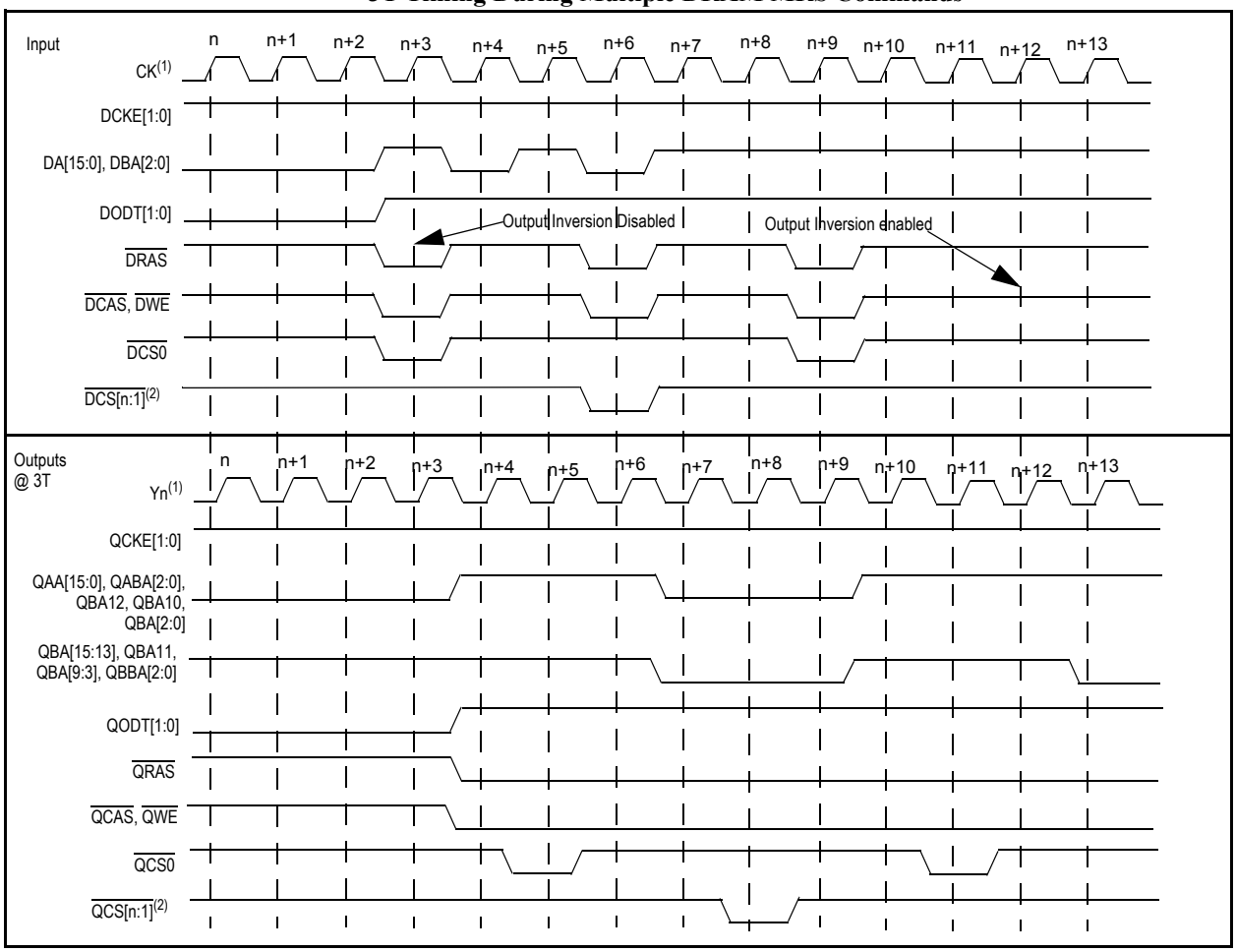


1 $\overline{CK}$ and $\overline{Yn}$ left out for better visibility.

2 n = 1 for QuadCS disabled, n = 3 for QuadCS enabled.

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3T Timing During Multiple DRAM MRS Commands



1 $\overline{CK}$ and $\overline{Yn}$ left out for better visibility.

2 n = 1 for QuadCS disabled, n = 3 for QuadCS enabled.

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CONTROL WORDS

The SSTE32882KB1 registers have internal control bits for adapting the configuration of certain device features. The control bits are accessed by the simultaneous assertion of both $\overline{DCS0}$ and $\overline{DCS1}$ in the QuadCS disabled mode. In the QuadCS enabled mode, the simultaneous assertion of both $\overline{DCS2}$ and $\overline{DCS3}$ during normal operation, and the assertion of all four $\overline{DCS[3:0]}$ inputs also results in control word access. However, assertion of any three $\overline{DCS[3:0]}$ inputs is not legal. Register Qn outputs including QxCKE0, QxCKE1, QxODT0 and QxODT1 remain in their previous state. Select signals $\overline{QxCS[n:0]}$ are set to high during control word access.

The SSTE32882KB1 allocates decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers need to be presented on DA3, DA4, DBA0 and DBA1. Bits DA[15:5] need to be low, and at least one DCKEn input must be high, for valid data access. If Power Down mode is enabled in RC9[DBA1], at least one DCKE must be high for valid control word access. The inputs on $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$, and DODT[1:0] can be either high or low, and are ignored by the SSTE32882KB1 during control word access. In all cases Address and command parity is checked during control word write operations. $\overline{ERROUT}$ is asserted and the command is ignored if a parity error is detected. Using this mechanism, controllers may use the SSTE32882KB1 to validate the address and command bus signal integrity to the module as long as one or more of the parity checked input signals DA3-DA15, DBA0, DBA1, $\overline{DRAS}$, $\overline{DCAS}$, $\overline{DWE}$ are kept high.

Control word access must be possible at any defined frequency independent of the current setting of RC2[DBA1] control registers.

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Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. The different control words and settings are described below. Any change to these control words requires some time for the device to settle. For changes to the control word setting, except for RC2 (bits DBA1 and DA3) and RC10, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (RC2: bits DBA1 and DA3) and RC10, this settling may take up to t_{STAB} time. All chip select inputs ($\overline{DCS}[n:0]$) must be kept high during that time. The Control Words can be accessed and written to when running within any one defined frequency band.

CONTROL WORD DECODING

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0 and DBA1 simultaneously with the assertion of the control word access through $\overline{DCS0}$ and $\overline{DCS1}$, or $\overline{DCS2}$ and $\overline{DCS3}$ in the QuadCS enabled mode, and the address of the control word on DA0, DA1, DA2 and DBA2.

The reset default state of Control Words 0 .. 5 and Control Words 8 .. 15 is “0”. The reset default state for Control Words 6 and 7 is vendor specific. Every time the device is reset, its default state is restored. Stopping the clocks (CK = $\overline{CK}$ = low) to put the device in low-power mode will not alter the control word settings.

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Control Word Decoding with QuadCS Mode Disabled

		Signal						
Control Word	**Symbol**	**$\overline{DCS0}$**	**$\overline{DCS1}$**	**DBA2**	**DA2**	**DA1**	**DA0**	**Meaning**
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Global Features Control word
Control word 1	RC1	L	L	L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2	L	L	L	L	H	L	Timing Control word
Control word 3	RC3	L	L	L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4	L	L	L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5	L	L	L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6	L	L	L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7	L	L	L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8	L	L	H	L	L	L	Additional IBT Setting Control Word
Control word 9	RC9	L	L	H	L	L	H	Power Saving Settings Control word
Control word 10	RC10	L	L	H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11	L	L	H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12	L	L	H	H	L	L	Reserved for future use
Control word 13	RC13	L	L	H	H	L	H	Reserved for future use
Control word 14	RC14	L	L	H	H	H	L	Reserved for future use
Control word 15	RC15	L	L	H	H	H	H	Reserved for future use

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Control Word Decoding with QuadCS Mode Enabled

		Signal					
Control Word	**Symbol**	**DCS[3:0]**	**DBA2**	**DA2**	**DA1**	**DA0**	**Meaning**
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	HLLL	X	X	X	X	Ilegal Input States
None	n/a	LHLL	X	X	X	X	
None	n/a	LLHL	X	X	X	X	
None	n/a	LLLH	X	X	X	X	
Control word 0	RC0	LLHH or HHLL or LLLL	L	L	L	L	Global Features Control word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2		L	L	H	L	Timing Control word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6		L	H	H	L	Reserved, free to use by vendor
Control word 7	RC7		L	H	H	H	Reserved, free to use by vendor
Control word 8	RC8		H	L	L	L	Additional IBT Setting Control Word
Control word 9	RC9		H	L	L	H	Power Saving Settings Control word
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11		H	L	H	H	Encoding for RDIMM Operating V_{DD}
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

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CONTROL WORD FUNCTIONS

The following sections describe the contents of each control word.

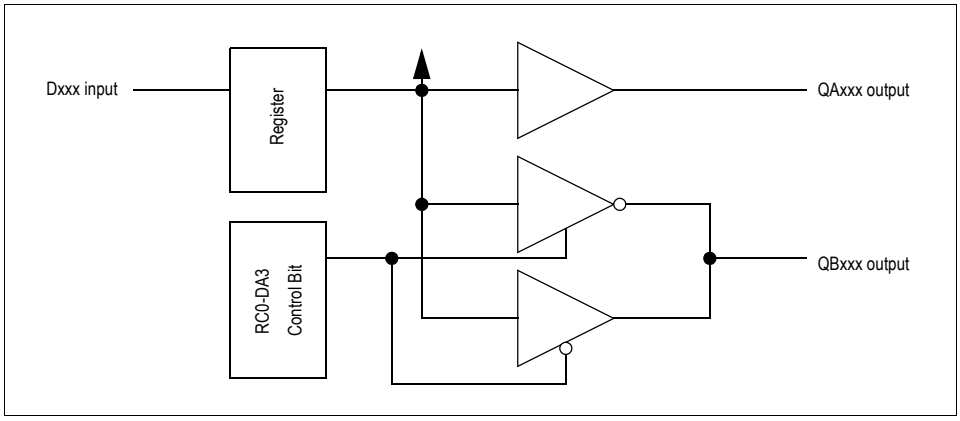
RC0: Global Features Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Output Inversion	Output Inversion enabled
x	x	x	1		Output Inversion disabled
x	x	0	x	Float outputs	Float disabled
x	x	1	x		Float enabled
x	0	x	x	A outputs disabled	A outputs enabled
x	1	x	x		A outputs disabled
0	x	x	x	B outputs disabled	B outputs enabled
1	x	x	x		B outputs disabled

Output Inversion: When Output Inversion is disabled, all A and B output drivers of the SSTE32882KB1 are driven to the same levels.

Output Inversion may be enabled to conserve power, reducing simultaneous switching output currents in the SSTE32882KB1. When Output Inversion is enabled, all A outputs will follow the equivalent inputs, however the following B outputs will be driven to the complement of the matching A output: QBA03-QBA9, QBA11, QBA13 - QBA15, QBBA0 - QBBA2. Output Inversion does not affect SSTE32882KB1 control word programming.

Output Inversion Functional Diagram



Output floating refers to allowing many A/B outputs to enter a hi-Z state when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g., V_{DD}, V_{TT}, or V_{SS}). When output floating is enabled, the following outputs (on both matching A and B outputs) are hi-Z when not actively driven: QxAn, QxBAn, $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, and $\overline{\text{QxWE}}$. Output floating is independent of Output Inversion and does not affect SSTE32882KB1 control word programming.

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A or B output disable allows the use of the SSTE32882KB1 in reduced parts count applications such as DDR3 Mini-RDIMMs. When output disable is asserted, all outputs on the corresponding side of the register, including the clock drivers, remain in Hi-Z at all times. When RC0[DBA0] = 1, all A-side Q-outputs and Y1 and Y3 outputs will be disabled. When RC0[DBA1] = 1, all B-side Q-outputs and Y0 and Y2 outputs will be disabled. When RC0[DBA0] = 1 and RC0[DBA1] = 1, all A-side and B-side Q-outputs and Yn outputs will be disabled.

RC1: Clock Driver Enable Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Disable Y0/$\overline{Y0}$ clock	Y0/$\overline{Y0}$ clock enabled
x	x	x	1		Y0/$\overline{Y0}$ clock disabled
x	x	0	x	Disable Y1/$\overline{Y1}$ clock	Y1/$\overline{Y1}$ clock enabled
x	x	1	x		Y1/$\overline{Y1}$ clock disabled
x	0	x	x	Disable Y2/$\overline{Y2}$ clock	Y2/$\overline{Y2}$ clock enabled
x	1	x	x		Y2/$\overline{Y2}$ clock disabled
0	x	x	x	Disable Y3/$\overline{Y3}$ clock	Y3/$\overline{Y3}$ clock enabled
1	x	x	x		Y3/$\overline{Y3}$ clock disabled

Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK/$\overline{CK}$ unless the system stops the clock inputs to the SSTE32882KB1 to enter the lowest power mode.

RC2: Timing Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Address- and command-nets pre-launch (Control Signals QxCKE, QxCS, QxODT do not apply)	Standard (1/2 Clock)
x	x	x	1		Address and command nets pre-launch (3/4 Clock)
x	x	0	x	1T/3T Output timing	1T timing
x	x	1	x		3T timing(1)
x	0	x	x	Input Bus Termination(2)	100 Ω
x	1	x	x		150 Ω
0	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x		Test Mode (Frequency Band 2)

1 There is no floating once 3T timing is activated.

2 If MIRROR is 'HIGH' then Input Bus Termination (IBT) is turned off, or on all inputs except the $\overline{DCSn}$ and DODTn inputs.

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The IBT control is also located in this control word, with two options of 100Ω or 150Ω which can be selected to adapt to different system scenarios. At power-up, the SSTE32882KB1 IBT defaults to 100Ω. The system controller can reprogram the termination resistance to 150Ω by setting this bit. Only the DAn, DBAn, $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{DCSn}}$, DODTn, DCKEn, and PAR_IN inputs have the IBT. The CK, $\overline{\text{CK}}$, FBIN, $\overline{\text{FBIN}}$, RESET, and MIRROR inputs do not have IBT.

Effective IBT Tolerance Requirement

	Min	Max
Total Effective IBT Value Tolerance[1]	-10%	+10%

1 Example: for 100 Ohm IBT, Min = 90 Ohms, Max = 110 Ohms

Mismatch Tolerance Between R-IBT-Up and R-IBT-Down

	Max
Mismatch Tolerance Between R-IBT-Up and R-IBT-Down[1]	ABS(5%)

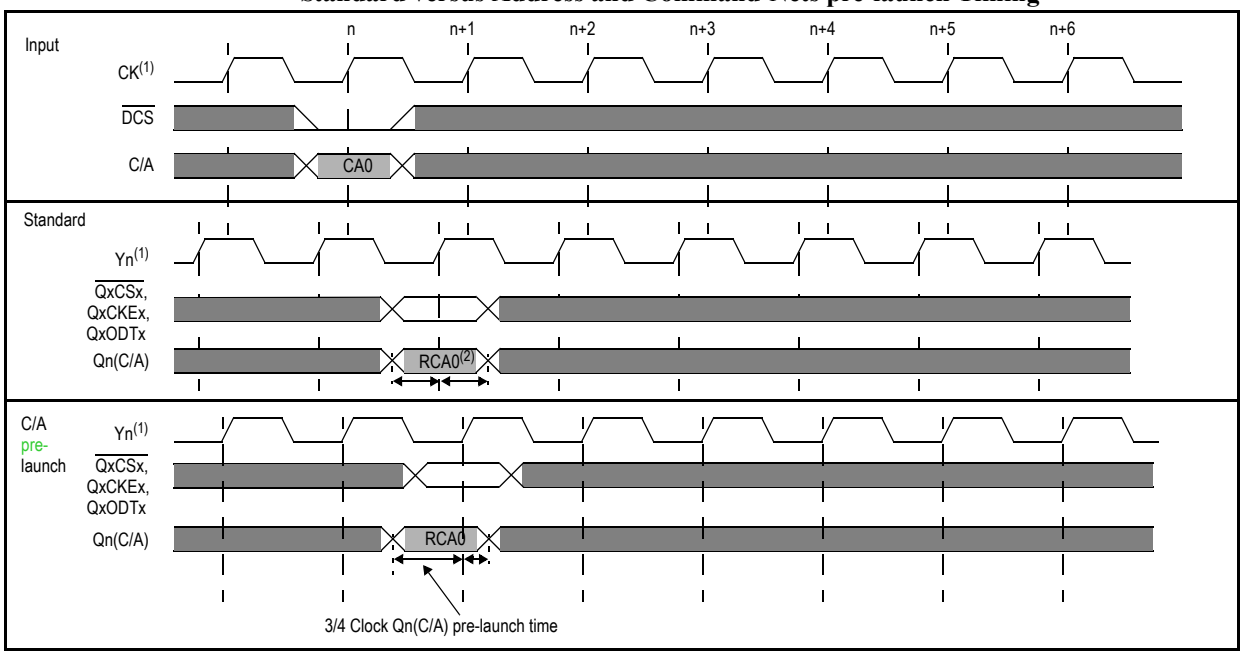
1 (1 - R-IBT-Up/R-IBT-Down) *100% < ABS(5%)

If MIRROR is ‘HIGH’ then it is assumed the register is located on the back side of a module where two registers are tied together on the input side. In this case, for the register on the back side, the IBT are turned off on all inputs except the $\overline{\text{DCSn}}$ and DODTn inputs.

The following diagram illustrates the pre-launch feature whereby double loaded nets in a 2-rank configuration can be driven with an earlier signal compared to output clock and control in order to compensate for the slower signal travel speed. This timing applies at all supported frequencies.

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Standard versus Address and Command-Nets pre-launch Timing



1 $\overline{CK}$ and $\overline{Yn}$ left out for better visibility.

2 RCA0 is re-driven command address signal based on input CA0.

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals =QxA0-QxAn, QxBA0-QxBAn, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$
- Control Signals = $\overline{QxCSn}$, QxCKEn, QxODTn
- CK = Yn .. $\overline{Yn}$

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RC3: CA Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Command/Address Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Command/Address Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

RC4: Control Signals Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Control Driver-A Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Reserved
x	x	1	1		Reserved
0	0	x	x	Control Driver-B Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Reserved
1	1	x	x		Reserved

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RC5: CK Driver Characteristics Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Clock Y1, $\overline{Y1}$, Y3, and $\overline{Y3}$ Output Drivers	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Reserved
0	0	x	x	Clock Y0, $\overline{Y0}$, Y2, and $\overline{Y2}$ Output Drivers	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Reserved

RC8: Additional IBT Setting Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	IBT Compatibility Settings	IBT as defined in RC2
0	x	x	x	Mirror Mode	IBT Off when MIRROR is HIGH[1]
1	x	x	x		IBT On when MIRROR is HIGH[2]
x	0	0	1	Input Bus Termination[1]	Reserved
x	0	1	0		200Ω
x	0	1	1		Reserved
x	1	0	0		300Ω
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Off[3]

1 If MIRROR is HIGH, then Input Bus Termination (IBT) is turned off on all inputs, except $\overline{DCSn}$ and DODTn inputs.

2 When DBA0 = 1, DA4 = 1, or DA3 = 1, IBT on all inputs is turned off no matter what the DBA1 setting may be.

3 With this setting, no matter what the logic level of the MIRROR input pin may be, IBT on all inputs (including $\overline{DCSn}$ and DODTn) is turned off.

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RC9: Power Saving Settings Control Word

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	x	0	Weak Drive Mode (when $\overline{DCS}$n=high, DA3=1 and RC0[DA4=1])	Floating as defined in RC0 [DA4]
x	x	x	1		Typical weak drive enabled[1] Weak Driver Impedance: 70Ω (min), 100Ω (nom), 120Ω (min)
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
1	0	x	x	CKE Power Down Mode	CKE power down with IBT ON, QxODT is a function of DxODT
1	1	x	x		CKE power down with IBT off, QxODT held LOW
0	x	x	x	CKE Power Down Mode Enable	Disabled
1	x	x	x		Enabled

1 When all $\overline{DCS}$ pins are HIGH (i.e. SDRAM is in deselected state), there is no memory access to the DRAM, and the Register output can either be in a Normal Drive Mode, floated, or driven under Weak Drive Mode. A Weak Drive Mode is a mode in which CA signal output drivers (QxA0-QxAn, QxBA0-QxBAn, $\overline{QxRAS}$, $\overline{QxCAS}$, $\overline{QxWE}$) will be driven 2.5 to 3 times weaker than the Light Drive as specified in RC3, and the SDRAM VIL/VIH DC limit will be maintained. The Weak Drive Mode entry and exit timing is bounded by tDIS and tEN respectively.

The SSTE32882KB1 features a weak drive mode, which is a variant of the floating mode set in RC0. If Bit DA4 of RC0 is set to '1', then Bit DA3 of RC9 selects between floating mode and weak drive mode.

The SSTE32882KB1 register supports different power down modes. By default, the Power Down feature is disabled (RC9[DBA1]=0). The register ignores CKE Power Down mode setting when this function is disabled. If the CKE Power Down mode is enabled (RC9[DBA1]=1), then power down is invoked once both DCKE0 and DCKE1 are low. Bit DBA0 selects how IBT and ODT behaves.

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RC10: Encoding for RDIMM Operating Speed

The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	0	0	0	f ≤ 800 MTS	DDR3/DDR3L/DDR3U-800 (default)
x	0	0	1	800 MTS < f ≤ 1066 MTS	DDR3/DDR3L/DDR3U-1066
x	0	1	0	1066 MTS < f ≤ 1333 MTS	DDR3/DDR3L/DDR3U-1333
x	0	1	1	1333 MTS < f ≤ 1600 MTS	DDR3/DDR3L/DDR3U-1600
x	1	0	0	1600 MTS < f ≤ 1866 MTS	DDR3-1866
x	1	0	1	1866 MTS < f ≤ 2133 MTS	DDR3-2133
x	1	1	0	Reserved	Reserved
x	1	1	1	Reserved	Reserved

RC11: Operating Voltage V_{DD} and V_{REFCA} Control Word[1]

RC11 is used to inform the SSTE32882KB1 under what operating voltage V_{DD} will be used. The register can use the information to optimize functionality and performance at DDR3L conditions.

Input				Definition	Encoding
DBA1	DBA0	DA4	DA3		
x	x	0	0	Register V_{DD} Operating Voltage	DDR3 1.5V mode
x	x	0	1		DDR3L 1.35V mode
x	x	1	0		DDR3U 1.25V mode
x	x	1	1		Reserved
x	0	x	x	Register VrefCA[2]	External VrefCA[2]
x	1	x	x		Internal VrefCA[2]
0	x	x	x		Reserved
1	x	x	x		Reserved

1. DDR3U 1.5 V, 1.35 V or 1.25 V register is backward compatible and operable to DDR3 & DDR3L specification. To guarantee all timings and specifications for DDR3 & DDR3L, the register must be configured accordantly.
2. Mandatory for all register supporting 1866 and beyond.

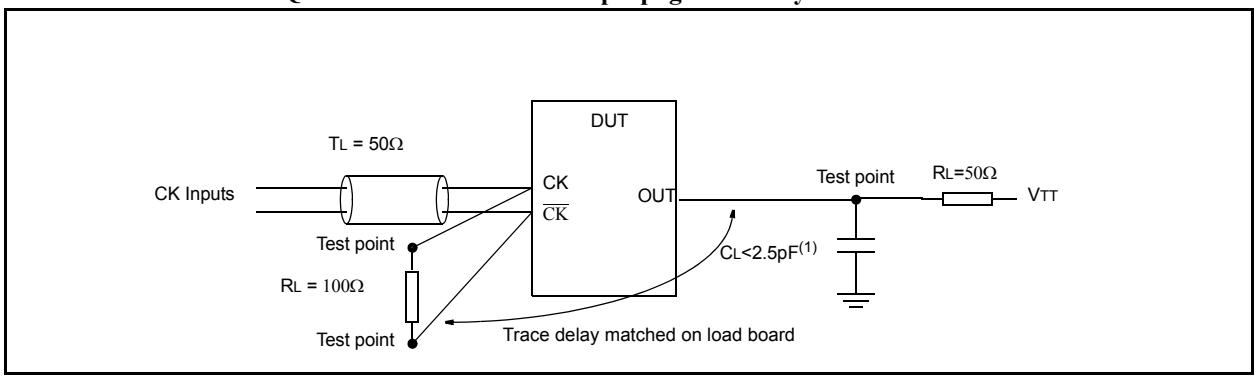
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Test Circuits and Switching Waveforms

Parameter Measurement Information

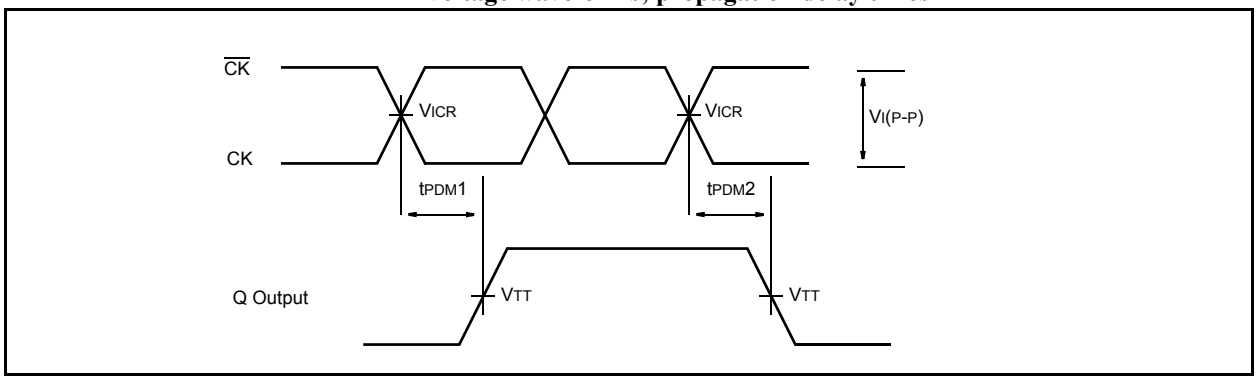
All input pulses are supplied by generators having the following characteristics: 300MHz ≤ PRR ≤ 945 MHz; Zo = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified. The outputs are measured one at a time with one transition per measurement.

Qn and Yn Load circuit for propagation delay and slew measurement



1 CL is parasitic (probe and jig capacitance).

Voltage waveforms; propagation delay times



VTT = VDD/2

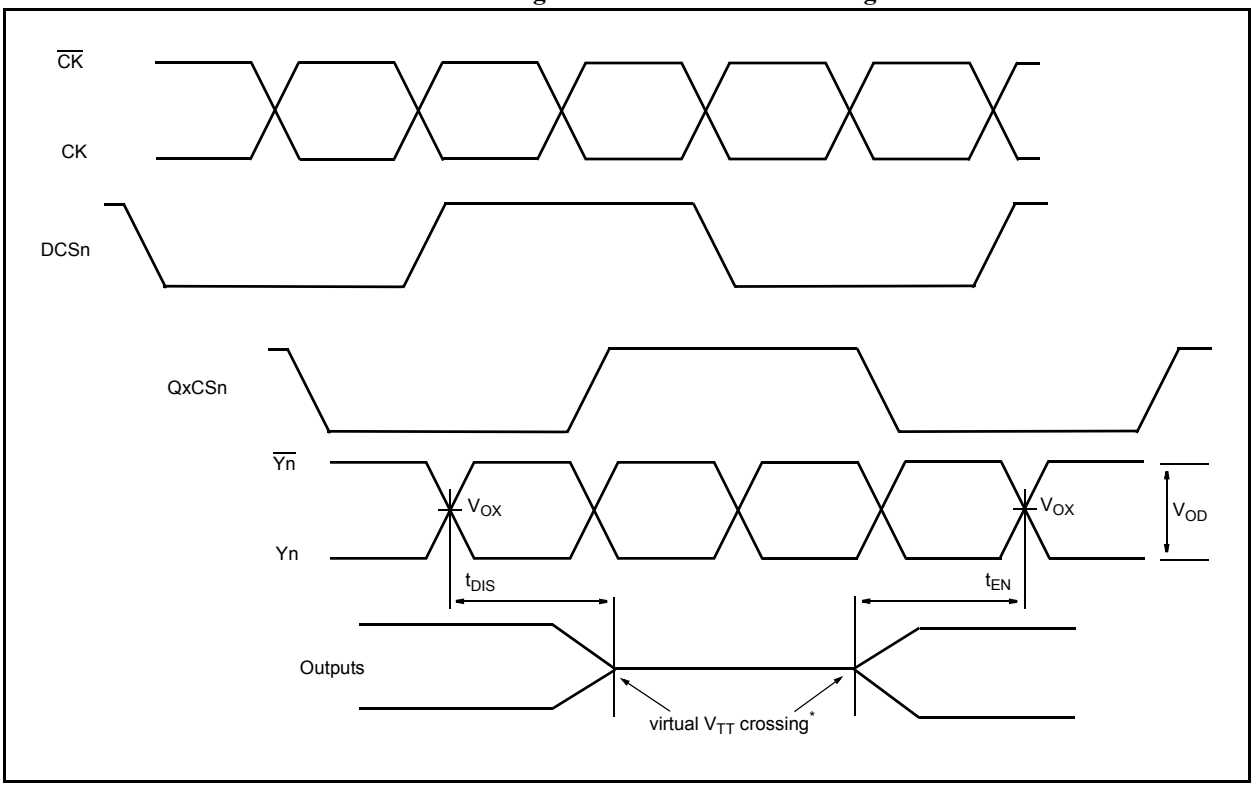
VICR Cross Point Voltage

VI(P-P) = 500mV (1.5V operation), 450mV (1.35V operation) or 400mv (1.25V operation).

tPDM1, tPDM2 the larger number of both has to be taken when performing tPDM max measurement, the smaller number of both has to be taken when performing tPDM min measurement.

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Voltage waveforms address floating

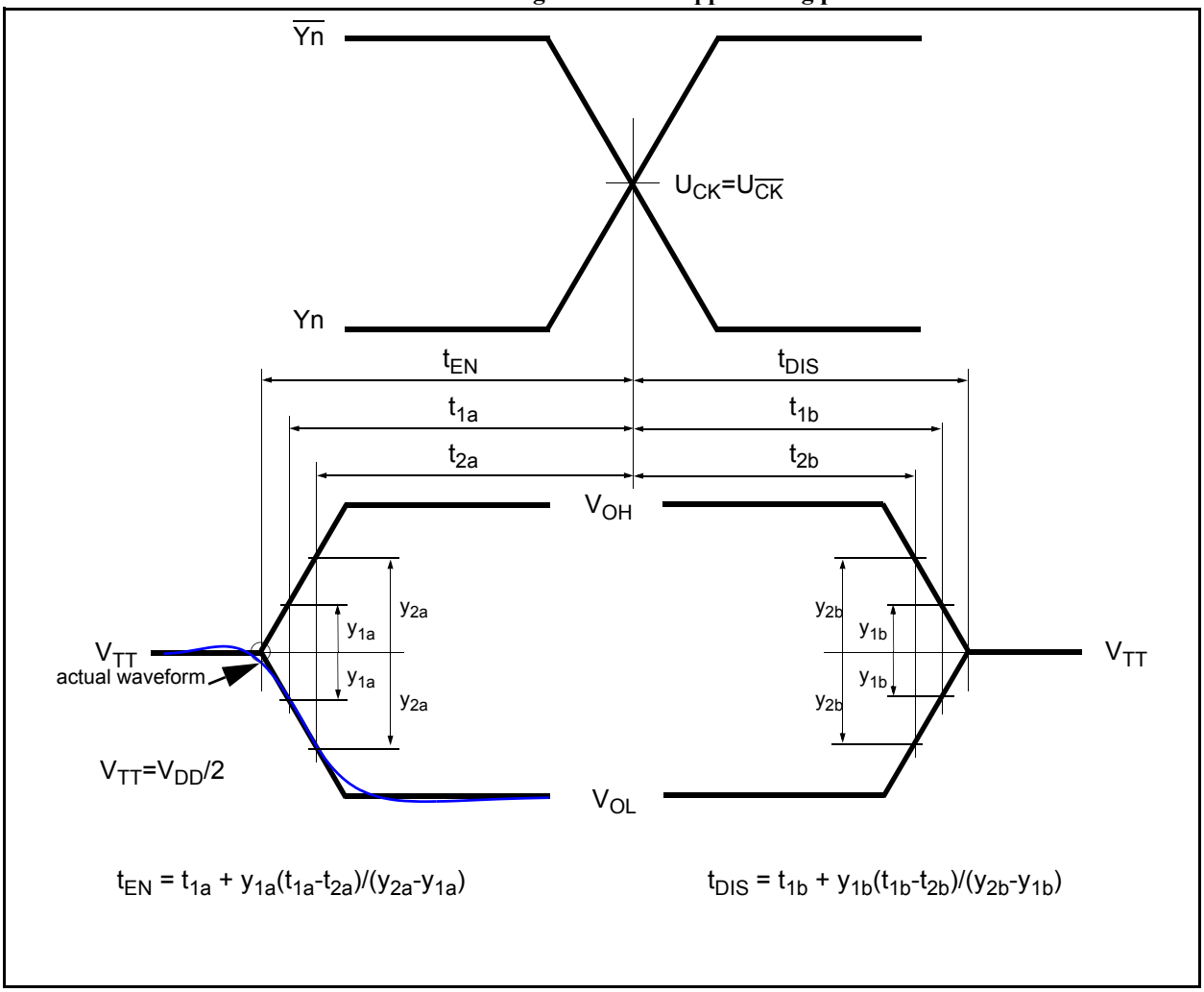


Refer to "Calculating the virtual V_{REF} crossing point".

Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occure later than the latest (HL/LH) transition. Regular transitions are measured between CK/$\overline{CK}$ and CA/V_{TT} crossings however a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in the Figure, "Calculating the virtual V_{TT} crossing point". The voltage levels for y_{xa} and y_{xb} are measured from V_{TT} (V_{DD}/2) and should be selected such that the region between t_1 and t_2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.

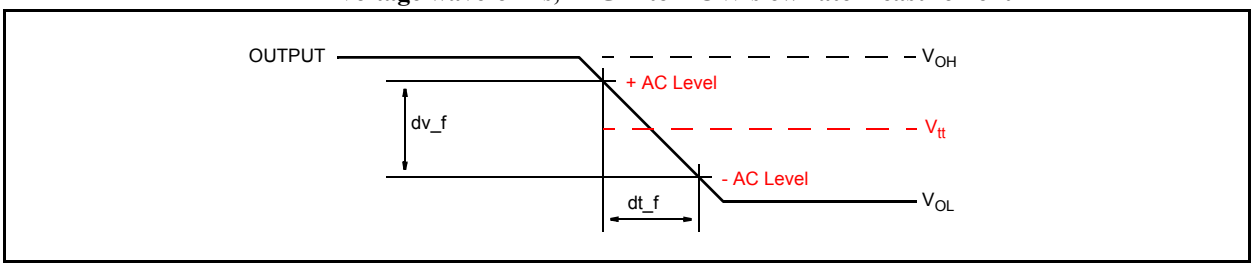
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Calculating the virtual V_{TT} crossing point

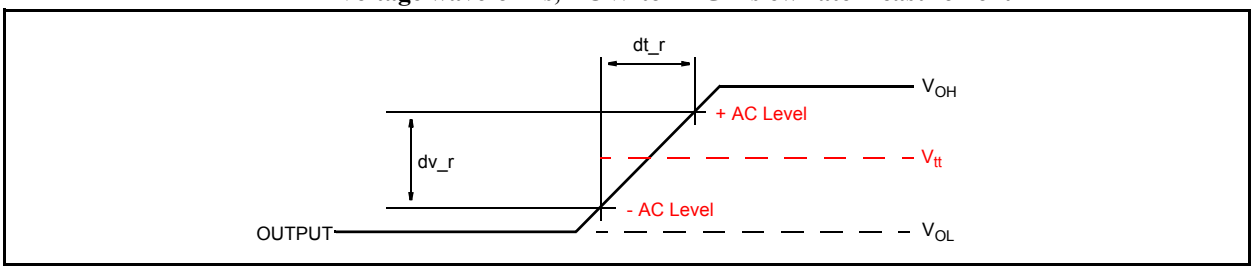


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Voltage waveforms, HIGH-to-LOW slew rate measurement



Voltage waveforms, LOW-to-HIGH slew rate measurement



AC Level for Slew Rate Measurement

	DDR3/DDR3L-800/1066/1333/1600	DDR3-1866
AC Level (1.5V)	150mV	135mv
AC Level (1.35V)	135mV	

AC Level for Slew Rate Measurement (DDR3U 1.25V)

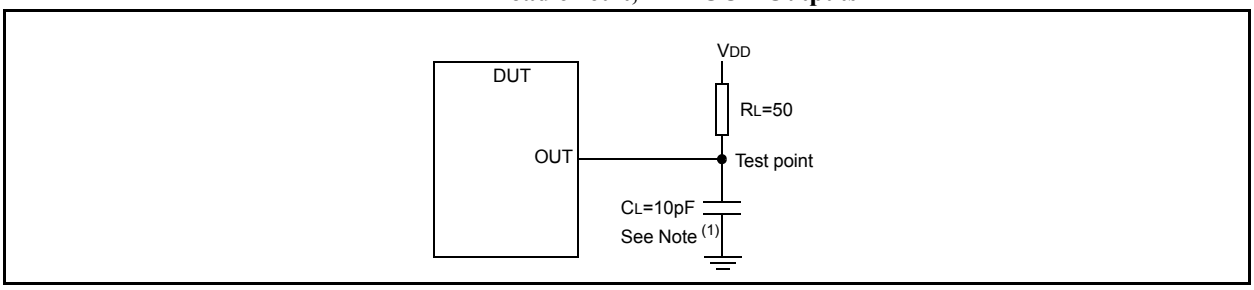
	DDR3U-800/1066/1333/1600
AC Level (1.25V)	125mV

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Error Output Load Circuit and Voltage Measurement Information

All input pulses are supplied by generators having the following characteristics: 300MHz ≤ PRR ≤ 945 MHz; Zo = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

Load circuit, $\overline{\text{ERROUT}}$ Outputs



1 CL includes probe and jig capacitance.

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The output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals =QxA0-QxAn, QxBA0-QxBAn, $\overline{\text{QxRAS}}$, $\overline{\text{QxCAS}}$, $\overline{\text{QxWE}}$
- Control Signals = $\overline{\text{QxCSn}}$, QxCKEn, QxODTn
- CK = Yn .. $\overline{\text{Yn}}$

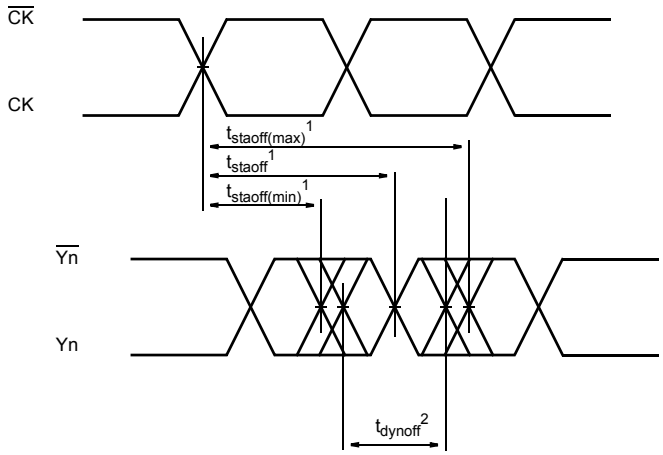
Register Output Slew-Rate & R-on Targets for Each Drive Strength as shown below.

Output Slew-Rate & R-on (targets)

Drive Settings	Output Driver R-on Targets (Ohms)			Output Slew-Rate (V/ns)					
				DDR3-800/1066/1333		DDR3-1600		DDR3L-800/1066/1333/ 1600	
	Min	Nom	Max	Min	Max	Min	Max	Min	Max
Light	22	26	30	2	7	2	5.5	1.8	5.0
Moderate	16	19	22	2	7	2	5.5	1.8	5.0
Strong	12	14	16	2	7	2	5.5	1.8	5.0

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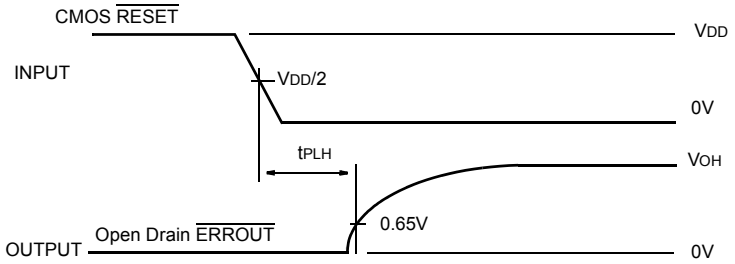
Measurement Requirement for tstaoff and tdynoff



1. t_{staoff} = propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge).

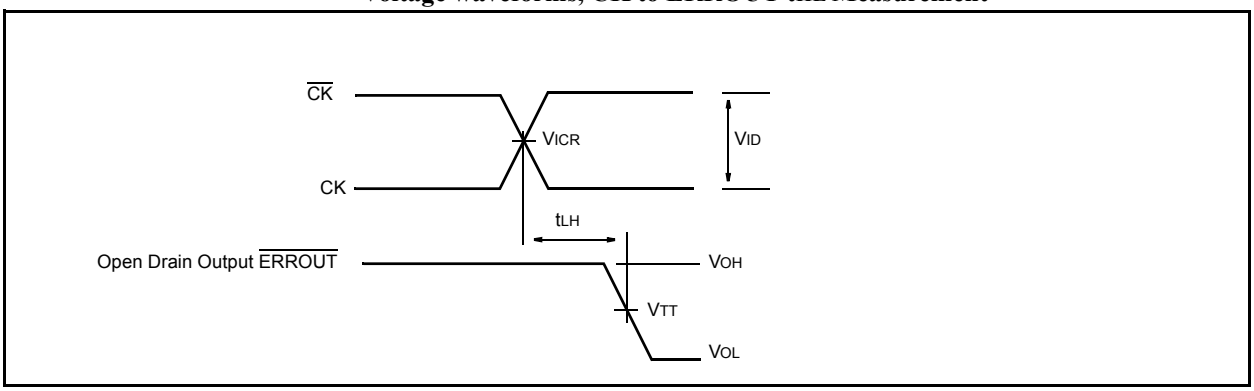
2. t_{dynoff} = maximum t_{staoff} variation over voltage and temperature.
This includes all sources of jitter and drift (e.g.Thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

Voltage waveforms, Reset to $\overline{\text{ERROUT}}$ t_{PLH} Measurement



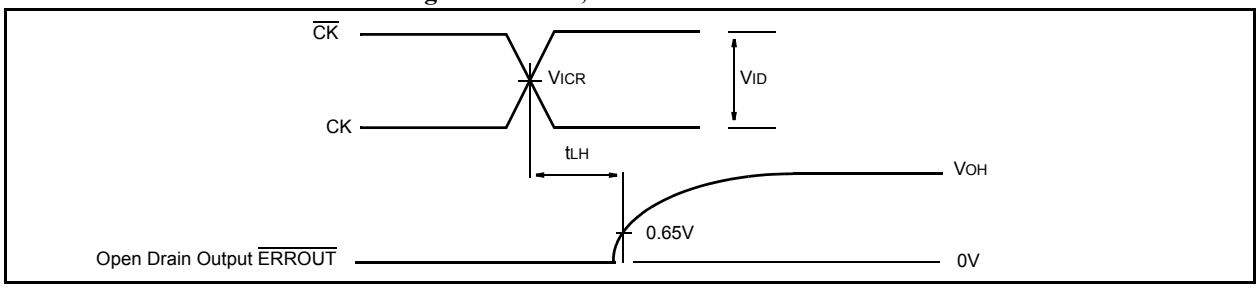
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Voltage waveforms, CK to $\overline{\text{ERROUT}}$ t_{HL} Measurement

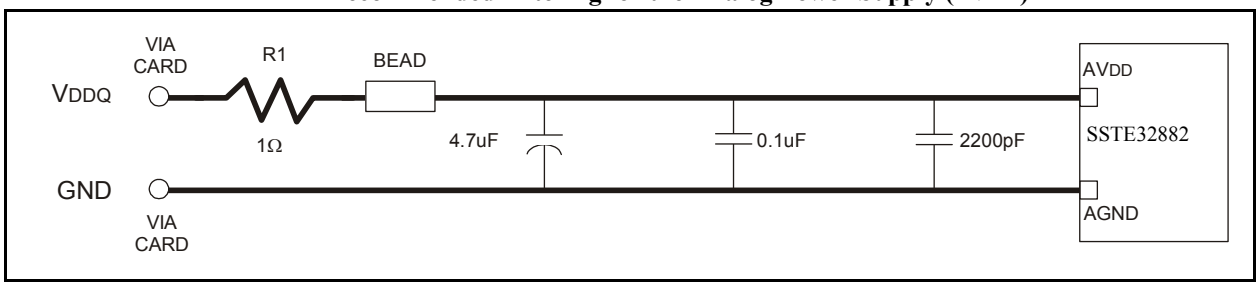


$V_{TT} = V_{DD}/2$

Voltage waveforms, CK to $\overline{\text{ERROUT}}$ t_{LH} Measurement



Recommended Filtering for the Analog Power Supply (AV_{DD})



Place the 2200pF capacitor close to the PLL.

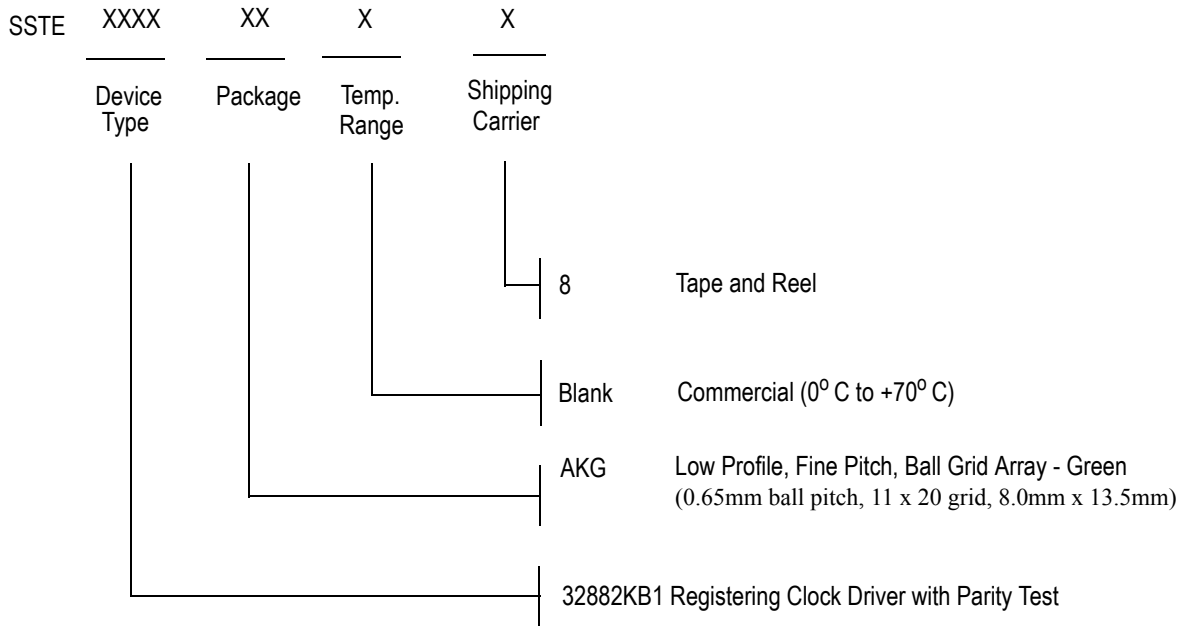
Use a wide trace for the PLL analog power and ground.

Connect PLL and caps to AGND trace and connect trace to one GND via (farthest from PLL).

Bead is 0.8Ω DC max, 600Ω at 100MHz.

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Ordering Information



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