Tsi308™ HyperTransport to PCI/X User Manual

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About this Document

This section discusses general document information about the *Tsi308 HyperTransport to PCI/X User Manual*. The following topics are described:

- "Scope" on page 13
- "Document Conventions" on page 13
- "Related Information" on page 15
- "Revision History" on page 15

Scope

The *Tsi308 HyperTransport to PCI/X User Manual* discusses the features, capabilities, and configuration requirements for the Tsi308. It is intended for hardware and software engineers who are designing system interconnect applications with these devices.

Document Conventions

This document uses a variety of conventions to establish consistency and to help you quickly locate information of interest. These conventions are briefly discussed in the following sections.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "n". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAMEn	NAMEn[3]
Active high	NAME	NAME[3]

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Object Size Notation

This document uses the following object size notation:

- A *byte* is an 8-bit object.
- A *word* is a 16-bit object.
- A *doubleword* (Dword) is a 32-bit object.

Numeric Notation

- Hexadecimal numbers are denoted by the prefix *0x*. For example, 0x04.
- Binary numbers are denoted by the prefix *0b*. For example, 0b010.
- Registers that have multiple iterations are denoted by {x..y} in their names; where *x* is first register and address, and *y* is the last register and address. For example, REG{0..3} indicates there are four versions of the register at different addresses: REG0, REG1, REG2, and REG3.

Symbols



This symbol indicates a basic design concept or information considered helpful.



This symbol indicates important configuration information or suggestions.



This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Document Status Information

User manuals are classified as Advance, Preliminary, or Final:

- Advance – Contains information that is subject to change, and is available once prototypes are released to customers.
- Preliminary – Contains information about a product that is near production-ready, and is revised as required.
- Final – Contains information about a final, customer-ready product, and is available once the product is released to production.

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Related Information

The following documents contain useful reference information for using this manual:

- *Tsi308 Device Errata and Design Notes*

Revision History

80D4000_MA001_04, Formal, September 2009

This document was rebranded as IDT. It does not include any technical changes.

80D4000_MA001_03, Preliminary, January 2007

This is the current release of the user manual. There have been slight modifications throughout the manual.

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1. Functional Description

This chapter discusses the following topics about the Tsi308:

- "Overview" on page 18
- "Features" on page 19
- "HyperTransport Interface" on page 20
- "PCI-X Interface" on page 21
- "Interrupt Controller" on page 23
- "Interface Levels" on page 23
- "Clocking" on page 24
- "Reset" on page 24

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1.1 Overview

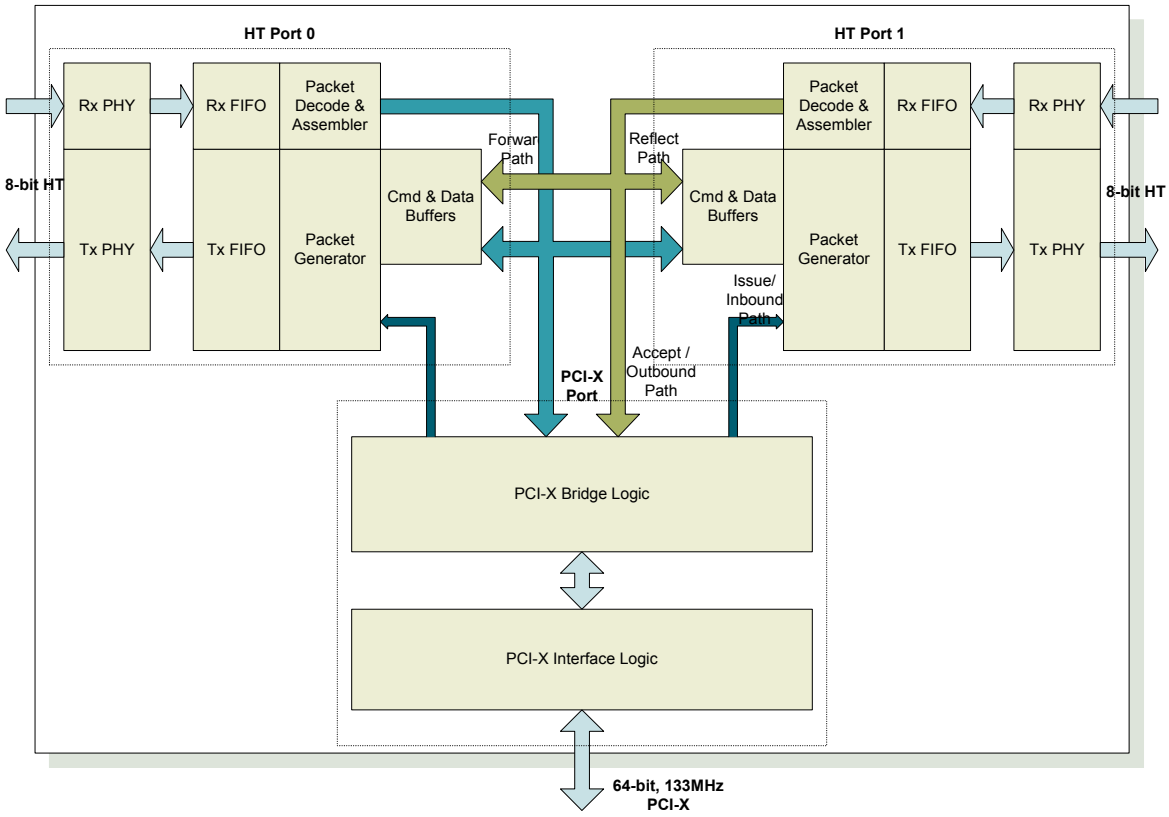
The Tsi308 is HyperTransport™-to-PCI-X Bridge that interfaces the new generation of HT based microprocessors and micro controllers to PCI or PCI-X based peripherals. It also connects HT based hosts to HT based peripherals.

The Tsi308 can be configured to support either single 64-bit PCI-X bus or two 32-bit PCI-X buses. The Tsi308 implements two bi-directional 8-bit HyperTransport™ interfaces that provide 1200 MByte per second of bandwidth in each direction. Up to 31 devices can be daisy-chained to build higher capacity systems with multiple PCI-X busses and HT based peripherals. A fairness algorithm allocates bandwidth among devices, thereby eliminating starvation of bridges at the end of the chain.

The Tsi308 breathes new life into systems that are encumbered by the limits of traditional PCI or PCI-X based fabrics. It reduces the time to market, design complexity and system costs of PCI-X and HT based systems.

The block diagram for Tsi308 is shown Figure 1 on page 18.

Figure 1: Tsi308 Block Diagram



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1.2 Features

The following sections describe the features of Tsi308.

1.2.1 General features

- Two Bidirectional 8-bit HyperTransport™ interfaces
  - Up to 600MHz DDR (Double Data Rate) for peak bandwidth of 1200 MB/s simultaneously in each direction
- Complies with Revision 1.05 of HyperTransport™ I/O Link Specification
  - Maximum link width supported is only 8-bits
  - Supports asymmetric link widths and frequencies
- Tunnels between the two HyperTransport™ interfaces
- Can be configured as single-ended cave device with only one link active
- The HT interfaces support double hosted chain (Host CPU on each port)
- Single 64-bit PCI-X bus or two 32-bit PCI-X buses
  - Device emulates two HT link devices (with virtual internal tunnel in dual PCI-X mode)
  - Implements two independent sets of CSRs in dual PCI-X mode
  - PCI-X bus can also operate in traditional PCI mode
  - Operating frequencies and mode of the two PCI-X buses are independently selectable
  - Supports 50, 66, 100 and 133 MHZ in PCI-X mode
  - Supports 25, 33, 50 and 66 MHZ in PCI mode
  - PCI-X mode complies to Revision 1.0b of PCI-X Addendum to the PCI Local Bus Specification
  - PCI mode complies to Revision 2.2 of PCI Local Bus Specification
- Supports Tsi301 software backward compatibility mode through hardware strap setting
- Supports daisy-chaining up to 31 devices. The bandwidth is shared among the devices using a fairness algorithm
- Programmable interrupt controller with up to 10 interrupts per PCI-X port
- Built-in 2-level PCI-X arbiter with support for up to 6 devices
  - Also supports external arbiter
- Transaction forwarding for the following commands
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands (downstream only)

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- *Type 1 to Type 0 configuration commands (downstream only)*

- Internal buffers to support high-speed operation, including:
  - 1536-bytes HT forwarding (512 bytes each for posted, non-posted and response)
  - Following buffers are supported for each PCI-X port
    - 1024-bytes upstream write (posted)
    - 2048-bytes upstream read (non-posted), among up to four outstanding requests
    - 512-bytes downstream write (posted)
    - 512-bytes downstream read (non-posted)
- 64-bit memory mapped space and 25-bit I/O space
- 64-bit Address Remapping (downstream) and one DMA Window (upstream)
- Full UnitID Clumping support
- Supports 64-bit Address Extension
- Evaluation board available with firmware and software drivers
- 6 Watt max, 1.8V core, 1.2V HT I/O, 3.3V PCI I/O
- Optional 5V tolerant PCI I/O in standard PCI mode while operating at 25 or 33 MHZ
- 388-pin HSBGA package
- Compatible with x86 systems
- Supports Online Insertion and Removal
- Supports Boundary scan
- Software and Hardware compatibility Revision A & Revision B

1.3 HyperTransport Interface

The Tsi308 HyperTransport-to-PCI-X bridge primary interface is a HyperTransport tunnel. The primary interface is compliant with HyperTransport™ I/O Link Specification, Revision 1.05. The interface contains two HyperTransport links, which allow the connection of multiple bridge, chips in a daisy-chain configuration. As shown in the figure above Tsi308 can be configured to behave as two independent tunnel devices that are connected through a virtual internal tunnel. In this mode each tunnel device can host a 32-bit PCI-X bus. The programming in this mode is pretty much transparent to software in a way that software treats them as if they are independent devices or chips.

Each HyperTransport link has an 8-bit DDR transmit and an 8-bit DDR receive port running at clock speeds up to 600 MHz, allowing for raw bandwidth of 1200 MB/s simultaneously in each direction.

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- For testing or connection to slower devices, the Tsi308 may be programmed to operate at slower link clock rates
- The Tsi308 supports both the synchronous and asynchronous modes of link initialization

1.4 PCI-X Interface

The Tsi308 secondary interface is a 64-bit, 133 MHz capable PCI-X bus that can be configured to have two completely independent 32-bit buses in split bus mode including buffer space and transaction handling. The two PCI-X ports are identical in split bus mode and the subsequent description applies to each port. The PCI-X interface can operate at 50, 66, 100 and 133 MHz, which can also operate at 25, 33, 50 and 66 MHz while operating in traditional PCI mode. Additionally PCI-X bus can be configured for compatibility with 3.3V or 5.0V operation while operating at up to 33 MHz in traditional PCI mode. At higher frequencies of PCI or while in PCI-X mode only 3.3V is supported.

The Tsi308 supports the full 64-bit memory-mapped space and 25-bit I/O space described in HyperTransport™ I/O Link Specification, Revision 1.05. In addition device supports 64-bit address remapping capability and a single upstream DMA window. PCI dual address cycle (DAC) support is provided both inbound and outbound to support memory-mapped space.

- The Tsi308 supports configuration accesses to devices 0-15, using Address/Data bits 16-31 for IDSEL#.
- The Tsi308 implements all parity and error checking features described in *PCI Local Bus Specification, Revision 2.2*.

1.4.1 PCI-X Master

As a PCI-X master, the Tsi308 chip can generate MemRd, MemWr, ConfigRd and ConfigWr cycles.

- The Tsi308 does not implement a cacheline size register and does not prefetch to PCI, so it never generates MemRdLine, MemRdMult or MemWrInv cycles.
- The Tsi308 does generate *Memory Read Block* but does not generate *Memory Write Block* cycles in PCI-X mode
- The Tsi308 does not support a Southbridge connection to PCI bus, so it never generates INTA cycles.
- The Tsi308 does not support burst I/O and burst Configuration cycles initiated from Host. These transactions are target aborted inside the chip and does not appear on the PCI-X bus.

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PCI-X master cycles that are retried or disconnected on the PCI-X bus are reissued locally by the Tsi308 until they complete. The Tsi308 can track up to two outstanding requests in the Outbound Request Controller, of which one is reserved for posted requests. The other one is used for either posted or non-posted. The reserved posted buffer allows the passage of posted requests in case of blockage of non-posted requests.

In addition to two request-tracking buffers, Tsi308's PCI-X port has 512 byte buffer spaces each for posted and non-posted requests.

1.4.2 PCI-X Slave

As a PCI-X slave, the Tsi308 can respond to all types of memory and I/O cycles. However, the Tsi308 never responds to PCI-X configuration cycles.

- The Tsi308 employs medium DEVSEL# timing.
- All PCI-X slave writes are posted excluding I/O writes which is non-posted.
- A total of 1024 bytes of buffering is provided on chip for posted requests
- All PCI-X slave reads are implemented as delayed requests (PCI) or split (PCI-X), with up to four requests outstanding at once and a maximum of 512 byte buffering is provided for each outstanding request to store the response data received from HT.
- Fast back to back transactions are supported.

Prefetching is supported for all flavors of memory read cycle while operating in standard PCI mode, which separate prefetch controls for each cycle type and a maximum prefetch per read of 512 bytes. Prefetching may be done once at the beginning of each read, or it may be enabled to continuously issue requests as data is drained to PCI. All prefetch data is discarded when the read disconnects on the PCI bus. The bridge chip provides buffer space for a total of 2048 bytes of read prefetch data per PCI-X port.

While operating in PCI-X mode, Tsi308 fetches only enough bytes to satisfy the byte count field that appears in the attribute phase of all PCI-X burst transactions. The Tsi308 can support any sized request up to 4096 bytes as specified in [2]. However since Tsi308 has only 512-byte buffer to store the read data per request, it will continue to fetch data from HyperTransport as the buffer is drained on to PCI-X in chunks of single ADB.

1.4.3 PCI-X Arbiter

The Tsi308 implements an on-chip PCI Arbiter with 6 request/grant pairs. The request/grant pairs include a high-priority set for the on-chip PCI master, and five symmetrical sets for external device use.

All connections to the arbiter are through external pins, to use internal arbiter user has to route request/grant outputs back into chip connecting to any of the six request/grant pairs. So Tsi308 can automatically be configured to interface to external arbiter.

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1.5 Interrupt Controller

The Tsi308 implements a HyperTransport interrupt controller. It supports 10 external interrupt sources per PCI port. To program interrupts Tsi308 implements *Interrupt Discovery and Configuration Capability Block* and associated *Interrupt Definition Registers* for each interrupt source. Each interrupt can independently be enabled and programmed to be level or edge-triggered and active high or low. In order for to be software compatible to previous generation Tsi301 chip, Tsi308 also implements an alternate register map to program the interrupts in a non-standard way. However these registers are visible to software only when Tsi308 is operating in Tsi301 software compatible mode by hardware strap settings and this is the only means to program interrupts in Tsi301 mode.

1.6 Interface Levels

A complete pinout of the Tsi308 is provided in the *Signals Chapter*. The grouping of signal types is shown in Table 1.

Table 1: HyperTransport PCI-X Bridge Interface Voltages

Interface	Group	Voltages
PCI/PCI-X	PCI	3.3 V, 5.0 V tolerant (while operating in standard PCI mode at or below 33 MHz clock frequency)
HyperTransport	HT	Differential, 600 mV swing, centered on 600 mV
Interrupts	MISC	1.8 V
Miscellaneous	MISC	1.8 V

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1.7 Clocking

During functional operation, the Tsi308's reference clocks (P0_CLK and P1_CLK) come from respective PCI-X bus clocks. These clocks are received from same sources that drive clocks to devices on the bridge's PCI-X buses and are nominally in phase with them; although they may be delayed relative to other PCI-X bus clocks. The P1_CLK is only used to clock the PCI-X interface logic of second PCI-X port (PCI_B) while the device is operating in split bus mode. The reference clock frequencies and bus mode (traditional PCI or PCI-X) are indicated by Px_M66EN, Px_PCIX_N and Px_133_N input pins where x denotes PCI-X bus (0 for PCI_A and 1 for PCI_B). The Px_PCIX_N and Px_133_N are normal TTL level signals derived from standard 3-state add-in card connector pin PCIXCAP. Since Tsi308 does not decode PCIXCAP, user has to implement an external three-level Comparator circuitry to generate Px_PCIX_N and Px_133_N. A reference circuit can be found in [3]. Though three pins above indicate operating mode (PCI or PCI-X) and frequency group (33MHz or 66 MHz or 133 MHz), Tsi308 needs exact operating frequency of a given bus to generate internal clocks as well as to generate PCI-X Initialization Pattern for devices on PCI-X bus as specified in [3]. This is done through hardware straps. These straps are sampled using combinational logic while warm/cold reset is in progress and used to combinationally generate PCI-X initialization pattern that is sampled by devices on PCI-X bus at the rising edge of PCI reset. Refer Chapter 4 for more details on Clocking and Hardware strap settings.

1.8 Reset

All the internal resets of Tsi308 and resets for secondary PCI-X ports are derived from HyperTransport PWROK and RESET# signals. The combination of these two signals defines ColdReset and WarmReset windows on HyperTransport chain. While PWROK is implemented as input-only, RESET# is implemented as in-out in Tsi308. The asserted state of RESET# is stretched by Tsi308 and released after internal PLLs are locked. The PCI-X and CORE PLLs are only reset upon ColdReset but WarmReset resets HyperTransport PLLs. This way software could re-program link frequencies and issue WarmReset for new frequencies to take effect.

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2. Interface Operation

This chapter discusses the following topics about the Tsi308:

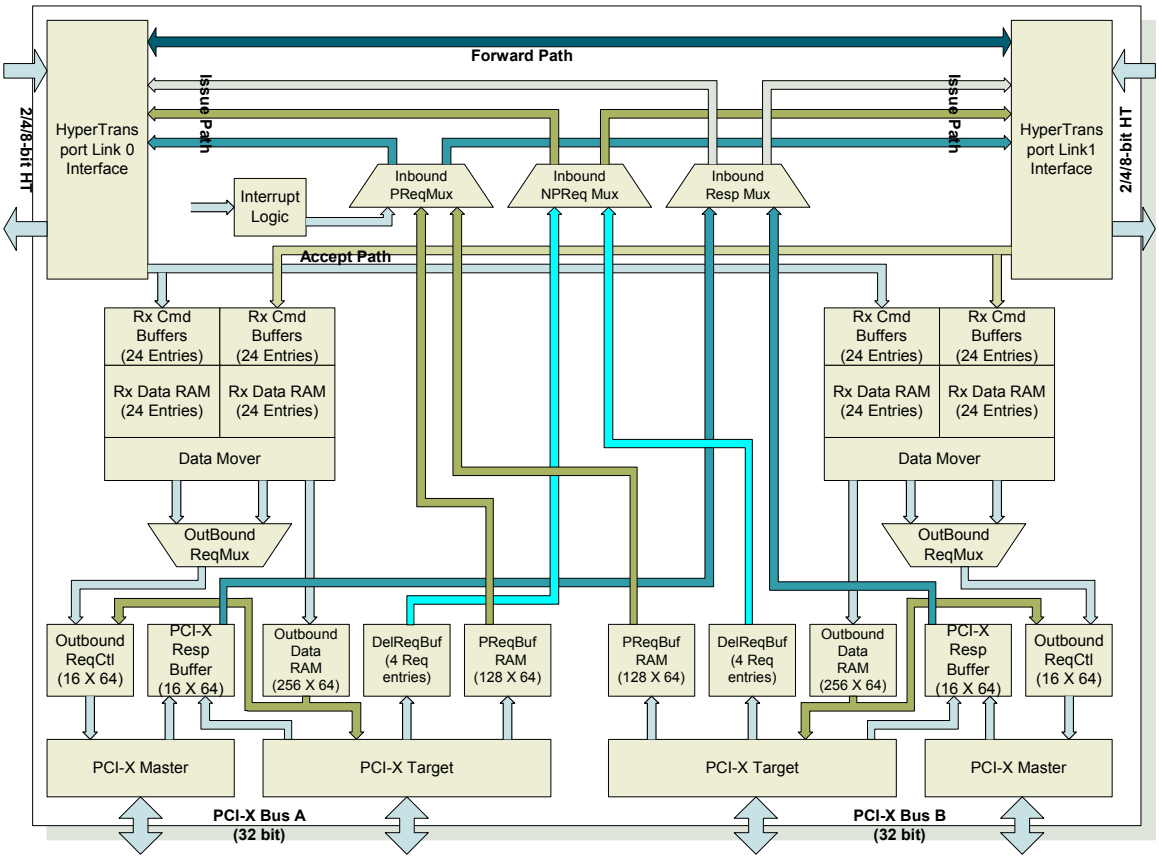
- "Overview" on page 25
- "HyperTransport Interface" on page 27
- "Outbound Transactions" on page 34
- "Inbound Transactions" on page 36
- "PCI-X Arbiter" on page 41
- "Online Insertion and Removal (OIR)" on page 42
- "LDTSTOP# Support" on page 42
- "Power Management" on page 43
- "Reset" on page 43
- "Error Handling" on page 45
- "Test Features" on page 52

2.1 Overview

This chapter details the operation of the HyperTransport-to- PCI-X Bridge chip.

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Figure 2: Block Diagram



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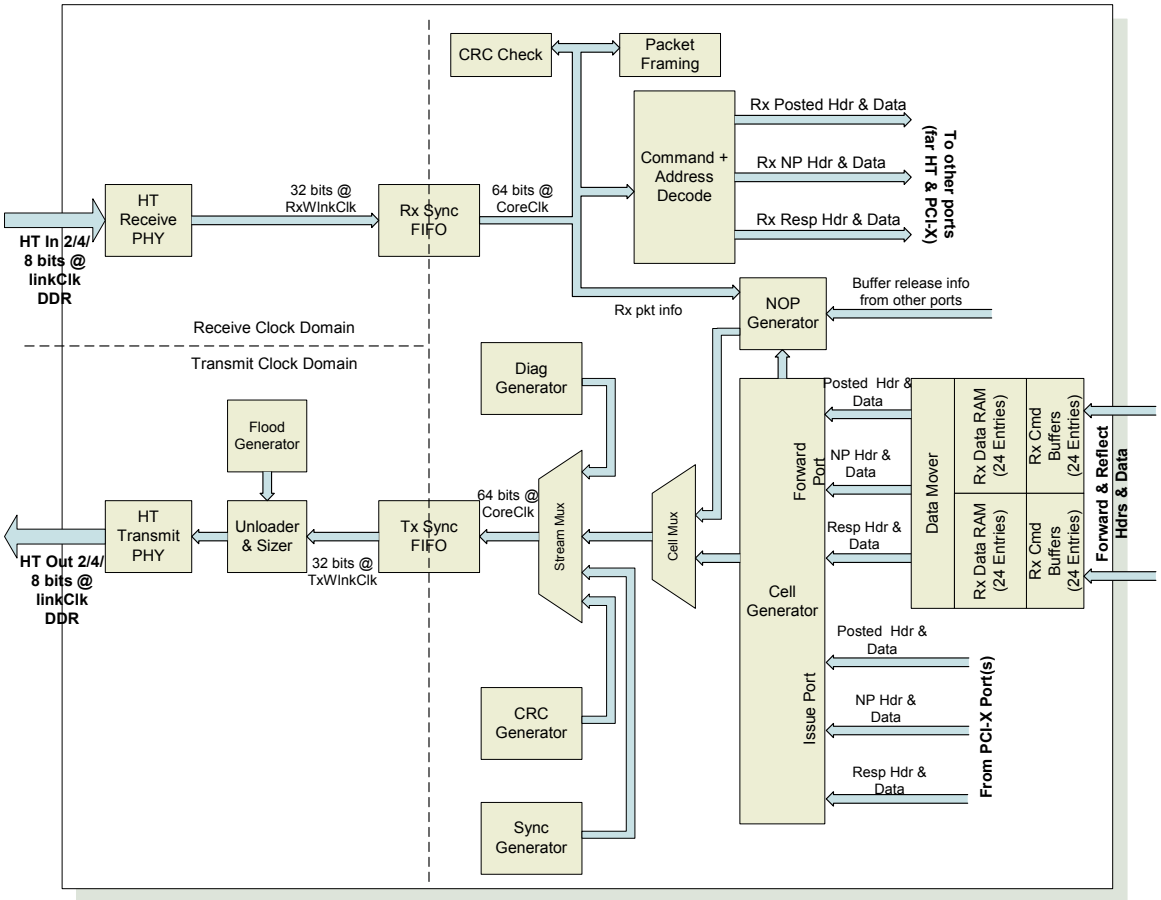
2.2 HyperTransport Interface

The Tsi308 HyperTransport interface consists of two identical link interfaces, each with a HyperTransport transmitter and receiver. Some central reset and error-handling logic is shared between the two links.

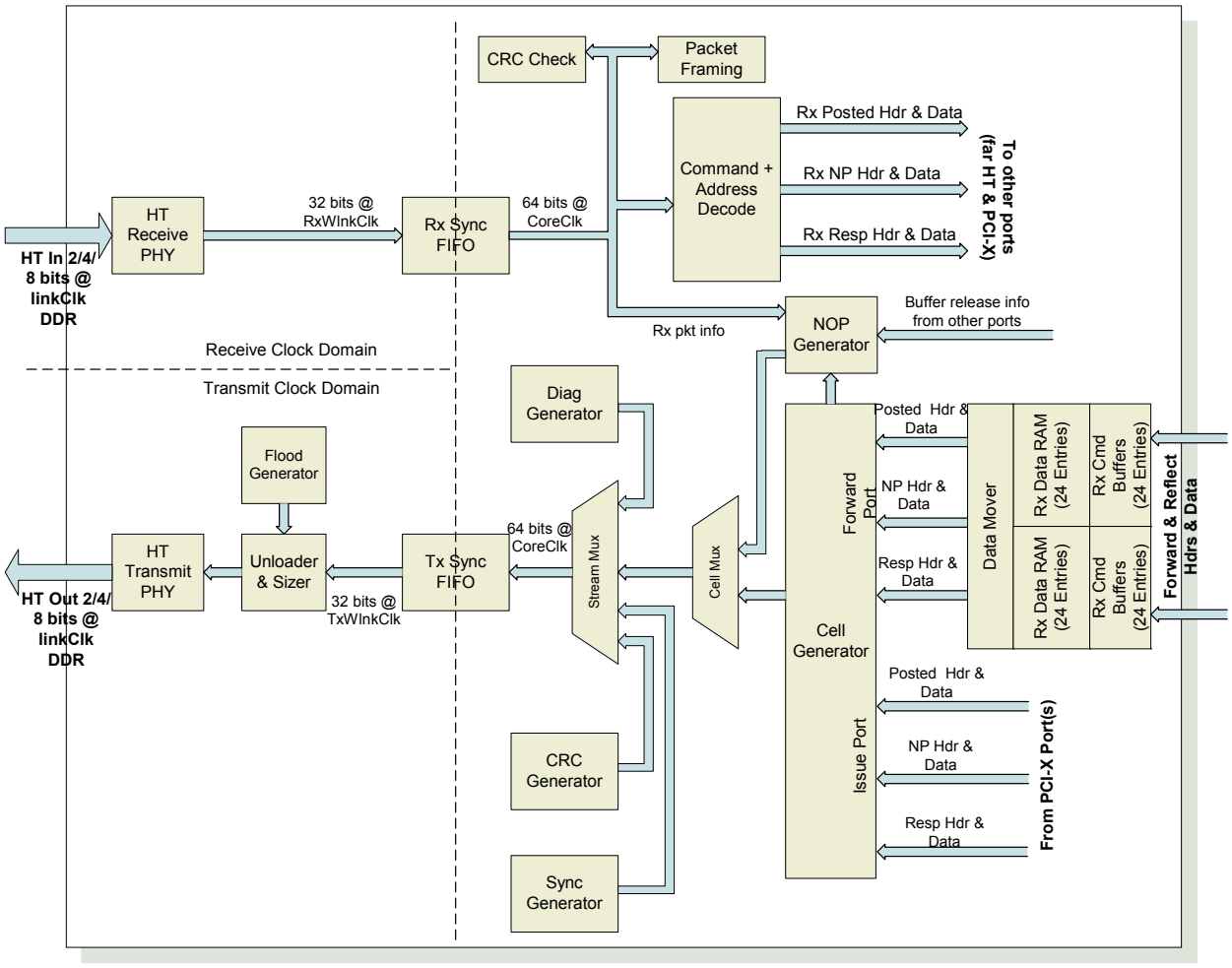
In the HyperTransport protocol, all logical packet transfer is between HyperTransport slaves and the host. Direct peer-to-peer communication is not allowed. To support peer-to-peer operations, packets are reflected through the host. Packets issued from the host to a HyperTransport slave are defined to travel downstream on the HyperTransport chain. Packets issued from a HyperTransport slave to the host are defined to travel upstream. Intermediate nodes in the daisy chain forward packets from link to link until they reach their final destination, which accepts the packet.

Link interfaces in the Tsi308 are symmetrical, which allows connection to either bridge link toward a host. The Tsi308 also supports being placed in a double-hosted chain with hosts on both ends.

Figure 3: Single HyperTransport Link Interface Block Diagram



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2.2.1 HyperTransport Packet Reception

Packets received from a HyperTransport link are decoded and routed to appropriate destination port where they are stored in Receive (Rx) buffers for subsequent transmission. HyperTransport flow control algorithm guarantees that no packet is received without buffer space to store it. Packet contents are divided into command information (including address) and data, with separate buffers for each.

For packets arriving from HT Links, each destination port (forward HT Link, PCI_A and PCI_B) has dedicated command and data buffers for two possible source ports (Both HT links could source data to any of the two PCI-X ports and each of the two HT Link Ports can receive forwarded data from other HT Link Port and reflected traffic) statically partitioned among the three virtual channels (posted, non-posted and response), with each channel allocated space to hold eight commands and eight data packets. However packets originated on PCI-X bus is locally buffered in respective PCI-X Ports and delivered directly to the appropriate HT Link.

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2.2.1.1 Packet Decode

As packets arrive from a HT link, the associated commands and addresses are decoded to determine if the Tsi308 is the packet target on HyperTransport chain and routed to the appropriate port where they are locally stored. Packets are checked in the destination port for ordering collisions against other packets resident in the buffers. The decode and collision results are stored in the buffers with the packets. The packet routing is as follows:

- Packets received on the HyperTransport interface may be routed to internal logic (CSRs), including PCI-X interfaces. This is “accepting” a packet.
- Packets may also be routed to the other HyperTransport link interface for transmission to the next device in the chain. This is “forwarding” a packet.
- A particular packet may be accepted, forwarded, or both.

The Tsi308 HyperTransport packet decode first determines whether the incoming packet is traveling upstream or downstream. This determination is based on the packet source information contained in the packet itself, not on which link is the upstream or downstream link.

- Upstream packets are always forwarded toward the host and are never accepted by the Tsi308 chip.
- Downstream RdSized and WrSized request packet addresses are decoded according to the HyperTransport Address Map described in Section 3.3 and are accepted if they match any Tsi308 address ranges of any PCI-X ports or internal CSRs.
- Downstream WrSized and RdSized that do not match any of the Tsi308 address ranges are forwarded to the next device in the chain.
- Broadcast request addresses are also decoded and accepted if they match a Tsi308 address range. However, these packets are also always forwarded.
- Fence and Flush requests are never accepted by Tsi308 and are always forwarded.
- Downstream response packets are accepted if their UnitID field matches the value in the BaseUnitID field of any of the Tsi308 LdtCmd register; otherwise, they are forwarded.

2.2.1.2 Collision Checking and Ordering

Collision checking is performed according to the HyperTransport protocol to determine if incoming packets are required to stay ordered behind packets already in the Rx buffers. Only packets headed to the same accept or forward destination may have ordering requirements. If a packet has an ordering collision, it may not be issued from the Rx buffers until the packet with which it collided has both been issued and reached an appropriate commit point to guarantee ordering. This ordering point varies by destination.

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Because the Outbound Request Controller (ORC) can reorder requests, requests accepted by the Tsi308 may not be committed until they are retired by ORC. For accesses to PCI-X bus, this means that the request reached the PCI-X bus and all data was transferred. Packets forwarded from one link to the other are either streamed – meaning that the transmission may start before the whole packet is received or a complete packet is first stored and then forwarded, avoiding possible “holes” on transmitting link if transmitting link bandwidth (link frequency * link width) is an order faster than that of receiving link. Since there is no specification defined way to determine the bandwidth of receiving link, Tsi308 implements a proprietary control bit (StoreForward) per link in its CSR which system software can program that tells the Tsi308 whether to stream (low latency) or not. It is the Rx Command Buffer’s responsibility to ensure that required packet ordering is maintained so packets can be committed as soon as they are passed to the link controller.

Packets that do not have any ordering requirements may leave the Rx buffers in a different order than they reached them, both among and within virtual channels. In general, Rx buffers select a packet choosing the oldest non-blocked packet in each channel to a given destination.

HyperTransport Ordering

The Table 2 lists ordering implemented in Tsi308 for packets issued from PCI/PCI-X to HyperTransport link and for packets forwarded from one HT link to other HT link.

Table 2: HyperTransport Ordering

Row Pass Column	Posted Request	Non-posted Request	Response
Posted Request	No	Yes	Yes
Non-posted Request	No	No	No
Response	No	Yes	No

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PCI Ordering

The Table 3 lists the ordering implemented in Tsi308 for packets traveling to PCI from HT interface.

Table 3: PCI Bus Transaction Ordering

Row Pass Column?	Posted Memory Write (PMW)	Delayed Read Request (DRR)	Delayed Write Request (DWR)	Delayed Read Completion (DRC)	Delayed Write Completion (DWC)
PMW	No	Yes	Yes	Yes	Yes
DRR	No	No	No	No	No
DWR	No	No	No	No	No
DRC	No	Yes	Yes	No	No
DWC	No	Yes	Yes	No	No

PCI-X Ordering

The Table 3 lists the ordering implemented in Tsi308 for packets traveling to PCI-X from HT interface.

Table 4: PCI-X Bus Transaction Ordering

Row Pass Column?	Posted Memory Write (PMW)	Split Read Request (SRR)	Split Write Request (SWR)	Split Read Completion (SRC)	Split Write Completion (SWC)
PMW	No	Yes	Yes	Yes	Yes
SRR	No	No	No	No	No
SWR	No	No	No	No	No
SRC	No	Yes	Yes	No	No
SWC	No	Yes	Yes	No	No

2.2.2 HyperTransport Address Map

The Tsi308 implements a single flat 64-bit address space for all accesses. All address spaces that can be reached from HyperTransport are mapped into this space. The Tsi308 checks addresses on incoming packets in each space for ranges that it accepts.

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2.2.2.1 Memory Mapped Space

The HyperTransport specification places Memory Mapped Space in the address range of 0000_0000_0000_0000h to 0000_00FC_FFFF_FFFFh. The Tsi308 accepts two ranges within this space, as enabled by MemSpaceEn in the Command (Cmd) CSR, consisting of the following:

- Memory Space, defined by the MemBase and MemLimit CSRs.
- Prefetchable Memory Space, defined by the PrefMemBaseUpper/PrefMemBase and PrefMemLimitUpper/PrefMemLimit CSRs.

Setting the VgaEn bit in the Bridge Control CSR creates an additional window of 00_000A_0000h to 00_000B_FFFFh, which is also accepted. The Tsi308 never does prefetching to PCI, so the prefetchable/nonprefetchable attribute of these ranges does not matter. RdSized requests to these ranges result in MemRd requests on PCI-X bus. WrSized requests to these ranges result in MemWr requests on the PCI-X bus. If above 4GB, addresses are passed straight through as a Dual Address Cycle (DAC).

2.2.2.2 I/O Space

The HyperTransport specification places PCI-X I/O space in the address range of 0000_00FD_FC00_0000h to 0000_00FD_FDFF_FFFFh. The Tsi308 strips the top 39 bits off of the addresses in this range.

- If enabled by I/OspaceEn in the Cmd CSR, the Tsi308 accepts requests that fall in the range defined by the I/O Base and I/O Range Base Upper, and I/O Limit and I/O Range Limit Upper CSRs.
- If set, the IsaEn bit in Bridge Control CSR creates a series of holes (the top 768 bytes of each 1 KB block in the low 64 KB) in this space that the Tsi308 does not accept.
- Setting the VgaEn bit in the Bridge Control CSR creates an additional set of windows (all addresses in the low 64 KB where the bottom 10 bits are in the ranges 3B0h – 3BBh or 3C0h – 3DFh), which the Tsi308 accepts. Accepted RdSized requests result in IoRd requests on PCI-X bus, and WrSized requests result in IoWr requests, with the bottom 25 bits of the HyperTransport address passed through. Bits 31:26 are 0.

2.2.2.3 Configuration Space

The HyperTransport specification places PCI-X configuration space in the address range of 0000_00FD_FE00_0000h to 0000_00FD_FFFF_FFFFh. Address bit 24 identifies requests as Type 0 or Type 1 configuration requests.

- Type 0 requests are accepted and routed to the Tsi308 internal configuration registers if their device number (bits 15:11) matches the value of BaseUnitID in the HyperTransport Command CSR.

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- Type 1 requests are accepted if their bus number (bits 23:16) falls within the range defined by the Secondary Bus Number and Subordinate Bus Number CSRs, inclusive. Type 1 requests are routed to PCI-X, as ConfigRd or ConfigWr cycles.

A Type 1 request with a bus number that exactly matches the Secondary Bus Number CSR becomes a PCI-X Type 0 configuration request, with AD[deviceNumber + 16] set.

- Type 1 requests with a bus number greater than Secondary Bus Number but less than or equal to Subordinate Bus number are passed on to PCI-X as Type 1 configuration cycles. Bits 23:2 of the address are left unchanged. The Tsi308 does not support the Type 1 configuration to Special cycle mapping.

2.2.2.4 Interrupt Space

The HyperTransport specification places interrupt space in the address range of 0000_00FD_F800_0000h to 0000_00FD_F8FF_FFFFh. The Tsi308 only accepts End of Interrupt (EOI) requests in this range, which should always be broadcasts. These EOI requests are routed to the interrupt controller.

2.2.3 HyperTransport Address Remap

Since HyperTransport technology is meant to provide a high-bandwidth backbone for I/O systems, which are likely to contain a variety of other buses with varying addressing capabilities, the HyperTransport specification defines mechanism to remap the HyperTransport addresses to locally defined addresses of other buses allowing mapping of the smaller address spaces of individual buses into different locations within the HyperTransport technology address map.

To support this, Tsi308 implements 64-bit Address Remapping Capability as specified in [1] with single upstream DMA window. This DMA window can also be used to set specific attributes in packets that originate on PCI-X and also fall inside the address ranges defined by the DMA window. An example of this attribute is that the user can program Tsi308 to set Isoc bit for all the packets that pass through the DMA window.



Address Remapping is enabled through CSRs and is only applicable to packets traveling from/to PCI-X. It is not applicable to forward packets

2.2.4 HyperTransport Packet Transmission

The HyperTransport packet generator logic is essentially a large arbiter/multiplexer that formats and combines packets from each of the three virtual channels issued from within the Tsi308. The output stream is combined with the stream of packets forwarded through the Tsi308 from the far HyperTransport link. This later multiplexing is also used to insert NOP/buffer release messages to the transmitter on the link's other end.

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Packet transmission is paced by the transmit buffer counters maintained in each virtual channel for both command/address and data, as the HyperTransport specification describes. These counters are decremented as packets are transmitted and incremented as buffer release messages are received from the transmitter at the link's other end. Transmit buffer counters can be throttled using the Transmit Buffer Counter Maximum CSRs (C8h and CCh).

2.2.4.1 Packet Insertion

To prevent devices close to the host bridge from starving devices further out in the chain of bandwidth, the Tsi308 implements the packet insertion fairness algorithm described in [1]. This algorithm throttles the insertion rate of packets from Tsi308 relative to packets being forwarded and attempts to balance the packet insertion rates of all devices on the chain.



When Tsi308 is operating in Dual Device Mode(Split PCI-X Bus), fairness is implemented on cumulative basis wherein insert rate is computed for a single device in standard way and then actual insertion rate is doubled to account for two devices in single node/chip.

Insertion of buffer release messages is forced, even when the outgoing transmission stream is busy. Forcing allows traffic to flow through the Tsi308 continuously while maintaining a relatively small number of Rx buffers. The Tsi308 forces a buffer release message as soon as possible when an Rx buffer is freed, subject to the requirements of the HyperTransport protocol. The frequency of buffer release messages is limited under HyperTransport Transmit Control CSR (6Eh) to prevent them from occupying too much bandwidth in a busy stream. Throttling buffer releases clumps the released messages together and raises their efficiency.

In a single-hosted HyperTransport chain, the Tsi308 may be at the end of the chain furthest from the host and therefore have no downstream link connection. In this case, packets are routed to the End of Chain (EOC) logic in the unconnected link interface. The EOC logic drops responses and posted requests and generates Non-Existent Access (NXA) Error responses back into the receiver for non-posted requests. These error responses then get forwarded back to the other HyperTransport link interface's reflect path Rx buffers and back to the requesting device. Error logging for the dropped packets occurs in the Link Control Registers CSRs (44h and 48h) in Tsi301 mode or in the Link Error Register (4Dh and 51h) in standard HyperTransport mode.

2.3 Outbound Transactions

Outbound transactions to the Tsi308 are those accepted from the HyperTransport chain. All outbound requests go first from the HyperTransport link interface on which they are received to the Outbound Request Controller (ORC). This controller is responsible for issuing the request to the appropriate destination functional unit and for tracking the request state while it is outstanding.

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The controller has two buffers, which allow state tracking for two outstanding requests. If both requests are outstanding in the controller at once, it rotates them in round-robin fashion to issue or reissue them. When the ORC filo fills, subsequent requests back up to the HyperTransport Rx buffers. Since the ORC doesn't guarantee ordering, the HyperTransport Rx buffers must not issue the second in an ordered pair of transactions until the first has completed.

The ORC is also responsible for managing space in the PCI response data buffer. All outbound non-posted requests, regardless of destination, must be allocated space in the response data buffer before they can be accepted from the Rx buffers through Data Mover (DM) by the ORC. Even though PCI response data buffer can hold two responses, ORC uses only request buffer for receiving non-posted requests from Rx command buffers, reserving the other buffer always for posted requests which in turn, provides the deadlock-avoidance guarantee required by [2] and [3] (non-posted requests are never allowed to block posted requests).

As requests complete at their destinations that fact is signaled back to the ORC (Normally PCI-X Master but PCI-X Target if request was non-posted and Tsi308 is operating in PCI-X mode), which allows the request buffer to be retired. If the request was non-posted, the transaction will require generation of a response to the host. ORC considers posted transactions as complete when the request completes at its destination and the buffer is retired. Non-posted transactions are complete when the response packet is issued to the HyperTransport transmit interface from which the request was received.

2.3.1 PCI-X Outbound Transactions

Outbound requests to PCI-X are handed to the PCI-X interface to be driven out to the bus. Write data comes from the Rx data buffers, Read data is returned from the bus and placed in the PCI Response Data Buffer.

When PCI-X bus A is configured as 64 bit at reset (P0_AD[14]), the interface automatically asserts P0_REQ64_N on all transactions for which it is legal. The PCI-X bus B can only be 32 bit.

The PCI-X interface supports Type 0 PCI configuration cycles to device numbers 0 through 15. Px_AD[31:16] (x = 0 for PCI-X A, 1 for PCI-X B) are driven with a one-hot encoding during these configuration cycles, with bit 16 asserted for accesses to device number 0. This logic assumes that one Px_AD bit is connected to the IDSEL# pin on each PCI slot through a series resister on the board.

If a request is retried or disconnected on the PCI, that fact is reported back to the ORC. The controller finishes any data movement associated with the disconnected transaction and then reissues the request from the point of disconnection. It continues to reissue a request until it completes or until the retry timer for the request expires. Because the ORC can handle two outstanding requests at a time, transactions repeatedly retried or disconnected may be reordered or interleaved.

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2.3.1.1 PCI-X Response Data Buffer

The PCI response data buffer contains read data returned from outbound reads to the PCI interface. This data buffer can hold a total of 64 bytes for one HyperTransport read requests.

Once the response is issued, the buffer is retired. Non-posted write requests still occupy space in the response data buffer, even though they have no read data.

2.3.1.2 End of Interrupt

When an interrupt is configured as level sensitive, upstream interrupt logic must respond to an interrupt request packet with an end of interrupt (EOI) packet. Until the EOI packet is received by the Tsi308, no new interrupt request packets will be generated by that interrupt pin.

2.4 Inbound Transactions

Inbound transactions are requests from the PCI-X bus or internal interrupt controller across HyperTransport to the host bridge. From there, they are routed to destinations behind the host bridge or reflected peer-to-peer back onto the HyperTransport chain. If the request is non-posted, the transaction also includes the response from the host bridge back to the original requesting unit.

The Tsi308 operates as a PCI-X target for requests from external PCI-X devices. All accepted requests are forwarded to the HyperTransport link interface leading to the host. Reads go through the delayed request buffers and are handled on the PCI-X bus as delayed requests when in standard PCI mode or as split requests when in PCI-X mode. All writes, except IO writes are posted into the posted request queue and allowed to immediately complete on the PCI-X bus.

2.4.1 PCI-X Address Map

Accesses on PCI-X bus are checked against the following ranges to determine whether the Tsi308 is the target of the access and should assert Px_DEVSEL_N to accept the request. The Tsi308 makes this determination with medium DEVSEL# timing. When PCI-X A bus is configured as 64-bit target at power up, the Tsi308 asserts P0_ACK64_N in response to P0_REQ64_N for requests it accepts.

- **Memory Mapped Cycles**. The Tsi308 implements a 64-bit space for memory mapped accesses and decodes DAC accesses for addresses above 4 GB. While operating in Tsi301 compatible mode address bits above 39 are ignored and result in the 40-bit space aliasing through PCI's 64-bit memory mapped space.

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Memory mapped addresses are compared to the range defined by the Memory Range Base Addr and Memory Range Limit Addr CSRs; and the range defined by the Prefetchable Memory Range Base Upper and Prefetchable Memory Range Base Addr, and Prefetchable Memory Range Limit Upper and Prefetchable Memory Range Limit Addr CSRs. Addresses that don't fall into any of these ranges are accepted for forwarding to HyperTransport as long as the MasterEn bit in Command CSR is set and bits [39:32] <= FCh.

- **I/O Cycles**. The Tsi308 implements a 64-bit space for I/O accesses. While operating in Tsi301 compatible mode, address bits above bit 24 are ignored and result in 25-bit space aliasing through PCI's 32-bit I/O space.

I/O addresses are compared to the range defined by I/O Range Base Upper and I/O Base, and I/O Range Limit Upper and I/O Limit CSRs. Accesses that miss the range are accepted for forwarding to HyperTransport, as long as MasterEn bit in the Command CSR is set.

- **Configuration and Special Cycles**. The Tsi308 never acts as a target for configuration or special cycles on PCI-X bus.

2.4.2 PCI-X Posted Write Queue

The Tsi308 responds as a PCI-X write target to PCI-X Memory Write, Memory Write Invalidate, and I/O Write commands. All of these writes are posted to the HyperTransport chain except I/O writes which is non-posted. The Tsi308 never responds to Configuration Writes. A total of 1024 bytes of buffering for posted data is provided per PCI-X bus.

Memory Write and Memory Write Invalidate commands stream data into the chip, disconnecting either on 4-KB boundaries or when all of the internal buffer space is filled. The Tsi308 generates the largest HyperTransport write operations possible, issuing them continuously as the data for each write is received from PCI-X.

As the bandwidth of HyperTransport exceeds the bandwidth of PCI-X, it is expected that the internal buffers will not fill and memory writes will proceed continuously at the full bandwidth of PCI-X bus.

2.4.3 PCI-X Delayed/Split Request Buffers

The Tsi308 acts as a PCI-X target for PCI-X Memory Read, Memory Read Line (PCI), Memory Read Multiple (PCI), Memory Read Block (PCI-X), I/O Write and I/O Read commands. The Tsi308 never responds to configuration read or interrupt acknowledge accesses. All supported read transactions are implemented as delayed requests (PCI) or split requests (PCI-X).

Incoming requests are assigned to a delayed request buffer. There are four delayed request buffers, enabled under CSR control, allowing up to four PCI-X read requests to be in progress at one time. If no delayed request buffers are free, incoming requests are retried until one is available. Once the request is assigned to a buffer, the interface continues to retry it on the PCI bus while read requests are issued to the HyperTransport interface.

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I/O writes are not allowed to stream and always disconnect after a single data beat on the PCI-X (32-bits). Each I/O write is issued to HyperTransport as an independent request.

2.4.4 Prefetching (PCI mode only)

While operating in standard PCI mode, the Tsi308 supports a variety of prefetching options configured under CSR control using two Read Control CSRs, Read Control 1 at 62h:60h and Read Control 2 at 5Eh:5Ch. Read Control 2 is applied for requests passing through DMA window and is reserved in Tsi301 compatible mode. However:

- I/O reads are never prefetchable.
- MemRdLines and MemRdMult may have prefetching individually configured.
- For systems in which MemRds are known to be side-effect free, MemReadPrefEn can be set to enable prefetching behavior for MemReads using the same parameters as MemRdLines.
- PrefEn can be used to globally enable or disable all prefetching.
- Nonprefetchable reads always request only the bytes required to satisfy the initial data beat of four or eight bytes on the PCI bus, which may result in either one or two HyperTransport requests.

Transactions for which prefetching is enabled issue a HyperTransport read for the remainder of the 64-byte aligned block containing the original request. These transactions also issue HyperTransport reads for the zero to seven complete 64-byte blocks following, as determined by the Read Control CSRs. The total number of reads that may be outstanding to HyperTransport at one time is limited by the Outbound Data Buffers.

When multiple reads to HyperTransport are issued for a single PCI read request due to prefetching or due to clear byte enables in a 64-bit nonprefetchable read on a 64-bit bus, each HyperTransport request is referred to as a subrequest of the PCI request. Each Delayed Request Buffer can track up to 8 subrequests at once. The total number of configured subrequests (number of enabled delayed request buffers * (the maximum number of subrequests each, rounded up to the next power of 2)) must not exceed the number of entries in the Outbound Data Buffers.

2.4.5 Memory Read Block (PCI-X mode only)

MemRdBlk command of PCI-X is analogous to MemRdLine or MemRdMultiple of PCI.

Since PCI-X request provides the byte count to be satisfied during the attribute phase of a PCI-X read transaction, read data for PCI-X requests are never prefetched, instead data is read just enough to satisfy the byte count of the original request.

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Similar to in PCI mode, Tsi308 can handle up to four PCI-X read requests and they are assigned to Delayed Request Buffers as usual, however a single PCI-X read request can request up to 4K bytes. The Tsi308 implements a maximum of 512 byte buffering per request. For reads requesting greater than 512 bytes, Tsi308 throttles the requests issued on HyperTransport by issuing a subrequest on HyperTransport if at least 64 bytes of buffer space is available in Outbound Data Buffer allotted for that particular request until the byte count is satisfied. As the data arrives from HyperTransport into Outbound Data Buffer, PCI-X Master behaving as Split Completer connects on PCI-X bus and transfers the data to the original requester in chunks of 128 bytes disconnecting at naturally aligned 128-byte boundary or Allowable Disconnect Boundary (ADB).

2.4.6 SrcTags

The SrcTag for each HyperTransport read request is formed by concatenating the delayed request buffer number with the number of the HyperTransport subrequest being issued by that buffer.

2.4.7 Sequences

HyperTransport subrequests that are part of the same PCI-X request must be tagged with a matching nonzero SeqID to guarantee ordering at the target. This 4-bit SeqID is formed by concatenating a leading 1 (guaranteeing a nonzero result) with the 2-bit delayed request buffer number and one bit that toggles for each occupation of the delayed request buffer. The concatenation prevents consecutive PCI-X reads from being issued with the same SeqID and appearing to have HyperTransport ordering requirements.

2.4.8 Read Responses

As the read responses return from HyperTransport, the data is stored in the Outbound Data Buffers. Even though sequenced requests are guaranteed to reach the target in order, responses may be received from the target out of order. When all the data from the first HyperTransport requests is received (the amount required is controlled by the InitCount fields of the Read Control CSRs), the PCI interface ceases retrying the request. Read data is supplied from the buffers when the request is next reissued. Data streams to the PCI bus until the transaction is disconnected by the PCI master or until the next data required is not present in the Outbound Data Buffers.

The difference in operation while operating in PCI-X mode is that:

- Original read request is split first time while latching request and requestor information.
- Tsi308 connects itself with original requester on PCI-X as Split Completer as opposed to waiting for the request to be reissued.
- Data is transferred in ADBs as PCI-X master is not allowed to disconnect arbitrarily.

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- Tsi308 generates one or more split completion transactions until the byte count of the original request is satisfied.

2.4.9 Continuous Prefetching (PCI mode only)

If continuous prefetching is enabled in the Read Control CSR, the Tsi308 issues further ascending read requests to fill buffers as they drain (up to a 4-KB page boundary) in an effort to make sure required data is always available. Otherwise, the transaction is disconnected as soon as all data from the initial reads is returned to the PCI bus.

2.4.10 Transaction Disconnects

Read transactions may be disconnected by the bridge when required data is not available in time. The Delayed Request buffer remains in use until all outstanding HyperTransport prefetch requests receive their responses; then it is retired and any leftover data is discarded (PCI mode only). Each delayed request buffer also has an associated discard timer loaded with one of the two values determined by the Secondary Discard Timer bit (9) of the Bridge Control CSR (3Eh) when the data is received from HyperTransport. If this timer expires before the data is called for by the PCI master, the data is discarded and the buffer is retired.

2.4.11 Outbound Data Buffer

The Tsi308 contains a central data buffer (four 512-byte entries) for the accumulation of read response data to return to the PCI-X bus. These four buffers correspond to four read requests in Delayed Request Buffers. Data returning from HyperTransport is loaded into the buffer based on the comparison between request information stored in the corresponding delayed request number and information contained in response header, and drained out to the PCI-X bus when the delayed request reconnects (PCI) or when the Tsi308's split completer connects.

2.4.12 Interrupt Generation

The Tsi308 interrupt controller supports 10 interrupts per PCI-X port. Each of these interrupts are enabled and configured independently through its Interrupt Definition Register CSR. However Tsi308 while operating in Tsi301 compatible mode, these interrupts are partitioned into different groups, each group consists of four interrupts or less and interrupts are configured in groups. The interrupt configuration options include: edge versus level sensitivity, polarity, and vector ID.

An incoming interrupt is first synchronized to the core clock domain and masked with its CSR enable bit to set the interrupt's bid in the Interrupt Request Register (IRR). A round-robin arbiter will then examine each IRR bit and forward requests to the primary bus logic, setting its In Service Register (ISR) bit. New interrupts from that pin will not be accepted as long as the ISR register is set.

- For edge sensitive interrupts, the ISR bit is cleared as soon as the primary interface logic accepts the inbound interrupt request

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- For level interrupts, the ISR bit is not cleared until an End of Interrupt (EOI) packet is received with a vector ID matching the ISR. Software may also write a 1 to 63rd bit of Interrupt Definition Register to clear the interrupt without an EOI.
- All interrupts and interrupt blocks are disabled at reset and must be enabled by software
- The ISR can also be monitored via the CSRs

2.4.12.1 Interrupt Diagnostic Mode

To simplify debugging interrupt software and hardware, each interrupt may be stimulated and monitored via CSR reads and writes (see the Interrupt Diagnostic Register for details). Writing a 1 to the Initiate field of the CSR will generate an interrupt on the interrupt line in the Pin Number field. The ISR bit may be observed by monitoring the Active field of the same CSR.



The Active field is always for the CSR indicated by the Pin Number field

2.5 PCI-X Arbiter

The Tsi308 includes a PCI-X arbiter for each PCI-X port. The arbiter is an independent unit. The Tsi308's internal PCI-X request and PCI-X grant signals are connected to pins as Px_REQ_OUT_N and Px_GNT_IN_N (x = 0 for PCI A and x = 1 for PCI B). It is possible to either use this arbiter or to bypass it and use an external arbiter.

The Tsi308's internal arbiter contains two round-robin arbitration groups: Px_REQ0_N and Px_REQ1_N through Px_REQ5_N. Within each group, arbitration is shared equally between the requests. Generally Px_REQ_OUT_N would be attached to Px_REQ0_N and Px_GNT_IN_N attached to Px_GNT0_N.

When there are no requests present, the arbiter either parks the bus at the last grant or (based on a CSR bit) at Px_GNT0_N, which is presumed to be the Tsi308's internal requester.

The PCI Control CSR ParkMaster bit allows the configuration of the internal PCI-X Arbiter parking.

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2.6 Online Insertion and Removal (OIR)

The Tsi308 device provides a hook to help users implement their own proprietary hot plugging outside of the device. The device implements an input pin (Px_OIR_DISCON_EVENT) in each of the two PCI-X interface logic which is asserted by the user when an attached PCI-X card is about to be removed. When asserted, Tsi308's PCI-X master finishes its current transfer if any progress at the time on PCI-X and stops generating any further traffic. Tsi308 starts sending dummy responses to HyperTransport for all the pending read requests (that are within the chip queue yet to be executed on PCI-X as well as the ones that have been already presented on PCI-X and are pending on PCI-X), and silently drops all the posted requests from HyperTransport meant for the affected PCI-X port.

This condition persists until software resets the PCI-X by writing a 1 to SecBusReset (bit 6) of Bridge Control Register.



Tsi308 neither logs this event in CSR nor generates an interrupt of this event. It is up to the user to notify the host of this event and initiating appropriate action if any.

For more information, see Section A on page 233.

2.7 LDTSTOP# Support

Tsi308 implements LDTSTOP# pin to support HT Link Disconnect/Re-connect sequence. When LDTSTOP# is asserted, Tsi308's transmitter finishes sending the current packet and then continues to send disconnect NOP packets through the end of current CRC window and continuing through the transmission of the CRC bits for the current window, the transmitter continues to drive disconnect NOP packets on the link for 64-bit times, after which point transmitter waits for the corresponding receiver on the same link to complete its disconnect sequence, and then disables its drives if LDTSTOP# tri-state enable bit is set. During disconnection of HT link, Tsi308's receiver continues to operate normally through the end of current CRC window until it receives the CRC bits for the current window and then disables its receivers if LDTSTOP# tri-state enable bit is set.

When LDTSTOP# is de-asserted, Tsi308's transmitter goes through link initialization sequence just like it does coming out of warm reset. Tsi308's receiver waits for 1 us before enabling its inputs after LDTSTOP# is de-asserted.

If system software re-programs Tsi308's link width and link frequency, it will take effect after HT Link Disconnect and Re-connect sequence.

Tsi308 registers buffer status prior to the disconnection. No new buffer release messages need to be sent after re-connection of HT links. Tsi308 does not flush out its internal buffers when LDTSTOP# is asserted. It just stores the packet and resumes the packet transmission after its link is re-connected to HT chain.

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2.8 Power Management

Tsi308 does power saving when operating in Single PCI-X mode by gating the clock to PCI-B logic internal to it. Tsi308 powers down P1_AD pads during Single PCI-X 32-bit mode operation. Tsi308 does not do any other power savings even though it has implemented PCI power management capability registers and SMAF field in CSR space. These registers are implemented to be compatible with x86 systems.

2.9 Reset

2.9.1 Cold Reset

Cold Reset of Tsi308 is caused by the deassertion of L_POWER_OK pin. At power-on, L_POWER_OK must remain deasserted until power and clocks are stable for at least 1 ms. L_RST_N must be asserted before L_POWER_OK asserts and remains asserted for at least 1 ms following.

Cold reset results in the initialization of all internal state, including the loading of internal registers from strapped PCI bus pins and the SRI (Serial ROM Interface). The PCI-X bus is held in reset until the deassertion of L_RST_N.

2.9.2 Warm Reset

Warm reset of the Tsi308 is caused by the assertion of L_RST_N while leaving L_POWER_OK asserted. Once asserted, L_RST_N must remain asserted for at least 1 ms.

Warm reset results in the initialization of most internal state, with the exception of state loaded from PCI-X bus sampling or the external ROM interface, and persistent error state. The PCI-X bus is held in reset until the deassertion of L_RST_N.



Tsi308 implements L_RST_N as in-out. It extends the asserted state of L_RST_N beyond 1 ms until internal PLLs are locked and configuration information from SROM is loaded

2.9.3 Reset Configuration

Configuration information is loaded into the Tsi308 at reset from PCI-X AD bus, P0_AD[31:0].

2.9.4 HyperTransport Link Initialization

On the deassertion of L_RST_N as part of a warm or cold reset sequence, the Tsi308 attempts to initialize both of its HyperTransport links as described in the HyperTransport specification.

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When link initialization is done, the InitDone CSR bit is set. Software polls this CSR bit to determine that the link is live and may be included in fabric initialization. InitDone remains clear if the Tsi308 is unable to initialize the link because of any of the following:

- There is no device at the other end.
- Communication with the device at the other end is not possible.
- The link is disabled because of a previous failure.

2.9.5 HyperTransport Fabric Initialization

Once hardware initialization of the individual links in the HyperTransport chain completes, host software is responsible for initializing the HyperTransport fabric. A sample initialization sequence proceeds according to the following example. If starting from the host, initialization proceeds recursively for each link in the chain.

Example initialization sequence:

1. Read the InitDone bit for the link to determine whether the link is live. Also, read the various link error bits to determine if the link has taken errors since reset that prevent it from functioning correctly. If the link is not live, or is taking fatal errors, fabric sizing is complete and you can proceed to Step 6.
2. All devices assume a HyperTransport UnitID of 0 at reset. Therefore, a configuration access to PCI device number 0 is accepted by the first uninitialized device on the chain. This is the device at the far end of the link currently being sized.
3. Performing a write to the HyperTransport Command register, without changing any fields, causes initialization of the master host bit. This indicates the HyperTransport link that connects toward the host bridge. Polling the error bits for that link determines whether the node on the far end is detecting any fatal errors on the link. If so, this link is not to be used, fabric sizing is complete, and you can proceed to Step 5.
4. Software reads the Class Code, Vendor ID, and Device ID from the device at the end of the current link to determine what type of device it is talking to.
5. Software writes the BaseUnitID register in the device with the next free HyperTransport unitID value, starting with 1 for the first device. It reads the unitCount register to determine how many unitID values the current device requires and increments the next free unitID value appropriately.
6. Return to Step 1 to size the next link in the chain. Because step 3 wrote the base unitID of the last sized device to a nonzero value, it no longer accepts accesses to device 0. Instead, it forwards them to the next device in the chain.
7. When sizing completes to the last live link in the chain, set the EndOfChain and TransmitOff bits for the outgoing link of the last device. This prevents the unused link from being driven and enables proper handling of HyperTransport packets that traverse the HyperTransport link without finding their target node.

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2.9.6 Secondary Bus Reset

The PCI-X bus may be placed and held in reset while the HyperTransport interface remains live. When the reset pin of the PCI-X bus (Px_RST_N) is asserted, all internal PCI-X buffers are flushed. Inbound writes that are in progress during the reset may be completed, depending on how far into the pipeline they are. Inbound reads are retired as their responses return from HyperTransport and the data dropped. Outbound operations to PCI-X are dropped and error status maintained and returned as if the operations had master aborted on the PCI-X bus. Software is responsible for coping with any transfers that were interrupted or dropped as a result of the reset. The interrupt controller is not affected by secondary bus reset.



Only the Tsi308 can initiate PCI-X bus reset. The PCI-X bus is placed and held in reset under CSR control

2.10 Error Handling

The Tsi308 provides a variety of error checking, logging, and containment functions to ensure correct operation and diagnose failures.

2.10.1 Reporting

The Tsi308 logs all errors it detects in CSRs that are persistent through a warm reset. CSR enables are used to mask and control routing of error notification. Not all signaling methods are available for all error types.

When the Tsi308 takes an error, it signals the system in one of three ways. The error-signaling methods are listed below in order of increasing severity:

For errors detected by the Tsi308 as a transaction target, errors may be signaled in the bridge chip response. The method of signaling in the response depends on the protocol of the bus on which the error is detected.

1. Transaction errors on non-posted HyperTransport requests may be indicated by an Error response.
2. Transaction errors on PCI may be indicated by a target abort, PERR# assertion, or premature disconnection before the data in error is transferred.

In each of these cases, the protocol on the given bus continues to run, and it is the requester's responsibility to take appropriate action on receipt of the error. Transmission of HyperTransport error responses (without NXA) sets the SigdTgtAbort bit in the Status CSR. Transmission of a target abort on PCI sets the SigdTgtAbort bit in the Secondary Bus Status CSR.

Errors may be signaled to the system by the error interrupt pins. Two pins, FATAL_ERR_N and NONFATAL_ERR_N, allow division of errors into two different priority classes.

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These pins can be directly connected to input pins on the Tsi308 interrupt controller or to an external interrupt controller. They are active-low, open drain outputs, which allows the pins to be wire-ORedwith other interrupt sources. They also provide edge-triggered interrupts, pulsing when an error is detected. Only in Tsi301 mode the SerrEn bit in the Command CSR serves as a master enable for the error interrupts, in addition to the enables for individual error conditions. Assertion of either error interrupt sets the SigdSerr bit in the Status CSR.

The HyperTransport transmitters can flood the link with synchronization packets. These propagate along the length of the chain and are detected by the host bridge. The host bridge is then responsible for taking appropriate action. The link has to pass through a warm reset sequence before it can be re-enabled, and all transactions in progress are lost. This option is only available for catastrophic

HyperTransport errors that render the chain untrustworthy. Any error that causes sync flooding also sets the LinkFail bit in the HyperTransport Link 0/1 Control CSR for the link on which the error was detected. The setting of LinkFail will cause that link to not be re-initialized on the next warm reset event. The SigdSerr bit in the Status CSR is also set.

2.10.2 HyperTransport Errors

2.10.2.1 Link Errors

HyperTransport link errors are detectable at the lowest levels of the HyperTransport protocol and indicate a basic failing of the HyperTransport link. These errors are not localizable to individual transactions, and all can bring down the link through sync flooding.

CRC is checked by all of the HyperTransport link receivers in accordance with the HyperTransport specification.

Basic protocol checks are performed for proper switching of the CTL signal and legal command encodings. An overflow error is detected if the HyperTransport flow control mechanism breaks down and packets are received with no space for them in the Rx buffers.

Table 5 indicates the CSR bits used to log and enable reporting of each HyperTransport link error type.

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Table 5: HyperTransport Link Error CSR Bits

Error	Log Bit	Sync Flood	Fatal Interrupt	NonFatal Interrupt
Bad CRC	LinkCtrl/ CrcErr[0]	LinkCtrl/ CrcSyncFloodEn	ErrCtrl/ CrcFatalEn	ErrCtrl/ CrcNonFatalEn
Protocol Error	LinkCtrl/ ProtErr	ErrCtrl/ ProtSyncFloodEn	ErrCtrl/ ProtFatalEn	ErrCtrl/ ProtNonFatalEn
Rx Overflow	LinkCtrl/ OvfErr	ErrCtrl/ OvfSyncFloodEn	ErrCtrl/ OvfFatalEn	ErrCtrl/ OvfNonFatalEn

In addition to these HyperTransport link errors, the Tsi308 also propagates sync packets out of its transmitters if sync flooding is detected on either receiver. This is not logged or reported. This condition represents propagation of an error report from another device, not error detection by the Tsi308.

2.10.2.2 Transmission Errors

End of Chain (EOC) accesses occur when the Tsi308 tries to transmit a packet from PCI, or the other HyperTransport link, on a link that is not live (there is nowhere to send the packet).

1. If the outgoing packet was a non-posted request, the Tsi308 generates a matching response with the error and NXA bits set and sends the response back to the requester. This is equivalent to a master abort on PCI and requires no logging or further action by the Tsi308.
2. If the outgoing packet was a broadcast, it is silently dropped (it has traversed the whole chain).
3. If the outgoing packet was not a non-posted request (either posted request or response) or a broadcast, then there is no in-band way to signal the error. The packet is dropped and may be signaled as an error, as shown in Table 6.

Table 6: HyperTransport Forwarding Error CSR Bits

Error	Log Bit	Sync Flood	Fatal Interrupt	NonFatal Interrupt
End of Chain Error	LinkCtrl/ NxaErr	ErrCtrl/ NxaSyncFloodEn (Only in Tsi301 mode)	ErrCtrl/ NxaFatalEn (Only in Tsi301 mode)	ErrCtrl/ NxaNonFatalEn (Only in Tsi301 mode)

Tsi308 supports Drop on Uninitialized Link, if this bit is set then a transmitter with its Initialization complete bit clear will always act as if the End of Chain bit were set.

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Tsi308 also supports 64 Bit Addressing Enable, If this bit is set, requests that access addresses above FF_FFFF_FFFFh can be issued or forwarded by this link interface with the Address Extension command. If this bit is clear, then any access above FF_FFFF_FFFFh will be master aborted as if the end of chain was reached.

2.10.2.3 Master Errors

The Tsi308 accepts received responses that match its unitId and compares the response srcTags to the bridge's outstanding request srcTags. When the response does not match an outstanding request, it is called a Response Match error.

If the response does match an outstanding request, it is routed back to the PCI bus. The response may contain an error assertion, indicated by the Error bit. In this case, the NXA bit indicates whether the error was caused by the access failing to reach a target (value of 1) or signaled by the target (value of 0).

- An NXA bit value of 1 is roughly equivalent to a PCI master abort.
- An NXA bit value of 0 is equivalent to a PCI target abort.

In general, these errors are signaled to the PCI bus in the same way as in a standard PCI-PCI bridge.

Tsi308 HyperTransport master error settings are described in Table 7.

Because the Tsi308 prefetches read data, it is possible that the error occurred on a location that the PCI device did not intend to access. If error responses are received for prefetch requests, the associated data is dropped. The prefetching stops at the point of the error, and the PCI transaction is disconnected when it reaches that point. If the PCI device then requests the data again, the request goes back to HyperTransport. If the error recurs, the response error is passed to PCI.

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Once a response reaches the delayed request buffers, it must wait there until the requesting PCI master reconnects. As soon as the initial HyperTransport request completes and places its data in the buffer, a timer starts. The timer may be initialized to one of two values, as configured by the SecDiscardTimer bit in the Bridge Control CSR. If the timer expires before the data is called for, that may be treated as an error.

Table 7: HyperTransport Master Errors CSR Bits

Error	Log Bit	Fatal Interrupt	NonFatal Interrupt	PCI
Response Match Error	Error/ RespMatchErr	Error/ RespMatchFatalEn	Error/ RespMatch NonFatalEn	No action
Error without NXA	Status/ RcvdTgtAbort	Not supported	Not supported	Target Abort
Error with NXA	Status/ RcvdMstrAbort	Not supported	Not supported	If BrCtrl/ MstrAbortMode = 1, Target Abort; Else, complete normally returning all 1s data
Discard Timeout	BrCtrl/ DiscardStat	BrCtrl/ DiscardSerrEn & Error/ DiscardSerrFatal	BrCtrl/ DiscardSerrEn & !Error/ DiscardSerrFatal	Data dropped; PCI master must re-request.

2.10.2.4 Slave Errors

The Tsi308 CSR master only supports accesses within a 32-bit aligned block. Accesses that span more than one 32-bit block receive HyperTransport error responses, equivalent to a PCI target abort. No other action is taken. Error responses may also be signaled to HyperTransport because of errors taken when the request was issued to PCI.

2.10.3 PCI Errors

2.10.3.1 PCI System Errors

PCI devices may assert an unrecoverable system error by asserting SERR# on the secondary PCI bus.

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Settings for this error are described in Table 8.

Table 8: PCI System Error CSR Bits

Error	Log Bit	Fatal Int	NonFatal Int
SERR# Assertion	SecStatus/Det SERR	BrCtrl/SerrEn & ErrCtrl/SerrFatalEn	BrCtrl/SerrEn &!ErrCtrl/SerrFatalEn

2.10.3.2 PCI Master Errors

PCI master errors refers to errors detected by the Tsi308 when acting as a master on the PCI bus. Master and Target Abort are defined in the *PCI Local Bus Specification, Revision 2*.2.

TRDY# timeout refers to a violation of the target latency requirements, as given by the Error/TrdyTimer CSR. Retry timeout refers to an excessive number of retries and/or disconnects, as given by the Error/Retry-Timer CSR.

All PCI requests issued are forwarded through the Tsi308 from HyperTransport. If the HyperTransport request was non-posted, error status may be returned to the HyperTransport requester in the response.

If it was posted, the error may only be signaled by the error interrupts. A single set of error-reporting controls is used for all posted requests, regardless of the specific error taken.

Table 9: PCI Master Errors CSR Bits

Error	Log Bit	Non-posted	Posted
Master Abort	SecStatus/SecStatus/	If BrCtrl/ MstrAbortMode = 1, Return Error response	If Error/PostFatalEn = 1, assert FATAL_ERR_N. If Error/ PostNonFatalEn = 1, assert NONFATAL_ERR_N.

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Table 9: PCI Master Errors CSR Bits

Error	Log Bit	Non-posted	Posted
Target Abort	SecStatus/ RcvdTgtAbort	Return Error response	If Error/PostFatalEn = 1, assert FATAL_ERR_N. If Error/ PostNonFatalEn = 1, assert NONFATAL_ERR_N.
TRDY# Timeout	Not supported	Return Error response	If Error/PostFatalEn = 1, assert FATAL_ERR_N. If Error/ PostNonFatalEn = 1, assert NONFATAL_ERR_N.
Retry Timeout	Error/RetryTimeout	Return Error response	If Error/PostFatalEn = 1, assert FATAL_ERR_N. If Error/ PostNonFatalEn = 1, assert NONFATAL_ERR_N.

All of the above errors return all 1s data for read requests, whether or not the response Error bit is set.

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2.10.3.3 PCI Parity Errors

All PCI devices are required to drive even parity on P_PAR when they are driving the bottom half of the P_AD bus, and on P_PAR64 when they are driving the top half.

The Tsi301 checks parity on the P_AD bus during command/address phases and data phases when it receives data. The Tsi308 then logs bad parity in the DetParErr bit of the Secondary Bus Status CSR. Other action is taken only if enabled by the ParErrRespEn bit in the Bridge Control CSR. The action taken depends on the type of information being transferred at the time of the error and in which direction the transfer was occurring.

Table 10 indicates the CSR bits used to log and enable reporting of each PCI parity error.

Table 10: PCI Parity Errors CSR Bits

Error in	Fatal Interrupt	NonFatal Interrupt	PCI
Command/Address	Error/ CmdPerrFatalEn	Error/ CmdPerrNonFatalEn	If decode has caused the Tsi308 to drive P_DEVSEL_N, Target Abort
Write Data to Tsi308	Not Supported	Not Supported	Assert P_PERR_N
Read Data to Tsi308	Not Supported	Not Supported	Set SecStatus/ MstrDParErr, return HyperTransport error response, and assert P_PERR_N

The Tsi308 may also sample P_PERR_N, asserted when it is driving write data out, indicating that a parity error was detected by the target of the write. If the ParErrRespEn bit is set and the request was a non-posted write, it receives an error response. If the request was a posted write and the PostFatalEn or NonPostFatalEn bits in the Error Control CSR are enabled, the error is signaled by one of the error interrupts.

2.11 Test Features

The following test features are included in the Tsi308 to facilitate testing of the chip.

2.11.1 JTAG

The Tsi308s's JTAG interface is compliant to IEEE 1149.1 standard. The basic test operation is controlled through five pins namely TCK, TMS, TDI, TDO and TRST_N. In Tsi308, JTAG interface is used for Memory BIST, JTAG CSR Read/Write, Force Tri-state, Boundary Scan and Core clock frequency selection during BIST.

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2.11.1.1 Memory BIST Controller

JTAG Memory BIST controller is the interface between JTAG and Memory BIST controllers in each of the four ports. It also decodes JTAG-MBIST instruction and generates BIST enable for the four ports. After BIST operation is over is collects the status information from all the four ports and sends out through JTAG controller.

2.11.1.2 CSR Read/Write Controller

JTAG CSR controller decodes the JTAG-CSR instruction and generates required signals for JTAG CSR read/write operation. It also returns JTAG CSR read data to the JTAG controller.

2.11.1.3 LDT BIST

LDT BIST controller generates Tri-State, Reset, PowerOK signals if JTAG-RUNBIST instruction is executed.

2.11.1.4 Boundary Scan

Boundary Scan is a DFT technique for testing chips and inter-connectivity among chips on printed circuit board. With JTAG insertion to the IC design circuitry, only few signals are needed to control the test activity of the chip instead of the ad-hoc Bed-of-Nails technique.

Boundary Scan JTAG instruction SAMPLE/PRELOAD access the boundary scan register via a data scan operation to take a sample of the functional data entering and leaving the device. This instruction is also used to preload test data into the boundary scan register prior to loading and EXTEST instruction.

The EXTEST instruction places the device into an external boundary test mode and selects the boundary scan register to be connected between TDI and TDO. During this instruction, the boundary scan cells associated with outputs are preloaded with test patterns to test downstream devices. The input boundary cells are set up to capture the input data for later analysis.

2.11.1.5 Signal setting for BSD

Following are the signal values to be set during BSD test.

TMODE

This signal need to be 1’b0 so that MODE1 and for tristate will be generated based on JTAG instructions. In the design, these two signals are forced to 1’b0 when TMODE is high (i.e., during ATPG).

Power Down

For all pads to be active during Boundary Scan, the power down signals generated inside the design have been forced to Low.

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2.11.1.6 Boundary Scan Chain Order

The following is the Boundary Scan Chain Order with the relevant information.

Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
0	bc_4	P1_BYPASS_E	input	*
1	bc_4	TX_BYPASS_CLK_E	input	*
2	bc_7	PLL_SEL_BK	bidir	3
3	bc_1	*	control	*
4	bc_7	PLL_SELDIV2	bidir	5
5	bc_1	*	control	*
6	bc_4	L0_TX_BYPASS_CLK	input	*
7	bc_1	L0_DCLK_TEST	output3	8
8	bc_1	*	control	*
9	bc_1	*	internal	*
10	bc_1	*	internal	*
11	bc_7	P1_TSTDIO	bidir	12
12	bc_1	*	control	*
13	bc_1	P0_TSTCLK	output3	14
14	bc_1	*	control	*
15	bc_1	P0_TSTDI	output3	16
16	bc_1	*	control	*
17	bc_7	P0_TSTDIO	bidir	18
18	bc_1	*	control	*
19	bc_4	P0_TSTDO	input	*
20	bc_1	P0_TSTMOD0	output3	21
21	bc_1	*	control	*
22	bc_1	P0_TSTMOD1	output3	23
23	bc_1	*	control	*
24	bc_1	P0_TSTMS	output3	25

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
25	bc_1	*	control	*
26	bc_1	SROM_SCK	output3	27
27	bc_1	*	control	*
28	bc_7	SROM_SDA	bidir	29
29	bc_1	*	control	*
30	bc_1	P0_RST_N	output3	31
31	bc_1	*	control	*
32	bc_4	P0_BYPASS_E	input	*
33	bc_4	P0_OIR_DISCON_EVENT	input	*
34	bc_4	REFCLK_C_I	input	*
35	bc_4	P0_CLK	input	*
36	bc_7	P0_AD0	bidir	37
37	bc_1	*	control	*
38	bc_7	P0_AD1	bidir	37
39	bc_7	P0_AD2	bidir	40
40	bc_1	*	control	*
41	bc_7	P0_AD3	bidir	40
42	bc_7	P0_AD4	bidir	43
43	bc_1	*	control	*
44	bc_7	P0_AD5	bidir	43
45	bc_7	P0_AD6	bidir	46
46	bc_1	*	control	*
47	bc_7	P0_AD7	bidir	46
48	bc_7	P0_AD8	bidir	49
49	bc_1	*	control	*
50	bc_7	P0_AD9	bidir	49
51	bc_7	P0_AD10	bidir	52

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
52	bc_1	*	control	*
53	bc_7	P0_AD11	bidir	52
54	bc_7	P0_AD12	bidir	55
55	bc_1	*	control	*
56	bc_7	P0_AD13	bidir	55
57	bc_7	P0_AD14	bidir	58
58	bc_1	*	control	*
59	bc_7	P0_AD15	bidir	58
60	bc_7	P0_AD16	bidir	61
61	bc_1	*	control	*
62	bc_7	P0_AD17	bidir	61
63	bc_7	P0_AD18	bidir	64
64	bc_1	*	control	*
65	bc_7	P0_AD19	bidir	64
66	bc_7	P0_AD20	bidir	67
67	bc_1	*	control	*
68	bc_7	P0_AD21	bidir	67
69	bc_7	P0_AD22	bidir	70
70	bc_1	*	control	*
71	bc_7	P0_AD23	bidir	70
72	bc_7	P0_AD24	bidir	73
73	bc_1	*	control	*
74	bc_7	P0_AD25	bidir	73
75	bc_7	P0_AD26	bidir	76
76	bc_1	*	control	*
77	bc_7	P0_AD27	bidir	76
78	bc_7	P0_AD28	bidir	79

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
79	bc_1	*	control	*
80	bc_7	P0_AD29	bidir	79
81	bc_7	P0_AD30	bidir	82
82	bc_1	*	control	*
83	bc_7	P0_AD31	bidir	82
84	bc_7	P0_CBE0_N	bidir	85
85	bc_1	*	control	*
86	bc_7	P0_CBE1_N	bidir	85
87	bc_7	P0_CBE2_N	bidir	88
88	bc_1	*	control	*
89	bc_7	P0_CBE3_N	bidir	88
90	bc_7	P0_DEVSEL_N	bidir	91
91	bc_1	*	control	*
92	bc_7	P0_FRAME_N	bidir	93
93	bc_1	*	control	*
94	bc_7	P0_IRDY_N	bidir	95
95	bc_1	*	control	*
96	bc_7	P0_TRDY_N	bidir	97
97	bc_1	*	control	*
98	bc_7	P0_STOP_N	bidir	99
99	bc_1	*	control	*
100	bc_7	P0_LOCK_N	bidir	101
101	bc_1	*	control	*
102	bc_7	P0_SERR_N	bidir	103
103	bc_1	*	control	*
104	bc_7	P0_PERR_N	bidir	105
105	bc_1	*	control	*

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
106	bc_7	P0_PAR	bidir	107
107	bc_1	*	control	*
108	bc_7	P0_PAR64	bidir	109
109	bc_1	*	control	*
110	bc_7	P0_REQ64_N	bidir	111
111	bc_1	*	control	*
112	bc_7	P0_ACK64_N	bidir	113
113	bc_1	*	control	*
114	bc_4	P0_REQ0_N	input	*
115	bc_4	P0_REQ1_N	input	*
116	bc_4	P0_REQ2_N	input	*
117	bc_4	P0_REQ3_N	input	*
118	bc_4	P0_REQ4_N	input	*
119	bc_4	P0_REQ5_N	input	*
120	bc_1	P0_GNT0_N	output3	121
121	bc_1	*	control	*
122	bc_1	P0_GNT1_N	output3	123
123	bc_1	*	control	*
124	bc_1	P0_GNT2_N	output3	125
125	bc_1	*	control	*
126	bc_1	P0_GNT3_N	output3	127
127	bc_1	*	control	*
128	bc_1	P0_GNT4_N	output3	129
129	bc_1	*	control	*
130	bc_1	P0_GNT5_N	output3	131
131	bc_1	*	control	*
132	bc_1	P0_REQ_OUT_N	output3	133

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
133	bc_1	*	control	*
134	bc_4	P0_GNT_IN_N	input	*
135	bc_4	P0_M66EN	input	*
136	bc_4	P0_PCIX_N	input	*
137	bc_4	P0_PCIX_133_N	input	*
138	bc_4	P0_BLK1_IRQ0	input	*
139	bc_4	P0_BLK1_IRQ1	input	*
140	bc_4	P0_BLK1_IRQ2	input	*
141	bc_4	P0_BLK1_IRQ3	input	*
142	bc_4	P0_BLK1_IRQ4	input	*
143	bc_4	P0_BLK0_IRQ4	input	*
144	bc_4	P0_BLK0_IRQ0	input	*
145	bc_4	P0_BLK0_IRQ1	input	*
146	bc_4	P0_BLK0_IRQ2	input	*
147	bc_4	P0_BLK0_IRQ3	input	*
148	bc_4	L1_TX_BYPASS_CLK	input	*
149	bc_1	L1_DCLK_TEST	output3	150
150	bc_1	*	control	*
151	bc_1	L1_CCLK_TEST	output3	152
152	bc_1	*	control	*
153	bc_4	P1_M66EN	input	*
154	bc_4	P1_PCIX_N	input	*
155	bc_4	P1_PCIX_133_N	input	*
156	bc_4	P1_OIR_DISCON_EVENT	input	*
157	bc_4	P1_BLK1_IRQ0	input	*
158	bc_4	P1_BLK1_IRQ1	input	*
159	bc_4	P1_BLK1_IRQ2	input	*

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
160	bc_4	P1_BLK1_IRQ3	input	*
161	bc_4	P1_BLK1_IRQ4	input	*
162	bc_4	P1_BLK0_IRQ0	input	*
163	bc_4	P1_BLK0_IRQ4	input	*
164	bc_4	P1_BLK0_IRQ1	input	*
165	bc_4	P1_BLK0_IRQ2	input	*
166	bc_4	P1_BLK0_IRQ3	input	*
167	bc_1	PCIB_CLK_TEST	output3	168
168	bc_1	*	control	*
169	bc_1	P1_RST_N	output3	170
170	bc_1	*	control	*
171	bc_4	P1_CLK	input	*
172	bc_7	P1_AD0	bidir	173
173	bc_1	*	control	*
174	bc_7	P1_AD1	bidir	173
175	bc_7	P1_AD2	bidir	176
176	bc_1	*	control	*
177	bc_7	P1_AD3	bidir	176
178	bc_7	P1_AD4	bidir	179
179	bc_1	*	control	*
180	bc_7	P1_AD5	bidir	179
181	bc_7	P1_AD6	bidir	182
182	bc_1	*	control	*
183	bc_7	P1_AD7	bidir	182
184	bc_7	P1_AD8	bidir	185
185	bc_1	*	control	*
186	bc_7	P1_AD9	bidir	185

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
187	bc_7	P1_AD10	bidir	188
188	bc_1	*	control	*
189	bc_7	P1_AD11	bidir	188
190	bc_7	P1_AD12	bidir	191
191	bc_1	*	control	*
192	bc_7	P1_AD13	bidir	191
193	bc_7	P1_AD14	bidir	194
194	bc_1	*	control	*
195	bc_7	P1_AD15	bidir	194
196	bc_7	P1_AD16	bidir	197
197	bc_1	*	control	*
198	bc_7	P1_AD17	bidir	197
199	bc_7	P1_AD18	bidir	200
200	bc_1	*	control	*
201	bc_7	P1_AD19	bidir	200
202	bc_7	P1_AD20	bidir	203
203	bc_1	*	control	*
204	bc_7	P1_AD21	bidir	203
205	bc_7	P1_AD22	bidir	206
206	bc_1	*	control	*
207	bc_7	P1_AD23	bidir	206
208	bc_7	P1_AD24	bidir	209
209	bc_1	*	control	*
210	bc_7	P1_AD25	bidir	209
211	bc_7	P1_AD26	bidir	212
212	bc_1	*	control	*
213	bc_7	P1_AD27	bidir	212

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
214	bc_7	P1_AD28	bidir	215
215	bc_1	*	control	*
216	bc_7	P1_AD29	bidir	215
217	bc_7	P1_AD30	bidir	218
218	bc_1	*	control	*
219	bc_7	P1_AD31	bidir	218
220	bc_7	P1_CBE0_N	bidir	221
221	bc_1	*	control	*
222	bc_7	P1_CBE1_N	bidir	221
223	bc_7	P1_CBE2_N	bidir	224
224	bc_1	*	control	*
225	bc_7	P1_CBE3_N	bidir	224
226	bc_7	P1_DEVSEL_N	bidir	227
227	bc_1	*	control	*
228	bc_7	P1_FRAME_N	bidir	229
229	bc_1	*	control	*
230	bc_7	P1_IRDY_N	bidir	231
231	bc_1	*	control	*
232	bc_7	P1_TRDY_N	bidir	233
233	bc_1	*	control	*
234	bc_7	P1_STOP_N	bidir	235
235	bc_1	*	control	*
236	bc_7	P1_LOCK_N	bidir	237
237	bc_1	*	control	*
238	bc_7	P1_SERR_N	bidir	239
239	bc_1	*	control	*
240	bc_7	P1_PERR_N	bidir	241

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Table 11: Boundary Scan Chain Order

Order	Bcell	Signal	Function	Control Number
241	bc_1	*	control	*
242	bc_7	P1_PAR	bidir	243
243	bc_1	*	control	*
244	bc_4	P1_REQ0_N	input	*
245	bc_4	P1_REQ1_N	input	*
246	bc_4	P1_REQ2_N	input	*
247	bc_4	P1_REQ3_N	input	*
248	bc_4	P1_REQ4_N	input	*
249	bc_4	P1_REQ5_N	input	*
250	bc_1	P1_GNT0_N	output3	251
251	bc_1	*	control	*
252	bc_1	P1_GNT1_N	output3	253
253	bc_1	*	control	*
254	bc_1	P1_GNT2_N	output3	255
255	bc_1	*	control	*
256	bc_1	P1_GNT3_N	output3	257
257	bc_1	*	control	*
258	bc_1	P1_GNT4_N	output3	259
259	bc_1	*	control	*
260	bc_1	P1_GNT5_N	output3	261
261	bc_1	*	control	*
262	bc_1	P1_REQ_OUT_N	output3	263
263	bc_1	*	control	*
264	bc_4	P1_GNT_IN_N	input	*
265	bc_4	L_POWER_OK	input	*
266	bc_4	LDTSTOP_N	input	*

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2.11.2 SCAN and ATPG

The Tsi308 implements a total of 21 scan chains. All of these 21 scan inputs and scan outputs are shared with various functional pins. The scan operation is controlled by the input signals, SCAN_EN and TMODE.

Scan Input and Output Pins lists the mapping of scan input and output pins onto functional pins.

Table 12: Scan Input and Output Pins

Chain Number	Scan Input	Scan Output
1	P0_BLK1_IRQ4	P1_AD0
2	P0_BLK0_IRQ4	P1_AD1
3	P0_BLK1_IRQ3	P1_AD2
4	P0_BLK1_IRQ2	P1_AD3
5	P0_BLK1_IRQ1	P1_AD4
6	P0_BLK1_IRQ0	P1_AD5
7	P0_BLK0_IRQ3	P1_AD6
8	P0_BLK0_IRQ2	P1_AD7
9	P0_BLK0_IRQ1	P1_AD8
10	P0_BLK0_IRQ0	P1_AD9
11	P1_BLK1_IRQ4	P1_AD10
12	P1_BLK0_IRQ4	P1_AD11
13	P1_BLK1_IRQ3	P1_AD12
14	P1_BLK1_IRQ2	P1_AD13
15	P1_BLK1_IRQ1	P1_AD14
16	P1_BLK1_IRQ0	P1_AD15
17	P1_BLK0_IRQ3	P1_AD16
18	P1_BLK0_IRQ2	P1_AD17
19	P1_BLK0_IRQ1	P1_AD18
20	P1_BLK0_IRQ0	P1_AD19
21	P0_REQ0_N	P0_TSTDI

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3. Clock Frequency and Mode Selection Hardware Straps

This chapter discusses the following topics about the Tsi308:

- "Overview" on page 67
- "Core Clock Frequency Selection in RevC mode" on page 69
- "PCI Bus A Frequency Selection in RevC mode" on page 70
- "PCI Bus B Frequency Selection in RevC mode" on page 70
- "PCI Bus A and Core Clock Frequency Selection in non-RevC mode" on page 71
- "PCI Bus B Frequency Selection in non-RevC mode" on page 72
- "Link Frequency Selection (Tsi301 mode only)" on page 72
- "Miscellaneous Straps" on page 74

3.1 Overview

Tsi308 has five PLLs: HT0_PLL_0, HT1_PLL_1, CORE_PLL, PCI_A_PLL and PCI_B_PLL.

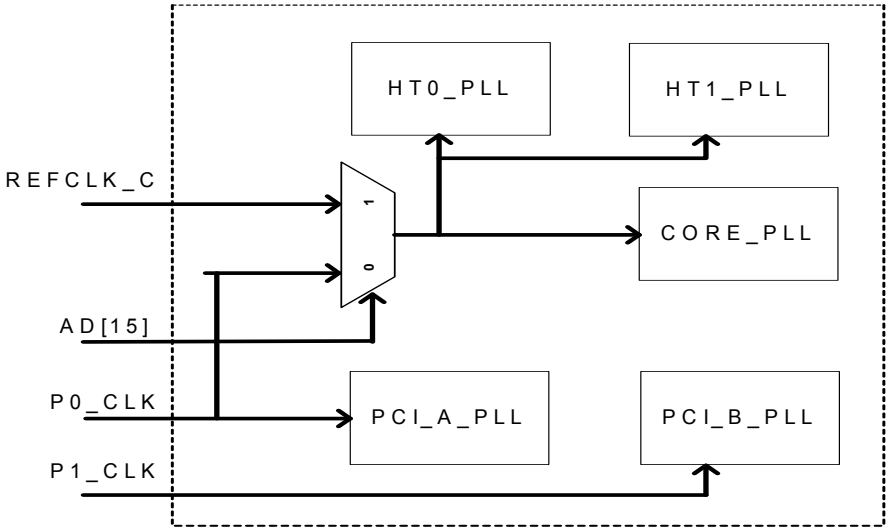
The reference clock for the first three PLLs is REFCLK_C in RevC mode and P0_CLK in non-RevC mode. The reference clock for PCI_A_PLL is P0_CLK and the reference clock for PCI_B_PLL is P1_CLK.

- HT0_PLL generates the HyperTransport transmit clock for Link 0.
- HT1_PLL generates the HyperTransport transmit clock for Link 1.
- CORE_PLL generates the clock for core logic.
- PCI_A_PLL generates the clock (PCI_CLK_A) for PCI bus A interface logic.
- PCI_B_PLL generates the clock(PCI_CLK_B) for PCI bus B interface logic.

Tsi308 Revision C is backward pin compatible with previous revisions(A & B). Tsi308 Revision C device can be dropped into the boards made for previous revisions. AD[15] is used to select between RevC or non-RevC modes. AD[15] = 1 for RevC mode and AD[15] = 0 for non-RevC mode.

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Figure 4: Primary clock inputs to Tsi308 PLLs



When operating in ‘non-RevC’ mode, P0_CLK is fed to an internal PLL that generates clock for the PCI_A interface logic as well as core clock. The P0_CLK is also fed to two other internal PLLs that generate HyperTransport transmit clocks for both the linksThe P1_CLK is fed to yet another PLL that generates clock for the PCI_B interface logic.

If the Tsi308 is to perform synchronous link initialization with HyperTransport devices on either side of it, the reference clock (P0_CLK) must be derived from the same base frequency source. If not, asynchronous link initialization must be used. No phase relationship is required in either mode.

When operating in ‘RevC mode’, Tsi308 derives core clock from REFCLK_C. RevC mode is set through hardware strap option. A CORE PLL is used to generate core clock. REFCLK_C is also fed to internal PLLs that generate HyperTransport transmit clocks for both the links. P0_CLK and P1_CLK are fed to corresponding internal PLLs that generate clocks for the PCI_A and PCI_B iterface logic respectively. If the Tsi308 is to perform synchronous link initialization with HyperTransport devices on either side of it, the reference clock (REFCLK_C) must be derived from the same base frequency source.

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For debug and test purposes, the Tsi308 allows bypassing of HT PLLs. It provides separate bypass clock inputs to both the HT links. All bypass clocks must be derived from the same base frequency source. The PCI_A ,PCI_B and core PLLs also can be bypassed. When PCI PLLs are bypassed PCI_A interface is run directly at P0_CLK and PCI_B interface is run directly at P1_CLK. When CORE PLL is bypassed, core runs directly at REFCLK_C in 'RevC mode' and runs directly at P0_CLK at other modes.



For all the straps that use P0_AD bus, logic 1 assumes that the signal is pulled high to 3.3v supply through a 4.7k ohm resister and logic 0 assumes that the signal is pulled low to ground through a 4.7k ohm resister.

Following sections describe the strap options.

3.2 Core Clock Frequency Selection in RevC mode

All the inputs to Core PLL are taken from the straps. These strap values are taken during cold reset period. Table 13 shows the valid strap combinations for Core PLL.

Table 13: Core Clock Frequency Selection Straps in RevC mode

P0_AD[23,22,21,20]	REFCLK_C (MHz)	Core Clock (MHz)
0001	25	100
0010	25	200
0011	33	133
0100	33	200
0101	50	100
0110	50	200
0111	66	133
1000	66	200
1001	100	200
1010	133	200
All other values are reserved		

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3.3 PCI Bus A Frequency Selection in RevC mode

Table 14 shows the valid strap combinations for PCI-A PLL.

Table 14: PCI-A Clock Frequency Selection Straps in RevC mode

P0_133_N	P0_PCIX_N	P0_M66EN	MODE	P0_AD[6]	PCI_CLK_A (MHz)
1	1	0	PCI	1	25
1	1	0	PCI	0	33
1	1	1	PCI	1	50
1	1	1	PCI	0	66
1	0	N/A	PCI-X	1	50
1	0	N/A	PCI-X	0	66
0	0	N/A	PCI-X	1	100
0	0	N/A	PCI-X	0	133

3.4 PCI Bus B Frequency Selection in RevC mode

Table 15 shows the valid strap combinations for PCI-A PLL.

Table 15: PCI-B Clock Frequency Selection Straps

P0_133_N	P1_PCIX_N	P1_M66EN	MODE	P0_AD[7]	PCI_CLK_A (MHz)
1	1	0	PCI	1	25
1	1	0	PCI	0	33
1	1	1	PCI	1	50
1	1	1	PCI	0	66
1	0	N/A	PCI-X	1	50
1	0	N/A	PCI-X	0	66
0	0	N/A	PCI-X	1	100
0	0	N/A	PCI-X	0	133

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3.5 PCI Bus A and Core Clock Frequency Selection in non-RevC mode

Table 16 shows all the valid strap combinations for setting PCI_CLK_A exact operating frequency that is also used to generate CoreClock.

Table 16: P0_CLK and CoreClock Frequency Selection Straps

P0_133_N	P0_PCIX_N	P0_M66EN	MODE	P0_AD[21,23:22]	P0_CLK/ PCI_CLK_A (MHz)	CoreClock (MHz)
1	1	0	PCI	001	25	100
1	1	0	PCI	011	25	200
1	1	0	PCI	000	33	133
1	1	0	PCI	010	33	200
1	1	0	PCI	110	Reserved	Reserved
1	1	1	PCI	001	50	100
1	1	1	PCI	011	50	200
1	1	1	PCI	000	66	133
1	1	1	PCI	010	66	200
1	1	1	PCI	110	Reserved	Reserved
1	0	N/A	PCI-X	001	50	100
1	0	N/A	PCI-X	011	50	200
1	0	N/A	PCI-X	000	66	133
1	0	N/A	PCI-X	010	66	200
1	0	N/A	PCI-X	110	Reserved	Reserved
0	0	N/A	PCI-X	001	100	200
0	0	N/A	PCI-X	011	Reserved	Reserved
0	0	N/A	PCI-X	000	133	200
0	0	N/A	PCI-X	010	Reserved	Reserved

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3.6 PCI Bus B Frequency Selection in non-RevC mode

Table 17 lists all the valid strap combinations that indicate operating frequency of P1_CLK that is also used to generate PCI_CLK_B.

Table 17: P1_CLK Frequency Selection Straps

P1_133_N	P1_PCIX_N	P1_M66EN	MODE	P0_AD[7]	P1_CLK/ PCI_CLK_B (MHz)
1	1	0	PCI	1	25
1	1	0	PCI	0	33
1	1	1	PCI	1	50
1	1	1	PCI	0	66
1	0	N/A	PCI-X	1	50
1	0	N/A	PCI-X	0	66
0	0	N/A	PCI-X	1	100
0	0	N/A	PCI-X	0	133

3.7 Link Frequency Selection (Tsi301 mode only)

Table 18 lists the valid strap combinations to preload HyperTransport Link 0 and Link 1 frequency.



This table is valid only when Tsi308 is operating in Tsi301 compatible mode. The link frequencies are initialized as specified in HyperTransport specification in normal mode.

Table 18: Link Transmit Clock Frequency Selection Straps

L0_clkSel (P0_AD[29:27])/ L1_clkSel (P0_AD[26:24])	Lx_TX_CLK_H/L (MHz)
001	200
010	300
000	400
011	500
100	600

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Table 18: Link Transmit Clock Frequency Selection Straps

L0_clkSel (P0_AD[29:27])/ L1_clkSel (P0_AD[26:24])	Lx_TX_CLK_H/L (MHz)
101	Reserved
110	Reserved
111	Reserved

For proper functioning of Tsi308, Core clock should be greater than or equal to 1/4th HT Link Frequency(DDR).

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3.8 Miscellaneous Straps

Table 18 lists the other miscellaneous mode selection straps.

Table 19: Miscellaneous Pin Straps

Strap / Pin Number	Description	Encoding	Comments
P0_AD[19] / A10	Link 0 Sync Pointer Control: When set, indicates that Link 0 transmit clock is derived from the same time base as the receive clock in the device to which it is connected. That means P0_CLK that is used by Tsi308 to generate L0_TX_CLK_H/L should be used by the device that is connected to Tsi308's Link 0 to generate its internal core clock that receives the data from Link 0.	0 -> Async 1 -> Sync	
P0_AD[18] / B10	Link 1 Sync Pointer Control: When set, indicates that Link 1 transmit clock is derived from the same time base as the receive clock in the device to which it is connected. That means P0_CLK that is used by Tsi308 to generate L1_TX_CLK_H/L should be used by the device that is connected to Tsi308's Link 1 to generate its internal core clock that receives the data from Link 1.	0 -> Async 1 -> Sync	
P0_AD[14] / B9	PCI/PCI-X Bus 0 Data Width: Configures the Tsi308 either as a single 64-bit bus or dual 32-bit (split bus) mode.	0 -> 64-bit 1 -> 32-bit	
P0_AD[2] / B5	PCI/PCI-X Bus 1 Enable: When set, enables Tsi308's 2nd 32-bit PCI/PCI-X bus. When cleared, Tsi308 will operate in single 32-bit or 64-bit bus mode depending on the value set on P0_AD[14].	1 -> Enabled 0 -> Disabled	May be set only when P0_AD[14] is cleared.

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Table 19: Miscellaneous Pin Straps

Strap / Pin Number	Description	Encoding	Comments
P0_AD[1] / C5	Reserved and should be driven zero	Must be set to 0.	
P0_AD[5] / B6	MOD_SEL_Tsi301: When set, configures Tsi308 to operate in IDT's previous generation Tsi301 software backward compatible mode.	1 -> Tsi301 0 -> Normal mode	
P0_AD[4] / C6	AP0_TYPEDET_N: When set, configures Tsi308's PCI Bus 0 input buffers to be 5V tolerant.	0 -> 3.3 V 1 -> 5 V	
P0_AD[3] / A5	AP1_TYPEDET_N: When set, configures Tsi308's PCI Bus 1 input buffers to be 5V tolerant.	0 -> 3.3 V 1 -> 5 V	
P0_AD[31] / B14	minRstCnt: ALSC Reserved.	Must be set to 0.	
PLL_TESTENB / AB1	Internal PLL Test Mode: ALSC Reserved.	Must be set to 1.	
P0_BYPASS_E / B3	PCI_A PLL Bypass Mmode: ALSC Reserved.	Must be set to 0.	
P1_BYPASS_E / AD3	PCI _B PLL Bypass Mode: ALSC Reserved.	Must be set to 0.	
L0_TX_BYPASS_CLK / AB2	HT Link 0 Transmit Bypass Clock: ALSC Reserved.	Should be set to 0.	
L1_TX_BYPASS_CLK / E25	HT Link 1 Transmit Bypass Clock: ALSC Reserved.	Should be set to 0.	
P0_AD[30] / C14	Reserved.	Current implementations should set to 0.	Reserved for future use.
P0_AD[20] / D11	Reserved.	Current implementation should set to 0.	Reserved for future use.

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Table 19: Miscellaneous Pin Straps

Strap / Pin Number	Description	Encoding	Comments
TMODE / AC3	Test Mode: ALSC Reserved.	Must be set to 0.	Used to bypass normal resets during ATPG scan mode. Also used to enable “capture” operation of scan
TRST_N / AB24	Test Mode Reset. ALSC Reserved.	Must be pulled low for normal operation	
SCAN_EN / AB3	Scan Enable: ALSC Reserved.	Should be set to 0.	Used during scan shift/hold operations of ATPG
P0_OIR_DISCON_EVENT / A3	Reserved.	Must be set to 0.	
P1_OIR_DISCON_EVENT / AB23	Reserved.	Must be set to 0.	
SPARE_PIN_1 / B2	REFCLK_C	RefClk C	REFCLK in Rev C mode
STOP_P0 / A2	ALSC Reserved.	Should be set to 0.	Reserved for future use.
STOP_P1 / A25	ALSC Reserved.	Should be set to 0.	Reserved for future use.

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4. Register Descriptions

This chapter discusses the following topics about Tsi308's registers:

- "Configuration Registers" on page 78
- "Summary of Configuration Registers" on page 81
- "64-bit Address Remapping Capability Indices" on page 85

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4.1 Configuration Registers

This chapter provides details about the configuration registers or control and status registers (CSRs) that Tsi308 implements for software to access and program. The Tsi308 supports various modes of operation and the following section outlines these operating modes.

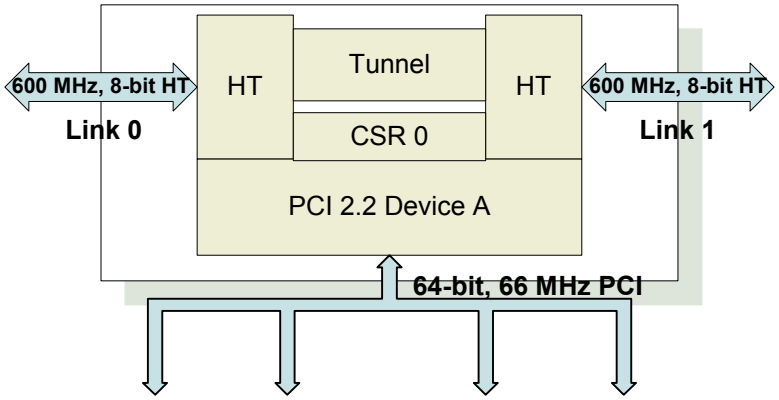
4.1.1 Operating Modes

From the software's viewpoint Tsi308 implements two major operating modes; Tsi301 backward compatible mode or Tsi301 mode and standard HT 1.05 compliant Tsi308 mode. Each of these two modes in turn support either a single 64-bit PCI-X (PCI) device or dual 32-bit PCI-X (PCI) devices.

4.1.1.1 Single Tsi301 (SP) Mode

In Single Tsi301 mode, Tsi308 behaves just like previous generation Tsi301 chip from software's viewpoint. It implements Tsi301 software compatible register set as specified in [5], so that existing software driver that is written for Tsi301 will work seamlessly. In this mode device may not support some of the features that are defined in HT 1.05 specification. However this mode provides some features that are not existent in Tsi301 chip in software transparent way, for example this mode supports HT link speeds up to 600 MHz beyond the 400 MHz supported by Tsi301 chip. This mode supports both sharing and non-sharing dual hosted chain implementation and allowed End Of Chain (EOC) bit to be set in any of the two links.

Figure 5: Single Tsi301 Mode

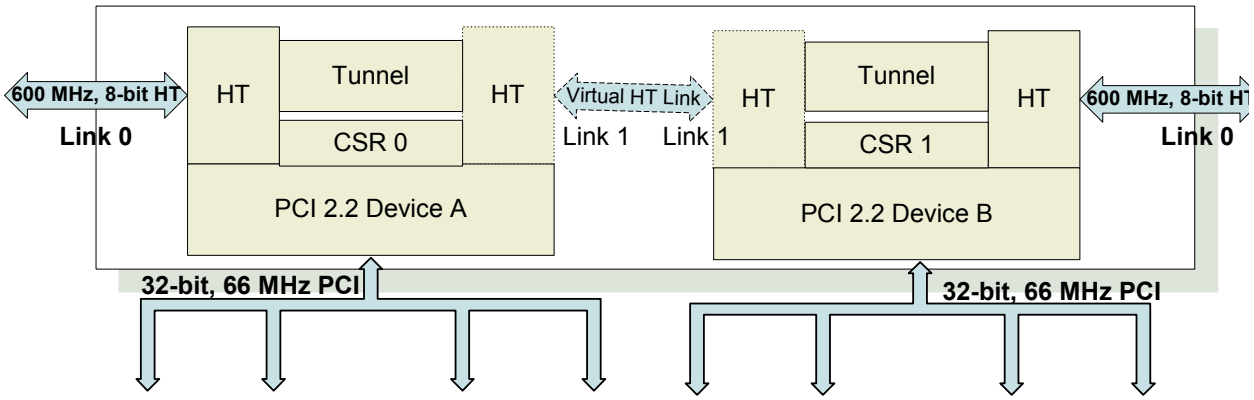


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4.1.1.2 Dual Tsi301 (DSP) Mode

The Dual Tsi301 Mode is same as Single Tsi301 Mode from software point of view, except that this mode implements two independently configured 32-bit PCI devices. The software views this mode as two independent 8-bit HyperTransport tunnel devices (nodes) each bridging to a 32-bit PCI. It implements two identical sets of CSR one for each of the two devices, Device A and Device B. The connection between two devices is through the emulation of a software transparent internal virtual link. This mode supports both sharing and non-sharing dual hosted chain implementation and also allows the logical End Of Chain (EOC) to be set in any of the two links of either device.

Figure 6: Dual Tsi301 Mode

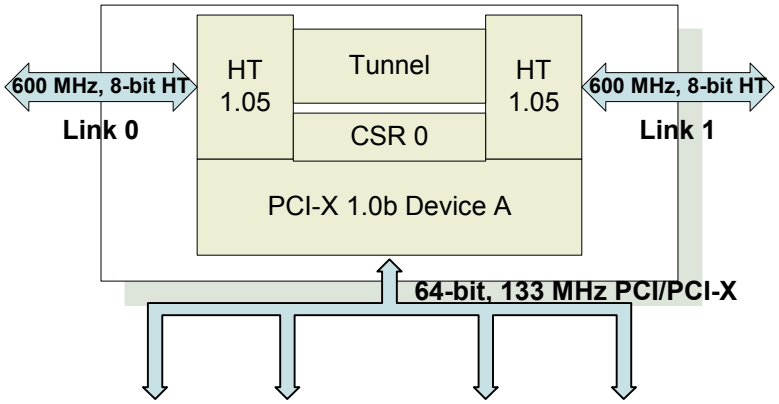


4.1.1.3 Tsi308 Single PCI-X Mode (GSP)

This mode implements standard HT 1.05 compliant tunnel device bridging to a single 64-bit PCI-X bus that can be operated in traditional PCI mode as well. The PCI-X mode is compliant to [3] and the standard PCI mode is compliant to [2]. The device A implements desired PCI-X functionality and device B is disabled in this mode. This mode supports both sharing and non-sharing dual hosted chain implementation and also allows End Of Chain to be set in either of the two links.

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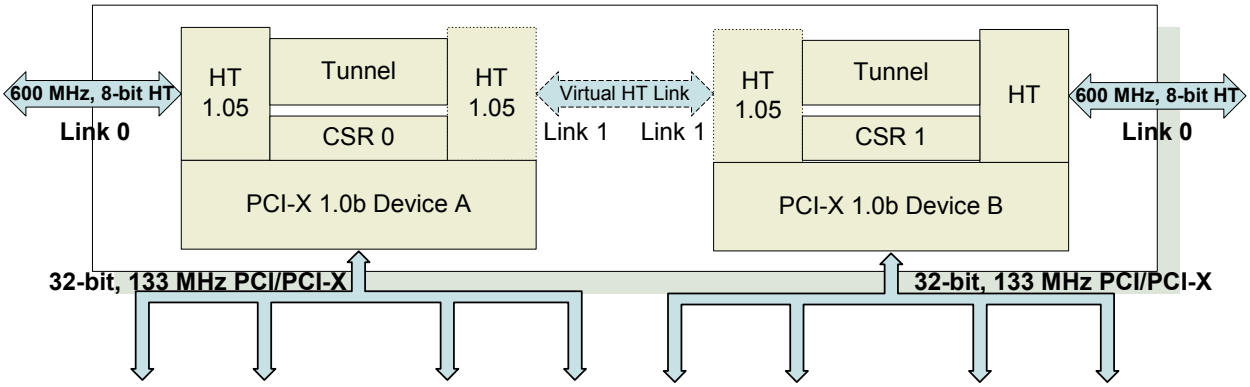
Figure 7: Tsi308 **Single PCI-X Mode**



4.1.1.4 Tsi308 Dual PCI-X Mode (GDP)

This mode implements standard HT 1.05 compliant tunnel device bridging to two independently configured 32-bit PCI-X buses. The software views this mode as two independent 8-bit HyperTransport tunnel devices (nodes) each bridging to a 32-bit PCI-X. It implements two independently configured CSR sets one for each of the two devices, Device A and Device B. The connection between two devices is through the emulation of a software transparent internal virtual link. This mode supports both sharing and non-sharing dual hosted chain implementation and also allows the logical End Of Chain (EOC) to be set in any of the two links of either device.

Figure 8: Tsi308 **Dual PCI-X Mode**



4.1.2 Configuration Mechanism

Configuration accesses are accepted from HyperTransport to the Tsi308 internal CSRs if they are Type 0 accesses with a device number equal to the value in the BaseUnitId field of the HyperTransport Command CSR (CSR 0 for Device A, CSR 1 for Device B if enabled).

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4.2 Summary of Configuration Registers

Table 20 summarizes the Tsi308 configuration register fields and offsets for various modes of operation. Since Tsi308 supports different modes of operation, some of the fields exist in more than one mode and may take different meaning. The following sub-sections describe the usage model.

4.2.1 Register Access Definitions

Access types are indicated as follows:

- R – Read. A read of this register returns the field.
- W – Write. A write of this register loads the value.
- C – Clear. A write of 1 to this field clears the field.

4.2.2 Register Access Rules

The following rules apply to Tsi308 CSR accesses.

- Reads to undefined fields return undefined data.
- Read Only fields are blocked from being written and return default values when read.

4.2.3 Mode Encodings

As described in previous sections the following abbreviations are used to denote various operating modes of Tsi308.

- **SP – Single Tsi301 mode:** Implements a 8-bit tunnel device (Device A) bridging to a single 64-bit PCI. It uses CSR 0 only and Device B and corresponding CSR 1 is not visible to the software. This mode supports both 32 and 64 bit PCI. CSR is software compatible to previous generation Tsi301 chip.
- **DSP – Dual Tsi301 mode:** Behaves as if two Tsi301 software compliant devices in single chip. CSR 0 is used by Device A and CSR 1 is used by Device B. This mode supports only 32-bit PCI devices.
- **GSP – Tsi308 Single PCI-X Mode:** Implements standard HT 1.05 compliant tunnel device with bridge to single 64-bit PCI-X. Only Device A is active and uses CSR 0. Device B and corresponding CSR 1 is not visible to software in this mode.
- **GDP – Tsi308 Dual PCI-X Mode:** Implements two standard HT1.05 compliant tunnel devices each bridging to a 32-bit PCI-X. Device A uses CSR 0 and Device B uses CSR 1.

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4.2.4 CSR Layout

Table 20 lists the layout of all the fields including offsets. The fields are color-coded to denote:

- Fields are valid in GSP, GDP and reserved in SP and DSP.
- Fields are multifunctional. They have different meaning in each mode.
- Fields are valid in SP and DSP modes. Reserved in GSP and GDP modes.
- Uncolored fields are valid in all the modes

Since Tsi308 implements two identical sets of CSR in dual device mode, only one set is described below and it has:

- Standard 256 byte space (00h-FFh) that can be accessed using the corresponding Device ID.
- Indirectly accessed 64-bit Address Remapping Registers
- Indirectly accessed Interrupt Definition Registers
- Indirectly accessed SROM Registers

Table 20: Tsi308 **CSR Header**

Device ID		Vendor ID		00
Status		Command		04
Class Code			Revision ID	08
BIST	Header Type	Primary Latency Timer	Cache line	0C
Base Address Register 0				10
Base Address Register 1				14
Sec Latency Timer	Subordinate Bus No.	Secondary Bus No.	Primary Bus No.	18
Secondary Bus Status		I/O Limit Addr	I/O Base Addr	1C
Memory Range Limit Addr		Memory Range Base Addr		20
Prefetchable Memory Range Limit Addr		Prefetchable Memory Range Base Addr		24
Prefetchable Memory Range Base Upper 32 bits				28
Prefetchable Memory Range Limit Upper 32 bits				2C
I/O Range Limit Upper 16 bits		I/O Range Base Upper 16 bits		30
Reserved			Capability 1 (Capabilities Pointer)	34
Expansion ROM				38

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Table 20: Tsi308 **CSR Header**

Bridge Control		Interrupt Pin	Interrupt Line	3C
HT Command (Slave/Primary)		Capability 2 (Capabilities Pointer)	HT Capability ID	40
Link 0 Width Control		HT Link 0 Control		44
Link 1 Width Control		HT Link 1 Control		48
Link 0 Freq Cap		Link 0 Freq/Error	HT Rev. ID	4C
Link 1 Freq Cap		Link 1 Freq/Error	Feature	50
Error Handling		Enumeration Scratch Pad		54
Reserved		Memory Limit Upper	Memory Base Upper	58
Reserved	Read Control 2			5C
PCI Control 1	Read Control 1			60
Error Control				64
Reserved	ParErr Report En	HT Error Control		68
Reserved	Transmit Control	HT Rx Data Buffer Allocation		6C
Link Impedance Control 0				70
Link Impedance Control 1				74
Capability Type (Interrupt Discovery and Configuration)	Index	Capability 3 (Capabilities Pointer)	HT Capability ID	78
Data port				7C
Reserved				80
Reserved				84
Reserved				88
Reserved				8C
Reserved				90
Reserved				94
Reserved				98
Reserved				9C
Block 0, Interrupt 1		Block 0, Interrupt 0		A0

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Table 20: Tsi308 **CSR Header**

Block 0, Interrupt 3		Block 0, Interrupt 2		A4
Block 1, Interrupt 1		Block 1, Interrupt 0		A8
Block 1, Interrupt 3		Block 1, Interrupt 2		AC
Block 1, Interrupt 4		Block 0, Interrupt 4		B0
Cap. Type (UnitID Clumping)	Reserved	Capability 4 (Capabilities Pointer)	HT Capability ID	B4
Clumping Support			R	B8
Clumping Enable			R	BC
Power Management Capabilities		Capability 7 (Capabilities Pointer)	PCI Power Mgmt. Capability ID	C0
Data	Bridge Support Extns	Power Management Control/Status Registers		C4
Reserved	Transmit Buffer Counter Max. 0			C8
Reserved	Transmit Buffer Counter Max. 1			CC
Reserved	SMAF Field	StoreForward	Test port	D0
Reserved			Sri Index	D4
Sri Data				D8
Diagnostics Link 0 Receive CRC Expected				DC
Cap. Type (Address Mapping Extension Block)	Type	I/O Size	# of DMA Map	Capability 5 (Capabilities Pointer)	HT Capability ID	E0
Reserved					Index	E4
Data Lower						E8
Data Upper						EC
PCIX Sec. Status			Capability 6 (Capabilities Pointer)		PCI-X Capability ID	F0
PCIX Bridge Status						F4
Upstream Split Transaction Control						F8
Downstream Split Transaction Control						FC

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4.3 64-bit Address Remapping Capability Indices

Table 21 lists the fields of 64-bit Address Remap Registers as specified in [1]. These fall under 64-bit Address Remapping Capability Block (Capability 4). The block is located at offset E0h-ECh, the registers under this block are accessed through the Index register at offset E4h and Data register at offset E8h-E9h. As shown in Table 21, the Tsi308 implements 64-bit Address Remapping Capability and a single upstream DMA window.

Table 21: 64-bit Address Remap Indexed Registers

Index 31			Index 0
00h	SBNP Window Base Lower	Reserved	SBNPCtrl
	SBNP Window Base Upper		
01h	SBPre Window Base Lower	Reserved	SBPreCtrl
	SBPre Window Base		
02h	Primary Bus Non-Prefetchable Window Base Upper		
	Primary Bus Non-Prefetchable Window Limit Upper		
03h	Reserved		
	Reserved		
04h	DMA Primary Base0 Lower	Reserved	DMACtrl0
	DMA Primary Base 0 Upper		
05h	DMA Secondary Base 0 Lower	Reserved	
	DMA Secondary Base 0 Upper		
06h	DMA Secondary Limit 0 Lower	Reserved	
	DMA Secondary Limit 0 Upper		
07h	Reserved		
	Reserved		

4.3.1 ISOC Bit Setting

Upstream requests that pass through the DMA window defined in Table 21, will have Isoc bit set if bit 2 (Isochronous) of DMA Window Control Register (DMACtrl0) is set. Note that it will only affect the bit setting and Tsi308 still sends traffic through same three base virtual channels. It doesn't implement dedicated Isochronous Virtual Channel buffers.

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4.3.2 Read Control 2 Register

The controls (prefetch length, prefetch count etc.) set in Read Control 2 register (offset 5Eh-5Ch) are used for upstream traffic that is passing through the address ranges of DMA window defined in Table 21.

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4.3.3 Interrupt Definition Registers

The Interrupt Definition Registers fall under Interrupt Discovery and Configuration Capability Block (Capability 2) located at offsets 78h-7Ch. The fields of Interrupt Definition Registers are as shown in Table 22, these are accessed indirectly through Index register located at offset 7Ah and Data register located at offset 7Ch-7Fh. The Tsi308 implements 10 interrupt sources per device, and each one of these interrupt sources implement a 64-bit definition register shown below. The register for Interrupt 0 would occupy indexes 10h and 11h, Interrupt 1 uses 12h and 13h, etc. Bits 31:0 are accessed through the lower (even) index and bits 63:32 are accessed through the high (odd) index.

Interrupts are programmed through Interrupt Definition Registers in RevB mode whereas they are programmed through IOAPIC Registers in RevC mode. So, Interrupt Definition Registers are valid only in RevB mode and they are reserved but may return non-zero value when read in Rev.C mode. This is because these registers are used in IOAPIC mode also.

Table 22: Interrupt Definition Registers

Bit	R/W Access	Initial Value	Field Name and Description
63	R/C	0	**Waiting for EOI:** If RQEOI is 1, then this bit is set by hardware when an interrupt request is sent and cleared by hardware when the EOI is returned. Software may write a 1 to this bit to clear it without an EOI.
62	R	1	**PassPW**: When 1, interrupt messages will be sent with the PassPW bit set and no ordering of the message with other upstream cycles is guaranteed. When 0, interrupt messages will be sent with PassPW clear, and the device must guarantee that the interrupt message will not pass upstream posted cycles within its queues. If a device supports only one of these behaviors, this bit is read-only and indicates which behavior is supported. For Tsi308, this bit is hardcoded to 1.
61:56	R	0	Reserved
55:32	R/W	0	IntrInfo[55:32]
31:24	R/W	F8h	**IntrInfo[31:24]:** Must default to F8h for compatibility with HT technology 1.01 and earlier devices. Values of F9 or above must not be used or conflicts with non-interrupt address spaces will result. Some hosts only recognize interrupts with this field set to F8h.
23:8	R/W	0	IntrInfo[23:8]
7	R	0	IntrInfo[7] *For Tsi308, this bit is hardcoded to 0.*

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Table 22: Interrupt Definition Registers

Bit	R/W Access	Initial Value	Field Name and Description
6	R/W	0	IntrInfo[6]
5	R/W	0	**IntrInfo[5]**: **Request EOI:** When set, after each interrupt request is sent, the device waits for the waiting for EOI bit to be cleared before sending another interrupt
4:2	R/W	0	**IntrInfo[4:2]: Message Type:** Some devices may allow only certain application-specific combinations of message type with other bits.
1	R/W	0	**Polarity:** For external interrupt sources, when this bit is set, the interrupt signal is active low. When clear, the interrupt signal is active-high. For internal interrupt sources, this bit is reserved
0	R/W	1	**Mask:** When this bit is set, interrupt messages will not be sent from this source.

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4.3.4 SRI Indices

This section defines the registers that are accessed indirectly through Sri Index located at offset D4h and Data register at offset D8h. All the offsets listed are accessed indirectly through Sri Index.

4.3.4.1 GG-Link0 Impedance Control Registers

These registers are in addition to the Link0 Impedance Control (73h-70h) registers. These extra registers are needed because impedance calibrator circuit used in Tsi308 is different from Tsi301.

Register Offset: 14h (indirect through Sri Index located at offset D4h)

Bit	R/W Access	Initial Value	Field Name and Description
2:0	R	010b	AvgWeight(n): The averaging weight. The default value is 2. avg = avg*(1-2**-n)+sample*2**-n
7:3	R	00h	Reserved: Always reads 0.
8	R	1b	CalRunCntl: (default is Run) 0 → Disable calibration 1 → Run (when running, CAL_OUT_RESULTS is continually updated)
9	R	0b	CMTermCntl: Enable calibration with common-mode termination. 0 = Disable 1 = Enable
10	R	1b	EnRxTerm: Enable Rx termination. This value is passed directly to the HyperTransport PHY. 0 = RX_IMP and CM_TERM are in effect. 1 = RX_IMP and CM_TERM have no effect.
11	R	0	CalRxSelNCntl : 0 selects the Rx calibration results to report in CAL_OUT_RESULTS. 1 selects the Tx calibration results to report in CAL_OUT_RESULTS.

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4.3.4.2 GG-Link1 Impedance Control Registers

These registers are in addition to the Link1 Impedance Control(77h-74h) registers. These extra registers are needed because impedance calibrator circuit used in Tsi308 is different from Tsi301.

Register Offset: 2Ch (indirect through Sri Index located at offset D4h).

Bit	R/W Access	Initial Value	Field Name and Description
2:0	R	010b	AvgWeight(n): The averaging weight. The default value is 2. avg = avg*(1-2**-n)+sample*2**-n
7:3	R	00h	Reserved: Always reads 0.
8	R	1b	CalRunCntl: (default is Run) 0 → Disable calibration 1 → Run (when running, CAL_OUT_RESULTS is continually updated)
9	R	0b	CMTermCntl: Enable calibration with common-mode termination. 0 = Disable 1 = Enable
10	R	1b	EnRxTerm: Enable Rx termination. This value is passed directly to the HyperTransport PHY. 0 = RX_IMP and CM_TERM are in effect. 1 = RX_IMP and CM_TERM have no effect.
11	R	0	CalRxSelNCntl : 0 selects the Rx calibration results to report in CAL_OUT_RESULTS. 1 selects the Tx calibration results to report in CAL_OUT_RESULTS.

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4.3.4.3 GG-Link0 Impedance Calibration Registers

Register Offset: 30h (indirect through Sri Index located at offset D4h)

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h	Calibrator Version
8	R	0h	CalDone: Calibration Done. This bit is set by hardware when the calibration sequence is done (CalOutResults has a new value).
9	R	0h	CalAcqdTx: Transmit Calibration Acquired. diff[avg-sample]<=1 for Tx(check <= Venkat)
10	R	0h	CalLostTx: Transmit Calibration Lost. CalAcqdTx = 0
11	R	0h	CalAcqdRx: Receive Calibration Acquired. diff[avg-sample]<=1 for Rx
12	R	0h	CalLostRx: Receive Calibration Lost. CalAcqdRx =0

4.3.4.4 GG-Link0 Impedance CalOut Registers

Register Offset : 34h (indirect through Sri Index located at offset D4h)

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	0h	CalOutResults: CAL_OUT for i=CAL_*X_IMP[4:0] where *=T/R if CalRxSelNCntl = 1/0. When CalRunCtl = 1, the value is updated automatically every 1K*clk(check -> Venkat) period. Reset/initialized to 0000FFFFh.

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4.3.4.5 GG-Link1 Impedance Calibration Registers

Register Offset: 38h (indirect through Sri Index located at offset D4h).

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h	Calibrator Version
8	R	0h	CalDone: Calibration Done. This bit is set by hardware when the calibration sequence is done (CalOutResults has a new value).
9	R	0h	CalAcqdTx: Transmit Calibration Acquired. diff[avg-sample]<=1 for Tx(check <= Venkat)
10	R	0h	CalLostTx: Transmit Calibration Lost. CalAcqdTx = 0
11	R	0h	CalAcqdRx: Receive Calibration Acquired. diff[avg-sample]<=1 for Rx
12	R	0h	CalLostRx: Receive Calibration Lost. CalAcqdRx =0

4.3.4.6 GG-Link1 Impedance CalOut Registers

Register Offset : 3Ch (indirect through Sri Index located at offset D4h)

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	0h	CalOutResults: CAL_OUT for i=CAL_*X_IMP[4:0] where *=T/R if CalRxSelNCntl = 1/0. When CalRunCtl = 1, the value is updated automatically every 1K*clk(check -> Venkat) period. Reset/initialized to 0000FFFFh.

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4.3.5 Tsi308 Registers

This section describes the bit position, type, default value and description of each register in Tsi308.

Behavior of the register in Tsi301 mode and Tsi308 mode is described explicitly when there is a conflict.

4.3.5.1 VendorID Register

Register Offset : 01h-00h

Bit	R/W Access	Initial Value	Field Name and Description
15:0	R	14D9h	Vendor ID: This value is defined as 14D9h for IDT (formerly Tundra Semiconductor).

4.3.5.2 Device ID Register

Register Offset : 03h–02h

Bit	R/W Access	Initial Value	Field Name and Description
15:0	R	Derived from straps	Device ID **SP/DSP:** This Device ID value of 0010h represents the Tsi301. GSP/ GDP: This Device ID value of 9000h represents Tsi308.

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4.3.5.3 Command Register

Register Offset : 05h–04h

Bit	R/W Access	Initial Value	Field Name and Description
15:11	R	0	Reserved: always reads 0.
10	R	0	**SP/DSP**: Reserved (always reads 0). **GSP/ GDP**: Interrupt Disable: If clear allows Tsi308 to assert a legacy INTx pin(if implemented) or send an INTx assertion message. Not persistent through warm reset. Tsi308 doesn't support it. Treated as reserved and reads 0.
9	R	0	**FastB2Ben:** This has no meaning for HyperTransport. Always reads 0.
8	R/W	0	SerrEn: **SP/DSP**: This enables system error interrupt pins FATAL_ERR_N and NONFATAL_ERR_N to be driven. 0 = SERR_N output driver disabled (default). 1 = SERR_N output driver enabled. **GSP/ GDP**: If this bit is set, Tsi308 floods all its outgoing links with sync packets when it detects an error that causes a sync flood. It this bit is clear, Tsi308 does not generate sync packets except as part of initial link synchronization, although it can still propagate them from one link to other within a chain. Not persistent through warm reset.
7	R	0	WaitCycCtrl: This has no meaning for HyperTransport. Always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
6	R(SP/DSP) R/W(GSP/ GDP)	0	**SP/DSP**: ParErrRespEn: Controls the bridge's response to parity errors on its primary interface. There are no parity errors on HyperTransport. Always reads 0. S/W write to this bit position is ignored. **GSP/ GDP**: Data Error Response: Allows Tsi308 to forward Data Error indications in TgtDone responses to be forwarded from the primary bus to the secondary bus. Not persistent through warm reset.
5	R	0	VGAPalSnpEn: controls the bridge's response to VGA-compatible palette write accesses. If enabled, the bridge decodes VGA palette accesses (I/O 3C6, 3C8, and 3C9) as belonging on the secondary bus. The Tsi308 does not support VGA palette snooping. Always reads 0.
4	R	0	MemWrInvEn: controls the ability of the bridge to generate Memory Write and Invalidate transactions as a master on the PCI bus; as controlled by the CacheLineSize register. This bit always reads 0.
3	R	0	SpecCycEn: controls the bridge's ability to respond to special cycle operations. Bridges do not respond to special cycle operations. This bit is hardwired to 0.

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Bit	R/W Access	Initial Value	Field Name and Description
2	R/W	0	MasterEn: controls the bridge's ability to operate as a master on the primary interface when forwarding memory or I/O transactions from the secondary inter face on behalf of a master on the secondary bus. If clear, the bridge will not respond to memory or I/O transactions on its secondary bus. 0 = Tsi308 not enabled to drive memory and I/O requests on HyperTransport. 1 = Tsi308 enabled to drive memory and I/O requests on HyperTransport. Not persistent through warm reset.
1	R/W	0	MemSpaceEn: Controls the bridge's response as a target to memory space accesses on the primary interface. If clear, the bridge will not accept any requests within the memory space range given below. **SP/DSP**: 00_0000_0000 - FC_FFFF_FFFF **GSP/ GDP**: 0000_0000_0000_0000 – 0000_00FC_FFFF_FFFF 0 = Disable memory space. 1 = Respond to memory space accesses. Not persistent through warm reset.
0	R/W	0	IoSpaceEn: controls the bridge's response as a target to I/O space transactions on the primary interface. If clear, the bridge does not accept any requests within the I/O space range given below. **SP/DSP**: FD_FC00_0000 – FD_FDFF_FFFF **GSP/ GDP**: 0000_00FD_FC00_0000 – 0000_00FD_FDFF_FFFF 0 = Disable I/O space. 1 = Respond to I/O space accesses. Not persistent through warm reset.

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4.3.5.4 Status Register

Register Offset : 07h–06h

Bit	R/W Access	Initial Value	Field Name and Description
15	R(SP/DSP) R/C(GSP/GDP)	0	**SP/DSP**: Data Parity Error Detected: This bit reports the detection of an address or data parity error by the bridge on its primary interface. HyperTransport does not have parity errors. Always reads 0. S/W write to this bit position is ignored **GSP/ GDP**: Data Error Detected: This bit is set by Tsi308 if it accepts a read response or posted request with a Data Error indicated from primary interface(HT). This bit is not set for TgtDone responses or forwarded packets with Data Error indicated. Persistent through warm reset.
14	R/C	0	**SERR Signaled:** This bit reports the assertion of a system error by a bridge on its primary interface; it may be cleared by writing a 1 to it. Persistent through warm reset. 0 = No error signaled. 1 = Tsi308 has asserted FATAL_ERR_N or NONFATAL_ERR_N or initiated sync flooding on the HyperTransport chain.
13	R/C	0	Received Master Abort: This bit reports the detection of a master abort termination by the bridge, when it is the master of a transaction on its primary interface. This is indicated on HyperTransport by an NXA error response. It may be cleared by writing a 1 to it. Persistent through warm reset. 0 = Tsi308 has not received an NXA error response on HyperTransport. 1 = Tsi308 has received an NXA error response on HyperTransport.
12	R/C	0	Received Target Abort: This bit reports the detection of a target abort by the bridge when it is the master of a transaction on its primary interface. This is indicated on HyperTransport by an error response without NXA. It may be cleared by writing a 1 to it. Persistent through warm reset. 0 = No error received. 1 = Tsi308 has received an HyperTransport error response.

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Bit	R/W Access	Initial Value	Field Name and Description
11	R/C	0	Signaled Target Abort: This bit reports the signaling of a target abort termination by the bridge, when it responds as the target of a transaction on its primary interface. This is indicated on HyperTransport by a response with the error bit set. It may be cleared by writing a 1 to it. Persistent through warm reset.
10:9	R	00b	DEVSEL_N Timing: Encodes the timing of the primary interface's DEVSEL. This is not meaningful for HyperTransport. Always reads 00. DEVSEL_N Timing always reads 00.
8	R(SP/DSP) R/C(GSP/GDP)	0	**SP/DSP:** PCI Parity Error Detected: This bit is used to report the detection of a parity error by the bridge when it is the master of the transaction. HyperTransport doesn't have parity errors. **GSP/ GDP**: Master Data Error: This bit is set by Tsi308 if Data Error Response bit of Command register is set and if Tsi308 issues a posted request on primary interface with Data Error bit set or accepts a response from primary interface with a Data Error indicated. This bit is not set if only forwarding packets with the Data Error bit set. Persistent through warm reset.
7	R	0	Fast BacktoBack Capability: This is not meaningful for HyperTransport. Always reads 0.
6	R	0	Reserved: (always reads 0).
5	R	0	66 MHz Capable PCI Bus: Indicates whether the primary interface is 66 MHz capable. Not meaningful for HyperTransport. Always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
4	R	1b	Capabilities List: This bit indicates that the configuration space of this device contains a capabilities list. Always reads 1.
3	R	0	SP/DSP: Reserved: (always reads 0). GSP/ GDP: Interrupt Status: This bit reflects the state of legacy INTx logic in the device, regardless of the state of the Interrupt Disable bit in the Command register. A 1 indicates that the interrupt source is active. A 0 indicates that the interrupt is inactive. Tsi308 doesn't support it. Treated as reserved and reads 0.
2:0	R	0h	Reserved: (always reads 0).

4.3.5.5 Revision ID Register

Register Offset : 08h

Bit	R/W Access	Initial Value	Field Name and Description
7:4	R	2	Revision ID:
3:0	R	0	Shipping code:

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4.3.5.6 Class Code Register

Register Offset: 0B–09h

Bit	R/W Access	Initial Value	Field Name and Description
23:16	R	06h	Base class of the device: 06h indicates a bridge.
15:8	R	04h	Subclass of the device: 04h indicates a PCI bridge.
7:0	R	00h	Programming Interface of the device: 00 indicates a positive decode device.

4.3.5.7 CacheLineSize Register

Register Offset : 0Ch

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	00h	Cache Line Size (in bytes): Must be a power of 2. This value is used to control generation of MemRdLine, MemRdMult, and MemWrInv commands by the PCI master when forwarding memory accesses from HT. If this value is left 0, the Tsi301 only generates MemRd and MemWr commands. For non-zero values, reads greater than 1 DW to prefetchable space generate MemRdMults if they cross a cacheline boundary. Otherwise, MemRdLines are generated. If enabled by the MemWrInvEn bit of the command register, writes that write an entire cacheline(all byte enables are asserted) generate MemWrInv commands. Tsi308 doesn't support any value other than 00h.

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4.3.5.8 Primary Latency Timer Register

Register Offset : 0Dh

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h	Primary Latency Timer: This is not used by the Tsi308. Always reads 0.

4.3.5.9 Header Type Register

Register Offset : 0Eh

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	01h or 81h based on strap value	Type: A value of 01h indicates that this is a bridge header. A value of 81h indicates this is a multi-functional header in RevC mode.

4.3.5.10 BIST Register

Register Offset : 0Fh

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h	BIST: Always reads 0.

4.3.5.11 Base Address Register 0

Register Offset : 13h–10h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	00000000h	Not used in the Tsi308. Always reads 0.

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4.3.5.12 Base Address Register 1

Register Offset : 17h–14h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	00000000h	Not used in the Tsi308. Always reads 0.

4.3.5.13 Primary Bus Number Register

Register Offset : 18h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	00h	Primary Bus Number: PCI bus number of the HyperTransport chain on which the Tsi308 is located. Not persistent through warm reset.

4.3.5.14 Secondary Bus Number Register

Register Offset : 19h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	00h	Secondary Bus Number: PCI bus number of the bus, which the Tsi308 sources. Not persistent through warm reset.

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4.3.5.15 Subordinate Bus Number Register

Register Offset : 1Ah

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	00h	Subordinate Bus Number: PCI bus number of the highest numbered bus behind the Tsi308. Not persistent through warm reset.

4.3.5.16 Secondary Latency Timer Register

Register Offset : 1Bh

Bit	R/W Access	Initial Value	Field Name and Description
7:3	R/W	00010	Timer: Controls how long the Tsi308 may continue to occupy the PCI-X Bus once the arbiter has taken the grant away in PCI clocks. Not persistent through warm reset.
2:0	R	000	Lower bits of Timer: Hardwired to zero to indicate eight clock granularity

4.3.5.17 I/O Base Address Register

Register Offset : 1Ch

Bit	R/W Access	Initial Value	Field Name and Description
7:4	R/W	0h	Address: bits 15:12 of the base of the I/O range. 11:0 are assumed to be 0, leading to a 4KB granularity. Not persistent through warm reset.
3:0	R	1h	Addressing Capability: Indicates the size of I/O addresses supported by the device, indicates 32 bits.

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4.3.5.18 I/O Limit Address Register

Register Offset : 1Dh

Bit	R/W Access	Initial Value	Field Name and Description
7:4	R/W	0h	Address: Bits 15:12 of the top of the I/O range. 11:0 are assumed to be 1, leading to a 4KB granularity. Not persistent through warm reset.
3:0	R	1h	Capability: Indicates the size of I/O addresses supported by the device is 32 bits.

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4.3.5.19 Secondary Bus Status Register

Register Offset : 1Fh–1Eh

Bit	R/W Access	Initial Value	Field Name and Description
15	R/C	0	Parity Error Detected: This bit reports the detection of an address or data parity error by the bridge on its secondary interface. Tsi308 sets this bit when any of the following three conditions is true: Detects an address parity error as a potential target. Detects a data parity error when the target of a write transaction. Detects a data parity error when the master of a read transaction. This bit is set regardless of the state of the *Parity Error Response Enable* bit in the Bridge Control Register. It may be cleared by writing a 1 to it. Persistent through warm reset.
14	R/C	0	Detect System Error: This bit reports the detection of a system error by a bridge on its secondary interface. It may be cleared by writing a 1 to it. Persistent through warm reset. 0 = No error detected. 1 = P_SERR_N assertion detected on the Tsi308 PCI bus.
13	R/C	0	Received Master Abort: This bit reports the detection of a master abort termination by the bridge, when it is the master of a transaction on its secondary inter face. It may be cleared by writing a 1 to it. Persistent through warm reset. 0 = No master abort detected. 1 = Tsi308 has detected a master abort.
12	R/C	0	Received Target Abort: This bit reports the detection of a target abort by the bridge when it is the master of a transaction on its secondary interface. It may be cleared by writing a 1 to it. Persistent through warm reset. 0 = No target abort received. 1 = Transaction aborted by target.
11	R/C	0	Signaled Target Abort: This bit reports the signaling of a target abort termination by the bridge, when it responds as the target of a transaction on its secondary interface. It may be cleared by writing a 1 to it. Persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
10:9	R	01	DEVSEL_N Timing: Encodes the timing of the secondary interface's DEVSEL. The Tsi308 PCI interface supports medium DEVSEL decoding. 00 = Fast 01 = Medium (the Tsi308 implements only this timing) 10 = Slow 11 = Reserved
8	R/C	0	Master Data Error: This bit is used to report the detection of a parity error by the bridge when it is the master of the transaction. Tsi308 sets this bit if the following three conditions are all true: Tsi308 is the bus master of the transaction on the secondary interface. Tsi308 asserted PERR# (read transaction) or detected PERR# asserted (write transaction). The *Parity Error Responses* bit in the Bridge Control Register is set. It is cleared by writing a 1 to the bit. Not persistent through warm reset. 0 = No parity error detected. 1 = Parity error detected.
7	R	1b	Fast Back2Back Capability: The Tsi308 supports fast backtoback transactions on the PCI interface. Always reads 1.
6	R	0	Reserved: (always reads 0).
5	R	1b	66 MHz Capable PCI Bus: Indicates whether the secondary interface is 66 MHz capable. The Tsi308 is 66 MHz capable.
4:0	R	00h	Reserved (always reads 0).

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4.3.5.20 Memory Range Base Address Register

Register Offset : 21h–20h

Bit	R/W Access	Initial Value	Field Name and Description
15:4	R/W	000h	Address: Bits 31:20 of the base of the memory range. Not persistent through warm reset.
3:0	R	0h	These bits are read only and return zeros when read. Only 32-bit addressing is supported.

4.3.5.21 Memory Range Limit Address Register

Register Offset 23h–22h

Bit	R/W Access	Initial Value	Field Name and Description
15:4	R/W	000h	Address: Bits 31:20 of the top (inclusive) of the memory range. Not persistent through warm reset.
3:0	R	0h	These bits are read only and return zeros when read. Only 32-bit addressing is supported.

4.3.5.22 Prefetchable Memory Range Base Address Register

Register Offset : 25h—24h

Bit	R/W Access	Initial Value	Field Name and Description
15:4	R/W	000h	Address: Bits 31:20 of the base of the prefetchable memory range. Not persistent through warm reset.
3:0	R	1h	Indicates whether the bridge supports 32- or 64-bit addressing for prefetchable memory space. 0 = 32-bit addressing 1 = 64-bit addressing

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4.3.5.23 Prefetchable Memory Range Limit Address

Register Offset : 27h–26h

Bit	R/W Access	Initial Value	Field Name and Description
15:4	R/W	000h	Address: Bits 31:20 of the top (inclusive) of the prefetchable memory range. Not persistent through warm reset.
3:0	R	1h	Indicates whether the bridge supports 32- or 64-bit addressing for prefetch able memory space. 0 = 32-bit addressing 1 = 64-bit addressing

4.3.5.24 Prefetch Memory Range Base Upper 32-Bit Address

Register Offset : 2Bh–28h

Bit	R/W Access	Initial Value	Field Name and Description
31:8	R(SP/DSP) /R/W(GSP/ GDP)	0h	As Tsi301 does not support Addresses above 1012GB, these bits are reserved and reads ‘zero’. These bits are used in Tsi308 mode as address extension (63:40) is supported.
7:0	R/W	0h	Address: Bits 39:32 of the prefetchable memory range base. Not persistent through warm reset.

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4.3.5.25 Prefetch Memory Range Limit Upper 32-Bit Address

Register Offset : 2Fh–2Ch

Bit	R/W Access	Initial Value	Field Name and Description
31:8	R(SP/DSP) /R/W(GSP/ GDP)	0h	As Tsi301 does not support Addresses above 1012GB, these bits are reserved and reads ‘zero’. These bits are used in Tsi308 mode as address extension (63:40) is supported.
7:0	R/W	0h	Address: Bits 39:32 of the prefetchable memory range limit. Not persistent through warm reset.

4.3.5.26 I/O Range Base Upper 16 Bits Register

Register Offset : 31h–30h

Bit	R/W Access	Initial Value	Field Name and Description
15:9	R/W	00h	Address: SP/DSP: Reserved. Tsi301 mode doesn’t support decode of address bits above 24. GSP/GDP: Bits 31:25 of the I/O range base. Not persistent through warm reset.
8:0	R/W	000h	Address: Bits 24:16 of the I/O range base. Not persistent through warm reset.

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4.3.5.27 I/O Range Limit Upper 16 Bits Register

Register Offset : 33h–32h

Bit	R/W Access	Initial Value	Field Name and Description
15:9	R/W	00h	Address: SP/DSP: Reserved. Tsi301 mode doesn't support decode of address bits above 24. GSP/GDP: Bits 31:25 of the I/O range limit. Not persistent through warm reset.
8:0	R/W	000h	Address: Bits 24:16 of the I/O range limit. Not persistent through warm reset.

4.3.5.28 Capability 1 Register

Register Offset : 34h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	40h	Pointer: Register number of the base of the first capabilities block.

4.3.5.29 Reserved Register

Register Offset : 37-35h

4.3.5.30 Expansion ROM Register

Register Offset : 3Bh–38h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	00000000h	Reserved.

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4.3.5.31 Interrupt Line Register

Register Offset : 3Ch

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	FFh	Register: The HyperTransport spec requires that this be a read/write register. Its value is not used internally. Not persistent through warm reset.

4.3.5.32 Interrupt Pin Register

Register Offset : 3Dh

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h	Reserved.

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4.3.5.33 Bridge Control Register

Register Offset : 3Fh–3Eh

Bit	R/W Access	Initial Value	Field Name and Description
15:12	R	0h	Reserved.
11	R/W	0	DiscardSerrEn: Discard Timer SERR# Enable **SP/DSP**: If set, treat a discard timer error as a system error. It can cause the assertion of either the FATAL_ERR_N or NONFATAL_ERR_N interrupts, depending on the state of the DiscardSerrFatal bit of the Error Control register. Not persistent through warm reset. **GSP/ GDP**: If set treats the discard timer error as a system error. It set and the SERR# Enable in the Command register is set Tsi308 floods both the HT links with sync packets. Not persistent through warm reset.
10	R/C	0	DiscardStat: this bit is set by hardware when a request is dropped due to an expired discard counter. It may be cleared by writing a 1 to it. Persistent through warm reset.
9	R/W	0	SecDiscardTimer: Sets the length of the timer on delayed requests. Once the initial subrequests of an inbound delayed transaction have completed on HyperTransport, the timer begins to run. If it expires before the PCI requester reissues the request, the transaction is dropped from the delayed request buffers. Not persistent through warm reset. 0 = count 2^{15} PCI clocks 1 = count 2^{10} PCI clocks
8	R	0	PrimDiscardTimer: Not meaningful for HyperTransport. Always reads 0.
7	R	0	FastB2Ben: Enables the generation of fast back-to-back transactions when the Tsi308 is the master on the PCI bus. Not persistent through warm reset. This bit is reserved.

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Bit	R/W Access	Initial Value	Field Name and Description
6	R/W	0	SecBusReset: If written to a 1, hardware will perform a reset sequence on the secondary bus. Clearing the bit will bring the secondary bus out of reset. Not persistent through warm reset.
5	R/W	0	MstrAbortMode: This bit controls the action taken by the bridge when a transaction that it is forwarding in either direction takes a master abort on the destination bus. The master abort is indicated on HyperTransport by an error response with NXA set If this bit is clear, writes are allowed to complete normally on the source bus, and reads have all 1's returned. **SP/DSP**: If it is set, the master abort will be treated as an error, returning error, returning a Target Abort Response (indicated on HyperTransport by a set error bit without NXA) for nonposted requests and causing a sideband error assertion (indicated by asserting the FATAL_ERR_N or NONFATAL_ERR_N interrupt pins, as enabled) for posted requests. **GSP/ GDP**: If it is set, the master abort will be treated as an error, returning error, returning a Target Abort Response (indicated on HyperTransport by a set error bit without NXA) for nonposted requests. For posted requests Tsi308 floods both the HT links with sync packets if SERR# Enable bit in the Command register is set. Not persistent through warm reset.
4	R	0	Reserved.
3	R/W	0	VgaEn: This bit modifies the response by the bridge to VGA compatible addresses, which are defined as memory addresses in the range 0_000A_0000h – 0_000B_FFFFh, and I/O space addresses in the bottom 64KB of PCI I/O space, where the bottom 10 bits are in the range 3B0h – 3BBh or 3C0h - 3DFh. Address bits 15:10 of I/O addresses are not decoded, allowing for ISA aliasing of the above address ranges. If set, the bridge will forward these addresses from the primary to the secondary bus and block forwarding them from the secondary to the primary bus; regardless of the contents of the memory and I/O range registers, the ISA Enable bit (in this register), or the VGA Palette Snoop Enable bit (in the Command register). Not persistent through warm reset. If this bit is set when the address mapping extensions are in use, the address decode behavior or the device may be undefined

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Bit	R/W Access	Initial Value	Field Name and Description
2	R/W	0	IsaEn - ISA Enable: This bit modifies the bridge response to ISA I/O addresses and only applies if: Addresses are enabled by the I/O Base registers, and are enabled by the I/O Limit registers, and are in the first 64 Kbytes of PCI I/O address space. If set, the bridge blocks any forwarding of the last 768 bytes in each 1 Kbyte block from primary to secondary I/O transaction addressing. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1 Kbyte block. 0 = Forward all I/O addresses in the range defined by the I/O Base and I/O Limit registers. 1 = Block forwarding ISA I/O addresses in the range defined by the I/O Base and I/O Limit registers that are in the first 64 Kbytes of PCI I/O address space. After reset, the default state of this bit must be 0. Not persistent through warm reset. If this bit is set when the address mapping extensions are in use, the address decode behavior or the device may be undefined
1	R/W	0	SerrEn: **SP/DSP**: This bit controls forwarding of system errors from the secondary interface to the primary interface. If it is set, SERR# on the secondary bus will cause a system error (indicated by the assertion of the FATAL_ERR_N or NONFATAL_ERR_N error interrupt pins), assuming that the SERR enable bit is set for the primary interface in the command register. Not persistent through warm reset. **GSP/ GDP**: Controls the mapping of system errors from the secondary bus(PCI/PCI-X) to primary bus(HT). It set and the SERR# Enable in the Command register is set then upon seeing SERR# assertion on PCI/PCI-X interface Tsi308 floods both the HT links with sync packets. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
0	R/W	0	**SP/DSP**: Parity Error Response Enable: Enables parity errors to be reported by P_PERR_N, FATAL_ERR_N or NONFATAL_ERR_N error interrupt. Not persistent through warm reset. **GSP/ GDP**: Data Error Response Enable: This bit must be set to allow Tsi308 to set the Master Data Error bit of the Secondary Status register. In addition setting this bit enables Tsi308 to forward address and data parity errors from secondary interface onto the primary interface as follows: **Address Parity Error**: When Tsi308 detects an address parity error on its secondary interface it takes the following actions: Floods its both outgoing links with sync packets if SERR# Enable bit in the Command register is set. Sets Parity Error Detected bit in its secondary status register. Sets SERR Signaled bit of the status register. If Tsi308 has claimed the cycle and terminated it by signaling a Target-Abort then Signaled Target Abort bit in its secondary status register is also set. **Data Parity Error**: If Tsi308 detects data parity error when it is the master of a transaction on its secondary interface it sets *Master Data Error* bit in the Secondary Status register. If Tsi308 detects data parity error when it is the target of a transaction on its secondary interface it sets *Parity Error Detected* bit in the Secondary Status register. In both cases Tsi308 forwards the data parity error onto primary interface by setting Data Error bit in the request or response packets.

4.3.5.34 HyperTransport Capability ID Register

Register Offset : 40h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	08h	Id: HyperTransport Capability ID assigned by the PCI SIG.

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4.3.5.35 Capability 2 Register

Register Offset : 41h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	78h/00h	SP/DSP: It is 00h as there are no additional capabilities **GSP/ GDP:** Pointer: pointer to the next capability block for Interrupt Discovery Capability location 78h

4.3.5.36 HyperTransport Command Register

Register Offset : 43h–42h

Bit	R/W Access	Initial Value	Field Name and Description
15:13	R	000b	Capability Type: Indicates what type of HyperTransport capability block this is. For a primary block, it is always 000b.
12	R(SP/DSP) R/W(GSP/ GDP)	0	SP/DSP: Reserved. **GSP/ GDP:** Drop on Uninitialized Link: This bit controls the packet forwarding behavior of Tsi308 when both *End of Chain* and *Initialization Complete* bits of Link Control register of receiving link are clear. When *Drop on Uninitialized Link* bit is set, Tsi308 behaves as if *End of Chain* bit is set if it receives packets when *Initialization Complete* bit is clear. When clear, Tsi308 stalls the forwarding until one or both of the bits above are set and take the appropriate action.
11	R/W	0	Default Direction: This determines which link requests initiated by this device will be placed on. Not persistent through warm reset. 0 = Send requests toward the Master Host Bridge (as determined by the Master Host field). 1 = Send requests in the opposite direction.

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Bit	R/W Access	Initial Value	Field Name and Description
10	R	0	Master Host: contains the number of the link pointing to the master host bridge on the HyperTransport chain. Updated with the link number that the register was written from whenever the HyperTransport Command register is written. In **DSP** and **GDP** mode, this bit is 1'b0 in the CSR of nearer link and is 1'b1 in the CSR of farther link.. This bit is updated with the link number in **SP** and **GSP** mode.
9:5	R	01h	Unit Count: The number of UnitIDs consumed. This number is always 1.
4:0	R/W	00h	Base Unit ID: This is the base of the range of HyperTransport UnitIDs occupied by this device. Not persistent through warm reset.

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4.3.5.37 HyperTransport Link 0 Control Register

Register Offset : 45h–44h

Bit	R/W Access	Initial Value	Field Name and Description
15	R(SP/DSP) R/W(GSP/GDP)	0h	SP/DSP: Reserved GSP/GDP: 64 Bit Addressing Enable If set Tsi308 accepts requests from HT that access addresses above FF_FFFF_FFFFh when issued with Address Extension command. If this bit is clear, then any request from HT that access above FF_FFFF_FFFFh will be master aborted by Tsi308 as if end of chain was reached. Similarly when this bit is clear, any request from PCI/PCI-X that access above FF_FFFF_FFFFh will be master aborted on PCI/PCI-X. If this bit is set then for requests from PCI/PCI-X that access above FF-FFFF-FFFFh, Tsi308 uses Address Extension command to forward them onto HT. Not persistent through warm reset.
14	R/C(SP/DSP) R/W (GSP/GDP)	0	**SP/DSP:** **NXA Error:** This bit is set whenever a response or posted write is dropped due to hitting end of chain. It can be cleared by writing a 1 to it. Persistent through warm reset. GSP/ GDP: Extended CTL Time: If this bit is set during the link initialization following LDTSTOP# disconnect sequence, CTL will be asserted for 50us
13	R/C(SP/DSP) R/W (GSP/GDP)	0	SP/DSP: Overflow Error: This bit is set whenever an overflow error is detected. It may be cleared by writing a 1 to it. Persistent through warm reset. GSP/ GDP: **LDTSTOP# Tristate Enable:** This bit controls whether the transmitter tristates the link during LDTSTOP# sequence. When this bit is set, transmitter tristates the link. When this bit is clear, transmitter continues to drive the link.

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Bit	R/W Access	Initial Value	Field Name and Description
12	R/C(SP/DSP) R(GSP/GDP)	0	SP/DSP: **Protocol Error:** This bit is set whenever a protocol error is detected. It may be cleared by writing a 1 to it. Persistent through warm reset. GSP/ GDP: Isochronous Flow Control Enable: Reserved and always reads 0.
11:8	R/C	0h	CRC Err: Each bit is set whenever a CRC error is detected on the corresponding byte lane of the link. Each bit may be cleared by writing a 1 to it.
7	R/S	0	Xmit Off: This bit shuts off the link transmitter to reduce EMI and power. The EOC bit should always be set prior to setting the XmitOff bit. It may only be set by software, not cleared. It may only be cleared by a warm or cold reset sequence on HyperTransport.
6	R/S	0	End Of Chain: This bit indicates that this link is not part of the logical Hyper Transport chain and that this device should be considered the end of the chain for packets coming from the other direction. Packets directed toward this link are dropped. Nonposted requests result in nonexistent address (NXA) error responses. It may only be set, not cleared, by software. Not persistent through warm reset.
5	R	0	Init Done: This read-only bit indicates that low-level link initialization has successfully completed on the link.
4	R/W	0	Link Fail: This bit is set to indicate that a failure has been detected on a link and it should not be used. It is persistent through warm reset and will prevent link initialization when set. It may be set either by hardware or software and cleared by software. Software written values do not take effect until the next warm reset.
3	R/W	0	CRC Force Error: When this bit is a 1, bad CRC will be generated on all outgoing traffic on the link. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
2	R/S	0	CRC Start Test: Writing a 1 to this bit causes hardware to initiate a CRC test sequence on the link. When the test sequence has completed, hardware will clear the bit. Not persistent through warm reset.
1	R/W	0	CRC Sync Flood Enable: if set, this bit causes CRC errors to be treated as fatal errors. When detected, they will cause all HyperTransport links from this device to be flooded with sync packets and the LinkFail bit to be set. Not persistent through warm reset.
0	R	0	Reserved.

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4.3.5.38 Link 0 Width Control(SP)/Link 0 Configuration Register(Tsi308)

Register Offset : 47h–46h

Bit	R/W Access	Initial Value	Field Name and Description
15	R	0h	SP/DSP: Reserved GSP/ GDP: **Doubleword Flow Control Out Enable(DwFcOutEn):** Tsi308 doesn't support it and always reads 0.
14:12	R(SP/DSP) R/W(GSP/ GDP)	000b	Link Width Out: This controls the used width of the outgoing link from this device. It must match the used incoming width of the device on the other end of the link: 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits **SP/DSP**: Only supports 8-bits **GSP/ GDP**: Supports 2, 4, or 8 bits. Tsi308 hardware initializes this register based on the result of link-width negotiation sequence. Software can write a different value to this register but chain must pass through warm reset sequence for the new width values to be reflected on the link. Persistent through warm reset.
11	R	0h	**SP/DSP:** Reserved. GSP/ GDP: **Doubleword Flow Control In Enable(DwFcInEn):** Tsi308 doesn't support it and always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
10:8	R(SP/DSP) R/W (GSP/ GDP)	000b	Link Width In: This controls the utilized width (may not exceed the physical width) of the incoming side of the link. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits **SP/DSP**: Supports only 8-bit wide link **GSP/ GDP**: Supports 2,4 or 8-bits Initialized by Tsi308 hardware after cold reset based on the results of the link-width negotiation sequence. Software can then write a different value into this register. The chain must pass through warm reset sequence for the new width values to be reflected on the link.
7	R	0	SP/DSP: **Reserved**. GSP/ GDP: **Doubleword Flow Control Out (DwFcOut):** Tsi308 doesn't support it and always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
6:4	R	000b	Max Link Width Out: Indicates the maximum width of the outgoing link supported by this device: Supports the maximum width of 8-bits. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits
3	R	0	**SP/DSP**: Reserved. GSP/ GDP: **Doubleword Flow Control In (DwFcIn):** Tsi308 doesn't support it and always reads 0.
2:0	R	000b	Max Link Width In: Indicates the maximum width of the incoming link supported by this device: Supports the maximum width of 8-bits. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits

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4.3.5.39 HyperTransport Link 1 Control Register

Tsi308 uses *HyperTransport Link 0 Control* of CSR0 for Link0 and *HyperTransport Link 0 Control* of CSR1 for Link1in **GDP** and **DSP** modes.

HyperTransport Link 1 Control of CSR0 is used for Link1 in **SP** and **GSP** modes.

CSR1 is not visible in these modes.

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Register Offset : 49h–48h

Bit	R/W Access	Initial Value	Field Name and Description
15	R(SP/DSP) R/W(GSP/GDP)	0h	**SP/DSP**: Reserved GSP/GDP: **64 Bit Addressing Enable:** If set Tsi308 accepts requests from HT that access addresses above FF_FFFF_FFFFh when issued with Address Extension command. If this bit is clear, then any request from HT that access above FF_FFFF_FFFFh will be master aborted by Tsi308 as if end of chain was reached. Similarly when this bit is clear, any request from PCI/PCI-X that access above FF_FFFF_FFFFh will be master aborted on PCI/PCI-X. If this bit is set then for requests from PCI/PCI-X that access above FF-FFFF-FFFFh, Tsi308 uses Address Extension command to forward them onto HT. Not persistent through warm reset.
14	R/C(SP) R(DSP) R/W (GSP/GDP)	0	SP: NXA Error: This bit is set whenever a response or posted write is dropped due to hitting end of chain. It can be cleared by writing a 1 to it. Persistent through warm reset. **DSP**: Not used. Reads 0. GSP/ GDP: **Extended CTL Time:** If this bit is set during the link initialization following LDTSTOP# disconnect sequence, CTL will be asserted for 50us
13	R/C(SP) R(DSP) R/W (GSP/GDP)	0	SP: Overflow Error: This bit is set whenever an overflow error is detected. It may be cleared by writing a 1 to it. Persistent through warm reset. **DSP:** Not used. Reads 0. **GSP/ GDP**: LDTSTOP# Tristate Enable This bit controls whether the transmitter tristates the link during LDTSTOP# sequence. When this bit is set, transmitter tristates the link. When this bit is clear, transmitter continues to drive the link.

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Bit	R/W Access	Initial Value	Field Name and Description
12	R/C(SP) R(DSP) R(GSP/ GDP)	0	SP: Protocol Error: This bit is set whenever a protocol error is detected. It may be cleared by writing a 1 to it. Persistent through warm reset. **DSP/GDP**: Not used. Reads 0. GSP: **Isochronous Flow Control Enable:** Reserved and always reads 0.
11:8	R/C(SP/GSP) R(DSP/ GDP)	0h	SP/GSP: CRC Err: Each bit is set whenever a CRC error is detected on the corresponding byte lane of the link. Each bit may be cleared by writing a 1 to it. **DSP/ GDP**: Not used. Reads 0.
7	R/S(SP) R(GSP) R(DSP/ GDP)	0	SP/GSP: **Xmit Off:** This bit shuts off the link transmitter to reduce EMI and power. The EOC bit should always be set prior to setting the XmitOff bit. It may only be set by software, not cleared. It may only be cleared by a warm or cold reset sequence on HyperTransport. **DSP/ GDP**: Not used. Reads 0.
6	R/S(SP) R(GSP) R(DSP/ GDP)	0	SP/GSP: End Of Chain: this bit indicates that this link is not part of the logical Hyper Transport chain and that this device should be considered the end of the chain for packets coming from the other direction. Packets directed toward this link are dropped. Nonposted requests result in nonexistent address (NXA) error responses. It may only be set, not cleared, by software. Not persistent through warm reset. **DSP/ GDP**: Not used. Reads 0.
5	R	0(SP/GSP) 1(DSP/ GDP)	SP/GSP: **Init Done:** This read-only bit indicates that low-level link initialization has successfully completed on the link. **DSP/ GDP:** Not used. Hardwired to 1.

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Bit	R/W Access	Initial Value	Field Name and Description
4	R/W	0	SP/GSP: **Link Fail:** This bit is set to indicate that a failure has been detected on a link and it should not be used. It is persistent through warm reset and will prevent link initialization when set. It may be set either by hardware or software and cleared by software. Software written values do not take effect until the next warm reset. **DSP/ GDP**: Not used.
3	R/W	0	SP/GSP: CRC Force Error: When this bit is a 1, bad CRC will be generated on all outgoing traffic on the link. Not persistent through warm reset. **DSP/ GDP:** Not used.
2	R/S(SP) R(GSP) R(DSP/ GDP)	0	SP/GSP: **CRC Start Test:** Writing a 1 to this bit causes hardware to initiate a CRC test sequence on the link. When the test sequence has completed, hardware will clear the bit. Not persistent through warm reset. **DSP/ GDP:** Not used.
1	R/W	0	SP/GSP: **CRC Sync Flood Enable:** if set, this bit causes CRC errors to be treated as fatal errors. When detected, they will cause all HyperTransport links from this device to be flooded with sync packets and the LinkFail bit to be set. Not persistent through warm reset. **DSP/ GDP:** Not used.
0	R	0	Reserved.

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4.3.5.40 Link 1 Width Control(SP)/Link 1 Configuration Register(Tsi308)

Tsi308 uses *Link0 Width Control(SP)/Link0 Configuration Register(*Tsi308*)* of CSR0 for Link0 and *Link0 Width Control(SP)/Link0 Configuration Register(*Tsi308*)* of CSR1 for Link1in **GDP** and **DSP** modes.

*Link 1 Width Control(SP)/Link 1 Configuration Register(*Tsi308*)*of CSR0 is used for Link1 in **SP** and **GSP** modes.

CSR1 is not visible in these modes.

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Register Offset : 4Bh–4Ah

Bit	R/W Access	Initial Value	Field Name and Description
15	R	0h	SP/DSP/GDP: Reserved GSP: Doubleword Flow Control Out Enable(DwFcOutEn): Tsi308 doesn't support it and always reads 0.
14:12	R(SP/ DSP) R/W(GSP/ GDP)	000b	Link Width Out: This controls the used width of the outgoing link from this device. It must match the used incoming width of the device on the other end of the link: 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits **SP:** Only supports 8-bits **GSP:** Supports 2, 4, or 8 bits. Tsi308 hardware initializes this register based on the result of link-width negotiation sequence. Software can write a different value to this register but chain must pass through warm reset sequence for the new width values to be reflected on the link. Persistent through warm reset. **GDP/DSP :** Not used.
11	R	0h	**SP/ GDP/DSP:** Reserved. GSP: **Doubleword Flow Control In Enable(DwFcInEn):** Tsi308 doesn't support it and always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
10:8	R(SP/DSP) R/W (GSP/ GDP)	000b	Link Width In: This controls the utilized width (may not exceed the physical width) of the incoming side of the link. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits **SP**: Supports only 8-bit wide link **GSP**: Supports 2,4 or 8-bits Initialized by Tsi308 hardware after cold reset based on the results of the link-width negotiation sequence. Software can then write a different value into this register. The chain must pass through warm reset sequence for the new width values to be reflected on the link. **GDP/DSP** *:* Not used.
7	R	0	**SP/DSP/ GDP**: Reserved. GSP: **Doubleword Flow Control Out (DwFcOut):** Tsi308 doesn’t support it and always reads 0.

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Bit	R/W Access	Initial Value	Field Name and Description
6:4	R	000b	Max Link Width Out: Indicates the maximum width of the outgoing link supported by this device: Supports the maximum width of 8-bits. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits
3	R	0	**SP/DSP**: Reserved. GSP/ GDP: **Doubleword Flow Control In (DwFcIn):** Tsi308 doesn't support it and always reads 0.
2:0	R	000b	Max Link Width In: Indicates the maximum width of the incoming link supported by this device: Supports the maximum width of 8-bits. 100b = 2 bits 101b = 4 bits 000b = 8 bits 001b = 16 bits 011b = 32 bits

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4.3.5.41 HyperTransport Revision ID Register

Register Offset: 4Ch

Bit	R/W Access	Initial Value	Field Name and Description
7:5	R	0h(SP/DSP) 1h(GSP/GDP)	MajorRevision: This field contains the major revision of the HT I/O Link Protocol Specification to which this chip confirms to: **SP/DSP**: Reads 3'b000 **GSP/ GDP**: Reads 3'b001
4:0	R	10001b(SP/DSP) 5'b00101(GSP/GDP)	MinorRevision: This field contains the minor revision of HT I/O Link Protocol Specification to which this chip confirms to: **SP/DSP**: Reads 5'b10001 **GSP/ GDP**: Reads 5'b00101

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4.3.5.42 Link0 Frequency & Link0 Error Registers

Register Offset : 4Dh

Bit	R/W Access	Initial Value	Field Name and Description
7	R(SP/DSP) R/W(GSP/ GDP)	0	**SP/DSP:** Reserved GSP/ GDP: **CTL Timeout:** This bit indicates how long CTL may be low before Tsi308 indicates a protocol error. 0 -> 1 millisecond 1 -> 1 full second Not persistent through warm reset.
6	R(SP/DSP) R/C(GSP/ GDP)	0	**SP/DSP:** Reserved GSP/ GDP: **End Of Chain Error:** This bit is set when a link transmitter receives a posted or response packet to be sent out when the link is the end of chain. This applies to forward packets received by this link as well as packets received by this link's transmitter from PCI/PCI-X interfaces. A link's transmitter is said to be End Of Chain if either End of Chain bit is set in link control register or Initialization Complete bit is clear and Drop On Uninitialized Link bit in the command register is set. This bit is also set if a 64-bit request reaches the link with 64-bit support disabled. Receiving a Device Message with the Silent Drop bit set will not set this bit Persistent through warm reset..

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Bit	R/W Access	Initial Value	Field Name and Description
5	R(SP/DSP) R/C(GSP/ GDP)	0	**SP/DSP:** Reserved GSP/ GDP: Overflow Error: This bit indicates a receive buffer overflow has been detected on the link. Overflow errors may be mapped to sync flood, fatal or nonfatal error interrupts. Persistent through warm reset.
4	R(SP/DSP) R/C(GSP/ GDP)	0	**SP/DSP:** RGSP/ GDP: Protocol Error: This bit indicates a protocol error has been detected on the link. Protocol errors may be mapped to sync flood, fatal or nonfatal error interrupts. Persistent through warm reset.
3:0	R(SP/DSP) R/W(GSP/ GDP)	0	**SP/DSP:** Reserved GSP/ GDP: Link Frequency: Specifies the operating frequency of the link's transmitter clock. The data rate is twice this value. The encoding of this field is shown below: 0000 = 200 MHz(default) 0001 = 300 MHz 0010 = 400 MHz 0011 = 500 MHz 0100 = 600 MHz If the register comes up 0000 at cold reset, software can write it to either 0000 through 0100 and go through warm reset to switch between 200 and 600 MHz operation. All other encodings are reserved and can lead to undefined behavior. In synchronous mode, both the receiver and transmitter operate at programmed frequency. Persistent through warm reset.

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4.3.5.43 Link0 Frequency Capability Register

Register Offset : 4E-4Fh

Bit	R/W Access	Initial Value	Field Name and Description
15:0	R	0(SP/DSP) Values based on core clock frequency(GSP/ GDP)	**SP/DSP**: Reserved GSP/ GDP: **Link Frequency Capability Register(LinkFreqCap):** It is a 16-bit read only register that indicates the clock frequency capabilities of the link. Each bit in LinkFreqCap corresponds to one of the 16 possible encodings of Link Frequency register. Bit N of LinkFreqCap corresponds to encoding N of the LinkFreq field. A 1 in LinkFreqCap means that the link supports the corresponding link frequency, and a 0 means the link doesn't support that frequency. Following table shows the maximum HT link frequency that can be supported for a core clock frequency and its corresponding Link Frequency Capability Register value. Core clock Freq Max. HT Link Freq. LinkFreqCap 100 MHz 400 MHz 0x0007 133 MHz 500 MHz 0x000f 200 MHz 600 MHz 0x001f

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4.3.5.44 Feature Capability Register(Tsi308)/Reserved(SP/DSP) Register

Register Offset : 50h

Bit	R/W Access	Initial Value	Field Name and Description
7:6	R	0h	**Reserved**.
5	R	1b	UnidID Reorder Disable: When set, Tsi308 orders traffic in all UnitIDs together within each virtual channel to support passive UnitID Clumping. Tsi308 always orders traffic in all UnitIDs together regardless of this bit setting by software
4	R	1b	64 Bit Addressing: If set, indicates that Tsi308 supports 64 bit addresses by accepting and forwarding Address Extension command doublewords.
3	R	0b	Extended CTL Time Required: Indicates if Tsi308 requires CTL to be asserted for 50 us during the initialization sequence after an LDTSTOP# disconnect.
2	R	0b	CRC Test Mode: Indicates if Tsi308 supports CRC test mode. Tsi308 does support CRC Test Mode as per [1] but erroneously reports a 0
1	R	1b	LDTSTOP#: Indicates if Tsi308 supports LDTSTOP# protocol.
0	R	0b	Isochronous Flow Control Mode: This bit indicates if Tsi308 supports isochronous flow control. Tsi308 doesn't support it. Reads 0.

4.3.5.45 Link1 Frequency & Link1 Error Registers.

Tsi308 uses *Link0 Frequency & Link0 Error Registers* of CSR0 for Link0 and *Link0 Frequency & Link0 Error Register* of CSR1 for Link1in **GDP** mode.

Link1 Frequency & Link1 Error Registers of CSR0 is used for Link1 in **GSP** mode.

CSR1 is not visible in these modes.These registers are reserved in SP/DSP modes and reads 0.

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Register Offset : 51h

Bit	R/W Access	Initial Value	Field Name and Description
7	R/W(GSP/ GDP)	0	GSP: **CTL Timeout:** This bit indicates how long CTL may be low before Tsi308 indicates a protocol error. 0 -> 1 millisecond 1 -> 1 full second Not persistent through warm reset. GDP: Not used
6	R/C(GSP /GDP)	0	GSP: **End Of Chain Error:** This bit is set when a link transmitter receives a posted or response packet to be sent out when the link is the end of chain. This applies to forward packets received by this link as well as packets received by this link's transmitter from PCI/PCI-X interfaces. A link's transmitter is said to be End Of Chain if either End of Chain bit is set in link control register or Initialization Complete bit is clear and Drop On Uninitialized Link bit in the command register is set. This bit is also set if a 64-bit request reaches the link with 64-bit support disabled. Receiving a Device Message with the Silent Drop bit set will not set this bit Persistent through warm reset. GDP: Not used

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Bit	R/W Access	Initial Value	Field Name and Description
5	R/C(GSP/ GDP)	0	GSP: Overflow Error: This bit indicates a receive buffer overflow has been detected on the link. Overflow errors may be mapped to sync flood, fatal or nonfatal error interrupts. Persistent through warm reset. GDP: Not used
4	R/C(GSP/ GDP)	0	GSP: Protocol Error: This bit indicates a protocol error has been detected on the link. Protocol errors may be mapped to sync flood, fatal or nonfatal error interrupts. Persistent through warm reset. GDP: Not used
3:0	R/W(GSP/ GDP)	0	GSP: Link Frequency: Specifies the operating frequency of the link's transmitter clock. The data rate is twice this value. The encoding of this field is shown below: 0000 = 200 MHz(default) 0001 = 300 MHz 0010 = 400 MHz 0011 = 500 MHz 0100 = 600 MHz If the register comes up 0000 at cold reset, software can write it to either 0000 through 0100 and go through warm reset to switch between 200 and 600 MHz operation. All other encodings are reserved and can lead to undefined behavior. In synchronous mode, both the receiver and transmitter operate at programmed frequency. Persistent through warm reset. GDP: Not used

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4.3.5.46 Link1 Frequency Capability Register

Tsi308 uses *Link0 Frequency Capability Registers* of CSR0 for Link0 and *Link0 Frequency Capability Register*s of CSR1 for Link1in **GDP** mode.

Link1 Frequency Capability Registers of CSR0 is used for Link1 in **GSP** mode.

CSR1 is not visible in these modes.

These registers are reserved in SP/DSP modes and reads 0.

Register Offset : 52-53h

Bit	R/W Access	Initial Value	Field Name and Description
15:0	R	Values based on core clock frequency	GSP: **Link Frequency Capability Register(LinkFreqCap):** It is a 16-bit read only register that indicates the clock frequency capabilities of the link. Each bit in LinkFreqCap corresponds to one of the 16 possible encodings of Link Frequency register. Bit N of LinkFreqCap corresponds to encoding N of the LinkFreq field. A 1 in LinkFreqCap means that the link supports the corresponding link frequency, and a 0 means the link doesn't support that frequency. Following table shows the maximum HT link frequency that can be supported for a core clock frequency and its corresponding Link Frequency Capability Register value. Core clock Freq Max. HT Link Freq. LinkFreqCap 100 MHz 400 MHz 0x0007 133 MHz 500 MHz 0x000f 200 MHz 600 MHz 0x001f GDP: Not used

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4.3.5.47 Enumeration Scratchpad Register(GSP/GDP)/Reserved(SP/DSP) Register

Register Offset : 54-55h

Bit	R/W Access	Initial Value	Field Name and Description
15:0	R/W	0000h	Enumeration Scratchpad Register: Provides a scratchpad for enumeration software. Not used by Tsi308 hardware.

4.3.5.48 Error Handling Register (GSP/GDP)/Reserved(SP/DSP) Register

Register Offset : 56-57h

Bit	R/W Access	Initial Value	Field Name and Description
15	R/W	0h	System Error NonFatal Enable: Not applicable to Slave/Secondary devices. Hardwired to 0.
14	R/W	0h	CRC Error NonFatal Enable: When asserted, this bit will cause the fatal error interrupt(NONFATAL_ERR_N) to be asserted whenever any of the CRC Error bits are asserted in either of the Link Control registers. Not persistent through warm reset.
13	R/W	0h	Response Error NonFatal Enable: When asserted, this bit will cause the fatal error interrupt(NONFATAL_ERR_N) to be asserted whenever the Response Error(bit 9 of this register) bit is asserted. Not persistent through warm reset.
12	R/W	0h	End of Chain Error NonFatal Enable: When asserted, this bit will cause the nonfatal error interrupt(NONFATAL_ERR_N) to be asserted whenever the End of Chain Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.
11	R/W	0h	Overflow Error Nonfatal Enable: When asserted, this bit will cause the nonfatal error interrupt(NONFATAL_ERR_N) to be asserted whenever the Overflow Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
10	R/W	0h	Protocol Error Nonfatal Enable: When asserted, this bit will cause the nonfatal error interrupt(NONFATAL_ERR_N) to be asserted whenever the Protocol Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.
9	R/C	0h	Response Error: This bit indicates that the given interface has received a response error. Persistent through warm reset.
8	R	0h	Chain Fail: This bit indicates that the chain has gone down. It is set whenever Tsi308 detects sync flooding or a sync-flood generating error. Cleared by reset of the failed chain. Not persistent through warm reset.
7	R	0h	System Error Fatal Enable: Not applicable to Slave/Secondary devices. Hardwired to 0.
6	R/W	0h	CRC Error Fatal Enable: When asserted, this bit will cause the fatal error interrupt(FATAL_ERR_N) to be asserted whenever any of the CRC Error bits are asserted in either of the Link Control registers. Not persistent through warm reset.
5	R/W	0h	Response Error Fatal Enable: When asserted, this bit will cause the fatal error interrupt(FATAL_ERR_N) to be asserted whenever the Response Error(bit 9 of this register) bit is asserted. Not persistent through warm reset.
4	R/W	0h	End of Chain Error Fatal Enable: When asserted, this bit will cause the fatal error interrupt(FATAL_ERR_N) to be asserted whenever the End of Chain Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.
3	R/W	0h	Overflow Error Fatal Enable: When asserted, this bit will cause the fatal error interrupt(FATAL_ERR_N) to be asserted whenever the Overflow Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
2	R/W	0h	Protocol Error Fatal Enable: When asserted, this bit will cause the fatal error interrupt(FATAL_ERR_N) to be asserted whenever the Protocol Error bit is set in one of the Link Error registers. Not persistent through warm reset.
1	R/W	0h	Overflow Error Flood Enable: When asserted, this bit will cause the link to be flooded with Sync packets whenever the Overflow Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.
0	R/W	0h	Protocol Error Flood Enable: When asserted, this bit will cause the link to be flooded with Sync packets whenever the Protocol Error bit is asserted in one of the Link Error registers. Not persistent through warm reset.

4.3.5.49 Memory Base Upper & Memory Limit Upper(GSP/GDP)/Reserved(SP/DSP) Register

Register Offset : 58-59h

Bit	R/W Access	Initial Value	Field Name and Description
15:8	R	00h	Memory Limit Upper 8 Bits: Since 64-bit Address Remapping Capability is supported, these locations are Reserved and reads zero
7:0	R	00h	Memory Base Upper 8 Bits: Since 64-bit Address Remapping Capability is supported, these locations are Reserved and reads zero

4.3.5.50 Reserved Register

Register Offset : 5A-5Bh

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4.3.5.51 Read Control 2 Register

These registers are reserved in SP/DSP modes. But they are valid in GSP and GDP modes. The attributes of Read Control 2 registers are applied for upstream packets instead of Read Control 1(62h-60h) if the an address of upstream request falls in DMA window of Address Remapping Indices.

Register Offset : 5Eh–5Ch

Bit	R/W Access	Initial Value	Field Name and Description
23:22	R	000b	Reserved.
21:19	R/W	000b	Line Prefetch Initial Count: Indicates the minimum number of lines that must be successfully prefetched from memory on a MemRdLine (or MemRd if prefetching is enabled for MemRd commands) before allowing the PCI requester to reconnect. Not persistent through warm reset.
18:16	R/W	000b	Multiple Prefetch Initial Count: Indicates the minimum number of lines that must be successfully prefetched from memory on a MemRdMult before allowing the PCI requester to reconnect. Not persistent through warm reset.
15:12	R/W	0h	Reserved.
11	R/W	0	Line Prefetch Continue: If set, and prefetching for MemRdLine commands is enabled, MemRdLine (and MemRd, if prefetching is enabled for MemRd commands) prefetching will be continuous. As each line of data is returned to PCI, another line will be read from HyperTransport, creating a moving prefetch window. Otherwise, prefetching will end when the specified number of lines has been fetched. Not persistent through warm reset.
10	R/W	0	MultPrefetchContinue: If set, and prefetching for MemRdMult commands is enabled, MemRdMult prefetching will be continuous. As each line of data is returned to PCI, another line is read from HyperTransport, creating a moving prefetch window. Otherwise, prefetching will end when the specified number of lines has been fetched. Not persistent through warm reset.
9:8	R/W	00b	PCI Delayed Requests: This controls the number of PCI delayed requests that may be outstanding at one time. The value in the register plus 1 is the number that will be allowed, enabling from one to four buffers. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
7:5	R/W	000b	Line Prefetch Count: This indicates the number of lines to be prefetched for MemRdLine commands, and MemRd commands if prefetching is enabled for them, in addition to the line containing the original request address. MemRd Line (and MemRd, if enabled) always prefetch at least to the end of the first line. This field may not be set to a larger value than Multiple Prefetch Count. Not persistent through warm reset.
4:2	R/W	000b	Multiple Prefetch Count: This indicates the number of lines to be prefetched for MemRdMult commands, in addition to the line containing the original request address. MemRdMults always prefetch at least to the end of the first line. Not persistent through warm reset.
1	R/W	0	Mem Rd Prefetch Enable: if set, PCI MemRd commands are treated as prefetchable using the same prefetch controls as for memRdLine. Otherwise, no prefetching is performed for MemRds, and they fetch only the initially requested DW or QW. Not persistent through warm reset.
0	R/W	1	Prefetch Enable: This bit enables prefetching for prefetchable read requests. If clear, no prefetching of any kind is performed. Not persistent through warm reset.

4.3.5.52 Reserved Register

Register Offset 5Fh

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4.3.5.53 Read Control 1 Register

Register Offset : 62h–60h

Bit	R/W Access	Initial Value	Field Name and Description
23:22	R	000b	Reserved.
21:19	R/W	000b	Line Prefetch Initial Count: Indicates the minimum number of lines that must be successfully prefetched from memory on a MemRdLine (or MemRd if prefetching is enabled for MemRd commands) before allowing the PCI requester to reconnect. Not persistent through warm reset.
18:16	R/W	000b	Multiple Prefetch Intitial Count: Indicates the minimum number of lines that must be successfully prefetched from memory on a MemRdMult before allowing the PCI requester to reconnect. Not persistent through warm reset.
15:12	R/W	0h	Reserved.
11	R/W	0	Line Prefetch Continue: If set, and prefetching for MemRdLine commands is enabled, MemRdLine (and MemRd, if prefetching is enabled for MemRd commands) prefetching will be continuous. As each line of data is returned to PCI, another line will be read from HyperTransport, creating a moving prefetch window. Otherwise, prefetching will end when the specified number of lines has been fetched. Not persistent through warm reset.
10	R/W	0	MultPrefetchContinue: If set, and prefetching for MemRdMult commands is enabled, MemRdMult prefetching will be continuous. As each line of data is returned to PCI, another line is read from HyperTransport, creating a moving prefetch window. Otherwise, prefetching will end when the specified number of lines has been fetched. Not persistent through warm reset.
9:8	R/W	00b	PCI Delayed Requests: This controls the number of PCI delayed requests that may be outstanding at one time. The value in the register plus 1 is the number that will be allowed, enabling from one to four buffers. Not persistent through warm reset.
7:5	R/W	000b	Line Prefetch Count: This indicates the number of lines to be prefetched for MemRdLine commands, and MemRd commands if prefetching is enabled for them, in addition to the line containing the original request address. MemRd Line (and MemRd, if enabled) always prefetch at least to the end of the first line. This field may not be set to a larger value than Multiple Prefetch Count. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
4:2	R/W	000b	Multiple Prefetch Count: This indicates the number of lines to be prefetched for MemRdMult commands, in addition to the line containing the original request address. MemRdMults always prefetch at least to the end of the first line. Not persistent through warm reset.
1	R/W	0	Mem Rd Prefetch Enable: if set, PCI MemRd commands are treated as prefetchable using the same prefetch controls as for memRdLine. other/Wise, no prefetching is performed for MemRds, and they fetch only the initially requested DW or QW. Not persistent through warm reset.
0	R/W	0b(SP/DSP)1b(GSP/GDP)	Prefetch Enable: This bit enables prefetching for prefetchable read requests. If clear, no prefetching of any kind is performed. Not persistent through warm reset.

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4.3.5.54 PCI Control Register

Register Offset : 63h

Bit	R/W Access	Initial Value	Field Name and Description
7:6	R	00b	Reserved.
5	R/W	0	Target Receive FIFO: If asserted, new requests from the PCI bus are only accepted when PCI interface's target receive FIFO is completely empty. When deasserted, writes are accepted as long as there is space in the FIFO for the write command and the first beat of data. Not persistent through warm reset. Tsi308 hardware doesn't use this value. It is ignored even when in Tsi301 mode
4	R/W	0h	Park Master: This bit controls where the arbiter defaults to when there is no PCI/PCI-X request outstanding. The default can be to grant the PCI/PCI-X bus to P_GNT0_N(assumed to be connected to Tsi308) or to grant the PCI bus to the most recent master on the bus. 0 -> Park PCI/PCI-X bus on most recent master. 1 -> Park PCI/PCI-X bus on P_GNT0_N Not persistent through warm reset.
3:0	R/W	Fh	ID Sel Charge: Number of PCI clocks to charge the AD lines on a Type 0 configuration cycle before asserting P_FRAME_N. Not persistent through warm reset.

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4.3.5.55 Error Control Register

Register Offset : 67h–64h

Bit	R/W Access	Initial Value	Field Name and Description
31	R	0	Reserved.
30	R/C	0	PCI Command/Address Parity Error: A parity error was detected on the PCI bus during the address phase. This is only logged if the Parity Error Response Enable bit in the Bridge Control register is set. Not persistent through warm reset.
29	R/C	0	Master Posted PCI Command Error: This is set whenever a PCI posted write intended by the Tsi308 fails to complete. Possible reasons are: Master Abort Received with Master Abort Mode = 1 Target Abort Received TRDY# Timeout Retry Timeout Write received PERR with Parity Error Response Enable = 1 Not persistent through warm reset.
28	R/W	0	Discard SERR Fatal: If a secondary bus discard timer expiration occurs with the Discard Timer SERR# Enable (DiscardSerrEn) asserted, this bit controls whether the SERR gets mapped to a fatal or nonfatal interrupt: 0 = Nonfatal 1 = Fatal Not persistent through warm reset.
27	R/C	0	Response Match Error: This chip received a response packet to its unitID, indicating that it belonged to a request issued from here, but no request with that SrcTag is outstanding. Persistent through warm reset.
26	R/W	0	Response Match Error Nonfatal Enable: A nonmatching response causes a nonfatal interrupt to be asserted, as enabled by SerrEn in the Command register. Not persistent through warm reset.
25	R/W	0	Response Match Error Fatal Enable: A nonmatching response causes a fatal interrupt to be asserted, as enabled by SerrEn in the Command register. Not persistent through warm reset.
24:22	R/C	0	Reserved.

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Bit	R/W Access	Initial Value	Field Name and Description
21	R/W	0	Command/Address Parity Error Nonfatal Enable : if asserted, detection of a command phase parity error on the PCI bus causes a nonfatal interrupt to be asserted, as enabled by SerrEn in the Command register. Not persistent through warm reset.
20	R/W	0	Command/Address Parity Error Fatal Enable: if asserted, detection of a command phase parity error on the PCI bus causes a fatal interrupt to be asserted, as enabled by SerrEn in the Command. Not persistent through warm reset.
19	R/W	0	Post Nonfatal Enable: if asserted, PCI master posted writes that fail to complete successfully on the bus result in a nonfatal interrupt assertion, if enabled by SerrEn in the Command. Not persistent through warm reset.
18	R/W	0	Post Fatal Enable: If asserted, PCI master posted writes that fail to complete successfully on the bus result in a fatal interrupt assertion, if enabled by SerrEn in the Command register. Not persistent through warm reset.
17	R/C	0	Retry Timeout: A master transaction was retried beyond the value in Retry Timer. Not persistent through warm reset.
16	R/C	0	TRDY Timeout: A master transaction took a TRDY timeout. Not persistent through warm reset.
15:8	R/W	80h	**Retry Timer:** Controls how many retries of a particular operation HyperTransport tries before giving up. Setting the disconnects timer to 0 disables it. Not persistent through warm reset.
7:0	R/W	80h	TRDY Timer: Controls the number of PCI clocks that the Tsi308/Tsi301 waits for TRDY or STOP when acting as a master before timing out. Setting timer to 0 disables it. Not persistent through warm reset.

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4.3.5.56 HyperTransport Error Control(SP/DSP)/Reserved(GSP/GDP) Register

Register Offset : 69h-68h

Bit	R/W Access	Initial Value	Field Name and Description
15-12	R	0h	Reserved
11	R/W	0h	SerrFatalEn: SerrEn bit of Bridge Control Register controls whether an interrupt gets generated at all when SERR assertion is detected. This bit controls whether the interrupt is Fatal or Nonfatal: 0 = Nonfatal Enable 1 = Fatal Enable Not persistent through warm reset.
10	R/W	0h	CrcNonFatalEn: CRC Nonfatal Enable. If asserted, detecting a HyperTransport CRC error causes a nonfatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
9	R/W	0h	CrcFatalEn: If asserted, detection of a HyperTransport CRC error causes a fatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
8	R/W	0h	NxaSyncFloodEn: If asserted, detection of a posted HT request or HT response hitting the end of the HT chain causes sync flooding and sets the LinkFail bit. Not persistent through warm reset.
7	R/W	0h	NxaNonFatalEn: If asserted, detecting a HyperTransport response or posted request hitting the end of the HyperTransport chain causes a nonfatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable

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Bit	R/W Access	Initial Value	Field Name and Description
6	R/W	0h	NxaFatalEn: If asserted, detection of a posted HyperTransport request or response hitting the end of the HyperTransport chain causes a fatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
5	R/W	0h	OvfSyncFloodEn: If asserted, detection of a HyperTransport receive buffer overflow error causes sync flooding and the LinkFail bit to be set. Not persistent through warm reset. 0 = Disable 1 = Enable
4	R/W	0h	OvfNonFatalEn: If asserted, detecting a HyperTransport receive buffer overflow error causes a nonfatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
3	R/W	0h	OvfFatalEn: If asserted, detection of a HyperTransport receive buffer overflow error causes a fatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
2	R/W	0h	ProtSyncFloodEn: If asserted, detection of a protocol error causes sync flooding and the LinkFail bit to be set. Not persistent through warm reset. 0 = Disable 1 = Enable
1	R/W	0h	ProtNonFatalEn: If asserted, detecting a protocol error causes a nonfatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable
0	R/W	0h	ProtFatalEn: If asserted, detection of a protocol error causes a fatal interrupt. Not persistent through warm reset. 0 = Disable 1 = Enable

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4.3.5.57 Parity Error Reporting Enable

This register is reserved in SP/DSP modes. But, they are valid in GSP and GDP modes.

Register Offset: 6Ah

Bit	R/W Access	Initial Value	Field Name and Description
7:1	R	0h	Reserved
0	R/W	0h	Parity Error Reporting Enable: By setting this bit, the PCI2HT packets will wait for two pci clock cycles to monitor the PERR# on the bus if any. This will add up the latency by two pci-clock cycles. This parity checking will be reported as Data-Error on HT.

4.3.5.58 Reserved Register

Register Offset: 6Bh

4.3.5.59 HyperTransport Rx Data Buffer Allocation Register

Register Offset : 6Dh-6Ch

Bit	R/W Access	Initial Value	Field Name and Description
15:14	R	00b	Reserved.
13:12	R/W	01b	WantPReq: The number of buffers minus one to try to keep released in the posted request channel. Not persistent through warm reset.
11:10	R/W	01b	WantNpReq: The number of buffers minus one to try to keep released in the nonposted request channel. Not persistent through warm reset.
9:8	R/W	01b	WantResp: The number of buffers minus one to try to keep released in the response channel. Not persistent through warm reset.
7:6	R	00b	Reserved.

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Bit	R/W Access	Initial Value	Field Name and Description
5:4	R/W	01b	NeedPReq: The minimum data buffer allocation to the posted request channel. Not persistent through warm reset.
3:2	R/W	01b	NeedNpReq: The minimum data buffer allocation to the nonposted request channel. Not persistent through warm reset.
0:1	R/W	01b	NeedResp: The minimum data buffer allocation to the response channel. Not persistent through warm reset.

4.3.5.60 HyperTransport Transmit Control Register

Register Offset : 6Eh

Bit	R/W Access	Initial Value	Field Name and Description
3:0	R/W	4h	BufRelSpace: controls the throttling of buffer release messages on a busy bus. If the bus is idle, buffer releases always get issued immediately. When the bus is busy, buffer release messages are forced into the packet stream. This field gives the minimum number of DW that must be allowed to pass between forced buffer releases to prevent them from absorbing too much bandwidth. Not persistent through warm reset.

4.3.5.61 Link Impedance Control 0 Register

Link Impedance Control 0 Register of CSR0 is used for Port0 and Link Impedance Control 0 Register of

CSR1 is used for Port1 in DSP/GDP modes.

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Register Offset : 73h–70h

Bit	R/W Access	Initial Value	Field Name and Description
31:27	R	00h	Current TxUp: current impedance value for transmit pull-up resistor.
26:22	R	00h	Current TxDown: current impedance value for transmit pull-down resistor.
21:17	R	00h	Current RxTerm: current impedance value for receive termination resistor.
16:12	R/W	10h	RxTerm: impedance value for receive termination resistor. Used when RxSel is set. Not persistent through warm reset.
11	R/W	0	RxSel: enables use of CSR receive impedance values. Not persistent through warm reset.
10:6	R/W	10h	TxUp: impedance value for transmit pull-up resistor. Used when TxSel is set. Not persistent through warm reset.
5:1	R/W	00h	TxDown: impedance value for transmit pull-down resistor. Used when TxSel is set. Not persistent through warm reset.
0	R/W	0	TxSel : enables use of CSR transmit impedance values. Not persistent through warm reset.

4.3.5.62 Link Impedance Control 1 Register

These registers are not used in DSP and GDP modes. But, they are valid in SP and GSP modes.

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Register Offset : 77h–74h

Bit	R/W Access	Initial Value	Field Name and Description
31:27	R	00h	Current Tx Up: Current impedance value for transmit pull-up resistor.
26:22	R	00h	Current Tx Down: Current impedance value for transmit pull-down resistor.
21:17	R	00h	Current Rx Term: Current impedance value for receive termination resistor.
16:12	R/W	10h	Rx Term: Impedance value for receive termination resistor. Used when RxSel is set. Not persistent through warm reset.
11	R/W	0	Rx Select: Enables use of CSR receive impedance values. Not persistent through warm reset.
10:6	R/W	10h	Tx Up: Impedance value for transmit pull-up resistor. Used when TxSel is set. Not persistent through warm reset.
5:1	R/W	00h	Tx Down: Impedance value for transmit pull-down resistor. Used when TxSel is set. Not persistent through warm reset.
0	R/W	0	Tx Select: Enables use of CSR transmit impedance values. Not persistent through warm reset.

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4.3.5.63 Interrupt Capability Registers

These registers are reserved in SP/DSP modes. But, they are valid in GSP/GDP modes.

Register Offset : 7Bh-78h

Bit	R/W Access	Initial Value	Field Name and Description
31:24	R	80h	Indicates that this is an interrupt discovery and configuration block
23:16	R/W	00h	Index. Points to the indexed location
15:8	R	B4h	Points to next capability register
7:0	R	08h	HT Capability ID

4.3.5.64 Interrupt Capability Registers

These registers are reserved in SP/DSP modes.But, they are valid in GSP/GDP modes.

Register Offset : 7Fh-7Ch

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R/W	0h	Dataport: Provides read or write access to the interrupt definition register selected by the Index defined above.

4.3.5.65 Reserved Registers

Register Offset : 9Fh–80h

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4.3.5.66 Blockx Interrupty Register

These registers are valid only in SP/DSP modes. They are reserved in other modes.

Register Offset : AFh–A0h (x=0 & 1; y=0,1,2 & 3)

Bit	R/W Access	Initial Value	Field Name and Description
15	R/W	0b	Interrupt Enable: 0 -> Disabled 1 -> Enabled
14	R/W	0b	Destination Mode 0 -> Physical 1 -> Logical
13:6	R/W	FFh	Destination ID:
5:4	R/W	00b	Message Type: Not persistent through warm reset. 00 -> Fixed 01 -> Arbitrated 10 -> SMI 11 -> NMI
3	R/W	0b	Polarity: Active polarity of interrupt 0 -> Active low 1 -> Active High
2	R/W	0b	Trigger Mode: Level/Edge trigger. Not persistent through warm reset. 0 -> Edge 1 -> Level
1:0	R/W	00b	Vector: interrupt vector. Not persistent through warm reset. 00 -> Interrupt0 01 -> Interrupt1 10 -> Interrupt2 11 -> Interrupt3

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4.3.5.67 Blockx Interrupt 4 Register

Register Offset : B3h–B0h (x=0 & 1)

Bit	R/W Access	Initial Value	Field Name and Description
15	R/W	0b	Interrupt Enable: 0 -> Disabled 1 -> Enabled
14	R/W	0b	Destination Mode: 0 -> Physical 1 -> Logical
13:6	R/W	FFh	Destination ID
5:4	R/W	00b	Message Type: Not persistent through warm reset. 00 -> Fixed 01 -> Arbitrated 10 -> SMI 11 -> NMI
3	R/W	0b	Polarity: Active polarity of interrupt 0 -> Active low 1 -> Active High
2	R/W	0b	Trigger Mode: Level/Edge trigger. Not persistent through warm reset. 0 -> Edge 1 -> Level
1:0	R/W	00b	Vector: Interrupt vector. Not persistent through warm reset. 00 -> Interrupt0 01 -> Interrupt1 10 -> Interrupt2 11 -> Interrupt3

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4.3.5.68 Unit ID Clumping Capability Register

These registers are valid only in GSP/GDP modes.

Register Offset : B7h–B4h

Bit	R/W Access	Initial Value	Field Name and Description
31:27	R	10010b	Unit ID Clumping Capability
26:16	R	00h	Reserved
15:8	R	E0h	Capability 4 - Next Capability pointer
7:0	R	08h	HT Capability ID

4.3.5.69 Unit ID Clumping Support Register

These registers are valid only in GSP/GDP modes

Register Offset : BCh-B8h

Bit	R/W Access	Initial Value	Field Name and Description
31:1	R	0h	Reads Zero as Tsi308 does not clump
0	R	0h	Reserved

4.3.5.70 Unit ID Clumping Enable Register

These registers are valid only in GSP/GDP modes

Register Offset : BFh-BDh

Bit	R/W Access	Initial Value	Field Name and Description
31:1	R/W	0h	Software programmable: Unit ID Clumping in the chain is written. Tsi308 orders packet accordingly
0	R	0h	Reserved

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4.3.5.71 PCI Power Management Capability ID Register

Register Offset: C0h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	01h(GSP/GDP)/0h(SP/DSP)	**SP/DSP:** Reserved GSP/GDP: **Capability ID:** This field, when '01h' identifies the linked list item as being the PCI Power Management registers.

4.3.5.72 PCI Power Management Next Capability Pointer Register

Register Offset: C1h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h(GSP/GDP)/00h(SP/DSP)	**SP/DSP:** Reserved GSP/GDP: **Next Cap. Pointer:** Points to the next capability block.

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4.3.5.73 Interrupt Diagnostics Register

These registers are multifunctional. The following definitions are valid only in SP/DSP modes.

Register Offset : C2h

Bit	R/W Access	Initial Value	Field Name and Description
7	R/W	0b	Reserved
6	R/W	0b	Initiate: writing a 1 asserts an interrupt as if it was coming from the pin. This bit is cleared by hardware once the interrupt is sent. This bit cannot be written by S/W once it's set. It can be written by S/W only after hardware clears this bit. Not persistent through warm reset.
5	R	0	Active: If 1, the given pin has an asserted (level) interrupt. Not persistent through warm reset.
4:0	R/W	00000b	Pin Number: Determines which pin the Activate and Initiate fields affect (019 only; others are reserved). 3:0 -> Block0, Interrupts 3,2,1 and 0 7:4 -> Block1, Interrupts 3,2,1 and 0 8 -> Block0, Interrupt4 9 -> Block1, Interrupt4 Not persistent through warm reset.

4.3.5.74 Interrupt Block Level0 Register

These registers are multifunctional. The following definitions are valid only in SP/DSP modes.

Register Offset : C3h

Bit	R/W Access	Initial Value	Field Name and Description
7	R	0b	Reserved
6	R/W	0b	Block Enable
5:0	R/W	000000b	Block Vector: upper vector bits for Block0 Interrupts. Not persistent through warm reset.

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4.3.5.75 Power Management Capabilities Register

These registers are multifunctional. The following definitions are valid only in GSP/GDP modes.

Register Offset: C3h-C2h

Bit	R/W Access	Initial Value	Field Name and Description
15:11	R	0b	**PME Support:** As Tsi308 doesn't support PME #, these bits read zeros
10	R	0b	D2_Support: 0= this function do not support D2 state and returns zero.
9	R	0	**D1_Support:** 0= this function do not support D1 state and returns zero.
8:6	R	0b	**Aux_Current:** Indicates that there is no requirement for auxiliary current as D3Cold device power state is not supported
5	R	0b	**DSI:** Indicates that there is no special initialization requirement
4	R	0b	Reserved
3	R	0b	**PMECLK:** Indicates that the PCI clock is required for PME# generation. As Tsi308 does not assert PME#, this bit reads zero.
2:0	R	010b	**Version:** A value of 010b indicates that this function complies with Revision 1.1 of the *PCI Bus Power Management Interface Specification*.

4.3.5.76 Interrupt Block Level1 Register

These registers are multifunctional. The following definitions are valid only in SP/DSP modes.

Register Offset : C4h

Bit	R/W Access	Initial Value	Field Name and Description
7	R	0b	Reserved
6	R/W	0b	Block Enable
5:0	R/W	000000b	Block Vector: Upper vector bits for Block1 Interrupts. Not persistent through warm reset.

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4.3.5.77 Interrupt Block Level2 Register

These registers are multifunctional. The following definitions are valid only in SP/DSP modes.

Register Offset : C5h

Bit	R/W Access	Initial Value	Field Name and Description
7	R	0b	Reserved
6	R/W	0b	Block Enable
5:0	R/W	000000b	Block Vector: Upper vector bits for Block2 Interrupts. Not persistent through warm reset.

4.3.5.78 Power Management Control & Status Registers

These registers are multifunctional. The following definitions are valid only in GSP/GDPmodes.

Register Offset : C5h-C4h

Bit	R/W Access	Initial Value	Field Name and Description
15	R	0b	**Note: PME_STS:** PME# Status. This bit reads zero as Tsi308 does not support PME#
14:9	R	000000b	**Note:** Reserved
8	R	0b	**Note: PME_EN:** PME# Enable. As per spec. it's a R/W. Since, Tsi308 does not support PME# this bit is hardwired to zero.
7:2	R	000000b	**Note:** Reserved
1:0	R/W	00b	**Note: PWRS:** Power State. It indicates the function's current power state. **Note:** 00 = D0, **Note:** 01 = D1, **Note:** 10 = D2, **Note:** 11 = D3hot **Note:** If software attempts to write an unsupported state(D1, D2, D3hot), the write operation completes normally on the bus; however, the data is discarded and no state change occurs.

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4.3.5.79 Bridge Support Extensions Register

Register Offset : C6h

Bit	R/W Access	Initial Value	Field Name and Description
7:1	R	0h	Reserved in all modes
0	R	0b	**SP/DSP:** Reserved GSP/GDP: **BPCC_EN:** 0= bus power/clock control policies defined in *PCI Bus Power Management Interface Specification Section 4.7.1* have been disabled

4.3.5.80 Reserved

These are reserved in all modes.

Register Offset : C7h

Bit	R/W Access	Initial Value	Field Name and Description
7-0	R	0h	Reserved

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4.3.5.81 Transmit Buffer Counter Maximum Count0 Register



Buffer releases in excess of these thresholds are discarded to allow throttling of traffic.

Register Offset : CAh-C8h

Bit	R/W Access	Initial Value	Field Name and Description
23:20	R/W	Fh	Rdata: response data buffer threshold. Not persistent through warm reset.
19:16	R/W	Fh	RCmd: response command buffer threshold. Not persistent through warm reset.
15:12	R/W	Fh	NpData: nonposted data buffer threshold. Not persistent through warm reset.
11:8	R/W	Fh	NpCmd: nonposted command buffer threshold. Not persistent through warm reset.
7:4	R/W	Fh	Pdata: posted data buffer threshold. Not persistent through warm reset.
3:0	R/W	Fh	PCmd: posted command buffer threshold. Not persistent through warm reset.

4.3.5.82 Transmit Buffer Counter Maximum Count1 Register

Register Offset : CEh-CCh

Bit	R/W Access	Initial Value	Field Name and Description
23:20	R/W	Fh	Rdata: Response data buffer threshold. Not persistent through warm reset.
19:16	R/W	Fh	RCmd: Response command buffer threshold. Not persistent through warm reset.
15:12	R/W	Fh	NpData: Nonposted data buffer threshold. Not persistent through warm reset.

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Bit	R/W Access	Initial Value	Field Name and Description
11:8	R/W	Fh	NpCmd: nonposted command buffer threshold. Not persistent through warm reset.
7:4	R/W	Fh	Pdata: posted data buffer threshold. Not persistent through warm reset.
3:0	R/W	Fh	PCmd: posted command buffer threshold. Not persistent through warm reset.

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4.3.5.83 Test Port Register

These registers are valid only in GSP/GDP modes. They are Reserved in other modes.

Register Offset : D0h

Bit	R/W Access	Initial Value	Field Name and Description
7	R/W	0h	**Tst_DO** data from the bus (input)
6	R/W	0h	**Tst_DI** data to the bus (output)
5	R/W	0h	**Tst_MS** signal (output)
4	R/W	0h	**Tst_Mod1** signal(output)
3	R/W	0h	**Tst_Mod0** signal(output)
2	R/W	0h	**Tst_Clk** signal (output)
1	R/W	0h	**DIO Direction**. It selects the direction of Tst_DIO. 0=output 1=input
0	R/W	0h	**Tst_DIO** signal(Input/Output). Its direction is based on DIO Direction bit.

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4.3.5.84 StoreForward Registe

Register Offset : D1h

Bit	R/W Access	Initial Value	Field Name and Description
7:5	R	0h	Reserved
4	R/W	0h	Initiate OIR: This bit allows Tsi308 to trigger OIR sequence through software. 0 = Disable 1 = Enable
3:2	R/W	Values from straps	PCI Frequency: These bits determine the new pci frequency range. PCI PLL takes values from these bits during warm reset or secondary bus reset through s/w. Initialization patterns are driven using these bits after warm reset or secondary bus reset in PCIX mode. These registers can be programmed regardless of the status of secondary bus reset. Programmed values will take effect only when the secondary bus is in reset via s/w. 00 – 25 MHz to 50 MHz 01 – 50 MHz to 66 MHz 10 – 66 MHz to 100 MHz 11 – 100 MHz to 133 MHz
1	R/W	1h	Store and Issue: mechanism for posted, non-posted and response packets. This will ensure the whole data is buffered and available for issuing on pci bus. This will be helpful mainly in HT2PCI path when PCI bandwidth is higher than HT Link bandwidth.
0	R/W	0h	Store and forward: mechanism for posted, non-posted and response packets. This will ensure the whole data is buffered and available for forwarding.

4.3.5.85 SMAF field

These register is valid only in GSP/GDP modes. They are reserved in all other modes.

Register Offset : D2h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R/W	0h	**SMAF field:** Corresponds to SMAF values that are from host.

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4.3.5.86 Reserved

Offset D3h is reserved and reads 0.

4.3.5.87 Sri Index Register

These registers are valid only in GSP/GDP modes.

Register Offset : D7h-D4h

Bit	R/W Access	Initial Value	Field Name and Description
31:8	R	0h	Reserved
7:0	R/W	0h	Sri Index: Points to the location where values from SriData has to be written or read.

4.3.5.88 Sri Data Register

These registers are valid only in GSP/GDP modes.

Register Offset : DBh-D8h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R	0h	Sri Data: Data is read in the location pointed by Sri Index.

4.3.5.89 Diagnostics Link 0 Received CRC Expected Register

These registers are valid only in SP/ DSP modes. They are reserved in other modes.

Register Offset : DFh-DCh

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R		Expected CRC value for Link 0: This register is for software use and will survive cold and warm reset as long as there is no power off.

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4.3.5.90 HT Capability ID Register

These registers are valid only in GSP/GDP modes.

Register Offset : E0h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	08h	Id : HT Capability ID assigned by the PCI SIG.

4.3.5.91 Capability 5 Register

These registers are valid only in GSP/GDP modes.

Register Offset : E1h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	F0h	Pointer : pointer to the next capability block. It points to PCI-X capability registers

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4.3.5.92 DMA Map Register

These registers are valid only in GSP/GDP modes.

Register Offset : E3h-E2h

Bit	R/W Access	Initial Value	Field Name and Description
15:11	R	14h	Type: HyperTransport 64-bit address remapping. Always reads 10100b, indicating this is a HyperTransport 64-bit address remapping.
10:9	R	1h	MapType: This field is 1h to indicate that Tsi308 implements 64-bit address remapping
8:4	R/W	00h	**IOSize:** This field defines the number of bits of downstream IO addresses are discarded. The default is 0 to pass all 25 bits of a HyperTransport technology IO cycle. All discarded bits are 0s on the secondary bus
3:0	R	1h	# of DMA mapping support.

4.3.5.93 Index Register

These registers are valid only in GSP/GDP modes.

Register Offset : E7h-E4h

Bit	R/W Access	Initial Value	Field Name and Description
31:6			Reserved
5:0	R/W	00xxxxh	Idx: This field is an index to the 64-bit address remap indexed registers.

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4.3.5.94 Data Lower Register

These registers are valid only in GSP/GDP modes.

Register Offset : EBh-E8h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R/W	0000_0000 h	DataLower: This is the lower 32 bit of the 64-bit address remap indexed registers accessed through the Idx field above.

4.3.5.95 Data Upper Register

These registers are valid only in GSP/GDP modes.

Register Offset : EFh-ECh

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R/W	0000_0000 h	DataUpper: This is the upper 32 bit of the 64-bit address remap indexed registers accessed through the Idx field above.

4.3.5.96 PCI-X Capability ID Register

These registers (FFh-F0h) are multifunctional. The following tables show the value they hold in GSP/GDP modes

Register Offset : F0h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	07h	**Id:** PCI-X capability ID assigned by the PCI SIG.

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4.3.5.97 Capability 6 Register

Register Offset : F1h

Bit	R/W Access	Initial Value	Field Name and Description
7:0	R	00h or c0h	Pointer: Pointer to the next capability block. In RevC mode, it points to C0h to support PCI power management capability. In non-RevC mode, it will be always 00h as we don't support any other capabilities

4.3.5.98 PCI-X Secondary Status Register

Register Offset : F3-F2h

Bit	R/W Access	Initial Value	Field Name and Description
15:9	R	0	Reserved
8-6	R	Values from Straps	This register enables configuration software to determine to what mode and (in PCI-X mode) what frequency the bridge set the secondary bus the last time secondary RST# was asserted. 0 = conventional mode 1 = 66 MHz 2 = 100 MHz 3 = 133 MHz 4,5,6,7 are reserved
5	R/C	0	**Split Request Delayed (write 1 to clear):** This bit is set any time the bridge has a request to forward a transaction on the secondary bus but cannot because there is not enough room within the limit specified in the Split Transaction Commitment Limit field in the Downstream Split Transaction Control register. Once set, this bit remains set until software writes a 1 to this location.
4	R/C	0	**Split Completion Overrun(write 1 to clear):** This bit is set if the bridge terminates a split completion on the secondary bus with Retry of Disconnect at Next ADB because the bridge buffers are full. Once set, this bit remains set until software writes a 1 to this location.

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Bit	R/W Access	Initial Value	Field Name and Description
3	R/C	0	**Unexpected Split Completion (write 1 to clear):** This bit is set if an unexpected split completion with a Requester ID equal to the bridge's secondary bus number, device number 00h, and function number 0 is received on the secondary interface. Once set, this bit remains set until software writes a 1 to this location. 0= No unexpected split completion has been received. 1= An unexpected split completion has been received.
2	R/C	0	**Split Completion Discarded(write 1 to clear):** This bit is set if the bridge discards a split completion. Once set, this bit remains set until software writes a 1 to this location.
1	R	1	133-MHz capable: This bit indicates bridge's secondary bus interface is capable of 133 MHz.
0	R	1(CSR0)/0(CSR1)	64-bit Device: This bit indicates the width of the bridge's secondary AD's interface. 0= 32-bit device 1= 64-bit device Device 0 can act as 64-bit in SP/GSP modes. Device 1 is not visible in the above mentioned modes. Device 1 will work only during DSP/ GDP modes and that in 32-bit mode.

4.3.5.99 PCI-X Bridge Status Register

Register Offset : F7-F4h

Bit	R/W Access	Initial Value	Field Name and Description
31:16	R	0	Reserved: Not applicable as primary interface is HT.
15:8	R	00h	Bus Number: This field contains the Primary Bus Number.
7:3	R	1Fh	Device Number: It indicates the number of this device.
2:0	R	0	**Function Number:** It indicates the number of this function. It's hardcoded to zero.

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4.3.5.100 Upstream Split Transaction Control Register

Register Offset : FBh-F8h

Bit	R/W Access	Initial Value	Field Name and Description
31:16	R/W	6h	**Split Transaction Commitment Limit:** Indicates the cumulative size for all memory read transactions forwarded by the bridge from secondary to primary bus. software is expected to leave these registers to its default values
15:0	R	5h	**Split Transaction Capacity:** Indicates the size of the buffer used for storing Split completion for requesters on the secondary bus addressing completers on the primary bus.

4.3.5.101 Downstream Split Transaction Control Register

Register Offset : FFh-FCh

Bit	R/W Access	Initial Value	Field Name and Description
31:16	R/W	6h	**Split Transaction Commitment Limit:** Indicates the cumulative size for all memory read transactions forwarded by the bridge from primary to secondary bus. software is expected to leave these registers to its default values.
15:0	R	5h	**Split Transaction Capacity:** Indicates the size of the buffer used for storing Split completion for requesters on the primary bus addressing completers on the secondary bus.

4.3.5.102 Diagnostics Link 0 Receive CRC Received Register

These registers are multifunctional and they hold the following values in SP/DSP modes.

Register Offset : F3h-F0h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R		Received CRC value for Link 0: This register is for software use and will survive cold and warm reset as long as there is no power off.

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4.3.5.103 Diagnostics Link 1 Receive CRC Expected Register

These registers are multifunctional and they hold the following values in SP/DSP modes.

Register Offset : F7h-F4h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R		**Expected CRC value for Link 1:** This register is for software use and will survive cold and warm reset as long as there is no power off.

4.3.5.104 Diagnostics Link 1 Receive CRC Received Register

These registers are multifunctional and they hold the following values in SP/DSP modes.

Register Offset : FCh-F8h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R		Received CRC value for Link 1: This register is for software use and will survive cold and warm reset as long as there is no power off.

4.3.5.105 Scratch Register

These registers are multifunctional and they hold the following values in SP/DSP modes.

Register Offset : FFh-FCh

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R/W		Scratch: Read/write software scratch register. Not persistent through warm reset.

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4.3.6 CSR Layout for IOAPIC

To be compatible with x86 systems, Tsi308 provides a memory-mapped version of the interrupt discovery and configuration register set. The memory-mapped register set is comparable to a standard IOAPIC register set and the redirection table entries would have the layout shown in Section 5.4.3.7. These registers are available in the Function1 pci configuration space for PCI-A & PCI-B. These registers are valid only in “GSP/GDP and RevC” mode. They are not visible in other modes as Tsi308 will be a single function device in those modes. In “GSP/GDP and RevC” mode, Interrupts can be programmed only by IOAPIC register set whereas in other modes it can be programmed by Interrupt Discovery registers.

Device ID	Vendor ID	00h
Status	Command	04h
Class Code	Revision ID	08h
Reserved		0Ch
BAR 0[31:0]		10h
BAR 0[63:32]		14h
Reserved		18h
Reserved		1Ch
Reserved		20h
Reserved		24h
Reserved		28h
Subsystem ID	Subsystem Vendor ID	2Ch
Reserved		30h
Reserved		34h
Reserved		38h
Reserved		3Ch

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4.3.6.1 Vendor ID and Device ID

Register Offset : 03h–00h

Bit	R/W Access	Initial Value	Field Name and Description
31:16	R	9001h	IOAPIC Device ID
15:0	R	1142h	Vendor ID

4.3.6.2 Command and Status

Register Offset : 07h–04h

Bit	R/W Access	Initial Value	Field Name and Description
31:3	R	0200_0000h	Default state
2	R/W	0h	PCI Master Enable: 1 = Enables IOAPIC to initiate the interrupts to host
1	R/W	0h	Memory Enable: 1 = Enables acess to the memory space specified at 10h
0	R	0h	Default state

4.3.6.3 IOAPIC Revision ID and Class Code

Register Offset : 0Bh–08h

Bit	R/W Access	Initial Value	Field Name and Description
31:08	R	080010	IOAPIC Class code
7:0	R	01	Revision ID

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4.3.6.4 IOAPIC BAR

Register Offset : 17h–10h

Bit	R/W Access	Initial Value	Field Name and Description
63:12	R/W	0000_0000_0000_0h	IOAPIC BAR: Specifies the IOAPIC register set address space
11:0	R	004h	Hardwired to indicate a 4KB block of 64-bit non-prefetchable memory space

4.3.7 IOAPIC Registers

Each IOAPIC register set support 10 interrupts. The IOAPIC registers are accessed by an indirect addressing scheme using two registers (IOAPIC INDEX and IOAPIC DATA) that are located in memory space specified by BAR0 in function 1 CSR. Memory Mapped Registers for accessing IOAPIC registers are given below:

4.3.7.1 IOAPIC INDEX

Register: 03-00h

Bit	R/W Access	Initial Value	Field Name and Description
31:8	R	0h	Reserved
7:0	R/W	0h	Index: It selects the IOAPIC Registers

4.3.7.2 IOAPIC DATA

Register: 13-10h

Bit	R/W Access	Initial Value	Field Name and Description
31:0	R/W	0h	IOAPIC Data Port: Data written to this location is actually to the address pointed by Index. Data read from this location is actually from the address pointed by Index.
7:0	R/W	0h	Index: It selects the IOAPIC Registers

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4.3.7.3 IOAPIC Registers

Address Offset	Bit	R/W Access	Initial Value	Field Name and Description
00h	31:28	R	0h	Reserved
00h	27:24	R/W	0h	IOAPIC ID: This register contains the 4 bit APIC ID. The ID serves as a physical name of the IOAPIC. All APIC devices using the APIC bus should have a unique APIC ID
00h	23:0	R	0h	Reserved

4.3.7.4 IOAPIC Version

Address Offset	Bit	R/W Access	Initial Value	Field Name and Description
01h	31:24	R	0h	Reserved
01h	23:16	R	09h	Maximum Redirection Entry: This field contains the entry number (0 being the lowest entry) of the highest entry in the I/O Redirection Table. The value is equal to the number of interrupt input pins for the IOAPIC minus one. Tsi308 supports 10 interrupts per port.
01h	15:8	R	0h	Reserved
01h	7:0	R	11h	APIC Version: This 8-bit field identifies the implementation version. The version number assigned to the IOAPIC is 11h

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4.3.7.5 IOAPIC Arbitration ID

Address Offset	Bit	R/W Access	Initial Value	Field Name and Description
02h	31:28	R	0h	Reserved
02h	27:24	R/W	0h	IOAPIC Arbitration ID: This register contains the bus arbitration priority for the IOAPIC
02h	23:0	R	0h	Reserved

4.3.7.6 Redirection Table

Address Offset	Bit	R/W Access	Initial Value	Field Name and Description
10h	31:0	R/W	0h	INTR0[31:0]
11h	31:0	R/W	0h	INTR0[63:32]
12h	31:0	R/W	0h	INTR1[31:0]
13h	31:0	R/W	0h	INTR1[63:32]
14h	31:0	R/W	0h	INTR2[31:0]
15h	31:0	R/W	0h	INTR2[63:32]
16h	31:0	R/W	0h	INTR3[31:0]
17h	31:0	R/W	0h	INTR3[63:32]
18h	31:0	R/W	0h	INTR4[31:0]
19h	31:0	R/W	0h	INTR4[63:32]
1Ah	31:0	R/W	0h	INTR5[31:0]
1Bh	31:0	R/W	0h	INTR5[63:32]
1Ch	31:0	R/W	0h	INTR6[31:0]
1Dh	31:0	R/W	0h	INTR6[63:32]
1Eh	31:0	R/W	0h	INTR7[31:0]

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Address Offset	Bit	R/W Access	Initial Value	Field Name and Description
1Fh	31:0	R/W	0h	INTR7[63:32]
20h	31:0	R/W	0h	INTR8[31:0]
21h	31:0	R/W	0h	INTR8[63:32]
22h	31:0	R/W	0h	INTR9[31:0]
23h	31:0	R/W	0h	INTR9[63:32]
3Fh-24h		R	0h	Reserved

4.3.7.7 INTERRUPT Definition Registers

Bit	R/W Access	Initial Value	Field Name and Description
63:56	R/W	0h	Intr Info[15:8] Destination
55:32	R/W	0h	Intr Info[55:32] Extended Destination: If a device does not support 32-bit destinations, this field is read-only 0.
31:17	R/O	0h	Reserved
16	R/W	1h	Mask: When this bit is set, the interrupt is masked.
15	R/W	0h	Intr Info[5] Request EOI: If set, after each interrupt request is sent the device waits for the Waiting for EOI bit to be cleared before sending another interrupt
14	R/O	0h	Waiting for EOI: If RQEOI is 1, then this bit is set by hardware when an interrupt request is sent and cleared by hardware when the EOI is returned.
13	R/W	0h	Polarity: For external interrupt sources, when this bit is set, the interrupt signal is active-low. If clear, the interrupt signal is active-high. For internal interrupt sources, this bit is reserved.
12	R/O	0h	Reserved
11	R/W	0h	Intr Info[6] Destination Mode: 0 = Physical, 1 = Logical
10:8	R/W	0h	Intr Info[4:2] Message Type[2:0]
7:0	R/W	0h	Intr Info[23:16] Vector

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5. Electrical Characteristics

This chapter defines the electrical characteristics of the Golden Gate HyperTransport-PCI/PCI-X bridge.

- “AC Timing Definitions” on page 184
- “Clock Parameters” on page 187
- “HyperTransport Output Timing Characteristics” on page 188
- “HyperTransport Input Timing Characteristics” on page 190
- “HyperTransport Interconnect Timing Characteristics” on page 192
- “HyperTransport Transfer Timing Characteristics” on page 193
- “HyperTransport Impedance Requirements” on page 195
- “HyperTransport DC Electrical Characteristics” on page 197
- “Reset Timing” on page 198
- “Power Consumption” on page 200
- “Thermal Data” on page 200
- “Thermal Recommendations” on page 201
- “ Power Sequencing” on page 202
- “Supply Operatiing Ranges” on page 202

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5.1 AC Timing Definitions

Figure 9: Timing Definitions Waveform

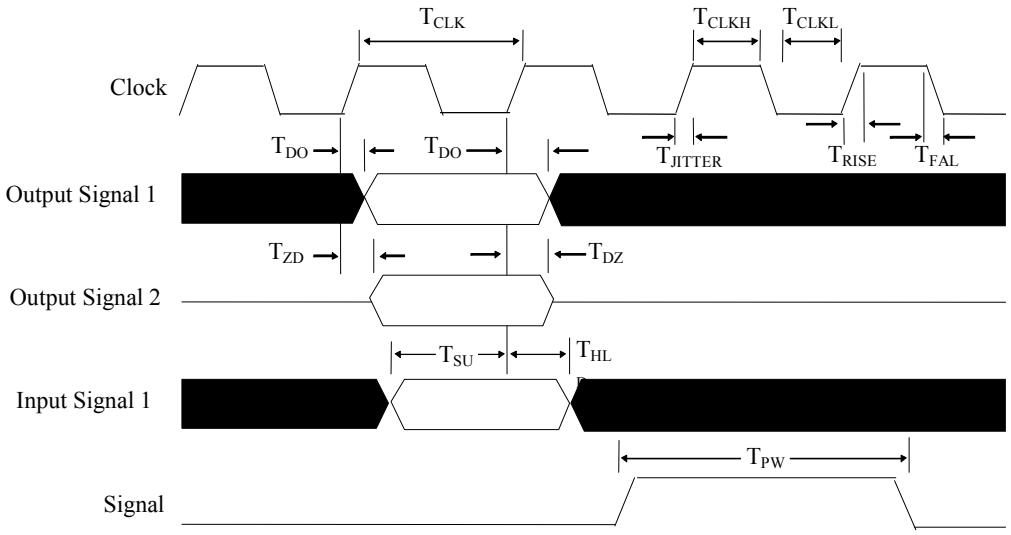


Table 23: AC Timing Definitions

Symbol	Definition
T_{CLK}	Clock period.
T_{CLKL}	Clock low. Amount of time the clock is low in one clock period.
T_{CLKH}	Clock high. Amount of time the clock is high in one clock period.
T_{RISE}	Rise time. Low to high transition time.
T_{FALL}	Fall time. High to low transition time.
T_{JITTER}	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
T_{DO}	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
T_{ZD}	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
T_{DZ}	Data valid to Z state. Amount of time after the reference clock edge that the valid takes to become tri-stated.

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Table 23: AC Timing Definitions

Symbol	Definition
T_{SU}	Input set-up. Amount of time before the reference clock edge that the input must be valid.
T_{HLD}	Input hold. Amount of time after the reference clock edge that the input must remain valid.
T_{PW}	Pulse width. Amount of time the input or output is active.

5.1.1 AC Timing Values

Table 24: Typical AC Timing Values

Symbol	Conditions	Bidirectional			Output			Units
		Min	Nom	Max	Min	Nom	Max	
Frequency	--	DC		100	DC		100	MHz
T_{CLK}	--	10		DC	10		DC	ns
T_{CLKH}	--	30		70	30		70	%
T_{CLKL}	--	30		70	30		70	%
T_{RISE}	2.2 pF		0.37			0.27		ns
	27 pF		2.36			1.83		ns
	53 pF		4.74			3.54		ns
	78 pF		7.31			5.33		ns
	100 pF		9.92			7.13		ns
T_{FALL}	2.2 pF		0.30			0.25		ns
	27 pF		2.30			1.80		ns
	53 pF		4.82			3.58		ns
	78 pF		7.41			5.36		ns
	100 pF		10.0			7.15		ns
T_{JITTER}	--		500			500		ps
T_{DO}	--	1		10	1		10	ns
T_{ZD}	--		10			10		ns
T_{DZ}	--		5			5		ns

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Table 24: Typical AC Timing Values

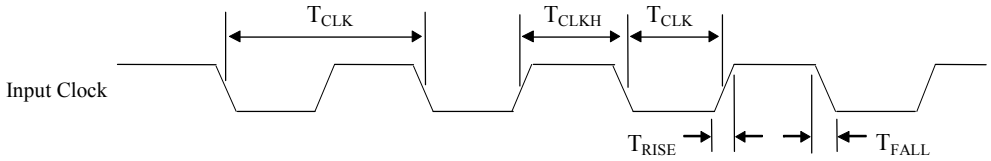
Symbol	Conditions	Bidirectional			Output			Units
		Min	Nom	Max	Min	Nom	Max	
T_{SU}	--		4			4		ns
T_{HLD}	--		1			1		ns
T_{PW}	--	10			10			ns

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5.2 Clock Parameters

5.2.1 Input Clock

Figure 10: Input Clock Parameters Waveform



(Ta = 0° C to +70° C Commercial, Vcc = +3.3 V)

Table 25: Input Clock Parameters

Symbol	25 MHz		33.33 MHz		50 MHz		66.66 MHz		100 MHz		133.33 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Frequency	24.95	25.05	33.27	33.40	49.9	50.1	66.53	66.8	99.8	100.2	133.07	133.6	MHz
T_{CLK}	39.92	40.08	29.94	30.06	19.96	20.04	14.97	15.03	9.98	10.02	7.49	7.51	ns
T_{CLKH}	12	28	9	21	6	14	4.5	10.5	3	7	2.25	5.25	ns
T_{CLKL}	12	28	9	21	6	14	4.5	10.5	3	7	2.25	5.25	ns
T_{RISE}	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	ns
T_{FALL}	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	-	3.0	ns

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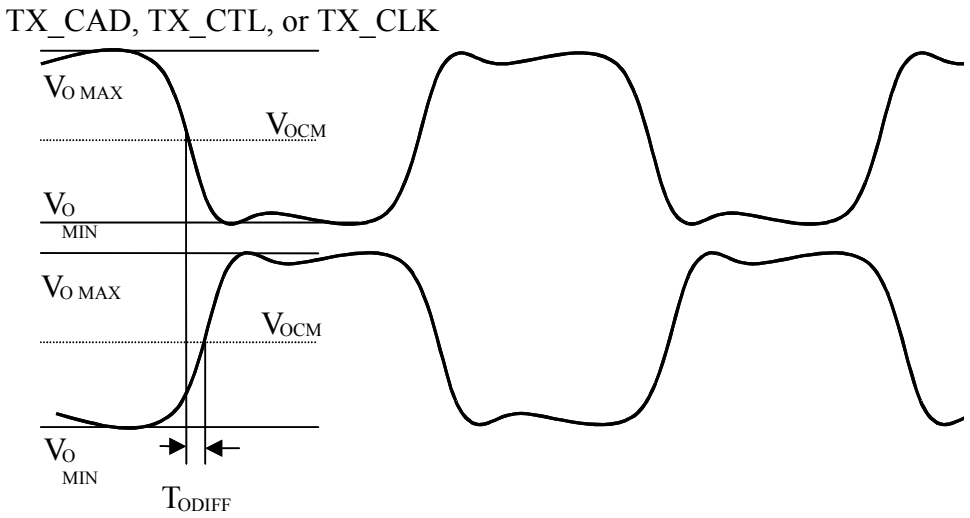
5.3 HyperTransport Output Timing Characteristics

5.3.1 Differential Output Skew

T_{ODIFF} defines the allowable output differential skew as defined by the time difference measured in a single-ended fashion at the midpoint of the transition of the true signal and the midpoint of the transition of the complement signal.

Differential output skew is limited primarily by DV_{OCM} such that at the given minimum output edge rate differential skew would cause a violation of DV_{OCM} before violating the output differential skew specification.

Figure 11: T_{ODIFF}



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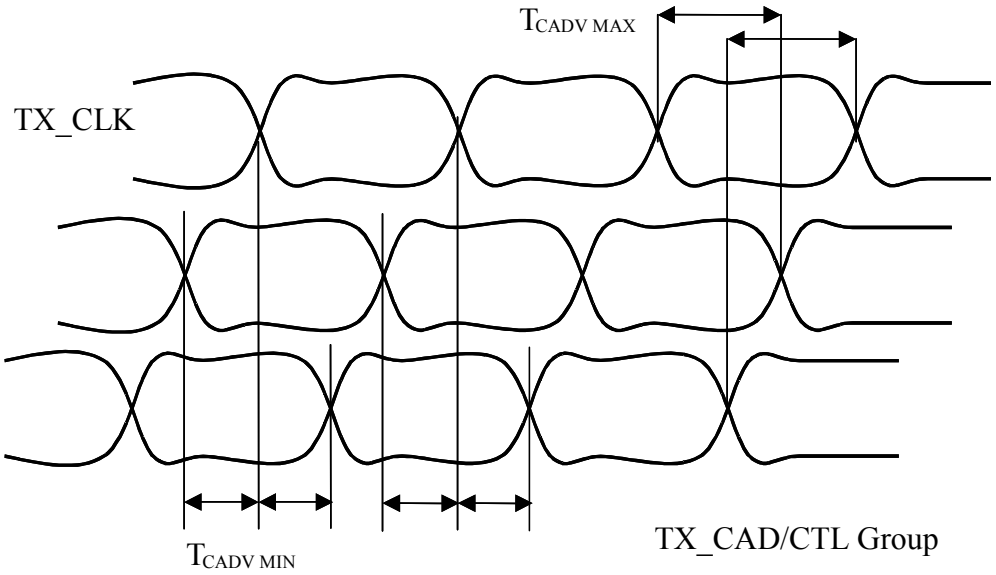
5.3.2 T_{CADV} (TCADValid)

T_{CADV} defines the TX_CAD/CTL valid time from TX_CAD/CTL to TX_CLK or from TX_CLK to TX_CAD/ CTL and is simultaneously an aggregate measurement of the accuracy of the transmitter to place the TX_CAD/CTL edges relative to TX_CLK edge, the minimum TX_CLK bit-time and, the TX_CAD/CTL group skew.

Nominally, TX_CLK is driven delayed by one-half of a bit-time from the TX_CAD/CTL transitions. This delay provides required setup and hold time to and from the TX_CLK edge at the receiver and therefore allows for simple data recovery. T_{CADV_MIN} is measured at the device pins from the crossing point of either the latest TX_CAD/CTL transition to the crossing point of the TX_CLK transition or the TX_CLK transition to the earliest TX_CAD/CTL transition. T_{CADV_MAX} is measured at the device pins from either the crossing point of the earliest TX_CAD/CTL transition to the crossing point of the TX_CLK transition or the TX_CLK transition to the latest TX_CAD/CTL transition.

Because T_{CADV} is an aggregate measure of different uncertainties, it must be measured over a large number of samples and under conditions defined to maximize TX_CAD/CTL group skew, TX_CLK edge placement error, and TX_CLK phase compression.

Figure 12: T_{CADV}



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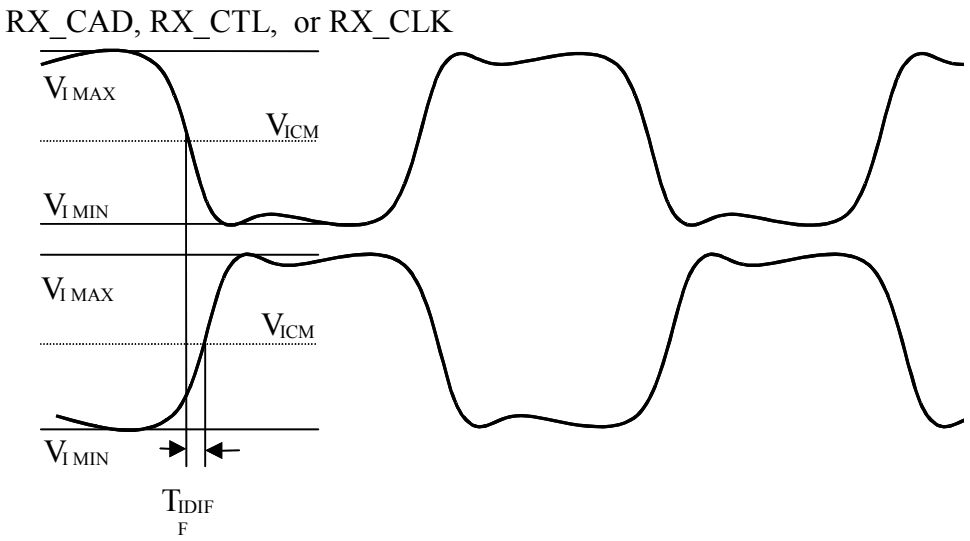
5.4 HyperTransport Input Timing Characteristics

5.4.1 Input Differential Skew

T_{IDIFF} defines the allowable input differential skew as defined by the time difference measured in a single-ended fashion at the midpoint of the transition of the true signal and the midpoint of the transition of the complement signal.

Differential input skew is limited primarily by DV_{ICM} such that at the given minimum output edge rate differential skew would cause a violation of DV_{ICM} before violating the output differential skew specification.

Figure 13: T_{IDIFF}



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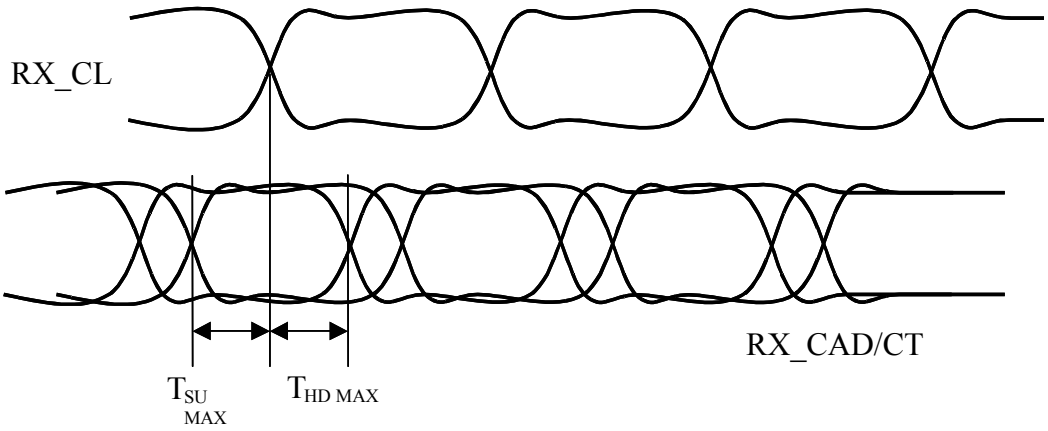
5.4.2 T_{SU} and T_{HD}

T_{SU} defines the receiverís required input setup time T_{SU} is measured from the crossing point of the last RX_CAD transition to the RX_CLK transition crossing point. T_{SU} accounts for receiver package skew, distribution skew, and device input setup time. .

T_{HD} defines the receiverís required input hold time. $_{HD}$ is measured from the crossing point of the earliest RX_CAD transition to the RX_CLK transition crossing point. T_{HD} accounts for receiver package skew, distribution skew, and device input hold time. T_{SU} and T_{HD} do not necessarily cover the required time to attain V_{ID_MIN} (AC) at the specified minimum input edge rates.$_{T}$

In the following figure, $T_{SU\ MAX}$ represents the maximum setup time that the device can require. This corresponds to the minimum setup time that the system can provide to the device input.

Figure 14: T_{SU} and T_{HD}



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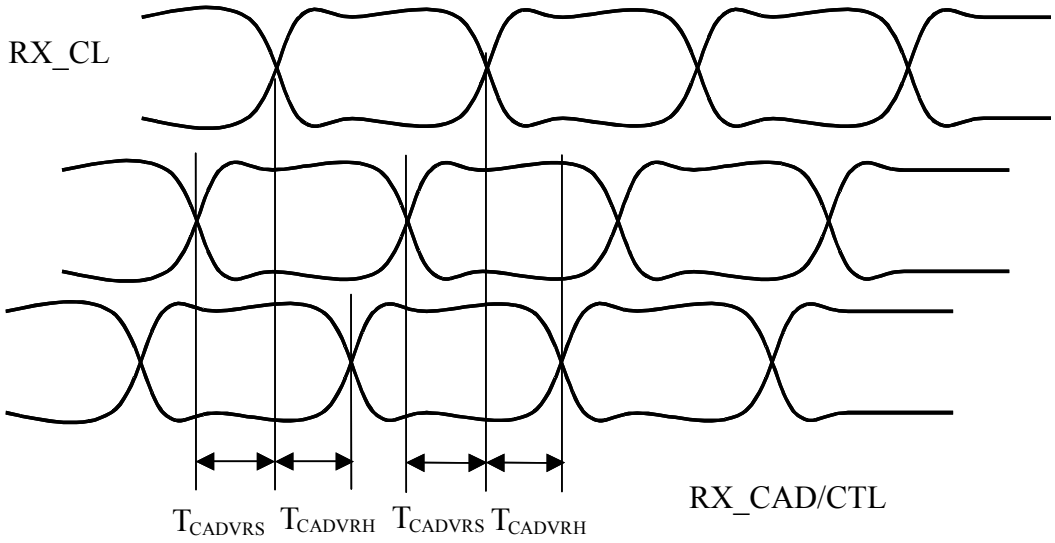
5.5 HyperTransport Interconnect Timing Characteristics

5.5.1 $T_{CADVRS/RH}$

$T_{CADVRS/RH}$ defines the remaining RX_CAD valid times to RX_CLK (T_{CADVRS}) and from RX_CLK to RX_CAD (T_{CADVRH}) measured at the receiver inputs. $T_{CADVRS/RH}$ are used as an aggregate and accumulative measure of the timing uncertainty composed of device output skew, clock edge placement error, and interconnect skew at the device inputs. As such, $T_{CADVRS/RH}$ must be measured over a large number of samples and conditions which will maximize device output skew, interconnect skew, and clock edge placement error.

T_{CADVRS} is measured from the crossing point of the last transitioning RX_CAD signal to the crossing point of the RX_CLK transitioning signal at the receiver. T_{CADVRH} is measured from the RX_CLK transitioning signal to the first RX_CAD signal at the receiver.

Figure 15: T_{CADVRS} / $_{TCADVRH}$



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5.6 HyperTransport Transfer Timing Characteristics

The following table defines the allowed values for the transfer timing characteristics.

Table 26: HyperTransport Link Transfer Timing Specifications

Parameter	Description	Link Speed	Min	Max	Units
T_{ODIFF}	Output Differential Skew	400 MT/s		70	ps
		600 MT/s		70	ps
		800 MT/s		70	ps
		1000 MT/s		60	ps
		1200 MT/s		60	ps
T_{IDIFF}	Input Differential Skew	400 MT/s	695	1805	ps
		600 MT/s	467	1200	ps
		800 MT/s	345	905	ps
		1000 MT/s	280	720	ps
		1200 MT/s	234	600	ps
T_{CADVRS}	Receiver input CADIN valid time to CLKIN	400 MT/s	460		ps
		600 MT/s	312		ps
		800 MT/s	225		ps
		1000 MT/s	194		ps
		1200 MT/s	166		ps
T_{CADVRS}	Receiver input CADIN valid time to CLKIN	400 MT/s	460		ps
		600 MT/s	312		ps
		800 MT/s	225		ps
		1000 MT/s	194		ps
		1200 MT/s	166		ps

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Table 26: HyperTransport Link Transfer Timing Specifications

Parameter	Description	Link Speed	Min	Max	Units
T_{CADVRH}	Receiver input CADIN valid time from CLKIN	400 MT/s	460		ps
		600 MT/s	312		ps
		800 MT/s	225		ps
		1000 MT/s	194		ps
		1200 MT/s	166		ps
T_{SU}	Receiver input setup time	400 MT/s	0	250	ps
		600 MT/s	0	215	ps
		800 MT/s	0	175	ps
		1000 MT/s	0	153	ps
		1200 MT/s	0	138	ps
T_{HD}	Receiver input hold time	400 MT/s	0	250	ps
		800 MT/s	0	175	ps
		1200 MT/s	0	138	ps

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5.7 HyperTransport Impedance Requirements

R_{TT} is the value of the differential input impedance of the receiver under DC conditions implemented with an on-die differential terminating resistor. This specification must be supported by any compensation technique used within the receiver across all device specific process, voltage, and temperature operating points. The R_{TT} value is defined to match the Z_{OD} of the coupled transmission lines and to provide a slightly overdamped single-ended termination.

R_{ON} is the driver output impedance under DC conditions. This range must be maintained over the valid V_{OD} range. This specification must be supported by any compensation technique used within the output driver across all device specific process, voltage, and temperature operating points. The R_{ON} value is defined to match one-half of the Z_{OD} of the coupled transmission lines.

DR_{ON} (pull-up) is the allowable difference in the driver output impedance between the true and complement when driving a logic ë0í and when driving a logic ë1í (additionally defined as when true is driven high and when complement is driven high). DR_{ON} (pull-up) is defined to limit differences in both output rising edge slew rate and the resulting differential skew and crossing point shift.

DR_{ON} (pull-down) is the allowable difference in the driver output impedance between the true and complement when driving a logic ë1í and when driving a logic ë0í (additionally defined as when true is driven low and when complement is driven low). DR_{ON} (pull-down) is defined to limit the differences in both output falling-edge slew rate and the resulting differential skew and crossing point shift.

The following table gives the DC specifications for these parameters.

Table 27: R_{TT} and R_{ON} DC Specifications

Parameter	Description	Min	Typ	Max	Units
R_{TT}	Differential Termination	90	100	110	W
R_{ON}	Driver Output Impedance	45	50	55	W
R_{ON} (pull-up)	High-Drive Impedance Magnitude Change	0	-	5	%
R_{ON} (pull-down)	Low-Drive Impedance Magnitude Change	0	-	5	%

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5.8 HyperTransport Signal AC Specifications

Figure 16: Output Loading for AC Timing

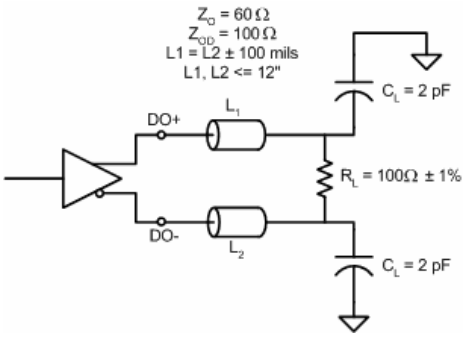


Table 28: HyperTransport Link Differential Signal AC Specifications

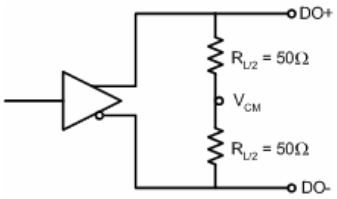
Parameter	Description	Min[a]	Typ[b]	Max[c]	Units
V_{OD}	Differential output voltage	400	600	820	mV
V_{OD}	Change in V_{OD} Magnitude	-75		75	mV
V_{OCM}	Output common-mode voltage	440	600	780	mV
V_{OCM}	Change in V_{OCM} magnitude	-50		50	mV
V_{ID}	Input differential voltage	300	600	900	mV
V_{ID}	Change in V_{ID} magnitude	-125		125	mV
V_{ICM}	Input common-mode voltage	385	600	845	mV
V_{ICM}	Change in V_{ICM} magnitude	-100		100	mV
T_R[d]	Input rising edge rate	2.0		8.0	V/ns
T_F	Input falling edge rate	2.0		8.0	V/ns

a. Minimum values assume V_{LDT} = V_{LDT} (min) as a measurement condition.
b. Typical values assume V_{LDT} = V_{LDT} (typ) as a measurement condition.
c. Maximum values assume V_{LDT} = V_{LDT} (max) as a measurement condition.
d. Input edge rates are measured in a differential fashion.

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5.9 HyperTransport DC Electrical Characteristics

Figure 17: Output Reference System Load



The following table defines the allowed values for each of the DC characteristics.

Table 29: HT Link Differential Signal DC Specifications

Parameter	Description	Min[a]	Typ[b]	Max[c]	Units
V_{OD}	Differential output voltage	495	600	715	mV
Delta V_{OD}	Change in V_{OD} Magnitude	15	-	15	mV
V_{OCM}	Output common-mode voltage	495	600	715	mV
Delta V_{OCM}	Change in V_{OCM} magnitude	15	-	15	mV
V_{ID}	Input differential voltage	200	600	1000	mV
V_{ID}	Change in V_{ID} magnitude	15	-	15	mV
V_{ICM}	Input common-mode voltage	440	600	780	mV
Delta V_{ICM}	Change in V_{ICM} magnitude	15	-	15	mV

a. Minimum values assume V_{LDT} = V_{LDT} (min) as a measurement condition.

b. Typical values assume V_{LDT} = V_{LDT} (typ) as a measurement condition.

c. Maximum values assume V_{LDT} = V_{LDT} (max) as a measurement condition.

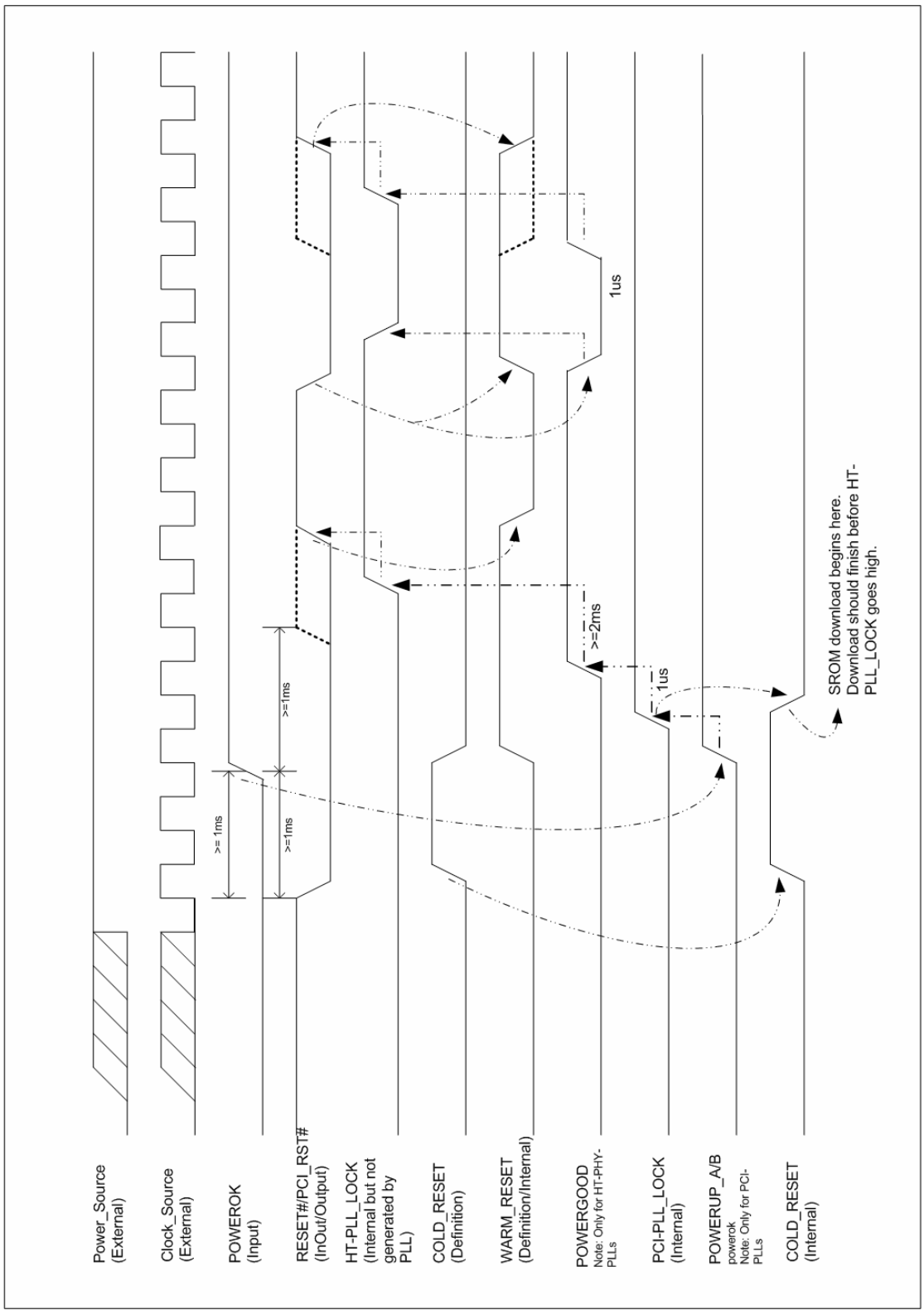
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5.10 Reset Timing

The following figure shows the reset timing of the Tsi308.

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Figure 18: Tsi308 **Reset Timing**



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5.11 Power Consumption

Tsi308 power consumption can be accurately calculated for specific configurations with a spreadsheet available upon request from Alliance Semiconductor.

5.12 Thermal Data

Table 30: Recommended Operating Temperature

Grade	Temperature
Commercial	0° to +70° ambient

Table 31: Thermal Maximum

Parameter	Value	Unit
Die Temperature Maximum	125	°C
Maximum Power	7	W

Table 32: Thermal Characteristics

Parameter	Symbol	Package	Air Flow	Value	Unit
Thermal resistance (junction to ambient)	JA	388 HSBGA	0 m/s	13.2	°C/W
			1 m/s	12.0	
			2 m/s	10.5	
		388 HSBGA w/ Heat Sink[a]	0 m/s	9.8	
			1 m/s	7.0	
			2 m/s	6.4	
Thermal resistance (junction to case)	JC	--	--	3.8	°C/W
Thermal Characterization Parameter (junction to top center)	Ψ_{JT}	--	--	2.4	°C/W

a. Recommended heat sink is Aavid 374524B00032.

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5.13 Thermal Recommendations

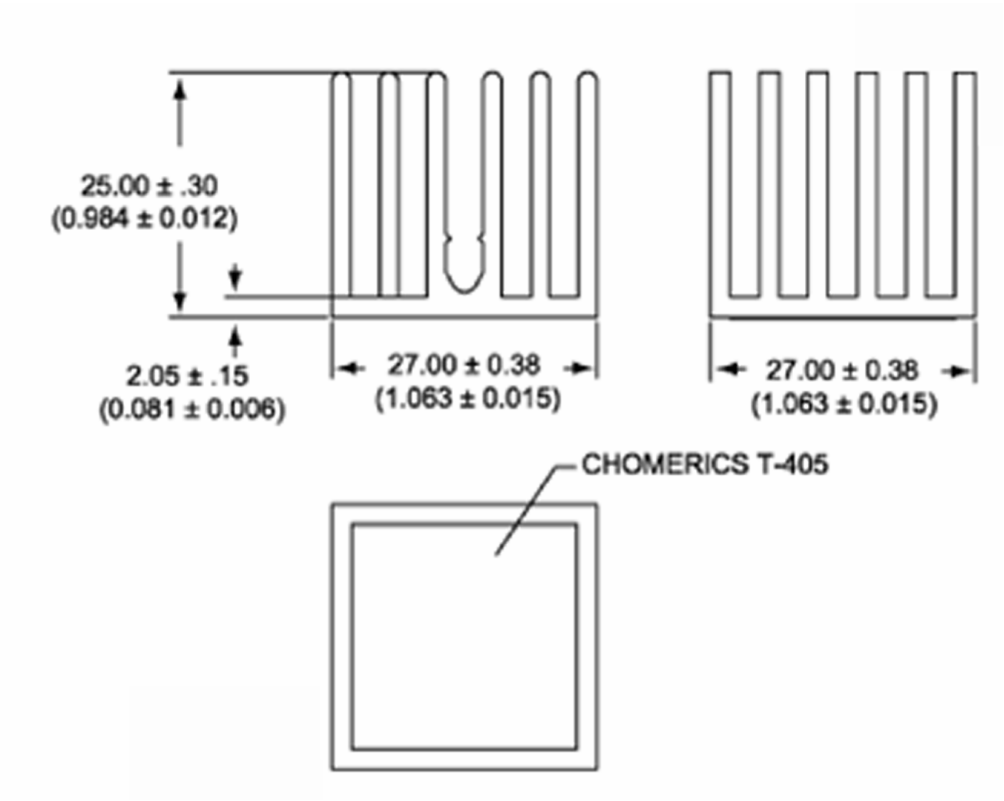
The worst-case scenario for the **Tsi308** device is to maintain a junction temperature of 125°C with an ambient temperature of 70°C and a power dissipation of 7 watts. The required $_{JA}$ to accomplish this is 7.9°C/W or less.

The actual, measured power dissipation of the device is 3.79 watts. A dissipation of 7 watts was a simulated value.

Table 32 shows the thermal performance possible by using the recommended Aavid 374524B00032 heat sink with 1 m/s or greater air flow.

Applications with a lower ambient temperature and/or less power dissipation may require less air flow and/or no heat sink.

Figure 19: Recommended Heat Sink for Tsi308



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5.14 Power Sequencing

The preferred power-on sequence for the **Tsi308** is from low voltage to high: +1.2V first, +1.8V second, then +3.3V. Tracking between the power supplies is not required.

The **Tsi308** can be powered up with the higher voltages first, but there will be more current drawn during the power-up period until the lower voltages reach their steady-state levels.

5.15 Supply Operatiing Ranges

Table 33: Supply Operating Ranges

Parameter	Minimum	Typical	Maximum	Unit
3.3V	3.13	3.3	3.46	V
1.8V Analog PLL Power	1.71	1.8	1.89	V
1.8V Core Logic Power	1.71	1.8	1.89	V
1.2V	1.14	1.2	1.26	V

5.16 Absolute Maximum Ratings

Table 34: Absolute Maximum Ratings

Parameter	Minimum	Typical	Maximum	Unit
3.3V	2.9	3.3	3.7	V
1.8V Analog PLL Power	1.6	1.8	2.0	V
1.8V Core Logic PLL	1.6	1.8	2.0	V
1.2V	1.0	1.2	1.4	V



Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions table is not implied.

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6. Packaging

This chapter discusses the following topics about Tsi308's packaging:

- "Package Specification" on page 204
- "Package Diagram" on page 232

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6.1 Package Specification

6.1.1 Pins Sorted by Name

Table 35: Tsi308 Sorted by Name

Pin Name	Pin
CAVDD0	Y4
CAVDD1	G23
CAVSS0	W4
CAVSS1	H23
CORE_CLK_TEST	A4
FATAL_ERR_N	AF3
L_POWER_OK	AF4
L_RST_N	AE4
L0_CCLK_TEST[a]	AA3
L0_DCLK_TEST*	AA4
L0_R50VLDT	N2
L0_R50VSS	N3
L0_RX_CAD_H[0]	F3
L0_RX_CAD_H[1]	F1
L0_RX_CAD_H[2]	G3
L0_RX_CAD_H[3]	H3
L0_RX_CAD_H[4]	H1
L0_RX_CAD_H[5]	K3
L0_RX_CAD_H[6]	K1
L0_RX_CAD_H[7]	M3
L0_RX_CAD_L[0]	F2
L0_RX_CAD_L[1]	G1
L0_RX_CAD_L[2]	G2
L0_RX_CAD_L[3]	H2

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
L0_RX_CAD_L[4]	J1
L0_RX_CAD_L[5]	K2
L0_RX_CAD_L[6]	L1
L0_RX_CAD_L[7]	M2
L0_RX_CLK_H	J3
L0_RX_CLK_L	J2
L0_RX_CTL_H	M1
L0_RX_CTL_L	N1
L0_TX_BYPASS_CLK	AB2
L0_TX_CAD_H[0]	AA2
L0_TX_CAD_H[1]	Y3
L0_TX_CAD_H[2]	AA1
L0_TX_CAD_H[3]	V2
L0_TX_CAD_H[4]	U2
L0_TX_CAD_H[5]	U1
L0_TX_CAD_H[6]	T2
L0_TX_CAD_H[7]	R1
L0_TX_CAD_L[0]	Y2
L0_TX_CAD_L[1]	W3
L0_TX_CAD_L[2]	Y1
L0_TX_CAD_L[3]	V3
L0_TX_CAD_L[4]	U3
L0_TX_CAD_L[5]	T1
L0_TX_CAD_L[6]	T3
L0_TX_CAD_L[7]	P1
L0_TX_CLK_H	W1
L0_TX_CLK_L	V1

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
L0_TX_CTL_H	P2
L0_TX_CTL_L	P3
L1_CCLK_TEST*	F23
L1_DCLK_TEST*	F24
L1_R50VLDT	P25
L1_R50VSS	P24
L1_RX_CAD_H[0]	AA24
L1_RX_CAD_H[1]	AA26
L1_RX_CAD_H[2]	Y24
L1_RX_CAD_H[3]	W24
L1_RX_CAD_H[4]	W26
L1_RX_CAD_H[5]	U24
L1_RX_CAD_H[6]	U26
L1_RX_CAD_H[7]	R24
L1_RX_CAD_L[0]	AA25
L1_RX_CAD_L[1]	Y26
L1_RX_CAD_L[2]	Y25
L1_RX_CAD_L[3]	W25
L1_RX_CAD_L[4]	V26
L1_RX_CAD_L[5]	U25
L1_RX_CAD_L[6]	T26
L1_RX_CAD_L[7]	R25
L1_RX_CLK_H	V24
L1_RX_CLK_L	V25
L1_RX_CTL_H	R26
L1_RX_CTL_L	P26
L1_TX_BYPASS_CLK	E25

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
L1_TX_CAD_H[0]	F25
L1_TX_CAD_H[1]	G24
L1_TX_CAD_H[2]	F26
L1_TX_CAD_H[3]	J25
L1_TX_CAD_H[4]	K25
L1_TX_CAD_H[5]	K26
L1_TX_CAD_H[6]	L25
L1_TX_CAD_H[7]	M26
L1_TX_CAD_L[0]	G25
L1_TX_CAD_L[1]	H24
L1_TX_CAD_L[2]	G26
L1_TX_CAD_L[3]	J24
L1_TX_CAD_L[4]	K24
L1_TX_CAD_L[5]	L26
L1_TX_CAD_L[6]	L24
L1_TX_CAD_L[7]	N26
L1_TX_CLK_H	H26
L1_TX_CLK_L	J26
L1_TX_CTL_H	N25
L1_TX_CTL_L	N24
LDTSTOP_N	AE3
NONFATAL_ERR_N	AF2
P0_ACK64_N	C19
P0_AD0	D5
P0_AD1	C5
P0_AD10	C8
P0_AD11	A8

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P0_AD12	D9
P0_AD13	C9
P0_AD14	B9
P0_AD15	A9
P0_AD16	D10
P0_AD17	C10
P0_AD18	B10
P0_AD19	A10
P0_AD2	B5
P0_AD20	D11
P0_AD21	C11
P0_AD22	B11
P0_AD23	A11
P0_AD24	C12
P0_AD25	A12
P0_AD26	C13
P0_AD27	B13
P0_AD28	A13
P0_AD29	D14
P0_AD3	A5
P0_AD30	C14
P0_AD31	B14
P0_AD4	C6
P0_AD5	B6
P0_AD6	A6
P0_AD7	C7
P0_AD8	B7

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P0_AD9	A7
P0_BLK0_IRQ0	E23
P0_BLK0_IRQ1	E24
P0_BLK0_IRQ2	D25
P0_BLK0_IRQ3	E26
P0_BLK0_IRQ4	C26
P0_BLK1_IRQ0	C24
P0_BLK1_IRQ1	D26
P0_BLK1_IRQ2	C25
P0_BLK1_IRQ3	D24
P0_BLK1_IRQ4	B26
P0_BYPASS_E	B3
P0_CBE0_N	A14
P0_CBE1_N	D15
P0_CBE2_N	C15
P0_CBE3_N	B15
P0_CLK	C4
P0_DEVSEL_N	A15
P0_FRAME_N	C16
P0_GNT_IN_N	B23
P0_GNT0_N	B21
P0_GNT1_N	A21
P0_GNT2_N	D22
P0_GNT3_N	C22
P0_GNT4_N	B22
P0_GNT5_N	A22
P0_IRDY_N	A16

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P0_LOCK_N	A17
P0_M66EN	A23
P0_OIR_DISCON_EVENT	A3
P0_PAR	B18
P0_PAR64	A18
P0_PCIX_133_N	B24
P0_PCIX_N	A24
P0_PERR_N	C18
P0_REQ_OUT_N	C23
P0_REQ0_N	B19
P0_REQ1_N	A19
P0_REQ2_N	C20
P0_REQ3_N	A20
P0_REQ4_N	D21
P0_REQ5_N	C21
P0_REQ64_N	D19
P0_RST_N	C2
P0_SERR_N	D18
P0_STOP_N	B17
P0_TRDY_N	C17
P0_TSTCLK	E4
P0_TSTDI	F4
P0_TSTDIO	E3
P0_TSTDO	E2
P0_TSTMOD0	E1
P0_TSTMOD1	D3
P0_TSTMS	D2

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P1_AD0	AE22
P1_AD1	AF22
P1_AD10	AF19
P1_AD11	AC18
P1_AD12	AD18
P1_AD13	AE18
P1_AD14	AF18
P1_AD15	AC17
P1_AD16	AD17
P1_AD17	AE17
P1_AD18	AF17
P1_AD19	AC16
P1_AD2	AD21
P1_AD20	AD16
P1_AD21	AE16
P1_AD22	AF16
P1_AD23	AD15
P1_AD24	AF15
P1_AD25	AD14
P1_AD26	AE14
P1_AD27	AF14
P1_AD28	AC13
P1_AD29	AD13
P1_AD3	AE21
P1_AD30	AE13
P1_AD31	AF13
P1_AD4	AF21

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P1_AD5	AC20
P1_AD6	AD20
P1_AD7	AE20
P1_AD8	AF20
P1_AD9	AD19
P1_BLK0_IRQ0	AE26
P1_BLK0_IRQ1	AF24
P1_BLK0_IRQ2	AE24
P1_BLK0_IRQ3	AD23
P1_BLK0_IRQ4	AF25
P1_BLK1_IRQ0	AA23
P1_BLK1_IRQ1	AD26
P1_BLK1_IRQ2	AD25
P1_BLK1_IRQ3	AD24
P1_BLK1_IRQ4	AC24
P1_BYPASS_E	AD3
P1_CBE0_N	AC12
P1_CBE1_N	AD12
P1_CBE2_N	AE12
P1_CBE3_N	AF12
P1_CLK	AD22
P1_DEVSEL_N	AD11
P1_FRAME_N	AF11
P1_GNT_IN_N	AF5
P1_GNT0_N	AC6
P1_GNT1_N	AD6
P1_GNT2_N	AE6

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
P1_GNT3_N	AF6
P1_GNT4_N	AC5
P1_GNT5_N	AD5
P1_IRDY_N	AD10
P1_LOCK_N	AC9
P1_M66EN	AB26
P1_OIR_DISCON_EVENT	AB23
P1_PAR	AF9
P1_PCIX_133_N	AC25
P1_PCIX_N	AC26
P1_PERR_N	AE9
P1_REQ_OUT_N	AE5
P1_REQ0_N	AC8
P1_REQ1_N	AD8
P1_REQ2_N	AE8
P1_REQ3_N	AF8
P1_REQ4_N	AD7
P1_REQ5_N	AF7
P1_RST_N	AE23
P1_SERR_N	AD9
P1_STOP_N	AF10
P1_TRDY_N	AE10
PAVDD0	D6
PAVDD1	AC22
PAVSS0	D7
PAVSS1	AC21
PCIA_CLK_TEST	B4

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Table 35: Tsi308 Sorted by Name

Pin Name	Pin
PCIB_CLK_TEST[b]	AF23
PLL_SEL_BK*	AC2
PLL_SELDIV2*	AC1
PLL_TESTENB	AB1
SCAN_EN	AB3
SROM_SCK	D1
SROM_SDA	C1
TCK	AD4
TDI	AD2
TDO	AE1
TMODE	AC3
TMS	AB25
TRST_N	AB24
TX_BYPASS_CLK_E*	AD1

a. Multiplexed pin – see Table 37 on page 226

b. Multiplexed pin – see Table 37 on page 226

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6.1.2 Pins Sorted by Number

Table 36: Tsi308 Sorted by Number

Pin	Pin Name
A3	P0_OIR_DISCON_EVENT
A4	CORE_CLK_TEST
A5	P0_AD3
A6	P0_AD6
A7	P0_AD9
A8	P0_AD11
A9	P0_AD15
A10	P0_AD19
A11	P0_AD23
A12	P0_AD25
A13	P0_AD28
A14	P0_CBE0_N
A15	P0_DEVSEL_N
A16	P0_IRDY_N
A17	P0_LOCK_N
A18	P0_PAR64
A19	P0_REQ1_N
A20	P0_REQ3_N
A21	P0_GNT1_N
A22	P0_GNT5_N
A23	P0_M66EN
A24	P0_PCIX_N
B3	P0_BYPASS_E
B4	PCIA_CLK_TEST
B5	P0_AD2

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
B6	P0_AD5
B7	P0_AD8
B9	P0_AD14
B10	P0_AD18
B11	P0_AD22
B13	P0_AD27
B14	P0_AD31
B15	P0_CBE3_N
B17	P0_STOP_N
B18	P0_PAR
B19	P0_REQ0_N
B21	P0_GNT0_N
B22	P0_GNT4_N
B23	P0_GNT_IN_N
B24	P0_PCIX_133_N
B26	P0_BLK1_IRQ4
C1	SROM_SDA
C2	P0_RST_N
C4	P0_CLK
C5	P0_AD1
C6	P0_AD4
C7	P0_AD7
C8	P0_AD10
C9	P0_AD13
C10	P0_AD17
C11	P0_AD21
C12	P0_AD24

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
C13	P0_AD26
C14	P0_AD30
C15	P0_CBE2_N
C16	P0_FRAME_N
C17	P0_TRDY_N
C18	P0_PERR_N
C19	P0_ACK64_N
C20	P0_REQ2_N
C21	P0_REQ5_N
C22	P0_GNT3_N
C23	P0_REQ_OUT_N
C24	P0_BLK1_IRQ0
C25	P0_BLK1_IRQ2
C26	P0_BLK0_IRQ4
D1	SROM_SCK
D2	P0_TSTMS
D3	P0_TSTMOD1
D5	P0_AD0
D6	PAVDD0
D7	PAVSS0
D9	P0_AD12
D10	P0_AD16
D11	P0_AD20
D14	P0_AD29
D15	P0_CBE1_N
D18	P0_SERR_N
D19	P0_REQ64_N

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
D21	P0_REQ4_N
D22	P0_GNT2_N
D24	P0_BLK1_IRQ3
D25	P0_BLK0_IRQ2
D26	P0_BLK1_IRQ1
E1	P0_TSTMOD0
E2	P0_TSTDO
E3	P0_TSTDIO
E4	P0_TSTCLK
E23	P0_BLK0_IRQ0
E24	P0_BLK0_IRQ1
E25	L1_TX_BYPASS_CLK
E26	P0_BLK0_IRQ3
F1	L0_RX_CAD_H[1]
F2	L0_RX_CAD_L[0]
F3	L0_RX_CAD_H[0]
F4	P0_TSTDI
F23	L1_CCLK_TEST[a]
F24	L1_DCLK_TEST*
F25	L1_TX_CAD_H[0]
F26	L1_TX_CAD_H[2]
G1	L0_RX_CAD_L[1]
G2	L0_RX_CAD_L[2]
G3	L0_RX_CAD_H[2]
G23	CAVDD1
G24	L1_TX_CAD_H[1]
G25	L1_TX_CAD_L[0]

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
G26	L1_TX_CAD_L[2]
H1	L0_RX_CAD_H[4]
H2	L0_RX_CAD_L[3]
H3	L0_RX_CAD_H[3]
H23	CAVSS1
H24	L1_TX_CAD_L[1]
H26	L1_TX_CLK_H
J1	L0_RX_CAD_L[4]
J2	L0_RX_CLK_L
J3	L0_RX_CLK_H
J24	L1_TX_CAD_L[3]
J25	L1_TX_CAD_H[3]
J26	L1_TX_CLK_L
K1	L0_RX_CAD_H[6]
K2	L0_RX_CAD_L[5]
K3	L0_RX_CAD_H[5]
K24	L1_TX_CAD_L[4]
K25	L1_TX_CAD_H[4]
K26	L1_TX_CAD_H[5]
L1	L0_RX_CAD_L[6]
L24	L1_TX_CAD_L[6]
L25	L1_TX_CAD_H[6]
L26	L1_TX_CAD_L[5]
M1	L0_RX_CTL_H
M2	L0_RX_CAD_L[7]
M3	L0_RX_CAD_H[7]
M26	L1_TX_CAD_H[7]

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
N1	L0_RX_CTL_L
N2	L0_R50VLDT
N3	L0_R50VSS
N24	L1_TX_CTL_L
N25	L1_TX_CTL_H
N26	L1_TX_CAD_L[7]
P1	L0_TX_CAD_L[7]
P2	L0_TX_CTL_H
P3	L0_TX_CTL_L
P24	L1_R50VSS
P25	L1_R50VLDT
P26	L1_RX_CTL_L
R1	L0_TX_CAD_H[7]
R24	L1_RX_CAD_H[7]
R25	L1_RX_CAD_L[7]
R26	L1_RX_CTL_H
T1	L0_TX_CAD_L[5]
T2	L0_TX_CAD_H[6]
T3	L0_TX_CAD_L[6]
T26	L1_RX_CAD_L[6]
U1	L0_TX_CAD_H[5]
U2	L0_TX_CAD_H[4]
U3	L0_TX_CAD_L[4]
U24	L1_RX_CAD_H[5]
U25	L1_RX_CAD_L[5]
U26	L1_RX_CAD_H[6]
V1	L0_TX_CLK_L

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
V2	L0_TX_CAD_H[3]
V3	L0_TX_CAD_L[3]
V24	L1_RX_CLK_H
V25	L1_RX_CLK_L
V26	L1_RX_CAD_L[4]
W1	L0_TX_CLK_H
W3	L0_TX_CAD_L[1]
W4	CAVSS0
W24	L1_RX_CAD_H[3]
W25	L1_RX_CAD_L[3]
W26	L1_RX_CAD_H[4]
Y1	L0_TX_CAD_L[2]
Y2	L0_TX_CAD_L[0]
Y3	L0_TX_CAD_H[1]
Y4	CAVDD0
Y24	L1_RX_CAD_H[2]
Y25	L1_RX_CAD_L[2]
Y26	L1_RX_CAD_L[1]
AA1	L0_TX_CAD_H[2]
AA2	L0_TX_CAD_H[0]
AA3	L0_CCLK_TEST[b]
AA4	L0_DCLK_TEST*
AA23	P1_BLK1_IRQ0
AA24	L1_RX_CAD_H[0]
AA25	L1_RX_CAD_L[0]
AA26	L1_RX_CAD_H[1]
AB1	PLL_TESTENB

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
AB2	L0_TX_BYPASS_CLK
AB3	SCAN_EN
AB23	P1_OIR_DISCON_EVENT
AB24	TRST_N
AB25	TMS
AB26	P1_M66EN
AC1	PLL_SELDIV2[C]
AC2	PLL_SEL_BK*
AC3	TMODE
AC5	P1_GNT4_N
AC6	P1_GNT0_N
AC8	P1_REQ0_N
AC9	P1_LOCK_N
AC12	P1_CBE0_N
AC13	P1_AD28
AC16	P1_AD19
AC17	P1_AD15
AC18	P1_AD11
AC20	P1_AD5
AC21	PAVSS1
AC22	PAVDD1
AC24	P1_BLK1_IRQ4
AC25	P1_PCIX_133_N
AC26	P1_PCIX_N
AD1	TX_BYPASS_CLK_E*
AD2	TDI
AD3	P1_BYPASS_E

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
AD4	TCK
AD5	P1_GNT5_N
AD6	P1_GNT1_N
AD7	P1_REQ4_N
AD8	P1_REQ1_N
AD9	P1_SERR_N
AD10	P1_IRDY_N
AD11	P1_DEVSEL_N
AD12	P1_CBE1_N
AD13	P1_AD29
AD14	P1_AD25
AD15	P1_AD23
AD16	P1_AD20
AD17	P1_AD16
AD18	P1_AD12
AD19	P1_AD9
AD20	P1_AD6
AD21	P1_AD2
AD22	P1_CLK
AD23	P1_BLK0_IRQ3
AD24	P1_BLK1_IRQ3
AD25	P1_BLK1_IRQ2
AD26	P1_BLK1_IRQ1
AE1	TDO
AE3	LDTSTOP_N
AE4	L_RST_N
AE5	P1_REQ_OUT_N

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
AE6	P1_GNT2_N
AE8	P1_REQ2_N
AE9	P1_PERR_N
AE10	P1_TRDY_N
AE12	P1_CBE2_N
AE13	P1_AD30
AE14	P1_AD26
AE16	P1_AD21
AE17	P1_AD17
AE18	P1_AD13
AE20	P1_AD7
AE21	P1_AD3
AE22	P1_AD0
AE23	P1_RST_N
AE24	P1_BLK0_IRQ2
AE26	P1_BLK0_IRQ0
AF2	NONFATAL_ERR_N
AF3	FATAL_ERR_N
AF4	L_POWER_OK
AF5	P1_GNT_IN_N
AF6	P1_GNT3_N
AF7	P1_REQ5_N
AF8	P1_REQ3_N
AF9	P1_PAR
AF10	P1_STOP_N
AF11	P1_FRAME_N
AF12	P1_CBE3_N

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Table 36: Tsi308 Sorted by Number

Pin	Pin Name
AF13	P1_AD31
AF14	P1_AD27
AF15	P1_AD24
AF16	P1_AD22
AF17	P1_AD18
AF18	P1_AD14
AF19	P1_AD10
AF20	P1_AD8
AF21	P1_AD4
AF22	P1_AD1
AF23	PCIB_CLK_TEST[d]
AF24	P1_BLK0_IRQ1
AF25	P1_BLK0_IRQ4

a. Multiplexed pin – see Table 37 on page 226
b. Multiplexed pin – seeTable 37 on page 226
c. Multiplexed pin – see Table 37 on page 226
d. Multiplexed pin – see Table 37 on page 226

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6.1.3 Multiplexed Pins

Table 37: Tsi308 Multiplexed Pins

Pin	Default Pin Name	Multiplexed Pin Name	Multiplex Select Pin
F23	L1_CCLK_TEST	P1_TSTMS	PLL_TESTENB
F24	L1_DCLK_TEST	P1_TSTMOD1	PLL_TESTENB
AA3	L0_CCLK_TEST	P1_TSTDIO	PLL_TESTENB
AA4	L0_DCLK_TEST	P1_TSTDI	PLL_TESTENB
AC1	PLL_SELDIV2	P1_TSTCLK	PLL_TESTENB
AC2	PLL_SEL_BK	P1_TSTMOD0	PLL_TESTENB
AD1	TX_BYPASS_CLK_E	P1_TSTDO	PLL_TESTENB
AF23	PCIB_CLK_TEST	SCAN_CLK	PLL_TESTENB

6.1.4 Power Pins

The tables in this section list the power pins for +1.2V HyperTransport power, +1.8V core power, +1.8V analog PLL power and ground, and +3.3V PCI and HT receive power.

6.1.4.1 +1.2V HyperTransport Power Pins

Table 38: Tsi308 +1.2V HyperTransport Power

Pin	Pin Name
P4	L0_VLDT
R3	L0_VLDT
U4	L0_VLDT
V4	L0_VLDT
J23	L1_VLDT
K23	L1_VLDT
M24	L1_VLDT
N23	L1_VLDT

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6.1.4.2 +1.8V Core Power Pins

Table 39: Tsi308 +1.8V Core Power

Pin	Pin Name
D17	VDD
H25	VDD
J4	VDD
L2	VDD
L11	VDD
L12	VDD
L15	VDD
L16	VDD
M11	VDD
M12	VDD
M15	VDD
M16	VDD
M23	VDD
R4	VDD
R11	VDD
R12	VDD
R15	VDD
R16	VDD
T11	VDD
T12	VDD
T15	VDD
T16	VDD
T25	VDD
V23	VDD

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Table 39: Tsi308 +1.8V Core Power

Pin	Pin Name
W2	VDD
AB4	VDD
AC10	VDD

6.1.4.3 +1.8V Analog PLL Power and Ground

Table 40: Tsi308 1.8V Analog PLL Power and Ground

Pin	Pin Name	Pin Type
Y4	CAVDD0	1.8V PLL Power
G23	CAVDD1	1.8V PLL Power
D6	PAVDD0	1.8V PLL Power
AC22	PAVDD1	1.8V PLL Power
A4	PAVDD2	1.8V PLL Power
W4	CAVSS0	PLL Ground
H23	CAVSS1	PLL Ground
D7	PAVSS0	PLL Ground
AC21	PAVSS1	PLL Ground
B4	PAVSS2	PLL Ground

6.1.4.4 +3.3V PCI Core and I/O Power and HT Receive Power

Table 41: Tsi308 +3.3V PCI Core and I/O Power and HT Receive Power

Pin	Pin Name
B8	VCC3V3 / VDDIO / VDDIOA
B12	VCC3V3 / VDDIO / VDDIOA
B16	VCC3V3 / VDDIO / VDDIOA
B20	VCC3V3 / VDDIO / VDDIOA
B25	VCC3V3 / VDDIO / VDDIOA

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Table 41: Tsi308 +3.3V PCI Core and I/O Power and HT Receive Power

Pin	Pin Name
C3	VCC3V3 / VDDIO / VDDIOA
D4	VCC3V3 / VDDIO / VDDIOA
D8	VCC3V3 / VDDIO / VDDIOA
D12	VCC3V3 / VDDIO / VDDIOA
D16	VCC3V3 / VDDIO / VDDIOA
D20	VCC3V3 / VDDIO / VDDIOA
D23	VCC3V3 / VDDIO / VDDIOA
G4	VCC3V3 / VDDIO / VDDIOA
K4	VCC3V3 / VDDIO / VDDIOA
L3	VCC3V3 / VDDIO / VDDIOA
T24	VCC3V3 / VDDIO / VDDIOA
U23	VCC3V3 / VDDIO / VDDIOA
Y23	VCC3V3 / VDDIO / VDDIOA
AC4	VCC3V3 / VDDIO / VDDIOA
AC7	VCC3V3 / VDDIO / VDDIOA
AC11	VCC3V3 / VDDIO / VDDIOA
AC15	VCC3V3 / VDDIO / VDDIOA
AC19	VCC3V3 / VDDIO / VDDIOA
AC23	VCC3V3 / VDDIO / VDDIOA
AE2	VCC3V3 / VDDIO / VDDIOA
AE7	VCC3V3 / VDDIO / VDDIOA
AE11	VCC3V3 / VDDIO / VDDIOA
AE15	VCC3V3 / VDDIO / VDDIOA
AE19	VCC3V3 / VDDIO / VDDIOA
AE25	VCC3V3 / VDDIO / VDDIOA

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6.1.5 Ground Pins

This table lists the common ground pins for +1.2V HyperTransport power, +1.8V core power, and +3.3V PCI and HT receive power. The PLL ground pins are listed in Section 6.1.4.3 on page 228.

Table 42: Tsi308 Ground Pins

Pin	Pin Name
A1	VSS
A26	VSS
D13	VSS
H4	VSS
L4	VSS
L13	VSS
L14	VSS
L23	VSS
M4	VSS
M13	VSS
M14	VSS
M25	VSS
N4	VSS
N11	VSS
N12	VSS
N13	VSS
N14	VSS
N15	VSS
N16	VSS
P11	VSS
P12	VSS
P13	VSS
P14	VSS

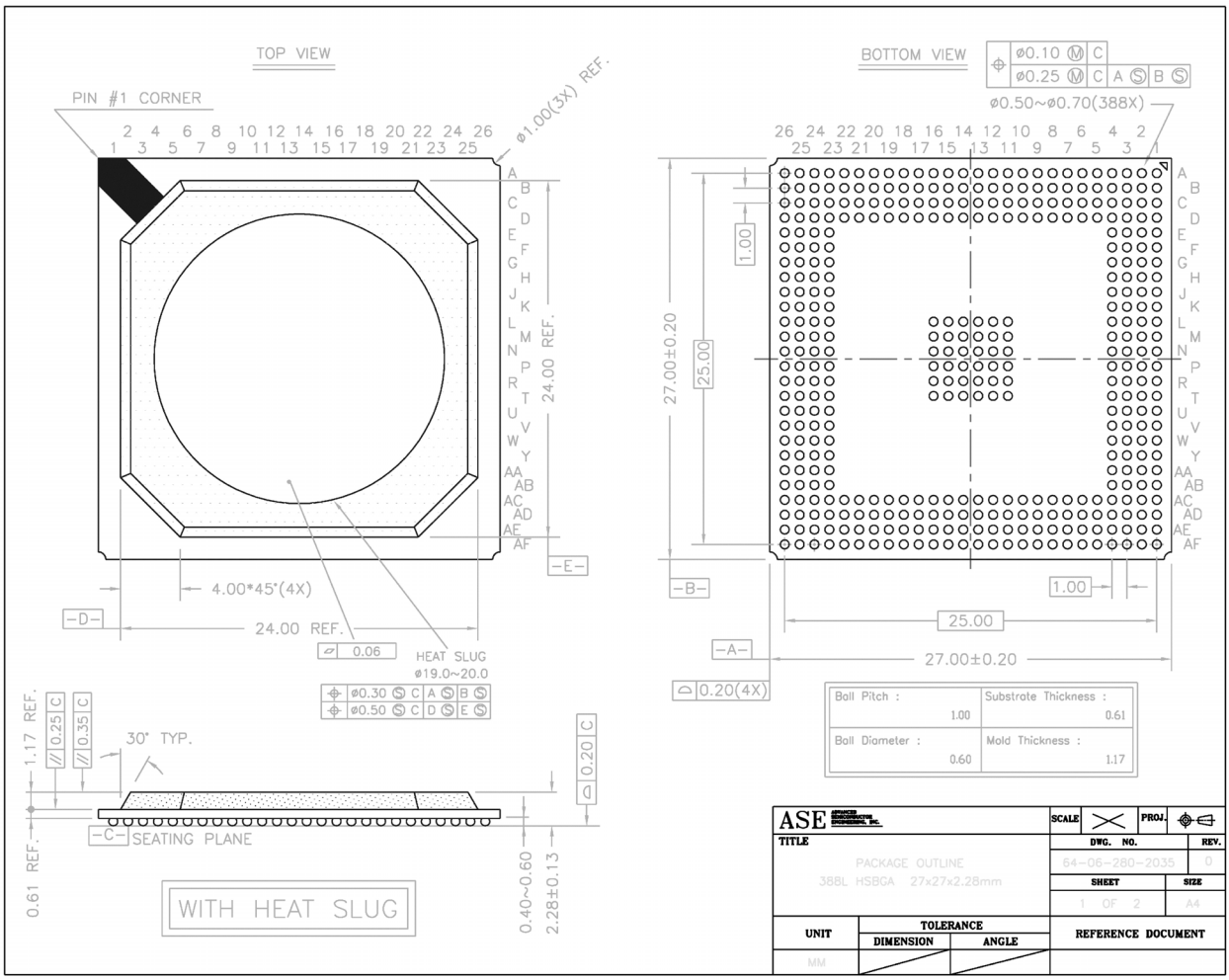
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Table 42: Tsi308 Ground Pins

Pin	Pin Name
P15	VSS
P16	VSS
P23	VSS
R2	VSS
R13	VSS
R14	VSS
R23	VSS
T4	VSS
T13	VSS
T14	VSS
T23	VSS
W23	VSS
AC14	VSS
AF1	VSS
AF26	VSS

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6.2 Package Diagram



6.2.1 Package Handling Procedures

- Moisture Classification Level: Level 3
- Storage: Parts may be stored in unopened vacuum-packed antistatic bag up to a minimum of 12 months at < 40°C and 90% humidity. Parts may be stored outside of bag indefinitely at 20% humidity.
- Floor Life: Packages will absorb moisture after opening the bag. Parts must be mounted on PCB within 48 hours after bag is opened; otherwise, baking is required. Floor life conditions are 30°C and 60% humidity.
- Baking Time: 12 hours @ 125°C.

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A. Online Insertion and Removal

This chapter discusses the following topics about Tsi308's online insertion options:

- "Overview" on page 233
- "Insertion and Removal Sequence" on page 233

A.1 Overview

Tsi308 supports Online Insertion and Removal of PCI/X cards on its secondary side. Switching of modes (PCI to PCIX and vice versa) and change of frequency is possible, upon insertion of the new card in RevC mode. Tsi308 uses P0_OIR_DISCON_EVENT and P1_OIR_DISCON_EVENT to support OIR operation on PCI-A and PCI-B ports respectively.

A.2 Insertion and Removal Sequence

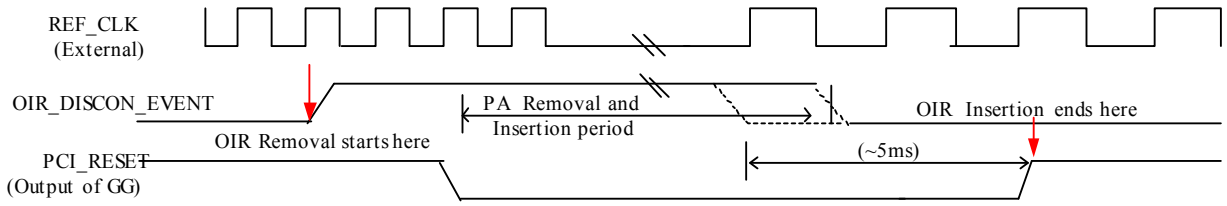
The following sequences explain the actions taken by Tsi308 after the detection of the OIR event.

1. Initial state of Tsi308 is assumed to be up and running.
2. The OIR logic in Tsi308 monitors the assertion of P0_OIR_DISCON_EVENT for PCI-A and P1_OIR_DISCON_EVENT for PCI-B.
3. Upon hot removal of PCI/X card, corresponding OIR_DISCON_EVENT gets asserted. The design requirement for the PCI/X card is such that, OIR_DISCON_EVENT signal is asserted first and then after few milli seconds the PCI/X card can be disconnected.
4. Tsi308 completes the ongoing transaction on the PCI port. Tsi308 asserts the REQ# to prevent other PCI masters from taking the bus. No further transactions happen on the PCI bus.
5. All the subsequent HT to PCI writes are dropped. HT to PCI read request results in the return of 0x0 data back to HT. Any pending PCI to HT writes are dropped internal to the Tsi308. PCI to HT reads are completed on the HT side but dropped on the PCI side. Flushing all the buffers and sending responses back to CPU takes 40us, after the assertion of OIR_DISCON_EVENT.
6. CPU writes to the SecBusReset (bit 6 of the Bridge Control Register) to reset the PCI port. The reference clock for the PCI port is assumed to be stable for few clock cycles (10 clock cycles) after the port is reset. Then the clocks can be shut off if needed. The reset bit is written only after the host CPU receives all the responses and there are no outstanding requests for the OIRed PCI port.

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7. Switching of modes from PCI to PCIX or vice versa can be done by setting proper strap values when the PCI side is in reset.
8. New PCI/X card can be inserted and powered up.
9. Clock for the PCI/X card is restarted or adjusted to a new frequency.
10. CPU writes the new PCI frequency values in CSR that are routed to PCI PLL. The standard frequencies for PCI mode are 25, 33, 50 and 66 MHz. Standard frequencies for PCI-X modes are 50, 66, 100 and 133 MHz. However the PCI frequencies can be adjusted to any value between the standard frequencies for each mode. Refer definitions for bits[3:2] in section 5.4.1.89 for CSR values, their corresponding PCI frequency ranges and when to program these values.
11. PCI PLL is allowed to lock to the new frequency. PCI PLL takes about 5ms to lock.
12. After the PCI PLL's are locked, CPU writes to the SecBusReset signal to deassert the reset bit. This pulls the PCI port out of reset.
13. Software initializes the PCI/X card through the Tsi308 device.

Figure 20: OIR Sequence



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B. Typical Applications

This chapter discusses the following topics about Tsi308's configuration options:

- "Recommendations for Use" on page 235
- "PCB Layout Guidelines" on page 237
- "Power Distribution" on page 243
- "AS90L10208 Die Pad-to-Ball Trace Length Information" on page 245
- "Example PCB Stackup for HyperTransport" on page 248

B.1 Recommendations for Use

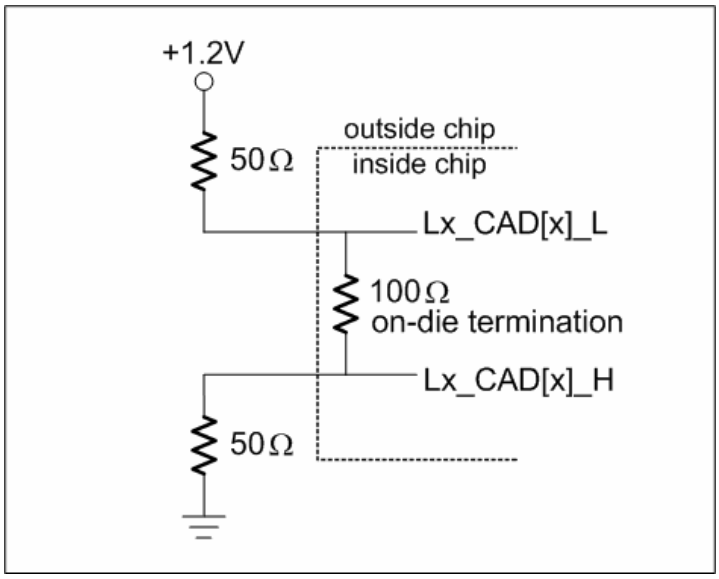
B.1.1 Unused HyperTransport CAD, CLK, and CTL Inputs

If using only one of the two available HyperTransport link interfaces, then the unused Lx_RX_CAD[7:0], Lx_CLK inputs must be pulled to their logic low levels. This means that Lx_CAD[x]_L must be pulled high and Lx_CAD[x]_H must be pulled low. A 50Ω pull-up / pull-down resistor value is recommended as this will hold Lx_CAD[x]_L at +0.9V and Lx_CAD[x]_H at +0.3V, both of which are correct HT logic levels. Figure 21 shows how the input terminations work.

This scheme would also be used to terminate unused inputs where a 2-bit or 4-bit HT interface was being used.

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Figure 21: Terminating Unused HT CAD Inputs

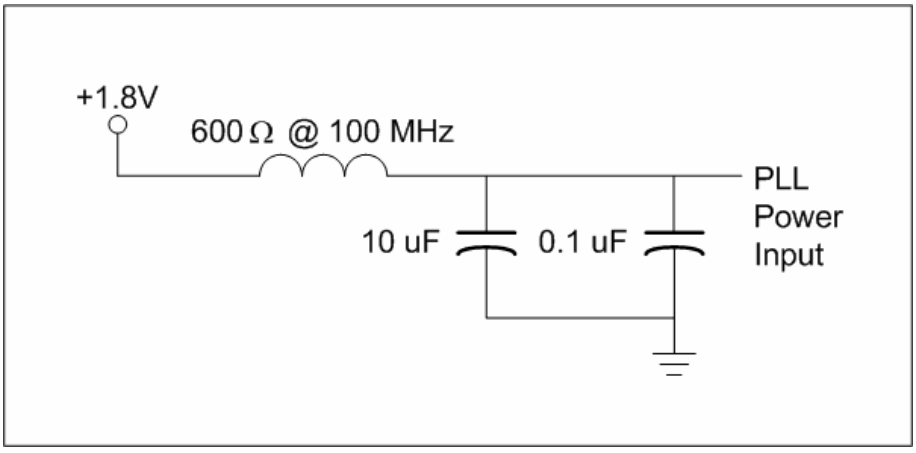


B.1.2 Analog PLL Power Filtering

For optimal performance of the AS90L10208 on-board PLLs, it is important to provide adequate power filtering for the dedicated PLL power pins, listed in § 8.3.3.

The recommended power filtering for each of the PLL power pins is a series ferrite bead followed by a low-ESR 10 µF capacitor and a 0.1 µF ceramic capacitor to GND. A diagram is shown in Figure 22. Each PLL power pin should have its own filter.

Figure 22: Recommended PLL Power Filtering



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It is recommended that the selected ferrite bead have a value of 600Ω @ 100 MHz and be capable of sustaining 200 mA current. It is not recommended that a resistor be used in place of the ferrite bead as the current drawn by the PLL will cause an unacceptable drop in voltage.

B.1.3 Decoupling Capacitor Recommendations

IDT recommends that each power pin (+1.2V, +1.8V, and +3.3V) of the Tsi308 have one 0.1 or 0.01 µF ceramic capacitor to GND. The use of surface-mount capacitor packs makes it easier to place these decoupling capacitors near and directly underneath the Tsi308 package.

In addition, several bulk capacitors are recommended. Tsi308 reference platforms have eight 10 µF X5R dielectric ceramic capacitors for +3.3V, eight of the same capacitors for +1.8V, and one each for +1.2V L0_VLDT and L1_VLDT. These bulk capacitors are placed directly adjacent to the Tsi308 package.

B.2 PCB Layout Guidelines

B.2.1 Tsi308 HyperTransport Interface Layout Guidelines

The Tsi308 is a PCI/PCI-X to HyperTransport bridge, that also acts as a HyperTransport tunnel. This layout guide focuses on the HyperTransport interface only. The AS90L10208 conforms to draft 1.05 of the HyperTransport specification.

HyperTransport is a parallel, unidirectional protocol with differential, DDR signaling on both the transmit and receive interfaces. The AS90L10208 supports link widths of 8, 4 and 2 bits and link frequencies of 800, 600, 500, 400, 300 and 200 MHz. The bus width can be independent between transmit and receive interfaces, permitting efficient allocation of system board resources, whereby a bigger bus width can be used for data intensive interfaces and a smaller bus width used for non-intensive applications.

HyperTransport uses a specialized version of LVDS I/Os, with a V_{LDT} of 1.2V. Low-voltage signaling combined with very high data speeds require strict adherence to good layout practices and power circuitry design on any board using the AS90L10208. The AS90L10208 supports a bus width of 2, 4, or 8 bits on both the transmit and receive interfaces on both of the HyperTransport ports.

These are the signals on the AS90L10208 HyperTransport interface:

- L_TX_CAD_H/L[7:0]
- L_TX_CLK_H/L
- L_TX_CTL_H/L
- L_RX_CAD_H/L[7:0]
- L_RX_CLK_H/L

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- L_RX_CTL_H/L
- L_RST_N
- L_POWER_OK
- LDTSTOP_N

The RST_N , POWER_OK and LDTSTOP_N signals are not subject to the same stringent layout requirements of the CAD, CTL, and CLK signals.

The ball assignments for the pins listed above on the AS90L10208 conform to the recommendations outlined in the *Interface Design Guide* published by the HyperTransport Technology Consortium, thereby allowing for easy point-to-point routing between conformant devices on the system board. Conformant devices have their ball out assigned in a manner that permits easier breakout for clean point-to-point routing without additional layer changes.

If the die pad-to-ball trace length matching of the device that interfaces to the AS90L10208 does not fall within the range recommended by the HyperTransport consortium in the *Interface Design Guide* or any layout constraints prevent straight point to point routing on the system board, then trace-by-trace compensation on the system board will be required to meet the constraints laid out in the Interface Design Guide for end to end trace length variations between different signals.

When using trace-by-trace compensated matching, the system board trace length must compensate for the mismatch in the package trace lengths on a trace-by-trace basis. Effectively, the length of the system board trace must be lengthened or shortened to compensate for short or long traces on the transmitter or receiver package. The following steps would produce this type of trace matching:

1. Gather trace-by-trace length data for both transmitter and receiver packages.
2. Identify the longest system board trace within each clock group. (Use Manhattan distances for approximation.)
3. Route the longest signal (differential pair) so the differential skew specification is met, and determine effective pad-to-pad signal length (adding transmitter and receiver package trace electrical lengths).
4. Assign length rules to each remaining signal trace such that the system board trace length plus the sum of the package trace electrical lengths equals the effective pad-to-pad signal length of the longest signal within the clock group.
5. Route the rest of the clock group.
6. Extract resulting system board trace lengths and add the sum of the package electrical lengths to determine if skew control has been maintained.

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The die pad-to-ball trace length data for the AS90L10208 is included in the AS90L10208 die pad-to-ball trace length information at the end of this document. Similar information for other devices that interface to the AS90L10208 should be available from the respective vendors.

B.2.2 Layout Guidelines

- All signals are ground referenced differential pairs.
- All HyperTransport signals are referenced to V_{SS} or V_{DD} (never to V_{LDT}).
- V_{LDT} = +1.2 V.
- No termination is required on the board. All termination is provided on-die.
- Ideally, all nets in a clock/data group break out on the same layer and route together. If a clock/data group is split between top and bottom routing layers, trace length must be inserted on top layer nets to approximately match the extra delay due to the vias for the bottom layer.
- Decoupling is required in the vicinity of a layer change.
- Routing is to be 20/5/5/5/20 mils for all HyperTransport nets. Route 50/5/5/5/50 mils when serpentining where the 50 mil clearance is any net to itself.
- Group electrical lengths are matched piecewise.

B.2.3 AS90L10208 Board Trace Electrical Specification

- V_{LDT} = 1.2 V ± 60 mV
- Maximum R_{DC} = 0.29 (Ω/in)
- Maximum R_{AC} = 1.50 (Ω/in) @ 1 GHz
- Maximum G_{AC} = 0.32 (S/in) @ 1 GHz
- Z_{OD} = 100Ω ± 10% (90 - 110Ω), (* Z_O can be 50 - 70Ω)
- Bus length vs. frequency:
- 400 Mb/s, 600 Mb/s, 800 Mb/sLength = 1.0 to 24.0 inches
- 1000 Mb/s, 1200 Mb/sLength = 1.0 to 12.0 inches
- 1600 Mb/s Length = 1.0 to 6.0 inches
- T_{PD} = 150 to 170 ps/in
- T_{PD_ODD} = 135 to 155 ps/in

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B.2.4 Routing Rules for Individual Signal Groups

B.2.4.1 CAD_H/L, CTL_H/L, CLK_H/L

- All signals are routed as a differential pair.
- All signals are routed 20/5/5/5/20 mils trace width/spacing.



The actual width/space/width may vary slightly depending on PCB variables such as stack-up and dielectric constant (E_r). The Z_{OD} is the governing factor. Each true signal is routed to within 25 mils of its compliment.

- If the total bus length is longer than 12.00 inches, the majority of the bus must be routed on a single layer.

The complete requirement for length matching and skew compensation is detailed in Table 43.

Table 43: System Board Design Rules

Description		Definition/Parameter	Rules		
1	H to L trace length matching (differential skew) using trace by trace compensation.	Defines the absolute length difference allowed between H and L signal traces. Parameter = DiffPCBskew 400 to 800 MT/s = 20 ps >800 MT/s = 5 ps	Link speed	Microstrip	Stripline
			400 MT/s	133	111
			600 MT/s	133	111
			800 MT/s	133	111
			1000 MT/s	33	28
			1200 MT/s	33	28
			1600 MT/s	33	28
2	CAD/CTL/CLK trace lengths	Defines the minimum and maximum overall trace lengths	Link speed	Min	Max
			400 to 800 MT/s	1 in	24 in
			800 to 1200 MT/s	1 in	12 in
			1600 MT/s	1 in	6 in

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Table 43: System Board Design Rules

Description		Definition/Parameter	Rules		
3	CLK to CAD/CTL trace length matching (CLK centering)	Defines the length difference allowed between the longest and shortest average of H and L for any CAD/CTL signal within a clock group and the average length of H and L for the associated CLK. Parameter = TPCBskew	Link speed	Microstrip	Stripline
			400 MT/s	333	276
			600 MT/s	333	276
			800 MT/s	200	167
			1000 MT/s	133	111
			1200 MT/s	100	84
			1600 MT/s	67	34
4	CAD/CTL to CAD/CTL trace length matching (group skew)	Defines the length difference allowed between the longest and shortest average of H and L for all CAD/CTL signals within a clock group. Parameter = TPCBskewcad	Link speed	Microstrip	Stripline
			400 MT/s	667	555
			600 MT/s	667	555
			800 MT/s	400	333
			1000 MT/s	266	222
			1200 MT/s	200	167
			1600 MT/s	133	111
6	CAD/CTL/CLK trace width (tr) and spacing (sp)	Recommended system board trace width and space. Parameter = Z_O, Z_{OD}	Link speed	Microstrip	Stripline
			400 MT/s	20/5/5/5/20	20/5/5/5/20
			600 MT/s	20/5/5/5/20	20/5/5/5/20

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Table 43: System Board Design Rules

Description		Definition/Parameter	Rules		
			800 MT/s	20/5/5/5/20	20/5/5/5/20
			1000 MT/s	20/5/5/5/20	20/5/5/5/20
			1200 MT/s	20/5/5/5/20	20/5/5/5/20
			1600 MT/s	20/5/5/5/20	20/5/5/5/20
7	CAD/CTL/CLK impedance control and stack up	Recommended dielectric thickness from signal layer to plane layer		Microstrip	Stripline
				4.7	6.0

B.2.4.2 L_POWER_OK, L_RST_N and LDTSTOP_N

Open-drain signals require a pull-up resistor to VDDIO, +2.5V or +3.3 V, depending on the other devices in the HT chain.

B.2.4.3 HyperTransport Trace Referencing to VSS/VDD

- HyperTransport is a ground-referenced differential bus. Differential pairs are weakly coupled and reference V_{SS} more than each other.
- Ideally, all HyperTransport signals reference V_{SS}/V_{DD}.
- If traces cross two reference planes, the plane separation should be 15 mils or less and should use one 0.01 uF 0603 or 0402 ceramic capacitor to bridge the boundary between the planes for every four diff-pairs.
- All signal groups must match the length requirement.

B.2.4.4 HyperTransport Trace Layer Changes

- In general, layer changes are discouraged for bus speeds > 400 Mb/s with the exception of vias for breakout under the package.
- If a clock/data group must change layers, place a pair's vias as close as possible in order to prevent a major Z_{OD} discontinuity. It is all right for the via anti-pad plane clearances to overlap in this instance.
- If a clock/data group is split between top and bottom routing layers, trace length must be inserted on the top layer nets to approximately match the extra delay due to the vias for the bottom layer routing.
- One 0.01 uF 0603 or 0402 ceramic decoupling capacitor is in the vicinity of layer transitions for every four differential pairs to minimize plane bounce.
- All signal groups must match the length requirement.

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B.3 Power Distribution

AS90L10208 power distribution is split into V_{LDT} (+1.2 V for HT PHY), V_{CORE} (+1.8 V for the core), V_{ANALOG} (+1.8 V for the PLL circuitry), and VDDIO (+3.3 V for the I/O).

- V_{ANALOG} should be derived from V_{CORE} using a ferrite bead.
- V_{CORE} should be supplied from a dedicated plane or an island in the power plane.
- V_{ANALOG} and VDDIO should be supplied from a dedicated island located close to the pins supplied by it.

HyperTransport supports a very high data-rate transaction. Careful design practices must be exercised to ensure a low DC and AC impedance path from the regulator that supplies V_{LDT}.

V_{LDT} to each HT link must be delivered by an independent interconnect in order to provide maximum isolation between the individual links. This will minimize the high frequency noise on the individual HyperTransport supply due to the switching of high data-rate signals on other HyperTransport links. AS90L10208 has dedicated V_{LDT} pins for each of its two, HyperTransport ports. It is recommended that a separate regulator be used for each port and that power is supplied from a dedicated island for each V_{LDT} in the power plane. Detailed information on V_{LDT} layout is provided in the following sections.

B.3.1 Number of Layers

The number of layers on the board dictates if V_{LDT} is routed on the board as a trace or as section of a plane. A larger number of layers alleviates some of the signal routing constraints allowing for placing a greater number of discrete decoupling capacitors closer to the AS90L10208 packages or on the back of the board. Ideally, power should be supplied from a dedicated island for each V_{LDT} in the power plane.

B.3.2 VLDT Layout

Regardless of the number of layers in the board, the HyperTransport voltage regulator should be as close to the AS90L10208 package as possible. The maximum recommended distance is 1.5 to 2.0 inches. If possible, a section of a plane on one of the inner signal layers should be used to deliver V_{LDT} to AS90L10208, as is done with 6- or 8-layer motherboards. This plane should be large enough to accommodate the placement of all V_{LDT} regulator components and to make connections to every V_{LDT} ball on the AS90L10208 package. The plane should be subdivided into islands, with each island used to supply an individual link.

If a V_{LDT} plane is not available, the minimum width of the trace should be 0.2 inches or greater whenever possible.

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B.3.3 Decoupling

The use of decoupling capacitors on the board is recommended. They should be placed as close to the package as possible without interfering with the signal routing. This can be implemented with an array of 0603 or 0402-size capacitors. If the application permits, the capacitors should be mounted on the back of the board directly under the package.

The best way to select the number of capacitors and their values is through SPICE simulations, if the circuit model for the power delivery system is available. If the circuit model is not available, the following guidelines should be used for component selection. There should be at least eight ceramic capacitors to ground of 0.01 uF or 0.1 uF capacitance - one for each V_{LDT} power pin. All capacitors should be of X7R dielectric or better.

B.3.4 Bulk Decoupling

Proper bulk decoupling is required for stable operation of the regulator and to ensure low-power delivery system impedance at low frequencies. It is recommended that low-ESR ceramic (X5R dielectric or better), OsCon, or aluminum polymer type capacitors be used for bulk decoupling.

B.3.5 Multiple HyperTransport Links

A single V_{LDT} regulator can be used to supply power to two HyperTransport links. The distance from the regulator to the AS90L10208 package should not exceed 1.5 to 2.0 inches. This scheme is recommended only for applications where board space is constrained so much that it is impossible to accommodate individual regulators for each port.

It is important to note that although a single voltage regulator can be used to feed two independent HyperTransport links, the board routing must consist of two separate traces leading from the regulator to the package. The traces should be 0.2 inches wide and should run separately for a minimum length of at least 1.0 inch. The minimum spacing between them should not be less than 0.1 inch. If these layout recommendations are not followed, significant coupling can be expected between the V_{LDT} links if they are connected to the same regulator. Regardless of which feeding scheme is used to deliver the power to the AS90L10208, it is recommended that decoupling capacitors be placed at the point where the traces connect to the AS90L10208.

Please note that it is not recommended that a single voltage regulator be used to feed more than two HyperTransport links in any application.

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B.4 AS90L10208 Die Pad-to-Ball Trace Length Information

Table 44 shows the pad-to-ball trace length inside the AS90L10208 package, in both millimeters and inches, for the HyperTransport differential signals. For convenience, the pad-to-ball propagation delay is also included. The propagation delay for each signal is 10 ps/mm.

Table 44: Pad-to-Ball Trace Length Information

Ball number	Signal Name	Pad to Ball Trace Length [mm]	Pad to Ball Trace Length [inches]	Pad to Ball Trace Propagation Delay [ps]
R1	L0_TX_CAD_H[7]	9.665	0.3805	96.65
P1	L0_TX_CAD_L[7]	9.660	0.3803	96.60
T2	L0_TX_CAD_H[6]	8.198	0.3227	81.98
T3	L0_TX_CAD_L[6]	8.342	0.3284	83.42
U1	L0_TX_CAD_H[5]	10.041	0.3953	100.41
T1	L0_TX_CAD_L[5]	10.004	0.3939	100.04
U2	L0_TX_CAD_H[4]	8.915	0.3510	89.15
U3	L0_TX_CAD_L[4]	8.861	0.3489	88.61
V2	L0_TX_CAD_H[3]	8.847	0.3483	88.47
V3	L0_TX_CAD_L[3]	8.607	0.3389	86.07
AA1	L0_TX_CAD_H[2]	11.856	0.4668	118.56
Y1	L0_TX_CAD_L[2]	11.819	0.4653	118.19
Y3	L0_TX_CAD_H[1]	9.150	0.3602	91.50
W3	L0_TX_CAD_L[1]	9.324	0.3671	93.24
AA2	L0_TX_CAD_H[0]	10.667	0.4203	106.77
Y2	L0_TX_CAD_L[0]	10.460	0.4118	104.60
W1	L0_TX_CLK_H	10.950	0.4311	109.50
V1	L0_TX_CLK_L	10.942	0.4308	109.42
P2	L0_TX_CTL_H	7.622	0.3001	76.22
P3	L0_TX_CTL_L	7.628	0.3003	76.28
M3	L0_RX_CAD_H[7]	7.591	0.2989	75.91
M2	L0_RX_CAD_L[7]	7.478	0.2944	74.78

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Table 44: Pad-to-Ball Trace Length Information

Ball number	Signal Name	Pad to Ball Trace Length [mm]	Pad to Ball Trace Length [inches]	Pad to Ball Trace Propagation Delay [ps]
K1	L0_RX_CAD_H[6]	10.061	0.3961	100.61
L1	L0_RX_CAD_L[6]	9.954	0.3919	99.54
K3	L0_RX_CAD_H[5]	7.957	0.3133	79.57
K2	L0_RX_CAD_L[5]	8.044	0.3167	80.44
H1	L0_RX_CAD_H[4]	10.806	0.4254	108.06
J1	L0_RX_CAD_L[4]	10.825	0.4262	108.25
H3	L0_RX_CAD_H[3]	8.634	0.3399	86.34
H2	L0_RX_CAD_L[3]	8.581	0.3378	85.81
G3	L0_RX_CAD_H[2]	11.060	0.4354	110.60
G2	L0_RX_CAD_L[2]	11.092	0.4367	110.92
F1	L0_RX_CAD_H[1]	11.691	0.4603	116.91
G1	L0_RX_CAD_L[1]	11.751	0.4627	117.51
F3	L0_RX_CAD_H[0]	9.897	0.3897	98.97
F2	L0_RX_CAD_L[0]	9.910	0.3902	99.10
J3	L0_RX_CLK_H	8.242	0.3245	82.42
J2	L0_RX_CLK_L	8.293	0.3265	82.93
M1	L0_RX_CTL_H	8.785	0.3459	87.85
N1	L0_RX_CTL_L	8.715	0.3431	87.15
M26	L1_TX_CAD_H[7]	9.720	0.3827	97.20
N26	L1_TX_CAD_L[7]	9.809	0.3862	98.09
L25	L1_TX_CAD_H[6]	8.286	0.3262	82.86
L24	L1_TX_CAD_L[6]	8.199	0.3228	81.99
K26	L1_TX_CAD_H[5]	10.078	0.3968	100.78
L26	L1_TX_CAD_L[5]	10.161	0.4000	101.61
K25	L1_TX_CAD_H[4]	8.387	0.3302	83.87
K24	L1_TX_CAD_L[4]	8.293	0.3265	82.93

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Table 44: Pad-to-Ball Trace Length Information

Ball number	Signal Name	Pad to Ball Trace Length [mm]	Pad to Ball Trace Length [inches]	Pad to Ball Trace Propagation Delay [ps]
J25	L1_TX_CAD_H[3]	8.956	0.3526	89.56
J24	L1_TX_CAD_L[3]	8.943	0.3521	89.43
F26	L1_TX_CAD_H[2]	11.833	0.4659	118.33
G26	L1_TX_CAD_L[2]	11.693	0.4603	116.93
G24	L1_TX_CAD_H[1]	8.977	0.3534	89.77
H24	L1_TX_CAD_L[1]	9.017	0.3550	90.17
F25	L1_TX_CAD_H[0]	10.331	0.4067	103.31
G25	L1_TX_CAD_L[0]	10.216	0.4022	102.16
H26	L1_TX_CLK_H	11.083	0.4363	110.83
G26	L1_TX_CLK_L	10.950	0.4311	109.50
N25	L1_TX_CTL_H	7.640	0.3008	76.40
N24	L1_TX_CTL_L	7.719	0.3039	77.19
R24	L1_RX_CAD_H[7]	7.636	0.3006	76.36
R25	L1_RX_CAD_L[7]	8.136	0.3203	81.36
U26	L1_RX_CAD_H[6]	10.046	0.3955	100.46
T26	L1_RX_CAD_L[6]	9.933	0.3911	99.33
U24	L1_RX_CAD_H[5]	8.778	0.3456	87.78
U25	L1_RX_CAD_L[5]	8.865	0.3490	88.65
W26	L1_RX_CAD_H[4]	10.925	0.4301	109.25
V26	L1_RX_CAD_L[4]	10.742	0.4229	107.42
W24	L1_RX_CAD_H[3]	8.886	0.3499	88.86
W25	L1_RX_CAD_L[3]	8.828	0.3475	88.28
Y24	L1_RX_CAD_H[2]	9.729	0.3830	97.29
Y25	L1_RX_CAD_L[2]	9.794	0.3856	97.94
AA26	L1_RX_CAD_H[1]	10.787	0.4247	107.87
Y26	L1_RX_CAD_L[1]	10.917	0.4298	109.17

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Table 44: Pad-to-Ball Trace Length Information

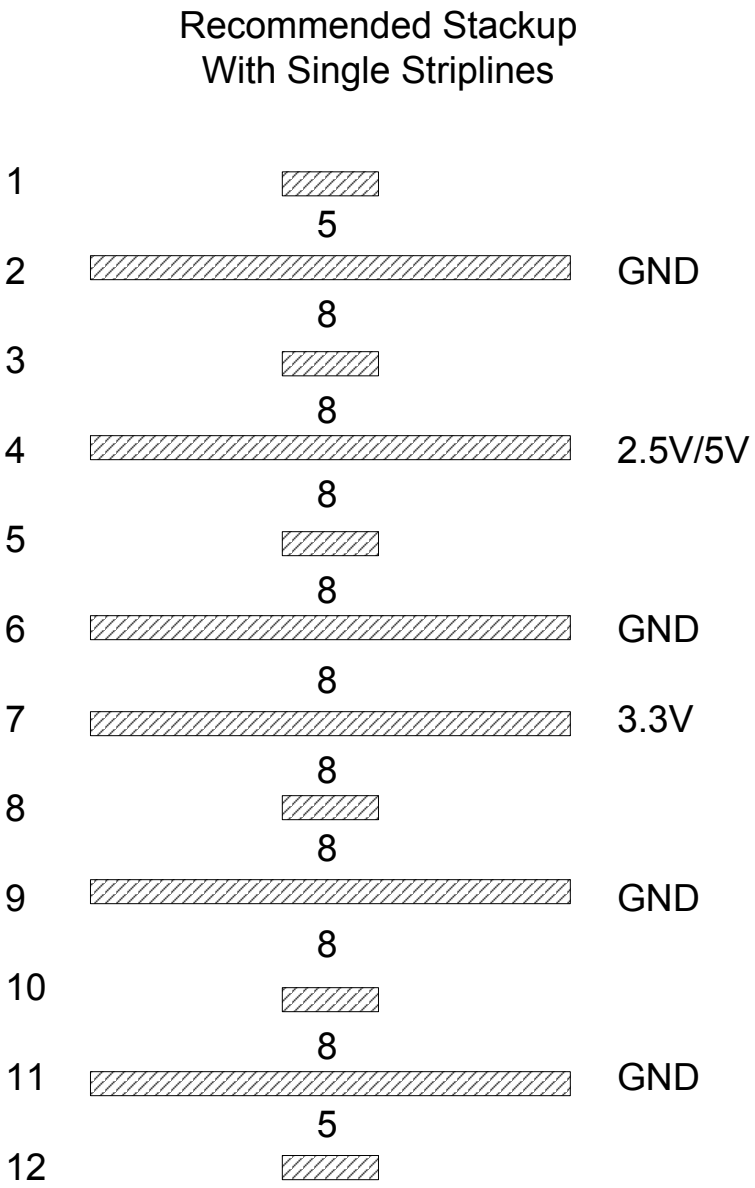
Ball number	Signal Name	Pad to Ball Trace Length [mm]	Pad to Ball Trace Length [inches]	Pad to Ball Trace Propagation Delay [ps]
AA24	L1_RX_CAD_H[0]	10.029	0.3948	100.29
AA25	L1_RX_CAD_L[0]	9.797	0.3857	97.97
V24	L1_RX_CLK_H	8.544	0.3364	85.44
V25	L1_RX_CLK_L	8.587	0.3381	85.87
R26	L1_RX_CTL_H	9.514	0.3746	95.14
P26	L1_RX_CTL_L	9.356	0.3684	93.56

B.5 Example PCB Stackup for HyperTransport

The following example PCB stack-up will provide a 60-ohm single-ended impedance or a 100-ohm differential impedance if a 5 mil wide trace is used with 5 mil spacing on any signal layer.

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Figure 23: PCB Stackup for HyperTransport



Notes on the Stackup Design:

1. The stackup is based on 5 mil nominal trace width on both internal and external layers.
2. Impedance is nominally 60Ω with the dielectrics shown. All internal signal layers are ½ oz copper.
3. All internal reference planes are 1 oz copper.
4. Overall board thickness is 91.6 mils measured between outer resin surfaces.

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C. Ordering Information

The following table contains ordering information for the Tsi308.

Table 45: Ordering Information

Part Number	Temperature	Package	Pin Count
Tsi308-600CE	Commercial	BGA	388
Tsi308-600CEV	Commercial	BGA (RoHS)	388

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