IDT® Tsi577
Serial RapidIO Switch

Hardware Manual

May 18, 2012

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About this Document

This section discusses general document information about the *Serial RapidIO Switch*. The following topics are described:

- "Scope" on page 5
- "Document Conventions" on page 5
- "Revision History" on page 7

Scope

The *Tsi577 Hardware Manual* discusses electrical, physical, and board layout information for the Tsi577. It is intended for hardware engineers who are designing system interconnect applications with these devices.

Document Conventions

This document uses a variety of conventions to establish consistency and to help you quickly locate information of interest. These conventions are briefly discussed in the following sections.

Non-differential Signal Notation

Non-differential signals are either active-low or active-high. An active-low signal has an active state of logic 0 (or the lower voltage level), and is denoted by a lowercase "b". An active-high signal has an active state of logic 1 (or the higher voltage level), and is not denoted by a special character. The following table illustrates the non-differential signal naming convention.

State	Single-line signal	Multi-line signal
Active low	NAME_b	NAMEn[3]
Active high	NAME	NAME[3]

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Differential Signal Notation

Differential signals consist of pairs of complement positive and negative signals that are measured at the same time to determine a signal's active or inactive state (they are denoted by "_p" and "_n", respectively). The following table illustrates the differential signal naming convention.

State	Single-line signal	Multi-line signal
Inactive	NAME_p = 0 NAME_n = 1	NAME_p[3] = 0 NAME_n[3] =1
Active	NAME_p = 1 NAME_n = 0	NAME_p[3] is 1 NAME_n[3] is 0

Symbols



This symbol indicates a basic design concept or information considered helpful.



This symbol indicates important configuration information or suggestions.



This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

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Revision History

May 18, 2012, Formal

- Updated the first paragraph in “Power Sequencing” on page 35
- Added Figure 38 (Analyzer Probe Footprint)

November 18, 2010, Formal

Added a note to Table 13

August 2009, Formal

There have been no technical changes to this document. The formatting has been updated to reflect IDT.

June 2009, Formal

There have been changes throughout the document.

September 2008, Advance

- Updated Table 8 on page 32 with new Tsi577 operating conditions

August 2008, Advance

- Updated Table 5 on page 29 with new Tsi577 thermal characteristics
- Updated Table 6 on page 29 with new simulated junction to ambient characteristics

August 2008, Advance

Although changes occurred throughout this document, the majority of changes were in “Signals and Package” on page 11.

June 2008, Advance

This was the first version of this document.

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Bibliography

1	*RapidIO Interconnect Specification (Revision 1.3)*	This specification explains RapidIO's logical layer, common transport layer, and physical layer protocol and packet formats. It also describes overall inter-operability requirements for the RapidIO protocol. For more information, see www.rapidio.org.
2	Enhancements to the RapidIO AC Specification	This document contains the AC specifications for the RapidIO physical layer.
3	ANSI/TIA/EIA-644-1995, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, March 1996.	This documents the LVDS electrical characteristics.
4	I^2C Specification	This specification defines the standard I2C bus interface, including specifications for all the enhancements. For more information, see www.semiconductors.philips.com document number: 9398 393 40011
5	High-Speed Digital System Design	Hall,Stephen H.,Garret W. Hall & James A. McCall, ©2000 John Wiley & Sons inc. ISBN 0-471-36090-2
6	*High-Speed Digital Design*	Johnson, Howard, Martin Graham ©1993 Prentice-Hall inc. ISBN 0-13-395724-1
7	*High Performance Printed Circuit Boards*	Harper, Charles A. ©1999 McGraw-Hill ISBN 0-07-026713-8
8	Transmission Line *RAPIDESIGNER*©	Application Note 905 ©1996 National Semiconductor Corp. Lit # 100905-002 & 633201-001
9	*High Speed PCB Design*	Ritchey, Lee W., James C. Blankenhorn ©1993 SMT Plus Inc., and Ritch Tech
10	Design Guidelines for Electronic Packaging *Utilizing High Speed Techniques*	The Institute for Interconnecting and Packaging Electronic Circuits ©1999 IPC Document # IPC-D-317A

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11	*High Speed Signal Propagation*	Johnson, Howard, Martin Graham ©2003 Prentice-Hall inc. ISBN 0-13-084408-X
12	*High Speed Digital Design and PCB Layout*	Hanson, Robert J. ©AmeriCom Test & SMT Technology Inc.
13	*1-10 GBps Serial Interconnect Requirements*	Solving High Speed Serial Design Challenges ©2004Xilinx
14	*10GBps Serial Backplanes Using Virtex-II Pro X*	Solving High Speed Serial Design Challenges ©2004Xilinx
15	*Designing Controlled-impedance Vias*	Thomas Neu, EDN magazine, October 2 2003
16	*Computer Circuits Electrical Design, First Edition,*	Ron K. Poon Prentice-Hall, Inc., 1995

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1. Signals and Package

This chapter describes the packaging (mechanical) features for the Tsi577. It includes the following information:

- "Signals" on page 11
- "Pinlist and Ballmap" on page 25
- "Package Characteristics" on page 26
- "Thermal Characteristics" on page 29

1.1 Signals

The following conventions are used in the signal description table:

- Signals with the suffix "_p" are the positive half of a differential pair.
- Signals with the suffix "_n" are the negative half of a differential pair.
- Signals with the suffix "_b" are active low.

Signals are classified according to the types defined in Table 1.

Table 1: Signal Types

Pin Type	Definition
I	Input
O	Output
I/O	Input/Output
OD	Open Drain
SRIO	Differential driver/receiver defined by *RapidIO Interconnect Specification (Revision 1.3)*
PU	Pulled Up internal to the Tsi577
PD	Pulled Down internal to the Tsi577
LVTTL	CMOS I/O with LVTTL thresholds
CML	Current Mode Logic - Defined by *RapidIO Interconnect Specification (Revision 1.3)*

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Table 1: Signal Types (Continued)

Pin Type	Definition
Hyst	Hysteresis
Core Power	Core supply
Core Ground	Ground for core logic
I/O Power	I/O supply
N/C	No connect These signals must be left unconnected.

1.1.1 Endian Ordering

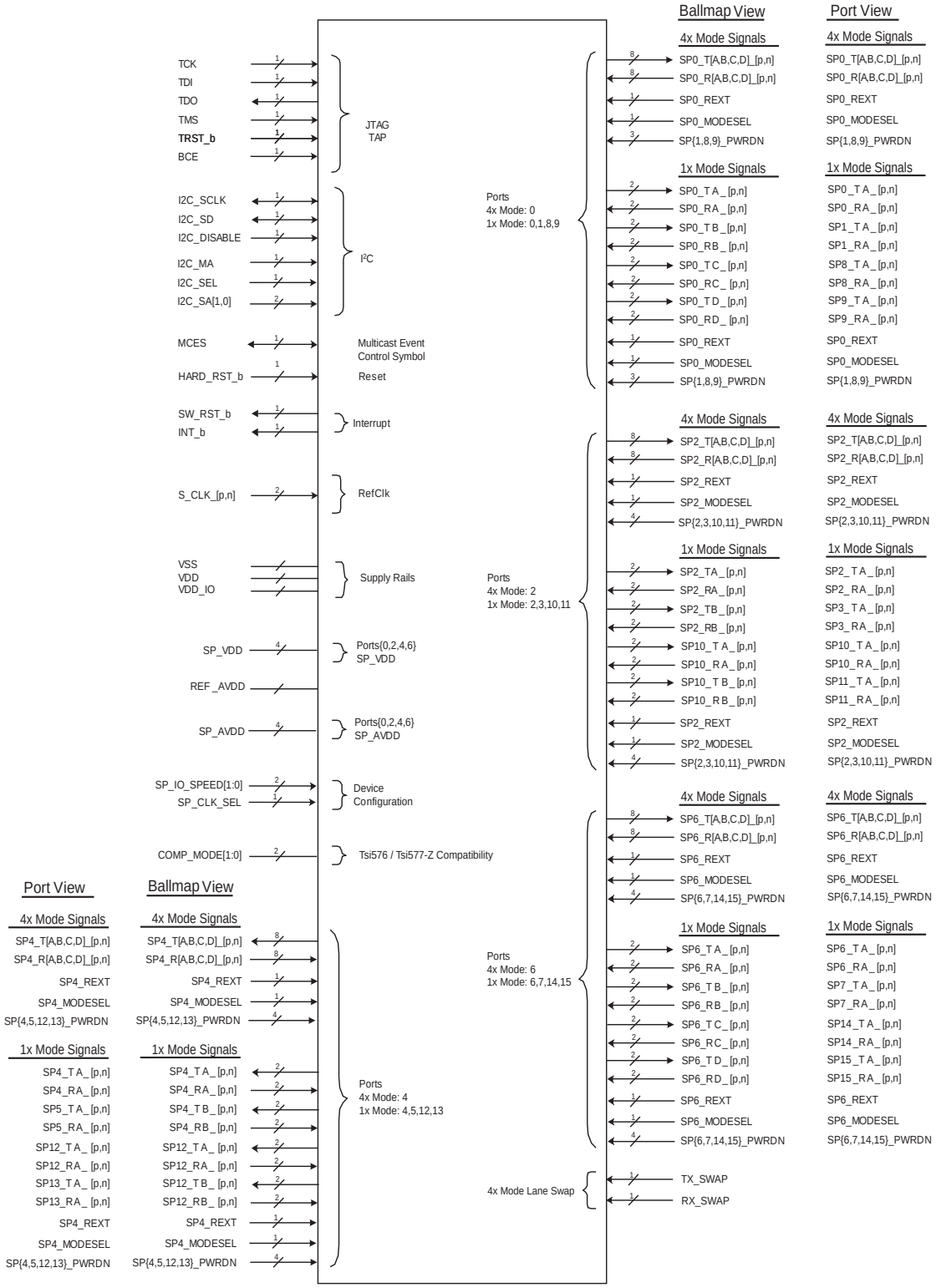
This document follows the bit-numbering convention adopted by *RapidIO Interconnect Specification (Revision 1.3)*, where [0:7] is used to represent an 8 bit bus with bit 0 as the most-significant bit.

1.1.2 Signal Grouping

Figure 1 shows two views of the signals: the ball map view and the port view. The ball map view shows the pins as they are named in the Tsi577 ball map. The port view shows the signals on the same balls that are configuration dependent.

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Figure 1: Signal Groupings



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The signals shown in Table 2 are described using the port view information (4x mode) in Figure 1. The ball map view in the figure is to show compatibility with the Tsi576 and Tsi577-Z devices.

Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
PORT n = 1x/4x Mode Serial RapidIO **PORT m = 1x Mode Serial RapidIO** **n = 0, 2, 4, 6** **m = n+1, n+8, n+9 for each value of n**			
Serial Port Transmit			
SP{n}_TA_p	O, SRIO	Port n Lane A Differential Non-inverting Transmit Data output (4x mode) Port n Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TA_n	O, SRIO	Port n Lane A Differential Inverting Transmit Data output (4x mode) Port n Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_p	O, SRIO	Port n Lane B Differential Non-inverting Transmit Data output (4x mode) Port m (=n+1) Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TB_n	O, SRIO	Port n Lane B Differential Inverting Transmit Data output (4x mode) Port m (=n+1) Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TC_p	O, SRIO	Port n Lane C Differential Non-inverting Transmit Data output (4x mode) Port m (=n+8) Differential Non-inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TC_n	O, SRIO	Port n Lane C Differential Inverting Transmit Data output (4x mode) Port m (=n+8) Differential Inverting Transmit Data output (1x mode)	No termination required.
SP{n}_TD_p	O, SRIO	Port n Lane D Differential Non-inverting Transmit Data output (4x mode) Port m (=n+9) Differential Non-inverting Transmit Data output (1x mode)	No termination required.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP{n}_TD_n	O, SRIO	Port n Lane D Differential Inverting Transmit Data output (4x mode) Port m (=n+9) Differential Inverting Transmit Data output (1x mode)	No termination required.
Serial Port Receive			
SP{n}_RA_p	I, SRIO	Port n Lane A Differential Non-inverting Receive Data input (4x node) Port n Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RA_n	I, SRIO	Port n Lane A Differential Inverting Receive Data input (4x mode) Port n Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_p	I, SRIO	Port n Lane B Differential Non-inverting Receive Data input (4x mode) Port m (=n+1) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RB_n	I, SRIO	Port n Lane B Differential Inverting Receive Data input (4x mode) Port m (=n+1) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RC_p	I, SRIO	Port n Lane C Differential Non-inverting Receive Data input (4x mode) Port m (=n+8) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RC_n	I, SRIO	Port n Lane C Differential Inverting Receive Data input (4x mode) Port m (=n+8) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RD_p	I, SRIO	Port n Lane D Differential Non-inverting Receive Data input (4x mode) Port m (=n+9) Differential Non-inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series
SP{n}_RD_n	I, SRIO	Port n Lane D Differential Inverting Receive Data input (4x mode) Port m (=n+9) Differential Inverting Receive Data input (1x mode)	DC blocking capacitor of 0.1uF in series

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Serial Port Configuration			
SP{n}_REXT	I	Used to connect a resistor to VSS to provide a reference current for the driver and equalization circuits.	Series resistor of 191Ω (1%) connected to VSS.
SPn_MODESEL (PWRUP)	I/O, LVTTL, PD	Selects the operating mode for all four serial ports within a given MAC n (n = {0,2,4,6}) 0 = MAC n operating in 4x+0x+0x+0x mode as described in section "4x + 0x + 0x + 0x Configuration" on page 77 1 = MAC n operating in 1x+1x+1x+1x mode as described in section "1x + 1x + 1x + 1x Configuration" on page 77 Note: The MAC_MODE in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407 overrides and determine the operating mode for the corresponding ports. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP{n}_PWRDN (PWRUP)	I/O, LVTTL, PU	Port n Transmit and Receive Power Down Control (where n = {2, 4, 6}) This signal controls the state of Port n inside a given MAC n. If Port n is in 4X mode, then the SPn_PWRDN controls the state of all four lanes (A/B/C/D) of SerDes Macro. If Port n is in 1X mode, related port m are controlled by SPm_PWRDN. If SPn_PWRDN is set and all three other ports in the same given MACn have their SPm_PWRDN set, then the given MACn SERDES is also powered down. When n=x, the related m ports are (x+1, x+8, x+9). 0 = Port n Powered Up 1 = Port n Powered Down Override SP{n}_PWRDN using PWDN_X4 field in the “SRIO MAC x Digital Loopback and Clock Selection Register” on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.
SP{m}_PWRDN (PWRUP)	I/O, LVTTL, PU	Port m Transmit and Receive Power Down Control (where m= {1, 3, 5, 7,8,9,10,11,12,13,14,15}) This signal controls the state of Port m. Note that Port m is never used when 4x mode is selected for a Serial Rapid I/O MAC, and it can be powered down. 0 = Port m Powered Up 1 = Port m Powered Down If SPn is in 1X mode and SPn_PWRDN is set and all three other ports in the same given MACn have their SPm_PWRDN set, then the given MACn SERDES is also powered down. Override SP{m}_PWRDN using PWDN_X1/X4 field in the “SRIO MAC x Digital Loopback and Clock Selection Register” on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
COMP_MODE[1:0] (PWRUP)	I, LVTTL, {PU, PD}	Tsi577 Compatibility Modes These signals are for backward compatibility with existing devices 00 = Tsi577-Z Replacement (16*1X ports) 01 = Tsi576 Replacement (2*4X + 8*1X) 10 = Tsi577 (default) 11 = Reserved For further detail refer to "Tsi577 Compatibility Modes" on page 25.	Pin must be tied off according to the required configuration. Either a 10K pull up to VDD_IO or a 10K pull-down to VSS. Internal pull-up/pull-down may be used for default setting of 2'b10
Serial Port Speed Select			
SP_IO_SPEED[1] (PWRUP)	I/O, LVTTL, PU	Serial Port Transmit and Receive operating frequency select. SP_IO_SPEED[1:0], these pin select the power-up serial port frequency for *all* ports. 00 = 1.25Gbit/s 01 = 2.5Gbit/s 10 = 3.125Gbit/s (default) 11 = Illegal Note; The SP_IO_SPEED[1:0] setting is equal to theIO_SPEED field in the "SRIO MAC x Digital Loopback and Clock Selection Register" on page 407. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-up may be used for logic 1.
SP_IO_SPEED[0] (PWRUP)	I/O, LVTTL, PD	See SP_IO_SPEED[1]	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
SP_CLK_SEL (PWRUP)	I/O, LVTTL, PD	Reference clock speed 1 = 125-MHz Reference clock 0 = 156.25-MHz Reference clock This signal configures the MPLL settings for the RapidIO SerDes. Output capability of this pin is only used in test mode.	Pin must be tied off according to the required configuration. Either a 10K pull-up to VDD_IO or a 10K pull-down to VSS. Internal pull-down may be used for logic 0.
Serial Port Lane Ordering Select			
SP_RX_SWAP (PWRUP)	I, LVTTL, PD	Configures the order of 4X receive/transmit lanes on serial ports. 0 = A, B, C, D 1 = D, C, B, A Override SP_RX(TX)_SWAP usingSWAP_RX(TX) field in the “SRIO MAC x Digital Loopback and Clock Selection Register” on page 407. This signal is ignored in 1X mode. Note: Ports that require the use of lane swapping for ease of routing will only function as 4x mode ports. The re-configuration of a swapped port to dual 1x mode operation results in the inability to connect to a 1x mode link partner.	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS through a 10K resistor if an external pull-down is desired.
SP_TX_SWAP (PWRUP)	I, LVTTL, PD	See SP_RX_SWAP	No termination required. Internal pull-down can be used for logic 0. Pull up to VDD_IO through 10K if external pull-up is desired. Pull down to VSS through 10K resistor if an external pull-down is desired.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Clock and Reset			
S_CLK_p	I, CML	Differential non-inverting reference clock. The clock is used for following purposes: SERDES reference clock, serial port system clock, ISF clock and test clock. The clock frequency is defined in the Minimum Clock Frequency Requirements section. The maximum frequency of this input clock is 156.25 MHz.	AC coupling capacitor of 0.1uF required.
S_CLK_n	I, CML		
HARD_RST_b	I LVTTL, Hyst, PU	Schmidt-triggered hard reset. Asynchronous active low reset for the entire device. The Tsi577 does not contain a voltage detector to generate internal reset.	Connect to a power-up reset source. See “Reset Requirements” on page 66 for more detail.
Interrupts			
INT_b	O, OD, LVTTL, 2mA	Interrupt signal (open drain output)	External pull-up required. Pull up to VDD_IO through a 10K resistor.
SW_RST_b	O, OD, LVTTL, 2mA	Software reset (open drain output): This signal is asserted when a RapidIO port receives a valid reset request on a RapidIO link. If self-reset is not selected, this pin remains asserted until the reset request is cleared from the status registers. If self-reset is selected, this pin remains asserted until the self reset is complete. If the Tsi577 is reset from the HARD_RST_b pin, this pin is de-asserted and remains de-asserted after HARD_RST_b is released. For more information, refer to “Resets” in the Tsi577 User’s Manual.	External pull-up required. Pull up to VDD_IO through a 10K resistor.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Miscellaneous			
Multicast			
MCES	I/O, LVTTL, PD	Multicast Event Symbol pin. As an input, an edge (rising or falling) will trigger a Multicast Event Control Symbol to be sent to all enabled ports. As an output, this pin will toggle its value every time an Multicast Event Control Symbol is received by any port which is enabled for Multicast event control symbols. Refer to section "Multicast-Event Control Symbols" on page 58 for further details.	No termination required. This pin must not be driven by an external source until all power supply rails are stable.
I^2C			
I2C_SCLK	I/O, OD, LVTTL, PU 8mA	I^2C clock, up to 100 kHz. This clock signal must be connected to the clock of the serial EEPROM on the I^2C bus.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate is required.
I2C_SD	I/O, OD, LVTTL, PU 8mA	I^2C input and output data bus (bidirectional open drain)	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through a minimum 470 ohms resistor if higher edge rate required.
I2C_DISABLE (PWRUP)	I, LVTTL, PD	Disable I^2C register loading after reset. When asserted, the Tsi577 will not attempt to load register values from I^2C.	No termination required.Pull up to VDD_IO through a 10K resistor if I^2C loading is not required.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
I2C_MA (PWRUP)	I, LVTTL, PU	I^2C Multibyte Address When driven high, I^2C module expects multi-byte peripheral addressing; otherwise, when driven low, single-byte peripheral address is assumed. The value on this pin, sets the PA_SIZE field in "I2C Master Configuration Register" on page 476 and PSIZE field in "I2C Boot Control Register" on page 496.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
I2C_SA[1:0] (PWRUP)	I, LVTTL, {PU, PU}	I^2C Slave Address pins The values on these two pins represent the values for the lower 2 bits of the 7-bit address of Tsi577 when acting as an I^2C slave (field SLV_ADDR in "I2C Slave Configuration Register" on page 493). These pins with I2C_SEL is also used to update the lower 2 bits of the 7-bit address of the EEPROM address it boots from (field BOOT_ADDR in "I2C Boot Control Register" on page 496) and to access an external slave (field DEV_ADDR in "I2C Master Configuration Register" on page 476).	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
I2C_SEL (PWRUP)	I, LVTTL, PU	I^2C Pin Select Together with the I2C_SA[1:0] pins, Tsi577 determines the lower 2 bits of the 7-bit address of the EEPROM address it boots from. When asserted, the I2C_SA[1:0] values are also used as the lower 2 bits of the EEPROM address. When de-asserted, the I2C_SA[1:0] pins are ignored and the lower 2 bits of the EEPROM address default to 00.	No termination required. Internal pull-up may be used for logic 1. Pull up to VDD_IO through 10K resistor if an external pull-up is desired. Pull down to VSS to change the logic state.
JTAG TAP Controller			
TCK	I, LVTTL, PD	IEEE 1149.1 Test Access Port Clock input	Pull up to VDD_IO through 10K resistor if not used.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
TDI	I, LVTTL, PU	IEEE 1149.1 Test Access Port Serial Data Input	Pull up to VDD_IO through a 10K resistor if the signal is not used or a if higher edge rate is required.
TDO	O, LVTTL, 8mA	IEEE 1149.1 Test Access Port Serial Data Output	No connect if JTAG is not used. Pull up to VDD_IO through a 10K resistor if used.
TMS	I, LVTTL, PU	IEEE 1149.1 Test Access Port Test Mode Select	Pull up to VDD_IO through a 10K resistor if not used.
TRST_b	I, LVTTL, PU	IEEE 1149.1 Test Access Port TAP Reset Input This input must be asserted during the assertion of HARD-RST_b. Afterwards, it may be left in either state. Combine the HARD_RST_b and TRST_b signals with an AND gate and use the output to drive the TRST_b pin.	Tie to VSS through a 10K resistor if not used.
BCE	I, LVTTL, PU	Boundary Scan compatibility enabled pin. This input is used to aid 1149.6 testing. This signal also enables system level diagnostic capability using features built into the SerDes. This signal must be tied to VDD_IO during normal operation of the device, and during JTAG accesses of the device registers	This signal should have the capability to be pulled-up or pulled-low. • The default setting is to be pulled-up. • Pulling the signal low enables the signal analyzer functionality on the SerDes • A 10K resistor to VDD_IO should be used.
Power Supplies			
SP_AVDD	-	3.3V supply for bias generator circuitry. This is required to be a low-noise supply.	Refer to “Decoupling Requirements” on page 59.
REF_AVDD	-	Analog 1.2V for Reference Clock (S_CLK_P/N). Clock distribution network power supply.	Refer to “Decoupling Requirements” on page 59.

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Table 2: Signal Descriptions and Recommended Termination

Pin Name	Type	Description	Recommended Termination[a]
Common Supply			
VDD_IO	-	Common 3.3V supply for LVTTL I/O	Refer to "Decoupling Requirements" on page 59.
VSS	-	Common ground supply for digital logic	Refer to "Decoupling Requirements" on page 59.
VDD	-	Common 1.2V supply for digital logic	Refer to "Decoupling Requirements" on page 59.
SP_VDD	-	1.2V supply for CDR, Tx/Rx, and digital logic for all RapidIO ports	Refer to "Decoupling Requirements" on page 59.

a. Signals for unused serial ports do not require termination and can be left as N/Cs.

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1.1.3 Tsi577 Compatibility Modes

Table 3 lists the different COMP_MODE[1:0] pin configurations which allow backward pin and software compatibility with the Tsi576 and Tsi577-Z devices.

- When Tsi577 is placed in a Tsi577-Z socket, COMP_MODE is automatically set to 00. The device powers up with all ports (0..15) in x1.
- When Tsi577 is placed in a Tsi576 socket, COMP_MODE is automatically set to 01
  - The Tsi577 powers up with ports 0 and 6 in 4x mode and ports 2 -> 5, 10 -> 13 in 1x mode (2*x4 + 8*x1). In this case, the maximum 1x mode ports is 12.
- The default mode for Tsi577 is 10.
  - Ports 0, 2, 4, 6 can be 4x mode or all 16 ports (0..15) can be 1x mode.

Table 3: Tsi577 Compatibility Modes

Device ID	COMP_MODE[1:0]	Max Number of Ports		Port Total	Description
0x577	00	4x mode	0	16	Tsi577-Z Replacement
		1x mode	16		
0x577	01	4x mode	2	16	Tsi576 Replacement
		1x mode	12		
0x577	10	4x mode	4	16	Tsi577 Mode (default)
		1x mode	16		
0x577	11	Reserved			

1.2 Pinlist and Ballmap

The pinlist and ballmap information for the Tsi577 are available by visiting www.IDT.com and registering. For more information, see the following documents:

- *Tsi577 Pinlist*
- *Tsi577 Ballmap*

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1.3 Package Characteristics

The Tsi577's package characteristics are summarized in the following table. Figure 2 and Figure 3 illustrate the Top and Side views of the Tsi577 package. Figure 4 shows the Bottom view of the device.

Table 4: Package Characteristics

Feature	Description
Package Type	Heat Slug Ball Grid Array (HSBGA)
Package Body Size	21 mm x 21 mm
JEDEC Specification	95-1 Section 14
Pitch	1.00 mm
Ball pad size	500 um
Soldermask opening	400 um
Moisture Sensitivity Level	3

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Figure 2: Package - Top View

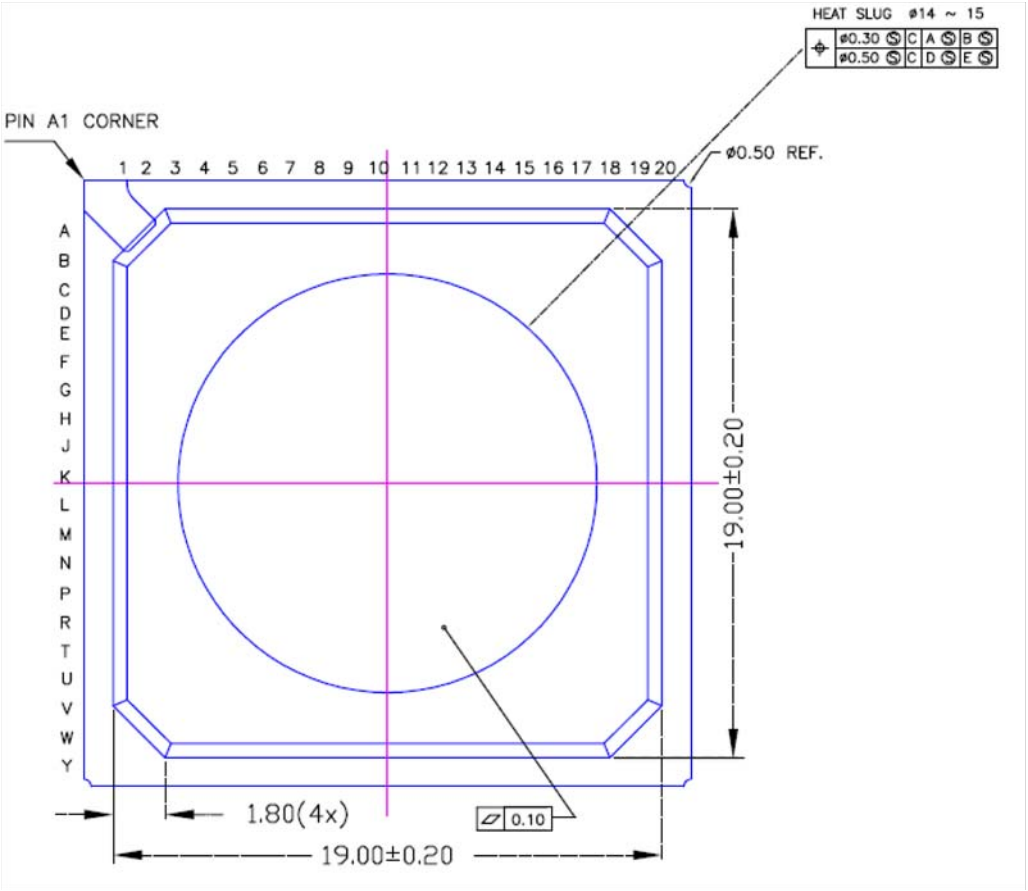
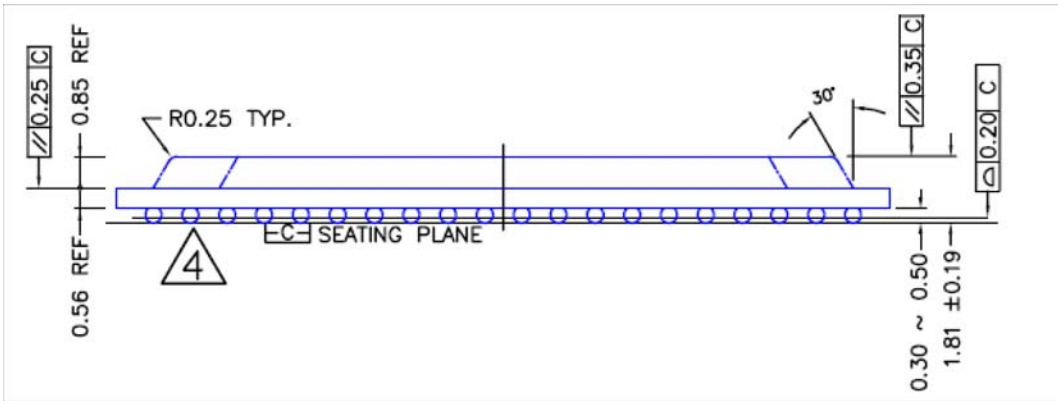
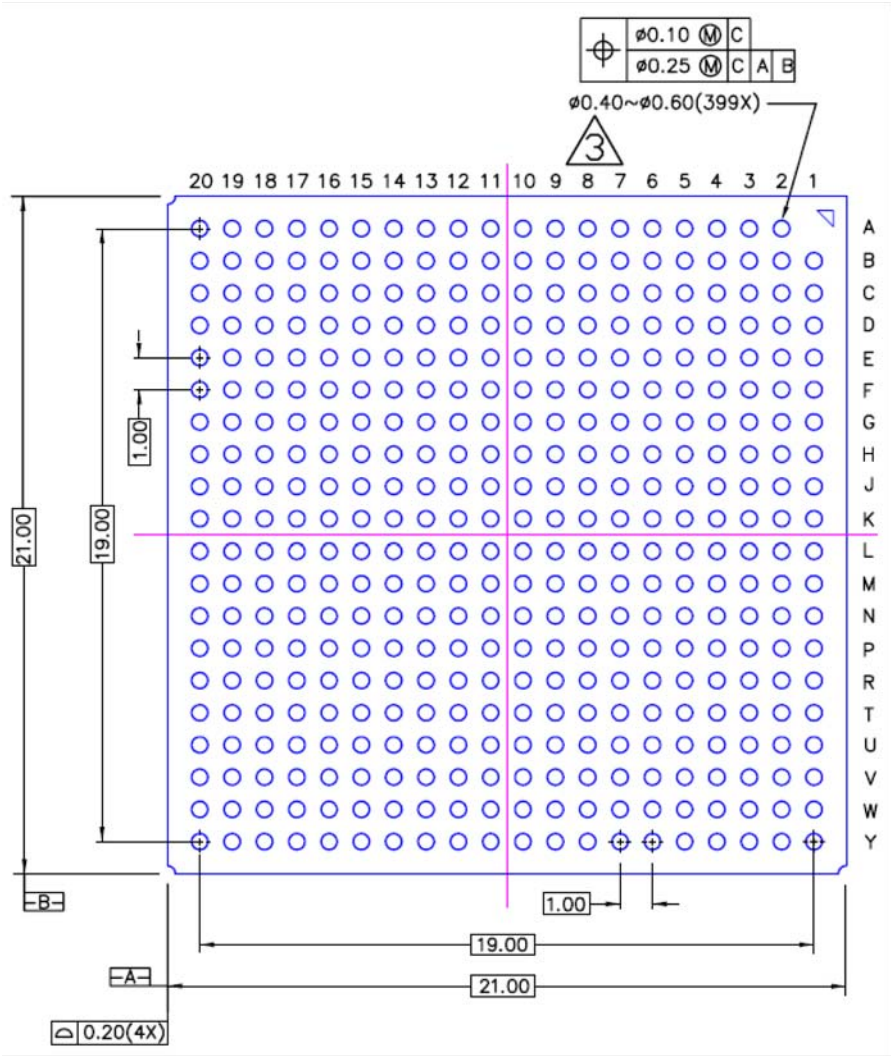


Figure 3: Package - Side View



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Figure 4: Package - Bottom View



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1.4 Thermal Characteristics

Heat generated by the packaged IC has to be removed from the package to ensure that the IC is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive, the IC temperature may exceed the temperature limits. A consequence of this is that the IC may fail to meet the performance specifications and the reliability objectives may be affected.

Failure mechanisms and failure rate of a device have an exponential dependence of the IC operating temperatures. Thus, the control of the package temperature, and by extension the Junction Temperature, is essential to ensure product reliability. The Tsi577 is specified safe for operation when the Junction Temperature is within the recommended limits.

Table 5 shows the simulated Theta jb and Theta jc thermal characteristics of the Tsi577 HSBGA package.

Table 5: Thermal Characteristics of Tsi577

Interface	Result
Theta jb (junction to board)	8.3 °C/watt
Theta jc (junction to case)	3.8 °C/watt

1.4.1 Junction-to-Ambient Thermal Characteristics (Theta ja)

Table 6 shows the simulated Theta ja thermal characteristic of the Tsi577 package. The results in Table 6 are based on a JEDEC Thermal Test Board configuration (JESD51-9) and do not factor in system level characteristics. As such, these values are for reference only.



The Theta ja thermal resistance characteristics of a package depend on multiple system level variables.

Table 6: Simulated Junction to Ambient Characteristics

Package	Theta ja at specified airflow (no Heat Sink)		
	0 m/s	1 m/s	2 m/s
Tsi577 HSBGA	12.3 C/watt	11.1 °C/watt	10.5 °C/watt

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1.4.2 System-level Characteristics

In an application, the following system-level characteristics and environmental issues must be taken into account:

- Package mounting (vertical / horizontal)
- System airflow conditions (laminar / turbulent)
- Heat sink design and thermal characteristics
- Heat sink attachment method
- PWB size, layer count and conductor thickness
- Influence of the heat dissipating components assembled on the PWB (neighboring effects)

Example on Thermal Data Usage

Based on the $Theta_{JA}$ data and specified conditions, the following formula can be used to derive the junction temperature (Tj) of the Tsi577 with a 0m/s airflow:

- $Tj = è_{JA} * P + Tamb.$

  Where: Tj is Junction Temperature, P is the Power consumption, Tamb is the Ambient Temperature

Assuming a power consumption (P) of 3 W and an ambient temperature (Tamb) of 70°C, the resulting junction temperature (Tj) would be 106.9°C.

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2. Electrical Characteristics

This chapter provides the electrical characteristics for the Tsi577. It includes the following information:

- "Absolute Maximum Ratings" on page 31
- "Recommended Operating Conditions" on page 32
- "Power" on page 33

2.1 Absolute Maximum Ratings

Operating the device beyond the operating conditions is not recommended. Stressing the Tsi577 beyond the Absolute Maximum Rating can cause permanent damage.

Table 7 lists the absolute maximum ratings.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$T_{storage}$	Storage Temperature	-55	125	°C
V_{DD_IO}	3.3 V DC Supply Voltage	-0.5	4.6	V
SP_AVDD	3.3 V Analog Supply Voltage	-0.5	4.6	V
V_{DD}, SP_VDD, REF_AVDD	1.2 V DC Supply Voltage	-0.3	1.7	V
$V_{I_SP\{n\}-R\{A-D\}_\{p,n\}}$	SERDES Port Receiver Input Voltage	-0.3	3	V
$V_{O_SP\{n\}-T\{A-D\}_\{p,n\}}$	SERDES Port VM Transmitter Output Voltage	-0.3	3	V
SP_AVDD	Transient di/dt	-	0.0917	A/nS
SP_VDD	Transient di/dt	-	0.136	A/nS

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Table 7: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{O_LVTTL}	LVTTL Output or I/O Voltage	-0.5	V_{DD_IO} +0.5	V
V_{ESD_HBM}	Maximum ESD Voltage Discharge Tolerance for Human Body Model (HBM). [Test Conditions per JEDEC standard - JESD22-A114-B]	-	2000	V
V_{ESD_CDM}	Maximum ESD Voltage Discharge Tolerance for Charged Device Model (CDM). Test Conditions per JEDEC standard - JESD22-C101-A	-	500	V

2.2 Recommended Operating Conditions

Table 8 lists the recommended operating conditions.

Continued exposure of Tundra's devices to the maximum limits of the specified junction temperature could affect the device reliability. Subjecting the devices to temperatures beyond the maximum/minimum limits could result in a permanent failure of the device.

Table 8: Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
T_j	Junction temperature	-40	125°	°C
V_{DD_IO}	3.3 V DC Supply Voltage	2.97	3.63	V
SP_AVDD	3.3 V Analog Supply Voltage	2.97	3.63	V
V_{DD},SP_VDD, REF_AVDD	1.2 V DC Supply Voltage	1.14	1.29	V
I_{VDD_IO}	3.3 V IO Supply Current[a]	-	15	mA
I_{SP_VDD}	SerDes Digital Supply Current[a]	-	570[b]	mA
I_{SP_AVDD}	3.3 V SerDes Supply Current[a]	-	840[b]	mA
I_{VDD}	1.2 V Core Supply Current[a]	-	2007[b]	mA
I_{REF_AVDD}	1.2 V Ref Clock Supply Current	-	12.5	mA
$V_{ripple1}$	Power Supply ripple for Voltage Supplies: SP_VDD, VDD and VDD_IO	-	100	mV_{pp}

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Table 8: Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{ripple2}$	Power Supply ripple for Voltage Supplies: SP_AVDD, REF_AVDD	-	50	mV_{pp}
I_{REXT}	External reference resistor current	-	10	uA

a. The current values provided are maximum values and dependent on device configuration, such as port usage, traffic, etc.

b. These values are estimates and will be updated in a future revision of the documentation.

2.3 Power

The following sections describe the Tsi577's power dissipation and power sequencing.

2.3.1 Power Dissipation

The power dissipation values provided are dependent on device configuration. The line rate, port configuration, traffic all impact the Tsi577's power consumption.

1x Mode

Table 9: Tsi577 Power Dissipation in 1x Mode, 16 Links in Operation

Line Rate	1.25 GBaud	2.5 GBaud	3.125 GBaud
VDD_CORE	0.768	1.158	1.334
SP_VDD	0.410	0.406	0.483
SP_AVDD	0.832	0.823	0.864
VDD_IO	0.005	0.004	0.004
Power (W)	2.015	2.390	2.685
Secondary Port Power W)	0.043	0.061	0.066
Primary Port Power (W)	0.303	0.342	0.401

Table 9 Notes:

- Power is provided for typical process and voltage, and 25°C ambient temperature
- VDD_CORE supplies the ISF and other internal digital logic

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- SP_VDD supplies the digital portion of the Serial RapidIO SerDes
- SP_AVDD supplies the analog portion of the Serial RapidIO SerDes
- VDD_IO supplies power for all non-Serial RapidIO I/O
- Power is modeled for link utilization of approximately 25%
- SerDes I/O drive parameters are set to default values in the SRIO MAC x SerDes Configuration Channel register (TX_BOOST) and the SRIO MAC x SerDes Configuration Global register (Tx_LVL)
- The primary port associated with each SerDes must be enabled before any secondary ports can be used

4x Mode

Table 10: Tsi577 Power Dissipation in 4x Mode, 4 Links in Operation

Line Rate	1.25 GBaud	2.5 GBaud	3.125 GBaud
VDD_CORE	0.467	0.633	0.717
SP_VDD	0.407	0.433	0534
SP_AVDD	0.837	0.838	0.926
VDD_IO	0.005	0.005	0.005
Power (W)	1.716	1.909	2.182
Port Power (W)	0.357	0.405	0.473

Table 10 Notes:

- Power is provided for typical process and voltage, and 25°C ambient temperature
- VDD_CORE supplies the ISF and other internal digital logic
- SP_VDD supplies the digital portion of the Serial RapidIO SerDes
- SP_AVDD supplies the analog portion of the Serial RapidIO SerDes
- VDD_IO supplies power for all non-Serial RapidIO I/O
- Power is modeled for link utilization of approximately 25%
- SerDes I/O drive parameters (TX_ATTEN, TX_BOOST) are set to default values in the SRIO MAC x SerDes Configuration Channel register

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2.3.2 Power Sequencing

Power-up option pins that are controlled by a logic device, in addition to all clocks, must not be driven until all power supply rails to the Tsi577 are stable. External devices also must not be permitted to sink current from, or source current to, the device because of the risk of triggering ESD protection or causing a latch-up condition.

The Tsi577 must have the supplies powered-up in the following order:

- VDD (1.2 V) must be powered up first
- SP_VDD (1.2 V) and REF_AVDD (1.2 V) should power up at approximately the same time as VDD
- Delays between the powering up of VDD, SP_VDD, and REF_AVDD are acceptable.
- No more than 50ms after VDD is at a valid level, VDD_IO (3.3 V) should be powered up to a valid level
- VDD_IO (3.3V) must not power up before VDD (1.2 V)
- SP_AVDD (3.3V) should power up at approximately the same time as VDD_IO
- Delays between powering up VDD_IO and SP_AVDD are acceptable
- SP_AVDD must not power up before SP_VDD



It is recommended that there is no more than 50ms between ramping of the 1.2 V and 3.3 V supplies. The power supply ramp rates must be kept between 10 V/s and 1x10E6 V/s to minimize power current spikes during power up.

If it is necessary to sequence the power supplies in a different order than that recommended above, the following precautions must be taken:

- Any power-up option pins must be current limited with 10 K ohms to VDD_IO or VSS as required to set the desired logic level.
- Power-up option pins that are controlled by a logic device must not be driven until all power supply rails to the Tsi577 are stable.

2.3.2.1 Power-down

Power down is the reverse sequence of power up:

- VDD_IO (3.3V) and SP_AVDD
- VDD (1.2V), SP_VDD and REF_AVDD power-down at the same time, or all rails falling simultaneously.
- Or all rails falling simultaneously

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2.4 Electrical Characteristics

This section describes the AC and DC signal characteristics for the Tsi577.

2.4.1 SerDes Receiver (SP{n}_RD_p/n)

Table 11 lists the electrical characteristics for the SerDes Receiver in the Tsi577.

Table 11: SerDes Receiver Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Z_{DI}	RX Differential Input impedance	90	100	110	Ohm	-
V_{DIFFI}	RX Differential Input Voltage	170	-	1600	mV	-
L_{CR}	RX Common Mode Return Loss	-	-	6	dB	Over a range 100MHz to 0.8* Baud Frequency
L_{DR}	RX Differential Return Loss	-	-	10	dB	Over a range 100MHz to 0.8* Baud Frequency
V_{LOS}	RX Loss of Input Differential Level	55	-	-	mV	Port Receiver Input level below which Low Signal input is detected
$T_{RX_ch_skew}$	RX Channel to Channel Skew Tolerance	-	-	24	ns	Between channels in a given x4 port @ 1.25/2.5Gb/s
		-	-	22	ns	Between channels in a given x4 port @ 3.125Gb/s
R_{TR},R_{TF}	RX Input Rise/Fall times	-	-	160	ps	Between 20% and 80% levels

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2.4.2 SerDes Transmitter (SP{n}_TD_p/n)

Table lists the electrical characteristics for the SerDes transmitter in the Tsi577.

Table 12: SerDes Transmitter Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Z_{SEO}	TX Single-Ended Output impedance	45	50	55	Ohm	-
Z_{DO}	TX Differential Output Impedance	90	100	110	Ohm	-
V_{SW}	TX Output Voltage Swing (Single-ended)	425	-	600	mVp-p	V_{SW} (in mV) = Z_{SEO}/2 x Inom x RIdr/Inom, where Ridr/Inom is the Idr to Inom ratio.
V_{DIFFO}	TX Differential Output Voltage Amplitude	-	2*V_{SW}	-	mVp-p	-
V_{OL}	TX Output Low-level Voltage	-	1.2 - V_{SW}	-	V	-
V_{OH}	TX Output High-level Voltage	-	1.2	-	V	-
V_{TCM}	TX common-mode Voltage	-	1.2 - V_{SW}/2	-	V	-
L_{DR1}	TX Differential Return Loss	-	-	10	dB	For (Baud Frequency)/10<Freq(f)<625MHz and
L_{DR2}	TX Differential Return Loss	-	-	10 + |10log(f/625MHz)|	dB	For 625MHz<=Freq(f)<= Baud Frequency
T_{TX_skew}	TX Differential signal skew	-	-	15	ps	Skew between _p and _n signals on a give Serial channel
T_{TR},T_{TF}	TX Output Rise/Fall times	80	-	110	ps	Between 20% and 80% levels

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2.4.3 Reference Clock, S_CLK_p/n

Table 13 lists the electrical characteristics for the differential SerDes Reference clock input (S_CLK_p/n) in the Tsi577.

Table 13: Reference Clock (S_CLK_p/n) Electrical Characteristics

Symbol	Parameter	Min[a]	Typ	Max	Unit	Notes
V_{SW}	Input voltage swing	0.1	0.5	1	V	-
V_{DIFF}	Differential input voltage swing	$V_{DIFF} = V_{SW} * 2$			V	-
V_{CM}	Differential Input Common Mode Range ((S_CLK_p + S_CLK_n)/2)	175	-	2000	mV	The S_CLK_p/n must be AC coupled.
Fin	Input Clock Frequency	122.88	-	156.25	MHz	-
$F_{S_CLK_P/N}$	Ref Clock Frequency Stability	-100	-	+100	ppm	PPM with respect to 156.25 MHz.
Fin_DC	Ref Clock Duty Cycle	40	50	60	%	-
T_{skew}	Ref Clock Skew	-	-	0.32	ns	Between _p and _n inputs.
T_{R_SCLK}, T_{F_SCLK}	S_CLK_p/n Input Rise/Fall Time	-	-	1	ns	-
$J_{CLK-REF}$	Total Phase Jitter, rms	-	-	3	ps_{rms}	See Below[b]
Zin	Input Impedance	80	100	114	ohms	-

a. RMS jitter from phase noise:
{** notation means “to the power of”}
{dBc will be a negative value from the data sheet}

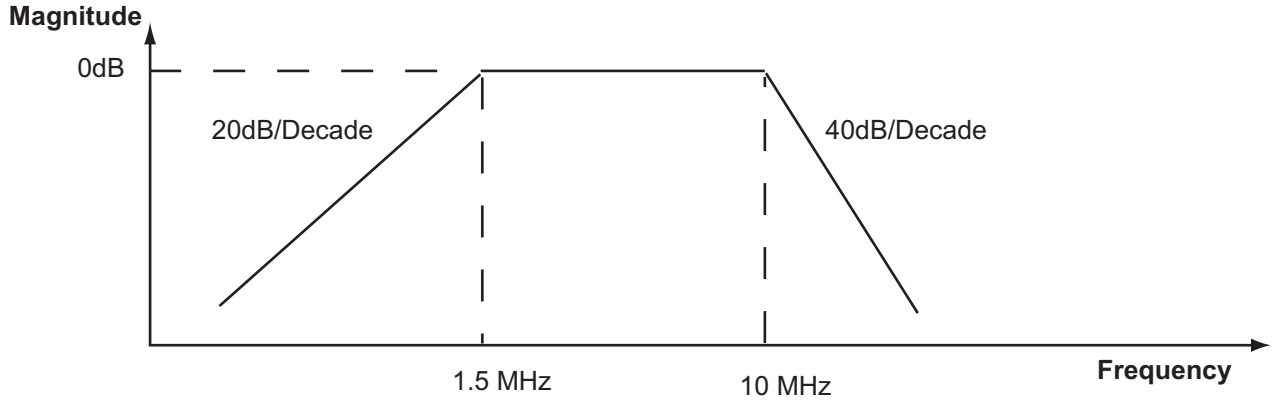
RMSjitter pS(rms)= [((10**(dBc/10))**1/2) * 2] / [2 * pi * (freq in hz)]
{For 312.5Mhz and a phase noise of -63dBc, the RMS jitter = 0.72pS}

Peak to Peak jitter from RMS:
RJ(p-p) = a * RJ(rms) where a= 14.069 (a constant based on bit error rate for a given standard deviation)

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b. Total Permissible Phase Jitter on the Reference Clock is 3 ps rms. This value is specified with assumption that the measurement is done with a 20 G Samples/s scope with more than 1 million samples taken. The zero-crossing times of each rising edges are recorded and an average Reference Clock is calculated. This average period may be subtracted from each sequential, instantaneous period to find the difference between each reference clock rising edge and the ideal placement to produce the Phase Jitter Sequence. The PSD of the phase jitter is calculated and integrated after being weighted with the transfer function shown in Figure 5. The square root of the resulting integral is the rms Total Phase Jitter.

Figure 5: Weighing function for RMS Phase Jitter Calculation



2.4.4 LVTTL I/O and Open Drain Signals

Table 14 lists the electrical characteristics for the 3.3 V digital LVTTL Interface pins on the Tsi577.

Table 14: LVTTL I/O and Open Drain Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	LVTTL Input Low Voltage	-	-	0.8	V	All inputs and I/Os of LVTTL type
V_{IH}	LVTTL Input High Voltage	2.0	-		V	All inputs and I/Os of LVTTL type
I_{IL}	LVTTL Input Low Current	-	-	10	uA	All non-PU inputs and I/Os of LVTTL type
I_{IH}	LVTTL Input High Current	-	-	-10	uA	All non-PD inputs and I/Os of LVTTL type
I_{OZL_PU}, I_{IL_PU}	LVTTL Input Low/ Output Tristate Current	5	-	100	uA	All PU inputs and I/Os of LVTTL type for voltages from 0 to V_{DD_IO} on the pin.

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Table 14: LVTTL I/O and Open Drain Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{OZH_PD}, I_{IH_PD}	LVTTL Input High/ Output Tristate Current	-5	-	-100	uA	All PD inputs and I/Os of LVTTL type for voltages from 0 to V_{DD_IO} on the pin.
V_{OL}	LVTTL Output Low Voltage	-	-	0.4	V	I_{OL}=2mA for INT_b, SW_RST_b, and TDO pins I_{OL}=8mA for I2C_CLK and I2C_SD pins
V_{OH}	LVTTL Output High Voltage	V_{DD_IO} -0.5	-	-	V	I_{OH}=2mA for INT_b, SW_RST_b, and TDO pins
$V_{OVERSHOOT}$	Dynamic Overshoot	-	-	0.9	V	0.9V Max with a maximum energy of 0.75 V-ns
$V_{UNDERSHOOT}$	Dynamic Undershoot	-	-	-0.9	V	-0.9V Max with a maximum energy of 0.75 V-ns
V_{Hyst}	LVTTL Input Hysteresis Voltage	-	200	-	mV	All Hyst inputs and I/Os of LVTTL type
C_{Pad}	LVTTL Pad Capacitance	-	-	10	pF	All pads of LVTTL type
T_{cfgpS}	Configuration Pin Setup Time	100	-	-	ns	For all Configuration pins with respect to HARD_RST_b rising edge
T_{cfgpH}	Configuration Pin Hold Time	100	-	-	ns	For all Configuration pins with respect to HARD_RST_b rising edge
T_{ISOV1}	INT_b/SW_RST_b Output Valid Delay from rising edge of S_CLK	-	-	15	ns	Measured between 50% points on both signals. Output Valid delay is guaranteed by design.
T_{ISOF1}	INT_b/SW_RST_b Output Float Delay from rising edge of S_CLK	-	-	15	ns	A float condition occurs when the output current becomes less than I_{LO}, where I_{LO} is 2 x I_{OZ}. Float delay guaranteed by design.
f_{MCES}	MCES pin frequency	-	-	1	MHz	both as input and output
R pull-up	Resistor pull-up	82K	-	260K	ohms	@Vil=0.8V
R pull-down	Resistor pull-down	28K	-	54K	ohms	@Vih=2.0V

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2.4.5 I²C Interface

Table 15 lists the AC specifications for Tsi577's I²C Interface. The I2C interfaces includes balls: I2C_SCLK, I2C_SD, I2C_DISABLE, I2C_MA, I2C_SEL, I2C_SA[1:0] and I2C_SEL.

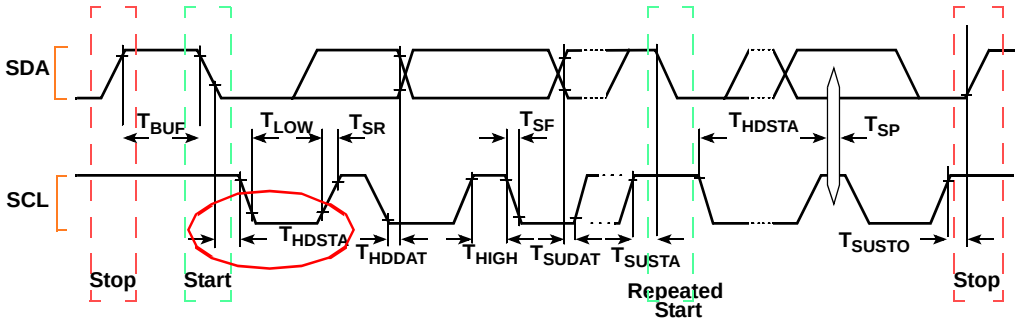
Table 15: AC Specifications for I²C Interface

Symbol	Parameter	Min	Max	Units	Notes
F_{SCL}	I2C_SD/I2C_SCLK Clock Frequency	0	100	kHz	-
T_{BUF}	Bus Free Time Between STOP and START Condition	4.7	-	µs	1
T_{LOW}	I2C_SD/I2C_SCLK Clock Low Time	4.7	-	µs	1
T_{HIGH}	I2C_SD/I2C_SCLK Clock High Time	4	-	µs	1
T_{HDSTA}	Hold Time (repeated) START condition	4	-	µs	1,2
T_{SUSTA}	Setup Time for a Repeated START condition	4.7	-	µs	1
T_{HDDAT}	Data Hold Time	0	3.45	µs	1
T_{SUDAT}	Data Setup Time	250	-	ns	1
T_{SR}	Rise Time for I2C_xxx (all I2C signals)	-	1000	ns	1
T_{SF}	Fall Time for I2C_xxx (all I2C signals)	-	300	ns	1
T_{SUSTOP}	Setup Time for STOP Condition	4	-	µs	1

Notes:

1. See Figure 6, I²C Interface Signal Timings
2. After this period, the first clock pulse is generated

Figure 6: I²C Interface Signal Timings



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2.4.6 Boundary Scan Test Interface Timing

Table 16 lists the test signal timings for Tsi577.

Table 16: Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency	0	25	MHz	-
T_{BSCH}	TCK High Time	50	-	ns	• Measured at 1.5V • Note test
T_{BSCL}	TCK Low Time	50	-	ns	• Measured at 1.5V • Note test
T_{BSCR}	TCK Rise Time	-	25	ns	• 0.8V to 2.0V • Note test
T_{BSCF}	TCK Fall Time	-	25	ns	• 2.0V to 0.8V • Note test
T_{BSIS1}	Input Setup to TCK	10	-	ns	-
T_{BSIH1}	Input Hold from TCK	10	-	ns	-
T_{BSOV1}	TDO Output Valid Delay from falling edge of TCK.[a]	-	15	ns	-
T_{OF1}	TDO Output Float Delay from falling edge of TCK	-	15	ns	-
$T_{BSTRST1}$	TRST_B release before HARD_RST_b release	-	10	ns	TRST_b must become asserted while HARD_RST_b is asserted during device power-up
$T_{BSTRST2}$	TRST_B release before TMS or TDI activity	1	-	ns	-

a. Outputs precharged to VDD.

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3. Layout Guidelines

This chapter describes the layout guidelines for the Tsi577. It includes the following information:

- “Impedance Requirements” on page 43
- “Tracking Topologies” on page 44
- “Power Distribution” on page 57
- “Decoupling Requirements” on page 59
- “Clocking and Reset” on page 63
- “Modeling and Simulation” on page 66
- “Testing and Debugging Considerations” on page 67
- “Reflow Profile” on page 69

3.1 Overview

The successful implementation of a Tsi577 in a board design is dependent on properly routing the Serial RapidIO signals and maintaining good signal integrity with a resultant low bit error rate. The sections that follow contain information for the user on principals that will maximize the signal quality of the links.

Since every situation is different, Tundra urges the designer to model and simulate their board layout and verify that the layout topologies chosen will provide the performance required of the product.

3.2 Impedance Requirements

The impedance requirement of the Serial RapidIO interface is 100 ohms differential.

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3.3 Tracking Topologies

The tracking topologies required to maintain a consistent differential impedance of 100 ohms to the signal placed on the transmission line are limited to Stripline and Microstrip types. The designer must decide whether the signalling must be moved to an outer layer of the board using a Microstrip topology, or if the signalling may be placed on an inner layer as stripline where shielding by ground and power planes above and below is possible.

In order to prevent consuming received eye margin, the =/- track skew of a lane should be constrained to a maximum of 15pS.

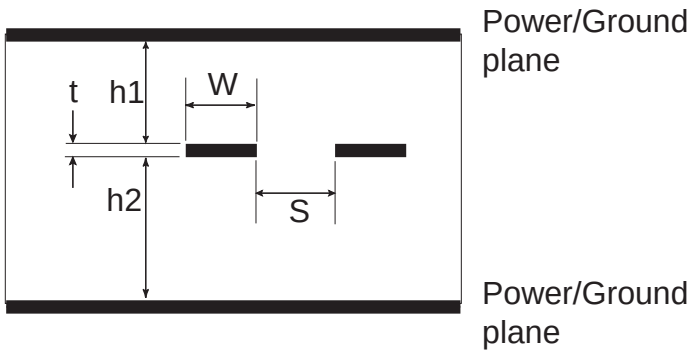
The skew limitation between the shortest lane and longest lane of the RX or TX of a port is 22 ns.

3.3.1 Stripline

The RapidIO buses should be routed in a symmetrical edge-coupled stripline structure in order to ensure a constant impedance environment. The symmetrical stripline construction is shown in Figure 7. This method also provides clean and equal return paths through VSS and VDD from the I/O cell of the Tsi577 to the adjacent RapidIO device. The use of broadside coupled stripline construction as shown in Figure 9 is discouraged because of its inability to maintain a constant impedance throughout the entire board signal layer.

The minimum recommended layer count of a board design consists of 12 layers. The optimum design consists of 16 layers. The designer should consider both of these designs and weigh their associated costs versus performance.

Figure 7: Recommended Edge Coupled Differential Stripline (symmetric when h1=h2)



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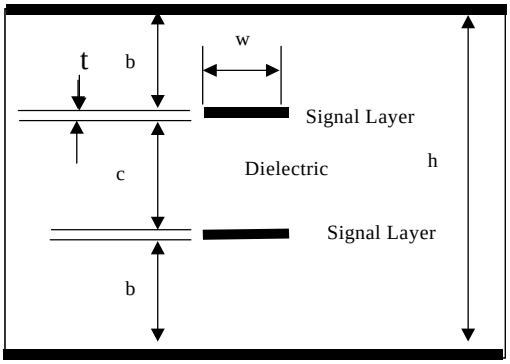
Figure 8: Equations for Stripline and Differential Stripline Impedance (in Ohms):

$$Zo = \frac{60}{\sqrt{\varepsilon_r}} \times \ln\left(\frac{1.9\left(2(h1 + h2) + t\right)}{0.67\,\pi\left(0.8w + t\right)}\right)$$

$$Zdiff = 2 \times Zo\left(1 - 0.374\; e^{-2.9\left[\frac{s}{h1+h2}\right]}\right)$$

The broadside coupled stripline construction is not recommended for use with RapidIO because of the manufacturing variations in layer spacings. These variations will cause impedance mismatch artifacts in the signal waveforms and will degrade the performance of the link.

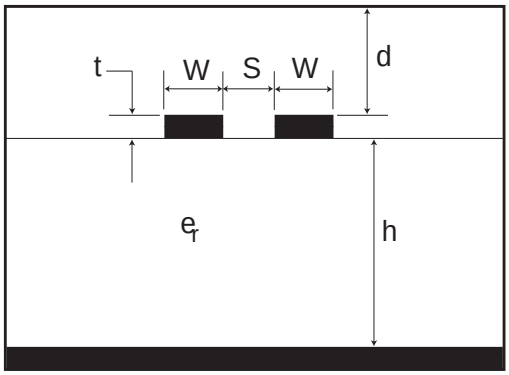
Figure 9: Not Recommended Broadside Coupled or Dual Stripline Construction



3.3.1.1 Microstrip

When it is necessary to place the differential signal pairs on the outer surfaces of the board, the differential microstrip construction is used. Figure 10 shows the construction of the microstrip topology. Below the figure are the design equations for calculating the impedance of the trace pair.

Figure 10: Differential Microstrip Construction



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Figure 11: Equations for the Differential Microstrip Construction:

$$Z_o = \frac{60}{\sqrt{0.475\varepsilon_r + 0.67}} \ln\left[\frac{4h}{0.67(0.8w + t)}\right] ohms$$

$$Z_{diff} \cong 2Z_o\left(1 - 0.48e^{-0.96\frac{s}{h}}\right) ohms$$

3.3.1.2 Signal Return Paths

The return path is the route that current takes to return to its source. It can take a path through ground planes, power planes, other signals, or integrated circuits. The return path is based on electro-magnetic field effects. The return path follows the path of least resistance nearest to the signal conductor. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar consideration.

A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance.

If via densities are large and most of the signals switch at the same time (as would be the case when a whole data group switches layers), the layer to layer bypass capacitors may fail to provide an acceptably short signal return path to maintain timing and noise margins.

When the signals are routed using symmetric stripline, return current is present on both the VDD and VSS planes. If a layer change must occur, then both VCC and VSS vias must be placed as close to the signal via as possible in order to provide the shortest possible path for the return current.

The following return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Do not route impedance controlled signals over splits in the reference planes.
- Do not route signals on the reference planes in the vicinity of system bus signals.
- Do not make signal layer changes that force the return path to make a reference plane change.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not route over via anti-pads or socket anti-pads.

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If reference plane changes must be made:

- Change from a VSS reference plane to another VSS reference plane and place a minimum of one via connecting the two planes as close as possible to the signal via. This also applies when making a reference plane change from one VCC plane to another VCC plane.
- For symmetric stripline, provided return path vias for both VSS and VCC.
- Do not switch the reference plane from VCC to VSS or vice versa.

3.3.1.3 Guard Traces

Guard traces are used to minimize crosstalk. Guard traces are tracks that run parallel to a signal trace for the entire length and are connected to the reference plane to which the signal(s) are associated. Guard traces can lower the radiated crosstalk by as much as 20dB.

The use of guard tracks requires some planning and foresight. The guard tracks will consume board real estate but in a dense routing where the potential for crosstalk is present, guard traces will save overall space that would have been consumed by separation space. Simulation has shown that a 5 mil ground trace with 5 mil spaces between the aggressor and receptor traces offers as much isolation as a 20 mil space between aggressor and receptor traces. The aggressor trace is the trace with a driven waveform on it. The receptor trace is the trace onto which the crosstalk is coupled.

Guard tracks are required to be s*titched* or connected with vias, to the reference plane associated with the signal. To ensure that there is no resonance on the guard traces, the stitching vias should be spaced at intervals that equal *1/20*λ of the 3rd harmonic.

Figure 12: Equation

$$\lambda = \sqrt{\varepsilon} \times {}^{c}\!/_{f}$$

$${}^{1}\!/_{20}\lambda_{3rd} = \frac{3\times10^{8} m/s}{20\times f_{3rd}}\sqrt{\varepsilon}$$

In the case of the 3.125 Gb/s data rate, the rise and fall times must be less than 40 pS. This relates to an upper frequency of 25 Ghz and a corresponding wavelength of 25 mm based on a permittivity of 4.3. Therefore, the stitching vias must not be further apart than 8 mm.

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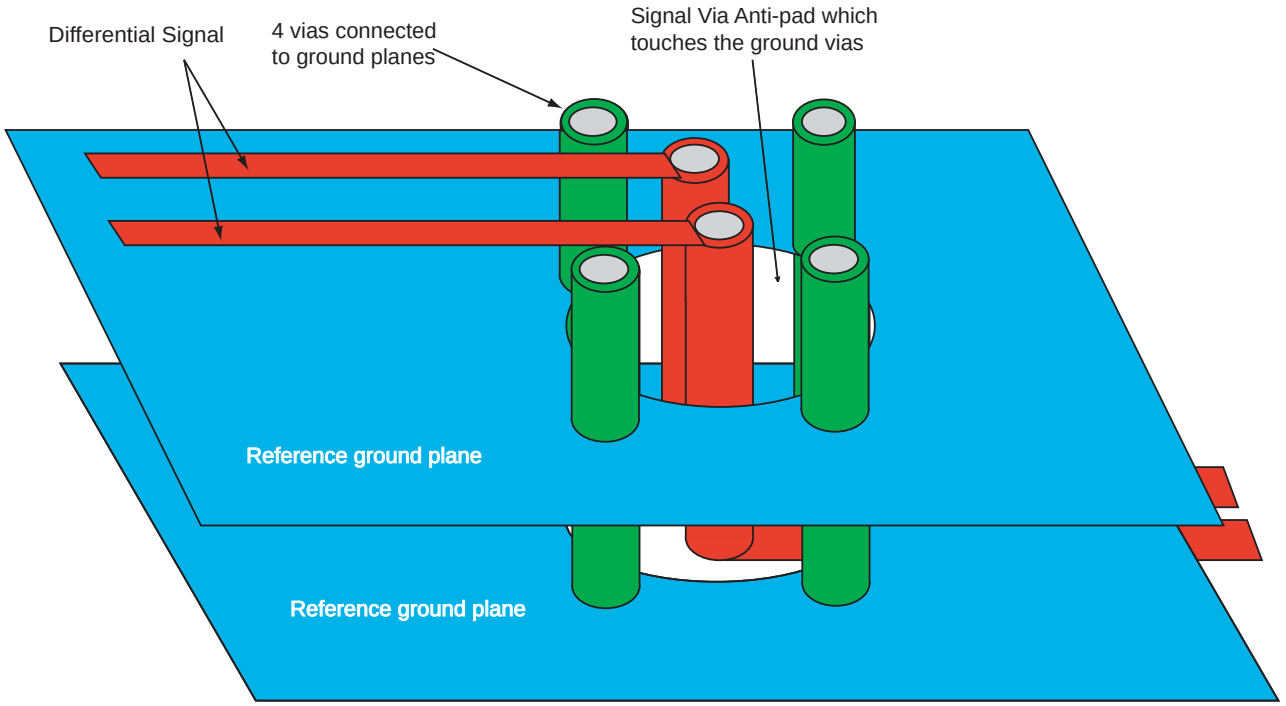
3.3.1.4 Via Construction

Due to the high frequency content of the Serial RapidIO signals, it is necessary to minimize the discontinuities imposed by crossing ground and power planes when it is necessary to transition to different signal layers. The use of a controlled impedance via is recommended The construction of a differential via is shown in Figure 13.

Tip

Detailed design information can be found in bibliography entry 15, "*Designing Controlled Impedance Vias*" by Thomas Neu, EDN Magazine October 2, 2003.

Figure 13: Differential Controlled Impedance Via



3.3.1.5 Layer Transitioning with Vias

The basic rule in high speed signal routing is to keep vias in the signal path down to a minimum. Vias can represent a significant impedance discontinuity and should be minimized. When routing vias, try to ensure that signals travel through the via rather than across the via.

A via where the signal goes through the via, has a much different effect than a via where the signal travels across the via. These two cases are shown in Figure 17 and in Figure 18. The "in" and "out" nodes of the via model are shown on the their corresponding locations in the figures.

Transitioning across a via that is not blind or buried leaves a stub which appears as a capacitive impedance discontinuity. The portion of the via that conducts current appears inductive while the stub that develops only an electric field will appear capacitive.

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In order to minimize the effects of a via on a signal, the following equations may be used to approximate the capacitance and inductance of the via design. It can be seen that the proximity of the pad and antipad have a direct relationship on the capacitance, and that the length of the barrel (h) has a direct effect on the inductance.

Figure 14: Equation 1

$$L = 5.08h\left[\ln\left(\frac{4h}{d}\right) + 1\right]$$

Equation parameters:

- L is the inductance in nH.
- h is the overall length of the via barrel.
- d is the diameter of the via barrel.

Figure 15: Equation 2

$$C = \frac{1.41\varepsilon_r TD_1}{D_2 - D_1}$$

Equation parameters:

- C is the capacitance in pF.
- T is the thickness of the circuit board or thickness of pre-preg.
- D_1 is the diameter of the via pad.
- D_2 is the diameter of the antipad.
- ε_r is the dielectric constant of the circuit board material.

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Figure 16: Via Construction

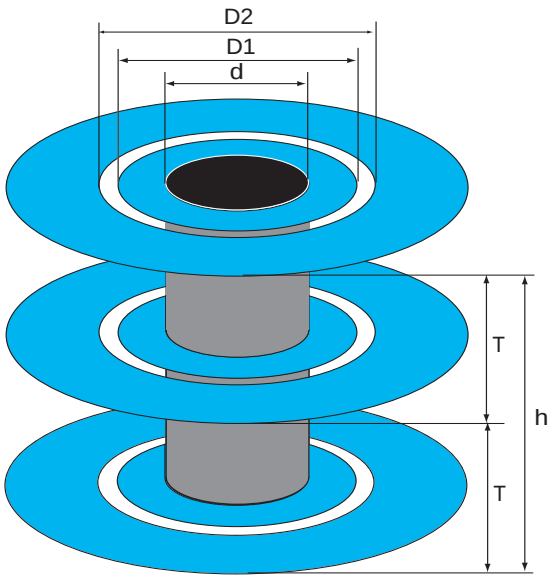


Figure 17: Signal Across a Via

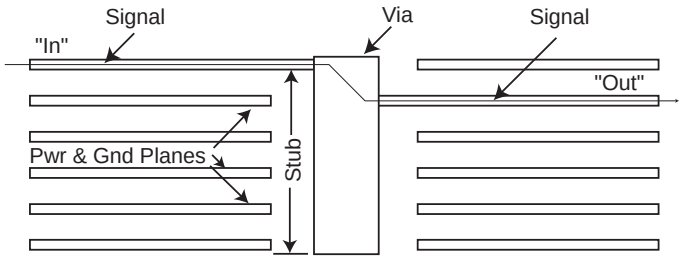
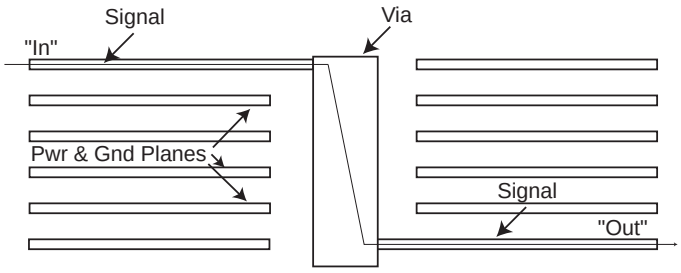


Figure 18: Signal Through a Via



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Because of the high frequencies present in the RapidIO signal, vias become a significant contributor to signal degradation. Most vias are formed by a cylinder going through the PCB board. Because the via has some length, there is an inductance associated with the via. Parasitic capacitance comes from the power and ground planes through which the via passes. From this structure, the model of the vias in RLC lumps as shown in Figure 19 and Figure 20.

The figure parameters are:

- Cvia is the total capacitance of the via to ground or power
- Rvia is the total resistance through the via, and Lvia is the total inductance of the via.

These parameters may be extracted using 3D parasitic extraction tools. By distributing the R, L, and C, the model better represents the fact that the capacitance, resistance and inductance are distributed across the length of the via. For the Via model to be accurate in simulation, the propagation delay of each LC section should be less than 1/10 of the signal risetime. This is to ensure the frequency response of the via is modeled correctly up to the frequencies of interest. More information may be found in reference [16].

Figure 19: Signal Transitioning Across a Via Simulation Model

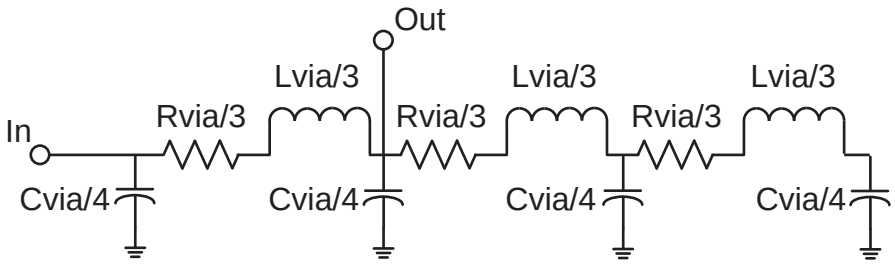
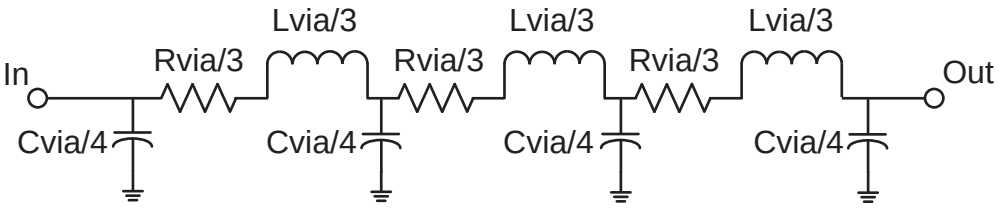


Figure 20: Signal Transitioning Through a Via Simulation Model



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3.3.1.6 Buried Vs. Blind

The use of buried and blind vias is recommended because in both cases the signal travels through the via and not across it. Examples of these two types of structures are shown in Figure 21 and Figure 22.

Figure 21: Buried Via Example

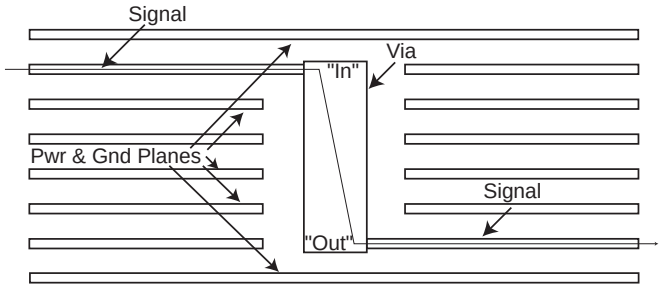
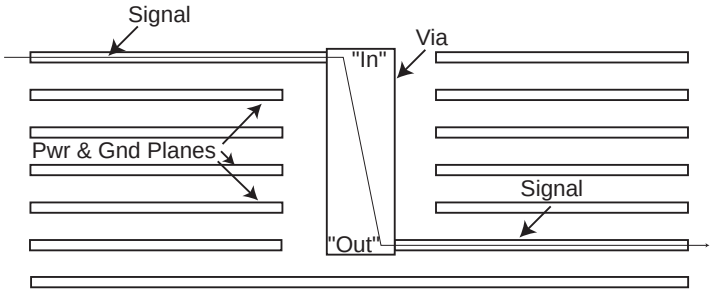


Figure 22: Blind Via Example



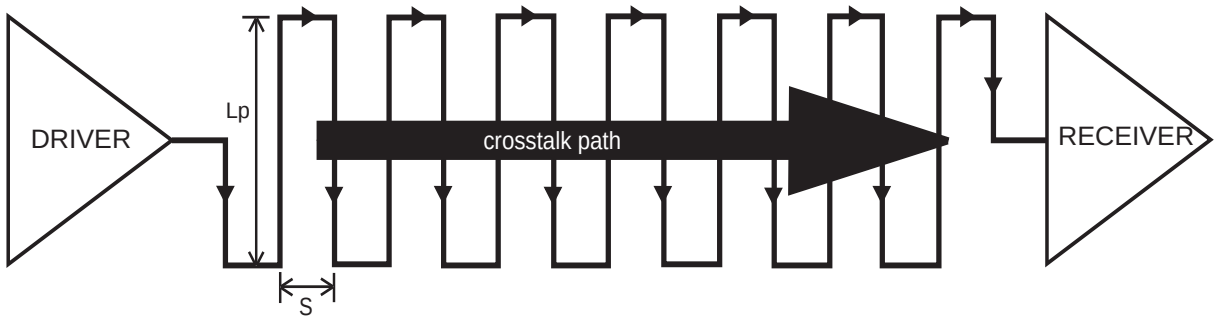
3.3.1.7 Serpentine Traces

During layout, it is necessary to adjust the lengths of tracks in order to accommodate the requirements of equal track lengths for pairs of signals. In the case of the differential signals, this ensures that both the negative and positive halves of the signals arrive at the receiver simultaneously, thus maximizing the data sampling window in the eye diagram. Creating a serpentine track is a method of adjusting the track length.

Ensure that the wave front does not propagate along the trace and through the crosstalk path perpendicular to the parallel sections, as shown in Figure 23. The arrival of a wave front at the receiver ahead of the wave front travelling along the serpentine route is caused by the self-coupling between the parallel sections of the transmission line (Lp).

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Figure 23: Serpentine Signal Routing



To maximize the signal integrity, clock lines should not be serpentine.

Figure 26 describes the guidelines for length matching a differential pair. If it is necessary to serpentine a trace, follow these guidelines:

- Make the minimum spacing between parallel sections of the serpentine trace (see “S” in Figure 23) at least 3 to 4 times the distance between the signal conductor and the reference ground plane.
- Minimize the total length (see “Lp” in Figure 23) of the serpentine section in order to minimize the amount of coupling.
- Use an embedded microstrip or stripline layout instead of a microstrip layout.

Tip

For a detailed discussion about serpentine layouts, refer to Section 12.8.5 of *“High-Speed Signal Propagation, Advanced Black Magic”* by Howard Johnson and Martin Graham.

3.3.2 Crosstalk Considerations

The Serial RapidIO signals easily capacitively couple to adjacent signals due to their high frequency. It is therefore recommended that adequate space be used between different differential pairs, and that channel transmit and receive be routed on different layers. Cross coupling of differential signals results in an effect called Inter-Symbol Interference (ISI). This coupling causes pattern dependent errors on the receptor, and can substantially increase the bit error rate of the channel.

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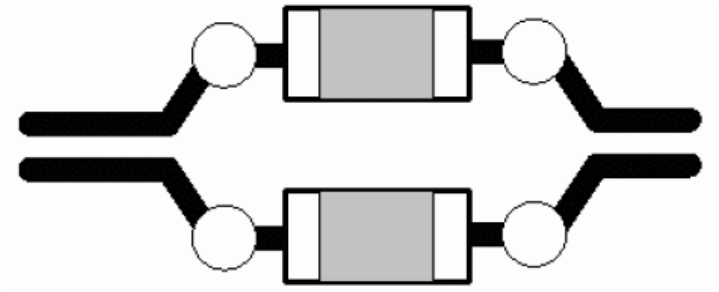
3.3.3 Receiver DC Blocking Capacitors

The Serial RapidIO interface requires that the port inputs be capacitor coupled in order to isolate the receiver from any common mode offset that may be present in the transmitter outputs. DC blocking capacitors should be selected such that they have low dissipation factor and low series inductance. The recommended capacitor value is 0.1uF ceramic in an 0402 size.

Figure 24 shows the recommended tracking and capacitor pad placement required. It will be necessary to model and simulate the effects of the changed track spacing on the channel quality and determine if any changes are required to the topology. An often used method of correcting the decreased impedance caused by the larger capacitor mounting pads is to create a slot in the shield plane below the capacitor bodies and soldering pads. Since the impedance change caused by the slot is dependent on the capacitor geometry, core thickness, core material characteristics and layer spacings, the size and shape of the slot will have to be determined by simulation.

Do not place the capacitors along the signal trace at a $\lambda/4$ increment from the driver in order to avoid possible standing wave effects.

Figure 24: Receiver Coupling Capacitor Positioning Recommendation



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3.3.4 Escape Routing

All differential nets should maintain a uniform spacing throughout a route. Separation of differential pairs to go around objects should not be allowed. Figure 25 illustrates several options for breaking out a differential pair from the Tsi577 device. The order of preference is from A to D.

Case D below has a small serpentine section used to match the inter-pair skew of the differential pair. In this case each serpentine section should be greater than 3 x W (W=width), and the gap should not increase by more than 2x. Figure 26 illustrates these requirements.

Figure 25: Escape Routing for Differential Signal Pairs

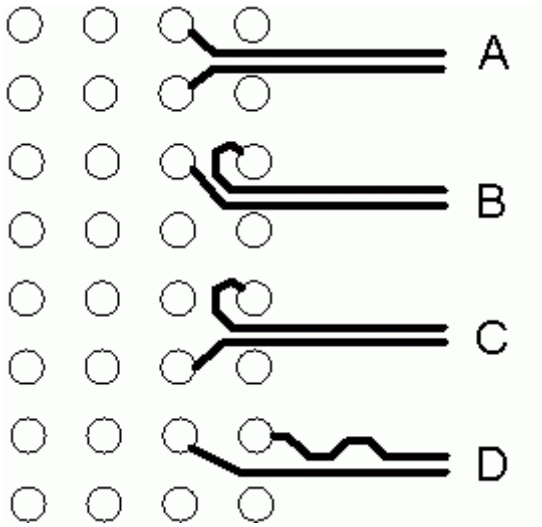
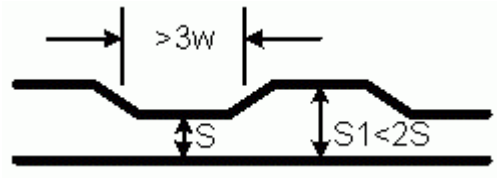


Figure 26: Differential Skew Matching Serpentine

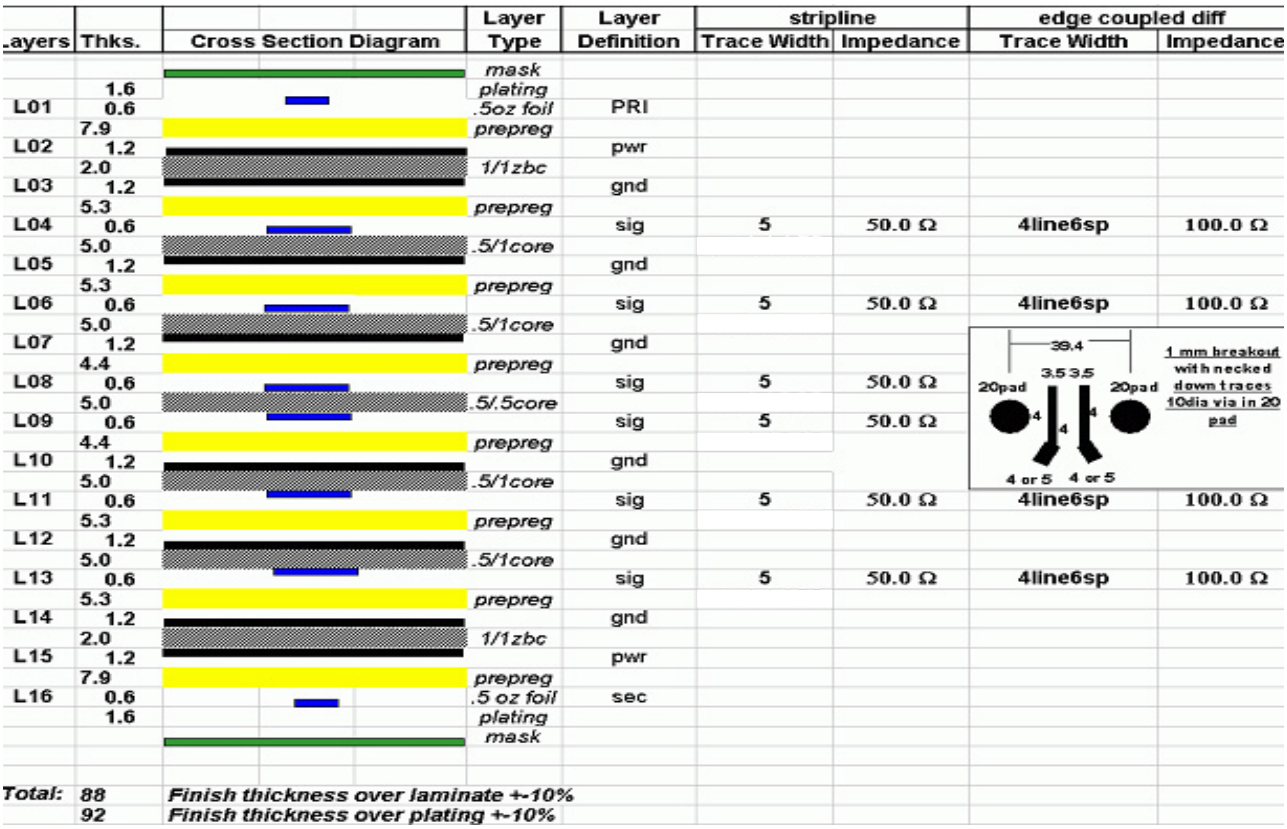


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3.3.5 Board Stackup

The recommended board stack up is shown in Figure 27. This design makes provision for four stripline layers and two outer microstrip layers. Layers eight and nine are provisioned as orthogonal low speed signal routing layers.

Figure 27: Recommended Board Stackup



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3.4 Power Distribution

The Tsi577 is a high speed device with both digital and analogue components in its design. The core logic has a high threshold of noise sensitivity within its 1.2 V operating range. However, the analogue portion of the switch is considerably more sensitive.

The correct treatment of the power rails, plane assignments, and decoupling is important to maximize Tsi577 performance. The largest indicator of poor performance on the Serial RapidIO interfaces is the presence of jitter. The die, I/O, and package designs have all been optimized to provide jitter performance well below the limits required by the Serial RapidIO specifications. The guidelines provided below will assist the user in achieving a board layout that will provide the best performance possible. The required decoupling by each voltage rail can be found in “Electrical Characteristics” on page 31. The ripple specifications for each rail are maximums, and every effort should be made to target the layout to achieve lower values in the design.

A solid, low impedance plane must be provided for the VDD 1.2V core supply referenced to VSS. It is strongly recommended that the VDD and VSS planes be constructed with the intent of creating a buried capacitance. The connection to the power supply must also be low impedance in order to minimize noise conduction to the other supply planes.

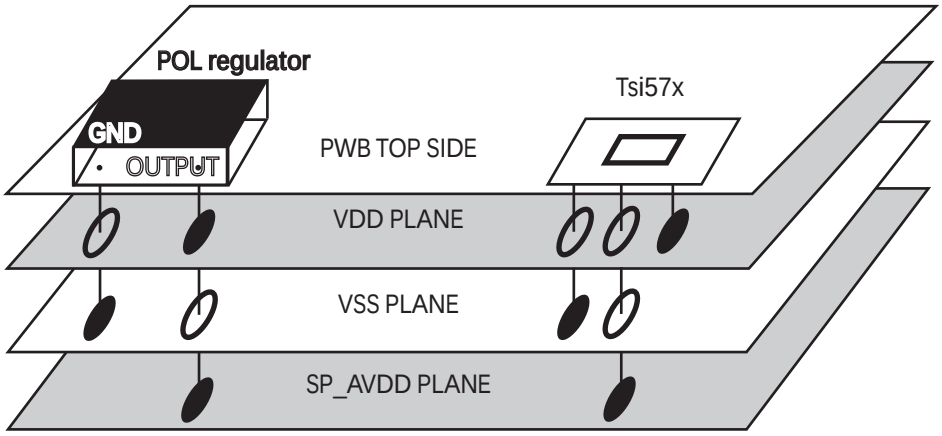
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A solid, low impedance plane must be provided for the SP_VDD 1.2V SerDes supply, referenced to the VSS plane. This supply can be derived from the same power supply as VDD, as long as a *Kelvin connection* is used. The preference however, is to use a separate power supply.

The term *Kelvin connection* is used to describe a single point of contact so that power from one power plane does not leak past the power supply pin into the other power plane. The leakage can be prevented by the fact the output of a power supply is a very low impedance point in order to be able to supply a large amount of current. Because it is such a low impedance point, any noise presented to it by the power plane is sent to ground.

A kelvin connection enables two power planes to be connected together at a single point. Using this technique, the same power supply module can be used to provide power to a noisy digital power plane (VDD), as well as a quiet analog power plane (SP_AVDD).

Figure 28: Kelvin Connection Example



Example of connection points described as a Kelvin Connection
VDD and SP_AVDD planes are only connected to each other at the POL regulator output pin.

The SP_AVDD 3.3V SerDes analogue supply also needs low impedance supply plane. This supply voltage powers the RapidIO receivers and transmitters, and their associated PLLs. Connect all of the SP_AVDD pins to this plane and decouple the plane directly to VSS. The plane must be designed as a low impedance plane in order to minimize transmitter jitter and maximize receiver sensitivity. Construction of this plane as a buried capacitance referenced to VSS is suggested.

The REF_AVDD pins provide power to the S_CLK distribution circuits in the switch. The voltage should be derived from the SP_VDD plane. One ferrite will suffice to isolate the SP_VDD from the REF_AVDD. Two decoupling capacitors should be assigned to each pin.

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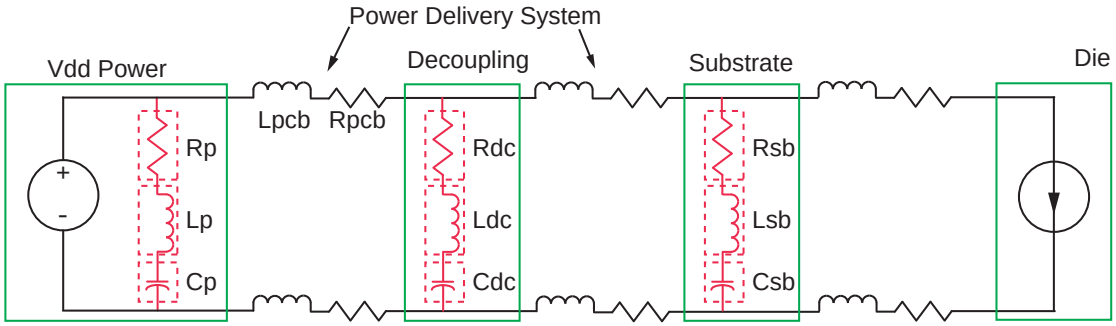
The VDD_IO supply powers the 3.3V I/O cells on the switch. This supply requires no special filtering other than the decoupling to the VSS plane.

3.5 Decoupling Requirements

This section deals with the subject of decoupling capacitors required by the Tsi577. To accomplish the goal of achieving maximum performance and reliability, the power supply distribution system needs to be broken down into its individual pieces, and each designed carefully.

Figure 29 shows the standard model for representing the components of a typical system. This figure also represents the parasitics present in a power distribution system.

Figure 29: System Power Supply Model



3.5.1 Component Selection

The recommended decoupling capacitor usage for the Tsi577 is shown in “Electrical Characteristics” on page 31. The capacitors should be selected with the smallest surface mount body that the applied voltage permits in order to minimize the body inductance. Ceramic X7R type are suggested for all of the values listed. The larger value capacitors should be low ESR type.

The components should be distributed evenly around the device in order to provide filtering and bulk energy evenly to all of the ports.

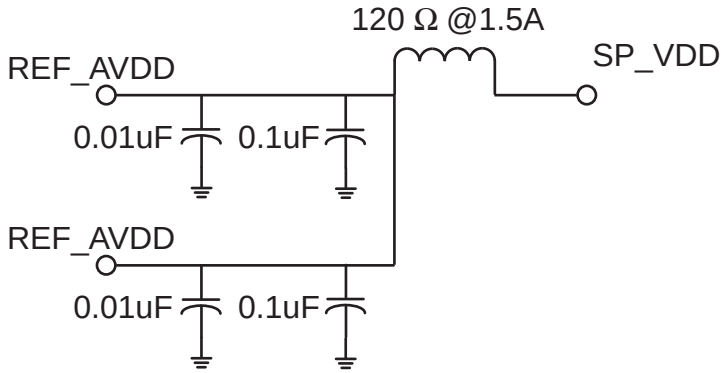
Use the Tsi577 ball map (available at www.tundra.com) to aid in the distribution of the capacitors.

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3.5.1.1 REF_AVDD

The REF_AVDD pins require extra care in order to minimize jitter on the transmitted signals. The circuit shown in Figure 30 is recommended for the REF_AVDD signal. One filter is required for the two pins.

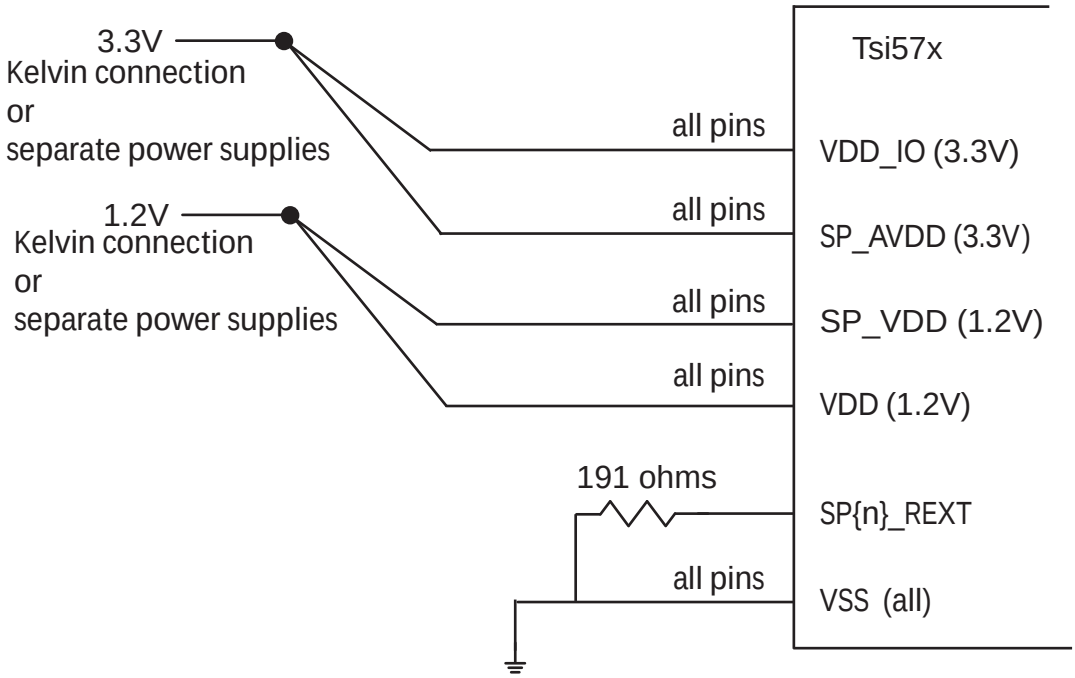
Figure 30: PLL Filter



3.5.1.2 Power and REXT

The circuit in Figure 31 shows the connection of the power rails as required by the device.

Figure 31: Power and REXT Diagram



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Table 17: Decoupling Capacitor Quantities and Values Recommended for the Tsi577

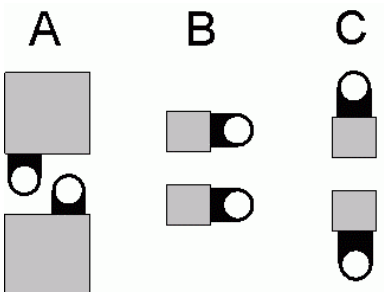
Voltage	Usage	Acronym	Component Requirements			
1.2V	Logic Core	VDD	20 x 0.1uF	20 x 0.01uF	16 x 1nF	16 x 22uF
1.2V	SerDes core, SerDes bias	SP_VDD	8 x 0.1uF	30 x 0.01uF	4 x 10uF	4 x 100uF
3.3V	SerDes transceivers	SPn_AVDD	8 x 0.1uF	8 x 0.01uF	-	-
3.3V	Single ended I/O ports	VDD_IO	12 x 0.1uF	12 x 0.01uF	-	-
1.2V	Clock distribution circuit	REF_AVDD	2 x 0.1uF	2 x 0.01uF	1 x ferrite bead 120 ohm @ 1.5Amp	

3.5.2 Effective Pad Design

Breakout vias for the decoupling capacitors should be kept as close together as possible. The trace connecting the pad to the via should also be kept as short as possible with a maximum length of 50mils. The width of the breakout traces should be 20mils, or the width of the pad.

Via sharing should not be used in board design with the Tsi577.

Figure 32: Recommended Decoupling Capacitor Pad Designs



3.5.3 Power Plane Impedance and Resonance

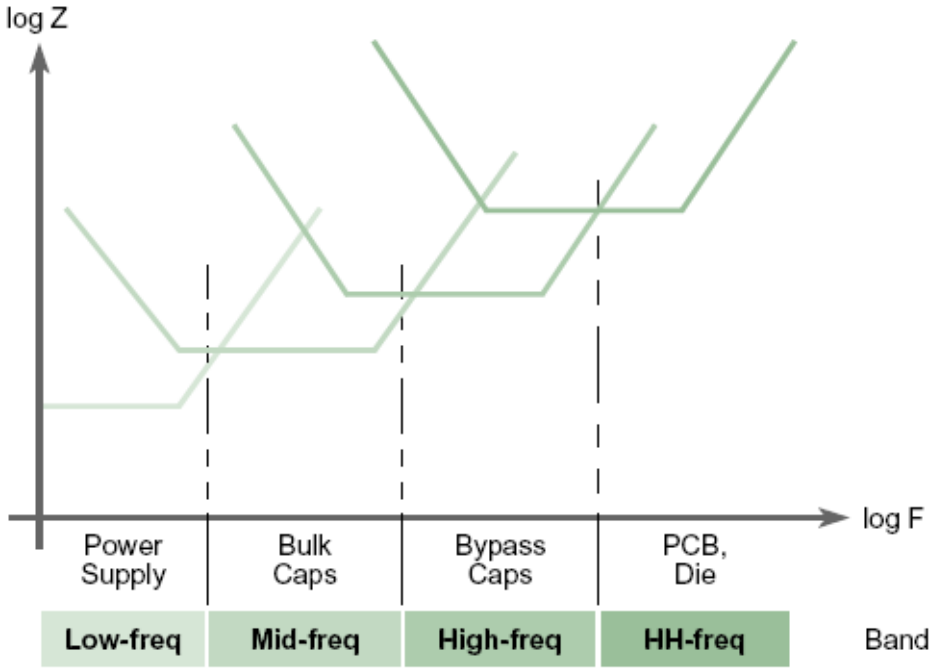
The intent of adding decoupling to a board is to lower the impedance of the power supply to the devices on the board. It is necessary to pay attention to the resonance of the combined bulk capacitance and to stagger the values in order to spread the impedance valleys broadly across the operating frequency range. Figure 34 demonstrates the concept of staggered bands of decoupling. Calculate the impedance of each of the capacitor values at the knee frequency to determine their impact on resonance.

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Figure 33: Equation

$$F_{knee} = \frac{0.5}{T_{rise}} \text{ where } T_{rise} = \text{time from 10\% to 90\%}$$

Figure 34: Decoupling Bypass Frequency Bands



As the frequency changes, each part of the power distribution system responds proportionally; the low-impedance power supply responds to slow events, bulk capacitors to mid-frequency events, and so forth.

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3.6 Clocking and Reset

This section discusses the requirements of the clock and reset inputs.

3.6.1 Clock Overview

The Tsi577 switch input reference clock is used to drive the switch's internal clock domains. The reference clock is described in Table 18.

Table 18: Clock Input Sources

Clock Input Pin	Type	Maximum Frequency	Clock Domain
S_CLK_[p/n]	Differential	125-156.25 MHz	Serial Transmit Domain (Nominally 156.25MHz) Internal Switching Fabric (ISF) Domain

3.6.1.1 Frequencies Required

The clock signals should be shielded from neighboring signal lines using ground traces on either side. This reduces jitter by minimizing crosstalk from the neighboring signal lines.

In order to preserve the quality of the low jitter 156.25 MHz clock, the shielding requirement of the clock lines is critical. It is possible that low-frequency noise can interfere with the operation of PLLs, which can cause the PLLs to modulate at the same frequency as the noise. The high-frequency noise is generally beyond the PLL bandwidth which is about 1/10th the S_CLK frequency. For more information, refer to Figure 5 on page 39.

3.6.1.2 Stability, Jitter and Noise Content

The maximum input jitter on the S_CLK input is 3pS RMS from 1.5 to 10 MHz to avoid passing through the PLL loop filter in the SerDes and affecting the transmit data streams. For more information, refer to Figure 5 on page 39.

Jitter Equation

The following equation can be used to convert Phase Noise in dBc to RMS jitter:

RMSjitter pS(rms) = $[((10^{(dBc/10)})^{1/2}) * 2] / [2 * pi * (frequency\ in\ hz)]$

Using this equation, an example of 312.5 MHz and a phase noise of -63dBc, would produce 0.72pS RMS jitter.

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3.6.2 Clock Domains

The Tsi577 contains a number of clock domains that are generated from the input reference clock. These domains are detailed in Table 19. The frequencies listed below is for standard RapidIO line rates. For more information about special line rate support see "Support for Non-standard Baud Rates" on page 79.

Table 19: Clock Domains

Clock Domain	Clock Source	Frequency (MHz)[a]	Description
Internal Register Domain	S_CLK_P/N Divided by 2	62.5, 78.125	This clock domain includes the register bus, and the register bus master and slave sub-blocks within each functional block. Registers for each block usually use the same clock as that block. The domain uses the input S_CLK_P/N divided by 2.
ISF Clock Domain	S_CLK_P/N	125, 156.25	This clock domain includes the Switch ISF, the Multicast Engine and the portion of each block that communicates with the Switch ISF. The domain uses the S_CLK_P/N.
Serial Receive Domain[b]	Individual RapidIO Received lanes	125/250/312.5	These clocks are the recovered clocks from the SerDes. Each lane will have its own recovered clocks. Its rates depend on the data baud rates. Frequencies quoted are for standard RapidIO line rates. Non-standard reference clock frequencies result in different frequencies for the Serial Receive Domain (see "Support for Non-standard Baud Rates").
Serial Transmit Domain	S_CLK_P/N	125/250/312.5	This clock domain clocks all the RapidIO transmit ports. The S_CLK_P/N input clocks the transmit logic. This clock generates the high-speed clock that outputs the serial data on output pins, SP{0..5}_T{A..D}_P/N. The maximum data rate for this domain is 3.125 Gbps per lane. The maximum data rate requires a 125 or 156.25 MHz SL_CLK_P/N reference clock.
I^2C Domain	S_CLK_P/N divided by 2, Further divided by 782	100 kHz	This clock domain drives the I^2C output clock pin, I2C_SCLK. This domain is generated by dividing the S_CLK_P/N input by a programmable value (see "I2C Interface"). The majority of the I^2C logic runs in the Internal Register Domain. Division by 782 produces the 100 kHz frequency when a 156.25 MHz RapidIO reference clock is supplied. Slower reference clocks require adjustment of the I^2C clock divider registers to achieve 100 kHz operation.

a. For electrical characteristics information, see "Electrical Characteristics".

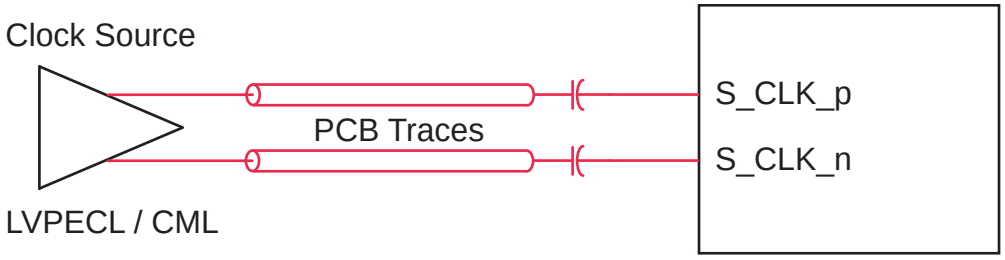
b. This is also known as SYS_CLK in the document.

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3.6.2.1 Interfacing to the S_CLK_x inputs

The interface for a LVPECL clock source to the receiver input cell is shown in Figure 35. Note that an AC-coupled interface is required so that only the AC information of the clock source is transmitted to the clock inputs of the Tsi577.

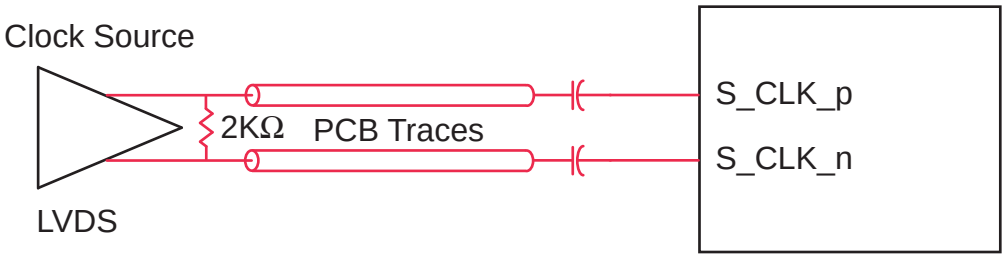
Figure 35: Tsi577 **driven by LVPECL or CML clock source**



The interface for an LVDS clock source to the converter cell is shown in Figure 36. Since an LVDS driver requires a DC termination path, a 2-K resistor should be inserted before the capacitors. This resistor can be placed anywhere along the signal path between the clock source and the AC-coupling capacitors, although Tundra recommends placing it close to the clock source.

Note that the effective termination resistance seen by the clock source is roughly 95Ω due to the parallel combination of this external resistor and the integrated termination resistor of the converter cell. Again, an AC-coupled interface is required so that only the AC information of the clock source is transmitted to the clock inputs of the Tsi577.

Figure 36: Tsi577 **driven by an LVDS clock source**



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3.6.3 Reset Requirements

The Tsi577 requires only one reset input, HARD_RST_b. The signal provided to the device must be a monotonic 3.3V swing that de-asserts a minimum of 1mS after supply rails are stable. The signal de-assertion is used to release synchronizers based on S_CLK which control the release from reset of the internal logic. S_CLK must therefore be operating and stable before the 1mS HARD_RST_b countdown begins.

TRST_b must be asserted while HARD_RST_b is asserted following a device power-up to ensure the correct setup of the tap controller. TRST_b is not required to be re-asserted for non power cycle assertions of HARD_RST_b.



The most versatile solution to this requirement is to AND the HARD_RST_b and TRST_b signals together to form an output to drive the TRST_b pin on the switch.

Power up option pins are double sampled at the release of HARD_RST_b. As such, there is no set-up time requirement, but the signals must be stable at the release of HARD_RST_b. There is a hold time requirement of 100nS or 20 S_CLK cycles minimum.

3.7 Modeling and Simulation

Verifying the signal integrity of the board design is very important for designs using GHz signalling. Tundra recommends that the designer invest in a simulation tool as an aid to a successful RapidIO design. Tools are available from companies such as Mentor Graphics (HyperLynx GHZ), Ansoft (SIwave) and SiSoft (SiAuditor).

3.7.1 IBIS

The use of IBIS for signal integrity checking at the high frequencies of the Serial RapidIO link have been found to be too inaccurate to be useful. Also, we have found that most tools do not yet support the *IBIS Specification (Revision 3.2)* for the support of multi-staged slew rate controlled buffers.

Contact Tundra, at www.tundra.com, for an IBIS file which supports the LVTTL pins on the device.

3.7.2 Encrypted HSPICE

Visit www.tundra.com to request the Model License Agreement form required to acquire the encrypted model.

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3.8 Testing and Debugging Considerations

Making provisions for debugging and testing tools speeds-up board bring-up. This section provides information on the probing requirements for monitoring the serial RapidIO link between two devices. At GHz frequencies, standard probing techniques are intrusive and cause excessive signal degradation introducing additional errors in the link stream. The recommended solution is an ultra low capacitance probe that operates in conjunction with a logic analyzer. The addition of the appropriate disassembler software to the analyzer makes it a very powerful tool for examining the traffic on a link and aiding in software debugging. Please contact your local test equipment vendor for appropriate solutions for your requirements.

3.8.1 Logic Analyzer Connection Pads

The pinout for a recommended Serial RapidIO 8-channel probe is shown in Table 20. This pin/signal assignment has been adopted by several tool vendors but is not an established standard.

The following notes apply:

Footprint Channel versus Lane/Link Designations

- Channel = either an upstream OR downstream differential pair for a given lane
- C<letter> = the designator for a channel which accepts a given differential pair of signals
- C<letter><p or n> = the two signals of the differential pair. The signals within a given pair may be assigned to either P or N regardless of polarity.

3.8.1.1 General Rules for Signal Pair Assignment of Analyzer Probe

The differential pairs that make up the Serial RapidIO links must be assigned to specific pins of the footprint in order to take advantage of the pre-assigned channel assignments provided by Nexus when purchasing the Serial RapidIO pre-processor.

Table 20: 8-Channel Probe Pin Assignment

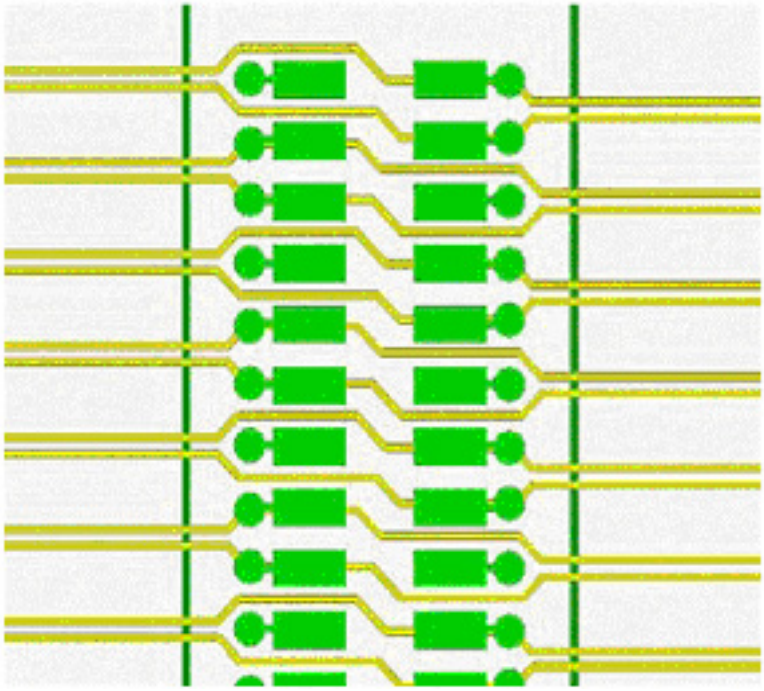
Pin Number	Signal Name	Pin Number	Signal Name
2	GND	1	CAp/Tx0
4	CBp/Rx0	3	CAn/Tx0
6	CBn/Rx0	5	GND
8	GND	7	CCp/Tx1
10	CDp/Rx1	9	CCn/Tx1
12	CDn/Rx1	11	GND

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Table 20: 8-Channel Probe Pin Assignment

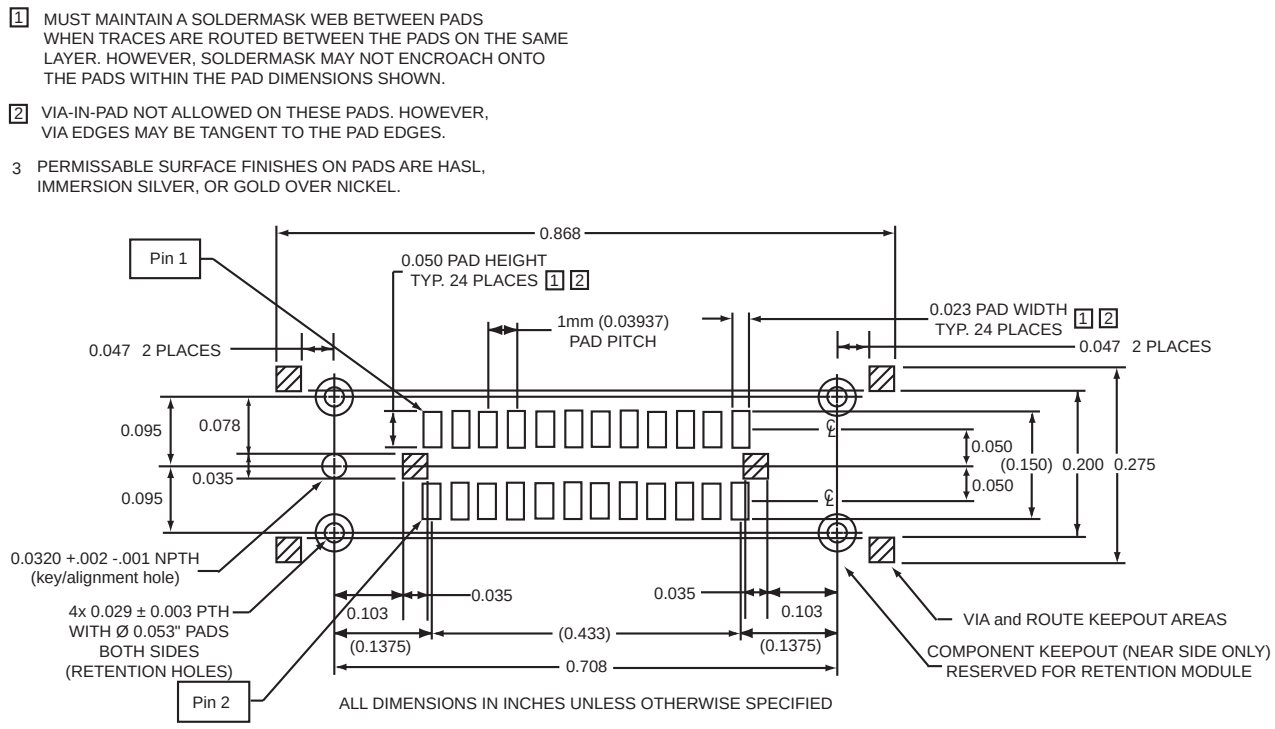
Pin Number	Signal Name	Pin Number	Signal Name
14	GND	13	CEp/Tx2
16	CFp/Rx2	15	CEn/Tx2
18	CFn/Rx2	17	GND
20	GND	19	CGp/Tx3
22	CHp/Rx3	21	CGn/Tx3
24	CHn/rX3	23	GND

Figure 37: Analyzer Probe Pad Tracking Recommendation



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Figure 38: Analyzer Probe Footprint



3.8.2 JTAG Connectivity

The Joint Test Action Group (JTAG) created the boundary-scan testing standard (documented in the *IEEE 1149.1 Standard*) for testing printed circuit boards (PCBs).

The boundary-scan approach involves designing boundary-scan circuitry into the integrated circuit. PCBs populated with 1149.1 compliant devices can be then tested for connectivity, correct device orientation, correct device location, and device identification. All the pins on compliant devices can be controlled and observed using (typically) five pins that are routed to the board edge connector. Board designers can develop a standard test for all 1149.1 compliant devices regardless of device manufacturer, package type, technology, or device speed.

In addition to the 1149.1 compliant boundary scan TAP controller, the Tsi577 also contains an 1149.6 compliant TAP controller to aid in the production testing of the SerDes pins.

The Tsi577 also has the capability to read and write all internal registers through the JTAG interface. Through this interface, users may load and modify configuration registers and look up tables without the use of RapidIO maintenance transactions or an I^2C EEPROM.

3.9 Reflow Profile

The Tsi577 adheres to JEDEC-STD-020C for its reflow profile. For the leaded version, the peak reflow temperature is 225ºC (+0/-5ºC). For the lead-free version, the peak reflow temperature is 260ºC (+0/-5ºC).

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A. Ordering Information

This chapter discusses ordering information and describes the part numbering system for the Tsi577.

A.1 Ordering Information

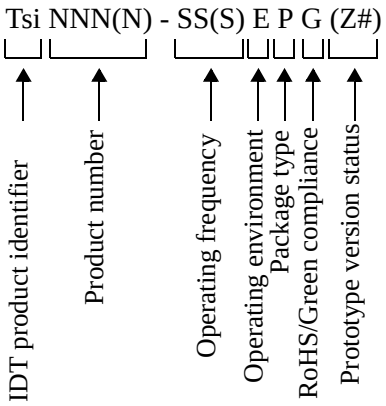
When ordering the Tsi577 please refer to the device by its full part number, as displayed in Table 21.

Table 21: Tsi577 Ordering Information

Part Number	Frequency	Temperature	Package	Pin Count
TSI577-10GCL	1.25 - 3.125 Gbit/s	Commercial	HSBGA	399
TSI577-10GCLV	1.25 - 3.125 Gbit/s	Commercial	HSBGA (RoHS)	399
TSI577-10GIL	1.25 - 3.125 Gbit/s	Industrial	HSBGA	399
TSI577-10GILV	1.25 - 3.125 Gbit/s	Industrial	HSBGA (RoHS)	399

A.2 Part Numbering Information

The part numbering system is explained as follows.



- ( ) – Indicates optional characters.
- Tsi – IDT system interconnect product identifier.
- NNNN – Product number (may be three or four digits).
- SS(S) – Maximum operating frequency or data transfer rate of the fastest interface. For operating frequency numbers, M and G represent MHz and GHz. For transfer rate numbers, M and G represent Mbps and Gbps.

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- E – Operating environment in which the product is guaranteed. This code may be one of the following characters:
  - C - Commercial temperature range (0 to +70°C)
  - I - Industrial temperature range (-40 to +85°C)
  - E - Extended temperature range (-55 to +125°C)
- P – The Package type of the product:
  - B - Ceramic ball grid array (CBGA)
  - E, L, J, and K - Plastic ball grid array (PBGA)
  - G - Ceramic pin grid array (CPGA)
  - M - Small outline integrated circuit (SOIC)
  - Q - Plastic quad flatpack (QFP)
- G – IDT products fit into three RoHS-compliance categories:
  - Y - RoHS Compliant (6of6) – These products contain none of the six restricted substances above the limits set in the EU Directive 2002/95/EC.
  - Y - RoHS Compliant (Flip Chip) – These products contain only one of the six restricted substances: Lead (Pb). These flip-chip products are RoHS compliant through the Lead exemption for Flip Chip technology, Commission Decision 2005/747/EC, which allows Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages.
  - V - RoHS Compliant/Green - These products follow the above definitions for RoHS Compliance and meet JIG (Joint Industry Guide) Level B requirements for Brominated Flame Retardants (other than PBBs and PBDEs).
- Z# – Prototype version status (optional). If a product is released as a prototype then a “Z” is added to the end of the part number. Further revisions to the prototype prior to production release would add a sequential numeric digit. For example, the first prototype version of device would have a “Z,” a second version would have “Z1,” and so on. The prototype version code is dropped once the product reaches production status.

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