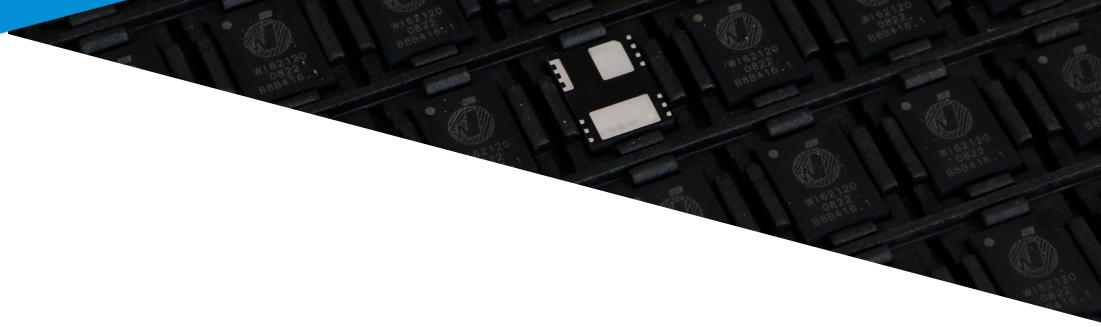


WI62120

Half-Bridge Power GaN IC

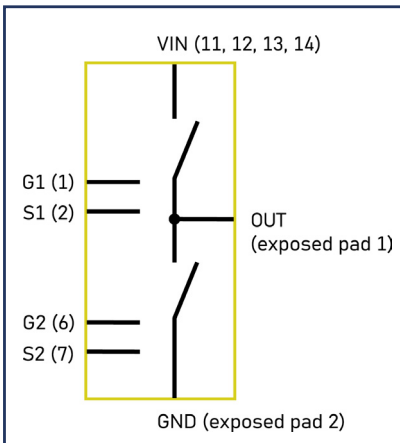
Description

The WI62120 is an enhancement mode GaN-on-silicon half-bridge power circuit of the WiseGan™ power integrated circuits family of Wise-integration. The properties of GaN allow high current, high voltage breakdown and high switching frequency.

Applications

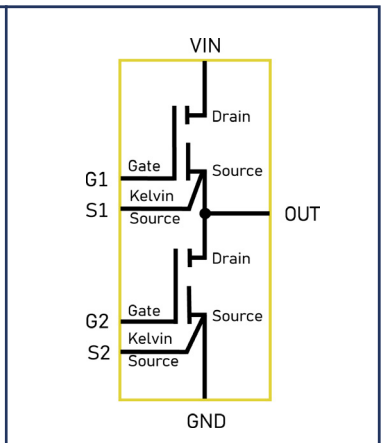
- High efficiency power conversion
- High density power conversion
- AC-DC, DC-DC, DC-AC
- Bridgeless Totem Pole PFC
- ACF (active clamp flyback)
- LLC resonant converter
- Half-bridge topologies
- Synchronous Buck or Boost
- Small-Medium UPS
- Fast Battery Charging

Symbol



Note :
Pin 2 & 7 are Kelvin Source connections

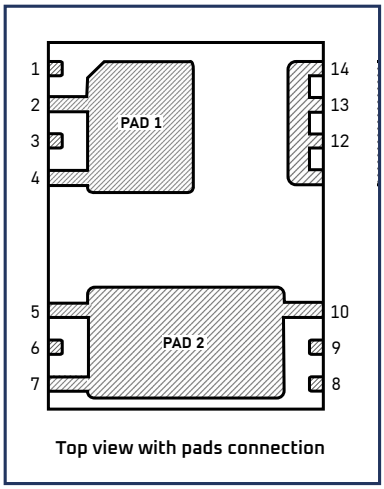
Internal diagram



Features

- 650 V enhancement mode half-bridge
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 120 mΩ per switch
- $I_{DS(max)}$ = 13 A
- Low inductance PQFN package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive up to 7 V
- High switching frequency (>1 MHz)
- Zero reverse recovery loss
- Small 6 x 8 mm PCB footprint

Pinout



Top view with pads connection

Table of contents

- Features 1
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Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Drain-to-Source Transient Voltage [1]	V_{DS}	750	V
Gate-to-Source Transient Voltage [2]	V_{GS}	-2 to +7	V
Operating Junction Temperature	T_J	-40 to +150	°C
Operating Storage Temperature	T_{stg}	-55 to +150	°C

[1] maximum duration is 1ms
[2] maximum duration is 1µs

Operating conditions

Parameter	Symbol	Value	Units
Continuous Drain-to-Source Voltage	$V_{DS\ (max)}$	650	V
Gate-to-Source Voltage	V_{GS}	0 to +6	V
Continuous Drain Current (T_J = 25°C)	I_D	13	A

Thermal Characteristics

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	1.9	K/W
Thermal Resistance (junction-to-ambient)	$R_{\Theta JA}$	35.5	K/W

ESD Ratings

Parameter	Symbol	Value	Units
Human Body Model	HBM	1000	V
Charged Device Model	CDM	1500	V

Static Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS} = 6 V, T_J = 25 °C, I_{DS} = 2 A		120	175	mΩ
		V_{GS} = 6 V, T_J = 150 °C, I_{DS} = 2 A		250		mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, T_J = 25 °C, I_{DS} = 10 mA	0.8	1.6	2.2	V
		V_{DS} = V_{GS}, T_J = 150 °C, I_{DS}= 10 mA		1.8		V
Internal Gate Resistance	R_G	open drain		2.82		Ω
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V, T_J = 25°C		0.3	1.3	µA
		V_{DS} = 650 V, V_{GS} = 0 V, T_J = 150°C		12		µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = 6 V, V_{DS} = 0 V, T_J = 25°C		42	110	µA
		V_{GS} = 6 V, V_{DS} = 0 V, T_J = 150 °C		350		µA
Source-to-Drain Reverse Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 5 A		3.25		V
		V_{GS} = 0 V, I_{SD} = 6 A		3.55		V

Dynamic Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Input Capacitance	C_{ISS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		92.7		pF
Reverse Transfer Capacitance	C_{RSS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		1.22		pF
Output Capacitance	C_{OSS}	V_{DS} =400 V, V_{GS} = 0V, f = 100 kHz		22.1		pF
Total Gate Charge	Q_G	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		2.75		nC
Gate to Source Charge	Q_{GS}	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		0.3		nC
Gate to Drain Charge	Q_{GD}	V_{DS} = 400 V, V_{GS} = 0 V to 6 V		1.0		nC
Output Charge	Q_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V		22.7		nC
Output Capacitance Stored Energy	E_{OSS}	V_{DS} = 400 V, V_{GS} = 0 V		2.8		µJ
Effective Output Capacitance (Energy related)	$C_{O(ER)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		34.6		pF
Effective Output Capacitance (Time related)	$C_{O(TR)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		56.7		pF

Static main characteristics (T_J = 25°C unless otherwise noted)

Figure 1. Output I_{DS} . V_{DS}

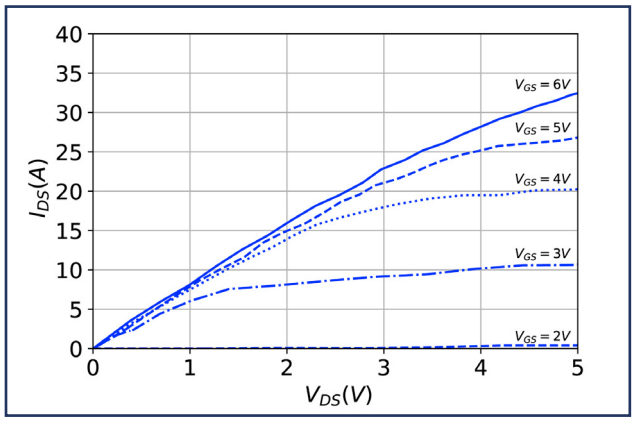


Figure 2. Simulated output I_{DS} . V_{DS} T_J = 125°C

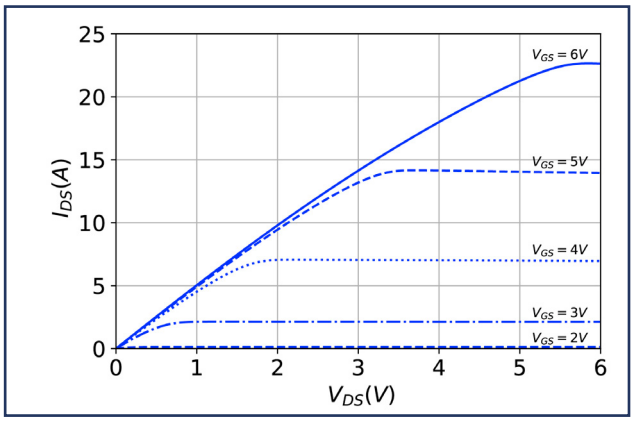


Figure 3. Capacitance

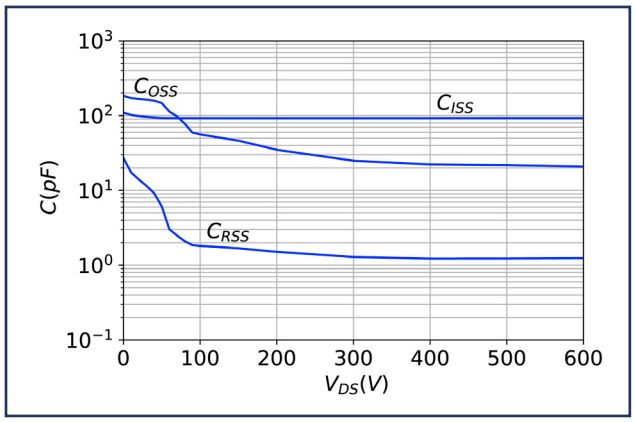


Figure 4. Gate Charge, Q_G

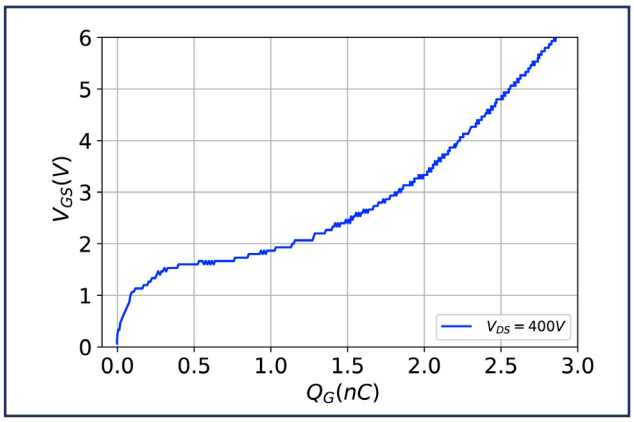


Figure 5. Stored Energy

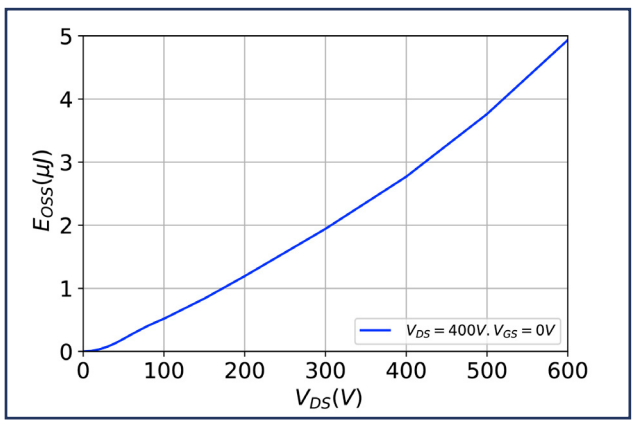


Figure 6. Output charge

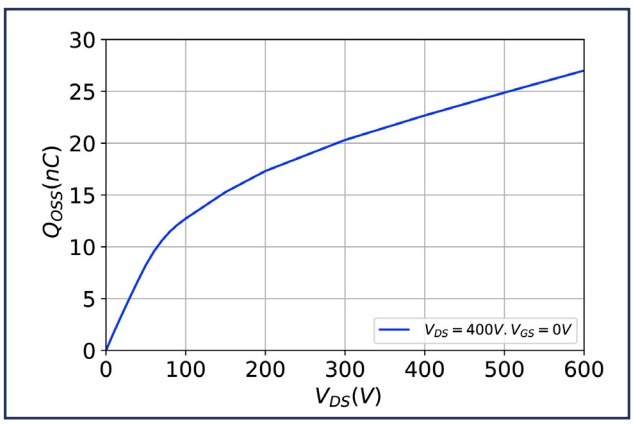


Figure 7. Drain-source leakage

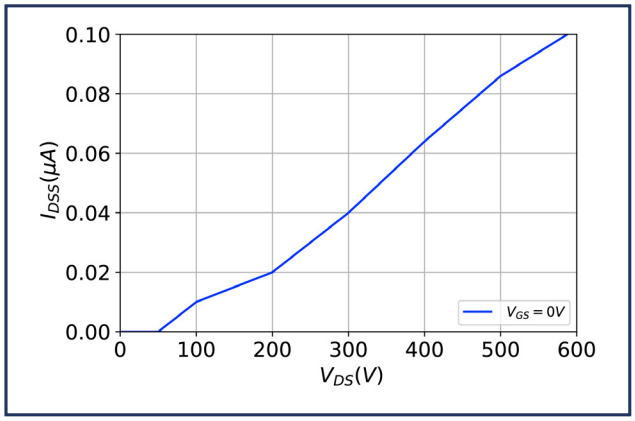


Figure 8. Drain-source leakage T_J = 125°C

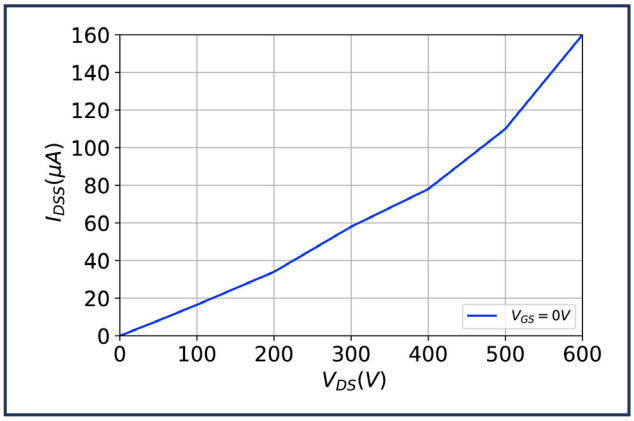


Figure 9. Gate-source leakage

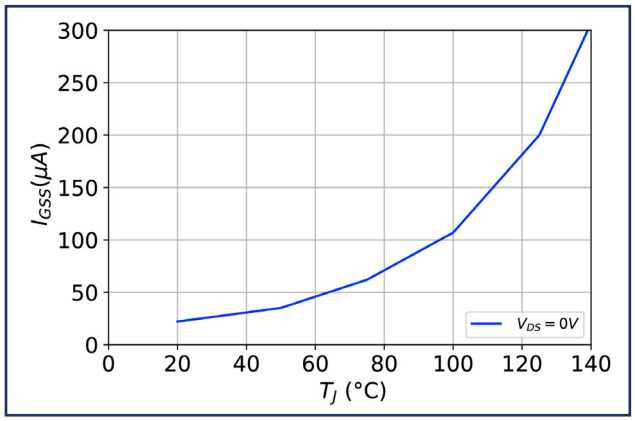


Figure 10. $V_{GS(th)}$ vs. Temperature

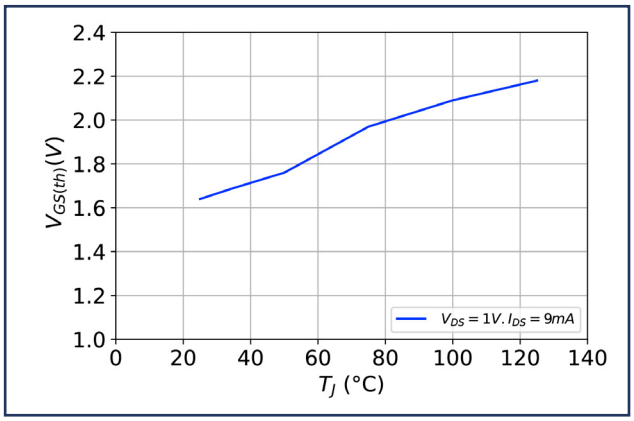


Figure 11. $R_{DS(ON)}$ vs. Temperature

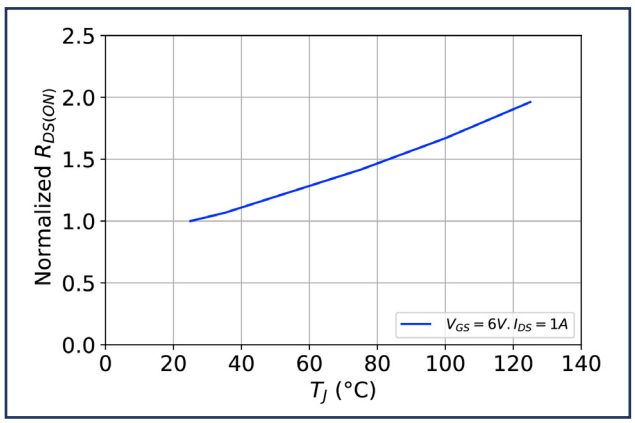


Figure 12. Transfer characteristics

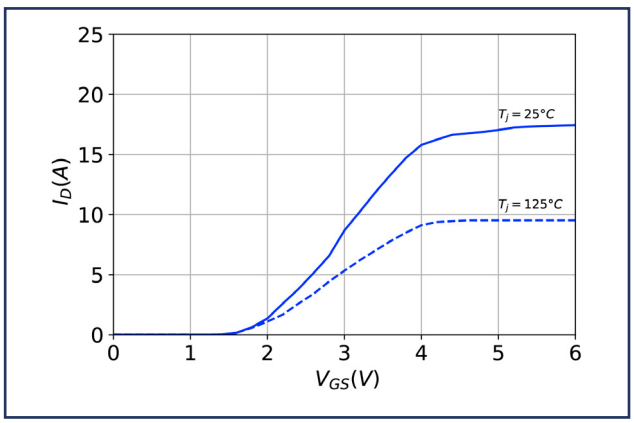


Figure 13. Reverse Conduction

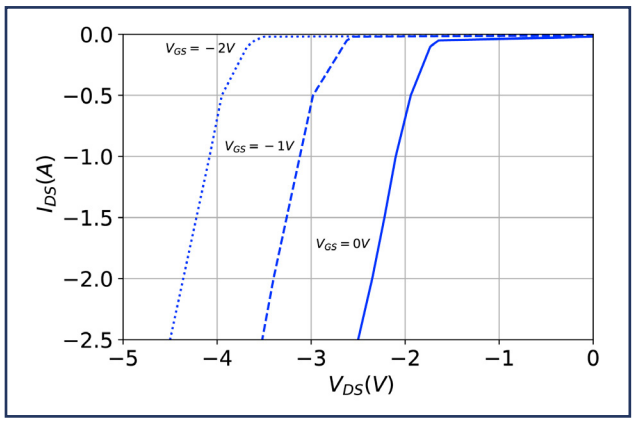
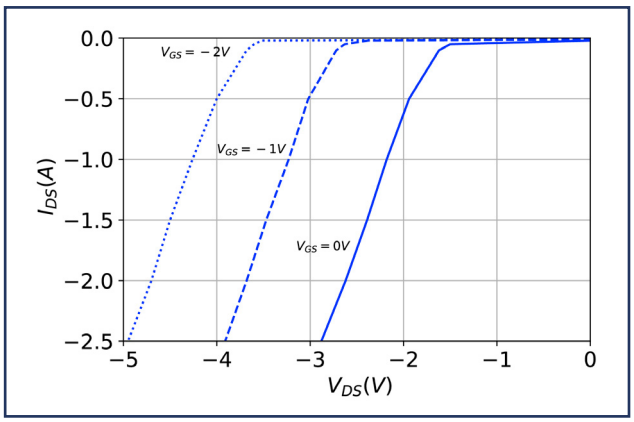
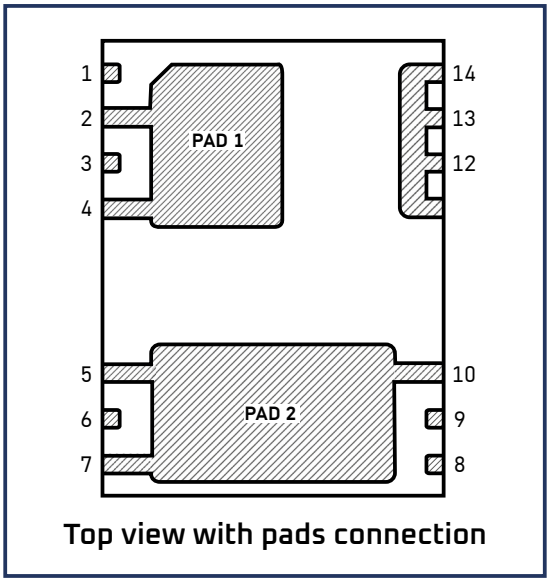


Figure 14. Reverse Conduction T_J = 125°C



Package and Packing information

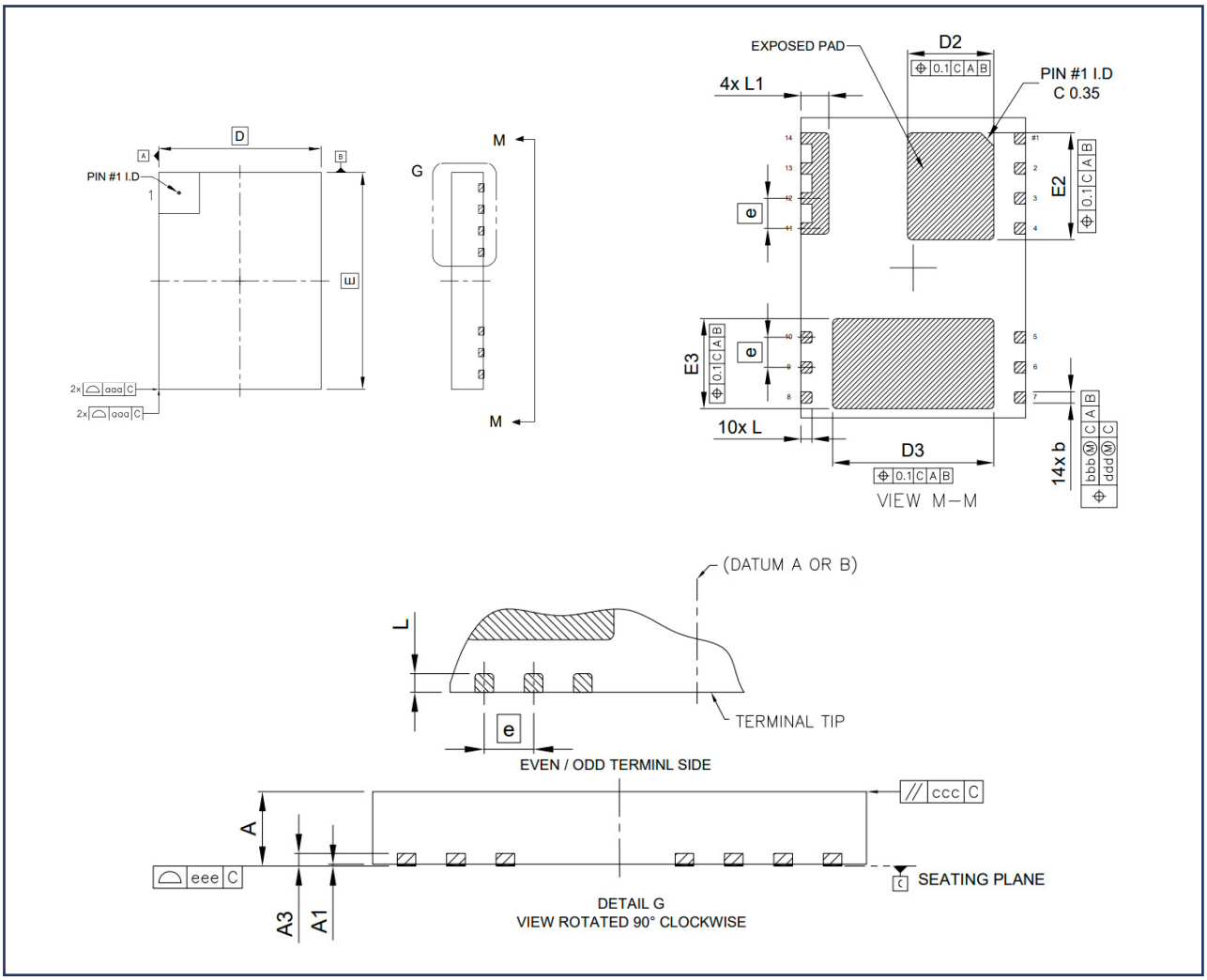
Pinout



Top view with pads connection

Number	Name	Function	Description
1	G1	Signal	Gate of high side GaN transistor
2	S1	Signal	Kelvin source of high side GaN transistor
3		NC	Not connected pin
4	OUT	Supply	Connected to PAD 1
5		UNC	Connected to PAD 2. Mechanical, leave unconnected.
6	G2	Signal	Gate of low side GaN transistor
7	S2	Signal	Kelvin source of low side GaN transistor
8		NC	Not connected pin
9		NC	Not connected pin
10		UNC	Connected to PAD 2. Mechanical, leave unconnected.
11	VIN	Power	Drain of high side GaN transistor
12	VIN	Power	Drain of high side GaN transistor
13	VIN	Power	Drain of high side GaN transistor
14	VIN	Power	Drain of high side GaN transistor
PAD1	OUT	Power	Source of high side and drain of low side GaN transistor
PAD2	GND	Power	Source of low side GaN transistor

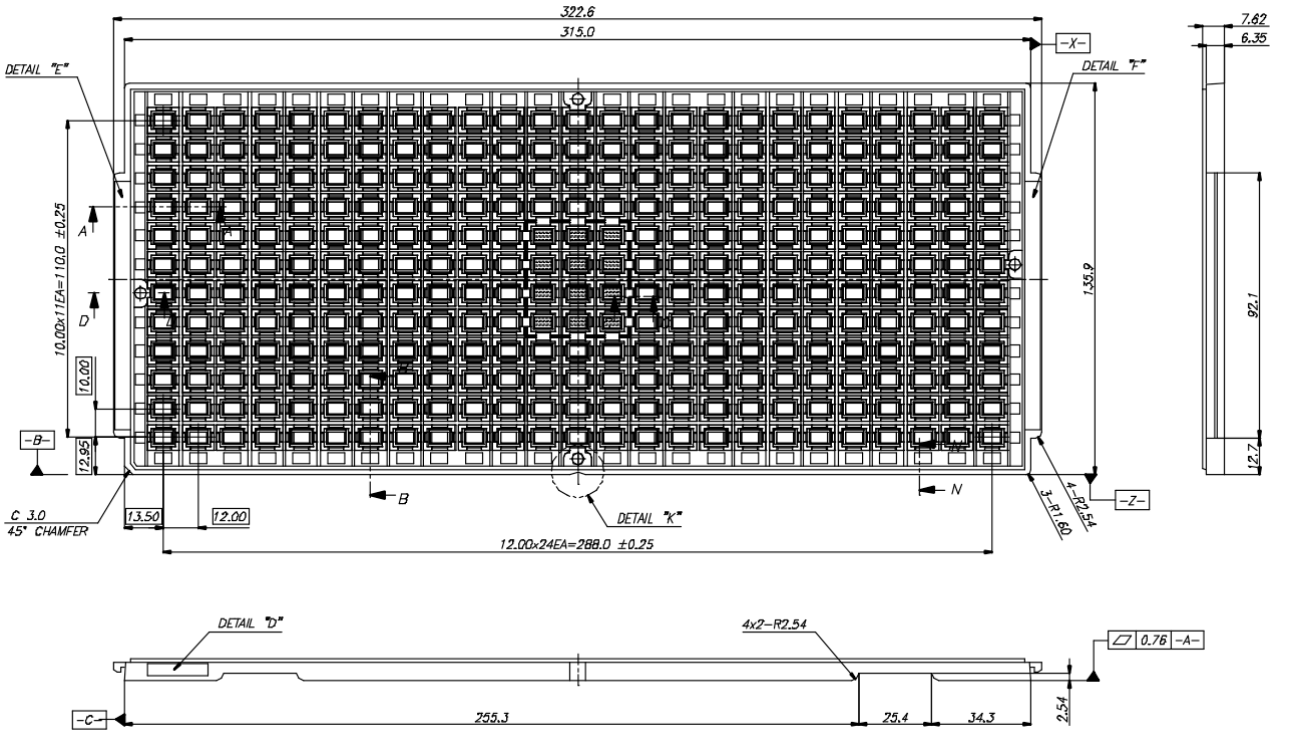
Package Outline Drawing



Dim	Min	Nom	Max	Unit
A	1.15	1.20	1.25	mm
A1	0.00		0.05	mm
A3		0.203 REF		mm
b	0.25	0.30	0.35	mm
D		6.00BSC		mm
E		8.00 BSC		mm
D2	2.20	2.30	2.40	mm
E2	2.75	2.85	2.95	mm
D3	4.20	4.30	4.40	mm

Dim	Min	Nom	Max	Unit
E3	2.30	2.40	2.50	mm
e		0.80 BSC		mm
L	0.25	0.30	0.35	mm
L1	0.70	0.75	0.80	mm
aaa		0.10		mm
bbb		0.10		mm
ccc		0.10		mm
ddd		0.05		mm
eee		0.08		mm

Tray dimensions



All dimensions are in mm.

Ordering Information

Ordering code	Package type	Packing method	Qty	Tray Qty	Box tray
WI62120AT	6 x 8 mm PQFN	Tray	1500	12 x 25 parts	5

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