Brief Description

The ZSC31015 is adjustable to nearly all piezo-resistive bridge sensors. Measured and corrected bridge values are provided at the SIG™ pin, which can be configured as an analog voltage output or as a one-wire serial digital output.

The digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSC31015 and a specific sensor are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or laser. Integrated diagnostics functions make the ZSC31015 particularly well suited for automotive applications.*

Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Programmable analog gain and digital gain; accommodates bridges with spans < 1mV/V and high offset
- Many diagnostic features on chip (e.g., EEPROM signature, bridge connection checks, bridge short detection, power loss detection)
- Independently programmable high and low clipping levels
- 24-bit customer ID field for module traceability
- Internal temperature compensation reference (no external components)
- Option for external temperature compensation with addition of single diode
- Output options: rail-to-rail ratiometric analog voltage (12-bit resolution), absolute analog voltage, digital one-wire interface
- Fast power-up to data out response; output available 5ms after power-up
- Current consumption depends on programmed sample rate: 1mA down to 250µA (typical)
- Fast response time: 1ms (typical)
- High voltage protection up to 30V with external JFET

Benefits

- No external trimming components required
- Simple PC-controlled configuration and calibration via one-wire interface
- High accuracy: ±0.1% FSO @ -25 to 85°C; ±0.25% FSO @ -50 to 150°C
- Single-pass calibration – quick and precise

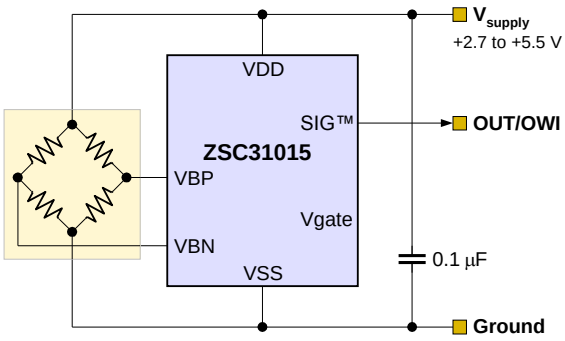
Available Support

- Evaluation Kit available
- Mass Calibration System available
- Support for industrial mass calibration available
- Quick circuit customization possible for large production volumes

Physical Characteristics

- Wide operation temperature: –50°C to +150°C
- Supply voltage 2.7 to 5.5V; with external JFET, 5.5 to 30V
- Small SOP8 package

ZSC31015 Application Circuit



* Not AEC-Q100-qualified.

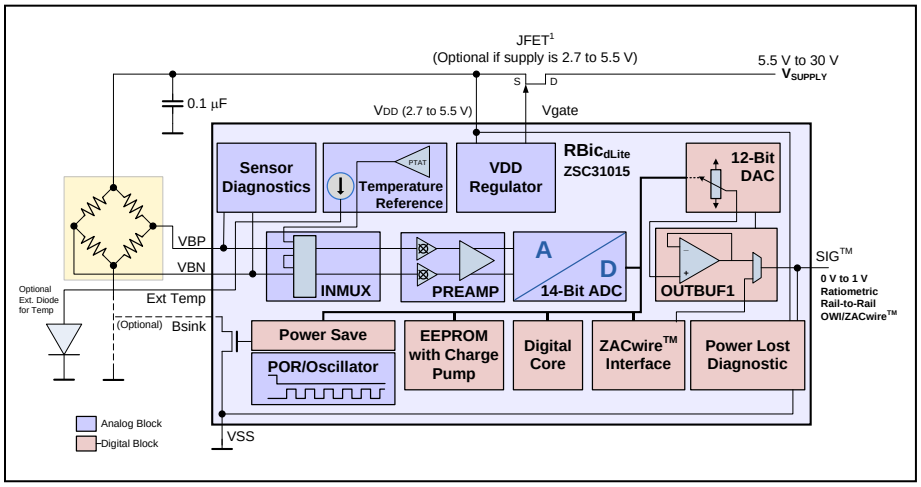
© 2019 Renesas Electronics Corporation

ZSC31015 Block Diagram

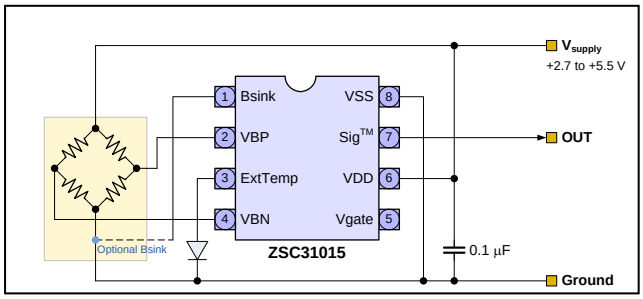
Highly Versatile Applications in Many Markets Including

- *Industrial*
- *Building Automation*
- *Office Automation*
- *White Goods*
- *Automotive **
- *Portable Devices*
- *Your Innovative Designs*

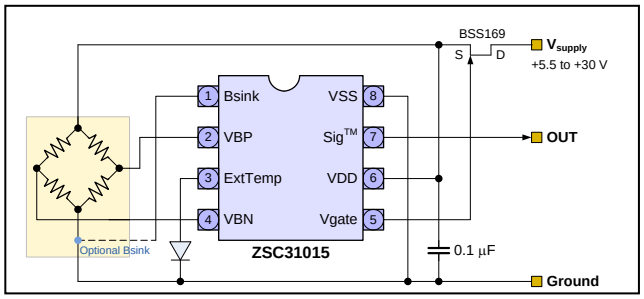
* Not AEC-Q100-qualified.



Rail-to-Rail Ratiometric Voltage Output Applications



Absolute Analog Voltage Output Applications



Ordering Examples *(See section 11 of the data sheet for additional temperature range options.)*

Sales Code	Description	Package
ZSC31015EEB	ZSC31015 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSC31015EEC	ZSC31015 Die — Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSC31015EEG1	ZSC31015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube: add “-T” to sales code. Reel: add “-R”
ZSC31015KIT	ZSC31015 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (SOP8 150mil) (ZACwire™ SSC Evaluation Software can be downloaded from www.IDT.com/ZSC31015)	Kit

Contents

1 Electrical Characteristics 7
1.1. Absolute Maximum Ratings 7
1.2. Recommended Operating Conditions 7
1.3. Electrical Parameters 8
1.3.1. Supply/Regulation Characteristics 8
1.3.2. Parameters for Analog Front-End (AFE) 8
1.3.3. Parameters for EEPROM 8
1.3.4. Parameters for A/D Converter 8
1.3.5. Parameters for Analog Output (DAC and Buffer) 8
1.3.6. Diagnostics 9
1.3.7. External Temperature Measurement 9
1.3.8. Parameters for ZACwire™ Serial Interface 9
1.3.9. Parameters for System Response 9
1.4. Analog Inputs versus Output Resolution 10
2 Circuit Description 13
2.1. Signal Flow and Block Diagram 13
2.2. Analog Front End 14
2.2.1. Bandgap/PTAT and PTAT Amplifier 14
2.2.2. Bridge Supply 14
2.2.3. PREAMP Block 14
2.2.4. Analog-to-Digital Converter (ADC) 15
2.3. Digital Signal Processor 15
2.3.1. EEPROM 17
2.3.2. One-Wire Interface – ZACwire™ 17
2.4. Output Stage 17
2.4.1. Digital to Analog Converter (Output DAC) with Programmable Clipping Limits 17
2.4.2. Output Buffer 18
2.4.3. Voltage Reference Block 18
2.5. Clock Generator / Power-On Reset (CLKPOR) 20
2.5.1. Trimming the Oscillator 20
2.6. Diagnostic Features 20
2.6.1. EEPROM Integrity 21
2.6.2. Sensor Connection Check 21
2.6.3. Sensor Short Check 22
2.6.4. Power Loss Detection 22
2.6.5. ExtTemp Connection Checks 22
3 Functional Description 23

© 2019 Renesas Electronics Corporation

3.1. General Working Mode 23
3.2. ZACwire™ Communication Interface 25
3.2.1. Properties and Parameters 25
3.2.2. Bit Encoding 25
3.2.3. Write Operation from Master to ZSC31015 26
3.2.4. ZSC31015 Read Operations 26
3.2.5. High Level Protocol 29
3.3. Command/Data Bytes Encoding 30
3.4. Calibration Sequence 31
3.5. EEPROM Bits 33
3.6. Calibration Math 37
3.6.1. Correction Coefficients 37
3.6.2. Interpretation of Binary Numbers for Correction Coefficients 37
3.7. Reading EEPROM Contents 41
4 Application Circuit Examples 42
4.1. Three-Wire Rail-to-Rail Ratiometric Output 42
4.2. Absolute Analog Voltage Output 43
4.3. Three-Wire Ratiometric Output with Over-Voltage Protection 44
4.4. Digital Output 44
4.5. Output Resistor/Capacitor Limits 44
5 EEPROM Restoration 45
5.1. Default EEPROM Contents 45
5.1.1. Osc_Trim 45
5.1.2. 1V_Trim/JFET_Trim 45
5.2. EEPROM Restoration Procedure 45
6 Pin Configuration and Package 47
7 ESD/Latch-Up-Protection 48
8 Test 48
9 Quality and Reliability 48
10 Customization 48
11 Part Ordering Codes 49
12 Related Documents 49
13 Definitions of Acronyms 50
14 Document Revision History 51

© 2019 Renesas Electronics Corporation

List of Figures

Figure 2.1 ZSC31015 Block Diagram 13
Figure 2.2 DAC Output Timing for Highest Update Rate 18
Figure 3.1 General Working Mode 24
Figure 3.2 Manchester Duty Cycle 25
Figure 3.3 19-Bit Write Frame 26
Figure 3.4 Read Acknowledge 26
Figure 3.5 Digital Output (NOM) Bridge Readings 27
Figure 3.6 Digital Output (NOM) Bridge Readings with Temperature 27
Figure 3.7 Read EEPROM Contents 28
Figure 3.8 Transmission of a Number of Data Packets 28
Figure 3.9 ZACwire™ Output Timing for Lower Update Rates 29
Figure 4.1 Rail-to-Rail Ratiometric Voltage Output – Temperature Compensation via External Diode 42
Figure 4.2 Absolute Analog Voltage Output – Temperature Compensation via Internal Temperature PTAT with External JFET Regulation 43
Figure 4.3 Ratiometric Output, Temperature Compensation via Internal Diode 44
Figure 5.1 EEPROM Validation and Restoration Procedure 46
Figure 6.1 ZSC31015 Pin-Out Diagram 47

© 2019 Renesas Electronics Corporation

List of Tables

Table 1.1 ADC Resolution Characteristics for an Analog Gain of 6 10
Table 1.2 ADC Resolution Characteristics for an Analog Gain of 24 11
Table 1.3 ADC Resolution Characteristics for an Analog Gain of 48 11
Table 1.4 ADC Resolution Characteristics for an Analog Gain of 96 12
Table 2.1 1V Reference Trim (1V vs. Trim for Nominal Process Run) 19
Table 2.2 Oscillator Trimming 20
Table 2.3 Summary of Diagnostic Features 21
Table 3.1 Pin Configuration and Latch-Up Conditions 25
Table 3.2 Special Measurement/Idle Time between Packets versus Update Rate 28
Table 3.3 Total Transmission Time for Different Update Rate Settings and Output Configuration 29
Table 3.4 Command/Data Bytes Encoding 30
Table 3.5 ZSC31015 EEPROM Bits 33
Table 3.6 Correction Coefficients 37
Table 3.7 Gain_B [13:0] Weightings 38
Table 3.8 Offset_B Weightings 38
Table 3.9 Gain_T Weightings 39
Table 3.10 Offset_T Weightings 39
Table 3.11 EEPROM Read Order 41
Table 6.1 Storage and Soldering Conditions for SOP-8 Package 47
Table 6.2 ZSC31015 Pin Configuration 47

© 2019 Renesas Electronics Corporation

1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Note: The absolute maximum ratings are stress ratings only. The device might not function or be operable above the operating conditions given in section 1.2. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_{DD}	-0.3	6.0	V
Voltages at Analog I/O – In Pin	V_{INA}	-0.3	VDD+0.3	V
Voltages at Analog I/O – Out Pin	V_{OUTA}	-0.3	VDD+0.3	V
Storage Temperature Range (≥10 hours)	T_{STOR}	-50	150	°C
Storage Temperature Range (<10 hours)	$T_{STOR<10h}$	-50	170	°C

Note: Also see Table 6.1 regarding soldering temperature and storage conditions.

1.2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage to Ground	V_{DD}	2.7	5.0	5.5	V
Analog Supply Voltage (with external JFET Regulator)	V_{SUPP}	5.5	7	30	V
Common Mode Voltage	V_{CM}	1		V_{DD} – 1.3	V
Ambient Temperature Range [1), 2)]	T_{AMB}	-50		150	°C
External Capacitance between V_{DD} and Ground	C_{VDD}	100	220	470	nF
Output Load Resistance to V_{DD} [3)]	$R_{L,OUT}$	5			kΩ
Output Load Resistance to VSS [3),4)]	$R_{L,OUT}$	5			kΩ
Output Load Capacitance [5)]	$C_{L,OUT}$	1	10	15	nF
Bridge Resistance [6),7)]	R_{BR}	0.3		100	kΩ
Power-On Rise Time	t_{PON}			100	ms

1) Note that the maximum EEPROM programming temperature is 85°C.
2) If buying die, designers should use caution not to exceed maximum junction temperature by proper package selection.
3) Only needed for Analog Output Mode; not needed for Digital Output Mode. When a pull-down resistor is used as the load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at R_L=5k; R_L=10k is recommended for this configuration.
4) Note: for unlocked devices or during calibration, the minimum value of output load resistance to VSS is 20kΩ.
5) Using the output for digital calibration, $C_{L,OUT}$ is limited by the maximum rise time $t_{ZAC,rise}$. See section 1.3.8.
6) Note: Minimum bridge resistance is a factor if using the Bsink feature. The rds(on) of the Bsink transistor is 8 to 10Ω when operating at V_{DD}=5V. This does give rise to a ratiometricity inaccuracy that becomes greater with low bridge resistances.
7) Note: Minimum bridge resistance is important if using certain diagnostic features. It must be at least 0.3kΩ at V_{DD}=2.7V and at least 0.6kΩ at V_{DD}=5V for the Sensor Short Check to function properly. For details, see section 2.6.3.

© 2019 Renesas Electronics Corporation

1.3. Electrical Parameters

See important table notes at the end of the table. Note: For parameters marked with an asterisk, there is no verification in mass production; the parameter is guaranteed by design and/or quality observation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.1. Supply/Regulation Characteristics						
Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Supply Current (varies with update rate and output mode)	I_{DD}	At minimum update rate		0.25		mA
		At maximum update rate		1.0	1.4	
Temperature Coefficient – PTAT Source *	T_{CPTAT}			20	100	ppm/K
Power Supply Rejection Ratio *	PSRR		60			dB
Power-On Reset Level	POR		1.4		2.6	V
1.3.2. Parameters for Analog Front-End (AFE)						
Leakage Current Pin VBP,VBN	I_{IN_LEAK}	Sensor connection and short check must be disabled.			±10	nA
1.3.3. Parameters for EEPROM						
Number Write Cycles	n_{WRI_EEP}	At 150°C			100	Cycles
		At 85°C			100k	Cycles
Data Retention	t_{WRI_EEP}	At 100°C			10	Years
1.3.4. Parameters for A/D Converter						
ADC Resolution	r_{ADC}				14	Bit
Integral Nonlinearity (INL) [1)]	INL_{ADC}	Based on ideal slope	-4		+4	LSB
Differential Nonlinearity (DNL) *	DNL_{ADC}		-1		+1	LSB
1.3.5. Parameters for Analog Output (DAC and Buffer)						
Max. Output Current	I_{OUT}	Max. current maintaining accuracy	2.2			mA
Resolution	Res	Referenced to V_{DD}			12	Bit
Absolute Error	E_{ABS}	DAC input to output			±0.2%	V_{DD}
Differential Nonlinearity *	DNL	No missing codes	-0.9		+3.0	LSB_{12Bit}
Upper Output Voltage Limit	V_{OUT}	R_L = 5 kΩ	95%			V_{DD}
Lower Output Voltage Limit	V_{OUT}	With 5kΩ pull down, 0 to1V output			16.5mV	mV
Output Short Circuit Protection Limit	I_{SC}	Depends on operating conditions. Short circuit protection must be enabled via Diag_cfg (EEPROM word [102:100]). See section 2.4.2.	3		40	mA
Analog Output Noise Peak-to-Peak	$V_{NOISE,PP}$	Shorted input			5 ±1LSB	mV

© 2019 Renesas Electronics Corporation

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1.3.6. Diagnostics						
Upper diagnostic output level	$V_{DIA,H}$		97.5%			V_{DD}
Lower diagnostic output level	$V_{DIA,L}$				2.5%	V_{DD}
Minimum load resistor for power loss [2)]	R_{L,OUT_PS}	Pull-up or pull-down in Analog Output Mode	5			kΩ
1.3.7. External Temperature Measurement						
External Temperature (ExtTemp) Signal Input Range	V_{TSE}		150		800	mV
Required External Temperature Diode Sensitivity	ST_{TSE}		1.9		3.25	mV/K
Temperature Span with External Temperature Diode	T_{TSE_SP}		-50		150	°C
1.3.8. Parameters for ZACwire™ Serial Interface						
ZACwire™ Line Resistance *	$R_{ZAC,load}$	The rise time must be $t_{ZAC,rise} = 2 * R_{ZAC,load} * C_{ZACload} \leq 5\mu s$. If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.			3.9	kΩ
ZACwire™ Load Capacitance *	$C_{ZAC,load}$		0	1	15	nF
Voltage Level Low *	$V_{ZAC,low}$			0	0.2	V_{DD}
Voltage Level High *	$V_{ZAC,low}$		0.8	1		V_{DD}
1.3.9. Parameters for System Response						
Start-Up-Time	t_{STA}	Power-up to output Update_rate = 1 kHz (1 ms)			8	ms
Response Time – Analog Output	t_{RESP-A}	Update_rate = 1 kHz (1 ms)		1	2	ms
Response and Transmission Time for Digital Output	$t_{RES,\ DIG}$	Varies with update rate. Value given at fastest rate.		1.6		ms
Sampling Rate	f_S	Update_rate = 1 kHz (1 ms)		1000		Hz
Overall Linearity Error– Digital	E_{LIND}	Bridge input to output		0.025	0.04	%
Overall Linearity Error – Analog	E_{LINA}	Bridge input to output		0.1	0.2	%
Overall Ratiometricity Error	RE_{out}	±10%VDD, Not using Bsink feature			0.035	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Overall Accuracy – Digital (only IC, without sensor bridge)	AC_{outD}	-25°C to 85°C			±0.1%	%FSO
		-50°C to 150°C			±0.25%	
Overall Accuracy – Analog [3), 4)] (only IC, without sensor bridge)	AC_{outA}	-25°C to 85°C			±0.25%	%FSO
		-40°C to 125°C			±0.35%	
		-50°C to 150°C			±0.5%	

1) Note: This is ± 4 LSBs for the 14-bit A-to-D conversion. This results in absolute accuracy to 12-bits on the A-to-D result. Non-linearity is typically better at temperatures less than 125°C.
2) When using a pull-down resistor as the load resistor, the power loss detection diagnostic for loss of VSS cannot be assured at R_L=5kΩ; R_L=10kΩ is recommended for this configuration.
3) Not included is the quantization noise of the DAC. The 12-bit DAC has a quantization noise of ± ½ LSB = 0.61mV (@ 5V VDD) = 0.0125%.
4) Analog output range 2.5% to 95%

1.4. Analog Inputs versus Output Resolution

The ZSC31015 has a fully differential chopper-stabilized pre-amplifier with four programmable gain settings. The output of the pre-amplifier feeds into a 14-bit charge-balanced ADC. Span, offset, temperature, and non-linearity correction are performed in the digital domain. Then the resulting corrected bridge value can be output in analog form through a 12-bit DAC or as a 16-bit serial digital packet. The resolution of the output depends on the input span (bridge sensitivity) and the analog gain setting programmed. Digital gains can vary from [0,32). Analog gains available are 6, 24, 48, and 96.

Note: At higher analog gain settings, there will be higher output resolution, but the ability of the ZSC31015 to handle large offsets decreases. This is expected because the offset is also amplified by the analog gain and can therefore saturate the ADC input.

The following tables outline the guaranteed minimum resolution for a given bridge sensitivity range.

Table 1.1 ADC Resolution Characteristics for an Analog Gain of 6

Analog Gain 6				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
57.8	80.0	105.8	38%	12.4
50.6	70.0	92.6	53%	12.2
43.4	60.0	79.4	73%	12.0
36.1	50.0	66.1	101%	11.7
28.9	40.0	52.9	142%	11.4
21.7	30.0	39.7	212%	11.4

1) In addition to Tco, Tcg.

Table 1.2 ADC Resolution Characteristics for an Analog Gain of 24

Analog Gain 24				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
18.1	25.0	33.1	17%	12.7
14.5	20.0	26.5	38%	12.4
7.2	10.0	13.2	142%	11.4
3.6	5.0	6.6	351%	10.4
1.8	2.5	3.3	767%	9.4
0.9	1.2	1.6	1670%	8.4

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

Table 1.3 ADC Resolution Characteristics for an Analog Gain of 48

Analog Gain 48				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
10.8	15.0	19.8	3%	13.0
7.2	10.0	13.2	38%	12.4
4.3	6.0	7.9	107%	11.7
2.9	4.0	5.3	194%	11.1
1.8	2.5	3.3	351%	10.4
1.0	1.4	1.85	678%	9.6
0.72	1.0	1.32	976%	9.1

1) In addition to Tco, Tcg.

Important Note: The yellow shadowed fields indicate that for these input spans with the selected analog gain setting, the quantization noise is higher than 0.1% FSO.

© 2019 Renesas Electronics Corporation

Table 1.4 ADC Resolution Characteristics for an Analog Gain of 96

Analog Gain 96				
Input Span [mV/V]			Allowed Offset (+/- % of Span) [1]	Minimum Guaranteed Resolution [Bits]
Min	Typ	Max		
4.3	6.0	7.9	21%	12.7
2.9	4.0	5.3	64%	12.1
1.8	2.5	3.3	142%	11.4
1.0	1.4	1.85	306%	10.6
0.72	1.0	1.32	455%	10.1

1) In addition to Tco, Tcg.

2 Circuit Description

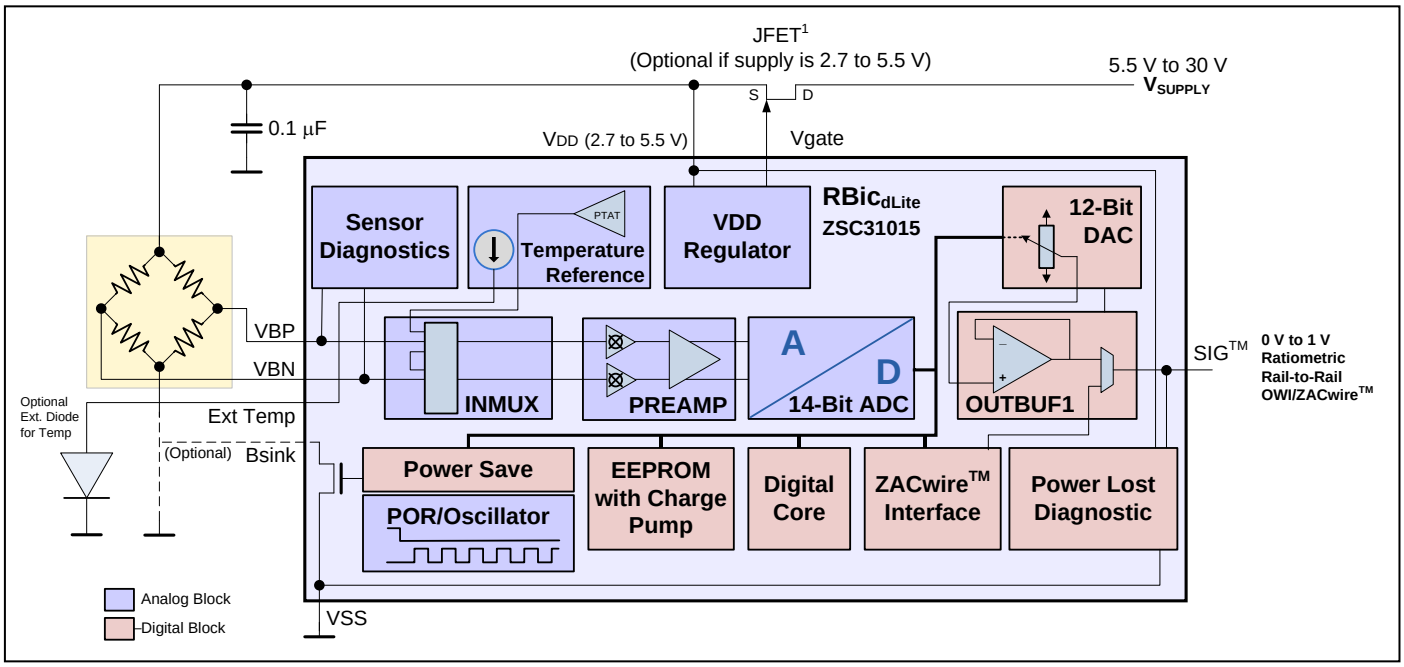
2.1. Signal Flow and Block Diagram

The ZSC31015 resistive bridge sensor interface ICs were specifically designed as cost-effective solutions for sensing in building automation, automotive *, industrial, office automation and white goods applications. The ZSC31015 employs IDT's high precision bandgap with proportional-to-absolute-temperature (PTAT) output; low-power 14-bit analog-to-digital converter (ADC, A2D, A-to-D); and an on-chip DSP core with EEPROM to precisely calibrate the bridge output signal.

Three selectable outputs, two analog and one digital, offer the ultimate in versatility across many applications. The ZSC31015 rail-to-rail ratiometric analog V_{out} signal (0V to ~5 V V_{out} @ V_{DD}=5V) suits most building automation and automotive requirements (12-bit resolution). Typical office automation and white goods applications require the 0 to ~1V V_{out} signal, which in the ZSC31015 is referenced to the internal bandgap. The ZSC31015 is capable of running in high-voltage (5.5 to 30V) systems when combined with an external JFET.

Direct interfacing to µP controllers is facilitated via IDT's single-wire serial ZACwire™ digital interface.

Figure 2.1 ZSC31015 Block Diagram



* Not AEC-Q100-qualified.

2.2. Analog Front End

2.2.1. Bandgap/PTAT and PTAT Amplifier

The highly linear Bandgap/PTAT section provides the PTAT signal to the ADC, which allows accurate temperature conversion. In addition, the ultra-low ppm Bandgap provides a stable voltage reference over temperature for the operation of the rest of the IC. If the bridge is not near the ZSC31015, an external diode can be used for temperature measurement/compensation.

The temperature signal (internal PTAT or external diode) is amplified through a path in the Pre-Amp and fed to the ADC for conversion. The most significant 12-bits of this converted result are used for temperature measurement and temperature correction of bridge readings. When temperature is output in Digital Mode, only the most significant 8 bits are given.

When external temperature is selected, add a diode from the ExtTemp pin to ground. The diode is biased with approximately 50µA during temperature measurement cycles. The voltage level on ExtTemp is amplified through the Pre-Amp and converted by the ADC. Ensure that the ExtTemp signal is in the range of 150mV to 800mV to prevent saturation of the ADC. If the selected diode has a sensitivity in the range of 1.9mV/^{o}C to 3.25mV/^{o}C, a corrected temperature output (in Digital Mode) can be achieved for a 200^{o}C temperature span (-50^{o}C to 150^{o}C).

2.2.2. Bridge Supply

The voltage-driven bridge is usually connected to V_{DD} and ground. As a power savings feature, the ZSC31015 also includes a switched transistor to interrupt the bridge current via pin 1 (Bsink). The transistor switching is synchronized to the analog-to-digital conversion and released after finishing the conversion. To utilize this feature, the low supply of the bridge should be connected to Bsink instead of ground.

Depending on the programmable update rate, the average current consumption (including bridge current) can be reduced to approximately 20%, 5%, or 1%. Note: this feature has no power savings benefit if using the fastest update rate mode.

2.2.3. PREAMP Block

The differential signal from the bridge is amplified through a chopper-stabilized instrumentation amplifier with very high input impedance designed for low noise and low drift. This pre-amp provides gain for the differential signal and re-centers its DC to V_{DD}/2. The output of the Pre-Amp block is fed into the ADC. The calibration sequence performed by the digital core includes an auto-zero sequence to null any drift in the Pre-Amp state over temperature.

The Pre-Amp can be set to a gain of 6, 24, 48, or 96 through an EEPROM setting.

The inputs to the Pre-Amp from (VBN/VBP pins) can be reversed via an EEPROM configuration bit.

© 2019 Renesas Electronics Corporation

2.2.4. Analog-to-Digital Converter (ADC)

A 14-bit/1ms 2nd order charge-balancing ADC is used to convert signals coming from the pre-amplifier. The converter, designed in full differential switched capacitor technique, is used for converting the various signals in the digital domain.

This principle offers the following advantages:

- High noise immunity because of the differential signal path and integrating behavior
- Independence from clock frequency drift and clock jitter
- Fast conversion time due to second-order mode

Four selectable values for the zero point of the input voltage allow conversion to adapt to the sensor's offset parameter. With the Reverse Input Polarity Mode and the negative digital gain options, this results in seven possible zero point adjustments (not eight because the -1/2,1/2 offset setting is the same regardless of gain polarity).

The conversion rate varies with the programmed update rate. The fastest conversation rate is 1k samples/s and the response time is then 1ms. Based on a best fit, the Integral Nonlinearity (INL) is less than 4 LSB_{14Bit}.

2.3. Digital Signal Processor

A digital signal processor (DSP) is used for processing the converted bridge data as well as performing temperature correction and computing the temperature value for output on the digital channel.

The digital core reads correction coefficients from EEPROM and can correct for the following:

- Bridge Offset
- Bridge Gain
- Variation of Bridge Offset over Temperature (Tco)
- Variation of Bridge Gain over Temperature (Tcg)
- A single second order effect (SOT) (Second Order Term)

The EEPROM contains a single SOT that can be applied to correct one and only one of the following:

- 2nd order behavior of bridge measurement
- 2nd order behavior of Tco
- 2nd order behavior of Tcg

© 2019 Renesas Electronics Corporation

If the SOT applies to correcting the bridge reading, then the correction formula for the bridge reading is represented as a two-step process as follows:

$$ZB = Gain_B(1 + \Delta T * Tcg) * (BR_Raw - Offset_B + \Delta T * Tco) \quad (1)$$

$$BR = ZB(1.25 + SOT * ZB) \quad (2)$$

Where:

BR	=	Corrected Bridge reading that is output as digital or analog on the SIG™ pin
ZB	=	Intermediate result in the calculations
BR_Raw	=	Raw Bridge reading from ADC
T_Raw	=	Raw Temp reading converted from PTAT signal or external diode
Gain_B	=	Bridge Gain term
Offset_B	=	Bridge Offset term
Tcg	=	Temperature Coefficient Gain
Tco	=	Temperature Coefficient Offset
ΔT	=	(**T_Raw – T_{SETL}**)
T_{SETL}	=	T_Raw reading at which low calibration was performed (typically 25°C)
SOT	=	Second-Order Term

Note For solving equation (1) the following condition must be met:

$$BR_Raw \geq BR / Gain_B$$

If this condition is not met, the analog Pre-Amp Gain must be set to a smaller value because a negative Offset_B is not supported.

If the **SOT** applies to correcting the 2nd order behavior of **Tco**, then the formula for bridge correction is as follows:

$$BR = Gain_B(1 + \Delta T * Tcg) * [BR_Raw - Offset_B + \Delta T(SOT * \Delta T + Tco)] \quad (3)$$

If the SOT applies to correcting the 2nd order behavior of Tcg, then the formula for bridge correction is as follows:

$$BR = Gain_B[1 + \Delta T(SOT * \Delta T + Tcg)] * [BR_Raw - Offset_B + \Delta T * Tco] \quad (4)$$

The bandgap reference gives a very linear PTAT signal, so temperature correction can always simply be accomplished with a linear gain and offset term.

© 2019 Renesas Electronics Corporation

Corrected Temperature Reading:

$$T = Gain_T(T_Raw + Offset_T) \quad (5)$$

Where:

T_Raw = Raw Temperature reading converted from PTAT signal or external diode

Offset_T = Offset Coefficient for Temperature

Gain_T = Gain Coefficient for Temperature

2.3.1. EEPROM

The EEPROM contains the calibration coefficients for gain and offset, etc., and the configuration bits, such as output mode, update rate, etc. The ZSC31015 also offers three user-programmable storage bytes for module traceability. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed. The EEPROM is implemented as a shift register. During an EEPROM read, the contents are shifted 8 bits before each transmission of one byte occurs. The charge pump is internally regulated to 12.5 V, and the programming time is 6ms.

See section 2.6.1 regarding EEPROM signatures for verifying EEPROM integrity.

Note: EEPROM writing can only be performed at temperatures lower than 85ºC.

2.3.2. One-Wire Interface – ZACwire™

The IC communicates via a one-wire serial interface. There are different commands available for the following:

- Reading the conversion result of the ADC (Get_BR_Raw, Get_T_Raw)
- Calibration commands
- Reading from the EEPROM (“dump” of entire contents)
- Writing to the EEPROM (trim setting, configuration, and coefficients)

2.4. Output Stage

2.4.1. Digital to Analog Converter (Output DAC) with Programmable Clipping Limits

A 12-bit DAC based on sub-ranging resistor strings is used for the digital-to-analog output conversion in the analog ratiometric and absolute analog voltage modes. Options during calibration configure the system to operate in either of these modes. The design allows for excellent testability as well as low power consumption. The DAC allows programming a lower and upper clipping limit (Low_Clip_Lim and Up_Clip_Lim bit fields respectively; see section 3.5) for the output signal (analog and digital). The internal 14-bit calculated bridge value is compared against the 14-bit value formed by {11,Up_Clip_Lim[6:0],11111} for the upper limit and against {00,Low_Clip_Lim[6:0],00000} for the lower limit. If the calculated bridge value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this value; otherwise it is output as is.

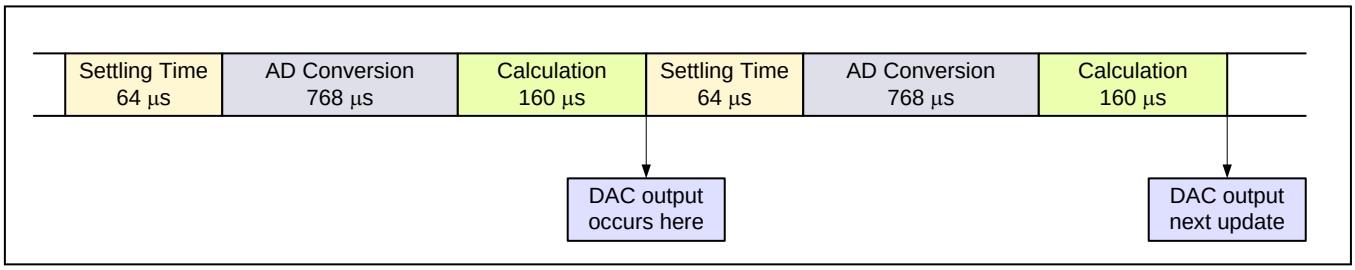
© 2019 Renesas Electronics Corporation

Example for the upper clipping level: If the Up_Clip_Lim[6:0] = 0000000, then the 14-bit value used for the clipping threshold is 11000000011111. This is 75.19% of full scale. Since there are 7 bits of upper clipping limit, there are 127 possible values between 75.19% and 100%. Therefore the resolution of the clipping limits 0.195%.

Example for the lower clipping level: If the Low_Clip_Lim[6:0] = 1111111, then the 14-bit value used for the clipping threshold is 00111111100000. This is 24.8% of full scale. Since there are 7 bits of lower clipping limit, there are 127 possible values between 0 and 24.8%. Therefore the resolution of the lower clipping limit is 0.195%.

Figure 2.2 shows the data timing of the DAC output for the update rate setting 00.

Figure 2.2 DAC Output Timing for Highest Update Rate



2.4.2. Output Buffer

A rail-to-rail op amp configured as a unity gain buffer can drive resistive loads (whether pull-up or pull-down) as low as 5kΩ and capacitances up to 15nF (for pure analog output). In addition, to limit the error due to amplifier offset voltage, an error compensation circuit is included which tracks and reduces offset voltage to < 1mV. The output of the ZSC31015 output can be permanently shorted to VDD or VSS without damaging the device. The output driver contains a current-limiting block that detects a hard short and limits the current to a safe level. The short circuit protection current can vary from a minimum of 3mA to a maximum of 40mA depending on operating conditions. Output short circuit protection can be enabled via Diag_cfg (EEPROM [102:100]). Enabling this protection is recommended when using the analog output.

2.4.3. Voltage Reference Block

A linear regulator control circuit is included in the Voltage Reference Block to interface with an external JFET to allow operation in systems where the supply voltage exceeds 5.5V. This circuit can also be used for over-voltage protection. The regulator set point has a coarse adjustment controlled by the JFET_cfg EEPROM bits that can adjust the set point around 5.0 or 5.5V. (See Table 3.5 for bit locations and section 2.3.1 regarding writing to the EEPROM.). The 1V trim setting (see below) can also act as a fine adjust for the regulation set point. The 5V reference can be trimmed within +/-15mV.

Note: If using the external JFET for over-voltage protection purposes (i.e., 5V at JFET drain and expecting 5V at JFET source), there will be a voltage drop across the JFET; therefore ratiometricity will be slightly compromised depending on the rds(on) of the chosen JFET. A Vishay J107 is the best choice because it has only an 8mV drop worst case. If using as regulation instead of over-voltage protection, a MMBF4392 or BSS169 also works well.

© 2019 Renesas Electronics Corporation

The Voltage Reference Block uses the absolute reference voltage provided by the bandgap to produce two regulated on-chip voltage references. A 1V reference is used for the output DAC high reference when the part is configured in 0-1V Analog Output Mode. For this reason, the 1V reference must be very accurate and includes trim so that its value can be trimmed within +/- 3mV of 1.00V. The 1V reference is also used as the on-chip reference for the JFET regulator block. The regulation set point of the JFET regulator can be fine-tuned using the 1V trim.

The reference trim setting is selected with the 1V_Trim/JFET_Trim bits in EEPROM. See Table 3.5 for bit locations. Table 2.1 shows the order of trim codes with 0111 for the lowest reference voltage and 1000 for the highest reference voltage.

Important: Optimal reference trim is determined during wafer-level testing and final package testing. Back-up copies of these bits are stored in bits in the CUST_ID0 bits for applications requiring accurate references. In this case, see section 5 for important notes and instructions for verifying the integrity of the 1V_Trim/JFET_Trim bits and if necessary, restoring the value from the CUST_ID0 bits before calibration.

Table 2.1 1V Reference Trim (1V vs. Trim for Nominal Process Run)

Order	1Vref/ 5Vref_trim3	1Vref/ 5Vref_trim2	1Vref/ 5Vref_trim1	1Vref/ 5Vref_trim0
Highest Reference Voltage	1	0	0	0
…	1	0	0	1
…	1	0	1	0
…	1	0	1	1
…	1	1	0	0
…	1	1	0	1
…	1	1	1	0
…	1	1	1	1
…	0	0	0	0
…	0	0	0	1
…	0	0	1	0
…	0	0	1	1
…	0	1	0	0
…	0	1	0	1
…	0	1	1	0
Lowest Reference Voltage	0	1	1	1

© 2019 Renesas Electronics Corporation

2.5. Clock Generator / Power-On Reset (CLKPOR)

If the power supply exceeds 2.5V (maximum), the reset signal de-asserts and the clock generator starts working at a frequency of approximately 512kHz (±20%). The exact value only influences the conversion cycle time and communication to the outside world but not the accuracy of signal processing. In addition, to minimize the oscillator error as the V_{DD} voltage changes, an on-chip regulator is used to supply the oscillator block.

2.5.1. Trimming the Oscillator

Settings for the Osc_Trim bits in EEPROM fine-tune the oscillator frequency. See Table 3.5 for bit locations and Table 2.2 for possible settings. The default value is 0_{HEX} to ensure communication on start-up.

Important: Optimal oscillator trimming is determined during wafer-level testing and final package testing, and this part-specific factory value, which can be copied to Osc_Trim, is stored in bits in the CUST_ID1 and CUST_ID2 EEPROM bits for applications requiring optimal response time. In this case, see section 5 for important notes and instructions for copying these optimal values to the Osc_Trim bits before calibration. It is strongly recommended that only the default value or the factory trim value be used because ZACwire™ communication is not guaranteed at different oscillator frequencies.

Table 2.2 Oscillator Trimming

Osc_Trim Bits	Delta Frequency (kHz)
100	+385
101	+235
110	+140
111	+65
000	Nominal
001	-40
010	-76
011	-110

Example: Programming $011_B \rightarrow$ the trimmed frequency = nominal value – 110 kHz.

2.6. Diagnostic Features

The ZSC31015 offers a full suite of diagnostic features to ensure robust system operation in the most “mission-critical” applications. If the part is programmed in Analog Output Mode, then diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD. If the part is programmed in Digital Output Mode, then diagnostic states will be indicated by a transmission with a generated parity error.

Table 2.3 gives a summary of the diagnostic features, which are explained in detail in the following sections. EEPROM settings that control diagnostic functions are given in section 3.5.

© 2019 Renesas Electronics Corporation

Table 2.3 Summary of Diagnostic Features

Detected Fault	Analog Diagnostic Level	ZACwire™ Diagnostic	Delay in Detection
EEPROM signature	Lower	Generates parity error	10ms after power-on
Loss of bridge positive	Upper	Generates parity error	2ms
Loss of bridge negative	Upper	Generates parity error	2ms
Open bridge connection	Upper	Generates parity error	2ms
Bridge input short	Upper	Generates parity error	2ms
ExtTemp pin open	Lower	Generates parity error	300ms
ExtTemp pin shorted to PWR/GND	Lower	Generates parity error	300ms
ExtTemp pin shorted to BP/BN†	Upper	Generates parity error	3ms
Loss of VDD	Lower	Transmissions stop	Dependent on R_L and C_L
Loss of VSS	Upper	Transmissions stop	Dependent on R_L and C_L

2.6.1. EEPROM Integrity

The contents of the EEPROM are protected by an 8-bit LFSR signature (linear feedback shift register). This signature is regenerated and stored in EEPROM every time EEPROM contents are changed. This signature is generated and checked for a match after Power-On-Reset prior to entering Normal Operation Mode. If the generated signature fails to match, the part will output a diagnostic state on the output.

In addition to an extensive temporal and code interlock mechanism used to prevent false writes to the EEPROM, the ZSC31015 offers an EEPROM lock mechanism for high-security applications. When EEPROM bits 105:103 are programmed with “011” or “110,” this 3-bit field will permanently disable the VPP charge pump and will not allow further writes to the EEPROM. See Table 2.3 in section 2.6 for more information.

2.6.2. Sensor Connection Check

Four dedicated comparators permanently check the range of the bridge inputs (BP/BN) to ensure they are within the envelope of 0.8V to 0.85∗VDD during all conversions. The two sensor inputs have a switched ohmic path to ground and if left floating, would be discharged. If any of the wires connecting the bridge break, this mechanism will detect it and put the ZSC31015 in a diagnostic state. This same diagnostic feature can also detect a short between BP/BN and the ExtTemp signal if an external diode is being used for temperature measurement. See Table 2.3 in section 2.6 for more information.

† A short from ExtTemp to BP/BN might not be detected in some circuit configurations.

© 2019 Renesas Electronics Corporation

2.6.3. Sensor Short Check

If a short occurs between BP/BN (bridge inputs), it would normally produce an in-range output signal and therefore would not be detected as a fault. This diagnostic mode, if enabled, will deliberately look for such a short. After the measurement cycle of the bridge, it will deliberately pull the BP bridge input to ground for 4μsec. At the end of this 4μsec window, it will check to see if the BN input "followed" it down below the 0.8V comparator checkpoint. If so, a short must exist between BP/BN, and the part will output a diagnostic state. The bridge will have a minimum of 480μsec recovery time prior to the next measurement. See Table 2.3 in section 2.6 for more information.

The bridge resistance must be taken into account if the Sensor Short diagnostic feature is used. At V_{DD}= 2.7V, the minimum bridge resistance is 0.3KΩ, and at V_{DD} = 5V, the minimum bridge resistance is 0.6KΩ.

2.6.4. Power Loss Detection

If the power or GND connection to the module containing the sensor bridge and the ZSC31015 is lost, the ZSC31015 will output a diagnostic state if a pull-up or pull-down terminating resistor greater than or equal to 5kΩ is connected in the final application. This diagnostic mode only works when the part is configured in Analog Output Mode. See Table 2.3 in section 2.6 for more information.

2.6.5. ExtTemp Connection Checks

When external temperature is selected and connection checking is enabled, the part performs range checking on the converted temperature value. If the internal ADC reading of the temperature is less than 1/32 of full scale or greater than 63/64 of full scale then a diagnostic state is asserted. If the ExtTemp pin is shorted to ground, the ADC reads less than 1/32. Because 100μA is sourced onto the ExtTemp pin during conversions, it naturally pulls up during these times. If the ExtTemp pin is open, it produces an ADC reading greater than 63/64 of full scale. Both these bad connection conditions would be detected and result in a diagnostic output. If internal temperature is selected or sensor connection check is not enabled, then this diagnostic check is not enabled. See Table 2.3 in section 2.6 for more information.

© 2019 Renesas Electronics Corporation

3 Functional Description

3.1. General Working Mode

The command/data transfer takes place via the one-wire SIG™ pin using the ZACwire™ serial communication protocol.

After power-on, the ZSC31015 waits for 3ms (= Command window) for the Start_CM command.

Without this command, the Normal Operation Mode (NOM) starts. In this mode, raw bridge values are converted, and the corrected values are presented on the output in analog or digital format (depending on the configuration stored in EEPROM).

Command Mode (CM) can only be entered during the 3ms command window after power-on. If the ZSC31015 receives the Start_CM command during the command window, it remains in the Command Mode. The CM allows changing to one of the other modes via command. After the command Start_RW, the ZSC31015 is in the Raw Mode (RM). Without correction, the raw values are transmitted to the digital output in a predefined order. The RM can only be stopped by a power-off. RM is used by the calibration software for collection of raw bridge and temperature data so the correction coefficients can be calculated.

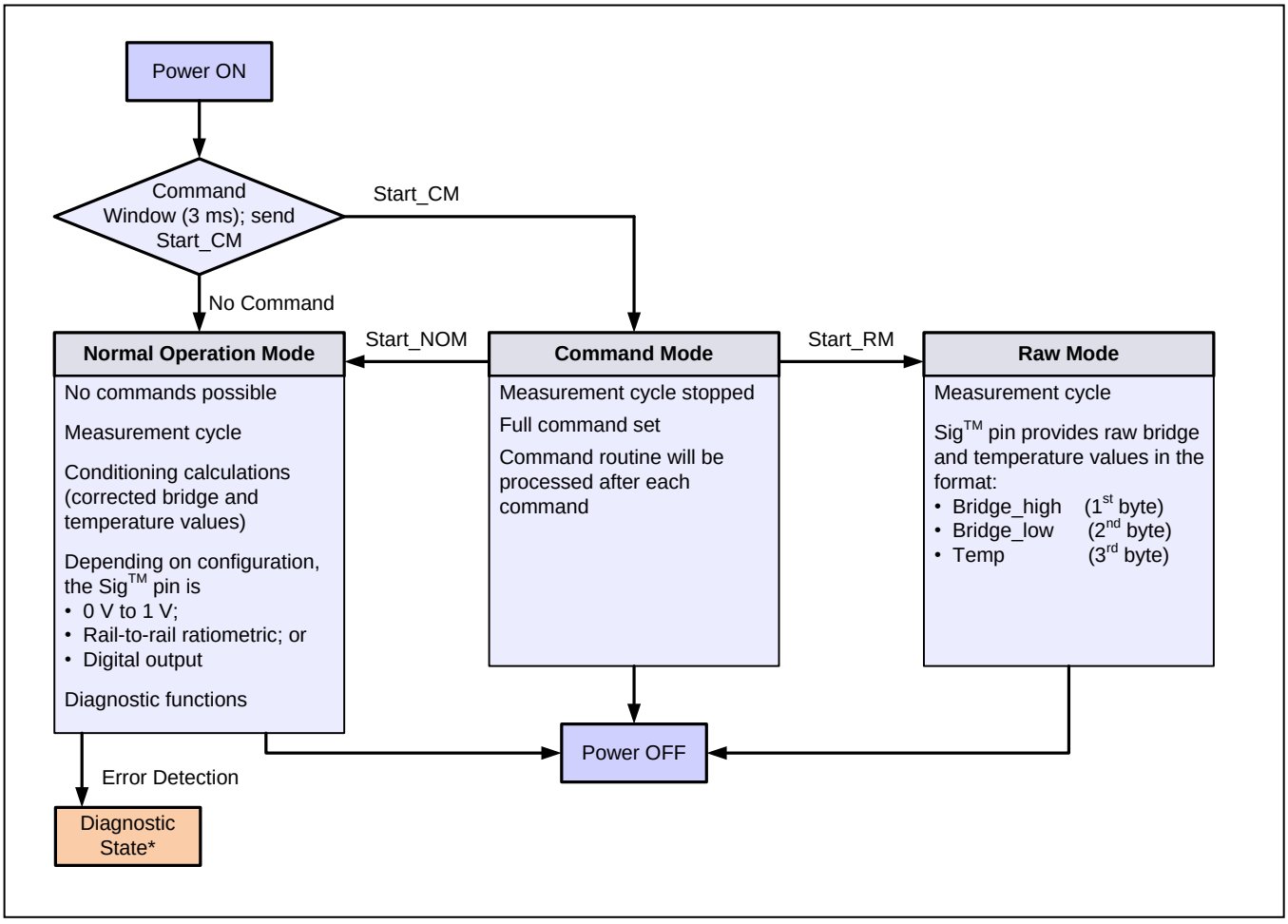
If diagnostic features are enabled and a diagnostic fault is detected, diagnostic states are indicated as follows depending on the programmed mode:

- In Analog Output Mode,
  diagnostic states are indicated by an output below 2.5% of VDD or above 97.5% of VDD.
- In Digital Output Mode,
  diagnostic states will be indicated by a transmission with a generated parity error.

For more details see section 2.6.

© 2019 Renesas Electronics Corporation

Figure 3.1 General Working Mode



* See section 2.6.

3.2. ZACwire™ Communication Interface

3.2.1. Properties and Parameters

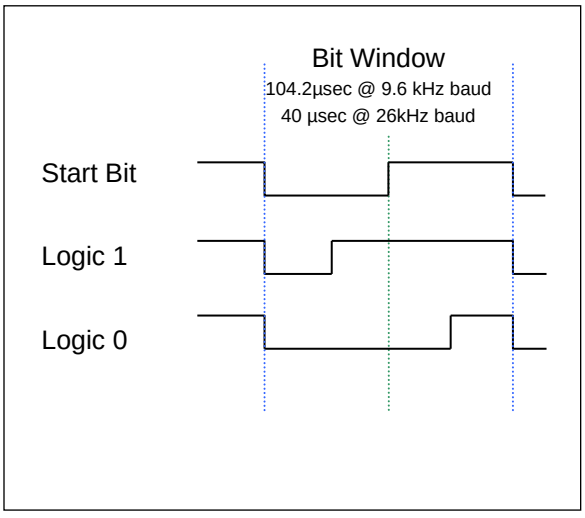
Table 3.1 Pin Configuration and Latch-Up Conditions

No.	Parameter	Symbol	Min	Typ	Max	Unit	Comments
1	Pull-up resistor (on-chip)	$R_{ZAC,pu}$		30		kΩ	On-chip pull-up resistor switched on during Digital Output Mode and during CM Mode (first 3 ms after power up).
2	Pull-up resistor (external)	R_{ZAC,pu_ext}	150			Ω	If the master communicates via a push-pull stage, no pull-up resistor is needed; otherwise, a pull-up resistor with a value of at least 150 Ω must be connected.
3	ZACwire™ rise time	$t_{ZAC,rise}$			5	µs	Any user RC network included in the Sig™ path must meet this rise time.
4	ZACwire™ line resistance [1)]	$R_{ZACload}$			3.9	kΩ	Also see section 1.3.8.
5	ZACwire™ load capacitance [1)]	$C_{ZAC,load}$	0	1	15	nF	Also see section 1.3.8.
6	Voltage low level	$V_{ZAC,low}$		0	0.2	V_{DD}	Rail-to-rail CMOS driver.
7	Voltage high level	$V_{ZAC,high}$	0.8	1		V_{DD}	Rail-to-rail CMOS driver.

1) The rise time must be $t_{ZAC,rise} = 2 * R_{ZACload} * C_{ZACload} \leq 5$ µs . If using a pull-up resistor instead of a line resistor, it must meet this specification. The absolute maximum for $C_{ZACload}$ is 15nF.

3.2.2. Bit Encoding

Figure 3.2 Manchester Duty Cycle



Start bit = 50% duty cycle used to set up strobe time

Logic 1 = 75% duty cycle

Logic 0 = 25% duty cycle

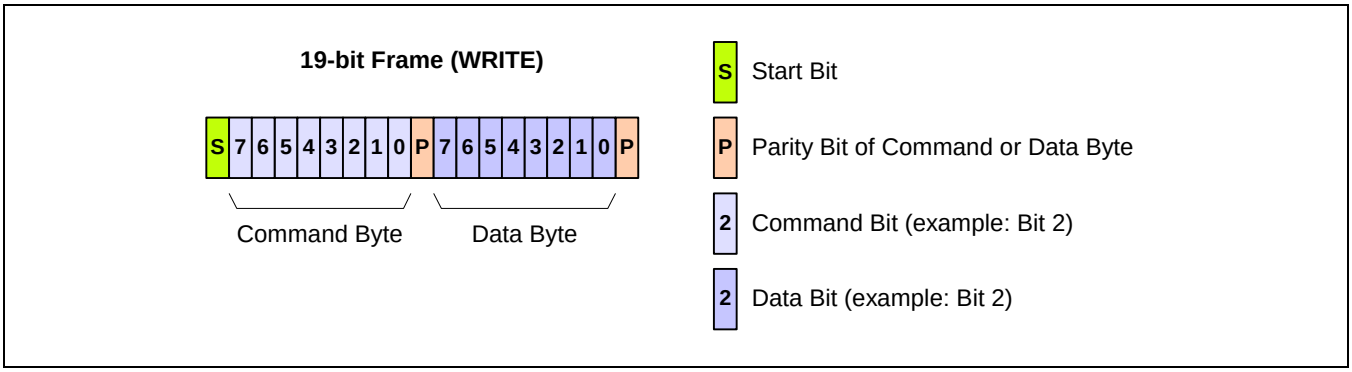
Stop Time

The ZACWire™ bus will be held high for 32µs (nominal) between consecutive data packets regardless of baud rate.

3.2.3. Write Operation from Master to ZSC31015

The calibration master sends a 19-bit packet frame to the IC.

Figure 3.3 19-Bit Write Frame



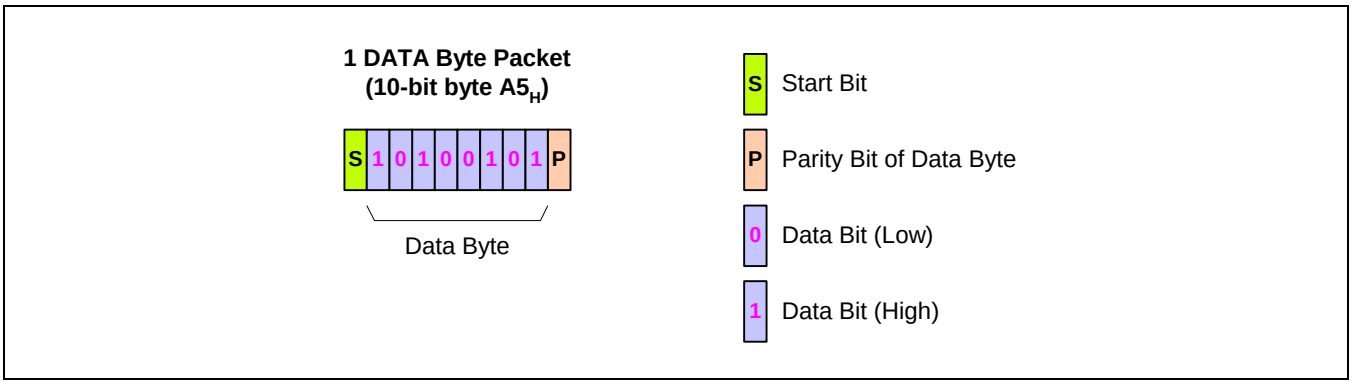
The incoming serial signal will be sampled at a 512 kHz clock rate. This protocol is very tolerant to clock skew, and can easily tolerate baud rates in the 6 kHz to 48 kHz range.

3.2.4. ZSC31015 Read Operations

The incoming frame will be checked for proper parity on both, command and data bytes, as well as for any edge time-outs prior to a full frame being received.

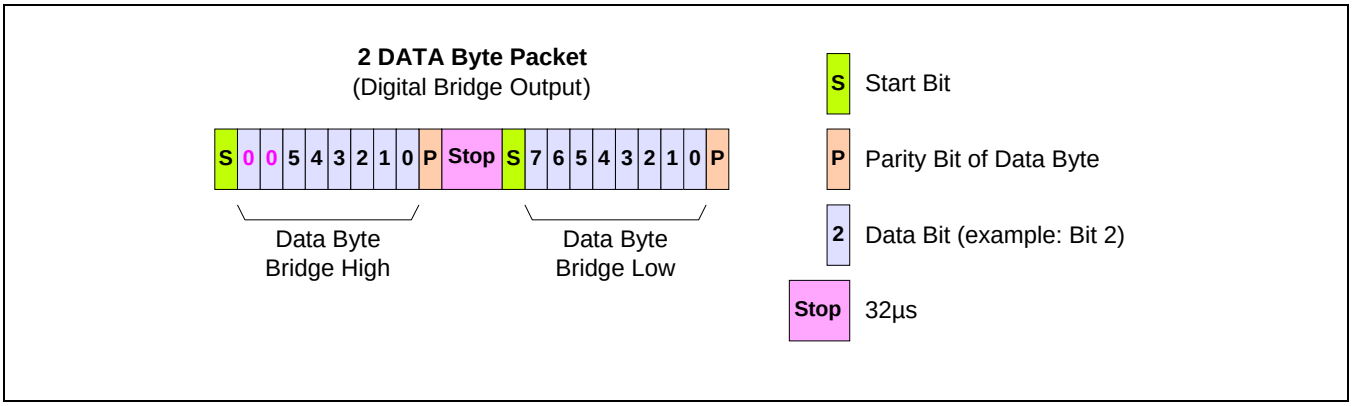
Once a command/data pair is received, the ZSC31015 will perform that command. After the command has been successfully executed by the ZSC31015, it will acknowledge success by a transmission of an $A5_{HEX}$-byte back to the master. If the master does not receive an $A5_{HEX}$ transmission within 130 ms of issuing the command, it must assume the command was either improperly received or could not be executed.

Figure 3.4 Read Acknowledge



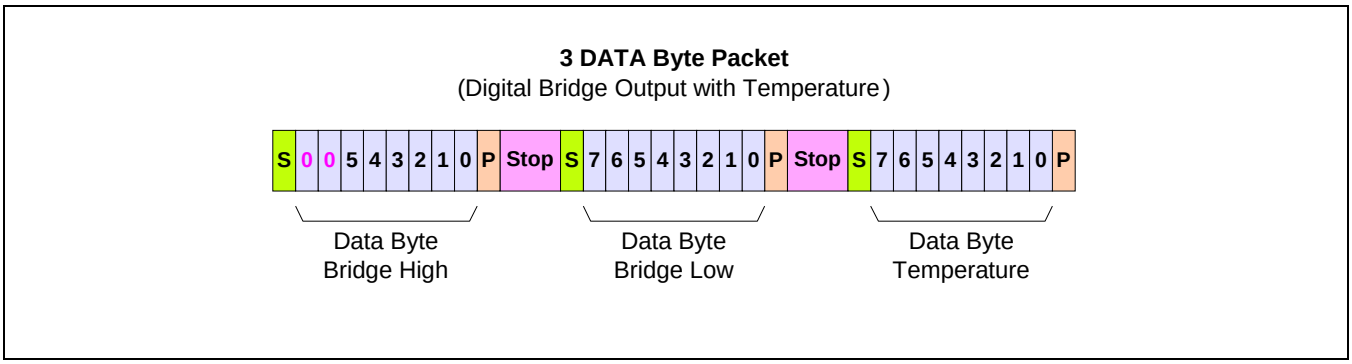
The ZSC31015 transmits 10-bit bytes (1 start bit, 8 data bits, 1 parity bit). During calibration and configuration, transmissions are normally either $A5_{HEX}$ or data. $A5_{HEX}$ indicates successful completion of a command. There are two different digital output modes configurable (digital output with temperature, and digital output with only bridge data). During Normal Operation Mode, if the part is configured for digital output of the bridge reading, it first transmits the high byte of bridge data, followed by the low byte. The bridge data is 14 bits in resolution, so the upper two bits of the high byte are always zero-padded. There is a half stop bit time between bytes in a packet. This means that for the time of a half a bit width, the signal level is high.

Figure 3.5 Digital Output (NOM) Bridge Readings



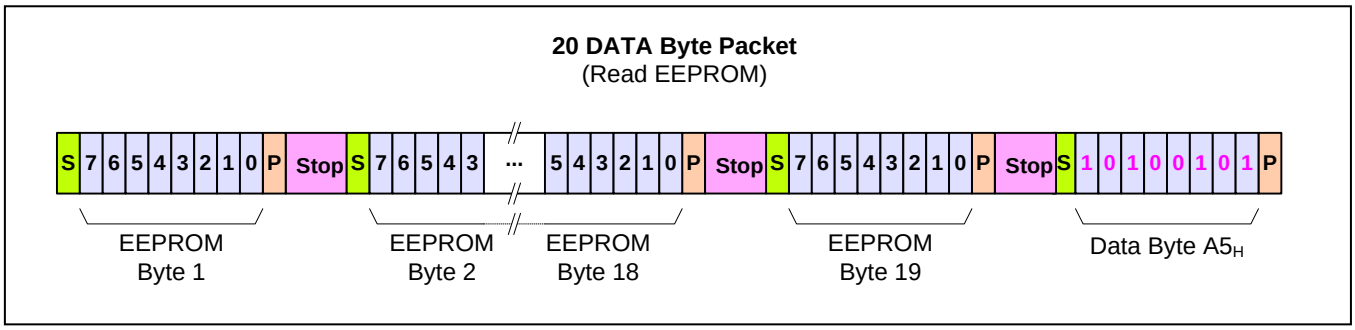
The second option for Digital Output Mode is digital output bridge reading with temperature. It will be transmitted as 3 data packets. The temperature byte represents an 8-bit temperature quantity spanning from -50 to 150°C.

Figure 3.6 Digital Output (NOM) Bridge Readings with Temperature



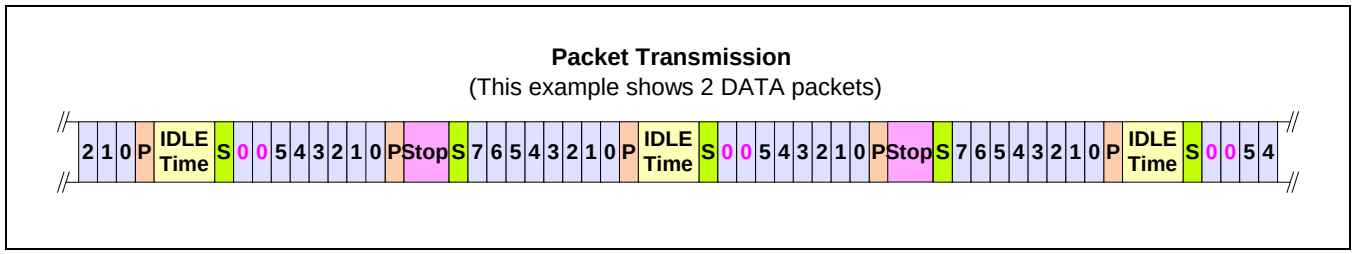
The EEPROM transmission occurs in a packet with 20 data bytes, as shown in Figure 3.7.

Figure 3.7 Read EEPROM Contents



There is a variable idle time between packets. This idle time varies with the update rate setting in EEPROM.

Figure 3.8 Transmission of a Number of Data Packets



The table below shows the idle time between packets versus the update rate. This idle time can vary by nominal +/-15% between parts and over a temperature range of -50 to 150ºC.

Table 3.2 Special Measurement/Idle Time between Packets versus Update Rate

Update Rate Setting	Idle Time between Packets	Special Measurement
00	1ms	Every 128 bridge measurements
01	4.85ms	Every 64 bridge measurements
10	22.5ms	Every 16 bridge measurements
11	118ms	Every 8 bridge measurements

Transmissions from the IC occur at one of two speeds depending on the update rate programmed in EEPROM. If the user chooses one of the two fastest update rates (1 ms or 5 ms) then the baud rate of the digital transmission will be 32 kHz (minimum 26kHz). If, however, the user chooses one of the two slower update rates (25 ms or 125 ms), then the baud rate of the digital transmission will be 8 kHz (maximum 9.6kHz).

The total transmission time for both digital output configurations is shown in Table 3.3.

© 2019 Renesas Electronics Corporation

Table 3.3 Total Transmission Time for Different Update Rate Settings and Output Configuration

Update Rate	Baud Rate*	Idle Time	Transmission Time – Bridge Only Readings			Transmission Time – Bridge & Temperature Readings		
1 ms (1 kHz)	32 kHz	1.0 ms	20.5 bits	31.30 µs	1.64 ms	31.0 bits	31.30 µs	1.97 ms
5 ms (200 Hz)	32 kHz	4.85 ms	20.5 bits	31.30 µs	5.49 ms	31.0 bits	31.30 µs	5.82 ms
25 ms (40 Hz)	8 kHz	22.5 ms	20.5 bits	125.00 µs	25.06 ms	31.0 bits	125.00 µs	26.38 ms
125 ms (8 Hz)	8 kHz	118.0 ms	20.5 bits	125.00 µs	120.56 ms	31.0 bits	125.00 µs	121.88 ms

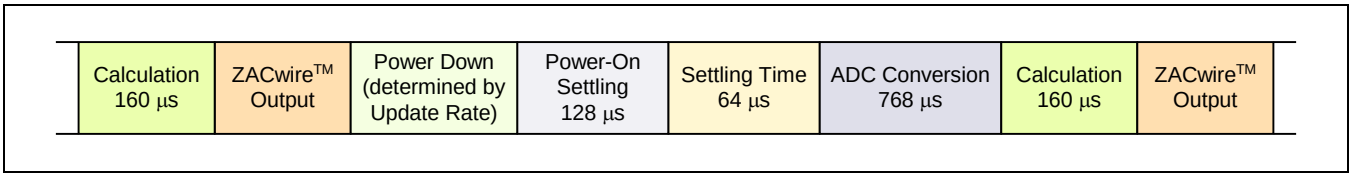
* Typical values. Minimum baud rate for 1 ms or 5 ms: 26kHz; maximum baud rate for 25 ms or 125 ms: 9.6kHz.

The temperature raw reading is performed less often than a bridge reading because the temperature changes more slowly.

The 3rd column in Table 3.2 shows the timing for the special measurements (temperature and bridge measurement) in the different update rate modes.

For lower update rates, the output is followed by a power-down as shown in Figure 3.9.

Figure 3.9 ZACwire™ Output Timing for Lower Update Rates



It is easy to program any standard microcontroller to communicate with the ZSC31015. IDT can provide sample code for a MicroChip PIC microcontroller.

3.2.5. High Level Protocol

The ZSC31015 will listen for a command/data pair to be transmitted for the 3 ms after the de-assertion of its internal Power On Reset (POR). If a transmission is not received within this time frame, then it will transition to Normal Operation Mode (NOM). In the NOM, it will output bridge data in 0-1V analog, rail-to-rail ratiometric analog, or digital depending on how the part is currently configured.

If the ZSC31015 receives a Start_CM command within the first 3 ms after the de-assertion of POR, then it will go into Command Mode (CM). In this mode, calibration/configuration commands will be executed. The ZSC31015 will acknowledge successful execution of commands by transmission of $A5_{HEX}$. The calibrating /configuring master will know a command was not successfully executed if no response is received after 130ms of issuing the command. Once in command interpreting/executing mode, the ZSC31015 will stay in this mode until power is removed or a Start NOM (Start Normal Operation Mode) command is received. The Start_CM command is used as an interlock mechanism to prevent a spurious entry into Command Mode on power up. The first command received within the 3ms window of POR must be a Start_CM command to enter into command interpreting mode. Any other commands will be ignored.

© 2019 Renesas Electronics Corporation

3.3. Command/Data Bytes Encoding

The 2-byte command sent to the ZSC31015 consists of 1 byte of command information and 1 byte of data information. Regardless of whether the command requires data or not, 2 bytes MUST be sent. Table 3.4 lists all the command/data pairings. (X=don't care.)

Table 3.4 Command/Data Bytes Encoding

Note: Refer to Table 3.5 for the location in EEPROM for the bit fields (e.g., Gain_B) referenced in the table.

Command Byte	Data	Description		
00_{HEX}	XX_{HEX}	Read EEPROM command via SIG™ pin.‡		
20_{HEX}	$5X_{HEX}$	DAC Ramp Test Mode. Gain_B[13:3] contains the starting point, and the increment is (Offset_B/8). The increment will be added every 125µsec.		
30_{HEX}	WD_{HEX} W = What D = Data	Trim/Configure: 3rd nibble determines what is trimmed/configured. The 4th nibble is data to be programmed.		
		3rd Nibble	4th Nibble Data	Description
		0_{HEX}	D_{HEX}	Trim oscillator. Least significant 3 bits of data used.
		1_{HEX}	D_{HEX}	Trim 1V reference. Least significant 4 bits of data used.
		2_{HEX}	D_{HEX}	Offset Mode. Least significant 4 bits of data used.
		3_{HEX}	D_{HEX}	Set output mode. Least significant 2 bits used.
		4_{HEX}	D_{HEX}	Set update rate. Least significant 2 bits used.
		5_{HEX}	D_{HEX}	Configure JFET regulation
		6_{HEX}	D_{HEX}	Program the Tc_cfg register. Least significant 3 bits used. Most significant bit of data nibble should be 0.
		7_{HEX}	D_{HEX}	Program EEPROM bits [99:96] {SOT_cfg,Pamp_Gain}
		D_{HEX}	3_{HEX} 0_{HEX},1_{HEX},2_{HEX} 6_{HEX} 4_{HEX},5_{HEX},7_{HEX}	Program EEPROM bits [105:103]: **EEPROM locked!** Int. PTAT used for temperature EEPROM unlocked, Int. PTAT used for temperature **EEPROM locked!** Ext. diode used for temperature EEPROM unlocked, Ext. diode used for temperature
		E_{HEX}	D_{HEX}	Program EEPROM bits [102:100] diag_cfg §
40_{HEX}	00_{HEX}	Start NOM => Ends Command Mode; transition to Normal Operation Mode.		
40_{HEX}	10_{HEX}	Start_RM = Start the Raw Mode (RM) In this mode, if Gain_B = 800_{HEX} and Gain_T = 80_{HEX}, then the digital output will simply be the raw values of the ADC for the Bridge reading, and the PTAT conversion.		
50_{HEX}	90_{HEX}	Start_CM => Start the Command Mode; used to enter Command Interpret Mode.		
60_{HEX}	YY_{HEX}	Program SOT (2nd Order Term)		
70_{HEX}	YY_{HEX}	Program T_{SETL} (Set the MSB to 0.)		

‡ For more details, refer to section 3.7.
§ For more details, refer to section 3.5.

Command Byte	Data	Description
80_{HEX}	YY_{HEX}	Program Gain_B upper 7-bits (Set the MSB to 0.)
90_{HEX}	YY_{HEX}	Program Gain_B lower 8-bits
$A0_{HEX}$	YY_{HEX}	Program Offset_B upper 6-bits (Set the two MSBs to 0.)
$B0_{HEX}$	YY_{HEX}	Program Offset_B lower 8-bits
$C0_{HEX}$	YY_{HEX}	Program Gain_T
$D0_{HEX}$	YY_{HEX}	Program Offset_T
$E0_{HEX}$	YY_{HEX}	Program Tco
$F0_{HEX}$	YY_{HEX}	Program Tcg
08_{HEX}	YY_{HEX}	Program Upper Clipping Limit (Set the MSB to 0.)
18_{HEX}	YY_{HEX}	Program Lower Clipping Limit (Set the MSB to 0.)
28_{HEX}	YY_{HEX}	Program Cust_ID0
38_{HEX}	YY_{HEX}	Program Cust_ID1
48_{HEX}	YY_{HEX}	Program Cust_ID2

3.4. Calibration Sequence

Although the ZSC31015 can work with many different types of resistive bridges, assume a pressure bridge is being used for the following discussion on calibration.

Calibration essentially involves collecting raw bridge and temperature data from the ZSC31015 for different known pressures and temperatures. This raw data can then be processed by the calibration master (typically a PC) to compute the coefficients, and the calculated coefficients can then be written to the ZSC31015.

IDT can provide software and hardware with samples to perform the calibration.

There are three main steps to calibration:

1. Assigning a unique identification to the ZSC31015. This identification is programmed in EEPROM and can be used as an index into the database stored on the calibration PC. This database will contain all the raw values of bridge readings and temperature readings for that part, as well as the known pressure (for this application) and temperature the bridge was exposed to. This unique identification can be stored in a concatenation of the following EEPROM registers: Cust_ID0, Cust_ID1, Cust_ID2. These registers can also form a permanent serial number.
2. Data collection. Data collection involves getting raw data from the bridge at different known pressures and temperatures. This data is then stored on the calibration PC using the unique identification of the ZSC31015 as the index to the database.
3. Coefficient calculation and write. Once enough data points have been collected to calculate all the desired coefficients then the coefficients can be calculated by the calibrating PC and written to the ZSC31015.

© 2019 Renesas Electronics Corporation

Step 1 – Assigning Unique Identification

Assigning a unique identification number is as simple as using the commands Program Cust_ID0, Program Cust_ID1 and Program Cust_ID2. These three 8-bit registers allow for more than 16 million unique devices. Gain_B must be programmed to 800_{HEX} (unity) and Gain_T must be programmed to 80_{HEX} (unity).

Step 2 – Data Collection

The number of unique (pressure, temperature) points that calibration must be performed at depends on the user's needs. The minimum is a 2-point calibration, and the maximum is a 5-point calibration. To acquire raw data from the part, set the ZSC31015 to enter Raw Mode. This is done by issuing a Start_CM (Start Command Mode $5090_{HEX)}$ command/data pair to the ZSC31015 followed by a Start_RM (Start Raw Mode 4010_{HEX}) command/data pair with the LSB of the upper data nibble set. Now if the Gain_B term has been set to unity (800_{HEX}) and the Gain_T term has also been set to unity (80_{HEX}), then the part will be in the Raw Mode and will output raw data on its SIG™ pin instead of corrected bridge and temperature. Capture several of these data points with the user's calibration system (16 each of bridge and temperature is recommended) and average them. Store these raw bridge and temperature settings in the database along with the known pressure and temperature.

The output format during Raw Mode is Bridge_High, Bridge_Low, Temp. Each of these is an 8-bit quantity. The upper 2-bits of Bridge_High are zero-filled. The Temp data (8-bits only) would not be enough information for accurate temperature calibration. Therefore the upper three bits of temperature information are not given, but rather assumed known. Therefore effectively 11-bits of temperature information are provided in this mode.

Step 3 – Coefficient Calculations

The math to perform the coefficient calculation is very complicated and will not be discussed in detail. There is a rough overview in section 3.6. IDT will provide software to perform the coefficient calculation. IDT can also provide source code for the algorithms in a C code format. After the coefficients are calculated, the final step is to write them to the EEPROM of the ZSC31015.

The number of calibration points required can be as few as two or as many as five. This depends on the precision desired and the behavior of the resistive bridge in use.

1. 2-point calibration can be used if only a gain and offset term are needed for a bridge with no temperature compensation for either term.
2. 3-point calibration would be used to obtain 1st order compensation for either a Tco or Tcg term but not both.
3. 3-point calibration could also be used to obtain 2nd order correction for the bridge but no temperature compensation of the bridge output.
4. 4-point calibration would be used to obtain 1st order compensation for both Tco and Tcg.
5. 4-point calibration could also be used to obtain 1st order compensation for Tco and a 2nd order correction for the bridge measurement.
6. 5-point calibration would be used to obtain both 1st order Tco correction and 1st order Tcg correction, plus a 2nd order correction that could be applied to one and only one of the following: 2nd order Tco, 2nd order Tcg, or 2nd order bridge.

© 2019 Renesas Electronics Corporation

3.5. EEPROM Bits

Table 3.5 shows the bit order and default settings for the EEPROM, which are programmed through the serial interface. See section 5 for important information for die/wafer customers.

Table 3.5 ZSC31015 EEPROM Bits

EEPROM Range	Description	Default Settings As of ww08/2009	Notes
2:0	Osc_Trim	0_{HEX} This default setting minimizes risk of communication failure on start-up. (Actual part-specific factory values for Osc_Trim are initially stored in bits in CUST_ID1 and CUST_ID2 for applications requiring optimal response time. See section 5 for important notes.)	See section 2.5 for details on oscillator trim. 100 => Fastest 101 => 3 clicks faster than nominal 110 => 2 clicks faster than nominal 111 => 1 click faster than nominal 000 => Nominal 001 => 1 click slower than nominal 010 => 2 clicks slower than nominal 011 => Slowest
6:3	1V_Trim/JFET_Trim	$ssss_{BIN}$ where “s” is the part-specific factory bit setting for the reference voltage trim value. (Back-up copies are stored in CUST_ID0 for applications requiring accurate references. See section 5 for important notes.)	See Table 2.1 in the “Voltage Reference Block” section.
10:7	A2D_Offset	3_{HEX}	The upper two bits are flip polarity and invert bridge input (negative gain) respectively. If both are used in conjunction, negative offset modes can be achieved. 00 => normal polarity, positive gain 01 => normal polarity, negative gain 10 => flip polarity, positive gain 11 => flip polarity, negative gain The lower two bits form the ADC offset selection. Offset selection: 11 => [-1/2,1/2] mode bridge inputs 10 => [-1/4,3/4] mode bridge inputs 01 => [-1/8,7/8] mode bridge inputs 00 => [-1/16,15/16] mode bridge inputs

© 2019 Renesas Electronics Corporation

EEPROM Range	Description	Default Settings As of ww08/2009	Notes
12:11	Output_Select	2_{HEX}	00 => Digital (3 bytes with parity) Bridge High {00,[5:0]} Bridge Low [7:0] Temp [7:0] 01 => 0-1V Analog 10 => Rail-to-Rail Ratiometric 11 => Digital (2 bytes with parity) (No Temp) Bridge High {00,[5:0]} Bridge Low [7:0]
14:13	Update_Rate	2_{HEX}	00 => 1 msec (1kHz) 01 => 5 msec (200Hz) 10 => 25 msec (40Hz) 11 => 125 msec (8 Hz)
16:15	JFET_cfg	3_{HEX}	00 => No JFET regulation (lower power) 01 => No JFET regulation (lower power) 10 => JFET regulation centered around 5.0V 11 => JFET regulation centered around 5.5V (i.e., over-voltage protection)
31:17	Gain_B	198_{HEX}	Bridge Gain (also see bits 10:7): Gain_B[14] => multiply x 8 Gain_B[13:0] => 14-bit unsigned number representing a number in the range [0,8)
45:32	Offset_B	0_{HEX}	Unsigned 14-bit offset for bridge correction
53:46	Gain_T	80_{HEX}	Temperature gain coefficient used to correct PTAT or ExtTemp reading
61:54	Offset_T	0_{HEX}	Temperature offset coefficient used to correct PTAT or ExtTemp reading
68:62	T_{SETL}	0_{HEX}	Stores Raw PTAT or ExtTemp reading at temperature in which low calibration points were taken
76:69	Tcg	0_{HEX}	Coefficient for temperature correction of bridge gain term: Tcg = 8-bit magnitude of Tcg term. Sign is determined by Tc_cfg (bits 87:85).
84:77	Tco	0_{HEX}	Coefficient for temperature correction of bridge offset term. Tco = 8-bit magnitude of Tco term. Sign and scaling are determined by Tc_cfg (bits 87:85)
87:85	Tc_cfg	0_{HEX}	This 3-bit term determines options for temperature compensation of the bridge. Tc_cfg[2] => If set, Tcg is negative Tc_cfg[1] => Scale magnitude of Tco term by 8, and if SOT applies to Tco, scale SOT by 8 Tc_cfg[0] => If set, Tco is negative

© 2019 Renesas Electronics Corporation

EEPROM Range	Description	Default Settings As of ww08/2009	Notes
95:88	SOT	0_{HEX}	2^{nd} Order Term. This term is a 7-bit magnitude with sign. SOT[7] = 1 ➔ negative SOT[7] = 0 ➔ positive SOT[6:0] = magnitude [0-127] This term can apply to a 2^{nd} order Tcg, Tco or bridge correction. (See Tc_cfg above.)
99:96	{SOT_cfg, Pamp_Gain}	5_{HEX}	Bits [99:98] = SOT_cfg 00 = SOT applies to Bridge 01 = SOT applies to Tcg 10 = SOT applies to Tco 11 = Prohibited Bits [97:96] = Pre-Amp Gain 00 => 6 01 => 24 (default setting) 10 => 48 11 => 96
102:100	Diag_cfg	7_{HEX}	This 3-bit term applies to diagnostic features Diag_cfg[2] → enable output short circuit protection. Diag _cfg[1] → enable sensor short checking. Diag_cfg[0] → enables sensor connection checking.
105:103	Lock_ExtTemp	0_{HEX}	EEPROM lock 011 or 110 => locked All other => unlocked When EEPROM is locked, the internal charge pump is disabled and the EEPROM can never be programmed again. Bit 105 (the MSB of this field) is also used for selecting external temperature measurement. 000,001,010,011=>Internal PTAT used for temp 100,101,110,111=>External diode used for temp
112:106	Up_Clip_Lim	$7F_{HEX}$	7-bit value used to select an upper clipping limit for the output. It affects both analog and digital output. The 14-bit upper clipping limit value is comprised of {11,Up_Clip_Lim[6:0],11111}. 127 different clipping levels are selectable between 75.19% and 100% of VDD.
119:113	Low_Clip_Lim	0_{HEX}	7-bit value used to select a lower clipping limit for the output. It affects both analog and digital output. The 14-bit lower clipping limit value is comprised of {00,Low_Clip_Lim[6:0],00000}. 127 different clipping levels are selectable between 0% and 24.8% of VDD.

© 2019 Renesas Electronics Corporation

EEPROM Range	Description	Default Settings As of ww08/2009	Notes
127:120	Cust_ID0	ss_{BIN} where “s” is a part-specific factory bit setting. During factory testing, two back-up copies of the optimal setting for the 1V_Trim/JFET_Trim bits are stored in [123:120] and in [127:124]. See important notes in section 5.	Customer ID byte 0 Can be used to store a customer part identification number. Caution: If the application requires accurate voltage references, do not overwrite this byte until completing the procedures in section 5.
135:128	Cust_ID1	xsss $xsss_{BIN}$ where “s” is a part-specific factory bit setting and x is “don’t care.” During factory testing, two copies of the optimal setting for the Osc_Trim bits are stored in [130:128] and in [134:132]. (Also in Cust_ID2.) See important notes in section 5.	Customer ID byte 1 Can be used to store a customer part identification number. Caution: If the application requires optimal response time, do not overwrite this byte until completing the procedures in section 5.
143:136	Cust_ID2	xxxx $xsss_{BIN}$ where “s” is a part-specific factory bit setting and X is “don’t care.” During factory testing, a copy of the optimal setting for the Osc_Trim bits is stored in [138:136]. (Also in Cust_ID1.) See important notes in section 5.	Customer ID byte 2 Can be used to store a customer part identification number. Caution: If the application requires optimal response time, do not overwrite this byte until completing the procedures in section 5.
151:144	Signature		8-bit EEPROM signature. Generated through a LFSR**. This signature is checked on power-on to ensure integrity of EEPROM contents.

** Linear feedback shift register

3.6. Calibration Math

3.6.1. Correction Coefficients

All terms are calculated external to the ZSC31015 and then programmed to the EEPROM through the serial interface.

Table 3.6 Correction Coefficients

Coefficient	Description
Gain_B	Gain term used to compensate span of Bridge reading
Offset_B	Offset term used to compensate offset of Bridge reading
Gain_T	Gain term used to compensate span of Temp reading
Offset_T	Offset term used to compensate offset of Temp reading
SOT	Second Order Term. The SOT can be applied as a second order correction term for one of the following: - Bridge measurement - Temperature coefficient of offset (Tco) - Temperature coefficient of gain (Tcg) The EEPROM bits 99:98 determine what SOT applies to.
T_{SETL}	RAW_PTAT or ExtTemp reading (upper 7-bits) at low temperature at which calibration was performed (typically room temperature)
Tcg	Temperature correction coefficient of bridge gain term. *This term has an 8-bit magnitude and a sign bit (Tc_cfg[2].*
Tco	Temperature correction coefficient of bridge offset term. This term has an 8-bit magnitude, a sign bit (Tc_cfg[0]), and a scaling bit (Tc_cfg[1]), which can multiply its magnitude by 8.

3.6.2. Interpretation of Binary Numbers for Correction Coefficients

BR_Raw should be interpreted as an unsigned number in the set [0, 16383] with a resolution of 1.

T_Raw should be interpreted as an unsigned number in the set [0, 16383], with a resolution of 4.

3.6.2.1. Gain_B Interpretation

Gain_B should be interpreted as a number in the set [0, 64]. The MSB (bit 14) is a scaling bit that will multiply the effect of the Gain_B[13:0] term by 8. The remaining bits Gain_B[13:0] represent a number in the range of [0,8) with Gain_B[13] having a weighting of 4, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.7 Gain_B [13:0] Weightings

Bit Position	Weighting
13	$2^2 = 4$
12	$2^1 = 2$
11	$2^0 = 1$
10	2^{-1}
…	…
3	2^{-8}
2	2^{-9}
1	2^{-10}
0	2^{-11}

Examples:

The binary number: 010010100110001_B = 4.6489; Gain_B[14] is 0_{BIN}, so the number represented by Gain_B[13:0] is not multiplied by 8.

The binary number: 101100010010110_B = 24.586; Gain_B[14] is 1_{BIN}, so the number represented by Gain_B[13:0] is multiplied by 8.

3.6.2.2. Offset_B Interpretation

Offset_B is a 14-bit unsigned binary number. The MSB has a weighting of 8192. The following bits then have a weighting of: 4096, 2048, 1024 …

Table 3.8 Offset_B Weightings

Bit Position	Weighting
13	8192
12	4096
11	2048
.	
.	
.	
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number 1111 1111 1100 = 4092.

3.6.2.3. Gain_T Interpretation

Gain_T should be interpreted as a number in the set [0,2]. Gain_T[7] has a weighting of 1, and each subsequent bit has a weighting of ½ the previous bit.

Table 3.9 Gain_T Weightings

Bit Position	Weighting
7	$2^0 = 1$
6	$2^{-1} = 0.5$
5	$2^{-2} = 0.25$
4	2^{-3}
3	2^{-4}
2	2^{-5}
1	2^{-6}
0	2^{-7}

3.6.2.4. Offset_T Interpretation

Offset_T is an 8-bit signed binary number in two's complement form. The MSB has a weighting of -128. The following bits then have a weighting of 64, 32, 16 …

Table 3.10 Offset_T Weightings

Bit Position	Weighting
7	-128
6	$2^6 = 64$
5	$2^5 = 32$
4	$2^4 = 16$
3	$2^3 = 8$
2	$2^2 = 4$
1	$2^1 = 2$
0	$2^0 = 1$

For example, the binary number $00101001_B = 41$.

3.6.2.5. Tco Interpretation

Tco is specified as having an 8-bit magnitude with an additional sign bit and a scalar bit (Tc_cfg). When the scalar bit is set, the signed Tco is multiplied by 8.

- Tco Resolution: 0.175 µV/V/^{o}C (input referred)
- Tco Range: ± 44.6 µV/V/^{o}C (input referred)

If the scaling bit is used, then the above resolution and range are scaled by 8 to give the following results:

- Tco Scaled Resolution: 1.40 µV/V/^{o}C (input referred)
- Tco Scaled Range: ± 357 µV/V/^{o}C (input referred)

3.6.2.6. Tcg Interpretation

Tcg is specified as an 8-bit magnitude with an additional sign bit (Tc_cfg).

- Tcg Resolution: 17.0 ppm/^{o}C
- Tcg Range: ±4335 ppm/^{o}C

3.6.2.7. SOT Interpretation

SOT is a 2nd order term that can apply to one and only one of the following: bridge non-linearity correction, Tco non-linearity correction, or Tcg non-linearity correction.

As it applies to bridge non-linearity correction:

- Resolution: 0.25% @ full scale
- Range: +25% @ full scale to -25% @ full scale
  (Saturation in internal arithmetic will occur at greater negative nonlinearities.)

As it applies to Tcg:

- Resolution: 0.3 ppm/(^{o}C)^{2}
- Range: +/- 38ppm/(^{o}C)^{2}

As it applies to Tco:

2 settings are possible. It is possible to scale the effect of SOT by 8. If Tc_cfg[1] is set, then both Tco and SOT's contribution to Tco are multiplied by 8.

- Resolution at unity scaling: 1.51nV/V/(^{o}C)^{2} (input referred)
- Range: +/- 0.192µV/V/(^{o}C)^{2} (input referred)

- Resolution at 8x scaling: 12.1nV/V/(^{o}C)^{2} (input referred)
- Range: +/- 1.54µV/V/(^{o}C)^{2} (input referred)

© 2019 Renesas Electronics Corporation

3.7. Reading EEPROM Contents

The contents of the entire EEPROM memory can be read out using the Read EEPROM command (00_{HEX}). This command causes the ZSC31015 to output consecutive bytes on the ZACwire™. After each transmission, the EEPROM contents are shifted by 8 bits. The bit order of these bytes is given in Table 3.11.

Table 3.11 EEPROM Read Order

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 1	Offset_B[7:0]							
Byte 2	Gain_T[1:0]		Offset_B[13:8]					
Byte 3	Offset_T[1:0]		Gain_T[7:2]					
Byte 4	T_{SETL}[1:0]		Offset_T[7:2]					
Byte 5	Tcg[2:0]			T_{SETL}[6:2]				
Byte 6	Tco[2:0]			Tcg[7:3]				
Byte 7	Tc_cfg[2:0]			Tco[7:3]				
Byte 8	SOT[7:0]							
Byte 9	Lock[0]	Diag_cfg[2:0]			SOT_cfg[3:0]			
Byte 10	Up_Clip_Lim[5:0]						Lock[2 :1]	
Byte 11	Low_Clip_Lim[6:0]							Up_Clip_Lim[6]
Byte 12	Cust_ID0[7:0]							
Byte 13	Cust_ID1[7:0]							
Byte 14	Cust_ID2[7:0]							
Byte 15	Signature[7:0]							
Byte 16	A2D_Offset[0]	1V_Trim[3:0] **				Osc_Trim[2:0] **		
Byte 17	JFET_cfg[0]	Update_Rate[1:0]		Output Select[1:0]		A2D_Offset[3:1]		
Byte 18	Gain_B[6:0]							JFET_cfg[1]
Byte 19	Gain_B[14:7]							
Byte 20	$A5_{HEX}$							

* SOT_cfg/Pamp_Gain
** 1V_Trim/JFET_Trim

4 Application Circuit Examples

The minimum output analog load resistor is R_L= 5kΩ. This optional load resistor can be configured as a pull-up or pull-down. If it is configured as a pull-down, it cannot be part of the module to be calibrated because this would prevent proper operation of the ZACwire™. If a pull-down load is desired, it must be added to system after module calibration.

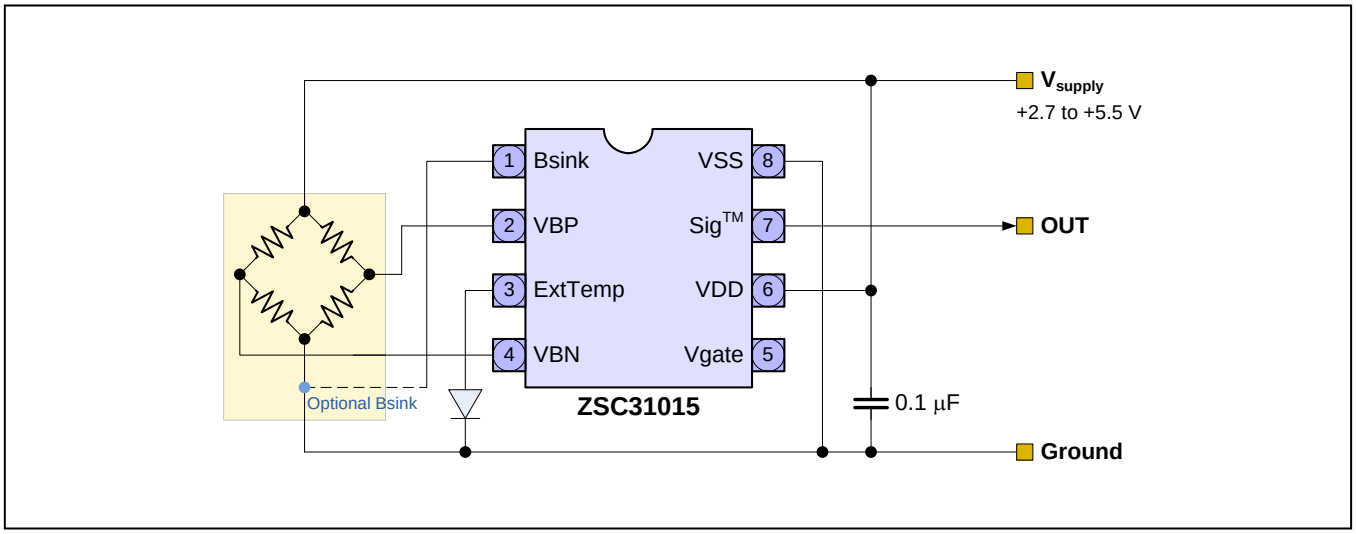
There is no output load capacitance needed.

EEPROM contents: OUTPUT_select, Config_JFET_Regulation, 1V_Trim/JFET-Trim.

4.1. Three-Wire Rail-to-Rail Ratiometric Output

This example shows an application circuit for rail-to-rail ratiometric voltage output configuration with temperature compensation via an external diode. The same circuitry is applicable for a 0 to 1V absolute analog output.

Figure 4.1 Rail-to-Rail Ratiometric Voltage Output – Temperature Compensation via External Diode



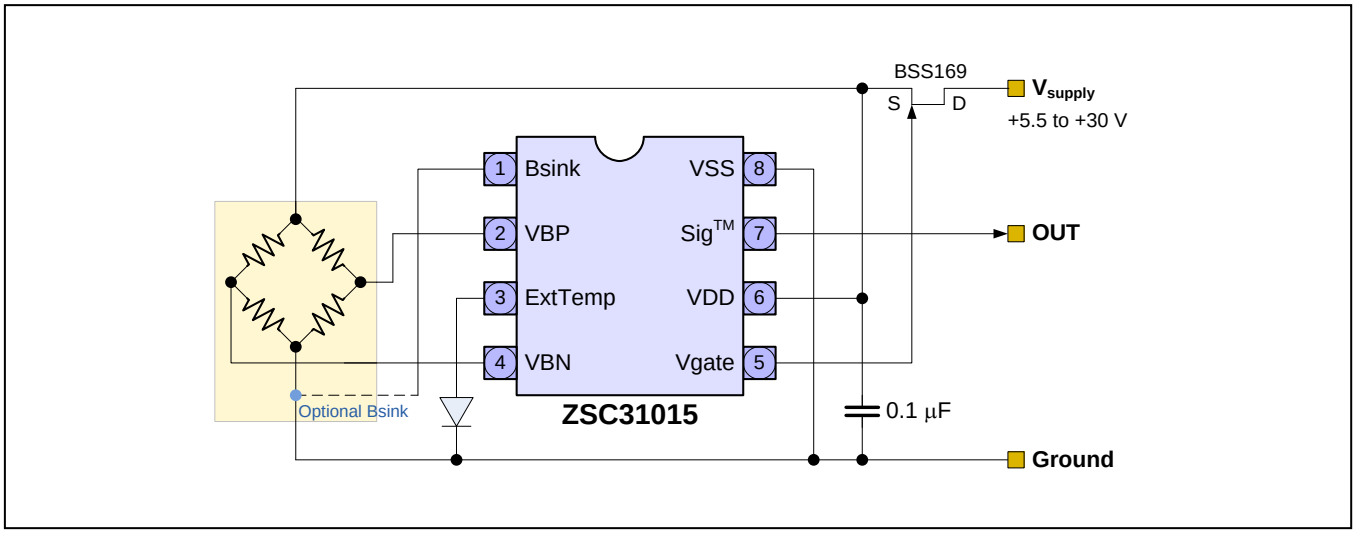
The optional bridge sink allows a power savings of bridge current. The output voltage can be either

- Rail-to-rail ratiometric analog output V_{DD}(=Vsupply).
- 0 to 1V absolute analog output. The absolute voltage output reference is trimmable 1V (+/-3mV) in the 1V Output Mode via a 4-bit EEPROM field. See section 2.4.3).

4.2. Absolute Analog Voltage Output

The figure below shows an application circuit for an absolute voltage output configuration with temperature compensation via internal temperature PTAT and external JFET regulation for all industry standard applications.

Figure 4.2 Absolute Analog Voltage Output – Temperature Compensation via Internal Temperature PTAT with External JFET Regulation



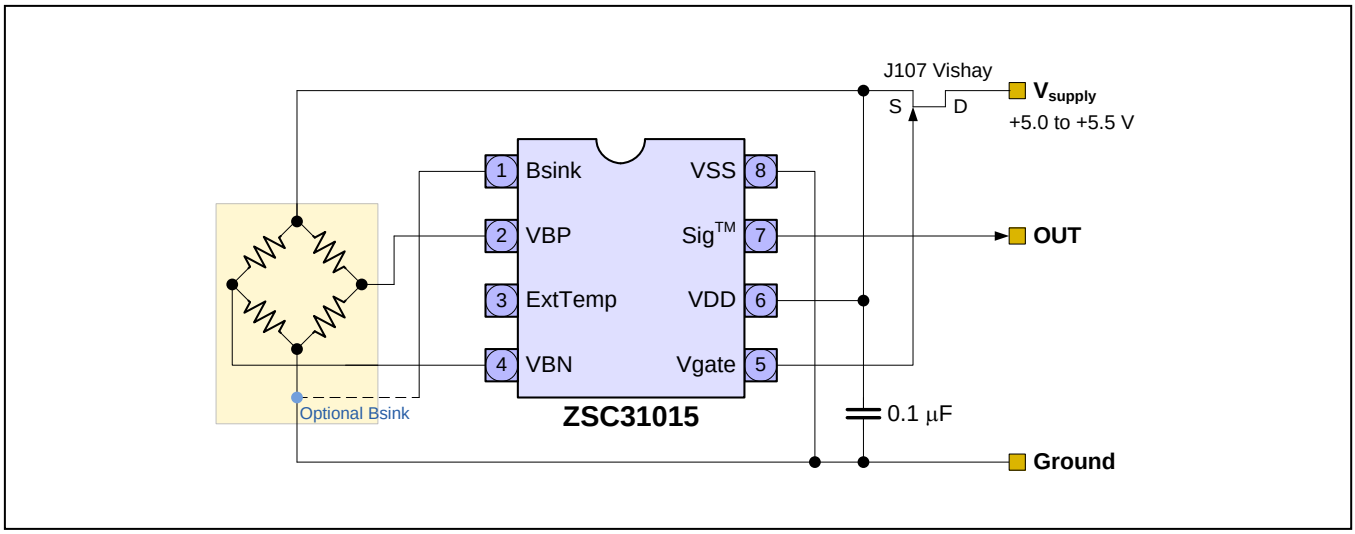
The output signal range can be one of the following options:

- 0 to 1 V analog output. The absolute voltage output reference is trimmable: 1 V (+/-3 mV) in the 1 V Output Mode via a 4-bit EEPROM field (see section 2.4.3).
- Rail-to-rail analog output. The on-chip reference for the JFET regulator block is trimmable: 5 V (±15 mV) in the Ratiometric Output Mode via a 4-bit EEPROM field. (See section 2.4.3).

4.3. Three-Wire Ratiometric Output with Over-Voltage Protection

The figure below shows an application circuit for a ratiometric output configuration with temperature compensation via an internal diode. In this application, the JFET is used for voltage protection. JFET_cfg (16:15) in the EEPROM are configured to 5.5V. There is an additional maximum error of 8mV caused by the non-zero rds(on) of the limiter JFET.

Figure 4.3 Ratiometric Output, Temperature Compensation via Internal Diode



4.4. Digital Output

For all three circuits, the output signal can also be digital. Depending on the output select bits, the bridge signal or the bridge signal and temperature signal are sent. For the digital output, no load resistor or load capacity is necessary. No pull down resistor is allowed. If a line resistor or pull-up resistor is used, the requirement for the rise time must be met (< 5 µs). The ZSC31015 output includes an internal pull up resistor of about 30 kΩ. The digital output can easily be read by firmware from a microcontroller, and IDT can provide the customer with software for developing the interface.

4.5. Output Resistor/Capacitor Limits

The limits for external components depend on the programmed output mode:

- Pure Analog Output Mode (calibration is done before): The only limit is the minimum load resistance of 5 kΩ.
- Pure Digital Output Mode with end-of-line calibration: The RC time constant of the ZACwire™ line must have a rise time < 5 µs.
- Analog output with digital communication during calibration: The RC time constant of the ZACwire™ line must have a rise time < 5 µs.

Warning: Any series line resistance forms a voltage divider in conjunction with the pull-up load device. If a series line resistance is needed, choose a low value relative to the pull-up load device.

5 EEPROM Restoration

If needed, the default settings for the ZSC31015 (see Table 3.5) can be reprogrammed as described in section 3. The following sections describe EEPROM content validation and handling during and/or after system assembly.

Important: During the sawing and dicing process, there is a possibility of the EEPROM contents flipping, and prevention cannot be guaranteed. This is primarily a concern for the factory trim settings, which are customized to each part.

The EEPROM default values programmed during the different test levels have been selected so that customer has the option to refresh/reprogram trim bits that might have flipped during sawing or dicing.

Important: The EEPROM lock is stored in the bit range 105:103. A value of 6_{HEX} or 3_{HEX} will lock the EEPROM forever by disabling the charge pump needed for EEPROM writing. The complete contents can also be validated using the EEPROM signature stored in bits [151:144], (see “Signature” in Table 3.5).

5.1. Default EEPROM Contents

During the wafer level test (wafer/dice delivery) and during final test for SOP8 packaged parts, the EEPROM is programmed with the default values listed in the Table 3.5. During the wafer level test, the Osc_trim bits [2:0] and 1V_Trim/JFET_Trim trim bits [6:3] are set to die-specific values.

5.1.1. Osc_Trim

The oscillator frequency is trimmed to a value of 512kHz±20% using the Osc_Trim bit setting. The 3-bit setting is copied twice to Cust_ID1[134:132] and [130:128] and then a third time to Cust_ID2[138:136] to ensure the factory settings are retained so that the customer can reprogram these values in the Osc_Trim bit if needed. Based on the most probable trimming, the default values for the Osc_Trim bits are always set to 0_{HEX} during factory testing to guarantee communication even if bits have flipped.

5.1.2. 1V_Trim/JFET_Trim

The 5V reference for the JFET regulation is factory trimmed during the final test to 5V±15mV using the 1V_Trim/ JFET_Trim bit setting. The 4-bit setting stored in EEPROM bits [6:3] is copied twice to the Cust_ID0 bits [127:124] and [123:120] to ensure the factory settings are retained so that the customer can reprogram these values in the 1V_Trim/JFET_Trim bits if needed.

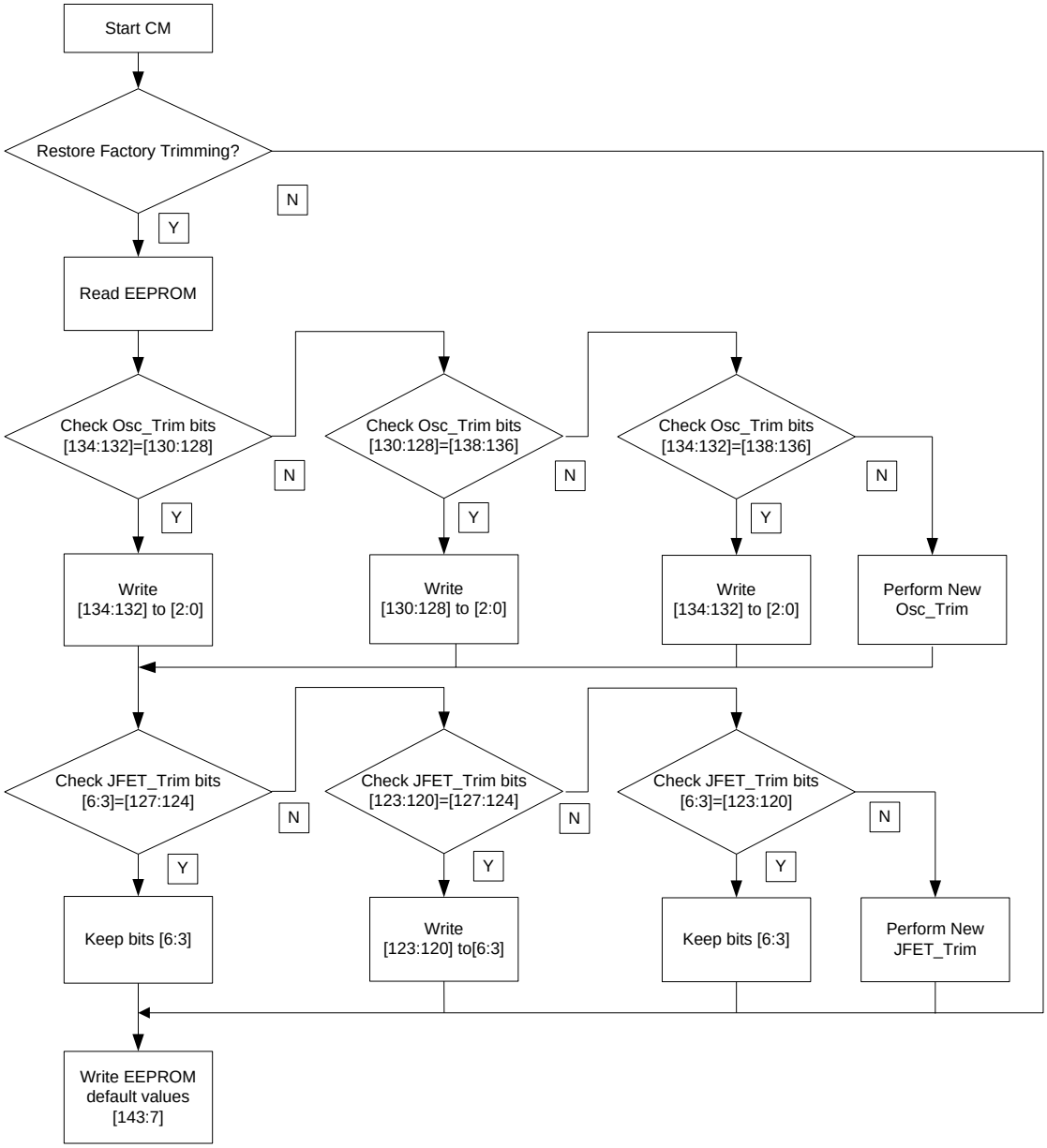
5.2. EEPROM Restoration Procedure

After module assembly, the EEPROM content should be refreshed. If JFET regulation is not used for the user’s application and optimized response time is not an important criterion, write the default values shown in Table 3.5 to the EEPROM bit range [143:7] and retain the existing values in the bit range [6:0]. If JFET regulation or optimized response time is required, the bit restoration procedure shown in the flow chart in Figure 5.1 must be used to keep the factory settings programmed during the testing. If customer oscillator trimming is required, see *ZSC31015_Tech_Notes_JFET_and_Osc_Trimming_revX.X .pdf* for instructions.)

Note: The EEPROM signature is re-calculated and updated after every EEPROM writing.

© 2019 Renesas Electronics Corporation

Figure 5.1 EEPROM Validation and Restoration Procedure



6 Pin Configuration and Package

The standard package of the ZSC31015 is an SOP-8 (3.81 mm / 150 mil body) with a lead-pitch 1.27 mm / 50 mil.

Table 6.1 Storage and Soldering Conditions for SOP-8 Package

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Maximum Storage Temperature	$T_{max_storage}$	Less than 10hrs, before mounting			150	°C
Minimum Storage Temperature:	$T_{min_storage}$	Store in original packing only	-50			°C
Maximum Dry-Bake Temperature	$T_{drybake}$	Less than100 hrs total, before mounting			125	°C
Soldering Peak Temperature	T_{peak}	Less than 30s (IPC/JEDEC-STD-020 Standard)			260	°C

Figure 6.1 ZSC31015 Pin-Out Diagram

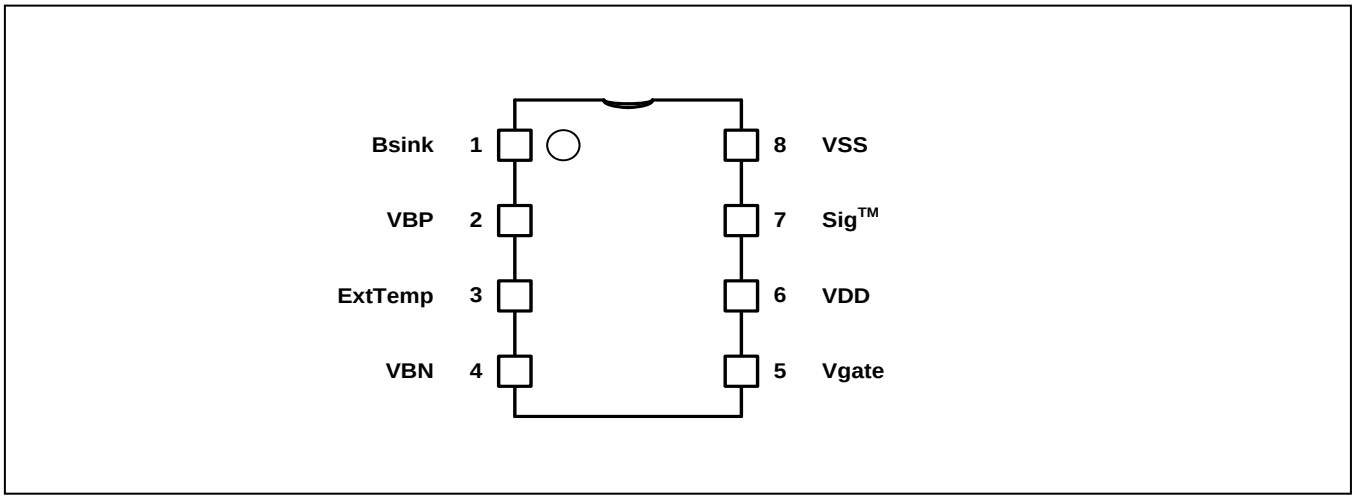


Table 6.2 ZSC31015 Pin Configuration

Pin No.	Name	Description
1	Bsink	Optional ground connection for bridge ground; used for power savings
2	VBP	Positive bridge connection
3	ExtTemp	External diode connection
4	VBN	Negative bridge connection
5	Vgate	Gate control for external JFET regulation/over-voltage protection
6	VDD	Supply voltage (2.7 to 5.5 V)
7	Sig™	ZACwire™ interface (analog out, digital out, calibration interface)
8	VSS	Ground supply

© 2019 Renesas Electronics Corporation

7 ESD/Latch-Up-Protection

All pins have an ESD protection of >4000V and a latch-up protection of ±100 mA or of +8V/ –4V (to VSS/VSSA). ESD protection referenced to the Human Body Model is tested with devices in SOP-8 packages during product qualification. The ESD test follows the Human Body Model with 1.5kΩ/100pF based on MIL 883, Method 3015.7.

8 Test

The test program is based on this datasheet. The final parameters that are tested during series production are listed in the tables of section 1.

The digital part of the IC includes a scan path, which can be activated and controlled during wafer test. Further test support for testing of the analog parts on wafer level is included in the DSP.

9 Quality and Reliability

A reliability investigation according to the in-house non-automotive standard has been performed.

10 Customization

For high-volume applications, which require an upgraded or downgraded functionality compared to the ZSC31015, IDT can customize the circuit design by adding or removing certain functional blocks.

For this customization, IDT has a considerable library of sensor-dedicated circuitry blocks, which enable IDT to provide a custom solution quickly. Please contact IDT for further information.

© 2019 Renesas Electronics Corporation

11 Part Ordering Codes

Please contact IDT Sales for additional information.

Sales Code	Description	Package
ZSC31015EEB	ZSC31015 Die — Temperature range: -50°C to +150°C	Unsawn on Wafer
ZSC31015EEC	ZSC31015 Die— Temperature range: -50°C to +150°C	Sawn on Wafer Frame
ZSC31015EEG1-R	ZSC31015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Reel
ZSC31015EEG1-T	ZSC31015 SOP8 (150 mil) — Temperature range: -50°C to +150°C	Tube
ZSC31015EAB	ZSC31015 Die — Temperature range: -40°C to +125°C	Unsawn on Wafer
ZSC31015EAC	ZSC31015 Die— Temperature range: -40°C to +125°C	Sawn on Wafer Frame
ZSC31015EAG1-R	ZSC31015 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Reel
ZSC31015EAG1-T	ZSC31015 SOP8 (150 mil) — Temperature range: -40°C to +125°C	Tube
ZSC31015EIB	ZSC31015 Die— Temperature range: -25°C to +85°C	Unsawn on Wafer
ZSC31015EIC	ZSC31015 Die — Temperature range: -25°C to +85°C	Sawn on Wafer Frame
ZSC31015EIG1-R	ZSC31015 SOP8 (150 mil) — Temperature range: -25°C to +85°C	Reel
ZSC31015EIG1-T	ZSC31015 SOP8 (150 mil) — Temperature range: -25°C to +85°C	Tube
ZSC31015KIT	ZSC31015 ZACwire™ SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (SOP8) (ZACwire™ SSC Evaluation Software can be downloaded from www.IDT.com/ZSC31015)	Kit

Contact IDT Sales for support and sales of IDT's ZSC31015 Mass Calibration System.

12 Related Documents

Document
ZACwire™ *SSC Evaluation Kit Description*
*ZSC31015 Die Dimensions and Pad Coordinates***
SSC Evaluation Kits Feature Sheet * (includes ordering codes)
ZSC31010/31015/31050 Application Note – External Protection Circuitry
IDT Wafer Dicing Guidelines

Visit the ZSC31015 product page (www.IDT.com/ZSC31015) or contact your nearest sales office for the latest version of these documents.

* Documents marked with an asterisk (*) can be found on the Evaluation Tools page (www.IDT.com).

** Documents marked with two asterisks (**) are available on request.

13 Definitions of Acronyms

Term	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
BUF	Buffer
CM	Command Mode
CMC	Calibration Microcontroller
DAC	Digital-to-Digital Converter
DNL	Differential Nonlinearity
DSP	Digital Signal Processor
DUT	Device Under Test
ESD	Electrostatic Discharge
FSO	Full-Scale Output
INL	Integrated Nonlinearity
LSB	Least Significant Bit
MUX	Multiplexer
NOM	Normal Operation Mode
OWI	One-Wire Interface
POC	Power-On Clear
POR	Power-On Reset Level
PSRR	Power Supply Rejection Ratio
PTAT	Proportional To Absolute Temperature
RM	Raw Mode
SOT	Second Order Term

© 2019 Renesas Electronics Corporation

14 Document Revision History

Revision	Date	Description
1.40	February 24, 2009	Revision to Byte 16 in Table 3.11. Revision to add an explanation for default setting in Table 3.5. Revision to "Lower Output Voltage Limit" specification in section 1.3.5. Revisions in sections 2.4.3 and 2.5.1 to text regarding regulator set point and optimal reference trim, including text about methods for preserving factory settings. Revision to caption for Figure 3.2 to clarify that timing is typical. Revision to text below Table 3.2 regarding minimum and maximum baud rate. Added note below Table 3.3 clarifying that timing is typical. Revisions to the default settings column and explanations for the Cust_ID0 and Cust_ID1 EEPROM words in Table 3.5. Addition of section 5 to explain methods for restoration of EEPROM settings.
1.50	May 14, 2009	Revised conditions for "Overall Ratiometricity Error" and "Overall Accuracy – Analog" specifications in section 1.3.9.
1.60	June 10, 2009	Added "Document Revision History" table.
1.70	March 29, 2010	Corrected start-up window time 1.5 to 3ms. This change applies only to rev C1 Silicon (marked as ZSC31015Cxx.) and higher. Stop bit definition is replaced by stop time definition. Relocated specs from Table 1.9 and deleted Table 1.9.
1.73	May 11, 2010	Added footnote to pages 2, 3, and 14 clarifying that the ZSC31015 is not AEC-Q100-qualified.
1.74	July 19, 2010	Added special measurement information to Table 3.2; revised precondition for equation (1).
1.80	July 27, 2010	Revised product name from ZMD31015 to ZSC31015.
1.90	March 24, 2011	Added EEPROM specifications to section 1.3 "Electrical Parameters." Added table 6.1 "Storage and Soldering Conditions" to section 6 "Pin Configuration and Package." Updated trim tolerances in sections 4.1and 4.2. Updated ZMDI contact information.
1.91	October 8, 2011	Revisions in section 1.3.4. Addition of part ordering numbers for all available temperature ranges to section 11. Update for sales contact information to add ZMDI's Korea office. Revision of product title.
1.92	January 12, 2012	Removed requirement of fastest update rate for analog output mode (applied to previous IC revision). Updated contact information for the USA.
2.00	October 28, 2012	Updates to contact information and part ordering numbers.
2.10	October 9, 2013	Update to section 1.2 to add new minimum specification for output load capacitance. Update to section 1.3.9 for t_{STA} maximum specification. Updates to contact information and imagery for cover and headers. Updates to part order options. Updates to related documents.
2.11	December 11, 2013	Update for part ordering tables: kit no longer includes DVD of software. Software is now downloaded from www.IDT.com/ZSC31015 to ensure user has the latest version of software.
2.12	June 3, 2014	Update to section 1.2 regarding minimum bridge resistance values. Update to section 2.6.3 regarding minimum bridge resistance values. Update for "Related Documents" section and ZMDI contact information.
	April 22, 2016	Changed to IDT branding. Release date is now the revision number.
	November 14, 2016	Correction of error in title regarding the product name.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.