BelaSigna R262

Wideband Voice Capture and Noise Reduction Solution

Introduction

BelaSigna® R262 is a complete system−on−chip (SoC) solution that provides wideband advanced noise reduction in voice capture applications such as mobile phones, VoIP applications including webcams and tablet computers, two−way radios and other applications that can benefit from improved voice clarity.

Featuring a novel approach to removing mechanical, stationary and non−stationary noise, the chip preserves voice naturalness for greater voice clarity and speech intelligibility even when the talker is further away or not optimally aligned with the microphones, providing unmatched freedom of movement for end−users. Designed to be compatible with a wide range of codecs, baseband chips and microphones without the need for calibration, BelaSigna R262 is easy to integrate, improving manufacturers' time to market.

Additional features include the ability to provide two simultaneously processed outputs and to configure them depending on the needs of a manufacturer's device. The chip includes a highly optimized DSP−based application controller with industry−leading energy efficiency and is packaged in a highly compact 5.3 mm^2 WLCSPs to fit into even the most sized−constrained architectures while allowing the use of common industry printed circuit board design technologies.

Key Features and Benefits

- Drop−in Solution that Works without Special Tuning
- Consistently Captures Voice Regardless of Acoustic Environment or the Orientation of the Handheld Device While in Use
- 360° Voice Pick−up Adjustable From 5 cm to 5 m
- No Constraints on Industrial Design or Microphone Model
- Simultaneous Dual−configurable Outputs
- De−reverberation
- Low Power Consumption (17 mA active and 40 μA stand−by)
- Miniature Size Allows Easy Integration into Existing Industrial Designs

Typical Applications

- Mobile Phones
- Notebook and Tablet Computers
- Two−Way Radios and PTT Devices
- VoIP Applications
- Any Device that would Benefit from Improved Voice Pick−up

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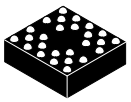

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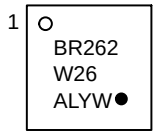
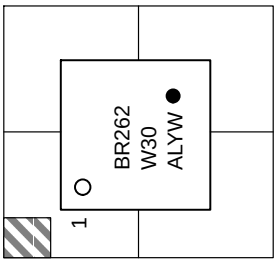
MARKING DIAGRAMS



BR262	= BelaSigna R262
W26	= 26−ball version
A	= Assembly Location
L	= Wafer Lot
YW	= Date Code Year & Week
●	= Pb−Free Package
○	= A1 Corner Indicator

ORIENTATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 22 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Power Supply (Applies on VBAT, VBATRCVR and VDDO for “Max” and for VSSA, VSSRCVR and VSSD for “Min”) (Note 1)	−0.3	4.0	V
Digital input pin voltage	VSSD − 0.3 V	VDDO + 0.3 V	V
Operating temperature range	−40	85	°C
Storage temperature range	−40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Time limit at maximum voltage must be less than 100 ms.

NOTE: Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

This device series incorporates ESD protection and is tested by the following methods:
- ESD Human Body Model (HBM) tested per AEC−Q100−002 (EIA/JESD22−A114)
- ESD Machine Model (MM) tested per AEC−Q100−003 (EIA/JESD22−A115)

This device series incorporates latch−up immunity and is tested in accordance with JESD78.

Electrical Performance Specifications

Table 2. ELECTRICAL CHARACTERISTICS (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
OVERALL							
Supply voltage	VBAT		1.65	3.3	3.63	V	
Maximum rise time		Between 0 V and 1.8 V			10	ms	
Average current consumption		Active mode, VBAT = 3.3 V, EXT_CLK = 2.048 MHz	16.0	16.5	17.0	mA	
		Bypass mode, VBAT = 3.3 V, EXT_CLK = 2.048 MHz	16.0	16.5	17.0	mA	
		Bypass mode, VBAT = 3.3 V, Internal clock	2.7	2.8	2.9	mA	
		Sleep mode, VBAT = 3.3 V	39	40		μA	
Peak active current		VBAT = 3.63 V		19	21	mA	
VREG (1 μF External Capacitor)							
Output voltage	VREG	Without load, or with microphone attached (0 to 200 μA)	0.95	1.00	1.05	V	●
PSRR		@ 1 kHz	40			dB	
Load regulation		@ 2 mA		5	20	mV/mA	
Load current					2	mA	
Line regulation			−1		5	mV/V	
VDDA (1 μF External Capacitor on VDDA + 100 nF External Capacitor on CAP0/CAP1)							
Output voltage	VDDA	Unloaded with VREG = 1 V	1.8	2.0	2.1	V	●
PSRR		@ 1 kHz	45			dB	
Load regulation		@ 1 mA		100	140	mV/mA	
Load current					1	mA	
Line regulation					2	mV/V	
VDDD (1 μF External Capacitor)							
Output voltage	VDDD		1.62	1.70	1.98	V	●

Table 2. ELECTRICAL CHARACTERISTICS (continued) (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
VMIC							
Output voltage		VMIC = VREG	0.95	1.00	1.05	V	●
		VMIC = VDDA	1.8	2.0	2.1	V	●
Load Regulation		VMIC = VREG		25	40	mV/mA	
		VMIC = VDDA		100	150	mV/mA	
POWER ON RESET							
POR Threshold		POR Release (VBAT going up)	1.52	1.60	1.71	V	●
		POR Activation (VBAT going down)	1.52	1.60	1.65	V	●
Boot Time		NRST to DMIC active using LSAD boot method		16.3		ms	
		NRST to DMIC active using SPI EEPROM boot method (Default custom application)		90		ms	
		NRST to DMIC active using I2C EEPROM boot method (Default custom application)		135		ms	
INPUT STAGE							
Sampling frequency	Fs	Defined by ROM−based application. (Note 2)		21.333		kHz	
Analog input voltage	Vin	No preamp gain on AI1 and AI3	0		2	Vpp	
	Vin	24 dB preamp gain by default on MIC0 and MIC2	0		125	mVpp	
Preamplifier gain tolerance		1 kHz	−2		2	dB	
Input impedance	Rin	0 dB preamplifier gain		250		kΩ	
		All other gain settings	510		585	kΩ	●
Input offset voltage		0 dB preamp gain			7	mV	
		All other gains			3	mV	
Channel cross coupling		Any 2 channels		−84	−60	dB	
Analog Filter cut−off frequency		LPF enabled (default)	10	20	30	kHz	
		LPF disabled	50			kHz	
Analog Filter passband flatness			−1		1	dB	
Analog filter stopband attenuation			60			dB	
Digital Filter cut−off frequency				Fs/2		kHz	
Digital Filter cut−off stopband attenuation			80			dB	
Total Harmonic Distortion + Noise (Peak value)	THDN	24 dB preamplifier gain VBAT = 3.3 V	−67	−70		dB	
Dynamic Range	DR	24 dB preamplifier gain VBAT = 3.3 V	81	82.5		dB	
Equivalent Input Noise	EIN	24 dB preamplifier gain VBAT = 3.3 V		3.7		μV	

2. Processed bandwidth limited to 8 kHz.

Table 2. ELECTRICAL CHARACTERISTICS (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
DIGITAL MICROPHONE OUTPUT							
DMIC input clock frequency		With preset 0 selected on CLOCK_SEL (Note 3)		2.048		MHz	
		With preset 3 selected on CLOCK_SEL (Note 3)		2.4		MHz	
		With preset 4 selected on CLOCK_SEL (Note 3)		2.8		MHz	
		With preset 5 selected on CLOCK_SEL (Note 3)		3.072		MHz	
Clock duty cycle		Any clock configuration	40	50	60	%	
Input clock jitter		Maximum allowed jitter on the DMIC_CLK			10	ns	
Clock to output transition time	DMIC_OUT		10	20	50	ns	
ANALOG OUTPUT STAGE							
Signal Range	Vout	One single ended DAC used	0		2	Vpp	
		Two DACs used as one differential output	0		4	Vpp	
Attenuator gain tolerance			−2		2	dB	
Output impedance	Rout	@ 12 dB output attenuation			19	kΩ	●
		@ 0 dB output attenuation			3	kΩ	
Channel cross coupling		@ 1 kHz			−50	dB	
Analog Filter cut−off frequency		LPF Enabled (default)	13.0		13.5	kHz	
		LPF Disabled	25		26	kHz	
Analog Filter passband flatness			−1		1	dB	
Analog filter stopband attenuation		> 60 kHz	90			dB	
Digital Filter cut−off frequency				Fs/2		kHz	
Digital Filter cut−off stopband attenuation			80			dB	
Total Harmonic Distortion + Noise (Peak value)	THDN		63	65		dB	●
Dynamic Range	DR		78	80		dB	●
Noise Floor				70	100	μV	●
DIRECT DIGITAL OUTPUT (available only through custom configuration)							
Supply voltage	VBATRCVR		1.8	3.3	3.63	V	
Signal Range	Vout	Differential Output @ 1 kHz	0		2*VBAT RCVR	Vpp	
		Single ended Output @ 1 kHz	0		VBAT RCVR	Vpp	
Output Impedance	Rout	Load between 1 mA and 30 mA @ 0°C		2.5	10	Ω	
Maximum Current					25	mA	
Total Harmonic Distortion + Noise (Peak value)	THDN		64	70		dB	●

3. Many other clock frequencies are available through custom configuration of the internal PLL and clocking subsystem. See later in this document and in the BelaSigna R262 Communications and Configuration Guide for more information on custom mode usage.

Table 2. ELECTRICAL CHARACTERISTICS (continued) (The typical parameters in Table 2 were measured at 20°C with a clean 3.3 V supply voltage (unless noted differently). Parameters marked as screened are tested on each chip. Other parameters are qualified for all process corners but not tested on every part.)

Parameter	Symbol	Test Conditions / Notes	Min	Typ	Max	Unit	Screened
DIRECT DIGITAL OUTPUT (available only through custom configuration)							
Dynamic Range	DR		80	86		dB	●
Noise Floor				50	75	μV	●
LOW−SPEED A/D							
Input voltage	Vin		0		2*VREG	V	
Sampling frequency		For each LSAD channel	1.6	MCLK/28	4.8	kHz	
Input impedance	Rin		1			MΩ	
Offset error		Input at VREG	−10		10	LSB	
Gain error		Input to VSSA or 2*VREG	−10		10	LSB	
INL	INL		−4		4	LSB	
DNL	DNL		−2		2	LSB	
DIGITAL PADS (VDDO = 1.8 V)							
Voltage level for Low input	VIL		−0.3		0.4	V	
Voltage level for High input	VIH		1.30		1.98	V	
Pull−up resistance			63	114	162	kΩ	
Pull−down resistance			87	153	205	kΩ	
Rise and Fall Time		20 pF load	2	3	5	ns	
DIGITAL PADS (VDDO = 3.3 V)							
Voltage level for Low input	VIL		−0.3		0.8	V	●
Voltage level for High input	VIH		1.8		3.6	V	●
Pull−up resistance			34	46	74	kΩ	●
Pull−down resistance			29	56	86	kΩ	●
Rise and Fall Time		20 pF load	1.0	1.5	2.0	ns	
DIGITAL PADS (Common parameters)							
Drive Strength				12		mA	
ESD Immunity	HBM	Human Body Model	2			kV	
	MM	Machine Model	200			V	
Latch−up Immunity		25°C, V < GNDO, V > VDDO	150			mA	
CLOCKING CIRCUITRY							
External clock frequency	EXT_CLK	With preset 6 selected on CLOCK_SEL (Note 3)		26		MHz	
Internal clock frequency	INT_CLK	With preset 7 selected on CLOCK_SEL (Note 3) Bypass Mode		5.2		MHz	
		With preset 7 selected on CLOCK_SEL (Note 3) Active Mode		48.2		MHz	
Reference clock duty cycle			40	50	60	%	
External Input clock jitter		Maximum allowed jitter on EXT_CLK			10	ns	
I^2C INTERFACE							
Maximum speed					400	kbps	

3. Many other clock frequencies are available through custom configuration of the internal PLL and clocking subsystem. See later in this document and in the BelaSigna R262 Communications and Configuration Guide for more information on custom mode usage.

Table 3. PIN CONNECTIONS

Pin Index	Pin Name	Description	A/D/P	I/O	Active	Pull
G1	MIC0	First microphone input	A	I		
E1	MIC2	Second microphone input	A	I		
E3	AI3/VMIC/LOUT0	Direct audio input / microphone bias / line−out preamp 0	A	I/O		
E7	A_OUT1	Audio output 1	A	O		
G7	CAP0	Charge pump capacitor connection	A	I/O		
F8	CAP1	Charge pump capacitor connection	A	I/O		
A1	DEBUG_RX	RS232 debug port serial input	D	I	L	U
B2	DEBUG_TX	RS232 debug port serial output	D	O	L	
F2	RESERVED	Reserved				
A3	EXT_CLK	External clock input	D	I		U
A7	SPI_CLK/CLOCK_SEL	SPI clock / Clock selection	D/A	O/I	L/−	
A9	SPI_CS/BOOT_SEL	SPI chip select / Booting method selection	D/A	O/I		
B8	SPI_SERO/CHAN_SEL	SPI serial output / Channel selection	D/A	O/I		
C9	SPI_SERI/ALPHA_SEL	SPI serial input / Mixing ratio selection	D/A	I/I		U/−
C7	DMIC_OUT	Digital microphone output	D	O		
C3	I2C_SDA	I^2C data	D	IO	L	U
C1	I2C_SCL	I^2C clock	D	IO	L	U
F6	VBAT	Power supply	P	I		
G9	VBATRCVR	Output driver power supply	P	I		
G5	VDDA	Analog supply voltage	P	O		
B6	VDDD	Digital power supply	P	O		
B4	VDDO	Digital I/O power supply	P	I		
G3	VREG	Analog supply voltage	P	O		
F4	VSSA	Analog ground	P	I		
A5	VSSD	Digital ground	P	I		
E9	VSSRCVR	Output driver ground	P	I		

A: Analog pin
D: Digital pin
P: Power pin
I: Input
O: Output
IO: Bi−directional
I/O & O/IL: Input or Output depending on the function being used
L: Active Low
H: Active High
U: Pulled up internally
D: Pulled down internally

Application Diagrams

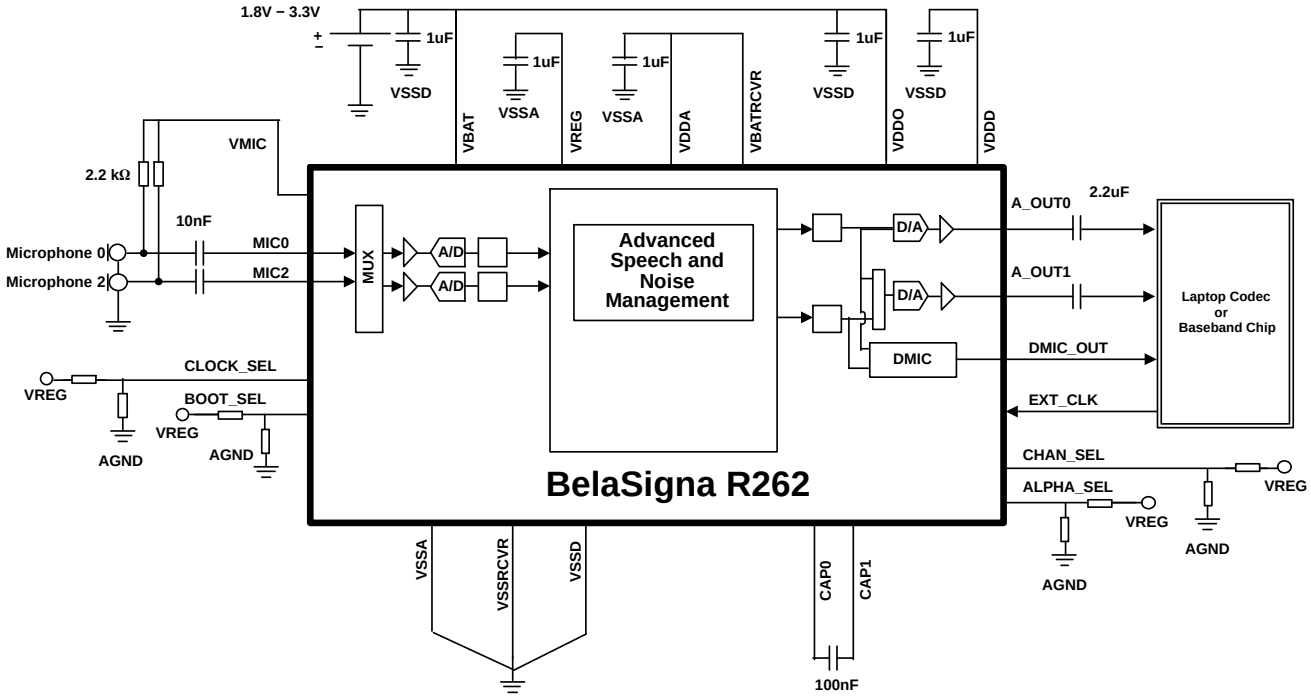


Figure 1. Typical Application Diagram

Applications Information

Recommended Circuit Design Guidelines

BelaSigna R262 is designed to allow both digital and analog processing in a single system. Due to the mixed−signal nature of this system, careful design consideration of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BelaSigna R262. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

Recommended Ground Design Strategy

The ground plane should be partitioned into two parts: the analog ground plane (VSSA) and the digital ground plane (VSSD). These two planes should be connected together at a single point, known as the star point. The star point should be located close to the negative terminal of the power source, as illustrated in Figure 2.

All ground returns should be routed separately back to the appropriate ground plane, i.e. do not share a ground return.

Ensure that different ground and/or power planes do not overlap each other if located on different layers in the board.

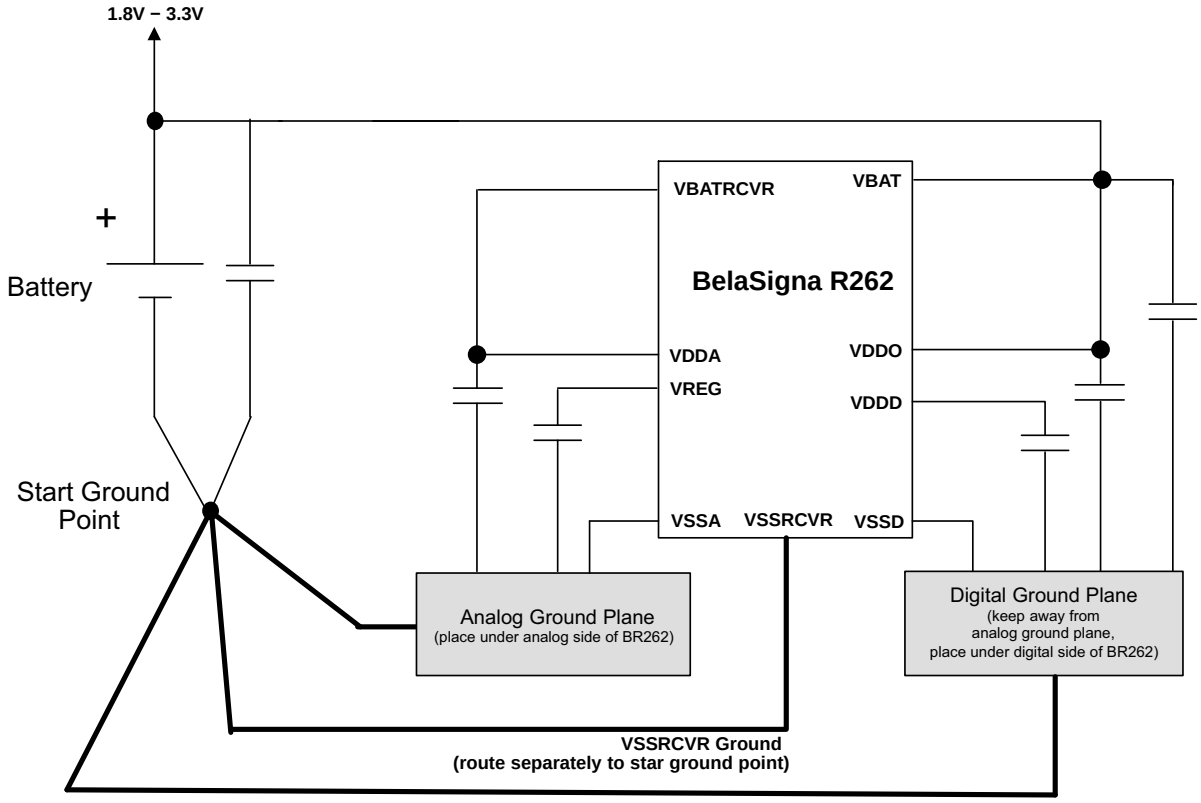


Figure 2. Schematic of Ground Scheme

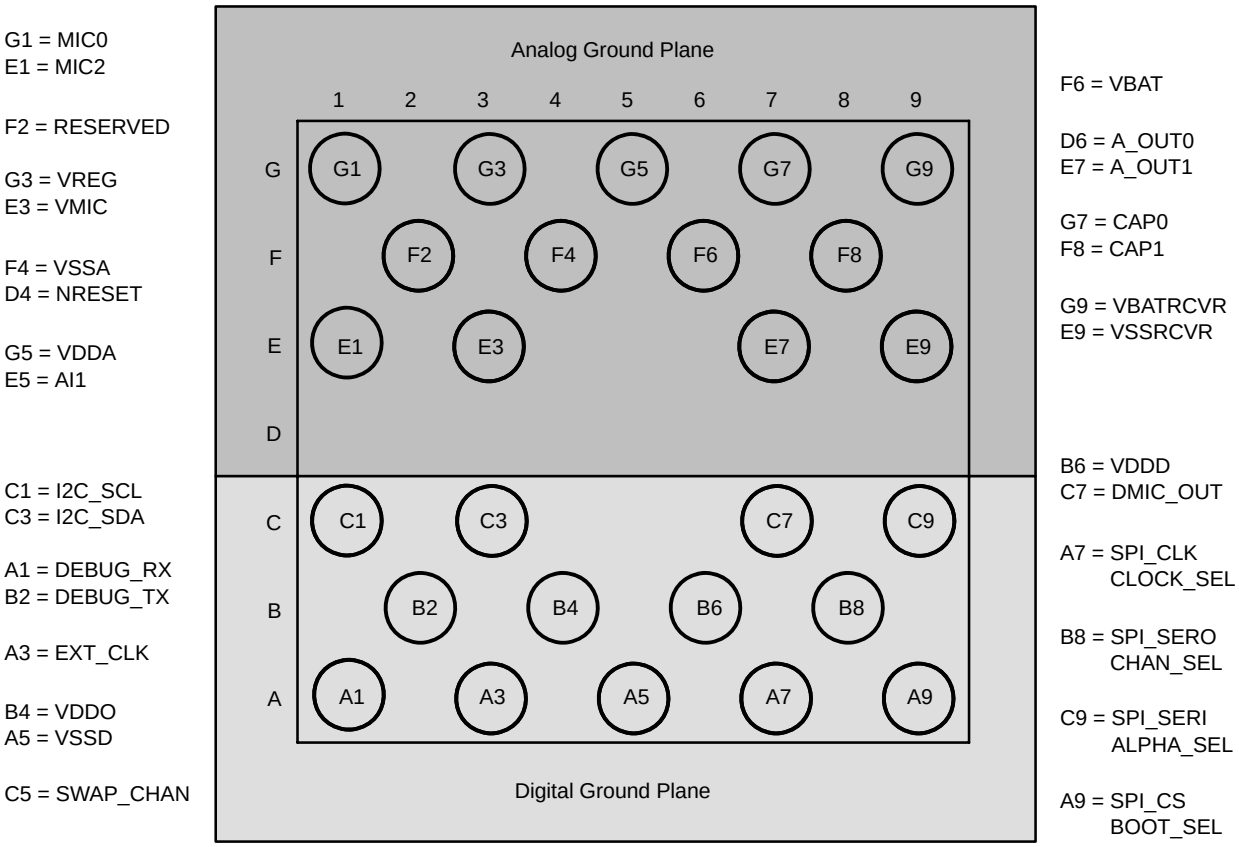


Figure 3. Proposed Ground Plane Positioning (soldering footprint view)

The VSSD plane is used as the ground return for digital circuits and should be placed under digital circuits. The VSSA plane should be kept as noise−free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or digital pads of BelaSigna R262 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For details on which signals require special design consideration, see Table 4 and Table 5.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

Internal Power Supplies

Power management circuitry in BelaSigna R262 generates separate digital (VDDD) and analog (VREG, VDDA) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads.

The digital I/O levels are defined by a separate power supply pin on BelaSigna R262 (VDDO). This pin must be externally connected by the application PCB, usually to VBAT.

Further details on these critical signals are provided in Table 4. Non−critical signals are outlined in Table 5. More information on the power supply architecture can be found in the Power Supply Unit section.

Table 4. CRITICAL SIGNALS

Pin Name	Description	Connection Guidelines
VBAT	Power supply	Place 1 μF (min) decoupling capacitor close to pin Connect negative terminal of capacitor to digital ground plane
VREG, VDDA	Internal regulator for analog blocks	Place separate 1 μF decoupling capacitors close to each pin Connect negative capacitor terminal to analog ground plane Keep away from digital traces and output traces VREG and VDDA may be used to generate microphone bias
VSSA	Analog ground return	Connect to analog ground plane
VDDD	Internal regulator for digital core	Place 1 μF decoupling capacitor close to pin Connect negative terminal of capacitor to digital ground plane
VSSD	Digital ground return	Connect to digital ground plane
VDDO	Digital I/O power	Place 1 μF decoupling capacitor close to pin Connect negative terminal of capacitor to digital ground plane Connect to VBAT, unless the pad ring must use different voltage levels
MIC0, MIC2, AI1/LOUT1, AI3/VMIC/LOUT0	Audio inputs / Microphone bias	Keep traces as short as possible Keep away from all digital traces and audio outputs Avoid routing in parallel with other traces Never connect AI3/VMIC/LOUT0 to ground
A_OUT0, A_OUT1	Audio outputs	Keep away from audio inputs Differential traces should be of approximately the same length Ideally, route lines parallel to each other
VSSRCVR	Output stage ground return	Connect to star ground point Keep away from all analog audio inputs
EXT_CLK	External clock input	Minimize trace length Keep away from analog signals If possible, surround with digital ground
DMIC_OUT	Digital Microphone Output	Minimize trace length Keep away from analog signals If possible, surround with digital ground

Table 5. NON−CRITICAL SIGNALS

Pin Name	Description	Connection Guidelines
CAP0, CAP1	Internal charge pump − capacitor connection	Place 100 nF capacitor very close to pins
I2C_SDA, I2C_SCL	I^2C port	Keep as short as possible. Place pull−up resistors (10 kΩ) to VDDO
SWAP_CHAN	Control GPIO	Not critical when used as GPIO
CLOCK_SEL, BOOT_SEL, CHAN_SEL and ALPHA_SEL	Low−speed A/D converters (Multiplexed with SPI port)	Not critical when used as LSAD Place resistive divider for hardware configuration of BelaSigna R262
SPI_CLK, SPI_CS, SPI_SERO, SPI_SERI	Serial peripheral interface port (Multiplexed with LSAD and GPIOs)	Keep away from analog input lines when used as SPI signals
NRESET	Reset	Not critical Leave unconnected if unused
DEBUG_RX, DEBUG_TX	Debug Port	Not critical If possible, connect to test points, otherwise connect DEBUG_RX to VDDO and leave DEBUG_TX floating
RESERVED	Reserved pin	Leave unconnected or connect to VSSA if PCB routing constraints force it
VBATRCVR	Output driver power supply	If the output driver is being used: − Place a separate 4.7 μF (min. 2.2 μF) decoupling capacitor close to pin − Connect positive terminal of capacitor to VBAT & VBATRCVR − Connect negative terminal of capacitor to VSSRCVR If the analog outputs or the DMIC output are being used: − Separate decoupling capacitor on VBATRCVR is not required − Connect VBATRCVR to VDDA (which has its own decoupling capacitor)

Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., MIC0, AI1, MIC2, AI3) is high (approximately 500 kΩ with preamplifiers enabled); therefore a 10 nF capacitor is sufficient to decouple the DC bias. This capacitor and the internal resistance form a first−order analog high pass filter whose cut−off frequency can be calculated by f_{3dB} (Hz) = 1/(R x C x 2π), which results in ~30 Hz for a 10 nF capacitor. This 10 nF capacitor value applies when the preamplifier is being used, in other words, when a non−unity gain is applied to the signals; for MIC0 and MIC2, the preamplifier is enabled by the ROM−based application. When the preamplifier is bypassed, the impedance is reduced; hence, the cut−off frequency of the resulting high−pass filter could be too high. In such a case, the use of a 30−40 nF serial capacitor is recommended. In cases where line−level analog inputs without DC bias are used, the capacitor may be omitted for transparent bass response. ON Semiconductor recommends the use of NPO/COG dielectric for SMT capacitors, as they have demonstrated better performance compared to other capacitors with X7R dielectric.

Microphone Power Supply

BelaSigna R262 provides a microphone power supply (VMIC) and ground (VSSA). In case VMIC cannot be used because of PCB routing constraints, the power supplies VREG (1.0 V) or VDDA (2.0 V) can alternatively be used. Keep audio input traces strictly away from output traces. Audio outputs must be kept away from microphone inputs to avoid cross−coupling.

Audio Outputs

The audio output traces should be as short as possible. The trace length of the two signals should be approximately the same to provide matched impedances.

Recommendation for Unused Pins

Table 6 shows the connection details for each pin when they are not used.

Table 6. UNUSED PIN RECOMMENDATIONS

Signal Name	Connection Guidelines
A_OUT0	Do not connect
A_OUT1	Do not connect
AI3/VMIC/LOUT0	Do not connect
AI1/LOUT1	Connect to VSSA
DMIC_OUT	Do not connect
SWAP_CHAN	Do not connect
NRESET	Do not connect

Architecture Detailed Information

The architecture of BelaSigna R262 is shown in Figure 4.

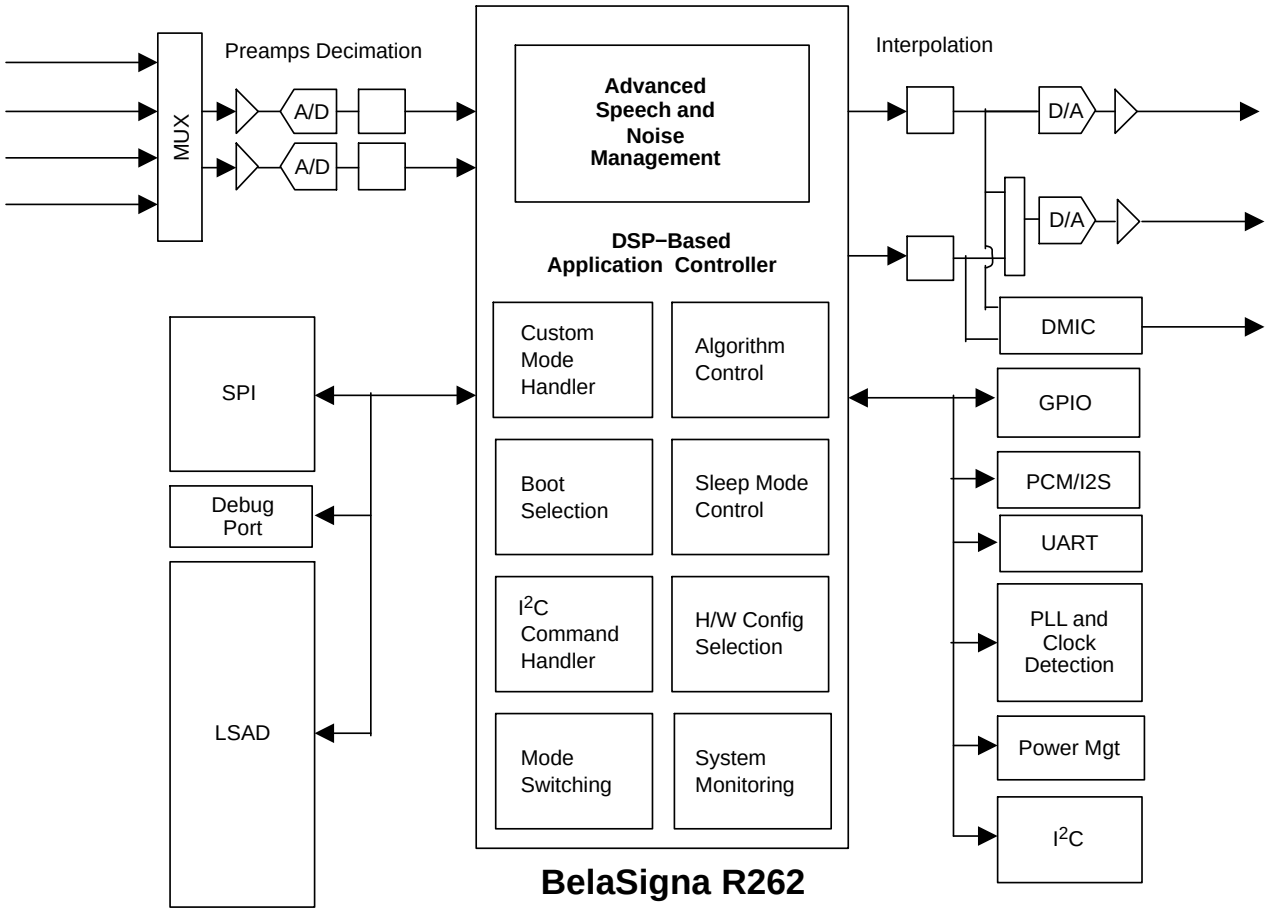


Figure 4. BelaSigna R262 Architecture: A Complete Audio Processing System

Algorithm Performance and Configuration

A detailed description of the functional blocks of the algorithm contained in BelaSigna R262, as well as performance metrics can be found in AND9109/D − Getting Started with BelaSigna R262.

For details on the configuration of the algorithm, refer to the BelaSigna R262 Communications and Configuration Guide.

Microphone Placement & Selection

The flexibility of the BelaSigna R262 noise reduction algorithm doesn't restrict microphone placements, but the default algorithm will operate optimally with omnidirectional microphones placed in the following configuration:

- The two microphones are facing the user's mouth
- The microphone centers are located within 10 to 25 mm from each other

As mentioned, other configurations that differ from the above guidelines are supported. For example, a 15 cm distance between the two microphones will not degrade the performance as long as the microphones are both facing the user's mouth. Alternatively, a configuration with one microphone at the front and one microphone at the back will not degrade the performance either, as long as the distance between the microphones is no more than 2 cm.

BelaSigna R262 does not require any acoustic microphone calibration procedure.

When selecting microphones to be used with BelaSigna R262, the following guidelines should be used:

- Two omni−directional microphones with similar characteristics should be used
- The microphone sensitivity should be approximately −42 dB (where 0 dB = 1 V/Pa, at 1 kHz)
- The microphones are two−terminal microphones
- The microphone power supply is either 1 V (recommended), or 2 V if it is to be provided by BelaSigna R262
- The dynamic range of BelaSigna R262 on its analog input channels is 2.0 V peak−to−peak, after amplification by the default gain value of 24 dB using BelaSigna R262's input preamplifiers
- When higher sensitivity microphones are used, the preamp gain should be adjusted to match the 2.0 Vpp input voltage swing on BelaSigna R262, but this will require special configuration of the ROM application, as described later. As an example, using microphones with a −22 dB sensitivity typically requires that the preamplifier gains be changed down to 12 dB.
- When MEMS microphone are to be used, a general increase of the algorithm performance can be expected due to the improved self noise of these microphones, compared to conventional electret microphones. For applications requiring microphone configurations differing significantly from the above recommendations, contact your local ON Semiconductor support representative.

Operating Modes

The default application stored in the ROM of BelaSigna R262 has four Operating Modes. The Operating Modes are summarized in Table 7.

Table 7. OPERATING MODES SUMMARY

Operating Mode	Switching	Description
Active	Active mode can be entered at boot time, depending on the BOOT_SEL configuration and when exiting Sleep mode. Active mode can also be entered via an I^2C command from another mode.	In Active mode, the noise reduction algorithm is executed. While in Active mode, BelaSigna R262 collects statistics on the input signals that can be retrieved via I^2C. These signal statistics can be used for level calibration and other debugging. For more information using Active mode for calibration and debugging see the BelaSigna R262 Communications and Configuration Guide.
Bypass	Bypass mode can be entered at boot time, depending on the BOOT_SEL configuration. It can also be entered via an I^2C command from another mode.	In Bypass mode, no signal processing is done on the audio inputs. The inputs are passed directly to the audio outputs. While in Bypass mode, BelaSigna R262 collects statistics on the input signals that can be retrieved via I^2C. These signal statistics can be used for level calibration and other debugging. For more information using Bypass mode for calibration and debugging see the BelaSigna R262 Communications and Configuration Guide.
Sleep	Sleep mode can be entered via I^2C commands. When Sleep mode is entered via I^2C, the chip will exit Sleep mode only based on activity on the I^2C_SCL pin. Sleep mode will be automatically entered if BelaSigna R262 detects that a required external clock is no longer present. For more information, see the Sleep Control section below.	In Sleep mode no signal processing is done. All analog blocks of the chip are disabled and the digital core continues to run off an internal low−speed oscillator, thereby allowing the external clock to be disabled when the chip is asleep. This is BelaSigna R262's lowest power operating mode.
Stand−By	Stand−By mode is an intermediate mode that is only used when exiting sleep mode by an I^2C command.	When I^2C is used to exit Sleep mode, the application will transition to Stand−By mode, and will wait until the master I^2C device issues a Switch_Mode command to enter another processing mode like Active or Bypass. If no such command is issued, BelaSigna R262 will return to Sleep mode and wait for a valid wake−up sequence.

Boot Control, Hardware Configuration and Digital Control

At power−on−reset, BelaSigna R262 will normally execute the application stored in ROM. During the boot process, BelaSigna R262 will read voltage levels on four different pins, which will determine the algorithm and hardware configuration that will be executed. All the configuration options are described later in this section; the four pins are CLOCK_SEL, BOOT_SEL, CHAN_SEL and ALPHA_SEL.

The BOOT_SEL pin controls the booting methods of BelaSigna R262. The signal on this pin is sampled by BelaSigna R262 during its booting process using a low−speed A/D converter (LSAD). Based on the actual voltage that the chip will read on this pin, it will automatically select a particular booting configuration, as described in Table 8.

Table 8. BOOT SELECTION OPTIONS (Note 4)

Preset	Voltage Level	Boot Method	Description
0−2	0.65 − 1.00 V	External Boot Mode	In this mode, BelaSigna R262 will not run the ROM based application. It will start looking for an SPI EEPROM to bootload a custom application from. If unsuccessful, it will look for an I^2C EEPROM to bootload a custom application; and lastly, if neither of the two previous operations to find an EEPROM are successful, it will enter a wait loop, allowing a master I^2C device to start downloading a custom application (e.g. a baseband controller).
3	0.50 − 0.63 V	Active Mode Talking distance selectable from Near− to Far−Talk (50 cm to 500 cm)	The noise reduction algorithm is running and can be configured for talking distances between 50 cm (Near−Talk) and 5 m (Far−Talk)
4	0.36 − 0.49 V	Active Mode Talking distance selectable from Close− to Far−Talk (5 cm to 500 cm)	The noise reduction algorithm is running and can be configured for talking distances between 5 cm (Close−Talk) and 5 m (Far−Talk)
5	0.22 − 0.35 V	Active Mode Talking distance selectable from Close− to Near−Talk (5 cm to 100 cm)	The noise reduction algorithm is running and can be configured for talking distances between 5 cm (Close−Talk) and 1 m (Near−Talk)
6	0.08 − 0.21 V	Bypass Diagnostic Mode 1 kHz sine wave play−out	BelaSigna R262 outputs a pure tone on the two output channels. This sine wave has a frequency of 1 kHz and an output level of 12 dB below full scale.
7	0 − 0.07 V	Bypass Diagnostic Mode Full stereo passthrough	BelaSigna R262 simply copies the input signals to the outputs.

4. For more details on the various operating modes of BelaSigna R262, please consult the BelaSigna R262 Communications and Configuration Guide.

Clocking, Channels & Algorithm Configuration

As mentioned in the Boot Control section, BelaSigna R262 is controlled by hardware configuration. Just like the BOOT_SEL signal discussed earlier, the CLOCK_SEL, CHAN_SEL and ALPHA_SEL pins are also sampled by BelaSigna R262 during its booting process using a low−speed A/D converters (LSAD). Based on the actual voltage that the chip reads on these pins, it will automatically select a particular clock, output stage, channels and algorithm configuration, as described in Tables 9, 10 and 11.

Table 9. CLOCK CONFIGURATION OPTIONS

Preset	Voltage Level	Clock Frequency	Description
0−2	0.65 − 1.00 V	2.048 MHz	A 2.048 MHz external clock is expected to be present on the EXT_CLK pin of BelaSigna R262
3	0.50 − 0.63 V	2.4 MHz	A 2.4 MHz external clock is expected to be present on the EXT_CLK pin of BelaSigna R262
4	0.36 − 0.49 V	2.8 MHz	A 2.8 MHz external clock is expected to be present on the EXT_CLK pin of BelaSigna R262
5	0.22 − 0.35 V	3.072 MHz	A 3.072 MHz external clock is expected to be present on the EXT_CLK pin of BelaSigna R262
6	0.08 − 0.21 V	26 MHz	A 26 MHz external clock is expected to be present on the EXT_CLK pin of BelaSigna R262
7	0 − 0.07 V	Internal Oscillator	BelaSigna R262 runs off its internal system clock. No clock signal must be present on the EXT_CLK pin. In this mode the sampling frequency can fluctuate slightly from one device to another; see the electrical characteristics for additional details. The performance of the algorithm itself is fully guaranteed.

Table 10. CHANNEL CONFIGURATION OPTIONS

Preset	Voltage Level	NR Outputs	Channel 0	Channel 1	Output Stage Configuration
0−2	0.65 − 1.00 V	Single	Start of Range (as per BOOT_SEL)	N/A	Mono, Differential
3	0.50 − 0.63 V	Dual	Start of Range (as per BOOT_SEL)	Mixed Output (as per BOOT_SEL & ALPHA_SEL)	Stereo, Single Ended
4	0.36 − 0.49 V	Dual	Mixed Output (as per BOOT_SEL & ALPHA_SEL)	End of Range (as per BOOT_SEL)	Stereo, Single Ended
5	0.22 − 0.35 V	Single	Mixed Output (as per BOOT_SEL & ALPHA_SEL)	N/A	Mono, Differential
6	0.08 − 0.21 V	Single	Mixed Output (as per BOOT_SEL & ALPHA_SEL)	Algorithm Disabled	Stereo, Single Ended
7	0 − 0.07 V	Single	Algorithm Disabled	Mixed Output (as per BOOT_SEL & ALPHA_SEL)	Stereo, Single Ended

Table 11. MIXER CONFIGURATION OPTIONS

Preset	Voltage Level	Mixing Ratio
0−2	0.65 − 1.00 V	0% (Start of Range)
3	0.50 − 0.63 V	20% (Between Start and End of Range)
4	0.36 − 0.49 V	40% (Between Start and End of Range)
5	0.22 − 0.35 V	60% (Between Start and End of Range)
6	0.08 − 0.21 V	80% (Between Start and End of Range)
7	0 − 0.07 V	100% (End of Range)

The use of a resistive divider as shown in Figure 5 allows the application to select the appropriate combination of clock, output stage and algorithm mode. The LSAD is using a voltage range between 0 and 1 V. The actual voltage levels that need to be guaranteed by the application circuitry are also mentioned in Figure 5. The figure proposes actual resistor values to reach the eight different presets.

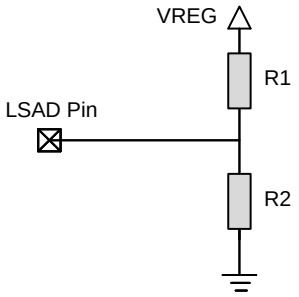


Figure 5. Resistive Dividers for LSAD Preset Selection

Preset	R1	R2	Voltage Range
0−2	10 kΩ	−	0.65 − 1.00 V
3	75 kΩ	100 kΩ	0.50 − 0.63 V
4	100 kΩ	75 kΩ	0.36 − 0.49 V
5	100 kΩ	39 kΩ	0.22 − 0.35 V
6	100 kΩ	16 kΩ	0.08 − 0.21 V
7	−	10 kΩ	0 − 0.07 V

The configuration is only read by the chip at boot time. Consequently, if the voltage on any of the four LSAD inputs changes during operation, it will only have an impact at the next power cycle.

Channel Swapping

BelaSigna R262 has provisions to swap the two output channels by using an external GPIO pin (SWAP_CHAN). The two output channels of BelaSigna R262 can be swapped whenever the digital signal on this pin transitions to low and stays low for at least 200 ms, as shown in Figure 6. The actual channel swapping can occur at any time during the 200 ms low period of the signal. This control mechanism has built-in button de-bouncing and will work with either a digital signal driven high or low by a host controller, or with a control signal provided by a mechanical button or switch.

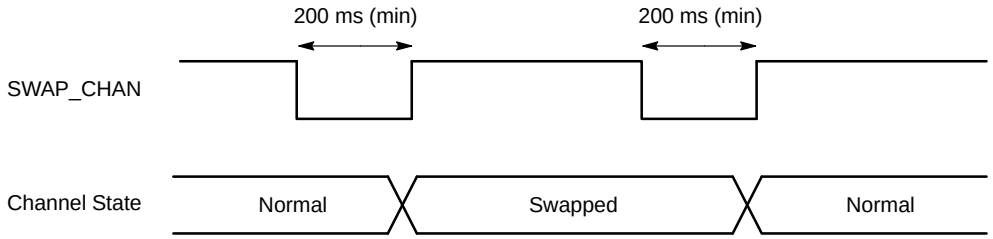


Figure 6. SWAP_CHAN Timing Diagram

Sleep Control

As described in Table 7, there are two methods to enter and exit from Sleep mode. Both of these methods are meant to be used independently, i.e. methods of putting the system into Sleep mode and waking it up from Sleep mode cannot be mixed in the same system design.

The first method for Sleep mode control is via the I^2C interface. The *Switch_Mode* command can be used directly to switch the system into and out of Sleep mode. If the *Switch_Mode* command is used to put the chip into Sleep mode, only another *Switch_Mode* command or a reset will take the system out of Sleep mode. When waking up by I^2C commands, the following I^2C operations have to be performed by the master I^2C to ensure proper wake−up:

1. Send a *NOP* command to wake up the I^2C interface. This command will not be interpreted by BelaSigna R262, so the master will have to deal with any I^2C errors that result.
2. Send the *Get_Status* command in a while−type loop, until a response from BelaSigna R262 is sent, and that confirms that the application is in Standby Mode.
3. Send a *Switch_Mode* command to enter the desired mode (Active or Bypass).

When the *NOP* command is sent and the chip wakes up, the master has about one second to complete the above procedure before the chip goes back to Sleep mode. This mechanism was put in place to deal with I^2C bus traffic that would wake the chip up unintentionally (i.e. communications between the master and another slave on the I^2C bus).

The second mechanism for entering Sleep mode is considered a fail safe mechanism to maintain a graceful system shutdown in the event that the clock source suddenly disappears. In this circumstance, the chip will enter sleep mode to ensure proper shutdown. More information on this can be found in the System Monitoring section.

I²C Command Handler

The BelaSigna R262 ROM application contains an I²C−based command and control interface, allowing many aspects of the chip's operation and hardware configuration to be controlled via I²C. This I²C interface is the recommended way to control the chip and to configure the application at run−time. The default I²C address of BelaSigna R262 is 0x61. The I²C interface protocol is fully supported by the SignaKlara Device Utility (SKDU) and other software tools provided by ON Semiconductor.

For more information on the I²C interface, please refer to the I²C interface section of this document, as well as the BelaSigna R262 Communications and Configuration Guide.

Reset

BelaSigna R262 can be forced to execute a power−on−reset by pulling the NRESET pin to ground for at least 100 ns. NRESET is not available on the 26−ball WLCSP package.

System Monitoring

The application software within BelaSigna R262 is equipped with a few blocks that monitor system sanity. A watchdog timer is used to ensure proper execution of the signal processing application. It is always active and is periodically acknowledged as a check that the application is still running. Once the watchdog times out, a hardware system reset will occur. System sanity is also monitored by the clock detection mechanism; the chip will automatically enter Sleep mode if it is in Active or Bypass mode and it detects that the external clock source (the signal on EXT_CLK) is stopped. In this case, the system will only exit Sleep mode when it detects that the external clock source has been restored or a reset occurs.

The power supply blocks of the system also monitor for minimum supply voltages as part of the power supervision strategy, as described in the Power Management section.

Analog Blocks

Input Stages

The BelaSigna R262 analog audio input stage is shown in Figure 7. The input stage is comprised of two individual channels. There are four configurable aspects of each channel – input multiplexing, preamplifier gain, filtering and line out. The input multiplexing allows one input to be selected from any of the four possible inputs and then routed to the input of the preamplifier. Each preamplifier can be configured for bypass or gain values of 12 to 30 dB in 3 dB steps. The filters can be configured as well; the DC removal high−pass filter can be bypassed, or set to a cut−off frequency of 5 Hz, 10 Hz or 20 Hz (default). The low−pass filter can be either enabled with a 20 kHz cut−off frequency (default), or bypassed. The lineout selection allows the preamplifier outputs to be routed back out via the auxiliary audio input pins. Note that the AI1/LOUT1 pin is not available on the 26−ball WLCSP package option.

Two analog−to−digital converters then convert the analog signals into the digital domain. The ADCs are running at a sampling rate of 21.3 kHz in Active mode and 16 kHz in Bypass mode. The sampling rate can potentially be changed using the I²C interface. Changing the sampling rate in Active mode will cause the noise cancellation algorithm to stop operating properly, so this should not be done; however, the sampling rate in Bypass mode could be changed to other values. Contact your local technical support for more information.

Input signal amplitudes can also be adjusted in the digital domain; digital gain for both converted signals can be adjusted by using I²C commands.

The ROM−based application pre−configures all these parameters in the input stage such that the algorithm operates properly. These parameters can be changed using the I²C interface, but careful design consideration should be taken when doing so, as this could alter the performance of the algorithm.

The AI3 pin is multiplexed with the microphone power supply (VMIC). The default mode for the microphone bias is to be used as a 2 V power supply. Consequently, any application that plans to use the AI3 input pin or the LOUT0 functionality has to change the VMIC setting to high−impedance mode, such as the pin can be properly used as an analog input or a line−out.

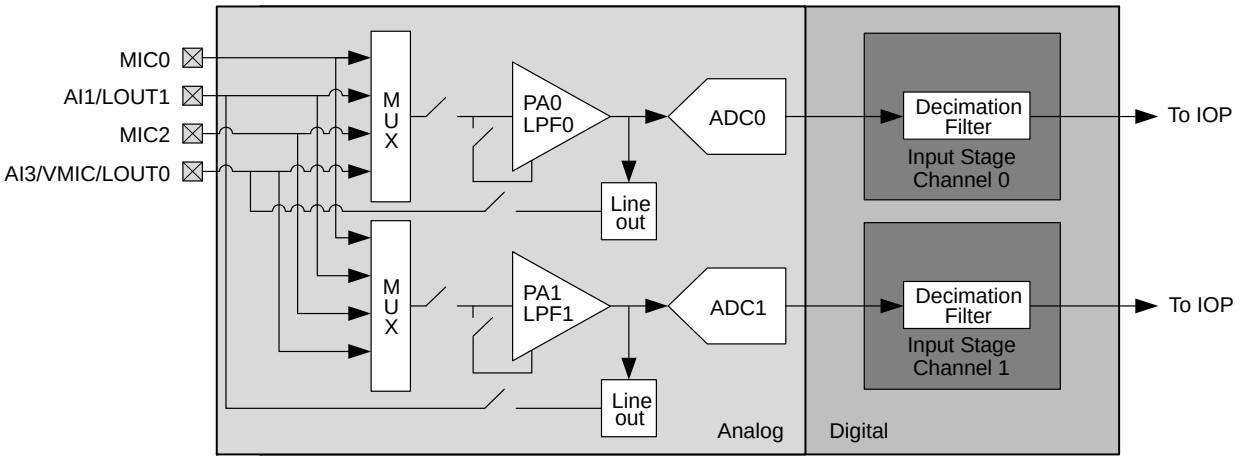


Figure 7. Input Stage

Output Stage

At all times, the application will produce two output channels. The content of each channel is determined by the hardware configuration.

The amplitude of both output channels can be controlled by I^2C commands, independently from the actual output stage configuration that was selected. A first parameter controls gain in 6 dB steps. A second parameter is a variable for fine gain adjustment. With these two parameters, a great level of flexibility is achieved to match the output level requirements of the target device, independently for each of the two output channels. The application has initialized these parameters for proper operation of the algorithm and correct output so careful design consideration should be taken when modifying these parameters.

The BelaSigna R262 output stage is shown in Figure 8. The output stage processes two channels although, depending on the configuration, one or both of the output signals are available on the output pins. There are four options for audio outputs from BelaSigna R262 – a digital microphone (DMIC) interface, a low−impedance output driver, a stereo single−ended analog output or a mono differential analog output. All outputs are generated from a sigma−delta modulator which produces a pulse density modulated (PDM) output signal and then provides it to the appropriate output system, based on the system configuration.

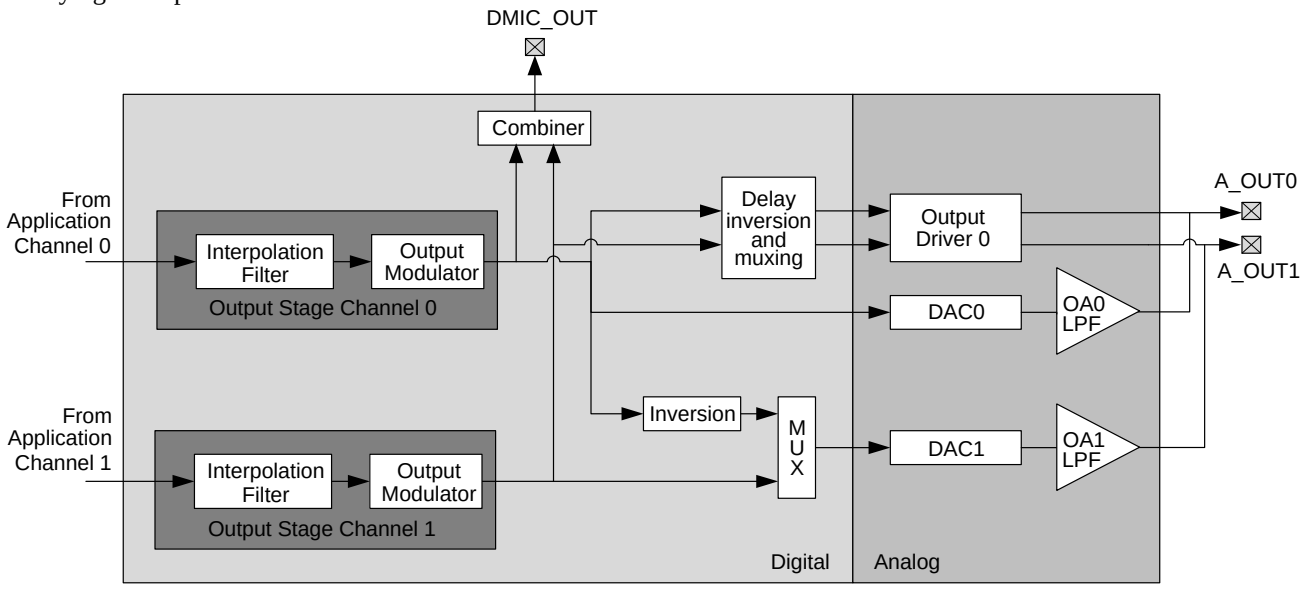


Figure 8. Output Stage

The digital microphone interface provides the PDM signals directly on a pin (DMIC_OUT), for interfacing with the DMIC input of external systems. When using this interface, the EXT_CLK input to BelaSigna R262 must be given a DMIC_CLK signal and the system clocking must be set up such that proper synchronization can happen between the incoming DMIC_CLK and the output data produced by BelaSigna R262 on its DMIC_OUT pin. Various DMIC_CLK frequencies are supported through hardware configuration on the CLOCK_SEL pin, as discussed earlier. Other frequencies can also be supported under certain conditions; see the clocking section of this document for

more information on the supported DMIC clock frequencies.

The DMIC output can be configured to carry a mono or stereo signal. In fact both left and right signals can be configured to either contain output stage channel 0 or output stage channel 1. Also, both left and right can be configured to be muted independently (driving a ‘0’ all the time).

Figure 9 shows the timing of the DMIC output data relative to the incoming DMIC_CLK signal. See Table 2 for electrical specifications of the timing parameters.

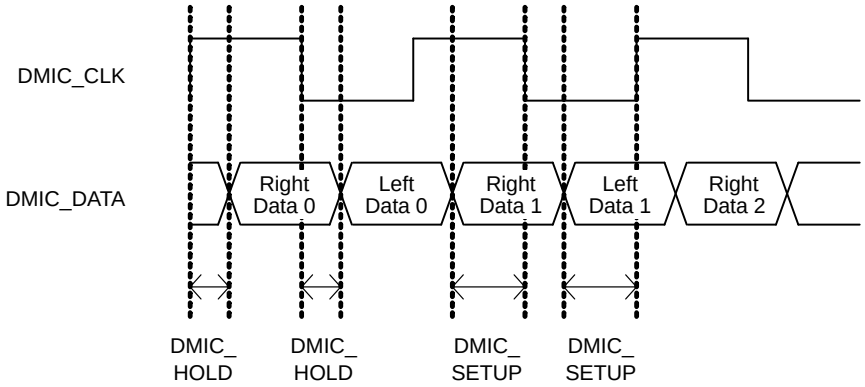


Figure 9. DMIC Timing Diagram

The application pre−configures the DMIC interface based on the CHAN_SEL pin; when in a stereo configuration, it always outputs a stereo signal with Channel 0 as the left signal, and Channel 1 as the right signal. When in a mono configuration, both the right and left signals will contain the data processed on Channel 0, unless the SWAP_CHAN pin was used to toggle the channels, in which case the DMIC output would see the Channel 1 output on both left and right signals.

When the DMIC interface is not required, the analog outputs can be used for interfacing at line−level or other signal levels, e.g. microphone levels for an external system such as an analog baseband chipset which expects low−level signals.

There are two configurable aspects of the analog output stage – the selection of stereo (two single−ended outputs) or mono (one differential output) and the output attenuation. When a stereo single−ended option is selected, each channel is filtered to generate an analog signal which is then scaled by a configurable output attenuator (OA in Figure 9). In mono differential mode, Channel 1 is replaced by an inverted version of Channel 0 such that the two output pins contain a differential signal for Channel 0. In this latter case, both output attenuators are used, so it is mandatory to ensure that they have the same attenuation settings. The default attenuation value is 0 dB for both channels. This can be configured using I^2C commands.

The 26−ball WLCSP package option doesn’t provide access to A_OUT0. Consequently, only A_OUT1 is available as an analog output. When using this package, careful design consideration must be taken to ensure that the desired signal is available on Channel 1, i.e. on the A_OUT1 pin.

A third output stage option is available on BelaSigna R262; using the Class−D output driver which can drive an output transducer without the need for a separate power amplifier. The output driver can also be configured for single ended stereo or differential mono through the same I^2C commands as described for the analog outputs. The output driver is disabled by the default application in ROM.

For optimal audio performance it is important to note that the VBATRCVR power supply must be connected differently, depending on whether the output driver or the analog outputs are being used:

- When using the analog outputs, VBATRCVR must be connected to VDDA on the application PCB
- When using the output driver, VBATRCVR must be connected to VBAT on the application PCB and must be decoupled with an external capacitor

When interfacing BelaSigna R262 with other processors like codecs or baseband chipsets, it is not recommended to use the Class−D output driver, but rather the analog outputs.

Clock Generation Circuitry

BelaSigna R262 is equipped with a fully configurable and flexible clocking system, which allows for many clocking configurations for various use cases. Computing applications typically require the use of a DMIC interface, which requires the BelaSigna R262 clocking system to provide full synchronization between an incoming DMIC clock and the DMIC data that the chip will produce. The clock frequencies that these systems usually operate with are in the range of 2.048 to 3.072 MHz. Mobile phone applications would typically use much higher clock frequencies; historically, baseband systems have been using 13 MHz or 26 MHz, or even 19.2 MHz or 38.4 MHz.

To support such a wide variety of clocking scenarios, BelaSigna R262 has a phase locked loop (PLL) integrated as one of the components of its clock generation circuitry. Clock frequencies can be selected using the CLOCK_SEL pin, as discussed previously. BelaSigna R262 can also

operate on its internal RC oscillator, offering the same performance, with the slight drawback that the sampling frequency will vary from device to device due to process variation affecting the RC oscillation frequency. When BelaSigna R262 is used with its analog outputs, this has no affect on performance and can be used safely. When synchronization with an external system is required, such as a DMIC codec, it is not possible to use the internal oscillator.

For more information on the configuration of this clocking architecture, refer to the BelaSigna R262 Communications and Configuration Guide.

Power Supply Unit

BelaSigna R262 uses multiple power supplies as can be seen on the simplified representation of the power supply unit in Figure 10.

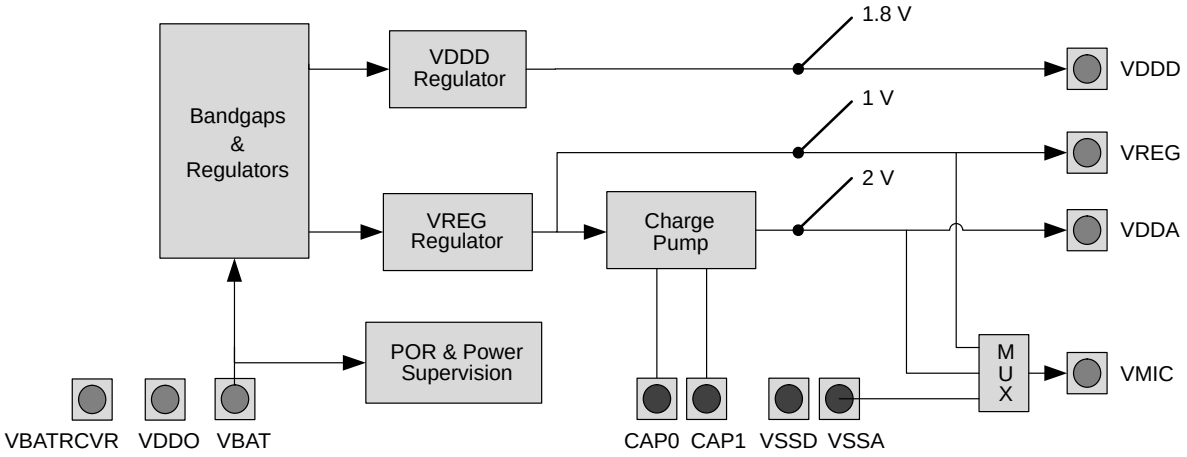


Figure 10. Power Supply Structure

Digital and analog sections of the chip have their own power supplies to allow exceptional audio quality. Several band gap reference circuits and voltage regulators are used to separate the power supplies to the various blocks that compose the BelaSigna R262 architecture.

Table 12 provides a short description of all the power supply pins of BelaSigna R262.

Table 12. POWER SUPPLY VOLTAGES

Voltage	Abbreviation	Description
Battery Supply Voltage	VBAT	The primary voltage supplied to BelaSigna R262 is VBAT. It is typically in the range 1.8 V – 3.3 V. BelaSigna R262 has internal voltage regulators that allow the application PCB to avoid the use of external voltage regulators.
Output Driver Supply Voltage	VBATRCVR	If powered independently and the output driver is to be used, VBATRCVR must be connected to VBAT on the application PCB. Alternatively, if the analog outputs are used, VBATRCVR should be connected to VDDA. A decoupling capacitor is only required when the output driver is being used.
Internal Digital Supply Voltage	VDDD	The internal digital supply voltage is used as the supply voltage for all internal digital components, including being used as the interface voltage at the internal side of the level translation circuitry attached to all of the digital pins. VDDD is provided as an output pad, where a decoupling capacitor to ground must be placed to filter power supply noise.
External I/O Supply Voltage	VDDO	VDDO is an externally provided power source. It is used by BelaSigna R262 as the external side of the level translation circuitry attached to all of the digital pins. Communication with external devices on digital pins will happen at the level defined on this pin.
Regulated Supply Voltage	VREG	VREG is a 1 V reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system. VREG can also be used as a microphone power supply, when the VMIC pin cannot be used.
Analog Supply Voltage	VDDA	VDDA is a 2 V reference voltage generated from the internal charge pump. It is a reference to the analog circuitry. It is available externally to allow for additional noise filtering of the regulated voltages within the system. The internal charge pump uses an external capacitor that is periodically refreshed to maintain the 2 V supply. VDDA can also be used as a microphone power supply, when the VMIC pin cannot be used.
Microphone Bias Voltage	VMIC	VMIC is a configurable microphone bias voltage. VMIC can be configured by the application to provide a 1 V or 2 V power supply to the microphones. It can also be grounded or put to High−Z mode to save power when the microphones don't have to be used. The ROM−based application configures VMIC to provide 2 V to the microphones when they are in use, and High−Z when the system is in Sleep mode.

Power Management Strategy & Battery Monitoring

BelaSigna R262 has a built−in power management unit that guarantees valid system operation under any voltage supply condition to prevent any unexpected audio output as the result of any supply irregularity. The unit constantly monitors the power supply and shuts down all functional units (including all units in the audio path) when the power supply voltage goes below a level at which point valid operation can no longer be guaranteed.

The power management unit on BelaSigna R262 includes power−on−reset (POR) functionality as well as power supervisory circuitry, as shown in Figure 10. These two components work together to ensure proper device operation under all supply conditions.

The POR sequence is designed to ensure proper system behavior during start−up and proper system configuration after start−up. At the start of the POR sequence, the audio output is disabled and all configuration and control registers are asynchronously reset to their default values.

The power supervisory circuitry monitors the supply voltage (VBAT). This circuit is used to start the system when VBAT reaches a safe startup voltage, and to reset the system when it drops below a relevant voltage threshold. The relevant parameters are shown in Table 13.

Table 13. POWER MANAGEMENT PARAMETERS

Parameters	Voltage Level
VBAT startup	1.65 V ± 80 mV
VBAT shutdown	1.6 V ± 50 mV

The POR sequence consists of two phases: voltage supply stabilization and boot ROM initialization. During the voltage supply stabilization phase, the following steps are performed:

1. The internal regulators are enabled and allowed to stabilize
2. The internal charge pump is enabled and allowed to stabilize
3. SYSCLK is connected to all of the system components (free−running PLL output)
4. The system runs the ROM application

At step 1, once the supply voltage rises above the startup voltage and remains there for more than 5 ms, a signal will enable the charge pump.

At step 2, another 5 ms delay is implemented to allow the charge pump to stabilize before toggling the POR signal, and thus enabling the digital core.

If the supply is consistent, the internal system voltage will then remain at a fixed nominal voltage. If a spike occurs that causes the voltage to drop below the shutdown internal system voltage, the system will shut down. If the voltage rises again above the startup voltage and remains there for the required time, a POR sequence will occur again.

Once the ROM application is running, more system monitoring is performed by the application; typically, the software will permanently monitor the presence of an external clock, and take the appropriate actions whenever it disappears. See the system monitoring section for more information.

Digital Communication Interfaces

Debug Port (UART)

BelaSigna R262 has an RS232−based UART that can be used to interface the chip from ON Semiconductor's communication tools. The debug port cannot be used for customer applications. BelaSigna R262 can only be configured using the I^2C interface. See the I^2C interface section for information on how communication tools can interface with BelaSigna R262.

General−Purpose Input Output (GPIO)

BelaSigna R262 has five GPIO pins which are all used with specific functionalities. The five signals are SPI_CLK/ CLOCK_SEL, SPI_CS/BOOT_SEL, SPI_SERO/ CHAN_SEL, SPI_SERI/ALPHA_SEL and SWAP_CHAN.

SWAP_CHAN is used as a GPIO, consequently, it has an internal pull − up resistor. When used as LSADs (CLOCK_SEL, BOOT_SEL, CHAN_SEL and ALPHA_SEL), the pull − ups are disabled. If left floating in LSAD mode, the pins have a weak pull − down to ground.

See the Booting Control, Output and Channel Control and Algorithm Control sections earlier in this document for details on the behavior of these GPIO and LSAD pins.

Serial Peripheral Interface (SPI) Port

An SPI port is available on BelaSigna R262 for applications such as communication with non−volatile memory (EEPROM). The I/O levels on this port are defined by the voltage on the VDDO pin. The SPI port operates in master mode only, which supports communications with slave SPI devices. The four signals needed by the SPI port are multiplexed with other functions on BelaSigna R262 (GPIOs, LSADs). The use of the SPI port requires careful design consideration with regards to the use of these other functions.

I^2C Interface

The I^2C interface is an industry − standard interface that can be used for high − speed transmission of data between BelaSigna R262 and an external device. The interface operates at speeds up to 400 kbit/sec. In product development mode, the I^2C interface is used for application debugging purposes, communicating with the BelaSigna R262 development tools, also known as SignaKlara Development Utility (SKDU). The interface always operates in slave mode and the slave address is 0x61.

A comprehensive command interface can be used with the SKDU and other tools provided by ON Semiconductor. It will offer a variety of support functions grouped in different categories like general system control (system reset, status information), application control (switching between operating modes, enabling or disabling the algorithm),

hardware setup (for custom configuration of the various hardware units like clocking, input/output stages), algorithm setup (amplitude management, tuning selection) and finally the low − level I^2C protocol is also supported.

The I^2C interface can also be used to communicate with a slave I^2C EEPROM. Using an I^2C EEPROM instead of an SPI EEPROM provides better flexibility as it avoids potential conflicts between GPIO/LSAD pins and the SPI pins. More details on this command interface can be found in the BelaSigna R262 Communications and Configuration Guide.

Interfaces Unused by the ROM−based Application

BelaSigna R262 also contains hardware provisions for a high speed PCM interface, as well as a high speed UART. These two interfaces are not used by the ROM−based application, hence cannot be used by default. Custom applications developed by ON Semiconductor could enable the use of these interfaces, should this be required.

Miscellaneous

Chip Identification

Chip identification information can be retrieved by using the Promira Serial Interface or Communications Accelerator Adaptor (CAA) along with protocol software provided by ON Semiconductor. For BelaSigna R262, the key identifier components and values are as follows:

Chip Family	Chip Version
0x02 (SK2)	0x3021

Long Term Storage Conditions

ON Semiconductor specifies a 24−month maximum storage time for WLCSP devices in pocket tapes and conditioned in dry bags, as stated in Table 14 below and defined by ON Semiconductor's guidelines on long term storage.

Table 14. LONG TERM STORAGE CONDITIONS

Storage Condition	Maximum Storage Time	Remarks
Temperature 18−28°C, Humidity 30−65%RH	24 months after die singulation/sawing date	Maximum 12 months storage at condition 18−28°C, 30−65%RH. Afterwards storage in vacuum moisture bag with desiccant and humidity card. Storage in nitrogen cabinet allowed.

Device Weight

BelaSigna R262 has an average weight of 10.84 mg.

Re−Flow Information

BelaSigna R262 is a Green, Pb−Free device. Download SOLDERRM/D − Soldering and Mounting Techniques Reference Guide.

Assembly / Design Notes

For PCB manufacture BelaSigna R262, any vias that might be placed below the WLCSP should all be covered in soldermask. The assembly process can use underfill under the WLCSP; it will provide another physical dielectric barrier, and will also enhance long term reliability over temperature and physical shock.

ON Semiconductor can provide BelaSigna R262 mounting footprint guidelines to assist your PCB design upon request. For additional information on the use of Chip Scale Packages and for advanced guidelines on mounting such devices to a PCB, please download AND8081/D − Flip−Chip CSP Packages from www.onsemi.com.

Table 15. ORDERING INFORMATION

Device	Marking	Package	Shipping †
BR262W26A103E1G	BR262W26	WLCSP26 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

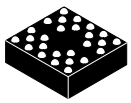
BELASIGNA is a registered trademark of Semiconductor Components Industries, LLC.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

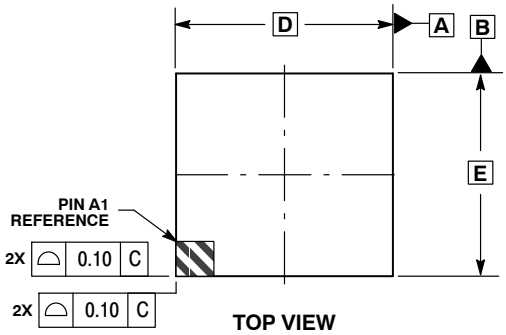
ON Semiconductor®

WLCSP26, 2.388x2.233
CASE 567CY−01
ISSUE A

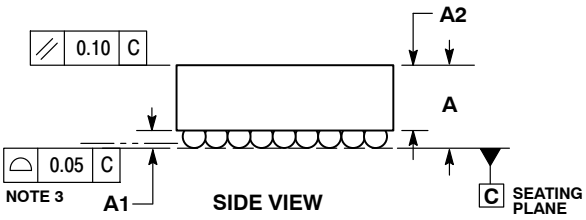
DATE 27 MAY 2011



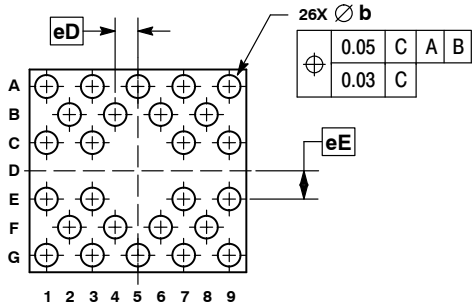
SCALE 4:1



TOP VIEW



SIDE VIEW

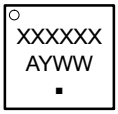


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.84	1.00
A1	0.17	0.23
A2	0.72 REF	
b	0.24	0.29
D	2.388 BSC	
E	2.233 BSC	
eD	0.252 BSC	
eE	0.310 BSC	

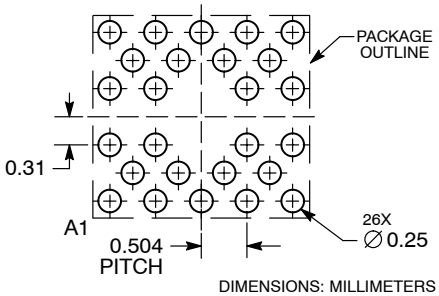
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**WLCSP26, 2.388X2.233**		**PAGE 1 OF 1**

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