CAT871, CAT872

Dual Input Reset Generator

Description

CAT871, CAT872 are dual input reset generators designed to restart microprocessor and microcontroller based systems when the watchdog timer or other resetting mechanisms have become disabled or failed.

CAT871, CAT872 monitor two inputs and output an active low reset pulse after both inputs have been active (logic low) for a factory preset minimum time. The reset pulse width is 2.2 ms for CAT871 and 70 ms for CAT872. Releasing either input from its active state before the minimum timeout period resets the internal timer and both inputs must return to being active before the timer will restart with a fresh count down.

CAT871, CAT872's open drain output is capable of sinking up to 3 mA of current and may be wire−OR'd with other open drain devices to drive a common reset input.

Features

- Operate on 1.65 V to 5.5 V Power Supplies
- Ultra Low Quiescent Current: 10 nA (typical)
- Schmitt Trigger Inputs
- 8 Factory Preset Delay Times from 0.5 s to 5 s to Choose From
- Small µLLGA−6 Package: 1.45 x 1.0 x 0.4 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones
- PDAs
- MP3 Players
- Personal Navigation Devices

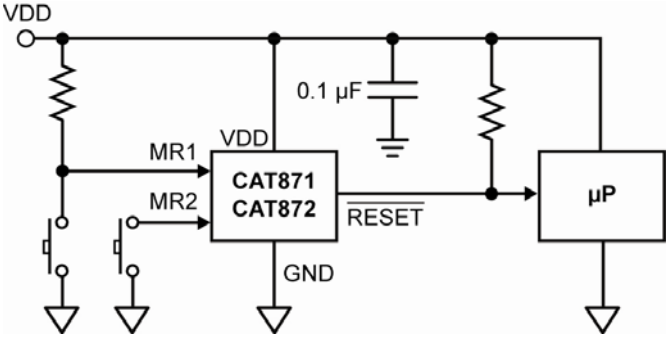
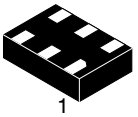


Figure 1. Application Schematic

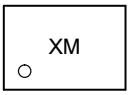
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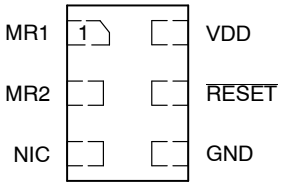
ULLGA−6
UL SUFFIX
CASE 613AF

MARKING DIAGRAM



X = Specific Device Code
(J = CAT871, K = CAT872)
M = Date Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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FUNCTIONAL BLOCK DIAGRAM

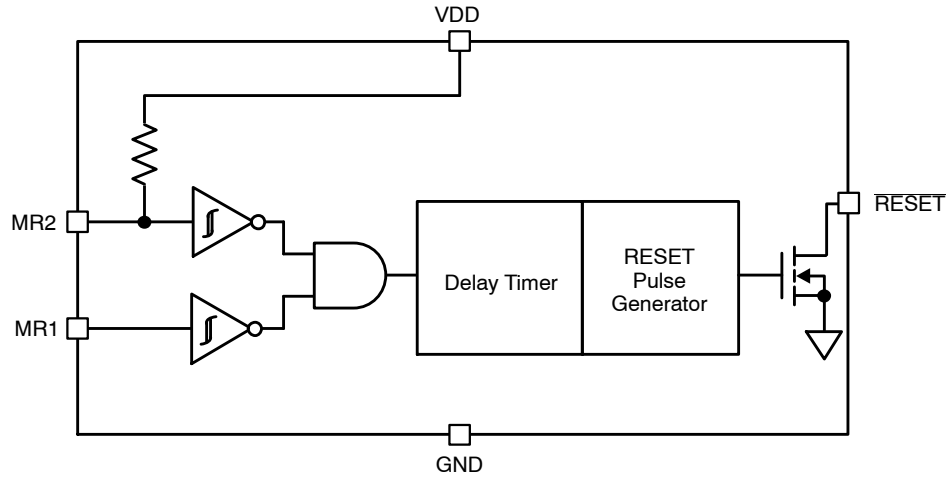


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	MR1	Manual reset input #1. CMOS input.
2	MR2	Manual reset input #2. CMOS input.
3	NIC	No Internal Connection. A voltage or signal applied to this pin will have no effect on device operation.
4	GND	System Ground.
5	$\overline{\text{RESET}}$	Reset Output. Active−low open drain output.
6	VDD	Positive Power Supply.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{DD}	−0.3 to 6	V
Output Voltage Range	V_{OUT}	−0.3 to 6 or (V_{DD} + 0.3), whichever is lower	V
Input Voltage; MR2, MR1	V_{IN}	−0.3 to 6 or (V_{DD} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Output Current; $\overline{\text{RESET}}$	I_{OUT}	10	mA
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage; VDD	V_{DD}	1.65	5.5	V
Input Voltage; MR1, MR2	V_{IN}	0	V_{DD}	V
Output Current; $\overline{\text{RESET}}$	I_{OUT}	0	3	mA
Ambient Temperature	T_A	−40	85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS
(V_{DD} = 1.65 V to 5.5 V. For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POWER						
V_{DD} Supply Voltage		V_{DD}	1.65		5.5	V
Quiescent Supply Current	MR1 = MR2 = V_{DD}.	I_{DD}		10	1000	nA
Operating Supply Current	MR1 = MR2 = 0 V Measured during setup period. Measurement includes current through internal 200 kΩ pull−up resistor on MR2				50	μA
LOGIC INPUTS AND OUTPUTS						
Input Voltage; HIGH	MR1, MR2	V_{IH}	0.7 x V_{DD}			V
Input Voltage; LOW	MR1, MR2	V_{IL}			0.25xV_{DD}	V
Hysteresis		V_{HYS}	−	250		mV
Input Current	MR1 = 0 V; V_{DD} = 5 V (no internal pull−up)	I_{PU}		50	300	nA
Input Current	MR2 = 0 V; V_{DD} = 5 V (internal 200 kΩ pull−up resistor)	I_{PU}		25		μA
Output Voltage; HIGH	External 10 kΩ pull−up resistor to V_{DD}	V_{OH}	V_{DD} − 0.1			V
Output Voltage; LOW	I_{SINK} = 3 mA, V_{DD} = 1.8 V	V_{OL}		0.1	0.4	V
TIMING						
Timeout	CAT87x−05	t_{LOW_DELAY}	0.41	0.50	0.59	s
	CAT87x−10		0.82	1.00	1.18	s
	CAT87x−15		1.23	1.50	1.77	s
	CAT87x−20		1.64	2.00	2.36	s
	CAT87x−25		2.05	2.50	2.95	s
	CAT87x−30		2.46	3.00	3.54	s
	CAT87x−40		3.28	4.00	4.72	s
	CAT87x−50		4.1	5.00	5.9	s
Reset Output Pulse Width	CAT871	t_R	1.8	2.2	2.6	ms
	CAT872		57	70	83	
TEST MODE (at T_A = 25°C) (Note 3)						
Start TEST window		t_{ST}			35	μs
Test Mode delay	MR1=0 V, MR2→8 cycles, delay measured after 8th rising edge of the MR2 clock pulse	t_D		250		μs
Test Mode Clock Frequency	Clock applied to MR2	f_{tm}		1		MHz
MR2 Test mode clock setup time	Measured from MR1 falling edge to first falling edge of MR2	t_P	1			μs
MR2 Input Voltage; LOW	MR2, Test mode operation	V_{IL_TM}			0.2xV_{DD}	V
MR2 Pulse Width		t_{pw}		500		ns

3. “Test Mode” parameters are not tested in production.

TIMING WAVEFORMS (Note 4)

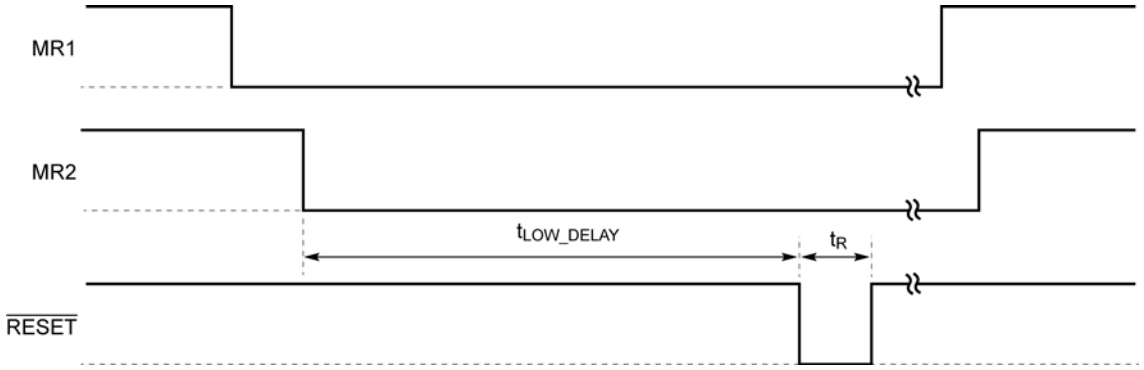


Figure 3. Timing Waveforms

4. The order of the MR inputs going low does not matter. The last input to go low marks the beginning of t_{LOW_DELAY}

TYPICAL CHARACTERISTICS

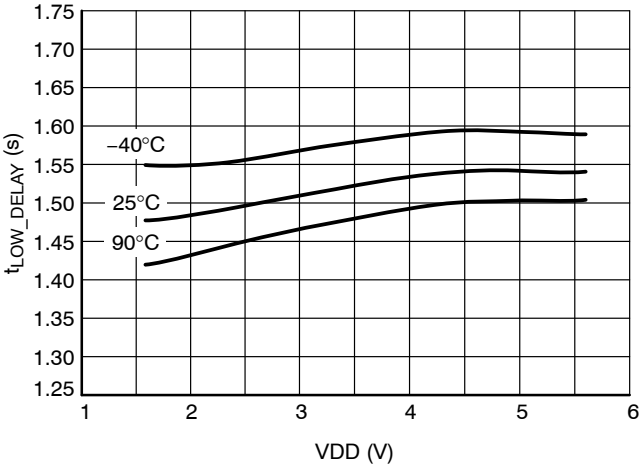


Figure 4. t_{LOW_DELAY} vs. VDD (CAT87x−1.5)

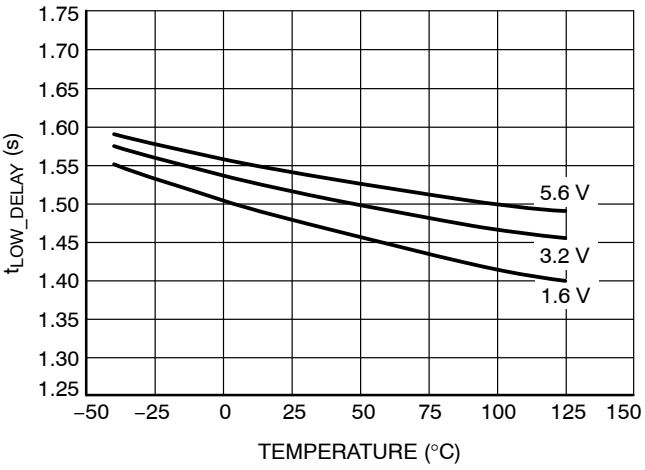


Figure 5. t_{LOW_DELAY} vs. Temperature (CAT87x−1.5)

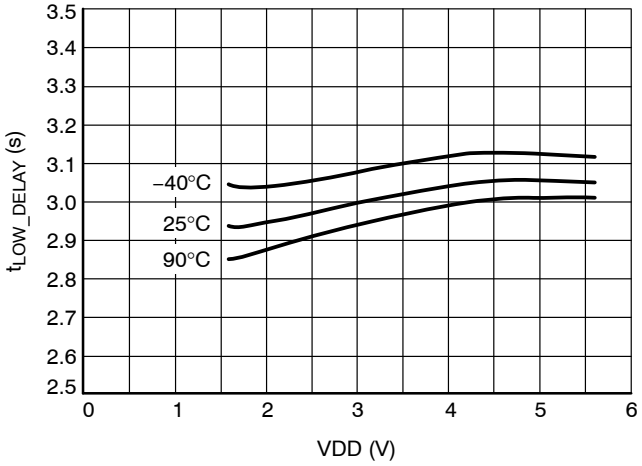


Figure 6. t_{LOW_DELAY} vs. VDD (CAT87x−3.0)

TYPICAL CHARACTERISTICS

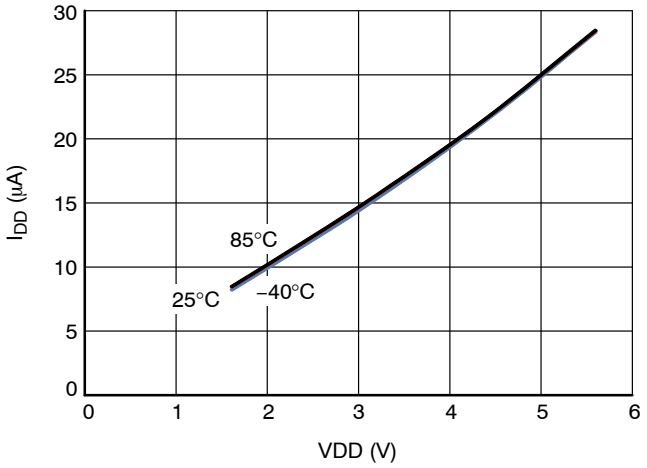


Figure 7. I_{DD} vs. VDD (MR1 = MR2 = 0)

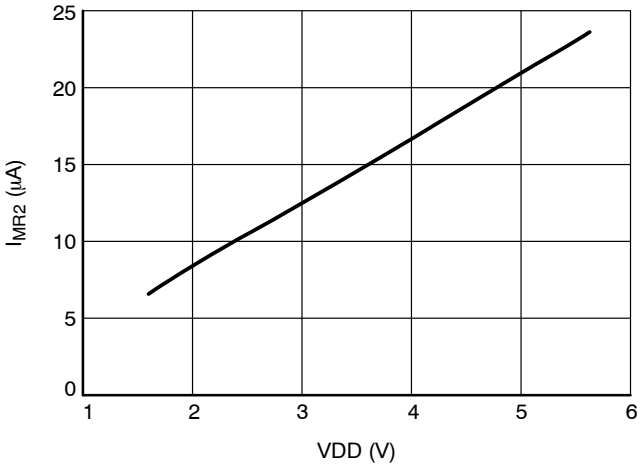


Figure 8. I_{MR2} @ MR2 = 0

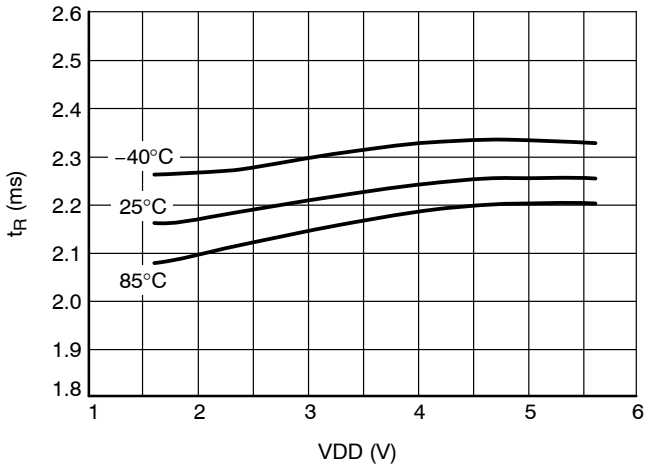


Figure 9. t_R vs. VDD for CAT871

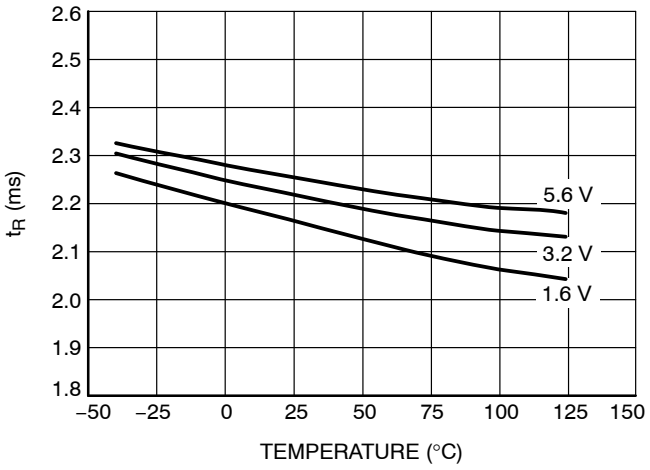


Figure 10. t_R vs. Temperature for CAT871

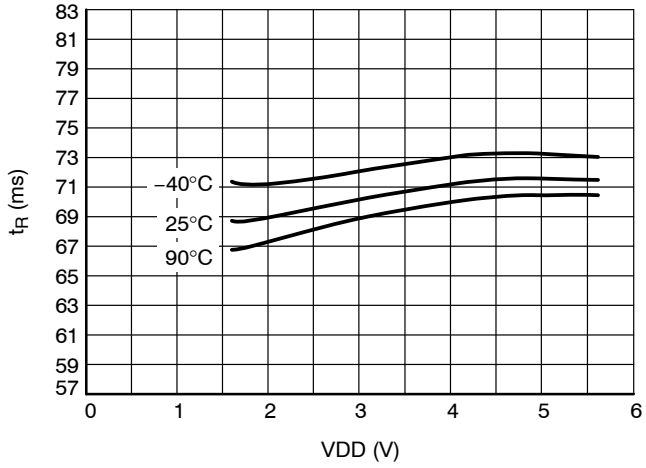


Figure 11. Reset Pulse Width for CAT872

SYSTEM DESCRIPTION AND APPLICATIONS INFORMATION

General

CAT871, CAT872 are designed for the manual resetting of microprocessors and microcontrollers when normal resetting mechanisms have failed. To prevent accidental resets, CAT871, CAT872 require both manual reset inputs be held low for a prescribed period before a reset pulse is issued to the system processor.

Manual Reset Inputs

MR1 and MR2 are Schmitt trigger CMOS inputs. Both inputs must go low and stay low for a predetermined period (t_{LOW_DELAY}) to generate a single reset pulse on the output. MR1 and MR2 operate independently and may be brought low at any time and in any order. The last input to reach 0 V starts the delay timer.

MR1 is a standard CMOS input and MR2 is also a CMOS input with an internal 200 kΩ pull−up resistor, thus MR2 can be left floating whereas MR1 must be biased by a pull−up resistor, powered switch or some other means external to the IC. (Consult factory for other input biasing options)

Delay Timer

When both MR1 and MR2 go low, an internal timing cycle is initiated. If any input goes high before the countdown timer has concluded its cycle, the timer will reset and will restart from the beginning when MR1 and MR2 return to being low.

If both manual reset inputs (MR1 and MR2) remain low after a reset pulse is issued, no second reset pulse will be issued after that.

Reset Output

CAT871, CAT872 provide an active−low open drain output to be wire−OR'd with other open drain reset devices. This output will sink up to 3 mA and as such will not be loaded down by low value (strong) pull−up resistors. The reset pulse is typically 2 ms long for CAT871 and 70 ms long for CAT872 and is issued at the conclusion of the delay timer's countdown sequence.

CAT871, CAT872 will not generate a reset pulse at power−up.

Delay Timer Testing

To aid in−circuit testing of the delay timer, a special test function has been included in CAT871, CAT872. This test mode, TOC, allows the delay timer to clock at an accelerated rate. Upon the conclusion of the countdown a standard width reset pulse will be issued and the chip will exit test mode.

To initiate TOC, MR1→ 0 V and a fast external CLK (typically 1 MHz) is applied on MR2, with the falling edge of the first clock pulse on MR2 delayed with tP from MR1→ 0 V. CAT871, CAT872 look for 8 sequential pulses to appear on MR2 within 35 μs to confirm TOC is desired. After the rising edge of the 8'th pulse, there will be a delay of 250 μs typical followed by a standard reset pulse at the reset output. This delay is independent of the normal timeout delay setting.

After issuing the reset pulse, CAT871, CAT872 exit TOC mode and returns to normal operation. If at any time during TOC both MR1 and MR2 are HIGH, CAT871, CAT872 will immediately exit TOC mode.

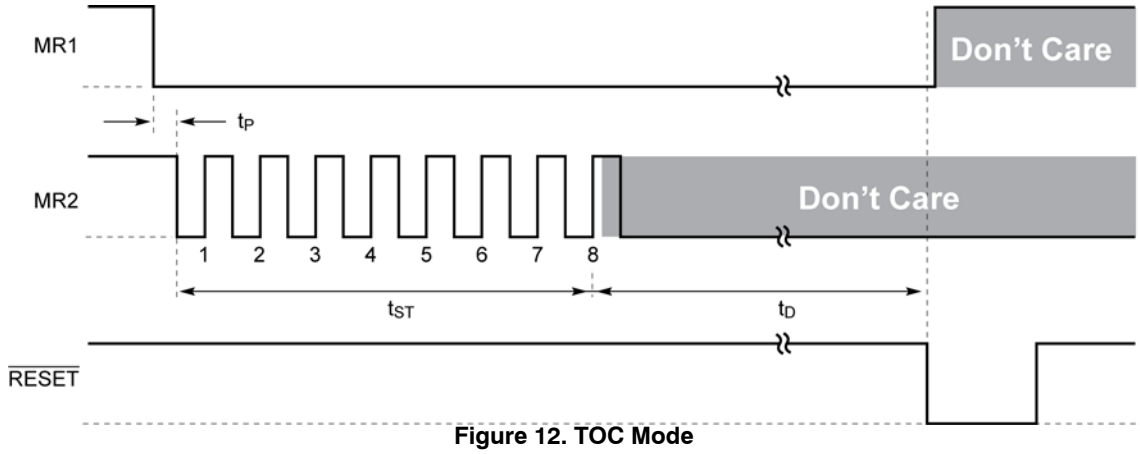


Figure 12. TOC Mode

APPLICATION INFORMATION

Reset Pulse Operation

When both MR1 and MR2 inputs are kept low, a single reset pulse is generated after the delay t_{LOW_DELAY}. Even with both MR1 and MR2 maintained low continuously after that time, no second reset pulse will be generated. The delay timer restarts if either MR1 or MR2 (or both) input transitions from high to low, as shown in the timing diagram in Figure 13.

System with Two Different Power Supply Voltages

The reset generator can be used in a system where the supply VDD is different than the MR1, MR2 input logic. Figure 14 shows an application schematic where the microcontroller uses a supply VBAT (3.6 V) that is higher than the VDD rail (1.8 V). MR1 and MR2 inputs are activated here by two separate switches connected to GND and pulling the inputs low when pressed. The Schottky diode provides the supply isolation needed between the CAT871/CAT872 (VDD) and the microcontroller (VBAT).

Operation with Low VDD Voltage and Brownout Condition

The CAT871, CAT872 reset generators require a minimum supply voltage VDD of 1.65 V to guarantee the normal operation within the specification. To prevent small VDD supply glitch, a small ceramic capacitor can be added between the VDD pin and GND.

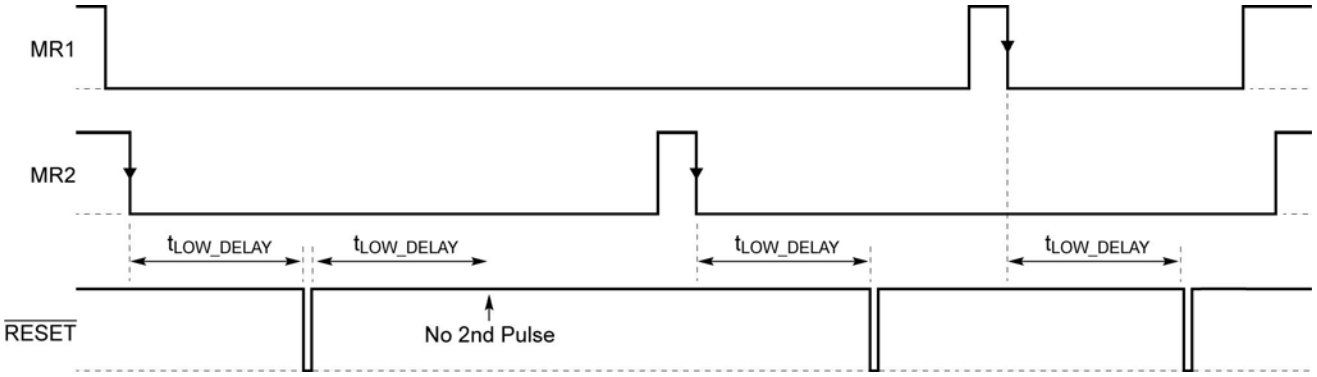


Figure 13. Reset Timing Diagram

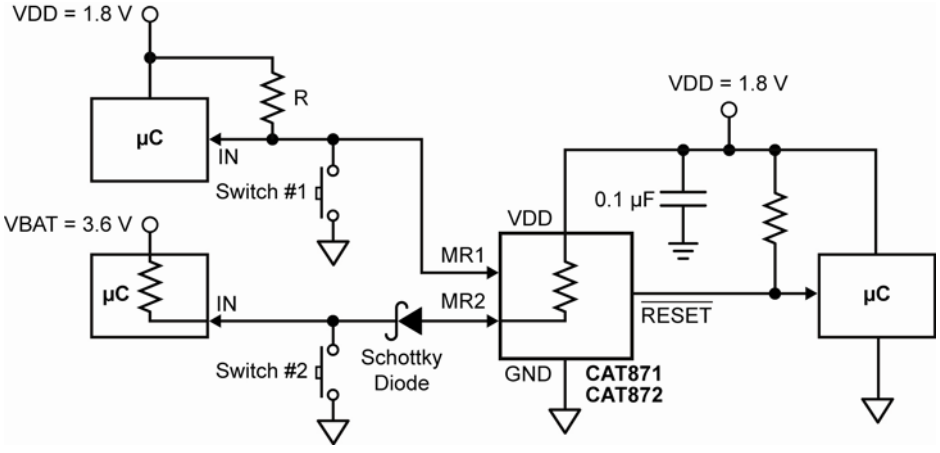
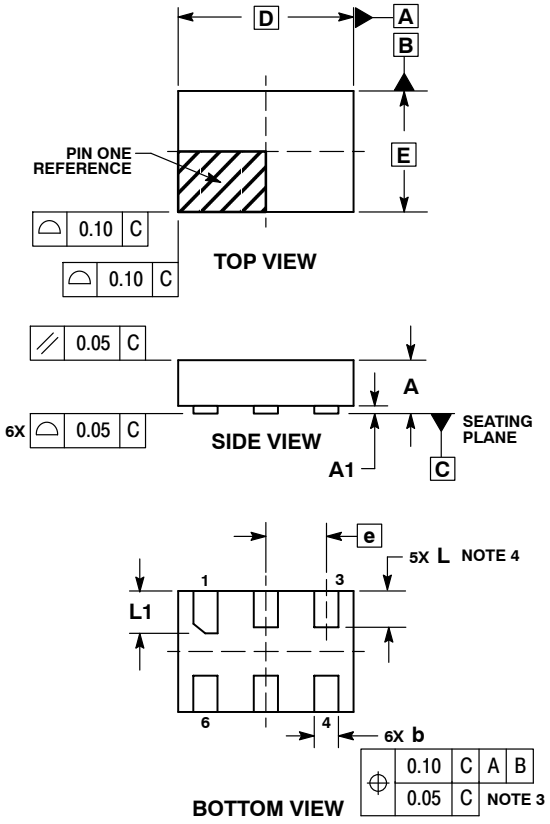


Figure 14. Application Schematic in Dual Supply System

PACKAGE DIMENSIONS

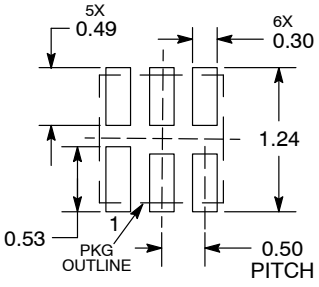
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CASE 613AF−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*

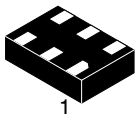


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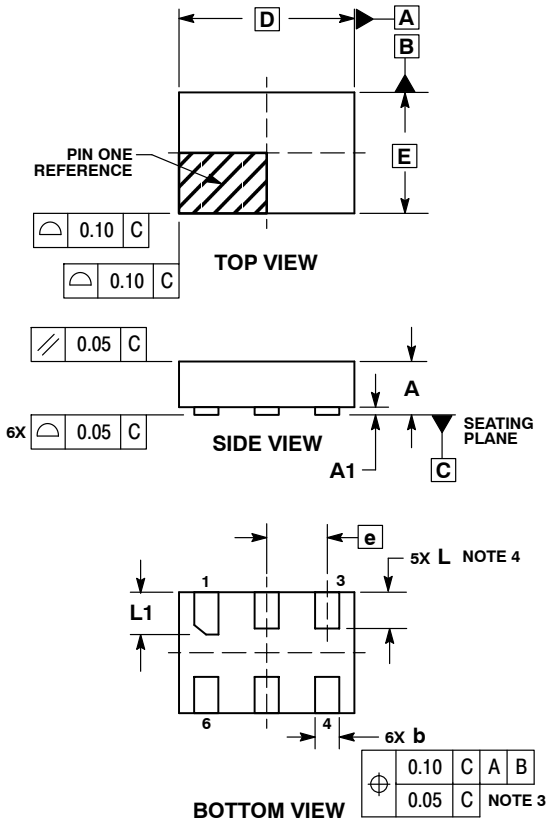
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ISSUE A

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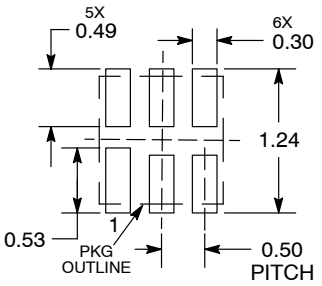
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	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

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