CPS-1848™ User Manual

Central Packet Switch

Formal Status
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About this Document

This document includes hardware and software information for the IDT CPS-1848 Central Packet Switch. The CPS-1848 is a high-performance Serial RapidIO 2.1-compliant switch that supports up to 18 1x ports.

Content Summary

- Device Overview provides an overview the CPS-1848's capabilities.
- RapidIO Ports explains the operation of the device's S-RIO ports.
- RapidIO Lanes discusses lane to port mapping, Loopback, and PRBS functions.
- Switch Fabric describes the switch core behavior and flow control processes.
- Performance discusses the packet switching performance characteristics of the CPS-1848.
- Event Management explains the CPS-1848's Error Management block. This block detects, filters, logs, counts, and reports error events from all of the device's functional blocks.
- I2C Interface describes the standard I2C bus interface used in the CPS-1848.
- JTAG and Boundary Scan describes the CPS-1848 JTAG Interface.
- Reset and Initialization provides reset and initialization steps.
- Registers provides the full memory map and complete description of the CPS-1848's registers.
- References provides a list of specifications referred to in this manual.

Additional Resources

In addition to this user manual, which explains the functionality of the CPS-1848 and how to use the device, and the device's datasheet which covers all electrical specifications, there are many additional resources available. For more information, contact IDT technical support at srio@idt.com.

Document Conventions and Definitions

This manual uses the following conventions and terms:

- To indicate signal states:
  - Differential signals use the suffix "_P" to indicate the positive half of a differential pair.
  - Differential signals use the suffix "_N" to indicate the negative half of a differential pair.
  - Non-differential signals use the suffix "_N" to indicate an active-low state.
- To define buses, the most significant bit (MSB) is on the left and least significant bit (LSB) is on the right. No leading zeros are included.
- To represent numerical values, either decimal, binary, or hexadecimal formats are used. The binary format is as follows: 0bDDD, where "D" represents either 0 or 1; the hexadecimal format is as follows: 0xDD, where "D" represents the hexadecimal digit(s); otherwise, it is decimal.
- Unless otherwise denoted, a byte is an 8-bit quantity; a word is a 32-bit quantity, and a double-word is an 8-byte (64-bit) quantity. This is in accordance with RapidIO convention.

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- A bit is set when its value is 0b1. A bit is cleared when its value is 0b0.
- This device follows big-endian convention (see figure). The ordering of bytes within words is called either “big endian” or “little endian”. Big-endian systems label byte zero as the most significant (left-most) byte of a word. Little-endian systems label byte zero as the least significant (right-most) byte of a word.

Big Endian	Bit 0 MS Bit Bit 7 LS Bit Most Signficant Byte Address offset: 0	Bit 8 MS Bit Bit 15 LS Bit Address Offset: 1	Bit 16 MS Bit Bit 23 LS Bit Address offset: 2	Bit 24 MS Bit Bit 31 LS Bit Least Signficant Byte Address offset: 3

Little Endian	Bit 31 MS Bit Bit 24 LS Bit Most Signficant Byte Address Offset: 3	Bit 23 MS Bit Bit 16 LS Bit Address Offset: 2	Bit 15 MS Bit Bit 8 LS Bit Address Offset: 1	Bit 7 MS Bit Bit 0 LS Bit Least Signficant Byte Address Offset: 0

- A read-only register, bit, or field can be read but not modified.
- A sticky bit remains set after it is set by hardware until a zero is written to it. Writing a one to a sticky has no effect on its value.



This symbol indicates important configuration information or suggestions.



This symbol indicates procedures or operating levels that may result in misuse or damage to the device.

Device Revision Information

This document supports all device revisions of the CPS-1848. Features that are applicable to a specific revision of the device are highlighted throughout the document (for more information, see Device Information CAR).

Revision History

June 2, 2014, Formal Manual

- Added an overview section to Packet Transfer Validation and Debug
- Added a note to PRBS Pattern Checker and Log (Revision C) (see the first note in the section)
- Updated the maintenance error information in Table 35, Table 44, Table 52, and Table 60 to align with the Logical/Transport Layer Control Capture CSR
- Updated the first three bullets in Error Log Event Notification Programming Model to indicate that ERR_XXX_MASK should be set to 0 to complete a comparison
- Changed the bit encoding of “4x to 1x lane 2” for Downgrade to 0b010 from 0b011 (see Table 36)
- Updated the description of Logical/Transport Layer Error Detect CSR[ILL_TRAN and UNSUP_TRAN]
- Changed bit 23 to reserved in Port {0..17} Operations Register and Broadcast Port Operations Register
- Updated the description of “Maintenance Packet Received that was Too Small or Too Large” and “Maintenance Transaction Field Error” in the table below Logical/Transport Layer Control Capture CSR

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October 24, 2013, Formal Manual

- Updated steps 2 and 5 in Table 13
- Updated the caution in VoQ Fairness/Starvation Avoidance
- Updated Input Scheduler
- Updated the second paragraph after Table 34
- Updated Figure 19
- Updated Logical and Transport Layer Events, including the addition of a note
- Updated Table 37, Table 53, Table 59, Table 60, Table 61
- Added a note to Physical Layer Events Notification
- Updated Table 67
- Added a note to Error Log Event Notification Programming Model
- Updated the description of Clearing and Handling Port Fail and Port Degraded Events
- Completed other minor improvements throughout the document

July 11, 2013, Formal Manual

- Updated the Register Values in Table 57 to indicate the correct reset values for the Error Log Match Register
- Updated the last example in Multicast Programming Examples – Direct Programming Model
- Completed other minor improvements throughout the document

February 7, 2013, Formal Manual

- Updated Maintenance Packet Routing
- Updated the caution in Generating a Reset Request
- Added a caution to Hot Extraction/Insertion
- Updated Switch Is Not Routing Packets Correctly
- Updated EEPROM Format Example
- Completed other minor improvements throughout the document

August 10, 2012, Formal Manual

- Changed the procedural order for checking a received PRBS sequence without 8b/10b encoding in PRBS Pattern Checker and Log (Revision C)
- Updated the second paragraph in Alert on Trace Match
- Changed the “error rate threshold” event in Table 37 to indicate “No Information is Captured”
- Updated Event Isolation, Table 8, and Table 9 with additional information about when a port detects an OUTPUT_FAIL condition
- Added a note to OUTPUT_PORT_EN in Port {0..17} Control 1 CSR
- Updated the introduction to Logical/Transport Layer Error Enable CSR
- Updated the description of STOP_EM in Error Log Control 2 Register
- Added a note to PRBS_MODE in Lane {0..47} Control Register

May 7, 2012, Formal Manual

- Updated Step 4 in Table 8 (Preparation For Hot Extraction on Port Y)
- Added a section on Packet Transfer Validation and Debug

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- Added a footnote to Table 7 (disabling IDLE2 operation)
- Updated User-Defined Patterns
- Added a section on 10-bit Loopback Mode Restrictions
- Added a note to Maintenance Packets with Enabled Trace Ports
- Added overview sections on error management in Event Management Overview
- Added a section on Packet Acknowledge Latency
- Updated Packet Throughput Performance
- Added a section on I2C Master Mode Validation Debug
- Added a section on Computing Timeout Values
- Updated the description of the [1:1] bit setting in Table 58
- Updated the procedure for Clearing and Handling Port Fail and Port Degraded Events
- Updated Inter-Command Delay and Table 74
- Updated the description of Port {0..17} VC0 Packets Received Counter Register.COUNT
- Added cautionary notes to the following error management registers: Logical/Transport Layer Error Enable CSR, Logical/Transport Layer Error Report Enable Register, Port {0..17} Error Report Enable Register, Port {0..17} Implementation Specific Error Rate Enable Register, and Lane {0..47} Error Report Enable Register
- Updated Note A associated with Port {0..17} Error and Status CSR.PORT_ERR
- Updated the description of AMP_PROG_EN and NEG1_CMD in Lane {0..47} Status 3 CSR
- Updated the description of Lane {0..47} Status 3 CSR.AMP_PROG_EN
- Updated the description of TX_SYMBOL_CTL and LANE_DIS in the Lane {0..47} Control Register and Broadcast Lane Control Register
- Changed the definition of the [20:31] fields to reserved in Lane {0..47} DFE 1 Register and Broadcast Lane DFE 1 Register
- Changed the definition of the [19:21] and [25:26] fields in the following registers to reserved: Lane {0..47} Error Report Enable Register, Lane {0..47} Error Rate Enable Register, Broadcast Lane Error Report Enable Register, and Broadcast Lane Error Rate Enable Register. These updates also impacted the following tables: Table 39, Table 47, and Table 62.
- Changed the definition of the [19:20] and [25] fields in the following registers to reserved: Lane {0..47} Error Detect Register and Broadcast Lane Error Detect Register. These updates also impacted the following tables: Table 39, Table 47, and Table 62.
- Added a note to OUTPUT_CREDIT_RSVN in the Switch Parameters 1 Register, and additional information to Switch Parameters 2 Register
- Updated the description of SELF_MCAST_EN in Port {0..17} Operations Register and Broadcast Port Operations Register

February 16, 2012, Formal Manual. Updated the document to support Revision C silicon and completed numerous improvements. Key changes include:

- Updated procedure in PRBS Pattern Checker and Log (Revision C). Also changed description to indicate that PRBS Pattern Checker applies only to Revision C.
- Updated Table 41, Table 49, and Table 64 to indicate that a “JTAG incomplete write” error applies only to Revision A/B
- Added a note to Configuration Register Access (Revision A/B) regarding the system reset sequence
- Added a note to Buffer Management Settings regarding the input buffer
- Added a new JTAG section that discusses Revision C functionality, Configuration Register Access (Revision C)
- Updated MINOR_REV and JTAG_REV in Device Information CAR
- Updated MAX_DESTID and MCAST_MASK in Switch Multicast Information CAR

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- Updated JTAG_ERR_EN in Aux Port Error Capture Enable Register
- Updated JTAG_ERR in Aux Port Error Detect Register
- Updated JTAG_LOG_EN in Aux Port Error Report Enable Register
- Updated JTAG Control Register (Revision A/B) to indicate it applies only to Revision A/B
- Added CC_MONITOR_STATUS, CC_MONITOR_EN, and CC_MONITOR_THRESH to Lane {0..47} Status 4 CSR
- Changed the 0b0010 setting of PRBS_MODE to in Lane {0..47} Control Register
- Added PRBS_RX_CHECKER_MODE to Lane {0..47} Control Register
- Added a note to Maintenance Dropped Packet Counter Register
- Changed the reset value of Port {0..17} Control 1 CSR[OUTPUT_PORT_EN] to 0b1
- Changed the reset value of Port {0..17} Lane Synchronization Register[VMIN] to 0b001, and updated the definition of VMIN
- Added Figure 18 to support Indy Revision C event management
- Added a note in Output Scheduler
- Added a note to Time to Live Events
- Added two notes to Port {0..17} Lane Synchronization Register
- Added a fourth register access to step 2 in Table 11
- Added Table 57 to indicate where events are enabled in various registers
- Added a new section on JTAG Clock Constraints
- Updated step 7 in I2C EEPROM Format
- Updated Received Retry Count Trigger Congestion Isolation
- Updated Link Initialization and Register Initialization
- Updated Port Reconfiguration Operations and Disabling IDLE2 Operation
- Updated Table 8 and Table 9 (Hot extraction)
- Updated the first note in Per-Port Reset
- Added a caution to 10-bit Loopback Mode and 8-bit Loopback Mode
- Removed the first (disable ports) and last rows (enable ports) from the tables in Lane Speed Change Examples
- Added a new paragraph (the last one) to Port and Lane Initialization Sequence
- Added a second caution to Alert on Trace Match
- Updated hot insertion/extraction procedure in Table 11 and Table 12
- Updated IMP_SPEC_ERR in Logical/Transport Layer Error Detect CSR and Logical/Transport Layer Error Enable CSR
- Updated IMP_SPEC in Logical/Transport Layer Control Capture CSR
- Added a note to Port {0..17} Link Maintenance Request CSR[CMD]
- Added a caution to Port {0..17} Local ackID CSR
- Updated COUNT in Port {0..17} VC0 Packets Received Counter Register
- Added a note to Port {0..17} VC0 Retry Symbols Transmitted Counter Register
- Added a note to Port {0..17} Link Maintenance Request CSR
- Added a caution to the beginning of Lane Speed Change Examples
- Updated Port {0..17} Error and Status CSR[PORT_UNAVL]
- Added a note to COUNT in each Counter register in Port Function Registers
- Added a note to Port {0..17} Error and Status CSR[OUTPUT_DROP]

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- Added a note to Device Reset and Control Register[RESET_TYPE]
- Updated Port {0..17} Control 2 CSR[SCRAM_DIS]
- Added a note to Lane {0..47} PRBS Generator Seed Register[PRBS_SEED]
- Added a note to Lane {0..47} Control Register[LANE_DIS]
- Added a note to Multicast Association Operations CSR[CMD]
- Added a note to Port {0..17} Operations Register[TX_FLOW_CTL_DIS]
- Added a note to Lane {0..47} Control Register[TX_RATE and RX_RATE]
- Updated bit 17 in Port {0..17} Error Detect CSR

November 1, 2011, Preliminary Manual

- Updated hot insertion/extraction procedure in Table 8, Table 10, and Table 12
- Updated JTAG_REV in the Device Information CAR to indicate multiple revision identifiers
- Completed various improvements throughout the document

October 12, 2011, Preliminary Manual. Updated the instructions for Hot Extraction/Insertion; introduced numerous improvements to the Registers; and completed various minor changes throughout the document.

July 15, 2011, Preliminary Manual

- Added a new chapter about Performance
- Removed references to SerDes TX to RX Loopback Mode and Port Level Loopback features, and their respective register functionality (SERDES_LPBK and PORT_LEVEL_LPBK_SWITCH_SIDE_EN fields)
- Completed other minor improvements throughout the document

February 22, 2011, Preliminary Manual

- Fixed minor errors and completed numerous improvements

November 2, 2010, Preliminary Manual

- Added a caution about JTAG register access in Configuration Register Access (Revision A/B)
- Added additional information about Port Reconfiguration Operations
- Updated Table 8, Table 9, and Table 10 in Hot Insertion/Extraction
- Added a new section, Signal Quality Optimization
- Added a second note about Port {0..17} Control 1 CSR.PWIDTH_OVRD

July 23, 2010, Preliminary Manual

- Changed the order of the PLL_SEL and PORT_SEL fields in the Device Reset Control Register; the PLL and port numbers were incorrectly reversed in these fields
- Added a note to PWIDTH_OVRD in the Port n Control 1 CSR
- Changed the default value of RX_DFE_DIS in Lane n DFE 1 CSR to 0b1
- Added a note to MAX_DESTID in the Switch Multicast Information CAR clarifying an incorrect default value for the field
- Added the VC Register Block Header Register into the registers chapter; however, this register is not supported by the CPS-1848.
- Added a new section called Port Reconfiguration Operations

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1. Device Overview

This chapter provides an overview of the CPS-1848's capabilities. Topics discussed include the following:

- Device Description
- Key Features
- Block Diagrams
- Typical Applications

1.1 Device Description

The CPS-1848 is a low-latency, 18 port, 48 lane, Gen2 RapidIO switch that supports a peak sustained throughput of 240 Gbps (see Figure 1). The switch is ideal for interconnecting Gen1 and Gen2 RapidIO endpoints, including microprocessors, DSPs, FPGAs, ASICs, and bridges. The CPS-1848 supports port widths of 1x, 2x, and 4x, and lane speeds of 1.25, 2.5, 3.125, 5.0, and 6.25 Gbaud. The switch supports the RapidIO long run specification (100 cm of FR4 with two connectors), so it is ideal for backplane and interchassis switching applications, as well as on-board interconnect.

All RapidIO packets that are compliant to the *RapidIO Specification (Rev. 2.1)*, Part 6: LP-Serial Physical Layer Specification and Part 3: Common Transport Specification, are accepted and routed by the CPS-1848. Packets are scheduled based on priority in accordance with the RapidIO specification. This includes FType 9 data streaming packets described in the RapidIO specification, Part 10: Data Streaming Specification.

RapidIO switching supports standard RapidIO routing functionality, including unicast and up to 40 multicast groups. The CPS-1848 exceeds the *RapidIO Specification (Rev. 2.1)* to support broadcast routing of packets and an innovative hierarchical routing scheme that supports all 64K 16-bit destIDs. The CPS-1848 supports the CRF bit to enable flow control based on eight separate priorities. The CPS-1848's queue aging function also ensures that high priority traffic does not starve low priority traffic under congestion. In addition, the CPS-1848 supports a powerful packet trace and filter functionality, and a separate routing path for maintenance packets.

The CPS-1848 is designed to support fault tolerant systems. *RapidIO Specification (Rev. 2.1)*, Part 8 "Error Management Extensions" support is supplemented by additional implementation specific event detection and notification functionality. Fault isolation support includes the RapidIO standard "leaky bucket" port failure handling, as well as implementation specific functions. Hot swap is fully supported through the use of "per port"' reset capability.

In addition to the RapidIO Interface, the CPS-1848 supports JTAG 1149.1 and 1149.6 test and register access interface, as well as I2C master and slave access.

1.2 Key Features

- RapidIO Interfaces
  - Up to 18 *RapidIO Specification (Rev. 2.1)* compliant ports
  - Up to 48 *RapidIO Specification (Rev. 2.1)* compliant full duplex lanes, supporting 4x, 2x, and 1x ports
  - 1.25, 2.5, 3.125, 5, or 6.25 Gbaud lane rates selectable for each port

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  - Short-, Medium-, and Long-run reach allow power to be optimized for short links while enabling connections up to 100 cm with two connectors
  - Receiver- and Transmitter-Controlled Flow Control
  - User-adjustable transmitter drive strength and emphasis
  - User-adjustable receiver equalization
  - Packet Trace: Each port can match the first 160 bits of every packet against up to four programmable values as comparison criteria to copy the matching packet to a programmable trace port
- Switch Fabric
  - Peak throughput of 240 Gbps
  - Cut-through and store-and-forward modes
  - Non-blocking architecture for both of unicast and multicast flows
  - Multicast splitting provides HOL blocking avoidance for congested multicast legs
  - Per-priority buffering
  - Supports eight RapidIO priorities
  - Supports Multicast Event Control Symbol Receipt and Generation
  - 40 Multicast masks with broadcast capability
  - Global route and per-port local route modes
- Supervision, Fault Management, Congestion Management
  - Compliant with *RapidIO Specification (Rev. 2.1), Part 8: Error Management Extensions Specification*
  - IDT-specific Error Handling including error event history logging and interrupt generation
  - Event detect, count, watermark, threshold, data capture, and host notification capabilities
  - Packet-Retry detect, count, threshold, and host notification capabilities
  - Software-assisted error recovery and per-port reset support seamless hot swap and port recovery
- I^2C Interface
  - Provides I2C port for maintenance and error reporting
  - Master or slave operation
  - Master allows power-on configuration from external ROM
  - Master mode configuration with external image compressing and checksum
- Clock and reset
  - Single input reference clock
  - Global hardware reset
  - Software resets
- Diagnostics, Performance Monitors, and Built-in Self Tests
  - BER measurement facilities including SerDes PRBS testing and protocol decode error counters
  - Various loopback modes
  - Memory BIST and SerDes BIST tests
  - Extensive packet counters and diagnostic counters
- Full JTAG Boundary Scan Support (IEEE1149.1 and 1149.6)

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1.3 Block Diagrams

Figure 1 shows a high-level overview of the device. Conceptually, the CPS-1848 consists of four quadrants numbered 0 to 3. Each quadrant consists of 12 lanes that can be mapped to four or five ports. Each quadrant can have combinations of 1x, 2x, and 4x ports (for more information, see Lane to Port Mapping).

The ports are connected through a non-blocking switch fabric. The ports and switch fabric support a separate routing path for maintenance packets which provides register access from any RapidIO port. In addition, the I^2C Interface and the JTAG 1149.1 Interface also support access to the CPS-1848's registers. Figure 1 is expanded upon in the following chapters as more information is provided about the device's lanes, ports, and switch fabric.

Figure 1: CPS-1848 Block Diagram

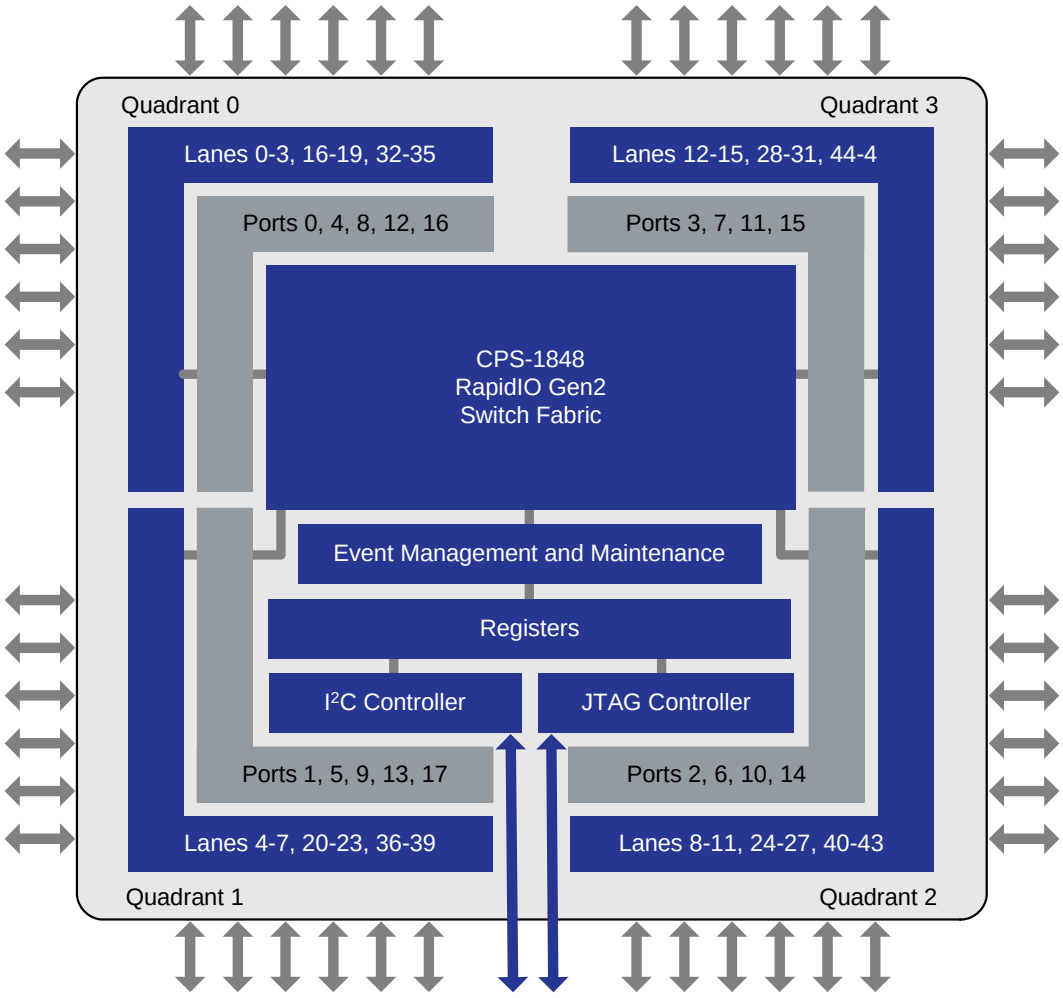

Figure 2 provides a summary of the device's interface signals.

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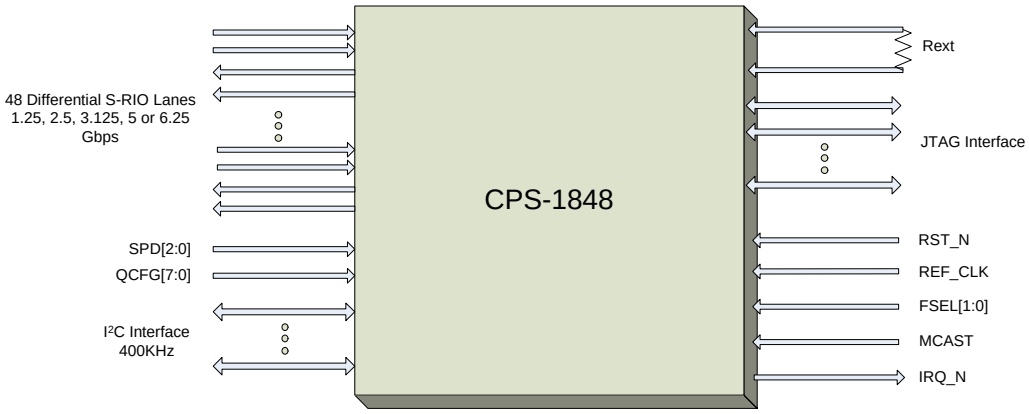
Figure 2: CPS-1848 Interconnect Diagram



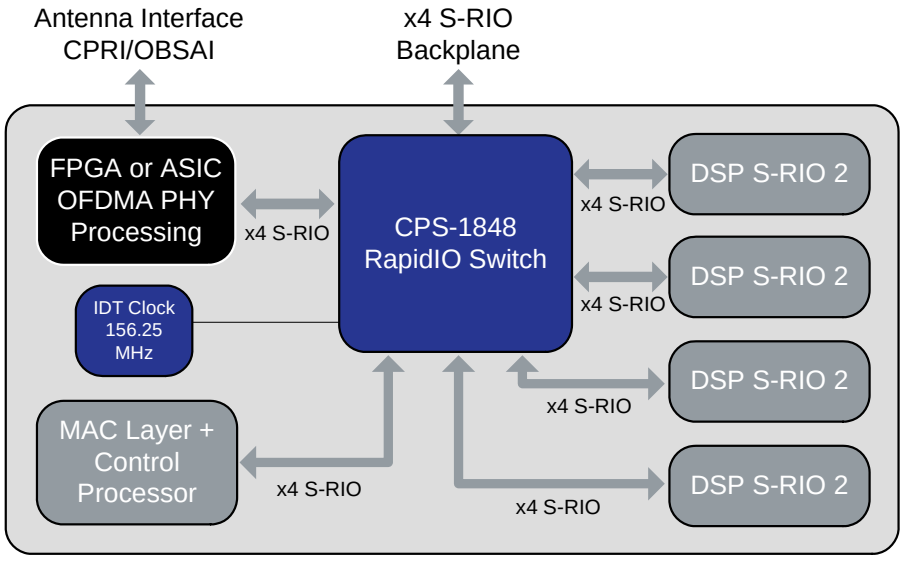
1.4 Typical Applications

The CPS-1848, in tandem with other RapidIO ecosystem switches and endpoints, enables next-generation compute density and power efficiency. This significantly increases channel capacity for 3G to 4G wireless infrastructure, media gateways, video conferencing, and military and medical imaging systems. Full peer-to-peer networking makes systems of arbitrary topology possible.

1.4.1 Wireless Application Benefits

- Carrier-grade reliable packet transport
- Gen2 performance to power ratio allows unprecedented compute density to enable 3G and 4G systems
- Switched architecture allows highly scalable system for micro and macro BTS implementations
- Carrier-grade 6.25 Gbaud SerDes enables backplane-based modular systems and system scaling by inter-chassis cabling
- Ecosystem-standard support for four priorities plus Critical Request flow provides strong QoS support for multiple data flows plus control plane

Figure 3: Wireless Application



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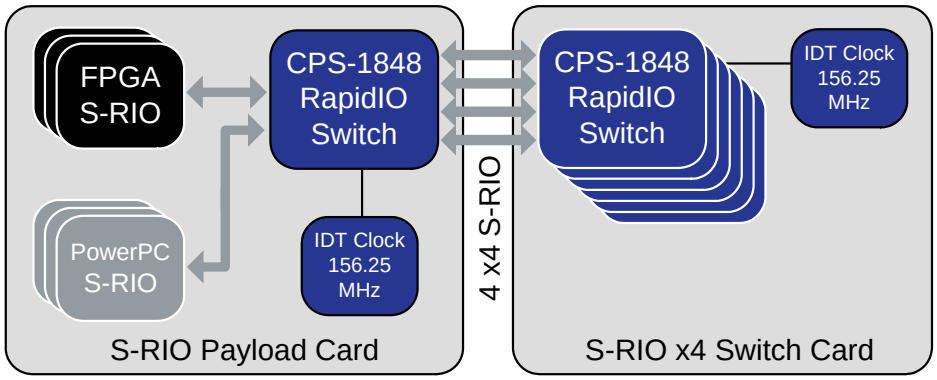
1.4.2 Defense and Aerospace Application Benefits

- S-RIO Error Management Extension support including Time-to-Live enables fault-tolerant systems
- VITA 41, Open VPX, and ATCA fabric mappings enable rapid development of modular, standards-based systems
- RapidIO-standard true peer-to-peer networking allows scaling of arbitrary topology and simplifies hot swap software implementation
- Per-port filter feature allows blocking errant packets or malicious attack (for example, denial of service, system memory reads and writes)

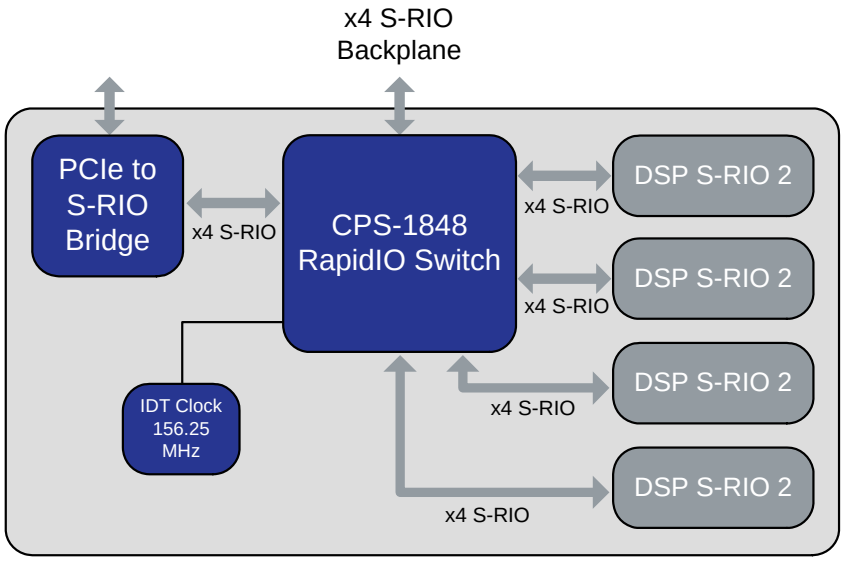
Figure 4: Military Open VPX System Application



1.4.3 Video and Imaging Application Benefits

- 40 multicast masks per port provides strong support for broadcasting or multicasting a specific data stream to multiple endpoints executing unique transforms, scaling, and CODECs

Figure 5: Video and Imaging Application



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2. RapidIO Ports

This chapter describes the S-RIO port functionality of the CPS-1848. Topics discussed include the following:

- Overview
- Key Features
- Packet Routing
- Flow Control
- Multicast Event Control Symbols
- Port Reconfiguration Operations
- Reset Control Symbol Processing
- Hot Extraction/Insertion
- Packet Trace and Filtering
- Packet Generation and Capture
- Packet Transfer Validation and Debug

2.1 Overview

Each CPS-1848 S-RIO port is compliant to the *RapidIO Specification (Rev. 2.1)*. Each port provides the S-RIO defined Physical Coding Sublayer (PCS) functionality and the packet exchange protocol management. Each port also connects to the associated SerDes blocks and the switch fabric block, as displayed in Figure 6.

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Figure 6: S-RIO Port Diagram

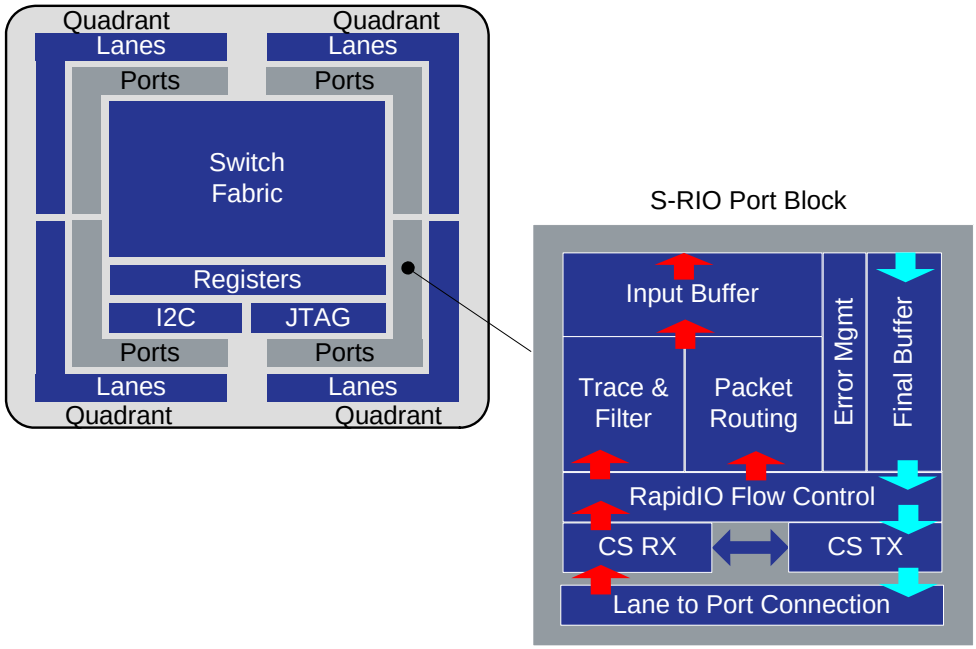

Figure 6 shows a block diagram of an S-RIO Port Block. The key components of this port diagram are discussed throughout the chapter.

2.2 Key Features

The S-RIO Block supports the following:

- 8b/10b codec
- Data scrambling/descrambling
- Lane/Link initialization management
- Control symbol generation
- Control symbol reception/decode
- IDLE sequence generation/control
- Receiver- and transmitter-controlled flow control
- S-RIO-based reset support
- Packet retransmission management
- Link maintenance and software-assisted error recovery
- Packet transmission cancellation
- Link error detection and recovery
- Packet forwarding
- IDT-specific packet trace and filtering

This functionality is compliant to the following S-RIO specifications:

- *RapidIO Specification (Rev. 2.1), Part 1: Input/Output Logical Specification*
- *RapidIO Specification (Rev. 2.1), Part 2: Message Passing Logical Specification*

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- *RapidIO Specification (Rev. 2.1), Part 3: Common Transport Specification*
- *RapidIO Specification (Rev. 2.1), Part 6: LP-Serial Physical Layer Specification*
- *RapidIO Specification (Rev. 2.1), Part 7: System and Device Interoperability Specification*
- *RapidIO Specification (Rev. 2.1), Part 8: Error Management Extensions Specification*
- *RapidIO Specification (Rev. 2.1), Part 9: Flow Control Logic Layer Extensions Specification*
- *RapidIO Specification (Rev. 2.1), Part 11: Multicast Extensions Specification*
- *RapidIO Specification (Rev. 2.1), Annex I: Software/System Bring Up Specification*

2.3 Packet Routing

The main function of each S-RIO port is to route received packets to the appropriate port(s) on the switch. Packet routing is supported in a RapidIO standard method using routing tables and standard RapidIO registers for multicast functionality. Packet routing is supplemented by implementation-specific registers for both the routing tables and for multicast. In addition, debug features such as packet trace and filtering augment the normal packet routing.

The following sections describe routing table operation and programming, multicast operation and programming, and the packet trace/filtering debug functionality.

2.3.1 Packet Routing Overview

Each S-RIO port provides a 256 entry Device Routing Table and a 256 entry Domain Routing Table. The scenario for the use of the Domain and Device Routing Tables is a large system that has multiple chassis connected together, and multiple boards in each chassis. The Domain Routing Table selects which chassis/board to route packets to, while the Device Routing Table routes packets to a specific processing element on a board.

Figure 7: Routing Table Flowchart

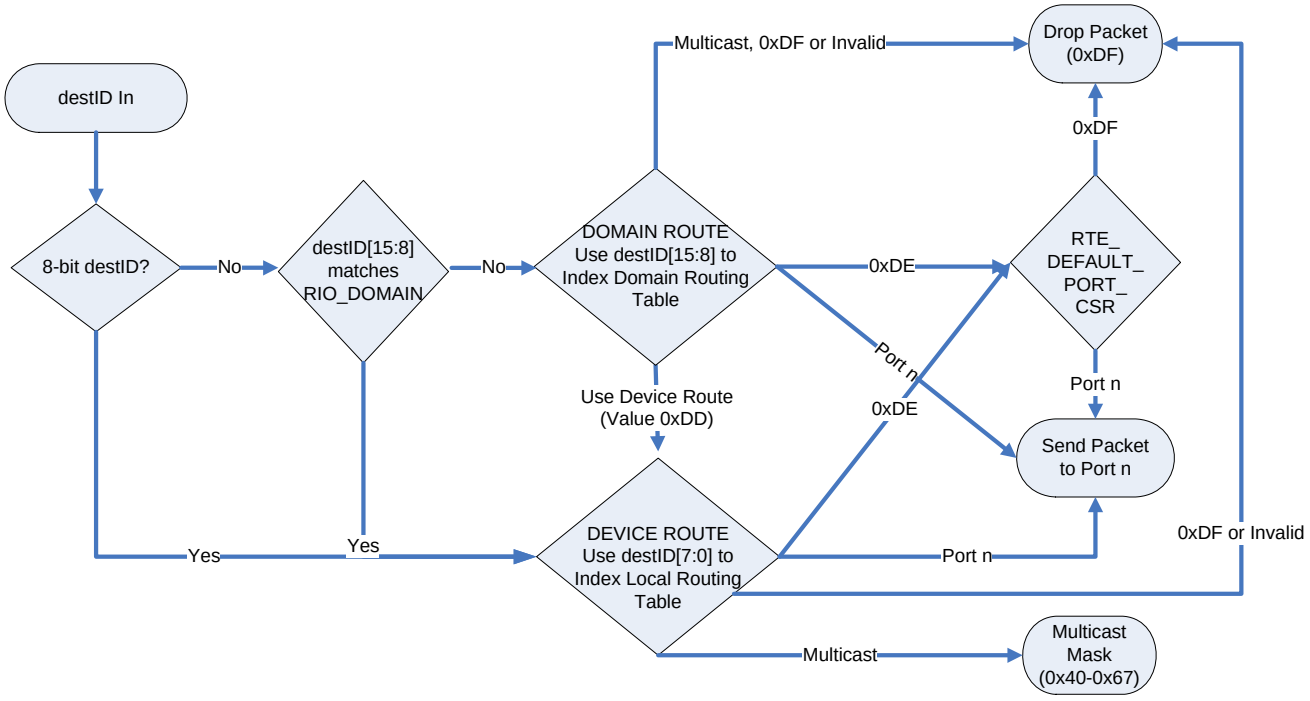

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Figure 7 shows the decision tree for routing a received packet. The Device Routing Table routes packets with 8-bit destIDs, and 16-bit destIDs whose most significant byte is 0. Packets with 16-bit destIDs whose most significant byte is non-zero are routed using the Domain Routing Table, unless:

- The most significant 8 bits of the 16-bit destID match the value programmed in the RapidIO Domain Register, or
- The Domain Routing Table entry for the destID has a value of 0xDD.

Table 1 explains the meaning of the Domain and Device Routing Table port entry values, and restrictions on which values can be programmed to the Domain or Device Routing Tables.



Programming a value into a routing table entry that is not allowed according to Table 1 causes packets whose destID matches that routing table entry to be discarded.



Programming the number of a port that has no lanes assigned to it causes that packet to be dropped (equivalent to No Route, value 0xDF).

Table 1: Route Table Reference Restrictions

Port Value Range	Reference To	Allowed in Device Route Table	Allowed in Domain Route Table
0x00–0x11	Port Numbers	Yes	Yes
0x12–0x3F	Reserved	No	No
0x40–0x67 (0x40 + Mask Index)	Multicast Mask	Yes	No
0x68–0xDC	Reserved	No	No
0xDD	Force Local	No	Yes
0xDE	Default Route	Yes	Yes
0xDF	No Route	Yes	Yes
0xE0–FF	Reserved	No	No

2.3.2 Unicast Programming Model

The CPS-1848 supports the RapidIO standard programming model through the following registers:

- Standard Route Table Entries Configuration destID Select CSR
- Standard Route Table Entry Configuration Port Select CSR
- Standard Route Table Entry Default Port CSR

The Standard Route Table Entries Configuration destID Select CSR specifies the destID whose routing is affected by writes to the Standard Route Table Entry Configuration Port Select CSR. The Standard Route Table Entry Configuration Port Select CSR can be read to determine the current route for a destID. Using the standard registers is called “indirect” routing table programming.



Reading or writing a routing table entry requires two accesses. These accesses must be handled as an atomic operation. If multiple software entities can access the routing table at the same time, mutual exclusion must be enforced to ensure that one entity’s routing table updates do not corrupt another entity’s efforts.

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Direct Routing Table Programming is the preferred access method in a multi-host system because it does not require mutual exclusion.

The standard programming model requires one implementation-specific register, RapidIO Domain Register, to support the Domain Routing Table. If the DESTID_MSB field of the Standard Route Table Entries Configuration destID Select CSR is 0, or if the DESTID_MSB matches the destID located in the RapidIO Domain Register DOMAIN field, the Device Routing Table is written. Otherwise, the LARGE_CFG_DEST_ID_MSB value determines which entry in the Domain Routing Table is updated.

As displayed in Unicast Programming Examples, there are some special values that can be programmed into the routing table. If 0xDE is written, packets with that destID are routed according to the port specified in the Standard Route Table Entry Default Port CSR. After reset, all destIDs are routed to the port value in this register:

- If 0xDD is programmed into the Broadcast Device Route Table Register {0..255}, the packet is discarded and the routing table entry is overwritten with a value of 0xDF.
- If 0xDD is programmed into the Broadcast Domain Route Table Register {0..255}, packets that are in that domain are routed according the Broadcast Device Routing Table.
- If a value of 0xDF is programmed into either the Domain or Device Routing Table, packets sent to that destID are discarded.

The CPS-1848 supports routing table programming functions beyond what is indicated in the *RapidIO Specification (Rev. 2.1)* (see Programming Examples).

2.3.2.1 Per-Port Routing Tables

The CPS-1848 has a routing table for each port. This allows packets with the same destID to be routed differently depending on which port they are received. This can be used to partition the switch, or to create virtual networks.

The Route Port Select Register selects whether all ports or one specific port is updated through the Standard Route Table Entries Configuration destID Select CSR and Standard Route Table Entry Configuration Port Select CSR. The Route Port Select Register default value selects all ports for routing table updates.

Port-writes generated by the CPS-1848 are routed using routing table entries that are programmed using broadcast registers (for more information, see Port-Write Programming Model).

2.3.2.2 Extended Configuration Mode – Block Reads/Writes

The CPS-1848 supports the optional standard mechanism for reading or writing four routing table entries at once for the Device Routing Table. These are called “Block” accesses. Block reads and writes are enabled by setting EXTD_EN to 1 in the Standard Route Table Entries Configuration destID Select CSR. A Block access can only occur when the DESTID_MSB selects the Device Routing Table.

Block accesses cannot be performed to the Domain Routing Table. They can only be performed for 8-bit destIDs, or using 16-bit destIDs 0x0000 through 0x00FF.

When Block accesses are enabled, reading the Standard Route Table Entry Configuration Port Select CSR for a Device Routing Table entry will return the values for four destIDs, starting with the destID specified in the Standard Route Table Entries Configuration destID Select CSR.

If a Block Read exceeds the end of the Device Routing Table, the Block Read results are undefined. For example, a Block Read for destID 0xFE will result in undefined data.

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When Block accesses are enabled, writing to the Standard Route Table Entry Configuration Port Select CSR for a Device Routing Table entry will update the entry for the destID specified in the Standard Route Table Entries Configuration destID Select CSR as well as the next three entries.

If a Block Write exceeds the end of the Device Routing Table, the Block Write wraps around to the beginning of the routing table. For example, a Block Write for destID 0xFE will update routing table entries for destIDs 0xFE, 0xFF, 0x00, and 0x01.

2.3.2.3 Direct Routing Table Programming

The CPS-1848 supports an implementation-specific routing table programming model whereby each routing table entry is memory mapped into register space. Similar to the indirect model, registers are defined that affect the routing tables on every port. Registers are also defined that affect just one port (see IDT Specific Routing Table Registers). Direct routing table programming has the advantage of allowing multiple devices to read and write the routing tables with no mutual exclusion requirements. Direct routing table programming also reduces the number of reads and writes that are required to configure a routing table compared to the use of the standard registers. Depending on the specific programming needs, Block accesses may be faster than direct routing table programming.

2.3.2.4 Maintenance Packet Routing

Maintenance packets are handled according to the hop count and destID fields. Maintenance packets with a non-zero hop count are routed through the switch based on their destID. Maintenance packets can be multicast, however system behavior when multicasting packets that require responses is not defined by the *RapidIO Specification (Rev. 2.1)*. Only port-write packets should be multicast.

Maintenance packets with a zero hop count are processed by the switch. The response packet is sent out the port that received the maintenance request. The source ID of the request packet becomes the destID of the response packet, and the destID of the request packet becomes the sourceID of the response packet.

For Revision A/B, Maintenance packets are not ordered with respect to non-maintenance packets. For Revision C, Maintenance packets with a non-zero hop count take the same path through the switch as non-maintenance packets.

2.3.3 Multicast Programming Model

The CPS-1848 supports the standard RapidIO programming model for multicast registers. This model consists of programming the multicast masks that determine how a packet will be replicated, and then associating destIDs with multicast masks. The registers include the following:

- Multicast Mask Port CSR – This register controls which destination ports are set in the multicast mask.
- Multicast Association Selection CSR – This register selects both the destID and multicast mask.
- Multicast Association Operations CSR – This register controls whether or not a destID is routed according to a multicast mask.

The CPS-1848 handles 8-bit destIDs, and 16-bit destIDs that start with 0x00, as the same. Forming an association for an 8-bit destID 0xXX forms an association with the 16-bit destID 0x00XX. The TYPE bit of the Multicast Association Operations CSR is ignored for 8-bit destIDs.

Multicast associations can be made only to destIDs in the Device Routing Table. The implication is that only 8-bit destIDs, or 16-bit destIDs that are routed according to the Device Routing Table, can be multicast.

The CPS-1848 supports multicast programming functions beyond what is specified in the *RapidIO Specification (Rev. 2.1)*. These functions are discussed in the following sections. For examples of multicast routing programming, see Multicast Programming Examples.

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2.3.3.1 Per-Port Multicast Programming

Similar to the Unicast Programming Model, the CPS-1848 Multicast Programming Model allows each of the 40 multicast masks, and the associations between destIDs and the multicast masks, to be unique for each port. This allows switches to be partitioned, and to form virtual networks.

The Multicast Route Select Register controls which ports multicast masks are being controlled by the standard multicast registers.

2.3.3.2 Direct Multicast Mask Programming

Also similar to the Unicast Programming Model, the CPS-1848 contains registers that memory map the multicast masks to register space. There are registers defined that update a multicast mask for all ports (see Broadcast Multicast Mask Register {0..39}), as well as port-specific multicast masks (see Port {0..17} Multicast Mask Register {0..39}).

Multicast routing requires a multicast mask to be associated with a destination ID. This can be accomplished by using the device routing tables to associate a multicast mask with one or more destination IDs.

2.3.3.3 Broadcast Routing

The *RapidIO Specification (Rev. 2.1)* requires that multicast packets are not replicated to the port that they are received on. This allows one multicast mask to be shared among many endpoints that do not want to receive the data they have sent.

In some applications, it is useful to receive a message that has been multicast. This capability is supported by the CPS-1848 on a per-port basis through the use of the SELF_MCAST_EN bit in the Port {0..17} Operations Register.

2.3.4 Programming Examples

This section contains examples of successful routing table and multicast programming.

2.3.4.1 Unicast Programming Examples

Table 2: Unicast Programming Examples – Indirect Programming

Example	Register	Offset	Value
Route destID 0x21 to port 3 for all ports.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00000021
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x00000003
Route destID 0x43 to port 10 for port 7.	Route Port Select Register	0x10070	0x00000008
	Standard Route Table Entries Configuration destID Select CSR)	0x70	0x00000043
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x0000000A
Route destID 0x4321 to port 5 for all ports.	Route Port Select Register	0x10070	0x00000000
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00004321
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x00000005

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Table 2: Unicast Programming Examples – Indirect Programming *(Continued)*

Example	Register	Offset	Value
Route destID 0x5500–0x55FF according to the Device Routing Table for all ports.	RapidIO Domain Register	0xF20020	0x00000055
Route destID 0x7700–0x79FF according to the Device Routing Table for all ports.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00007700
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DD
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00007800
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DD
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00007900
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DD
Set the default output port to 0x05.	Standard Route Table Entry Default Port CSR	0x78	0x00000005
Route destID 0x7A00–0x7AFF to the default port.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00007A00
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DE
Discard all packets sent to destID 0x45.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00000045
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DF
Discard all packets sent to destID 0x7B00–0x7BFF.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00007B00
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DF
Read Broadcast routing table entry for destID 0x88.	Standard Route Table Entries Configuration destID Select CSR	0x70	0x00000088
	Standard Route Table Entry Configuration Port Select CSR	0x74	Read
Read Port 3 routing table entry for destID 0x99.	Route Port Select Register	0x10070	0x00000004
	Standard Route Table Entries Configuration destID Select CSR	0x70	99
	Standard Route Table Entry Configuration Port Select CSR	0x74	Read

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Table 2: Unicast Programming Examples – Indirect Programming *(Continued)*

Example	Register	Offset	Value
Route destIDs 0x11, 0x12, 0x13 and 0x14 to ports 10, 11, 12, and 13.	Route Port Select Register	0x10070	0x00000000
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x80000011
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x0D0C0B0A
Read the routing for destIDs 0x24, 0x25, 0x26, and 0x27 for port 7.	Route Port Select Register	0x10070	0x00000008
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x80000024
	Standard Route Table Entry Configuration Port Select CSR	0x74	Read

Table 3: Unicast Programming Examples – Direct Programming

Example	Register	Offset	Value
Route destID 0x21 to port 3 for all ports.	Broadcast Device Route Table Register {0..255}	0xE00084	0x00000003
Route destID 0x43 to port 10 for port 7.	Port {0..17} Device Route Table Register {0..255}	0xE1710C	0x0000000A
Route destID 0x43xx to port 5 for all ports.	Broadcast Domain Route Table Register {0..255}	0xE0050C	0x00000005
Route destID 0x5500 to 0x55FF according to the Device Routing Table for all ports.	Broadcast Domain Route Table Register {0..255}	0xE00554	0x000000DD
Route destID 0x7700 to 0x79FF according to the Device Routing Table for all ports.	Broadcast Domain Route Table Register {0..255}	0xE005DC	0x000000DD
		0xE005E0	0x000000DD
		0xE005E4	0x000000DD
Set the default port to 5.	Standard Route Table Entry Default Port CSR	0x78	0x00000005
Route destID 0x7A00 to 0x7AFF to the default port.	Broadcast Domain Route Table Register {0..255}	0xE005E8	0x000000DE
Discard all packets sent to destID 0x45.	Broadcast Device Route Table Register {0..255}	0xE00114	0x000000DF
Discard all packets sent to destID 0x7B00 to 0x7BFF.	Broadcast Domain Route Table Register {0..255}	0xE005EC	0x000000DF
Read Broadcast Routing Table entry for destID 0x88.	Broadcast Device Route Table Register {0..255}	0xE00220	Read
Read Port 3 Routing Table entry for destID 0x99.	Port {0..17} Device Route Table Register {0..255}	0xE13264	Read

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2.3.4.2 Multicast Programming Examples

Table 4: Multicast Programming Examples – Indirect Programming Model

Example	Register	Offset	Value
Multicast DestID 0x01 to ports 4, 5, 6, and 7 on all ports using multicast mask 0x27.	Multicast Mask Port CSR	0x80	0x00270410
			0x00270510
			0x00270610
			0x00270710
	Multicast Association Selection CSR	0x84	0x00010027
	Multicast Association Operations CSR	0x88	0x00000060
Reprogram Multicast Mask 0x20 to send to only ports 10, 11, and 12.	Multicast Mask Port CSR	0x80	0x00200040
			0x00200A10
			0x00200B10
			0x00200C10
Associate DestID 0x03 with Multicast Mask 0x20 on all ports except port 11. The association is performed in two steps: 1. Associate all ports with the mask. 2. Disassociate port 11.	Multicast Association Selection CSR	0x84	0x00030020
	Multicast Association Operations CSR	0x88	0x00000060
	Multicast Route Select Register	0x10080	0x0000000C
	Multicast Association Operations CSR	0x88	0x00000020[1]
Allow DestID 0xFF00 through FFFF to be multicast according to the Device Routing Table on all ports.	Route Port Select Register	0x10070	0x00000000
	Standard Route Table Entries Configuration destID Select CSR	0x70	0x0000FF00
	Standard Route Table Entry Configuration Port Select CSR	0x74	0x000000DD

1. When a multicast mask is disassociated from a destID, the destID routing table value is 0xDF (drop packets).

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Table 5: Multicast Programming Examples – Direct Programming Model

Example	Register	Offset	Value
Multicast DestID 0x01 to ports 4, 5, 6 and 7 on all ports using multicast mask 0x27.	Broadcast Multicast Mask Register {0..39}	0xF3009C	0x000000F0
	Broadcast Device Route Table Register {0..255}	0xE00004	0x00000067
Reprogram Multicast Mask 0x20 to send to only ports 10, 11, and 12.	Broadcast Multicast Mask Register {0..39}	0xF30080	0x00001C00
Multicast DestID 0x05 to ports 6, 7, 8 and 9 using multicast mask 3 on port 6 and mask 4 on port 7, 8, and 9. Multicast will only occur for packets received by ports 6, 7, 8 and 9.	Port {0..17} Multicast Mask Register {0..39}	0xF3860C	0x000003C0
	Port {0..17} Device Route Table Register {0..255}	0xE16014	0x00000043
	Port {0..17} Multicast Mask Register {0..39}	0xF38710	0x000003C0
	Port {0..17} Device Route Table Register {0..255}	0xE17014	0x00000044
	Port {0..17} Multicast Mask Register {0..39}	0xF38810	0x000003C0
	Port {0..17} Device Route Table Register {0..255}	0xE18014	0x00000044
	Port {0..17} Multicast Mask Register {0..39}	0xF38910	0x000003C0
	Port {0..17} Device Route Table Register {0..255}	0xE19014	0x00000044

2.4 Flow Control

The CPS-1848 supports a variety of flow control functions. Receiver- and transmitter-controlled flow control are the most basic RapidIO flow control functions. One of these functions is always active on a link. In receiver-controlled flow control, the receiver tells the transmitter when it cannot accept a packet due to a lack of resources by issuing a retry. The transmitter then resumes packet transfer with a packet of higher priority than the one that was retried, if such a packet is available, and retries (or resends) the original packet at a later time, perhaps with increased priority.

Transmitter-controlled flow control is the default mode of each port. In this mode, the transmitter only sends packets which the receiver can accept. The choice between receiver- and transmitter-controlled flow control is made automatically as part of Port and Lane Initialization Sequence. The flow control mode that is active on a link is reported in the RX_FC field of the Port {0..17} Status and Control Register. For more information on receiver and transmitter-controlled flow control, see Part 6 of the *RapidIO Specification (Rev. 2.1)*.

2.4.1 Transmitter- and Receiver-Controlled Flow Control Programming Model

Transmitter- and receiver-controlled flow control decide which packets to send based on a packet's priority. The CPS-1848 supports the four standard RapidIO priorities numbered 0 to 3 where 3 is the highest priority. The CPS-1848 also supports the Critical Request Flow (CRF) bit which extends the number of priorities supported from four to eight.



Transmitter-controlled flow control can be disabled on a port using the TX_FLOW_CTL_DIS bit in the Port {0..17} Operations Register.

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Priority 0, 1 and 2 packets all have buffer allocation values associated with them. These flow control values are called “watermarks”, a shortened form of “high watermark”: the highest point on shore that water reaches. The watermark associated with a specific priority determines when a buffer is too full to accept/transmit packets of a specific priority. Note that there is no watermark for priority 3 packets, since priority 3 packets must always be accepted whenever buffers are available.

When transmitter-controlled flow control is active on a port, the transmitter must have watermark values for the packets which it transmits to the receiver. The watermarks reside in the Port {0..17} Watermarks Register. These watermarks define the number of available buffers at which point packets of that priority will stop being transmitted. If a system is rarely congested, the default values for this register will deliver optimal performance.



The watermark values in the Port {0..17} Watermarks Register should be set based on the buffer size of the link partner and the required traffic characteristics for packets of each priority. The default values will result in optimal throughput when traffic is bursty and congestion is rare in the system, as they maximize the number of low priority packets that can be accepted. When congestion is normal and traffic of a specific priority must have guaranteed throughput, adjust the watermark values to reserve sufficient buffers in the link partner. Depending on the link latency, two or three buffers per congested priority must be reserved to ensure line rate throughput.

2.5 Multicast Event Control Symbols

Multicast Event Control Symbols (MECS) distribute events with low latency and little variability in distribution delays throughout a RapidIO system. An MECS can be received by a CPS-1848 port, or can be triggered by the MCAST pin on the device. Once an MECS event has been received/triggered, the MECSs are transmitted by each port with the MCAST_CS field set to one in the Port {0..17} Control 1 CSR. Note that the port which received the MECS does not transmit the MECS.



The CPS-1848 provides a physical pin called MCAST that can generate an MECS to all Multicast Event participant egress ports (for more information, see the *CPS-1848 Datasheet*).



If two or more MECSs are received close enough in time that more than one is waiting for transmission on a port, then at least one of them is forwarded. The other(s) may not be (For information on minimum period duration between MECSs, see Multicast-Event Control Symbol (MECS) Latency). The most recently received MECS will be transmitted. Regardless of how many MECSs are received under these conditions, at least one will be transmitted from each participant port.

2.6 Port Reconfiguration Operations

When one of the following port configuration events occur, a CPS-1848 port will require a re-initialization or reset (see Table 6).

Table 6: Port Reconfiguration Operations

Port Configuration Event	Recommended Port Operation
Quadrant Configuration Register change	Port reset (see PORT_SEL in Device Reset and Control Register)
PLL {0..11} Control 1 Register.PLL_DIV_SEL change	PLL reset (see PLL_SEL in Device Reset and Control Register)
Lane {0..47} Control Register.TX_RATE or RX_RATE Lane rate change	Port reset (see PORT_SEL in Device Reset and Control Register). For examples of reconfiguring port and lane speeds, see Lane and Port Speeds.
Port {0..17} Error and Status CSR.IDLE2_EN change	Port reset (see PORT_SEL in Device Reset and Control Register)

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Table 6: Port Reconfiguration Operations *(Continued)*

Port Configuration Event	Recommended Port Operation
Lane {0..47} Control Register.LANE_DIS Lane disable/enable	Port reset (see PORT_SEL in Device Reset and Control Register)
Port {0..17} Operations Register.TX_FLOW_CTL_DIS TX Flow control disable/enable	Force-reinit required (see FORCE_REINIT in Port {0..17} Operations Register)



These recommended port operations also apply when any of these port configuration events are performed within an EEPROM load. After each event, the recommended operation should be implemented within the EEPROM load (for more information, see the note in EEPROM Format).

2.6.1 Disabling IDLE2 Operation

When operating at lane speeds of 5 Gbaud or less, IDLE2 operation should be disabled in order to improve link performance, as displayed in Table 7.

Table 7: Disabling IDLE2 Operation on Port 3

Step	Register	Offset	Value
1. Disable IDLE2 by setting IDLE2_EN to 0.	Port {0..17} Error and Status CSR	0x0001B8	0x80000000
2. Perform a port reset by writing to PORT_SEL.[1]	Device Reset and Control Register	0xF20300	0x80000008
3. Once the port achieves PORT_OK (PORT_OK is 1), then disable IDLE2 on the connected port using maintenance packet, I2C, or JTAG.	Port {0..17} Error and Status CSR	0x0001B8	-

1. After performing a port reset, clear Port {0..17} Error and Status CSR.PORT_ERR if it was set during the reset process (for more information, see HS-LP Controlled Recovery). For Revision A/B devices, a Link-Request control symbol must be sent to clear the fatal error condition before clearing PORT_ERR.

2.7 Reset Control Symbol Processing

A RapidIO device can be reset using a RapidIO reset request. This type of reset request consists of four reset request control symbols received with no intervening control symbols, except status control symbols.

The CPS-1848 can handle a RapidIO reset request in one of two ways, based on the value of the PORT_RST_CTL field of the Device Control 1 Register. A value of 0 resets the entire CPS-1848, while a value of 1 resets just the port that received the reset request. For more information about a “per-port” reset, see the following section.

2.7.1 Per-Port Reset

A per-port reset causes a RapidIO port to behave as follows:

1. All outstanding error states and retry states are cleared. This includes input-error and output-error.
2. All unacknowledged, transmitted packets are discarded, and tracking of transmitted packets is cleared.
3. Any current packet being received is discarded by the switch. The packet is not acknowledged.
4. Tracking of outstanding Link-Request/Input-Status (error recovery) control symbols is reset.

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5. The next transmitted and received ackID values are reset to 0. The next packet to be transmitted by the port will have ackID 0. The expected ackID of the next packet is 0.
6. Detectable errors on control symbols or packets received by the port in the cycle in which the reset event occurs are ignored.
7. Packets stored in the port's input buffer are discarded.
8. Packets stored in the crosspoint buffers that feed the port's final buffer of the port are discarded while the port is held in reset.
9. Packets stored in the port's final buffer are discarded.

If many congested ports were sending packets to the reset port, some packets may exist in the final buffer after the reset. It is also possible for maintenance responses to be sent after the reset because maintenance requests with a hop count of 0 are processed outside of the receiving port.

10. The Port {0..17} Error and Status CSR is updated as follows:
    - PORT_UNINIT is set to 1
    - PORT_OK is set to 0
    - INPUT_ERR_STOP is set to 0
    - INPUT_ERR is set to 0
    - INPUT_RETRY_STOP is set to 0
    - OUTPUT_ERR_STOP is set to 0
    - OUTPUT_ERR is set to 0
    - OUTPUT_RETRY_STOP is set to 0
    - OUTPUT_RETRIED is set to 0
    - OUTPUT_RETRY is set to 0
    - PORT_ERR is set to 0 (Revision C)

The following is applicable to Revision A/B.

PORT_ERR is not cleared by a per-port reset. If PORT_ERR is set then the port will drop all packets routed to the Final Buffer, including maintenance packet responses.

To recover, the port must send a Link-Request/Input Status control symbol and receive a response. This will clear the PORT_ERR and packet drop condition. The CPS-1848 will send a Link-Request/Input Status control symbol when either of the following occurs:

- A Packet Not Accepted control symbol is received
- 0b100 is written to the Port {0..17} Link Maintenance Request CSR.CMD

For more information on clearing PORT_ERR, see HS-LP Controlled Recovery.

11. The link begins to retrain, starting from the SILENT state.

Routing table programming is retained after a per-port reset.

All registers other than the registers referenced above retain the values they had before the per-port reset request was received.

Writing to the Port {0..17} Link Maintenance Request CSR for the correct port requires knowledge of the port number on the link partner. If it is possible to be connected to one of many ports, it is necessary to write to the Port {0..17} Link Maintenance Request CSR for each port.

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2.7.2 Port Disable/Enable

When a port is disabled and then enabled by setting and clearing Port {0..17} Control 1 CSR.PORT_DIS, the behavior of the port is as described in Per-Port Reset. The only difference is that packets are discarded for the entire period when PORT_DIS is set.

ackID resynchronization is required when PORT_DIS is set and cleared.

The procedure for ackID resynchronization is specific to the link partner device. If the link partner is a CPS Gen2 device, resetting the link partner port and the local port will resynchronize the ackIDs (for more information, see System Controlled Recovery).

2.7.3 Generating a Reset Request

The CPS-1848 can generate a reset request to its link partner by writing 0x0000_0003 to the Port {0..17} Link Maintenance Request CSR.

In some systems, it may be necessary to check that the link partner has acted on the reset request. This should be apparent when the Port {0..17} Error and Status CSR PORT_OK bit is cleared, and the Port {0..17} Error and Status CSR PORT_UNINIT bit is asserted. Event notification can be configured to send a port-write or assert an interrupt when this occurs (for more information, see Event Management).

Once the link partner acts on the reset request, Port {0..17} Control 1 CSR.PORT_LOCKOUT should be asserted until the link has retrained. This will cause all packets destined for the port to be discarded.

If the link partner accepts the reset, it will clear the expected and transmitted ackID values to 0. The Port {0..17} Local ackID CSR should be cleared to 0, and the CLR bit in this register should be set to 1. This will cause all outstanding unacknowledged packets to be dropped.

A Link-Request/Input-Status control symbol should be sent to the link partner by writing to Port {0..17} Link Maintenance Request CSR[CMD] after a reset request followed by a link-response.

Alternatively, the procedure for hot insertion can reset the link partner and discard all packets, as described in Link Partner Insertion.

2.8 Hot Extraction/Insertion

The hot extraction and insertion procedure is used to replace or upgrade hardware. It can also reset and then re-establish communication with link partners, whether or not they have been physically replaced.

The following sections use the phrase “hot-swap link partner” (HS-LP) to identify the entity that is the subject of the hot extraction/insertion or reset. The HS-LP can be the link partner of the CPS-1848, or can be the CPS-1848 itself.

Hot Extraction/Insertion support requires exclusive use of the following registers. No Standard Physical Layer Errors can be enabled when Hot Extraction/Insertion functionality is required.

- Port {0..17} Error Report Enable Register
- Lane {0..47} Error Report Enable Register
- Port {0..17} Implementation Specific Error Rate Enable Register

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2.8.1 Hot Extraction

This section describes configuration options to manage controlled and uncontrolled removal/reset of the link partner. The primary considerations when removing/resetting a link partner are:

- Timely notification that the link partner has been removed/reset
- Management of packets sent to the link partner when it has been removed/reset
- Isolation of the system from the link partner if the system design requires central coordination to admit new resources into the system
- Preparing for link partner recovery

2.8.2 Controlled Removal/Reset

To perform controlled removal or reset of a HS-LP, the following steps should be followed. Note that the programming model for performing steps 1 to 4 is located in Preparation For Hot Extraction on Port Y.

1. Disable event notification for the HS-LP, except for extraction/insertion events.
2. Discard packets originated by or routed to the HS-LP.
3. Prevent acceptance of new packets from the HS-LP.
4. Reset and/or extract the HS-LP.
5. Confirm the reset/extraction by reception of an extraction event as described below.
6. Prepare the port for the insertion/return of the link partner as found in Preparation For Hot Insertion on Port Y.

Packets destined for a HS-LP usually should be discarded, since the link partner lacks the context and/or configuration to correctly handle these packets. Also, if traffic continues at a rate that can exhaust the switch buffers while the link partner is not accepting packets, the system can congest and fail. For these reasons, it is assumed that the system should not have transactions flowing in either direction through the CPS-1848 port when preparing for a hot extraction or link partner reset.

The act of removing/resetting the HS-LP will cause errors to be detected on the link. Additionally, since the link partner is no longer present, events unrelated to hot swap/reset should be suppressed. Events related to hot swap/reset can be received to confirm that the link partner has been removed and/or successfully reset.

Once link partner removal/reset has been confirmed, if the link partner is expected to reappear, the port must be prepared for link partner insertion and/or reset completion.

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Table 8: Preparation For Hot Extraction on Port Y

Step	Register	Offset	Mask and Value	Description
1. Disable event notification except for hot swap events.	Port {0..17} Error Rate CSR	0x1068 + (0x40*Y)	0x00000000	Disable error rate bias, clear error rate counter.
	Port {0..17} Error Rate Threshold CSR	0x106C + (0x40*Y)	0x01000000	Set error rate threshold to detect an OUTPUT_FAIL condition (Port {0..17} Error and Status CSR) if one or more errors occur.
	Lane {0..47} Error Rate Enable Register	0xFF8010 + (0x100 * lane_num)	0x00000003	Enable error reporting for loss of lane ready and loss of lane sync events. Repeat for each lane associated with the port.
	Port {0..17} Control 1 CSR	0x00015C + (0x20*Y)	0xXXXXXXXC	Set STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN bits to prevent congestion when the link partner is removed. For more information on when STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN are set, see Event Isolation.
	Port {0..17} Operations Register	F40004 + (0x100*Y)	0x10000000 (PORT_INT_EN) or 0x08000000 (PORT_PW_EN)	Ensure at least one of PORT_INT_EN or PORT_PW_EN is set to ensure notification occurs.
	Port {0..17} Error Report Enable Register	0x031044 + (0x40*Y)	0x80000000	Enable port-writes and interrupt notification for the Hot Extraction events.
	Port {0..17} Implementation Specific Error Report Enable Register	0x03104C + (0x40*Y)	0x80000000	Disable all error reporting except ERR_RATE_EN bit. The default is all bits are enabled in the register; however, this setup can trigger an unexpected event.
	If port-writes are used, ensure that port-write destinations and routing are configured according to Port-Write Formats, Programming Model, and Generation.			
2. Discard all packets sent to the HS-LP.	Configure routing tables to discard packets sent to this port, as described in Packet Routing. This should stop packets from accumulating in the Final Buffer.			
3. Discard all packets received from the HS-LP.	Configure the port's routing table to discard all packets received by this port, as described in Packet Routing. This should stop requests from being issued by the HS-LP.			

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Table 8: Preparation For Hot Extraction on Port Y *(Continued)*

Step	Register	Offset	Mask and Value	Description
4. Do not accept packets from the HS-LP.	Port {0..17} Control 1 CSR	0x15C + (0x20*Y)	0xXXXXXXXF	Ensure PORT_LOCKOUT, STOP_ON_PORT_FAIL_ENC_EN, and DROP_PKT_EN are set. Note: Responses may be in flight to/from the HS-LP at this point.
	Device Control 1 Register	0xF2000C	0x0XXXXXXX	Ensure that the FATAL_ERR_PKT_MGT bit is cleared. Packets sent to the HS-LP will be discarded due to the port error detected.

At this point, removing or resetting the link partner will result in an OUTPUT_FAIL and/or FATAL_ERR_PKT_MGT condition. This will cause any packets in the final buffer of the CPS-1848 port connected to the HS-LP to be discarded.



To guarantee that all packets associated with the HS-LP have been discarded, it is necessary to wait for the Time-to-Live (TTL) timeout period before allowing the HS-LP back in to the system. The TTL value is programmed using Packet Time to Live CSR.TTL.



Packets associated with the HS-LP may have been discarded by the actions taken above. For deterministic operation, IDT recommends that the HS-LP is reset.

A port-write or interrupt indicating an OUTPUT_FAIL or PORT_ERR standard event acts as confirmation that the HS-LP has been removed or reset. Once this confirmation is received, the system can prepare the CPS-1848 port to bring the HS-LP back into the system.

Port preparation consists of the following:

1. Clearing all error conditions on the port
2. Continuing to isolate the HS-LP from the remainder of the system
3. Receiving notification when the HS-LP has reappeared

Isolation of the HS-LP and notification of HS-LP reappearance are only necessary when it is the responsibility of system software, not the HS-LP, to bring the HS-LP back into the system.

Table 9: Preparation For Hot Insertion on Port Y

Step	Register	Offset	Value	Description
1. Clear all error conditions on Port Y.	Device Reset and Control Register	0xF20300	0x8000YYYY	Perform a per-port reset on port Y to clear errors. Note that “YYYY” in the Value column is a vector with bit “Y” set.
	Ensure Port {0..17} Implementation Specific Error Detect Register.PORT_INIT bit is not set due to the hot extraction. If it is set, write a 0 to clear it.			

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Table 9: Preparation For Hot Insertion on Port Y *(Continued)*

Step	Register	Offset	Value	Description
2. Isolate the HS-LP from the remainder of the system.	Configure the port's routing table to discard all packets received by this port, as described in Packet Routing. This should stop requests from being issued by the HS-LP.			
	Configure the device's routing table to discard all packets sent to this port, as described in Packet Routing. This should stop requests from being issued to the HS-LP.			
	Port {0..17} Control 1 CSR	0x15C + (0x20*Y)	0xXXXXXXXF	Ensure PORT_LOCKOUT, STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN are set. Note: There may be responses in flight to and from the HS-LP at this point. For more information on when STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN are set, see Event Isolation.
3. Configure event management for notification.	Port {0..17} Error Report Enable Register	0x31044 + (0x40*Y)	0x80000000	Enable reporting for implementation-specific errors.
	Port {0..17} Implementation Specific Error Report Enable Register	0x3104C + (0x40*Y)	0x00000020	Ensure that the PORT_INIT_EN event is enabled. This indicates when the port has successfully trained. Note: No other error events will be reported by the port until the port has initialized.
	Port {0..17} Operations Register	F40004 + (0x100*Y)	0x10000000 (PORT_INT_EN) or 0x08000000 (PORT_PW_EN)	Ensure at least one of PORT_INT_EN or PORT_PW_EN is set to ensure notification occurs.
	If port-writes are used, ensure that port-write destinations and routing are configured according to Port-Write Formats, Programming Model, and Generation.			

2.8.2.1 Unexpected Extraction

In systems that do not have central control software, or those that allow the removal of components without prior coordination with the system, it is by definition not possible to perform the steps in Controlled Removal/Reset. It is only possible to recover the system after a component is removed.

This recovery process consists of the following considerations:

1. All packets destined for the removed component must be discarded automatically.
2. The remaining components of the system may need to be informed that the component has been removed.
3. The link may need to be prepared for the HS-LP to bring itself back into the system.

Automatic discard of packets destined for a failed port uses a method similar to that described in Controlled Removal/Reset.



An unexpected extraction cannot be distinguished from link re-initialization. This implies that if a link re-initializes, the system will react as if the link partner has been removed and re-inserted.

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Informing the remaining components in the system of the HS-LP's extraction can be completed by multicasting a port-write, or through a shared interrupt.

Table 10: Preparation of Port That Can be Subjected to Unexpected Hot Extraction Event

Step	Register	Offset	Value	Description
1. Enable event notification.	Port {0..17} Error Rate CSR	0x1068 + (0x40*Y)	0x00000000	Disable error rate bias, clear error rate counter.
	Port {0..17} Error Rate Threshold CSR	0x106C + (0x40*Y)	0x01000000	Set error rate threshold to detect an OUTPUT_FAIL condition (Port {0..17} Error and Status CSR) if one or more errors occur.
	Lane {0..47} Error Rate Enable Register	0xFF8010 + (0x100 * lane_num)	0x00000003	Enable error reporting for loss of lane ready and loss of lane sync events. Repeat for each lane associated with the port.
	Port {0..17} Control 1 CSR	0x00015C + (0x20*Y)	0xXXXXXXXC	Set STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN bits to prevent congestion when the link partner is removed.
	Port {0..17} Operations Register	F40004 + (0x100*Y)	0x10000000 (PORT_INT_EN) or 0x08000000 (PORT_PW_EN)	Ensure at least one of PORT_INT_EN or PORT_PW_EN is set to ensure notification occurs.
	Port {0..17} Error Report Enable Register	0x031044 + (0x40*Y)	0x80000000	Enable port-writes and interrupt notification for the Hot Extraction events.
	Port {0..17} Implementation Specific Error Report Enable Register	0x03104C + (0x40*Y)	0x80000000	Disable all error reporting except ERR_RATE_EN bit. The default is all bits are enabled in the register; however, this setup can trigger an unexpected event.
	If port-writes are used, ensure that port-write destinations and routing are configured according to Port-Write Formats, Programming Model, and Generation.			

After a surprise extraction, if system software is responsible for bringing a new link partner into the system, the steps described in Table 8 and Table 9 should be performed to ensure that all packets in flight to/from the HS-LP are discarded, and that system software is informed when the HS-LP reappears in the system.

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2.8.3 Link Partner Insertion

Similar to extraction, the steps required to deal with insertion of a link partner depend on whether system software is responsible for allowing the HS-LP into the system, or if the HS-LP is responsible for bringing itself into the system. In general, the entity responsible for bringing the HS-LP into the system is called the Recovery Controller.

Once the HS-LP has been inserted, the ability to transfer maintenance packets must be re-established as a first step toward the HS-LP's participation in the system. The extraction of an HS-LP usually causes multiple errors to be detected. By design, these errors include link communication failure and can include packet discard. These errors can prevent the transfer of maintenance packets. To establish maintenance packet transfer, it is necessary to achieve the following two objectives:

1. Clear error conditions on the link, which may have occurred during hot insertion
2. Ensure ackID synchronization between the HS-LP and the link partner

The procedure for clearing error conditions and synchronizing ackIDs depends on whether the HS-LP or another node in the system is the Recovery Controller, and the specific link configuration. Common scenarios involving the CPS-1848 are described in the following sections. Application notes for hot extraction/hot insertion of other devices are also available from www.idt.com.

Once maintenance packets can be exchanged, the Recovery Controller can then do the following:

1. Undo whatever preparation was done due to a controlled extraction
2. Clear any other error conditions associated with an uncontrolled extraction
3. Bring the HS-LP back into the system

These steps are system specific, and so are not described here.

2.8.3.1 System Controlled Recovery

The procedure described in Table 11 assumes that the steps captured in Table 8 and Table 9 were performed, whether the extraction was controlled or uncontrolled.



The steps in Table 9 should be performed for all ports that do not have link partners when the system is powered up, but which could have link partners inserted on them while the system is operating.



When the Recovery Controller resides on the CPS-1848 side of the link connected to the HS-LP, it is assumed that the HS-LP has been reset. To guarantee that this is the case, IDT recommends that the Recovery Controller reset the HS-LP as part of this procedure. This ensures consistent starting conditions if the link initialization was not the result of a hot-swap event.

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Table 11: System Recovery Controller Operation, HS-LP on Port Y

Step	Register	Offset	Value	Description
1. Establish routing to/from the HS-LP.	Configure routing tables to allow maintenance access to CPS-1848 port and the HS-LP. The procedures are described in Packet Routing.			
2. Disable event notification and isolation functions.	Port {0..17} Error Rate Enable CSR	0x1044 + (0x40*Y)	0x00000000	Disable all events
	Port {0..17} Error Rate Threshold CSR	0x106C + (0x40*Y)	0x00000000	Disable OUTPUT_FAIL condition on implementation specific event (see Port {0..17} Error and Status CSR).
	Lane {0..47} Error Rate Enable Register	0xFF8010 + (0x100 * lane_num)	0x00000000	Disable error reporting. Repeat for each lane associated with the port.
	Port {0..17} Control 1 CSR	0x15C + (0x20*port_num)	Value is port specific	Ensure PORT_LOCKOUT, STOP_ON_PORT_FAIL_ENC_EN, and DROP_ENABLE are cleared.
3. Reset the HS-LP and CPS-1848 port Y simultaneously.	Port {0..17} Local ackID CSR	0x140 + (0x20*Y)	0x80000000	Clear outstanding packets, and clear ackIDs to 0.
	Port {0..17} Link Maintenance Request CSR	0x140 + (0x20*Y)	0x00000003	Issue a “reset” request to the HS-LP. This register can be written more than once to ensure that the link partner receives a valid reset request.
	Port {0..17} Link Maintenance Response CSR	0x144 + (0x20*Y)	Read	Confirm that the reset request has been sent.
	Device Reset and Control Register	0xF20300	0x8000YYYY	Perform a per-port reset on port Y to clear errors. Note: This step should be performed immediately after resetting the HS-LP to clear error conditions at both ends of the link simultaneously.
	Port {0..17} Link Maintenance Request CSR	0x140 + (0x20*Y)	0x00000004	Issue a Link Request/Input Status request to the HS-LP. This will clear a PORT_ERR failure on the CPS-1848 port, if it exists, and allow packets to be sent.

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2.8.3.2 HS-LP Controlled Recovery

If the HS-LP is the Recovery Controller then recovery of the link requires the procedure in Table 12 to be completed. Note that the procedure assumes that the HS-LP is another CPS-1848, or a device with a compatible programming model. If the HS-LP is not a CPS-1848 then HS-LP implementation-specific register accesses may be necessary. Register references made with address computations are for the CPS-1848. Register references made without address computations are for the HS-LP.

The procedure in Table 12 assumes that both the HS-LP and the CPS-1848 are connected using a cable. This implies that each end of the new link could have exchanged packets with different link partners prior to connecting the cable.

The HS-LP port must support the Software Assisted Error Recovery version of the LP-Serial Extended Feature Block to successfully resume packet exchange on the link.

Table 12: HS-LP Recovery Controller

Step	Register	Offset	Value	Description
1. Clear ackIDs and reinitialize HS-LP (Local) port.	Device Reset and Control Register or Implementation Specific	0xF20300 HS-LP (Local)	0x8000YYYY or Implementation Specific	Reset HS-LP (Local) port n. If the HS-LP (Local) is not a CPS-1848 (Remote), the register address and value written are implementation specific.
2. Disable and clear error conditions that prevent transmission of link requests by the HS-LP (Local).	Port {0..17} Error Rate Enable CSR	0x1044 + (0x40*Y) HS-LP (Local)	0x00000000	Disable all events.
	Port {0..17} Error Rate Threshold CSR	0x106C + (0x40*Y) HS-LP (Local)	0x00000000	Disable OUTPUT_FAIL condition on implementation specific event (see Port {0..17} Error and Status CSR).
	Port {0..17} Error Rate CSR	0x1068 + (0x40*Y) HS-LP (Local)	0x00000000	Clear ERR_RATE_CNTR value.
	Lane {0..47} Error Rate Enable Register	0xFF8010 + (0x100 * lane_num) HS-LP (Local)	0x00000000	Disable error reporting. Repeat for each lane associated with the port.
	Port {0..17} Error and Status CSR	0x000158 + (0x20*Y) HS-LP (Local)	0x07000000	Clear OUTPUT_DROP, OUTPUT_FAIL, and OUTPUT_DEGR.
3. Reset HS-LP (Local) and CPS-1848 (Remote) to clear link errors.	Port {0..17} Link Maintenance Request CSR	0x000140 + (0x20*Y) HS-LP (Local)	0x00000003	Issue a “reset” request to the CPS-1848. Note: The CPS-1848 must have Device Control 1 Register.PORT_RST_CTL set to 1 to perform per-port resets.
	Device Reset and Control Register or Implementation Specific	0xF20300 HS-LP (Local)	0x8000YYYY or Implementation Specific	Reset HS-LP (Local) port n. Register values are given assuming that the HS-LP (Local) is a CPS-1848 (Remote). If the HS-LP (Local) is not a CPS-1848 (Remote), the register address and value written are implementation specific. Note: This step should be performed immediately after resetting the CPS-1848 (Remote) to clear error conditions at both ends of the link simultaneously.

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Table 12: HS-LP Recovery Controller *(Continued)*

Step	Register	Offset	Value	Description
4. HS-LP (Local) clears potential input-error stopped state on the CPS-1848 (Remote).	Port {0..17} Link Maintenance Request CSR	0x000140 + (0x20 * Y) HS-LP (Local)	0x00000004	After reset, the CPS-1848 (Remote) may be in the input-error stopped state. Issue an "input-status" request to the CPS-1848 (Remote).
5. Check for error conditions.	Device Identity CAR	0x000000 CPS-1848 (Remote)	Read	Read the Device Identity CAR of the CPS-1848. If the read completes successfully then packet exchange can resume. Note: If the CPS-1848 always experiences a PORT_ERR condition on extraction, do not perform this step.
6. If the CPS-1848 (Remote) port is known, clear ackIDs.	Port {0..17} Local ackID CSR	0x000148 + (0x20 * Y) CPS-1848 (Remote)	0x80000000	Clear ackIDs on the CPS-1848 (Remote) port.
If the CPS-1848 (Remote) port is *not* known, skip step 6 and proceed to step 7.	Device Reset and Control Register or Implementation Specific	0xF20300 HS-LP (Local)	0x8000YYYY or Implementation Specific	Reset HS-LP (Local) port n. Register values are given assuming that the HS-LP (Local) is a CPS-1848 (Remote). If the HS-LP (Local) is not a CPS-1848 (Remote), the register address and value written are implementation specific.
	Port {0..17} Link Maintenance Request CSR	0x000140 + (0x20 * Y) HS-LP (Local)	0x00000003	Issue a "reset" request to the CPS-1848 (Remote). Note: The CPS-1848 (Remote) must have Device Control 1 Register.PORT_RST_CTL set to 1 to perform per-port resets.
	Packet exchange can resume once the link has completed initialization. Clear error status bits on HS-LP (Local) and CPS-1848 (Remote).			

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Table 12: HS-LP Recovery Controller *(Continued)*

Step	Register	Offset	Value	Description

7. If the CPS-1848 (Remote) port is not known, resynchronize ackIDs.	For each CPS-1848 (Remote) port that the HS-LP (Local) can be connected to {
	For ackID from 0 up to N (where N is 31 for IDLE1 and 63 for IDLE2) {
	Write ackID to HS-LP (Local) Port {0..17} Local ackID CSR.INBOUND while retaining outstanding/outbound values.
	Write 0x4 to CPS-1848 (Remote) Port {0..17} Link Maintenance Request CSR.CMD
	Read HS-LP (Local) Port {0..17} Local ackID CSR.INBOUND
	If INBOUND <> ackID
	Exit both loops, ackID resynchronization complete.
	}
	}			

	Port {0..17} Local ackID CSR	0x00148 + (0x20*Y) HS-LP (Local)	0x0000YYYY	Clear HS-LP (Local) inbound ackID while retaining existing outstanding/outbound ackID.
	Port {0..17} Local ackID CSR	0x00148 + (0x20*Y) CPS-1848 (Remote)	0x81000000	Clear outstanding/outbound ackID on CPS-1848 (Remote) and set inbound ackID to 0x01.
	Port {0..17} Local ackID CSR	0x00148 + (0x20*Y) HS-LP (Local)	0x80000000	Clear own ackID.
	Port {0..17} Link Maintenance Request CSR	0x00140 + (0x20*Y) HS-LP (Local)	0x00000003	Issue a “reset” request to the CPS-1848 (Remote).
	Device Reset and Control Register or Implementation Specific	0xF20300 HS-LP (Local)	0x8000YYYY or Implementation Specific	Reset HS-LP (Local) port n. Register values are given assuming that the HS-LP (Local) is a CPS-1848 (Remote). If the HS-LP (Local) is not a CPS-1848 (Remote), the register address and value written are implementation specific.
	Clear error status bits on HS-LP (Local) and CPS-1848 (Remote). Packet exchange can now resume.			

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2.9 Packet Trace and Filtering

2.9.1 Packet Trace

Each S-RIO port can compare a received packet against a set of configurable predefined values, and, if a match occurs, include a reference to a configurable output port as part of its forwarding information passed to the switch fabric. This function is defined as the “Trace” function. When all bits of the packet data match corresponding bits in a specific programmable value (after the value’s mask has been applied), the Trace Criteria is met and a copy of the packet is forwarded to the trace enabled output port.

Each S-RIO port provides output port routing references derived from a received packet's destID (including multicast references), as well as a routing reference to the configured trace port to the switch fabric. Each S-RIO port also provides a uniquely configurable trace function so that trace can be enabled on up to 18 ports simultaneously. To enable the trace function, set TRACE_EN to 1 in the Device Control 1 Register.

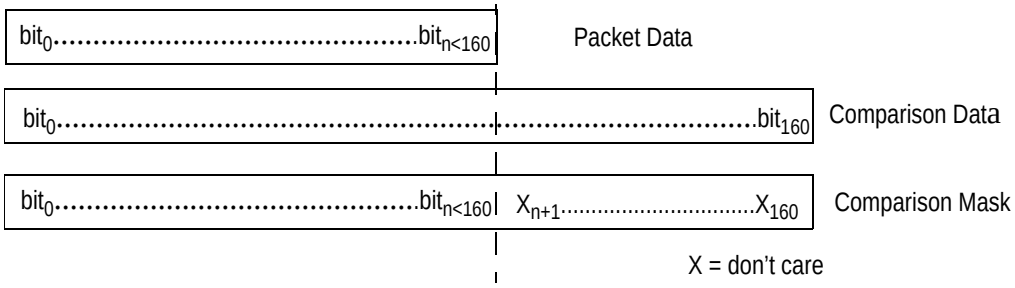
2.9.1.1 Trace Criteria

The property of an S-RIO port matching a packet with a “Trace Criteria” refers to a successful comparison of the first 160 bits in a received packet to multiple pre-programmed values stored at that port. A successful match against a Trace Criteria will trigger the S-RIO port to flag the trace port (to the switch fabric) for packet forwarding.

Each S-RIO port provides a set of four uniquely configurable 160-bit comparison values that can selectively be applied using a bit mask to the first 160 bits of each packet that the block receives. Each S-RIO port also provides a bit mask for each of the four programmable 160-bit comparison values that define which of the first 160 bits of packet data are relevant to the comparison. A value of 1 in the comparison value mask indicates that the corresponding bits in the programmed value and the corresponding bit in the packet data is compared. A value of 0 in the comparison value mask is used as a “don’t care”. A don’t care value will result in an automatic match of the corresponding bits in the programmable value with the corresponding packet data bits. When all bits of the packet data match with a corresponding bit in a specific programmable value (after the value’s mask has been applied) the Trace Criteria has been met and a copy of the packet is forwarded to the trace enabled output port. The packet trace is triggered by a logical “OR” of the comparison match results (packet data with the four programmable values) such that if at least one match occurs, packet forwarding to the trace enabled port is enabled.

Note that the trace criteria is based on the entire contents of the comparison value and its corresponding bit mask. If the number of bits in the packet being compared is less than 160 bits, the excess bits in the mask must be set as “don't care,” as displayed in Figure 8.

Figure 8: Trace Criteria



The Trace Criteria architecture is displayed in Figure 9.

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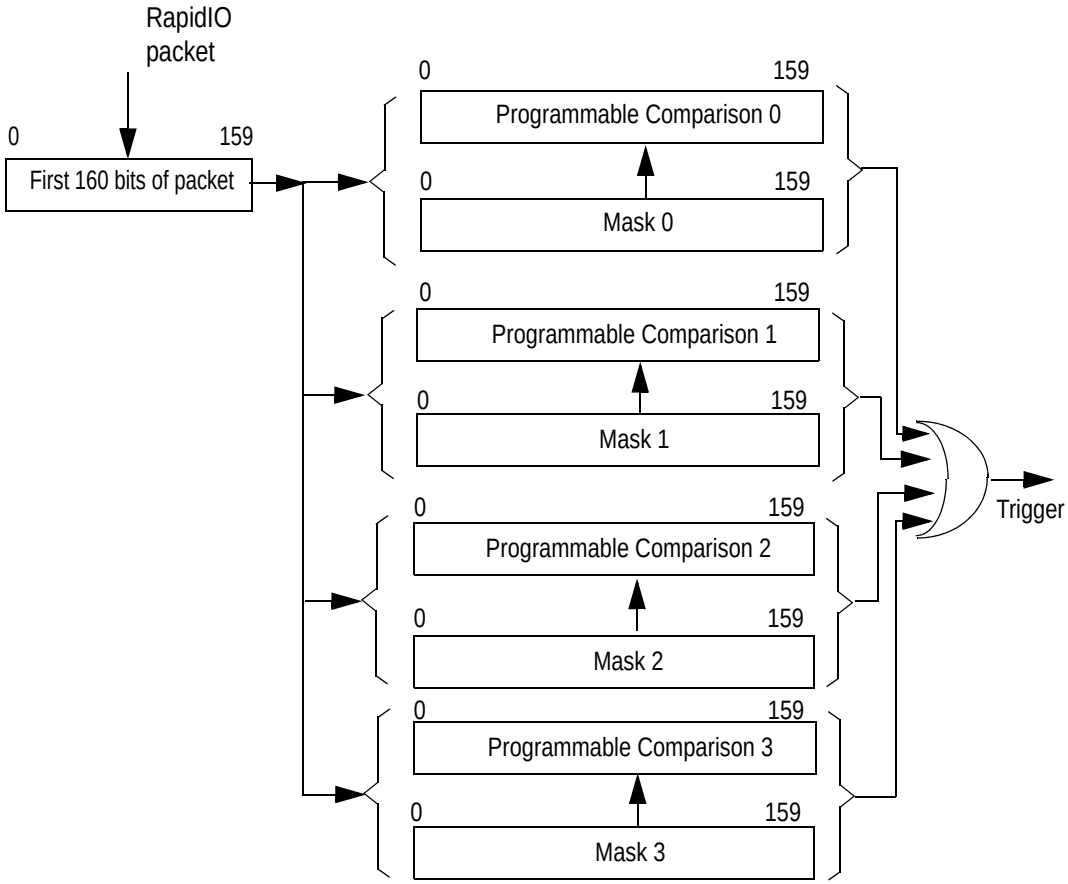
Figure 9: Trace Function within a Port



From an application perspective, the support for comparison over the first 160 bits of the packet is to ensure that the trace function can cover the largest RapidIO header (including those using extended addressing) plus at least the first 32 bits of the payload. This implementation is flexible across the first 160 bits of the packet and ensures that the following parameters (among others) can be used as trace criteria:

- The header's ftype field (4 bits)
- The header's destID field (8 or 16 bits)
- The header's mbox field (up to 8 bits)
- The first 32 bits of the packet payload (32 bits)

If an S-RIO port detects an error in a received packet, the packet will not be forwarded to the trace port; however, it can still be reported as a trace match.

2.9.1.2 Trace Port Features

Each S-RIO port supports a trace port functionality. The user can define which output port is enabled for the Trace function. For a specific device, all packets that match the Trace criteria from all trace-enabled inputs are routed to the same configured, trace-enabled output port.

Note that the device supports configurations where the trace port and the output port referenced by a received packet are defined to be the same port. In the case where there is a trace match and the packet's destID references the output port configured as the trace port, the packet will be forwarded only once regardless of the packet type.

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2.9.1.3 Trace Routing Features

Each S-RIO port supports two operation modes for the trace routing function:

- Default Trace Routing – Device Control 1 Register.TRACE_OUTPUT_PORT_MODE = 0
- Optional Trace Routing – Device Control 1 Register.TRACE_OUTPUT_PORT_MODE = 1

2.9.1.3.1 Default Trace Routing Mode

In default mode, the trace enabled S-RIO port accepts RapidIO traffic (referenced by the received packet's destID field) as well as traffic that matches the trace criteria of all ports. Trace-triggered packets are handled by the trace-enabled output port in the same way as it handles all other packets. Normal RapidIO priority and flow control rules apply.

2.9.1.3.2 Optional Trace Routing Mode

In optional mode, only packets that have matched a port's trace criteria are routed to the trace port. A received packet that does not match the Trace Criteria, but whose destID field references the trace enabled output port will not be forwarded to the trace port. If this packet has a destID that references a multicast operation that includes the trace port, the packet is forwarded to all ports except for the trace enabled port. A packet that does not match a port's trace criteria whose destID only references the trace port is handled as an error packet and is dropped. Trace-triggered packets are handled by the trace-enabled output port in the same way as it handles all other packets. Normal RapidIO priority and flow control rules apply.

A user can configure the trace port into "trace only" mode, and at the same time configure the port's route table to allow packets to be routed to the trace port (including packets that do not match the trace criteria). With this configuration, packets received by a port that are to be routed to the trace port (as defined by that port's route table) will be dropped by the device if they do not match the trace criteria. Packets in this scenario that match the trace criteria are forwarded.

2.9.1.3.3 Maintenance Packets with Enabled Trace Ports

Type 8 packets are handled in the same way as all other packets for both Trace Routing Modes defined above. Type 8 packets that are received at a trace-enabled input port that have a hop count of 0 are forwarded to the trace port if the trace criteria at that port is met.



For Revision C, a Maintenance packet with a hop count greater than 0 is forwarded to the destination port(s) with its hop count decremented by 1. The same packet (with its hop count decremented by 1) is also forwarded to a trace port if trace criteria is matched.

For Revision A/B, a Maintenance packet with a hop count greater than 0 is forwarded to a trace port if trace criteria is matched, however, its hop count remains unchanged. The same packet (with its hop count now decremented by 1) is forwarded to the destination port(s).

2.9.1.3.4 No Route Conditions

Packets that meet the trace criteria are routed to the trace port even if the packet destID reference in the port's route table indicates "no route".

2.9.1.3.5 Trace Function Dynamic Programmability

By offering dynamic programmability, each S-RIO port can modify trace function parameters without disabling the normal operation of the port functionality. The dynamic programmability of the trace function allows the user to do the following additional tasks:

- To enable/disable the trace function on an input port by input port basis
- To assign the trace function to any single output port
- To change the packet trace comparison values of any port. Note that the packet trace function at the port must be disabled to make this change
- To enable/disable any/all trace comparison values of any port

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The user can change a comparison value or mask (same value) for all ports with a write to a single address. The device provides an individual enable/disable feature for each comparison value for each port (four values for each of the 18 ports). To change a comparison value the user must first disable the value for use as a comparison. The user can then change the value and then re-enable it. While this value is being changed, the port can receive normal traffic and will continue to trace on the other three values (if enabled).

Note that to change the trace port definition, the trace function must be disabled globally (all values of all ports). Broadcast trace enable/disable requires a write to only a single address.

2.9.1.3.6 *Alert on Trace Match*

Each S-RIO port can generate and transmit a port-write maintenance packet when a received packet meets the Trace criteria of any port. The ability to activate and deactivate this function dynamically is provided on a per-port basis. If enabled, once the device sends a port-write because of a trace match, it will temporarily disable sending port-writes on subsequent trace matches until it receives a maintenance write command to re-enable the ability to do so. This functionality is accessible through the Port {0..17} Trace Port-Write Reset Register. This is to prevent a flood of port-writes to the system-level maintenance processor if a large number of packets is received that match the trace criteria. Note that this disable on trace matches will not affect the generation of port-writes for any other reason.

The STOP_EM bit of the Error Log Control 2 Register disables all IDT maintenance packet port-writes generated by the device. This bit also applies to port-writes that are generated as a result of trace matches. Trace match based port-writes are enabled via TRACE_PW_EN in the Port {0..17} Operations Register. Standard port-write packet generation is not affected by this bit.

Each S-RIO port supports a set of counters that increment each time the port receives a packet that matches the Trace criteria. Each S-RIO port supports a counter for each of the four comparison values. These counters are accessible in the same way that all other device counters are made accessible. All trace counters are 32 bits.



Packets that are retried or stomped may still match the trace and/or filter criteria. The associated trace and filter counters will increment for retried or stomped packets. To limit this impact, use transmitter-controlled flow control (see Transmitter- and Receiver-Controlled Flow Control Programming Model).



If a packet can match multiple trace S-RIO ports, only the counter(s) that are associated with the first completed match or matches are incremented. A match is completed when the remainder of a packet is compared against zero values in the Port x Trace y Mask z Registers. If multiple matches complete at the same time, only those counters will increment.

2.9.1.3.7 *Flow Control with Trace Enabled*

Each S-RIO port supports S-RIO-defined receiver- and transmitter-controlled flow control when Trace is enabled. If buffer contention exists at the trace port such that packets which reference the trace port cannot be received, then the packet will not be received into the switch Input Buffer and an appropriate request for retransmission of the packet is transmitted to the link partner.

2.9.1.3.8 *Errored Packets*

Each S-RIO port does not support packet trace for packets that are not acknowledged or are retried at the physical layer, such as packets with CRC errors and packets that are longer than 276 bytes. Each port supports trace for packets with logical errors (for example, invalid type, or Maintenance packets that are longer than 20 words) as long as they match the trace criteria. Trace matching continues, however, regardless of the port's error state.

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2.9.1.3.9 *Trace Configuration*

The Trace function is enabled globally at the device level for all S-RIO ports by setting TRACE_EN to 1 in the Device Control 1 Register. When broadcast trace is enabled the Trace Output Port (TRACE_OUT_PORT) defined in the Device Control 1 Register is enabled. This register also controls the mode of the Trace Output Port (TRACE_OUT_PORT_MODE), as default or trace only.

Each S-RIO port supports an enable of each of its four trace criteria values, TRACE_n_EN, in its respective Port {0..17} Operations Register. This is independent such that a match on any specific value does not depend on a match of any other value. The Port {0..17} Operations Register also controls whether or not a packet that matches a port's trace criteria will cause the device to generate a port-write packet.

2.9.1.3.10 *Cut-Through Forward with Trace*

Each S-RIO port supports Cut-Through forwarding when Trace is enabled if configured to do so.

2.9.2 Packet Filtering

Along with the ability to trace packets using comparisons against up to four comparison values, each S-RIO port can filter packets based on comparisons against these same values. If this packet filtering is enabled, a successful comparison of the first 160 bits in a received packet to a port's pre-programmed values will cause the device to drop or "filter" the packet. A successful comparison also prevents an S-RIO port from "accepting/processing" a maintenance packet (if a maintenance packet that met the filter criteria had a hop count of 0).

Each S-RIO port can filter packets to be enabled/disabled for each unique comparison value at that port.

Each S-RIO port can enable/disable packet trace and packet filtering simultaneously for each unique comparison value. If both packet filtering and packet trace are enabled and a match occurs between a received packet and a comparison value, then the packet will be dropped but will also be traced to the specified trace port. If packet filtering is enabled but trace is not, then the packet is filtered and not traced to the specified trace port.

The device provides a counter at each port for each comparison value which provides a continuous count of the number of packets that were filtered at each port as a result of a successful match against each comparison value.



Packets that are retried or stomped may still match the trace and/or filter criteria. The associated trace and filter counters will increment for retried or stomped packets. To limit this impact, use transmitter-controlled flow control (see Transmitter- and Receiver-Controlled Flow Control Programming Model).

2.10 Packet Generation and Capture

The CPS-1848 supports a special test mode called Packet Generation and Capture (PGC) that enables initial system debug and integration. PGC mode allows users to generate one or more packets, route those packets through the switch to a connected device, and to capture up to 25 response packets received for that request. This mode can issue maintenance read and write packets to verify connectivity to other endpoints and switches in a system before software is available. It can also test a system's reaction to incorrectly formed request or response packets.

PGC mode is normally controlled using debug tools connected directly to the CPS-1848's I2C or JTAG interfaces when no other control entity exists in the system. It is also possible to use PGC mode during the normal operation of a system.



PGC mode requires the resources of two RapidIO ports on the device. These ports cannot be used for any other purpose when PGC mode is active.

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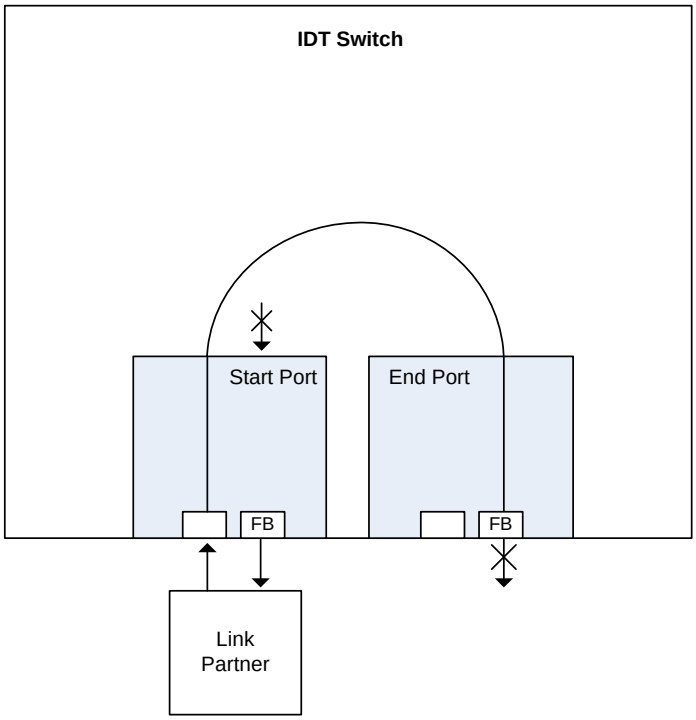
2.10.1 Packet Generation and Capture Mode Overview

PGC mode requires two spare ports: a Start Port and an End Port. A request packet is composed in the Final Buffer (FB) of the Start Port, and then sent. The request packet can be transmitted directly to the desired link partner, or looped back through a cable external to the SerDes lane(s) allocated to the Start Port. Packets received in the Input Buffer on the Start Port are routed according to the routing table settings for that port. If a response packet is expected, the response packet can be routed to the End Port, where the response packet is captured in the Final Buffer. The response packet can then be read out.

The Start Port and End Port must be in a PORT_OK status condition in order for packet generation and capture to operate. PORT_OK status can be achieved by connecting to a link partner or by connecting the port's TX lanes to its RX lanes.

There are two scenarios for the use of PGC mode. The first sends a packet directly to the link partner connected to the Start Port, as displayed in Figure 10. The response is received by the Start Port, and routed to the End Port.

Figure 10: System Connectivity Test in PGC Mode – Transmitted Directly to Link Partner



In the second scenario, the Start Port is put into loopback mode so that the packet can be sent to any other switch port, as displayed in Figure 11 (see also Port Loopback Mode). The response packet from the link partner is then routed to the End Port.

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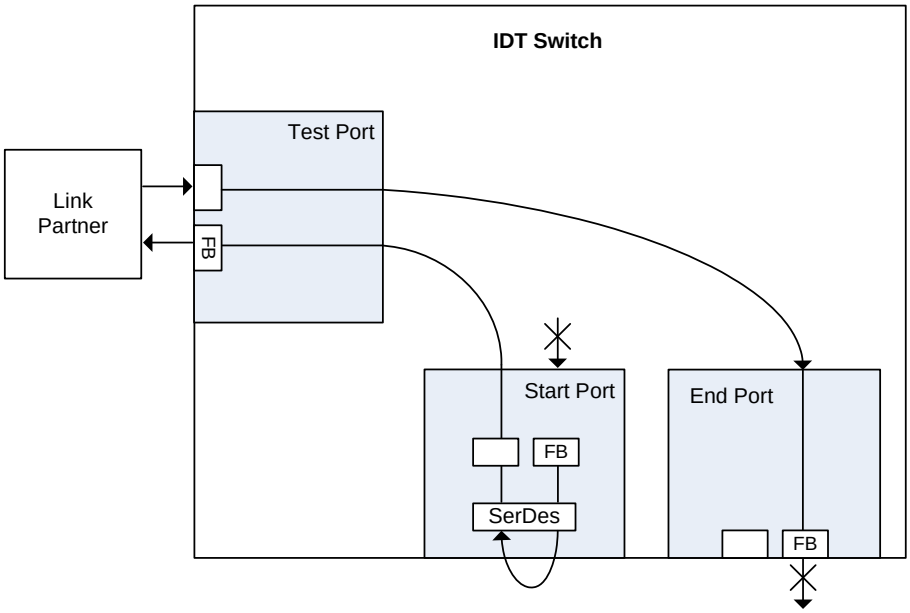
Figure 11: System Testing using PGC Mode – Cabled Loopback through SerDes



2.10.2 Packet Generation and Capture Mode Programming Model

The following example describes how to use PGC mode to perform a system connectivity test with a link partner. A single maintenance read packet is sent to the link partner from port 3, and the maintenance read response packet is read out of port 4. The destID for the link partner is 0xAA, and the destID for the response is 0xBB.

The Start Port and End Port must be in a PORT_OK status condition in order for packet generation and capture to operate. PORT_OK status can be achieved by connecting to a link partner or by connecting the port's TX lanes to its RX lanes.

Table 13: PGC Mode Example – Connectivity Test

Step	Register	Offset	Value	Description
1. Configure routing	Port {0..17} Device Route Table Register {0..255}	0xE132EC	0x00000004	Route destID 0xBB to End port 4.
2. Configure PGC mode	Device Control 1 Register	0xF2000C	0x1XXXXXXX	Set PGC Mode Enable bit.
	Port {0..17} Packet Generation and Capture Mode Configuration Register	0x100140	0x00002004	Configure port 4 as the End port. The End port will capture packets for priority 1 packets with the CRF bit set.
	Port {0..17} Packet Generation and Capture Mode Configuration Register	0x100130	0x00001001	Configure port 3 as the Start port. The Start port will send packets as if they were priority 0 with the CRF bit set.

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Table 13: PGC Mode Example – Connectivity Test *(Continued)*

Step	Register	Offset	Value	Description
3. Write maintenance read packet into Start port buffer	Port {0..17} Packet Generation and Capture Mode Data Register	0x100134	0x0008AABB	Bytes 0–3 of Maintenance Read.
	-	0x100130	0x00005401	Enable write access to Final Buffer, and set SOP for first data of maintenance packet at priority 0.
	-	0x100134	0x08000100	Bytes 4–7 of Maintenance Read
	-	0x100130	0x00005001	Clear SOP for remaining data writes
	-	0x100134	0x00001DFE	Bytes 8–11 of Maintenance Read
	-	0x100130	0x00005801	Set EOP for last data write
			0x00001000	Clear EOP, and disable write access to Final Buffer
4. Transfer packets	-	0x100130	0x00011000	Start packet transfer
	-	0x100140	Read	Check that RX_DONE bit (0x00008000) is set before continuing. Note: 0x00006004 must be written to offset 0x100140 before each read from offset 0x100144.

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Table 13: PGC Mode Example – Connectivity Test *(Continued)*

Step	Register	Offset	Value	Description
5. Read out maintenance read response	Port {0..17} Packet Generation and Capture Mode Configuration Register	0x100140	0x00006004	Enable read access to final buffer priority 1 queue.
	Port {0..17} Packet Generation and Capture Mode Data Register	0x100144	Read 0x0048BBAA	Bytes 0–3 of Maintenance Read Response
	-	0x100140	Read	Check that SOP bit is set.
			0x00006004	Enable read access to final buffer priority 1 queue.
	-	0x100144	Read 0x2000FE00	Bytes 4–7 of Maintenance Read Response
	-	0x100140	Read	Check that SOP and EOP bits are 0.
		0x100140	0x00006004	Enable read access to final buffer priority 1 queue.
	-	0x100144	Read 0x0000XXXX	Bytes 8–11 of Maintenance Read Response, where XXXX is the most significant 2 bytes of the link partners Device Identity CAR
	-	0x100140	Read	Check that SOP and EOP bits are 0.
			0x00006004	Enable read access to final buffer priority 1 queue.
	-	0x100144	Read 0xXXXX0000	Bytes 12–15 of Maintenance Read Response, where XXXX is the least significant 2 bytes of the link partners Device Identity CAR.
	-	0x100140	Read	Check that SOP and EOP bits are 0.
			0x00006004	Enable read access to final buffer priority 1 queue.
	-	0x100144	Read 0x0000XXXX	Bytes 16–19 of Maintenance Read Response, where XXXX is the CRC for the response packet.
	-	0x100140	Read	Check that SOP is 0, and EOP bit is 1.
			0x00006004	Enable read access to final buffer priority 1 queue.

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The Start Port can revert to normal operation without resetting the CPS-1848. The End Port, however, cannot revert to normal operation until a software or hardware device reset. The End Port can receive only the first 25 packets.

2.11 Packet Transfer Validation and Debug

2.11.1 Overview

The performance counter registers that are described in the following sections should be the first tool to use when validating and debugging the transfer of packets.

Except for the counters captured below, all other counters are “informational only” and should not be relied on to be completely accurate or consistent.

2.11.1.1 Receive Port Counters

For a stream of receive packets, assuming Packet Accepted has been sent for all received packets, no new packets have been received, and no error recovery has occurred, the following relationship exists:

- Port {0..17} VC0 Acknowledgements Transmitted Counter Register = Port {0..17} VC0 Received Packets Dropped Counter Register + Port {0..17} VC0 Packets Received Counter Register
- Port {0..17} VC0 Packets Received Counter Register – Increments when EOP is detected, and the packet is not retried, not dropped due to no-route, and not invalid (bad TTYPE, maintenance packet too long).
- Port {0..17} VC0 Received Packets Dropped Counter Register – Increments when a packet is dropped due to no-route and/or invalid TT field is detected.
- Port {0..17} VC0 Acknowledgements Transmitted Counter Register – Increments when packet-accepted CS is sent.
- Port {0..17} Not Acknowledgements Transmitted Counter Register – Increments when packet-not-accepted CS is sent. No relation to other counters (NACK’d packets are not counted as received or dropped).
- Port {0..17} VC0 Retry Symbols Transmitted Counter Register – Increments when a retry CS is sent. No relation to other counters (retried packets are not counted as received nor dropped).

2.11.1.2 Transmit Port Counters

For a stream of transmit packets, assuming all outstanding packet acknowledgments (PA, NACK, RTRY) have been received, and no error recovery occurs, the following relationship exists:

- Port {0..17} VC0 Packets Transmitted Counter Register = Port {0..17} VC0 Acknowledgements Received Counter Register + Port {0..17} Not Acknowledgements Received Counter Register + Port {0..17} VC0 Retry Symbols Received Counter Register.
- Port {0..17} VC0 Packets Transmitted Counter Register – Increments when a packet is transmitted all the way to EOP, including retransmissions.
- Port {0..17} VC0 Acknowledgements Received Counter Register – Increments when a packet-accepted CS is received.
- Port {0..17} Not Acknowledgements Received Counter Register – Increments when a packet-not-accepted CS, with cause other than “lack of resources,” is received.
- Port {0..17} VC0 Retry Symbols Received Counter Register – Increments when a retry CS, packet-not-accepted CS with cause “lack of resources,” is received.

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2.11.2 Successful Packet Transfer

The registers in Table 14 are useful for confirming successful packet transfer. These registers should be checked for the switch path used by each pair of endpoints, in both directions.

Table 14: Success Case Packet Transfer Counters

Packet Counter Register	Description	Implication
Port {0..17} VC0 Acknowledgements Transmitted Counter Register	This counter indicates the number of packets that the switch port successfully received from the link partner.	If this number is unexpectedly 0, see Switch Cannot Accept Packets.
Port {0..17} VC0 Packets Received Counter Register	This counter indicates the number of packets that the switch saw the link partner attempt to send.	If this counter is not the same as the Port {0..17} VC0 Acknowledgements Transmitted Counter Register, there may be retries and/or error conditions on the link.
Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register	This counter indicates the number of successfully received packets that are transferred through the fabric to this port.	If Port {0..17} VC0 Acknowledgements Transmitted Counter Register is not 0 on the port that should be receiving packets, and this counter is 0 on the port that should be transmitting the packets, this indicates a routing configuration issue.
Port {0..17} VC0 Acknowledgements Received Counter Register	This counter indicates the number of packets that the switch port successfully sent to the link partner.	If this counter is 0, there may be a configuration issue on the switch or on the link partner.
Port {0..17} VC0 Packets Transmitted Counter Register	This counter indicates the number of packets that the switch port attempted to send to the link partner.	If this counter is not the same as the Port {0..17} VC0 Acknowledgements Received Counter Register, there may be retries and/or error conditions on the link.

2.11.3 Switch Cannot Accept Packets

The performance counters in Table 15 can be used as a first step in debugging why a switch port cannot accept packets.

Table 15: Packet Counters and Configuration Issues – Switch Cannot Accept Packets

Packet Counter Register	Description	Implication
Port {0..17} Not Acknowledgements Transmitted Counter Register	This counter indicates the number of packets that the switch port acknowledged with a Packet Not Accepted control symbol.	If this counter is not 0, the switch has a configuration or status that prevents packet acceptance (see Table 16).
Port {0..17} VC0 Retry Symbols Transmitted Counter Register	This counter indicates the number of packets that the switch port acknowledged with a Retry control symbol.	If this counter is not 0, the switch is configured to accept packets but is congested. This may indicate that there is a bandwidth mismatch in the system. It may also indicate that the switch is unable to send packets to the destination (for more information, see Switch Cannot Transmit Packets).

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Table 15: Packet Counters and Configuration Issues – Switch Cannot Accept Packets

Packet Counter Register	Description	Implication
Port {0..17} Filter Match Counter Value 0 Register through Port {0..17} Filter Match Counter Value 3 Register	This counter indicates the number of received packets that the switch filtering mechanism has dropped.	Packets are being dropped because they are filtered. Check that the correct packets are being filtered.
Port {0..17} VC0 Received Packets Dropped Counter Register	This counter indicates the number of packets dropped by the receive port.	Packets are being dropped due to error status, routing configuration, or other configuration issues.

The configuration and status values for the port that are relevant to packet reception are listed in Table 16.

Table 16: Configuration and Status Values to Check – Switch Cannot Accept Packets

Packet Counter Register	Bit Field	Debug Notes
Port {0..17} Error and Status CSR	PORT_OK	If this bit is set to 0, the link is not connected to the link partner. For more information, see the *Debugging IDT S-RIO Gen2 Switches Using RapidFET JTAG*.
	PORT_ERR	If this bit is set to 1, the standard hardware error recovery has failed. For more information, see HS-LP Controlled Recovery.
	INPUT_ERR_STOP	If this bit is set to 1, the switch input port has detected an error and error recovery is not complete. Check that the Port Link Timeout Control CSR has been initialized according to the guidelines in Initialization.
Port {0..17} Control 1 CSR	PORT_DIS	This bit must be cleared to allow the port to train.
	INPUT_PORT_EN	This bit must be set to allow the port to accept non-maintenance packets.
	PORT_LOCKOUT	This bit must be cleared to allow the port to accept packets.
Port {0..17} Implementation Specific Error Detect Register	RTE_ISSUE	Packet received that is dropped according to the conditions for this event. For more information, see the description of this bit field.
	RX_DROP	Reception of non-maintenance packets has been disabled (see INPUT_PORT_EN).

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2.11.4 Switch Is Not Routing Packets Correctly

If some packets are routed correctly, and some are dropped, check for the isolation events described in Event Isolation. To ensure that routing tables are being programmed as expected, check the registers in Table 17.

Table 17: Packet Counters and Configuration Issues – Switch Is Not Routing Packets Correctly

Packet Counter Register	Description	Implication
Route Port Select Register	This register determines which port the Standard Route Table Entries Configuration destID Select CSR and Standard Route Table Entry Configuration Port Select CSR are applied to.	If this register is set incorrectly, routing table changes using the standard registers will be applied to the incorrect port (for more information, see Packet Routing).
Multicast Route Select Register	This register determines which port the Multicast Mask Port CSR, Multicast Association Selection CSR and Multicast Association Operations CSR are applied to.	If this register is set incorrectly, multicast routing changes using the standard registers will be applied to the incorrect port (for more information, see Packet Routing).
RapidIO Domain Register	This register overrides Domain routing table entry, and determines which 16-bit device IDs are routed using the Device routing table.	If this register is set incorrectly, packets with 16-bit device IDs may be unexpectedly routed using the Device routing table (for more information, see Packet Routing).
Port {0..17} Operations Register	The SELF_MCAST_EN bit causes multicast packets to be sent back to the port they were received on, if that port is part of the multicast mask.	If SELF_MCAST_EN is set incorrectly, multicast packets may be unexpectedly received by the device that originated them (for more information, see Packet Routing).

For Revision A/B, if maintenance packets are not routed correctly, enable all events in the Logical/Transport Layer Error Enable CSR and check that no events are seen in the Logical/Transport Layer Error Detect CSR. Debug the cause of any events seen.

For Revision C, if maintenance packets with a hop count equal to 0 are not routed correctly, enable all events in the Logical/Transport Layer Error Enable CSR and check that no events are seen in the Logical/Transport Layer Error Detect CSR. Debug the cause of any events seen.

If trace functionality is active on any port, packets may be sent to the trace port unexpectedly. To determine where traced packets will be sent, and whether non-traced traffic may be sent on the trace port, check the TRACE_OUT_PORT_MODE, TRACE_OUT_PORT, and TRACE_EN fields in the Device Control 1 Register. To determine which ports have trace functionality enabled and what packets will be traced, check the TRACE_x_EN bits in the Port {0..17} Operations Register.

If filter functionality is active on any port, packets may be dropped unexpectedly. To determine which ports have filter functionality enabled, and which packets will be dropped, check the FILTER_x_EN bits in the Port {0..17} Operations Register.

If the registers in Table 17 are set correctly, then each route must be verified individually (for more information, see Packet Routing).

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2.11.5 Switch Cannot Transmit Packets

The performance counters in Table 18 can be used as a first step in debugging possible configuration or status issues that prevent successful transmission of packets.

Table 18: Packet Counters and Configuration Issues – Switch Cannot Transmit Packets

Packet Counter Register	Description	Implication
Port {0..17} Not Acknowledgements Received Counter Register	This counter indicates the number of packets that the link partner negatively acknowledged.	If this counter is not 0, the switch is sending packets to the link partner. The link partner is rejecting the packets. Debug the link partner configuration and status.
Port {0..17} VC0 Retry Symbols Received Counter Register	This counter indicates the number of packets that the link partner acknowledged with a Retry.	The link partner is configured to accept packets, but is congested. Debug the link partner's ability to accept packets.
Port {0..17} VC0 Transmitted Packets Dropped Counter Register	This counter indicates the number of packets dropped by the switch port's transmit logic.	Packets are being dropped due to errors or configuration issues (see Table 19).
Port {0..17} VC0 TTL Packets Dropped Counter Register	This counter indicates the number of packets dropped due to exceeding the Time To Live (TTL) period.	The TTL period is too short to allow packets to be sent successfully. Disable the TTL function or increase the time to live period (see Packet Time to Live CSR and Computing Timeout Values).
Port {0..17} VC0 CRC Limit Packets Dropped Counter Register	This counter indicates the number of packets dropped due to exceeding the number of consecutive Packet-Not-Accepted responses.	The Port {0..17} Operations Register[CRC_RETX_LIMIT] value is set too low. Alternatively, error detection has been suppressed on the switch input port, and a corrupted packet has been forwarded through the switch to a link partner with error detection enabled. Check Port {0..17} Control 1 CSR[ERR_CHK_DIS] on all input ports.

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The configuration and status values for the port that are relevant to packet transmission are listed in Table 19.

Table 19: Configuration and Status Values to Check – Switch Cannot Transmit Packets

Packet Counter Register	Bit Field	Debug Notes
Port {0..17} Error and Status CSR	PORT_OK	If this bit is 0, the link is not connected to the link partner. For more information, see the *Debugging IDT S-RIO Gen2 Switches Using RapidFET JTAG Application Note*, available from www.idt.com.
	PORT_ERR	The standard hardware error recovery has failed. Packets will not be transmitted until this state is cleared. The switch may be configured to drop packets in this state. For information on recovery, see HS-LP Controlled Recovery.
	OUTPUT_ERR_STOP	If this bit is set to 1, the switch output port has detected an error, and error recovery is not complete. Packets will not be transmitted until OUTPUT_ERR_STOP has been cleared. Check that the Port Link Timeout Control CSR has been initialized according to the guidelines in Computing Timeout Values. Check that the link partner configuration and status will allow it to complete error recovery and accept packets.
	OUTPUT_DROP	If this bit is set to 1, the port has dropped at least one packet.
	OUTPUT_FAIL	If this bit is set to 1, the port has detected a failure condition, and may be configured to halt packet transmission and/or to drop packets (for more information, see Physical Layer Events).
Port {0..17} Control 1 CSR	PORT_DIS	This bit must be cleared to allow the port to train.
	OUTPUT_PORT_EN	This bit must be set to allow the port to transmit non-maintenance packets. For Revision C of the CPS-1848, the reset value for this bit is 1; for Revision A/B, the reset value is 0.
	PORT_LOCKOUT	This bit must be cleared to transmit any packets.
Port {0..17} Implementation Specific Error Detect Register	TX_DROP	Packet transmission has been disabled (see OUTPUT_PORT_EN in Port {0..17} Control 1 CSR).

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2.11.6 Requesting Debug Assistance

If you are unable to resolve issues in your system using the information in this document, please contact IDT RapidIO support. As part of the request, please submit the following register values for all ports on the device. This is the first step in resolving the issue.

1. Port {0..17} Error and Status CSR
2. Port {0..17} Control 1 CSR
3. Port {0..17} Error Detect CSR
4. Port {0..17} Implementation Specific Error Detect Register

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3. RapidIO Lanes

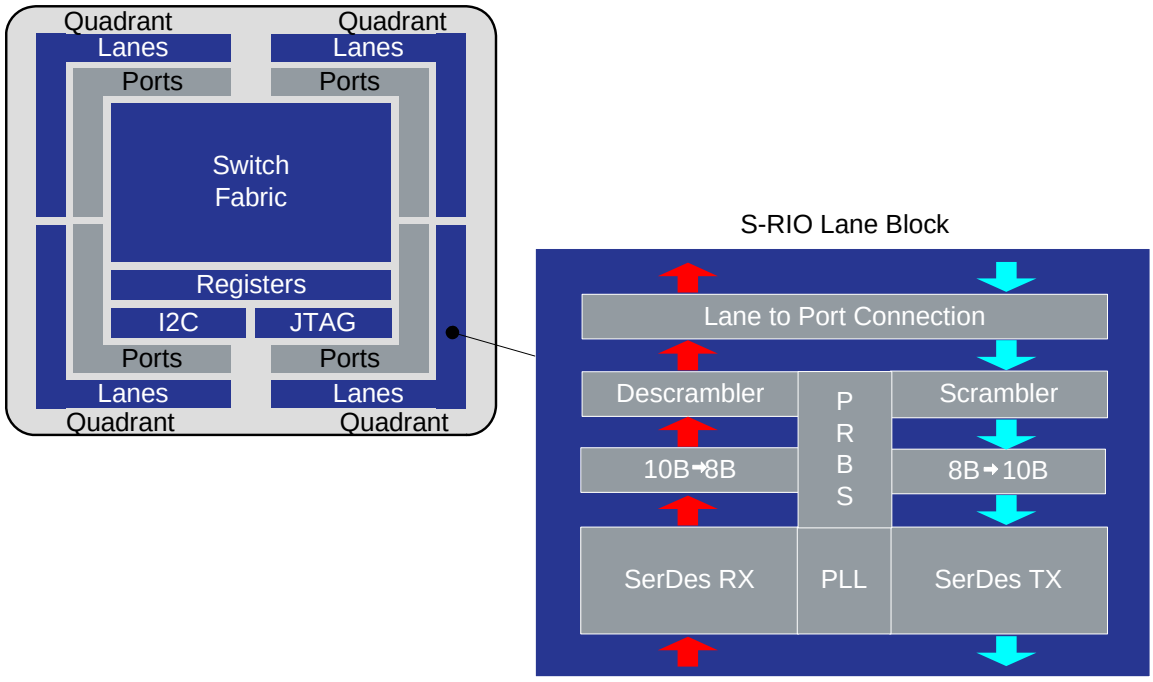
The CPS-1848 S-RIO lane blocks include the Serializer/Deserializer (SerDes), as well as the logic to convert between the SerDes interface and the port interface.

Topics discussed include the following:

- Lane to Port Mapping
- Lane and Port Speeds
- Lane, PLL, and Port Power-Down
- Port and Lane Initialization Sequence
- Loopback Capabilities
- Bit Error Rate Testing

Figure 12 shows a block diagram of an S-RIO Lane Block. The key components of this lane diagram are discussed throughout the chapter.

Figure 12: S-RIO Lane Block Diagram



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3.1 Lane to Port Mapping

As displayed in Table 20, each S-RIO port can be comprised of one, two, or four lanes (this is called port width). After a device reset, the CPS-1848's port width settings and lane to port mapping are configured based on the setting of the QCFG[7:0] pins (for more information, see the *CPS-1848 Datasheet*).

Software can also control the device's port width settings and lane to port mapping using the Quadrant Configuration Register. Table 20 shows the supported mapping of lanes to ports for each CPS-1848 quadrant based on the value of the QUADx_CFG field in the Quadrant Configuration Register.

Table 20: Lane to Port Mapping[1]

QUADx_CFG / QCFG[2] Setting	PLL	Port Width	Mapping	
			Port	Lane(s)
Quadrant 0 / QCFG[1:0]				
00	0	4x	0	0–3
	4	4x	4	16–19
	8	4x	8	32–35
	-	-	12, 16 (Unused)	-
01	0	2x	0	0–1
	0	2x	12	2–3
	4	4x	4	16–19
	8	4x	8	32–35
	-	-	16 (Unused)	-
10	0	2x	0	0–1
	0	2x	12	2–3
	4	4x	4	16–19
	8	2x	8	32–33
	8	2x	16	34–35
11	0	2x	0	0–1
	0	1x	12	2
	0	1x	16	3
	4	4x	4	16–19
	8	4x	8	32–35

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Table 20: Lane to Port Mapping[1] *(Continued)*

QUADx_CFG / QCFG[2] Setting	PLL	Port Width	Mapping	
			Port	Lane(s)
Quadrant 1 / QCFG[3:2]				
00	1	4x	1	4–7
	5	4x	5	20–23
	9	4x	9	36–39
	-	-	13, 17 (Unused)	-
01	1	2x	1	4–5
	1	2x	13	6–7
	5	4x	5	20–23
	9	4x	9	36–39
	-	-	17 (Unused)	-
10	1	2x	1	4–5
	1	2x	13	6–7
	5	4x	5	20–23
	9	2x	9	36–37
	9	2x	17	38–39
11	1	2x	1	4–5
	1	1x	13	6
	1	1x	17	7
	5	4x	5	20–23
	9	4x	9	36–39
Quadrant 2 / QCFG[5:4]				
00	2	4x	2	8–11
	6	4x	6	24–27
	10	4x	10	40–43
	-	-	14 (Unused)	-
01	2	2x	2	8–9
	2	2x	14	10–11
	6	4x	6	24–27
	10	4x	10	40–43

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Table 20: Lane to Port Mapping[1] *(Continued)*

QUADx_CFG / QCFG[2] Setting	PLL	Port Width	Mapping	
			Port	Lane(s)
10	-	Undefined	-	-
11	-	Undefined	-	-
Quadrant 3 / QCFG[7:6]				
00	3	4x	3	12–15
	7	4x	7	28–31
	11	4x	11	44–47
	-	-	15 (Unused)	-
01	3	2x	3	12–13
	3	2x	15	14–15
	7	4x	7	28–31
	11	4x	11	44–47
10	-	Undefined	-	-
11	-	Undefined	-	-

1. After a configuration change is made using Quadrant Configuration Register, IDT recommends resetting each port as described in Table 6.
2. After a device reset, the value of QCFG[7:0] determines the CPS-1848's quadrant configurations. Software can also control the quadrant configurations based on the value of QUADx_CFG in the Quadrant Configuration Register.



The least significant lane number represents the lowest lane of the port. For example, for lanes 4–7, lane 4 is the lowest lane of the port and lane 7 is the highest lane of the port.

A port can operate with fewer lanes than the number assigned to it using the PWIDTH_OVRD field of the Port {0..17} Control 1 CSR. Examples of the use of this field are displayed in Table 21.

Table 21: PWIDTH_OVRD Examples

Maximum Port Width	Desired Port Width	PORT_WIDTH_OVRD	Description
4x	2x	0b101	Use only the two lowest numbered lanes assigned to the port.
4x	1x	0b010	Use only the lowest numbered lane assigned to the port.
2x	1x	0b010	Use only the lowest numbered lane assigned to the port.



Changing the width of a port causes the port to reinitialize. For more information on the port initialization process, see Port and Lane Initialization Sequence.

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3.2 Lane and Port Speeds

Each S-RIO port can support all lane rates. CPS-1848 ports that are connected to the same group of four lanes have restrictions on their possible lane rates. Ports can operate in either of two lane-speed groups:

1. 6.25 Gbaud, 3.125 Gbaud
2. 5.0 Gbaud, 2.5 Gbaud, 1.25 Gbaud

Each SerDes has a single PLL. The PLL can be configured to operate at 2.5 GHz, supporting the 5.0/2.5/1.25 Gbaud lane speed groups, or at 3.125 GHz, supporting the 6.25/3.125 Gbaud speed group. Each lane can be configured to support a multiple of the base PLL frequency.

A port's speed is controlled through changing the speed of the lanes connected to the port. The speeds available are controlled through the following registers and fields:

- PLL_DIV_SEL field of the PLL {0..11} Control 1 Register (selection of lane-speed group)
- TX_RATE and RX_RATE fields in the Lane {0..47} Control Register (lane rate from a lane-speed group)

IDT recommends that S-RIO ports be disabled before changing any lane speeds. Ports can be disabled by setting PORT_DIS to 1 in Port {0..17} Control 1 CSR. Ports can be enabled after all lane speeds have been configured by setting PORT_DIS set to 0.

Changing the configuration of a PLL affects all ports and lanes associated with that PLL. All ports and lanes associated with a PLL require a port reset, as described in Table 6.

3.2.1 Lane Speed Change Examples

When changing port speeds from 1.25 Gbaud to 3.125 or 6.25 Gbaud, change RX_RATE and TX_RATE in the Lane {0..47} Control Register before changing PLL_DIV_SEL in the PLL {0..11} Control 1 Register.

When changing port speeds from 3.125 or 6.25 Gbaud to 1.25 Gbaud, change PLL_DIV_SEL in the PLL {0..11} Control 1 Register before changing RX_RATE and TX_RATE in the Lane {0..47} Control Register.

This first example assumes that Quadrant 0 of the CPS-1848 uses a configuration value of 0b01 (see Table 20). This connects port 0 to lanes 0 and 1, and port 12 to lanes 2 and 3. Assume that port 0 and 12 are currently operating at a lane rate of 5 Gbaud. In addition, assume that port 0 should operate at 6.25 Gbaud, and port 12 should operate at 3.125 Gbaud. Changing the PLL selected for the SerDes affects both ports and requires a per-port reset of both ports. The register accesses listed in Table 22 are required to reconfigure the lane speeds of the ports.

Table 22: Changing Lane Speed Group on Ports 0 and 12 – Example 1

Step	Offset	Mask and Value	Description
Change PLL selection	0xFF0000 PLL {0..11} Control 1 Register	0x00000001	Select 6.25/3.125 Speed Group by setting the PLL_DIV_SEL bit.

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Table 22: Changing Lane Speed Group on Ports 0 and 12 – Example 1 *(Continued)*

Step	Offset	Mask and Value	Description
Select 6.25 Gbaud lane rate for lanes 0 and 1 (Port 0)	0xFF8000 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b10. Set LANE_DIS field to 0.
	0xFF8100 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b10. Set LANE_DIS field to 0.
Select 3.125 Gbaud lane rate for lanes 2 and 3 (Port 12)	0xFF8200 Lane {0..47} Control Register	0xXXXXX0A	Set TX_RATE and RX_RATE fields to 0b01. Set LANE_DIS field to 0.
	0xFF8300 Lane {0..47} Control Register	0xXXXXX0A	Set TX_RATE and RX_RATE fields to 0b01. Set LANE_DIS field to 0.
Reset the ports to allow the PLL and lane rate changes to take effect	0xF20300 Device Reset and Control Register	0x80041001	Reset PLL 0 along with ports 0 and 12.

In the second example assume that the lane speed of port 5, which is connected to lanes 20 to 23 in quadrant 1, must change from 2.5 Gbaud to 5 Gbaud operation. Port 5 does not need to be reset in this case because the lane rate is in the same lane speed group. The register operations required to perform this change are displayed in Table 23.

Table 23: Changing Lane Speed on Port 5 – Example 2

Step	Offset	Mask and Value	Description
Select 5 Gbaud lane rate for lanes 20, 21, 22 and 23	0xFF9400 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b10. Set LANE_DIS field to 0.
	0xFF9500 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b10. Set LANE_DIS field to 0.
	0xFF9600 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b01. Set LANE_DIS field to 0.
	0xFF9700 Lane {0..47} Control Register	0xXXXXX14	Set TX_RATE and RX_RATE fields to 0b01. Set LANE_DIS field to 0.

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3.3 Lane, PLL, and Port Power-Down

Systems operate more efficiently if they can save the power consumed by unused lanes, PLLs, and ports. The CPS-1848 allows software to manually or automatically turn off these resources when not required, as described below:

- Lane power-down – To disable an unused lane, set LANE_DIS to 1 in the Lane {0..47} Control Register.
- PLL power-down – If all lanes associated with a PLL are disabled, additional power savings can be realized by powering down the PLL. To power down a PLL, set the PLL_PWR_DWN bit to 1 in the PLL {0..11} Control 1 Register.
- Port power-down – If a port does not have any lanes connected to it, the port is automatically powered down.

3.4 Port and Lane Initialization Sequence

The CPS-1848's S-RIO ports support a RapidIO standard, multi-step initialization process. For more information, see Part 6 of the *RapidIO Specification (Rev. 2.1)*. Port and lane initialization follows these steps:

1. Achieve lane synchronization. When lane synchronization is achieved, valid 10-bit code groups are received reliably.
   — The number of valid code groups that must be received error-free before deciding that lane synchronization has been achieved is controlled through VMIN in the Port {0..17} Lane Synchronization Register.
2. IDLE sequence negotiation. The CPS-1848 attempts to use the RapidIO Gen2 IDLE2 sequence for all lane speeds. If the CPS-1848 detects that the link partner is using the RapidIO Gen1 IDLE1 sequence, it selects the IDLE1 sequence.
   — The IDLE sequence selected is located in the IDLE_SEQ bit of the Port {0..17} Error and Status CSR.



It is not possible to disable the use of the IDLE2 sequence for 6.25 Gbaud lane rates. For lane rates of less than 6.25 Gbaud, IDLE2 sequence can be disabled by clearing IDLE2_EN in the Port {0..17} Error and Status CSR.

The IDLE2 sequence must be used for 6.25 Gbaud lane rates.

3. If the IDLE2 sequence is active, the CPS-1848 performs the following:
   — Lane polarity inversion detection and correction. To simplify board layouts, the CPS-1848 can automatically detect and correct when the positive and negative traces of a differential pair for a lane are inverted. Lane inversion status for each lane is located in the Lane {0..47} Status 0 CSR.RX_INVERT bit.
   — Lane reversal detection and correction: the CPS-1848 can automatically detect and correct if the lanes on a multilane port are connected in reverse order. This can simplify board layouts. Lane reversal status for each CPS-1848 port is located in Port {0..17} Implementation Specific Error Detect Register.REORDER.



RapidIO Gen1 devices support the IDLE1 sequence only. It is not possible to reverse the lane ordering of a port when the IDLE1 sequence is used; therefore, the link partner's lanes must be connected in the correct order.



The use of lane reversal is not recommended for links that support hot swap, or that are expected to successfully downgrade if there is a hardware error.

4. Whether IDLE1 or IDLE2 is selected, multilane ports attempt to align the different lanes to ensure that striped data is correctly decoded. When IDLE2 is active, this step occurs once lane polarity and lane reversal have been resolved. Lane alignment occurs simultaneously with transmitter emphasis/receiver equalization optimization. Note that this step is not necessary for ports constrained to operate as single lane (1x) ports.
5. The widest supported port operating width will be selected once all steps have completed. The maximum time allowed for IDLE sequence negotiation, IDLE2 sequence optimization, and lane alignment (if necessary) is 32 milliseconds. The operating width of the port is located in the Port {0..17} Control 1 CSR.INIT_PWIDTH field.
6. Status control symbols are transmitted and received to ensure that control symbols can be exchanged correctly on the port.

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7. The link-level flow control mode (transmitter or receiver controlled) is negotiated as part of the exchange of status control symbols. The CPS-1848 always attempts to use transmitter-controlled flow control, and reverts to receiver-controlled flow control if the link partner does not support the transmitter method.
   - To disable the use of transmitter-controlled flow control on a port, set the Port {0..17} Operations Register.TX_FLOW_CTL_DIS bit.
   - The flow control mode that is currently selected is indicated in Port {0..17} Status and Control Register.RX_FC.
8. Once at least seven consecutive status control symbols have been received, and at least 15 have been transmitted, the port asserts the PORT_OK bit and clears the PORT_UNINIT bit in the Port {0..17} Error and Status CSR. Thereafter, the port can exchange packets and detect/report transmission errors.

Clear error conditions on the link, which may have occurred during link initialization.

The above sequence reliably initializes single or multi-lane links as long as at least one of the redundant lanes in each direction is working. However, consistent with the *RapidIO Specification (Rev. 2.1)*, the initialization sequence for 4x ports was not designed to operate correctly when connected to multiple, separate 1x ports on the redundant lanes. This type of configuration is not supported.

3.4.1 Signal Quality Optimization

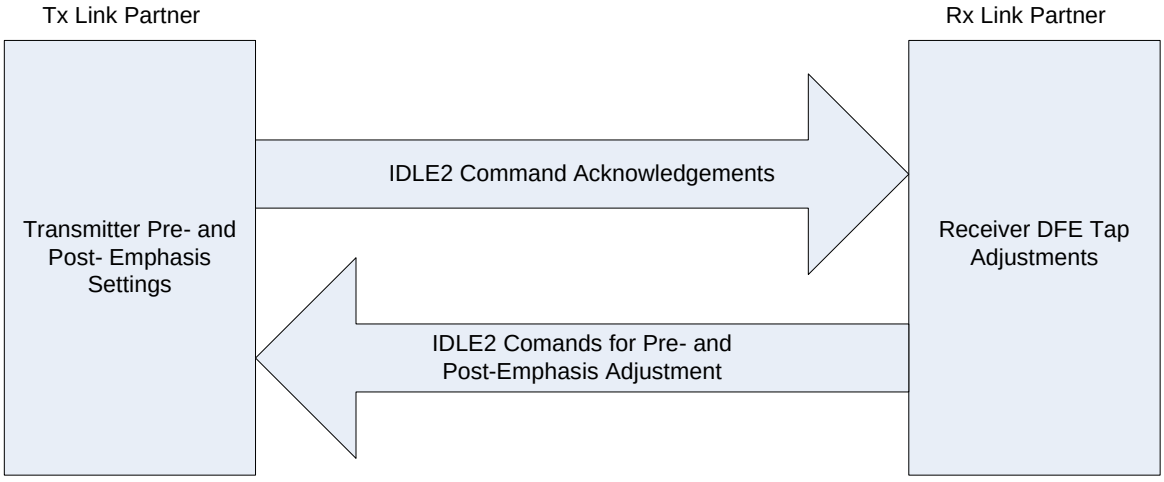
The default values for the signal quality settings are sufficient for channels that are compliant with the RapidIO specification's short- and medium-reach channel definitions (50 cm with up to two connectors). However, the default signal quality settings may need to change for long channels and/or high lane speeds.

The CPS-1848 supports two methods for optimizing the signal quality of a lane (see Figure 13):

- Transmit emphasis
- Receiver Decision Feedback Equalization (DFE)

Transmit emphasis changes the characteristics of the transmit signal based on the bit that was previously transmitted, and the bit that will be transmitted after the current bit. Receiver DFE changes the received signal to reduce electrical effects created by previously received bits.

Figure 13: Optimizing Lane Signal Quality



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The CPS-1848 supports lane lengths up to those specified by the RapidIO medium-run PHY standard without link partner transmit emphasis or DFE. The transmit emphasis settings of the CPS-1848 and the link partner may need to be adjusted for channels longer than medium run. Depending on the electrical characteristics of the channel, CPS-1848 receiver DFE may also be necessary for channels longer than medium run.

3.4.1.1 CPS-1848 Transmitter Emphasis Control

The RapidIO specification defines a transmitter emphasis function that is controlled by two filter coefficients called the Pre and Post taps. The CPS-1848 transmitter emphasis coefficients can be changed by writing them directly.

3.4.1.1.1 Register Control of CPS-1848 Transmit Emphasis

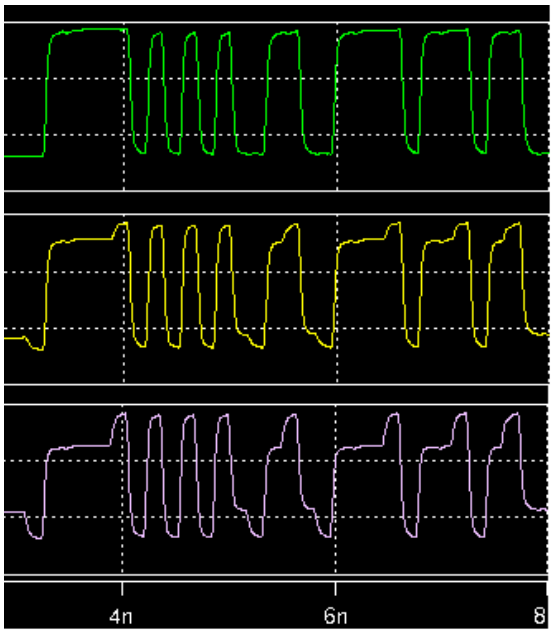
The CPS-1848 transmit emphasis is controlled by each lane using commands written to the POS1_CMD and NEG1_CMD fields in the Lane {0..47} Status 3 CSR. The supported commands include pre and post tap value increases and decreases, as well as changes to configured reset and preset tap values. The reset and preset values for each of the two pre-emphasis taps are configured through writes to the Lane {0..47} Status 2 CSR.

The output waveform has three parameters that can be modified by writing the desired value to the register field:

- NEG1_TAP[4:0] (Lane {0..47} Status 3 CSR) – This corresponds to the Pre tap.
- TX_AMP_CTL[5:0] (Lane {0..47} Control Register)
- POS1_TAP[5:0] (Lane {0..47} Status 3 CSR) – This corresponds to the Post tap.

The adjustment of NEG1_TAP and POS1_TAP tap change the spectral content of the waveform with the intent of improving the eye shape at the receiver. The TX_AMP_CTL control adjusts the signal amplitude to allow the signal amplitude to be reduced for short links, or to be increased on lossy and long links. The NEG1_TAP and POS1_TAP selections are applied only to sequences of two or more bits of the same value. The TX_AMP_CTL control is applied to all bits on the lane. The following figures show the relationship between the waveform voltage change imposed by the tap setting (in dB volts) and the register (DAC, or Digital Analog Converter) value programmed in the NEG1_TAP field of the corresponding Lane {0..47} Status 3 CSR.

The following waveform shows the effects on the waveform for NEG1_TAP settings of zero (top), 0b01111 (middle), and 0b11111 (bottom). The POS1_TAP is set to 0 and the TX_AMP_CTL value is set to 52 (default).



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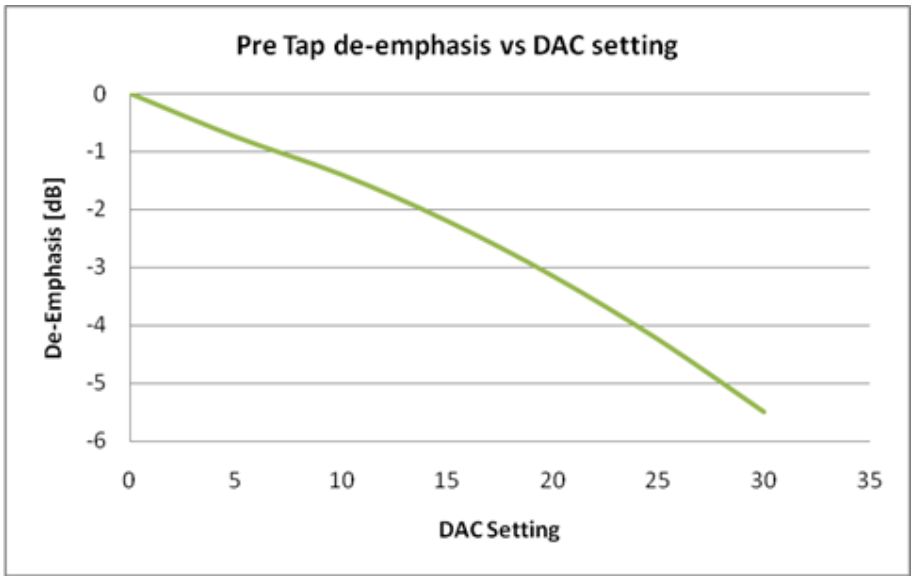
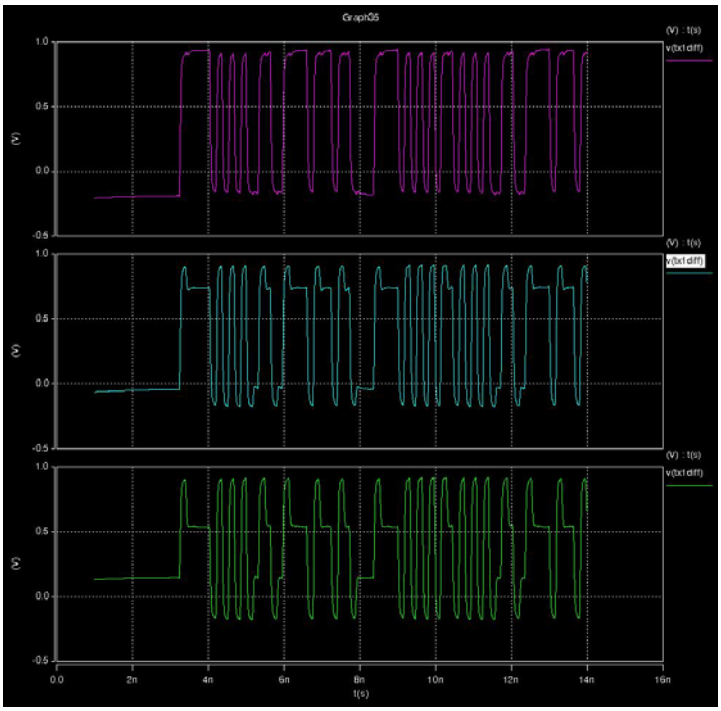
As the NEG1_TAP setting is increased the step size of the previous bits to the last bit increases. The following graph shows the change in the step size as the register (DAC) value is increased. The dB value is calculated as: 20log (previous bits amplitude / last bit amplitude).



The following figure shows the effects on the waveform for the POS1_TAP settings of zero (top), 30 (middle) and 63 (bottom). The NEG1_TAP is set to 0 and the TX_AMP_CTL value is set to 52 (default).



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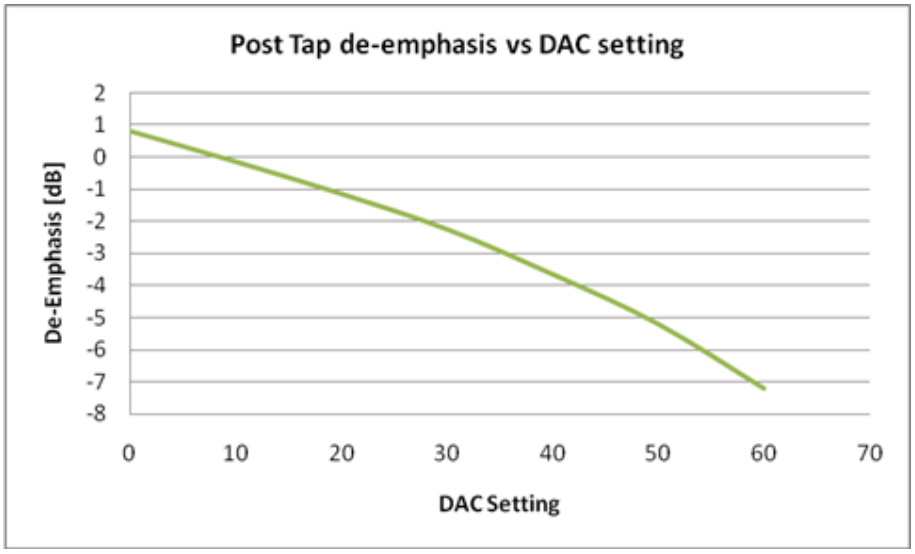
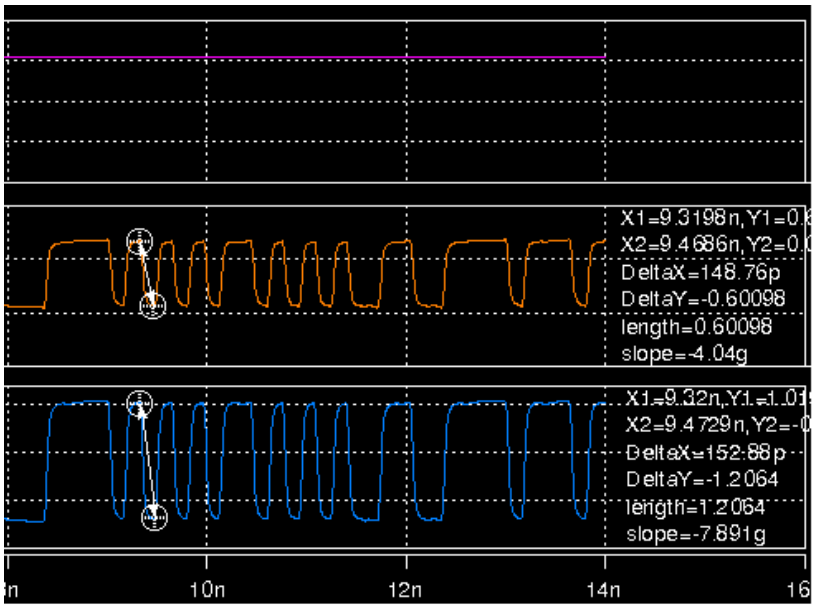
As the POS1_TAP value is increased, the step size from the initial bit amplitude to the subsequent bit amplitude increases. The following graph shows the change in the step size. The dB value is calculated as: 20log (step amplitude / first bit amplitude).



The following figure shows the effects on the waveform for the TX_AMP_CTL settings of zero (top), 30 (middle), and 60 (bottom). The NEG1_TAP and POS1_TAP controls are set to 0.



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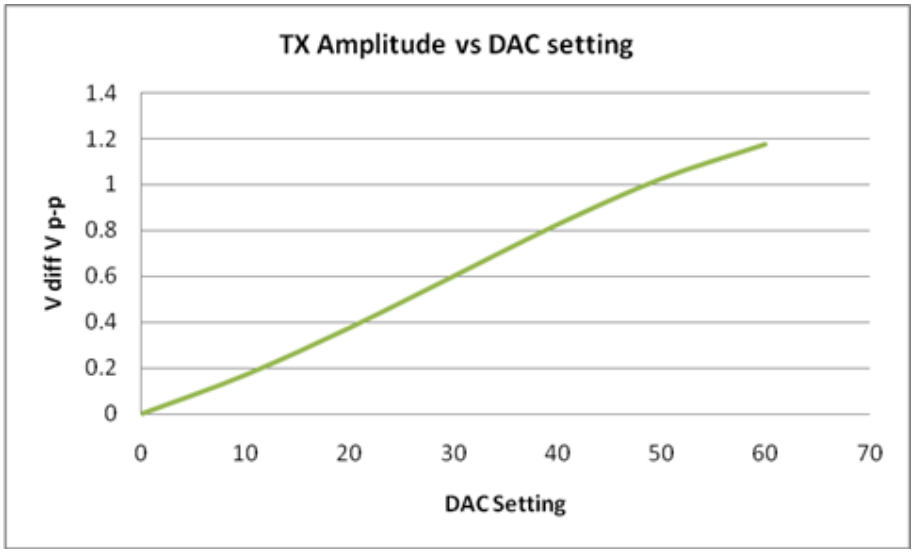
As the TX_AMP_CTL value in the Lane {0..47} Control Register is increased, the waveform amplitude increases. The following graph shows the change in the amplitude as the register (DAC) value is increased. The amplitude is measured in volts peak-to-peak differential.



3.4.1.2 Receiver DFE Control

The receiver DFE function is controlled by fields in the Lane {0..47} DFE 1 Register and Lane {0..47} DFE 2 Register. DFE is enabled using the Lane {0..47} DFE 1 Register.RX_DFE_DIS bit.

The CPS-1848 receiver DFE design has five “taps” numbered 0 to 4, in addition to a tap offset value. These values can be controlled through register accesses. The programming model for software control of the receiver DFE taps makes use of a paired “select” control bit and a tap value field for each tap. The following are the pairs of select control bits and tap values:

- Lane {0..47} DFE 1 Register.TAP_0_SEL and Lane {0..47} DFE 2 Register.TAP_0_CFG
- Lane {0..47} DFE 1 Register.TAP_1_SEL and Lane {0..47} DFE 2 Register.TAP_1_CFG
- Lane {0..47} DFE 1 Register.TAP_2_SEL and Lane {0..47} DFE 2 Register.TAP_2_CFG
- Lane {0..47} DFE 1 Register.TAP_3_SEL and Lane {0..47} DFE 2 Register.TAP_3_CFG
- Lane {0..47} DFE 1 Register.TAP_4_SEL and Lane {0..47} DFE 2 Register.TAP_4_CFG

The “select” control bit must be set to 1 in order for the associated tap value field to have any effect. IDT recommends that Tap 4 should be half the value of Tap 3, Tap 3 should be half the value of Tap 2, and Tap 2 should be half the value of Tap 1. Note that the signed Tap values should all be positive.

To load tap values, the Lane {0..47} DFE 2 Register.CFG_EN bit must transition from 0 to 1.

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3.4.1.3 Bit Error Rate Measurement for RapidIO Compliant Data

Bit error rate testing is facilitated by use of the Error Management Extensions registers. The physical layer error management extensions registers can be used to count the number of received bit errors on the link. To configure a port to count bit errors, perform the steps outlined in the following table.

Table 24: Configuring Bit Error Measurement

Step	Offset	Value
Enable all Rx error events	0x1044 (Port 0) Port {0..17} Error Rate Enable CSR	0x004E8015
Clear counter to 0, allow counter to reach 0xFF	0x1068 (Port 0) Port {0..17} Error Rate CSR	0x00030000
Disable event notification	0x106C (Port 0) Port {0..17} Error Rate Threshold CSR	0x00000000

Once the above steps are completed for a port, the Port {0..17} Error Rate CSR.ERR_RATE_CNTR field can be read to determine the number of errors seen since the counter was last cleared to 0.

The above algorithm reports all detectable errors for a port. If a port has multiple lanes, it is not possible to attribute the errors to a particular lane. To monitor errors on an lane-by-lane basis, use the ERR_8B10B field of the Lane {0..47} Status 0 CSR.

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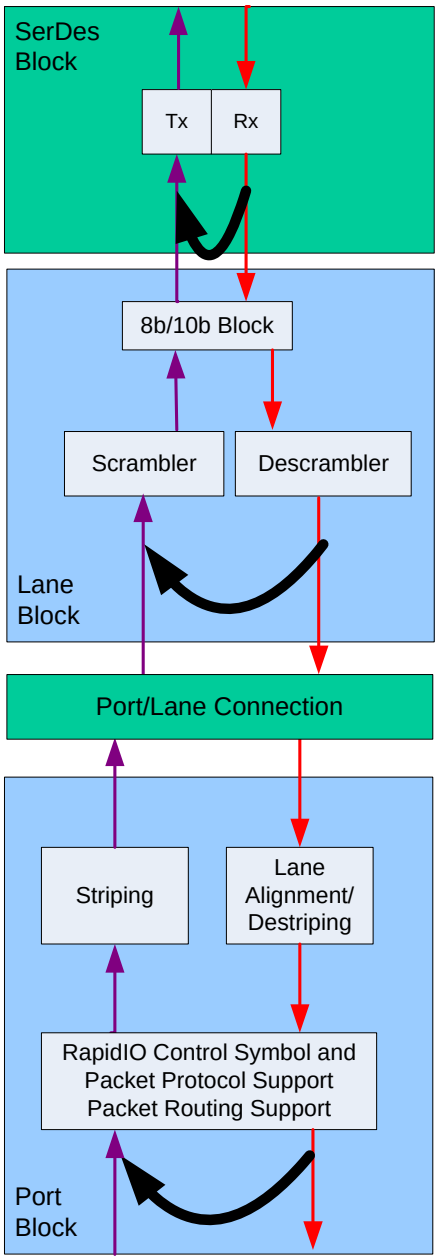
3.5 Loopback Capabilities

The CPS-1848 supports several lane and port loopback points that can be used for test and fault isolation purposes. These loopback points are displayed in Figure 14 and are discussed in the following sections.

Figure 14: Loopback Locations



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3.5.1 Lane Loopback Modes

3.5.1.1 10-bit Loopback Mode

10-bit loopback mode is controlled on individual lanes through the LPBK_10BIT_EN bit of the Lane {0..47} Control Register. The 10-bit loopback mode path loops back the serial data before 10-bit code group recognition is attempted. A clock signal can be extracted from the data, but no code group recognition is attempted at this point.

Without code group recognition, it is not possible for the receiver to compensate for the frequency difference between the transmitter and receiver. This implies that the looped back signal is subject to overruns or underruns due to transmit/receive frequency differences. To avoid this issue, the link partners must use the same reference clock source to ensure that receivers and transmitters operate at exactly the same frequency.



10-bit loopback does not contain a re-timer; therefore, the link partners must use the same reference clock source to ensure that the receivers and transmitters operate at exactly the same frequency.

3.5.1.1.1 10-bit Loopback Mode Restrictions

Although 10-bit loopback is controlled on an individual lane basis, the SerDes blocks are not completely decoupled from the port functions. When a port is configured in 4x mode, 10-bit loopback does not function properly on the upper lane of the 4x port. Therefore, the port must be configured in 1x and 2x mode before setting the lanes to 10-bit loopback (see Port Reconfiguration Operations). Since ports 4, 5, 6, 10, and 11 can only operate in 4x mode, 10-bit loopback is not functional on those ports.

3.5.1.2 8-bit Loopback Mode

8-bit loopback mode is controlled on individual lanes through the LPBK_8BIT_EN bit of the Lane {0..47} Control Register. This mode correctly retransmits data that has been successfully recognized as a valid 10-bit code group, and translated to an 8-bit value. If valid 10-bit code groups are not received, the retransmitted stream may vary from the received stream.

When the lane is operating at 6.25 Gbaud, the RapidIO Specification requires transmitted data to be scrambled, and received data must be descrambled. The scrambling and descrambling is done in accordance with the RapidIO protocol. To accommodate tests that do not use RapidIO compliant data, scrambling functionality can be disabled on a port basis using SCRAM_DIS in the Port {0..17} Control 2 CSR.



8-bit loopback does not contain a re-timer; therefore, the link partners must use the same reference clock source to ensure that the receivers and transmitters operate at exactly the same frequency.



The RapidIO Specification states that data scrambling/descrambling can be disabled only for tests. Data scrambling/descrambling must be enabled for normal operation.

3.5.2 Port Loopback Mode

3.5.2.1 Routing Table Loopback

Each S-RIO port can route packets back out the port they were received on. This mode is supported by the routing tables (for more information, see Packet Routing).

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3.6 Bit Error Rate Testing

Bit Error Rate (BER) measurement is supported as part of the RapidIO protocol, as well as through the per-lane status registers. For more information, see the Lane {0..47} Status 0 CSR and the registers that follow. BER measurement when the RapidIO protocol is active restricts the data patterns generated to valid 8b/10b codes.

The CPS-1848 has a Pseudo-Random Binary Sequence (PRBS) generator capability that supports testing based on random bit sequences.



The CPS-1848 cannot check PRBS sequences; it can only generate PRBS sequences.

This caution is applicable to Revision A and B only.

PRBS-based BER testing is performed on individual lanes. The programming model for PRBS testing consists of the following registers:

- Lane {0..47} Control Register – PRBS enable and pattern selection
- Lane {0..47} PRBS Generator Seed Register – PRBS pattern “seed” value
- Lane {0..47} PRBS Error Counter Register – Count of errors detected for PRBS (Revision C only)

Each Lane Level Block has a PRBS generator that is enabled by setting PRBS_EN and XMITPRBS to 1 in the Lane {0..47} Control Register. The generator supports five user-selectable PRBS polynomials and three user-defined fixed patterns, as described in the following sections.

3.6.1 PRBS Polynomials

The following polynomials are supported by the CPS-1848:

1. $x^{23}+x^{18}+1$ — For additional definition of the polynomial, see CCITT O.1S1/ITU-T O.150 section 5.6 [SONET].
2. $x^{31}+x^{28}+1$ — For additional definition of the polynomial, see ITU-T O.150 section 5.8 (and XAUI, IEEE Std. 802.3-2008).
3. $x^{10}+x^{7}+1$ — For additional definition of the polynomial, CCITT O.1S2/ITU-T O.192.
4. $x^{15}+x^{14}+1$
5. $x^{7}+x^{6}+1$

By default, the first value, also called as the seed, for all polynomials is all 1s. To change the seed used by the polynomial, program the Lane {0..47} PRBS Generator Seed Register.



When a PRBS polynomial is selected, a seed value of 0 is a programming error.



Only bits that are controlled by the polynomial are used when programming the seed value. For example, if $x^{23}+x^{18}+1$ is the polynomial selected, only the least significant 24 bits (8–31) of the Lane {0..47} PRBS Generator Seed Register are relevant.

The Lane Level Block allows the PRBS seed to be changed by programming the Lane {0..47} PRBS Generator Seed Register. Note that a value of all zeros produces indeterminate results. This register is used for programming the two 10-bit re-circulating seeds. The first 10 bits of this register is used for one seed and the next 10 bits for the other.

3.6.2 User-Defined Patterns

In addition to random bit sequences, the CPS-1848 also supports patterns that are deterministic. There are three pattern options. The pattern value is the least significant 10 bits (22–31) of the Lane {0..47} PRBS Generator Seed Register:

1. Send the pattern value continuously
2. Send the pattern value, followed by its inverse value, continuously

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3. Send 0, the pattern value, 0x3FF, and the inverse of the pattern value, continuously

Patterns can be sent using either 8-bit (8b/10b encoded) or 10-bit (unchanged) format. The format is controlled by the Lane {0..47} Control Register.PRBS_UNIDIR_BERT_MODE_EN. However, only 10-bit patterns can be checked.

The CPS-1848 can *generate* all user-defined patterns in both 8-bit and 10-bit mode (see Lane {0..47} Control Register.PRBS_UNIDIR_BERT_MODE_EN).

(Revision C only) The CPS-1848 can *check* user-defined patterns in 10-bit mode only (see Lane {0..47} Control Register.PRBS_UNIDIR_BERT_MODE_EN).

3.6.3 PRBS Pattern Generator

The CPS-1848 BER generator sources data that is checked by the link partner. In the following example, the CPS-1848 is responsible only for transmitting data and PRBS is configured on lane 12 to use the polynomial $x^{23}+x^{18}+1$.

Table 25: Programming Model for CPS-1848 Data Generation, Link Partner Checking

Step	Offset	Value	Description
Enable PRBS transmission with selected polynomial	0xFF8C00 Lane {0..47} Control Register	0x009C1E80	Enable PRBS for selected polynomial. The lower 16 bits of this value reflect default values, therefore they may be different for your application.

3.6.4 PRBS Pattern Checker and Log (Revision C)

All lanes associated with a port must be configured per each step before proceeding to the next step in the procedure.

In addition when operating in 8-bit PRBS mode, steps 3 to 4 and steps 4 to 5 in the PRBS Checking procedure, and steps 4 to 5 and steps 5 to 6 in the PRBS Generation and Checking procedure must be completed within the following time constraints; otherwise the PRBS test may fail:

- 8 ms when the I2C clock is operating at 400 kHz
- 2 ms when the I2C clock is operating at 100 kHz

When enabling the PRBS checker, complete a single write to each field setting instead of setting multiple bits with the same register write command.

The PRBS checker can be enabled when the link is down or not connected. If the checker is in 10-bit mode and the receive link is floating, the checker can receive and lock onto a stream of zeros from the SerDes. In this case, the checker cannot detect errors (even if the link is down).

Register accesses for PRBS test configuration must start at least 1 second after the port is enabled.

3.6.4.1 PRBS Generation

To configure the CPS-1848 to generate a PRBS sequence without 8b/10b encoding, perform the following steps:

1. Set Lane {0..47} PRBS Generator Seed Register[PRBS_SEED] as required.
2. Set Lane {0..47} Control Register[PRBS_MODE] to the selected polynomial and set PRBS_UNIDIR_BERT_MODE_EN as required (set to 0 for 8-bit mode; set to 1 for 10-bit mode).

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3. Set Lane {0..47} Control Register[XMITPRBS] to 1.
4. Set Lane {0..47} Control Register[PRBS_EN] to 1.

3.6.4.2 PRBS Checking

To configure the CPS-1848 to *check* a received PRBS sequence without 8b/10b encoding, perform the following steps:

1. Set Lane {0..47} PRBS Generator Seed Register[PRBS_SEED] as required.
2. Set Lane {0..47} Control Register[PRBS_MODE] to the expected polynomial and set PRBS_UNIDIR_BERT_MODE_EN as required (set to 0 for 8-bit mode; set to 1 for 10-bit mode).
3. Set Lane {0..47} Control Register[PRBS_TRAIN] to 1.
4. Set Lane {0..47} Control Register[PRBS_RX_CHECKER_MODE] as required (set to 0 for 8-bit mode; set to 1 for 10-bit mode).
5. Set Lane {0..47} Control Register[PRBS_EN] to 1.
6. Read Lane {0..47} PRBS Error Counter Register – This will clear errors that occurred during configuration.
7. Set Lane {0..47} Control Register[PRBS_TRAIN] to 0 – Errors are not reported when in training mode.
8. Read Lane {0..47} PRBS Error Counter Register – Check for errors other than from configuration while running a PRBS test.

3.6.4.3 PRBS Generation and Checking

If the same device is being used for both *generation and checking*, the following should be used:

1. Set Lane {0..47} PRBS Generator Seed Register[PRBS_SEED] as required.
2. Set Lane {0..47} Control Register[PRBS_MODE] to the selected polynomial and set PRBS_UNIDIR_BERT_MODE_EN as required (set to 0 for 8-bit mode; set to 1 for 10-bit mode).
3. Set Lane {0..47} Control Register[PRBS_TRAIN] to 1.
4. Set Lane {0..47} Control Register[XMITPRBS] to 1.
5. Set Lane {0..47} Control Register[PRBS_RX_CHECKER_MODE] as required (set to 0 for 8-bit mode; set to 1 for 10-bit mode).
6. Set Lane {0..47} Control Register[PRBS_EN] to 1.
7. Read Lane {0..47} PRBS Error Counter Register – This will clear errors that occurred during configuration.
8. Set Lane {0..47} Control Register[PRBS_TRAIN] to 0 – Errors are not reported when in training mode.
9. Read Lane {0..47} PRBS Error Counter Register – Check for errors other than from configuration while running a PRBS test.

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4. Switch Fabric

The S-RIO Switch Fabric is a buffered crossbar design that transfers S-RIO packets from a set of input ports to an associated set of output ports. The switch block supports switching between up to 18 ports.

Topics discussed include the following:

- Key Features
- Switch Fabric Architecture
- Input Buffer
- Input Buffer to Crosspoint Buffer Transfers
- Crosspoint Buffers
- Crosspoint Buffer to Final Buffer Transfers
- Maintenance Transaction Support
- Final Buffer

4.1 Key Features

The Switch Fabric supports the following key features:

- Switching between up to 18 S-RIO ports, with a maximum port data rate of 20 Gbps input and 20 Gbps output
- Peak aggregate data rate of 240 Gbps
- Low latency (for more information, see Performance)
- Each port can buffer up to 12 packets from the link partner, and up to 34 packets to be sent to the link partner
- Non-blocking across all ports and all priority levels
- Supports the packet ordering and deadlock avoidance rules defined in the *RapidIO Specification (Rev. 2.1), Part 6*.
- Supports S-RIO virtual channel: VC0. For VC0, the switch supports the use of the CRF bit such that within a specific priority, a packet with the CRF bit set can pass one without the CRF bit set. The CRF bit is supported for all four levels of basic S-RIO priority.
- (Revision A/B) Separate path for maintenance packets
- (Revision C) Separate path for maintenance packets with a hop count of 0. Maintenance packets with a hop count greater than 0 take the same path as non-maintenance packets.
- Can multicast and broadcast a received packet to multiple output ports
- Supports cut-through and store-and-forward packet forwarding modes
- Supports an optional queue aging function to ensure fairness across priorities

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4.2 Switch Fabric Architecture

Figure 15: Switch Fabric Block Diagram

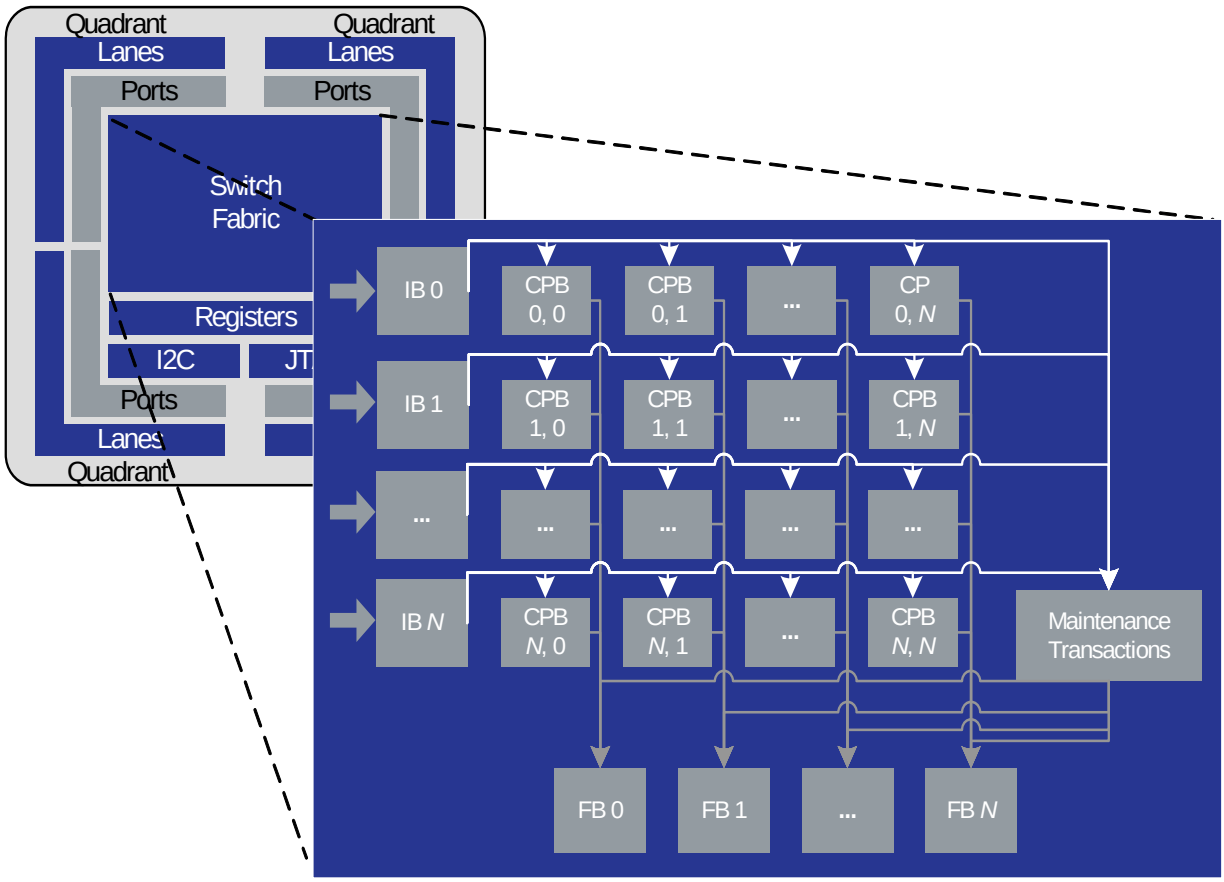

Figure 15 shows the buffer architecture of the Switch Fabric, where *N* is the number of ports configured within the device.

For Revision C, maintenance packets with a hop count equal to 0 use the Maintenance Transactions buffer.

As displayed in Figure 15, the Switch Fabric contains three types of buffers:

- Input Buffer (IB) – This buffer stores packets received from the link partner.
- Crosspoint Buffers (CPB) – This buffer stores packets for an Input Buffer/Final Buffer combination. The Switch Fabric has a matrix of Crosspoint Buffers.
- Final Buffer (FB) – This buffer stores packets to be transferred to the link partner.

Maintenance packets that are received with a hop count other than 0 (for Revision C, a hop count equal to 0) are handled as a separate flow by the Switch Fabric. There is a separate path between each Input Buffer and the centralized Maintenance Transactions handling block, and a separate path from the Maintenance Transactions block to each Final Buffer.

More information about buffer sizing, arbitration, and controls for buffers and transaction arbitration are discussed in the following sections.

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4.3 Input Buffer

The Input Buffer can store a maximum of 12 packets of any size. The Input Buffer enforces buffer allocation rules that are consistent with the RapidIO specification requirements for VC0 deadlock avoidance. The VC0 buffer allocation rules are enforced according to packet priority only – the CRF bit is not taken into account. Buffer allocation rules control the number of free buffers at which packets of a specific priority stop being accepted. There are two modes, controlled by the Switch Parameters 1 Register.BUF_ALLOC field, as displayed in Table 26.

Table 26: Input Buffer Allocation Mode

Priority	One Buffer Per Priority Mode	Two Buffers Per Priority Mode
3	0 buffers free	0 buffers free
2	1 buffer free	2 buffers free
1	2 buffers free	4 buffers free
0	3 buffers free	6 buffers free



The Switch Parameters 1 Register.BUF_ALLOC also controls buffer allocation for the Crosspoint Buffers and Final Buffers.

For example, if “Two Buffers Per Priority” mode is selected, five buffers are free and a packet of priority 1 is received, that packet can be accepted. If another packet of priority 1 is received, that packet will be retried because there are now only four buffers free. Note that packets of priority 3 will be accepted whenever there is a free buffer.

4.4 Input Buffer to Crosspoint Buffer Transfers

The CPS-1848 can wait until the entire packet has been received, or can start to forward the packet to a Crosspoint Buffer as soon as possible. Once a packet’s destID information has been received, the CPS-1848 can determine what output port to send the packet to. “Store-and-Forward” mode indicates a packet must be completely received before being forwarded, while “Cut-Through” indicates a packet should be forwarded as soon as possible. “Store-and-forward” and “Cut-through” mode are selected for all input ports using the Device Control 1 Register.CUT_THRU_EN field.



Store-and-Forward is the default mode. Use Cut-Through mode only if all active ports have the same capacity (for example, all ports are 2x with a lane rate of 5 Gbps). Cut-Through mode, however, can cause congestion in the Switch Fabric if there is a mix of fast and slow ports in the system.

Packets accepted by the Input Buffer are managed using Virtual Output Queues (VoQs). There is a set of VoQs for maintenance packets with a hop count of 0, and one set of VoQs for each Crosspoint Buffer. A set of VoQs consists of a list of packets at each priority and CRF combination.

Non-maintenance packets that are multicast have one VoQ entry for each Crosspoint Buffer to which they will be transferred. Maintenance packets with a hop count of 0 have a single entry in the set of VoQs associated with the maintenance block. If a Maintenance packet is to be multicast (that is, a port-write), the packet is replicated by the Maintenance Block.

The highest priority packet available in an Input Buffer is transferred first. Maintenance packets with a hop count of 0 have the highest priority regardless of their RapidIO priority. If no maintenance packet with a hop count of 0 can be transferred, then packets with priority 3 and the CRF bit set are sent, followed by packets with priority 3 and the CRF bit cleared, and so on down to packets with priority 0 and the CRF bit cleared. If there are packets with the same priority being sent to different Crosspoint Buffers, the packet chosen is based on a round-robin basis among the VoQs.

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4.4.1 VoQ Fairness/Starvation Avoidance

The operation of the CPS-1848 usually ensures the forward progress of all packets with minimal latency. However, under conditions of high congestion or pathological traffic patterns, the input scheduling algorithm can result in unbounded latency for low priority packets. To correct this behavior if it occurs, the CPS-1848 uses a fairness mechanism based on Oldest Queue First scheduling. The fairness mechanism limits the maximum latency for low priority packets. This scheduler mode is enabled by default but can be disabled by setting Switch Parameters 1 Register.ARB_MODE to 0b111.



The starvation avoidance mode can significantly influence packet transmission behavior; therefore, the recommended setting for Switch Parameters 1 Register.ARB_MODE is 0b111.

Only enable the fairness scheduling option to reduce large latency for low priority packets.

Each VoQ contains an age counter that increments whenever there is a packet in this VoQ and a packet from another VoQ is transferred. Once the age counter reaches the threshold programmed in the Switch Parameters 1 Register.INPUT_STARV_LIM field, the VoQ is handled as “old”. If any VoQs are “old”, then the age counter for that VoQ is frozen. The scheduling algorithm attempts to transfer packets from “old” VoQs for a given priority. If no “old” VoQs can transfer packets, then a VoQ that is not old is selected.

A VoQ has its “old” status cleared, and its age counter reset to 0, when the VoQ becomes empty.

4.4.2 Multicast Packets

When a packet is multicast, each VoQ associated with the Crosspoint Buffer that the packet must be sent to has an entry added to it for that packet. When a packet that is being multicast is selected for transfer, the other VoQs are checked to see if that packet is the first packet in the VoQ. If it is, and the associated Crosspoint Buffer can accept the packet, then the packet is transferred simultaneously to those Crosspoint Buffers as well as the Crosspoint Buffer originally selected.

If the multicast packet is not replicated to all ports on the first attempt at multicasting, the VoQs that have entries for that packet are marked as “old” immediately. This allows the multicast operation to complete as soon as possible.

4.5 Crosspoint Buffers

Each Crosspoint Buffer can store nine packets of any size. The Crosspoint Buffer enforces buffer allocation rules that are consistent with the RapidIO specification requirements for VC0 deadlock avoidance. The VC0 buffer allocation rules are enforced according to packet priority only – the CRF bit is not taken into account. Buffer allocation rules control the number of free buffers at which packets of a specific priority stop being accepted. There are two modes controlled by the BUF_ALLOC field in the Switch Parameters 1 Register, as displayed in the following table.

Table 27: Crosspoint Buffer Allocation Mode

Priority	One Buffer Per Priority	Two Buffers Per Priority
3	0 buffers free	0 buffers free
2	1 buffer free	2 buffers free
1	2 buffers free	4 buffers free
0	3 buffers free	6 buffers free

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4.6 Crosspoint Buffer to Final Buffer Transfers

The oldest of the set of highest priority packets is transferred to the associated Final Buffer before all other packets. Maintenance packets are handled as having the highest priority, regardless of their RapidIO priority. For Revision A/B, the priority of non-maintenance packets includes the CRF bit. For Revision C, the priority of non-maintenance packets and maintenance packets with a hop count greater than 0 includes the CRF bit.

The Final Buffer selects which Crosspoint Buffer to get packets from using Round Robin Scheduling. To select Round Robin Scheduling, set Switch Parameters 1 Register.ARB_MODE to 0b111.

4.7 Maintenance Transaction Support

For Revision A/B, all maintenance transactions are transferred from the Input Buffer to the central Maintenance transaction support block. Crosspoint buffers never contain Maintenance transactions that were received with a hop count greater than 0. Crosspoint buffers, however, may contain Maintenance transactions with a hop count of 0 because the hop count is decremented by the Port Level Block.

For Revision C, all maintenance transactions with a hop count equal to 0 are transferred from the Input Buffer to the central Maintenance transaction support block. Crosspoint buffers never contain Maintenance transactions that were received with a hop count equal to 0. Crosspoint buffers, however, may contain Maintenance transactions with a hop count of 0 because the hop count is decremented by the Port Level Block.



For Revision A/B, there is no ordering relationship between non-maintenance and maintenance packets. For Revision C, there is no ordering relationship between non-maintenance packets and maintenance packets with a hop count equal to 0.

Transfers from the Input Buffer to the Maintenance function are performed on a strict priority basis. If the priority of the maintenance packets is the same among the Input Buffers, a round-robin arbitration is used. For Revision A/B, the lowest priority maintenance packet has a higher priority than the highest priority non-maintenance packet. For Revision C, the lowest priority maintenance packet with a hop count equal to 0 has a higher priority than the highest priority non-maintenance packet.

The Maintenance function terminates maintenance packets with a hop count of 0. If the maintenance packet is a read or write request, the requested register access is performed, a maintenance response packet is formulated, and the response is sent back out the port the maintenance request packet was received on.

If the maintenance packet does not have a hop count of 0, the CPS-1848 decrements the hop count, recomputes the CRC, and forwards the packet. The packet is routed according to the routing table and multicast configuration of the port that received the maintenance packet.



The CPS-1848 supports maintenance read and write requests that are only 4-byte aligned and 4 bytes in size. All other maintenance request sizes and alignments are not executed by the device.

If a maintenance request is not 4-byte aligned and 4 bytes in size, the response packet for the request will have a status of “error.”

The Maintenance function is also responsible for originating port-write packets that indicate an event has been detected by the CPS-1848. For more information about originating and sending port-writes, see Port-Write Formats, Programming Model, and Generation.

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4.8 Final Buffer

Each Final Buffer can store 34 packets of any size. The Final Buffer enforces buffer allocation rules that are consistent with the RapidIO specification requirements for VC0 deadlock avoidance. The VC0 buffer allocation rules are enforced according to packet priority only – the CRF bit is not taken into account. Buffer allocation rules control the number of free buffers at which packets of a specific priority stop being accepted. There are two modes, controlled by the Switch Parameters 1 Register.BUF_ALLOC field, as displayed in Table 26.



The Switch Parameters 1 Register.BUF_ALLOC also controls buffer allocation for the Input Buffers and Crosspoint Buffers.

The CPS-1848 supports an additional option for Final Buffer allocation. If BUF_ALLOC in the Switch Parameters 1 Register is 0, then FB_ALLOC in the same register provides additional options for the number of buffers free when packets of a specific priority are no longer accepted. The options are captured in Table 28. Under congestion, larger buffer allocations allow line rate transfers to occur on links with high latency. However, larger buffer allocations also cause congestion to occur earlier for lower priority packets.

Table 28: Final Buffer Allocation

Priority	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111
3	N/A	N/A	0	0	0	0	0	0
2			2	3	4	5	6	7
1			4	6	8	10	12	14
0			6	9	12	15	18	21

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5. Performance

This chapter discusses the packet switching performance characteristics of the CPS-1848. Topics discussed include the following:

- Overview
- Performance Monitoring
- Performance Measurements
- Port-to-Port Performance Characteristics

5.1 Overview

Performance for packet switching is characterized by three measurements: throughput, latency, and latency jitter. Performance is specified for error-free transmission and reception of packets, and for end-to-end transfers through the CPS-1848.

Performance is specified for a single switch. Performance for larger systems can be computed from this data.

5.1.1 Throughput

Throughput for packets is a measurement of the amount of packet data that can be transferred in a given amount of time. It can be presented in different forms:

- Percentage of a link's bandwidth (for example, 56% of a 1x @ 6.25 Gbaud)
- Number of packets of a given size per unit time (for example, 3000 44-byte packets per second)
- Bit transfer rate (for example, 300 Mbps)

Throughput measurements include only successfully transferred packets. Measured throughput does not include control symbols, retried packets, or other non-packet data transmitted/received on a link (/K/ and /R/ characters).

5.1.2 Latency

Latency is the amount of time between when a packet is received and when it is transmitted. The specific time at which a packet is received and transmitted are deemed to have started, however, must still be defined. Latency is measured as the time interval between the first bit of the Start-of-Packet arriving at the ingress of the CPS-1848 and that same bit leaving the device.

Figure 16 displays the path a packet flows through the CPS-1848. For CPS-1848 latency performance, packet reception time begins with the time the first bit of a packet is seen on the input pins. Packet transmission begins when the first bit of a packet is transmitted on the output pins.

As part of the resolution of resource contention, higher priority packets can pass packets of lower priority. Latencies should therefore increase as the priority of a packet decreases. The latency of higher priority packets are consistently low.

A specific time for packet latency can be specified only when there are no conditions that create resource contention between packets. For example, if a single stream of packets passing from an ingress port to an egress port is the only traffic handled by the CPS-1848, it is possible to specify the latency for the packets in this stream.

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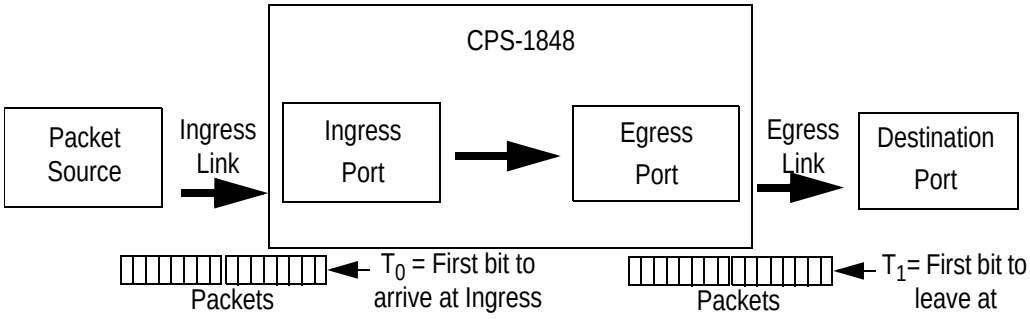
A complex traffic pattern is defined as one that has resource contention, due to congestion. Complex traffic patterns make specifying the exact latency figure that each packet experiences difficult because the amount of contention that a packet experiences can vary widely. As such, these scenarios are not covered in this document.

Figure 16: Latency Example



Latency Equation: Latency = T_1-T_0

5.1.3 Latency Variation

In the CPS-1848, packets can experience an extra one or two clock cycles of delay over the minimum latency when crossing from one clock domain to another clock domain.

Another factor which contributes to latency variation is when the transmitted packet experiences errors on the link. If transmitter-controlled flow control mode is used between the CPS-1848 and the destination port, the CPS-1848 will not send the first bit if the destination has no available buffers.

Multicast packets will have no latency variation from port to port when there are no contentions.

These factors should be considered when creating a system timing budget (see Table 30).

5.2 Performance Monitoring

The main purpose of the performance monitoring functionality is to observe the data traffic on an S-RIO port. The RapidIO traffic can come from different sources – different processing endpoints – and can cause data congestion in one of the destination interfaces. This congestion can have a negative impact on overall system performance. Performance monitoring can be used to identify and help prevent situations that negatively impact system performance.

Performance monitoring decisions can be made by system software in real-time. The system software can be programmed to routinely read the performance monitoring registers, analyze the traffic flow patterns, and re-route accordingly to avoid congestion.

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Each S-RIO port in the CPS-1848 has a copy of the performance monitoring registers. Table 29 lists the statistic parameters that are available from the Inbound and Outbound registers, as part of each port's performance monitoring capabilities.

Table 29: Performance Monitoring Parameters

Parameters	Registers	Description
Number of transmit packets for all priorities (0, 1, 2, and 3)	Port {0..17} VC0 Packets Transmitted Counter Register	Used to count the number of packets sent by an S-RIO link.
Number of receive packets for all priorities (0, 1, 2, and 3)	Port {0..17} VC0 Packets Received Counter Register	Used to count the number of packets received by an S-RIO link.

The following sections describe the use of these parameters for monitoring the performance of the S-RIO ports in the CPS-1848.

5.2.1 Traffic Efficiency

To characterize the efficiency of system traffic, the following parameters are used:

1. Packet rate (number of packets / time) – It is calculated using the number of packets transmitted from the Port {0..17} VC0 Packets Transmitted Counter Register.
2. Average packet size (number of 32-bit words / number of packets) – It is computed with user-supplied value.
3. Utilization ((packet rate * packet size) / max capacity) – It is calculated using parameters 1 and 2.

These values are derived from the number of packets and the number of 32-bit words on each port. The calculations of the packet rate, packet size, and utilization are completed externally.

5.2.2 Congestion Detection

Congestion in the S-RIO ports can be detected by monitoring the counter registers outlined below for the inbound and outbound ports.

The counter registers in the outbound direction are:

- Port {0..17} VC0 Acknowledgements Received Counter Register
- Port {0..17} Not Acknowledgements Received Counter Register
- Port {0..17} VC0 Retry Symbols Received Counter Register

The counter registers in the inbound direction are:

- Port {0..17} VC0 Acknowledgements Transmitted Counter Register
- Port {0..17} Not Acknowledgements Transmitted Counter Register
- Port {0..17} VC0 Retry Symbols Transmitted Counter Register

5.2.3 Resetting Performance Registers

The Receive and Transmit counter registers are cleared after every read and saturate at the maximum counter values.

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5.3 Performance Measurements

Performance measurements for complex traffic patterns can be specified for two different configurations of performance settings. The first configuration is for lightly loaded systems, where the likelihood of resource contention is low. This is known as the “fair share” performance configuration.

The second configuration is for congested systems that optimize the throughput and latency of the highest priority packets at the expense of lower priority packets. This is known as the “high priority” performance configuration.

Configurations that are different from fair share and high priority will have performance figures between the two values.

The switch architecture of the CPS-1848 is optimized for performance under various traffic patterns, and requires minimal changes from the default settings to achieve this requirement. The optimization of the switch supports various traffic conditions where congestion is encountered for specific priority packets used.

With a Combined Input Crosspoint Queue (CICQ) architecture, the input buffer and final buffer do not have to make any agreements. The input buffer distributes packets to crosspoint buffers based on which output port the packet is destined for. The crosspoint buffers help to pull packets from the input buffers to free them so that contention is minimized and to allow more data to flow from the source. Packets are pulled into a port’s final buffer from its crosspoint buffers as they become available. Packets are then fed to the port’s transmission path from the final buffer.

There are, however, a few parameters that require adjustments for specific usage case as listed below:

- Input Buffer, Crosspoint Buffer, and Final Buffer Allocation
  - Buffer Allocation Size
  - Switching Arbitration mode
- Store-and-Forward mode versus Cut-Through mode
- Transmitter-Controlled Flow Control mode versus Receiver-Controlled Flow Control mode

The following sections describe the various modes.

5.3.1 Buffer Management Settings

There are three stages of buffering in the CPS-1848: Input buffer, Crosspoint buffer, and Final Buffer. The Input Buffer can accept up to 12 packets.

Each Crosspoint Buffer can accept up to 9 packets. The final buffer can accept up to 34 packets.

5.3.1.1 Buffer Allocation Size

There are two fields in the Switch Parameters 1 Register that configure the CPS-1848’s buffers. BUF_ALLOC configures both the input buffer and the crosspoint buffer, while FB_ALLOC configures the final buffer if BUF_ALLOC is 0.

The configuration of these fields defines the minimum number of buffer pages that are allocated in a given buffer for each priority. For more information about buffer availability and configuration, see Switch Fabric.

Input and crosspoint buffers have two buffer reservation modes. Single buffer reservation mode is used to minimize the occurrences of congestion, while multi-buffer (double) reservation mode is used to provide high throughput for all priorities when congestion occurs.

In certain traffic conditions, multi-buffer reservation ensures that line rate performance can be maintained for higher priority packets in the event that congestion exists for low priority packets. However, this lowers the maximum number of low priority packets that can be stored in the Input Buffer at a given time.

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Similarly, the final buffer can reserve 1 to 7 buffers per priority level using BUF_ALLOC and FB_ALLOC. The usage case is same as the input buffers. The



The final buffer allocation has a greater impact for switch-to-switch links – endpoints can usually sink packets at line rate.

5.3.1.2 Switching Arbitration Mode

The switching arbitration mode is configured using Switch Parameters 1 Register.ARB_MODE.

5.3.1.2.1 Input Scheduler

The input scheduler uses a fairness mechanism to prevent packets of the same priority from being starved. The fairness mechanism uses a process known as “aging,” whereby each queue has an “age flag” that indicates if the queue is young or old. Each queue also has a counter that is incremented each time a packet of that priority is transferred from the ingress port to the crosspoint buffer. Whenever the counter for a queue exceeds the value programmed in Switch Parameters 1 Register.INPUT_STARV_LIM, the queue is flagged as old. An old queue becomes young when the queue is empty.

The input scheduler determines which queue should be selected for the next transfer using the following algorithm:

1. Determine the highest priority packet(s) that can make forward progress.
2. For those queues at that priority, select the next queue in the round-robin among the old queues.
3. If no old queues exist, select the next queue in the round-robin among the young queues.

This same fairness mechanism is used to ensure multicast throughput. A multicast transaction can be sent simultaneously to all target crosspoint buffers. If it is not sent simultaneously, the multicast transaction becomes old and is given priority over all other flows in the queue of the same SRIO priority.

5.3.1.2.2 Output Scheduler

The output scheduler uses a proportional fairness algorithm to select from multiple crosspoint buffers in order to move a packet to the final buffer. A round-robin mode is also available that instead of trying to achieve fairness for all outbound data, it supports priority-based round-robin arbitration. The proportional fairness algorithm implements credit-based arbitration for bandwidth allocation. The main purpose of the proportional fairness algorithm is to provide equal share of bandwidth to move packets from a port's set of crosspoint buffers to its final buffer.

There are three parameters for configuring the fairness of the output arbitration algorithm:

- OUTPUT_CREDIT_RSVN in the Switch Parameters 1 Register
- OUTPUT_CREDIT_MIN and OUTPUT_CREDIT_MAX in the Switch Parameters 2 Register

The Output Credit Minimum/Maximum values set the bounds for the minimum and maximum number of credit values that can accumulate. For normal operation, the default values in these registers do not need to be modified. The OUTPUT_CREDIT_RSVN is used to adjust the credit allocation for each crosspoint buffer. There is no single value that is optimal for all traffic conditions. However, in general a small value is optimal for smaller packets while for maximum sized packets, the default value (2 maximum sized packets) should provide more proportional fairness. For mixed sized packets, a value somewhere in between should produce more optimal results.



When using 17 or 18 ports of the CPS-1848, software must set the default credit count to be less than 455 for all ports using Switch Parameters 1 Register[OUTPUT_CREDIT_RSVN].

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5.3.2 Store-and-Forward or Cut-Through Mode

The CPS-1848 supports two buffer management modes: Store-and-Forward and Cut-Through. Store-and-Forward mode ensures an incoming packet is completely received before it is forwarded, while the use of Cut-Through mode forwards the incoming packet as soon as possible.

The Store-and-Forward mode is the default mode. Use Cut-Through mode only if all active ports have the same capacity (for example, all ports are 2x with a lane rate of 5 Gbps). The selection of Store-and-Forward and Cut-Through mode for all input ports is made using CUT_THRU_EN in the Device Control 1 Register.

5.3.3 Transmitter-Controlled or Receiver-Controlled Flow Control Mode

Receiver- and transmitter-controlled flow control are the most basic flow control functions supported by RapidIO. One of these functions is always active on a link. The choice between receiver- and transmitter-controlled flow control is made automatically as part of the Port and Lane Initialization Sequence.

5.3.3.1 Transmitter-Controlled Flow Control

Transmitter-controlled flow control is the default mode for each port. In this mode, the transmitter sends packets only when the link partner has indicated that it has available input buffer space to receive them.

Buffer watermarks are used to manage the link-partners receive buffers. It restricts the transmission of lower priority packets to the advantage of higher priority packets. Watermark settings directly affect throughput and indirectly latency and latency variation. For more information on watermarks, see Port {0..17} Watermarks Register.



The watermark settings need to be configured based on the link partner's buffers and buffer management.

The default watermark settings should be used for the *fair share* configuration for both S-RIO ingress buffer management and S-RIO egress buffer management.

The default watermark settings are aligned with the RapidIO specification as follows:

- Last buffer is reserved for priority 3 packet
- Second last buffer is reserved for a priority 2 or 3 packet
- Third last buffer is reserved for a priority 1, 2 or 3 packet
- All other buffers may be used by packets of any priority

5.3.3.2 Receiver-Controlled Flow Control

In receiver-controlled flow control, the receiver informs the transmitter when it cannot accept a packet by issuing a retry (usually because of a lack of resources). The transmitter may resume packet transfer with a packet of higher priority than the one that was retried, if such a packet is available.

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5.4 Port-to-Port Performance Characteristics

The performance numbers in this section use a simple measurement consisting of a port-to-port traffic model to characterize the maximum throughput and minimum latency performance of the CPS-1848. In this case, all traffic is of the same size and priority. Due to the simple type of traffic, the throughput and latency performance numbers do not change with the priority of the packets.

5.4.1 Packet Latency Performance

Table 30 shows the 4x, 2x, and 1x mode latency numbers under no congestion with default arbitration and watermark settings. The numbers are based on the same ingress and egress port widths and baud rates. The minimum latency is the minimum time an ingress packet takes to appear on the egress port.



Cut-through mode is assumed to be configured when measuring latency performance.

Table 30: 4x/2x/1x Latency Numbers Under No Congestion

Reference Clock	Ingress and Egress Port Width	Ingress and Egress Baud Rate (Gbaud)	Minimum Latency (ns)[1]
156.25 MHz	4x mode	6.25	106.0
		5,0	111.6
		3.125	128.4
		2.5	139.6
		1.25	195.6
	2x mode	6.25	109.2
		5.0	115.6
		3.125	134.8
		2.5	147.6
		1.25	211.6
	1x mode	6.25	115.6
		5.0	123.6
		3.125	147.6
		2.5	163.6
		1.25	243.6

1. Due to the asynchronous ability of the clock frequencies within the CPS-1848, the latency numbers can increase by as much as two 312.5 MHz clock period and two reference clock (REF_CLK) period.

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5.4.1.1 Packet Acknowledge Latency

Packet throughput can also be limited by the speed at which a port can issue a Packet-Accepted control symbol to its link partner. The *RapidIO Specification (Rev. 2.1)* requires an egress port to retain a transmitted packet in its transmit buffer until it has received a Packet-Accepted control symbol for the packet. Once the transmitting port has received the control symbol, the packet can be discarded from the buffer. If a system contains devices with varying EOP-Packet-Accepted latencies, in the condition where the fabric can issue Packet-Accepted to the source of the packets in a shorter time relative to the speed at which the target of the packets can, the fabric may congest and begin applying backpressure to the source in order to pace the flow of packets to the target.

Table 31 lists the typical latency from the receipt of a packet EOP to the issuance of a Packet-Accepted control symbol.

Table 31: Typical Latency from Receipt of Packet EOP to Packet Accept Issuance

Received Packet Type	Typical Latency
NRead Request	127 ns
NRead Response	100 ns
NWrite Request	127 ns
Maintenance Read	122 ns
Maintenance Read Response	102 ns
Maintenance Write	128 ns
Maintenance Write Response	96 ns

5.4.2 Packet Throughput Performance

Packet throughput varies from the packet type, availability of resources within the CPS-1848, ability for source and destination of traffic to generate or receive packets, retries of packet, and actual data rates.

A *bubble* is a control symbol inserted by an egress port into a packet to maintain the baud rate of the port. The appearance of a bubble indicates that the egress port is under-utilized.

In a typical application, an S-RIO packet stream consists of an Start-of-Packet (SOP) control symbol followed by a payload. However, with certain packet types, the CPS-1848 injects an End-of-Packet (EOP) control symbol following the payload.



All packets that are non-modulo-8 including header and payload that use an IDLE1 control symbol, will experience a slight performance degradation due to this bubble phenomenon.

Another factor affecting the performance of an S-RIO link is the protocol's requirement for the transmitting port to insert the /K/R/R/R/ clock compensation sequence at least once every 5000 code groups. The insertion of the clock compensation sequence can occur transparently or non-transparently depending on the proximity of outbound packets to the 5000 code group boundary.

Based on the traffic on the link as the code group approaches 5000, one of the following behaviors will occur:

- If the link is transmitting IDLE characters, the clock compensation sequence will be inserted transparently into the idle stream.
- If packets are being transmitted and there are gaps between the packets, the port will attempt to insert the clock compensation sequence between the packet delimiting control symbols.

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- If packets are being transmitted back-to-back with no idle gaps between the packets, and the 5000 code group boundary has arrived, the current packet will be stomped and the clock compensation sequence will be inserted. The stomped packet will then be re-transmitted in its entirety.

5.4.2.1 One Port-to-One Port Throughput Performance

Under a non-congested port-to-port packet traffic situation and non-bubble condition, when the ingress and egress ports have the same baud rate (1.25, 2.5, 3.125, 5.0, or 6.25 Gbaud), the ingress and egress can maintain back-to-back (line rate) packet transfers.

When the ingress line rate exceeds the egress port's line rate, a retry occurs at the ingress port when the buffer is filled to the capacity permitted by the priority of the packets. The egress port still maintains its maximum packet rate with no bubble.

5.4.2.2 Many Ports-to-One Port Throughput Performance

Under a non-congested and non-bubble condition, many ports-to-one port packet traffic scenario, when all of the total ingress line rates are the same as the egress line rate (for example, four 1x mode, 6.25 Gbaud ingress ports all going to one 4x mode, 6.25 Gbaud egress port), the ingress port and egress port will always maintain line rates. This means there will be no retry of packets at the ingress and no bubble occurring in the egress packet streams. This is true for any payload size and different priorities. The arbitration scheme within the CPS-1848 allocates sufficient bandwidth for each ingress port.

When the total of the ingress line rates exceeds that of the egress port, retries occur at one or more of the ingress ports if the packet density exceeds the capacity of the egress port. The egress port still maintains its maximum packet rate with no bubble. This is true for any payload size and priorities.

5.4.2.3 One Port-to-Many Port Throughput Performance

Under a non-congested and non-bubble condition, one port-to-many ports packet traffic scenario, when the ingress line rate is the same as the total egress line rates – for example one 4x mode, 6.25 Gbaud ingress port splitting to four 1x mode, 6.25 Gbaud egress ports – the ingress and egress always maintain line rates. This means there is no retry of packets in the ingress port and no bubble-packet in the egress packet streams. This is true for any payload size and different priorities. The arbitration scheme within the CPS-1848 divides the traffic according to the egress port bandwidths.

When the ingress line rate exceeds that of the total of the egress ports, retries occur at the ingress port when the packet density exceeds the buffer capacity. The egress ports still maintain their maximum packet rates with no bubble. This is true for any payload size and priorities.

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5.4.3 Multicast Latency Performance

Since multicast involves more than one egress port and each egress port can have independent traffic conditions, a multicast packet can appear at the destination egress ports at different times. A minimum multicast latency is defined as the shortest time from the arrival of the first bit of a packet at an ingress port that will be multicast, to the appearance of the first bit of the multicast packet at an egress port under no resource contention.

Table 32: 4x/2x/1x Multicast Latency Numbers Under No Congestion

Ingress and Egress Port Width	Ingress and Egress Baud Rate (Gbaud)	Minimum Latency (ns)[1]	Maximum Latency (ns)[1 2]
4x mode	6.25	106.0	114.2
	5.0	111.6	120.6
	3.125	128.4	135.0
	2.5	139.6	152.6
	1.25	195.6	216.6
2x mode	6.25	109.2	117.4
	5.0	115.6	124.6
	3.125	134.8	141.4
	2.5	147.6	160.6
	1.25	211.6	232.6
1x mode	6.25	115.6	123.8
	5.0	123.6	132.6
	3.125	147.6	154.2
	2.5	163.6	176.6
	1.25	243.6	264.6

1. Due to the asynchronous ability of the clock frequencies within the CPS-1848, the latency numbers can vary as much as two 312.5 MHz clock period and two reference clock (REF_CLK) period.
2. Under no contention, the minimum variation is 0 ns.

5.4.4 Multicast Throughput Performance

The maximum input payload bandwidth of a CPS-1848 S-RIO port is 20 Gbps. This corresponds to a line rate of 4x mode, 6.25 Gbaud at the ingress port. The maximum input bandwidth of a port can be sourced from one ingress port or multiple ingress ports.

When any of the egress ports has a line rate lower than the ingress port's bandwidth, retries occur at the ingress port. In this situation, the egress port maintains its line rate. For example, when an egress port is set to 4x mode, 2.5 Gbaud while the ingress port is receiving a single or aggregated input data at maximum 20 Gbps, retries happen at the ingress port(s). However, the egress port still maintains its line rate with no bubble inserted in the packet stream.

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5.4.5 Multicast-Event Control Symbol (MECS) Latency

The propagation time (delay) of the notification for both receipt of MECS and External pin triggered are listed in Table 33.

Propagation delay is specified using the maximum value of Multicast-Event forwarding delay through the switch. Variation in propagation time can be derived using maximum forwarding delay minus the minimum forwarding delay through the switch.

Table 33: 4x/2x/1x Multicast-Event Control Symbol Latency Numbers

Ingress and Egress Port Width	Ingress and Egress Baud Rate (Gbaud)	Receipt of Control Symbol (ns)		Triggered by External Pin (ns)	
		Minimum	Maximum	Minimum	Maximum
4x mode	6.25	112.4	147.6	79.4	98.6
	5.0	118.8	154.0	84.2	103.4
	3.125	138.0	173.2	98.6	117.8
	2.5	150.8	186.0	108.2	127.4
	1.25	214.8	250.0	156.2	175.4
2x mode	6.25	115.6	150.8	79.4	98.6
	5.0	122.8	158.0	84.2	103.4
	3.125	144.4	179.6	98.6	117.8
	2.5	158.8	194.0	108.2	127.4
	1.25	230.8	266.0	156.2	175.4
1x mode	6.25	122.0	157.2	79.4	98.6
	5.0	130.8	166.0	84.2	103.4
	3.125	157.2	192.4	98.6	117.8
	2.5	174.8	210.0	108.2	127.4
	1.25	262.8	298.0	156.2	175.4

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6. Event Management

This chapter discusses the event (error) management capabilities of the CPS-1848. Topics discussed include the following:

- Event Management Overview
- Event Detection
- Event Notification
- Event Isolation
- Event Clearing and Recovery

6.1 Event Management Overview

Event management consists of four distinct steps. These steps can also be followed when designing the error management system:

1. Event Detection – Which events should be detected, and what information should be captured for each event.
2. Event Notification – What notification function (interrupts, port-writes, none) should be triggered when an event is detected.
3. Isolation/automatic reactions to events – How can the CPS-1848 prevent the event from impacting the remainder of the system.
4. Event Recovery/Clearing events – How to determine what event occurred, how to clear the event, how to recover from the event.

The CPS-1848 can detect a large number of events. Many events related to RapidIO protocol errors are always detected. Other events are detected only when the CPS-1848 is configured to do so. Detected events may cause the capture of related information.

Figure 17 shows the event categories that comprise the event management scheme. Each event category has reporting control values for individual events. The diagram shows the relationship of control values for event reporting. Table 34 lists the register bits that enable the various types of events.

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Figure 17: Event Management Overview (Revision A/B)

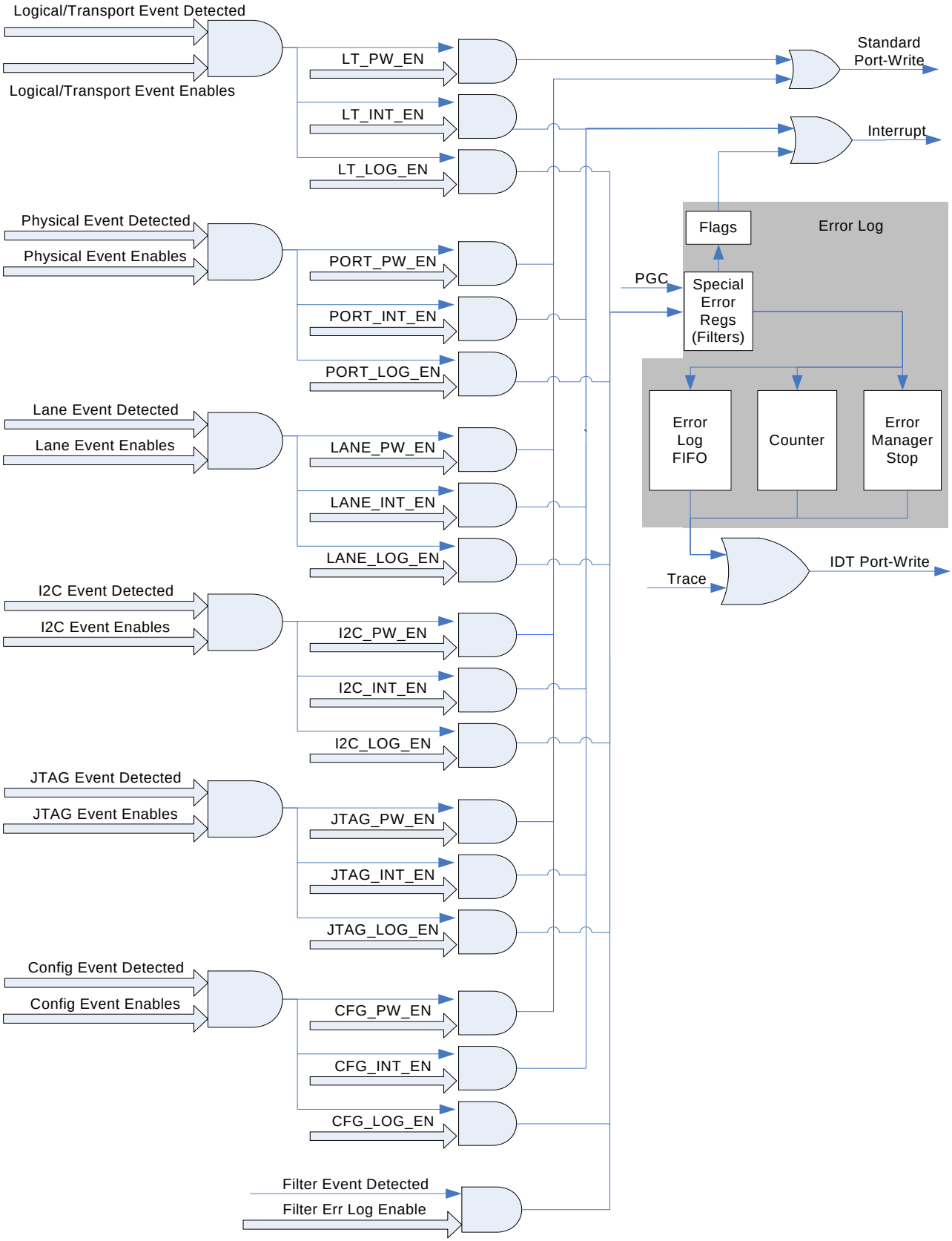

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Figure 18: Event Management Overview (Revision C)

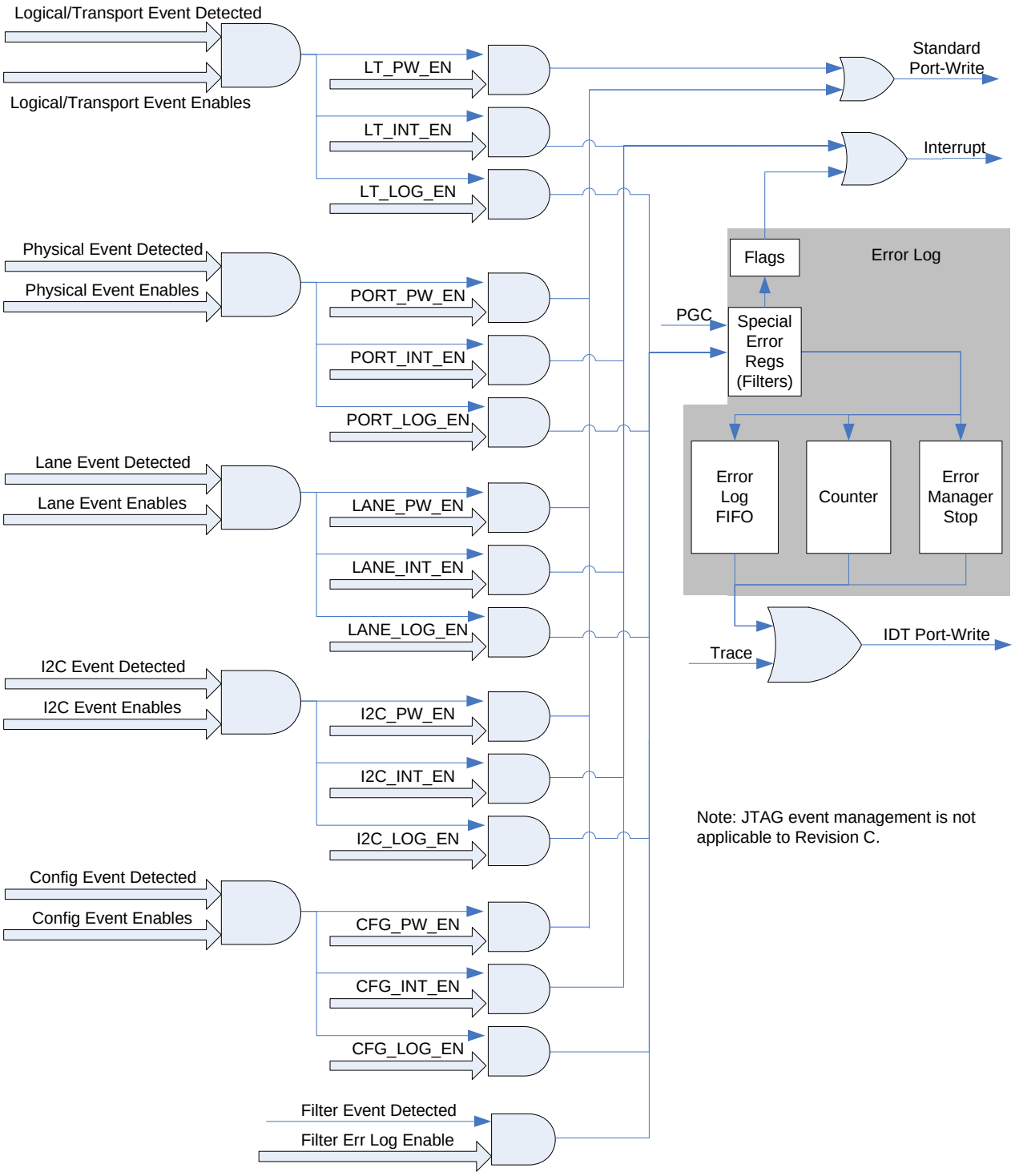

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Table 34: Event Management Enable Bits

Event Category	Enable Bits
Logical/Transport	Device Control 1 Register.LT_PW_EN Device Control 1 Register.LT_INT_EN Port {0..17} Operations Register.LT_LOG_EN
Physical	Port {0..17} Operations Register.PORT_PW_EN Port {0..17} Operations Register.PORT_INT_EN Port {0..17} Operations Register.PORT_LOG_EN
Lane	Lane {0..47} Control Register.LANE_PW_EN Lane {0..47} Control Register.LANE_INT_EN Port {0..17} Operations Register.LANE_LOG_EN
I2C	I2C Master Control Register.I2C_PW_EN I2C Master Control Register.I2C_INT_EN Aux Port Error Report Enable Register.I2C_LOG_EN
JTAG[1]	JTAG Control Register (Revision A/B).JTAG_PW_EN JTAG Control Register (Revision A/B).JTAG_INT_EN Aux Port Error Report Enable Register.JTAG_LOG_EN
Configuration	Configuration Block Error Report Register.CFG_PW_EN Configuration Block Error Report Register.CFG_INT_EN Configuration Block Error Report Register.CFG_LOG_EN

1. JTAG Event Management is applicable to Revision A/B only.

The CPS-1848 has two functions for notifying a software entity that it has detected an event: a port-write and an interrupt signal. A RapidIO port-write packet is a type of maintenance packet “in band” notification of an event. These packets are sent at the recommended highest priority and can always make forward progress through the CPS-1848. Event notification can also be performed using the interrupt output signal, IRQ_N, which may be directly connected to the interrupt input of another device.

An interrupt is asserted and standard port-writes are sent when an enabled event is detected. Interrupts are asserted until the event is cleared or disabled in the associated interrupt enable register.

If port-write reporting is enabled, a port-write that conforms to the Part 8 Error Management Extensions format of the *RapidIO Specification (Rev. 2.1)* will be sent. If Error Log reporting is enabled, the encoded event is preserved in the Error Log and may, depending on Error Log settings, trigger the transmission of an IDT port-write. For more information about standard and IDT port-writes, see Port-Write Formats, Programming Model, and Generation. For more information about the Error Log functionality, see Error Log Event Notification Programming Model.

A detected event that has event reporting enabled may trigger one or more event reporting functions. The CPS-1848 interrupt signal, for example, may be asserted if the interrupt enable for that category of event is set. For more information about interrupts, see Interrupt Notification.

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Some events indicate that the CPS-1848's link partner cannot accept packets. Packets routed to the failed link partner will therefore cause congestion in the CPS-1848, and may eventually lead to system failure. Depending on the system's fault tolerance strategy, the CPS-1848 can be configured to retain packets, discard packets on transmission errors, or discard all packets sent to the failed link partner.

Once the system maintenance software has been notified of an event, this software is responsible for reacting to the event and clearing the event.

Some events have a different event reporting design. Trace events, filter events, and PGC mode events are reported only through the Error Log. IDT port-writes can be sent depending on the Error Log configuration.

6.1.1 Logical/Transport Layer Events Overview

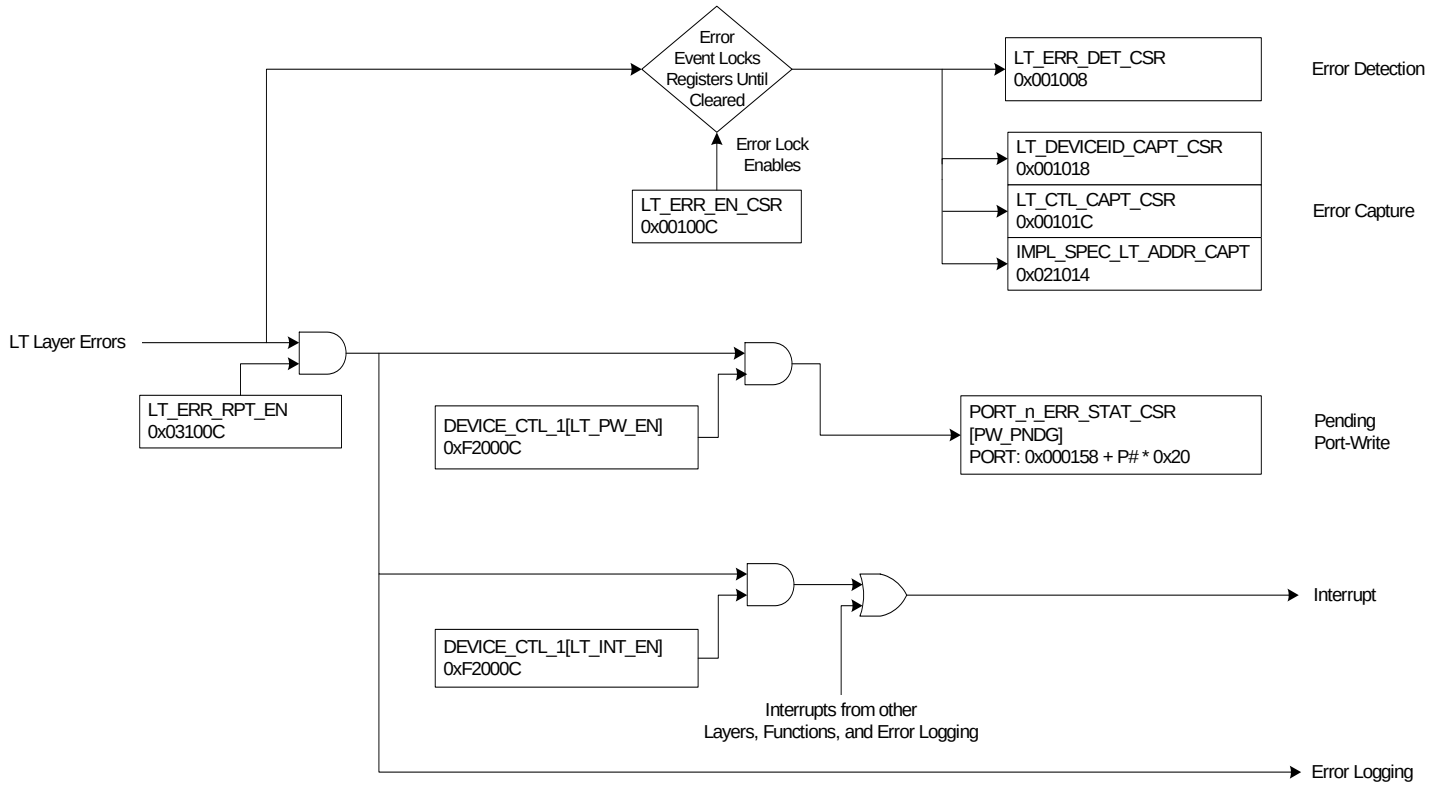
Logical/transport layer events supported by switches are defined in the *RapidIO Interconnect Specification (Revision 2.1)*, Part 8 Error Management Specification. Errors are always detected but only captured when enabled. Errors are enabled in the Logical/Transport Layer Error Enable CSR, and are indicated in the Logical/Transport Layer Error Detect CSR. Information about the packet that contained the detected error is latched in the Logical/Transport Layer deviceID Capture CSR, Logical/Transport Layer Control Capture CSR, and Impl. Specific Logical/Transport Layer Address Capture Register.

Logical/transport layer events enabled in the Logical/Transport Layer Error Report Enable Register can be reported through port-writes or interrupts, and captured in the error log, depending on the configuration of the registers as shown in Figure 19.

Port-writes and interrupts are disabled by default for Logical/Transport layer events.

The same settings should be used in the Logical/Transport Layer Error Report Enable Register and Logical/Transport Layer Error Enable CSR; otherwise, different settings may result in not reporting detected events, or port-writes/interrupts with no indication of the cause.

Figure 19: Logical/Transport Layer Error Management Programming Model Flow Chart



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6.1.2 Physical Layer Error Management Overview

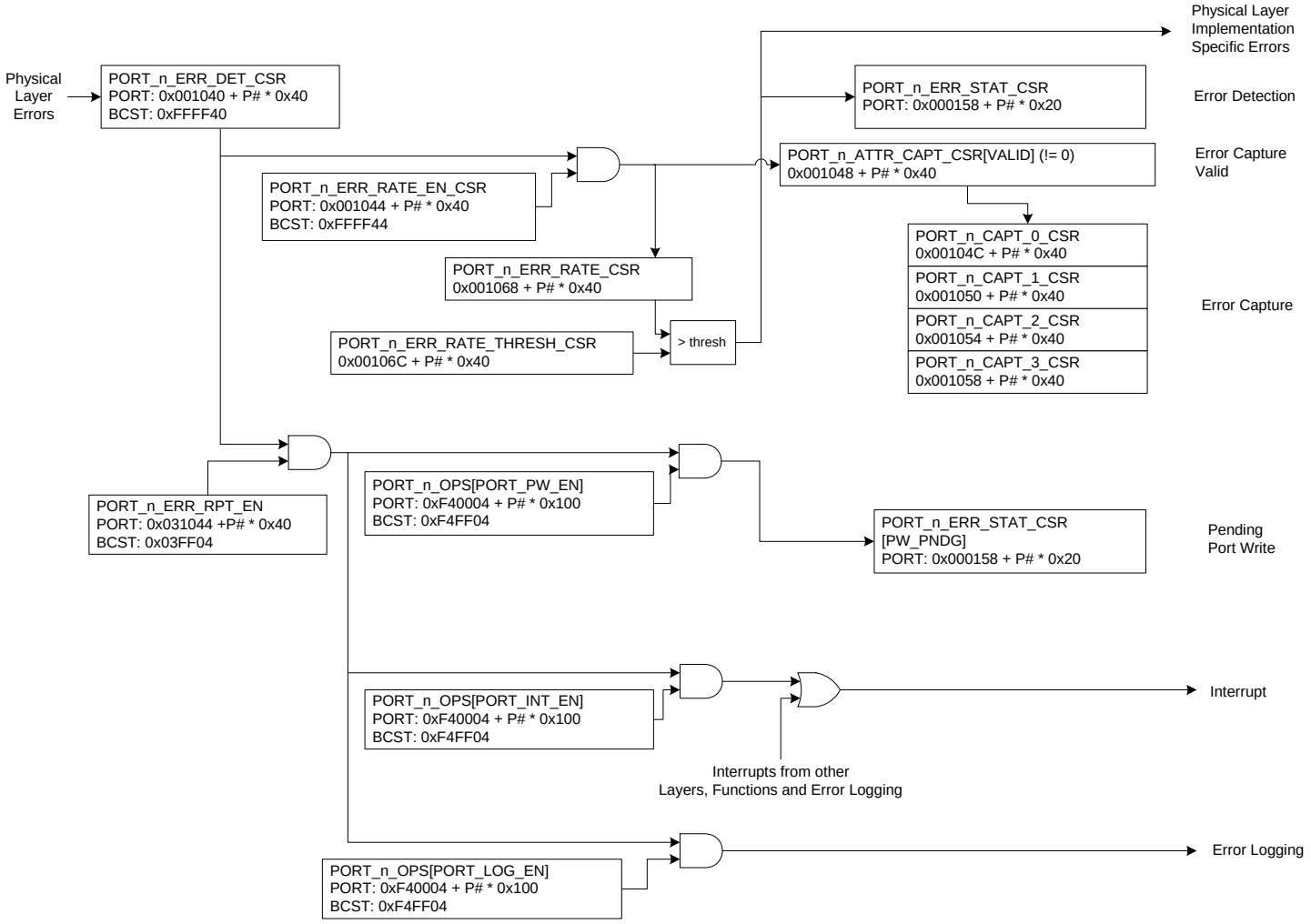
The CPS-1848 can detect many types of physical layer errors. Physical layer errors are grouped into "Standard" physical layer errors, which are defined by the *RapidIO Interconnect Specification (Revision 2.1)*, Part 8 Error Management Specification, and "Implementation Specific" errors, which are specific to IDT devices. These two types have slightly different programming models, as displayed in Figure 20 and Figure 21.

Standard physical layer errors are always indicated in the Port {0..17} Error Detect CSR. When enabled in the Port {0..17} Error Rate Enable CSR, error information is captured for the events in the four error capture registers, Port {0..17} Capture 0 CSR to Port {0..17} Capture 3 CSR; enabled events are also counted. If the event counts exceed the threshold values programmed in the Port {0..17} Error Rate Threshold CSR, additional events are detected and isolation can be triggered. Events enabled in the Port {0..17} Error Report Enable Register can be reported to software using port-writes or interrupts, or captured in the error log, depending on the configuration of the registers displayed in Figure 20.

Port-writes and interrupts are disabled by default for individual Standard Physical Layer events.

Individual Standard Physical Layer Errors should not be enabled in the Port {0..17} Error Report Enable Register because these occur at a rate consistent with the bit error rate of the lanes associated with each port, and therefore are part of the normal operation of the system.

Figure 20: Standard Physical Layer Error Management Programming Model Flow Chart



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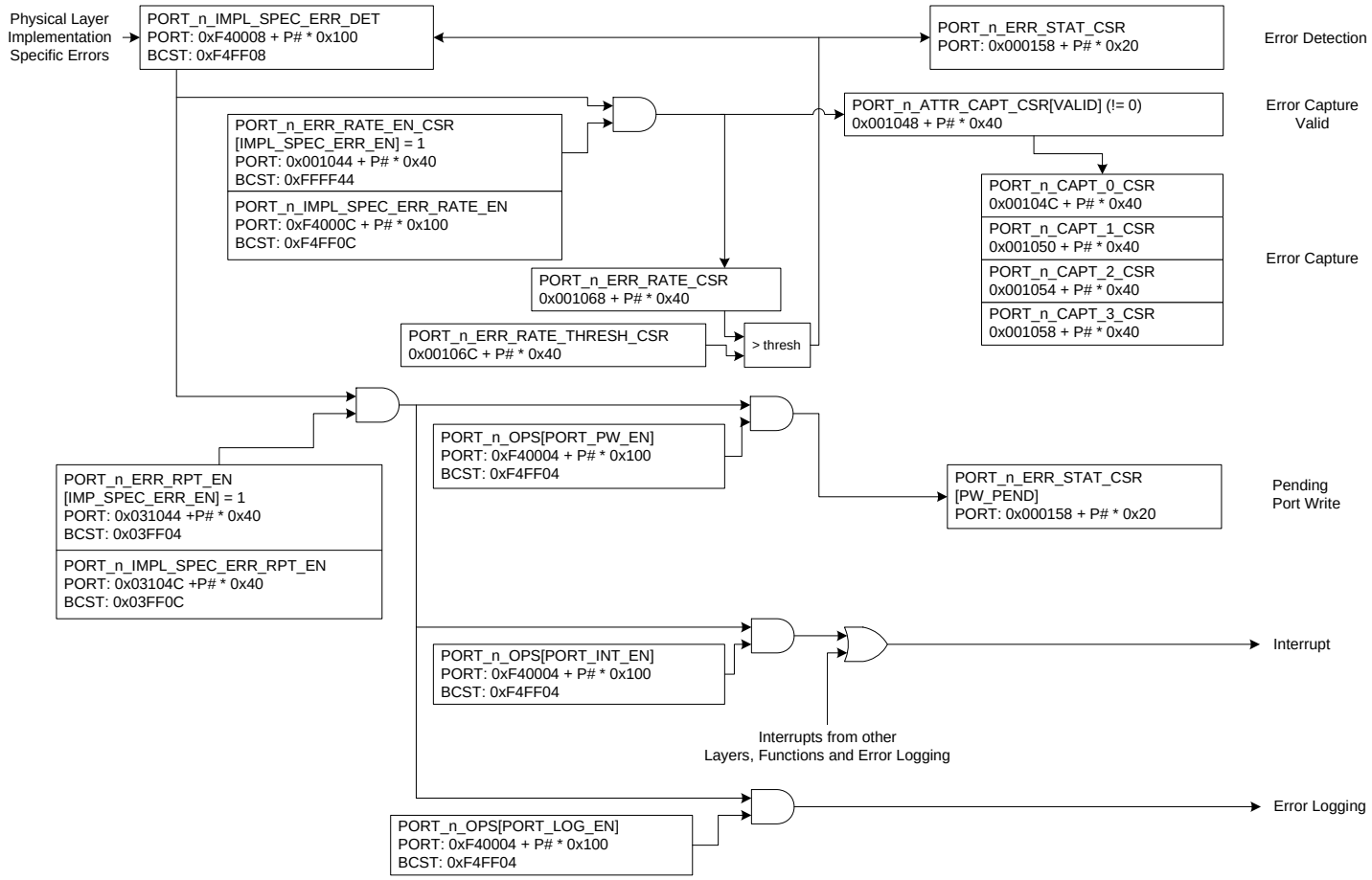
Implementation-specific physical layer errors are all reported through the IMP_SPEC_ERR bit in the Port {0..17} Error Detect CSR. When events are enabled in the Port {0..17} Implementation Specific Error Rate Enable Register, the events contribute to the Standard error counters and thus can trigger threshold events, as displayed in Figure 21. Events enabled in this register can be reported to software using port-writes or interrupts, or captured in the error log, depending on the configuration of the registers displayed in Figure 21.

Port-writes and interrupts are disabled by default for individual Standard Physical Layer events.

Individual Implementation Specific Physical Layer Errors should not be enabled in the Port {0..17} Implementation Specific Error Report Enable Register because these occur at a rate consistent with the bit error rate of the lanes associated with each port, and therefore are part of the normal operation of the system.

Figure 21: Implementation Specific Physical Layer Error Management Programming Model Flow Chart



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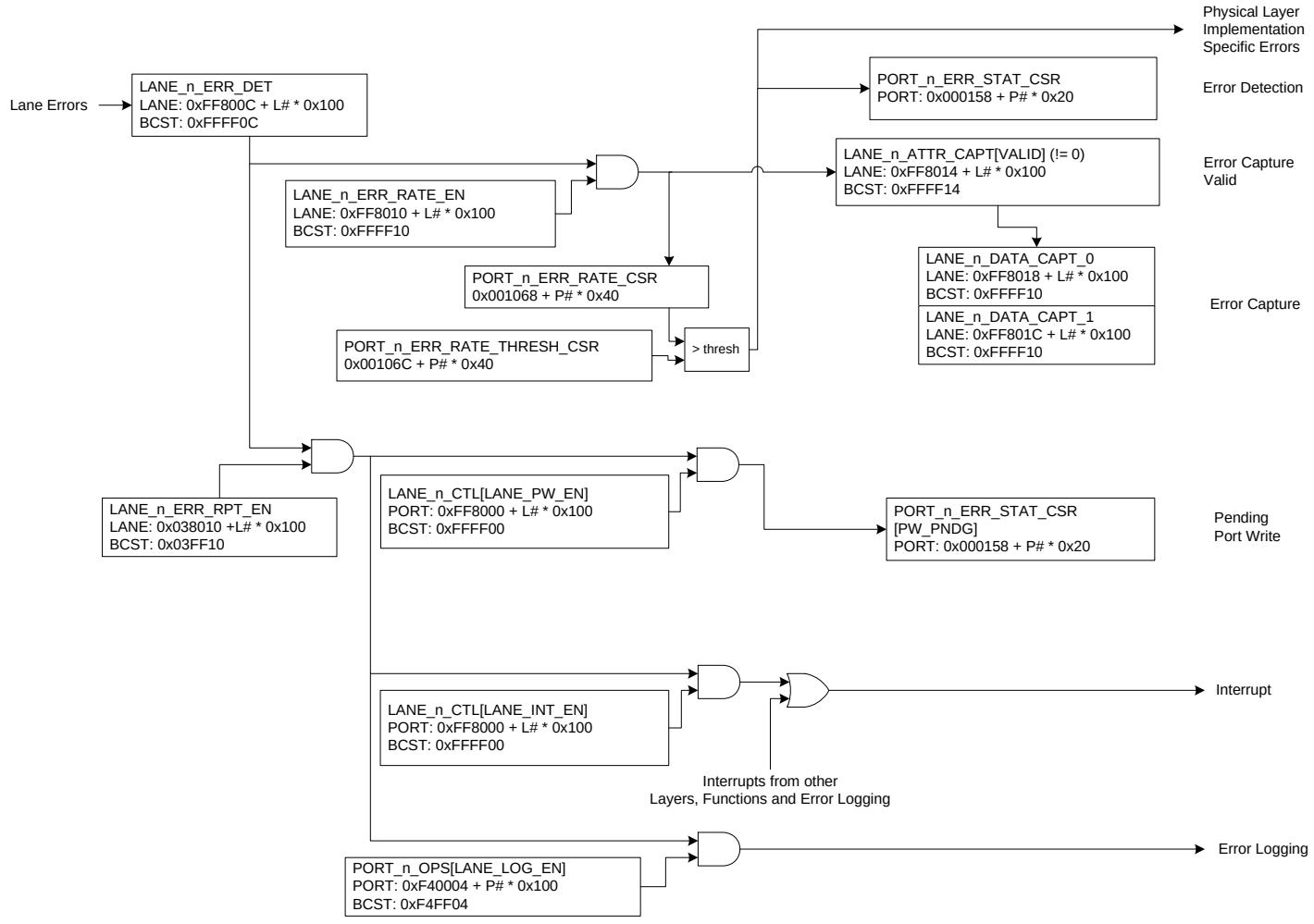
6.1.3 Lane Error Management Overview

Each CPS-1848 port is connected to 1, 2, or 4 lanes. Each lane can detect and report errors. Errors detected at the lane level are indicated in the Lane {0..47} Error Detect Register. Information about lane events is captured if the event is enabled in the Lane {0..47} Error Rate Enable Register. Enabled events also contribute to the standard port error threshold events if the IMP_SPEC_ERR bit is set in the Port {0..17} Error Detect CSR. Events enabled in the Lane {0..47} Error Report Enable Register can be reported to software using port-writes or interrupts, or captured in the error log, depending on the configuration of the registers displayed in Figure 22.

Port-writes and interrupts are disabled by default for individual Lane events.

Individual lane errors should not be enabled in the Lane {0..47} Error Report Enable Register because these occur at a rate consistent with the bit error rate of each lane, and therefore are part of the normal operation of the system.

Figure 22: Lane Error Management Programming Model Flow Chart



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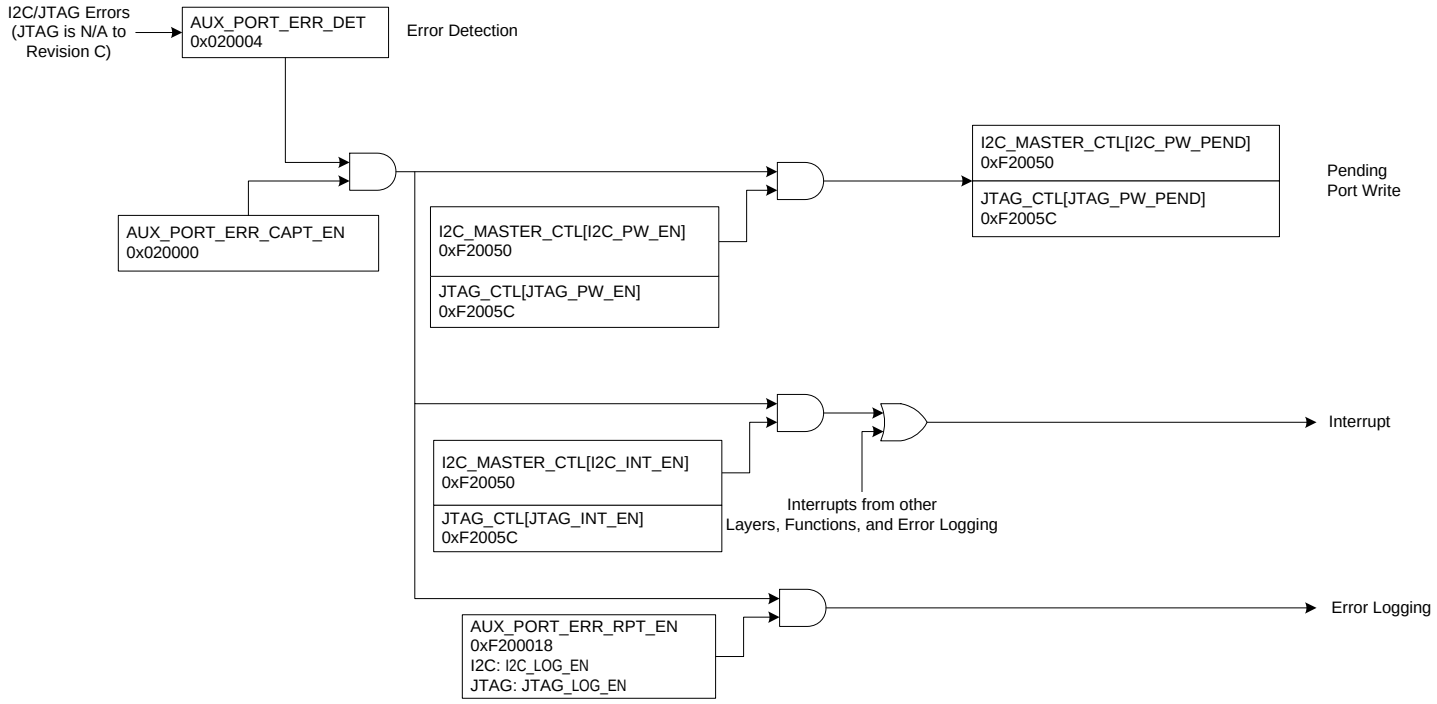
6.1.4 I²C Error Management Overview

I²C events are always indicated in the Aux Port Error Detect Register. I²C events that are enabled in the Aux Port Error Capture Enable Register can be reported to software using port-writes or interrupts, or captured in the error log, depending on the configuration of the registers displayed in Figure 23.

Figure 23: I2C Error Management Programming Model Flow Chart



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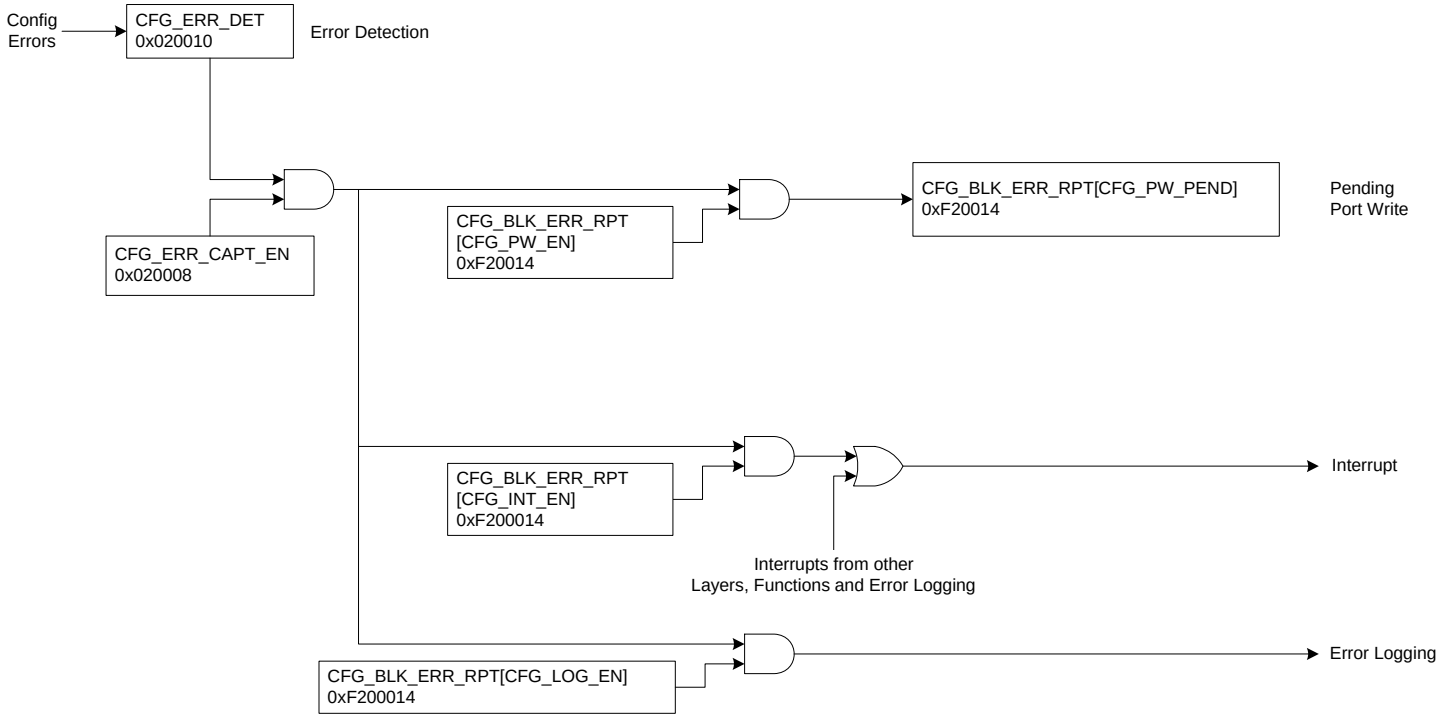
6.1.5 Configuration Error Management Overview

Configuration events are always indicated in the Configuration Block Error Detect Register. Configuration events that are enabled in the Configuration Block Error Capture Enable Register can be reported to software using port-writes or interrupts, or captured in the error log, depending on the configuration of the registers displayed in Figure 23.

Figure 24: Configuration Error Management Programming Model Flow Chart



6.2 Event Detection

The CPS-1848 detects the following types of events:

- Logical and Transport Layer Events
- Physical Layer Events
- Lane Events
- I2C Events
- JTAG Events (Revision A/B Only)
- Configuration Block Events
- Trace and Filter Events
- Packet Generation and Capture Mode Events
- Error Log Events

6.2.1 Logical and Transport Layer Events

This type of error is caused by incorrect maintenance requests (for example, Maintenance Read Size Invalid) and maintenance responses (for example, unsolicited responses). The detection of logical and transport layer events is controlled by the Logical/Transport Layer Error Enable CSR.

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The CPS-1848 detects transport layer events (that is, ILL_TRAN) for all packets. The device detects logical layer events for maintenance packets only when they have a hop count of 0. For more information on these events, see the Logical/Transport Layer Error Detect CSR.

Logical and Transport layer events are listed in Table 35. This table has four columns:

- Event Name – The short form by which the event is identified.
- Detection Enable – Any register settings required to enable detection of the event. “Always Detected” means that there are no controls to disable detection of the event.
- Information Capture Enable – The register settings required to enable the event to have information captured, and to enable notification.
- Information Captured – Summary of information captured for the event, as well as status bit that indicate the event was detected. Multiple status bits may be set, however, information is captured only for the first enabled event. Subsequent events do not have any information captured. The Information Captured column contains two values:
  - Standard: Information is captured in the Logical/Transport Layer deviceID Capture CSR, Logical/Transport Layer Control Capture CSR, and Impl. Specific Logical/Transport Layer Address Capture Register.
  - Standard, no address: Information is captured in the Logical/Transport Layer deviceID Capture CSR and Logical/Transport Layer Control Capture CSR. No information is captured in the Impl. Specific Logical/Transport Layer Address Capture Register.



The CPS-1848 does not support the RapidIO standard address capture register for logical layer errors.



Multiple errors in the same packet may cause multiple bits to be set in the Logical/Transport Layer Control Capture CSR. For example, a Maintenance Read Size Invalid error and a Maintenance Received with Data error are both detected when a Maintenance Read Request has the dual defects of requesting more than 64 bytes and includes data.

Table 35: Logical/Transport Layer Event Enable and Information Capture Summary

Event	Detection Enable	Information Capture Enable	Information Captured
Illegal transaction decode	Always Detected	Logical/Transport Layer Error Enable CSR.ILL_TRAN_EN	Standard
Unsolicited response	Always Detected	Logical/Transport Layer Error Enable CSR.UNSOL_RESP_EN	Standard, no address
Unsupported transaction	Always Detected	Logical/Transport Layer Error Enable CSR.UNSUP_TRAN_EN	Standard, no address
Maintenance read size invalid	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 31]
Maintenance write size invalid	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 30]

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Table 35: Logical/Transport Layer Event Enable and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Maintenance read received with data	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 29]
Maintenance write received without data	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 28]
Maintenance packet received was too short or too long	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 27]
Maintenance transaction field error	Always Detected	Logical/Transport Layer Error Enable CSR. IMP_SPEC_ERR_EN	Standard. Logical/Transport Layer Control Capture CSR.IMP_SPEC [Bit 25]

6.2.2 Physical Layer Events

Physical layer events are events related to reliable packet transfers such as transmission errors and protocol errors. Most physical layer events trigger the standard RapidIO error recovery function, which ensures packet delivery. A low rate of transmission errors will occur on a RapidIO link.

RapidIO physical layer events are in Table 37. This table has four columns:

- Event Name – The short form by which the event is consistently identified.
- Detection Enable – Any register settings required to enable detection of the event. “Always Detected” means that there are no controls to disable detection of the event.
- Information Capture Enable – The register settings required to enable the event to supply the leaky bucket. These register settings also enable capture of information associated with the event.
- Information Captured – Summary of information captured for the event, as well as status bit which indicates the event was detected. Multiple status bits may be set, however information is only captured for the first enabled event. Subsequent events do not have any information captured. The values in the “Information Captured” column are described in Table 36.

Table 36: Physical Layer Events Information Captured Value Descriptions

Value	Description
No Info	No information is captured for this event.
Control Symbol	Control symbol information is captured for the event. This information is in the following registers: Port {0..17} Attributes Capture CSR Port {0..17} Capture 0 CSR Port {0..17} Capture 1 CSR. Note that information is located only in the Port {0..17} Capture 1 CSR if IDLE2/long control symbols are active.

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Table 36: Physical Layer Events Information Captured Value Descriptions *(Continued)*

Value	Description
Packet	Packet information is captured for the event. This information is in the following registers: Port {0..17} Attributes Capture CSR: INFO_TYPE is 0b100 Port {0..17} Capture 0 CSR Port {0..17} Capture 1 CSR Port {0..17} Capture 2 CSR Port {0..17} Capture 3 CSR For base address information, see Port Error Management Register Base Addresses. Note: Depending on the length of the packet received, some of the registers may not contain valid data. Up to 16 bytes of packet data can be captured, starting from the first byte of the received packet. Note: The first byte of the received packet includes the ackID used for that packet.
Destriped Data	Eight data characters are captured for the event. This information is in the following registers: Port {0..17} Attributes Capture CSR: INFO_TYPE is 0b100 Port {0..17} Capture 0 CSR contains the most significant 4 bytes of the destriped 8 bytes of data. Port {0..17} Capture 1 CSR contains the least significant 4 bytes of the destriped 8 bytes of data.
Register	The written register data that caused the event is captured. This information is in the following registers: Port {0..17} Attributes Capture CSR: INFO_TYPE is 0b100 Port {0..17} Capture 0 CSR contains the 4 bytes of data written to the register.
AckID	Captures the ackID associated with a timeout error. This information is in the following registers: Port {0..17} Attributes Capture CSR: INFO_TYPE is 0b100 Port {0..17} Capture 0 CSR[22] indicates the type of timeout. 0 = Packet Acknowledge timeout 1 = Link-Response timeout Port {0..17} Capture 0 CSR[26:31] contains the ackID value that timed out
Downgrade	Port {0..17} Attributes Capture CSR: INFO_TYPE is 0b100 Encoding of link width downgrade is as follows in Port {0..17} Capture 0 CSR[29:31]: 0b000 = 4x to 2x or 0b001 = 4x to 1x lane 0 0b010 = 4x to 1x lane 2 0b011 = 2x to 1x lane 0 0b100 = 2x to 1x lane 1 0b101 = 2x to 1x lane 0 if lane 0 and lane 1 are ready and aligned
Data Character	One data character is captured for the event. This information is in the following registers: Port {0..17} Attributes Capture CSR Port {0..17} Capture 0 CSR[24:31] contains the data character.

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary

Event	Detection Enable	Information Capture Enable	Information Captured
Control symbol CRC error	Always Detected	Port {0..17} Error Rate Enable CSR.CS_CRC_ERR_EN = 1	Control Symbol Port {0..17} Error Detect CSR.CS_CRC_ERR
Received an acknowledgement control symbol with unexpected ackID	Always Detected	Port {0..17} Error Rate Enable CSR. UNEXP_ACKID_EN = 1	Control Symbol Port {0..17} Error Detect CSR.UNEXP_ACKID
Received a packet not accepted control symbol	Always Detected	Port {0..17} Error Rate Enable CSR.CS_NOT_ACC_EN = 1	Control Symbol Port {0..17} Error Detect CSR.CS_NOT_ACC
Received a packet with a bad ackID	Always Detected	Port {0..17} Error Rate Enable CSR.PKT_ILL_ACKID_EN = 1	Packet Port {0..17} Error Detect CSR.PKT_ILL_ACKID
Received a packet with bad CRC	Always Detected	Port {0..17} Error Rate Enable CSR.PKT_CRC_ERR_EN = 1	Packet Port {0..17} Error Detect CSR.PKT_CRC_ERR
Received a packet that exceeds 276 bytes	Always Detected	Port {0..17} Error Rate Enable CSR.PKT_ILL_SIZE_EN = 1	Packet Port {0..17} Error Detect CSR.PKT_ILL_SIZE
Received a data character in IDLE1	Always Detected	Port {0..17} Error Rate Enable CSR.IDLE1_ERR_EN = 1	Data Character Port {0..17} Error Detect CSR.IDLE1_ERR
Non-outstanding ackID in Link-Response	Always Detected	Port {0..17} Error Rate Enable CSR.LR_ACKID_ILL_EN = 1	Control Symbol Port {0..17} Error Detect CSR.LR_ACKID_ILL
Protocol error	Always Detected	Port {0..17} Error Rate Enable CSR.PRTCL_ERR_EN = 1	Control Symbol Port {0..17} Error Detect CSR.PRTCL_ERR
Delineation error	Always Detected	Port {0..17} Error Rate Enable CSR.DELIN_ERR_EN = 1	Destriped Data Port {0..17} Error Detect CSR.DELIN_ERR
Unsolicited acknowledgement control symbol	Always Detected	Port {0..17} Error Rate Enable CSR.CS_ACK_ILL_EN = 1	Control Symbol Port {0..17} Error Detect CSR.CS_ACK_ILL
Link timeout	Port Link Timeout Control CSR.TIME_OUT_VAL <> 0	Port {0..17} Error Rate Enable CSR.LINK_TIMEOUT_EN = 1	AckID Port {0..17} Error Detect CSR.LINK_TIMEOUT

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Received a packet when an error rate threshold event has occurred and drop packet mode is enabled	Port {0..17} Control 1 CSR.DROP_PKT_EN = 1 and Port {0..17} Error Rate Enable CSR <> 0 and Port {0..17} Error Rate Threshold CSR.FAIL_THRESH <> 0	Port {0..17} Error Rate Enable CSR. IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.ERR_RATE_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.ERR_RATE Port {0..17} Error and Status CSR.OUTPUT_DROP
A packet was dropped due to a TTL event	Packet Time to Live CSR.TTL is not 0	Port {0..17} Error Rate Enable CSR. IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register. TTL_EVENT_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.TTL_EVENT and Port {0..17} Error and Status CSR.OUTPUT_DROP
A transmitted packet was dropped via CRC error retransmit limit	Port {0..17} Operations Register.CRC_RETX_LIMIT <> 0	Port {0..17} Error Rate Enable CSR. IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.CRC_EVENT_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.CRC_EVENT and Port {0..17} Error and Status CSR.OUTPUT_DROP
Received a packet with a CRC error with CRC error suppression enabled	Port {0..17} Control 1 CSR.ERR_CHK_DIS = 0	Port {0..17} Error Rate Enable CSR. IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.CRC_EVENT_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.CRC_EVENT
Received a NAK other than lack of resources	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.PNA_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.PNA Port {0..17} Error Detect CSR.CS_NOT_ACC
Received an unsolicited link response	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.UNSOL_LR_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.UNSOL_LR Port {0..17} Error Detect CSR.PRTCL_ERR

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Received an unexpected ackID	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.UNEXP_ACKID_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.UNEXP_ACKID Port {0..17} Error Detect CSR.UNEXP_ACKID
Received a packet when no buffer available	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.PNA_RETRY_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.PNA_RETRY Port {0..17} Error Detect CSR.PKT_CRC_ERR
Received a packet that references no route and is dropped	Routing Table Value is 0xDF (no route) or 0xDD (use local) in Device Routing Table	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RTE_ISSUE_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE
Received a packet that references a disabled port and is dropped	Port {0..17} Control 1 CSR.PORT_DIS = 1	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RTE_ISSUE_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE
Received a packet that references a port configuration in port lockout and is dropped	Port {0..17} Control 1 CSR.PORT_LOCKOUT = 1	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RTE_ISSUE_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE
Received a packet that references a port in the fatal error state and is dropped	Device Control 1 Register.FATAL_ERR_PKT_MGT = 0 and Port {0..17} Error and Status CSR.PORT_ERR = 1	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RTE_ISSUE_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Set outstanding ackID invalid	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.SET_ACKID_EN = 1	Register Port {0..17} Implementation Specific Error Detect Register.SET_ACKID
Discarded a non-maintenance packet to be transmitted	Port {0..17} Control 1 CSR.OUTPUT_PORT_EN = 0 and Port {0..17} Control 1 CSR.PORT_LOCKOUT = 0	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.TX_DROP_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.TX_DROP
RX retry count triggered congestion	Port {0..17} Congestion Retry Counter Register.RETRY_LIM <> 0 and Port {0..17} Status and Control Register. RETRY_LIM_EN = 1	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.MANY_RETRY_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.MANY_RETRY
Discarded a received non-maintenance packet Note: The packet is not accepted by the receiver, but the transmitter retains the packet. The packet remains in the system.	Port {0..17} Control 1 CSR.INPUT_PORT_EN = 0 and Port {0..17} Control 1 CSR.PORT_LOCKOUT = 0	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RX_DROP_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.RX_DROP
Received a packet that has an invalid TT	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.BAD_TT_EN = 1	Packet Port {0..17} Implementation Specific Error Detect Register.BAD_TT
Received a packet that is too short	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.SHORT_EN = 1	Packet - only first 4 bytes of packet Port {0..17} Implementation Specific Error Detect Register.SHORT

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Unsolicited restart from retry	Always Detected Significant error if Transmitter-controlled Flow Control is active (Port {0..17} Status and Control Register.RX_FC = 0)	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.UNSOL_RFR_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.UNSOL_RFR Port {0..17} Error Detect CSR.PRTCL_ERR
Fatal link response timeout	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.FATAL_TO_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.FATAL_TO
Received a retry control symbol with a valid ackID	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RETRY_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.RETRY
Received a retry control symbol with unexpected ackID	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RETRY_ACKID_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.RETRY_ACKID Port {0..17} Error Detect CSR.OUTPUT_RETRY
Stomp timeout	Port Link Timeout Control CSR.TIMEOUT <> 0	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.STOMP_TO_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.STOMP_TO
Stomp received	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.RX_STOMP_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.RX_STOMP

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Link request with reserved command encoding	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.LR_CMD_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.LR_CMD
Double link request	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.LR_X2_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.LR_X2 Port {0..17} Error Detect CSR.PRTCL_ERR
Received EOP outside of a packet	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.UNEXP_EOP_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.UNEXP_EOP Port {0..17} Error Detect CSR.PRTCL_ERR
Received stomp outside of a packet	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.UNEXP_STOMP_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.UNEXP_STOMP Port {0..17} Error Detect CSR.PRTCL_ERR
Port initialization TX required	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.PORT_INIT_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.PORT_INIT Port {0..17} Error and Status CSR.PORT_OK = 1, PORT_UNINIT = 0
Port width downgrade	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.PORT_WIDTH_EN = 1	Downgrade Port {0..17} Implementation Specific Error Detect Register.PORT_WIDTH

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Table 37: Physical Layer "Leaky Bucket" Events and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
IDLE character in packet	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.IDLE_IN_PKT_EN = 1	Port {0..17} Capture 0 CSR[0:31] contains the 4 bytes of the packet in which IDLE characters were found. Port {0..17} Implementation Specific Error Detect Register.IDLE_IN_PKT
Loss of alignment	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.LOA_EN = 1	No Info Port {0..17} Implementation Specific Error Detect Register.LOA
Bad control character sequence	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.BAD_CTL_EN = 1	Control Symbol Port {0..17} Implementation Specific Error Detect Register.BAD_CTL
Lanes reordered	Always Detected	Port {0..17} Error Rate Enable CSR.IMP_SPEC_ERR_EN = 1 and Port {0..17} Implementation Specific Error Rate Enable Register.REORDER_EN = 1	Port {0..17} Capture 0 CSR encodes lane information: [28:31] – Lane detected for Lane 0 of port [24:27] – Lane detected for Lane 1 of port [20:23] – Lane detected for Lane 2 of port [16:19] – Lane detected for Lane 3 of port Port {0..17} Implementation Specific Error Detect Register.REORDER Lane {0..47} Status 0 CSR.LANE

6.2.2.1 Time to Live Events

Each S-RIO port supports the Time to Live (TTL) function identified in the *RapidIO Specification (Rev. 2.1), Part 8*. Time-to-live tracking begins once a packet has been completely received by the Final Buffer. If a packet remains in the Final Buffer longer than the time specified by Packet Time to Live CSR.TTL, the following actions are taken:

- The packet is discarded
- Port {0..17} Error and Status CSR.OUTPUT_DROP is set

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- The port's dropped packet counter is incremented
- If notification is enabled, the system is notified by a port-write and/or interrupt

If a packet is transmitted from the Final Buffer to the link partner when a TTL timeout occurs for the packet, the port continues transmitting the packet to its normal completion. If NACKed by the link partner, the packet is not retransmitted and is considered a dropped packet with action taken as defined above.

If a packet transmission is completed from the Final Buffer to the link partner and then a TTL timeout occurs for the packet, the port will wait for the ACK/NACK control symbol before processing the timeout event. If the packet is accepted by the link partner, it is removed from the Final Buffer and normal transmission continues without notification of a dropped packet condition. If the packet is NACKed by the link partner, the packet is not retransmitted and is considered a dropped packet with subsequent action as defined above.



When a CPS-1848 port's link partner re-initializes or is extracted from the system, packets may be discarded due to TTL. Depending on the timing of the extraction, it may not be possible for the switch port to resume transmission without software intervention.

For more information on hot insertion and extraction, see Hot Extraction/Insertion.

6.2.3 Lane Events

Lane events are related to individual lane behaviors. Within the RapidIO protocol, lane behaviors are limited to 8b/10b encoding, idle sequences operation, and lane initialization. Information about all lane events is in Table 39. This table has four columns:

- Event Name – The short form by which the event is consistently identified.
- Detection Enable – Any register settings required to enable detection of the event. "Always Detected" means that there are no controls to disable detection of the event.
- Information Capture Enable – The register settings required to enable the event to supply the leaky bucket. These register settings also enable capture of information associated with the event.
- Information Captured – Summary of information captured for the event, as well as the status bit that indicates the event was detected. Multiple status bits may be set, however information is captured only for the first enabled event. Subsequent events do not have any information captured. The values in the "Information Captured" column are described in Table 38

Table 38: Lane Event Information Captured Value Descriptions

Value	Description
No Info	No information is captured for this event.
CS Field	The decoded content of the IDLE2 Control and Status field is captured in the following registers: • Lane {0..47} Attributes Capture Register: INFO_TYPE is set to 0b100 • Lane {0..47} Data Capture 0 Register The Lane {0..47} Data Capture 0 Register contains the data in the CS Field of the received IDLE2 sequence.
Data	The last four 8-bit characters received on the link are captured in the following registers: • Lane {0..47} Attributes Capture Register: INFO_TYPE is set to 0b100 • Lane {0..47} Data Capture 0 Register

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Table 38: Lane Event Information Captured Value Descriptions *(Continued)*

Value	Description
RX TX Type	Capture information about transmitter and receiver types. • Lane {0..47} Data Capture 0 Register [31:30] = Local Receiver Type — 0b00 = Short — 0b01 = Long — 0b10 = Medium • Lane {0..47} Data Capture 0 Register [29] = Remote Receiver Type — 0 = Short — 1 = Long
Character	Capture information about 10b code group, 8b character and control/data determination. • Lane {0..47} Data Capture 0 Register [22:31] = 10-bit data • Lane {0..47} Data Capture 0 Register [12:19] = 8-bit data • Lane {0..47} Data Capture 0 Register [11] = Control or Data (0 = K, 1 = D)
Training State	Indicates the current training state for this port's receiver and the link partner's receiver, consistent with the last IDLE2 frame received from the link partner. • Lane {0..47} Data Capture 0 Register [31] = Local receiver trained state • Lane {0..47} Data Capture 0 Register [30] = Remote receiver trained state

Table 39: Lane Event Enable and Information Capture Summary

Event	Detection Enable	Information Capture Enable	Information Captured
Lane inversion detected	Always Detected	Lane {0..47} Error Rate Enable Register.LANE_INVER_DET_EN	No Info Lane {0..47} Error Detect Register.LANE_INVER_DET
IDLE2 framing error	Always Detected on links which use IDLE2	Lane {0..47} Error Rate Enable Register.IDLE2_FRAME_EN	Data Lane {0..47} Error Detect Register.IDLE2_FRAME
Receiver/transmitter type mismatch	Always Detected on links which use IDLE2	Lane {0..47} Error Rate Enable Register.TX_RX_MISMATCH_EN	RX TX Type Lane {0..47} Error Detect Register.TX_RX_MISMATCH
Loss of descrambler sync	Port {0..17} Control 2 CSR.SCRAM_DIS = 0	Lane {0..47} Error Rate Enable Register.DESCRAM_SYNC_EN	No Info Lane {0..47} Error Detect Register.DESCRAM_SYNC
Received an illegal or invalid character	Always Detected	Lane {0..47} Error Rate Enable Register.BAD_CHAR_EN	Character Lane {0..47} Error Detect Register.BAD_CHAR

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Table 39: Lane Event Enable and Information Capture Summary *(Continued)*

Event	Detection Enable	Information Capture Enable	Information Captured
Loss of lane ready	Always Detected on links using IDLE2	Lane {0..47} Error Rate Enable Register.LANE_RDY_EN	Training State Lane {0..47} Error Detect Register.LANE_RDY
Loss of lane sync	Always Detected	Lane {0..47} Error Rate Enable Register.LANE_SYNC_EN	No Info Lane {0..47} Error Detect Register.LANE_SYNC

6.2.4 I²C Events

The I2C Interface can detect a number of events, none of which affects the operation of the switch. No additional information is captured for I2C events other than the fact that the event occurred.

Table 40: I2C Event Enable and Information Capture Summary

Event	Detection Enable	Information Capture Enable	Information Captured
I2C checksum error	I2C Master Control Register.CHKSUM_DIS = 0	Aux Port Error Capture Enable Register.I2C_CHKSUM_ERR_EN	Aux Port Error Detect Register.I2C_CHKSUM_ERR
I2C unexpected start/stop	Always Detected	Aux Port Error Capture Enable Register.UNEXP_START_STOP_EN	Aux Port Error Detect Register.UNEXP_START_STOP
I2C 22-bit memory address incomplete	Always Detected	Aux Port Error Capture Enable Register.I2C_ADDR_ERR_EN	Aux Port Error Detect Register.I2C_ADDR_ERR
I2C acknowledgement error	Always Detected	Aux Port Error Capture Enable Register.I2C_ACK_ERR_EN	Aux Port Error Detect Register.I2C_ACK_ERR
I2C length error	Always Detected	Aux Port Error Capture Enable Register.I2C_LENGTH_ERR_EN	Aux Port Error Detect Register.I2C_LENGTH_ERR

6.2.5 JTAG Events (Revision A/B Only)

The JTAG Interface can detect a single event that affects the operation of the switch; however, no JTAG events are detected by Revision C parts. No additional information is captured for the JTAG events other than the fact that the event occurred.

Table 41: JTAG Event Enable and Information Capture Summary (Revision A/B Only)

Event	Detection Enable	Information Capture Enable	Information Captured
JTAG incomplete write	Always Detected	Aux Port Error Capture Enable Register.JTAG_ERR_EN	Aux Port Error Detect Register.JTAG_ERR

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6.2.6 Configuration Block Events

Register accesses to the CPS-1848 can cause the detection of a number of events which indicate illegal register programming has occurred. No additional information is captured for configuration block events, other than the fact that the event occurred.

Table 42: Configuration Block Event Enable and Information Capture Summary

Event	Detection Enable	Information Capture Enable	Information Captured
Multicast translation error	Always Detected	Configuration Block Error Capture Enable Register.BAD_MCAST_EN	Configuration Block Error Detect Register.BAD_MCAST
Route table configuration error	Always Detected	Configuration Block Error Capture Enable Register.BAD_RTE_EN	Configuration Block Error Detect Register.BAD_RTE
Force local configuration error	Always Detected	Configuration Block Error Capture Enable Register.RTE_FORCE_EN	Configuration Block Error Detect Register.RTE_FORCE
Port configuration error	Always Detected	Configuration Block Error Capture Enable Register.BAD_PORT_EN	Configuration Block Error Detect Register.BAD_PORT
Multicast mask configuration error	Always Detected	Configuration Block Error Capture Enable Register.BAD_MASK_EN	Configuration Block Error Detect Register.BAD_MASK

6.2.7 Trace and Filter Events

When the Packet Trace and Filtering functions match a packet, an event is sent to the Error Log. No status bits, other than an entry in the Error Log, are associated with these events. There are two events: TRACE_MATCH_OCCURRED and FILTER_MATCH_OCCURRED.

6.2.8 Packet Generation and Capture Mode Events

When at least one packet is received by the End Buffer while the device is in Packet Generation and Capture (PGC) mode, an event is sent to the Error Log. No status bits other than an entry in the Error Log are associated with this event. This event is called PGC_CMPL.

6.2.9 Error Log Events

All events can be reported to the Error Log. The Error Log functionality is summarized in Figure 25 (Note: The Error Report for JTAG is applicable to Revision A/B only).

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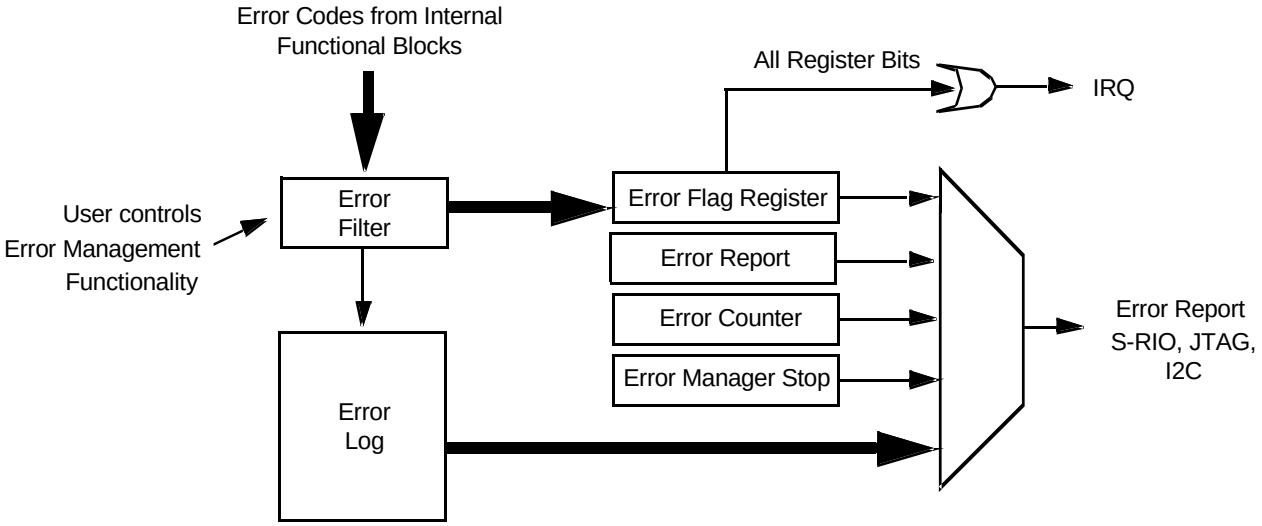
Figure 25: Error Management Block Architecture



The Error Log is a 256 entry buffer which captures detected events that have reporting enabled, as described in Event Notification. Each error log buffer entry consists of an event source, an event group, and an error type. The encoding of event source and error type is captured in the following sections.

The device provides eight Error Log Match Register {0..7} that can be configured to detect when specific events are reported to the Error Log. While these registers have many functions related to notification, they also determine if an event feeds the Error Log Events Register. If the counter reaches its maximum value, 0xFFFF, this constitutes a reportable event.

If the event selected by a Error Log Match Register {0..7} is detected, then the bit in the Error Log Match Status Register associated with that Error Log Match Register {0..7} is set. Setting bits in the Error Log Match Status Register does not constitute an event, but does inform the user which Error Log Match Register {0..7} has detected an event.

6.2.9.1 Error Log Event Source Encoding

Each functional block that supports the error reporting function is defined as an “Event Source”. The CPS-1848 allows the user to enable and disable the error reporting functionality of each of these sources. Regardless of whether or not reporting is enabled, all errors that are received by the Error Management Block are stored in the Error Log. The list of non-S-RIO error sources and their respective codes is provided in Table 43.

Table 43: Event Source Encoding

Event Source	Source Codes
Lane 0	0x40
Lane 1	0x41
Lane 2	0x42
Lane 3	0x43
Lane 4	0x44
Lane 5	0x45
Lane 6	0x46
Lane 7	0x47

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Table 43: Event Source Encoding *(Continued)*

Event Source	Source Codes
Lane 8	0x48
Lane 9	0x49
Lane 10	0x4A
Lane 11	0x4B
Lane 12	0x4C
Lane 13	0x4D
Lane 14	0x4E
Lane 15	0x4F
Lane 16	0x50
Lane 17	0x51
Lane 18	0x52
Lane 19	0x53
Lane 20	0x54
Lane 21	0x55
Lane 22	0x56
Lane 23	0x57
Lane 24	0x58
Lane 25	0x59
Lane 26	0x5A
Lane 27	0x5B
Lane 28	0x5C
Lane 29	0x5D
Lane 30	0x5E
Lane 31	0x5F
Lane 32	0x60
Lane 33	0x61
Lane 34	0x62
Lane 35	0x63
Lane 36	0x64
Lane 37	0x65
Lane 38	0x66
Lane 39	0x67

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Table 43: Event Source Encoding *(Continued)*

Event Source	Source Codes
Lane 40	0x68
Lane 41	0x69
Lane 42	0x6A
Lane 43	0x6B
Lane 44	0x6C
Lane 45	0x6D
Lane 46	0x6E
Lane 47	0x6F
Port 0	0x2A
Port 1	0x29
Port 2	0x34
Port 3	0x33
Port 4	0x32
Port 5	0x31
Port 6	0x3C
Port 7	0x3B
Port 8	0x3A
Port 9	0x39
Port 10	0x3D
Port 11	0x3E
Port 12	0x1C
Port 13	0x1D
Port 14	0x27
Port 15	0x26
Port 16	0x25
Port 17	0x24
LT Layer	0x1E
Configuration	0x00
JTAG[1]	0x00
I^2C	0x00

1. JTAG event source is applicable to Revision A/B only.

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When an error is detected by one of the above sources, both the Error Source and Error Code number are logged into the Error Log FIFO. The Error Source is a 7-bit field that indicates the location of the error. The Error Code is an 8-bit field that designates the type of error that occurred. The Error Management Block provides a single Error Log and arbitrates between error sources for access to the Error Log. The Error Management Block records all of the errors up to the speed of arbitration between all the sources (for more information, see Performance).

The CPS-1848 provides an Error Log Data Register for reading out the first error from the Error Log. This register lists the location and type of error (Error Source, Error Code: 15 bits) occurred. When the register is read, the device returns the first entry in the Error Log.

The device allows the user to reset the contents of the Error Log FIFO, Error Log Counter, and Error Flags using the Error Log Control 2 Register.

6.2.9.2 Error Log Logical Transport Event Encoding

Table 44 defines the Error Codes to be captured in the Error Log associated with the Logical Layer Transport Errors defined in the *RapidIO Specification (Rev. 2.1), Part 8*.

Table 44: Error Codes for Implementation Specific LT Errors

Error	Error Code	Corresponding Detect Bit in Logical/Transport Layer Error Detect CSR	Corresponding Detect Bit in Logical/Transport Layer Control Capture CSR
Maintenance read size invalid	0x31	IMP_SPEC_ERR	MTC_BAD_READ_SIZE
Maintenance write size invalid	0x32	IMP_SPEC_ERR	MTC_BAD_WR_SIZE
Maintenance transaction field error	0x33	IMP_SPEC_ERR	MTC_TTYPE_ERR
Maintenance read received with data	0x34	IMP_SPEC_ERR	MTC_READ_WITH_DATA
Maintenance write received without data	0x35	IMP_SPEC_ERR	MTC_WR_WITHOUT_DATA
Maintenance packet received that was too small or too large	0x36	IMP_SPEC_ERR	MTC_PKT_SIZE_ERR

6.2.9.3 Error Log Port Event Log Encoding

Table 45 defines the Error Codes to be captured in the Error Log associated with the port-level errors defined in the *RapidIO Specification (Rev. 2.1), Part 8*.

Table 45: Error Log Standard Port Error Encoding

Error	Error Code	Corresponding Detect Bit in Port {0..17} Error Detect CSR	Corresponding Detect Bit in Port {0..17} Implementation Specific Error Detect Register
Delineation error	0x71	DELIN_ERR	N/A
Protocol error	0x78	PRTCL_ERR	LR_X2
Protocol error	0x79	PRTCL_ERR	LR_CMD

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Table 45: Error Log Standard Port Error Encoding *(Continued)*

Error	Error Code	Corresponding Detect Bit in Port {0..17} Error Detect CSR	Corresponding Detect Bit in Port {0..17} Implementation Specific Error Detect Register
Illegal control symbol acknowledgement	0x7E	CS_ACK_ILL	N/A
Control symbol CRC error	0x80	CS_CRC_ERR	N/A
Packet CRC error	0x81	PKT_CRC_ERR	N/A
Illegal packet ackID	0x82	PKT_ILL_ACKID	N/A
Protocol error	0x83	PRTCL_ERR	UNEXP_STOMP
Protocol error	0x84	PRTCL_ERR	UNEXP_EOP
Acknowledgement control symbol with unexpected ackID	0x87	UNEXP_ACKID	UNEXP_ACKID
Acknowledgement control symbol with unexpected ackID	0x88	UNEXP_ACKID	RETRY_ACKID
Control symbol not acknowledged	0x8A	CS_NOT_ACC	N/A
Link response illegal ackID	0x8B	LR_ACKID_ILL	N/A
Link timeout	0x8D	LINK_TIMEOUT	N/A
Protocol error	0x8E	PRTCL_ERR	UNSOL_RFR
Protocol error	0x8F	PRTCL_ERR	UNSOL_LR
Illegal packet size	0x90	PKT_ILL_SIZE	N/A
IDLE1 error	0xA0	IDLE1_ERR	N/A

Table 46 defines the Error Codes to be captured in the Error Log associated with the port-level Errors defined in the *RapidIO Specification (Rev. 2.1), Part 8*. This table defines the codes for error that are logged a as result of detecting a port-level error that is defined in Part 8 of the specification, but covered in the Implementation Specific definition portion of the port error detect.

Table 46: Error Log Implementation Specific Port Error Encoding

Error	Error Code	Corresponding Detect Bit in Port {0..17} Error Detect CSR	Corresponding Detect Bit in Port {0..17} Implementation Specific Error Detect Register
Set outstanding ackID	0x72	IMP_SPEC	SET_ACKID
Discarded a non-maintenance packet to be transmitted	0x73	IMP_SPEC	TX_DROP
IDLE character in packet	0x74	IMP_SPEC	IDLE_IN_PKT

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Table 46: Error Log Implementation Specific Port Error Encoding *(Continued)*

Error	Error Code	Corresponding Detect Bit in Port {0..17} Error Detect CSR	Corresponding Detect Bit in Port {0..17} Implementation Specific Error Detect Register
Port width downgrade	0x75	IMP_SPEC	PORT_WIDTH
Lanes reordered	0x76	IMP_SPEC	REORDER
Loss of alignment	0x77	IMP_SPEC	LOA
Double link request	0x78	IMP_SPEC	LR_X2
Link request with reserved command field encoding	0x79	IMP_SPEC	LR_CMD
Stomp timeout	0x7A	IMP_SPEC	STOMP_TO
Stomp received	0x7B	IMP_SPEC	RX_STOMP
Received a packet that was too short	0x7D	IMP_SPEC	SHORT
Bad control character sequence	0x7F	IMP_SPEC	BAD_CTL
Received stomp outside of a packet	0x83	IMP_SPEC	UNEXP_STOMP
Received EOP outside of a packet	0x84	IMP_SPEC	UNEXP_EOP
Port initialization TX acquired	0x85	IMP_SPEC	PORT_INIT
Discarded a received non-maintenance packet	0x86	IMP_SPEC	RX_DROP
Received an accepted control symbol with unexpected ackID	0x87	IMP_SPEC	UNEXP_ACKID
Received a retry control symbol with unexpected ackID	0x88	IMP_SPEC	RETRY_ACKID
Received a retry control symbol with an invalid ackID	0x89	IMP_SPEC	RETRY
Fatal link response timeout	0x8C	IMP_SPEC	FATAL_TO
Unsolicited restart from retry	0x8E	IMP_SPEC	UNSOL_RFR
Received unsolicited link response	0x8F	IMP_SPEC	UNSOL_LR
Received a packet with an invalid TT	0x91	IMP_SPEC	BAD_TT
Received NACK other than lack of resources	0x92	IMP_SPEC	PNA

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Table 46: Error Log Implementation Specific Port Error Encoding *(Continued)*

Error	Error Code	Corresponding Detect Bit in Port {0..17} Error Detect CSR	Corresponding Detect Bit in Port {0..17} Implementation Specific Error Detect Register
Received a packet when no buffer available	0x97	IMP_SPEC	PNA_RETRY
Transmitted packet dropped via CRC retransmit error	0x99	IMP_SPEC	CRC_EVENT
Received a packet that references no route and is dropped	0xA1	IMP_SPEC	RTE_ISSUE
Received a packet that references a disabled port and is dropped	0xA2	IMP_SPEC	RTE_ISSUE
Received a packet that references a port in the fatal error state and is dropped	0xA3	IMP_SPEC	RTE_ISSUE
Packet was dropped due to TTL event	0xA4	IMP_SPEC	TTL_EVENT
Received a packet with a CRC error with CRC error suppression enabled	0xA6	IMP_SPEC	CRC_EVENT
Received a packet when an output failed threshold event has occurred and drop packet mode is enabled	0xA7	IMP_SPEC	ERR_RATE
Received a packet that references a port configured in port lockout and is dropped	0xA9	IMP_SPEC	RTE_ISSUE
RX retry count triggered congestion event	0xAA	IMP_SPEC	MANY_RETRY

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6.2.9.3.1 *Error Log Lane Event Encoding*

Table 47 defines the error codes to be captured in the Error Log associated with the lane-level errors defined in the *RapidIO Specification (Rev. 2.1)*. Since these errors are not covered in the *RapidIO Specification (Rev. 2.1), Part 8*, they are considered implementation-specific and are defined in IDT implementation space.

Table 47: Error Log Lane Level Encoding

Error	Error Code	Corresponding Detect Bit in Lane {0..47} Error Detect Register
Loss of lane sync	0x60	LANE_SYNC
Loss of lane ready	0x61	LANE_RDY
Received an illegal or invalid character	0x62	BAD_CHAR
Loss of descrambler sync	0x63	DESCRAM_SYNC
Receiver/transmitter mismatch	0x64	TX_RX_MISMATCH
IDLE2 framing error	0x67	IDLE2_FRAME
Lane inversion detected	0x68	LANE_INVER_DET

6.2.9.3.2 *I^2C Error Codes*

The I^2C errors displayed in the following table can be detected by the CPS-1848. If I^2C error reporting is enabled each error can be sent to the Error Log when detected.

Table 48: I^2C Errors and Codes

Error	Error Code	Corresponding Detect Bit in Aux Port Error Detect Register
I2C length error	0x10	I2C_LENGTH_ERR
I2C acknowledgement error	0x11	I2C_ACK_ERR
I2C 22-bit memory address incomplete error	0x12	I2C_ADDR_ERR
I2C unexpected start/stop	0x13	UNEXP_START_STOP
I2C checksum error	0x14	I2C_CHKSUM_ERR

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6.2.9.3.3 *JTAG Error Encoding (Revision A/B Only)*

The JTAG error displayed in the following table is detectable by the CPS-1848. If JTAG error reporting is enabled the error can be sent to the Error Log when detected.

Table 49: JTAG Errors and Codes (Revision A/B Only)

Error	Error Code	Corresponding Detect Bit in Aux Port Error Detect Register
JTAG incomplete write	0x20	JTAG_ERR

6.2.9.3.4 *Configuration Event Encoding*

The CPS-1848 can detect the configuration errors listed in Table 50. If configuration error reporting is enabled each error can be sent to the Error Log when detected.

Table 50: Configuration Errors and Codes

Error	Error Code	Corresponding Detect Bit in Configuration Block Error Detect Register
Multicast mask configuration error	0x50	BAD_MASK
Port configuration error	0x53	BAD_PORT
Force local configuration error	0x54	RTE_FORCE
Route table configuration error	0x55	BAD_RTE
Multicast translation error	0x56	BAD_MCAST

6.2.9.3.5 *Trace, Filter, and PGC Mode Event Error Log Encoding*

The Trace, Filter and PGC mode events have their own special encoding that is not associated with any other status bits. These events are listed in the following table.

Table 51: Trace, Filter, and PGC Mode Error Log Encoding

Error	Error Code
Trace match occurred	0x9E
Filter match occurred	0x9F
Packet Generation and Capture Complete	0xA8

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6.3 Event Notification

The CPS-1848 supports two forms of event notification: RapidIO port-write packets, and interrupts. Port-writes are further described in Port-Write Formats, Programming Model, and Generation, and interrupts are discussed in Interrupt Notification.

When Logical/Transport layer events, I2C events, JTAG events (Revision A/B only), or configuration events are detected, the notification function is triggered immediately.

A low rate of RapidIO physical layer events is expected on any RapidIO link, as stated in Event Detection. Event notification can be triggered immediately when any RapidIO physical layer error is detected. Another method is to notify software only when the rate of physical layer errors exceeds a system specific threshold. This is done using the RapidIO standard “leaky bucket” function as described in Physical Layer Events.

All physical layer events are linked to the “leaky bucket” function, which consists of a counter and two threshold values. The counter is incremented when physical layer errors occur, and is decremented at a configurable rate. The first threshold is a link degraded threshold, which indicates that the rate of physical layer errors is starting to impact the performance of the link. The second is a link failed threshold, which indicates that the link should be considered inoperable due to the error rate. Both link degraded and link failed thresholds create RapidIO standard events that can result in port-writes being sent and/or interrupt assertion.

Additionally, all events can be sent to the IDT-specific Error Log function. The Error Log function consists of the following:

- A 256 entry buffer that captures all events in the order in which they occurred globally in the switch
- 8 mask/value registers that can trigger port-write transmission and/or interrupt assertion when specific events are reported
- A counter that increments with every event received. When the counter reaches a programmable threshold a port-write and/or interrupt are triggered.

For more information about the Error Log functionality, see Error Log Events.

6.3.1 Logical Layer Events Notification

According to the RapidIO specification, logical/transport layer events may trigger port-writes and/or interrupt notification when information capture is enabled. The CPS-1848 allows logical/transport layer events to trigger port-writes and/or interrupt notification even when information capture is not enabled, through the use of the Logical/Transport Layer Error Report Enable Register.

An event that has notification enabled in the Logical/Transport Layer Error Report Enable Register can trigger a Standard port-write if Device Control 1 Register.LT_PW_EN is set (see Table 52).

An event that has notification enabled in the Logical/Transport Layer Error Report Enable Register can trigger an interrupt if Device Control 1 Register.LT_INT_EN is set (see Table 52).

Enabled logical/transport layer errors are always sent to the Error Log.

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To generate an IDT port-write for logical/transport layer events, see Error Log Events.

Table 52: Logical/Transport Layer Event Notification Control

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Illegal transaction decode	Logical/Transport Layer Error Report Enable Register.ILL_TRAN_EN = 1 and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.ILL_TRAN_EN = 1 and Device Control 1 Register.LT_INT_EN = 1	Logical/Transport Layer Error Report Enable Register.ILL_TRAN_EN = 1
Unsolicited response	Logical/Transport Layer Error Report Enable Register.UNSOL_RESP_EN = 1 and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.UNSOL_RESP_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.UNSOL_RESP_EN = 1
Unsupported transaction	Logical/Transport Layer Error Report Enable Register.UNSUP_TRAN_EN = 1 and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.UNSUP_TRAN_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.UNSUP_TRAN_EN = 1
Maintenance read size invalid	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1
Maintenance write size invalid	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1
Maintenance read received with data	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1
Maintenance write received without data	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1

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Table 52: Logical/Transport Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Maintenance transaction field error	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1
Maintenance packet received was too short or too long	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1[1] and Device Control 1 Register.LT_PW_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1 and Device Control 1 Register.LT_INIT_EN = 1	Logical/Transport Layer Error Report Enable Register.IMP_SPEC_ERR_EN = 1

1. For more information on the location of this enable bit, see the table below Logical/Transport Layer Control Capture CSR.

6.3.2 Physical Layer Events Notification

According the RapidIO specification, physical layer events trigger notification only if the leaky bucket degraded or failure threshold values are exceeded. Notification can occur in the form of a port-write or an interrupt.

A single packet or control symbol can cause multiple physical layer events to be detected. The leaky bucket counter is incremented by 1 for each erroneous control symbol and packet, regardless of the number of physical layer events detected in individual control symbols or packets.

The CPS-1848 exceeds the RapidIO specification required notifications to allow individual physical layer events to trigger interrupt or Standard port-write notification. Additionally, the Error Log allows IDT port-write notification for selected events, as described in Error Log Event Notification Programming Model.

To enable Standard port-write notification for any physical layer event, the Port {0..17} Operations Register. PORT_PW_EN bit must be set (see Table 53).

To enable interrupt notification for any physical layer event, the Port {0..17} Operations Register.PORT_INT_EN bit must be set (see Table 53).

To enable Error Log reporting of port events, the Port {0..17} Operations Register.PORT_LOG_EN bit must be set (see Table 53). For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

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Table 53: Physical Layer Event Notification Control

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Control symbol CRC error	Port {0..17} Error Report Enable Register.CS_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.CS_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.CS_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received an acknowledgement control symbol with unexpected ackID	Port {0..17} Error Report Enable Register. UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register. UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register. UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet not accepted control symbol	Port {0..17} Error Report Enable Register.CS_NOT_ACC_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.CS_NOT_ACC_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.CS_NOT_ACC_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet with a bad ackID	Port {0..17} Error Report Enable Register.PKT_ILL_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.PKT_ILL_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.PKT_ILL_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet with bad CRC	Port {0..17} Error Report Enable Register.PKT_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.PKT_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.PKT_CRC_ERR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet that exceeds 276 bytes	Port {0..17} Error Report Enable Register.PKT_ILL_SIZE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.PKT_ILL_SIZE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.PKT_ILL_SIZE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a data character in IDLE1	Port {0..17} Error Report Enable Register.IDLE1_ERR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.IDLE1_ERR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.IDLE1_ERR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Non-outstanding ackID in Link-Response	Port {0..17} Error Report Enable Register.LR_ACKID_ILL_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.LR_ACKID_ILL_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.LR_ACKID_ILL_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Protocol error	Port {0..17} Error Report Enable Register.PRTCL_ERR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.PRTCL_ERR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.PRTCL_ERR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Delineation error	Port {0..17} Error Report Enable Register.DELIN_ERR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.DELIN_ERR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.DELIN_ERR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Unsolicited acknowledgement control symbol	Port {0..17} Error Report Enable Register.CS_ACK_ILL_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.CS_ACK_ILL_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.CS_ACK_ILL_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Link timeout	Port {0..17} Error Report Enable Register.LINK_TIMEOUT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Error Report Enable Register.LINK_TIMEOUT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Error Report Enable Register.LINK_TIMEOUT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet when an error rate threshold event has occurred and drop packet mode is enabled	Port {0..17} Implementation Specific Error Report Enable Register.ERR_RATE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.ERR_RATE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.ERR_RATE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
A packet was dropped due to a TTL event	Port {0..17} Implementation Specific Error Report Enable Register. TTL_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register. TTL_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register. TTL_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
A transmitted packet was dropped via CRC error retransmit limit	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Received a packet with a CRC error with CRC error suppression enabled	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.CRC_EVENT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a NAK other than lack of resources	Port {0..17} Implementation Specific Error Report Enable Register.PNA_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register. PNA_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register. PNA_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received an unsolicited link response	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_LR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_LR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_LR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received an unexpected ackID	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet when no buffer available	Port {0..17} Implementation Specific Error Report Enable Register.PNA_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PNA_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PNA_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet that references no route and is dropped	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet that references a disabled port and is dropped	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Received a packet that references a port configuration in port lockout and is dropped	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet that references a port in the fatal error state and is dropped	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RTE_ISSUE_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Set outstanding ackID invalid	Port {0..17} Implementation Specific Error Report Enable Register.SET_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.SET_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.SET_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Discarded a non-maintenance packet to be transmitted	Port {0..17} Implementation Specific Error Report Enable Register.TX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.TX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.TX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
RX retry count triggered congestion	Port {0..17} Implementation Specific Error Report Enable Register.MANY_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.MANY_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.MANY_RETRY_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Discarded a received non-maintenance packet Note: The packet is not accepted by the receiver, but the transmitter retains the packet. The packet remains in the system.	Port {0..17} Implementation Specific Error Report Enable Register.RX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RX_DROP_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a packet that has an invalid TT	Port {0..17} Implementation Specific Error Report Enable Register.BAD_TT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.BAD_TT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.BAD_TT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Received a packet that is too short	Port {0..17} Implementation Specific Error Report Enable Register.SHORT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.SHORT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.SHORT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Unsolicited restart from retry	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_RFR_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_RFR_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNSOL_RFR_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Fatal link response timeout	Port {0..17} Implementation Specific Error Report Enable Register.FATAL_TO_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.FATAL_TO_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.FATAL_TO_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a retry control symbol with a valid ackID	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received a retry control symbol with unexpected ackID	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RETRY_ACKID_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Stomp timeout	Port {0..17} Implementation Specific Error Report Enable Register.STOMP_TO_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.STOMP_TO_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.STOMP_TO_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Stomp received	Port {0..17} Implementation Specific Error Report Enable Register.RX_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RX_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.RX_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Link request with reserved command encoding	Port {0..17} Implementation Specific Error Report Enable Register.LR_CMD_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LR_CMD_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LR_CMD_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Double link request	Port {0..17} Implementation Specific Error Report Enable Register.LR_X2_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LR_X2_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LR_X2_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received EOP outside of a packet	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_EOP_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_EOP_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_EOP_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Received stomp outside of a packet	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.UNEXP_STOMP_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Port initialization TX required	Port {0..17} Implementation Specific Error Report Enable Register.PORT_INIT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PORT_INIT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PORT_INIT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Port width downgrade	Port {0..17} Implementation Specific Error Report Enable Register.PORT_WIDTH_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PORT_WIDTH_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.PORT_WIDTH_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
IDLE character in packet	Port {0..17} Implementation Specific Error Report Enable Register.IDLE_IN_PKT_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.IDLE_IN_PKT_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.IDLE_IN_PKT_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

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Table 53: Physical Layer Event Notification Control *(Continued)*

Event	Standard Port-Write Reporting	Interrupt Reporting	Error Log Reporting
Loss of alignment	Port {0..17} Implementation Specific Error Report Enable Register.LOA_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LOA_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.LOA_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Bad control character sequence	Port {0..17} Implementation Specific Error Report Enable Register.BAD_CTL_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.BAD_CTL_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.BAD_CTL_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1
Lanes reordered	Port {0..17} Implementation Specific Error Report Enable Register.REORDER_EN = 1 and Port {0..17} Operations Register.PORT_PW_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.REORDER_EN = 1 and Port {0..17} Operations Register.PORT_INT_EN = 1	Port {0..17} Implementation Specific Error Report Enable Register.REORDER_EN = 1 and Port {0..17} Operations Register.PORT_LOG_EN = 1

6.3.3 Lane Event Notification

In order for lane errors to trigger any event notification function, the bit associated with the event(s) of interest must be enabled in the Lane {0..47} Error Report Enable Register.

Lane events can trigger interrupt or Standard port-write notification. To enable Standard port-write notification for Lane events, the Lane {0..47} Control Register.LANE_PW_EN bit must be set. Once this bit is set, lane events that are in the Lane {0..47} Error Report Enable Register will cause a port-write to be sent.

To enable interrupt notification for any lane event, the Lane {0..47} Control Register.LANE_INT_EN bit must be set. Once this bit is set, lane events that are enabled in Lane {0..47} Error Report Enable Register will cause the interrupt line to be asserted.

To enable Error Log reporting of all enabled lane events for a port, the Port {0..17} Operations Register.LANE_LOG_EN bit must be set. Once this bit is set for all lanes assigned to that port, all lane events that are enabled in the Lane {0..47} Error Report Enable Register will be reported to the Error Log. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

6.3.4 I^2C Event Notification

I^2C events can trigger interrupt or Standard port-write notification. To enable Standard port-write notification for I^2C events, the I2C Master Control Register. I2C_PW_EN bit must be set. Once this bit is set, I^2C events that are enabled as described in I2C Events will cause a port-write to be sent.

To enable interrupt notification for any I^2C event, the I2C Master Control Register.I2C_INT_EN bit must be set. Once this bit is set, I^2C events that are enabled as described in I2C Events will cause the interrupt line to be asserted.

To enable Error Log reporting of I^2C events, the Aux Port Error Report Enable Register.I2C_LOG_EN bit must be set. Once this bit is set, I^2C events that are enabled as described in I2C Events will be reported to the Error Log. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

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6.3.5 JTAG 1149.1 Event Notification (Revision A/B Only)

JTAG events can trigger interrupt or Standard port-write notification. To enable Standard port-write notification for JTAG events, the JTAG Control Register (Revision A/B).JTAG_PW_EN bit must be set. Once this bit is set, JTAG events that are enabled as described in JTAG Events (Revision A/B Only) will cause a port-write to be sent.

To enable interrupt notification for any JTAG event, the JTAG Control Register (Revision A/B).JTAG_INT_EN bit must be set. Once this bit is set, JTAG events that are enabled as described in JTAG Events (Revision A/B Only) will cause the interrupt line to be asserted.

To enable Error Log reporting of JTAG events, the Aux Port Error Report Enable Register.JTAG_LOG_EN bit must be set. Once this bit is set, JTAG events that are enabled as described in JTAG Events (Revision A/B Only) will be reported to the Error Log. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

6.3.6 Configuration Block Event Notification

Configuration events can trigger interrupt or Standard port-write notification. To enable Standard port-write notification for Configuration events, the Configuration Block Error Report Register. CFG_PW_EN bit must be set. Once this bit is set, Configuration events that are enabled as described in Configuration Block Events will cause a port-write to be sent.

To enable interrupt notification for any configuration event, the Configuration Block Error Report Register.CFG_INT_EN bit must be set. Once this bit is set, configuration events that are enabled as described in Configuration Block Events will cause the interrupt line to be asserted.

To enable Error Log reporting of Configuration events, the Configuration Block Error Report Register.CFG_LOG_EN bit must be set. Once this bit is set, configuration events that are enabled as described in Configuration Block Events will be reported to the Error Log. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

6.3.7 Trace and Filter Event Notification

When a packet matches at least one of the trace filters in a port, this event can cause an IDT port-write to be sent immediately. To cause an IDT port-write to be sent whenever there is a TRACE_MATCH_OCCURRED event, configure the following register bits:

- Port {0..17} Operations Register.PORT_LOG_EN = 1
- Port {0..17} Operations Register.TRACE_PW_EN = 1

FILTER_MATCH_OCCURRED events are always reported to the Error Log when Port {0..17} Operations Register.PORT_LOG_EN is set. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

6.3.8 Packet Generation and Capture Mode Event Notification

Packet Generation and Capture (PGC) events are always sent to the Error Log. For more information on how the Error Log can assert interrupts and send IDT port-writes, see Error Log Event Notification Programming Model.

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6.3.9 Port-Write Formats, Programming Model, and Generation

Port-write commands are signaled by the S-RIO port when an error is detected and captured either as defined in the *RapidIO Specification (Rev. 2.1), Part 8*, or as detected and captured using the IDT implementation-specific definition for errors that are not defined in Part 8 (such as lane-level errors). Two types of port-write packets can be generated by the CPS-1848:

- Standard port-write (see Table 55) – This packet has a 16-byte payload. Its format is defined in *RapidIO Specification (Rev. 2.1), Part 8.*
- IDT port-writes (see Table 56) – This packet has an 8-byte payload. Its format is IDT specific.

The type of port-write format that has been received can be determined based on the length of the port-write payload. For endpoints that do not capture the length of a received port-write payload, IDT recommends that devices generating Standard port-writes set at least one of the most significant two bits of the RapidIO standard Component Tag CSR, as these bits are never set in an IDT port-write.

6.3.9.1 Port-Write Programming Model

The registers listed in Table 54 control the physical and transport layer fields of Standard and IDT port-writes. These fields determine where port-writes are sent and their priority in the system. These fields must be configured before port-writes can be successfully received.

Table 54: Port-Write Programming Model Registers and Fields

Register	Field Name	Discussion
Port-Write Target deviceID CSR	DESTID_MSB, DESTID	destID for the endpoint(s) that will receive the port-writes. Note that port-writes can be multicast.
	LARGE	0 = 8-bit destIDs are used 1 = 16-bit destIDs are used
Port-Write Control Register	SRCID_MSB, SRCID	This value is reserved in the port-write. If the port-write receiver can capture the sourceID field of the port-write, this field can transfer static information in the port write. Otherwise, leave as 0.
	PRIO	RapidIO physical layer priority for all port-writes. Recommend that this be set to 0b11 (Priority 3)
	CRF	Critical Request Flow indicator for all port-writes. Recommend that this be set to 1.
	Note: A port-write packet does not support per-port route table.	

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6.3.9.2 Standard (Type 1) Port-Write Format

Standard port-writes are formatted as defined in the *RapidIO Specification (Rev. 2.1)*. The format is displayed in the following table.

Table 55: Standard (Type 1) Port-Write Format

Data Payload Byte Offset	Word	
0x0	Component Tag CSR	
0x4	Port {0..17} Error Detect CSR	
0x8	Implementation Specific	Port ID (byte)
0xC	Logical/Transport Layer Error Detect CSR	

This format supports the representation of errors from more than one error source in a Standard port-write command. However, the occurrence of errors from more than one source simultaneously is expected to be infrequent and not characteristic of typical conditions. In general, if errors from more than one error source occur simultaneously, then multiple port-write packets are issued such that each port-write represents an error from a single error source only.

The CPS-1848 supports corner cases to this rule however. For example, the Standard port-write format supports multiple errors from a source in the case of logical/transport layer errors and port-level errors.

Figure 26 summarizes how errors are reported in the Standard port-write packet data payload format for each potential error source (Note: JTAG error source is applicable to Revision A/B only).

Figure 26: Type 1 Port-Write Packet Data Payload Format

Rank	***Error source***	***LT-Layer[1] Error Detect CSR***	***Port n Error Detect CSR***	***Port ID (byte)***	***Implementation Specific***
1	LT Error	LT-Layer Error Detect CSR	0	port number	[23:8]=0, [7:0]=error_code
2	Port *n* Error	0	Port n Error Detect CSR	port number	[23:8]=0, [7:0]=error_code
3	Lane Error	0	0	Port number	[23:16]=0, [15:8]=ESlane, [7:0]=EClane
4	Config Error	0	0	0	[23:16]=0, [15:8]=ESconfig, [7:0]=ECconfig
5	I2C Error	0	0	0	[23:16]=0, [15:8]=ESI2C[2], [7:0]=ECI2C[3]
6	JTAG Error	0	0	0	[23:16]=0, [15:8]=ESJTAG, [7:0]=ECJTAG

NOTES:
[1]LT-Layer = Logical/transport layer
[2]ESI2C = Error source code identifying the I2C block (same as used in error logging)
[3]ECI2C = Error code for the particular I2C-related error which is detected

The Rank column indicates the precedence with which error source are handled in the event that they detect errors simultaneously (for example if an LT error occurred simultaneously with a Configuration Block error, then the LT error should be reported first). The Error source column lists the potential sources of CPS-1848 errors. All other columns represent the values that are stored in the various fields in the port-write command definition.

In all error reporting scenarios, the field of the Standard port-write format called Component Tag CSR is assigned with the value of the Component Tag CSR defined in the *RapidIO Specification (Rev. 2.1), Part 3*. This field is filled with the current value of the CPS-1848 register of the same name.

The method in which the remaining fields of the Type 1 port-write format are assigned is discussed in the following separate sections per classification of the error type.

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6.3.9.2.1 *Standard Port-Writes for Logical/Transport Layer Events*

The rank of Logical/Transport errors in Figure 26 indicates that, in the presence of errors from multiple error sources, the errors associated with the logical/transport layer outranks all other error sources and are reported in the next enabled Type 1 port-write packet.

The field of the Type 1 format named “Logical/Transport Layer Error Detect CSR” are filled with the current contents of the Logical/Transport Layer Error Detect CSR.

The field of the Type 1 format named Port {0..17} Error Detect CSR is filled with 32 bits of zero data because no port-level errors are reported in a Type 1 port-write in which logical/transport layer errors are being reported.

The field of the Type 1 format named “Port ID (byte)” is filled with an 8-bit value of the logical port number identifying the port that the packet arrived on which led to the detection of a L/T error.

The field of the Type 1 format named “Implementation specific” reports the Error Log code for the implementation-specific logical/transport layer errors, as in Table 44. The use of the implementation-specific field for the LT errors are relevant only when bit 31 of the Logical/Transport Layer Error Detect CSR is set to indicate that an implementation-specific LT error has occurred. If no implementation-specific event has occurred, the “Implementation Specific” field of the port-write contains a 0 value. If multiple implementation-specific events have occurred, only the first is reported.



The Logical/Transport Layer Error Detect CSR could have multiple bits set simultaneously.

6.3.9.2.2 *Standard Port-Writes for Port Events*

After logical/transport layer errors, port-level errors have the next highest priority for representation in Standard port-write packets.

For port-level errors the field of the Standard format named “Logical/Transport Layer Error Detect CSR” are set to all zeros. The field of the Type 1 named “Port n Error Detect CSR” are filled with the current value of the Port {0..17} Error Detect CSR from the port in which the error is detected. Note that multiple port-level errors can be indicated with the same port-write if multiple bits are set in this field. The “Port ID (byte)” field of the Standard format contains the logical port number identifying the port that detected the event.

In the same way as the reporting of LT errors, the Implementation Specific field for port-level errors reports additional IDT-defined implementation specific port-level errors beyond those defined by RapidIO specification. The presence of implementation-specific events is indicated if the Port {0..17} Error Detect CSR.IMP_SPEC_ERR bit is set in the port-write. The event code for the first implementation-specific port event detected is located in the least significant byte of the Standard port-write’s “Implementation Specific” field. These event codes are defined in Table 45 and Table 46. The remainder of the port-writes “Implementation Specific” field is set to 0.

6.3.9.2.3 *Standard Port-Writes for Lane Events*

Errors detected in an S-RIO lane-level block are reported as the next highest port-write priority if no logical/transport layer errors or port-level errors have been detected.

For lane-level errors, the Type 1 format fields in the Logical/Transport Layer Error Detect CSR and Port {0..17} Error Detect CSR are filled with a 32-bit zero value. The field named “Port ID (byte)” is filled with the 8-bit value of the port number identifying the port to which the lane in question is mapped through the lane-to-port mapping registers.

The “Implementation Specific” field represents a single lane-level error in the IDT specific error source and error code format, which is used in the Type 2 port-write packet payload associated with error logging. Bits [7:0] of the implementation specific field in the Type 1 format carry the value of the error code in Table 47. Bits [15:8] of the implementation-specific field carry the 8-bit value that identifies the physical lane number as the error source. Bits [23:16] of the implementation-specific field are always set to zero within the context of reporting lane-level errors in the Standard format.

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6.3.9.2.4 *Standard Port-Writes for Configuration, I²C, and JTAG Errors*

Standard port-writes that communicate the detection of configuration, I²C, or JTAG (Revision A/B only) errors have a consistent format. No events are in the Logical/Transport Layer Error Detect CSR and Port {0..17} Error Detect CSR, so these fields contain 0s. Similarly, no port number is associated with these events so the port number field is also always 0.

The middle byte of the "Implementation Specific" field communicates the event source for the port-write, as defined in Table 43. The least significant byte of the "Implementation Specific" field communicates the event type for that source, as defined in Table 48, Table 49, and Table 50. The most significant byte of the "Implementation Specific" field is always 0.

6.3.9.3 IDT (Type 2) Port-Write Format

IDT port-writes are sent by the Error Log. For more information on how the Error Log can generate interrupt and port-write notifications for events, see Error Log Event Notification Programming Model. The encoding of fields in IDT port-writes is discussed in Error Log Events. The full maintenance packet generated are as displayed in Table 56.

Table 56: IDT (Type 2) Port-Write Format

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Rsvd		Error Source						Error Code							
Error Flags								Error Counter							
Error Counter								Rsvd							
Rsvd															

The fields in the in the IDT Port-Write Payload are in the Error Log registers. They are described as follows:

- Error Source – Event source encoding, as defined in Table 43
- Error Code – Event encoding. Depending on the Error Source, defined in Table 44 to Table 51
- Error Flags – Least significant byte of the Error Log Match Status Register
- Error Counter – The CNT field of the Error Log Events Register

6.3.9.4 Port-Write Generation

Port-writes can be generated when an event is detected if port-write notification is enabled for an event. For more information, see the following:

- Logical Layer Events Notification
- Physical Layer Events Notification
- Lane Event Notification
- I2C Event Notification
- JTAG 1149.1 Event Notification (Revision A/B Only)
- Configuration Block Event Notification
- Trace and Filter Event Notification
- Packet Generation and Capture Mode Event Notification

Port-writes can also be generated by programming the Error Log Error Log Match Register {0..7} to select the required events and generate a port-write. For more information, see Error Log Event Notification Programming Model.

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6.3.10 Interrupt Notification

An interrupt can be immediately asserted when an event is detected if interrupt notification is enabled for an event. For more information, see the following:

- Logical Layer Events Notification
- Physical Layer Events Notification
- Lane Event Notification
- I2C Event Notification
- JTAG 1149.1 Event Notification (Revision A/B Only)
- Configuration Block Event Notification
- Trace and Filter Event Notification
- Packet Generation and Capture Mode Event Notification

Interrupts can also be generated by programming the Error Log Match Register {0..7} to select the required events and assert an interrupt. For more information, see Error Log Event Notification Programming Model.

This interrupt signal is implemented with an open-drain driver and active low. An interrupt is de-asserted when a detected event is cleared or disabled.

6.3.11 Error Log Event Notification Programming Model

The Error Log Error Log Match Register {0..7} can select events reported to the Error Log for interrupt or port-write notification. Events are encoded as a source and an 8-bit event code. For purposes of selection, the event code is partitioned into the upper 4 bits called the error group, and the lower four bits called the error number. The method of selection depends on the following pairs of fields in the Error Log Match Register {0..7}:

- ERR_SOURCE_MASK and ERR_SOURCE – ERR_SOURCE_MASK is set to 0 if the source of reported events should be compared to the ERR_SOURCE field.
- ERR_GROUP_MASK and ERR_GROUP – ERR_GROUP_MASK is set to 0 if the upper 4 bits of the event code should be compared to the ERR_GROUP value.
- ERR_NUM_MASK and ERR_NUM – ERR_NUM_MASK is set to 0 if the lower 4 bits of the event code should be compared to the ERR_NUM value.

Once an event has matched the enabled source, group, and number, there are four different methods to trigger notification, also in the Error Log Match Register {0..7}. The following bits determine how or if notification occurs. Multiple bits can be set at the same time, so that multiple notification functions are invoked:

- MAINT_PKT_EN – Send an IDT port-write.



Error Log Control 2 Register.MAINT_PKT_DIS must be cleared to send port-writes from the error log.

- FLAG_EN – Set the associated FLAG bit in the Error Log Match Status Register, and assert an interrupt (for more information, see Error Flags).
- CNT_EN – Increment the Error Log Events Register (for more information, see Error Counter).
- STOP_EN – Stop accepting more event reports into the Error Log, and optionally send an IDT port-write (for more information, see Error Management Stop).



The CPS-1848 interrupt line is an active-low signal (for more information, see the *CPS-1848 Datasheet*).

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6.3.11.1 Error Flags

If any bit is set in the Error Log Match Status Register, the interrupt signal is asserted. If the Error Log Register.ALL_FLAG_STOP bit is set, then when all flags are asserted, the following actions occur:

- The Error Log stops accepting more event reports
- The Error Log Control 2 Register.STOP_EM bit is set
- An IDT port-write is transmitted



All 8 flag bits must be asserted, which requires that all Error Log Match Register {0..7} settings must have detected an event.

6.3.11.2 Error Counter

Using the Error Log Match Register {0..7}, the user can define which errors when detected, increment the Error Log Events Register. If the counter reaches its maximum value of 0xFFFF it will stop incrementing, and remain at its maximum value until it is reset. If the Error Log Register.CNTR_MAX_STOP bit is set, and the counter reaches its maximum value, then the Error Log stops accepting more event reports and generates a port-write based on the register description.

The Counter is reset when the Error Manager is reset, or the CNT_RESET bit is set in the Error Log Control 2 Register.

6.3.11.3 Error Management Stop

The Error Manager will stop if a specific error is detected and the Error Log Match Register {0..7}.STOP_EN. bit is set. The user can stop the Error Manager by setting Error Log Control 2 Register.STOP_EM to 1. The user must set the same bit to 0 to enable the Error Manager function.

The Event Log stops accepting further events when the Error Manager is stopped.

6.3.11.4 Error Log Notification Examples

The examples in Table 57 demonstrate how to trigger IDT port-writes and interrupts under various scenarios. This assumes that the events have been configured to be reported to the Error Log as described in Event Notification.

Table 57: Error Log Event Notification Examples

Scenario	Step	Register Address	Register Value
Send an IDT port-write when lane 2 loses lane-sync	Configure Error Log Error Log Match Register {0..7} (n=3) for Notification	0xFD0014	0x00024260
Send an Interrupt when any lane loses lane-sync	Configure Error Log Error Log Match Register {0..7} (n=0) for Notification	0xFD0008	0x00440060
Count all lane events detected by the CPS-1848	Configure Error Log Error Log Match Register {0..7} (n=7) to count all lane events	0xFD0024	0x00580060

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6.4 Event Isolation

The RapidIO Error Management Extensions specify four standard event isolation behaviors when the physical layer error counters reach the port failed threshold value (Port {0..17} Error and Status CSR.OUTPUT_FAIL is set). The event isolation behavior selected depends on the STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN fields in the Port {0..17} Control 1 CSR. The behaviors are described in Table 58.



Event isolation is in effect while Port {0..17} Error and Status CSR.PORT_FAIL is set.

The value of the physical layer counters does not affect the event isolation behavior when PORT_FAIL is set. This behavior is not compliant to the *RapidIO Specification (Rev. 2.1)*.

Table 58: Standard Event Isolation Behaviors

Bit Setting		Port Behavior
STOP_ON_PORT_FAIL_ENC_EN	DROP_PKT_EN	
0	0	The port continues to attempt to transmit packets to the connected device if the Output Failed Encountered (OUTPUT_FAIL) bit is set in Port {0..17} Error and Status CSR and/or if the Error Rate Failed threshold has been met or exceeded in the Port {0..17} Error Rate Threshold CSR.
0	1	The port discards packets that receive a Packet-not-accepted control symbol when the Error Rate Failed Threshold has been met or exceeded. When a packet is discarded, the port sets the Output Packet-dropped bit in the Port {0..17} Error and Status CSR. If the output port "heals", the Error Rate Counter falls below the Error Rate Failed Threshold and the output port continues to forward all packets.
1	0	The port stops attempting to send packets to the connected device when the Output Failed Encountered (OUTPUT_FAIL) bit is set. The output port becomes congested.
1	1	The port discards all output packets without attempting to send them when the port's Output Failed Encountered (OUTPUT_FAIL) bit is set. When a packet is discarded, the port sets the Output Packet-dropped (OUTPUT_DROP) bit in the Port {0..17} Error and Status CSR. If the output port "heals," the Error Rate Counter may fall below the Error Rate Failed Threshold. However, contrary to the *RapidIO Specification (Rev. 2.1)*, the port will continue to discard packets until this state is cleared, as described in Clearing and Handling Port Fail and Port Degraded Events.

When a port detects an OUTPUT_FAIL condition and STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN are set, the port (or device) must be reset to safely clear the OUTPUT_FAIL condition. One implication of this requirement is that when STOP_ON_FAIL_ENC_EN and DROP_PKT_EN are set, the Port {0..17} Error Rate CSR[ERR_RATE_BIAS] must be set to 0 to prevent the port from "healing" on its own.



When STOP_ON_PORT_FAIL_ENC_EN and DROP_PKT_EN are set, only events which indicate that the link partner has been removed can be used to detect an OUTPUT_FAIL condition. These events are restricted to those documented in Hot Extraction/Insertion. Use of any other events requires a device reset to recover the CPS-1848 after an OUTPUT_FAIL condition is detected. For more information on device resets, see Resets after Power-Up.

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The CPS-1848 supports additional packet discard isolation functions to reduce the congestion impact of error events (see Table 59). They are discussed in subsequent sections

Table 59: Additional Packet Discard Isolation Trigger Functions

Event	Isolation Behavior
Fatal link response timeout	If Device Control 1 Register.FATAL_ERR_PKT_MGT is 0, then packets routed to a port with Port {0..17} Error and Status CSR.PORT_ERR asserted are dropped, and the port's Port {0..17} Error and Status CSR.OUTPUT_DROP bit is asserted. This event is detected when the packet is dropped. The Port {0..17} VC0 Transmitted Packets Dropped Counter Register counter is incremented for every packet dropped.
Received retry count trigger congestion	When the MANY_RETRY event is triggered for a port, all further packets routed to that port are dropped and the port's Port {0..17} Error and Status CSR.OUTPUT_DROP bit is asserted. The Port {0..17} VC0 Transmitted Packets Dropped Counter Register counter is incremented for every packet dropped.
TTL event	When the CPS-1848 Time-to-Live functionality is enabled, packets that are in the switch for longer than the configured Time-to-Live period are discarded. The port's Port {0..17} Error and Status CSR.OUTPUT_DROP bit is asserted. The Port {0..17} VC0 TTL Packets Dropped Counter Register counter is incremented for every packet dropped.
Transmit packet dropped via CRC retransmit limit	When the CPS-1848 CRC retransmission limit is enabled, packets transmitted that have exceeded the programmed CRC retransmission limit are discarded. The port's Port {0..17} Error and Status CSR.OUTPUT_DROP bit is asserted. The Port {0..17} VC0 CRC Limit Packets Dropped Counter Register counter is incremented for every packet dropped.
Received a packet with a CRC error while CRC error suppression enabled	When the CPS-1848 error suppression functionality is enabled, packets received that have a CRC error detected are discarded. The Port {0..17} VC0 Received Packets Dropped Counter Register counter is incremented for every packet dropped.
Received a packet that references a disabled port and is dropped	When Port {0..17} Control 1 CSR.PORT_DIS is set, packets routed to that port are dropped silently by the receiving port. The disabled port sets the Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE bit. The disabled port's Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register and Port {0..17} VC0 Transmitted Packets Dropped Counter Register will increment. No other counters on the disabled port will increment, including any of the dropped packet counters. This event is detected when the packet is dropped.
Received a packet that references a port configured in port lockout and is dropped	When Port {0..17} Control 1 CSR.PORT_LOCKOUT is set on a port, packets routed to that port are dropped. The locked out port sets Port {0..17} Error and Status CSR.OUTPUT_DROP and Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE. The locked out port's Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register and Port {0..17} VC0 Transmitted Packets Dropped Counter Register will increment.

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Table 59: Additional Packet Discard Isolation Trigger Functions *(Continued)*

Event	Isolation Behavior
Discarded a non-maintenance packet to be transmitted	When Port {0..17} Control 1 CSR.PORT_LOCKOUT and OUTPUT_PORT_EN are cleared, non-maintenance packets routed to that port are dropped. The port sets Port {0..17} Error and Status CSR.OUTPUT_DROP and Port {0..17} Implementation Specific Error Detect Register.TX_DROP bit. The port's Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register and Port {0..17} VC0 Transmitted Packets Dropped Counter Register will increment. This event is detected when the packet is dropped.
Discarded a received non-maintenance packet	When Port {0..17} Control 1 CSR.PORT_LOCKOUT and INPUT_PORT_EN are cleared, non-maintenance packets transmitted by the link partner are refused. The port sets Port {0..17} Implementation Specific Error Detect Register.RX_DROP. The port's Port {0..17} Not Acknowledgements Transmitted Counter Register will increment with every retransmission attempted by the link partner. This event is detected when the packet is refused.
Received a packet that references no route and is dropped	The packet is dropped by the receiving port. The port sets the Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE. The port's Port {0..17} VC0 Received Packets Dropped Counter Register will increment. When a packet is received whose destID selects a routing table entry with "no route", that packet is dropped. This event is detected when the packet is dropped.

6.4.1 Fatal Link Response Timeout Isolation

This isolation function is useful if communication with a link partner can be spontaneously interrupted and the application cannot continue to operate correctly due to resulting congestion. Possible causes are that the link partner reset itself, or the link begins to retrain during normal operation.

In the event of errors, the standard RapidIO error recovery function attempts to recover communication. If no response is received from the link partner, or if the CPS-1848 detects that ackID synchronization has been lost through reception of a link-response control symbol with an invalid ackID, then it is certain that communication cannot be re-established without software intervention.

Since software intervention can take significant time during which congestion related failure can occur, this isolation function allows packets to be discarded.

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6.4.2 Received Retry Count Trigger Congestion Isolation

When traffic patterns are engineered to avoid retries, the detection of retries can indicate that the real-time aspects of the system have failed. This isolation function can be invoked to ensure that the forward progress of other traffic flows is not impacted by this failure as indicated by the presence of too many consecutive retries.

To enable retry count congestion isolation:

1. Set Port {0..17} Congestion Retry Counter Register[RETRY_LIM] to a value that will indicate unexpected congestion in the system.
2. Set Port {0..17} Status and Control Register[RETRY_LIM_EN] to enable detection of the MANY_RETRY event.

   The detection of a MANY_RETRY event immediately triggers packet discard until the MANY_RETRY event is cleared. When the Port {0..17} VC0 Transmitted Packets Dropped Counter Register is enabled by setting Port {0..17} Operations Register[CNTRS_EN], this register indicates how many packets were dropped due to a MANY_RETRY event.

To enable notification for a MANY_RETRY event:

1. Set Port {0..17} Implementation Specific Error Report Enable Register[MANY_RETRY_EN].

   A MANY_RETRY event is indicated by Port {0..17} Implementation Specific Error Detect Register[MANY_RETRY].

To clear the MANY_RETRY event:

1. Write 1 to Port {0..17} Status and Control Register[CLR_MANY_RETRY].

6.4.3 TTL Event Isolation

For users who are unable to make use of the CPS-1848 VoQ Fairness/Starvation Avoidance function, time-to-live functionality enables the detection of pathological traffic patterns that prevent lower priority packets from making forward progress in an acceptable amount of time.

The discard of these packets serves three purposes:

- It notifies the user that some packets are not making forward progress in the required amount of time, ensuring that traffic engineering defects are detected and corrected.
- It ensures that requests that have timed out at an endpoint have been completely flushed from the system.
- It slowly flushes packets that cannot make forward progress in the system, freeing resources for higher priority packets and assisting in system recovery.

6.4.4 Transmit Packet Dropped via CRC Retransmit Limit Isolation

A packet can become corrupted as it passes through the CPS-1848 under rare circumstances. The packet's corruption is detected by the link partner, which prevents the packet from being successfully transmitted by the CPS-1848.

The CRC retransmission limit isolation function will discard a packet corrupted in this manner quickly, avoid the impact associated with other slower isolation functions, such as time-to-live. This isolation function ensures that packets are only dropped in this rare case.

6.4.5 Packet Received With a CRC Error While CRC Error Suppression Enabled Isolation

The CRC error suppression isolation function supports system operation when a traffic flow cannot accept the additional latency of error recovery from retransmission errors.

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6.4.6 Software Controlled Isolation Functions

The following isolation functions/events are invoked under software control:

- Packet received that references a disabled port and is dropped
- Packet received that references a port configured in port lockout and is dropped
- Discarded a non-maintenance packet to be transmitted
- Discarded a received non-maintenance packet
- Packet received that references no route and is dropped

These isolation functions enable software to prevent a CPS-1848 link partner from accessing all or part of the system, and to ensure that unauthorized access to a CPS-1848 link partner cannot occur.

A port should be disabled if no link partner is ever expected to be present on the link (see Port {0..17} Control 1 CSR.PORT_DIS). A port should be placed in port-lockout if a new link partner may appear (see Port {0..17} Control 1 CSR.PORT_LOCKOUT).

INPUT_PORT_EN and OUTPUT_PORT_EN isolation should be used to enable configuration and limited communication with a new link partner.

The “No Route” routing table value should be used to prevent one link partner from accessing another link partner, or to ensure that no link partners attempt to use a specific destID.



Packet filtering functionality can implement finer grained isolation of the link partner from the remainder of the system (for more information, see Packet Trace and Filtering).

6.5 Event Clearing and Recovery

After an event is detected and reported, the software entity that receives the report must perform any reconfiguration of the system necessary to continue system operation. The software entity must also clear the event, and disable any isolation function that was activated.

IDT recommends that once one event has been received, all outstanding events should be handled. Only one event usually will be outstanding at any specific time. There are situations that can result in the detection of multiple events.

The following sections describe how to clear each event, and provide advice on the handling of each event.

6.5.1 Logical Layer Event Clearing and Handling

Table 60 describes how to clear and handle logical layer events.

Table 60: Logical/Transport Layer Event Enable and Information Capture Summary

Event	Clearing The Event	Event Handling Discussion
Illegal transaction decode	Logical/Transport Layer Error Detect CSR.ILL_TRAN = 0	This error could indicate a hardware/software failure in the originating endpoint, or a highly unlikely transmission error.
Unsolicited response	Logical/Transport Layer Error Detect CSR.UNSOL_RESP = 0	Receipt of a maintenance response implies a routing error. Check the routing for the destID latched in the Logical/Transport Layer deviceID Capture CSR. There should be a timeout for a maintenance request originated by the sourceID latched in this same register.

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Table 60: Logical/Transport Layer Event Enable and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Unsupported transaction	Logical/Transport Layer Error Detect CSR.UNSUP_TRAN = 0	Receipt of a port-write implies a routing error. Check the routing for the destID latched in the Logical/Transport Layer deviceID Capture CSR.
Maintenance read size invalid	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	Indicates an incorrect request generated by the endpoint associated with the sourceID latched in the Logical/Transport Layer deviceID Capture CSR. A software/hardware error needs to be corrected.
Maintenance write size invalid	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	Indicates an incorrect request generated by the endpoint associated with the sourceID latched in the Logical/Transport Layer deviceID Capture CSR. A software/hardware error needs to be corrected.
Maintenance read received with data	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	This error could indicate a hardware/software failure in the originating endpoint, or a highly unlikely transmission error.
Maintenance write received without data	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	This error could indicate a hardware/software failure in the originating endpoint, or a highly unlikely transmission error.
Maintenance transaction field error	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	This error could indicate a hardware/software failure in the originating endpoint, or a highly unlikely transmission error.
Maintenance packet received was too short or too long	Logical/Transport Layer Error Detect CSR.IMP_SPEC_ERR = 0	This error could indicate a hardware/software failure in the originating endpoint, or a highly unlikely transmission error.

6.5.2 Physical Layer Events Clearing and Handling

Almost all physical layer events are the result of transmission errors. Some, however, indicate that ackID synchronization has been lost, or that the link partner has disappeared. In these cases, more significant handling work must be done.



Note that for all events, the Port {0..17} Attributes Capture CSR.VALID bit must be cleared to 0 to enable information capture for future events.

Table 61: Physical Layer Events and Information Capture Summary

Event	Clearing The Event	Event Handling Discussion
Control symbol CRC error	Port {0..17} Error Detect CSR.CS_CRC_ERR = 0	Transmission error - hardware error recovery
Received an acknowledgement control symbol with unexpected ackID	Port {0..17} Error Detect CSR.UNEXP_ACKID = 0	See Loss of AckID Synchronization
Received a packet not accepted control symbol	Port {0..17} Error Detect CSR.CS_NOT_ACC = 0	Transmission error - hardware error recovery
Received a packet with a bad ackID	Port {0..17} Error Detect CSR.PKT_ILL_ACKID = 0	Transmission error - hardware error recovery. See Loss of AckID Synchronization.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Received a packet with bad CRC	Port {0..17} Error Detect CSR.PKT_CRC_ERR = 0	Transmission error - hardware error recovery
Received a packet that exceeds 276 bytes	Port {0..17} Error Detect CSR.PKT_ILL_SIZE = 0	Transmission error - hardware error recovery.
Received a data character in IDLE1	Port {0..17} Error Detect CSR.IDLE1_ERR = 0	Transmission error - hardware error recovery
Non-outstanding ackID in Link-Response	Port {0..17} Error Detect CSR.LR_ACKID_ILL = 0	See Loss of AckID Synchronization
Protocol error	Port {0..17} Error Detect CSR.PRTCL_ERR = 0	Most likely the result of a transmission error, which is corrected through hardware error recovery. May indicate loss of ackID synchronization. See Loss of AckID Synchronization.
Delineation error	Port {0..17} Error Detect CSR.DELIN_ERR = 0	Transmission error - hardware error recovery This event is typically caused by a single bit error on the link. It may occur as part of the normal operation of a system. This event is likely to be reported when SILENT is detected.
Unsolicited acknowledgement control symbol	Port {0..17} Error Detect CSR.CS_ACK_ILL = 0	May indicate loss of ackID synchronization. See Loss of AckID Synchronization
Link timeout	Port {0..17} Error Detect CSR.LINK_TIMEOUT = 0	Most likely the result of link partner going silent due to reset or multiple transmission errors. May indicate imminent loss of ackID synchronization. See Loss of AckID Synchronization.
Received a packet when an error rate threshold event has occurred and drop packet mode is enabled	Port {0..17} Implementation Specific Error Detect Register.ERR_RATE = 0 then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Clearing and Handling Port Fail and Port Degraded Events
A packet was dropped due to a TTL event	Port {0..17} Implementation Specific Error Detect Register. TTL_EVENT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	This is an indication that: Other, lower latency isolation functions are not configured correctly Pathological traffic conditions can cause packet latency to be larger than what was expected The time-to-live period is set too short If the packet latched is a request that requires a response, or a response packet, an endpoint should report a related logical layer response timeout either before or after this event has occurred.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
A transmitted packet was dropped via CRC error retransmit limit	Port {0..17} Implementation Specific Error Detect Register.CRC_EVENT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	This is an indication that a packet was corrupted within the switch. This should be an extremely rare occurrence.
Received a packet with a CRC error with CRC error suppression enabled	Port {0..17} Implementation Specific Error Detect Register.CRC_EVENT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Transmission error – there should not be any logical layer timeouts related to this packet discard.
Received a NAK other than lack of resources	Port {0..17} Implementation Specific Error Detect Register.PNA = 0 then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	The reasons found in the control symbol indicate the severity of the error: 1, 2, 4, 5, 7, and 15 all indicate that a transmission error has been detected and hardware error recovery is sufficient to recover. 3 (non-maintenance packet reception is stopped) indicates that the link partner has isolated itself. The system should prevent non-maintenance packets from being routed to this port, and/or configure an isolation function for this port. 6 (lack of resources) should not be latched in this case.
Received an unsolicited link response	Port {0..17} Implementation Specific Error Detect Register.UNSOL_LR = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Loss of AckID Synchronization
Received an unexpected ackID	Port {0..17} Implementation Specific Error Detect Register.UNEXP_ACKID = 0 then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Loss of AckID Synchronization
Received a packet when no buffer available	Port {0..17} Implementation Specific Error Detect Register.PNA_RETRY = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Expected event under receiver-controlled flow control, hardware error recovery function is sufficient. May indicate incorrect or speculative operation under transmitter-controlled flow control.
Received a packet that references no route and is dropped	Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	If packets are not expected to be sent to “no route” destIDs and dropped, this indicates a configuration/software implementation error.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Received a packet that references a disabled port and is dropped	Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	If packets are not expected to be sent to disabled ports and dropped, this indicates a configuration/software implementation error.
Received a packet that references a port configuration in port lockout and is dropped	Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	If packets are not expected to be sent to locked out ports and dropped, this indicates a configuration/software implementation error.
Received a packet that references a port in the fatal error state and is dropped	Port {0..17} Implementation Specific Error Detect Register.RTE_ISSUE = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Loss of AckID Synchronization
Set outstanding ackID invalid	Port {0..17} Implementation Specific Error Detect Register.SET_ACKID = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Loss of AckID Synchronization
Discarded a non-maintenance packet to be transmitted	Port {0..17} Implementation Specific Error Detect Register.TX_DROP = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	If packets are not expected to be sent to ports with the Port {0..17} Control 1 CSR.OUTPUT_PORT_EN isolation function enabled, this indicates a configuration/software implementation error.
RX retry count triggered congestion	Port {0..17} Implementation Specific Error Detect Register.MANY_RETRY = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Indicates that traffic is not being accepted at the engineered rate. This indicates a configuration/software implementation error.
Discarded a received non-maintenance packet Note: The packet is not accepted by the receiver, but the transmitter retains the packet. The packet remains in the system.	Port {0..17} Implementation Specific Error Detect Register.RX_DROP = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	If packets are not expected to be sent to ports with the INPUT_EN isolation function enabled, this indicates a configuration/software implementation error.
Received a packet that has an invalid TT	Port {0..17} Implementation Specific Error Detect Register.BAD_TT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Receipt of a packet with valid CRC and invalid TT code indicates a hardware configuration or implementation error, or an extremely rare transmission error.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Received a packet that is too short	Port {0..17} Implementation Specific Error Detect Register.SHORT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Transmission error. Packet should also have a bad CRC, which should result in hardware error recovery.
Unsolicited restart from retry	Port {0..17} Implementation Specific Error Detect Register.UNSOL_RFR = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Could be sent by the link partner after this end of the link has been reset. May indicate a hardware/software implementation error.
Fatal link response timeout	Port {0..17} Implementation Specific Error Detect Register.FATAL_TO = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Indicates that the link partner has stopped responding to the error recovery function, or ackID sync has been lost. See Loss of AckID Synchronization.
Received a retry control symbol with a valid ackID	Port {0..17} Implementation Specific Error Detect Register.RETRY = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Expected event under receiver-controlled flow control. If retries should not be received, see the Received Retry Count Trigger Congestion Isolation.
Received a retry control symbol with unexpected ackID	Port {0..17} Implementation Specific Error Detect Register.RETRY_ACKID = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	See Loss of AckID Synchronization
Stomp timeout	Port {0..17} Implementation Specific Error Detect Register.STOMP_TO = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Indicates that the link partner has stopped responding to the error recovery function, or ackID sync/link state has been lost due to link partner reset. See Loss of AckID Synchronization
Stomp received	Port {0..17} Implementation Specific Error Detect Register.RX_STOMP = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Expected event if the link partner is a switch operating in cut-through mode. Hardware error recovery is sufficient.
Link request with reserved command encoding	Port {0..17} Implementation Specific Error Detect Register.LR_CMD = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Link partner may be a device compliant to a version of the *RapidIO Specification* after 2.1, or may be incorrectly implemented. Ignore the link request and continue normal operation. No hardware error recovery is used.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Double link request	Port {0..17} Implementation Specific Error Detect Register.LR_X2 = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Link partner may be a device compliant to a version of the *RapidIO Specification* after 2.1, or may be incorrectly implemented. Ignore the link request and continue normal operation. No hardware error recovery is used.
Received EOP outside of a packet	Port {0..17} Implementation Specific Error Detect Register.UNEXP_EOP = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Either of the following may have occurred: • A hardware/software failure in the originating endpoint • A (highly unlikely) transmission error
Received stomp outside of a packet	Port {0..17} Implementation Specific Error Detect Register.UNEXP_STOMP = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Either of the following may have occurred: • A hardware/software failure in the originating endpoint • A (highly unlikely) transmission error
Port initialization TX required	Port {0..17} Implementation Specific Error Detect Register.PORT_INIT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Indicates the link completed reinitialization. If the link partner was reset, this may indicate that ackID synchronization has been lost. See Loss of AckID Synchronization.
Port width downgrade	Port {0..17} Implementation Specific Error Detect Register.PORT_WIDTH = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Indicates a significant loss of bandwidth on the link. Software may attempt reinitialization of the port to determine if this was the result of a permanent or transient error condition. Isolation functions may be necessary to reduce congestion caused by loss of bandwidth.
IDLE character in packet	Port {0..17} Implementation Specific Error Detect Register.IDLE_IN_PKT = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Transmission error - hardware error recovery
Loss of alignment	Port {0..17} Implementation Specific Error Detect Register.LOA = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Multiple transmission errors have caused the link to reinitialize. Note that no packets are lost, and link state is retained.

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Table 61: Physical Layer Events and Information Capture Summary *(Continued)*

Event	Clearing The Event	Event Handling Discussion
Bad control character sequence	Port {0..17} Implementation Specific Error Detect Register.BAD_CTL = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	Transmission error - hardware error recovery
Lanes reordered	Port {0..17} Implementation Specific Error Detect Register.REORDER = 0, then Port {0..17} Error Detect CSR.IMP_SPEC_ERR = 0	May be expected on some boards due to lane connections between devices.

6.5.2.1 Loss of AckID Synchronization

Each S-RIO port supports the software-assisted error recovery registers defined in the *RapidIO Specification (Rev. 2.1)*. These registers include the Port {0..17} Link Maintenance Request CSR, the Port {0..17} Link Maintenance Response CSR, and the Port {0..17} Local ackID CSR. A set of each of these three registers are provided per S-RIO port. Their use is described in subsequent sections.

Additionally, if the link partner supports a per-port reset function, it may be possible to cleanly recover from loss of ackID sync by resetting the link partner (for more information, see Reset Control Symbol Processing).

6.5.2.1.1 Usage Definition for Port {0..17} Link Maintenance Request CSR

A write to this register forces the S-RIO port to transmit a Link-Request symbol on the associated link. The command field in the transmitted symbol are the contents of the CMD field written into this register. A read of this register returns the value of the CMD field in the register.

Support is provided for the following CMD field values:

- 0b011 = Reset device
- 0b100 = Input status

6.5.2.1.2 Port {0..17} Link Maintenance Request CSR (Reset Command Field)

When a write to this register is received with the CMD field set to 0b011 (reset device) the device will:

- Cease all current and pending transmissions (data and S-RIO control symbols – including multicast control symbols)
- Transmit four Link-Request – Reset Symbols in succession. After transmitting the Link-Request - Reset Symbols, the port will enter the output error state and wait for a corresponding Link-Response.

6.5.2.1.3 Usage Definition for Port {0..17} Link Maintenance Response CSR

This register is read-only and contains the information contained in the most recently received Link-Response by the specific port. When read, it returns this data.

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6.5.2.1.4 *Usage Definition for Port {0..17} Local ackID CSR*

All fields defined for this register are supported.



Before changing the contents of Port {0..17} Local ackID CSR, ensure that Port {0..17} Error and Status CSR[OUTPUT_FAIL] is clear and will remain clear. Changing this register when OUTPUT_FAIL is set will result in undefined device operation.

6.5.2.1.5 *Clear Outstanding ackIDs*

The CLR bit in the Port {0..17} Local ackID CSR is write only. When set to 1, the S-RIO port handles all previously transmitted packets for which acks have not been received as having been properly received from the link partner. Acknowledgment processing for these packets is then no longer required.

6.5.2.1.6 *Inbound ackID*

Each S-RIO port supports both reads from and writes to the INBOUND field in the Port {0..17} Local ackID CSR. If read, the S-RIO port will return the value of the expected ackID of the next received packet.

If written, this field will set the expected ackID for the next received packet to the value supplied with the write. If the port receiver is in a stopped state it returns to the normal operational state after updating the expected ID value. If a packet is received during this transition, it is dropped without response.

6.5.2.1.7 *Outbound ackID*

Each S-RIO port supports both reads from and writes to the OUTBOUND field in the Port {0..17} Local ackID CSR. If read, the S-RIO port will return to the value that the device will use for the next transmitted packet.

If written, the effect depends on whether or not there are outstanding ackIDs. If there are no outstanding ackIDs, the next transmitted packet will use the ackID written into this register. If there are outstanding ackIDs, the packets that have been previously transmitted (without the device having received an acknowledgement), are retransmitted using ackIDs that start from the value written into this register.

6.5.2.1.8 *Outstanding ackID*

Each S-RIO port supports both reads from and writes to the OUTSTD field in the Port {0..17} Local ackID CSR. If read, this field indicates the value of the next expected acknowledgement (ackID field of control symbol) from the port's link partner.

6.5.2.2 Clearing and Handling Port Fail and Port Degraded Events

To clear a Port Degraded threshold event, the following register accesses must be performed in the order listed. Once done, this clears the detected errors, and enables information to be captured for new errors:

1. Disable the events feeding the Port {0..17} Error Rate CSR.ERR_RATE_CNTR.
2. Clear the Port {0..17} Error Rate CSR.ERR_RATE_CNTR.
3. Clear the Port {0..17} Error and Status CSR.PW_PNDG.
4. Re-enable events that supplied Port {0..17} Error Rate CSR.ERR_RATE_CNTR.

To clear a Port Fail threshold event, the following register accesses must be performed in the order listed. Once done, this clears the detected errors, disables the PORT_FAIL isolation function, and enables information to be captured for new errors:

1. Disable the events feeding the Port {0..17} Error Rate CSR.ERR_RATE_CNTR.
2. Clear the Port {0..17} Error Rate CSR.ERR_RATE_CNTR.
3. Clear the Port {0..17} Error and Status CSR.PW_PNDG.
4. Reset the port using a reset request from the link partner, or through the Device Reset and Control Register.
5. Clear up any error conditions resulting from the per-port reset (see HS-LP Controlled Recovery).

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6. Re-enable events that supplied Port {0..17} Error Rate CSR.ERR_RATE_CNTR.
7. Resume normal packet exchange on the link.

6.5.3 Lane Event Clearing and Handling

Table 62 describes how to clear and handle lane events.

Table 62: Lane Event Clearing and Handling

Event	Clearing The Event	Event Handling Discussion
Lane inversion detected	Lane {0..47} Error Detect Register.LANE_INVER_DET = 0	May be expected on some boards due to lane connections between devices.
IDLE2 framing error	Lane {0..47} Error Detect Register.IDLE2_FRAME = 0	Transmission error. Hardware error recovery is invoked only if the link and port have been initialized, as indicated by Port {0..17} Error and Status CSR.PORT_OK = 1 and PORT_UNINIT = 0.
Receiver/transmitter mismatch	Lane {0..47} Error Detect Register.TX_RX_MISMATCH = 0	Link partners will attempt to establish communication, but this may be unsuccessful. This is an “information only” event.
Loss of descrambler sync	Lane {0..47} Error Detect Register.DESCRAM_SYNC = 0	Transmission error. Hardware error recovery is invoked only if the link and port have been initialized, as indicated by Port {0..17} Error and Status CSR.PORT_OK = 1 and PORT_UNINIT = 0.
Received an illegal or invalid character	Lane {0..47} Error Detect Register.BAD_CHAR = 0	Transmission error. Hardware error recovery is invoked only if the link and port have been initialized, as indicated by Port {0..17} Error and Status CSR.PORT_OK = 1 and PORT_UNINIT = 0.
Loss of lane ready	Lane {0..47} Error Detect Register.LANE_RDY = 0	This indicates that transmit pre-emphasis adjustment has restarted. This may result in link reinitialization.
Loss of lane synchronization	Lane {0..47} Error Detect Register.LANE_SYNC = 0	This indicates that the error rate on the link is too high for reliable communication. This usually means that the link partner is attempting link reinitialization.

6.5.4 I^2C Event Clearing and Handling

Table 63 describes how to clear and handle I^2C events.

Table 63: I^2C Event Clearing and Handling

Event	Clearing The Event	Event Handling Discussion
I2C checksum error	Aux Port Error Detect Register.I2C_CHKSUM_ERR = 0	The EEPROM accessed does not have a valid format. Change the EEPROM contents to have the correct checksum, or disable EEPROM checksum verification.
I2C unexpected start/stop	Aux Port Error Detect Register.UNEXP_START_STOP = 0	I^2C slave was the target of an aborted transaction.

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Table 63: I2C Event Clearing and Handling

Event	Clearing The Event	Event Handling Discussion
I2C 22-bit memory address incomplete	Aux Port Error Detect Register.I2C_ADDR_ERR = 0	I2C slave was the target of a transaction with an incorrect address size.
I2C acknowledgement error	Aux Port Error Detect Register.I2C_ACK_ERR = 0	When detected by the I2C master, this means that no device acknowledged the request, or that the device did not acknowledge receipt of a written byte. When detected by the I2C slave, this means that the master did not acknowledge the transmission of a read byte.
I2C length error	Aux Port Error Detect Register.I2C_LENGTH_ERR = 0	When detected by the I2C slave, this means that the master did not sent four bytes for a write, or requested more than four bytes for a read transaction.

6.5.5 JTAG 1149.1 Events (Revision A/B Only)

Table 64 describes how to clear and handle JTAG events.

Table 64: JTAG Event Clearing and Handling (Revision A/B Only)

Event	Clearing The Event	Event Handling Discussion
JTAG incomplete write	Aux Port Error Detect Register.JTAG_ERR = 0	A write to registers transaction was partially completed. This may be caused by normal operation (JTAG Interface reset).

6.5.6 Configuration Block Events

Table 65 describes how to clear and handle Configuration Block events.

Table 65: Configuration Block Event Clearing and Handling

Event	Clearing The Event	Event Handling Discussion
Multicast translation error	Configuration Block Error Detect Register.BAD_MCAST = 0	Software or debug tool operation error.
Route table configuration error	Configuration Block Error Detect Register.BAD_RTE = 0	Software or debug tool operation error.
Force local configuration error	Configuration Block Error Detect Register.RTE_FORCE = 0	Software or debug tool operation error.
Port configuration error	Configuration Block Error Detect Register.BAD_PORT = 0	Software or debug tool operation error.
Multicast mask configuration error	Configuration Block Error Detect Register.BAD_MASK = 0	Software or debug tool operation error.

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6.5.7 Trace, Filter, and PGC Events

Table 66 describes how to clear trace, filter, and PGC mode events. As these are all debug mode events, their handling is entirely up to the user.

Table 66: Trace, Filter, and PGC Mode Event Clearing

Event	Clearing The Event
Trace match occurred	Clear the Port {0..17} Trace Match Counter Value 0 Register, Port {0..17} Trace Match Counter Value 1 Register, Port {0..17} Trace Match Counter Value 2 Register, and/or Port {0..17} Trace Match Counter Value 3 Register counters for the port where the trace match occurred.
Filter match occurred	Clear the Port {0..17} Filter Match Counter Value 0 Register, Port {0..17} Filter Match Counter Value 1 Register, Port {0..17} Filter Match Counter Value 2 Register and/or Port {0..17} Filter Match Counter Value 3 Register counters for the port where the filter match occurred.
Packet generation and capture complete	Recovery from Packet Generation and Capture mode requires that the START and END ports are reset using the Device Reset and Control Register. This will clear the event. For more information on Packet Generation and Capture mode, see Packet Generation and Capture.

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7. I²C Interface

This chapter discusses the I²C capabilities of the CPS-1848. Topics discussed include the following:

- Overview
- Master/Slave Configuration
- Temporary Master Mode
- Slave Mode

7.1 Overview

The I²C Interface is compliant with the *I²C Specification* as a slave device and as a temporary master. The I²C port can be thought of primarily as a control plane access point for the CPS-1848. An external device such as a host processor can use it to access the CPS-1848's registers. The port can also be used by the CPS-1848 to load registers.

The use of the I²C port is not targeted as a bridge to other external devices through the CPS-1848's RapidIO ports. There is no special safeguard on the I²C address assignment inside the device. Users should assign the I²C address as per specification.

7.2 Master/Slave Configuration

The CPS-1848 provides an external signal, MM_N, to configure the device in Master mode or Slave mode out of reset. When this signal is tied to GND, it configures the device into temporary Master mode after reset. If left floating, it will configure the device into Slave mode after reset. If not connected to GND, the MM_N signal will default to high.

7.3 Temporary Master Mode

The CPS-1848 supports temporary Master mode to directly obtain its configuration from an external EEPROM using I²C. As such, in Master mode the device can read/download its registers from an external EEPROM.

The device supports configuration into temporary Master mode in two ways:

1. If an external Master mode signal is tied to GND, the device will come out of reset in Master mode.
2. If the Master mode signal is left floating the device will come out of reset in Slave mode, but can be configured to transition to Master mode. This is done by setting I2C frequency (SPD_SEL), slave address (EPROM_ADDR), and checksum disable (CHKSUM_DIS) in I2C Master Control Register and I2C Master Status and Control Register.

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7.3.1 Obtaining Configuration in Master Mode

If the Master mode signal, MM_N, is tied to GND, the CPS-1848 will attempt to load its configuration registers after the device reset sequence has completed. The CPS-1848 uses a 7-bit address of 1010[ID2][ID1][ID0] as the slave address of the device from which it will obtain its configuration. [ID2][ID1][ID0] are external signals to the device, and are the same three lower bits that would be used for the device's I^2C address when configured as a slave. When configured to come out of reset as an I^2C master, the device supports communication only with an external device that has a 7-bit address. 10-bit I^2C addressing is not supported in this mode. The data includes a CRC value that the CPS-1848 uses to compare against its own calculated value to determine the validity of the registers load. The registers are loaded from the EEPROM regardless of the value of the checksum, but a flag is set (I2C Master Status and Control Register.CHKSUM_FAIL) if the CRC fails.

When in this mode, the state of the external ADS signal is ignored. Once the CPS-1848 completes its configuration sequence (successfully or unsuccessfully), it reverts to Slave mode (where the ADS signal becomes active).

7.3.2 Commanded Master Mode

The CPS-1848 can be commanded into temporary Master mode using a maintenance write to the I2C Master Control Register and I2C Master Status and Control Register. In this scenario, the device has come out of reset in Slave mode with the Master mode external signal left floating, or optionally tied to V_{DD3} (3.3V). Writing to START_READ in the I2C Master Status and Control Register causes the device to transition from Slave to temporary Master mode and read the EEPROM from the address specified in the EPROM_START_ADDR.

Commanded Master mode provides more configuration sequence flexibility. In this scenario the EEPROM slave address, and the EEPROM start address for the download, are both programmable. Whether or not a checksum comparison is performed to validate the download is also programmable. These configuration sequence options are established by writes to the I2C Master Control Register and I2C Master Status and Control Register.

During (and after) the configuration sequence, the CPS-1848 provides status information about the operation. This status includes whether any I^2C errors occurred, whether the operation is active or finished (see I2C Master Status and Control Register.READING), and whether the operation was successful (see I2C Master Status and Control Register.SUCCESS). The ability to abort the operation using a maintenance write to the I2C Master Status and Control Register is also provided.

When the device is in temporary Master mode, the state of the external ADS signal is ignored. Once the device completes its configuration sequence (successfully or unsuccessfully), it reverts to slave mode (where the ADS signal will become active).

7.3.3 Master Clock Frequency

While in Master mode, the CPS-1848 can be configured to supply a clock of either 100 kHz (Standard mode) or 400 kHz (Fast mode). For more information, see I2C Master Control Register.SPD_SEL.

7.3.4 EEPROM Format

The device's register map is based on the concept of configuration blocks whose definition and accompanying data is located at specific places in the EEPROM address map. The definition of the register map is as follows:

1. Byte addresses 0x0000 and 0x0001 contain the version number to be used as an initial verification of the registers (see Table 67). Each address must contain the value 0xAA, otherwise the EEPROM contents will not be loaded.
2. Byte addresses 0x0002 and 0x0003 define the number of configuration blocks that are in the register map. This value is one less than the number of configuration blocks in the device. For one image, the value should be 0x00 for each address.
3. Byte address 0x0004 is the start of the first block. All blocks have the same format.
4. The first byte in the block encodes the lower 8 bits [7:0] of a 10-bit word defining the number of registers represented in this block. A value of 0 = 1 register, 1 = 2 registers, and so on.
5. The first two bits in the second byte (bits 7 and 6) are the upper two bits of the number of registers loaded. The lower 6 bits are the upper bits of the address (bits [21:16]).

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6. Bytes 3 and 4 of the block encode the address to load the data that follows. The 22-bit address is the 24-bit device register address with the lower 2 bits dropped and assumed to be zero.
7. The remainder of the bytes of the block contain the data to be loaded into consecutive register addresses.

   Registers in the memory-mapped routing table section (range 0xE00000–0xE217FF) are treated as 8-bit registers, and require a single byte to load each register. All other registers in the device require four bytes per register. The example in Table 69 shows the loading of both types of registers.
8. Subsequent blocks use the same format, number of registers, address, and data.
9. Note, registers that are only 8 bits wide will only load 8 bits of data from the EEPROM. The data for subsequent registers will be every 8 bits.
10. The last two bytes of the register map represent the CRC for the image (for more information, see CRC Calculation).

A tabular view of this definition is displayed below.



When a port or lane configuration operation occurs within the EEPROM load, IDT recommends a subsequent port re-initialization or reset (for more information, see Port Reconfiguration Operations).

Table 67: EEPROM Register Address Map

EEPROM Address (Byte-Level Addresses)	Bits	EEPROM Contents	Comments
0x0000	0:7	First byte of Version Number [0:7]	This value must be = 0xAA. The two version bytes are used as an early validation of the format of the memory block. If the read value from the EEPROM does not equal 0xAA the read configuration sequence will be terminated.
0x0001	0:7	Second byte of Version Number [8:15]	This value must be = 0xAA.
0x0002	0:7	First byte of a 16-bit value that defines the total number of configuration blocks to read [0:7]	-
0x0003	0:7	Second byte of a 16-bit value that defines the total number of configuration blocks to read [8:15]	For n configuration blocks, the value entered here is n-1
0x0004	0:7	The lower 8 bits of a 10-bit value that defines the number of words in configuration Block 1.	Represents bits [0:7] of the 10-bit block count. For m words, the value entered here is m-1.
0x0005	0:1	Bits 8:9 of the 10-bit block count	-
0x0005	2:7	Bits 0:5 of the block address	-
0x0006	0:7	Bits 6:13 of the block address	-
0x0007	0:7	Bits 14:21 of the block address	Register addresses are always 4-byte aligned, therefore bits 22:23 are zero.
0x0008:0x000B	All	Bits 0:31 of the data to load into EEPROM address, 0x0005 to 0x0007	-
0x000C:0x000F	All	Bits 0:31 of the data to load into the above address + 1	-

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Table 67: EEPROM Register Address Map *(Continued)*

EEPROM Address (Byte-Level Addresses)	Bits	EEPROM Contents	Comments
...	...	Remainder of block 1	-
n	0:7	The lower 8 bits of a 10-bit value that defines the number of words in configuration Block 2.	Represents bits [0:7] of the 10-bit block count. For m words, the value entered here is m-1.
n + 1	7:6	Bits 8:9 of the 10-bit block count	-
n + 1	2:7	Bits 0:5 of the block address	-
n + 2	0:7	Bits 6:13 of the block address	-
n + 3	0:7	Bits 14:21 of the block address	Bits 22:23 are zero
n + 4:n + 7	All	Bits 0:31 of the data to load into the above address, (n + 1) to (n + 3)	-
n + 8:n + 11	All	Bits 0:31 of the data to load into address + 1 above	-
...	...	Remainder of block 2	-
...	...	Remainder of blocks M	-
z	0:7	Bits 0:7 of CRC	-
z + 1	0:7	Bits 8:15 of CRC	-

7.3.5 CRC Calculation

The EEPROM's contents are protected by a 16-bit CRC at the end of the loaded image. The CRC does not prevent incorrect data from loading; however, the CPS-1848 will set the CHKSUM_FAIL status bit in the I2C Master Control Register to indicate that the CRC failed.

The CRC is calculated using a standard CRC-16 polynomial x16 + x15 + x2 + 1 with an initial value of zero. The algorithm used by the CPS-1848 to calculate the CRC differs from standard CRC algorithms in that the standard CRC algorithm normally pads the data by the width of the CRC as a final 16 bits of data to shift through the algorithm. The CPS-1848 does not do that, therefore, the standard CRC-16 algorithm will not generate a correct CRC. The following algorithm will generate the CRC-16 expected at the end of the EEPROM.

```
unsigned short icrc16(unsigned char* data, int numBytes) {
  unsigned short remainder = 0;
  unsigned char  crc[16];
  unsigned char  byte;
  unsigned char  bit_Pos;
  unsigned char  bit_Pos_Mask;
  unsigned char  carry;
  unsigned char  serial_data;
  unsigned int   word;
  int data_byte_size;
  int i, b;
```


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```
    remainder = 0;
    memset(crc, 0, sizeof(crc));

    for (b=0; b < numBytes; b++) {
      byte = data[b];

      bit_Pos_Mask = 0x80;

    for (bit_Pos = 0; bit_Pos < 8; bit_Pos++) {
        carry = crc[15];
        if (bit_Pos_Mask & byte)
           serial_data = 1;
        else
           serial_data = 0;
        for (i=15; i>=0; i--) {
          if (i == 15) {
            crc[i] = carry ^ crc[i-1];
          } else if (i == 2) {
            crc[i] = carry ^ crc[i-1];
          } else if (i == 0) {
            crc[i] = carry ^ serial_data;
          } else {
            crc[i] = crc[i-1];
          }
        }
        bit_Pos_Mask >>= 1;
      }
    }

    for (i=15; i>=0; i--) {
      remainder |= (crc[i] << i);
    }

    return (remainder);
  }
```


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7.3.6 Register Map Example

The following is a sample list of registers to be configured through an I2C EEPROM, and the I2C values required to set those registers.

Table 68: Register Map Example

Register	Value	Comment
0x00015C	0x00600000	Block 1
0xE00000	0x01	Block 2
0xE00004	0x02	-
0xE00008	0x03	-
0xE0000C	0x04	-
0xE00010	0x05	-
0xE00014	0x06	-
0xE00018	0x07	-
0xE0001C	0x08	-
0x6c	0x14	Block 3

7.3.7 EEPROM Format Example

Table 69: EEPROM Format Example

EEPROM Address	Data	Comment
0x0000	0xAA	Version Number
0x0001	0xAA	-
0x0002	0x00	-
0x0003	0x02	Number of Blocks = 3
0x0004	0x00	Start of Block 1 - Register count = 1
0x0005	0x00	-
0x0006	0x00	-
0x0007	0x57	Address = 0x15C >> 2 = 0x57
0x0008	0x00	Data for block 1 = 0x00600000
0x0009	0x60	-
0x000A	0x00	-
0x000B	0x00	-

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Table 69: EEPROM Format Example *(Continued)*

EEPROM Address	Data	Comment
0x000C	0x08	Start of Block 2 - Register count = 9
0x000D	0x38	Address = 0xE00000 >> 2 = 0x380000
0x000E	0x00	-
0x000F	0x00	-
0x0010	0x01	Data for address 0xE00000
0x0011	0x02	Data for address 0xE00004
0x0012	0x03	Data for address 0xE00008
0x0013	0x04	Data for address 0xE00010
0x0014	0x05	Data for address 0xE00014
0x0015	0x06	Data for address 0xE00018
0x0016	0x07	Data for address 0xE0001C
0x0017	0x08	Data for address 0xE00020
0x0018	0x09	Data for address 0xE00024
0x0019	0x00	Start of Block 3 - Register count = 1
0x001A	0x00	Address = 0x6c >> 2 = 0x1B
0x001B	0x00	-
0x001C	0x1B	-
0x001D	0x00	Data for address 0x6c = 0x00000014
0x001E	0x00	-
0x001F	0x00	-
0x0020	0x14	-
0x0021	0xD7	CRC = 0xD746
0x0022	0x46	-

7.3.8 I²C Master Mode Validation Debug

I²C Master operation is controlled by configuration pins and device registers. For more information on I²C Master configuration pins, see the *CPS-1848 Datasheet*.

The CPS-1848 detects when an I²C EEPROM image has an invalid CRC and sets the CHKSUM_FAIL bit of the I2C Master Status and Control Register. This bit can be verified by initialization software to confirm that the EEPROM load was successful. In the event of failure, software can be notified automatically through an interrupt or port-write. For information on enabling interrupt and port-write notification, see I2C Event Notification.

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7.4 Slave Mode

When the CPS-1848 is configured as a slave, its physical device address is defined by 10 external pins, ID[9:0]. The device can operate as either a 10-bit or 7-bit addressable device, as defined by an additional external pin called ADS. If the ADS pin is tied to V_{DD3} (3.3V), then the device operates as a 10-bit addressable device using ID[9:0]. If the ADS pin is tied to GND, then the device operates as a 7-bit addressable device as defined by ID[6:0].

Table 70: I^2C Address Pins

Pin	Name
ID [9]	I2C address bit 9 (10-bit mode only)
ID [8]	I2C address bit 8 (10-bit mode only)
ID [7]	I2C address bit 7 (10-bit mode only)
ID [6]	I2C address bit 6
ID [5]	I2C address bit 5
ID [4]	I2C address bit 4
ID [3]	I2C address bit 3
ID [2]	I2C address bit 2
ID [1]	I2C address bit 1
ID [0]	I2C address bit 0

7.4.1 Signaling in Slave Mode

Communication with the CPS-1848 in Slave mode on the I^2C bus supports the following cases:

1. Master device to CPS-1848:
   a. Master device addresses the CPS-1848 as a slave
   b. Master device (master-transmitter), sends data to the CPS-1848 (slave-receiver)
   c. Master device terminates the transfer
2. CPS-1848 to Master device:
   a. Master device addresses the CPS-1848 (slave)
   b. Master device (master-receiver) receives data from the CPS-1848 (slave-transmitter)
   c. Master device terminates the transfer.

Full signaling definition is defined in the *I^2C Specification*. Standard waveforms are displayed in the following figures.

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Figure 27: Bit Transfer on the I^{2}C Bus

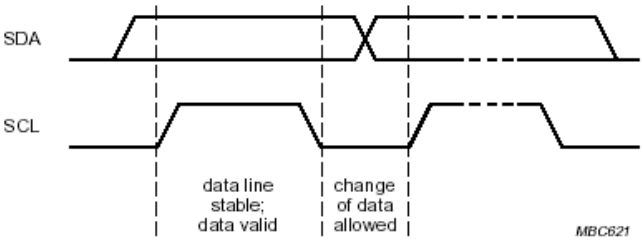

Figure 28: START and STOP Signaling

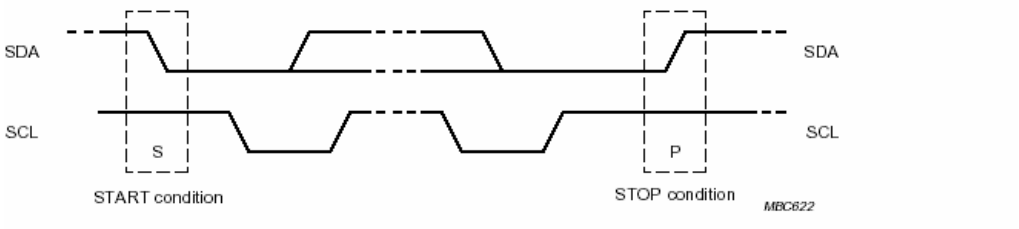

Figure 29: Data Transfer

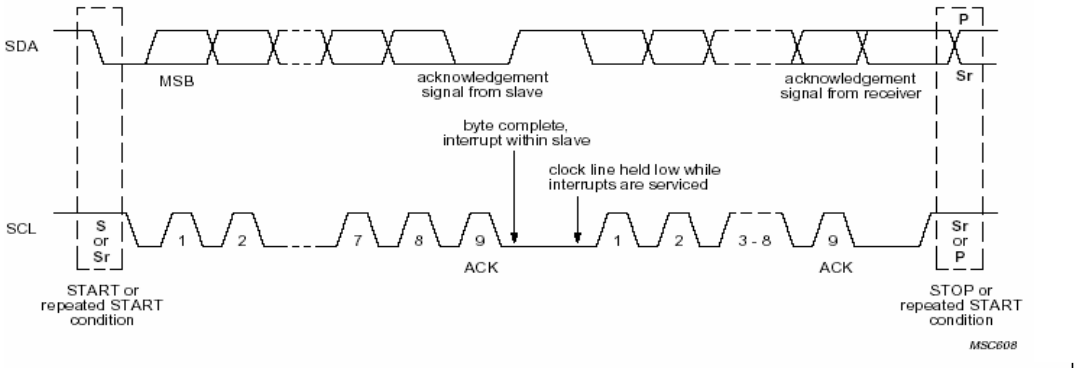

Figure 30: Acknowledgment

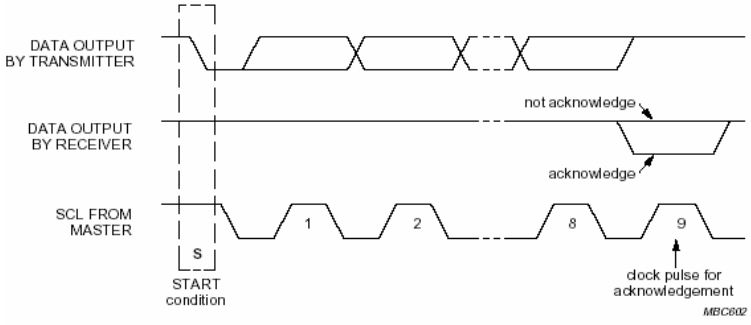

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Figure 31: Master Addressing a Slave with a 7-bit Address (Transfer Direction is Not Changed)

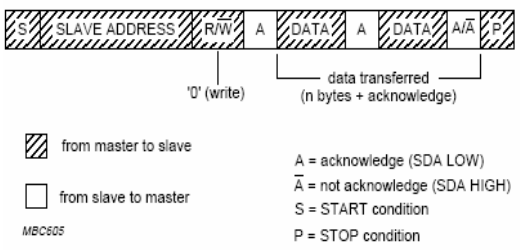

Figure 32: Master Reads a Slave Immediately After the First Byte

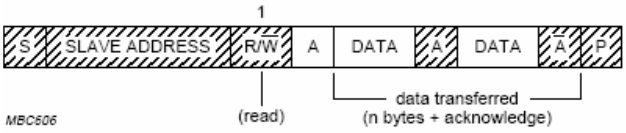

Figure 33: Combined Format

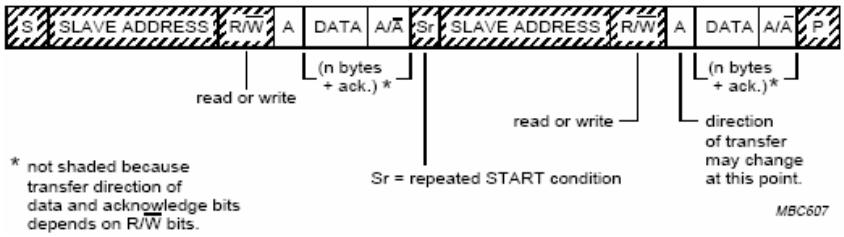

Figure 34: Master Addresses a Slave-Receiver with 10-bit Address



Figure 35: Master Addresses a Slave Transmitter with 10-bit Address

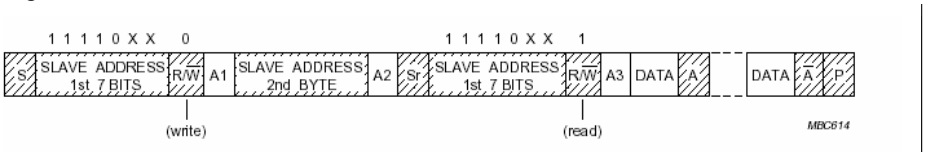

Figure 36: Combined Format – Master Addresses a Slave with 10-bit Address[1]

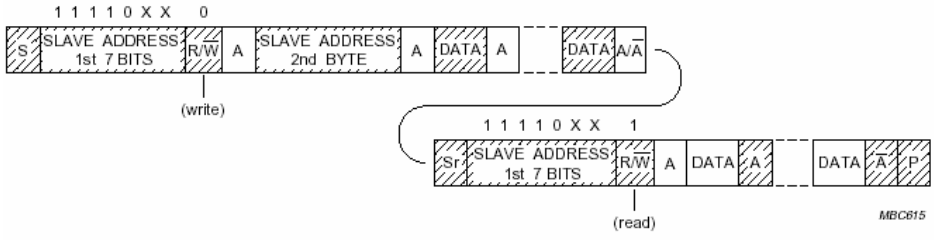

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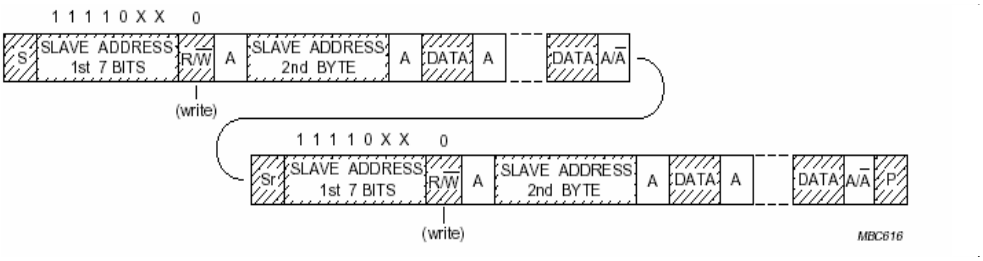
Figure 37: Combined Format – Master Transmits Data to Two Slaves, Both with 10-bit Address



7.4.2 Connecting to Standard-, Fast-, and Hs-Mode Devices as a Slave

The CPS-1848 supports Fast / Standard (F/S) modes of operation. As per the *I²C specification*, in mixed speed communication the CPS-1848 supports HS and Fast-mode devices at 400 kbps, and Standard-mode devices at 100 kbps. The CPS-1848 supports speed negotiation on mixed speed buses as defined in the *I²C Specification*.

7.4.3 CPS-1848 Memory Access through I²C as a Slave

The CPS-1848 supports direct memory access through its I²C Interface as defined in the *I²C Specification*. It requires the memory address to be specified during writes to its registers. This provides directed memory accesses through the I²C bus.

The CPS-1848 write procedure requires 22 bits of memory address to be provided following the device address. Thus, the following are required:

1. A device address (one or two bytes depending on 10-bit/7-bit addressing)
2. A memory address (3 bytes yielding 22-bits of memory address)
3. A 32-bit data payload (4 bytes)

Note that the device address can be configured to any arbitrary value using the external address select pins. A slave address should also be used that is unique to each device on the bus. IDT also recommends to avoid using reserved addresses as specified in the *I²C Specification*, such as CBUS addresses. Providing the I²C access is correct, the CPS-1848 will respond accordingly – even when the slave address is set to specification reserved address ranges.

As a slave, the CPS-1848 read procedure has the memory address section of the transfer removed. To perform a read, the proper access will be to perform a write operation (which provides a 22-bit address) and then to issue a repeated start after the acknowledge bit following the third byte of memory address. The master will issue a read command selecting the CPS-1848 through the standard device address procedure with the R/W bit high. Note that in 10-bit device address mode (ADS is 1), only the two MSBs need be provided during this read. Data from the previously loaded address will immediately follow the device address protocol. It will be possible to issue a stop or repeated start anytime during the write data payload procedure, but it must be before the final acknowledge; that is, canceling the write before the write operation is completed and performed. Also, the CPS-1848 I²C Interface will allow the master to access other devices attached to the I²C bus before returning to select the CPS-1848 for the subsequent read operation from the loaded address. Subsequent reads will begin at the address specified I²C during the last write.

1. Then transmits data to slave and reads data from slave.

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Figure 38: Write Protocol with 10-bit Slave Address (ADS is 1)

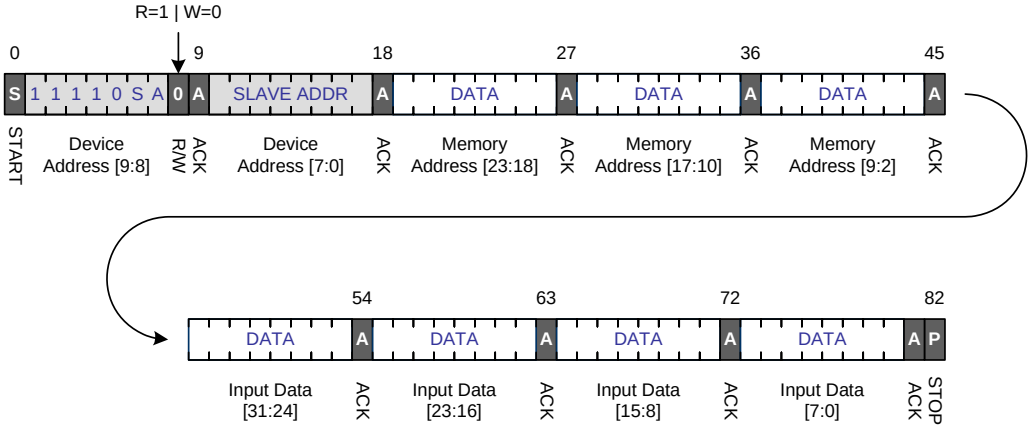

Figure 39: Read Protocol with 10-bit Slave Address (ADS is 1)

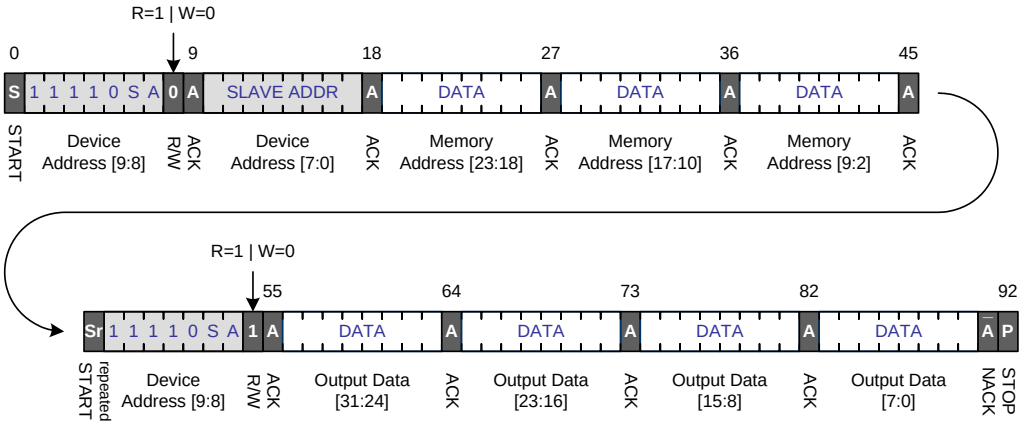

Figure 40: Write Protocol with 7-bit Slave Address (ADS is 0)

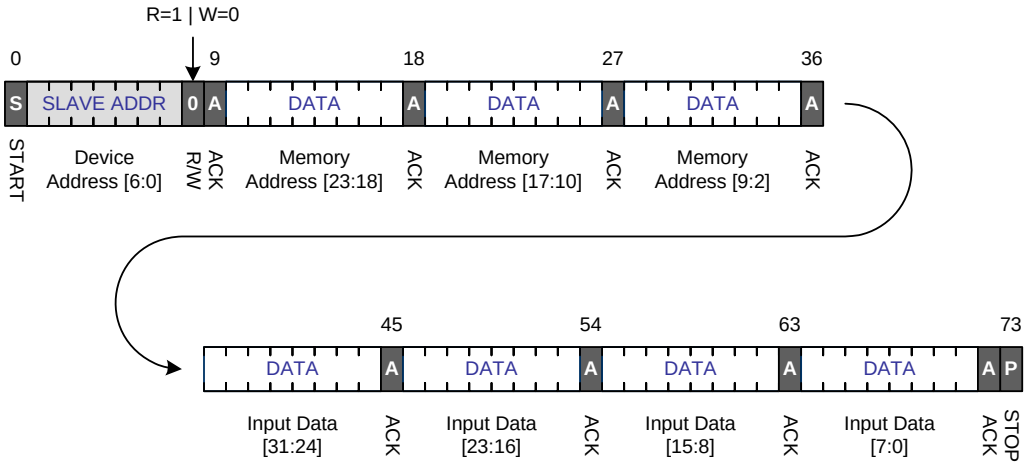

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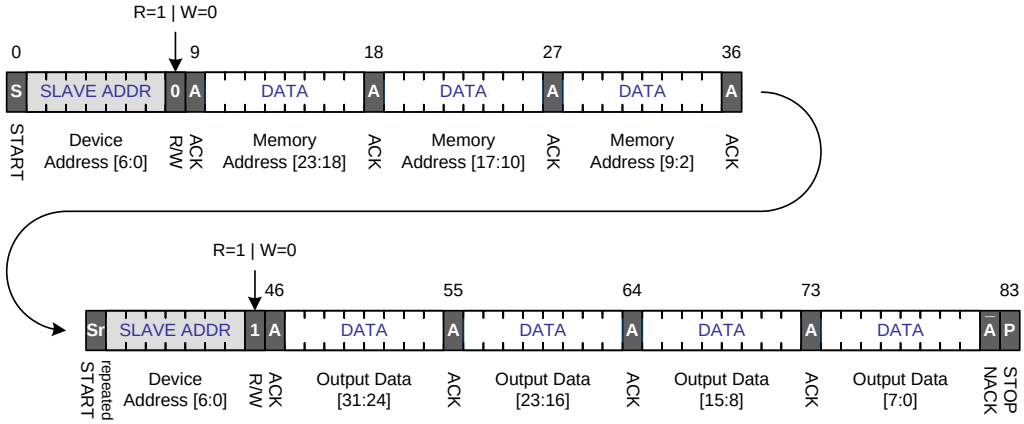
Figure 41: Read Protocol with 7-bit Slave Address (ADS is 0)



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8. JTAG and Boundary Scan

This chapter discusses the functionality of the JTAG TAP port interface and Configuration Register Access (CRA) capability. The chapter consists of two sections that describe Configuration Register Access: one for Revision A/B devices, and the other for Revision C. All other content is applicable to all revisions of the CPS-1848. For the full specifications, see the *CPS-1848 Datasheet*.

Topics discussed include the following:

- Overview
- JTAG and AC Extest Compliance
- Test Instructions
- Device ID Register
- Initialization and Reset
- Configuration Register Access (Revision A/B)
- Configuration Register Access (Revision C)
- JTAG Clock Constraints
- Boundary Scan

8.1 Overview

The CPS-1848 supports all the mandatory instructions defined in the *IEEE 1149.1 Specification*. The TAP Controller allows access to the device's configuration registers. Boundary scan testing of the AC-coupled I/Os are performed in accordance with IEEE 1149.6 (AC Extest).

8.2 JTAG and AC Extest Compliance

All DC pins are compliant with the IEEE 1149.1 specification. All AC-coupled pins fully comply with the IEEE 1149.6 specification. All 1149.1 and 1149.6 boundary scan cells are on the same chain. No additional control cells are provided for independent selection of negative and / or positive terminals of the Tx or Rx pairs.

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8.3 Test Instructions

Table 71: Test Instructions

IR Code [3:0]	Instruction	Comments
0x0	Ex_Test	Implemented per IEEE 1149.1-2001
0x1	Sample/Preload	Implemented per IEEE 1149.1-2001
0x2	ID Code	Implemented per IEEE 1149.1-2001 Device ID = 0x374
0x3	High Z	Implemented per IEEE 1149.1-2001
0x4	Clamp	Implemented per IEEE 1149.1-2001
0x5	Ex_Test Pulse	Implemented per IEEE 1149.6
0x6	Ex_Test Train	Implemented per IEEE 1149.6
0x7	Reserved	-
0x8	Reserved	-
0x9	Reserved	-
0xA	Configuration Register Access	IDT-specific Read and Write Access to Configuration Register space
0xB	Reserved	-
0xC	Reserved	-
0xD	Reserved	-
0xE	Reserved	-
0xF	Bypass	Implemented per IEEE 1149.1-2001

8.4 Device ID Register

The JTAG Device ID register length is 32 bits wide. The Capture Data Register value is the Device ID.

The JTAG Device ID register is mapped to the DEVICE field in the Device Identity CAR. The CPS-1848 provides no correlation between the value in this register and the device's I^2C address. There is no provision to read the I^2C address from the TAP port.

The 11-bit JTAG Vendor ID is 0xB3 where the MSB is 1 (the code itself uses an ODD parity bit in the 8th bit). As per the *IEEE 1149.1 Specification*, the first 7 bits of the Vendor ID will be the first 7 bits of the EIA/JEP106 code "discarding the parity bit." Thus, the JTAG IDCODE read from the TAP port is 0x33.

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8.5 Initialization and Reset

At power-up, the TRST_N signal must be asserted LOW to bring the TAP Controller up in a known, reset state. As per the *IEEE 1149.1 Specification*, the user can alternatively hold the TMS pin high while clocking TCK five times (minimum) to reset the controller. To deactivate JTAG, tie TRST_N low so that the TAP Controller remains in a known state at all times. All of the other JTAG input pins are internally biased such that by leaving them unconnected they are automatically disabled. Note that JTAG inputs are OK to float because they have leakers (as required by the *IEEE 1149.1 Specification*).

8.6 Configuration Register Access (Revision A/B)



The system reset sequence for the CPS-1848 must be completed before a JTAG Configuration Register Access operation is started.

In addition to the S-RIO and I^2C ports, the TAP port provides another interface to access any of the CPS-1848's configuration registers. Through the use of the "Configuration Register Access" opcode, writes and reads to any register are possible. The same JTAG instruction is used for both writes and reads of the Configuration Register space. Bit zero of the TDI data stream defines whether or not the command is a write or a read.

Table 72: Configuration Registers

Bits	Field Name	Size	Description
[0]	jtag_config_wr_n	1	0 = Write configuration register 1 = Read configuration register
[22:1]	jtag_config_addr	22	Starting address of the memory-mapped configuration register
[54:23]	jtag_config_data	32	Reads: Data shifted out (one 32-bit word per read) is read from the configuration register at address jtag_config_addr. Writes: Data shifted in (one 32-bit word per write) is written to the configuration register at address jtag_config_addr.



The CPS-1848's JTAG functionality does not support register access when it is part of a chain of JTAG devices. The CPS-1848 must be the only device on the JTAG bus when its registers are accessed using JTAG. Register access, however, can still be performed from the RapidIO or I2C interfaces.

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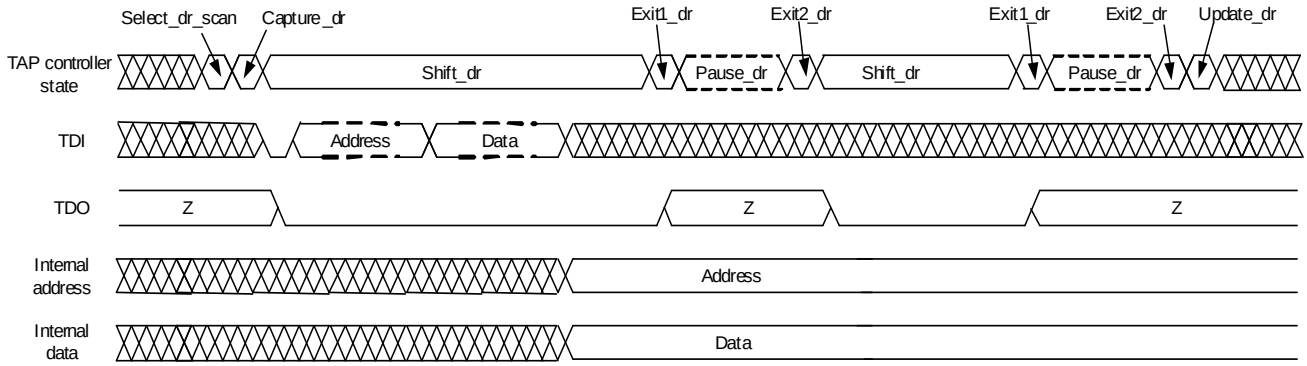
8.6.1 Configuration Register Access – Writes

When bit 0 of the data stream is 0, data shifted in after the address is written to the address specified in jtag_config_addr. The TDO pin will transmit all 0s. Write timing is displayed in the following figure.

Figure 42: JTAG Write Access Timing Diagram

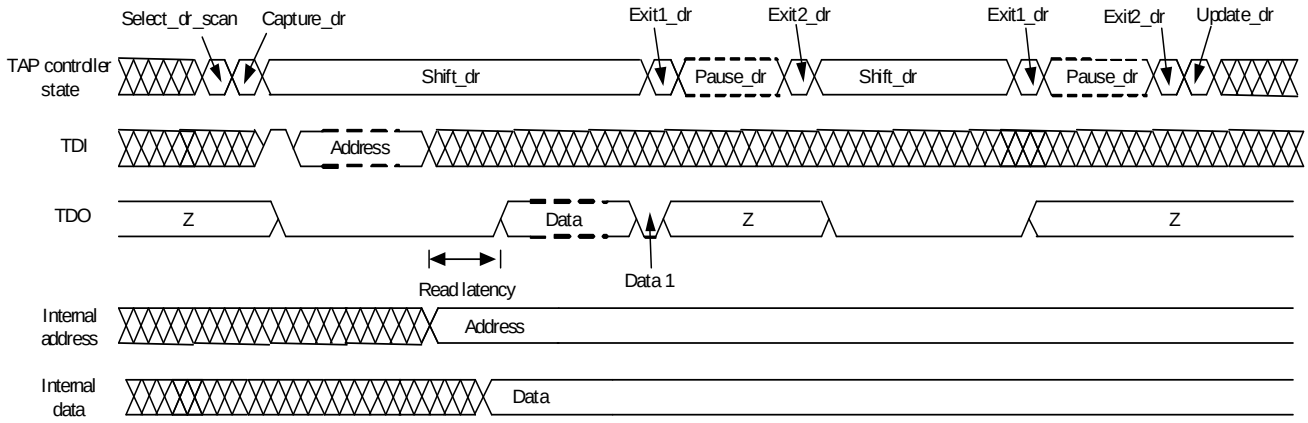


The CPS-1848 can report an unexpected termination of a register write using JTAG, and that JTAG sourced write data is not on a 32-bit boundary – this applies to writes to configuration registers. The error code for this report is defined in JTAG Error Encoding (Revision A/B Only).

8.6.2 Configuration Register Access – Reads

When bit 0 of the data stream is 1, data shifted out is read from the address specified in jtag_config_addr. The TDI pin is not used after the address is shifted in. Read timing is displayed in the following figure.

Figure 43: JTAG Read Access Timing Diagram



The read latency value is 16 JTAG clock cycles. This value applies to both full rate and half rate core clock rates.

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8.7 Configuration Register Access (Revision C)

The system reset sequence for the CPS-1848 must be completed before a JTAG Configuration Register Access operation is started.

In addition to the S-RIO and I^2C ports, the TAP Controller provides another interface to access any of the CPS-1848's configuration registers. Through the use of the "Configuration Register Access" opcode, writes and reads can be made to any register. The same JTAG command and status instruction is used for both writes and reads of the Configuration Register space (see Table 73).

Table 73: JTAG Configuration Register Access Command and Status Instruction

Bits	Field Name	Size	Description
0	READY	1	This is part of the status of the previous JTAG register access command. The READY bit for the previous command is shifted out on TDO as the next command is shifted in. 0b0 = Previous command did not have time to finish 0b1 = Previous command did have time to finish The agent that applies JTAG register access commands is required to wait a minimum period of time after issuing a command to allow that command to finish (see Table 74). If this minimum delay requirement is violated and command B is applied too soon after command A, command A may not have enough time to finish when its status is shifted out. In this case, the READY bit that is shifted out for command A would be 0 and command B would be ignored by the CPS-1848. The value shifted into the READY bit is ignored by the CPS-1848.
1	ERROR	1	This is part of the status of the previous JTAG register access command. The ERROR bit for the previous command is shifted out on TDO as the next command is shifted in. 0b0 = Previous command finished without an error 0b1 = Previous command finished with an error An error indication on this bit signals that an error occurred on the internal configuration access register infrastructure within the CPS-1848. The nature of the error is not accessible through this interface. Possible error causes include: invalid address, parity error, and timeout. The value shifted into the ERROR bit is ignored by the CPS-1848.
33:2	DATA	32	This is the write data for the current command that is shifted in on TDI. The data for the previous instruction is shifted out on TDO. Note: The data shifted in is not meaningful for Read or NOP commands because these commands do not require input data. If the previous command was a Read, the data shifted out is the read data for that Read. If the previous command was a Write, the data shifted out is the write data for that Write. If the previous command was a NOP, the data shifted out is meaningless.

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Table 73: JTAG Configuration Register Access Command and Status Instruction *(Continued)*

Bits	Field Name	Size	Description
35:34	CMD	2	0b0x = NOP command. NOP commands allow shifting out of the results of the previous command without starting a new command. 0b10 = Read 0b11 = Write
57:36	ADDR	22	This is the most significant 22 bits of the 24-bit register address offset. S-RIO configuration registers are 4-byte aligned and therefore the lower 2 bits of the offset are always 0.

A 58-bit instruction is shifted in through TDI with bit 0 being applied first and bit 57 applied last. As the new instruction is shifted in through TDI, the previous instruction and its status are shifted out through TDO with bit 0 emerging first and bit 57 emerging last.

8.7.1 Inter-Command Delay

In order to do a JTAG register access operation, the TAP Controller must first be loaded with the Configuration Register Access instruction by shifting 0xA into the Instruction Register (see Table 71).

Once the TAP Controller is in the Configuration Register Access state, commands can be shifted in, and their results shifted out, as shown in Figure 44. This figure shows the standard JTAG state machine that is implemented in the CPS-1848's TAP Controller. Each inter-state arc is annotated with the TMS input value needed to traverse that arc.

The CPS-1848 JTAG register access mechanism allows only one command to be in progress at a time (see Figure 44). For example, JTAG register access command B cannot be started until JTAG register access command A has completed. To allow sufficient time for command A to finish before starting command B, the agent that applies JTAG register access commands must hold the TAP Controller in the JTAG Run-Test/Idle state for a minimum amount of time between register access commands.

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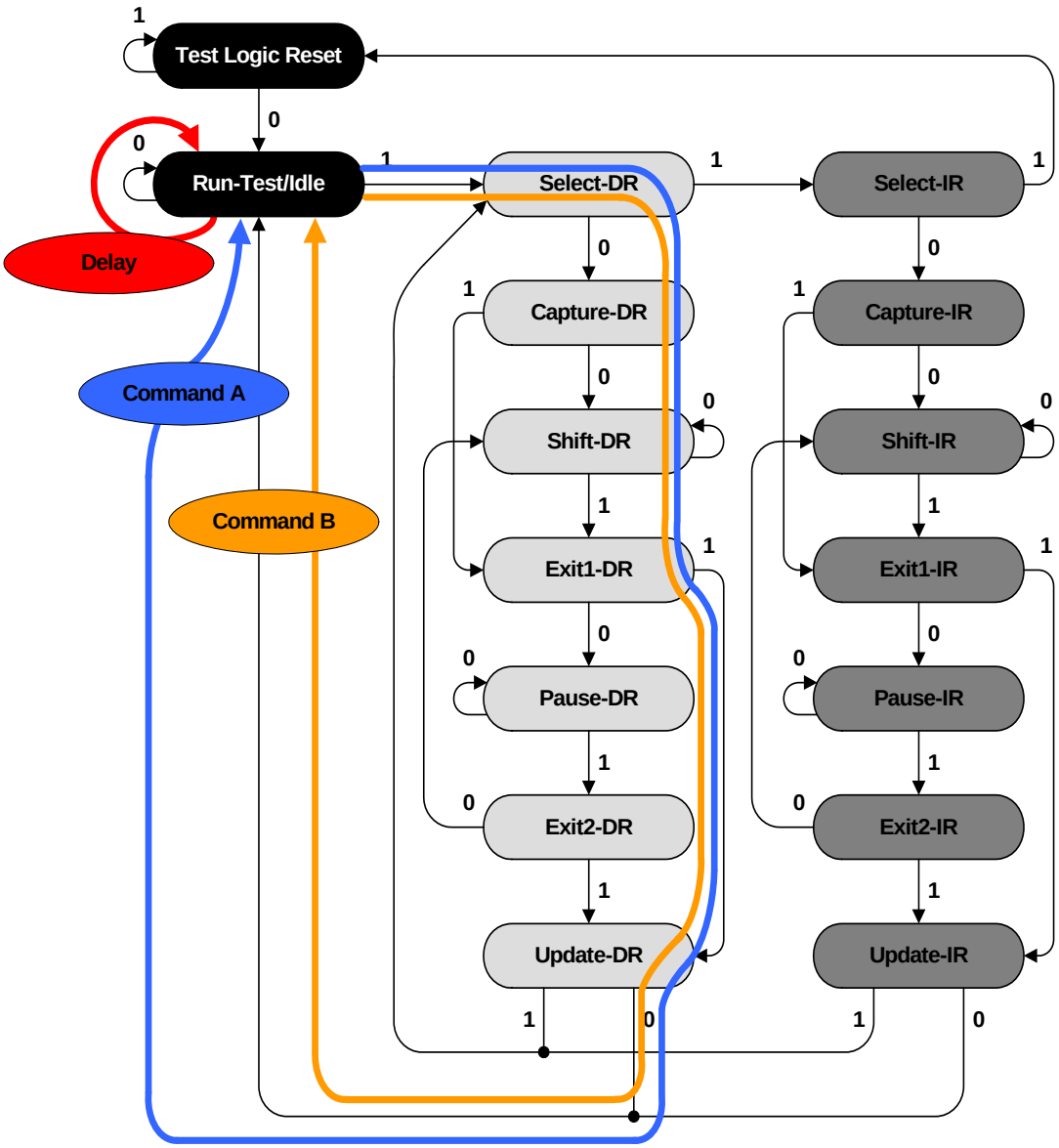
Figure 44: Inter-Command Delay



Superimposed on the state machine are the sequence of states required for register access command A, the inter-command delay, and register access command B. The blue line shows the sequence of states needed to apply command A. The orange line shows the sequence of states needed to apply command B. The red line shows the inter-command delay that must be applied after Command A before command B can be started.

Table 74 summarizes the minimum inter-command delay requirement.

Table 74: Minimum Inter-Command Delay

Core Clock Rate (MHz)	Minimum Inter-command Delay in Run-Test/Idle (Microseconds)
312.5	1
156.25	2

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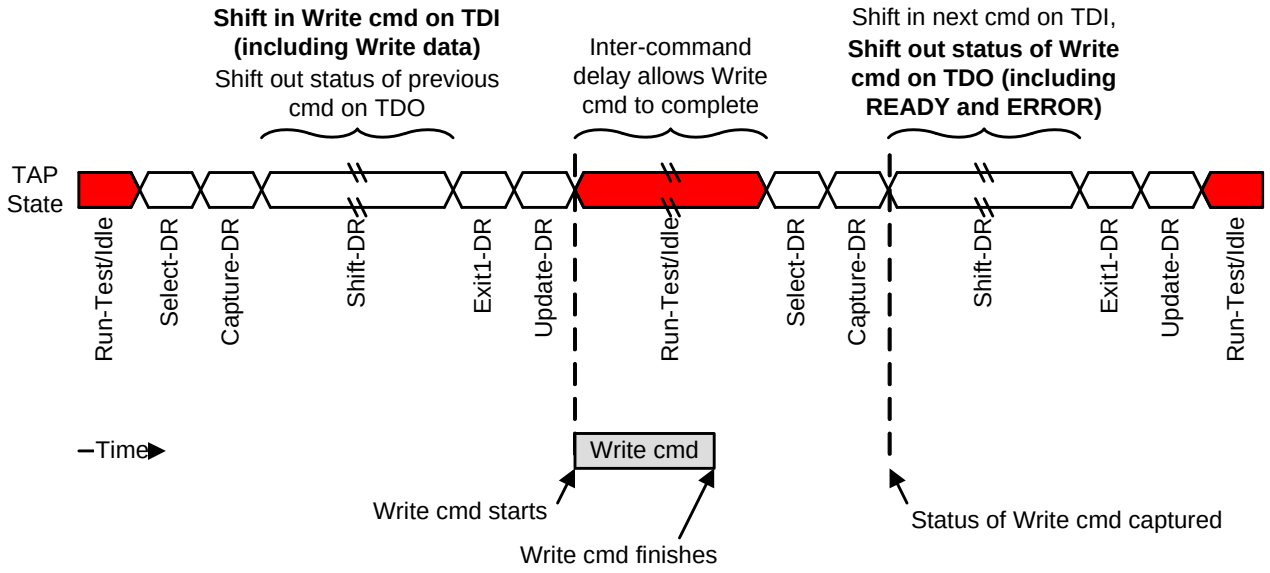
8.7.2 Configuration Register Access – Writes

The timing of a typical JTAG register access Write command is shown in Figure 45. Note that the status of the Write command is obtained while shifting in the next command. If the Write is the last functional command, a NOP command can be shifted in while the Write status is shifted out.

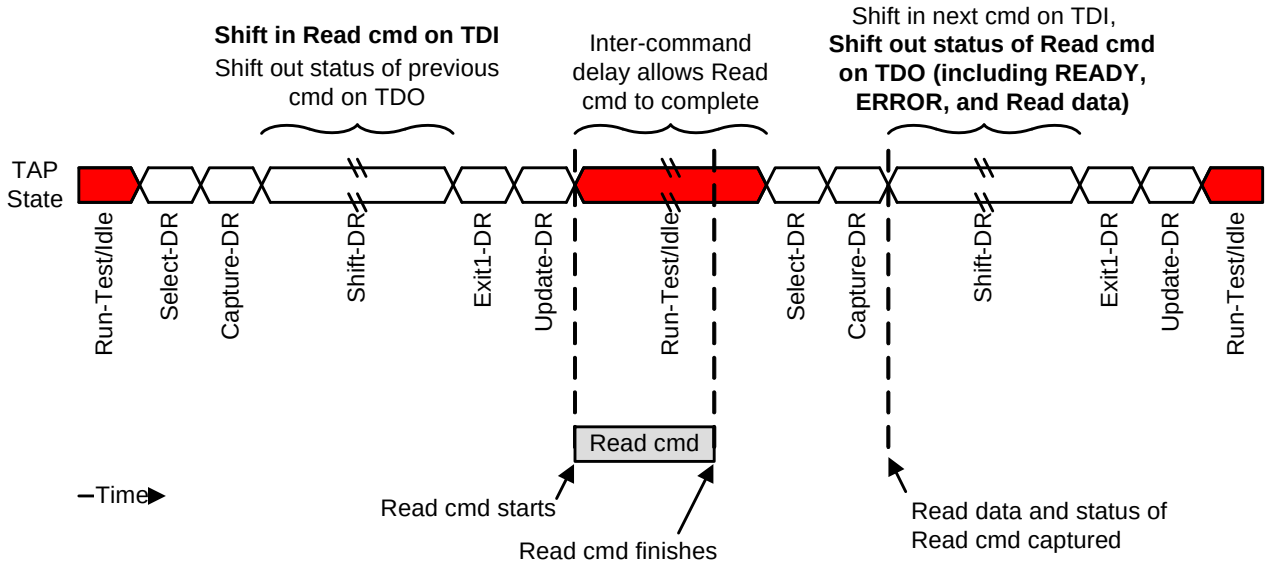
Figure 45: JTAG Register Access – Write Timing Diagram



8.7.3 Configuration Register Access – Reads

The timing of a typical JTAG register access Read command is shown in Figure 46. Note that the status of the Read command, including the read data, is obtained while shifting in the next command. If the Read is the last functional command, a NOP command can be shifted in while the Read status and data are shifted out.

Figure 46: JTAG Register Access – Read Timing Diagram



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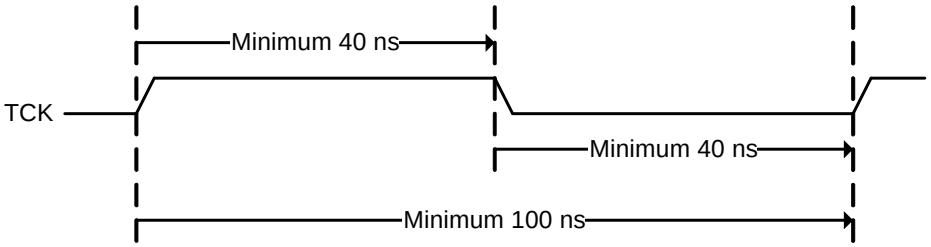
8.8 JTAG Clock Constraints

The JTAG clock (TCK) must have a minimum period of 100 ns, and the minimum edge-to-edge spacing must be 40 ns (see Figure 47).

Figure 47: JTAG Clock Constraints



8.9 Boundary Scan

JTAG instructions are provided to make all the device inputs observable and all the outputs controllable.

All external I/Os support Boundary Scan testing as defined in IEEE 1149.1 and 1149.6. All input / output possibilities are tested including support for leakage testing, and providing users easy debugging by isolating the CPS-1848 from other devices on a PCB board.

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9. Reset and Initialization

This chapter discusses the reset and initialization options of the CPS-1848. Topics discussed include the following:

- Hardware Reset
- Initialization

9.1 Hardware Reset

Before the CPS-1848 can be initialized, it must be reset.

9.1.1 Power-Up Reset

When power is applied to the CPS-1848, it is expected that the RST_N and TRST_N signals are asserted. This ensures that the RapidIO functionality, and the test port functionality, of the CPS-1848 have a deterministic state after reset.

There are requirements for reference clock stability and power sequencing that apply only to a power-up reset. Once a power-up reset has completed, the reference clock and power supply are expected to remain stable during subsequent resets.

Power-up resets configure the device according to the settings of the configuration pins. For more information about power-up reset electrical requirements, see the *CPS-1848 Datasheet.*



The configuration pin settings should choose lane and port configuration values that allow the system host to connect to the CPS-1848. This enables rapid initialization of the CPS-1848 over RapidIO after a reset has completed.

9.1.2 Resets after Power-Up

There are four methods to reset the CPS-1848:

1. Driving the RST_N pin
2. Writing to the Device Soft Reset Register
3. Receiving an S-RIO reset request when Device Control 1 Register.PORT_RST_CTL is 0
4. Writing 1 to the RESET_TYPE and DO_RESET fields in the Device Reset and Control Register

The first three methods for resetting the CPS-1848 are equivalent to a power-up reset, whereby the following occurs:

- All PLLs are reset
- All internal registers revert to their default values
- The device configuration is determined by the configuration pins.

The fourth method has slightly different behavior as follows:

- Only PLLs selected in the PLL_SEL field in the Device Reset and Control Register will be reset
- All internal registers retain their current values
- All ports and lanes are reset

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Software can cause a reset by writing to the Device Soft Reset Register through the I2C port, the JTAG port, or the default S-RIO port by a host processor. Any S-RIO link partner can also reset the CPS-1848 by sending a RapidIO reset request. For more information about RapidIO reset requests, see Reset Control Symbol Processing.



The CPS-1848 link initialization sequence begins immediately upon the release of a hardware reset.

9.2 Initialization

Once the CPS-1848 completes a reset, the device has a deterministic state. The initialization of the device proceeds from this state in three steps:

1. I2C initialization
2. Link initialization
3. Register initialization

These three initialization steps are discussed in the following sections.

9.2.1 I2C Initialization

The I2C Interface can load register values from an EEPROM to change CPS-1848 configuration before it can be initialized from RapidIO. IDT recommends that the following register values are loaded from an EEPROM to provide information to the system host when enumerating a system with a dynamic configuration:

- RapidIO Assembly Identification CAR Override
- RapidIO Assembly Information CAR Override
- Port {0..17} Control 1 CSR, ENUM_B and PORT_LOCKOUT bit fields, if necessary

  If PORT_LOCKOUT is set, packets will not be accepted by that port. This ensures that the CPS-1848's initialization is completed before packets are transferred.

For more information on loading register values from an EEPROM, see I2C Interface.

9.2.2 Link Initialization

When RST_N is released, the RapidIO lanes and ports follow the initialization procedure discussed in Port and Lane Initialization Sequence. EEPROM boot loading also begins at RST_N release and runs concurrently with link initialization. During link initialization and while EEPROM boot loading is occurring, only JTAG access is possible. As EEPROM and link initialization complete, those interfaces permit access to the device.

If register changes that affect the lane or port configuration are loaded during the EEPROM boot load (see Lane to Port Mapping and Lane and Port Speeds), the link initialization process will be terminated and re-started from a silent state. Depending on the state of link partner initialization, this may cause the link partner to enter the input-error stopped state.

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9.2.3 Register Initialization

To initialize the CPS-1848's registers, complete the following steps in the order indicated:



Steps 1a, 4d, and 5 are not required if register initialization is taking place through an EEPROM.

1. Disable a port using one of the following steps:
   a. Disable a port before it is reconfigured by register changes (see Port {0..17} Control 1 CSR.PORT_DIS).
   b. Disable a port if a link partner is not expected to be present on the link (see Port {0..17} Control 1 CSR.PORT_DIS). A port should be placed in port-lockout if a new link partner may appear on the link (see Port {0..17} Control 1 CSR.PORT_LOCKOUT).
2. Change the lane to port mapping if the required mapping is different from the configuration pin settings (see Lane to Port Mapping).
3. Change the lane to port speed setting if the required setting is different from the configuration pin settings (see Lane and Port Speeds).
   a. Change the speed per-lane using Lane {0..47} Control Register[TX_RATE and RX_RATE].
   b. Change the PLL speed using the PLL {0..11} Control 1 Register.
   c. Reset the PLLs using the Device Reset and Control Register.
4. Configuration (no ordering is required for the following steps).
   a. Program the route table as described in Programming Examples.
   b. (Revision A/B only) Change Port {0..17} Lane Synchronization Register[VMIN] to 0b001 for 5 Gbaud or higher.
   c. Change Port Link Timeout Control CSR[TIMEOUT] to a recommended value of 20–50 us (see Computing Timeout Values).
   d. Enable all counters and error management as displayed in the following table (this is an optional step).

Read/Write	Offset	Value	Purpose
The following writes will configure CPS-1848's counters and error management for all ports.			
Write	0xF4FF04 Broadcast Port Operations Register	0x0640_0070	• Sets CNTRS_EN = 0b1 and SILENCE_CTL = 0b101 • Enables PORT_LOG_EN, LANE_LOG_EN, and LT_LOG_EN logging
Write	0x03FF04 Broadcast Port Error Report Enable Register	0x807E_8037	Enables reporting of various error types for all ports
Write	0xFD0008 Error Log Match Register {0..7}	0x0078_0000	Records and counts all errors, flag
The following reads are of the CPS-1848's error logs.			
Read	0xFD002C Error Log Events Register	XXXX_XXXX	Identifies the number of errors that occurred
Read	0xFD0004 Error Log Data Register	XXXX_XXXX	Identifies the error source, group, and number. To determine which error occurred, see Error Log Event Source Encoding.

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e. Program other configuration settings such as cut-thru mode (CUT_THRU_EN), and per-port reset behavior (PORT_RST_CTL) using the Device Control 1 Register.

5. If the port has a link partner, enable the port by clearing Port {0..17} Control 1 CSR.PORT_DIS and PORT_LOCKOUT.
6. Disable IDLE2 functions as described in Disabling IDLE2 Operation.
7. Reset the port(s) using the Device Reset and Control Register (see Per-Port Reset).

   The CPS-1848's ports will revert back to their default values after a port reset.
8. Configure the port width using Port {0..17} Control 1 CSR[PWIDTH_OVRD] if the required setting is different from the intended configuration.
9. Enable the ports to receive and transmit packets by setting Port {0..17} Control 1 CSR[INPUT_PORT_EN and OUTPUT_PORT_EN] to 1.

9.2.4 Computing Timeout Values

This section discusses two timeout periods:

- Port Link Timeout Control CSR – The default value for TIMEOUT must be changed because it is unsuitable for most systems.
- Packet Time to Live CSR – The switch TTL function is disabled by default. If the TTL function is required for correct system operation, the field's default value must be changed.

9.2.4.1 Setting the Port Link Timeout Control CSR

Each RapidIO device has a standard register that defines the response timeout for the physical level protocol, such as receipt of a link response control symbol after sending a link request. In the CPS-1848, this standard register is known as the Port Link Timeout Control CSR, and must be set correctly to ensure low latency packet transfer during error conditions.

In compliance to the *RapidIO Specification (Rev. 2.1)*, the Port Link Timeout Control CSR has a default timeout period of 5.9 seconds. This timeout period, however, is too long for most applications.

Since there is one counter per device, the timeout value set must be for worst-case latency for all link partners connected to the CPS-1848. The latency for response control symbols varies with the implementation of the link partner and the link speed. The formula for setting TIMEOUT in the Port Link Timeout Control CSR is as follows:

ROUNDUP (MAX (LPLatency [0:n-1]) / 352)

Where:

- There are "n" link partners
- LPLatency is the maximum latency, in nanoseconds, for the link partner to do the following:
  - Return a Packet Accepted, Packet Not Accepted, or Retry control symbol in response to a packet
  - Return a Link Request control symbol in response to a Packet Not Accepted or Stomp control symbol
  - Return a Link Response control symbol in response to a request:
- MAX returns the largest of a list of values
- ROUNDUP computes the smallest integer that is larger than the parameter value

Typically, the TIMEOUT value should be less than 10 microseconds. However, some link partner implementations, particularly FPGA implementations, can increase the TIMEOUT value beyond 10 microseconds.

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9.2.4.2 Setting the Packet Time to Live CSR

The TTL field in the Packet Time to Live CSR determines the maximum amount of time that a packet can exist in the CPS-1848's Final Buffer. It ensures both the request and response packets associated with a transaction that has timed out no longer exist in the system. Depending on the system traffic patterns, this can be much longer than what is defined in the Port Link Timeout Control CSR.

If the system does not use request packets that require responses during normal operation, the TTL function does not need to be enabled. For example, systems that make exclusive use of NWRITE/SWRITE and data streaming transactions do not require the TTL function.

The TTL period must be set to a value greater than the maximum time that a packet exists in the switch's Final Buffer. If the system has predictable (systolic) flows, then the RapidIO System Modeling Tool (which is available from IDT) can be used to model the traffic flows and determine the maximum latency of all packets through a switch. The RapidIO System Modeling Tool can also be used for randomized traffic flows to predict the maximum latency of packets.

For some systems, setting the TTL function is an exercise in trial and error.

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10. Registers

This chapter discusses the CPS-1848's configuration registers. Topics discussed include the following:

- Overview
- Address Map
- RapidIO Capability Registers (CARs)
- RapidIO Control and Status Registers (CSRs)
- LP-Serial Extended Features Registers with Software Assisted Error Recovery
- Error Management Extensions Block Registers
- Lane Status Registers
- IDT Specific Miscellaneous Registers
- IDT Specific Event Notification Control Registers
- IDT Specific Routing Table Registers
- Trace Comparison Values and Masks Registers
- Global Device Configuration Registers
- Implementation Specific Multicast Mask Registers
- Port Function Registers
- Implementation Specific Error Logging Registers
- Special Error Registers
- PLL Registers
- Lane Control Registers
- Error Management Broadcast Registers

10.1 Overview

The CPS-1848 register file is addressable through I^2C, JTAG, and any RapidIO port, and is built with 22-bit addresses and 32-bit words, as specified by the *RapidIO Specification (Rev. 2.1)*. All unused address space should be considered RESERVED.

10.1.1 RapidIO Compliance

The CPS-1848 is compliant to the *RapidIO Specification (Rev. 2.1)*. The device supports the "Generic: All devices" requirements in the *RapidIO Specification (Rev. 2.1), Part 7: System and Device Interoperability Specification*. This requirement suggests support for a number of RapidIO-specific registers. The CPS-1848 supports each of these registers except for the "Destination Operations CAR". The *RapidIO Specification (Rev. 2.1), Part 1: Input/Output Logical Specification* defines this register as being applicable to switches only.

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10.1.2 Interpretation of Reserved Register Bits

The CPS-1848 uses the S-RIO definition for the management of reserved register bits. This treatment is defined in Table 3-2 of the *RapidIO Specification (Rev. 2.1), Part 3*. Under the "Target Behavior" column, the expected return of the reserved bits of a register read is 0 for all S-RIO defined reserved registers. The CPS-1848 has extended this definition to its "Implementation Defined Space" as well. Although the device initializes with zeros in these bit positions, it does not prevent the user from writing to these bits. When writing registers with reserved fields, IDT recommends writing zeros to those reserved fields.

10.1.3 Backward Compatibility

The *RapidIO Specification (Rev. 2.1)* maintains backward compatibility with the *RapidIO Specification (Rev. 1.3)* where possible. Thus, the S-RIO standard registers are similarly backward compatible. IDT has also made the CPS-1848 backward compatible with previous IDT 1.3-compliant switch devices. IDT-specific functions and associated registers are similarly backward compatible where possible.

10.1.4 Register Type Field Definitions

Type	Description
RW	Read/Write.
RO	Read Only. Must mask for all writes.
WO	Write Only. Reading these fields returns undefined data.
RR	Reset on Read. These registers are cleared to 0 when read.
FR	Fixed Read. These values are constant.
W1R	Write Once Reset.

10.2 Address Map

The CPS-1848's address map is listed in Table 75. For most registers, there is one instance for each port. The address on each register indicates the address for port 0. For all other ports, there is an offset from port 0.

Table 75: Address Map

Base Address	Register (Full Name)	Register (Short Name)
RapidIO Capability Registers (CARs)		
0x000000	Device Identity CAR	DEV_IDENT_CAR
0x000004	Device Information CAR	DEV_INF_CAR
0x000008	Assembly Identity CAR	ASSY_IDENT_CAR
0x00000C	Assembly Information CAR	ASSY_INF_CAR
0x000010	Processing Element Features CAR	PROC_ELEM_FEAT_CAR
0x000014	Switch Port Information CAR	SWITCH_PORT_INF_CAR
0x000018	Source Operations CAR	SRC_OPS_CAR
0x000030	Switch Multicast Support CAR	SWITCH_MCAST_SUP_CAR
0x000034	Switch Route Table Entries Table Limit CAR	SWITCH_RTE_TBL_LIM_CAR

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x000038	Switch Multicast Information CAR	SWITCH_MULT_INF_CAR
RapidIO Control and Status Registers (CSRs)		
0x000068	Host Base deviceID Lock CSR	HOST_BASE_DEVICEID_LOCK_CSR
0x00006C	Component Tag CSR	COMP_TAG_CSR
0x000070	Standard Route Table Entries Configuration destID Select CSR	RTE_DESTID_CSR
0x000074	Standard Route Table Entry Configuration Port Select CSR	RTE_PORT_CSR
0x000078	Standard Route Table Entry Default Port CSR	RTE_DEFAULT_PORT_CSR
0x000080	Multicast Mask Port CSR	MCAST_MASK_PORT_CSR
0x000084	Multicast Association Selection CSR	MCAST_ASSOC_SEL_CSR
0x000088	Multicast Association Operations CSR	MCAST_ASSOC_OP_CSR
LP-Serial Extended Features Registers with Software Assisted Error Recovery		
0x000100	Port Maintenance Block Header Register	PORT_MAINT_BLK_HEAD
0x000120	Port Link Timeout Control CSR	PORT_LINK_TO_CTL_CSR
0x00013C	Port General Control CSR	PORT_GEN_CTL_CSR
Per Port Registers		
0x000140	Port {0..17} Link Maintenance Request CSR	PORT_0_LINK_MAINT_REQ_CSR
0x000144	Port {0..17} Link Maintenance Response CSR	PORT_0_LINK_MAINT_RESP_CSR
0x000148	Port {0..17} Local ackID CSR	PORT_0_LOCAL_ACKID_CSR
0x000154	Port {0..17} Control 2 CSR	PORT_0_CTL_2_CSR
0x000158	Port {0..17} Error and Status CSR	PORT_0_ERR_STAT_CSR
0x00015C	Port {0..17} Control 1 CSR	PORT_0_CTL_1_CSR
0x000160	Port 1 – Starting Address	
0x000180	Port 2 – Starting Address	
0x0001A0	Port 3 – Starting Address	
0x0001C0	Port 4 – Starting Address	
0x0001E0	Port 5 – Starting Address	
0x000200	Port 6 – Starting Address	
0x000220	Port 7 – Starting Address	
0x000240	Port 8 – Starting Address	
0x000260	Port 9 – Starting Address	
0x000280	Port 10 – Starting Address	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x0002A0	Port 11 – Starting Address	
0x0002C0	Port 12 – Starting Address	
0x0002E0	Port 13 – Starting Address	
0x000300	Port 14 – Starting Address	
0x000320	Port 15 – Starting Address	
0x000340	Port 16 – Starting Address	
0x000360	Port 17 – Starting Address	
Virtual Channel Extended Features Block Registers		
0x000600	VC Register Block Header Register	VC_REGISTER_BLK_HEAD
RapidIO Specification (Rev. 2.1), Part 8 Error Management Extension Registers		
0x001000	Error Management Extensions Block Header Register	ERR_MGT_EXTENSION_BLK_HEAD
0x001008	Logical/Transport Layer Error Detect CSR	LT_ERR_DET_CSR
0x00100C	Logical/Transport Layer Error Enable CSR	LT_ERR_EN_CSR
0x001018	Logical/Transport Layer deviceID Capture CSR	LT_DEVICEID_CAPT_CSR
0x00101C	Logical/Transport Layer Control Capture CSR	LT_CTL_CAPT_CSR
0x001028	Port-Write Target deviceID CSR	PW_TARGET_DEVICEID_CSR
0x00102C	Packet Time to Live CSR	PKT_TTL_CSR
Per Port Registers		
0x001040	Port {0..17} Error Detect CSR	PORT_0_ERR_DET_CSR
0x001044	Port {0..17} Error Rate Enable CSR	PORT_0_ERR_RATE_EN_CSR
0x001048	Port {0..17} Attributes Capture CSR	PORT_0_ATTR_CAPT_CSR
0x00104C	Port {0..17} Capture 0 CSR	PORT_0_CAPT_0_CSR
0x001050	Port {0..17} Capture 1 CSR	PORT_0_CAPT_1_CSR
0x001054	Port {0..17} Capture 2 CSR	PORT_0_CAPT_2_CSR
0x001058	Port {0..17} Capture 3 CSR	PORT_0_CAPT_3_CSR
0x001068	Port {0..17} Error Rate CSR	PORT_0_ERR_RATE_CSR
0x00106C	Port {0..17} Error Rate Threshold CSR	PORT_0_ERR_RATE_THRESH_CSR
0x001080	Port 1 – Starting Address	
0x0010C0	Port 2 – Starting Address	
0x001100	Port 3 – Starting Address	
0x001140	Port 4 – Starting Address	
0x001180	Port 5 – Starting Address	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x0011C0	Port 6 – Starting Address	
0x001200	Port 7 – Starting Address	
0x001240	Port 8 – Starting Address	
0x001280	Port 9 – Starting Address	
0x0012C0	Port 10 – Starting Address	
0x001300	Port 11 – Starting Address	
0x001340	Port 12 – Starting Address	
0x001380	Port 13 – Starting Address	
0x0013C0	Port 14 – Starting Address	
0x001400	Port 15 – Starting Address	
0x001440	Port 16 – Starting Address	
0x001480	Port 17 – Starting Address	
LP-Serial Lane Extended Features Registers		
0x002000	Lane Status Block Header Register	LANE_STATUS_BLK_HEAD
0x002010	Lane {0..47} Status 0 CSR	LANE_0_STATUS_0_CSR
0x002014	Lane {0..47} Status 1 CSR	LANE_0_STATUS_1_CSR
0x002018	Lane {0..47} Status 2 CSR	LANE_0_STATUS_2_CSR
0x00201C	Lane {0..47} Status 3 CSR	LANE_0_STATUS_3_CSR
0x002020	Lane {0..47} Status 4 CSR	LANE_0_STATUS_4_CSR
Lanes 1–47	For address offsets, see Lane {0..47} Status Base Addresses.	
IDT Specific Miscellaneous Registers		
0x010070	Route Port Select Register	RTE_PORT_SEL
0x010080	Multicast Route Select Register	MCAST_RTE_SEL
Per Port Registers		
0x011000	Port {0..17} Watermarks Register	PORT_0_WM
0x011010	Port {0..17} Watermarks Register	PORT_1_WM
0x011020	Port {0..17} Watermarks Register	PORT_2_WM
0x011030	Port {0..17} Watermarks Register	PORT_3_WM
0x011040	Port {0..17} Watermarks Register	PORT_4_WM
0x011050	Port {0..17} Watermarks Register	PORT_5_WM
0x011060	Port {0..17} Watermarks Register	PORT_6_WM
0x011070	Port {0..17} Watermarks Register	PORT_7_WM

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x011080	Port {0..17} Watermarks Register	PORT_8_WM
0x011090	Port {0..17} Watermarks Register	PORT_9_WM
0x0110A0	Port {0..17} Watermarks Register	PORT_10_WM
0x0110B0	Port {0..17} Watermarks Register	PORT_11_WM
0x0110C0	Port {0..17} Watermarks Register	PORT_12_WM
0x0110D0	Port {0..17} Watermarks Register	PORT_13_WM
0x0110E0	Port {0..17} Watermarks Register	PORT_14_WM
0x0110F0	Port {0..17} Watermarks Register	PORT_15_WM
0x011100	Port {0..17} Watermarks Register	PORT_16_WM
0x011110	Port {0..17} Watermarks Register	PORT_17_WM
0x01F000	Broadcast Watermarks Register	BCAST_WM
IDT Specific Event Notification Control Registers		
0x020000	Aux Port Error Capture Enable Register	AUX_PORT_ERR_CAPT_EN
0x020004	Aux Port Error Detect Register	AUX_PORT_ERR_DET
0x020008	Configuration Block Error Capture Enable Register	CFG_ERR_CAPT_EN
0x020010	Configuration Block Error Detect Register	CFG_ERR_DET
0x021014	Impl. Specific Logical/Transport Layer Address Capture Register	IMPL_SPEC_LT_ADDR_CAPT
0x03100C	Logical/Transport Layer Error Report Enable Register	LT_ERR_RPT_EN
Per Port Registers		
0x031044	Port {0..17} Error Report Enable Register	PORT_0_ERR_RPT_EN
0x03104C	Port {0..17} Implementation Specific Error Report Enable Register	PORT_0_IMPL_SPEC_ERR_RPT_EN
0x031084	Port 1 – Starting Address	
0x0310C4	Port 2 – Starting Address	
0x031104	Port 3 – Starting Address	
0x031144	Port 4 – Starting Address	
0x031184	Port 5 – Starting Address	
0x0311C4	Port 6 – Starting Address	
0x031204	Port 7 – Starting Address	
0x031244	Port 8 – Starting Address	
0x031284	Port 9 – Starting Address	
0x0312C4	Port 10 – Starting Address	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x031304	Port 11 – Starting Address	
0x031344	Port 12 – Starting Address	
0x031384	Port 13 – Starting Address	
0x0313C4	Port 14 – Starting Address	
0x031404	Port 15 – Starting Address	
0x031444	Port 16 – Starting Address	
0x031484	Port 17 – Starting Address	
0x038010	Lane {0..47} Error Report Enable Register	LANE_0_ERR_RPT_EN
Lanes 1–47	For address offsets, see Lane n Error Report Enable Base Addresses.	
0x03FF04	Broadcast Port Error Report Enable Register	BCAST_PORT_ERR_RPT_EN
0x03FF0C	Broadcast Port Implementation Specific Error Report Enable Register	BCAST_PORT_IMPL_SPEC_ERR_RPT_EN
0x03FF10	Broadcast Lane Error Report Enable Register	BCAST_LANE_ERR_RPT_EN
Packet Generation and Capture Registers		
0x100100	Port {0..17} Packet Generation and Capture Mode Configuration Register	PORT_0_PGC_MODE
0x100104	Port {0..17} Packet Generation and Capture Mode Data Register	PORT_0_PGC_DATA
0x100110	Port 1 – Starting Address	
0x100120	Port 2 – Starting Address	
0x100130	Port 3 – Starting Address	
0x100140	Port 4 – Starting Address	
0x100150	Port 5 – Starting Address	
0x100160	Port 6 – Starting Address	
0x100170	Port 7 – Starting Address	
0x100180	Port 8 – Starting Address	
0x100190	Port 9 – Starting Address	
0x1001A0	Port 10 – Starting Address	
0x1001B0	Port 11 – Starting Address	
0x1001C0	Port 12 – Starting Address	
0x1001D0	Port 13 – Starting Address	
0x1001E0	Port 14 – Starting Address	
0x1001F0	Port 15 – Starting Address	
0x100200	Port 16 – Starting Address	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0x100210	Port 17 – Starting Address	
IDT Specific Routing Table Registers		
0xE00000–E003FC	Broadcast Device Route Table Register {0..255}	BCAST_DEV_RTE_TABLE_{0..255}
0xE00400–E007FC	Broadcast Domain Route Table Register {0..255}	BCAST_DOM_RTE_TABLE_{0..255}
0xE10000–E103FC	Port {0..17} Device Route Table Register {0..255}	PORT_0_DEV_RTE_TABLE_{0..255}
0xE10400–E107FC	Port {0..17} Domain Routing Table Register {0..255}	PORT_0_DOM_RTE_TABLE_{0..255}
Ports 1–17	For address offsets, see Base Addresses for IDT Specific Routing Table Registers	
Trace Comparison Values and Masks		
0xE40000	Port {0..17} Trace 0 Value 0 Register	PORT_0_TRACE_0_VAL_{0..4}
0xE40004	Port {0..17} Trace 0 Value 1 Register	
0xE40008	Port {0..17} Trace 0 Value 2 Register	
0xE4000C	Port {0..17} Trace 0 Value 3 Register	
0xE40010	Port {0..17} Trace 0 Value 4 Register	
0xE40014	Port {0..17} Trace 0 Mask 0 Register	PORT_0_TRACE_0_MASK_{0..4}
0xE40018	Port {0..17} Trace 0 Mask 1 Register	
0xE4001C	Port {0..17} Trace 0 Mask 2 Register	
0xE40020	Port {0..17} Trace 0 Mask 3 Register	
0xE40024	Port {0..17} Trace 0 Mask 4 Register	
0xE40028	Port {0..17} Trace 1 Value 0 Register	PORT_0_TRACE_1_VAL_{0..4}
0xE4002C	Port {0..17} Trace 1 Value 1 Register	
0xE40030	Port {0..17} Trace 1 Value 2 Register	
0xE40034	Port {0..17} Trace 1 Value 3 Register	
0xE40038	Port {0..17} Trace 1 Value 4 Register	
0xE4003C	Port {0..17} Trace 1 Mask 0 Register	PORT_0_TRACE_1_MASK_{0..4}
0xE40040	Port {0..17} Trace 1 Mask 1 Register	
0xE40044	Port {0..17} Trace 1 Mask 2 Register	
0xE40048	Port {0..17} Trace 1 Mask 3 Register	
0xE4004C	Port {0..17} Trace 1 Mask 4 Register	
0xE40050	Port {0..17} Trace 2 Value 0 Register	PORT_0_TRACE_2_VAL_{0..4}
0xE40054	Port {0..17} Trace 2 Value 1 Register	
0xE40058	Port {0..17} Trace 2 Value 2 Register	
0xE4005C	Port {0..17} Trace 2 Value 3 Register	
0xE40060	Port {0..17} Trace 2 Value 4 Register	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xE40064	Port {0..17} Trace 2 Mask 0 Register	PORT_0_TRACE_2_MASK_{0..4}
0xE40068	Port {0..17} Trace 2 Mask 1 Register	
0xE4006C	Port {0..17} Trace 2 Mask 2 Register	
0xE40070	Port {0..17} Trace 2 Mask 3 Register	
0xE40074	Port {0..17} Trace 2 Mask 4 Register	
0xE40078	Port {0..17} Trace 3 Value 0 Register	PORT_0_TRACE_3_VAL_{0..4}
0xE4007C	Port {0..17} Trace 3 Value 1 Register	
0xE40080	Port {0..17} Trace 3 Value 2 Register	
0xE40084	Port {0..17} Trace 3 Value 3 Register	
0xE40088	Port {0..17} Trace 3 Value 4 Register	
0xE4008C	Port {0..17} Trace 3 Mask 0 Register	PORT_0_TRACE_3_MASK_{0..4}
0xE40090	Port {0..17} Trace 3 Mask 1 Register	
0xE40094	Port {0..17} Trace 3 Mask 2 Register	
0xE40098	Port {0..17} Trace 3 Mask 3 Register	
0xE4009C	Port {0..17} Trace 3 Mask 4 Register	
0xE40100	Port 1 – Starting Address	
0xE40200	Port 2 – Starting Address	
0xE40300	Port 3 – Starting Address	
0xE40400	Port 4 – Starting Address	
0xE40500	Port 5 – Starting Address	
0xE40600	Port 6 – Starting Address	
0xE40700	Port 7 – Starting Address	
0xE40800	Port 8 – Starting Address	
0xE40900	Port 9 – Starting Address	
0xE40A00	Port 10 – Starting Address	
0xE40B00	Port 11 – Starting Address	
0xE40C00	Port 12 – Starting Address	
0xE40D00	Port 13 – Starting Address	
0xE40E00	Port 14 – Starting Address	
0xE40F00	Port 15 – Starting Address	
0xE41000	Port 16 – Starting Address	
0xE41100	Port 17 – Starting Address	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xE4F000	Broadcast Trace 0 Value 0 Register	BCAST_TRACE_0_VAL_{0..4}
0xE4F004	Broadcast Trace 0 Value 1 Register	
0xE4F008	Broadcast Trace 0 Value 2 Register	
0xE4F00C	Broadcast Trace 0 Value 3 Register	
0xE4F010	Broadcast Trace 0 Value 4 Register	
0xE4F014	Broadcast Trace 0 Mask 0 Register	BCAST_TRACE_0_MASK_{0..4}
0xE4F018	Broadcast Trace 0 Mask 1 Register	
0xE4F01C	Broadcast Trace 0 Mask 2 Register	
0xE4F020	Broadcast Trace 0 Mask 3 Register	
0xE4F024	Broadcast Trace 0 Mask 4 Register	
0xE4F028	Broadcast Trace 1 Value 0 Register	BCAST_TRACE_1_VAL_{0..4}
0xE4F02C	Broadcast Trace 1 Value 1 Register	
0xE4F030	Broadcast Trace 1 Value 2 Register	
0xE4F034	Broadcast Trace 1 Value 3 Register	
0xE4F038	Broadcast Trace 1 Value 4 Register	
0xE4F03C	Broadcast Trace 1 Mask 0 Register	BCAST_TRACE_1_MASK_{0..4}
0xE4F040	Broadcast Trace 1 Mask 1 Register	
0xE4F044	Broadcast Trace 1 Mask 2 Register	
0xE4F048	Broadcast Trace 1 Mask 3 Register	
0xE4F04C	Broadcast Trace 1 Mask 4 Register	
0xE4FF50	Broadcast Trace 2 Value 0 Register	BCAST_TRACE_2_VAL_{0..4}
0xE4F054	Broadcast Trace 2 Value 1 Register	
0xE4F058	Broadcast Trace 2 Value 2 Register	
0xE4F05C	Broadcast Trace 2 Value 3 Register	
0xE4F060	Broadcast Trace 2 Value 4 Register	
0xE4F064	Broadcast Trace 2 Mask 0 Register	BCAST_TRACE_2_MASK_{0..4}
0xE4F068	Broadcast Trace 2 Mask 1 Register	
0xE4F06C	Broadcast Trace 2 Mask 2 Register	
0xE4F070	Broadcast Trace 2 Mask 3 Register	
0xE4F074	Broadcast Trace 2 Mask 4 Register	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xE4F078	Broadcast Trace 3 Value 0 Register	BCAST_TRACE_3_VAL_{0..4}
0xE4F07C	Broadcast Trace 3 Value 1 Register	
0xE4F080	Broadcast Trace 3 Value 2 Register	
0xE4F084	Broadcast Trace 3 Value 3 Register	
0xE4F088	Broadcast Trace 3 Value 4 Register	
0xE4F08C	Broadcast Trace 3 Mask 0 Register	BCAST_TRACE_3_MASK_{0..4}
0xE4F090	Broadcast Trace 3 Mask 1 Register	
0xE4F094	Broadcast Trace 3 Mask 1 Register	
0xE4F098	Broadcast Trace 3 Mask 2 Register	
0xE4F09C	Broadcast Trace 3 Mask 4 Register	
Global Device Configuration Registers		
0xF2000C	Device Control 1 Register	DEVICE_CTL1
0xF20014	Configuration Block Error Report Register	CFG_BLK_ERR_RPT
0xF20018	Aux Port Error Report Enable Register	AUX_PORT_ERR_RPT_EN
0xF20020	RapidIO Domain Register	RIO_DOMAIN
0xF20024	Port-Write Control Register	PW_CTL
0xF2002C	RapidIO Assembly Identification CAR Override	ASSY_IDENT_CAR_OVRD
0xF20030	RapidIO Assembly Information CAR Override	ASSY_INF_CAR_OVRD
0xF20040	Device Soft Reset Register	DEVICE_SOFT_RESET
0xF20050	I2C Master Control Register	I2C_MASTER_CTL
0xF20054	I2C Master Status and Control Register	I2C_MASTER_STAT_CTL
0xF2005C	JTAG Control Register (Revision A/B)	JTAG_CTL
0xF20060	External MCES Trigger Counter Register	EXT_MECS_TRIG_CNTR
0xF20064	Maintenance Dropped Packet Counter Register	MAINT_DROP_PKT_CNTR
0xF20068	Switch Parameters 1 Register	SWITCH_PARAM_1
0xF2006C	Switch Parameters 2 Register	SWITCH_PARAM_2
0xF20200	Quadrant Configuration Register	QUAD_CFG
0xF20300	Device Reset and Control Register	DEVICE_RESET_CTL
Implementation Specific Multicast Mask Registers		
0xF30000–F3009C	Broadcast Multicast Mask Register {0..39}	BCAST_MCAST_MASK_0
0xF38000–F3809C	Port {0..17} Multicast Mask Register {0..39}	PORT_0_MCAST_MASK_0
Ports 1–17	For address offsets, see Implementation Specific Multicast Mask Base Addresses.	

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
Port *n* Function Registers		
0xF40004	Port {0..17} Operations Register	PORT_0_OPS
0xF40008	Port {0..17} Implementation Specific Error Detect Register	PORT_0_IMPL_SPEC_ERR_DET
0xF4000C	Port {0..17} Implementation Specific Error Rate Enable Register	PORT_0_IMPL_SPEC_ERR_RATE_EN
0xF40010	Port {0..17} VC0 Acknowledgements Transmitted Counter Register	PORT_0_VC0_PA_TX_CNTR
0xF40014	Port {0..17} Not Acknowledgements Transmitted Counter Register	PORT_0_NACK_TX_CNTR
0xF40018	Port {0..17} VC0 Retry Symbols Transmitted Counter Register	PORT_0_VC0_RTRY_TX_CNTR
0xF4001C	Port {0..17} VC0 Packets Transmitted Counter Register	PORT_0_VC0_PKT_TX_CNTR
0xF40020	Port {0..17} Trace Match Counter Value 0 Register	PORT_0_TRACE_CNTR_0
0xF40024	Port {0..17} Trace Match Counter Value 1 Register	PORT_0_TRACE_CNTR_1
0xF40028	Port {0..17} Trace Match Counter Value 2 Register	PORT_0_TRACE_CNTR_2
0xF4002C	Port {0..17} Trace Match Counter Value 3 Register	PORT_0_TRACE_CNTR_3
0xF40030	Port {0..17} Filter Match Counter Value 0 Register	PORT_0_FILTER_CNTR_0
0xF40034	Port {0..17} Filter Match Counter Value 1 Register	PORT_0_FILTER_CNTR_1
0xF40038	Port {0..17} Filter Match Counter Value 2 Register	PORT_0_FILTER_CNTR_2
0xF4003C	Port {0..17} Filter Match Counter Value 3 Register	PORT_0_FILTER_CNTR_3
0xF40040	Port {0..17} VC0 Acknowledgements Received Counter Register	PORT_0_VC0_PA_RX_CNTR
0xF40044	Port {0..17} Not Acknowledgements Received Counter Register	PORT_0_NACK_RX_CNTR
0xF40048	Port {0..17} VC0 Retry Symbols Received Counter Register	PORT_0_VC0_RTRY_RX_CNTR
0xF4004C	Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register	PORT_0_VC0_CPB_TX_CNTR
0xF40050	Port {0..17} VC0 Packets Received Counter Register	PORT_0_VC0_PKT_RX_CNTR
0xF40058	Port {0..17} Trace Port-Write Reset Register	PORT_0_TRACE_PW_CTL
0xF40060	Port {0..17} Lane Synchronization Register	PORT_0_LANE_SYNC
0xF40064	Port {0..17} VC0 Received Packets Dropped Counter Register	PORT_0_VC0_PKT_DROP_RX_CNTR
0xF40068	Port {0..17} VC0 Transmitted Packets Dropped Counter Register	PORT_0_VC0_PKT_DROP_TX_CNTR

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xF4006C	Port {0..17} VC0 TTL Packets Dropped Counter Register	PORT_0_VC0_TTL_DROP_CNTR
0xF40070	Port {0..17} VC0 CRC Limit Packets Dropped Counter Register	PORT_0_VC0_CRC_LIMIT_DROP_CNTR
0xF400CC	Port {0..17} Congestion Retry Counter Register	PORT_0_RETRY_CNTR
0xF400F0	Port {0..17} Status and Control Register	PORT_0_STATUS_AND_CTL
0xF40100	Port 1 – Starting Address	
0xF40200	Port 2 – Starting Address	
0xF40300	Port 3 – Starting Address	
0xF40400	Port 4 – Starting Address	
0xF40500	Port 5 – Starting Address	
0xF40600	Port 6 – Starting Address	
0xF40700	Port 7 – Starting Address	
0xF40800	Port 8 – Starting Address	
0xF40900	Port 9 – Starting Address	
0xF40A00	Port 10 – Starting Address	
0xF40B00	Port 11 – Starting Address	
0xF40C00	Port 12 – Starting Address	
0xF40D00	Port 13 – Starting Address	
0xF40E00	Port 14 – Starting Address	
0xF40F00	Port 15 – Starting Address	
0xF41000	Port 16 – Starting Address	
0xF41100	Port 17 – Starting Address	
0xF4FF04	Broadcast Port Operations Register	BCAST_PORT_OPS
0xF4FF08	Broadcast Port Implementation Specific Error Detect Register	BCAST_PORT_IMPL_SPEC_ERR_DET
0xF4FF0C	Broadcast Port Implementation Specific Error Rate Enable Register	BCAST_PORT_IMPL_SPEC_ERR_RATE_EN
Implementation Specific Error Logging Registers		
0xFD0000	Error Log Register	LOG_CTL
0xFD0004	Error Log Data Register	LOG_DATA
0xFD0008	Error Log Match Register {0..7}	LOG_MATCH_0
0xFD000C	Error Log Match Register {0..7}	LOG_MATCH_1
0xFD0010	Error Log Match Register {0..7}	LOG_MATCH_2

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xFD0014	Error Log Match Register {0..7}	LOG_MATCH_3
0xFD0018	Error Log Match Register {0..7}	LOG_MATCH_4
0xFD001C	Error Log Match Register {0..7}	LOG_MATCH_5
0xFD0020	Error Log Match Register {0..7}	LOG_MATCH_6
0xFD0024	Error Log Match Register {0..7}	LOG_MATCH_7
0xFD0028	Error Log Match Status Register	LOG_MATCH_STATUS
0xFD002C	Error Log Events Register	LOG_EVENTS
0xFD0030	Error Log Control 2 Register	LOG_CTL2
PLL Domain Control Registers		
0xFF0000	PLL {0..11} Control 1 Register	PLL_0_CTL_1
0xFF0004	PLL {0..11} Control 2 Register	PLL_0_CTL_2
0xFF0010	PLL 1 – Starting Address	
0xFF0020	PLL 2 – Starting Address	
0xFF0030	PLL 3 – Starting Address	
0xFF0040	PLL 4 – Starting Address	
0xFF0050	PLL 5 – Starting Address	
0xFF0060	PLL 6 – Starting Address	
0xFF0070	PLL 7 – Starting Address	
0xFF0080	PLL 8 – Starting Address	
0xFF0090	PLL 9 – Starting Address	
0xFF00A0	PLL 10 – Starting Address	
0xFF00B0	PLL 11 – Starting Address	
0xFF0FF0	Broadcast PLL Control Register	BCAST_PLL_CTL
Implementation Specific Lane Control Registers		
0xFF8000	Lane {0..47} Control Register	LANE_0_CTL
0xFF8004	Lane {0..47} PRBS Generator Seed Register	LANE_0_PRBS_GEN_SEED
0xFF8008	Lane {0..47} PRBS Error Counter Register	LANE_0_PRBS_ERR_CNTR
0xFF800C	Lane {0..47} Error Detect Register	LANE_0_ERR_DET
0xFF8010	Lane {0..47} Error Rate Enable Register	LANE_0_ERR_RATE_EN
0xFF8014	Lane {0..47} Attributes Capture Register	LANE_0_ATTR_CAPT
0xFF8018	Lane {0..47} Data Capture 0 Register	LANE_0_DATA_CAPT_0
0xFF801C	Lane {0..47} Data Capture 1 Register	LANE_0_DATA_CAPT_1
0xFF8028	Lane {0..47} DFE 1 Register	LANE_0_DFE_1

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Table 75: Address Map *(Continued)*

Base Address	Register (Full Name)	Register (Short Name)
0xFF802C	Lane {0..47} DFE 2 Register	LANE_0_DFE_2
Lanes 1–47	For address offsets, see Lane Control Registers.	
0xFFFF00	Broadcast Lane Control Register	BCAST_LANE_CTL
0xFFFF04	Broadcast Lane PRBS Generator Seed Register	BCAST_LANE_GEN_SEED
0xFFFF0C	Broadcast Lane Error Detect Register	BCAST_LANE_ERR_DET
0xFFFF10	Broadcast Lane Error Rate Enable Register	BCAST_LANE_ERR_RATE_EN
0xFFFF14	Broadcast Lane Attributes Capture Register	BCAST_LANE_ATTR_CAPT
0xFFFF18	Broadcast Lane DFE 1 Register	BCAST_LANE_DFE_1
0xFFFF1C	Broadcast Lane DFE 2 Register	BCAST_LANE_DFE_2
Error Management Broadcast Registers		
0xFFFF40	Broadcast Port Error Detect Register	BCAST_PORT_ERR_DET
0xFFFF44	Broadcast Port Error Rate Enable Register	BCAST_PORT_ERR_RATE_EN

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10.3 RapidIO Capability Registers (CARs)

These *RapidIO Specification (Rev. 2.1)* registers communicate a device's capabilities.

10.3.1 Device Identity CAR

Register Name: DEV_IDENT_CAR Reset Value: 0x0374_0038	Register Offset: 0x000000

Bits	0	1	2	3	4	5	6	7
00:07	DEVICE							
08:15	DEVICE							
16:23	VENDOR							
24:31	VENDOR							

Bits	Name	Description	Type	Reset Value
0:15	DEVICE	Device Identification. This is the vendor-assigned JTAG ID of the device.	FR	0x0374
16:31	VENDOR	Device Vendor Identifier. This value is assigned by the RapidIO Trade Association for IDT.	FR	0x0038

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10.3.2 Device Information CAR

Register Name: DEV_INF_CAR Reset Value: 0x0002_0002	Register Offset: 0x000004

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	MAJOR_REV				MINOR_REV			
16:23	Reserved							
24:31	Reserved				JTAG_REV			

Bits	Name	Description	Type	Reset Value
0:7	Reserved	Reserved	RO	0
8:10	MAJOR_REV	Device Major Revision field.	FR	0
11:15	MINOR_REV	Device Minor Revision field. 0b00000 = Revision A 0b00001 = Revision B 0b00010 = Revision C	FR	0b00010
16:27	Reserved	Reserved	RO	0
28:31	JTAG_REV	Device Revision Level. Same as the Version Level in the JTAG deviceID register. 0b000 = Revision A/B 0b010 = Revision C	RO	0b010

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10.3.3 Assembly Identity CAR

Register Name: ASSY_IDENT_CAR Reset Value: 0x0000_0000	Register Offset: 0x000008

Bits	0	1	2	3	4	5	6	7
00:07	ASSY							
08:15	ASSY							
16:23	VENDOR							
24:31	VENDOR							

Bits	Name	Description	Type	Reset Value
0:15	ASSY	This field identifies the type of assembly used. It is assigned by the assembly supplier. For more information, see RapidIO Assembly Identification CAR Override.	FR	0
16:31	VENDOR	Assembly Vendor Identifier. This field identifies the manufacturing vendor of the assembly containing this device. It is assigned by the RTA.	FR	0

10.3.4 Assembly Information CAR

Register Name: ASSY_INF_CAR Reset Value: 0x0000_0100	Register Offset: 0x00000C

Bits	0	1	2	3	4	5	6	7
00:07	ASSY_REV							
08:15	ASSY_REV							
16:23	EF_PTR							
24:31	EF_PTR							

Bits	Name	Description	Type	Reset Value
0:15	ASSY_REV	Assembly revision level. For more information, see RapidIO Assembly Information CAR Override.	FR	0
16:31	EF_PTR	Extended features pointer. This value points to the first entry in the extended features list, Port Maintenance Block Header Register.	FR	0x0100

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10.3.5 Processing Element Features CAR

Register Name: PROC_ELEM_FEAT_CAR Reset Value: 0x1800_0779	Register Offset: 0x000010

Bits	0	1	2	3	4	5	6	7
00:07	BRIDGE	MEM	PROC	SWITCH	MULTIPORT	Reserved		
08:15	Reserved							
16:23	Reserved				FLOW_ARB	MCAST	EXTD_RTE	STD_RTE
24:31	FLOW_CTL	CRC_ERR_REC	CRF	CTLS	EXT_FEAT	EXT_ADDR		

Bits	Name	Description	Type	Reset Value
0	BRIDGE	The device can bridge between S-RIO and another non-S-RIO interface 0 = Not supported 1 = Supported	FR	0
1	MEM	The device does not have physically addressable local address space and cannot be accessed as an endpoint through non-maintenance operations 0 = Not supported 1 = Supported	FR	0
2	PROC	Support for processor that executes code 0 = Not supported 1 = Supported	FR	0
3	SWITCH	Support for switching between RapidIO ports 0 = Not supported 1 = Supported	FR	1
4	MULTIPORT	The device supports the LP-Serial IDLE2 sequence 0 = Not supported 1 = Device supports multiple external S-RIO ports	FR	1
5:19	Reserved	Reserved	RR	0
20	FLOW_ARB	Flow arbitration support 0 = Not supported 1 = Supported	FR	0

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Bits	Name	Description	Type	Reset Value
21	MCAST	Multicast extensions support 0 = Not supported 1 = Supported	FR	1
22	EXTD_RTE	Extended route table configuration support 0 = Not supported 1 = Supported	FR	1
23	STD_RTE	Standard route table configuration support 0 = Not supported 1 = Supported	FR	1
24	FLOW_CTL	Flow control support 0 = Not supported 1 = Supported	FR	0
25	CRC_ERR_REC	Support for suppression of error recovery on CRC error 0 = Not supported 1 = Supported Note: This is defined in *RapidIO Specification (Rev. 1.3)* but is not specified in the *RapidIO Specification (Rev. 2.1)*.	FR	1
26	CRF	Critical Request Flow support 0 = Not supported 1 = Supported	FR	1
27	CTLS	Common Transport Large System support 0 = Not supported 1 = Supported. The device supports 16-bit sourceIDs and destIDs.	FR	1
28	EXT_FEAT	Extended Features Pointer is valid 0 = Not supported 1 = Supported. The device has an extended features list and a valid pointer to it.	FR	1
29:31	EXT_ADDR	Number of address bits supported 0b111 = 66, 50, and 34-bit addresses 0b101 = 66 and 34-bit addresses 0b011 = 50 and 34-bit addresses 0b001 = 34-bit addresses All other values are reserved.	FR	0b001

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10.3.6 Switch Port Information CAR

Register Name: SWITCH_PORT_INF_CAR Reset Value: 0x0000_1200	Register Offset: 0x000014

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	TOTAL							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RR	0
16:23	TOTAL	The total number of S-RIO ports that can be configured through the CPS-1848's registers.	RO	0x12
24:31	PORT	The port number from which the maintenance read operation accessed this register. Note: When accessed through the DEVICE's I2C or JTAG interface, the port number is not a predictable value.	RO	0x00

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10.3.7 Source Operations CAR

Register Name: SRC_OPS_CAR Reset Value: 0x0000_0004	Register Offset: 0x000018

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	NREAD	NWRITE	SWRITE	NWRITE_R	MSG	DOORBELL	Reserved	ATOMIC_TEST_AND_SWAP
24:31	ATOMIC_INCR	ATOMIC_DECR	ATOMIC_SET	ATOMIC_CLR	Reserved	PW	Reserved	

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RR	0
16	NREAD	Device can source a read operation 0 = Not supported	FR	0
17	NWRITE	Device can source a write operation 0 = Not supported	FR	0
18	SWRITE	Device supports a streaming write operation 0 = Not supported	FR	0
19	NWRITE_R	Device supports a write with response operation 0 = Not supported	FR	0
20	MSG	Device supports a data message operation 0 = Not supported	FR	0
21	DOORBELL	Device supports a doorbell operation 0 = Not supported	FR	0
22	Reserved	Reserved	RR	0
23	ATOMIC_TEST_AND_SWAP	Device supports an atomic test and swap operation 0 = Not supported	FR	0
24	ATOMIC_INCR	Device supports an atomic increment operation 0 = Not supported	FR	0
25	ATOMIC_DECR	Device supports an atomic decrement operation 0 = Not supported	FR	0

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Bits	Name	Description	Type	Reset Value
26	ATOMIC_SET	Device supports an atomic set operation 0 = Not supported	FR	0
27	ATOMIC_CLR	Device supports an atomic clear operation 0 = Not supported	FR	0
28	Reserved	Reserved	RR	0
29	PW	Device can source a port-write operation 1 = Supported	FR	1
30:31	Reserved	Reserved	RR	0

10.3.8 Switch Multicast Support CAR

Register Name: SWITCH_MCAST_SUP_CAR Reset Value: 0x0000_0000	Register Offset: 0x000030

Bits	0	1	2	3	4	5	6	7
00:07	SIMPLE	Reserved						
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0	SIMPLE	Device supports the simple multicast model 0 = Not supported	FR	0
1:31	Reserved	Reserved	RR	0

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10.3.9 Switch Route Table Entries Table Limit CAR

Register Name: SWITCH_RTE_TBL_LIM_CAR Reset Value: 0x0000_00FF	Register Offset: 0x000034

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	MAX_DESTID							
24:31	MAX_DESTID							

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RR	0
16:31	MAX_DESTID	The maximum number of configurable destIDs that are supported per port is 256.	FR	0x00FF

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10.3.10 Switch Multicast Information CAR

Register Name: SWITCH_MULT_INF_CAR Reset Value: 0x00FF_0028	Register Offset: 0x000038

Bits	0	1	2	3	4	5	6	7
00:07	BLK	PER_PORT	MAX_DESTID					
08:15	MAX_DESTID							
16:23	MCAST_MASK							
24:31	MCAST_MASK							

Bits	Name	Description	Type	Reset Value
0	BLK	Block association support 0 = Not supported	FR	0
1	PER_PORT	Per Ingress port association support 0 = Not supported	FR	0
2:15	MAX_DESTID	The maximum number of destIDs that can be associated with a multicast mask. • Revision C = 0x0FF (256 destIDs) • Revision A/B = 0x100 (257 destIDs). This value incorrectly indicates that 257 destIDs can be mapped to a multicast mask; however, the value should be 0x0FF (256 destIDs)	FR	0x0FF
16:31	MCAST_MASK	The number of multicast masks that are supported by the device. For Revision C, the reset value is based on the number of supported masks, 40, or 0x0028. For Revision A/B, the reset value is based on 40 masks x 18 ports = 720 masks, or 0x02D0.	FR	0x0028

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10.4 RapidIO Control and Status Registers (CSRs)

These *RapidIO Specification (Rev. 2.1)* registers control aspects of operation of the entire device.

10.4.1 Host Base deviceID Lock CSR

Register Name: HOST_BASE_DEVICEID_LOCK_CSR Reset Value: 0x0000_FFFF	Register Offset: 0x000068

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	HOST_BASE_DEVICEID							
24:31	HOST_BASE_DEVICEID							

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RO	0
16:31	HOST_BASE_DEVICEID	Base deviceID for the device that initializes this device. The behavior of this field is as defined in the *RapidIO Specification (Rev. 2.1), Part 3*.	RW	0xFFFF

10.4.2 Component Tag CSR

Register Name: COMP_TAG_CSR Reset Value: 0x0000_0000	Register Offset: 0x00006C

Bits	0	1	2	3	4	5	6	7
00:07	CTAG							
08:15	CTAG							
16:23	CTAG							
24:31	CTAG							

Bits	Name	Description	Type	Reset Value
0:31	CTAG	Component Tag for this device. This field is written by software. It is used for labeling and identifying port-write transactions to the host.	RW	0

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10.4.3 Standard Route Table Entries Configuration destID Select CSR

Register Name: RTE_DESTID_CSR Reset Value: 0x0000_0000	Register Offset: 0x000070

Bits	0	1	2	3	4	5	6	7
00:07	EXTD_EN	Reserved						
08:15	Reserved							
16:23	DESTID_MSB							
24:31	DESTID_LSB							

Bits	Name	Description	Type	Reset Value
0	EXTD_EN	Extended Configuration Enable. 0 = Disable 1 = Enable	RW	0
1:15	Reserved	Reserved	RO	0
16:23	DESTID_MSB	For a large common transport system, this field specifies the most significant byte of the destID used to select an entry in the switch route table when using the Standard Route Table Entry Configuration Port Select CSR.	RW	0
24:31	DESTID_LSB	Defines the destID used to select an entry in the switch routing table.	RW	0

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10.4.4 Standard Route Table Entry Configuration Port Select CSR

For more information on routing packets using this register, see Packet Routing.

Register Name: RTE_PORT_CSR Reset Value: 0x0000_00DE	Register Offset: 0x000074

Bits	0	1	2	3	4	5	6	7
00:07	PORT_3							
08:15	PORT_2							
16:23	PORT_1							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:7	PORT_3	This is the output port that all messages intended for DESTID_LSB + 3 are sent.	RW	0
8:15	PORT_2	This is the output port that all messages intended for DESTID_LSB + 2 are sent.	RW	0
16:23	PORT_1	This is the output port that all messages intended for DESTID_LSB + 1 are sent.	RW	0
24:31	PORT	This is the output port that all messages intended for DESTID_LSB are sent. 0x00–0x11 = Output Port Number 0x40–0x68 = Multicast Mask Number 0xDD = The packet is discarded and the routing table entry is overwritten with a value of 0xDF. 0xDE = Use Default Port Route, as set in Standard Route Table Entry Default Port CSR 0xDF = No Route, discard packets All other values are reserved and result in packet discard.	RW	0xDE

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10.4.5 Standard Route Table Entry Default Port CSR

Register Name: RTE_DEFAULT_PORT_CSR Reset Value: 0x0000_0000	Register Offset: 0x000078

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	DEFAULT_PORT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	DEFAULT_PORT	This defines the device's default output port (for more information, see Packet Routing).	RW	0

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10.4.6 Multicast Mask Port CSR

Register Name: MCAST_MASK_PORT_CSR Reset Value: 0x0000_0000	Register Offset: 0x000080

Bits	0	1	2	3	4	5	6	7
00:07	MCAST_MASK							
08:15	MCAST_MASK							
16:23	EGRESS_PORT							
24:31	Reserved	MASK_CMD			Reserved			PORT_STATUS

Bits	Name	Description	Type	Reset Value
0:15	MCAST_MASK	Defines the multicast mask to be modified/queried as determined by the MASK_CMD	RW	0
16:23	EGRESS_PORT	Defines the port number that is modified/queried by the MASK_CMD	RW	0
24	Reserved	Reserved	RO	0
25:27	MASK_CMD	0b000 = Write to verify 0b001 = Add port 0b010 = Delete port 0b100 = Delete all ports 0b101 = Add all ports All other values are reserved.	RW	0b000
28:30	Reserved	Reserved	RO	0
31	PORT_STATUS	Indicates the existence of the egress port and multicast mask pair as a result of the last Write_to_Verify command. 0 = Port not enabled in the multicast mask 1 = Port is enabled in the multicast mask	RO	0

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10.4.7 Multicast Association Selection CSR

Register Name: MCAST_ASSOC_SEL_CSR Reset Value: 0x0000_0000	Register Offset: 0x000084

Bits	0	1	2	3	4	5	6	7
00:07	DESTID_MSB							
08:15	DESTID_LSB							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:7	DESTID_MSB	Selects the most significant byte of a large transport destID for an association operation	RW	0
8:15	DESTID_LSB	Selects a destID for an association operation	RW	0
16:31	MASK	Selects the multicast mask number for an association	RW	0

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10.4.8 Multicast Association Operations CSR

Register Name: MCAST_ASSOC_OP_CSR Reset Value: 0x0000_0000	Register Offset: 0x000088

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	TYPE	CMD		Reserved				STATUS

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24	TYPE	0 = Small transport association 1 = Large transport association	RW	0
25:26	CMD	Command when register is written 0b00 = Write to verify 0b01 = Delete association 0b11 = Add association Note: The value assigned to “Delete association” is inconsistent with the *RapidIO Specification (Rev. 2.1)*.	RW	0b00
27:30	Reserved	Reserved	RO	0
31	STATUS	Contains the result of the last write to verify command 0 = No association 1 = Association present	RO	0

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10.5 LP-Serial Extended Features Registers with Software Assisted Error Recovery

Part 6 of the *RapidIO Specification (Rev. 2.1)* specifies a register extension block ("Generic Endpoint-Free Devices with Software Assisted Error Recovery") which contains status information and control values for various physical layer functions of the RapidIO processing element. These registers are defined in this section.

10.5.1 Port Maintenance Block Header Register

Register Name: PORT_MAINT_BLK_HEAD Reset Value: 0x0600_0009	Register Offset: 0x000100

Bits	0	1	2	3	4	5	6	7
00:07	EF_PTR							
08:15	EF_PTR							
16:23	EF_ID							
24:31	EF_ID							

Bits	Name	Description	Type	Reset Value
0:15	EF_PTR	Extended features pointer. This value points to the next entry in the extended features list, VC Register Block Header Register.	RO	0x0600
16:31	EF_ID	Hard Wired Extended Features ID	RO	0x0009

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10.5.2 Port Link Timeout Control CSR

This register contains the timeout value for the device's S-RIO ports. This timeout is for link events such as sending a packet to receiving the corresponding acknowledgement, and sending a link-request to receiving the corresponding link-response.

Register Name: PORT_LINK_TO_CTL_CSR Reset Value: 0xFFFF_FF00	Register Offset: 0x000120

Bits	0	1	2	3	4	5	6	7
00:07	TIMEOUT							
08:15	TIMEOUT							
16:23	TIMEOUT							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:23	TIMEOUT	Timeout internal value Timeout period is: TIMEOUT * 352 ns	RW	0xFFFFFF
24:31	Reserved	Reserved	RO	0

10.5.3 Port General Control CSR

Register Name: PORT_GEN_CTL_CSR Reset Value: 0x0000_0000	Register Offset: 0x00013C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved		DISCV	Reserved				
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:1	Reserved	Reserved	RO	0
2	DISCV	0 = Device not discovered 1 = Device discovered	RW	0
3:31	Reserved	Reserved	RO	0

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10.5.4 Port {0..17} S-RIO Extended Features Base Addresses

Port	Address
0	0x000140
1	0x000160
2	0x000180
3	0x0001A0
4	0x0001C0
5	0x0001E0
6	0x000200
7	0x000220
8	0x000240
9	0x000260
10	0x000280
11	0x0002A0
12	0x0002C0
13	0x0002E0
14	0x000300
15	0x000320
16	0x000340
17	0x000360

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10.5.5 Port {0..17} Link Maintenance Request CSR

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

The captured ackID is not used to accept any outstanding packets or restart transmission of packets. If the captured ackID is invalid, then Port {0..17} Error and Status CSR[PORT_ERR] is set but Port {0..17} Error Detect CSR[LR_ACKID_ILL] is not set.

Register Name: PORT_{0..17}_LINK_MAINT_REQ_CSR Reset Value: 0x0000_0000	Register Offset: 0x000140 + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved					CMD		

Bits	Name	Description	Type	Reset Value
0:28	Reserved	Reserved	RO	0
29:31	CMD	Command to be sent in the link-request control symbol. If read, this field returns the last written value. 0b011 = Reset device 0b100 = Input status 0b000–0b010 = Reserved 0b101–0b111 = Reserved Note: Writing 0b011 sends four reset control symbols to the link partner. Note: Transmitting an “Input status” request will cause the Port {0..17} Error and Status CSR[OUTPUT_ERR] bit to be set. Note (Revision A/B only): The Port {0..17} Error and Status CSR[OUTPUT_FAIL] bit must be clear and remain clear before any link request can be sent.	RW	0b000

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10.5.6 Port {0..17} Link Maintenance Response CSR

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

Register Name: PORT_{0..17}_LINK_MAINT_RESP_CSR Reset Value: 0x0000_0000	Register Offset: 0x000144 + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALID	Reserved						
08:15	Reserved							
16:23	Reserved					ACKID_STATUS		
24:31	ACKID_STATUS			LINK_STATUS				

Bits	Name	Description	Type	Reset Value
0	VALID	If the previous Link-Request causes a Link-Response, then this bit indicates that the Link-Response has been received and the status fields are valid. If the Link-Request did not cause a Link-Response, this bit indicates that the Link-Request has been transmitted. This bit clears on read.	RR	0
1:20	Reserved	Reserved	RO	0
21:26	ACKID_STATUS	ackID status field from the Link-Response control symbol. The value of the next ackID expected by the receiver. Note: Bit 21 is available only when IDLE2 is in use on the link.	RO	0
27:31	LINK_STATUS	Link status field from the Link-Response control symbol 0b00010 = Error 0b00100 = Retry-stopped 0b00101 = Error-stopped 0b10000 = OK All others are Reserved	RO	0b00000

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10.5.7 Port {0..17} Local ackID CSR

Before changing the contents of this register, ensure that Port {0..17} Error and Status CSR[OUTPUT_FAIL] is clear and will remain clear. Changing this register when OUTPUT_FAIL is set will result in undefined device operation.

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

Register Name: PORT_{0..17}_LOCAL_ACKID_CSR Reset Value: 0x0000_0000	Register Offset: 0x000148 + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	CLR	Reserved	INBOUND					
08:15	Reserved							
16:23	Reserved		OUTSTD					
24:31	Reserved		OUTBOUND					

Bits	Name	Description	Type	Reset Value
0	CLR	1 = Discard all outstanding unacknowledged packets. This bit should be written only when trying to recover a failed link. This bit will return 0 when read.	WO	0
1	Reserved	Reserved	RO	0
2:7	INBOUND	Input port next expected ackID. Note: Bit 2 is available only when IDLE2 is in use on the link. Note: This field is cleared when PORT_DIS is set to 1 in the Port {0..17} Control 1 CSR.	RW	0
8:17	Reserved	Reserved	RO	0
18:23	OUTSTD	The output port unacknowledged ackID status. The next acknowledge control symbol ackID field that indicates the ackID value expected in the next received acknowledge control symbol. Note: Bit 18 is available only when IDLE2 is in use on the link. Note: This field is cleared when PORT_DIS is set to 1 in the Port {0..17} Control 1 CSR.	RW	0
24:25	Reserved	Reserved	RO	0
26:31	OUTBOUND	The next transmitted ackID value for the port. Writing this value can force retransmission of outstanding unacknowledged packets in order to manually use error recovery. Note: Bit 26 is available only when IDLE2 is in use on the link. Note: This field is cleared when PORT_DIS is set to 1 in the Port {0..17} Control 1 CSR.	RW	0

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10.5.8 Port {0..17} Error and Status CSR

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

Register Name: PORT_{0..17}_ERR_STAT_CSR Reset Value: 0xE000_0001	Register Offset: 0x000158 + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	IDLE2	IDLE2_EN	IDLE_SEQ	Reserved		OUTPUT_DROP	OUTPUT_FAIL	OUTPUT_DEGR
08:15	Reserved			OUTPUT_RETRY	OUTPUT_RETRIED	OUTPUT_RETRY_STOP	OUTPUT_ERR	OUTPUT_ERR_STOP
16:23	Reserved					INPUT_RETRY_STOP	INPUT_ERR	INPUT_ERR_STOP
24:31	Reserved			PW_PNDG	PORT_UNAVL	PORT_ERR	PORT_OK	PORT_UNINIT

Bits	Name	Description	Type	Reset Value
0	IDLE2	Indicates whether the port supports IDLE2 sequence for throughput rates of less than 6.25 Gbaud 0 = Not supported 1 = Supported	RO	1
1	IDLE2_EN	Controls whether the IDLE2 sequence is enabled for baud rates less than 6.25 Gbaud 0 = Disable 1 = Enable Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	1
2	IDLE_SEQ	Indicates which IDLE sequence is active 0 = IDLE1 (RapidIO Gen1) is active 1 = IDLE2 (RapidIO Gen2) is active	RO	1
3:4	Reserved	Reserved. Bit 4 is defined as FLOW_CTL_MODE in the *RapidIO Specification (Rev. 2.1)*. For more information on the CPS-1848's implementation of this bit, see RX_FC in the Port {0..17} Status and Control Register.	RO	0
5	OUTPUT_DROP	1 = The port discarded a packet at the output. Once set, it remains set until a 1 is written to clear. Note: OUTPUT_DROP cannot be set when the port is disabled (Port {0..17} Control 1 CSR[PORT_DIS] is set to 1).	W1R	0

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Bits	Name	Description	Type	Reset Value
6	OUTPUT_FAIL	1 = The port encountered a failure condition such that the port's failed error threshold has been reached. Once set, it remains set until a 1 is written to clear.	W1R	0
7	OUTPUT_DEGR	1 = The port encountered a degraded condition such that the port's degraded error threshold has been reached. Once set, it remains set until a 1 is written to clear.	W1R	0
8:10	Reserved	Reserved	RO	0
11	OUTPUT_RETRY	1 = Output Retry Encountered. The port encountered a retry condition. This bit is set when OUTPUT_RETRY_STOP is set, and once set, it remains set until written with a 1 to clear.	W1R	0
12	OUTPUT_RETRIED	1 = Output retried. The port received a packet retry control symbol and cannot make forward progress. This bit is set when OUTPUT_RETRY_STOP is set, and cleared when a packet accepted or packet-not-accepted control symbol is received.	RO	0
13	OUTPUT_RETRY_STOP	1 = Output Retry - Port is stopped. The output port received a Packet-Retry control symbol and is in the output retry-stopped state.	RO	0
14	OUTPUT_ERR	1 = Output Error was encountered. The output port encountered (and possibly recovered from) a transmission error. This bit is set when OUTPUT_ERR_STOP is set and once set it remains set until written with a 1 to clear	W1R	0
15	OUTPUT_ERR_STOP	1 = Output Error. The output port is in the Output Error-Stopped state.	RO	0
16:20	Reserved	Reserved	RO	0
21	INPUT_RETRY_STOP	1 = Input Retry. The input port is in the input retry-stopped state.	RO	0
22	INPUT_ERR	1 = Input Error was encountered. The input port encountered (and possibly recovered from) a transmission error. This bit is to be set when INPUT_ERR_STOP is set. Once set, it remains set until written with a 1 to clear.	W1R	0
23	INPUT_ERR_STOP	1 = Input Error - Port is stopped. The input port is in the Input-Error Stopped state.	RO	0
24:26	Reserved	Reserved	RO	0
27	PW_PNDG	1 = Pending port-write. The port encountered a condition that required it to initiate a Port-Write. Once set, this bit remains set until written with a 1 to clear.	W1R	0
28	PORT_UNAVL	0 = This port is always available	RO	0

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Bits	Name	Description	Type	Reset Value
29	PORT_ERR	Port Error Status[a b] (Revision A/B): To clear this bit, see System Controlled Recovery and HS-LP Controlled Recovery. (Revision C): To clear this bit, reset the port and the link partner.	W1R	0
30	PORT_OK	0 = The port is uninitialized. 1 = The port is initialized and is exchanging error free control symbols with the attached device.	RO	0
31	PORT_UNINIT	1 = The port (input and output) is not initialized. Ports are uninitialized after reset. Note: PORT_UNINIT may or may not be 1 when PORT_OK is 0. PORT_OK is the only status bit that indicates whether a port can exchange packets.	RO	1

a. This bit is set when the port enters the fatal error state as defined in the *RapidIO Specification (Rev. 2.1)*, Part 6. For example:
* Too many response timeouts occur (16)
* A link-response is received with an invalid ackID
Part 6 also requires that this bit be reset when it is read. However, this functionality creates an issue when the field is read while the port is still in the fatal error state in that the state of the bit no longer represents the state of the port. To prevent this behavior, the Port Level Block does not reset this bit on a read while it is in the fatal error state (for more information, see HS-LP Controlled Recovery).

b. (Revision A/B only) This bit is not cleared by a per-port reset. If it is set then the port will drop all packets routed to the Final Buffer, including maintenance packet responses. To recover, the port must send a link-request/input status control symbol and receive a response. This will clear the PORT_ERR and packet drop condition. The CPS-1848 will send a link-request/input-status control symbol when either of the following occurs:
* A packet-not-accepted control symbol is received
* 0b100 is written to the Port {0..17} Link Maintenance Request CSR.CMD

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10.5.9 Port {0..17} Control 1 CSR

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

Register Name: PORT_{0..17}_CTL_1_CSR Reset Value: 0xD040_0001	Register Offset: 0x00015C + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	PWIDTH		INIT_PWIDTH			PWIDTH_OVRD		
08:15	PORT_DIS	OUTPUT_PORT_EN	INPUT_PORT_EN	ERR_CHK_DIS	MCAST_CS	Reserved	ENUM_B	Reserved
16:23	Reserved				ERR_MASK			
24:31	ERR_MASK				STOP_ON_PORT_FAIL_ENC_EN	DROP_PKT_EN	PORT_LOCKOUT	PORT_TYPE

Bits	Name	Description	Type	Reset Value
0:1	PWIDTH	Indicates the port width modes supported by the port 0b00 = No support for 2x or 4x 0b01 = No support for 2x; support for 4x 0b10 = Support for 2x; no support for 4x 0b11 = Support for 2x and 4x Note: 1x is supported by all ports. Note: The definition of 0b01 and 0b10 is consistent with the *RapidIO Specification (Rev. 2.0)*. This definition is incompatible with the *RapidIO Specification (Rev. 1.3)* and earlier specifications, and is incompatible with the *RapidIO Specification (Rev. 2.1)* and later specifications.	RO	0b11
2:4	INIT_PWIDTH	Initialized Port Width 0b000 = Single-lane port 0b001 = Single-lane port; lane R (redundancy lane) 0b010 = 4x lane port 0b011 = 2x lane port All others are reserved Note: 1x with redundancy is not considered a 2x port – it is a 1x port.	RO	0b010

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Bits	Name	Description	Type	Reset Value
5:7	PWIDTH_OVRD	Software port configuration of the width modes during port initialization 0b000 = No override 0b001 = Reserved 0b010 = Force single-lane port 0b011 = Force single-lane port; lane R (redundancy lane) 0b100 = Reserved 0b101 = 2x mode enabled, 4x mode disabled 0b110 = 4x mode enabled, 2x mode disabled 0b111 = 2x and 4x modes enabled The port does not allow the enabling of a width mode that is not supported by the port. A change in the value of this field will cause the port to re-initialize using the new field value. Note: This field is cleared when PORT_DIS is toggled from 1 to 0.	RW	0b000
8	PORT_DIS	Port Disable 0 = Enable port receivers/drivers 1 = Disable port receivers/drivers; they are unable to receive/transmit any packets or control symbols Note: When PORT_DIS is 1, ackID values are cleared to zero. For more information, see Port {0..17} Local ackID CSR.	RW	0
9	OUTPUT_PORT_EN	Output port transmit enable 0 = The port is stopped and not enabled to issue any packets except to route or respond to I/O logical Maintenance packets. Control symbols are not affected and are sent normally. 1 = Port is enabled to issue any packets Note: When OUTPUT_PORT_EN is cleared from 1 to 0, packets routed to this port are discarded. Any packets already in the Final Buffer are transmitted. Note: For Revision C, the reset value for this bit is 1. For Revision A/B, the reset value is 0.	RW	0b1
10	INPUT_PORT_EN	Input port receive enable 0 = The port is stopped and only enabled to route or respond to I/O logical Maintenance packets. Other packets generate Packet-Not-Accepted control symbols to force an error condition to be signaled by the sending device. Control symbols are not affected and are handled normally. 1 = Port is enabled to respond to any packets	RW	0

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Bits	Name	Description	Type	Reset Value
11	ERR_CHK_DIS	0 = S-RIO transmission error checking and recovery enabled 1 = S-RIO transmission error checking and recovery disabled	FR	0
12	MCAST_CS	0 = Do not send multicast event control symbols to this port 1 = Send multicast event control symbols to this port	RW	0
13	Reserved	Reserved	RO	0
14	ENUM_B	An enumeration boundary aware system enumeration algorithm honors this flag. The algorithm on either the ingress or egress port will not enumerate past a port with this bit set. This provides for software enforced enumeration domains with the S-RIO fabric. The device simply stores whatever value is written into this field.	RW	0
15:19	Reserved	Reserved	RO	0
20:27	ERR_MASK	Suppress packet re-transmission on CRC error. 0b0000_0000 = Error recovery suppression disabled 0bxxxx_xxx1 = Suppress CRF = 0, priority 0 re-transmission 0bxxxx_xx1x - Suppress CRF = 0, priority 1 re-transmission 0bxxxx_x1xx - Suppress CRF = 0, priority 2 re-transmission 0bxxxx_1xxx - Suppress CRF = 0, priority 3 re-transmission 0bxxx1_xxxx - Suppress CRF = 1, priority 0 re-transmission 0bxx1x_xxxx - Suppress CRF = 1, priority 1 re-transmission 0bx1xx_xxxx - Suppress CRF = 1, priority 2 re-transmission 0b1xxx_xxxx - Suppress CRF = 1, priority 3 re-transmission Either set all bits or no bits in this field to ensure consistent operation when a packet's PRIO or CRF field is corrupted. The receipt of a packet with a CRC error when the bit that matches the packet's priority is set causes the packet to be acknowledged and dropped. Note that Port {0..17} Error and Status CSR.OUTPUT_DROP is not set. Instead, Port {0..17} Implementation Specific Error Detect Register.CRC_EVENT is set on the receiving port.	RW	0b000000 00
28	STOP_ON_PORT_ FAIL_ENC_EN	This bit is used with the DROP_PKT_EN bit to force certain behavior when the Error Rate Failed Threshold has been met (for more information, see Table 58).	RW	0
29	DROP_PKT_EN	This bit is used with the STOP_ON_PORT_FAIL_ENC_EN bit to force certain behavior when the Error Rate Failed Threshold has been met (for more information, see Table 58).	RW	0

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Bits	Name	Description	Type	Reset Value
30	PORT_LOCKOUT	When this bit is cleared, the packets that can be received and issued are controlled by the state of the OUTPUT_PORT_EN and INPUT_PORT_EN bits in this register. When this bit is set = 1, this port is stopped and is not enabled to issue or receive any packets; the input port can still follow the training procedure and can still send and respond to Link-Requests; all received packets return Packet-Not-Accepted control symbols to force an error condition to be signaled by the sending device.	RW	0
31	PORT_TYPE	This indicates the port type 1 = Serial port	FR	1

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10.5.10 Port {0..17} Control 2 CSR

For base address information, see Port {0..17} S-RIO Extended Features Base Addresses.

Register Name: PORT_{0..17}_CTL_2_CSR Reset Value: 0x0000_0000	Register Offset: 0x000154 + (0x20 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				AUTOBAUD	Reserved		
08:15	Reserved							
16:23	Reserved							
24:31	Reserved				INACT_LANES_EN	SCRAM_DIS	Reserved	

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4	AUTOBAUD	0 = Automatic baud rate discovery is not supported	FR	0
5:27	Reserved	Reserved	RO	0
28	INACT_LANES_EN	0 = All lane enables (active and inactive) are controlled solely by the port's Initialization State Machine 1 = Enables the receivers of all of the port's current inactive lanes. Enables the drivers of all of the port's current inactive lanes if and only if the port's Initialization State Machine is not in the Silent state. If IDLE2 is used on the active lanes of the port, the inactive lanes of the port will report their lane number and port width on the CS field marker and handle commands carried in the CS field as if they were active lanes.	RW	0

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Bits	Name	Description	Type	Reset Value
29	SCRAM_DIS	Scrambler and Descrambler Disable 1 = Disable the transmit scrambler and receive descrambler for control symbol and packet data characters. Control symbol and packet data characters are neither scrambled in the transmitter before transmission nor descrambled in the receiver upon reception. The transmit scrambler remains enabled for the generation of pseudo-random data characters for the IDLE2 random data field. Note: When modifying this bit, it should be applied to all ports associated within the same PLL. For example: • Quadrant 0 / QCFG[1:0] = 0b00: Should modify offset Port 0 of Port {0..17} Control 2 CSR • Quadrant 0 / QCFG[1:0] = 0b11: Should modify offsets Port 0, 12, and 16 of Port {0..17} Control 2 CSR	RW	0
30:31	Reserved	Reserved	RO	0

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10.6 Virtual Channel Extended Features Block Registers

Part 6 of the *RapidIO Specification (Rev. 2.1)* specifies a register extension block that contains status information and control values for related to Virtual Channel operation for a RapidIO processing element. These registers are defined in this section.

10.6.1 VC Register Block Header Register

Register Name: VC_REGISTER_BLK_HEAD Reset Value: 0x1000_000A	Register Offset: 0x000600

Bits	0	1	2	3	4	5	6	7
00:07	EF_PTR							
08:15	EF_PTR							
16:23	EF_ID							
24:31	EF_ID							

Bits	Name	Description[a]	Type	Reset Value
0:15	EF_PTR	Extended features pointer. This value points to the next entry in the extended features list, Error Management Extensions Block Header Register.	RO	0x1000
16:31	EF_ID	Hard Wired Extended Features ID	RO	0x000A

a. This register is not supported by the CPS-1848; however, the EF_PTR value is valid for the device.

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10.7 Error Management Extensions Block Registers

Part 8 of the *RapidIO Specification (Rev. 2.1)* specifies a register extension block which contains status information and control values for logical and physical layer error management for RapidIO devices. These registers are defined in this section.

10.7.1 Error Management Extensions Block Header Register

Register Name: ERR_MGT_EXTENSION_BLK_HEAD Reset Value: 0x2000_0007	Register Offset: 0x001000

Bits	0	1	2	3	4	5	6	7
00:07	EF_PTR							
08:15	EF_PTR							
16:23	EF_ID							
24:31	EF_ID							

Bits	Name	Description	Type	Reset Value
0:15	EF_PTR	Extended features pointer. This value points to the next entry in the extended features list, Lane Status Block Header Register.	RO	0x2000
16:31	EF_ID	Hard Wired Extended Features ID	RO	0x0007

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10.7.2 Logical/Transport Layer Error Detect CSR

A write to any field in this register locks the written value when the corresponding EN is set in the next register. A software write of zeros to all fields that are non-zero is required to unlock error detection. Another unlocking function is also supported (see notes on Logical/Transport Layer Error Enable CSR).

Register Name: LT_ERR_DET_CSR Reset Value: 0x0000_00000	Register Offset: 0x001008

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				ILL_TRAN	Reserved		
08:15	UNSOL_RESP	UNSUP_TRAN	Reserved					
16:23	Reserved							
24:31	Reserved							IMP_SPEC_ERR

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4	ILL_TRAN	1 = Illegal transaction decode. Received a Maintenance read/write request packet with an invalid size, a Maintenance read request with data, or a Maintenance write received without data.	RW	0
5:7	Reserved	Reserved	RO	0
8	UNSOL_RESP	1 = Received a Maintenance response with hop count of 0.	RW	0
9	UNSUP_TRAN	1 = Received an unsupported transaction. Received a port-write with hop count of 0.	RW	0
10:30	Reserved	Reserved	RO	0
31	IMP_SPEC_ERR	1 = Detected an IDT implementation-specific error (see also Logical/Transport Layer Control Capture CSR)	RW	0

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10.7.3 Logical/Transport Layer Error Enable CSR

A software write of zero to all enabled fields corresponding to errors that have caused an error detect lock (see Logical/Transport Layer Error Detect CSR) will unlock the error detect function. To activate the error capturing function, set the enable bit in this register and then ensure that the corresponding status bit in the Logical/Transport Layer Error Detect CSR is clear.



The same settings should be used in the Logical/Transport Layer Error Report Enable Register and this register; otherwise, detected events may not be reported, or port-writes/interrupts may be sent/asserted with no indication of the cause.

Register Name: LT_ERR_EN_CSR Reset Value: 0x0000_00000	Register Offset: 0x00100C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				ILL_TRAN_EN	Reserved		
08:15	UNSOL_RESP_EN	UNSUP_TRAN_EN	Reserved					
16:23	Reserved							
24:31	Reserved							IMP_SPEC_ERR_EN

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4	ILL_TRAN_EN	1 = Illegal transaction decode error enable. Enable capture and lock as defined in the *RapidIO Specification (Rev. 2.1), Part 8*, due to supported request/response packet with undefined field values.	RW	0
5:7	Reserved	Reserved	RO	0
8	UNSOL_RESP_EN	1 = Unsolicited response error enable. Enable capture and lock as defined in the *RapidIO Specification (Rev. 2.1), Part 8*, due to receiving an unsolicited/unexpected response packet (only maintenance responses).	RW	0
9	UNSUP_TRAN_EN	1 = Enable the capture of unsupported transactions (port-writes with a hop count of 0).	RW	0
10:30	Reserved	Reserved	RO	0
31	IMP_SPEC_ERR_EN	1 = Enable capture of IDT implementation-specific errors (see also Logical/Transport Layer Control Capture CSR)	RW	0

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10.7.4 Logical/Transport Layer deviceID Capture CSR

The contents of this register are locked simultaneously with the values in the Logical/Transport Layer Error Detect CSR, and can be unlocked using same method.

Register Name: LT_DEVICEID_CAPT_CSR Reset Value: 0x0000_00000	Register Offset: 0x001018

Bits	0	1	2	3	4	5	6	7
00:07	DESTID_MSB							
08:15	DESTID_LSB							
16:23	SOURCEID_MSB							
24:31	SOURCEID							

Bits	Name	Description	Type	Reset Value
0:7	DESTID_MSB	Most significant byte of the destID associated with the error.	RW	0
8:15	DESTID_LSB	The destID associated with the error.	RW	0
16:23	SOURCEID_MSB	Most significant byte of the sourceID associated with the error.	RW	0
24:31	SOURCEID	The sourceID associated with the error.	RW	0

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10.7.5 Logical/Transport Layer Control Capture CSR

The contents of this register are locked simultaneously with the values in the Logical/Transport Layer Error Detect CSR, and can be unlocked using same method.

Multiple errors in the same packet may cause multiple bits to be set in this register. For example, a Maintenance Read Size Invalid error and a Maintenance Received with Data error are both detected when a Maintenance Read Request has the dual defects of requesting more than 64 bytes and includes data.

Register Name: LT_CTL_CAPT_CSR Reset Value: 0x0000_00000	Register Offset: 0x00101C

Bits	0	1	2	3	4	5	6	7
00:07	FTYPE				TTYPE			
08:15	Reserved							
16:23	Reserved							
24:31	IMP_SPEC							

Bits	Name	Description	Type	Reset Value
0:3	FTYPE	Format type associated with the error	RW	0
4:7	TTYPE	Transaction type associated with the error	RW	0
8:23	Reserved	Reserved	RO	0
24:31	IMP_SPEC	Implementation-specific information associated with the error	RW	0

Logical/Transport Layer Error Detect CSR [31]	Logical/Transport Layer Control Capture CSR [24:31]	Error Description[a]
0b1	0b0000_0000	No Error
0b1	0b0000_0001	Maintenance Read Size Invalid (MTC_BAD_READ_SIZE) Triggered when a read request maintenance packet has an invalid size (that is, not 8, 16, 32, or 64 bytes). A response packet with an error status is generated.
0b1	0b0000_0010	Maintenance Write Size Invalid (MTC_BAD_WR_SIZE) Triggered when: • A write request maintenance packet has an invalid size (that is, not 8, 16, 32, or 64 bytes). A response packet with an error status is generated. • A maintenance payload size does not match the configured size (for example, a payload size of 64 bytes requires 64 bytes of payload).

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Logical/Transport Layer Error Detect CSR [31]	Logical/Transport Layer Control Capture CSR [24:31]	Error Description[a]
0b1	0b0000_0100	Maintenance Read Received with Data (MTC_READ_WITH_DATA) Triggered if a Maintenance read request packet is received with a payload. A response packet with an error status is generated.
0b1	0b0000_1000	Maintenance Write Received without Data (MTC_WR_WITHOUT_DATA) Triggered if a Maintenance write packet is received without a payload. A response packet with an error status is generated.
0b1	0b0001_0000	Maintenance Packet Received was Too Small or Too Large (MTC_PKT_SIZE_ERR) Triggered if the maintenance packet header fields are incomplete, or if the write payload exceeds 64 bytes.
0b1	0b0010_0000	Reserved
0b1	0b0100_0000	Maintenance Transaction Field Error (MTC_TTPYE_ERR) Triggered when the TTYPE of an inbound maintenance packet with a hop count of 0 is a value other than a read request (0b0000) or a write request (0b0001).
0b1	All other values	Reserved

a. Errors are detected in Maintenance packets with a hop count of 0.

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10.7.6 Port-Write Target deviceID CSR

Register Name: PW_TARGET_DEVICEID_CSR Reset Value: 0x0000_00000	Register Offset: 0x001028

Bits	0	1	2	3	4	5	6	7
00:07	DESTID_MSB							
08:15	DESTID							
16:23	LARGE	Reserved						
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:7	DESTID_MSB	Most significant byte of the destID to be used for all port-writes (large transport only).	RW	0
8:15	DESTID	destID to be used for all port-writes.	RW	0
16	LARGE	Large transport. deviceID size to use for a port-write: 0 = Small transport 1 = Large transport	RW	0
17:31	Reserved	Reserved	RO	0

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10.7.7 Packet Time to Live CSR

Register Name: PKT_TTL_CSR Reset Value: 0x0000_00000	Register Offset: 0x00102C

Bits	0	1	2	3	4	5	6	7
00:07	TTL							
08:15	TTL							
16:23	Reserved							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:15	TTL	Time-to-live value. Maximum amount of time a packet can live in the Final Buffer. TTL is disabled if this field is 0. To set a TTL value use the following formula: TTL x 1.6 us.	RW	0
16:31	Reserved	Reserved	RO	0

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10.7.8 Port Error Management Register Base Addresses

Port	Address
0	0x001040
1	0x001080
2	0x0010C0
3	0x001100
4	0x001140
5	0x001180
6	0x0011C0
7	0x001200
8	0x001240
9	0x001280
10	0x0012C0
11	0x001300
12	0x001340
13	0x001380
14	0x0013C0
15	0x001400
16	0x001440
17	0x001480

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10.7.9 Port {0..17} Error Detect CSR

This register indicates Standard physical layer errors except IMP_SPEC_ERR, which indicates IDT implementation specific errors. The broadcast version of this register is Broadcast Port Error Detect Register, which will write the same value to all ports. For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_ERR_DET_CSR Reset Value: 0x0000_0000	Register Offset: 0x001040 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR	Reserved						
08:15	Reserved	CS_CRC_ERR	UNEXP_ACKID	CS_NOT_ACC	PKT_ILL_ACKID	PKT_CRC_ERR	PKT_ILL_SIZE	Reserved
16:23	IDLE1_ERR	Reserved						
24:31	Reserved		LR_ACKID_ILL	PRTCL_ERR	Reserved	DELIN_ERR	CS_ACK_ILL	LINK_TIMEOUT

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR	1 = Detected an IDT implementation-specific error (see Port {0..17} Implementation Specific Error Detect Register)	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR	1 = Detected a control symbol with a bad CRC	RW	0
10	UNEXP_ACKID	1 = Detected an acknowledge control symbol with an unexpected ackID	RW	0
11	CS_NOT_ACC	1 = Detected a packet-not-accepted control symbol	RW	0
12	PKT_ILL_ACKID	1 = Detected a packet with a bad ackID	RW	0
13	PKT_CRC_ERR	1 = Detected a packet with bad CRC Note: This error is suppressed when Port {0..17} Operations Register.CRC_DIS bit is set and Port {0..17} Control 1 CSR.ERR_MASK bit is set for the priority of a packet received with a CRC error.	RW	0
14	PKT_ILL_SIZE	1 = Detected a packet that exceeded the maximum allowed size	RW	0
15	Reserved	Reserved	RO	0
16	IDLE1_ERR	1 = Detected a data character in an IDLE1 sequence	RW	0
17:25	Reserved	Reserved	RO	0

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(Continued)

Bits	Name	Description	Type	Reset Value
26	LR_ACKID_ILL	1 = Detected a link-response with an ackID that is not outstanding	RW	0
27	PRTCL_ERR	1 = Detected a protocol error	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR	1 = Detected a delineation error	RW	0
30	CS_ACK_ILL	1 = Detected an an unexpected packet or retry control symbol. Note: This does not include packet-not-accept control symbols.	RW	0
31	LINK_TIMEOUT	1 = Detected a link timeout error	RW	0

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10.7.10 Port {0..17} Error Rate Enable CSR

The broadcast version of this register is Broadcast Port Error Rate Enable Register, which will write the same value to all ports. For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_ERR_RATE_EN_CSR Reset Value: 0x0000_00000	Register Offset: 0x001044 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR_EN	Reserved						
08:15	Reserved	CS_CRC_ERR_EN	UNEXP_ACKID_EN	CS_NOT_ACC_EN	PKT_ILL_ACKID_EN	PKT_CRC_ERR_EN	PKT_ILL_SIZE_EN	Reserved
16:23	IDLE1_ERR_EN	Reserved						
24:31	Reserved		LR_ACKID_ILL_EN	PRTCL_ERR_EN	Reserved	DELIN_ERR_EN	CS_ACK_ILL_EN	LINK_TIMEOUT_EN

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
10	UNEXP_ACKID_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
11	CS_NOT_ACC_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
12	PKT_ILL_ACKID_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
13	PKT_CRC_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
14	PKT_ILL_SIZE_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
15	Reserved	Reserved	RO	0
16	IDLE1_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
17:25	Reserved	Reserved	RO	0

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Bits	Name	Description	Type	Reset Value
26	LR_ACKID_ILL_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
27	PRTCL_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
30	CS_ACK_ILL_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
31	LINK_TIMEOUT_EN	1 = Enable the capture and counting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0

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10.7.11 Port {0..17} Attributes Capture CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_ATTR_CAPT_CSR Reset Value: 0x0000_00000	Register Offset: 0x001048 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	INFO_TYPE			ERR_TYPE				
08:15	Reserved							
16:23	Reserved							IMP_DEP
24:31	IMP_DEP				Reserved			VALID

Bits	Name	Description	Type	Reset Value
0:2	INFO_TYPE	Type of logged information 0b000 = Packet 0b001 = Reserved 0b010 = Short control symbol (only error capture register 0 is valid) 0b011 = Long control symbol (only error capture registers 0 and 1 are valid) 0b100 = Implementation-specific data is logged 0b101 = Reserved 0b110 = Undefined S-bit error 0b111 = Reserved	RW	0b000
3:7	ERR_TYPE	This is an encoded value representing the bit number in the Port {0..17} Error Detect CSR, which indicates the error that was captured. The actual bit numbering of the encoded value is 31 decimal minus “error detect bit position.”	RW	0x00
8:22	Reserved	Reserved	RO	0
23:27	IMP_DEP	Only valid if ERR_TYPE is set to represent bit 0 in the Port {0..17} Error Detect CSR; that is, ERR_TYPE = 0b11111. This field contains the bit number in the Port {0..17} Implementation Specific Error Detect Register which represents the error that was captured.	RW	0
28:30	Reserved	Reserved	RO	0
31	VALID	1 = The Capture registers contain valid information. For information on what is captured for which event, see Physical Layer Events.	RW	0

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10.7.12 Port {0..17} Capture 0 CSR

This register provides storage for capturing packets and long/short control symbols. For short control symbols, the full 32 bits are used because the delimited control symbol is captured.

The Port {0..17} Error Detect CSR and the Port {0..17} Capture 0 CSR–3, are writable by software to allow debug of the system error recovery and threshold method. For debug, software must write the Port {0..17} Attributes Capture CSR to set the VALID bit after writing the packet/control symbol information in the other capture registers.

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_CAPT_0_CSR Reset Value: 0x0000_00000	Register Offset: 0x00104C + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_0							
08:15	CAPT_0							
16:23	CAPT_0							
24:31	CAPT_0							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_0	4 Bytes of a delimited short Control Symbol, or Bytes 0:3 of a delimited long Control symbol, or Bytes 0:3 of the Packet Header. For control symbols, the most significant byte is the control symbol delimiting special character. Bit 22 indicates the type of timeout error: 0 = Package Acknowledge timeout 1 = Link-Response timeout	RW	0

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10.7.13 Port {0..17} Capture 1 CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_CAPT_1_CSR Reset Value: 0x0000_00000	Register Offset: 0x001050 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_1							
08:15	CAPT_1							
16:23	CAPT_1							
24:31	CAPT_1							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_1	Bytes 4:7 of a delimited long Control symbol, or Bytes 4:7 of the Packet Header. For long control symbols, the least significant byte is the control symbol delimiting special character.	RW	0

10.7.14 Port {0..17} Capture 2 CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_CAPT_2_CSR Reset Value: 0x0000_00000	Register Offset: 0x001054 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_2							
08:15	CAPT_2							
16:23	CAPT_2							
24:31	CAPT_2							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_2	Bytes 8:11 of the Packet Header	RW	0

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10.7.15 Port {0..17} Capture 3 CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_CAPT_3_CSR Reset Value: 0x0000_00000	Register Offset: 0x001058 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_3							
08:15	CAPT_3							
16:23	CAPT_3							
24:31	CAPT_3							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_3	Bytes 12:15 of the Packet Header	RW	0

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10.7.16 Port {0..17} Error Rate CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_ERR_RATE_CSR Reset Value: 0x8000_0000	Register Offset: 0x001068 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE_BIAS							
08:15	Reserved						ERR_RATE_REC	
16:23	PEAK_ERR_RATE							
24:31	ERR_RATE_CNTR							

Bits	Name	Description	Type	Reset Value
0:7	ERR_RATE_BIAS	The error rate bias value. 0x00 = Do not decrement the error rate counter 0x01 = Decrement every 1 ms (+/- 34%) 0x02 = Decrement every 10 ms (+/- 34%) 0x04 = Decrement every 100 ms (+/- 34%) 0x08 = Decrement every 1 s (+/- 34%) 0x10 = Decrement every 10 s (+/- 34%) 0x20 = Decrement every 100 s (+/- 34%) 0x40 = Decrement every 1000 s (+/- 34%) 0x80 = Decrement every 10000 s (+/- 34%)	RW	0x80
8:13	Reserved	Reserved	RO	0
14:15	ERR_RATE_REC	An increment limit to the error rate counter above the failed threshold. 0b00 = Only count 2 errors above 0b01 = Only count 4 error above 0b10 = Only count 16 errors above 0b11 = No limit	RW	0b00
16:23	PEAK_ERR_RATE	The peak value attained by the error rate counter. The primary intention for the writes is to clear the register (a write value of 0x00). This value does not clear on read.	RW	0

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Bits	Name	Description	Type	Reset Value
24:31	ERR_RATE_CNTR	A count of the events that have been detected and enabled as described in Event Detection. Note: A single packet or control symbol can cause multiple physical layer events to be detected. The leaky bucket counter is incremented by 1 for each erroneous control symbol and packet, regardless of the number of physical layer events detected in individual control symbols or packets. Note: IDT encourages caution when writing to this counter since the error threshold function is driven by it (if enabled). The primary intention for the writes is to clear the register (a write value of 0x00). This value does not clear on read.	RW	0

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10.7.17 Port {0..17} Error Rate Threshold CSR

For base address information, see Port Error Management Register Base Addresses.

Register Name: PORT_{0..17}_ERR_RATE_THRESH_CSR Reset Value: 0xFFFF_0000	Register Offset: 0x00106C + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	FAIL_THRESH							
08:15	DEGR_THRESH							
16:23	Reserved							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:7	FAIL_THRESH	The threshold trigger value for reporting an error condition due to a failed link. 0x00 = Disable the trigger 0x01 = Threshold value of 1 0x02 = Threshold value of 2 ... 0xFF = Threshold value of 255	RW	0xFF
8:15	DEGR_THRESH	The threshold trigger value for reporting an error condition due to a degrading link. 0x00 = Disable the trigger 0x01 = Threshold value of 1 0x02 = Threshold value of 2 ... 0xFF = Threshold value of 255	RW	0xFF
16:31	Reserved	Reserved	RO	0

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10.8 Lane Status Registers

Part 6 of the *RapidIO Specification (Rev. 2.1)* specifies a register extension block which contains status information and control values for each physical lane supported by a RapidIO device. These registers are defined in this section.

10.8.1 Lane {0..47} Status Base Addresses

Lane	Address
0	0x002010
1	0x002030
2	0x002050
3	0x002070
4	0x002090
5	0x0020B0
6	0x0020D0
7	0x0020F0
8	0x002110
9	0x002130
10	0x002150
11	0x002170
12	0x002190
13	0x0021B0
14	0x0021D0
15	0x0021F0
16	0x002210
17	0x002230
18	0x002250
19	0x002270
20	0x002290
21	0x0022B0
22	0x0022D0
23	0x0022F0
24	0x002310
25	0x002330
26	0x002350

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Lane	Address
27	0x002370
28	0x002390
29	0x0023B0
30	0x0023D0
31	0x0023F0
32	0x002410
33	0x002430
34	0x002450
35	0x002470
36	0x002490
37	0x0024B0
38	0x0024D0
39	0x0024F0
40	0x002510
41	0x002530
42	0x002550
43	0x002570
44	0x002590
45	0x0025B0
46	0x0025D0
47	0x0025F0

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10.8.2 Lane Status Block Header Register

For base address information, see Lane Status Registers.

Register Name: LANE_STATUS_BLK_HEAD Reset Value: 0x0000_0000D	Register Offset: 0x002000

Bits	0	1	2	3	4	5	6	7
00:07	EF_PTR							
08:15	EF_PTR							
16:23	EF_ID							
24:31	EF_ID							

Bits	Name	Description	Type	Reset Value
0:15	EF_PTR	Extended features pointer. This value points to the next entry in the extended features list. A value of 0x0000 indicates that this is the last entry.	RO	0
16:31	EF_ID	Hard Wired Extended Features ID	RO	0x000D

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10.8.3 Lane {0..47} Status 0 CSR

For base address information, see Lane Status Registers.

Register Name: LANE_{0..47}_STATUS_0_CSR Reset Value: Undefined	Register Offset: 0x002010 + (0x20 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	PORT							
08:15	LANE				TX_TYPE	TX_MODE	RX_TYPE	
16:23	RX_INVERT	RX_TRAINED	RX_LANE_SYNC	LP_RX_TRAINED	RX_LANE_RDY	ERR_8B10B		
24:31	ERR_8B10B	RX_SYNC_CHG	RX_TRAINED_CHG	Reserved	STATUS_1	STATUS_CSR		

Bits	Name	Description	Type	Reset Value
0:7	PORT	0x00 = Port 0 0x01 = Port 1 ... 0x11 = Port 17	RO	Undefined
8:11	LANE	The number of the lane within the port to which the transmitting lane is assigned. 0x0 = Lane 0 0x1 = Lane 1 0x2 = Lane 2 0x3 = Lane 3 All others are reserved.	RO	Undefined
12	TX_TYPE	0 = Short transmitter type 1 = Long transmitter type	FR	1
13	TX_MODE	0 = Short run transmitter mode 1 = Long run transmitter mode	RO	1
14:15	RX_TYPE	0b00 = Short run receiver type 0b01 = Medium run receiver type 0b10 = Long run receiver type 0b11 = Reserved	FR	0b10
16	RX_INVERT	0 = Receiver input not inverted 1 = Receiver input inverted	RO	0
17	RX_TRAINED	0 = Receiver not trained 1 = Receiver trained	RO	0

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Bits	Name	Description	Type	Reset Value
18	RX_LANE_SYNC	0 = Receiver lane not in sync 1 = Receiver lane in sync	RO	0
19	LP_RX_TRAINED	0 = Link partner receiver not trained 1 = Link partner receiver trained This bit represents the value state of the local far_rcvr_trained signal defined in *Part 6* of the *RapidIO Specification (Rev. 2.1)*.	RO	0
20	RX_LANE_RDY	Receiver Lane Ready 0 = Not ready 1 = Ready	RO	0
21:24	ERR_8B10B	A saturating count of 8b/10b decoding errors that have been detected for this lane since the field was last read. The field is reset to 0b0000 when the register is read.	RR	0b0000
25	RX_SYNC_CHG	Indicates whether the lane_sync signal for this lane has changed state since the bit was last read. The bit is reset to 0 when the register is read. 0 = The state of lane_sync did not change since the bit was last read. 1 = The state of lane_sync changed since the bit was last read.	RR	0
26	RX_TRAINED_CHG	Indicates whether the lane_ready signal for this lane has changed state since the bit was last read. The bit is reset to 0 when the register is read. 0 = The state of lane_ready did not change since the bit was last read. 1 = The state of lane_ready changed since the bit was last read.	RR	0
27	Reserved	Reserved	RO	0
28	STATUS_1	1 = Lane Status CSR 1 is implemented	RO	1
29:31	STATUS_CSR	Indicates which set of lane status registers (2 through 7) are implemented by the device 0b000 = None of the Lane Status CSRs 2:7 are implemented 0b001 = Lane Status CSR 2 is implemented 0b010 = Lane status CSRs 2:3 are implemented 0b011 = Lane status CSRs 2:4 are implemented 0b100 = Lane status CSRs 2:5 are implemented 0b101 = Lane status CSRs 2:6 are implemented 0b110 = Lane status CSRs 2:7 are implemented 0b111 = Reserved	RO	0b011

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10.8.4 Lane {0..47} Status 1 CSR

For base address information, see Lane Status Registers.

Register Name: LANE_{0..47}_STATUS_1_CSR Reset Value: 0x2000_0000	Register Offset: 0x002014 + (0x20 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	IDLE2_RX	CURRENT	VALUES_CHG	LP_RX_TYPE	LP_TRAINED	LP_PORT_WIDTH		
08:15	LP_LANE				LP_NEG1_TAP		LP_POS1_TAP	
16:23	LP_SCRAM	Reserved						
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0	IDLE2_RX	0 = No IDLE2 sequence has been received since the lane was last reset. 1 = An IDLE2 sequence has been received at some time since the lane was last reset.	RO	0
1	CURRENT	This field indicates whether the information in this register that is collected from the IDLE2 sequence is current. When asserted, this field indicates that the information is from the last IDLE2 CS Marker and CS field that were received by the lane without detected errors and that the lane's lane_sync signal has remained asserted since the last CS Marker and CS field was received. 0 = Not current 1 = Current	RO	0
2	VALUES_CHG	This field indicates whether the values of any of the other 31 bits in this register have changed since the register was last read. This bit is set to zero when the register is read. 0 = Values have not changed 1 = Values have changed	RR	1
3	LP_RX_TYPE	Link Partner Receiver Type 0 = Short run 1 = Medium or long run	RO	0

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Bits	Name	Description	Type	Reset Value
4	LP_TRAINED	Link Partner Lane Receiver Trained 0 = Not trained 1 = Trained The value of this bit represents the latest updated value received in the IDLE2 CS_Field bit “receiver trained” from the link partner.	RO	0
5:7	LP_PORT_WIDTH	Link Partner Port Width 0b000 = 1x mode 0b001 = 2x mode 0b010 = 4x mode 0b011 = 8x mode (RapidIO standard support) 0b100 = 16x mode (RapidIO standard support) All others are reserved.	RO	0b000
8:11	LP_LANE	Receiver lane number of the link partner port detected in IDLE2 (these bits do not apply in IDLE1). 0x0 = Lane 0 0x1 = Lane 1 0x2 = Lane 2 0x3 = Lane 3	RO	0
12:13	LP_NEG1_TAP	Link Partner Emphasis Status Tap (Negative 1) 0b00 = Tap not implemented 0b01 = Tap at minimum emphasis 0b10 = Tap at maximum emphasis 0b11 = Tap at intermediate emphasis	RO	0b00
14:15	LP_POS1_TAP	Link Partner Emphasis Status Tap (Positive 1) 0b00 = Tap not implemented 0b01 = Tap at minimum emphasis 0b10 = Tap at maximum emphasis 0b11 = Tap at intermediate emphasis	RO	0b00
16	LP_SCRAM	Link Partner Scrambling/Descrambling 0 = Disable 1 = Enable	RO	0
17:31	Reserved	Reserved	RO	0

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10.8.5 Lane {0..47} Status 2 CSR

For base address information, see Lane Status Registers.



This register controls transmitter emphasis values which are a part of IDLE2 signal quality optimization. Control of transmitter emphasis values using IDLE2 is not supported.

Register Name: LANE_{0..47}_STATUS_2_CSR Reset Value: 0x0000_0000	Register Offset: 0x002018 + (0x20 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				NEG1_ON_PRE			
08:15	NEG1_ON_PRE	Reserved			POS1_ON_PRE			
16:23	POS1_ON_PRE	Reserved			NEG1_ON_RST			
24:31	Reserved		POS1_ON_RST					

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4:8	NEG1_ON_PRE	Value to set the -1 (pre) tap to when a preset pre-emphasis command in an IDLE2 sequence is received.	RW	0
9:10	Reserved	Reserved	RO	0
11:16	POS1_ON_PRE	Value to set the +1 (post) tap to when a preset pre-emphasis command in an IDLE2 sequence is received.	RW	0
17:18	Reserved	Reserved	RO	0
19:23	NEG1_ON_RST	Value to set the -1 (pre) tap to when a reset pre-emphasis command in an IDLE2 sequence is received.	RW	0
24:25	Reserved	Reserved	RO	0
26:31	POS1_ON_RST	Value to set the +1 (post) tap to when a reset pre-emphasis command in an IDLE2 sequence is received.	RW	0

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10.8.6 Lane {0..47} Status 3 CSR

For base address information, see Lane Status Registers.

Register Name: LANE_{0..47}_STATUS_3_CSR Reset Value: 0xDFF8_0000	Register Offset: 0x00201C + (0x20 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	UNUSED	Reserved	AMP_PROG_EN	GBAUD_1p25	GBAUD_2p5	GBAUD_3p125	GBAUD_5	GBAUD_6p25
08:15	GBAUD_1p25_EN	GBAUD_2p5_EN	GBAUD_3p125_EN	GBAUD_5_EN	GBAUD_6p25_EN	NEG1_CMD		
16:23	NEG1_CMD	POS1_CMD				NEG1_TAP		
24:31	NEG1_TAP	POS1_TAP						

Bits	Name	Description	Type	Reset Value
0	UNUSED	Reserved	RW	1
1	Reserved	Reserved	RO	1
2	AMP_PROG_EN	Local Transmitter Amplitude Control Enable Setting this bit enables local control of the Lane {0..47} Control Register.TX_AMP_CTL field. 0 = User cannot change the transmitter's output amplitude level 1 = User can change the transmitter's output amplitude level	RW	0
3	GBAUD_1p25	0 = Not supported 1 = Supported	RO	1
4	GBAUD_2p5	0 = Not supported 1 = Supported	RO	1
5	GBAUD_3p125	0 = Not supported 1 = Supported	RO	1
6	GBAUD_5	0 = Not supported 1 = Supported	RO	1
7	GBAUD_6p25	0 = Not supported 1 = Supported	RO	1
8	GBAUD_1p25_EN	0 = Not supported 1 = Supported	RO	1

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Bits	Name	Description	Type	Reset Value
9	GBAUD_2p5_EN	0 = Not supported 1 = Supported	RO	1
10	GBAUD_3p125_EN	0 = Not supported 1 = Supported	RO	1
11	GBAUD_5_EN	0 = Not supported 1 = Supported	RO	1
12	GBAUD_6p25_EN	0 = Not supported 1 = Supported	RO	1
13:16	NEG1_CMD	Local Pre-emphasis Command 0x0 = No command 0x1 = Reset remote pre-emphasis 0x2 = Preset remote pre-emphasis 0x3 = Increment +1 tap 0x4 = Decrement +1 tap 0x5 = Increment -1 tap 0x6 = Decrement -1 tap All others are reserved.	WO	0
17:20	POS1_CMD	Local Pre-emphasis Command 0x0 = No command 0x1 = Reset local pre-emphasis 0x2 = Preset local pre-emphasis 0x3 = Increment +1 tap 0x4 = Decrement +1 tap 0x5 = Increment -1 tap 0x6 = Decrement -1 tap All others are reserved.	WO	0
21:25	NEG1_TAP	Local Transmitter Pre-emphasis Tap Control. Current value of the -1 (pre) tap	RW	0
26:31	POS1_TAP	Local Transmitter Post Tap Control. Current value of the +1 (post) tap	RW	0

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10.8.7 Lane {0..47} Status 4 CSR

For base address information, see Lane Status Registers.

Register Name: LANE_{0..47}_STATUS_4_CSR Reset Value: 0x8001_1388	Register Offset: 0x002020 + (0x20 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	UNUSED	Reserved						
08:15	Reserved						CC_MONITOR_STATUS	CC_MONITOR_EN
16:23	CC_MONITOR_THRESH							
24:31	CC_MONITOR_THRESH							

Bits	Name	Description	Type	Reset Value
0	UNUSED	Reserved	RW	1
1:13	Reserved	Reserved	RO	0
14	CC_MONITOR_STATUS	1 = Clock Compensation Monitor failed to receive a valid RR sequence within CC_MONITOR_THRESH character groups	RO	0
15	CC_MONITOR_EN	0 = Disable Clock Compensation Sequence Monitor 1 = Enable Clock Compensation Sequence Monitor	RW	1
16:31	CC_MONITOR_THRESH	The number of character groups to be used as a threshold for the reception of a valid RR sequence. The default value is 5000 character groups. Note: Do not write 0 to this field.	RW	0x1388

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10.9 IDT Specific Miscellaneous Registers

10.9.1 Route Port Select Register

Register Name: RTE_PORT_SEL Reset Value: 0x0000_0000	Register Offset: 0x010070

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved				PORT			

Bits	Name	Description	Type	Reset Value
0:26	Reserved	Reserved	RO	0
27:31	PORT	Defines the port whose route table is affected when a write to or a read from the Standard Route Table Entry Configuration Port Select CSR 0b00000 = Broadcast access to all Port Route Table 0b00001 = Access is for Port 0 Route Table 0b00010 = Access is for Port 1 Route Table 0b00011 = Access is for Port 2 Route Table 0b00100 = Access is for Port 3 Route Table 0b00101 = Access is for Port 4 Route Table 0b00110 = Access is for Port 5 Route Table 0b00111 = Access is for Port 6 Route Table 0b01000 = Access is for Port 7 Route Table 0b01001 = Access is for Port 8 Route Table 0b01010 = Access is for Port 9 Route Table 0b01011 = Access is for Port 10 Route Table 0b01100 = Access is for Port 11 Route Table 0b01101 = Access is for Port 12 Route Table 0b01110 = Access is for Port 13 Route Table 0b01111 = Access is for Port 14 Route Table 0b10000 = Access is for Port 15 Route Table 0b10001 = Access is for Port 16 Route Table 0b10010 = Access is for Port 17 Route Table All other values are undefined.	RW	0b00000

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10.9.2 Multicast Route Select Register

Register Name: MCAST_RTE_SEL Reset Value: 0x0000_0000	Register Offset: 0x010080

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved				PORT			

Bits	Name	Description	Type	Reset Value
0:26	Reserved	Reserved	RO	0
27:31	PORT	Defines the port whose route table is affected when writes to or reads from the Multicast Mask Port CSR, Multicast Association Selection CSR, and Multicast Association Operations CSR, are received. 0b00000 = Broadcast access to all Port Route Table 0b00001 = Access is for Port 0 Route Table 0b00010 = Access is for Port 1 Route Table 0b00011 = Access is for Port 2 Route Table 0b00100 = Access is for Port 3 Route Table 0b00101 = Access is for Port 4 Route Table 0b00110 = Access is for Port 5 Route Table 0b00111 = Access is for Port 6 Route Table 0b01000 = Access is for Port 7 Route Table 0b01001 = Access is for Port 8 Route Table 0b01010 = Access is for Port 9 Route Table 0b01011 = Access is for Port 10 Route Table 0b01100 = Access is for Port 11 Route Table 0b01101 = Access is for Port 12 Route Table 0b01110 = Access is for Port 13 Route Table 0b01111 = Access is for Port 14 Route Table 0b10000 = Access is for Port 15 Route Table 0b10001 = Access is for Port 16 Route Table 0b10010 = Access is for Port 17 Route Table All other values are undefined.	RW	0b00000

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10.9.3 Port n Watermarks Base Addresses

Port	Offset from Base
0	0x011000
1	0x011010
2	0x011020
3	0x011030
4	0x011040
5	0x011050
6	0x011060
7	0x011070
8	0x011080
9	0x011090
10	0x0110A0
11	0x0110B0
12	0x0110C0
13	0x0110D0
14	0x0110E0
15	0x0110F0
16	0x011100
17	0x011110

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10.9.4 Port {0..17} Watermarks Register

The watermark values in this register should be set based on the buffer size of the link partner and the required traffic characteristics for packets of each priority. For more information, see Transmitter- and Receiver-Controlled Flow Control Programming Model.

For base address information, see Port n Watermarks Base Addresses. The broadcast version of this register is Broadcast Watermarks Register.

Register Name: PORT_{0..17}_WM Reset Value: 0x0000_20C4	Register Offset: 0x011000 + (0x10 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved						PRIO_2	
16:23	PRIO_2				PRIO_1			
24:31	PRIO_1		PRIO_0					

Bits	Name	Description	Type	Reset Value
0:13	Reserved	Reserved	RO	0
14:19	PRIO_2	Value of Watermark 2 (WM2) for transmitter-controlled flow control functionality.[a]	RW	0x02
20:25	PRIO_1	Value of Watermark 1 (WM1) for transmitter-controlled flow control functionality.[a]	RW	0x03
26:31	PRIO_0	Value of Watermark 0 (WM0) for transmitter-controlled flow control functionality.[a]	RW	0x04

a. As defined in the *RapidIO Specification (Rev. 2.1)*.

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10.9.5 Broadcast Watermarks Register

The per-port version of this register is Port {0..17} Watermarks Register.

Register Name: BCAST_WM Reset Value: 0x0000_0000	Register Offset: 0x01F000

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved						PRIO_2	
16:23	PRIO_2				PRIO_1			
24:31	PRIO_1		PRIO_0					

Bits	Name	Description	Type	Reset Value
0:13	Reserved	Reserved	RO	0
14:19	PRIO_2	Value of Watermark 2 (WM2) for transmitter-controlled flow control functionality.[a]	RW	0
20:25	PRIO_1	Value of Watermark 1 (WM1) for transmitter-controlled flow control functionality.[a]	RW	0
26:31	PRIO_0	Value of Watermark 0 (WM0) for transmitter-controlled flow control functionality.[a]	RW	0

a. As defined in the *RapidIO Specification (Rev. 2.1)*.

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10.10 IDT Specific Event Notification Control Registers

The CPS-1848 supports a number of RapidIO related implementation-specific event detection/notification functions, as well as event detection/notification for the JTAG (CPS-1848 Revision A/B only) and I2C interfaces on the device. These registers report the status of and contain control values for this functionality.

10.10.1 Aux Port Error Capture Enable Register

This register enables the capture of I^2C events.

Register Name: AUX_PORT_ERR_CAPT_EN Reset Value: 0x0000_0000	Register Offset: 0x020000

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved		JTAG_ERR_EN	I2C_CHKSUM_ERR_EN	UNEXP_START_STOP_EN	I2C_ADDR_ERR_EN	I2C_ACK_ERR_EN	I2C_LENGTH_ERR_EN

Bits	Name	Description	Type	Reset Value
0:25	Reserved	Reserved	RO	0
26	JTAG_ERR_EN	0 = Disable 1 = Enable JTAG incomplete write error capture Note: This bit is applicable to CPS-1848 Revision A/B only.	RW	0
27	I2C_CHKSUM_ERR_EN	0 = Disable 1 = Enable I2C EPROM checksum error capture	RW	0
28	UNEXP_START_STOP_EN	0 = Disable 1 = Enable I2C unexpected start/stop error capture	RW	0
29	I2C_ADDR_ERR_EN	0 = Disable 1 = Enable I2C memory address incomplete error capture	RW	0
30	I2C_ACK_ERR_EN	0 = Disable 1 = Enable I2C acknowledge error capture	RW	0
31	I2C_LENGTH_ERR_EN	0 = Disable 1 = Enable I2C length error capture	RW	0

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10.10.2 Aux Port Error Detect Register

This register detects I^2C events.

Register Name: AUX_PORT_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0x020004

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved		JTAG_ERR	I2C_CHKSUM_ERR	UNEXP_START_STOP	I2C_ADDR_ERR	I2C_ACK_ERR	I2C_LENGTH_ERR

Bits	Name	Description	Type	Reset Value
0:25	Reserved	Reserved	RO	0
26	JTAG_ERR	0 = No error 1 = An unexpected termination of write data to registers was detected if serial data input is not 32-bit aligned. Note: This bit is applicable to CPS-1848 Revision A/B only.	RW	0
27	I2C_CHKSUM_ERR	0 = No error 1 = In Master mode, at the end of a configuration image update, the checksum value in the image did not match the calculated value.	RW	0
28	UNEXP_START_STOP	0 = No error 1 = As a slave, the device has encountered an unexpected START or STOP. When this occurs during addressing or during a memory address transfer the operation is aborted. When this occurs after memory address transfer is complete (but before data transfer is complete) the memory address counter is updated, but the memory access will be aborted.	RW	0
29	I2C_ADDR_ERR	0 = No error 1 = An unexpected START/STOP was seen before all three bytes of a memory address are received. This occurs when the device is in slave mode and being addressed by the Master I2C device. The memory address is not updated, and the write operation is aborted.	RW	0

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Bits	Name	Description	Type	Reset Value
30	I2C_ACK_ERR	0 = No error 1 = An acknowledgement was expected but not received. This error can occur in Master or Slave mode. If the error occurs in Master mode, the data transfer will be terminated and the error will be captured.	RW	0
31	I2C_LENGTH_ERR	0 = No error 1 = I2C transmission has an invalid data payload length (read or write transaction)	RW	0

10.10.3 Configuration Block Error Capture Enable Register

Register Name: CFG_ERR_CAPT_EN Reset Value: 0x0000_0000	Register Offset: 0x020008

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved			BAD_MCAST_EN	BAD_RTE_EN	RTE_FORCE_EN	BAD_PORT_EN	BAD_MASK_EN

Bits	Name	Description	Type	Reset Value
0:26	Reserved	Reserved	RO	0
27	BAD_MCAST_EN	0 = Disable 1 = Enable multicast translation error capture	RW	0
28	BAD_RTE_EN	0 = Disable 1 = Enable route table configuration error capture	RW	0
29	RTE_FORCE_EN	0 = Disable 1 = Enable force local configuration error capture	RW	0
30	BAD_PORT_EN	0 = Disable 1 = Enable port configuration error capture	RW	0
31	BAD_MASK_EN	0 = Disable 1 = Enable multicast mask configuration error capture	RW	0

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10.10.4 Configuration Block Error Detect Register

Register Name: CFG_ERR_DET Reset Value: 0x0000_0000	Register Offset:0x020010

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved			BAD_MCAST	BAD_RTE	RTE_FORCE	BAD_PORT	BAD_MASK

Bits	Name	Description	Type	Reset Value
0:26	Reserved	Reserved	RO	0
27	BAD_MCAST	0 = No error 1 = User has accessed a multicast register and a bit is high that does not correspond to a valid port on the device. The write will still occur, and any other valid ports will be changed.	RW	0
28	BAD_RTE	0 = No error 1 = A route table (or pointer table) has been read and its value reference results in an illegal port value. A value of 8'ff will be returned to the user to indicate a failure occurred.	RW	0
29	RTE_FORCE	0 = No error 1 = A FORCE_LOCAL value was used in an attempt to program the Device Route Table. A NO_RTE will be written into the Device Route Table instead.	RW	0
30	BAD_PORT	0 = No error 1 = A direct write to a route table is attempted with an invalid PORT number. A NO_RTE will be written into the route table instead. This is also triggered when the Multicast Mask Port CSR is written to that contains an invalid egress port number. or An attempt has been made to configure the CPS-1848 to use an invalid trace port.	RW	0

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Bits	Name	Description	Type	Reset Value
31	BAD_MASK	0 = No error 1 = A direct write to a route table has been attempted with an invalid mask number. A NO_RTE will be written into the route table instead. or The user has attempted to program the Domain Route Table with a multicast mask number. or The Multicast Mask Port CSR was written to with an invalid mask. or The Multicast Association Selection CSR was written to with an invalid mask number. or A write-to-verify command in the Multicast Association Operations CSR has resulted in an access to the Domain Route Table. This is because the Domain Route Table can only store ports and no-routes (not multicast masks). or A read of an invalid address has been attempted.	RW	0

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10.10.5 Impl. Specific Logical/Transport Layer Address Capture Register

The contents of this register are unlocked simultaneously with the values in the Logical/Transport Layer Error Detect CSR.

Register Name: IMPL_SPEC_LT_ADDR_CAPT Reset Value: 0x0000_0000	Register Offset: 0x021014

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved		LT_ADDR					
16:23	LT_ADDR							
24:31	LT_ADDR							

Bits	Name	Description	Type	Reset Value
0:9	Reserved	Reserved	RO	0
10:31	LT_ADDR	Concatenation of the CFG_OFFSET field and the WTR field for Maintenance transactions.	RW	0

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10.10.6 Logical/Transport Layer Error Report Enable Register

The same settings should be used in the Logical/Transport Layer Error Enable CSR and this register; otherwise, detected events may not be reported, or port-writes/interrupts may be sent/asserted with no indication of the cause.

Register Name: LT_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x03100C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				ILL_TRAN_EN	Reserved		
08:15	UNSOL_RESP_EN	UNSUP_TRAN_EN	Reserved					
16:23	Reserved							
24:31	IMP_SPEC_ERR_EN							

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4	ILL_TRAN_EN	1 = Enable the reporting of the corresponding error in the Logical/Transport Layer Error Detect CSR.	RW	0
5:7	Reserved	Reserved	RO	0
8	UNSOL_RESP_EN	1 = Enable the reporting of the corresponding error in the Logical/Transport Layer Error Detect CSR.	RW	0
9	UNSUP_TRAN_EN	1 = Enable the reporting of the corresponding error in the Logical/Transport Layer Error Detect CSR.	RW	0
10:23	Reserved	Reserved	RO	0
24:31	IMP_SPEC_ERR_EN	1 = Enable the reporting of the corresponding error in the Logical/Transport Layer Error Detect CSR.	RW	0

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10.10.7 Port {0..17} Error Report Enable Base Addresses

Port	Base Address
0	0x031044
1	0x031084
2	0x0310C4
3	0x031104
4	0x031144
5	0x031184
6	0x0311C4
7	0x031204
8	0x031244
9	0x031284
10	0x0312C4
11	0x031304
12	0x031344
13	0x031384
14	0x0313C4
15	0x031404
16	0x031444
17	0x031484

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10.10.8 Port {0..17} Error Report Enable Register

Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. The broadcast version of this register is Broadcast Port Error Report Enable Register. For base address information, see Port {0..17} Error Report Enable Base Addresses.



Hot Extraction/Insertion support requires exclusive use of these registers. No Standard Physical Layer Errors can be enabled when Hot Extraction/Insertion functionality is required.

Register Name: PORT_{0..17}_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x031044 + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR_EN	Reserved						
08:15	Reserved	CS_CRC_ERR_EN	UNEXP_ACKID_EN	CS_NOT_ACC_EN	PKT_ILL_ACKID_EN	PKT_CRC_ERR_EN	PKT_ILL_SIZE_EN	Reserved
16:23	IDLE1_ERR_EN	Reserved						
24:31	Reserved		LR_ACKID_ILL_EN	PRTCL_ERR_EN	Reserved	DELIN_ERR_EN	CS_ACK_ILL_EN	LINK_TIMEOUT_EN

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
10	UNEXP_ACKID_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
11	CS_NOT_ACC_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
12	PKT_ILL_ACKID_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
13	PKT_CRC_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
14	PKT_ILL_SIZE_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
15	Reserved	Reserved	RO	0

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Bits	Name	Description	Type	Reset Value
16	IDLE1_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
17:25	Reserved	Reserved	RO	0
26	LR_ACKID_ILL_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
27	PRTCL_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
30	CS_ACK_ILL_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0
31	LINK_TIMEOUT_EN	1 = Enable the reporting of the corresponding error in the Port {0..17} Error Detect CSR.	RW	0

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10.10.9 Port {0..17} Implementation Specific Error Report Enable Register

This register allows the user to define when an implementation specific error is captured at a finer granularity. Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. The broadcast version of this register is Broadcast Port Implementation Specific Error Report Enable Register.

Register Name: PORT_{0..17}_IMPL_SPEC_ERR_RPT_EN Reset Value: 0xFF7F_FFFF	Register Offset: 0x03104C + (0x40 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE_EN	TTL_EVENT_EN	CRC_EVENT_EN	PNA_EN	UNSOL_LR_EN	UNEXP_ACKID_EN	PNA_RETRY_EN	RTE_ISSUE_EN
08:15	Reserved	SET_ACKID_EN	TX_DROP_EN	MANY_RETRY_EN	RX_DROP_EN	Reserved	BAD_TT_EN	SHORT_EN
16:23	UNSOL_RFR_EN	FATAL_TO_EN	RETRY_EN	RETRY_ACKID_EN	STOMP_TO_EN	RX_STOMP_EN	LR_CMD_EN	LR_X2_EN
24:31	UNEXP_EOP_EN	UNEXP_STOMP_EN	PORT_INIT_EN	PORT_WIDTH_EN	IDLE_IN_PKT_EN	LOA_EN	BAD_CTL_EN	REORDER_EN

Bits	Name	Description	Type	Reset Value
0	ERR_RATE_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
1	TTL_EVENT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
2	CRC_EVENT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
3	PNA_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
4	UNSOL_LR_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
5	UNEXP_ACKID_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
6	PNA_RETRY_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
7	RTE_ISSUE_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
8	Reserved	Reserved	RO	0
9	SET_ACKID_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1

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Bits	Name	Description	Type	Reset Value
10	TX_DROP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
11	MANY_RETRY_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
12	RX_DROP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
13	Reserved	Reserved	RW	1
14	BAD_TT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
15	SHORT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
16	UNSOL_RFR_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
17	FATAL_TO_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
18	RETRY_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
19	RETRY_ACKID_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
20	STOMP_TO_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
21	RX_STOMP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
22	LR_CMD_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
23	LR_X2_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
24	UNEXP_EOP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
25	UNEXP_STOMP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
26	PORT_INIT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
27	PORT_WIDTH_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1

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Bits	Name	Description	Type	Reset Value
28	IDLE_IN_PKT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
29	LOA_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
30	BAD_CTL_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1
31	REORDER_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	1

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10.10.10 Broadcast Port Error Report Enable Register

Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. The per-port version of this register is Port {0..17} Error Report Enable Register.

Register Name: BCAST_PORT_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x03FF04

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR_EN	Reserved						
08:15	Reserved	CS_CRC_ERR_EN	UNEXP_ACKID_EN	CS_NOT_ACC_EN	PKT_ILL_ACKID_EN	PKT_CRC_ERR_EN	PKT_ILL_SIZE_EN	Reserved
16:23	IDLE1_ERR_EN	Reserved						
24:31	Reserved		LR_ACKID_ILL_EN	PRTCL_ERR_EN	Reserved	DELIN_ERR_EN	CS_ACK_ILL_EN	LINK_TIMEOUT_EN

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
10	UNEXP_ACKID_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
11	CS_NOT_ACC_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
12	PKT_ILL_ACKID_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
13	PKT_CRC_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
14	PKT_ILL_SIZE_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
15	Reserved	Reserved	RO	0
16	IDLE1_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
17:25	Reserved	Reserved	RO	0

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Bits	Name	Description	Type	Reset Value
26	LR_ACKID_ILL_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
27	PRTCL_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
30	CS_ACK_ILL_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0
31	LINK_TIMEOUT_EN	1 = Enable the reporting of errors to the corresponding bit in the Port {0..17} Error Detect CSR.	RW	0

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10.10.11 Broadcast Port Implementation Specific Error Report Enable Register

Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. The per-port version of this register is Port {0..17} Implementation Specific Error Report Enable Register.

Register Name: BCAST_PORT_IMPL_SPEC_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x03FF0C

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE_EN	TTL_EVENT_EN	CRC_EVENT_EN	PNA_EN	UNSOL_LR_EN	UNEXP_ACKID_EN	PNA_RETRY_EN	RTE_ISSUE_EN
08:15	Reserved	SET_ACKID_EN	TX_DROP_EN	MANY_RETRY_EN	RX_DROP_EN	Reserved	BAD_TT_EN	SHORT_EN
16:23	UNSOL_RFR_EN	FATAL_TO_EN	RETRY_EN	RETRY_ACKID_EN	STOMP_TO_EN	RX_STOMP_EN	LR_CMD_EN	LR_X2_EN
24:31	UNEXP_EOP_EN	UNEXP_STOMP_EN	PORT_INIT_EN	PORT_WIDTH_EN	IDLE_IN_PKT_EN	LOA_EN	BAD_CTL_EN	REORDER_EN

Bits	Name	Description	Type	Reset Value
0	ERR_RATE_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
1	TTL_EVENT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
2	CRC_EVENT_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
3	PNA_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
4	UNSOL_LR_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
5	UNEXP_ACKID_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
6	PNA_RETRY_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
7	RTE_ISSUE_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
8	Reserved	Reserved	RO	0
9	SET_ACKID_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0
10	TX_DROP_EN	1 = Enable reporting of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register	RW	0

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(Continued)

Bits	Name	Description	Type	Reset Value
11	MANY_RETRY_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
12	RX_DROP_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
13	Reserved	Reserved	RW	0
14	BAD_TT_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
15	SHORT_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
16	UNSOL_RFR_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
17	FATAL_TO_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
18	RETRY_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
19	RETRY_ACKID_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
20	STOMP_TO_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
21	RX_STOMP_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
22	LR_CMD_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
23	LR_X2_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
24	UNEXP_EOP_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
25	UNEXP_STOMP_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
26	PORT_INIT_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
27	PORT_WIDTH_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
28	IDLE_IN_PKT_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
29	LOA_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0

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(Continued)

Bits	Name	Description	Type	Reset Value
30	BAD_CTL_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0
31	REORDER_EN	1 = Enable reporting of the corresponding error in the Broadcast Port Implementation Specific Error Detect Register	RW	0

10.10.12 Lane n Error Report Enable Base Addresses

Lane	Base Address
0	0x038010
1	0x038110
2	0x038210
3	0x038310
4	0x038410
5	0x038510
6	0x038610
7	0x038710
8	0x038810
9	0x038910
10	0x038A10
11	0x038B10
12	0x038C10
13	0x038D10
14	0x038E10
15	0x038F10
16	0x039010
17	0x039110
18	0x039210
19	0x039310
20	0x039410
21	0x039510
22	0x039610
23	0x039710
24	0x039810

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Lane	Base Address
25	0x039910
26	0x039A10
27	0x039B10
28	0x039C10
29	0x039D10
30	0x039E10
31	0x039F10
32	0x03A010
33	0x03A110
34	0x03A210
35	0x03A310
36	0x03A410
37	0x03A510
38	0x03A610
39	0x03A710
40	0x03A810
41	0x03A910
42	0x03AA10
43	0x03AB10
44	0x03AC10
45	0x03AD10
46	0x03AE10
47	0x03AF10

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10.10.13 Lane {0..47} Error Report Enable Register

Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. For base address information, see Lane n Error Report Enable Base Addresses. The broadcast version of this register is Broadcast Lane Error Report Enable Register. For more information on the use of this register, see Event Notification.

Hot Extraction/Insertion support requires exclusive use of these registers. No Standard Physical Layer Errors can be enabled when Hot Extraction/Insertion functionality is required.

Register Name: LANE_{0..47}_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x038010 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED_EN	LANE_INVER_DET_EN
24:31	IDLE2_FRAME_EN	Reserved		TX_RX_MISMATCH_EN	DESCRAM_SYNC_EN	BAD_CHAR_EN	LANE_RDY_EN	LANE_SYNC_EN

Bits	Name	Description	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
23	LANE_INVER_DET_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
24	IDLE2_FRAME_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
28	DESCRAM_SYNC_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
29	BAD_CHAR_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
30	LANE_RDY_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
31	LANE_SYNC_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0

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10.10.14 Broadcast Lane Error Report Enable Register

Each bit in this register can enable/disable reporting of an error type using interrupt, port-write, and error log. The per-port version of this register is Lane {0..47} Error Report Enable Register. For more information, see Lane Event Notification.

Register Name: BCAST_LANE_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0x03FF10

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED_EN	LANE_INVER_DET_EN
24:31	IDLE2_FRAME_EN	Reserved		TX_RX_MISMATCH_EN	DESCRAM_SYNC_EN	BAD_CHAR_EN	LANE_RDY_EN	LANE_SYNC_EN

Bits	Name	Description	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
23	LANE_INVER_DET_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
24	IDLE2_FRAME_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
28	DESCRAM_SYNC_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
29	BAD_CHAR_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
30	LANE_RDY_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0
31	LANE_SYNC_EN	1 = Enable reporting of the corresponding error in the Lane {0..47} Error Detect Register.	RW	0

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10.11 Packet Generation and Capture Registers

For more information on how to use these registers, see Packet Generation and Capture.

10.11.1 Packet Generation and Capture Base Addresses

Port	Address
0	0x100100
1	0x100110
2	0x100120
3	0x100130
4	0x100140
5	0x100150
6	0x100160
7	0x100170
8	0x100180
9	0x100190
10	0x1001A0
11	0x1001B0
12	0x1001C0
13	0x1001D0
14	0x1001E0
15	0x1001F0
16	0x100200
17	0x100210

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10.11.2 Port {0..17} Packet Generation and Capture Mode Configuration Register

For base address information, see Packet Generation and Capture Base Addresses.

Register Name: PORT_{0..17}_PGC_MODE Reset Value: 0x0000_0000	Register Offset: 0x100100 + (0x10 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							START
16:23	RX_DONE	EN	END_PORT	START_PORT	EOP	SOP	FLOW_TYPE	
24:31	FLOW_TYPE							

Bits	Name	Description	Type	Reset Value
0:14	Reserved	Reserved	RO	0
15	START	1 = Start the data transmission from the Start port to End port.	RW	0
16	RX_DONE	The transmitted packet is ready to be read from the destination port's Final Buffer.	RO	0
17	EN	1 = Enable data structure access for internal data structure. Write access for the Start port. Read access for End port.	RW	0
18	END_PORT	0 = This port is not the End port for the PGC test. 1 = This port is the End port for the PGC test.	RW	0
19	START_PORT	0 = This port is not the Start port for the PGC test. 1 = This port is the Start port for the PGC test.	RW	0
20	EOP	0 = This data word does not represent the last word in a PGC packet. 1 = This data word represents the last word in a PGC packet.	RW	0
21	SOP	0 = This data word does not represent the first word in a PGC packet. 1 = This data word represents the first word in a PGC packet.	RW	0
22:31	FLOW_TYPE	0b0000000001 = VC0 PRI 0 CRF 0 0b0000000010 = VC0 PRI 0 CRF 1 0b0000000100 = VC0 PRI 1 CRF 0 0b0000001000 = VC0 PRI 1 CRF 1 0b0000010000 = VC0 PRI 2 CRF 0 0b0000100000 = VC0 PRI 2 CRF 1 0b0001000000 = VC0 PRI 3 CRF 0 0b0010000000 = VC0 PRI 3 CRF 1	RW	0

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10.11.3 Port {0..17} Packet Generation and Capture Mode Data Register

For base address information, see Packet Generation and Capture Base Addresses.

Register Name: PORT_{0..17}_PGC_DATA Reset Value: 0x0000_0000	Register Offset: 0x100104 + (0x10 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	DATA							
08:15	DATA							
16:23	DATA							
24:31	DATA							

Bits	Name	Description	Type	Reset Value
0:31	DATA	This field is used to write packets to the Start port, and to retrieve packets from the End port. For more information, see Packet Generation and Capture.	RW	0x0

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10.12 IDT Specific Routing Table Registers

The CPS-1848 supports a memory-mapped model for routing table registers. The “broadcast” versions of these registers update routing tables for all ports. The “per-port” versions of these registers are port specific.

10.12.1 Base Addresses for IDT Specific Routing Table Registers

Port	Device Table Base Address	Domain Table Base Address
Broadcast	0xE00000	0xE00400
0	0xE10000	0xE10400
1	0xE11000	0xE11400
2	0xE12000	0xE12400
3	0xE13000	0xE13400
4	0xE14000	0xE14400
5	0xE15000	0xE15400
6	0xE16000	0xE16400
7	0xE17000	0xE17400
8	0xE18000	0xE18400
9	0xE19000	0xE19400
10	0xE1A000	0xE1A400
11	0xE1B000	0xE1B400
12	0xE1C000	0xE1C400
13	0xE1D000	0xE1D400
14	0xE1E000	0xE1E400
15	0xE1F000	0xE1F400
16	0xE20000	0xE20400
17	0xE21000	0xE21400

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10.12.2 Broadcast Device Route Table Register {0..255}

This is the broadcast device routing register for destID 0–255. The per-port version of this register is Port {0..17} Device Route Table Register {0..255}.

Register Name: BCAST_DEV_RTE_TABLE_{0..255} Reset Value: 0x0000_00DE	Register Offset: 0xE00000 + (0x4 * DestID)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	PORT	0x00–0x11 = Output Port Number 0x40–0x68 = Multicast Mask Number 0xDD = The packet is discarded and the routing table entry is overwritten with a value of 0xDF. 0xDE = Use Default Port Route, as set in Standard Route Table Entry Default Port CSR 0xDF = No Route, discard packets All other values are reserved and result in packet discard. Note: For more information, see Table 1.	RW	0xDE

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10.12.3 Broadcast Domain Route Table Register {0..255}

This is the broadcast domain routing register for destID 0–255. The per-port version of this register is Port {0..17} Domain Routing Table Register {0..255}.

Register Name: BCAST_DOM_RTE_TABLE_{0..255} Reset Value: 0x0000_00DE	Register Offset: 0xE00400 + (0x4 * DestID)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	PORT	0x00–0x11 = Output Port Number 0xDD = Use Device Routing Table; valid in Domain Routing Table only 0xDE = Use Default Route 0xDF = No Route, discard packets All other values are reserved and result in packet discard.	RW	0xDE

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10.12.4 Port {0..17} Device Route Table Register {0..255}

This is the port-specific device routing register for destID 0–255. The broadcast version of this register is Broadcast Device Route Table Register {0..255}

Register Name: PORT_{0..17}_DEV_RTE_TABLE_{0..255} Reset Value: 0x0000_00DE	Register Offset: 0xE10000 + (0x1000 * port_num) + (0x4 * DestID)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	PORT	0x00–0x11 = Output Port Number 0x40–0x68 = Multicast Mask Number 0xDE = Use Default Port Route, as set in Standard Route Table Entry Default Port CSR 0xDF = No Route, discard packets All other values are reserved and result in packet discard. Note: For more information, see Table 1.	RW	0xDE

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10.12.5 Port {0..17} Domain Routing Table Register {0..255}

This is the port-specific domain routing register for destID 0–255. The broadcast version of this register is Port {0..17} Domain Routing Table Register {0..255}

Register Name: PORT_{0..17}_DOM_RTE_TABLE_{0..255} Reset Value: 0x0000_00DE	Register Offset: 0xE10400 + (0x1000 * port_num) + (0x4 * Domain)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	PORT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	PORT	0x00–0x11 = Output Port Number 0xDD = Use Device Routing Table, valid in Domain Routing Table only 0xDF = No Route, discard packets All other values are reserved and result in packet discard.	RW	0xDE

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10.13 Trace Comparison Values and Masks Registers

10.13.1 Base Addresses for Trace Comparison Values and Masks Registers

Port	Offset Address
0	0xE40000
1	0xE40100
2	0xE40200
3	0xE40300
4	0xE40400
5	0xE40500
6	0xE40600
7	0xE40700
8	0xE40800
9	0xE40900
10	0xE40A00
11	0xE40B00
12	0xE40C00
13	0xE40D00
14	0xE40E00
15	0xE40F00
16	0xE41000
17	0xE41100

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10.13.2 Port {0..17} Trace 0 Value 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_0_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE40000 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the first packet bit ... Bit 31 is compared to the 32nd packet bit	RW	0

10.13.3 Port {0..17} Trace 0 Value 1 Register

Register Name: PORT_{0..17}_TRACE_0_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE40004 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	RW	0

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10.13.4 Port {0..17} Trace 0 Value 2 Register

Register Name: PORT_{0..17}_TRACE_0_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE40008 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	RW	0

10.13.5 Port {0..17} Trace 0 Value 3 Register

Register Name: PORT_{0..17}_TRACE_0_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4000C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	RW	0

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10.13.6 Port {0..17} Trace 0 Value 4 Register

Register Name: PORT_{0..17}_TRACE_0_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE40010 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	RW	0

10.13.7 Port {0..17} Trace 0 Mask 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_0_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE40014 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the first comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	RW	0

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10.13.8 Port {0..17} Trace 0 Mask 1 Register

Register Name: PORT_{0..17}_TRACE_0_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE40018 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd comparison bit ... Bit 31 is a mask for the 64th comparison bit	RW	0

10.13.9 Port {0..17} Trace 0 Mask 2 Register

Register Name: PORT_{0..17}_TRACE_0_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4001C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	RW	0

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10.13.10 Port {0..17} Trace 0 Mask 3 Register

Register Name: PORT_{0..17}_TRACE_0_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE40020 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	RW	0

10.13.11 Port {0..17} Trace 0 Mask 4 Register

Register Name: PORT_{0..17}_TRACE_0_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE40024 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	RW	0

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10.13.12 Port {0..17} Trace 1 Value 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_1_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE40028 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the first packet bit ... Bit 31 is compared to the 32nd packet bit	RW	0

10.13.13 Port {0..17} Trace 1 Value 1 Register

Register Name: PORT_{0..17}_TRACE_1_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4002C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	RW	0

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10.13.14 Port {0..17} Trace 1 Value 2 Register

Register Name: PORT_{0..17}_TRACE_1_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE40030 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	RW	0

10.13.15 Port {0..17} Trace 1 Value 3 Register

Register Name: PORT_{0..17}_TRACE_1_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE40034 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	RW	0

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10.13.16 Port {0..17} Trace 1 Value 4 Register

Register Name: PORT_{0..17}_TRACE_1_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE40038 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	RW	0

10.13.17 Port {0..17} Trace 1 Mask 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_1_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE4003C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the first comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	RW	0

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10.13.18 Port {0..17} Trace 1 Mask 1 Register

Register Name: PORT_{0..17}_TRACE_1_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE40040 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd comparison bit ... Bit 31 is a mask for the 64th comparison bit	RW	0

10.13.19 Port {0..17} Trace 1 Mask 2 Register

Register Name: PORT_{0..17}_TRACE_1_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE40044 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	RW	0

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10.13.20 Port {0..17} Trace 1 Mask 3 Register

Register Name: PORT_{0..17}_TRACE_1_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE40048 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	RW	0

10.13.21 Port {0..17} Trace 1 Mask 4 Register

Register Name: PORT_{0..17}_TRACE_1_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4004C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	RW	0

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10.13.22 Port {0..17} Trace 2 Value 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_2_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE40050 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the 1st packet bit ... Bit 31 is compared to the 32nd packet bit	RW	0

10.13.23 Port {0..17} Trace 2 Value 1 Register

Register Name: PORT_{0..17}_TRACE_2_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE40054 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	RW	0

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10.13.24 Port {0..17} Trace 2 Value 2 Register

Register Name: PORT_{0..17}_TRACE_2_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE40058 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	RW	0

10.13.25 Port {0..17} Trace 2 Value 3 Register

Register Name: PORT_{0..17}_TRACE_2_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4005C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	RW	0

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10.13.26 Port {0..17} Trace 2 Value 4 Register

Register Name: PORT_{0..17}_TRACE_2_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE40060 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	RW	0

10.13.27 Port {0..17} Trace 2 Mask 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_2_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE40064 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	RW	0

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10.13.28 Port {0..17} Trace 2 Mask 1 Register

Register Name: PORT_{0..17}_TRACE_2_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE40068 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd comparison bit ... Bit 31 is a mask for the 64th comparison bit	RW	0

10.13.29 Port {0..17} Trace 2 Mask 2 Register

Register Name: PORT_{0..17}_TRACE_2_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4006C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	RW	0

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10.13.30 Port {0..17} Trace 2 Mask 3 Register

Register Name: PORT_{0..17}_TRACE_2_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE40070 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	RW	0

10.13.31 Port {0..17} Trace 2 Mask 4 Register

Register Name: PORT_{0..17}_TRACE_2_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE40074 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	RW	0

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10.13.32 Port {0..17} Trace 3 Value 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_3_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE40078 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the 1st packet bit ... Bit 31 is compared to the 32nd packet bit	RW	0

10.13.33 Port {0..17} Trace 3 Value 1 Register

Register Name: PORT_{0..17}_TRACE_3_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4007C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	RW	0

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10.13.34 Port {0..17} Trace 3 Value 2 Register

Register Name: PORT_{0..17}_TRACE_3_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE40080 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	RW	0

10.13.35 Port {0..17} Trace 3 Value 3 Register

Register Name: PORT_{0..17}_TRACE_3_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE40084 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 0 is compared to the 128th packet bit	RW	0

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10.13.36 Port {0..17} Trace 3 Value 4 Register

Register Name: PORT_{0..17}_TRACE_3_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE40088 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	RW	0

10.13.37 Port {0..17} Trace 3 Mask 0 Register

For base address information, see Trace Comparison Values and Masks Registers.

Register Name: PORT_{0..17}_TRACE_3_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE4008C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	RW	0

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10.13.38 Port {0..17} Trace 3 Mask 1 Register

Register Name: PORT_{0..17}_TRACE_3_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE40090 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd comparison bit ... Bit 31 is a mask for the 64th comparison bit	RW	0

10.13.39 Port {0..17} Trace 3 Mask 2 Register

Register Name: PORT_{0..17}_TRACE_3_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE40094 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	RW	0

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10.13.40 Port {0..17} Trace 3 Mask 3 Register

Register Name: PORT_{0..17}_TRACE_3_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE40098 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	RW	0

10.13.41 Port {0..17} Trace 3 Mask 4 Register

Register Name: PORT_{0..17}_TRACE_3_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4009C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	RW	0

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10.13.42 Broadcast Trace 0 Value 0 Register

Register Name: BCAST_TRACE_0_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F000

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the 1st packet bit ... Bit 31 is compared to the 32nd packet bit	WO	0

10.13.43 Broadcast Trace 0 Value 1 Register

Register Name: BCAST_TRACE_0_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F004

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	WO	0

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10.13.44 Broadcast Trace 0 Value 2 Register

Register Name: BCAST_TRACE_VAL_1_BLK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F008

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	WO	0

10.13.45 Broadcast Trace 0 Value 3 Register

Register Name: BCAST_TRACE_0_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F00C

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	WO	0

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10.13.46 Broadcast Trace 0 Value 4 Register

Register Name: BCAST_TRACE_0_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F010

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	WO	0

10.13.47 Broadcast Trace 0 Mask 0 Register

Register Name: BCAST_TRACE_0_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F014

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	WO	0

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10.13.48 Broadcast Trace 0 Mask 1 Register

Register Name: BCAST_TRACE_0_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F018

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd packet comparison bit ... Bit 31 is a mask for the 64th comparison bit	WO	0

10.13.49 Broadcast Trace 0 Mask 2 Register

Register Name: BCAST_TRACE_0_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F01C

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	WO	0

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10.13.50 Broadcast Trace 0 Mask 3 Register

Register Name: BCAST_TRACE_0_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F020

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	WO	0

10.13.51 Broadcast Trace 0 Mask 4 Register

Register Name: BCAST_TRACE_0_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F024

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	WO	0

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10.13.52 Broadcast Trace 1 Value 0 Register

Register Name: BCAST_TRACE_1_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F028

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the first packet bit ... Bit 31 is compared to the 32nd packet bit	WO	0

10.13.53 Broadcast Trace 1 Value 1 Register

Register Name: BCAST_TRACE_1_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F02C

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	WO	0

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10.13.54 Broadcast Trace 1 Value 2 Register

Register Name: BCAST_TRACE_1_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F030

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	WO	0

10.13.55 Broadcast Trace 1 Value 3 Register

Register Name: BCAST_TRACE_1_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F034

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	WO	0

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10.13.56 Broadcast Trace 1 Value 4 Register

Register Name: BCAST_TRACE_1_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F038

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	WO	0

10.13.57 Broadcast Trace 1 Mask 0 Register

Register Name: BCAST_TRACE_1_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F03C

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	WO	0

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10.13.58 Broadcast Trace 1 Mask 1 Register

Register Name: BCAST_TRACE_1_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F040

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd packet comparison bit ... Bit 31 is a mask for the 64th comparison bit	WO	0

10.13.59 Broadcast Trace 1 Mask 2 Register

Register Name: BCAST_TRACE_1_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F044

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	WO	0

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10.13.60 Broadcast Trace 1 Mask 3 Register

Register Name: BCAST_TRACE_1_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F048

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	WO	0

10.13.61 Broadcast Trace 1 Mask 4 Register

Register Name: BCAST_TRACE_1_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F04C

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	WO	0

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10.13.62 Broadcast Trace 2 Value 0 Register

Register Name: BCAST_TRACE_2_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F050

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the 1st packet bit ... Bit 31 is compared to the 32nd packet bit	WO	0

10.13.63 Broadcast Trace 2 Value 1 Register

Register Name: BCAST_TRACE_2_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F054

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	WO	0

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10.13.64 Broadcast Trace 2 Value 2 Register

Register Name: BCAST_TRACE_2_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F058

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	WO	0

10.13.65 Broadcast Trace 2 Value 3 Register

Register Name: BCAST_TRACE_2_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F05C

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	WO	0

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10.13.66 Broadcast Trace 2 Value 4 Register

Register Name: BCAST_TRACE_2_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F060

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	WO	0

10.13.67 Broadcast Trace 2 Mask 0 Register

Register Name: BCAST_TRACE_2_MASK__0 Reset Value: 0x0000_0000	Register Offset: 0xE4F064

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	WO	0

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10.13.68 Broadcast Trace 2 Mask 1 Register

Register Name: BCAST_TRACE_2_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F068

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd packet comparison bit ... Bit 31 is a mask for the 64th comparison bit	WO	0

10.13.69 Broadcast Trace 2 Mask 2 Register

Register Name: BCAST_TRACE_2_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F06C

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	WO	0

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10.13.70 Broadcast Trace 2 Mask 3 Register

Register Name: BCAST_TRACE_2_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F070

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	WO	0

10.13.71 Broadcast Trace 2 Mask 4 Register

Register Name: BCAST_TRACE_2_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F074

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	WO	0

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10.13.72 Broadcast Trace 3 Value 0 Register

Register Name: BCAST_TRACE_3_VAL_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F078

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the first 32 bits received in the packet. Bit 0 is compared to the first packet bit ... Bit 31 is compared to the 32nd packet bit	WO	0

10.13.73 Broadcast Trace 3 Value 1 Register

Register Name: BCAST_TRACE_3_VAL_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F07C

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 33rd packet bit ... Bit 31 is compared to the 64th packet bit	WO	0

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10.13.74 Broadcast Trace 3 Value 2 Register

Register Name: BCAST_TRACE_3_VAL_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F080

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 65th packet bit ... Bit 31 is compared to the 96th packet bit	WO	0

10.13.75 Broadcast Trace 3 Value 3 Register

Register Name: BCAST_TRACE_3_VAL_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F084

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 97th packet bit ... Bit 31 is compared to the 128th packet bit	WO	0

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10.13.76 Broadcast Trace 3 Value 4 Register

Register Name: BCAST_TRACE_3_VAL_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F088

Bits	0	1	2	3	4	5	6	7
00:07	VALUE							
08:15	VALUE							
16:23	VALUE							
24:31	VALUE							

Bits	Name	Description	Type	Reset Value
0:31	VALUE	This value is used for a bit-by-bit comparison against the next 32 bits received in the packet. Bit 0 is compared to the 129th packet bit ... Bit 31 is compared to the 160th packet bit	WO	0

10.13.77 Broadcast Trace 3 Mask 0 Register

Register Name: BCAST_TRACE_3_MASK_0 Reset Value: 0x0000_0000	Register Offset: 0xE4F08C

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the first 32 bits of the comparison value. Bit 0 is a mask for the 1st comparison value bit ... Bit 31 is a mask for the 32nd comparison bit	WO	0

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10.13.78 Broadcast Trace 3 Mask 1 Register

Register Name: BCAST_TRACE_3_MASK_1 Reset Value: 0x0000_0000	Register Offset: 0xE4F090

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 33rd packet comparison bit ... Bit 31 is a mask for the 64th comparison bit	WO	0

10.13.79 Broadcast Trace 3 Mask 2 Register

Register Name: BCAST_TRACE_3_MASK_2 Reset Value: 0x0000_0000	Register Offset: 0xE4F094

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 65th comparison bit ... Bit 31 is a mask for the 96th comparison bit	WO	0

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10.13.80 Broadcast Trace 3 Mask 3 Register

Register Name: BCAST_TRACE_3_MASK_3 Reset Value: 0x0000_0000	Register Offset: 0xE4F098

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 97th comparison bit ... Bit 31 is a mask for the 128th comparison bit	WO	0

10.13.81 Broadcast Trace 3 Mask 4 Register

Register Name: BCAST_TRACE_3_MASK_4 Reset Value: 0x0000_0000	Register Offset: 0xE4F09C

Bits	0	1	2	3	4	5	6	7
00:07	MASK							
08:15	MASK							
16:23	MASK							
24:31	MASK							

Bits	Name	Description	Type	Reset Value
0:31	MASK	This value is used for a bit-by-bit mask against the next 32 bits of the comparison value. Bit 0 is a mask for the 129th comparison bit ... Bit 31 is a mask for the 160th comparison bit	WO	0

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10.14 Global Device Configuration Registers

10.14.1 Device Control 1 Register

Register Name: DEVICE_CTL_1 Reset Value: Undefined	Register Offset: 0xF2000C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved	FATAL_ERR_PKT_MGT	EXT_MECS_EN	PGC_EN	Reserved	LT_INT_EN	LT_PW_EN	Reserved
08:15	Reserved							TRACE_OUT_PORT_MODE
16:23	TRACE_EN	Reserved	CLK_RATE_CTL	CUT_THRU_EN	Reserved			
24:31	Reserved		TRACE_OUT_PORT					PORT_RST_CTL

Bits	Name	Description	Type	Reset Value
0	Reserved	Reserved	RO	0
1	FATAL_ERR_PKT_MGT	Action to take when Port {0..17} Error and Status CSR.PORT_ERR is set. 0 = Drop 1 = Congest	RW	0
2	EXT_MECS_EN	0 = External MECS trigger is disabled 1 = External MECS trigger is enabled	RW	0
3	PGC_EN	Packet Generation and Capture mode (Used for test purposes) 0 = Disable 1 = Enable	RW	0
4	Reserved	Reserved	RO	0
5	LT_INT_EN	Generate an interrupt if a *RapidIO Specification (Rev. 2.1)*, *Part 8* Logical/Transport error is detected 0 = Do not generate 1 = Generate	RW	0
6	LT_PW_EN	Generate a port-write if a *RapidIO Specification (Rev. 2.1)*, *Part 8* Logical/Transport error is detected 0 = Do not generate 1 = Generate	RW	0
7:14	Reserved	Reserved	RO	0

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(Continued)

Bits	Name	Description	Type	Reset Value
15	TRACE_OUT_PORT_MODE	0 = Trace port is used for normal referenced traffic and for trace match data 1 = Trace port is only used for trace match data.	RW	0
16	TRACE_EN	1 = Enables the Trace Function at the device level	RW	0
17	Reserved	Reserved	RO	0
18	CLK_RATE_CTL	0 = Internal system clock is 156.25 MHz 1 = Internal system clock is 312.5 MHz Note: The reset value of this field is determined by the setting of the FSEL0 pin.	RO	Undefined
19	CUT_THRU_EN	Controls transfer mode from the Input Buffer 0 = Store-and-Forward mode 1 = Cut-Through mode	RW	0
20:25	Reserved	Reserved	RO	0
26:30	TRACE_OUT_PORT	Defines the output port that transmitted traced packets (only one valid port at a time). 0x00 = Port 0 is the trace port 0x01 = Port 1 is the trace port ... 0x11 = Port 17 is the trace port	RW	0x00
31	PORT_RST_CTL	Defines action when an S-RIO reset request is received 0 = Reset device 1 = Reset the port that received the reset request	RW	0

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10.14.2 Configuration Block Error Report Register

This register enables/disables error reporting to the Error Manager from the device's configuration logic.

Register Name: CFG_BLK_ERR_RPT Reset Value: 0x0000_0000	Register Offset: 0xF20014

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved				CFG_PW_PEND	CFG_INT_EN	CFG_PW_EN	CFG_LOG_EN

Bits	Name	Description	Type	Reset Value
0:27	Reserved	Reserved	RO	0
28	CFG_PW_PEND	1 = The Configuration Block has encountered a condition that required it to initiate a port-write. Once set, this bit remains set until written with a 1 to clear. Only valid if Configuration Block port-writes are enabled. For more information, see Configuration Block Event Notification.	W1R	0
29	CFG_INT_EN	0 = Disable interrupt due to Configuration Block error 1 = Enable interrupt due to Configuration Block error	RW	0
30	CFG_PW_EN	0 = Disable port-write due to Configuration Block error 1 = Enable port-write due to Configuration Block error	RW	0
31	CFG_LOG_EN	0 = Disable error reporting to Error Log due to Configuration Block error 1 = Enable error reporting to Error Log due to Configuration Block error	RW	0

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10.14.3 Aux Port Error Report Enable Register

This register enables/disables error reporting to the Error Manager from the device's JTAG and/or I^2C logic.

Register Name: AUX_PORT_ERR_RPT_EN Reset Value: 0x0000_0000	Register Offset: 0xF20018

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved						I2C_LOG_EN	JTAG_LOG_EN

Bits	Name	Description	Type	Reset Value
0:29	Reserved	Reserved	RO	0
30	I2C_LOG_EN	I^2C Error Logging/Reporting to the Error Log 0 = Disable 1 = Enable	RW	0
31	JTAG_LOG_EN	JTAG Error Logging/Reporting to the Error Log 0 = Disable 1 = Enable Note: This bit is applicable to CPS-1848 Revision A/B only.	RW	0

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10.14.4 RapidIO Domain Register

This register defines the CPS-1848's domain.

Register Name: RIO_DOMAIN Reset Value: 0x0000_0000	Register Offset: 0xF20020

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	DOMAIN							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	DOMAIN	Device Domain Configuration. This field determines what value for the most significant 8 bits of a 16-bit device ID are routed according to the Device routing table. For more information, see Packet Routing.	RW	0

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10.14.5 Port-Write Control Register

Register Name: PW_CTL Reset Value: 0x0000_0000	Register Offset: 0xF20024

Bits	0	1	2	3	4	5	6	7
00:07	SRCID_MSB							
08:15	SRCID							
16:23	PRIO		CRF	Reserved				
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:7	SRCID_MSB	Most significant byte of the sourceID to be used for all port-writes. The size of the sourceID is determined by Port-Write Target deviceID CSR.LARGE as follows: 0 = Small transport; LSB is the sourceID 1 = Large transport	RW	0
8:15	SRCID	sourceID to be used for all port-writes.	RW	0
16:17	PRIO	S-RIO Priority information to be used for port-writes. The recommended setting is 0b11.	RW	0
18	CRF	S-RIO Critical Request Flow information to be used for port-writes. The recommended setting is 1.	RW	0
19:31	Reserved	Reserved	RO	0

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10.14.6 RapidIO Assembly Identification CAR Override

This register provides the user control over the values that are used in the S-RIO defined ASSY_IDENT_CAR.

Register Name: ASSY_IDENT_CAR_OVRD Reset Value: 0x0000_0000	Register Offset: 0xF2002C

Bits	0	1	2	3	4	5	6	7
00:07	ASSY							
08:15	ASSY							
16:23	VENDOR							
24:31	VENDOR							

Bits	Name	Description	Type	Reset Value
0:15	ASSY	This value is assigned to the ASSY field in the Assembly Identity CAR.	RW	0
16:31	VENDOR	This value is assigned to the VENDOR field in the Assembly Identity CAR.	RW	0

10.14.7 RapidIO Assembly Information CAR Override

Register Name: ASSY_INF_CAR_OVRD Reset Value: 0x0000_0000	Register Offset: 0xF20030

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	ASSY_REV							
24:31	ASSY_REV							

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RO	0
16:31	ASSY_REV	This value is assigned to the ASSY_REV field of the Assembly Information CAR.	RW	0

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10.14.8 Device Soft Reset Register

Register Name: DEVICE_SOFT_RESET Reset Value: 0x0000_0000	Register Offset:0xF20040

Bits	0	1	2	3	4	5	6	7
00:07	SOFT_RESET							
08:15	SOFT_RESET							
16:23	SOFT_RESET							
24:31	SOFT_RESET							

Bits	Name	Description	Type	Reset Value
0:31	SOFT_RESET	0x00030097 = Reset the device (for more information, see Resets after Power-Up).	WO	0

10.14.9 I2C Master Control Register

Register Name: I2C_MASTER_CTL Reset Value: Undefined	Register Offset: 0xF20050

Bits	0	1	2	3	4	5	6	7
00:07	Reserved			I2C_PW_PEND	I2C_INT_EN	I2C_PW_EN	SPD_SEL	Reserved
08:15	Reserved	CLK_DIV						
16:23	Reserved				CHKSUM_DIS	Reserved	EPROM_ADDR	
24:31	EPROM_ADDR							

Bits	Name	Description	Type	Reset Value
0:2	Reserved	Reserved	RO	0
3	I2C_PW_PEND	Pending I2C port-write 1 = The I2C Block has encountered a condition that required it to initiate a port-write. Once set, this bit remains set until written with a 1 to clear. Valid only if I2C port-writes are enabled.	W1R	0

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Bits	Name	Description	Type	Reset Value
4	I2C_INT_EN	0 = Disable 1 = I2C interrupt enable. Valid only if I2C error reporting is enabled.	RW	0
5	I2C_PW_EN	0 = Disable 1 = I2C port-write enable. Valid only if I2C error reporting is enabled	RW	0
6	SPD_SEL	Master Frequency Select 0 = 400 kHz (Fast mode) 1 = 100 kHz (Standard mode)	RW	0
7:8	Reserved	Reserved	RO	0
9:15	CLK_DIV	Internal use only. Do not write to this field.	RW	0x62
16:19	Reserved	Reserved	RO	0
20	CHKSUM_DIS	0 = Verify checksum with EEPROM read 1 = Do not verify checksum with EEPROM read	RW	0
21	Reserved	Reserved	RO	0
22:31	EPROM_ADDR	EPROM Slave Address 0b0001010[ID2][ID1][ID0] I2C address to use for the EEPROM for commanded master mode. Note: The initial value of this field is determined by the setting of the ID[9:0] external pins.	RW	Undefined

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10.14.10 I2C Master Status and Control Register

Register Name: I2C_MASTER_STAT_CTL Reset Value: 0x0000_0000	Register Offset: 0xF20054

Bits	0	1	2	3	4	5	6	7
00:07	Reserved				UNEXP_START_STOP	NACK	WORD_ERR_22BIT	WORD_ERR_32BIT
08:15	CHKSUM_FAIL	READING	SUCCESS	ABORT	Reserved			START_READ
16:23	EPROM_START_ADDR							
24:31	EPROM_START_ADDR							

Bits	Name	Description	Type	Reset Value
0:3	Reserved	Reserved	RO	0
4	UNEXP_START_STOP	1 = An unexpected I2C start or stop was detected. Reset on read	RR	0
5	NACK	1 = An expected ack was not received. Reset on read	RR	0
6	WORD_ERR_22BIT	1 = 22 bits of read data were expected but the operation was terminated prematurely. Reset on read	RR	0
7	WORD_ERR_32BIT	1 = 32 bits of read data were expected but the operation was terminated prematurely. Reset on read	RR	0
8	CHKSUM_FAIL	1 = The ckecksum verification of a I2C read operation failed. Reset on read	RR	0
9	READING	0 = I2C read operation is not in progress 1 = I2C read operation is in progress This bit will stay high as long as the sequence is in progress and then will go low after it completes.	RO	0
10	SUCCESS	1 = A previous Master I2C read operation is complete and was successful. If successful this bit will stay high until the next sequence is initiated.	RO	0
11	ABORT	1 = Abort any pending I2C master operation.	WO	0
12:14	Reserved	Reserved	RO	0
15	START_READ	1 = Initiate the start of an I2C EEPROM read.	WO	0
16:31	EPROM_START_ADDR	EEPROM address offset where I2C Master read operation should occur	RW	0

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10.14.11 JTAG Control Register (Revision A/B)



This register is applicable to CPS-1848 Revision A/B only.

Register Name: JTAG_CTL Reset Value: 0x0000_0000	Register Offset: 0xF2005C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved					JTAG_INT_EN	JTAG_PW_EN	JTAG_PW_PEND

Bits	Name	Description	Type	Reset Value
0:28	Reserved	Reserved	RO	0
29	JTAG_INT_EN	0 = Disable JTAG S-RIO interrupt 1 = Enable JTAG S-RIO interrupt	RW	0
30	JTAG_PW_EN	0 = Disable JTAG S-RIO port-write 1 = Enable JTAG S-RIO port-write	RW	0
31	JTAG_PW_PEND	Pending port-write 1 = The device has encountered a JTAG error condition that required it to initiate a port-write. Once set, this bit remains set until written with a 1 to clear. Valid only if JTAG port-writes are enabled.	W1R	0

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10.14.12 External MCES Trigger Counter Register

This counter acts as a programmable divider between the Multicast Control Symbol (MCES) external input pin and the generation of an MCES control symbol. When the number of pulses received matches the trigger count, an MCES control symbol is generated. The counter automatically resets after triggering.

Register Name: EXT_MECS_TRIG_CNTR Reset Value: 0x0000_00FF	Register Offset: 0xF20060

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	TRIG_CNT							

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:31	TRIG_CNT	Initial Count of the External Multicast Control Symbol Trigger Count.	RW	0xFF

10.14.13 Maintenance Dropped Packet Counter Register

Register Name: MAINT_DROP_PKT_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF20064

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	For Revision A/B, a saturating count of maintenance packets that have been dropped by the maintenance block. For Revision C, a saturating count of maintenance packets with a hop count equal to 0 that have been dropped by the maintenance block. Note: For Revision C, maintenance packets that are dropped due to “no route” are not counted by this register.	RR	0

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10.14.14 Switch Parameters 1 Register

Register Name: SWITCH_PARAM_1 Reset Value: 0x000C_0C9F	Register Offset: 0xF20068

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved			FB_ALLOC			BUF_ALLOC	ARB_MODE
16:23	ARB_MODE		OUTPUT_CREDIT_RSVN					
24:31	OUTPUT_CREDIT_RSVN			INPUT_STARV_LIM				

Bits	Name	Description	Type	Reset Value
0:10	Reserved	Reserved	RO	0
11:13	FB_ALLOC	Final Buffer Allocation Size This field reserves buffer space for higher priorities. It is ignored if BUF_ALLOC is configured for single buffer allocation mode. Highest priority packets can use all the buffers if they arrive first (no need to reserve for lower priority). However, if lower priority packet arrive first, they cannot use all the buffers if there are no higher priority packets that are currently in the buffer. Instead, the reserved buffer guarantees that higher priority packets can be handled if they arrive at a later time. 000–001 = Reserved 010 = 2 buffers reserved for each VC0 priority 1, 2, and 3 011 = 3 buffers reserved for each VC0 priority 1, 2, and 3 100 = 4 buffers reserved for each VC0 priority 1, 2, and 3 101 = 5 buffers reserved for each VC0 priority 1, 2, and 3 110 = 6 buffers reserved for each VC0 priority 1, 2, and 3 111 = 7 buffers reserved for each VC0 priority 1, 2, and 3	RW	0b011
14	BUF_ALLOC	Buffer Allocation Mode 0 = Multi-buffer reservation mode. Minimum of two pages are allocated to each priority (1, 2, 3) in input and crosspoint buffers. 1 = Single buffer reservation mode. Minimum of one page is allocated to each priority (1, 2, 3) in input, crosspoint and final buffers.	RW	0

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Bits	Name	Description	Type	Reset Value
15:17	ARB_MODE	Switching Arbitration Mode 0b000 = Normal mode: Input scheduler aging is enabled. Output Scheduler proportional fairness is enabled. 0b001–0b010 = Reserved 0b011 = Strict priority mode: Input scheduler aging is enabled Output Scheduler is in round-robin only mode (proportional fairness is disabled) 0b100–0b110 = Reserved 0b111 = Round-robin mode: Input scheduler aging is disabled. Output scheduler is in round-robin only mode (proportional fairness is disabled).	RW	0b000
18:26	OUTPUT_CREDIT_RSVN	Default bandwidth reservation value (all ports) for the output scheduler algorithm. This value must be less than the credit maximum and greater than the minimum values defined in the Switch Parameters 2 Register. Note: In order to achieve better credit out-of-bound detection when the ports are subjected to uneven traffic flows (for example, 272-byte packet on one port and 32-byte packet on another), the OUTPUT_CREDIT_MIN/MAX values in the Switch Parameters 2 Register should be increased to greater than 2000 (0x7D0). The default value of these fields is 1000 (0x3E8).	RW	0x64
27:31	INPUT_STARV_LIM	Threshold value for Input Scheduler Starvation Prevention.	RW	0x1F

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10.14.15 Switch Parameters 2 Register

In order to achieve better credit out-of-bound detection when the ports are subjected to uneven traffic flows (for example, 272-byte packet on one port and 32-byte packet on another), the OUTPUT_CREDIT_MIN/MAX values in this register should be increased to greater than 2000 (0x7D0).

Register Name: SWITCH_PARAM_2 Reset Value: 0x03E8_03E8	Register Offset: 0xF2006C

Bits	0	1	2	3	4	5	6	7
00:07	OUTPUT_CREDIT_MIN							
08:15	OUTPUT_CREDIT_MIN							
16:23	OUTPUT_CREDIT_MAX							
24:31	OUTPUT_CREDIT_MAX							

Bits	Name	Description	Type	Reset Value
0:15	OUTPUT_CREDIT_MIN	Minimum output scheduler credit value. Reset if reached. Note: This is a negative credit value.	RW	0x3E8
16:31	OUTPUT_CREDIT_MAX	Maximum output scheduler credit value. Reset if reached. Note: This is a positive credit value.	RW	0x3E8

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10.14.16 Quadrant Configuration Register

This register configures the port width and lane to port mapping of the CPS-1848's quadrants. The following register table shows the port width configuration based on the value of the QUADx_CFG field. For lane to port mapping based on the value programmed into the same field, see Table 20.

Before changing this register, see Port Reconfiguration Operations for the correct procedure to follow.

Register Name: QUAD_CFG Reset Value: Undefined	Register Offset: 0xF20200

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	QUAD3_CFG		QUAD2_CFG		QUAD1_CFG		QUAD0_CFG	

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24:25	QUAD3_CFG	0b00 = 3 by 4x ports 0b01 = 2 by 4x, 2 by 2x ports 0b10 = Undefined 0b11 = Undefined Note: The initial value of this field is determined by the setting of the QCFG[7:6] external pins.	RW	Undefined
26:27	QUAD2_CFG	0b00 = 3 by 4x ports 0b01 = 2 by 4x, 2 by 2x ports 0b10 = Undefined 0b11 = Undefined Note: The initial value of this field is determined by the setting of the QCFG[5:4] external pins.	RW	Undefined
28:29	QUAD1_CFG	0b00 = 3 by 4x ports 0b01 = 2 by 4x, 2 by 2x ports 0b10 = 1 by 4x, 4 by 2x ports 0b11 = 2 by 4x, 1 by 2x, 2 by 1x ports Note: The initial value of this field is determined by the setting of the QCFG[3:2] external pins.	RW	Undefined

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Bits	Name	Description	Type	Reset Value
30:31	QUAD0_CFG	0b00 = 3 by 4x ports 0b01 = 2 by 4x, 2 by 2x ports 0b10 = 1 by 4x, 4 by 2x ports 0b11 = 2 by 4x, 1 by 2x, 2 by 1x ports Note: The initial value of this field is determined by the setting of the QCFG[1:0] external pins.	RW	Undefined

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10.14.17 Device Reset and Control Register

Register Name: DEVICE_RESET_CTL Reset Value: 0x0000_0000	Register Offset: 0xF20300

Bits	0	1	2	3	4	5	6	7
00:07	DO_RESET	RESET_TYPE	PLL_SEL					
08:15	PLL_SEL						PORT_SEL	
16:23	PORT_SEL							
24:31	PORT_SEL							

Bits	Name	Description	Type	Reset Value
0	DO_RESET	1 = Reset the structures defined in the PORT_SEL field if RESET_TYPE is 0. If RESET_TYPE is 1 then a soft reset of the entire device is triggered.	WO	0
1	RESET_TYPE	This register can be used for two types of resets: 0 = Reset the local facilities that are defined in this register (that is, specific ports and PLLs) is performed. PLL_SEL and PORT_SEL are active for this setting. 1 = Reset all device-level digital logic (global reset) except for the configuration registers is performed. This includes all lanes, ports, the switch fabric, the maintenance block, the I2C Interface and the JTAG logic. PORT_SEL is not active for this reset, but PLL_SEL indicates that PLL resets can also be triggered with this reset. Note: This reset requires the CPS-1848 to be quiescent (it is not transmitting or receiving packets).	RW	0
2:13	PLL_SEL	When DO_RESET is 1, all PLLs represented by bits in this field that are set to 1 are reset. Bit 2 = PLL 11 Bit 3 = PLL 10 ... Bit 13 = PLL 0 Note: The main use of this field is to initiate resets to specific PLLs when a modification to the PLL_DIV_SEL field in the PLL {0..11} Control 1 Register is made that requires a reset to a specific PLL. PORT_SEL is expected to be used in conjunction with the PLL resets selected in this field.	RW	0

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Bits	Name	Description	Type	Reset Value
14:31	PORT_SEL	When DO_RESET is 1 and RESET_TYPE is 0, all ports represented by bits in this field that are set to 1 are reset. Bit 14 = Port 17 Bit 15 = Port 16 ... Bit 31 = Port 0 Note: The main use of this field is to initiate resets to specific ports when a modification to the PLL_DIV_SEL field in the PLL {0..11} Control 1 Register is made that requires a port-level reset.	RW	0

10.15 Implementation Specific Multicast Mask Registers

10.15.1 Implementation Specific Multicast Mask Base Addresses

Port	Offset from Base
Broadcast	0xF30000
0	0xF38000
1	0xF38100
2	0xF38200
3	0xF38300
4	0xF38400
5	0xF38500
6	0xF38600
7	0xF38700
8	0xF38800
9	0xF38900
10	0xF38A00
11	0xF38B00
12	0xF38C00
13	0xF38D00
14	0xF38E00
15	0xF38F00
16	0xF39000
17	0xF39100

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10.15.2 Broadcast Multicast Mask Register {0..39}

The per-port version of this register is Port {0..17} Multicast Mask Register {0..39}.

Register Name: BCAST__MCAST_MASK_{0..39} Reset Value: 0x0000_0000	Register Offset: 0xF30000 + (0x4 * multicast_mask_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved						PORT_MASK	
16:23	PORT_MASK							
24:31	PORT_MASK							

Bits	Name	Description	Type	Reset Value
0:13	Reserved	Reserved	RO	0
14:31	PORT_MASK	Each bit represents one output port. Bit 14 = Port 17 ... Bit 30 = Port 1 Bit 31 = Port 0 Where, 0 = Port is not included in Multicast Mask Number *m* for port_num *n* 1 = Port is included in Multicast Mask Number *m* for port_num *n*	RW	0

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10.15.3 Port {0..17} Multicast Mask Register {0..39}

For base address information, see Implementation Specific Multicast Mask Registers. The broadcast version of this register is Broadcast Multicast Mask Register {0..39}.

Register Name: PORT_{0..17}_MCAST_MASK_{0..39} Reset Value: 0x0000_0000	Register Offset: 0xF38000 + (0x100 * port_num) + (0x4 * multicast_mask_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved						PORT_MASK	
16:23	PORT_MASK							
24:31	PORT_MASK							

Bits	Name	Description	Type	Reset Value
0:13	Reserved	Reserved	RO	0
14:31	PORT_MASK	Each bit represents one output port. Bit 14 = Port 17 ... Bit 30 = Port 1 Bit 31 = Port 0 Where, 0 = Port is not included in Multicast Mask Number *m* for port_num *n* 1 = Port is included in Multicast Mask Number *m* for port_num *n*	RW	0

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10.16 Port Function Registers

10.16.1 Port {0..17} Function Registers Base Addresses

Port	Offset Address
0	0xF40000
1	0xF40100
2	0xF40200
3	0xF40300
4	0xF40400
5	0xF40500
6	0xF40600
7	0xF40700
8	0xF40800
9	0xF40900
10	0xF40A00
11	0xF40B00
12	0xF40C00
13	0xF40D00
14	0xF40E00
15	0xF40F00
16	0xF41000
17	0xF41100

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10.16.2 Port {0..17} Operations Register

For base address information, see Port Function Registers. The broadcast version of this register is Broadcast Port Operations Register.

Register Name: PORT_{0..17}_OPS Reset Value: 0x0240_0000	Register Offset: 0xF40004 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved		CRC_DIS	PORT_INT_EN	PORT_PW_EN	CNTRS_EN	SILENCE_CTL	
08:15	SILENCE_CTL		Reserved	FORCE_REINIT	TX_FLOW_CTL_DIS	Reserved	SELF_MCAST_EN	FILTER_3_EN
16:23	FILTER_2_EN	FILTER_1_EN	FILTER_0_EN	TRACE_3_EN	TRACE_2_EN	TRACE_1_EN	TRACE_0_EN	Reserved
24:31	TRACE_PW_EN	PORT_LOG_EN	LANE_LOG_EN	LT_LOG_EN	CRC_RETX_LIMIT			Reserved

Bits	Name	Description	Type	Reset Value
0:1	Reserved	Reserved	RO	0
2	CRC_DIS	CRC Check Disable 0 = Perform normal packet CRC 1 = Packet CRC check reports valid CRC regardless of condition	RW	0
3	PORT_INT_EN	0 = Do not generate interrupt if an error is detected 1 = Generate interrupt if an error is detected	RW	0
4	PORT_PW_EN	0 = Do not generate port-write if an error is detected 1 = Generate port-write if an error is detected	RW	0
5	CNTRS_EN	0 = Disable port-level counters 1 = Enable port-level counters	RW	0
6:9	SILENCE_CTL	Changes the amount of time spent in the silent state of the port initialization state machine. Default is 120 microseconds. Each increment represents 13.1 microseconds of change.	RW	0b1001
10	Reserved	Reserved	RW	0
11	FORCE_REINIT	1 = Force the initialization state machine back to the silent state. This causes the loss of the link.	WO	0

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Bits	Name	Description	Type	Reset Value
12	TX_FLOW_CTL_DIS	Transmitter-controlled flow control 0 = Enable 1 = Disable Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	0
13	Reserved	Reserved	RO	0
14	SELF_MCAST_EN	0 = Disable 1 = Enable Note: If this port is included in any multicast mask, multicast packets received on this port will be multicast back out this port. If this bit is set, software must handle multicast back to itself. Note that multicasting packets back to the port that the packet was received on is contrary to the *RapidIO Specification (Rev. 2.1)*.	RW	0
15	FILTER_3_EN	0 = Disable filter comparison 3 1 = Enable filter	RW	0
16	FILTER_2_EN	0 = Disable filter comparison 2 1 = Enable filter	RW	0
17	FILTER_1_EN	0 = Disable filter comparison 1 1 = Enable filter	RW	0
18	FILTER_0_EN	0 = Disable filter comparison 0 1 = Enable filter	RW	0
19	TRACE_3_EN	0 = Disable trace comparison (TC) Value 3 1 = Enable TC Value 3	RW	0
20	TRACE_2_EN	0 = Disable TC Value 2 1 = Enable TC Value 2	RW	0
21	TRACE_1_EN	0 = Disable TC Value 1 1 = Enable TC Value 1	RW	0
22	TRACE_0_EN	0 = Disable TC Value 0 1 = Enable TC Value 0	RW	0
23	Reserved	Reserved	RW	0
24	TRACE_PW_EN	0 = Do not generate a port-write on a trace match 1 = Generate a port-write on a trace match Note: This bit is active only if PORT_LOG_EN is set to 1.	RW	0

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Bits	Name	Description	Type	Reset Value
25	PORT_LOG_EN	0 = Disable error logging for port-level errors 1 = Enable error logging for port-level errors	RW	0
26	LANE_LOG_EN	0 = Disable error logging for lane-level errors 1 = Enable error logging for lane-level errors	RW	0
27	LT_LOG_EN	0 = Disable error logging for logical/transport errors 1 = Enable error logging for logical/transport errors	RW	0
28:30	CRC_RETX_LIMIT	0b000 = No CRC retransmission limit 0b001–0b111 = The number of CRC retransmissions allowed before packet is dropped.	RW	0b000
31	Reserved	Reserved	RO	0

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10.16.3 Port {0..17} Implementation Specific Error Detect Register

This register allows the user to define when an implementation-specific error is captured at a finer granularity. For base address information, see Port Function Registers. The broadcast version of this register is Broadcast Port Implementation Specific Error Detect Register.

Register Name: PORT_{0..17}_IMPL_SPEC_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0xF40008 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE	TTL_EVENT	CRC_EVENT	PNA	UNSOL_LR	UNEXP_ACKID	PNA_RETRY	RTE_ISSUE
08:15	Reserved	SET_ACKID	TX_DROP	MANY_RETRY	RX_DROP	Reserved	BAD_TT	SHORT
16:23	UNSOL_RFR	FATAL_TO	RETRY	RETRY_ACKID	STOMP_TO	RX_STOMP	LR_CMD	LR_X2
24:31	UNEXP_EOP	UNEXP_STOMP	PORT_INIT	PORT_WIDTH	IDLE_IN_PKT	LOA	BAD_CTL	REORDER

Bits	Name	Description	Type	Reset Value
0	ERR_RATE	1 = The port encountered a condition when the error rate has exceeded the programmed error rate threshold.	RW	0
1	TTL_EVENT	1 = A packet has been stored in the port output buffer for a period of time that exceeds the time to live timeout value. This also represents a dropped packet event.	RW	0
2	CRC_EVENT	1 = Detected a CRC anomaly. Possibilities include: • A packet has encountered a number of retries that has exceeded the programmed CRC limit and was dropped. • A packet was received with a CRC error on a port that has been configured for CRC Retransmission Suppression and was dropped.	RW	0
3	PNA	1 = Received a NACK with a cause other than lack of resources; however, the user may want to turn off the counting of NACKs due to lack of resources (which some may view as not being an error). The methodology achieved with this bit is to turn off all NACKs via CS_NOT_ACC in the Port {0..17} Error Detect CSR (Part 8 level) so that the user can disable the counting of lack of resource NACKs (by disabling all NACKs at the Part 8 level) and then re-enable the counting of all other NACKs with this bit.	RW	0
4	UNSOL_LR	1 = Received an unsolicited Link-Response	RW	0
5	UNEXP_ACKID	1 = Received an acknowledge control symbol with an unexpected ackID	RW	0

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Bits	Name	Description	Type	Reset Value
6	PNA_RETRY	1 = A packet could not be accepted because the RX buffers were full	RW	0
7	RTE_ISSUE	1 = A routing issue occurred. Possibilities include: • A packet was received that referenced the “no route” condition and was dropped • A packet was received that referenced a port which is disabled and was dropped • A packet was received that referenced an output port that is configured in Port Lockout mode (see Section 2.2 in the *RapidIO Specification (Rev. 2.1), Part 8*) • A packet was received that references an output port that is in the Fatal Error State	RW	0
8	Reserved	Reserved	RO	0
9	SET_ACKID	1 = A write to the Local ackID register used an invalid outstanding ackID field	RW	0
10	TX_DROP	1 = The port dropped a non-maintenance packet when the transmission of non-maintenance packets was disabled	RW	0
11	MANY_RETRY	1 = The port detected a retry count that triggered a link partner congestion event	RW	0
12	RX_DROP	1 = Received a non-maintenance packet when the reception of non-maintenance packets was disabled. Note that the term “discard” refers to a NACK (as required by the Port {0..17} Control 1 CSR) when the input port is disabled. The packet is not dropped in terms of the dropped packet counter.	RW	0
13	Reserved	Reserved	RW	0
14	BAD_TT	1 = Received a packet with an invalid TT field	RW	0
15	SHORT	1 = Received a packet with only 32 bits of data between the packet delimiters	RW	0
16	UNSOL_RFR	1 = Received a restart from retry control symbol while the receiver was not in the Input-Retry Stopped state	RW	0
17	FATAL_TO	1 = A Link-Response was not received after 15 Link-Requests were transmitted, causing a fatal error	RW	0
18	RETRY	1 = Received a retry control symbol with a valid ackID	RW	0
19	RETRY_ACKID	1 = Received a retry control symbol with an unexpected ackID	RW	0
20	STOMP_TO	1 = Transmitted a STOMP control symbol but the link partner did not reply with a packet retry (or a packet NACK)	RW	0

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Bits	Name	Description	Type	Reset Value
21	RX_STOMP	1 = Received a STOMP control symbol	RW	0
22	LR_CMD	1 = Received a Link-Request with a reserved command field encoding	RW	0
23	LR_X2	1 = Received a second Link-Request before the Link-Response was transmitted for the first one	RW	0
24	UNEXP_EOP	1 = Received an EOP control symbol that did not terminate a packet	RW	0
25	UNEXP_STOMP	1 = Received a STOMP control symbol that did not terminate a packet	RW	0
26	PORT_INIT	1 = Indicates that port initialization acquired after completing the transmission of 15 Status control symbols	RW	0
27	PORT_WIDTH	1 = The maximum configured port width could not be initialized and the port selected a lower lane width	RW	0
28	IDLE_IN_PKT	1 = An IDLE character (K, A, R, M) was detected in a received packet	RW	0
29	LOA	1 = Alignment was lost	RW	0
30	BAD_CTL	1 = The sequence of received control characters indicates a protocol error. For example, in 4x mode the lane 0 character is a control character and there is one or more control characters present on the remaining lanes (excluding the case of an idle column). Also indicates in 1x mode that a control symbol has a control character present in the data segment.	RW	0
31	REORDER	1 = The port detected that lanes were reordered during port initialization because of information in IDLE2 sequence.	RW	0

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10.16.4 Port {0..17} Implementation Specific Error Rate Enable Register

This register allows the user to define when an implementation specific error is captured at a finer granularity. For base address information, see Port Function Registers. The broadcast version of this register is Broadcast Port Implementation Specific Error Rate Enable Register.

Hot Extraction/Insertion support requires exclusive use of these registers. No Standard Physical Layer Errors can be enabled when Hot Extraction/Insertion functionality is required.

When an event is disabled in this register, the corresponding event in the Port {0..17} Implementation Specific Error Detect Register is not affected.

Register Name: PORT_{0..17}_IMPL_SPEC_ERR_RATE_EN Reset Value: 0xFF7F_FFFF	Register Offset: 0xF4000C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE_EN	TTL_EVENT_EN	CRC_EVENT_EN	PNA_EN	UNSOL_LR_EN	UNEXP_ACKID_EN	PNA_RETRY_EN	RTE_ISSUE_EN
08:15	Reserved	SET_ACKID_EN	TX_DROP_EN	MANY_RETRY_EN	RX_DROP_EN	Reserved	BAD_TT_EN	SHORT_EN
16:23	UNSOL_RFR_EN	FATAL_TO_EN	RETRY_EN	RETRY_ACKID_EN	STOMP_TO_EN	RX_STOMP_EN	LR_CMD_EN	LR_X2_EN
24:31	UNEXP_EOP_EN	UNEXP_STOMP_EN	PORT_INIT_EN	PORT_WIDTH_EN	IDLE_IN_PKT_EN	LOA_EN	BAD_CTL_EN	REORDER_EN

Bits	Name	Description	Type	Reset Value
0	ERR_RATE_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
1	TTL_EVENT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
2	CRC_EVENT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
3	PNA_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
4	UNSOL_LR_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
5	UNEXP_ACKID_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
6	PNA_RETRY_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1

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(Continued)

Bits	Name	Description	Type	Reset Value
7	RTE_ISSUE_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
8	Reserved	Reserved	RO	0
9	SET_ACKID_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
10	TX_DROP_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
11	MANY_RETRY_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
12	RX_DROP_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
13	Reserved	Reserved	RW	1
14	BAD_TT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
15	SHORT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
16	UNSOL_RFR_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
17	FATAL_TO_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
18	RETRY_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
19	RETRY_ACKID_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
20	STOMP_TO_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
21	RX_STOMP_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
22	LR_CMD_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
23	LR_X2_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
24	UNEXP_EOP_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1

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(Continued)

Bits	Name	Description	Type	Reset Value
25	UNEXP_STOMP_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
26	PORT_INIT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
27	PORT_WIDTH_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
28	IDLE_IN_PKT_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
29	LOA_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
30	BAD_CTL_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1
31	REORDER_EN	1 = Enable the capture of the corresponding error in the Port {0..17} Implementation Specific Error Detect Register.	RW	1

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10.16.5 Port {0..17} VC0 Acknowledgements Transmitted Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_PA_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40010 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packet acknowledgements transmitted by the port for VC0 packets. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.6 Port {0..17} Not Acknowledgements Transmitted Counter Register

Register Name: PORT_{0..17}_NACK_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40014 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packet not acknowledgements (NACKs) transmitted by the port. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.7 Port {0..17} VC0 Retry Symbols Transmitted Counter Register

Register Name: PORT_{0..17}_VC0_RTRY_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40018 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of the number of retry symbols transmitted by the port for VC0 packets. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.8 Port {0..17} VC0 Packets Transmitted Counter Register

Register Name: PORT_{0..17}_VC0_PKT_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF4001C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of all packets that are transmitted by the port (includes retransmissions) for VC0 packets. Counted on EOP. Excludes partially transmitted packets. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.9 Port {0..17} Trace Match Counter Value 0 Register

Register Name: PORT_{0..17}_TRACE_CNTR_0 Reset Value: 0x0000_0000	Register Offset: 0xF40020 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets at the port that have met the defined trace criteria with comparison value 0. Note: The Packet Trace counters are incremented for each packet received. This implies that retried packets which match the trace criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.10 Port {0..17} Trace Match Counter Value 1 Register

Register Name: PORT_{0..17}_TRACE_CNTR_1 Reset Value: 0x0000_0000	Register Offset: 0xF40024 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets at the port that have met the defined trace criteria with comparison value 1. Note: The Packet Trace counters are incremented for each packet received. This implies that retried packets which match the trace criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.11 Port {0..17} Trace Match Counter Value 2 Register

Register Name: PORT_{0..17}_TRACE_CNTR_2 Reset Value: 0x0000_0000	Register Offset: 0xF40028 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets at the port that have met the defined trace criteria with comparison value 2. Note: The Packet Trace counters are incremented for each packet received. This implies that retried packets which match the trace criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.12 Port {0..17} Trace Match Counter Value 3 Register

Register Name: PORT_{0..17}_TRACE_CNTR_3 Reset Value: 0x0000_0000	Register Offset: 0xF4002C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets at the port that have met the defined trace criteria with comparison value 3. Note: The Packet Trace counters are incremented for each packet received. This implies that retried packets which match the trace criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.13 Port {0..17} Filter Match Counter Value 0 Register

Register Name: PORT_{0..17}_FILTER_CNTR_0 Reset Value: 0x0000_0000	Register Offset: 0xF40030 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets that have met the defined filter criteria with comparison Value 0. Note: The Packet Filtering counters are incremented for each packet received. This implies that retried packets which match the filter criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.14 Port {0..17} Filter Match Counter Value 1 Register

Register Name: PORT_{0..17}_FILTER_CNTR_1 Reset Value: 0x0000_0000	Register Offset: 0xF40034 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets that have met the defined filter criteria with comparison Value 1. Note: The Packet Filtering counters are incremented for each packet received. This implies that retried packets which match the filter criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.15 Port {0..17} Filter Match Counter Value 2 Register

Register Name: PORT_{0..17}_FILTER_CNTR_2 Reset Value: 0x0000_0000	Register Offset: 0xF40038 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets that have met the defined filter criteria with comparison Value 2. Note: The Packet Filtering counters are incremented for each packet received. This implies that retried packets which match the filter criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.16 Port {0..17} Filter Match Counter Value 3 Register

Register Name: PORT_{0..17}_FILTER_CNTR_3 Reset Value: 0x0000_0000	Register Offset: 0xF4003C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packets that have met the defined filter criteria with comparison Value 3. Note: The Packet Filtering counters are incremented for each packet received. This implies that retried packets which match the filter criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.17 Port {0..17} VC0 Acknowledgements Received Counter Register

Register Name: PORT_{0..17}_VC0_PA_RX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40040 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packet acknowledgements received by the port for VC0 packets. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.18 Port {0..17} Not Acknowledgements Received Counter Register

Register Name: PORT_{0..17}_NACK_RX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40044 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of packet not acknowledgements received by the port for all VCs. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.19 Port {0..17} VC0 Retry Symbols Received Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_RTRY_RX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40048 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of received retry symbols by the port for VC0 packets. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.20 Port {0..17} VC0 Switch Crosspoint Buffer Output Packet Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_CPB_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF4004C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets sent to the Final Buffer from the Crosspoint buffers in a switch port column. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.21 Port {0..17} VC0 Packets Received Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_PKT_RX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40050 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets received by the port. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit. (Revision A/B) Note: If the routing tables indicate that a packet should be dropped, and tracing is active, this counter will still increment if the decision not to trace the packet occurs during reception of bytes 8–21 of the packet. (Revision C) Note: If the routing tables indicate that a packet should be dropped, and tracing is active, this counter *will not* increment if the decision not to trace the packet occurs during reception of bytes 8–21 of the packet.	RR	0

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10.16.22 Port {0..17} Trace Port-Write Reset Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_TRACE_PW_CTL Reset Value: 0x0000_0000	Register Offset: 0xF40058 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							PW_DIS

Bits	Name	Description	Type	Reset Value
0:30	Reserved	Reserved	RO	0
31	PW_DIS	0 = Generation of maintenance port-write packets (for trace matches only) is enabled 1 = Generation of maintenance port-write packets (for trace matches only) is disabled	RW	0

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10.16.23 Port {0..17} Lane Synchronization Register

Register Name: PORT_{0..17}_LANE_SYNC Reset Value: 0x0000_0001	Register Offset: 0xF40060 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved					VMIN		

Bits	Name	Description	Type	Reset Value
0:28	Reserved	Reserved	RO	0
29:31	VMIN	The value of Vmin to be used in each of the port's lane synchronization state machines. Vmin is defined as follows: Revision C 0b000 = Vmin = 127 0b001 = Vmin = 2^{12} - 1 0b010 = Vmin = 2^{13} - 1 0b011 = Vmin = 2^{14} - 1 0b100 = Vmin = 2^{15} - 1 0b101 = Vmin = 2^{16} - 1 0b110–0b111 = Vmin = 0 Revision A/B 0b000 = Vmin = 127 0b001 = Vmin = 2^{11} - 1 0b010 = Vmin = 2^{12} - 1 0b011 = Vmin = 2^{13} - 1 0b100 = Vmin = 2^{14} - 1 0b101 = Vmin = 2^{15} - 1 0b110–0b111 = Vmin = 0 Note: The VMIN value used by a lane is the VMIN value programmed into the lowest numbered port for each quad. For example, the VMIN value for port 0 controls the VMIN value for lanes 0–3. Note: For Revision C, the reset value for this bit is 0b001. For Revision A/B, the reset value is 0b000. Note: For link speeds of 5 Gbaud or higher, 0b001 or higher should be used as recommended by the *RapidIO Specification (Rev. 2.1)*.	RW	0b001

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10.16.24 Port {0..17} VC0 Received Packets Dropped Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_PKT_DROP_RX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40064 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets dropped by the port's receiver logic. Note: To be consistent with the *RapidIO Specification (Rev. 2.1)*, packets are dropped silently when multicast using a port mask value of all 0s (no ports selected). This counter does not increment when packets are multicast using a port mask value of all 0s. For more information, see Multicast Programming Model. Note: This counter works only when the CPS-1848 is configured in Store-and-forward mode (CUT_THRU_EN is set to 0 in Device Control 1 Register). Note: The Packet Trace and Filtering counters are incremented for each packet received. This implies that retried packets which match the trace or filter criteria will cause the counter to increment. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.25 Port {0..17} VC0 Transmitted Packets Dropped Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_PKT_DROP_TX_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40068 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets that have been dropped by the port's transmit logic. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.26 Port {0..17} VC0 TTL Packets Dropped Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_TTL_DROP_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF4006C + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets that have been dropped by the port's transmit logic because of TTL events. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

10.16.27 Port {0..17} VC0 CRC Limit Packets Dropped Counter Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_VC0_CRC_LIMIT_DROP_CNTR Reset Value: 0x0000_0000	Register Offset: 0xF40070 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	COUNT							
08:15	COUNT							
16:23	COUNT							
24:31	COUNT							

Bits	Name	Description	Type	Reset Value
0:31	COUNT	A saturating count of VC0 packets that have been dropped by the port's transmit logic because of CRC LIMIT events. Note: To enable this counter, set the Port {0..17} Operations Register[CNTRS_EN] bit.	RR	0

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10.16.28 Port {0..17} Congestion Retry Counter Register

Register Name: PORT_{0..17}_RETRY_CNTR Reset Value: 0xFFFF_0000	Register Offset: 0xF400CC + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	RETRY_LIM							
08:15	RETRY_LIM							
16:23	Reserved							
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:15	RETRY_LIM	Threshold value to trigger congested link partner recovery	RW	0xFFFF
16:31	Reserved	Reserved	RO	0

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10.16.29 Port {0..17} Status and Control Register

For base address information, see Port Function Registers.

Register Name: PORT_{0..17}_STATUS_AND_CTL Reset Value: 0x0000_0000	Register Offset: 0xF400F0 + (0x100 * port_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved					CLR_MANY_RETRY	RETRY_LIM_EN	RX_FC

Bits	Name	Description	Type	Reset Value
0:28	Reserved	Reserved	RO	0
29	CLR_MANY_RETRY	1 = This commands the port to exit the Drop Packet State (after a retry count threshold event)	WO	0
30	RETRY_LIM_EN	0 = Disable the congestion retry counter 1 = Enable the congestion retry counter	RW	0
31	RX_FC	0 = Transmitter-controlled flow control 1 = Receiver-controlled flow control	RO	0

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10.16.30 Broadcast Port Operations Register

The per-port version of this register is Port {0..17} Operations Register.

Register Name: BCAST_PORT_OPS Reset Value: 0x0000_0000	Register Offset: 0xF4FF04

Bits	0	1	2	3	4	5	6	7
00:07	Reserved		CRC_DIS	PORT_INT_EN	PORT_PW_EN	CNTRS_EN	SILENCE_CTL	
08:15	SILENCE_CTL		Reserved	FORCE_REINIT	TX_FLOW_CTL_DIS	Reserved	SELF_MCAST_EN	FILTER_3_EN
16:23	FILTER_2_EN	FILTER_1_EN	FILTER_0_EN	TRACE_3_EN	TRACE_2_EN	TRACE_1_EN	TRACE_0_EN	Reserved
24:31	TRACE_PW_EN	PORT_LOG_EN	LANE_LOG_EN	LT_LOG_EN	CRC_RETX_LIMIT			Reserved

Bits	Name	Description	Type	Reset Value
0:1	Reserved	Reserved	RO	0
2	CRC_DIS	0 = Perform normal packet CRC 1 = Packet CRC check reports valid CRC regardless of condition	WO	0
3	PORT_INT_EN	0 = Do not generate interrupt if an error is detected 1 = Generate interrupt if an error is detected	WO	0
4	PORT_PW_EN	0 = Do not generate port-write if an error is detected 1 = Generate port-write if an error is detected	WO	0
5	CNTRS_EN	0 = Disable port-level counters 1 = Enable port-level counters	RW	0
6:9	SILENCE_CTL	Changes the amount of time spent in the silent state of the port initialization state machine. Default is 120 microseconds. Each increment represents 13.1 microseconds of change.	WO	0
10	Reserved	Reserved	RW	0
11	FORCE_REINIT	1 = Force the initialization state machine back to the silent state. This causes the loss of the link.	WO	0
12	TX_FLOW_CTL_DIS	Transmitter-controlled flow control 0 = Enable 1 = Disable Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	WO	0
13	Reserved	Reserved	RO	0

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(Continued)

Bits	Name	Description	Type	Reset Value
14	SELF_MCAST_EN	0 = Disable 1 = Enable Note: If this port is included in any multicast mask, multicast packets received on this port will be multicast back out this port. If this bit is set, software must handle multicast back to itself. Note that multicasting packets back to the port that the packet was received on is contrary to the *RapidIO Specification (Rev. 2.1)*.	WO	0
15	FILTER_3_EN	0 = Disable filter comparison 3 1 = Enable filter	WO	0
16	FILTER_2_EN	0 = Disable filter comparison 2 1 = Enable filter	WO	0
17	FILTER_1_EN	0 = Disable filter comparison 1 1 = Enable filter	WO	0
18	FILTER_0_EN	0 = Disable filter comparison 0 1 = Enable filter	WO	0
19	TRACE_3_EN	0 = Disable TC Value 3 1 = Enable TC Value 3	WO	0
20	TRACE_2_EN	0 = Disable TC Value 2 1 = Enable TC Value 2	WO	0
21	TRACE_1_EN	0 = Disable TC Value 1 1 = Enable TC Value 1	WO	0
22	TRACE_0_EN	0 = Disable TC Value 0 1 = Enable TC Value 0	WO	0
23	Reserved	Reserved	WO	0
24	TRACE_PW_EN	0 = Do not generate a port-write on a trace match 1 = Generate a port-write on a trace match Note: This bit is active only if PORT_LOG_EN is set to 1.	WO	0
25	PORT_LOG_EN	0 = Disable error logging for port-level errors 1 = Enable error logging for port-level errors	WO	0
26	LANE_LOG_EN	0 = Disable error logging for lane-level errors 1 = Enable error logging for lane-level errors	WO	0
27	LT_LOG_EN	0 = Disable error logging for LT errors 1 = Enable error logging for LT errors	WO	0
28:30	CRC_RETX_LIMIT	0b000 = No retransmission limit 0b001–0b111 = The number of retransmissions allowed before packet is dropped.	WO	0b000

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Bits	Name	Description	Type	Reset Value
31	Reserved	Reserved	RO	0

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10.16.31 Broadcast Port Implementation Specific Error Detect Register

This register captures implementation specific physical layer errors. The per-port version of this register is Port {0..17} Implementation Specific Error Detect Register.

Register Name: BCAST_PORT_IMPL_SPEC_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0xF4FF08

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE	TTL_EVENT	CRC_EVENT	PNA	UNSOL_LR	UNEXP_ACKID	PNA_RETRY	RTE_ISSUE
08:15	Reserved	SET_ACKID	TX_DROP	MANY_RETRY	RX_DROP	Reserved	BAD_TT	SHORT
16:23	UNSOL_RFR	FATAL_TO	RETRY	RETRY_ACKID	STOMP_TO	RX_STOMP	LR_CMD	LR_X2
24:31	UNEXP_EOP	UNEXP_STOMP	PORT_INIT	PORT_WIDTH	IDLE_IN_PKT	LOA	BAD_CTL	REORDER

Bits	Name	Description	Type	Reset Value
0	ERR_RATE	1 = The port encountered a condition when the error rate has exceeded the programmed error rate threshold.	RW	0
1	TTL_EVENT	1 = A packet has been stored in the port output buffer for a period of time that exceeds the time to live timeout value. This also represents a dropped packet event.	RW	0
2	CRC_EVENT	1 = A CRC anomaly has been detected Possibilities include: • A packet has encountered a number of retries that has exceeded the programmed CRC limit and was dropped. • A packet was received with a CRC Error on a port that is configured for CRC Retransmission Suppression and was dropped.	RW	0
3	PNA	1 = Received a NACK with a cause other than lack of resources. The Port_n_Error register has a bit for all NACKs; however, the user may want to be able to turn off the counting of NACKs due to lack of resources (which some may view as not being an error). The methodology achieved with this bit is to turn off all NACKs via CS_NOT_ACC in the Port {0..17} Error Detect CSR so that the user can disable the counting of lack of resource NACKs (by disabling all NACKs at the Part 8 level), and then re-enable the counting of all other NACKs with this bit.	RW	0
4	UNSOL_LR	1 = Received an unexpected Link-Response	RW	0

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Bits	Name	Description	Type	Reset Value
5	UNEXP_ACKID	1 = Received an acknowledge control symbol with an unexpected ackID	RW	0
6	PNA_RETRY	1 = A packet could not be accepted because the RX buffers were full	RW	0
7	RTE_ISSUE	1 = A routing issue occurred. Possibilities include: • A packet was received that referenced the “no route” condition and was dropped • A packet was received that referenced a port which is disabled and was dropped • A packet was received that referenced an output port that is configured in Port Lockout mode (see Section 2.2 in the *RapidIO Specification (Rev. 2.1), Part 8*) • A packet was received that references an output port that is in the Fatal Error State	RW	0
8	Reserved	Reserved	RO	0
9	SET_ACKID	1 = A write to the Local ackID register used an invalid outstanding ackID field	RW	0
10	TX_DROP	1 = The port dropped a non-maintenance packet when the transmission of non-maintenance packets was disabled	RW	0
11	MANY_RETRY	1 = The port detected a retry count that triggered a link partner congestion event.	RW	0
12	RX_DROP	1 = Received a non-maintenance packet when the reception of non-maintenance packets was disabled. Note that the term “discard” refers to a NACK (as required by the Port {0..17} Control 1 CSR) when the input port is disabled. The packet is not dropped in terms of the dropped packet counter.	RW	0
13	Reserved	Reserved	RW	0
14	BAD_TT	1 = Received a packet with an invalid tt field	RW	0
15	SHORT	1 = A packet was received with only 32 bits of data between the packet delimiters	RW	0
16	UNSOL_RFR	1 = Received a restart from retry control symbol while the receiver was not in the Input-Retry Stopped state	RW	0
17	FATAL_TO	1 = A Link-Response was not received after 15 Link-Requests were transmitted, causing a fatal error	RW	0
18	RETRY	1 = Received a retry control symbol with a valid ackID	RW	0
19	RETRY_ACKID	1 = Received a retry control symbol with an unexpected ackID	RW	0

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Bits	Name	Description	Type	Reset Value
20	STOMP_TO	1 = Transmitted a STOMP control symbol but the link partner did not reply with a packet retry (or a packet NACK)	RW	0
21	RX_STOMP	1 = Received a STOMP control symbol	RW	0
22	LR_CMD	1 = Received a Link-Request with a reserved command field encoding	RW	0
23	LR_X2	1 = Received a second Link-Request before the Link-Response was transmitted for the first one	RW	0
24	UNEXP_EOP	1 = Received an EOP control symbol that did not terminate a packet	RW	0
25	UNEXP_STOMP	1 = Received a STOMP control symbol that did not terminate a packet	RW	0
26	PORT_INIT	1 = Indicates that port initialization acquired after completing the transmission of 15 Status control symbols	RW	0
27	PORT_WIDTH	1 = The maximum configured port width could not be initialized and the port selected a lower lane width	RW	0
28	IDLE_IN_PKT	1 = An IDLE character (K, A, R, M) was detected in a received packet	RW	0
29	LOA	1 = Alignment was lost	RW	0
30	BAD_CTL	1 = The sequence of received control characters indicates a protocol error. For example, in 4x mode the lane 0 character is a control character and there is one or more control characters present on the remaining lanes (excluding the case of an idle column). Also indicates in 1x mode that a control symbol has a control character present in the data segment.	RW	0
31	REORDER	1 = The port detected that lanes were reordered during port initialization because of information in the IDLE2 sequence	RW	0

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10.16.32 Broadcast Port Implementation Specific Error Rate Enable Register

This register allows the user to define when an implementation specific error is captured at a finer granularity. The per-port version of this register is Port {0..17} Implementation Specific Error Rate Enable Register.

Hot Extraction/Insertion support requires exclusive use of these registers. No Standard Physical Layer Errors can be enabled when Hot Extraction/Insertion functionality is required.

When an event is disabled in this register, the corresponding event in the Broadcast Port Implementation Specific Error Detect Register is not affected.

Register Name: BCAST_PORT_IMPL_SPEC_ERR_RATE_EN Reset Value: 0x0000_0000	Register Offset: 0xF4FF0C

Bits	0	1	2	3	4	5	6	7
00:07	ERR_RATE_EN	TTL_EVENT_EN	CRC_EVENT_EN	PNA_EN	UNSOL_LR_EN	UNEXP_ACKID_EN	PNA_RETRY_EN	RTE_ISSUE_EN
08:15	Reserved	SET_ACKID_EN	TX_DROP_EN	MANY_RETRY_EN	RX_DROP_EN	Reserved	BAD_TT_EN	SHORT_EN
16:23	UNSOL_RFR_EN	FATAL_TO_EN	RETRY_EN	RETRY_ACKID_EN	STOMP_TO_EN	RX_STOMP_EN	LR_CMD_EN	LR_X2_EN
24:31	UNEXP_EOP_EN	UNEXP_STOMP_EN	PORT_INIT_EN	PORT_WIDTH_EN	IDLE_IN_PKT_EN	LOA_EN	BAD_CTL_EN	REORDER_EN

Bits	Name	Description	Type	Reset Value
0	ERR_RATE_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
1	TTL_EVENT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
2	CRC_EVENT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
3	PNA_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
4	UNSOL_LR_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
5	UNEXP_ACKID_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
6	PNA_RETRY_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
7	RTE_ISSUE_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0

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Bits	Name	Description	Type	Reset Value
8	Reserved	Reserved	RO	0
9	SET_ACKID_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
10	TX_DROP_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
11	MANY_RETRY_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
12	RX_DROP_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
13	Reserved	Reserved	RW	0
14	BAD_TT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
15	SHORT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
16	UNSOL_RFR_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
17	FATAL_TO_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
18	RETRY_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
19	RETRY_ACKID_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
20	STOMP_TO_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
21	RX_STOMP_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
22	LR_CMD_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
23	LR_X2_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
24	UNEXP_EOP_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
25	UNEXP_STOMP_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0

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Bits	Name	Description	Type	Reset Value
26	PORT_INIT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
27	PORT_WIDTH_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
28	IDLE_IN_PKT_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
29	LOA_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
30	BAD_CTL_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0
31	REORDER_EN	1 = Enable the capture of the corresponding event in the Port {0..17} Implementation Specific Error Detect Register.	RW	0

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10.17 Implementation Specific Error Logging Registers

10.17.1 Error Log Register

Register Name: LOG_CTL Reset Value: 0x0000_0000	Register Offset: 0xFD0000

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved					LOG_TBL_OVERWRITE	CNTR_MAX_STOP	ALL_FLAG_STOP

Bits	Name	Description	Type	Reset Value
0:28	Reserved	Reserved	RO	0
29	LOG_TBL_OVERWRITE	0 = Discard further errors when the error log is full 1 = Overwrite the error log with new errors when it is full	RW	0
30	CNTR_MAX_STOP	0 = When the error counter reaches the maximum value, 0xFFFF, do not stop the error log function 1 = When the error counter reaches the maximum value, 0xFFFF, stop the error log function and generate a port-write packet	RW	0
31	ALL_FLAG_STOP	0 = When all error flags are asserted, do not stop the Error Management block 1 = When all error flags are asserted, stop the error log function and generate a port-write packet	RW	0

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10.17.2 Error Log Data Register

Register Name: LOG_DATA Reset Value: 0x0000_0000	Register Offset: 0xFD0004

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved	ERR_SOURCE						
24:31	ERR_GROUP				ERR_NUM			

Bits	Name	Description	Type	Reset Value
0:16	Reserved	Reserved	RO	0
17:23	ERR_SOURCE	Error source (7 bits)	RO	0
24:27	ERR_GROUP	Error group	RO	0
28:31	ERR_NUM	Error number	RO	0

10.18 Special Error Registers

10.18.1 Special Error Registers Base Addresses

Base Address	Associated Registers
0xFD0008	LOG_MATCH_0
0xFD000C	LOG_MATCH_1
0xFD0010	LOG_MATCH_2
0xFD0014	LOG_MATCH_3
0xFD0018	LOG_MATCH_4
0xFD001C	LOG_MATCH_5
0xFD0020	LOG_MATCH_6
0xFD0024	LOG_MATCH_7

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10.18.2 Error Log Match Register {0..7}

For base address information, see Special Error Registers.

Register Name: LOG_MATCH_{0..7} Reset Value: 0x0000_0000	Register Offset: 0xFD0008 + (0x4 * reg_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved	ERR_SOURCE_MASK	ERR_GROUP_MASK	ERR_NUM_MASK	CNT_EN	FLAG_EN	MAINT_PKT_EN	STOP_EN
16:23	Reserved	ERR_SOURCE						
24:31	ERR_GROUP				ERR_NUM			

Bits	Name	Description	Type	Reset Value
0:8	Reserved	Reserved	RO	0
9	ERR_SOURCE_MASK	0 = Compare the error source 1 = Do not compare the error source	RW	0
10	ERR_GROUP_MASK	0 = Compare the error group 1 = Do not compare the error group	RW	0
11	ERR_NUM_MASK	0 = Compare the error number 1 = Do not compare the error number	RW	0
12	CNT_EN	1 = Enable counting the error	RW	0
13	FLAG_EN	1 = Enable flagging the error and generating an interrupt	RW	0
14	MAINT_PKT_EN	1 = Enable the generation of a port-write packet for each received event	RW	0
15	STOP_EN	1 = Enable stopping the error log function and generation of a port-write packet	RW	0
16	Reserved	Reserved	RO	0
17:23	ERR_SOURCE	Error Source (7 bits)	RW	0
24:27	ERR_GROUP	Error Group. Most significant 4 bits of Event Code.	RW	0
28:31	ERR_NUM	Error Number. Least significant 4 bits of Event Code.	RW	0

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10.18.3 Error Log Match Status Register

Register Name: LOG_MATCH_STATUS Reset Value: 0x0000_0000	Register Offset: 0xFD0028

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	FLAG_ERR_7	FLAG_ERR_6	FLAG_ERR_5	FLAG_ERR_4	FLAG_ERR_3	FLAG_ERR_2	FLAG_ERR_1	FLAG_ERR_0

Bits	Name	Description	Type	Reset Value
0:23	Reserved	Reserved	RO	0
24	FLAG_ERR_7	Asserted to indicate an error applies to Register 7 in Error Log Match Register {0..7}. This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
25	FLAG_ERR_6	Asserted to indicate an error applies to Register 6 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
26	FLAG_ERR_5	Asserted to indicate an error applies to Register 5 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
27	FLAG_ERR_4	Asserted to indicate an error applies to Register 4 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
28	FLAG_ERR_3	Asserted to indicate an error applies to Register 3 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
29	FLAG_ERR_2	Asserted to indicate an error applies to Register 2 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
30	FLAG_ERR_1	Asserted to indicate an error applies to Register 1 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0
31	FLAG_ERR_0	Asserted to indicate an error applies to Register 0 in Error Log Match Register {0..7}). This field can be reset by FLAG_RESET in the Error Log Control 2 Register.	RR	0

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10.18.4 Error Log Events Register

Register Name: LOG_EVENTS Reset Value: 0x0000_0000	Register Offset: 0xFD002C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	CNT							
24:31	CNT							

Bits	Name	Description	Type	Reset Value
0:15	Reserved	Reserved	RO	0
16:31	CNT	Error log event count. If the counter reaches its maximum value of 0xFFFF it will stop incrementing, and remain at its maximum value until it is reset. CNT is reset when the Error Manager is reset, or CNT_RESET is set in the Error Log Control 2 Register.	RO	0

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10.18.5 Error Log Control 2 Register

Register Name: LOG_CTL2 Reset Value: 0x0000_0000	Register Offset: 0xFD0030

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved		STOP_EM	MAINT_PKT_DIS	ERR_FIFO_RESET	CNT_RESET	FLAG_RESET	Reserved

Bits	Name	Description	Type	Reset Value
0:25	Reserved	Reserved	RO	0
26	STOP_EM	0 = Enable error management 1 = Stop error management. Disable all IDT maintenance packet port-writes, including those resulting from trace matches. Note: When set to 1, it does not affect standard S-RIO port-writes.	RW	0
27	MAINT_PKT_DIS	0 = Generation of the maintenance packets (for error logging/reporting -- type 2) is enabled 1 = Generation of the maintenance packets (for error logging/reporting -- type 2) is disabled Note: The port-write due to trace match is not impacted by this bit.	RW	0
28	ERR_FIFO_RESET	1 = Reset the error FIFO	RW	0
29	CNT_RESET	1 = Reset the error count register	RW	0
30	FLAG_RESET	1 = Reset the flag register	RW	0
31	Reserved	Reserved	RO	0

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10.19 PLL Registers

10.19.1 PLL Register Base Addresses

PLL Domain	Address
0	0xFF0000
1	0xFF0010
2	0xFF0020
3	0xFF0030
4	0xFF0040
5	0xFF0050
6	0xFF0060
7	0xFF0070
8	0xFF0080
9	0xFF0090
10	0xFF00A0
11	0xFF00B0

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10.19.2 PLL {0..11} Control 1 Register

For base address information, see PLL Registers. The broadcast version of this register is Broadcast PLL Control Register.

When a port or lane configuration operation occurs, IDT recommends a subsequent port re-initialization or reset (for more information, see Port Reconfiguration Operations).

Register Name: PLL_{0..11}_CTL_1 Reset Value: Undefined	Register Offset: 0xFF0000 + (0x10 * pll_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved						PLL_PWR_DOWN	PLL_DIV_SEL

Bits	Name	Description	Type	Reset Value
0:29	Reserved	Reserved	RO	0
30	PLL_PWR_DOWN	1 = Remove power from the PLL	RW	0
31	PLL_DIV_SEL	Selects (6.25 Gbaud, 3.125 Gbaud) or (5 Gbaud, 2.5 Gbaud, 1.25 Gbaud). The default value depends on the SPD[2] pin. 0 = 5.0, 2.5, 1.25 Gbaud 1 = 6.25, 3.125 Gbaud Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow. Note: The initial value of this field is determined by the setting of the SPD[2] external pin.	RW	Undefined

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10.19.3 PLL {0..11} Control 2 Register

For base address information, see PLL Registers.

Register Name: PLL_{0..11}_CTL_2 Reset Value: 0x0000_0001	Register Offset: 0xFF0004 + (0x10 * pll_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved						PLL_AUTO_RESET	Reserved

Bits	Name	Description	Type	Reset Value
0:29	Reserved	Reserved	RO	0
30	PLL_AUTO_RESET	1 = Pulse occurred on PLL auto reset output	RR	0
31	Reserved	Reserved	RO	1

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10.19.4 Broadcast PLL Control Register

The per-port version of this register is PLL {0..11} Control 1 Register.

Register Name: BCAST_PLL_CTL Reset Value: Undefined	Register Offset: 0xFF0FF0

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							PLL_DIV_SEL

Bits	Name	Description	Type	Reset Value
0:30	Reserved	Reserved	RO	0
31	PLL_DIV_SEL	Selects (6.25 Gbaud, 3.125 Gbaud) or (5 Gbaud, 2.5 Gbaud, 1.25 Gbaud). The default value depends on the SPD[2] pin. 0 = 5.0, 2.5, 1.25 Gbaud 1 = 6.25, 3.125 Gbaud Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow. Note: The initial value of this field is determined by the setting of the SPD[2] external pin.	RW	Undefined

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10.20 Lane Control Registers

10.20.1 Lane Control Base Addresses

Lane	Address
0	0xFF8000
1	0xFF8100
2	0xFF8200
3	0xFF8300
4	0xFF8400
5	0xFF8500
6	0xFF8600
7	0xFF8700
8	0xFF8800
9	0xFF8900
10	0xFF8A00
11	0xFF8B00
12	0xFF8C00
13	0xFF8D00
14	0xFF8E00
15	0xFF8F00
16	0xFF9000
17	0xFF9100
18	0xFF9200
19	0xFF9300
20	0xFF9400
21	0xFF9500
22	0xFF9600
23	0xFF9700
24	0xFF9800
25	0xFF9900
26	0xFF9A00
27	0xFF9B00

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Lane	Address
28	0xFF9C00
29	0xFF9D00
30	0xFF9E00
31	0xFF9F00
32	0xFFA000
33	0xFFA100
34	0xFFA200
35	0xFFA300
36	0xFFA400
37	0xFFA500
38	0xFFA600
39	0xFFA700
40	0xFFA800
41	0xFFA900
42	0xFFAA00
43	0xFFAB00
44	0xFFAC00
45	0xFFAD00
46	0xFFAE00
47	0xFFAF00

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10.20.2 Lane {0..47} Control Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane Control Register.

Register Name: LANE_{0..47}_CTL Reset Value: Undefined	Register Offset: 0xFF8000 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved			PRBS_MODE				Reserved
08:15	PRBS_UNIDIR_BERT_MODE_EN	LANE_INT_EN	LANE_PW_EN	PRBS_TRAIN	PRBS_EN	XMITPRBS	PRBS_RX_CHECKER_MODE	Reserved
16:23	LPBK_10BIT_EN	LPBK_8BIT_EN	Reserved	TX_SYMBOL_CTL		TX_AMP_CTL		
24:31	TX_AMP_CTL			TX_RATE		RX_RATE		LANE_DIS

Bits	Name	Description	Type	Reset Value
0:2	Reserved	Reserved	RO	0
3:6	PRBS_MODE	Select PRBS polynomial 0b0000 = $X^{23}+X^{18}+1$ 0b0001 = $X^{31}+X^{28}+1$ 0b0010 = Reserved (Revision C only) 0b0010 = Recirculating seed (Revision A/B only) 0b0011 = $X^{10}+X^{7}+1$ 0b0100 = $X^{15}+X^{14}+1$ 0b0101 = $X^{7}+X^{6}+1$ 0b0110 = 10-bit pattern – fixed 0b0111 = Balanced pattern – fixed 10-bit pattern and its inverse (pattern, ~pattern) 0b1000 = 40-bit pattern (0b0000000000, 10-bit fixed pattern, 0b1111111111, ~ pattern) 0b1001–1111 = Reserved Note: For 8-bit mode, 0b0110, 0b0111, and 0b1000 are supported for PRBS generation only.	RW	0b0000
7	Reserved	Reserved	RO	0

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Bits	Name	Description	Type	Reset Value
8	PRBS_UNIDIR_BERT_MODE_EN	When PRBS is enabled, this bit enables testing with a non S-RIO based BERT function. The 10-bit PRBS generator will be used and the 8b/10b encoder will be bypassed. 0 = Disable 1 = Enable Note: For more information, see User-Defined Patterns.	RW	0
9	LANE_INT_EN	0 = Do not generate interrupt on lane-level error detect 1 = Generate interrupt on lane-level error detect	RW	0
10	LANE_PW_EN	0 = Do not generate port-write on error detect 1 = Generate port-write on error detect	RW	0
11	PRBS_TRAIN	PRBS RX training mode 0 = Disable 1 = Enable Note: Errors are not reported when in training mode.	RW	0
12	PRBS_EN	Enable load of initial PRBS seed from CSR 0 = Disable PRBS 1 = Enable load	RW	0
13	XMITPRBS	Select data source to transmit 0 = Normal data 1 = PRBS data	RW	0
14	PRBS_RX_CHECKER_MODE	0 = Enable 8-bit RX PRBS checker 1 = Enable 10-bit RX PRBS checker Note: This bit is applicable to Revision C only.	RW	0
15	Reserved	Reserved	RW	0
16	LPBK_10BIT_EN	Loopback enable at the 10-bit boundary within Lane *n* 0 = Disable 1 = Enable For more information, see 10-bit Loopback Mode.	RW	0
17	LPBK_8BIT_EN	Loopback enable at the 8-bit boundary within Lane *n* 0 = Disable 1 = Enable For more information, see 8-bit Loopback Mode.	RW	0
18	Reserved	Reserved	RW	0

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Bits	Name	Description	Type	Reset Value
19:20	TX_SYMBOL_CTL	This controls the slew rate of the transmitter. 0b00 = Slowest transitions 0b11 = Fastest transitions Note: This field is recommended to be always set to 0b11.	RW	0b11
21:26	TX_AMP_CTL	Selects the local SerDes drive strength. Default is long run. The low end of the long run range d'40. Short run nominal depends on link speed. If above 5 Gbaud, short run nominal is d'28. If below 5 Gbaud, short run nominal is d'32. Note: To enable write access to this field, set AMP_PROG_EN to 1 in the Lane {0..47} Status 3 CSR.	RW	0b110100
27:28	TX_RATE	These bits in conjunction with the PLL_DIV_SEL bit in the PLL {0..11} Control 1 Register determine the transfer rate of the lane. PLL_DIV_SEL = 0 0b00 = 1.25 Gbaud 0b01 = 2.5 Gbaud 0b1X = 5.0 Gbaud PLL_DIV_SEL = 1 0b00 = RES 0b01 = 3.125 Gbaud 0b1X = 6.25 Gbaud Default is configured with the value of the external SPD[1:0] signals Note: It is a programming error to set the value of this field differently from the value of RX_RATE. Note: The initial value of this field is determined by the setting of the SPD[1:0] external pins. Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	Undefined

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Bits	Name	Description	Type	Reset Value
29:30	RX_RATE	These bits in conjunction with the PLL_DIV_SEL bit in the PLL {0..11} Control 1 Register register determine the receive rate of the lane. PLL_DIV_SEL = 0 0b00 = 1.25 Gbaud 0b01 = 2.5 Gbaud 0b1X = 5.0 Gbaud PLL_DIV_SEL = 1 0b00 = Reserved 0b01 = 3.125 Gbaud 0b1X = 6.25 Gbaud The default is configured with the value of the external SPD[1:0] signals. Note: It is a programming error to set the value of this field differently from the value of TX_RATE. Note: The initial value of this field is determined by the setting of the SPD[1:0] external pins. Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	Undefined
31	LANE_DIS	Power down Lane *n* 0 = Lane *n* enabled (not powered down) 1 = Lane *n* is disabled Note: Lane 0 of a port should only be disabled if all lanes of a port are unused. Note: Changing the state of the LANE_DIS bit will require a re-initialization or reset. Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	0

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10.20.3 Lane {0..47} PRBS Generator Seed Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane PRBS Generator Seed Register.

Register Name: LANE_{0..47}_PRBS_GEN_SEED Reset Value: 0x7FFF_FFFF	Register Offset: 0xFF8004 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved	PRBS_SEED						
08:15	PRBS_SEED							
16:23	PRBS_SEED							
24:31	PRBS_SEED							

Bits	Name	Description	Type	Reset Value
0	Reserved	Reserved	RO	0
1:31	PRBS_SEED	Seed value for PRBS generation. It can be used for polynomial seed or as the actual data depending on the value of PRBS_MODE in Lane {0..47} Control Register. Note: The polynomial seed must be set to a non-zero value in order for the PRBS generator to work as intended. In addition, at least one of the bits between the highest power of the selected polynomial and index 0 must be set to 1 to guarantee proper pseudo-random generation.	RW	0x7FFFFFFF

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10.20.4 Lane {0..47} PRBS Error Counter Register

Register Name: LANE_{0..47}_PRBS_ERR_CNTR Reset Value: 0x0000_0000	Register Offset: 0xFF8008 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							PRBS_ERR
24:31	PRBS_ERR_CNT							

Bits	Name	Description	Type	Reset Value
0:22	Reserved	Reserved	RO	0
23	PRBS_ERR	1 = A PRBS error occurred	RR	0
24:31	PRBS_ERR_CNT	PRBS error counter for this lane.	RR	0

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10.20.5 Lane {0..47} Error Detect Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane Error Detect Register.

Register Name: LANE_{0..47}_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0xFF800C + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED	LANE_INVER_DET
24:31	IDLE2_FRAME	Reserved		TX_RX_MISMATCH	DESCRAM_SYNC	BAD_CHAR	LANE_RDY	LANE_SYNC

Bits	Name	Description	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED	1 = A link speed was requested that is not supported because of the PLL configuration.	RW	0
23	LANE_INVER_DET	1 = A lane polarity inversion was detected and compensated for; only reported when correction is applied.	RW	0
24	IDLE2_FRAME	1 = An error was detected with the received IDLE2 frame.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH	1 = The link partner receiver and local transmitter mismatched, long/short.	RW	0
28	DESCRAM_SYNC	1 = Loss of receiver descrambler synchronization occurred while receiving scrambled control symbol and packet data.	RW	0
29	BAD_CHAR	1 = A character that was received was not in the valid set of characters. This could be an illegal special character or a code group with no valid decoding.	RW	0
30	LANE_RDY	1 = Lane ready was lost but sync remained high.	RW	0
31	LANE_SYNC	1 = Lane sync was lost.	RW	0

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10.20.6 Lane {0..47} Error Rate Enable Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane Error Rate Enable Register.

Register Name: LANE_{0..47}_ERR_RATE_EN Reset Value: 0x0000_0000	Register Offset: 0xFF8010 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED_EN	LANE_INVER_DET_EN
24:31	IDLE2_FRAME_EN	Reserved		TX_RX_MISMATCH_EN	DESCRAM_SYNC_EN	BAD_CHAR_EN	LANE_RDY_EN	LANE_SYNC_EN

Bits	Name	Description[a]	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED_EN	0 = Disable 1 = Enable capturing that a link speed was requested that is not supported because of the PLL configuration.	RW	0
23	LANE_INVER_DET_EN	0 = Disable 1 = Enable capturing that a lane polarity inversion was detected and compensated for; only reported when correction is applied.	RW	0
24	IDLE2_FRAME_EN	0 = Disable 1 = Enable capturing that an error was detected within the received IDLE2 frame.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH_EN	0 = Disable 1 = Enable capturing that the link partner receiver and local transmitter mismatched, long/short.	RW	0
28	DESCRAM_SYNC_EN	0 = Disable 1 = Enable capturing of loss of receiver descrambler synchronization while receiving scrambled control symbol and packet data.	RW	0

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Bits	Name	Description[a]	Type	Reset Value
29	BAD_CHAR_EN	0 = Disable 1 = Enable capturing that a character that was received was not in the valid set of characters. This could be an illegal special character or a code group with no valid decoding.	RW	0
30	LANE_RDY_EN	0 = Disable 1 = Enable capturing that Lane ready was lost but sync remained high.	RW	0
31	LANE_SYNC_EN	0 = Disable 1 = Enable capturing that Lane sync was lost.	RW	0

a. When a bit in this register is set, it enables Port {0..17} Error Rate CSR.ERR_RATE_CNTR to increment.

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10.20.7 Lane {0..47} Attributes Capture Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane Attributes Capture Register.

Register Name: LANE_{0..47}_ATTR_CAPT Reset Value: 0x0000_0000	Register Offset: 0xFF8014 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	INFO_TYPE			ERR_TYPE				
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							VALID

Bits	Name	Description	Type	Reset Value
0:2	INFO_TYPE	Type of logged information 0b000 = Packet 0b001 = Reserved 0b010 = Short control symbol (only Lane {0..47} Data Capture 0 Register is valid) 0b011 = Long control symbol (only Lane {0..47} Data Capture 0 Register and Lane {0..47} Data Capture 1 Register are valid) 0b100 = Implementation-specific data is logged 0b101–0b111 = Reserved	RW	0
3:7	ERR_TYPE	The encoded value of the bit in the Lane {0..47} Error Detect Register that describes the error captured in Lane {0..47} Data Capture 0 Register and Lane {0..47} Data Capture 1 Register. For example: 31 - 10 (UNEXP_ACKID, bit 10) = 21 -> 0b10101. Note: The actual bit numbering of the encoded value is ERR_TYPE.	RW	0b00000
8:30	Reserved	Reserved	RO	0
31	VALID	1 = Lane capture registers contain valid information.	RW	0

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10.20.8 Lane {0..47} Data Capture 0 Register

For base address information, see Lane Control Registers.

Register Name: LANE_{0..47}_DATA_CAPT_0 Reset Value: 0x0000_0000	Register Offset: 0xFF8018 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_DATA							
08:15	CAPT_DATA							
16:23	CAPT_DATA							
24:31	CAPT_DATA							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_DATA	Captured data as defined in Lane Events.	RW	0

10.20.9 Lane {0..47} Data Capture 1 Register

For base address information, see Lane Control Registers.

Register Name: LANE_{0..47}_DATA_CAPT_1 Reset Value: 0x0000_0000	Register Offset: 0xFF801C + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	CAPT_DATA							
08:15	CAPT_DATA							
16:23	CAPT_DATA							
24:31	CAPT_DATA							

Bits	Name	Description	Type	Reset Value
0:31	CAPT_DATA	Captured data as defined in Lane Events.	RW	0

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10.20.10 Lane {0..47} DFE 1 Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane DFE 1 Register.

Register Name: LANE_{0..47}_DFE_1 Reset Value: 0x0004_0555	Register Offset: 0xFF8028 + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved			UNUSED		RX_DFE_DIS	TAP_OFFSET_SEL	TAP_4_SEL
16:23	TAP_3_SEL	TAP_2_SEL	TAP_1_SEL	TAP_0_SEL	Reserved			
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:10	Reserved	Reserved	RO	0
11:12	UNUSED	Reserved	RW	0
13	RX_DFE_DIS	Revision B and later devices 1 = Disable RX DFE Revision A device 1 = Enable RX DFE Supported combinations include: • RX_DFE_DIS = 1, TAP_x_SEL = 0: Received signal is not modified by DFE and coefficient updates cannot be written to the register fields. • RX_DFE_DIS = 1, TAP_x_SEL = 1: Coefficients can be written into registers but updates will have no effect on the received signal when LANE_{0..47}_DFE_2.CFG_EN transitions from 0 to 1. • RX_DFE_DIS = 0, TAP_x_SEL = 1: Coefficients can be written into registers and updates will have an effect on the received signal when LANE_{0..47}_DFE_2.CFG_EN transitions from 0 to 1.	RW	1
14	TAP_OFFSET_SEL	1 = Enable register adjustment of TAP_OFFSET Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
15	TAP_4_SEL	1 = Enable register adjustment of Tap 4 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
16	TAP_3_SEL	1 = Enable register adjustment of Tap 3 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0

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Bits	Name	Description	Type	Reset Value
17	TAP_2_SEL	1 = Enable register adjustment of Tap 2 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
18	TAP_1_SEL	1 = Enable register adjustment of Tap 1 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
19	TAP_0_SEL	1 = Enable register adjustment of Tap 0 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
20:31	Reserved	Reserved	RW	0x555

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10.20.11 Lane {0..47} DFE 2 Register

For base address information, see Lane Control Registers. The broadcast version of this register is Broadcast Lane DFE 2 Register.

Register Name: LANE_{0..47}_DFE_2 Reset Value: 0x1048_8010	Register Offset: 0xFF802C + (0x100 * lane_num)

Bits	0	1	2	3	4	5	6	7
00:07	Reserved			TAP_OFFSET_CFG				
08:15	TAP_OFFSET_CFG	TAP_4_CFG			TAP_3_CFG			
16:23	TAP_2_CFG					TAP_1_CFG		
24:31	TAP_1_CFG			TAP_0_CFG				CFG_EN

Bits	Name	Description	Type	Reset Value
0:2	Reserved	Reserved	RO	0
3:8	TAP_OFFSET_CFG	DC differential offset cancellation. IDT recommends that this field not be changed from the reset default value. • Most significant bit is a sign bit, with 1 meaning “positive” and 0 meaning “negative” • Positive values range from 0b100000 (Positive 0) up to 0b111111 (+31) • Negative values range from 0b011111 (-1) down to 0b000001 (-31)	RW	0b100000
9:11	TAP_4_CFG	Tap 4 is the coefficient used to adjust the signal based on the value of the bit received 4 bits before the current bit. • Most significant bit is a sign bit, with 1 meaning “positive” and 0 meaning “negative” • Positive values range from 0b100 (Positive 0) up to 0b111 (+3) • Negative values range from 0b011 (-1) down to 0b001 (-3) • 0b000 is undefined	RW	0b100
12:15	TAP_3_CFG	Tap 3 is the coefficient used to adjust the received signal based on the value of the bit received 3 bits before the current bit. • Most significant bit is a sign bit, with 1 meaning “positive” and 0 meaning “negative” • Positive values range from 0b1000 (Positive 0) up to 0b1111 (+7) • Negative values range from 0b0111 (-1) down to 0b0001 (-7) • 0b0000 is undefined	RW	0b1000

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Bits	Name	Description	Type	Reset Value
16:20	TAP_2_CFG	Tap 2 is the coefficient used to adjust the received signal based on the value of the bit received 2 bits before the current bit. • Most significant bit is a sign bit, with 1 meaning “positive” and 0 meaning “negative” • Positive values range from 0b10000 (Positive 0) up to 0b11111 (+15) • Negative values range from 0b01111 (-1) down to 0b00001 (-15) • 0b00000 is undefined	RW	0b10000
21:26	TAP_1_CFG	Tap 1 is the coefficient used to adjust the received signal based on the value of the bit received immediately before the current bit. • Positive values range from 0b000000 (0) up to 0b011111 (+31) • Values 0b100000–0b111111 are equivalent to +31.	RW	0b000000
27:30	TAP_0_CFG	Tap 0 is a Variable Gain Amplifier. The values range from 0 up to +15.	RW	0b1000
31	CFG_EN	Load coefficient output values into DFE DACs based on “_CFG” register fields when this field transitions from 0 to 1. Note: The values of all taps are programmed into the DFE DACs when this bit transitions from 0 to 1, regardless of the value of the “_SEL” bits in the Lane {0..47} DFE 1 Register. The DFE DACs have no effect on the received signal if RX_DFE_DIS = 1 in the same register.	RW	0

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10.20.12 Broadcast Lane Control Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} Control Register.

Register Name: BCAST_LANE_CTL Reset Value: Undefined	Register Offset: 0xFFFF00

Bits	0	1	2	3	4	5	6	7
00:07	Reserved			PRBS_MODE				Reserved
08:15	PRBS_UNIDIR_BERT_MODE_EN	LANE_INT_EN	LANE_PW_EN	PRBS_TRAIN	PRBS_EN	XMITPRBS	PRBS_RX_CHECKER_MODE	Reserved
16:23	LPBK_10BIT_EN	LPBK_8BIT_EN	Reserved	TX_SYMBOL_CTL		TX_AMP_CTL		
24:31	TX_AMP_CTL			TX_RATE		RX_RATE		LANE_DIS

Bits	Name	Description	Type	Reset Value
0:2	Reserved	Reserved	RO	0
3:6	PRBS_MODE	Select PRBS polynomial 0b0000 = $X^{23}+X^{18}+1$ 0b0001 = $X^{31}+X^{28}+1$ 0b0010 = Reserved (Revision C only) 0b0010 = Recirculating seed (Revision A/B only) 0b0011 = $X^{10}+X^{7}+1$ 0b0100 = $X^{15}+X^{14}+1$ 0b0101 = $X^{7}+X^{6}+1$ 0b0110 = 10-bit pattern – fixed 0b0111 = Balanced pattern – fixed 10-bit pattern and its inverse (pattern, ~pattern) 0b1000 = 40-bit pattern (0b0000000000, 10-bit fixed pattern, 0b1111111111, ~ pattern) 0b1001–1111 = Reserved Note: For 8-bit mode, 0b0110, 0b0111, and 0b1000 are supported for PRBS generation only.	RW	0b0000
7	Reserved	Reserved	RO	0

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Bits	Name	Description	Type	Reset Value
8	PRBS_UNIDIR_BERT_MODE_EN	When PRBS is enabled, this bit enables testing with a non S-RIO based BERT function. The 10-bit PRBS generator will be used and the 8b/10b encoder will be bypassed. 0 = Disable 1 = Enable Note: For more information, see User-Defined Patterns.	RW	0
9	LANE_INT_EN	0 = Do not generate interrupt on lane-level error detect 1 = Generate interrupt on lane-level error detect	RW	0
10	LANE_PW_EN	0 = Do not generate port-write on error detect 1 = Generate port-write on error detect	RW	0
11	PRBS_TRAIN	0 = Disable PRBS RX training mode 1 = Enable PRBS RX training mode Note: Errors are not reported when in training mode.	RW	0
12	PRBS_EN	Enable load of initial PRBS seed from CSR 0 = Disable PRBS 1 = Enable load	RW	0
13	XMITPRBS	Select data source to transmit 0 = Normal data 1 = PRBS data	RW	0
14	PRBS_RX_CHECKER_MODE	0 = Enable 8-bit RX PRBS checker 1 = Enable 10-bit RX PRBS checker Note: This bit is applicable to Revision C only.	RW	0
15	Reserved	Reserved	RW	0
16	LPBK_10BIT_EN	Loopback enable at the 10-bit boundary within Lane *n* 0 = Disable 1 = Enable For more information, see 10-bit Loopback Mode.	RW	0
17	LPBK_8BIT_EN	Loopback enable at the 8-bit boundary within Lane *n* 0 = Disable 1 = Enable For more information, see 8-bit Loopback Mode.	RW	0
18	Reserved	Reserved	RW	0

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Bits	Name	Description	Type	Reset Value
19:20	TX_SYMBOL_CTL	This controls the slew rate of the transmitter. 0b00 = Slowest transitions 0b11 = Fastest transitions Note: This field is recommended to be always set to 0b11.	RW	0b00
21:26	TX_AMP_CTL	Selects the local SerDes drive strength. Default is long run. The low end of the long run range d'40. Short run nominal depends on link speed. If above 5 Gbaud, short run nominal is d'28. If below 5 Gbaud, short run nominal is d'32. Note: To enable write access to this field, set AMP_PROG_EN to 1 in the Lane {0..47} Status 3 CSR.	RW	0b110100
27:28	TX_RATE	These bits in conjunction with the PLL_DIV_SEL bit in the PLL {0..11} Control 1 Register determine the transfer rate of the lane. PLL_DIV_SEL = 0 0b00 = 1.25 Gbaud 0b01 = 2.5 Gbaud 0b1X = 5.0 Gbaud PLL_DIV_SEL = 1 0b00 = RES 0b01 = 3.125 Gbaud 0b1X = 6.25 Gbaud Default is configured with the value of the external SPD[1:0] signals Note: It is a programming error to set the value of this field differently from the value of RX_RATE. Note: The initial value of this field is determined by the setting of the SPD[1:0] external pins. Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	Undefined

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Bits	Name	Description	Type	Reset Value
29:30	RX_RATE	These bits in conjunction with the PLL_DIV_SEL bit in the PLL {0..11} Control 1 Register register determine the receive rate of the lane. PLL_DIV_SEL = 0 0b00 = 1.25 Gbaud 0b01 = 2.5 Gbaud 0b1X = 5.0 Gbaud PLL_DIV_SEL = 1 0b00 = Reserved 0b01 = 3.125 Gbaud 0b1X = 6.25 Gbaud The default is configured with the value of the external SPD[1:0] signals. Note: It is a programming error to set the value of this field differently from the value of TX_RATE. Note: The initial value of this field is determined by the setting of the SPD[1:0] external pins. Note: Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	Undefined
31	LANE_DIS	Power down Lane *n* 0 = Lane *n* enabled (not powered down) 1 = Lane *n* is disabled Note: Lane 0 of a port should only be disabled if all lanes of a port are unused. Note: Changing the state of the LANE_DIS bit will require a re-initialization or reset. Before changing this field value, see Port Reconfiguration Operations for the correct procedure to follow.	RW	0

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10.20.13 Broadcast Lane PRBS Generator Seed Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} PRBS Generator Seed Register.

Register Name: BCAST_LANE_GEN_SEED Reset Value: 0x0000_0000	Register Offset: 0xFFFF04

Bits	0	1	2	3	4	5	6	7
00:07	Reserved	PRBS_SEED						
08:15	PRBS_SEED							
16:23	PRBS_SEED							
24:31	PRBS_SEED							

Bits	Name	Description	Type	Reset Value
0	Reserved	Reserved	RO	0
1:31	PRBS_SEED	Seed value for PRBS generation. It can be used for polynomial seed or as the actual data depending on the value of PRBS_MODE in Broadcast Lane Control Register. Note: The polynomial seed must be set to a non-zero value in order for the PRBS generator to work as intended. In addition, at least one of the bits between the highest power of the selected polynomial and index 0 must be set to 1 to guarantee proper pseudo-random generation. Note: The reset value of this broadcast register is irrelevant to device functionality.	RW	0

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10.20.14 Broadcast Lane Error Detect Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} Error Detect Register.

Register Name: BCAST_LANE_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0xFFFF0C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED	LANE_INVER_DET
24:31	IDLE2_FRAME	Reserved		TX_RX_MISMATCH	DESCRAM_SYNC	BAD_CHAR	LANE_RDY	LANE_SYNC

Bits	Name	Description	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED	1 = A link speed was requested that is not supported because of the PLL configuration.	RW	0
23	LANE_INVER_DET	1 = A lane polarity inversion was detected and compensated for; only reported when correction is applied.	RW	0
24	IDLE2_FRAME	1 = An error was detected with the received IDLE2 frame.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH	1 = The link partner receiver and local transmitter mismatched, long/short.	RW	0
28	DESCRAM_SYNC	1 = Loss of receiver descrambler synchronization occurred while receiving scrambled control symbol and packet data.	RW	0
29	BAD_CHAR	1 = A character that was received was not in the valid set of characters. This could be an illegal special character or a code group with no valid decoding.	RW	0
30	LANE_RDY	1 = Lane ready was lost but sync remained high. LANE_RDY = LANE_SYNC and rcvr_trained (internal signal) rcvr_trained is de-asserted when the local lane receiver controls adaptive equalization in the receiver (not applicable to the CPS-1848), and/or the connected lane transmitter and the training of the equalization in either the lane receiver or the connected lane transmitter through IDLE2 commands has not been completed. Otherwise, asserted.	RW	0
31	LANE_SYNC	1 = Lane sync was lost.	RW	0

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10.20.15 Broadcast Lane Error Rate Enable Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} Error Rate Enable Register.

Register Name: BCAST_LANE_ERR_RATE_EN Reset Value: 0x0000_0000	Register Offset: 0xFFFF10

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved			UNUSED			BAD_SPEED_EN	LANE_INVER_DET_EN
24:31	IDLE2_FRAME_EN	Reserved		TX_RX_MISMATCH_EN	DESCRAM_SYNC_EN	BAD_CHAR_EN	LANE_RDY_EN	LANE_SYNC_EN

Bits	Name	Description[a]	Type	Reset Value
0:18	Reserved	Reserved	RO	0
19:21	UNUSED	Reserved	RW	0
22	BAD_SPEED_EN	0 = Disable 1 = Enable capturing that a link speed was requested that is not supported because of the PLL configuration.	RW	0
23	LANE_INVER_DET_EN	0 = Disable 1 = Enable capturing that a lane polarity inversion was detected and compensated for; only reported when correction is applied.	RW	0
24	IDLE2_FRAME_EN	0 = Disable 1 = Enable capturing that an error was detected within the received IDLE2 frame.	RW	0
25:26	Reserved	Reserved	RW	0
27	TX_RX_MISMATCH_EN	0 = Disable 1 = Enable capturing that the link partner receiver and local transmitter mismatched, long/short.	RW	0
28	DESCRAM_SYNC_EN	0 = Disable 1 = Enable capturing of loss of receiver descrambler synchronization while receiving scrambled control symbol and packet data.	RW	0

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Bits	Name	Description[a]	Type	Reset Value
29	BAD_CHAR_EN	0 = Disable 1 = Enable capturing that a character that was received was not in the valid set of characters. This could be an illegal special character or a code group with no valid decoding.	RW	0
30	LANE_RDY_EN	0 = Disable 1 = Enable capturing that Lane ready was lost but sync remained high.	RW	0
31	LANE_SYNC_EN	0 = Disable 1 = Enable capturing that Lane sync was lost.	RW	0

a. When a bit in this register is set, it enables Port {0..17} Error Rate CSR.ERR_RATE_CNTR to increment.

10.20.16 Broadcast Lane Attributes Capture Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} Attributes Capture Register.

Register Name: BCAST_LANE_ATTR_CAPT Reset Value: 0x0000_0000	Register Offset: 0xFFFF14

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved							
16:23	Reserved							
24:31	Reserved							VALID

Bits	Name	Description	Type	Reset Value
0:30	Reserved	Reserved	RO	0
31	VALID	1 = The Lane capture registers contain valid information.	RW	0

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10.20.17 Broadcast Lane DFE 1 Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} DFE 1 Register.

Register Name: BCAST_LANE_DFE_1 Reset Value: 0x0000_0000	Register Offset: 0xFFFF18

Bits	0	1	2	3	4	5	6	7
00:07	Reserved							
08:15	Reserved			UNUSED		RX_DFE_DIS	TAP_OFFSET_SEL	TAP_4_SEL
16:23	TAP_3_SEL	TAP_2_SEL	TAP_1_SEL	TAP_0_SEL	Reserved			
24:31	Reserved							

Bits	Name	Description	Type	Reset Value
0:10	Reserved	Reserved	RO	0
11:12	UNUSED	Reserved	RW	0
13	RX_DFE_DIS	Revision B and later devices 1 = Disable RX DFE Revision A device 1 = Enable RX DFE Supported combinations include: • RX_DFE_DIS = 1, TAP_x_SEL = 0: Received signal is not modified by DFE and coefficient updates cannot be written to the register fields. • RX_DFE_DIS = 1, TAP_x_SEL = 1: Coefficients can be written into registers but updates will have no effect on the received signal when LANE_{0..47}_DFE_2.CFG_EN transitions from 0 to 1. • RX_DFE_DIS = 0, TAP_x_SEL = 1: Coefficients can be written into registers and updates will have an effect on the received signal when LANE_{0..47}_DFE_2.CFG_EN transitions from 0 to 1.	RW	0
14	TAP_OFFSET_SEL	1 = Enable register adjustment of TAP_OFFSET. Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
15	TAP_4_SEL	1 = Enable register adjustment of Tap 4 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0

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Bits	Name	Description	Type	Reset Value
16	TAP_3_SEL	1 = Enable register adjustment of Tap 3 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
17	TAP_2_SEL	1 = Enable register adjustment of Tap 2 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
18	TAP_1_SEL	1 = Enable register adjustment of Tap 1 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
19	TAP_0_SEL	1 = Enable register adjustment of Tap 0 DFE coefficient Note: It is a programming error if this bit is set to 0 when RX DFE is enabled.	RW	0
20:31	Reserved	Reserved	RW	0

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10.20.18 Broadcast Lane DFE 2 Register

A read of this register returns the last value written. Each port's value may differ from this broadcast register. The per-port version of this register is Lane {0..47} DFE 2 Register.

Register Name: BCAST_LANE_DFE_2 Reset Value: 0x0000_0000	Register Offset: 0xFFFF1C

Bits	0	1	2	3	4	5	6	7
00:07	Reserved			TAP_OFFSET_CFG				
08:15	TAP_OFFSET_CFG	TAP_4_CFG			TAP_3_CFG			
16:23	TAP_2_CFG					TAP_1_CFG		
24:31	TAP_1_CFG			TAP_0_CFG				CFG_EN

Bits	Name	Description	Type	Reset Value
0:2	Reserved	Reserved	RO	0
3:8	TAP_OFFSET_CFG	Value to load into Offset coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
9:11	TAP_4_CFG	Value to load into T4 coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
12:15	TAP_3_CFG	Value to load into T3 coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
16:20	TAP_2_CFG	Value to load into T2 coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
21:26	TAP_1_CFG	Value to load into T1 coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
27:30	TAP_0_CFG	Value to load into T0 coefficient. For more information, see Lane {0..47} DFE 2 Register.	RW	0
31	CFG_EN	Load coefficient outputs based on register fields. For more information, see Lane {0..47} DFE 2 Register.	RW	0

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10.21 Error Management Broadcast Registers

These registers write the same value to every port's copy of the associated RapidIO standard register.

10.21.1 Broadcast Port Error Detect Register

This is the broadcast version of the per-port RapidIO standard register Port {0..17} Error Detect CSR. A read of this register returns the last value written. Each port's value may differ from this broadcast register.

Register Name: BCAST_PORT_ERR_DET Reset Value: 0x0000_0000	Register Offset: 0xFFFF40

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR	Reserved						
08:15	Reserved	CS_CRC_ERR	UNEXP_ACKID	CS_NOT_ACC	PKT_ILL_ACKID	PKT_CRC_ERR	PKT_ILL_SIZE	Reserved
16:23	IDLE1_ERR	Reserved						
24:31	Reserved		LR_ACKID_ILL	PRTCL_ERR	Reserved	DELIN_ERR	CS_ACK_ILL	LINK_TIMEOUT

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR	0 = Did not detect an IDT implementation-specific error 1 = Detected an IDT implementation-specific error	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR	0 = Did not detect a control symbol with a bad CRC 1 = Detected a control symbol with a bad CRC	RW	0
10	UNEXP_ACKID	0 = Did not detect a an acknowledge control symbol with an unexpected ackID 1 = Detected an acknowledge control symbol with an unexpected ackID	RW	0
11	CS_NOT_ACC	0 = Did not detect a packet-not-accepted control symbol 1 = Detected a packet-not-accepted control symbol	RW	0
12	PKT_ILL_ACKID	0 = Did not detect a packet with a bad ackID 1 = Detected a packet with a bad ackID	RW	0
13	PKT_CRC_ERR	0 = Did not detect a packet with bad CRC 1 = Detected a packet with bad CRC	RW	0
14	PKT_ILL_SIZE	0 = Did not detect a packet of an illegal size 1 = Detected a packet of an illegal size	RW	0

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(Continued)

Bits	Name	Description	Type	Reset Value
15	Reserved	Reserved	RO	0
16	IDLE1_ERR	0 = Did not detect a data character in an IDLE1 sequence 1 = Detected a data character in an IDLE1 sequence	RW	0
17:25	Reserved	Reserved	RO	0
26	LR_ACKID_ILL	0 = Did not detect a link-response with an ackID that is not outstanding 1 = Detected a link-response with an ackID that is not outstanding	RW	0
27	PRTCL_ERR	0 = Did not detect a protocol error 1 = Detected a protocol error	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR	0 = Did not detect a delineation error 1 = Detected a delineation error	RW	0
30	CS_ACK_ILL	0 = Did not detect an unsolicited acknowledgement control symbol. 1 = Detected an unsolicited acknowledgement control symbol.	RW	0
31	LINK_TIMEOUT	0 = Did not detect a link timeout error 1 = Detected a link timeout error	RW	0

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10.21.2 Broadcast Port Error Rate Enable Register

This is the broadcast version of the per-port RapidIO standard register, Port {0..17} Error Rate Enable CSR. A read of this register returns the last value written. Each port's value may differ from this broadcast register.

Register Name: BCAST_PORT_ERR_RATE_EN Reset Value: 0x0000_0000	Register Offset: 0xFFFF44

Bits	0	1	2	3	4	5	6	7
00:07	IMP_SPEC_ERR_EN	Reserved						
08:15	Reserved	CS_CRC_ERR_EN	UNEXP_ACKID_EN	CS_NOT_ACC_EN	PKT_ILL_ACKID_EN	PKT_CRC_ERR_EN	PKT_ILL_SIZE_EN	Reserved
16:23	IDLE1_ERR_EN	Reserved						
24:31	Reserved		LR_ACKID_ILL_EN	PRTCL_ERR_EN	Reserved	DELIN_ERR_EN	CS_ACK_ILL_EN	LINK_TIMEOUT_EN

Bits	Name	Description	Type	Reset Value
0	IMP_SPEC_ERR_EN	0 = Disable the capture of IDT implementation-specific errors. 1 = Enable the capture of IDT implementation-specific errors.	RW	0
1:8	Reserved	Reserved	RO	0
9	CS_CRC_ERR_EN	0 = Disable the capture of a control symbol with bad CRC. 1 = Enable the capture of a control symbol with bad CRC.	RW	0
10	UNEXP_ACKID_EN	0 = Disable the capture of a acknowledge control symbol with unexpected ackID. 1 = Enable the capture of a acknowledge control symbol with unexpected ackID.	RW	0
11	CS_NOT_ACC_EN	0 = Disable the capture of a packet-not-accepted control symbol. 1 = Enable the capture of a packet-not-accepted control symbol.	RW	0
12	PKT_ILL_ACKID_EN	0 = Disable the capture of a packet with bad ackID. 1 = Enable the capture of a packet with bad ackID.	RW	0
13	PKT_CRC_ERR_EN	0 = Disable the capture of a packet with bad CRC. 1 = Enable the capture of a packet with bad CRC.	RW	0
14	PKT_ILL_SIZE_EN	0 = Disable the capture of a packet with an illegal size. 1 = Enable the capture of a packet with an illegal size.	RW	0
15	Reserved	Reserved	RO	0

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(Continued)

Bits	Name	Description	Type	Reset Value
16	IDLE1_ERR_EN	0 = Disable the capture of a data character in an IDLE1 sequence. 1 = Enable the capture of a data character in an IDLE1 sequence.	RW	0
17:25	Reserved	Reserved	RO	0
26	LR_ACKID_ILL_EN	0 = Disable the capture of a link-response with an ackID that is not outstanding. 1 = Enable the capture of a link-response with an ackID that is not outstanding.	RW	0
27	PRTCL_ERR_EN	0 = Disable the capture of protocol errors. 1 = Enable the capture of protocol errors.	RW	0
28	Reserved	Reserved	RO	0
29	DELIN_ERR_EN	0 = Disable the capture of delineation errors. 1 = Enable the capture of delineation errors.	RW	0
30	CS_ACK_ILL_EN	0 = Disable the capture of an unsolicited acknowledgement control symbol. 1 = Enable the capture of an unsolicited acknowledgement control symbol. Note: This does not include packet-not-accept control symbols.	RW	0
31	LINK_TIMEOUT_EN	0 = Disable the capture of link timeout errors. 1 = Enable the capture of link timeout errors.	RW	0

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11. References

For additional information, see the following documents:

- *RapidIO Specification (Rev. 2.1)*, Part 1: Input/Output Logical Specification
- *RapidIO Specification (Rev. 2.1)*, Part 2: Message Passing Logical Specification
- *RapidIO Specification (Rev. 2.1)*, Part 3: Common Transport Specification
- *RapidIO Specification (Rev. 2.1)*, Part 6: LP-Serial Physical Layer Specification
- *RapidIO Specification (Rev. 2.1)*, Part 7: System and Device Interoperability Specification
- *RapidIO Specification (Rev. 2.1)*, Part 8: Error Management Extensions Specification
- *RapidIO Specification (Rev. 2.1)*, Part 9: Flow Control Logic Layer Extensions Specification
- *RapidIO Specification (Rev. 2.1)*, Part 11: Multicast Extensions Specification
- *RapidIO Specification (Rev. 2.1)*, Annex I: Software/System Bring Up Specification
- IEEE Std 1149.1-2001 IEEE Standard Test Access Port and Boundary-Scan Architecture
- IEEE Std 1149.6-2003 IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks
- *The I^2C-Bus Specification* (v 2.1), January 2000, Philips

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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