User's Manual

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RZ/T1 Group

User's Manual: Hardware

RZ Family RZ/T Series

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Objective and Target Users

This manual was written to explain the hardware functions and electrical characteristics of this LSI to the target users, i.e. those who will be using this LSI in the design of application systems. Target users are expected to understand the fundamentals of electrical circuits, logic circuits, and microcomputers.
This manual is organized in the following items: an overview of the product, descriptions of the CPU, system control functions, and peripheral functions, electrical characteristics of the device, and usage notes.

When designing an application system that includes this LSI, take all points to note into account.
Points to note are given in their contexts and at the final part of each section, and in the section giving usage notes.

The list of revisions is a summary of major points of revision or addition for earlier versions. It does not cover all revised items. For details on the revised points, see the actual locations in the manual.

The following documents have been prepared for the RZ/T1 Group. Before using any of the documents, please visit our web site to verify that you have the most up-to-date available version of the document.

Document Type	Contents	Document Title	Document No.
Data Sheet	Overview of hardware and electrical characteristics	—	—
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral specifications, electrical characteristics, and timing charts) and descriptions of operation	RZ/T1 Group User's manual: Hardware	This User's manual
User's manual: Software	Please find this information from the Arm® Ltd. home page.		
Application Note	Examples of applications and sample programs	—	—
Renesas Technical Update	Preliminary report on the specifications of a product, document, etc.	—	—

2. Description of Registers

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings. The standard format and notation for bit charts and tables are described below.

X.X.X ... Register

Address(es): xxxx xxxxxh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	... [1:0]		...4	—	—	—	...0
Value after reset:	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	... 0	... Bit	0: ..... 1: Setting prohibited (3)	R/W (1)
b3 to b1	—	Reserved (2)	The read value is 0. The write value should be 0.	R/W
b4	... 4	... Bit	0: 1:	R
b6, b5	... [1:0]	... Bit	0 0: ..... 0 1: ..... Settings other than above are prohibited (3)	R/(W)*
b7	—	Reserved	The read value is undefined. Writing to this bit has no effect.	R

(1) R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable. However, writing to this bit or field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit or field is readable. Writing to this bit or field has no effect.

(2) Reserved. Make sure to use the specified value when writing to this bit or field; otherwise, the correct operation is not guaranteed.

(3) Setting prohibited. The correct operation is not guaranteed if such a setting is performed.

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
Hi-Z	High Impedance
I/O	Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
UART	Universal Asynchronous Receiver/Transmitter

4. Description of the Access Size

Access size:
8 bits = Byte
16 bits = Word
32 bits = Longword

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300 MHz/450 MHz/600 MHz, MCU with Arm® Cortex®-R4 and -M3*1, on-chip FPU, 498/747/996 DMIPS, up to 1 Mbyte of on-chip extended SRAM, Ethernet MAC, EtherCAT*1, USB 2.0 high-speed, CAN, various communications interfaces such as an SPI multi-I/O bus controller, ΔΣ interface, safety functions, encoder interfaces*1, and security functions*1

Features

■ On-chip 32-bit Arm Cortex-R4 processor
- High-speed realtime control with maximum operating frequency of 300/450/600 MHz
  Capable of 498/747/996 DMIPS (in operation at 300/450/600 MHz)
- On-chip 32-bit Arm Cortex-R4 (revision r1p4)
- Tightly coupled memory (TCM) with ECC: 512 Kbytes/32 Kbytes
- Instruction cache/data cache with ECC: 8 Kbytes per cache
- High-speed interrupt
- The FPU supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single-precision and double-precision.
- Harvard architecture with 8-stage pipeline
- Supports the memory protection unit (MPU)
- Arm CoreSight architecture, includes support for debugging through JTAG and SWD interfaces

■ On-chip 32-bit Arm Cortex-M3 processor (in products incorporating an R-IN engine)
- 150-MHz operating frequency
- On-chip 32-bit Arm Cortex-M3 (revision r2p1)
- RISC Harvard architecture with 3-stage pipeline
- Supports the memory protection unit (MPU)

■ Low power consumption
- Standby mode, sleep mode, and module stop function

■ On-chip extended SRAM
- Up to 1 Mbyte of the on-chip extended SRAM with ECC
- 150 MHz

■ Data transfer
- DMAC: 16 channels × 2 units
- DMAC for the Ethernet controller: 1 channel

■ Event link controller
- Module operations can be started by event signals rather than by interrupt handlers.
- Linked operation of modules is available even while the CPU is in the sleep state.

■ Reset and power supply voltage control
- Four reset sources including a pin reset
- Dual power-voltage configuration: 3.3 V (I/O unit), 1.2 V (internal)

■ Clock functions
- External clock/oscillator input frequency: 25 MHz
- CPU clock frequency: Up to 300/450/600 MHz
- Low-speed on-chip oscillator (LOCO): 240 kHz

■ Independent watchdog timer
- Operated by a clock signal obtained by frequency-dividing the clock signal from the low-speed on-chip oscillator: Up to 120 kHz

■ Safety functions
- Register write protection, input clock oscillation stop detection, CRC, IWDTa, and A/D self-diagnosis
- An error control module is incorporated to generate a pin signal output, interrupt, or internal reset in response to errors originating in the various modules.

■ Security functions (optional)*2
- Boot mode with security through encryption

■ Encoder interfaces (optional)
- 2 channels*3
- EnDat 2.2, BiSS-C, FA-CODER, A-format, and HIPERFACE DSL-compliant interfaces*4
- Frequency-divided output from an encoder



PRBG0320GA-A 17 × 17 mm, 0.8-mm pitch
PRBG0320GB-A 17 × 17 mm, 0.8-mm pitch

PLQP0176LD-A 20 × 20 mm, 0.4-mm pitch

■ Various communications interfaces
- Ethernet
  - EtherCAT slave controller: 2 ports (optional)
  - Ethernet MAC: 1 port (an Ethernet switch is not used)
    or
  - Ethernet MAC: 1 port (an Ethernet switch to support 2 ports is used)
- USB 2.0 high-speed host/function : 1 channel
- CAN (compliant with ISO11898-1): 2 channels (max.)
- SCIFA with 16-byte transmission and reception FIFOs: 5 channels
- I^2C bus interface: 2 channels for transfer at up to 400 kbps
- RSPIa: 4 channels
- SPIBSC: Provides a single interface for multi-I/O compatible serial flash memory

■ External address space
- Buses for high-speed data transfer at 75 MHz (max.)
- Support for up to 6 CS areas
- 8-, 16-, or 32-bit bus space is selectable per area

■ Up to 33 extended-function timers
- 16-bit TPUa (12 channels), MTU3a (9 channels), GPTa (4 channels): Input capture, output compare, PWM waveform output
- 16-bit CMT (6 channels), 32-bit CMTW (2 channels)

■ Serial sound interface (1 channel)

■ ΔΣ interface
- Up to 4 ΔΣ modulators are connectable externally.

■ 12-bit A/D converters
- 12 bits × 2 units (max.)
  (8 channels for unit 0; 16 channels for unit 1)
- Self diagnosis
- Detection of analog input disconnection

■ Temperature sensor for measuring temperature within the chip

■ General-purpose I/O ports
- 5-V tolerance, open drain, input pull-up

■ Multi-function pin controller
- The locations of input/output functions for peripheral modules are selectable from among multiple pins.

■ Operating temperature range
- Tj = -40°C to +125°C
  Tj: Junction temperature

Note 1. Optional
Note 2. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.
Note 3. For use of two channels, use them in combination of any two protocols among EnDat2.2, BiSS-C, FA-CODER, and A-format.
Note 4. BiSS is a registered trademark of iC-Haus GmbH.

1. Overview

1.1 Outline of Specifications

This LSI circuit is a high-performance MCU equipped with the Arm® Cortex®-R4 processor with FPU and Cortex-M3 processor (for products incorporating an R-IN engine), and incorporating integrated peripheral functions necessary for system configuration. Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package. For details, see Table 1.2, List of Functions.

Table 1.1 Outline of Specifications (1 / 7)

Classification	Module/Function	Description
CPU	Central processing unit (Cortex-R4)	• Maximum operating frequency 320-pin FBGA: 300 MHz/450 MHz/600 MHz 176-pin HLFQFP: 450 MHz • 32-bit CPU Cortex-R4 designed by Arm (core revision r1p4) • Address space: 4 Gbytes • Instruction cache: 8 Kbytes (with ECC) • Data cache: 8 Kbytes (with ECC) • Tightly coupled memory (TCM) ATCM: 512 Kbytes (with ECC) BTCM: 32 Kbytes (with ECC) • Instruction set: Arm v7-R architecture, so support includes Thumb® and Thumb-2 • Data arrangement Instructions: Little endian Data: Little endian • Memory protection unit (MPU)
	Central processing unit (Cortex-M3) (for products incorporating an R-IN engine)	• Operating frequency: 150 MHz • 32-bit CPU Cortex-M3 designed by Arm (core revision r2p1) • Address space: 4 Gbytes • Instruction set: Arm v7-M architecture, so support includes Thumb® and Thumb-2 • Data arrangement Instructions: Little endian Data: Little endian • Memory protection unit (MPU)
	FPU (Cortex-R4)	• Supports addition, subtraction, multiplication, division, multiply-and-accumulate, and square-root operations at single- and double-precision. • Registers 32-bit single-word registers: 32 bits × 32 (can be used as 16 double-word registers: 64 bits × 16)
Memory	On-chip extended SRAM with ECC	• Capacity: Up to 1 Mbyte • Operating frequency: 150 MHz • SEC-DED (single error correction/double error detection)
Operating modes		• The operating mode can be selected from the following three boot modes SPI boot mode (for booting up from serial flash memory) 16-bit bus boot mode (NOR Flash) 32-bit bus boot mode (NOR Flash)
Clock	Clock generation circuit	• The input clock can be selected from an external clock or external resonator. • Detection of input clock oscillation stopping • The following clocks are generated. CPU clock: 300/450/600 MHz (max.) System clock: 150 MHz (fixed) High-speed peripheral module clock: 150 MHz (fixed) Low-speed peripheral module clock: 75 MHz (fixed) ADCCLK in the 12-bit A/D converter (S12ADCa): 60 MHz (max.) External bus clock: 75 MHz (max.) Low-speed on-chip oscillator: 240 kHz (fixed)
Reset		RES# pin reset, error control module (ECM) reset, software reset

Table 1.1 Outline of Specifications (2 / 7)

Classification	Module/Function	Description
Low power	Low-power consumption function	• Standby mode (Cortex-R4) • Sleep mode (Cortex-M3) (for products incorporating an R-IN engine) • Module stop function
Interrupt	Cortex-R4 vector interrupt controller (VIC)	• Peripheral function interrupts: 290 sources / 292 sources (for products incorporating an R-IN engine) • External interrupts: 20 sources (NMI, IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins) • Software interrupts: 1 source • Non-maskable interrupts: 2 sources • Sixteen levels specifiable for the order of priority
	Cortex-M3 nested-type vector interrupt controller (NVIC) (only included in products incorporating an R-IN engine)	• Peripheral function interrupts: 101 sources • External interrupts: 19 sources (IRQ0 to IRQ15, ETH0_INT, ETH1_INT, and ETH2_INT pins) • Software interrupts: 1 source • Non-maskable interrupts: 1 source • Sixteen levels specifiable for the order of priority
External bus extension	Bus state controller (BSC)	• The external address space is divided into six areas (CS0 to CS5) for management. • The following features settable for each area independently. Bus size (8, 16, or 32 bits): Available sizes depend on the area. Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas) Idle wait cycle insertion (between same area access cycles or different area access cycles) Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. • Outputs a chip select signal (CS0# to CS5#) according to the target area (CS assert or negate timing can be selected by software) • SDRAM refresh Auto refresh or self-refresh mode selectable • SDRAM burst access
Data transfer	Direct memory access controller (DMAC)	• 2 units (16 channels for unit 0, 16 channels for unit 1) • Transfer modes: Single transfer mode and block transfer mode • Transfer size Unit 0: 1/2/4/16/32/64 bytes Unit 1: 1/2/4/16 bytes • Activation sources: External requests (DREQ0 to DREQ2), external interrupts, on-chip peripheral module requests, and software requests
I/O ports	General-purpose I/O ports	• 320-pin FBGA I/O pins: 209 Input pins: 9 Pull-up/pull-down resistors: 209 5-V tolerance: 9 • 176-pin HLFQFP I/O pins: 97 Input pins: 5 Pull-up/pull-down resistors: 97 5-V tolerance: 5
Event link controller (ELC)		• Up to 103 event signals can be interlinked with the operation of modules. • In particular, the operation of timer modules can be started by input event signals. • Event-linked operation of signals of ports B and E is to be possible.
Multi-function pin controller (MPC)		The locations of input/output functions are selectable from among multiple pins.

Table 1.1 Outline of Specifications (3 / 7)

Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 2 units*1 • Maximum 16 lines of pulse input/output × 2 units • Select from among seven or eight counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Input capture/output compare function • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Output of PWM waveforms in up to 15 phases × 2 units in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 4 channels) depending on the channel. • PPG output trigger can be generated (unit 0 only) • Capable of generating conversion start triggers for the A/D converters • Digital noise filtering of signals from the input capture pins • Event linking by the ELC (unit 0 only)
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 10, 11, 12 or 14 counter-input clock signals for each channel (with maximum operating frequency of 150 MHz) • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at crest or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2 in cascade connection) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital noise filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC

Table 1.1 Outline of Specifications (4 / 7)

Classification	Module/Function	Description
Timers	General PWM timer (GPTa)	• 16 bits × 4 channels • Counting up or down (saw-wave), counting up and down (triangle-wave) selectable for all channels • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 150 MHz) • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of automatic three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: software, and compare-match • Generation of triggers for A/D converter conversion • Digital noise filter function for signals on the input capture and external trigger pins • Event linking by the ELC
	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units*1 • Pulse output with the MTU3a or TPUa output as a trigger • Maximum of 32 pulse-output possible
	Compare match timer (CMT)	• (16 bits × 2 channels) × 3 units • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Event linking by the ELC (channel 1 of unit 0 only)
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four counter-input clock signals for each channel (with maximum operating frequency of 75 MHz) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Digital noise filter function for signals on the input capture pins • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel Products incorporating an R-IN engine: 14 bits × 2 channels • Select from among six counter-input clock signals for each channel (with maximum operating frequency of 75 MHz)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: Low-speed on-chip oscillator (LOCO)/2 Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 (with maximum operating frequency of 120 kHz)
	Port output enable 3 (POE3)	• Control of the high-impedance state of the MTU3a / GPTa's waveform output pins • Initiation by inputs on 4 pins, POE0#, POE4#, POE8#, and POE10# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by input clock oscillation-stoppage detection, PLL oscillation abnormality detection, or software • Additional programming of output control target pins is enabled

Table 1.1 Outline of Specifications (5 / 7)

Classification	Module/Function	Description
Communication function	Ethernet MAC (ETHERC)	• 1 port (Use of two ports is possible with the Ethernet switch function) • IEEE802.3 is supported • 10BASE and 100BASE are supported • Full duplex and half duplex are supported • Automatic pause packet transmission function • Auto broadcast suspension function by the pause packet reception • MII/RMII interface is supported
	Ethernet switch	• 2-port PHY interfaces • IEEE802.3 • 10BASE and 100BASE are supported • Full and half duplex • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with four priority levels • Multicasting and broadcasting • VLAN frame • IEEE1588 timer module • Cut-through and hub features • Device level ring (DLR)
	EtherCAT Slave Controller (ECATC)*2	• 1 channel (2 ports)*3 • EtherCAT Slave Controller IP core (made by Beckhoff Automation GmbH) implemented
	USB 2.0 HS host/ function module	• 1 port • Compliance with the USB 2.0 specification • Transfer rate High speed (480 Mbps), full speed (12 Mbps) • Communications buffer Incorporates 1 Kbyte of RAM for host mode Incorporates 8 Kbytes of RAM for function mode
	Serial communication interface with FIFO (SCIFA)	• 5 channels • Serial communications modes: Asynchronous, clock synchronous • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Both the transmission and reception sections are equipped with 16-byte FIFO buffers, allowing continuous transmission and reception. • Bit rate modulation
	I^2C bus interface (RIICa)	• 2 channels • Supports I^2C bus format • Supports the multi-master • Max. transfer rate: 400 kbps • Event linking by the ELC
	CAN module (RSCAN)	• 2 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • Message buffers Max. 64 × 2 channels of reception message buffers, which are used by all channels 16 transmission message buffers per channel • Max. transfer rate: 1 Mbps

Table 1.1 Outline of Specifications (6 / 7)

Classification	Module/Function	Description
Communication function	Serial peripheral interface (RSPIa)	• 4 channels • RSPI transfer facility Using the MOSI (master out slave in), MISO (master in slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped automatically with the reception buffer full for master reception • Event linking by the ELC
	SPI multi I/O bus controller (SPIBSC)	• 1 channel • One serial flash memory with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • Maximum transfer rate: 300 Mbps (for quad)
Serial sound interface (SSI)		• 1 channel • Duplex communication • Support of various serial audio formats • Support of master and slave functions • Generation of serial bit clock • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of eight-stage FIFO for transmission and reception • Support of WS continue mode in which the SSIWS signal is not stopped.
ΔΣ interface (DSMIF)		• 4 channels (unit 0: 3 channels, unit 1: 1 channel) • Up to 4 ΔΣ modulators are externally connectable • Sync filter can be selected as first, second, or third order
12-bit A/D converter (S12ADCa)		• 12 bits × 2 units (unit 0: 8 channels, unit 1: 16 channels)*1 • 12-bit resolution • Conversion time Unit 0: 0.483 µs per channel Unit 1: 0.883 µs per channel • Operating mode Scan mode (single scan mode, continuous scan mode, or group scan mode) Group A priority control (only for group scan mode) • Sample-and-hold function Common sample-and-hold circuit included In addition, channel-dedicated sample-and-hold function (4 channels: in unit 0 only) included • Sampling variable Sampling time can be set up for each channel • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: VREFL1, VREFH1 × 1/2, VREFH1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU3a, GPTa, TPUa) trigger, external trigger • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ±1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 0).

Table 1.1 Outline of Specifications (7 / 7)

Classification	Module/Function	Description
Safety	Register write protection function	Protects important registers from being overwritten in cases where a program runs out of control.
	CRC calculator (CRC)	• CRC code generation for arbitrary amounts of data in 8-, 16-, or 32-bit units • Select any of four generating polynomials: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (32-Ethernet), $X^{16} + X^{12} + X^5 + 1$ (16-CCITT), $X^8 + X^4 + X^3 + X^2 + 1$ (8-SAEJ1850), $X^8 + X^5 + X^3 + X^2 + X + 1$ (8-0x2F)
	Input clock oscillation stop function	Input clock oscillation stop detection: Available
	Clock monitor circuit (CLMA)	Monitors the abnormal output clock frequency from the PLL circuit or low-speed on-chip oscillator.
	Data operation circuit (DOC)	The function to compare, add, or subtract 16-bit data
	Error control module (ECM)	• Generates an interrupt, internal reset, or error output for the error signal input from each module. • Time-out function • The error control is duplicated in the master and the checker.
Security	Secure boot mode*4	As an option, a boot mode with encryption as a security function is available.
Encoder interfaces*5		• 2 channels*6 • EnDat 2.2, BiSS-C, FA-CODER, A-format, and HIPERFACE DSL-compliant interfaces • Frequency-divided output from an encoder
Power supply voltage		VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
Operating temperature		Tj = -40 to +125°C
Package		320-pin FBGA: 17 × 17 mm, 0.8-mm pitch PRBG0320GA-A 176-pin HLFQFP: 20 × 20 mm, 0.4-mm pitch PLQP0176LD-A
Debugging interface		• CoreSight architecture designed by Arm • Debugging function by the JTAG/SWD interface, and trace function by the trace port/SWV interface

Note 1. One unit for 176-pin devices (only unit 0 is provided)
Note 2. EtherCAT is a registered trademark of Beckhoff Automation GmbH, Germany. (optional)
Note 3. Not included in 176-pin devices.
Note 4. See Table 1.3, List of Products, for the products that have the secure boot mode. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.
Note 5. This applies to the devices with the encoder interfaces. For details, contact our sales representative.
Note 6. For use of two channels, use them in combination of any two protocols among EnDat2.2, BiSS-C, FA-CODER, and A-format.

Table 1.2 Comparison of Functions for Different Packages

Module/Function		RZ/T1 Group		
		320 Pins		
		R-IN Engine Incorporated	R-IN Engine Not-Incorporated	176 Pins
External bus	External bus width	32 bits		
Interrupt	External interrupt	NMI, IRQ0 to IRQ15, ETH0_INT, ETH1_INT, ETH2_INT		NMI, IRQ0 to IRQ15, ETH0_INT, ETH1_INT
DMA	DMA controller (DMAC)	ch0 to ch31		
Timers	16-bit timer pulse unit (TPUa)	ch0 to ch11 (Unit 0, Unit 1)		ch0 to ch5 (Unit 0)
	Multi-function timer pulse unit 3 (MTU3a)	ch0 to ch8		
	General-purpose PWM timer (GPTa)	ch0 to ch3		
	Port output enable 3 (POE3)	Available		
	Programmable pulse generator (PPG)	Unit 0, Unit 1		Unit 0
	Compare match timer (CMT)	ch0 to ch5		
	Compare match timer W (CMTW)	ch0, ch1		
	Watchdog timer (WDTA)	ch0, ch1	ch0	
	Independent watchdog timer (IWDTa)	Available		
Communication function	Ethernet controller (ETHERC)	1 port*1		
	EtherCAT slave controller (ECATC)	2 ports*1	2 ports*1 (optional)	Not supported
	USB 2.0 HS host/function module (USB)	ch0		
	Serial communications interface with FIFO (SCIFA)	ch0 to ch4		
	I^2C bus interface (RIICa)	ch0, ch1		
	Serial peripheral interface (RSPIa)	ch0 to ch3		
	CAN module (RSCAN)	ch0, ch1		
	SPI multi I/O bus controller (SPIBSC)	ch0		
Serial sound interface (SSI)		ch0		
ΔΣ interface (DSMIF)		ch0 to ch3		
12-bit A/D converter (S12ADCa)		AN000 to AN007 (unit 0) AN100 to AN115 (unit 1)		AN000 to AN007 (unit 0)
Temperature sensor		Available		
CRC calculator (CRC)		Available		
Data operation circuit (DOC)		Available		
Clock monitor circuit (CLMA)		Available		
Secure boot mode*2		Optional		
Event link controller (ELC)		Available		
Encoder interfaces*3		Optional		Not supported

Note 1. Combining the Ethernet controller and the EtherCAT slave controller (optional) makes a total of three ports. The Ethernet controller can support two ports with the use of the Ethernet switch.
Note 2. See Table 1.3, List of Products for the products that have the secure boot mode. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.
Note 3. For details, contact our sales representative.

1.2 List of Products

Table 1.3 is a list of products.

Table 1.3 List of Products (1 / 3)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910001CFP	176 pins (PLQP0176LD-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	—
R7S910101CFP	176 pins (PLQP0176LD-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	—
R7S910002CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	—
R7S910002CBA	320 pins (PRBG0320GB-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	—
R7S910102CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	—
R7S910006CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	450 MHz	Not supported	—
R7S910006CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 Mbyte	Not supported	450 MHz	Not supported	—
R7S910106CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	450 MHz	Available	—
R7S910007CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	—
R7S910007CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	—
R7S910107CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Available	—
R7S910011CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	Encoder I/F
R7S910011CBA	320 pins (PRBG0320GB-A)	Cortex-R4	Not supported	Not supported	450 MHz	Not supported	Encoder I/F
R7S910111CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Not supported	450 MHz	Available	Encoder I/F
R7S910013CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	Encoder I/F
R7S910013CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Not supported	Encoder I/F
R7S910113CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 Mbyte	Not supported	600 MHz	Available	Encoder I/F
R7S910015CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910015CBA	320 pins (PRBG0320GB-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910115CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Available	R-IN Engine (CM3 : 150MHz)
R7S910016CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)

Table 1.3 List of Products (2 / 3)

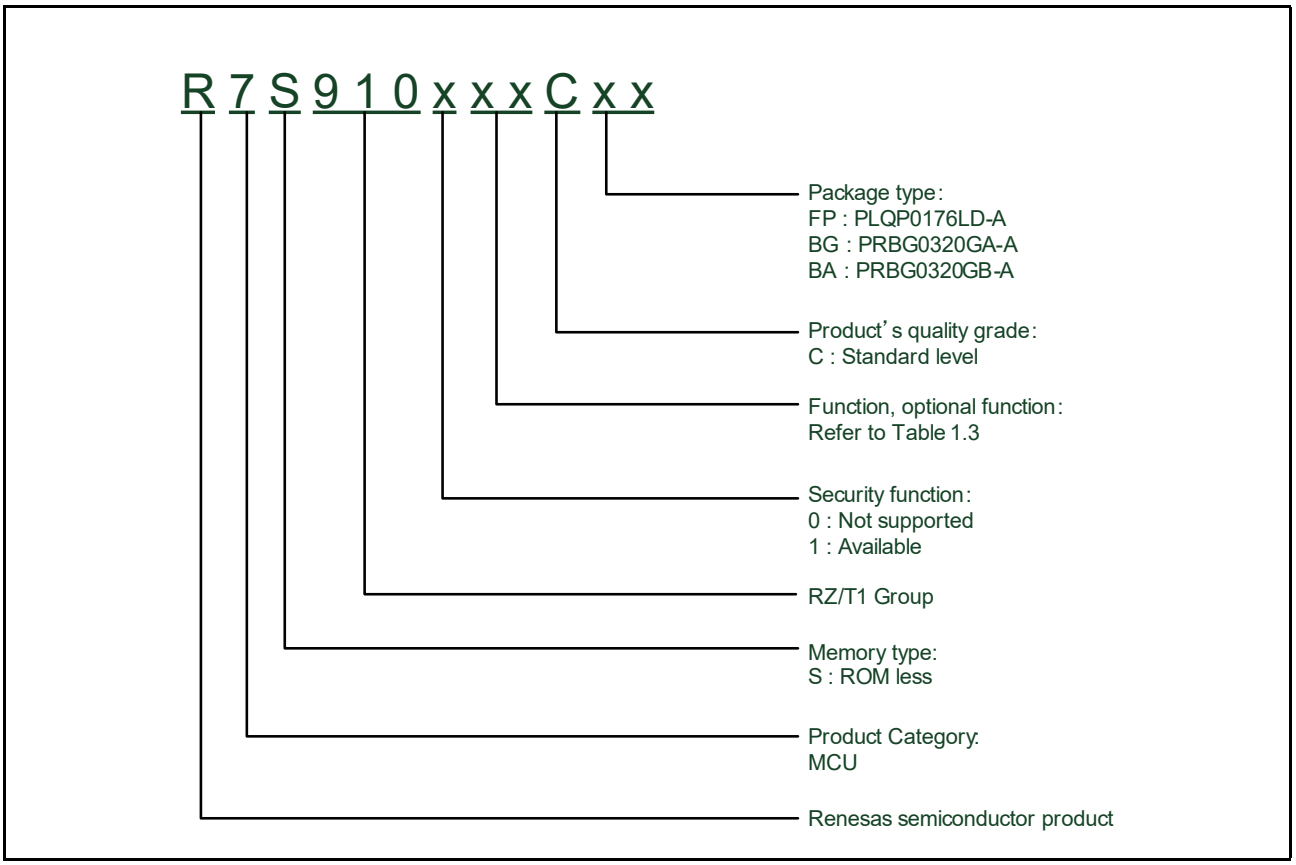
Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910016CBA	320 pins (PRBG0320GB-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910116CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	450 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910017CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910017CBA	320 pins (PRBG0320GB-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	R-IN Engine (CM3 : 150MHz)
R7S910117CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	R-IN Engine (CM3 : 150MHz)
R7S910018CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910018CBA	320 pins (PRBG0320GB-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Not supported	Encoder I/F R-IN Engine (CM3 : 150MHz)
R7S910118CBG	320 pins (PRBG0320GA-A)	Cortex-R4	(1 MB for R-IN Engine)	Supported	600 MHz	Available	Encoder I/F R-IN Engine (CM3 : 150 MHz)
R7S910025CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	—
R7S910025CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	—
R7S910125CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	—
R7S910026CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	Encoder I/F
R7S910026CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 MB	Supported	450 MHz	Not supported	Encoder I/F
R7S910126CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	450 MHz	Available	Encoder I/F
R7S910027CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	—
R7S910027CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	—
R7S910127CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	—
R7S910028CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	Encoder I/F
R7S910028CBA	320 pins (PRBG0320GB-A)	Cortex-R4	1 MB	Supported	600 MHz	Not supported	Encoder I/F
R7S910128CBG	320 pins (PRBG0320GA-A)	Cortex-R4	1 MB	Supported	600 MHz	Available	Encoder I/F

Table 1.3 List of Products (3 / 3)

Part No.	Package	CPU	On-Chip Extended SRAM Capacity	EtherCAT	Operating Frequency (max.)	Security Function *1	Optional Function
R7S910035CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	—
R7S910035CBA	320 pins (PRBG0320GB-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	—
R7S910135CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	—
R7S910036CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	Encoder I/F
R7S910036CBA	320 pins (PRBG0320GB-A)	Cortex-R4	Not supported	Supported	300 MHz	Not supported	Encoder I/F
R7S910136CBG	320 pins (PRBG0320GA-A)	Cortex-R4	Not supported	Supported	300 MHz	Available	Encoder I/F

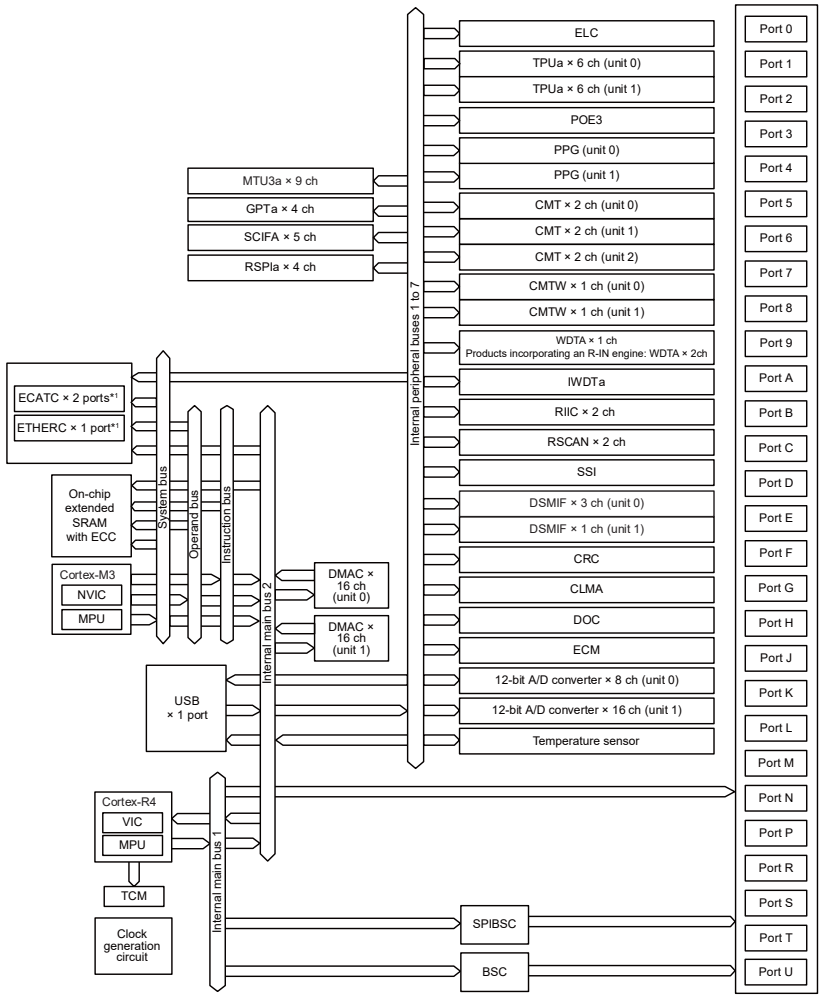
Note: See the separate documents regarding the encoder I/F.
Note 1. Details of these optional functions will only be disclosed after completion of a binding non-disclosure agreement. For details, contact our sales representative.

1.3 Product type name



1.4 Block Diagram

Figure 1.1 shows a block diagram of a 320-pin device.



ETHERC:	Ethernet controller
ECATC:	EtherCAT slave controller
DMAC:	DMA controller
BSC:	Bus state controller
SPIBSC:	SPI multi I/O bus controller
WDTA:	Watchdog timer
IWDTa:	Independent watchdog timer
SCIFA:	Serial communication interface with FIFO
RSPIa:	Serial peripheral interface
USB:	USB 2.0 HS host/function module
VIC:	Vector interrupt controller
NVIC:	Nested-type vector interrupt controller
MPU:	Memory protection unit
ELC:	Event link controller
TPUa:	16-bit timer pulse unit
MTU3a:	Multi-function timer pulse unit 3
POE3:	Port output enable 3

GPTa:	General-purpose PWM timer
PPG:	Programmable pulse generator
CMT:	Compare match timer
CMTW:	Compare match timer W
RIICa:	I^2C bus interface
RSCAN:	CAN module
SSI:	Serial sound interface
DSMIF:	ΔΣ interface
CRC:	CRC (cyclic redundancy check) calculator
CLMA:	Clock monitor circuit
DOC:	Data operation circuit
ECM:	Error control module

Note 1. Combining the Ethernet controller and the EtherCAT slave controller (optional) makes a total of three ports. The Ethernet controller can support two ports with the use of the Ethernet switch.

Figure 1.1 Block Diagram

1.5 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 7)

Classifications	Pin Name	I/O	Description
Power supply	VDD	Input	Power supply pin. Connect this pin to the system power supply.
	VSS	Input	Ground pin. Connect this pin to the system power supply (0 V).
	VCCQ33	Input	Power supply pin for I/O pins
	PLLVDD0, PLLVDD1	Input	Power supply pins for the on-chip PLL oscillator
	PLLVSS0, PLLVSS1	Input	Ground pins for the on-chip PLL oscillator. Connect these pins to the system power supply (0 V).
Clock	XTAL	Output	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	EXTAL	Input	
	CKIO	Output	Outputs the external bus clock for external devices.
	AUDIO_CLK	Input	Inputs the external clock for audio.
	CLKOUT25M0, CLKOUT25M1, CLKOUT25M2	Output	Output the external clock for Ethernet PHY.
Operating mode control	MD0 to MD2	Input	Input the operating mode select signal.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	BSCANP	Input	Inputs the boundary scan enable signal. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
	OSCTH	Input	Inputs the clock input mode select signal. When an external clock is input, this pin should be driven high. When a crystal resonator is connected, it should be driven low.
	ERROROUT#	Output	Outputs the error signal from the error control module (ECM).
	RSTOUT#	Output	Outputs the reset signal externally.
Debugging interface	TRST#	Input	Test reset pin for on-chip emulator
	TMS	I/O	Test mode select pin for on-chip emulator
	TDI	Input	Test data input pin for on-chip emulator
	TDO	Output	Test data output pin for on-chip emulator
	TCK	Input	Test clock pin for on-chip emulator
	TRACECLK	Output	Outputs the clock for synchronization with the trace data.
	TRACECTL	Output	Outputs the enable signal for trace control.
	TRACEDATA0 to TRACEDATA7	Output	Output the trace data.

Table 1.4 Pin Functions (2 / 7)

Classifications	Pin Name	I/O	Description
Bus state controller (BSC)	A25 to A0	Output	Output the address.
	D31 to D0	I/O	Input and output the data.
	CS0# to CS5#	Output	Output the chip select signal for the external memory or device.
	RD#	Output	Outputs the strobe signal which indicates reading is in progress.
	RD/WR#	Output	Outputs the strobe signal which indicates the read or write access.
	BS#	Output	Outputs the status signal which indicates the start of bus cycles.
	AH#	Output	Outputs the address hold signal for the device that uses the multiplexed I/O bus.
	WAIT#	Input	Inputs the external wait control signal which inserts a wait cycle into the bus cycles.
	WE0#	Output	Outputs the write strobe signal to D7 to D0.
	WE1#	Output	Outputs the write strobe signal to D15 to D8.
	WE2#	Output	Outputs the write strobe signal to D23 to D16.
	WE3#	Output	Outputs the write strobe signal to D31 to D24.
	DQMLL	Output	Outputs the data mask enable signal to D7 to D0 when SDRAM is connected.
	DQMLU	Output	Outputs the data mask enable signal to D15 to D8 when SDRAM is connected.
	DQMUL	Output	Outputs the data mask enable signal to D23 to D16 when SDRAM is connected.
	DQMUU	Output	Outputs the data mask enable signal to D31 to D24 when SDRAM is connected.
	RAS#	Output	Outputs the low-address strobe signal to the SDRAM. This pin should be connected to the RAS# pin on the SDRAM.
	CAS#	Output	Outputs the column-address strobe signal to the SDRAM. This pin should be connected to the CAS# pin on the SDRAM.
	CKE	Output	Outputs the clock enable signal to the SDRAM. This pin should be connected to the CKE pin on the SDRAM.
Direct memory access controller (DMAC)	DREQ0 to DREQ2	Input	Input the DMA transfer request signal from the external device.
	DACK0 to DACK2	Output	Output the acknowledge signal which indicates acceptance of the DMA transfer request from the external device.
	TEND0 to TEND2	Output	Output the DMA transfer end signal.
Interrupt	NMI	Input	Inputs the non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Input the external interrupt request signal.
	ETH0_INT, ETH1_INT, ETH2_INT	Input	Input the Ethernet PHY interrupt request signal.

Table 1.4 Pin Functions (3 / 7)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3a)	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	MTU0.TGRA to MTU0.TGRD input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	MTU1.TGRA and MTU1.TGRB input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	MTU2.TGRA and MTU2.TGRB input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	MTU3.TGRA to MTU3.TGRD input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	MTU4.TGRA to MTU4.TGRD input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW input capture input/ dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	MTU6.TGRA to MTU6.TGRD input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	MTU7.TGRA to MTU7.TGRD input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	MTU8.TGRA to MTU8.TGRD input capture input/output compare output
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	External clock input pins for MTU3a
Port output enable 3 (POE3)	POE0#, POE4#, POE8#, POE10#	Input	Input the request signal to place the MTU3a or GPTa in the high impedance state.
General-purpose PWM timer (GPTa)	GTIOC0A, GTIOC0B	I/O	GPT0.GTCCRA and GPT0.GTCCRB input capture input/output compare output/PWM output pins
	GTIOC1A, GTIOC1B	I/O	GPT1.GTCCRA and GPT1.GTCCRB input capture input/output compare output/PWM output pins
	GTIOC2A, GTIOC2B	I/O	GPT2.GTCCRA and GPT2.GTCCRB input capture input/output compare output/PWM output pins
	GTIOC3A, GTIOC3B	I/O	GPT3.GTCCRA and GPT3.GTCCRB input capture input/output compare output/PWM output pins
	GTETRG	Input	External trigger input pin for GPTa

Table 1.4 Pin Functions (4 / 7)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit (TPUa)	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins
	TIOCA1, TIOCB1	I/O	TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins
	TIOCA2, TIOCB2	I/O	TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins
	TIOCA4, TIOCB4	I/O	TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins
	TIOCA5, TIOCB5	I/O	TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	External clock input pins for TPUa (unit 0)
	TIOCA6, TIOCB6, TIOCC6, TIOCD6	I/O	TGRA6 to TGRD6 input capture input/output compare output/ PWM output pins
	TIOCA7, TIOCB7	I/O	TGRA7 and TGRB7 input capture input/output compare output/ PWM output pins
	TIOCA8, TIOCB8	I/O	TGRA8 and TGRB8 input capture input/output compare output/ PWM output pins
	TIOCA9, TIOCB9, TIOCC9, TIOCD9	I/O	TGRA9 to TGRD9 input capture input/output compare output/ PWM output pins
	TIOCA10, TIOCB10	I/O	TGRA10 and TGRB10 input capture input/output compare output/ PWM output pins
	TIOCA11, TIOCB11	I/O	TGRA11 and TGRB11 input capture input/output compare output/ PWM output pins
	TCLKE, TCLKF, TCLKG, TCLKH	Input	External clock input pins for TPUa (unit 1)
Programmable pulse generator (PPG)	PO0 to PO31	Output	Pulse output pins
Compare match timer W (CMTW)	TIC0 to TIC3	Input	CMTW input capture input pins
	TOC0 to TOC3	Output	CMTW output compare output pins
Serial communication interface with FIFO (SCIFA)	SCK0 to SCK4	I/O	Clock I/O pins
	RXD0 to RXD4	Input	Input the receive data.
	TXD0 to TXD4	Output	Output the transmit data.
	CTS0# to CTS4#	I/O	Hardware flow control input (transmission enable signal)/general output
	RTS0# to RTS4#	Output	Hardware flow control output (transmission request signal)/general output
I^2C bus interface (RIICa)	SCL0, SCL1	I/O	Clock I/O pins. The bus can be directly driven by the N-channel open drain.
	SDA0, SDA1	I/O	Data I/O pins. The bus can be directly driven by the N-channel open drain.

Table 1.4 Pin Functions (5 / 7)

Classifications	Pin Name	I/O	Description
Ethernet controller (ETHERC)	ETH0_TXC, ETH1_TXC, ETH2_TXC	Input	Input the 10 M/100 M transmission clock (2.5 MHz/25 MHz).
	ETH0_TXEN, ETH1_TXEN, ETH2_TXEN	Output	Output the transmission enable signal.
	ETH0_TXER, ETH1_TXER, ETH2_TXER	Output	Output the transmission error signal.
	ETH0_TXD0 to 3, ETH1_TXD0 to 3, ETH2_TXD0 to 3	Output	Output the transmission data signal.
	ETH0_RXC, ETH1_RXC, ETH2_RXC	Input	Receive clock input pins
	ETH0_RXDV, ETH1_RXDV, ETH2_RXDV	Input	Input the receive data enable signal.
	ETH0_RXER, ETH1_RXER, ETH2_RXER	Input	Input the receive data error signal.
	ETH0_RXD0 to 3, ETH1_RXD0 to 3, ETH2_RXD0 to 3	Input	Input the receive data signal.
	ETH0_CRS, ETH1_CRS, ETH2_CRS	Input	Input the carrier sense signal.
	ETH0_COL, ETH1_COL, ETH2_COL	Input	Input the collision detection signal.
	ETH_MDC, MII2_MDC	Output	Output the management interface clock.
	ETH_MDIO, MII2_MDIO	I/O	Management data signal I/O pins
	PHYLINK0, PHYLINK1	Input	Input the PHY Link signal.
	ETHSWSECOUT	Output	Outputs the Ethernet switch SYNCOUT signal.
	PHYRESETOUT#, PHYRESETOUT2#	Output	Output the PHY RESET signal (PHYRESETOUT#: for Ether0 and Ether1, PHYRESETOUT2#: for Ether2)
EtherCAT slave controller (ECATC) (optional)	CATLEDRUN	Output	Outputs the EtherCAT RUN LED signal.
	CATIRQ	Output	Outputs the EtherCAT IRQ signal.
	CATLEDSTER	Output	Outputs the EtherCAT Dual-color state LED signal.
	CATLEDERR	Output	Outputs the EtherCAT error LED signal.
	CATLINKACT0, CATLINKACT1	Output	Output the EtherCAT link/activity LED signal.
	CATSYNC0, CATSYNC1	Output	Output the EtherCAT SYNC signal.
	CATLATCH0	Input	Input the EtherCAT LATCH signal.
	CATLATCH1	Input	Input the EtherCAT LATCH signal.
	CATI2CCLK	Output	Outputs the EtherCAT EEPROM I^2C clock signal.
	CATI2CDATA	I/O	Inputs/outputs the EtherCAT EEPROM I^2C data signal.

Table 1.4 Pin Functions (6 / 7)

Classifications	Pin Name	I/O	Description
USB 2.0 host/function module	VDD33_USB	Input	Power supply input pin for USB
	VSS_USB	Input	Ground input pin for USB
	DVDD_USB	Input	Digital power supply input pin for USB
	USB_RREF	Input	Reference current input pin for USB. Connect this pin to the VSS_USB pin via 200 Ω (±1%).
	USB_DP	I/O	USB bus D+ data I/O pin
	USB_DM	I/O	USB bus D- data I/O pin
	USB_VBUSEN	Output	Outputs the VBUS power enable signal for USB.
	USB_OVRCUR	Input	Inputs the overcurrent signal for USB.
	USB_VBUSIN	Input	USB cable connection/disconnection detection input pin
CAN module (RSCAN)	CRXD0, CRXD1	Input	Receive data input pins
	CTXD0, CTXD1	Output	Transmit data output pins
Serial peripheral interface (RSPIa)	RSPCK0 to RSPCK3	I/O	Clock I/O pins
	MOSI0 to MOSI3	I/O	Master transmit data I/O pins
	MISO0 to MISO3	I/O	Slave transmit data I/O pins
	SSL00, SSL10, SSL20, SSL30	I/O	Slave select signal I/O pins
	SSL01, SSL02, SSL03, SSL11	Output	Slave select signal output pins
SPI multi I/O bus controller (SPIBSC)	SPBCLK	Output	Clock output pin
	SPBSSL	Output	Slave select signal output pin
	SPBMO/SPBIO0	I/O	Master transmit data/data 0 I/O pin
	SPBMI/SPBIO1	I/O	Master input data/data 1 I/O pin
	SPBIO2, SPBIO3	I/O	Data 2, data 3 I/O pins
Serial sound interface (SSI)	SSISCK0	I/O	SSI serial bit clock I/O pin
	SSIWS0	I/O	Word select I/O pin
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	AUDIO_CLK	Input	Master clock pin for audio
ΔΣ interface (DSMIF)	MCLK0 to MCLK3	I/O	Clock I/O pins
	MDAT0 to MDAT3	Input	Data input pins
12-bit A/D converter (S12ADCa)	AN000 to AN007, AN100 to AN115	Input	Analog input pins for A/D converter
	ADTRG0, ADTRG1	Input	External trigger input pins for the start of A/D conversion
	AN1_ANEX0	Output	Extended analog outpu pin
	AN1_ANEX1	Input	Extended analog input pin
Analog power supply	AVCC0	Input	Analog power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Reference power supply input pin for the 12-bit A/D converter (unit 0). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.

Table 1.4 Pin Functions (7 / 7)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC1	Input	Analog power supply input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	AVSS1	Input	Analog ground input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
	VREFH1	Input	Reference power supply input pin for the 12-bit A/D converter (unit 1). Connect this pin to the VCCQ33 pin if the 12-bit A/D converter is not to be used.
	VREFL1	Input	Reference ground pin for the 12-bit A/D converter (unit 1). Connect this pin to the VSS pin if the 12-bit A/D converter is not to be used.
I/O ports	P00 to P07	I/O	8-bit I/O pin
	P10 to P17	I/O	8-bit I/O pin
	P20 to P27	I/O	8-bit I/O pins
	P30 to P37	Input, I/O	1-bit input pin (P30), 7-bit I/O pins (P31 to P37) I/O pins
	P40 to P47	I/O	8-bit I/O pins
	P50 to P56	I/O	7-bit I/O pins
	P60 to P67	I/O	8-bit I/O pins
	P70 to P77	I/O	8-bit I/O pins
	P80 to P87	I/O	8-bit I/O pins
	P90 to P97	I/O	8-bit I/O pins
	PA0 to PA7	I/O	8-bit I/O pins
	PB0 to PB7	I/O	8-bit I/O pins
	PC0 to PC7	Input	8-bit input pins
	PD0 to PD7	I/O	8-bit I/O pins
	PE0 to PE7	I/O	8-bit I/O pins
	PF5 to PF7	I/O	3-bit I/O pins
	PG0 to PG7	I/O	8-bit I/O pins
	PH0 to PH7	I/O	8-bit I/O pins
	PJ0 to PJ7	I/O	8-bit I/O pins
	PK0 to PK7	I/O	8-bit I/O pins
	PL0 to PL7	I/O	8-bit I/O pins
	PM0 to PM7	I/O	8-bit I/O pins
	PN0 to PN7	I/O	8-bit I/O pins
	PP0 to PP7	I/O	8-bit I/O pins
	PR0 to PR7	I/O	8-bit I/O pins
	PS0 to PS7	I/O	8-bit I/O pins
	PT0 to PT7	I/O	8-bit I/O pins
	PU0 to PU7	I/O	8-bit I/O pins
Encoder I/F*1	ENCIF00 to ENCIF12	I/O	I/O pins for multi-protocol encoder interface

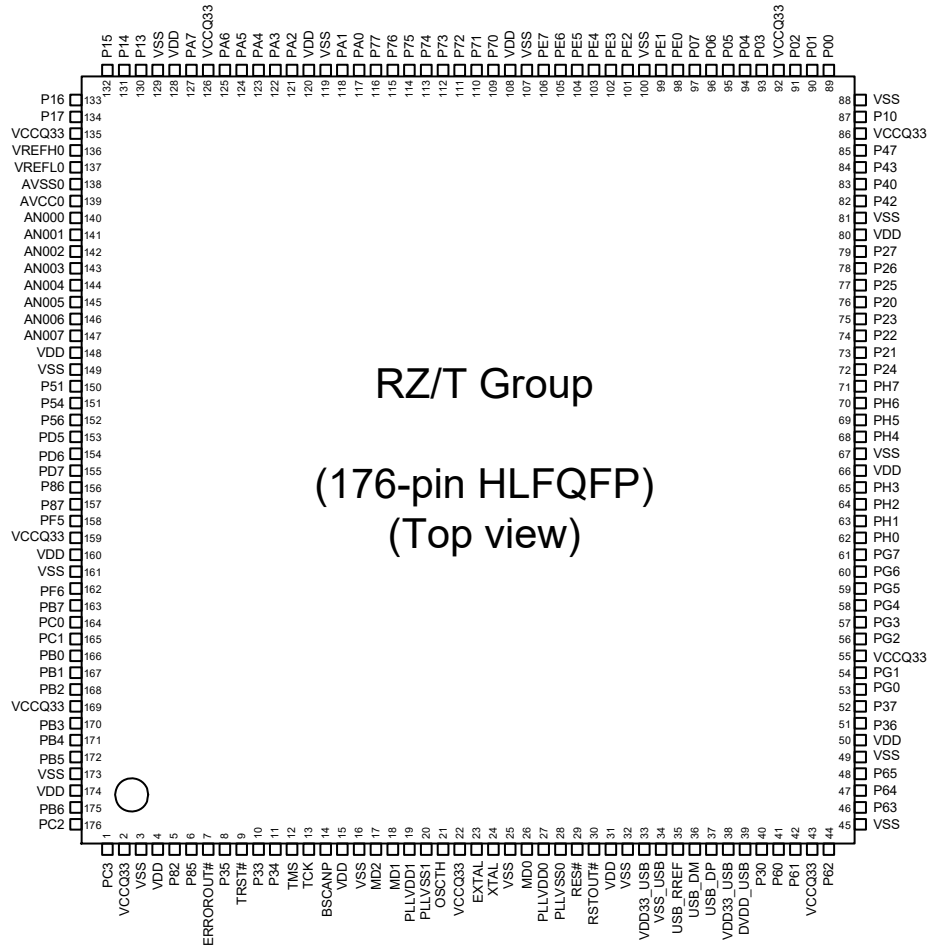
Note 1. Only in products with the encoder interfaces.

1.6 Pin Assignments

Figure 1.2 and Figure 1.3 show the pin arrangement. Table 1.5 and Table 1.6 show the pin assignments. Table 1.7 and Table 1.8 show the lists of pin functions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	PC2	PJ3	PJ1	PF7	PB4	PB0	PC0	PF6	VCCQ33	P54	VSS	AN007	AN005	AN002	AVCC0	AVCC1	VREFH1	P17	VSS	A
B	PJ5	PJ4	PC3	PJ2	PJ0	PB5	PB2	PC1	PB7	P86	PD7	P52	AN006	AN003	AN001	AVSS0	AVSS1	VREFL1	P16	P15	B
C	PJ7	PJ6	PU2	PL7	PL5	PB6	PB3	PB1	PF5	P87	PD6	P53	P51	AN004	AN000	VREFL0	VREFH0	PD2	P14	P13	C
D	P81	P80	PU3															PD0	P96	P95	D
E	P84	P82	PU1		PU0	PL6	PL4	PL2	PL0	PK7	PK6	PD5	P56	PD4	VCCQ33	PD1		P97	P94	P93	E
F	PC4	P83	P85		PU4	VSS	VCCQ33	PL3	PL1	PK5	PK4	P55	P50	PD3	PK2	P90		P92	P91	P12	F
G	PU6	PC5	VCCQ33		PU5	PM0									PK3	PA7		PA4	PA3	P11	G
H	PU7	PM1	P35		ERROROUT#	VCCQ33		VDD	VDD	VDD	VDD	VDD	VSS		PA6	PA5		PA2	PK0	PK1	H
J	PM6	PM3	PM2		P33	TRST#		VDD	VSS	VSS	VSS	VSS	VDD		VCCQ33	PA1		PA0	PT7	PT6	J
K	PM7	PM5	PM4		P34	PLLVDD1		VDD	VSS	VSS	VSS	VSS	VDD		VSS	P77		P76	P75	PT5	K
L	MD1	MD2	TMS		TCK	PLLVSS1		VDD	VSS	VSS	VSS	VSS	VDD		VSS	PE7		P72	P73	P74	L
M	XTAL	EXTAL	OSCTH		BSCANP	PLLVDD0		VDD	VSS	VSS	VSS	VSS	VDD		VCCQ33	PE6		P70	PT4	P71	M
N	VSS	MD0	RSTOUT#		RES#	PLLVSS0		VDD	VSS	VDD	VDD	VDD	VDD		PE2	PE4		PE5	PT2	PT3	N
P	VSS_USB	VDD33_USB	USB_REF		P31	VCCQ33									P06	P07		PE3	PT0	PT1	P
R	USB_DP	USB_DM	P30		PN0	PN2	PG0	PG2	PG7	PH2	PH4	PH6	P23	P27	P47	VCCQ33		VCCQ33	PS6	PS7	R
T	DVDD_USB	VDD33_USB	P32		PC6	P37	P36	PG3	PG6	PH3	VCCQ33	PH5	VCCQ33	P26	VCCQ33	VSS		VSS	PE0	PE1	T
U	P60	P63	PN1															P00	P04	P03	U
V	P61	P64	PN3	PN4	PC7	PG1	PG4	PG5	PH0	PH1	PH7	P20	P21	VSS	P45	P46	PS2	P05	P01	P02	V
W	P62	P65	PN5	PN6	PP0	PP2	PP4	PP6	PP7	PR1	PR3	PR5	P24	P22	P44	P43	PS1	PS3	PS4	PS5	W
Y	VSS	P67	P66	PN7	PP1	PP3	PP5	VSS	PR0	PR2	PR4	PR6	PR7	P25	P41	P42	P40	PS0	P10	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 1.2 Pin Arrangement (320-Pin FBGA) (Top View)



Note 1. This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (176-Pin HLFQFP).

Note 2. It is recommended to connect the exposed die pad of HLFQFP to VSS.

Figure 1.3 Pin Arrangement (176-pin HLFQFP)

Table 1.5 Pin Assignments (320-Pin FBGA) (1 / 8)

Pin Number	Pin Name
A1	VSS
A2	PC2 / ETH0_TXC / ETH1_RXD2 / CATI2CDATA / SDA0
A3	PJ3 / IRQ11 / ETH0_TXD0 / ADTRG0
A4	PJ1 / ETH0_TXD2 / CATLEDSTER / RSPCK3
A5	PF7 / IRQ7 / A25 / ETH0_TXER / RTS3# / SSL30
A6	PB4 / A24 / ETH1_COL / ETH0_RXER / CATSYNC0 / CATLATCH0 / RXD3 / MOSI3 / MDAT0
A7	PB0 / ETH1_RXDV / MTCLKB / TCLKD / TIC3
A8	PC0 / WAIT# / ETH1_RXD2 / GTETRG / SCL1 / MDAT3
A9	PF6 / ETH1_RXD0 / MTIOC3D / GTIOC0B / TOC2
A10	VCCQ33
A11	P54 / CLKOUT25M1 / MOSI2
A12	VSS
A13	AN007
A14	AN005
A15	AN002
A16	AVCC0
A17	AVCC1
A18	VREFH1
A19	P17 / CS5# / ETH1_TXER / PHYRESETOUT# / ADTRG0
A20	VSS
B1	PJ5 / ETH0_RXD1 / TIOCD0 / RXD3
B2	PJ4 / ETH0_RXD0 / TXD3
B3	PC3 / ETH0_RXC / ETH0_RXDV / CATI2CCLK / RXD4 / SCL0 / CRXD1
B4	PJ2 / IRQ10 / ETH0_TXD1 / MISO3
B5	PJ0 / IRQ8 / ETH0_TXD3 / CATLEDERR / MOSI3
B6	PB5 / ETH_MDIO / TCLKB / POE0# / POE10# / CTS3# / RSPCK3
B7	PB2 / ETH1_RXC / ETH0_RXD1 / CATSYNC1 / CATLATCH1 / MTIOC1A / SSL30 / MDAT1
B8	PC1 / IRQ9 / ETH1_RXD3 / PHYLINK0 / SDA1 / MDAT2
B9	PB7 / ETH1_RXD1 / MTIOC3B / GTIOC0A / TOC3
B10	P86 / AN1_ANEX0 / ETH1_TXD0 / MTIOC4B / GTIOC2A / TOC1 / RSPCK2
B11	PD7 / AN115 / ETH1_TXD1 / MTIOC4D / GTIOC2B / TOC0
B12	P52 / ETH0_INT / SSL20
B13	AN006
B14	AN003
B15	AN001
B16	AVSS0
B17	AVSS1
B18	VREFL1
B19	P16 / CS4# / CS2# / MTIOC3B / GTIOC0A / ENCIF12
B20	P15 / CS3# / CKE / MTIOC3D / GTIOC0B / ENCIF11
C1	PJ7 / IRQ15 / ETH0_RXD3 / CATLEDRUN / CTS3#
C2	PJ6 / IRQ14 / ETH0_RXD2 / CATIRQ / SCK3
C3	PU2 / IRQ2 / ETH2_CRS / TIOCD9 / RXD3
C4	PL7 / IRQ15 / ETH2_RXDV

Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8)

Pin Number	Pin Name
C5	PL5 / ETH2_RXD2 / TIOCA8
C6	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
C7	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
C8	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
C9	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
C10	P87 / AN1_ANEX1 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
C11	PD6 / AN114 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
C12	P53 / ETH1_INT / MISO2
C13	P51 / IRQ1 / PHYLINK1 / RSPCK2
C14	AN004
C15	AN000
C16	VREFL0
C17	VREFH0
C18	PD2 / AN110 / WAIT#
C19	P14 / CAS# / MTIOC4A / GTIOC1A / ENCIF10
C20	P13 / RAS# / MTIOC4C / GTIOC1B
D1	P81 / ETH0_RXER / TIOCC0 / CTS4#
D2	P80 / IRQ8 / ETH0_RXDV / TIOCC3 / RTS4#
D3	PU3 / ETH2_COL / TIOCD6 / TXD3
D18	PD0 / AN108 / CS4#
D19	P96 / AN106 / POE0# / POE10# / ENCIF09
D20	P95 / AN105 / IRQ13 / MTCLKA / CTS2#
E1	P84 / ETH0_COL / CATLINKACT1 / RXD4
E2	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
E3	PU1 / ETH2_RXC / TIOCA11 / SCK3
E5	PU0 / ETH2_RXER / TIOCA10
E6	PL6 / ETH2_RXD3 / TIOCA9
E7	PL4 / IRQ4 / ETH2_RXD1
E8	PL2 / ETH2_TXEN / TIOCA6 / ADTRG1
E9	PL0 / ETH2_TXD0 / TIOCB9
E10	PK7 / ETH2_TXD2 / TIOCB7
E11	PK6 / ETH2_TXD3 / TIOCB6
E12	PD5 / AN113 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
E13	P56 / BS# / ETH1_TXER
E14	PD4 / AN112 / ETH2_INT
E15	VCCQ33
E16	PD1 / AN109 / CS1#
E18	P97 / AN107 / IRQ7 / A25 / ADTRG1
E19	P94 / AN104 / IRQ4 / MTCLKB / RTS2# / ENCIF08
E20	P93 / AN103 / MTIOC1A / TIC3 / SCK2 / ENCIF07
F1	PC4 / CATI2CCLK / TCLKH / SCL0
F2	P83 / IRQ11 / ETH0_CRS / CATLINKACT0 / TXD4
F3	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
F5	PU4 / MII2_MDC / TIOCC9 / CTS3#
F6	VSS

Table 1.5 Pin Assignments (320-Pin FBGA) (3 / 8)

Pin Number	Pin Name
F7	VCCQ33
F8	PL3 / ETH2_RXD0 / TIOCA7
F9	PL1 / ETH2_TXC / TIOCB10
F10	PK5 / ETH2_TXD1 / TIOCB8
F11	PK4 / ETH2_TXER / TIOCB11 / MOSI2
F12	P55 / IRQ5 / A24 / ETHSWSECOUT
F13	P50 / IRQ8 / CS1# / PHYLINK0
F14	PD3 / AN111 / PHYRESETOUT2#
F15	PK2 / A23
F16	P90 / AN100 / RAS# / TIOCA5 / TXD4
F18	P92 / AN102 / CS5# / TOC3 / RXD2
F19	P91 / AN101 / CAS# / TXD2 / ENCIF06
F20	P12 / MTIOC4B / GTIOC2A
G1	PU6 / PHYRESETOUT# / TCLKF / CTS4#
G2	PC5 / CATI2CDATA / TCLKG / SDA0
G3	VCCQ33
G5	PU5 / IRQ13 / MII2_MDIO / TIOCC6 / RTS3#
G6	PM0 / CLKOUT25M2 / TXD4
G15	PK3 / A24
G16	PA7 / IRQ7 / D31 / A22 / MTIOC6B / GTIOC3B / RTS2# / MCLK0
G18	PA4 / D28 / ETH1_INT / TIOCA3 / ADTRG0 / RXD2 / TEND2 / MDAT1
G19	PA3 / D27 / ETHSWSECOUT / GTETRG / TIOCA2 / SCK2 / DACK2 / MCLK2
G20	P11 / IRQ9 / MTIOC4D / GTIOC2B
H1	PU7 / CATIRQ / RXD4
H2	PM1 / CATLEDERR / SCK4
H3	P35 / NMI
H5	ERROROUT#
H6	VCCQ33
H8	VDD
H9	VDD
H10	VDD
H11	VDD
H12	VDD
H13	VSS
H15	PA6 / IRQ6 / D30 / A21 / GTIOC3A / CTS2# / MDAT0
H16	PA5 / D29 / ETH0_INT / ETH1_TXER / TIOCA4 / TXD2 / MCLK1
H18	PA2 / D26 / MTIOC3B / GTIOC0A / SSL02 / DREQ2 / MDAT2/ ENCIF05
H19	PK0 / CAS# / PO31 / ENCIF11
H20	PK1 / CS5# / ENCIF12
J1	PM6 / IRQ6 / CATLINKACT0 / PO19
J2	PM3 / CATSYNC0 / CATLATCH0 / PO16
J3	PM2 / CATSYNC1 / CATLATCH1 / TCLKE / RTS4#
J5	P33 / TDO
J6	TRST#
J8	VDD

Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8)

Pin Number	Pin Name
J9	VSS
J10	VSS
J11	VSS
J12	VSS
J13	VDD
J15	VCCQ33
J16	PA1 / D25 / MTIOC3D / GTIOC0B / MISO0 / AUDIO_CLK / TRACEDATA7 / MCLK3
J18	PA0 / D24 / MTIOC4A / GTIOC1A / MOSI0 / TRACEDATA6 / MDAT3
J19	PT7 / A22 / DACK2 / ENCIF10
J20	PT6 / A21 / DREQ2
K1	PM7 / CATLINKACT1 / PO20
K2	PM5 / CATLEDSTER / PO18
K3	PM4 / CATLEDRUN / PO17
K5	P34 / TDI
K6	PLLVDD1
K8	VDD
K9	VSS
K10	VSS
K11	VSS
K12	VSS
K13	VDD
K15	VSS
K16	P77 / D23 / MTIOC4C / GTIOC1B / RSPCK0 / TRACEDATA5
K18	P76 / D22 / MTIOC4B / GTIOC2A / SSL01 / SSIWS0 / TRACEDATA4
K19	P75 / IRQ13 / D21 / MTIOC4D / GTIOC2B / SSL00 / TRACEDATA3/ ENCIF04
K20	PT5 / BS# / PO30 / TEND2
L1	MD1
L2	MD2
L3	TMS
L5	TCK
L6	PLLVSS1
L8	VDD
L9	VSS
L10	VSS
L11	VSS
L12	VSS
L13	VDD
L15	VSS
L16	PE7 / D15 / MTIOC7A / TIOCD3 / POE8# / SCK1 / RSPCK0 / TRACEDATA7
L18	P72 / D18 / MTIOC1A / TIC2 / TXD1 / SSITXD0 / TRACEDATA0 / ENCIF02
L19	P73 / IRQ3 / D19 / MTCLKB / RXD1 / SSIRXD0 / TRACEDATA1 / ENCIF03
L20	P74 / D20 / MTCLKA / CTS1# / SSL03 / SSISCK0 / TRACEDATA2
M1	XTAL
M2	EXTAL
M3	OSCTH

Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8)

Pin Number	Pin Name
M5	BSCANP
M6	PLLVDD0
M8	VDD
M9	VSS
M10	VSS
M11	VSS
M12	VSS
M13	VDD
M15	VCCQ33
M16	PE6 / IRQ6 / D14 / MTIOC0A / TIOCD0 / RXD1 / MISO0 / TRACEDATA6
M18	P70 / IRQ0 / D16 / MTIOC6D / RTS1# / USB_OVRCUR / TRACECLK / ENCIF00
M19	PT4 / CS3# / PO29
M20	P71 / D17 / POE0# / POE10# / TOC2 / SCK1 / TRACECTL / ENCIF01
N1	VSS
N2	MD0
N3	RSTOUT#
N5	RES#
N6	PLLVSS0
N8	VDD
N9	VSS
N10	VDD
N11	VDD
N12	VDD
N13	VDD
N15	PE2 / IRQ2 / D10 / MTCLKC / TIOCB4 / SSL02 / TRACEDATA2
N16	PE4 / D12 / MTIOC0B / TIOCC0 / RTS1# / SSL00 / TRACEDATA4
N18	PE5 / D13 / MTIOC0C / TIOCC3 / TXD1 / MOSI0 / TRACEDATA5
N19	PT2 / TIOCA1 / TIOCB1 / PO27
N20	PT3 / IRQ11 / TIOCA0 / TIOCB0 / PO28 / CTS2# / ENCIF09
P1	VSS_USB
P2	VDD33_USB
P3	USB_RREF
P5	P31 / USB_VBUSEN
P6	VCCQ33
P15	P06 / D6 / MTIOC2B / TIOCB0
P16	P07 / D7 / MTIOC2A / TIOCB1
P18	PE3 / IRQ3 / D11 / MTIOC0D / TIOCB5 / CTS1# / SSL01 / TRACEDATA3
P19	PT0 / IRQ0 / TIOCA3 / TIOCB3 / PO25 / SCK2 / ENCIF07
P20	PT1 / TIOCA2 / TIOCB2 / PO26 / RTS2# / ENCIF08
R1	USB_DP
R2	USB_DM
R3	P30 / CRXD0 / USB_VBUSIN
R5	PN0 / MTIOC8D / SSL10
R6	PN2 / IRQ10 / MTIOC8B / MOSI1
R7	PG0 / A1 / PO2

Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8)

Pin Number	Pin Name
R8	PG2 / A3 / PO4 / TOC0 / RSPCK1
R9	PG7 / A8 / PO9
R10	PH2 / A11 / MTIOC2A / PO12
R11	PH4 / IRQ4 / A13 / PO14
R12	PH6 / A15 / MTIOC7D / RTS0#
R13	P23 / A0 / MTIC5U / TXD0 / DACK1
R14	P27 / A20 / MTIOC8C / TIOCB0 / RTS0#
R15	P47 / WE3#/DQMUU/AH# / MTIOC6C
R16	VCCQ33
R18	VCCQ33
R19	PS6 / IRQ14 / TIOCA5 / TIOCB5 / PO23 / RXD2 / ENCIF06
R20	PS7 / TIOCA4 / TIOCB4 / PO24 / TXD2
T1	DVDD_USB
T2	VDD33_USB
T3	P32 / IRQ10 / USB_OVRCUR
T5	PC6 / TCLKC / SCL1 / CRXD0 / DREQ0 / USB_VBUSIN
T6	P37 / WE1#/DQMLU / PO1
T7	P36 / WE0#/DQMLL / PO0
T8	PG3 / A4 / PO5 / TIC1 / MISO1
T9	PG6 / A7 / TCLKB / PO8 / SSL11
T10	PH3 / A12 / MTIOC1B / PO13
T11	VCCQ33
T12	PH5 / A14 / PO15
T13	VCCQ33
T14	P26 / A19 / MTIOC8D / DREQ1
T15	VCCQ33
T16	VSS
T18	VSS
T19	PE0 / D8 / MTIOC1B / TIOCB2 / TRACEDATA0
T20	PE1 / D9 / MTCLKD / TIOCB3 / SSL03 / TRACEDATA1
U1	P60 / SPBSSL / CTXD0 / TEND0
U2	P63 / SPBMO/SPBIO0
U3	PN1 / MTIOC8C / PO21 / MISO1 / ENCIF09
U18	P00 / D0 / MTIOC6A / TIOCA1 / ADTRG1 / TRACECTL
U19	P04 / D4 / MTIOC3C / TIOCA5
U20	P03 / D3 / MTIC5U / TIOCA4
V1	P61 / SPBIO3 / CTXD1 / DACK0
V2	P64 / SPBMI/SPBIO1
V3	PN3 / MTIOC8A / RSPCK1
V4	PN4 / IRQ12 / MTIOC6C / TIOCC6 / SSL11
V5	PC7 / TIC0 / SDA1 / CRXD1
V6	PG1 / A2 / PO3
V7	PG4 / A5 / PO6 / TOC1 / MOSI1
V8	PG5 / A6 / TCLKA / PO7 / SSL10
V9	PH0 / A9 / PO10

Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8)

Pin Number	Pin Name
V10	PH1 / A10 / MTIOC2B / PO11
V11	PH7 / A16 / MTIC5W
V12	P20 / A17 / MTCLKD
V13	P21 / IRQ1 / CS0# / MTIC5V / TIOCB1 / CTS0#
V14	VSS
V15	P45 / CS2#
V16	P46 / CKE
V17	PS2 / MTIOC7C / SSIWS0
V18	P05 / D5 / MTIOC3A
V19	P01 / D1 / MTIC5W / TIOCA2
V20	P02 / D2 / MTIC5V / TIOCA3
W1	P62 / SPBCLK
W2	P65 / SPBIO2 / DREQ0
W3	PN5 / IRQ5 / MTIOC6A / TIOCD9 / ENCIF10
W4	PN6 / MTIOC3C / TIOCC9 / MCLK3 / ENCIF11
W5	PP0 / POE8# / TEND0 / MCLK2
W6	PP2 / MTIOC0C / TCLKH / MCLK1
W7	PP4 / MTIOC0A / MCLK0
W8	PP6 / TIOCA11 / RXD1 / TRACECTL / ENCIF06
W9	PP7 / TCLKF / TCLKH / SCK1 / DACK1 / TRACECLK
W10	PR1 / IRQ9 / POE4# / CTS1# / TEND1 / TRACEDATA1 / ENCIF08
W11	PR3 / TIOCA10 / TIOCB10 / TRACEDATA3 / ENCIF01
W12	PR5 / TIOCA8 / TIOCB8 / TRACEDATA5 / ENCIF03
W13	P24 / IRQ12 / RD/WR# / RXD0
W14	P22 / IRQ2 / RD# / MTIOC7B / TIOCD0 / SCK0
W15	P44 / IRQ12 / WAIT# / TCLKD / ADTRG0 / CTS0#
W16	P43 / WE2#/DQMUL / MTIOC8B / USB_VBUSEN
W17	PS1 / IRQ1 / MTIOC7B / SSISCK0
W18	PS3 / MTIOC7A / SSIRXD0
W19	PS4 / MTIOC6D / SSITXD0
W20	PS5 / MTIOC6B
Y1	VSS
Y2	P67 / IRQ15 / GTIOC3B / CTXD0 / TEND0 / USB_OVRCUR
Y3	P66 / IRQ14 / GTIOC3A / CTXD1 / DACK0 / USB_VBUSEN
Y4	PN7 / MTIOC3A / TIOCD6 / DREQ0 / MDAT3 / ENCIF12
Y5	PP1 / MTIOC0D / DACK0 / MDAT2
Y6	PP3 / MTIOC0B / TCLKC / MDAT1
Y7	PP5 / PO22 / MDAT0
Y8	VSS
Y9	PR0 / TCLKE / TCLKG / TXD1 / DREQ1 / TRACEDATA0 / ENCIF07
Y10	PR2 / TIOCA11 / TIOCB11 / RTS1# / TRACEDATA2 / ENCIF00
Y11	PR4 / TIOCA9 / TIOCB9 / TRACEDATA4 / ENCIF02
Y12	PR6 / TIOCA7 / TIOCB7 / TRACEDATA6 / ENCIF04
Y13	PR7 / TIOCA6 / TIOCB6 / TRACEDATA7 / ENCIF05
Y14	P25 / A18 / MTCLKC / TEND1

Table 1.5 Pin Assignments (320-Pin FBGA) (8 / 8)

Pin Number	Pin Name
Y15	P41 / BS# / SCK0
Y16	P42 / MTIOC7C / RXD0
Y17	P40 / MTIOC8A / TXD0
Y18	PS0 / MTIOC7D / AUDIO_CLK
Y19	P10 / IRQ0 / CKIO / TIOCA0 / TRACECLK
Y20	VSS

Table 1.6 Pin Assignments (176-Pin HLFQFP) (1 / 4)

Pin Number	Pin Name
1	PC3 / ETH0_RXC / ETH0_RXDV / RXD4 / SCL0 / CRXD1
2	VCCQ33
3	VSS
4	VDD
5	P82 / ETH0_TXEN / ETH1_CRS / TIOCD3 / SCK4 / RTS3# / USB_OVRCUR
6	P85 / IRQ5 / CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN
7	ERROROUT#
8	P35 / NMI
9	TRST#
10	P33 / TDO
11	P34 / TDI
12	TMS
13	TCK
14	BSCANP
15	VDD
16	VSS
17	MD2
18	MD1
19	PLLVDD1
20	PLLVSS1
21	OSCTH
22	VCCQ33
23	EXTAL
24	XTAL
25	VSS
26	MD0
27	PLLVDD0
28	PLLVSS0
29	RES#
30	RSTOUT#
31	VDD
32	VSS
33	VDD33_USB
34	VSS_USB
35	USB_RREF
36	USB_DM
37	USB_DP
38	VDD33_USB
39	DVDD_USB
40	P30 / CRXD0 / USB_VBUSIN
41	P60 / SPBSSL / CTXD0 / TEND0
42	P61 / SPBIO3 / CTXD1 / DACK0
43	VCCQ33
44	P62 / SPBCLK

Table 1.6 Pin Assignments (176-Pin HLFQFP) (2 / 4)

Pin Number	Pin Name
45	VSS
46	P63 / SPBMO/SPBIO0
47	P64 / SPBMI/SPBIO1
48	P65 / SPBIO2 / DREQ0
49	VSS
50	VDD
51	P36 / WE0#/DQMLL / PO0
52	P37 / WE1#/DQMLU / PO1
53	PG0 / A1 / PO2
54	PG1 / A2 / PO3
55	VCCQ33
56	PG2 / A3 / PO4 / TOC0 / RSPCK1
57	PG3 / A4 / PO5 / TIC1 / MISO1
58	PG4 / A5 / PO6 / TOC1 / MOSI1
59	PG5 / A6 / TCLKA / PO7 / SSL10
60	PG6 / A7 / TCLKB / PO8 / SSL11
61	PG7 / A8 / PO9
62	PH0 / A9 / PO10
63	PH1 / A10 / MTIOC2B / PO11
64	PH2 / A11 / MTIOC2A / PO12
65	PH3 / A12 / MTIOC1B / PO13
66	VDD
67	VSS
68	PH4 / IRQ4 / A13 / PO14
69	PH5 / A14 / PO15
70	PH6 / A15 / MTIOC7D / RTS0#
71	PH7 / A16 / MTIC5W
72	P24 / IRQ12 / RD/WR# / RXD0
73	P21 / IRQ1 / CS0# / MTIC5V / TIOCB1 / CTS0#
74	P22 / IRQ2 / RD# / MTIOC7B / TIOCD0 / SCK0
75	P23 / A0 / MTIC5U / TXD0 / DACK1
76	P20 / A17 / MTCLKD
77	P25 / A18 / MTCLKC / TEND1
78	P26 / A19 / MTIOC8D / DREQ1
79	P27 / A20 / MTIOC8C / TIOCB0 / RTS0#
80	VDD
81	VSS
82	P42 / MTIOC7C / RXD0
83	P40 / MTIOC8A / TXD0
84	P43 / WE2#/DQMUL / MTIOC8B / USB_VBUSEN
85	P47 / WE3#/DQMUU/AH# / MTIOC6C
86	VCCQ33
87	P10 / IRQ0 / CKIO / TIOCA0 / TRACECLK
88	VSS
89	P00 / D0 / MTIOC6A / TIOCA1 / TRACECTL

Table 1.6 Pin Assignments (176-Pin HLFQFP) (3 / 4)

Pin Number	Pin Name
90	P01 / D1 / MTIC5W / TIOCA2
91	P02 / D2 / MTIC5V / TIOCA3
92	VCCQ33
93	P03 / D3 / MTIC5U / TIOCA4
94	P04 / D4 / MTIOC3C / TIOCA5
95	P05 / D5 / MTIOC3A
96	P06 / D6 / MTIOC2B / TIOCB0
97	P07 / D7 / MTIOC2A / TIOCB1
98	PE0 / D8 / MTIOC1B / TIOCB2 / TRACEDATA0
99	PE1 / D9 / MTCLKD / TIOCB3 / SSL03 / TRACEDATA1
100	VSS
101	PE2 / IRQ2 / D10 / MTCLKC / TIOCB4 / SSL02 / TRACEDATA2
102	PE3 / IRQ3 / D11 / MTIOC0D / TIOCB5 / CTS1# / SSL01 / TRACEDATA3
103	PE4 / D12 / MTIOC0B / TIOCC0 / RTS1# / SSL00 / TRACEDATA4
104	PE5 / D13 / MTIOC0C / TIOCC3 / TXD1 / MOSI0 / TRACEDATA5
105	PE6 / IRQ6 / D14 / MTIOC0A / TIOCD0 / RXD1 / MISO0 / TRACEDATA6
106	PE7 / D15 / MTIOC7A / TIOCD3 / POE8# / SCK1 / RSPCK0 / TRACEDATA7
107	VSS
108	VDD
109	P70 / IRQ0 / D16 / MTIOC6D / RTS1# / USB_OVRCUR / TRACECLK
110	P71 / D17 / POE0# / POE10# / TOC2 / SCK1 / TRACECTL
111	P72 / D18 / MTIOC1A / TIC2 / TXD1 / SSITXD0 / TRACEDATA0
112	P73 / IRQ3 / D19 / MTCLKB / RXD1 / SSIRXD0 / TRACEDATA1
113	P74 / D20 / MTCLKA / CTS1# / SSL03 / SSISCK0 / TRACEDATA2
114	P75 / IRQ13 / D21 / MTIOC4D / GTIOC2B / SSL00 / TRACEDATA3
115	P76 / D22 / MTIOC4B / GTIOC2A / SSL01 / SSIWS0 / TRACEDATA4
116	P77 / D23 / MTIOC4C / GTIOC1B / RSPCK0 / TRACEDATA5
117	PA0 / D24 / MTIOC4A / GTIOC1A / MOSI0 / TRACEDATA6 / MDAT3
118	PA1 / D25 / MTIOC3D / GTIOC0B / MISO0 / AUDIO_CLK / TRACEDATA7 / MCLK3
119	VSS
120	VDD
121	PA2 / D26 / MTIOC3B / GTIOC0A / SSL02 / DREQ2 / MDAT2
122	PA3 / D27 / ETHSWSECOUT / GTETRG / TIOCA2 / SCK2 / DACK2 / MCLK2
123	PA4 / D28 / ETH1_INT / TIOCA3 / ADTRG0 / RXD2 / TEND2 / MDAT1
124	PA5 / D29 / ETH0_INT / ETH1_TXER / TIOCA4 / TXD2 / MCLK1
125	PA6 / IRQ6 / D30 / A21 / GTIOC3A / CTS2# / MDAT0
126	VCCQ33
127	PA7 / IRQ7 / D31 / A22 / MTIOC6B / GTIOC3B / RTS2# / MCLK0
128	VDD
129	VSS
130	P13 / RAS# / MTIOC4C / GTIOC1B
131	P14 / CAS# / MTIOC4A / GTIOC1A
132	P15 / CS3# / CKE / MTIOC3D / GTIOC0B
133	P16 / CS4# / CS2# / MTIOC3B / GTIOC0A
134	P17 / CS5# / ETH1_TXER / PHYRESETOUT# / ADTRG0

Table 1.6 Pin Assignments (176-Pin HLFQFP) (4 / 4)

Pin Number	Pin Name
135	VCCQ33
136	VREFH0
137	VREFL0
138	AVSS0
139	AVCC0
140	AN000
141	AN001
142	AN002
143	AN003
144	AN004
145	AN005
146	AN006
147	AN007
148	VDD
149	VSS
150	P51 / IRQ1 / PHYLINK1 / RSPCK2
151	P54 / CLKOUT25M1 / MOSI2
152	P56 / BS# / ETH1_TXER
153	PD5 / A21 / ETH1_TXD3 / ETH0_TXD0 / TIC0 / SSL20 / MCLK3
154	PD6 / A22 / ETH1_TXD2 / ETH0_TXD1 / TIC1 / MISO2 / MCLK2
155	PD7 / ETH1_TXD1 / MTIOC4D / GTIOC2B / TOC0
156	P86 / ETH1_TXD0 / MTIOC4B / GTIOC2A / TOC1 / RSPCK2
157	P87 / A23 / ETH1_TXC / ETH0_RXD0 / MTIOC4C / GTIOC1B / MCLK1
158	PF5 / ETH1_TXEN / MTIOC4A / GTIOC1A / TIC2
159	VCCQ33
160	VDD
161	VSS
162	PF6 / ETH1_RXD0 / MTIOC3D / GTIOC0B / TOC2
163	PB7 / ETH1_RXD1 / MTIOC3B / GTIOC0A / TOC3
164	PC0 / WAIT# / ETH1_RXD2 / GTETRG / SCL1 / MDAT3
165	PC1 / IRQ9 / ETH1_RXD3 / PHYLINK0 / SDA1 / MDAT2
166	PB0 / ETH1_RXDV / MTCLKB / TCLKD / TIC3
167	PB1 / ETH1_RXER / MTCLKA / TCLKC / CTS4#
168	PB2 / ETH1_RXC / ETH0_RXD1 / MTIOC1A / SSL30 / MDAT1
169	VCCQ33
170	PB3 / IRQ3 / CS1# / ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1 / MCLK0
171	PB4 / A24 / ETH1_COL / ETH0_RXER / RXD3 / MOSI3 / MDAT0
172	PB5 / ETH_MDIO / TCLKB / POE0# / POE10# / CTS3# / RSPCK3
173	VSS
174	VDD
175	PB6 / ETH_MDC / TCLKA / SCK3 / RTS4# / MISO3
176	PC2 / ETH0_TXC / ETH1_RXD2 / SDA0

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (1 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
A1	VSS							
A2		PC2			ETH0_TXC / ETH1_RXD2 / CATI2CDATA / SDA0			
A3		PJ3			ETH0_TXD0		IRQ11	ADTRG0
A4		PJ1			ETH0_TXD2 / CATLEDSTER / RSPCK3			
A5		PF7	A25		ETH0_TXER / RTS3# / SSL30		IRQ7	
A6		PB4	A24		ETH1_COL / ETH0_RXER / CATSYNC0 / CATLATCH0 / RXD3 / MOSI3	MDAT0		
A7		PB0		MTCLKB / TCLKD / TIC3	ETH1_RXDV			
A8		PC0	WAIT#	GTETRG	ETH1_RXD2 / SCL1	MDAT3		
A9		PF6		MTIOC3D / GTIOC0B / TOC2	ETH1_RXD0			
A10	VCCQ33							
A11		P54			CLKOUT25M1 / MOSI2			
A12	VSS							
A13								AN007
A14								AN005
A15								AN002
A16	AVCC0							
A17	AVCC1							
A18	VREFH1							
A19		P17	CS5#		ETH1_TXER / PHYRESETOUT#			ADTRG0
A20	VSS							
B1		PJ5		TIOCD0	ETH0_RXD1 / RXD3			
B2		PJ4			ETH0_RXD0 / TXD3			
B3		PC3			ETH0_RXC / ETH0_RXDV / CATI2CCLK / RXD4 / SCL0 / CRXD1			
B4		PJ2			ETH0_TXD1 / MISO3		IRQ10	
B5		PJ0			ETH0_TXD3 / CATLEDERR / MOSI3		IRQ8	
B6		PB5		TCLKB / POE0# / POE10#	ETH_MDIO / CTS3# / RSPCK3			

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
B7		PB2		MTIOC1A	ETH1_RXC / ETH0_RXD1 / CATSYNC1 / CATLATCH1 / SSL30	MDAT1		
B8		PC1			ETH1_RXD3 / PHYLINK0 / SDA1	MDAT2	IRQ9	
B9		PB7		MTIOC3B / GTIOC0A / TOC3	ETH1_RXD1			
B10		P86		MTIOC4B / GTIOC2A / TOC1	ETH1_TXD0 / RSPCK2			AN1_ ANEX0
B11		PD7		MTIOC4D / GTIOC2B / TOC0	ETH1_TXD1			AN115
B12		P52			ETH0_INT / SSL20			
B13								AN006
B14								AN003
B15								AN001
B16	AVSS0							
B17	AVSS1							
B18	VREFL1							
B19		P16	CS4# / CS2#	MTIOC3B / GTIOC0A		ENCIF12		
B20		P15	CS3# / CKE	MTIOC3D / GTIOC0B		ENCIF11		
C1		PJ7			ETH0_RXD3 / CATLEDRUN / CTS3#		IRQ15	
C2		PJ6			ETH0_RXD2 / CATIRQ / SCK3		IRQ14	
C3		PU2		TIOCD9	ETH2_CRS / RXD3		IRQ2	
C4		PL7			ETH2_RXDV		IRQ15	
C5		PL5		TIOCA8	ETH2_RXD2			
C6		PB6		TCLKA	ETH_MDC / SCK3 / RTS4# / MISO3			
C7		PB3	CS1#		ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1	MCLK0	IRQ3	
C8		PB1		MTCLKA / TCLKC	ETH1_RXER / CTS4#			
C9		PF5		MTIOC4A / GTIOC1A / TIC2	ETH1_TXEN			
C10		P87	A23	MTIOC4C / GTIOC1B	ETH1_TXC / ETH0_RXD0	MCLK1		AN1_ ANEX1
C11		PD6	A22	TIC1	ETH1_TXD2 / ETH0_TXD1 / MISO2	MCLK2		AN114
C12		P53			ETH1_INT / MISO2			
C13		P51			PHYLINK1 / RSPCK2		IRQ1	
C14								AN004

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
C15								AN000
C16	VREFL0							
C17	VREFH0							
C18		PD2	WAIT#					AN110
C19		P14	CAS#	MTIOC4A / GTIOC1A		ENCIF10		
C20		P13	RAS#	MTIOC4C / GTIOC1B				
D1		P81		TIOCC0	ETH0_RXER / CTS4#			
D2		P80		TIOCC3	ETH0_RXDV / RTS4#		IRQ8	
D3		PU3		TIOCD6	ETH2_COL / TXD3			
D18		PD0	CS4#					AN108
D19		P96		POE0# / POE10#		ENCIF09		AN106
D20		P95		MTCLKA	CTS2#		IRQ13	AN105
E1		P84			ETH0_COL / CATLINKACT1 / RXD4			
E2		P82		TIOCD3	ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR			
E3		PU1		TIOCA11	ETH2_RXC / SCK3			
E5		PU0		TIOCA10	ETH2_RXER			
E6		PL6		TIOCA9	ETH2_RXD3			
E7		PL4			ETH2_RXD1		IRQ4	
E8		PL2		TIOCA6	ETH2_TXEN			ADTRG1
E9		PL0		TIOCB9	ETH2_TXD0			
E10		PK7		TIOCB7	ETH2_TXD2			
E11		PK6		TIOCB6	ETH2_TXD3			
E12		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		AN113
E13		P56	BS#		ETH1_TXER			
E14		PD4			ETH2_INT			AN112
E15	VCCQ33							
E16		PD1	CS1#					AN109
E18		P97	A25				IRQ7	ADTRG1 / AN107
E19		P94		MTCLKB	RTS2#	ENCIF08	IRQ4	AN104
E20		P93		MTIOC1A / TIC3	SCK2	ENCIF07		AN103
F1		PC4		TCLKH	CATI2CCLK / SCL0			
F2		P83			ETH0_CRS / CATLINKACT0 / TXD4		IRQ11	

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (4 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
F3		P85			CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN		IRQ5	
F5		PU4		TIOCC9	MII2_MDC / CTS3#			
F6	VSS							
F7	VCCQ33							
F8		PL3		TIOCA7	ETH2_RXD0			
F9		PL1		TIOCB10	ETH2_TXC			
F10		PK5		TIOCB8	ETH2_TXD1			
F11		PK4		TIOCB11	ETH2_TXER / MOSI2			
F12		P55	A24		ETHSWSECOUT		IRQ5	
F13		P50	CS1#		PHYLINK0		IRQ8	
F14		PD3			PHYRESETOUT2#			AN111
F15		PK2	A23					
F16		P90	RAS#	TIOCA5	TXD4			AN100
F18		P92	CS5#	TOC3	RXD2			AN102
F19		P91	CAS#		TXD2	ENCIF06		AN101
F20		P12		MTIOC4B / GTIOC2A				
G1		PU6		TCLKF	PHYRESETOUT# / CTS4#			
G2		PC5		TCLKG	CATI2CDATA / SDA0			
G3	VCCQ33							
G5		PU5		TIOCC6	MII2_MDIO / RTS3#		IRQ13	
G6		PM0			CLKOUT25M2 / TXD4			
G15		PK3	A24					
G16		PA7	D31 / A22	MTIOC6B / GTIOC3B	RTS2#	MCLK0	IRQ7	
G18		PA4	D28 / TEND2	TIOCA3	ETH1_INT / RXD2	MDAT1		ADTRG0
G19		PA3	D27 / DACK2	GTETRG / TIOCA2	ETHSWSECOUT / SCK2	MCLK2		
G20		P11		MTIOC4D / GTIOC2B			IRQ9	
H1		PU7			CATIRQ / RXD4			
H2		PM1			CATLEDERR / SCK4			
H3		P35					NMI	
H5	ERROROUT#							
H6	VCCQ33							
H8	VDD							
H9	VDD							
H10	VDD							
H11	VDD							

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
H12	VDD							
H13	VSS							
H15		PA6	D30 / A21	GTIOC3A	CTS2#	MDAT0	IRQ6	
H16		PA5	D29	TIOCA4	ETH0_INT / ETH1_TXER / TXD2	MCLK1		
H18		PA2	D26 / DREQ2	MTIOC3B / GTIOC0A	SSL02	MDAT2 / ENCIF05		
H19		PK0	CAS#	PO31		ENCIF11		
H20		PK1	CS5#			ENCIF12		
J1		PM6		PO19	CATLINKACT0		IRQ6	
J2		PM3		PO16	CATSYNC0 / CATLATCH0			
J3		PM2		TCLKE	CATSYNC1 / CATLATCH1 / RTS4#			
J5	TDO	P33						
J6	TRST#							
J8	VDD							
J9	VSS							
J10	VSS							
J11	VSS							
J12	VSS							
J13	VDD							
J15	VCCQ33							
J16	TRACEDATA7	PA1	D25	MTIOC3D / GTIOC0B	MISO0	AUDIO_CLK / MCLK3		
J18	TRACEDATA6	PA0	D24	MTIOC4A / GTIOC1A	MOSI0	MDAT3		
J19		PT7	A22 / DACK2			ENCIF10		
J20		PT6	A21 / DREQ2					
K1		PM7		PO20	CATLINKACT1			
K2		PM5		PO18	CATLEDSTER			
K3		PM4		PO17	CATLEDRUN			
K5	TDI	P34						
K6	PLLVDD1							
K8	VDD							
K9	VSS							
K10	VSS							
K11	VSS							
K12	VSS							
K13	VDD							
K15	VSS							
K16	TRACEDATA5	P77	D23	MTIOC4C / GTIOC1B	RSPCK0			

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (6 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
K18	TRACEDATA4	P76	D22	MTIOC4B / GTIOC2A	SSL01	SSIWS0		
K19	TRACEDATA3	P75	D21	MTIOC4D / GTIOC2B	SSL00	ENCIF04	IRQ13	
K20		PT5	BS# / TEND2	PO30				
L1	MD1							
L2	MD2							
L3	TMS							
L5	TCK							
L6	PLLVSS1							
L8	VDD							
L9	VSS							
L10	VSS							
L11	VSS							
L12	VSS							
L13	VDD							
L15	VSS							
L16	TRACEDATA7	PE7	D15	MTIOC7A / TIOCD3 / POE8#	SCK1 / RSPCK0			
L18	TRACEDATA0	P72	D18	MTIOC1A / TIC2	TXD1	SSITXD0 / ENCIF02		
L19	TRACEDATA1	P73	D19	MTCLKB	RXD1	SSIRXD0 / ENCIF03	IRQ3	
L20	TRACEDATA2	P74	D20	MTCLKA	CTS1# / SSL03	SSISCK0		
M1	XTAL							
M2	EXTAL							
M3	OSCTH							
M5	BSCANP							
M6	PLLVDD0							
M8	VDD							
M9	VSS							
M10	VSS							
M11	VSS							
M12	VSS							
M13	VDD							
M15	VCCQ33							
M16	TRACEDATA6	PE6	D14	MTIOC0A / TIOCD0	RXD1 / MISO0		IRQ6	
M18	TRACECLK	P70	D16	MTIOC6D	RTS1# / USB_OVRCUR	ENCIF00	IRQ0	
M19		PT4	CS3#	PO29				
M20	TRACECTL	P71	D17	POE0# / POE10# / TOC2	SCK1	ENCIF01		
N1	VSS							
N2	MD0							

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
N3	RSTOUT#							
N5	RES#							
N6	PLLVSS0							
N8	VDD							
N9	VSS							
N10	VDD							
N11	VDD							
N12	VDD							
N13	VDD							
N15	TRACEDATA2	PE2	D10	MTCLKC / TIOCB4	SSL02		IRQ2	
N16	TRACEDATA4	PE4	D12	MTIOC0B / TIOCC0	RTS1# / SSL00			
N18	TRACEDATA5	PE5	D13	MTIOC0C / TIOCC3	TXD1 / MOSI0			
N19		PT2		TIOCA1 / TIOCB1 / PO27				
N20		PT3		TIOCA0 / TIOCB0 / PO28	CTS2#	ENCIF09	IRQ11	
P1	VSS_USB							
P2	VDD33_USB							
P3	USB_RREF							
P5		P31			USB_VBUSEN			
P6	VCCQ33							
P15		P06	D6	MTIOC2B / TIOCB0				
P16		P07	D7	MTIOC2A / TIOCB1				
P18	TRACEDATA3	PE3	D11	MTIOC0D / TIOCB5	CTS1# / SSL01		IRQ3	
P19		PT0		TIOCA3 / TIOCB3 / PO25	SCK2	ENCIF07	IRQ0	
P20		PT1		TIOCA2 / TIOCB2 / PO26	RTS2#	ENCIF08		
R1	USB_DP							
R2	USB_DM							
R3		P30			CRXD0 / USB_VBUSIN			
R5		PN0		MTIOC8D	SSL10			
R6		PN2		MTIOC8B	MOSI1		IRQ10	
R7		PG0	A1	PO2				
R8		PG2	A3	PO4 / TOC0	RSPCK1			
R9		PG7	A8	PO9				
R10		PH2	A11	MTIOC2A / PO12				
R11		PH4	A13	PO14			IRQ4	
R12		PH6	A15	MTIOC7D	RTS0#			
R13		P23	A0 / DACK1	MTIC5U	TXD0			
R14		P27	A20	MTIOC8C / TIOCB0	RTS0#			
R15		P47	WE3# / DQMUU / AH#	MTIOC6C				

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
R16	VCCQ33							
R18	VCCQ33							
R19		PS6		TIOCA5 / TIOCB5 / PO23	RXD2	ENCIF06	IRQ14	
R20		PS7		TIOCA4 / TIOCB4 / PO24	TXD2			
T1	DVDD_USB							
T2	VDD33_USB							
T3		P32			USB_OVRCUR		IRQ10	
T5		PC6	DREQ0	TCLKC	SCL1 / CRXD0 / USB_VBUSIN			
T6		P37	WE1# / DQMLU	PO1				
T7		P36	WE0# / DQMLL	PO0				
T8		PG3	A4	PO5 / TIC1	MISO1			
T9		PG6	A7	TCLKB / PO8	SSL11			
T10		PH3	A12	MTIOC1B / PO13				
T11	VCCQ33							
T12		PH5	A14	PO15				
T13	VCCQ33							
T14		P26	A19 / DREQ1	MTIOC8D				
T15	VCCQ33							
T16	VSS							
T18	VSS							
T19	TRACEDATA0	PE0	D8	MTIOC1B / TIOCB2				
T20	TRACEDATA1	PE1	D9	MTCLKD / TIOCB3	SSL03			
U1		P60	TEND0		CTXD0 / SPBSSL			
U2		P63			SPBMO / SPBIO0			
U3		PN1		MTIOC8C / PO21	MISO1	ENCIF09		
U18	TRACECTL	P00	D0	MTIOC6A / TIOCA1				ADTRG1
U19		P04	D4	MTIOC3C / TIOCA5				
U20		P03	D3	MTIC5U / TIOCA4				
V1		P61	DACK0		CTXD1 / SPBIO3			
V2		P64			SPBMI / SPBIO1			
V3		PN3		MTIOC8A	RSPCK1			
V4		PN4		MTIOC6C / TIOCC6	SSL11		IRQ12	
V5		PC7		TIC0	SDA1 / CRXD1			
V6		PG1	A2	PO3				
V7		PG4	A5	PO6 / TOC1	MOSI1			
V8		PG5	A6	TCLKA / PO7	SSL10			
V9		PH0	A9	PO10				
V10		PH1	A10	MTIOC2B / PO11				
V11		PH7	A16	MTIC5W				

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10)

Pin Number 320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
V12		P20	A17	MTCLKD				
V13		P21	CS0#	MTIC5V / TIOCB1	CTS0#		IRQ1	
V14	VSS							
V15		P45	CS2#					
V16		P46	CKE					
V17		PS2		MTIOC7C		SSIWS0		
V18		P05	D5	MTIOC3A				
V19		P01	D1	MTIC5W / TIOCA2				
V20		P02	D2	MTIC5V / TIOCA3				
W1		P62			SPBCLK			
W2		P65	DREQ0		SPBIO2			
W3		PN5		MTIOC6A / TIOCD9		ENCIF10	IRQ5	
W4		PN6		MTIOC3C / TIOCC9		MCLK3 / ENCIF11		
W5		PP0	TEND0	POE8#		MCLK2		
W6		PP2		MTIOC0C / TCLKH		MCLK1		
W7		PP4		MTIOC0A		MCLK0		
W8	TRACECTL	PP6		TIOCA11	RXD1	ENCIF06		
W9	TRACECLK	PP7	DACK1	TCLKF / TCLKH	SCK1			
W10	TRACEDATA1	PR1	TEND1	POE4#	CTS1#	ENCIF08	IRQ9	
W11	TRACEDATA3	PR3		TIOCA10 / TIOCB10		ENCIF01		
W12	TRACEDATA5	PR5		TIOCA8 / TIOCB8		ENCIF03		
W13		P24	RD/WR#		RXD0		IRQ12	
W14		P22	RD#	MTIOC7B / TIOCD0	SCK0		IRQ2	
W15		P44	WAIT#	TCLKD	CTS0#		IRQ12	ADTRG0
W16		P43	WE2# / DQMUL	MTIOC8B	USB_VBUSEN			
W17		PS1		MTIOC7B		SSISCK0	IRQ1	
W18		PS3		MTIOC7A		SSIRXD0		
W19		PS4		MTIOC6D		SSITXD0		
W20		PS5		MTIOC6B				
Y1	VSS							
Y2		P67	TEND0	GTIOC3B	CTXD0 / USB_OVRCUR		IRQ15	
Y3		P66	DACK0	GTIOC3A	CTXD1 / USB_VBUSEN		IRQ14	
Y4		PN7	DREQ0	MTIOC3A / TIOCD6		MDAT3 / ENCIF12		
Y5		PP1	DACK0	MTIOC0D		MDAT2		
Y6		PP3		MTIOC0B / TCLKC		MDAT1		
Y7		PP5		PO22		MDAT0		
Y8	VSS							
Y9	TRACEDATA0	PR0	DREQ1	TCLKE / TCLKG	TXD1	ENCIF07		
Y10	TRACEDATA2	PR2		TIOCA11 / TIOCB11	RTS1#	ENCIF00		

Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (10 / 10)

Pin Number				Timer	Communication	Others		
320-Pin FBGA	Power Supply Clock System Control	I/O Port	Bus	(MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	(ETHERC, ECATC*1, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	(SSI, DSMIF, Encoder I/F)	Interrupt	S12ADCa
Y11	TRACEDATA4	PR4		TIOCA9 / TIOCB9		ENCIF02		
Y12	TRACEDATA6	PR6		TIOCA7 / TIOCB7		ENCIF04		
Y13	TRACEDATA7	PR7		TIOCA6 / TIOCB6		ENCIF05		
Y14		P25	A18 / TEND1	MTCLKC				
Y15		P41	BS#		SCK0			
Y16		P42		MTIOC7C	RXD0			
Y17		P40		MTIOC8A	TXD0			
Y18		PS0		MTIOC7D		AUDIO_CLK		
Y19	TRACECLK	P10	CKIO	TIOCA0			IRQ0	
Y20	VSS							

Note 1. Optional

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (1 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
1		PC3			ETH0_RXC / ETH0_RXDV / RXD4 / SCL0 / CRXD1			
2	VCCQ33							
3	VSS							
4	VDD							
5		P82		TIOCD3	ETH0_TXEN / ETH1_CRS / SCK4 / RTS3# / USB_OVRCUR			
6		P85			CLKOUT25M0 / TXD4 / SCK4 / USB_VBUSEN		IRQ5	
7	ERROROUT#							
8		P35					NMI	
9	TRST#							
10	TDO	P33						
11	TDI	P34						
12	TMS							
13	TCK							
14	BSCANP							
15	VDD							
16	VSS							
17	MD2							
18	MD1							
19	PLLVDD1							
20	PLLVSS1							
21	OSCTH							
22	VCCQ33							
23	EXTAL							
24	XTAL							
25	VSS							
26	MD0							
27	PLLVDD0							
28	PLLVSS0							
29	RES#							
30	RSTOUT#							
31	VDD							
32	VSS							
33	VDD33_USB							
34	VSS_USB							
35	USB_RREF							

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (2 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
36	USB_DM							
37	USB_DP							
38	VDD33_USB							
39	DVDD_USB							
40		P30			CRXD0 / USB_VBUSIN			
41		P60	TEND0		CTXD0 / SPBSSL			
42		P61	DACK0		CTXD1 / SPBIO3			
43	VCCQ33							
44		P62			SPBCLK			
45	VSS							
46		P63			SPBMO / SPBIO0			
47		P64			SPBMI / SPBIO1			
48		P65	DREQ0		SPBIO2			
49	VSS							
50	VDD							
51		P36	WE0# / DQMLL	PO0				
52		P37	WE1# / DQMLU	PO1				
53		PG0	A1	PO2				
54		PG1	A2	PO3				
55	VCCQ33							
56		PG2	A3	PO4 / TOC0	RSPCK1			
57		PG3	A4	PO5 / TIC1	MISO1			
58		PG4	A5	PO6 / TOC1	MOSI1			
59		PG5	A6	TCLKA / PO7	SSL10			
60		PG6	A7	TCLKB / PO8	SSL11			
61		PG7	A8	PO9				
62		PH0	A9	PO10				
63		PH1	A10	MTIOC2B / PO11				
64		PH2	A11	MTIOC2A / PO12				
65		PH3	A12	MTIOC1B / PO13				
66	VDD							
67	VSS							
68		PH4	A13	PO14			IRQ4	
69		PH5	A14	PO15				
70		PH6	A15	MTIOC7D	RTS0#			
71		PH7	A16	MTIC5W				
72		P24	RD/WR#		RXD0		IRQ12	
73		P21	CS0#	MTIC5V / TIOCB1	CTS0#		IRQ1	
74		P22	RD#	MTIOC7B / TIOCD0	SCK0		IRQ2	

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (3 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
75		P23	A0 / DACK1	MTIC5U	TXD0			
76		P20	A17	MTCLKD				
77		P25	A18 / TEND1	MTCLKC				
78		P26	A19 / DREQ1	MTIOC8D				
79		P27	A20	MTIOC8C / TIOCB0	RTS0#			
80	VDD							
81	VSS							
82		P42		MTIOC7C	RXD0			
83		P40		MTIOC8A	TXD0			
84		P43	WE2# / DQMUL	MTIOC8B	USB_VBUSEN			
85		P47	WE3# / DQMUU/AH#	MTIOC6C				
86	VCCQ33							
87	TRACECLK	P10	CKIO	TIOCA0			IRQ0	
88	VSS							
89	TRACECTL	P00	D0	MTIOC6A / TIOCA1				
90		P01	D1	MTIC5W / TIOCA2				
91		P02	D2	MTIC5V / TIOCA3				
92	VCCQ33							
93		P03	D3	MTIC5U / TIOCA4				
94		P04	D4	MTIOC3C / TIOCA5				
95		P05	D5	MTIOC3A				
96		P06	D6	MTIOC2B / TIOCB0				
97		P07	D7	MTIOC2A / TIOCB1				
98	TRACEDATA 0	PE0	D8	MTIOC1B / TIOCB2				
99	TRACEDATA 1	PE1	D9	MTCLKD / TIOCB3	SSL03			
100	VSS							
101	TRACEDATA 2	PE2	D10	MTCLKC / TIOCB4	SSL02		IRQ2	
102	TRACEDATA 3	PE3	D11	MTIOC0D / TIOCB5	CTS1# / SSL01		IRQ3	
103	TRACEDATA 4	PE4	D12	MTIOC0B / TIOCC0	RTS1# / SSL00			
104	TRACEDATA 5	PE5	D13	MTIOC0C / TIOCC3	TXD1 / MOSI0			
105	TRACEDATA 6	PE6	D14	MTIOC0A / TIOCD0	RXD1 / MISO0		IRQ6	

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (4 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
106	TRACEDATA 7	PE7	D15	MTIOC7A / TIOCD3 / POE8#	SCK1 / RSPCK0			
107	VSS							
108	VDD							
109	TRACECLK	P70	D16	MTIOC6D	RTS1# / USB_OVRCUR		IRQ0	
110	TRACECTL	P71	D17	POE0# / POE10# / TOC2	SCK1			
111	TRACEDATA 0	P72	D18	MTIOC1A / TIC2	TXD1	SSITXD0		
112	TRACEDATA 1	P73	D19	MTCLKB	RXD1	SSIRXD0	IRQ3	
113	TRACEDATA 2	P74	D20	MTCLKA	CTS1# / SSL03	SSISCK0		
114	TRACEDATA 3	P75	D21	MTIOC4D / GTIOC2B	SSL00		IRQ13	
115	TRACEDATA 4	P76	D22	MTIOC4B / GTIOC2A	SSL01	SSIWS0		
116	TRACEDATA 5	P77	D23	MTIOC4C / GTIOC1B	RSPCK0			
117	TRACEDATA 6	PA0	D24	MTIOC4A / GTIOC1A	MOSI0	MDAT3		
118	TRACEDATA 7	PA1	D25	MTIOC3D / GTIOC0B	MISO0	AUDIO_CLK/ MCLK3		
119	VSS							
120	VDD							
121		PA2	D26 / DREQ2	MTIOC3B / GTIOC0A	SSL02	MDAT2		
122		PA3	D27 / DACK2	GTETRG / TIOCA2	ETHSWSECOUT / SCK2	MCLK2		
123		PA4	D28 / TEND2	TIOCA3	ETH1_INT / RXD2	MDAT1		ADTRG0
124		PA5	D29	TIOCA4	ETH0_INT / ETH1_TXER / TXD2	MCLK1		
125		PA6	D30 / A21	GTIOC3A	CTS2#	MDAT0	IRQ6	
126	VCCQ33							
127		PA7	D31 / A22	MTIOC6B / GTIOC3B	RTS2#	MCLK0	IRQ7	
128	VDD							
129	VSS							
130		P13	RAS#	MTIOC4C / GTIOC1B				
131		P14	CAS#	MTIOC4A / GTIOC1A				
132		P15	CS3# / CKE	MTIOC3D / GTIOC0B				
133		P16	CS4# / CS2#	MTIOC3B / GTIOC0A				

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (5 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
134		P17	CS5#		ETH1_TXER / PHYRESETOUT#			ADTRG0
135	VCCQ33							
136	VREFH0							
137	VREFL0							
138	AVSS0							
139	AVCC0							
140								AN000
141								AN001
142								AN002
143								AN003
144								AN004
145								AN005
146								AN006
147								AN007
148	VDD							
149	VSS							
150		P51			PHYLINK1 / RSPCK2		IRQ1	
151		P54			CLKOUT25M1 / MOSI2			
152		P56	BS#		ETH1_TXER			
153		PD5	A21	TIC0	ETH1_TXD3 / ETH0_TXD0 / SSL20	MCLK3		
154		PD6	A22	TIC1	ETH1_TXD2 / ETH0_TXD1 / MISO2	MCLK2		
155		PD7		MTIOC4D / GTIOC2B / TOC0	ETH1_TXD1			
156		P86		MTIOC4B / GTIOC2A / TOC1	ETH1_TXD0 / RSPCK2			
157		P87	A23	MTIOC4C / GTIOC1B	ETH1_TXC / ETH0_RXD0	MCLK1		
158		PF5		MTIOC4A / GTIOC1A / TIC2	ETH1_TXEN			
159	VCCQ33							
160	VDD							
161	VSS							
162		PF6		MTIOC3D / GTIOC0B / TOC2	ETH1_RXD0			
163		PB7		MTIOC3B / GTIOC0A / TOC3	ETH1_RXD1			
164		PC0	WAIT#	GTETRG	ETH1_RXD2 / SCL1	MDAT3		

Table 1.8 List of Pin and Pin Functions (176-Pin HLFQFP) (6 / 6)

Pin Number 176-Pin HLFQFP	Power Supply Clock System Control	I/O Port	Bus	Timer (MTU3a, GPTa, TPUa, PPG, POE3, CMTW)	Communication (ETHERC, SCIFA, RSPIa, RIICa, RSCAN, SPIBSC, USB)	Others (SSI, DSMIF)	Interrupt	S12ADCa
165		PC1			ETH1_RXD3 / PHYLINK0 / SDA1	MDAT2	IRQ9	
166		PB0		MTCLKB / TCLKD / TIC3	ETH1_RXDV			
167		PB1		MTCLKA / TCLKC	ETH1_RXER / CTS4#			
168		PB2		MTIOC1A	ETH1_RXC / ETH0_RXD1 / SSL30	MDAT1		
169	VCCQ33							
170		PB3	CS1#		ETH1_CRS / PHYRESETOUT# / TXD3 / CTXD1	MCLK0	IRQ3	
171		PB4	A24		ETH1_COL / RXD3 / MOSI3 / ETH0_RXER	MDAT0		
172		PB5		TCLKB / POE0# / POE10#	ETH_MDIO / CTS3# / RSPCK3			
173	VSS							
174	VDD							
175		PB6		TCLKA	ETH_MDC / SCK3 / RTS4# / MISO3			
176		PC2			ETH0_TXC / ETH1_RXD2 / SDA0			

2. CPU

These LSI products include a Cortex-R4 CPU or, in products incorporating an R-IN engine, a Cortex-R4 CPU and Cortex-M3 CPU. The revision of each module is r1p4 (Cortex-R4) and r2p1 (Cortex-M3).

2.1 Overview

Table 2.1 Specifications of CPU

Item		Specification
Cortex-R4 (r1p4)	Minimum instruction execution time	One clock per instruction
	Address space	4 Gbytes
	Instruction cache size	8 Kbytes (with ECC)
	Data cache size	8 Kbytes (with ECC)
	Tightly coupled memory (TCM) size	ATCM: 512 Kbytes (with ECC) BTCM: 32 Kbytes (with ECC)
	Instruction set	Arm v7-R architecture supporting Thumb®/Thumb-2
	Data arrangement	Instruction: Little endian Data: Little endian
	Memory protection	Memory protection unit (MPU)
	FPU	• Supports addition, subtraction, multiplication, division, product-sum operation, and square-root operation in single-precision and double-precision • 32-bit single word register: 32 registers Can also be used as 16 64-bit double word registers
Cortex-M3 (r2p1) (in products incorporating an R-IN engine)	Minimum instruction execution time	One clock per instruction
	Address space	4 Gbytes
	Instruction set	Arm v7-M architecture supporting Thumb®/Thumb-2
	Data arrangement	Instruction: Little endian Data: Little endian
	Memory protection	Memory protection unit (MPU)

For details, refer to the following documents supplied by Arm.

- Arm Architecture Reference Manual Arm v7-A and Arm v7-R edition Issue C
- Arm v7-M Architecture Reference Manual

2.2 Configuration Information

Table 2.2 lists the configuration information for the Cortex-R4 of this LSI.

Table 2.2 Setting Values for Cortex-R4 Configuration Signals

Item		Setting Value
Endian	CFGEE	0
	CFGIE	0
Interrupt	CFGNMFI	1
Exception vector	TEINIT	0
	VINITHI	1
TCM configuration	INITRAMA	1
	INITRAMB	1
	LOCZRAMA	1
	CFGATCMSZ[3:0]	Ah
	CFGBTCMSZ[3:0]	6h
	ENTCM1IF	0
	SLBTCMSB	1 (don't care)
ECC, etc.	PARECCENRAM[2:0]	000b
	ERRENRAM[2:0]	000b
	RMWENRAM[1:0]	00b
	PARLVRAM	0 (don't care)

Table 2.3 only applies to products incorporating an R-IN engine and lists information on the configuration of the Cortex-M3 they incorporate.

Table 2.3 Setting Values for Cortex-M3 Configuration Signals

Item	Setting Value
BIGEND	0
DNOTITRANS	0
MPUDISABLE	0
STKALIGNINIT	1
DBGEN	1

2.3 Restrictions on CPU

For details on restrictions on Cortex-R4 and Cortex-M3 mounted on this LSI, refer to the information provided at the website of Arm.

2.4 Register Descriptions

2.4.1 ATCM Wait Control Register (SYTATCMWAIT)

SYTATCMWAIT is a register that controls ATCM access wait.
This register can be protected by the register write protection function. When writing to this register, cancel the write protection of bit 3 in the protection register (PRCR). For details, see section 11, Register Write Protection Function.

Address(es): A00B 0800h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ATCMWAIT[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	ATCMWAIT[1:0]	ATCM Wait Setting *1, *2	b1 b0 0 0: 1-wait with optimization 0 1: 1-wait without optimization 1 0: 0-wait 1 1: Setting prohibited	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the CPU clock frequency is 450 MHz or 600 MHz, set these bits for “1-wait with optimization” or “1-wait without optimization”.
For 320-pin FBGA, “0-wait” can be set only when the CPU clock frequency is 150 MHz or 300 MHz. It cannot be set when the frequency is 450 MHz or 600 MHz.
For 176-pin HLFQFP, “0-wait” can be set only when the CPU clock frequency is 150 MHz. It cannot be set when the frequency is 300 MHz or 450 MHz.

Note 2. If the ATCMWAIT[1:0] setting changes, operation cannot be guaranteed when the bus maser such as CPU accesses ACTM (including instruction fetch). To prevent fetch access from CPU, these bits should be handled by programs allocated in memory areas other than ATCM.

ATCMWAIT[1:0] Bits (ATCM Wait Setting)

These bits specify the number of memory access waits for ATCM.
In case of “with optimization”, memory access speed can be increased practically to 0-wait by prefetching the next address when instructions are fetched from sequential addresses in ATCM.

2.4.2 Semaphore Enable Register (SYTSEMFEN) (Only in products incorporating an R-IN engine)

SYTSEMFEN is a register that controls read clear function of the semaphore register n (SYTSEMFn, n = 0 to 7).

Address(es): A00B 0920h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEMFEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SEMFEN	Semaphore Enable	0: Read clear function disabled. 1: Read clear function enabled.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SEMFEN Bit (Semaphore Enable)

This bit specifies enable/disable of the read clear function of the semaphore register n. When the semaphore register (SYTSEMFn) is used, set this bit to 1 to enable the read clear function (n = 0 to 7).

2.4.3 Semaphore Register n (SYTSEMFn, n = 0 to 7) (Only in products incorporating an R-IN engine)

The SYTSEMFn register is used to perform semaphore for synchronization and exclusive control between the main CPU (Cortex-R4) and the sub-CPU (Cortex-M3). Resource status can be controlled when the resource is shared between CPUs.

Address(es): SYTSEMF0: A00B 0930h, SYTSEMF1: A00B 0934h, SYTSEMF2: A00B 0938h, SYTSEMF3: A00B 093Ch, SYTSEMF4: A00B 0940h, SYTSEMF5: A00B 0944h, SYTSEMF6: A00B 0948h, SYTSEMF7: A00B 094Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEMFn
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SEMFn	Semaphore Bit n	0: Resource being used 1: Resource not being used	R/W*1
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the read clear function is disabled (SYTSEMFEN.SEMFEN bit = 0), reading this bit does not clear it and its value is maintained.

SEMFn Bit (Semaphore Bit n)

This bit is used to set the status of the resource shared between CPUs to indicate whether the resource is being used or not. Writing 1 to this bit maintains it value. When the read clear function is enabled (SYTSEMFEN.SEMFEN bit = 1), reading this bit clears its value to 0.

Semaphore Control Procedure between the Main CPU (Cortex-R4) and the Sub-CPU (Cortex-M3)

When the semaphore register 0 (SYTSEMF0) is used for semaphore control for a resource A, for example, the following procedure takes place:

(1) Use the initialization routine of the main CPU to set the SYTSEMFEN.SEMFEN bit to 1 (this enables the read clear function).
(2) Set the SEMF0 bit to 1 (resource not being used) in the semaphore register 0 (SYTSEMF0).
(3) For example, when the sub-CPU attempts to use the resource A, the sub-CPU reads the semaphore register 0 (SYTSEMF0) repeatedly until 1 is read.
(4) When SEMF0 = 1 is read, the sub-CPU confirms that the resource is not being used.
This operation clears the SEMF0 bit of the semaphore register 0 (SYTSEMF0) to 0.
(5) Then the sub-CPU uses the resource A.
If the main CPU attempts to use the resource A while the sub-CPU is using it, 0 is read from the SYTSEMF0.SEMF0 bit (resource A being used by the sub-CPU). The main CPU repeats read operation and waits until the resource is released.
(6) When the sub-CPU completes its use of the resource A, 1 is written in the SYTSEMF0.SEMF0 bit to indicate that the resource A is released.
(7) If the main CPU attempts to use the resource A after the above step (6), it confirms whether the resource is used or not by reading the SYTSEMF0.SEMF0 bit. When the SYTSEMF0.SEMF0 bit is 1, the main CPU starts to use the resource A. This operation clears the SYTSEMF0.SEMF0 bit to 0.

2.5 Usage Notes

2.5.1 Releasing the Cortex-M3 from the Reset State

After power for the RZ/T1 is on, or after an RES# pin reset, ECM reset, or software reset, the initial setting is for the Cortex-M3 and WDTA for the Cortex-M3 to remain in the reset state.
To use the Cortex-M3 and WDTA for the Cortex-M3, control software reset register 2 (SWRR2) to release them from the reset state.
For details, see section 6.2.3, Software Reset Register 2 (SWRR2) (for products incorporating an R-IN engine).

2.5.2 Handling of Semaphore Register n (SYTSEMFn, n = 0 to 7)

For writing to a shared memory, for example, the target resource is to be made available by setting semaphore register n (SYTSEMFn). At this time, the previous round of writing to the same memory must have been completed. This is ensured by executing the DMB instruction before setting semaphore register n (see the following example program). By doing so, setting of the concerned register becomes possible only after the previous round of writing to the target memory is completed.

- Program Example

```
asm(“dmb”);                              // DMB instruction
SYSTEM.SYTSEMF0.BIT.SEMF0 = 1;
```

Note: The program format may differ from a compiler to another. Confirm the specification of the compiler you are using.

3. Operating Modes

3.1 Overview

This LSI chip is intended for booting up from an external flash memory. Three boot modes are available for types of flash memory that support three different operating modes. In each of the boot modes, the user program stored in the corresponding external flash memory is booted up and then runs.
Secure boot mode (in which a user program is protected by encryption) can also be selected for the products that support security function*1.

Note 1. This function is provided upon signing a nondisclosure agreement. For details, contact Renesas Electronics Corporation's sales office.

3.2 Types and Selection of Operating Modes

One of the three types of operating modes can be selected, depending on the method of connecting to an external memory. An operating mode is selected based on the input levels of the mode setting pins (MD2, MD1, and MD0) at the time pin reset (except software reset 2) is released.

Table 3.1 describes the relationship between the input levels of the mode setting pins (MD2, MD1, and MD0) at the time reset is released and the selected operating mode. For details on individual operating modes, see section 3.5, Operating Mode Descriptions.

Table 3.1 Selection of Operating Mode for Each Combination of Levels of Mode Setting Pins (MD2, MD1, and MD0)

Mode Setting Pins			
MD2	**MD1**	**MD0**	**Operating Mode**
Low	Low	Low	SPI boot mode (Serial flash) Boots a program from a serial flash memory connected to the SPI multi-I/O bus space.
Low	High	Low	16-bit bus boot mode (NOR flash) Boots a program from a NOR flash memory (bus width: 16 bits) connected to the CS0 space.
Low	High	High	32-bit bus boot mode (NOR flash) Boots a program from a NOR flash memory (bus width: 32 bits) connected to the CS0 space.
Other than above			Reserved (Setting prohibited)

3.3 Hardware Used in Individual Operating Modes

Table 3.2 describes hardware used in individual operating modes.
“Pins to be Used” indicates pins required to execute each operating mode. The functions for these pins are automatically configured at boot.

Table 3.2 Hardware Used in Individual Operating Modes

Operating Mode	Peripheral Module	Pins to be Used
SPI boot mode (Serial flash)	SPI Multi-I/O bus controller (SPIBSC)	SPBCLK, SPBSSL SPBMO, SPBMI
16-bit bus boot mode (NOR flash)	Bus state controller (BSC)	A20 to A1, D15 to D0 CS0#, RD#
32-bit bus boot mode (NOR flash)	Bus state controller (BSC)	A20 to A2, D31 to D0 CS0#, RD#

3.4 Register Descriptions

3.4.1 Mode Monitor Register (MDMONR)

Mode monitor register (MDMONR) indicates input levels of the MD2, MD1, and MD0 pins.

Address(es): A00B 0A60h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MD2	MD1	MD0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1 *1	0/1 *1	0/1 *1

Bit	Symbol	Bit Name	Description	R/W
b0	MD0	MD0 pin status flag	0: The MD0 pin is “Low”. 1: The MD0 pin is “High”.	R
b1	MD1	MD1 pin status flag	0: The MD1 pin is “Low”. 1: The MD1 pin is “High”.	R
b2	MD2	MD2 pin status flag	0: The MD2 pin is “Low”. 1: The MD2 pin is “High”.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. This value differs depending on the pin level at the time reset is released. For details, see section 6, Reset.

3.5 Operating Mode Descriptions

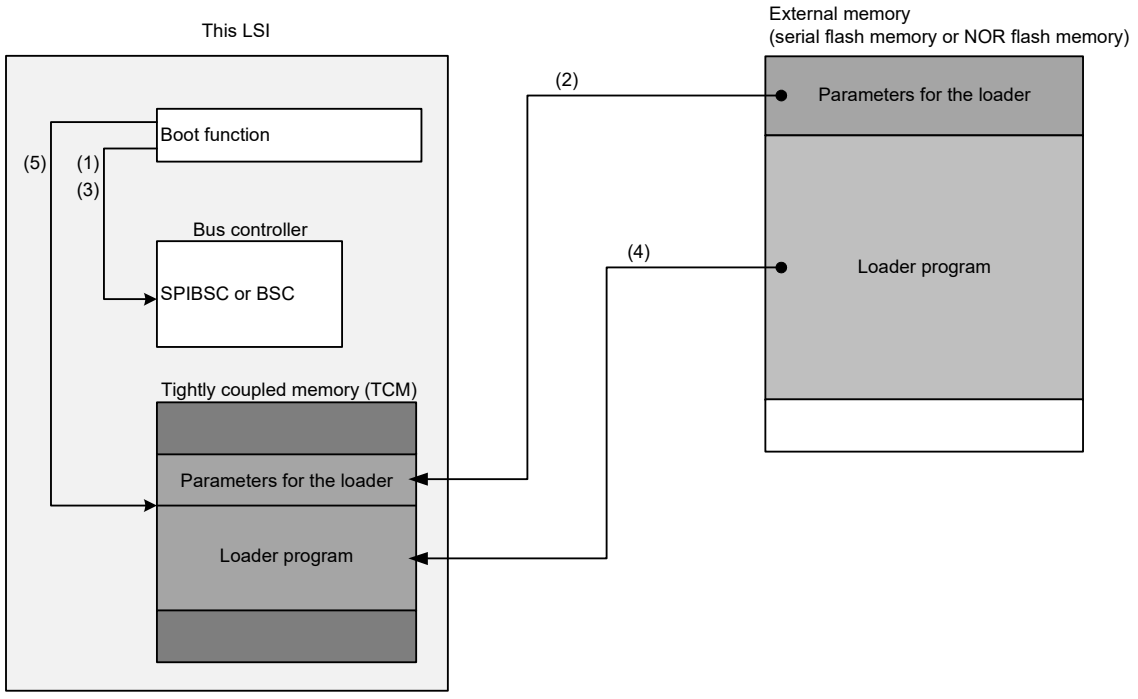
3.5.1 Boot Function

After reset is released on this LSI, the boot function executes the boot processing described below. The boot processing can extract a loader program that was stored in an external memory in advance by a user, to the internal tightly coupled memory (TCM) area, and hand over the processing to the loader program at the start address of that program.

(1) Setting the bus controller (SPIBSC or BSC) specified by the mode setting pins (MD2, MD1, and MD0)
(2) Loading parameters for the loader from an external memory, and executing checksum
(3) Setting for speeding up the bus controller (SPIBSC or BSC) by using parameters for the loader
(4) Loading the loader program from an external memory
(5) Branching off to the start address of the loader program extracted to the tightly coupled memory (TCM)

Parameters for the loader can have configuration information that suite for the user system, such as, loader program information, cache setting for speeding up the boot processing, and bus controller (SPIBSC or BSC) settings. Parameters for the loader must be stored in an external memory in advance by a user.

Figure 3.1 shows the operating overview of boot processing.

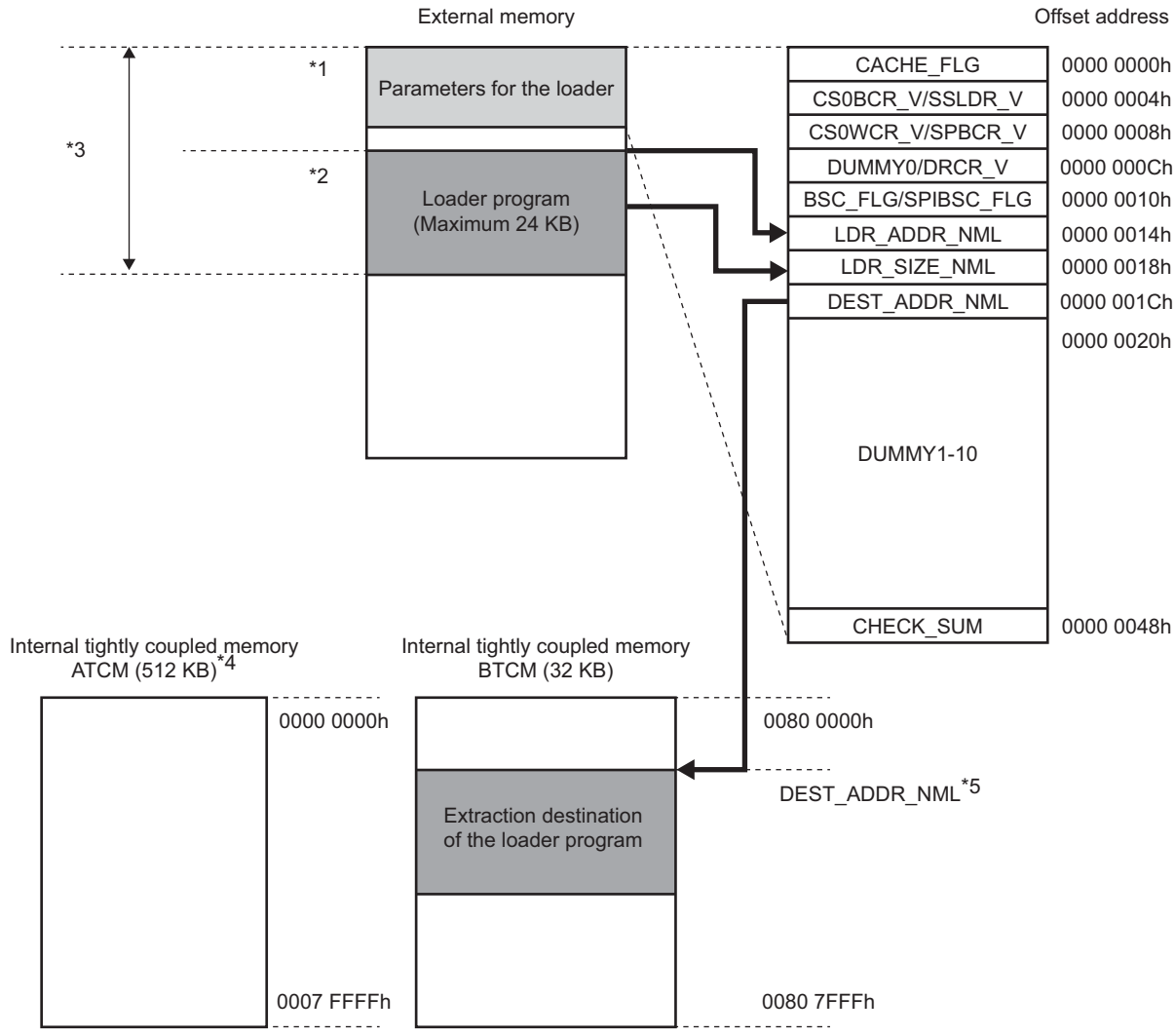


(1) Set the bus controller specified by the operating mode.
(2) Transfer the parameters for the loader from an external memory.
(3) Configure the bus controller based on the parameters for the loader.
(4) Transfer the loader program from an external memory.
(5) Hand over the processing to the loader program in the TCM area.

Figure 3.1 Operating Overview of Boot Processing

3.5.2 Parameters for the Loader

The parameters for the loader are setting parameters for boot processing, which are loaded from an external memory during boot processing and used by the boot function. The parameters for the loader specify information, such as the cache settings during boot processing in individual operating modes, setting of the bus controller (SPIBSC or BSC) used for communication with an external memory, and the size of the loader program.
Figure 3.2 shows memory assignment of the loader program and parameters for the loader.



Note 1. The parameters for the loader must be stored in the following address range:
SPI boot mode: SPI multi-I/O bus space (3000 0000h and higher)
16-bit or 32-bit bus boot mode: External address space (CS0) (4000 0000h and higher)
Note 2. The loader program can be stored in any address (LDR_ADDR_NML). Note that, however, the program size (LDR_SIZE_NML) must be multiples of 512 bytes and no more than 24 Kbytes.
Note 3. In SPI boot mode, address output is 3 bytes, so only use addresses in the range from 3000 0000h to 30FF FFFFh.
In 16-bit or 32-bit bus boot mode, use addresses in the range from 4000 0000h to 401F FFFFh because the address output pins (A1 to A20 for 16-bit bus boot mode and A2 to A20 for 32-bit bus boot mode) of the bus state controller (BSC) is used in this mode.
Note 4. The ATCM area is assumed to be used for storing user application programs.
Note 5. Specify the extraction destination area of the loader program so that the area falls in the range from 0080 2000h to 0080 7FFFh.

Figure 3.2 Memory Assignment of the Loader Program and Parameters for the Loader

Table 3.3 describes parameter information for the loader in 16-bit or 32-bit bus boot mode. Table 3.4 describes parameter information for the loader in SPI boot mode.

Table 3.3 Parameter Information for the Loader in 16-bit or 32-bit Bus Boot Mode

Offset Address	Parameter Name	Description
0000 0000h	CACHE_FLG	Selects whether to enable the I1 cache and D1 cache of Cortex-R4 during boot processing (for speeding up). 0000 0001h: Enables the I1 and D1 caches. Other setting values than above: Disables the I1 and D1 caches.
0000 0004h	CS0BCR_V	Setting value of the CS0 space bus control register (CS0BCR) This parameter value is set to the CS0BCR register during the setting for speeding up of BSC in (3) of section 3.5.1, Boot Function.*1
0000 0008h	CS0WCR_V	Setting value of the CS0 space wait control register (CS0WCR) This parameter value is set to the CS0WCR register during the setting for speeding up of BSC in (3) of section 3.5.1, Boot Function.*1
0000 000Ch	DUMMY0	Option (Not used in this mode.)
0000 0010h	BSC_FLG	Selects whether to change the BSC setting back to the initial value after the boot processing finishes. 2236 0679h: Changes the BSC setting value back to the initial value after the boot processing finishes. Other setting values than above: Retains the BCS setting value used in the boot processing.*2
0000 0014h	LDR_ADDR_NML	Sets the start address of the loader program stored in the external memory.*3
0000 0018h	LDR_SIZE_NML	Specifies the size of the loader program. Note that the program size must be multiples of 512 bytes and no more than 24 Kbytes.*3
0000 001Ch	DEST_ADDR_NML	Specifies the start address of the tightly coupled memory (BTCM) that is used as the extraction destination of the loader program. Specify the extraction destination area of the loader program so that the area falls in the range from 0080 2000h to 0080 7FFFh.
0000 0020h	DUMMY1	Option (Not used in this mode.)
0000 0024h	DUMMY2	Option (Not used in this mode.)
0000 0028h	DUMMY3	Option (Not used in this mode.)
0000 002Ch	DUMMY4	Option (Not used in this mode.)
0000 0030h	DUMMY5	Option (Not used in this mode.)
0000 0034h	DUMMY6	Option (Not used in this mode.)
0000 0038h	DUMMY7	Option (Not used in this mode.)
0000 003Ch	DUMMY8	Option (Not used in this mode.)
0000 0040h	DUMMY9	Option (Not used in this mode.)
0000 0044h	DUMMY10	Option (Not used in this mode.)
0000 0048h	CHECK_SUM	Checksum value for the parameters for the loader This parameter specifies the sum of the higher-order 16 bits and the lower-order 16 bits of the parameters (in unsigned long (32-bit) format) in the range of the offset addresses 0000h to 0044h*4.

Note 1. For details on the CS0BCR and CS0WCR registers, see section 14, Bus State Controller.
Note 2. For details on the settings of individual peripheral modules after the boot processing finishes, see section 3.5.5.1, Operation Settings in 16-Bit and 32-Bit Bus Boot Modes.
Note 3. LDR_ADDR_NML must be in the range from 4000 004Ch and LDR_ADDR_NML + LDR_SIZE_NML ≤ 4020 0000h in the external address space (CS0).
Note 4. An example for calculating CHECK_SUM is given below.
If CS0BCR_V = 36DB 0C00h,
CS0WCR_V = 0000 0340h,
LDR_ADDR_NML = 4000 004Ch,
LDR_SIZE_NML = 0000 6000h,
DEST_ADDR_NML= 0080 2000h, and
others = 0000 0000h,
CHECK_SUM is calculated as below ((0000h) is omitted in the formula):
CHECK_SUM = (36DBh) + (0C00h) + (0340h) + (4000h) + (004Ch) + (6000h) + (0080h) + (2000h) = (0001 06E7h)

Table 3.4 Parameter Information for the Loader in SPI Boot Mode

Offset Address	Parameter Name	Description
0000 0000h	CACHE_FLG	Selects whether to enable the I1 cache and D1 cache of Cortex-R4 at boot processing (for speeding up). 0000 0001h: Enables the I1 and D1 caches. Other setting values than above: Disables the I1 and D1 caches.
0000 0004h	SSLDR_V	Setting value of the SSL delay register (SSLDR) This parameter value is set to the SSLDR register during the setting for speeding up of SPIBSC in (3) of section 3.5.1, Boot Function.*1
0000 0008h	SPBCR_V	Setting value of the bit-rate configuration register (SPBCR) This parameter value is set to the SPBCR register during the setting for speeding up of SPIBSC in (3) of section 3.5.1, Boot Function.*1
0000 000Ch	DRCR_V	Setting value of the data read control register (DRCR) This parameter value is set to the DRCR register during the setting for speeding up of SPIBSC in (3) of section 3.5.1, Boot Function.*1
0000 0010h	SPIBSC_FLG	Selects whether to change the SPIBSC setting back to the initial value after the boot processing finishes. 2236 0679h: Changes the SPIBSC setting value back to the initial value after the boot processing finishes. Other setting values than above: Retains the SPIBCS setting value used during boot processing.*2
0000 0014h	LDR_ADDR_NML	Sets the start address of the loader program stored in the external memory.*3
0000 0018h	LDR_SIZE_NML	Specifies the size of the loader program. Note that the program size must be multiples of 512 bytes and no more than 24 Kbytes.*3
0000 001Ch	DEST_ADDR_NML	Specifies the start address of the tightly coupled memory (BTCM) that is used as the extraction destination of the loader program. Specify the extraction destination area of the loader program so that the area falls in the range from 0080 2000h to 0080 7FFFh.
0000 0020h	DUMMY1	Option (Not used in this mode.)
0000 0024h	DUMMY2	Option (Not used in this mode.)
0000 0028h	DUMMY3	Option (Not used in this mode.)
0000 002Ch	DUMMY4	Option (Not used in this mode.)
0000 0030h	DUMMY5	Option (Not used in this mode.)
0000 0034h	DUMMY6	Option (Not used in this mode.)
0000 0038h	DUMMY7	Option (Not used in this mode.)
0000 003Ch	DUMMY8	Option (Not used in this mode.)
0000 0040h	DUMMY9	Option (Not used in this mode.)
0000 0044h	DUMMY10	Option (Not used in this mode.)
0000 0048h	CHECK_SUM	Checksum value of the parameters for the loader This parameter specifies the sum of the higher-order 16 bits and the lower-order 16 bits of the parameters (in unsigned long (32-bit) format) in the range of the offset addresses 0000h to 0044h.*4

Note 1. For details about the SSLDR, SPBCR, and DRCR registers, see section 37, SPI Multi I/O Bus Controller (SPIBSC).
Note 2. For details about the setting status of the individual peripheral modules after the boot processing finishes, see section 3.5.4.1, Operation Settings in SPI Boot Mode.
Note 3. LDR_ADDR_NML must be in the range from 3000 004Ch and LDR_ADDR_NML + LDR_SIZE_NML ≤ 3100 0000h in the external address space (SPI).
Note 4. An example for calculating CHECK_SUM is given below.
If SSLDR_V = 0007 0707h,
SPBCR_V = 0000 0003h,
LDR_ADDR_NML = 3000 004Ch,
LDR_SIZE_NML = 0000 6000h,
DEST_ADDR_NML = 0080 2000h, and
others = 0000 0000h,
CHECK_SUM is calculated as below ((0000h) is omitted in the formula):
CHECK_SUM = (0007h) + (0707h) + (0003h) + (3000h) + (004Ch) + (6000h) + (0080h) + (2000h) = (0000 B7DDh)

3.5.3 Loader Program

The loader program is a user program that is transferred from an external memory to the internal tightly coupled memory (TCM) by the boot function, and starts its processing after the boot processing finishes. The loader program can execute such processing that suites the user system, for example, extracting a user application program from an external memory to the internal TCM area and executing it at high speed.
Set the loader program so that the following conditions are satisfied:

- Program size (LDR_SIZE_NML): Multiples of 512 bytes and no more than 24 Kbytes
- Storage address in the external memory (LDR_ADDR_NMI) in 16-bit or 32-bit bus boot mode: Address range from A1 to A20 for 16-bit bus boot mode and A2 to A20 for 32-bit bus boot mode
- Storage address in the external memory (LDR_ADDR_NML) in SPI boot mode: Address range from 3000 004Ch and LDR_ADDR_NML + LDR_SIZE_NML ≤ 3100 0000h

These setting values must be stored in an external memory as parameters for the loader. For details, see section 3.5.2, Parameters for the Loader.

3.5.4 SPI Boot Mode (Serial Flash)

In SPI boot mode, this LSI boots a program from an external serial flash memory connected to the SPI multi-I/O bus space.
In this mode, the SPI multi-I/O bus controller is set to the mode of reading the external address space, and the SPBCLK, SPBSSL, SPBMO, and SPBMI pins are enabled.
After the reset is released, this LSI executes the boot processing. The loader program stored in a serial flash memory connected to the SPI multi-I/O bus space is extracted to the internal memory (TCM), and then the processing is executed.
Figure 3.3 shows the connection diagram of this LSI with a serial flash memory.

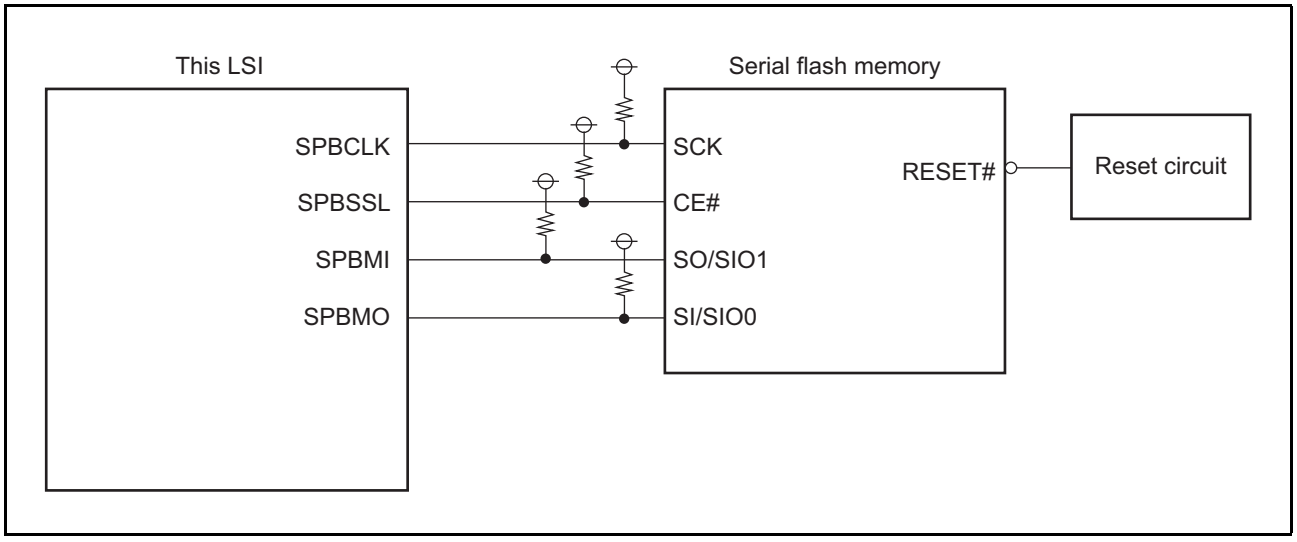


Figure 3.3 Connection Diagram of This LSI with a Serial Flash Memory

3.5.4.1 Operation Settings in SPI Boot Mode

Immediately after the boot processing starts in SPI boot mode after the reset is released, this LSI operates with the following initial setting values, and executes processing until transferring parameters for the loader.

- CPU clock (CPUCLK): 150 MHz
- SPIBSC bit rate (SPBCLK): 18.75 MHz
- Supported command: Read (03h)
- Address output: 3 bytes
- Dummy cycles: None
- Data read width: 1 bit
- SPI mode: CPOL = 0 (positive pulse)
  CPHAR = 0 (data reception at odd edge)
  CPHAT = 0 (data transmission at even edge)

After the parameters for the loader are loaded, the settings for the I1 and D1 caches of Cortex-R4 and for the SSLDR, SPBCR, and DRCR registers are performed based on the values of parameters CACHE_FLG, SSLDR_V, SPBCR_V, and DRCR_V, so that the processing can be speed up.

Table 3.5 describes the setting values of the individual peripheral modules and registers at the time SPI boot mode finishes.

Also, Table 3.6 describes the setting values of Arm general-purpose registers at the time the boot processing finishes, and Table 3.7 describes the status of the Arm CP15 registers at the time the boot finishes.

Table 3.5 Setting Values of the Individual Peripheral Modules and Registers at the Time SPI Boot Mode Finishes

		Setting Value at the Time the Boot Processing Finishes	
Peripheral Module	**Register**	**When SPIBSC is initialized (SPIBSC_FLG = 2236 0679h)**	**When SPIBSC is not initialized (SPIBSC_FLG ≠ 2236 0679h)**
Low power consumption	MSTPCRC	0000 7DFEh (Initial value)	0000 7DFEh
SPIBSC	SSLDR	0007 0707h (Initial value)	Setting value of SSLDR_V
	SPBCR	0000 0003h (Initial value)	Setting value of SPBCR_V
	DRCR	0000 0000h (Initial value)	Setting value of DRCR_V
I/O ports	PORT6 .PMR	1Dh*1	1Dh*1
	MPC.PmnPFS	1Bh*1	1Bh*1

Note 1. Bits corresponding to the SPBCLK, SPBSSL, SPBMI, and SPBMO pins

Table 3.6 Setting Values of the Arm General-Purpose Registers at the Time the Boot Processing Finishes

No.	Register Name	Setting Values for Individual Processor Modes					
		User Mode/Current Mode	IRQ	FIQ	Undef	Abort	SVC
1	R0	Undefined	—	—	—	—	—
2	R1	Undefined	—	—	—	—	—
3	R2	Undefined	—	—	—	—	—
4	R3	Undefined	—	—	—	—	—
5	R4	Undefined	—	—	—	—	—
6	R5	Undefined	—	—	—	—	—
7	R6	Undefined	—	—	—	—	—
8	R7	Undefined	—	—	—	—	—
9	R8	Undefined	—	Undefined	—	—	—
10	R9	Undefined	—	Undefined	—	—	—
11	R10	Undefined	—	Undefined	—	—	—
12	R11	Undefined	—	Undefined	—	—	—
13	R12	Undefined	—	Undefined	—	—	—
14	R13(sp)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
15	R14(lr)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
16	R15(pc)	Arbitrary	—	—	—	—	—
17	cpsr	xxxx xx93h ([31:8] is undefined.) [7]I = 1 [6]F = 0*1 [5]T = 0 [4:0]MD = 10011b(SVC)	—	—	—	—	—
18	spsr	—	Undefined	Undefined	Undefined	Undefined	Undefined

—: Non-existent register

sp: Stack pointer

lr: Link register (which stores the return address when calling a subroutine call)

pc: Program counter

cpsr: Abbreviation of “current program status register”. It monitors or controls internal operations.

spsr: Abbreviation of “saved program status register”. It saves cpsr in the previous mode.

Note 1. In this product, the non-maskable interrupt has been assigned to FIQ. The boot processing changes the [6]F bit of the CPSR register from 1 to 0 to enable non-maskable interrupt after the boot processing finishes.

Note: After the boot processing sets the [6]F bit in the CPSR register to 0, if a non-maskable interrupt (FIQ exception) occurs before the processing reaches the branch to the loader program, the processing is jumped to the FIQ exception handler address and goes into an infinite loop. For details, see section 3.5.8, Note.

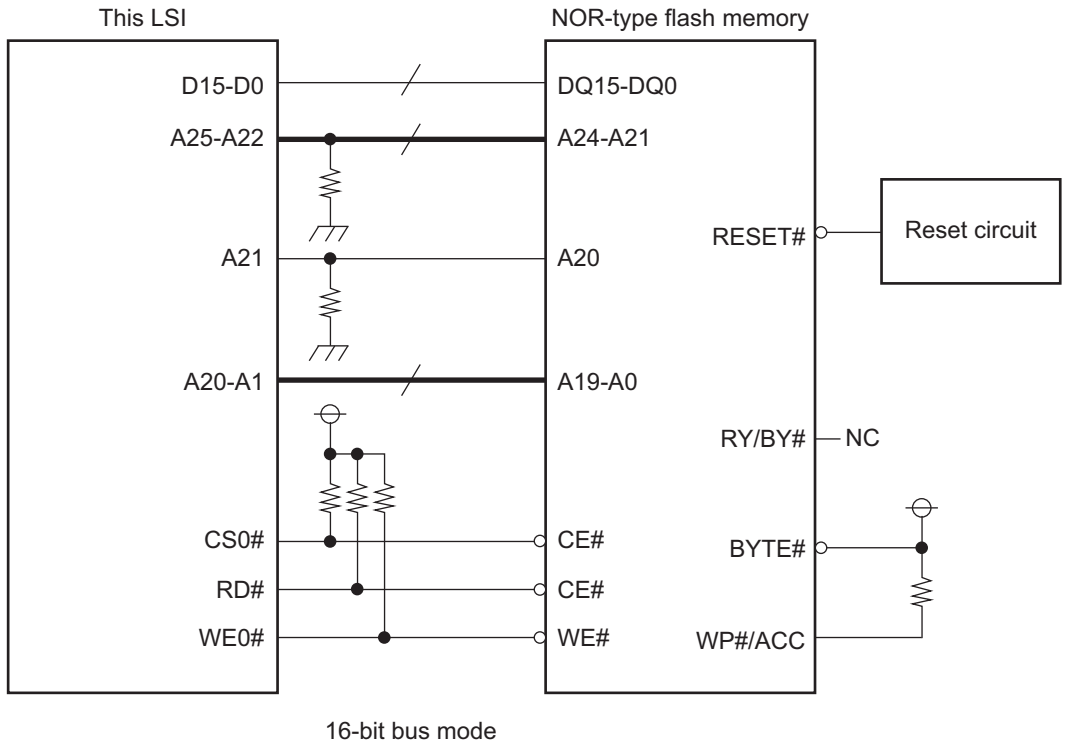
Table 3.7 Status of the Arm CP15 Registers at the Time the Boot Finishes

Register Name	Symbol	Setting Value at the Time the Boot Processing Finishes	Remarks
System control register	SCTLR	09E5 2878h*1	[24]VE = 1: Sets the IRQ exception vector address in VIC.
System control auxiliary register	ACTLR	0E00 0020h (When ATCM and BTCM are used)	ECC enable for TCM All areas of ATCM and BTCM are written and processed in 32-bit units during boot processing and initialized.
Invalidate all Instruction Caches Register	—	—	The I1 cache entry is not invalidated after the boot processing finishes.
Invalidate all Data Caches Register	—	—	The D1 cache entry is not invalidated after the boot processing finishes.
MPU Memory Region Number Register	RGNR	0000 0000h	All MPU settings are initialized even when the cache is enabled by the parameters for the loader.
Data Region Base Address Register	DRBAR	0000 0000h	
Data Region Size and Enable Register	DRSR	0000 0000h	
Data Region Access Control Register	DRACR	0000 0000h	

Note 1. When the boot processing finishes, the register is in high vector status, where V[13] = 1 (FFFF 0000h). Use the loader program to write appropriate processing in the low vectors (0000 0000h), and then to change the register to low vector status, where V[13] = 0 (0000 0000h).

3.5.5 16-Bit and 32-Bit Bus Boot Modes (NOR Flash Memory)

In 16-bit and 32-bit bus boot modes, this LSI boots a program from an external NOR flash memory connected to the external address space (CS0). The bus width is fixed to 16 bits or 32 bits, respectively.
In 16-bit bus boot mode, the A20 to A1, D15 to D0, CS0#, and RD# pins of the bus state controller are enabled.
In 32-bit bus boot mode, the A20 to A2, D31 to D0, CS0#, and RD# pins of the bus state controller are enabled.
After the reset is released, this LSI executes the boot processing. The loader program stored in a NOR flash memory connected to the CS0 space is extracted to the internal memory (TCM), and then the processing is executed.
Figure 3.4 shows the connection diagram of this LSI with a NOR flash memory.



Note: The 32-bit-bus boot mode requires the connection of two flash memory chips. In this case, D31 to D16 should be connected to the second flash memory chip and A2 should be connected to A0.

Figure 3.4 Connection Diagram of This LSI with a NOR Flash Memory

3.5.5.1 Operation Settings in 16-Bit and 32-Bit Bus Boot Modes

After the reset is released, if the boot processing starts in 16-bit or 32-bit bus boot mode, the following setting values are used:

- CPU clock (CPUCLK): 150 MHz
- External bus clock (CKIO): 50 MHz

After the parameters for the loader are loaded, the settings for the I1 and D1 caches of Cortex-R4 and for the CS0BCR and CS0WCR registers are performed based on the values of parameters CACHE_FLG, CS0BCR_V, and CS0WCR_V, so that the processing can be speed up.

Table 3.8 describes the setting values of the individual peripheral modules and registers at the time 16-bit or 32-bit bus boot mode finishes.

The setting values of Arm general-purpose registers and the status of the CP15 registers at the time the boot processing finishes are the same as those in SPI bus boot mode. For details, see Table 3.6 and Table 3.7.

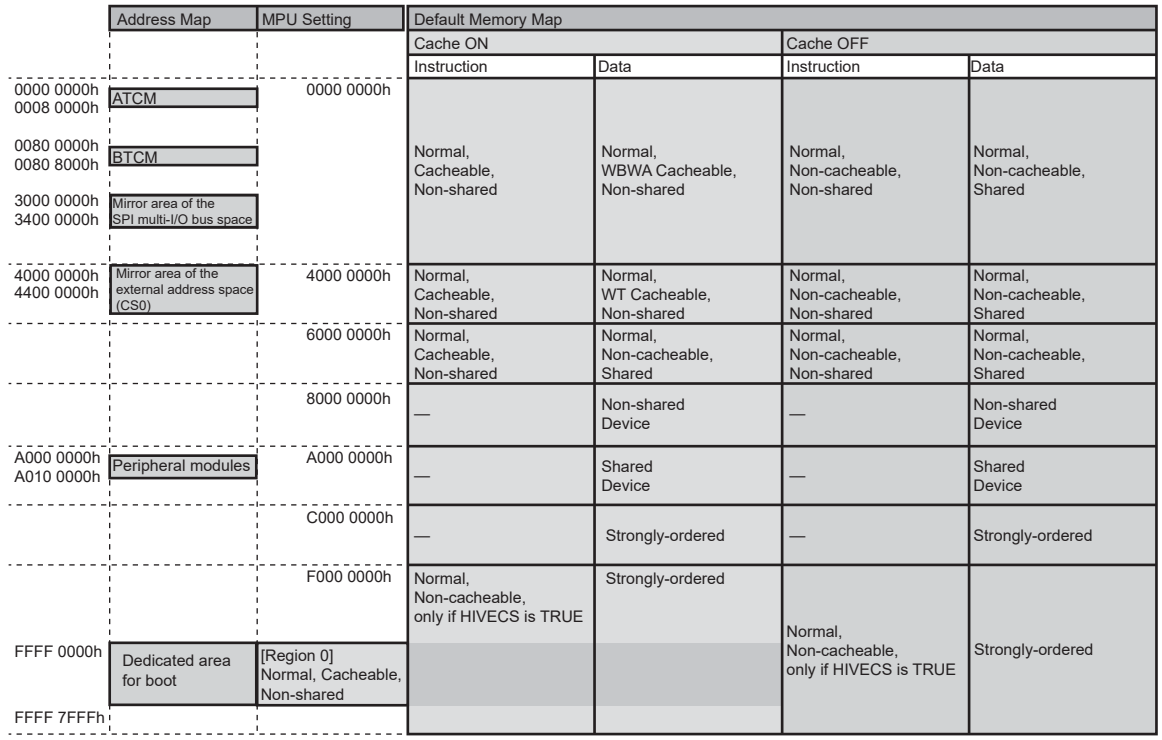
Table 3.8 Setting Values of the Individual Peripheral Modules and Registers at the Time 16-bit or 32-bit Bus Boot Mode Finishes

		Setting Value at the Time the Boot Processing Finishes	
Peripheral Module	**Register**	**When BSC is initialized (BSC_FLG = 2236 0679h)**	**When BSC is not initialized (BSC_FLG ≠ 2236 0679h)**
Low power consumption	MSTPCRC	0000 7F7Eh	0000 7F7Eh (Initial value)
BSC	CS0BCR	36DB 0C00h (Initial value)	Setting value of CS0BCR_V
	CS0WCR	0000 0500h (Initial value)	Setting value of CS0WCR_V
I/O ports	PORTn.PMR	Only the corresponding bits are 1.*1	Only the corresponding bits are 1.*1
	MPC.PmnPFS	22h*1	22h*1

Note 1. The bits corresponding to A1 to A20 pins, D0 to D15 pins, RD# pin, and CS0# pin in 16-bit bus boot mode.
The bits corresponding to A2 to A20 pins, D0 to D31 pins, RD# pin, and CS0# pin in 32-bit bus boot mode.

3.5.6 MPU Setting

The boot function uses the primary instruction cache (I1) and primary data cache (D1) of Cortex-R4 when the parameter CACHE_FLG for the loader is set to 0000 0001h.
However, the dedicated area for boot processing (FFFF 0000h to FFFF 7FFFh), which is used by the boot function, is set as the non-cache area in the default map of Cortex-R4, so the MPU (memory protection unit) redefines the cache area during the boot processing.
The boot function defines the high-vector area (FFFF 0000h to FFFF 7FFFh) as the cache area of Region 0, and uses other areas for the default memory map.
When the boot processing finishes, the I1 and D1 caches are invalidated, and all areas are initialized to the default memory map.
Figure 3.5 shows the relationship between the memory map definition during the boot processing and the default memory map of Cortex-R4.



Note 1. Because SCTLR[17] BR is set to 1, the default memory map is applied to the areas for which no region is set.

Figure 3.5 Relationship Between the Memory Map Definition During the Boot Processing and the Default Memory Map of Cortex-R4

3.5.7 Boot-Related Information and Error Processing

The boot function determines whether the boot processing finishes normally, and retains the result in a specific address. If the processing is determined to be an error, the boot processing is aborted, and an infinite loop is executed.
If the debugger is connected, reading the result of the boot processing that was stored in a specific address at the point of break can determine the error source.
Table 3.9 describes the error sources and the results of the boot processing.

Table 3.9 Error Sources and Results of Boot Processing

Storage Address*1	Stored Value*1	Error Sources and Results of Boot Processing
0080 09C4h	0	The boot processing finished normally.
	-1	A mode error occurred. When the setting is prohibited in the read value of the mode monitor register (MDMONR)
	-2	Checksum error of the parameters for the loader When the checksum (CHECK_SUM) of the parameters for the loader does not match
	-3	Error in a parameter for the loader When one of the following is satisfied: - The size of the loader program is smaller than 512 bytes. - The size of the loader program is larger than 24 Kbytes. - The size of the loader program is not a multiple of 512 bytes. - The destination address of the loader program is outside of the TCM area.

Note 1. The access size is 32 bits.

3.5.8 Note

3.5.8.1 Exception Processing

Only the reset exception due to the RES#-pin reset can be accepted during the boot processing. When a reset exception occurs, this LSI is reset, and the boot processing restarts. If an exception processing other than reset exception occurs, the jump instruction to the relevant exception handler address repeats an infinite loop.

Table 3.10 Exception Processing During the Boot Processing

Exception	Handler Address	Operation During the Boot Processing
Reset exception	FFFF 0000h	Branched to the reset exception handler
Undefined instruction exception	FFFF 0004h	Branched to the undefined instruction exception handler (Infinite loop)
Software interrupt exception	FFFF 0008h	Branched to the software interrupt exception handler (Infinite loop)
Prefetch abort exception	FFFF 000Ch	Branched to the prefetch abort exception handler (Infinite loop)
Data abort exception	FFFF 0010h	Branched to the data abort exception handler (Infinite loop)
IRQ exception	FFFF 0018h	Branched to the IRQ exception handler (Infinite loop)
FIQ exception	FFFF 001Ch	Branched to the FIQ exception handler (Infinite loop)

Note: Before the boot processing finishes, the register is in high vector status, where SCTLR V[13] = 1 (FFFF 0000h). Use the loader program to write appropriate processing in the low vectors (0000 0000h), and then to change the register to low vector status, where V[13] = 0 (0000 0000h).

3.5.8.2 Serial Flash Memory in SPI Boot Mode

In SPI boot mode, after release from the reset state, boot processing starts by reading from the serial flash memory via the SPI multi-I/O bus controller (SPIBSC) with the initial settings given in section 3.5.4.1, Operation Settings in SPI Boot Mode.

The setting of serial flash memory can be changed via the SPIBSC after the processing to boot up is finished. Depending on the settings, however, reading from the serial flash memory may not be possible when boot processing needs to be started again following a reset. Therefore, caution is required on this point.

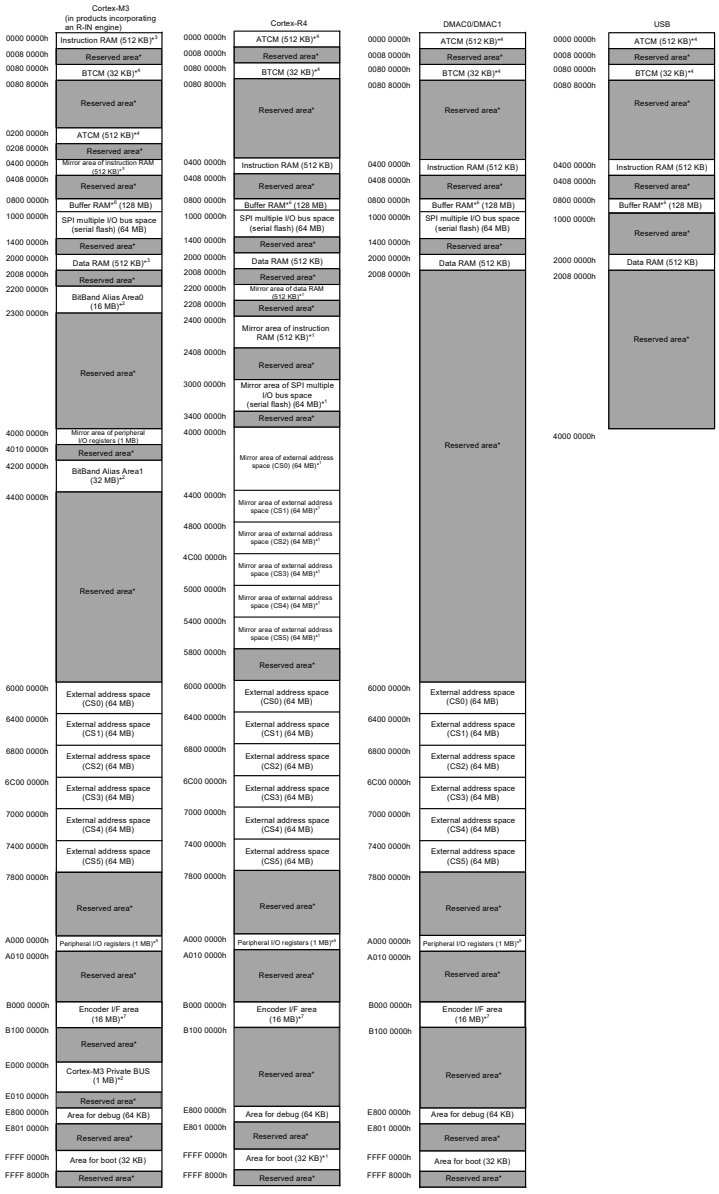
When the active level of the signal on the RES# pin is applied to reset this LSI chip, the serial flash memory can be simultaneously initialized by input of the same reset signal to the reset pin of the serial flash memory. Therefore, we recommend using serial flash memory that includes a reset pin. As the reset signal of a serial flash memory in a small package may be multiplexed with another pin function, make sure that the reset function is selected.

In addition, when an internal reset such as a software reset or ECM reset is to be generated, initialize the serial flash memory by software in advance so that it can be connected in boot processing.

4. Address Space

4.1 Address Space

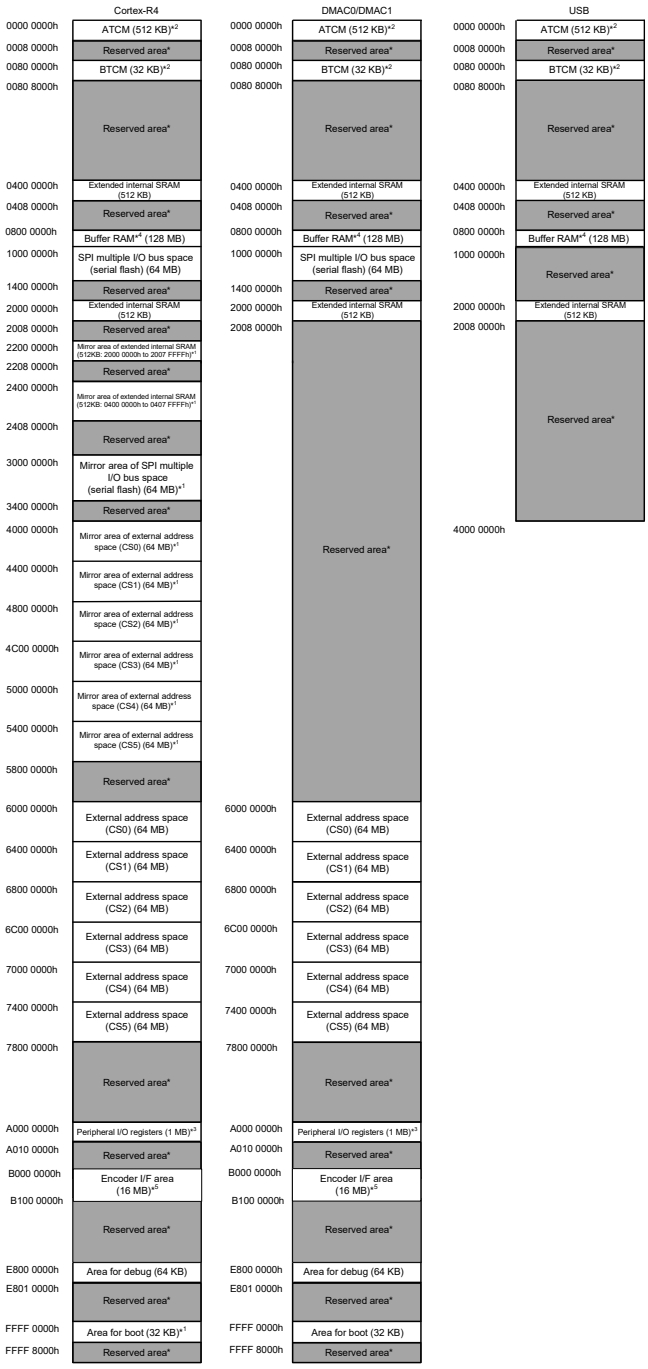
This LSI has a 4-Gbyte address space ranging from 0000 0000h to FFFF FFFFh. That is, up to total 4 Gbytes of program and data areas can be accessed linearly.
Figure 4.1, Figure 4.2 and Figure 4.3 show the memory maps for respective products.
Accessible areas will differ depending on the operating mode and the states of control bits.
In addition, since a non-cached access area from each bus master is assigned to the same area in this product, in access from the Cortex-R4, a mirror area is set as a cache-enabled area. The MPU should not enable caching of areas other than the mirror area.



Note 1. Can be cached.
(For other areas, caching should not be enabled by the MPU.)
Note 2. Accessible only from Cortex-M3. Bitband alias areas 0 and 1 are the data RAM and the peripheral I/O registers area, respectively.
Note 3. Cortex-M3 SRAM space (Extra-RAM)
Note 4. Cortex-R4 tightly coupled memory space
Note 5. Peripheral space
Note 6. For details, see section 28.3.1.3, Buffer Allocator.
Note 7. Peripheral space. Only for products with the encoder IF (optional).

Note: Reserved areas should not be accessed.

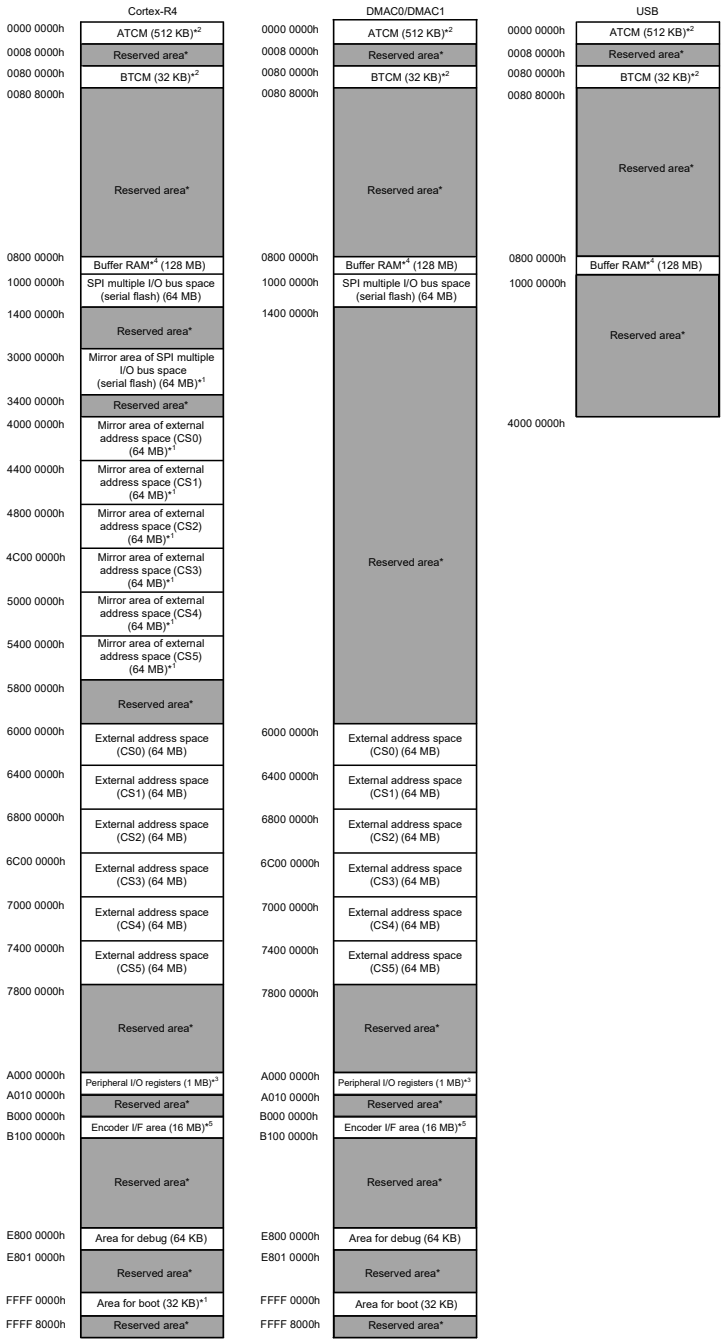
Figure 4.1 Memory Map



Note 1. Can be cached.
(For other areas, caching should not be enabled by the MPU.)
Note 2. Cortex-R4 tightly coupled memory space
Note 3. Peripheral space
Note 4. For details, see section 28.3.1.3, Buffer Allocator.
Note 5. Peripheral space. Only for products with the encoder IF (optional).

Note: Reserved areas should not be accessed.

Figure 4.2 Memory Map (1-Mbyte Extended Internal SRAM)



Note 1. Can be cached.
(For other areas, caching should not be enabled by the MPU.)
Note 2. Cortex-R4 tightly coupled memory space
Note 3. Peripheral space
Note 4. For details, see section 28.3.1.3, Buffer Allocator.
Note 5. Peripheral space. Only for products with the encoder I/F (optional).

Note: Reserved areas should not be accessed.

Figure 4.3 Memory Map (0-Kbyte Extended Internal SRAM)

5. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

5.1 I/O Register Addresses (Address Order)

Table 5.1 List of I/O Registers (Address Order) (1 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0000h	PORT0	Port direction register	PDR	16	16
A000 0002h	PORT1	Port direction register	PDR	16	16
A000 0004h	PORT2	Port direction register	PDR	16	16
A000 0006h	PORT3	Port direction register	PDR	16	16
A000 0008h	PORT4	Port direction register	PDR	16	16
A000 000Ah	PORT5	Port direction register	PDR	16	16
A000 000Ch	PORT6	Port direction register	PDR	16	16
A000 000Eh	PORT7	Port direction register	PDR	16	16
A000 0010h	PORT8	Port direction register	PDR	16	16
A000 0012h	PORT9	Port direction register	PDR	16	16
A000 0014h	PORTA	Port direction register	PDR	16	16
A000 0016h	PORTB	Port direction register	PDR	16	16
A000 0018h	PORTC	Port direction register	PDR	16	16
A000 001Ah	PORTD	Port direction register	PDR	16	16
A000 001Ch	PORTE	Port direction register	PDR	16	16
A000 001Eh	PORTF	Port direction register	PDR	16	16
A000 0020h	PORTG	Port direction register	PDR	16	16
A000 0022h	PORTH	Port direction register	PDR	16	16
A000 0024h	PORTJ	Port direction register	PDR	16	16
A000 0026h	PORTK	Port direction register	PDR	16	16
A000 0028h	PORTL	Port direction register	PDR	16	16
A000 002Ah	PORTM	Port direction register	PDR	16	16
A000 002Ch	PORTN	Port direction register	PDR	16	16
A000 002Eh	PORTP	Port direction register	PDR	16	16
A000 0030h	PORTR	Port direction register	PDR	16	16
A000 0032h	PORTS	Port direction register	PDR	16	16
A000 0034h	PORTT	Port direction register	PDR	16	16
A000 0036h	PORTU	Port direction register	PDR	16	16
A000 0040h	PORT0	Port output data register	PODR	8	8
A000 0041h	PORT1	Port output data register	PODR	8	8
A000 0042h	PORT2	Port output data register	PODR	8	8
A000 0043h	PORT3	Port output data register	PODR	8	8
A000 0044h	PORT4	Port output data register	PODR	8	8
A000 0045h	PORT5	Port output data register	PODR	8	8
A000 0046h	PORT6	Port output data register	PODR	8	8
A000 0047h	PORT7	Port output data register	PODR	8	8
A000 0048h	PORT8	Port output data register	PODR	8	8
A000 0049h	PORT9	Port output data register	PODR	8	8
A000 004Ah	PORTA	Port output data register	PODR	8	8
A000 004Bh	PORTB	Port output data register	PODR	8	8
A000 004Ch	PORTC	Port output data register	PODR	8	8
A000 004Dh	PORTD	Port output data register	PODR	8	8
A000 004Eh	PORTE	Port output data register	PODR	8	8
A000 004Fh	PORTF	Port output data register	PODR	8	8
A000 0050h	PORTG	Port output data register	PODR	8	8
A000 0051h	PORTH	Port output data register	PODR	8	8

Table 5.1 List of I/O Registers (Address Order) (2 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0052h	PORTJ	Port output data register	PODR	8	8
A000 0053h	PORTK	Port output data register	PODR	8	8
A000 0054h	PORTL	Port output data register	PODR	8	8
A000 0055h	PORTM	Port output data register	PODR	8	8
A000 0056h	PORTN	Port output data register	PODR	8	8
A000 0057h	PORTP	Port output data register	PODR	8	8
A000 0058h	PORTR	Port output data register	PODR	8	8
A000 0059h	PORTS	Port output data register	PODR	8	8
A000 005Ah	PORTT	Port output data register	PODR	8	8
A000 005Bh	PORTU	Port output data register	PODR	8	8
A000 0060h	PORT0	Port input data register	PIDR	8	8
A000 0061h	PORT1	Port input data register	PIDR	8	8
A000 0062h	PORT2	Port input data register	PIDR	8	8
A000 0063h	PORT3	Port input data register	PIDR	8	8
A000 0064h	PORT4	Port input data register	PIDR	8	8
A000 0065h	PORT5	Port input data register	PIDR	8	8
A000 0066h	PORT6	Port input data register	PIDR	8	8
A000 0067h	PORT7	Port input data register	PIDR	8	8
A000 0068h	PORT8	Port input data register	PIDR	8	8
A000 0069h	PORT9	Port input data register	PIDR	8	8
A000 006Ah	PORTA	Port input data register	PIDR	8	8
A000 006Bh	PORTB	Port input data register	PIDR	8	8
A000 006Ch	PORTC	Port input data register	PIDR	8	8
A000 006Dh	PORTD	Port input data register	PIDR	8	8
A000 006Eh	PORTE	Port input data register	PIDR	8	8
A000 006Fh	PORTF	Port input data register	PIDR	8	8
A000 0070h	PORTG	Port input data register	PIDR	8	8
A000 0071h	PORTH	Port input data register	PIDR	8	8
A000 0072h	PORTJ	Port input data register	PIDR	8	8
A000 0073h	PORTK	Port input data register	PIDR	8	8
A000 0074h	PORTL	Port input data register	PIDR	8	8
A000 0075h	PORTM	Port input data register	PIDR	8	8
A000 0076h	PORTN	Port input data register	PIDR	8	8
A000 0077h	PORTP	Port input data register	PIDR	8	8
A000 0078h	PORTR	Port input data register	PIDR	8	8
A000 0079h	PORTS	Port input data register	PIDR	8	8
A000 007Ah	PORTT	Port input data register	PIDR	8	8
A000 007Bh	PORTU	Port input data register	PIDR	8	8
A000 0080h	PORT0	Port mode register	PMR	8	8
A000 0081h	PORT1	Port mode register	PMR	8	8
A000 0082h	PORT2	Port mode register	PMR	8	8
A000 0083h	PORT3	Port mode register	PMR	8	8
A000 0084h	PORT4	Port mode register	PMR	8	8
A000 0085h	PORT5	Port mode register	PMR	8	8
A000 0086h	PORT6	Port mode register	PMR	8	8
A000 0087h	PORT7	Port mode register	PMR	8	8
A000 0088h	PORT8	Port mode register	PMR	8	8
A000 0089h	PORT9	Port mode register	PMR	8	8

Table 5.1 List of I/O Registers (Address Order) (3 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 008Ah	PORTA	Port mode register	PMR	8	8
A000 008Bh	PORTB	Port mode register	PMR	8	8
A000 008Ch	PORTC	Port mode register	PMR	8	8
A000 008Dh	PORTD	Port mode register	PMR	8	8
A000 008Eh	PORTE	Port mode register	PMR	8	8
A000 008Fh	PORTF	Port mode register	PMR	8	8
A000 0090h	PORTG	Port mode register	PMR	8	8
A000 0091h	PORTH	Port mode register	PMR	8	8
A000 0092h	PORTJ	Port mode register	PMR	8	8
A000 0093h	PORTK	Port mode register	PMR	8	8
A000 0094h	PORTL	Port mode register	PMR	8	8
A000 0095h	PORTM	Port mode register	PMR	8	8
A000 0096h	PORTN	Port mode register	PMR	8	8
A000 0097h	PORTP	Port mode register	PMR	8	8
A000 0098h	PORTR	Port mode register	PMR	8	8
A000 0099h	PORTS	Port mode register	PMR	8	8
A000 009Ah	PORTT	Port mode register	PMR	8	8
A000 009Bh	PORTU	Port mode register	PMR	8	8
A000 0100h	PORT0	Pull-up/pull-down control register	PCR	16	16
A000 0102h	PORT1	Pull-up/pull-down control register	PCR	16	16
A000 0104h	PORT2	Pull-up/pull-down control register	PCR	16	16
A000 0106h	PORT3	Pull-up/pull-down control register	PCR	16	16
A000 0108h	PORT4	Pull-up/pull-down control register	PCR	16	16
A000 010Ah	PORT5	Pull-up/pull-down control register	PCR	16	16
A000 010Ch	PORT6	Pull-up/pull-down control register	PCR	16	16
A000 010Eh	PORT7	Pull-up/pull-down control register	PCR	16	16
A000 0110h	PORT8	Pull-up/pull-down control register	PCR	16	16
A000 0112h	PORT9	Pull-up/pull-down control register	PCR	16	16
A000 0114h	PORTA	Pull-up/pull-down control register	PCR	16	16
A000 0116h	PORTB	Pull-up/pull-down control register	PCR	16	16
A000 011Ah	PORTD	Pull-up/pull-down control register	PCR	16	16
A000 011Ch	PORTE	Pull-up/pull-down control register	PCR	16	16
A000 011Eh	PORTF	Pull-up/pull-down control register	PCR	16	16
A000 0120h	PORTG	Pull-up/pull-down control register	PCR	16	16
A000 0122h	PORTH	Pull-up/pull-down control register	PCR	16	16
A000 0124h	PORTJ	Pull-up/pull-down control register	PCR	16	16
A000 0126h	PORTK	Pull-up/pull-down control register	PCR	16	16
A000 0128h	PORTL	Pull-up/pull-down control register	PCR	16	16
A000 012Ah	PORTM	Pull-up/pull-down control register	PCR	16	16
A000 012Ch	PORTN	Pull-up/pull-down control register	PCR	16	16
A000 012Eh	PORTP	Pull-up/pull-down control register	PCR	16	16
A000 0130h	PORTR	Pull-up/pull-down control register	PCR	16	16
A000 0132h	PORTS	Pull-up/pull-down control register	PCR	16	16
A000 0134h	PORTT	Pull-up/pull-down control register	PCR	16	16
A000 0136h	PORTU	Pull-up/pull-down control register	PCR	16	16
A000 0142h	PORT1	Drive strength control register	DSCR	16	16
A000 0200h	MPC	Port 00 pin function control register	P00PFS	8	8
A000 0201h	MPC	Port 01 pin function control register	P01PFS	8	8

Table 5.1 List of I/O Registers (Address Order) (4 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0202h	MPC	Port 02 pin function control register	P02PFS	8	8
A000 0203h	MPC	Port 03 pin function control register	P03PFS	8	8
A000 0204h	MPC	Port 04 pin function control register	P04PFS	8	8
A000 0205h	MPC	Port 05 pin function control register	P05PFS	8	8
A000 0206h	MPC	Port 06 pin function control register	P06PFS	8	8
A000 0207h	MPC	Port 07 pin function control register	P07PFS	8	8
A000 0208h	MPC	Port 10 pin function control register	P10PFS	8	8
A000 0209h	MPC	Port 11 pin function control register	P11PFS	8	8
A000 020Ah	MPC	Port 12 pin function control register	P12PFS	8	8
A000 020Bh	MPC	Port 13 pin function control register	P13PFS	8	8
A000 020Ch	MPC	Port 14 pin function control register	P14PFS	8	8
A000 020Dh	MPC	Port 15 pin function control register	P15PFS	8	8
A000 020Eh	MPC	Port 16 pin function control register	P16PFS	8	8
A000 020Fh	MPC	Port 17 pin function control register	P17PFS	8	8
A000 0210h	MPC	Port 20 pin function control register	P20PFS	8	8
A000 0211h	MPC	Port 21 pin function control register	P21PFS	8	8
A000 0212h	MPC	Port 22 pin function control register	P22PFS	8	8
A000 0213h	MPC	Port 23 pin function control register	P23PFS	8	8
A000 0214h	MPC	Port 24 pin function control register	P24PFS	8	8
A000 0215h	MPC	Port 25 pin function control register	P25PFS	8	8
A000 0216h	MPC	Port 26 pin function control register	P26PFS	8	8
A000 0217h	MPC	Port 27 pin function control register	P27PFS	8	8
A000 0218h	MPC	Port 30 pin function control register	P30PFS	8	8
A000 0219h	MPC	Port 31 pin function control register	P31PFS	8	8
A000 021Ah	MPC	Port 32 pin function control register	P32PFS	8	8
A000 021Bh	MPC	Port 33 pin function control register	P33PFS	8	8
A000 021Ch	MPC	Port 34 pin function control register	P34PFS	8	8
A000 021Dh	MPC	Port 35 pin function control register	P35PFS	8	8
A000 021Eh	MPC	Port 36 pin function control register	P36PFS	8	8
A000 021Fh	MPC	Port 37 pin function control register	P37PFS	8	8
A000 0220h	MPC	Port 40 pin function control register	P40PFS	8	8
A000 0221h	MPC	Port 41 pin function control register	P41PFS	8	8
A000 0222h	MPC	Port 42 pin function control register	P42PFS	8	8
A000 0223h	MPC	Port 43 pin function control register	P43PFS	8	8
A000 0224h	MPC	Port 44 pin function control register	P44PFS	8	8
A000 0225h	MPC	Port 45 pin function control register	P45PFS	8	8
A000 0226h	MPC	Port 46 pin function control register	P46PFS	8	8
A000 0227h	MPC	Port 47 pin function control register	P47PFS	8	8
A000 0228h	MPC	Port 50 pin function control register	P50PFS	8	8
A000 0229h	MPC	Port 51 pin function control register	P51PFS	8	8
A000 022Ah	MPC	Port 52 pin function control register	P52PFS	8	8
A000 022Bh	MPC	Port 53 pin function control register	P53PFS	8	8
A000 022Ch	MPC	Port 54 pin function control register	P54PFS	8	8
A000 022Dh	MPC	Port 55 pin function control register	P55PFS	8	8
A000 022Eh	MPC	Port 56 pin function control register	P56PFS	8	8
A000 0230h	MPC	Port 60 pin function control register	P60PFS	8	8
A000 0231h	MPC	Port 61 pin function control register	P61PFS	8	8
A000 0232h	MPC	Port 62 pin function control register	P62PFS	8	8

Table 5.1 List of I/O Registers (Address Order) (5 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0233h	MPC	Port 63 pin function control register	P63PFS	8	8
A000 0234h	MPC	Port 64 pin function control register	P64PFS	8	8
A000 0235h	MPC	Port 65 pin function control register	P65PFS	8	8
A000 0236h	MPC	Port 66 pin function control register	P66PFS	8	8
A000 0237h	MPC	Port 67 pin function control register	P67PFS	8	8
A000 0238h	MPC	Port 70 pin function control register	P70PFS	8	8
A000 0239h	MPC	Port 71 pin function control register	P71PFS	8	8
A000 023Ah	MPC	Port 72 pin function control register	P72PFS	8	8
A000 023Bh	MPC	Port 73 pin function control register	P73PFS	8	8
A000 023Ch	MPC	Port 74 pin function control register	P74PFS	8	8
A000 023Dh	MPC	Port 75 pin function control register	P75PFS	8	8
A000 023Eh	MPC	Port 76 pin function control register	P76PFS	8	8
A000 023Fh	MPC	Port 77 pin function control register	P77PFS	8	8
A000 0240h	MPC	Port 80 pin function control register	P80PFS	8	8
A000 0241h	MPC	Port 81 pin function control register	P81PFS	8	8
A000 0242h	MPC	Port 82 pin function control register	P82PFS	8	8
A000 0243h	MPC	Port 83 pin function control register	P83PFS	8	8
A000 0244h	MPC	Port 84 pin function control register	P84PFS	8	8
A000 0245h	MPC	Port 85 pin function control register	P85PFS	8	8
A000 0246h	MPC	Port 86 pin function control register	P86PFS	8	8
A000 0247h	MPC	Port 87 pin function control register	P87PFS	8	8
A000 0248h	MPC	Port 90 pin function control register	P90PFS	8	8
A000 0249h	MPC	Port 91 pin function control register	P91PFS	8	8
A000 024Ah	MPC	Port 92 pin function control register	P92PFS	8	8
A000 024Bh	MPC	Port 93 pin function control register	P93PFS	8	8
A000 024Ch	MPC	Port 94 pin function control register	P94PFS	8	8
A000 024Dh	MPC	Port 95 pin function control register	P95PFS	8	8
A000 024Eh	MPC	Port 96 pin function control register	P96PFS	8	8
A000 024Fh	MPC	Port 97 pin function control register	P97PFS	8	8
A000 0250h	MPC	Port A0 pin function control register	PA0PFS	8	8
A000 0251h	MPC	Port A1 pin function control register	PA1PFS	8	8
A000 0252h	MPC	Port A2 pin function control register	PA2PFS	8	8
A000 0253h	MPC	Port A3 pin function control register	PA3PFS	8	8
A000 0254h	MPC	Port A4 pin function control register	PA4PFS	8	8
A000 0255h	MPC	Port A5 pin function control register	PA5PFS	8	8
A000 0256h	MPC	Port A6 pin function control register	PA6PFS	8	8
A000 0257h	MPC	Port A7 pin function control register	PA7PFS	8	8
A000 0258h	MPC	Port B0 pin function control register	PB0PFS	8	8
A000 0259h	MPC	Port B1 pin function control register	PB1PFS	8	8
A000 025Ah	MPC	Port B2 pin function control register	PB2PFS	8	8
A000 025Bh	MPC	Port B3 pin function control register	PB3PFS	8	8
A000 025Ch	MPC	Port B4 pin function control register	PB4PFS	8	8
A000 025Dh	MPC	Port B5 pin function control register	PB5PFS	8	8
A000 025Eh	MPC	Port B6 pin function control register	PB6PFS	8	8
A000 025Fh	MPC	Port B7 pin function control register	PB7PFS	8	8
A000 0260h	MPC	Port C0 pin function control register	PC0PFS	8	8
A000 0261h	MPC	Port C1 pin function control register	PC1PFS	8	8
A000 0262h	MPC	Port C2 pin function control register	PC2PFS	8	8

Table 5.1 List of I/O Registers (Address Order) (6 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0263h	MPC	Port C3 pin function control register	PC3PFS	8	8
A000 0264h	MPC	Port C4 pin function control register	PC4PFS	8	8
A000 0265h	MPC	Port C5 pin function control register	PC5PFS	8	8
A000 0266h	MPC	Port C6 pin function control register	PC6PFS	8	8
A000 0267h	MPC	Port C7 pin function control register	PC7PFS	8	8
A000 0268h	MPC	Port D0 pin function control register	PD0PFS	8	8
A000 0269h	MPC	Port D1 pin function control register	PD1PFS	8	8
A000 026Ah	MPC	Port D2 pin function control register	PD2PFS	8	8
A000 026Bh	MPC	Port D3 pin function control register	PD3PFS	8	8
A000 026Ch	MPC	Port D4 pin function control register	PD4PFS	8	8
A000 026Dh	MPC	Port D5 pin function control register	PD5PFS	8	8
A000 026Eh	MPC	Port D6 pin function control register	PD6PFS	8	8
A000 026Fh	MPC	Port D7 pin function control register	PD7PFS	8	8
A000 0270h	MPC	Port E0 pin function control register	PE0PFS	8	8
A000 0271h	MPC	Port E1 pin function control register	PE1PFS	8	8
A000 0272h	MPC	Port E2 pin function control register	PE2PFS	8	8
A000 0273h	MPC	Port E3 pin function control register	PE3PFS	8	8
A000 0274h	MPC	Port E4 pin function control register	PE4PFS	8	8
A000 0275h	MPC	Port E5 pin function control register	PE5PFS	8	8
A000 0276h	MPC	Port E6 pin function control register	PE6PFS	8	8
A000 0277h	MPC	Port E7 pin function control register	PE7PFS	8	8
A000 027Dh	MPC	Port F5 pin function control register	PF5PFS	8	8
A000 027Eh	MPC	Port F6 pin function control register	PF6PFS	8	8
A000 027Fh	MPC	Port F7 pin function control register	PF7PFS	8	8
A000 0280h	MPC	Port G0 pin function control register	PG0PFS	8	8
A000 0281h	MPC	Port G1 pin function control register	PG1PFS	8	8
A000 0282h	MPC	Port G2 pin function control register	PG2PFS	8	8
A000 0283h	MPC	Port G3 pin function control register	PG3PFS	8	8
A000 0284h	MPC	Port G4 pin function control register	PG4PFS	8	8
A000 0285h	MPC	Port G5 pin function control register	PG5PFS	8	8
A000 0286h	MPC	Port G6 pin function control register	PG6PFS	8	8
A000 0287h	MPC	Port G7 pin function control register	PG7PFS	8	8
A000 0288h	MPC	Port H0 pin function control register	PH0PFS	8	8
A000 0289h	MPC	Port H1 pin function control register	PH1PFS	8	8
A000 028Ah	MPC	Port H2 pin function control register	PH2PFS	8	8
A000 028Bh	MPC	Port H3 pin function control register	PH3PFS	8	8
A000 028Ch	MPC	Port H4 pin function control register	PH4PFS	8	8
A000 028Dh	MPC	Port H5 pin function control register	PH5PFS	8	8
A000 028Eh	MPC	Port H6 pin function control register	PH6PFS	8	8
A000 028Fh	MPC	Port H7 pin function control register	PH7PFS	8	8
A000 0290h	MPC	Port J0 pin function control register	PJ0PFS	8	8
A000 0291h	MPC	Port J1 pin function control register	PJ1PFS	8	8
A000 0292h	MPC	Port J2 pin function control register	PJ2PFS	8	8
A000 0293h	MPC	Port J3 pin function control register	PJ3PFS	8	8
A000 0294h	MPC	Port J4 pin function control register	PJ4PFS	8	8
A000 0295h	MPC	Port J5 pin function control register	PJ5PFS	8	8
A000 0296h	MPC	Port J6 pin function control register	PJ6PFS	8	8
A000 0297h	MPC	Port J7 pin function control register	PJ7PFS	8	8

Table 5.1 List of I/O Registers (Address Order) (7 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 0298h	MPC	Port K0 pin function control register	PK0PFS	8	8
A000 0299h	MPC	Port K1 pin function control register	PK1PFS	8	8
A000 029Ah	MPC	Port K2 pin function control register	PK2PFS	8	8
A000 029Bh	MPC	Port K3 pin function control register	PK3PFS	8	8
A000 029Ch	MPC	Port K4 pin function control register	PK4PFS	8	8
A000 029Dh	MPC	Port K5 pin function control register	PK5PFS	8	8
A000 029Eh	MPC	Port K6 pin function control register	PK6PFS	8	8
A000 029Fh	MPC	Port K7 pin function control register	PK7PFS	8	8
A000 02A0h	MPC	Port L0 pin function control register	PL0PFS	8	8
A000 02A1h	MPC	Port L1 pin function control register	PL1PFS	8	8
A000 02A2h	MPC	Port L2 pin function control register	PL2PFS	8	8
A000 02A3h	MPC	Port L3 pin function control register	PL3PFS	8	8
A000 02A4h	MPC	Port L4 pin function control register	PL4PFS	8	8
A000 02A5h	MPC	Port L5 pin function control register	PL5PFS	8	8
A000 02A6h	MPC	Port L6 pin function control register	PL6PFS	8	8
A000 02A7h	MPC	Port L7 pin function control register	PL7PFS	8	8
A000 02A8h	MPC	Port M0 pin function control register	PM0PFS	8	8
A000 02A9h	MPC	Port M1 pin function control register	PM1PFS	8	8
A000 02AAh	MPC	Port M2 pin function control register	PM2PFS	8	8
A000 02ABh	MPC	Port M3 pin function control register	PM3PFS	8	8
A000 02ACh	MPC	Port M4 pin function control register	PM4PFS	8	8
A000 02ADh	MPC	Port M5 pin function control register	PM5PFS	8	8
A000 02AEh	MPC	Port M6 pin function control register	PM6PFS	8	8
A000 02AFh	MPC	Port M7 pin function control register	PM7PFS	8	8
A000 02B0h	MPC	Port N0 pin function control register	PN0PFS	8	8
A000 02B1h	MPC	Port N1 pin function control register	PN1PFS	8	8
A000 02B2h	MPC	Port N2 pin function control register	PN2PFS	8	8
A000 02B3h	MPC	Port N3 pin function control register	PN3PFS	8	8
A000 02B4h	MPC	Port N4 pin function control register	PN4PFS	8	8
A000 02B5h	MPC	Port N5 pin function control register	PN5PFS	8	8
A000 02B6h	MPC	Port N6 pin function control register	PN6PFS	8	8
A000 02B7h	MPC	Port N7 pin function control register	PN7PFS	8	8
A000 02B8h	MPC	Port P0 pin function control register	PP0PFS	8	8
A000 02B9h	MPC	Port P1 pin function control register	PP1PFS	8	8
A000 02BAh	MPC	Port P2 pin function control register	PP2PFS	8	8
A000 02BBh	MPC	Port P3 pin function control register	PP3PFS	8	8
A000 02BCh	MPC	Port P4 pin function control register	PP4PFS	8	8
A000 02BDh	MPC	Port P5 pin function control register	PP5PFS	8	8
A000 02BEh	MPC	Port P6 pin function control register	PP6PFS	8	8
A000 02BFh	MPC	Port P7 pin function control register	PP7PFS	8	8
A000 02C0h	MPC	Port R0 pin function control register	PR0PFS	8	8
A000 02C1h	MPC	Port R1 pin function control register	PR1PFS	8	8
A000 02C2h	MPC	Port R2 pin function control register	PR2PFS	8	8
A000 02C3h	MPC	Port R3 pin function control register	PR3PFS	8	8
A000 02C4h	MPC	Port R4 pin function control register	PR4PFS	8	8
A000 02C5h	MPC	Port R5 pin function control register	PR5PFS	8	8
A000 02C6h	MPC	Port R6 pin function control register	PR6PFS	8	8
A000 02C7h	MPC	Port R7 pin function control register	PR7PFS	8	8

Table 5.1 List of I/O Registers (Address Order) (8 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 02C8h	MPC	Port S0 pin function control register	PS0PFS	8	8
A000 02C9h	MPC	Port S1 pin function control register	PS1PFS	8	8
A000 02CAh	MPC	Port S2 pin function control register	PS2PFS	8	8
A000 02CBh	MPC	Port S3 pin function control register	PS3PFS	8	8
A000 02CCh	MPC	Port S4 pin function control register	PS4PFS	8	8
A000 02CDh	MPC	Port S5 pin function control register	PS5PFS	8	8
A000 02CEh	MPC	Port S6 pin function control register	PS6PFS	8	8
A000 02CFh	MPC	Port S7 pin function control register	PS7PFS	8	8
A000 02D0h	MPC	Port T0 pin function control register	PT0PFS	8	8
A000 02D1h	MPC	Port T1 pin function control register	PT1PFS	8	8
A000 02D2h	MPC	Port T2 pin function control register	PT2PFS	8	8
A000 02D3h	MPC	Port T3 pin function control register	PT3PFS	8	8
A000 02D4h	MPC	Port T4 pin function control register	PT4PFS	8	8
A000 02D5h	MPC	Port T5 pin function control register	PT5PFS	8	8
A000 02D6h	MPC	Port T6 pin function control register	PT6PFS	8	8
A000 02D7h	MPC	Port T7 pin function control register	PT7PFS	8	8
A000 02D8h	MPC	Port U0 pin function control register	PU0PFS	8	8
A000 02D9h	MPC	Port U1 pin function control register	PU1PFS	8	8
A000 02DAh	MPC	Port U2 pin function control register	PU2PFS	8	8
A000 02DBh	MPC	Port U3 pin function control register	PU3PFS	8	8
A000 02DCh	MPC	Port U4 pin function control register	PU4PFS	8	8
A000 02DDh	MPC	Port U5 pin function control register	PU5PFS	8	8
A000 02DEh	MPC	Port U6 pin function control register	PU6PFS	8	8
A000 02DFh	MPC	Port U7 pin function control register	PU7PFS	8	8
A000 02FFh	MPC	Write protection register	PWPR	8	8
A000 2000h	DMAC	Common control register	CMNCR	32	32
A000 2004h	BSC	CS0 space bus control register	CS0BCR	32	32
A000 2008h	BSC	CS1 space bus control register	CS1BCR	32	32
A000 200Ch	BSC	CS2 space bus control register	CS2BCR	32	32
A000 2010h	BSC	CS3 space bus control register	CS3BCR	32	32
A000 2014h	BSC	CS4 space bus control register	CS4BCR	32	32
A000 2018h	BSC	CS5 space bus control register	CS5BCR	32	32
A000 2028h	BSC	CS0 space wait control register	CS0WCR_0, CS0WCR_1, CS0WCR_2	32	32
A000 202Ch	BSC	CS1 space wait control register	CS1WCR	32	32
A000 2030h	BSC	CS2 space wait control register	CS2WCR_0, CS2WCR_1	32	32
A000 2034h	BSC	CS3 space wait control register	CS3WCR_0, CS3WCR_1	32	32
A000 2038h	BSC	CS4 space wait control register	CS4WCR_0, CS4WCR_1	32	32
A000 203Ch	BSC	CS5 space wait control register	CS5WCR	32	32
A000 204Ch	BSC	SDRAM control register	SDCR	32	32
A000 2050h	BSC	Refresh timer control/status register	RTCSR	32	32
A000 2054h	BSC	Refresh timer counter	RTCNT	32	32
A000 2058h	BSC	Refresh time constant register	RTCOR	32	32
A000 2060h	BSC	Timeout cycle constant register 0	TOSCOR0	32	32
A000 2064h	BSC	Timeout cycle constant register 1	TOSCOR1	32	32
A000 2068h	BSC	Timeout cycle constant register 2	TOSCOR2	32	32

Table 5.1 List of I/O Registers (Address Order) (9 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A000 206Ch	BSC	Timeout cycle constant register 3	TOSCOR3	32	32
A000 2070h	BSC	Timeout cycle constant register 4	TOSCOR4	32	32
A000 2074h	BSC	Timeout cycle constant register 5	TOSCOR5	32	32
A000 2080h	BSC	Timeout status register	TOSTR	32	32
A000 2084h	BSC	Timeout enable register	TOENR	32	32
A000 2C0Ch	BSC	CKIO control register	CKIOSET	32	32
A000 2CFCh	BSC	CKIOSET protect register	CKIOKEY	8	8
A000 5000h	SPIBSC	Common control register	CMNCR	32	32
A000 5004h	SPIBSC	SSL delay register	SSLDR	32	32
A000 5008h	SPIBSC	Bit rate register	SPBCR	32	32
A000 500Ch	SPIBSC	Data read control register	DRCR	32	32
A000 5010h	SPIBSC	Data read command setting register	DRCMR	32	32
A000 5014h	SPIBSC	Data read extended address setting register	DREAR	32	32
A000 5018h	SPIBSC	Data read option setting register	DROPR	32	32
A000 501Ch	SPIBSC	Data read enable setting register	DRENR	32	32
A000 5020h	SPIBSC	SPI mode control register	SMCR	32	32
A000 5024h	SPIBSC	SPI mode command setting register	SMCMR	32	32
A000 5028h	SPIBSC	SPI mode address setting register	SMADR	32	32
A000 502Ch	SPIBSC	SPI mode option setting register	SMOPR	32	32
A000 5030h	SPIBSC	SPI mode enable setting register	SMENR	32	32
A000 5038h	SPIBSC	SPI mode read data register 0	SMRDR0	32	8, 16, 32
A000 5040h	SPIBSC	SPI mode write data register 0	SMWDR0	32	8, 16, 32
A000 5048h	SPIBSC	Common status register	CMNSR	32	32
A000 5058h	SPIBSC	Data read dummy cycle setting register	DRDMCR	32	32
A000 5060h	SPIBSC	SPI mode dummy cycle setting register	SMDMCR	32	32
A001 0000h	VIC	IRQ status register 0	IRQS0	32	32
A001 0004h	VIC	IRQ status register 1	IRQS1	32	32
A001 0008h	VIC	IRQ status register 2	IRQS2	32	32
A001 000Ch	VIC	IRQ status register 3	IRQS3	32	32
A001 0010h	VIC	IRQ status register 4	IRQS4	32	32
A001 0014h	VIC	IRQ status register 5	IRQS5	32	32
A001 0018h	VIC	IRQ status register 6	IRQS6	32	32
A001 001Ch	VIC	IRQ status register 7	IRQS7	32	32
A001 0040h	VIC	Interrupt input status register 0	RAIS0	32	32
A001 0044h	VIC	Interrupt input status register 1	RAIS1	32	32
A001 0048h	VIC	Interrupt input status register 2	RAIS2	32	32
A001 004Ch	VIC	Interrupt input status register 3	RAIS3	32	32
A001 0050h	VIC	Interrupt input status register 4	RAIS4	32	32
A001 0054h	VIC	Interrupt input status register 5	RAIS5	32	32
A001 0058h	VIC	Interrupt input status register 6	RAIS6	32	32
A001 005Ch	VIC	Interrupt input status register 7	RAIS7	32	32
A001 0080h	VIC	Interrupt enable register 0	IEN0	32	32
A001 0084h	VIC	Interrupt enable register 1	IEN1	32	32
A001 0088h	VIC	Interrupt enable register 2	IEN2	32	32
A001 008Ch	VIC	Interrupt enable register 3	IEN3	32	32
A001 0090h	VIC	Interrupt enable register 4	IEN4	32	32
A001 0094h	VIC	Interrupt enable register 5	IEN5	32	32
A001 0098h	VIC	Interrupt enable register 6	IEN6	32	32

Table 5.1 List of I/O Registers (Address Order) (10 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 009Ch	VIC	Interrupt enable register 7	IEN7	32	32
A001 00A0h	VIC	Interrupt enable clear register 0	IEC0	32	32
A001 00A4h	VIC	Interrupt enable clear register 1	IEC1	32	32
A001 00A8h	VIC	Interrupt enable clear register 2	IEC2	32	32
A001 00ACh	VIC	Interrupt enable clear register 3	IEC3	32	32
A001 00B0h	VIC	Interrupt enable clear register 4	IEC4	32	32
A001 00B4h	VIC	Interrupt enable clear register 5	IEC5	32	32
A001 00B8h	VIC	Interrupt enable clear register 6	IEC6	32	32
A001 00BCh	VIC	Interrupt enable clear register 7	IEC7	32	32
A001 0100h	VIC	Interrupt detection type selection register 0	PLS0	32	32
A001 0104h	VIC	Interrupt detection type selection register 1	PLS1	32	32
A001 0108h	VIC	Interrupt detection type selection register 2	PLS2	32	32
A001 010Ch	VIC	Interrupt detection type selection register 3	PLS3	32	32
A001 0110h	VIC	Interrupt detection type selection register 4	PLS4	32	32
A001 0114h	VIC	Interrupt detection type selection register 5	PLS5	32	32
A001 0118h	VIC	Interrupt detection type selection register 6	PLS6	32	32
A001 011Ch	VIC	Interrupt detection type selection register 7	PLS7	32	32
A001 0120h	VIC	Edge detection bit clear register 0	PIC0	32	32
A001 0124h	VIC	Edge detection bit clear register 1	PIC1	32	32
A001 0128h	VIC	Edge detection bit clear register 2	PIC2	32	32
A001 012Ch	VIC	Edge detection bit clear register 3	PIC3	32	32
A001 0130h	VIC	Edge detection bit clear register 4	PIC4	32	32
A001 0134h	VIC	Edge detection bit clear register 5	PIC5	32	32
A001 0138h	VIC	Edge detection bit clear register 6	PIC6	32	32
A001 013Ch	VIC	Edge detection bit clear register 7	PIC7	32	32
A001 01A0h	VIC	Interrupt level control register 8	LVLC8	32	32
A001 01A4h	VIC	Interrupt level control register 9	LVLC9	32	32
A001 01C0h	VIC	Interrupt priority level mask register 0	PRLM0	32	32
A001 01C4h	VIC	Interrupt priority level mask clear register 0	PRLC0	32	32
A001 01C8h	VIC	User mode enable register 0	UEN0	32	32
A001 0200h	VIC	Interrupt address register 0	HVA0	32	32
A001 0210h	VIC	Interrupt service status register 0	ISS0	32	32
A001 0214h	VIC	Interrupt service status register 1	ISS1	32	32
A001 0218h	VIC	Interrupt service status register 2	ISS2	32	32
A001 021Ch	VIC	Interrupt service status register 3	ISS3	32	32
A001 0220h	VIC	Interrupt service status register 4	ISS4	32	32
A001 0224h	VIC	Interrupt service status register 5	ISS5	32	32
A001 0228h	VIC	Interrupt service status register 6	ISS6	32	32
A001 022Ch	VIC	Interrupt service status register 7	ISS7	32	32
A001 0230h	VIC	Interrupt service current register 0	ISC0	32	32
A001 0234h	VIC	Interrupt service current register 1	ISC1	32	32
A001 0238h	VIC	Interrupt service current register 2	ISC2	32	32
A001 023Ch	VIC	Interrupt service current register 3	ISC3	32	32
A001 0240h	VIC	Interrupt service current register 4	ISC4	32	32
A001 0244h	VIC	Interrupt service current register 5	ISC5	32	32
A001 0248h	VIC	Interrupt service current register 6	ISC6	32	32
A001 024Ch	VIC	Interrupt service current register 7	ISC7	32	32
A001 0404h	VIC	Interrupt address storage register 1	VAD1	32	32

Table 5.1 List of I/O Registers (Address Order) (11 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0408h	VIC	Interrupt address storage register 2	VAD2	32	32
A001 040Ch	VIC	Interrupt address storage register 3	VAD3	32	32
A001 0410h	VIC	Interrupt address storage register 4	VAD4	32	32
A001 0414h	VIC	Interrupt address storage register 5	VAD5	32	32
A001 0418h	VIC	Interrupt address storage register 6	VAD6	32	32
A001 041Ch	VIC	Interrupt address storage register 7	VAD7	32	32
A001 0420h	VIC	Interrupt address storage register 8	VAD8	32	32
A001 0424h	VIC	Interrupt address storage register 9	VAD9	32	32
A001 0428h	VIC	Interrupt address storage register 10	VAD10	32	32
A001 042Ch	VIC	Interrupt address storage register 11	VAD11	32	32
A001 0430h	VIC	Interrupt address storage register 12	VAD12	32	32
A001 0434h	VIC	Interrupt address storage register 13	VAD13	32	32
A001 0438h	VIC	Interrupt address storage register 14	VAD14	32	32
A001 043Ch	VIC	Interrupt address storage register 15	VAD15	32	32
A001 0440h	VIC	Interrupt address storage register 16	VAD16	32	32
A001 0444h	VIC	Interrupt address storage register 17	VAD17	32	32
A001 0448h	VIC	Interrupt address storage register 18	VAD18	32	32
A001 044Ch	VIC	Interrupt address storage register 19	VAD19	32	32
A001 0450h	VIC	Interrupt address storage register 20	VAD20	32	32
A001 0454h	VIC	Interrupt address storage register 21	VAD21	32	32
A001 0458h	VIC	Interrupt address storage register 22	VAD22	32	32
A001 045Ch	VIC	Interrupt address storage register 23	VAD23	32	32
A001 0460h	VIC	Interrupt address storage register 24	VAD24	32	32
A001 0464h	VIC	Interrupt address storage register 25	VAD25	32	32
A001 0468h	VIC	Interrupt address storage register 26	VAD26	32	32
A001 046Ch	VIC	Interrupt address storage register 27	VAD27	32	32
A001 0470h	VIC	Interrupt address storage register 28	VAD28	32	32
A001 0474h	VIC	Interrupt address storage register 29	VAD29	32	32
A001 0478h	VIC	Interrupt address storage register 30	VAD30	32	32
A001 047Ch	VIC	Interrupt address storage register 31	VAD31	32	32
A001 0480h	VIC	Interrupt address storage register 32	VAD32	32	32
A001 0484h	VIC	Interrupt address storage register 33	VAD33	32	32
A001 0488h	VIC	Interrupt address storage register 34	VAD34	32	32
A001 048Ch	VIC	Interrupt address storage register 35	VAD35	32	32
A001 0490h	VIC	Interrupt address storage register 36	VAD36	32	32
A001 0494h	VIC	Interrupt address storage register 37	VAD37	32	32
A001 0498h	VIC	Interrupt address storage register 38	VAD38	32	32
A001 049Ch	VIC	Interrupt address storage register 39	VAD39	32	32
A001 04A0h	VIC	Interrupt address storage register 40	VAD40	32	32
A001 04A4h	VIC	Interrupt address storage register 41	VAD41	32	32
A001 04A8h	VIC	Interrupt address storage register 42	VAD42	32	32
A001 04ACh	VIC	Interrupt address storage register 43	VAD43	32	32
A001 04B0h	VIC	Interrupt address storage register 44	VAD44	32	32
A001 04B4h	VIC	Interrupt address storage register 45	VAD45	32	32
A001 04B8h	VIC	Interrupt address storage register 46	VAD46	32	32
A001 04BCh	VIC	Interrupt address storage register 47	VAD47	32	32
A001 04C0h	VIC	Interrupt address storage register 48	VAD48	32	32
A001 04C4h	VIC	Interrupt address storage register 49	VAD49	32	32

Table 5.1 List of I/O Registers (Address Order) (12 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 04C8h	VIC	Interrupt address storage register 50	VAD50	32	32
A001 04CCh	VIC	Interrupt address storage register 51	VAD51	32	32
A001 04D0h	VIC	Interrupt address storage register 52	VAD52	32	32
A001 04D4h	VIC	Interrupt address storage register 53	VAD53	32	32
A001 04D8h	VIC	Interrupt address storage register 54	VAD54	32	32
A001 04DCh	VIC	Interrupt address storage register 55	VAD55	32	32
A001 04E0h	VIC	Interrupt address storage register 56	VAD56	32	32
A001 04E4h	VIC	Interrupt address storage register 57	VAD57	32	32
A001 04E8h	VIC	Interrupt address storage register 58	VAD58	32	32
A001 04ECh	VIC	Interrupt address storage register 59	VAD59	32	32
A001 04F0h	VIC	Interrupt address storage register 60	VAD60	32	32
A001 04F4h	VIC	Interrupt address storage register 61	VAD61	32	32
A001 04F8h	VIC	Interrupt address storage register 62	VAD62	32	32
A001 04FCh	VIC	Interrupt address storage register 63	VAD63	32	32
A001 0500h	VIC	Interrupt address storage register 64	VAD64	32	32
A001 0504h	VIC	Interrupt address storage register 65	VAD65	32	32
A001 0508h	VIC	Interrupt address storage register 66	VAD66	32	32
A001 050Ch	VIC	Interrupt address storage register 67	VAD67	32	32
A001 0510h	VIC	Interrupt address storage register 68	VAD68	32	32
A001 0514h	VIC	Interrupt address storage register 69	VAD69	32	32
A001 0518h	VIC	Interrupt address storage register 70	VAD70	32	32
A001 051Ch	VIC	Interrupt address storage register 71	VAD71	32	32
A001 0520h	VIC	Interrupt address storage register 72	VAD72	32	32
A001 0524h	VIC	Interrupt address storage register 73	VAD73	32	32
A001 0528h	VIC	Interrupt address storage register 74	VAD74	32	32
A001 052Ch	VIC	Interrupt address storage register 75	VAD75	32	32
A001 0530h	VIC	Interrupt address storage register 76	VAD76	32	32
A001 0534h	VIC	Interrupt address storage register 77	VAD77	32	32
A001 0538h	VIC	Interrupt address storage register 78	VAD78	32	32
A001 053Ch	VIC	Interrupt address storage register 79	VAD79	32	32
A001 0540h	VIC	Interrupt address storage register 80	VAD80	32	32
A001 0544h	VIC	Interrupt address storage register 81	VAD81	32	32
A001 0548h	VIC	Interrupt address storage register 82	VAD82	32	32
A001 054Ch	VIC	Interrupt address storage register 83	VAD83	32	32
A001 0550h	VIC	Interrupt address storage register 84	VAD84	32	32
A001 0554h	VIC	Interrupt address storage register 85	VAD85	32	32
A001 0558h	VIC	Interrupt address storage register 86	VAD86	32	32
A001 055Ch	VIC	Interrupt address storage register 87	VAD87	32	32
A001 0560h	VIC	Interrupt address storage register 88	VAD88	32	32
A001 0564h	VIC	Interrupt address storage register 89	VAD89	32	32
A001 0568h	VIC	Interrupt address storage register 90	VAD90	32	32
A001 056Ch	VIC	Interrupt address storage register 91	VAD91	32	32
A001 0570h	VIC	Interrupt address storage register 92	VAD92	32	32
A001 0574h	VIC	Interrupt address storage register 93	VAD93	32	32
A001 0578h	VIC	Interrupt address storage register 94	VAD94	32	32
A001 057Ch	VIC	Interrupt address storage register 95	VAD95	32	32
A001 0580h	VIC	Interrupt address storage register 96	VAD96	32	32
A001 0584h	VIC	Interrupt address storage register 97	VAD97	32	32

Table 5.1 List of I/O Registers (Address Order) (13 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0588h	VIC	Interrupt address storage register 98	VAD98	32	32
A001 058Ch	VIC	Interrupt address storage register 99	VAD99	32	32
A001 0590h	VIC	Interrupt address storage register 100	VAD100	32	32
A001 0594h	VIC	Interrupt address storage register 101	VAD101	32	32
A001 0598h	VIC	Interrupt address storage register 102	VAD102	32	32
A001 059Ch	VIC	Interrupt address storage register 103	VAD103	32	32
A001 05A0h	VIC	Interrupt address storage register 104	VAD104	32	32
A001 05A4h	VIC	Interrupt address storage register 105	VAD105	32	32
A001 05A8h	VIC	Interrupt address storage register 106	VAD106	32	32
A001 05ACh	VIC	Interrupt address storage register 107	VAD107	32	32
A001 05B0h	VIC	Interrupt address storage register 108	VAD108	32	32
A001 05B4h	VIC	Interrupt address storage register 109	VAD109	32	32
A001 05B8h	VIC	Interrupt address storage register 110	VAD110	32	32
A001 05BCh	VIC	Interrupt address storage register 111	VAD111	32	32
A001 05C0h	VIC	Interrupt address storage register 112	VAD112	32	32
A001 05C4h	VIC	Interrupt address storage register 113	VAD113	32	32
A001 05C8h	VIC	Interrupt address storage register 114	VAD114	32	32
A001 05CCh	VIC	Interrupt address storage register 115	VAD115	32	32
A001 05D0h	VIC	Interrupt address storage register 116	VAD116	32	32
A001 05D4h	VIC	Interrupt address storage register 117	VAD117	32	32
A001 05D8h	VIC	Interrupt address storage register 118	VAD118	32	32
A001 05DCh	VIC	Interrupt address storage register 119	VAD119	32	32
A001 05E0h	VIC	Interrupt address storage register 120	VAD120	32	32
A001 05E4h	VIC	Interrupt address storage register 121	VAD121	32	32
A001 05E8h	VIC	Interrupt address storage register 122	VAD122	32	32
A001 05ECh	VIC	Interrupt address storage register 123	VAD123	32	32
A001 05F0h	VIC	Interrupt address storage register 124	VAD124	32	32
A001 05F4h	VIC	Interrupt address storage register 125	VAD125	32	32
A001 05F8h	VIC	Interrupt address storage register 126	VAD126	32	32
A001 05FCh	VIC	Interrupt address storage register 127	VAD127	32	32
A001 0600h	VIC	Interrupt address storage register 128	VAD128	32	32
A001 0604h	VIC	Interrupt address storage register 129	VAD129	32	32
A001 0608h	VIC	Interrupt address storage register 130	VAD130	32	32
A001 060Ch	VIC	Interrupt address storage register 131	VAD131	32	32
A001 0610h	VIC	Interrupt address storage register 132	VAD132	32	32
A001 0614h	VIC	Interrupt address storage register 133	VAD133	32	32
A001 0618h	VIC	Interrupt address storage register 134	VAD134	32	32
A001 061Ch	VIC	Interrupt address storage register 135	VAD135	32	32
A001 0620h	VIC	Interrupt address storage register 136	VAD136	32	32
A001 0624h	VIC	Interrupt address storage register 137	VAD137	32	32
A001 0628h	VIC	Interrupt address storage register 138	VAD138	32	32
A001 062Ch	VIC	Interrupt address storage register 139	VAD139	32	32
A001 0630h	VIC	Interrupt address storage register 140	VAD140	32	32
A001 0634h	VIC	Interrupt address storage register 141	VAD141	32	32
A001 0638h	VIC	Interrupt address storage register 142	VAD142	32	32
A001 063Ch	VIC	Interrupt address storage register 143	VAD143	32	32
A001 0640h	VIC	Interrupt address storage register 144	VAD144	32	32
A001 0644h	VIC	Interrupt address storage register 145	VAD145	32	32

Table 5.1 List of I/O Registers (Address Order) (14 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0648h	VIC	Interrupt address storage register 146	VAD146	32	32
A001 064Ch	VIC	Interrupt address storage register 147	VAD147	32	32
A001 0650h	VIC	Interrupt address storage register 148	VAD148	32	32
A001 0654h	VIC	Interrupt address storage register 149	VAD149	32	32
A001 0658h	VIC	Interrupt address storage register 150	VAD150	32	32
A001 065Ch	VIC	Interrupt address storage register 151	VAD151	32	32
A001 0660h	VIC	Interrupt address storage register 152	VAD152	32	32
A001 0664h	VIC	Interrupt address storage register 153	VAD153	32	32
A001 0668h	VIC	Interrupt address storage register 154	VAD154	32	32
A001 066Ch	VIC	Interrupt address storage register 155	VAD155	32	32
A001 0670h	VIC	Interrupt address storage register 156	VAD156	32	32
A001 0674h	VIC	Interrupt address storage register 157	VAD157	32	32
A001 0678h	VIC	Interrupt address storage register 158	VAD158	32	32
A001 067Ch	VIC	Interrupt address storage register 159	VAD159	32	32
A001 0680h	VIC	Interrupt address storage register 160	VAD160	32	32
A001 0684h	VIC	Interrupt address storage register 161	VAD161	32	32
A001 0688h	VIC	Interrupt address storage register 162	VAD162	32	32
A001 068Ch	VIC	Interrupt address storage register 163	VAD163	32	32
A001 0690h	VIC	Interrupt address storage register 164	VAD164	32	32
A001 0694h	VIC	Interrupt address storage register 165	VAD165	32	32
A001 0698h	VIC	Interrupt address storage register 166	VAD166	32	32
A001 069Ch	VIC	Interrupt address storage register 167	VAD167	32	32
A001 06A0h	VIC	Interrupt address storage register 168	VAD168	32	32
A001 06A4h	VIC	Interrupt address storage register 169	VAD169	32	32
A001 06A8h	VIC	Interrupt address storage register 170	VAD170	32	32
A001 06ACh	VIC	Interrupt address storage register 171	VAD171	32	32
A001 06B0h	VIC	Interrupt address storage register 172	VAD172	32	32
A001 06B4h	VIC	Interrupt address storage register 173	VAD173	32	32
A001 06B8h	VIC	Interrupt address storage register 174	VAD174	32	32
A001 06BCh	VIC	Interrupt address storage register 175	VAD175	32	32
A001 06C0h	VIC	Interrupt address storage register 176	VAD176	32	32
A001 06C4h	VIC	Interrupt address storage register 177	VAD177	32	32
A001 06C8h	VIC	Interrupt address storage register 178	VAD178	32	32
A001 06CCh	VIC	Interrupt address storage register 179	VAD179	32	32
A001 06D0h	VIC	Interrupt address storage register 180	VAD180	32	32
A001 06D4h	VIC	Interrupt address storage register 181	VAD181	32	32
A001 06D8h	VIC	Interrupt address storage register 182	VAD182	32	32
A001 06DCh	VIC	Interrupt address storage register 183	VAD183	32	32
A001 06E0h	VIC	Interrupt address storage register 184	VAD184	32	32
A001 06E4h	VIC	Interrupt address storage register 185	VAD185	32	32
A001 06E8h	VIC	Interrupt address storage register 186	VAD186	32	32
A001 06ECh	VIC	Interrupt address storage register 187	VAD187	32	32
A001 06F0h	VIC	Interrupt address storage register 188	VAD188	32	32
A001 06F4h	VIC	Interrupt address storage register 189	VAD189	32	32
A001 06F8h	VIC	Interrupt address storage register 190	VAD190	32	32
A001 06FCh	VIC	Interrupt address storage register 191	VAD191	32	32
A001 0700h	VIC	Interrupt address storage register 192	VAD192	32	32
A001 0704h	VIC	Interrupt address storage register 193	VAD193	32	32

Table 5.1 List of I/O Registers (Address Order) (15 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0708h	VIC	Interrupt address storage register 194	VAD194	32	32
A001 070Ch	VIC	Interrupt address storage register 195	VAD195	32	32
A001 0710h	VIC	Interrupt address storage register 196	VAD196	32	32
A001 0714h	VIC	Interrupt address storage register 197	VAD197	32	32
A001 0718h	VIC	Interrupt address storage register 198	VAD198	32	32
A001 071Ch	VIC	Interrupt address storage register 199	VAD199	32	32
A001 0720h	VIC	Interrupt address storage register 200	VAD200	32	32
A001 0724h	VIC	Interrupt address storage register 201	VAD201	32	32
A001 0728h	VIC	Interrupt address storage register 202	VAD202	32	32
A001 072Ch	VIC	Interrupt address storage register 203	VAD203	32	32
A001 0730h	VIC	Interrupt address storage register 204	VAD204	32	32
A001 0734h	VIC	Interrupt address storage register 205	VAD205	32	32
A001 0738h	VIC	Interrupt address storage register 206	VAD206	32	32
A001 073Ch	VIC	Interrupt address storage register 207	VAD207	32	32
A001 0740h	VIC	Interrupt address storage register 208	VAD208	32	32
A001 0744h	VIC	Interrupt address storage register 209	VAD209	32	32
A001 0748h	VIC	Interrupt address storage register 210	VAD210	32	32
A001 074Ch	VIC	Interrupt address storage register 211	VAD211	32	32
A001 0750h	VIC	Interrupt address storage register 212	VAD212	32	32
A001 0754h	VIC	Interrupt address storage register 213	VAD213	32	32
A001 0758h	VIC	Interrupt address storage register 214	VAD214	32	32
A001 075Ch	VIC	Interrupt address storage register 215	VAD215	32	32
A001 0760h	VIC	Interrupt address storage register 216	VAD216	32	32
A001 0764h	VIC	Interrupt address storage register 217	VAD217	32	32
A001 0768h	VIC	Interrupt address storage register 218	VAD218	32	32
A001 076Ch	VIC	Interrupt address storage register 219	VAD219	32	32
A001 0770h	VIC	Interrupt address storage register 220	VAD220	32	32
A001 0774h	VIC	Interrupt address storage register 221	VAD221	32	32
A001 0778h	VIC	Interrupt address storage register 222	VAD222	32	32
A001 077Ch	VIC	Interrupt address storage register 223	VAD223	32	32
A001 0780h	VIC	Interrupt address storage register 224	VAD224	32	32
A001 0784h	VIC	Interrupt address storage register 225	VAD225	32	32
A001 0788h	VIC	Interrupt address storage register 226	VAD226	32	32
A001 078Ch	VIC	Interrupt address storage register 227	VAD227	32	32
A001 0790h	VIC	Interrupt address storage register 228	VAD228	32	32
A001 0794h	VIC	Interrupt address storage register 229	VAD229	32	32
A001 0798h	VIC	Interrupt address storage register 230	VAD230	32	32
A001 079Ch	VIC	Interrupt address storage register 231	VAD231	32	32
A001 07A0h	VIC	Interrupt address storage register 232	VAD232	32	32
A001 07A4h	VIC	Interrupt address storage register 233	VAD233	32	32
A001 07A8h	VIC	Interrupt address storage register 234	VAD234	32	32
A001 07ACh	VIC	Interrupt address storage register 235	VAD235	32	32
A001 07B0h	VIC	Interrupt address storage register 236	VAD236	32	32
A001 07B4h	VIC	Interrupt address storage register 237	VAD237	32	32
A001 07B8h	VIC	Interrupt address storage register 238	VAD238	32	32
A001 07BCh	VIC	Interrupt address storage register 239	VAD239	32	32
A001 07C0h	VIC	Interrupt address storage register 240	VAD240	32	32
A001 07C4h	VIC	Interrupt address storage register 241	VAD241	32	32

Table 5.1 List of I/O Registers (Address Order) (16 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 07C8h	VIC	Interrupt address storage register 242	VAD242	32	32
A001 07CCh	VIC	Interrupt address storage register 243	VAD243	32	32
A001 07D0h	VIC	Interrupt address storage register 244	VAD244	32	32
A001 07D4h	VIC	Interrupt address storage register 245	VAD245	32	32
A001 07D8h	VIC	Interrupt address storage register 246	VAD246	32	32
A001 07DCh	VIC	Interrupt address storage register 247	VAD247	32	32
A001 07E0h	VIC	Interrupt address storage register 248	VAD248	32	32
A001 07E4h	VIC	Interrupt address storage register 249	VAD249	32	32
A001 07E8h	VIC	Interrupt address storage register 250	VAD250	32	32
A001 07ECh	VIC	Interrupt address storage register 251	VAD251	32	32
A001 07F0h	VIC	Interrupt address storage register 252	VAD252	32	32
A001 07F4h	VIC	Interrupt address storage register 253	VAD253	32	32
A001 07F8h	VIC	Interrupt address storage register 254	VAD254	32	32
A001 07FCh	VIC	Interrupt address storage register 255	VAD255	32	32
A001 0804h	VIC	Interrupt priority level storage register 1	PRL1	32	32
A001 0808h	VIC	Interrupt priority level storage register 2	PRL2	32	32
A001 080Ch	VIC	Interrupt priority level storage register 3	PRL3	32	32
A001 0810h	VIC	Interrupt priority level storage register 4	PRL4	32	32
A001 0814h	VIC	Interrupt priority level storage register 5	PRL5	32	32
A001 0818h	VIC	Interrupt priority level storage register 6	PRL6	32	32
A001 081Ch	VIC	Interrupt priority level storage register 7	PRL7	32	32
A001 0820h	VIC	Interrupt priority level storage register 8	PRL8	32	32
A001 0824h	VIC	Interrupt priority level storage register 9	PRL9	32	32
A001 0828h	VIC	Interrupt priority level storage register 10	PRL10	32	32
A001 082Ch	VIC	Interrupt priority level storage register 11	PRL11	32	32
A001 0830h	VIC	Interrupt priority level storage register 12	PRL12	32	32
A001 0834h	VIC	Interrupt priority level storage register 13	PRL13	32	32
A001 0838h	VIC	Interrupt priority level storage register 14	PRL14	32	32
A001 083Ch	VIC	Interrupt priority level storage register 15	PRL15	32	32
A001 0840h	VIC	Interrupt priority level storage register 16	PRL16	32	32
A001 0844h	VIC	Interrupt priority level storage register 17	PRL17	32	32
A001 0848h	VIC	Interrupt priority level storage register 18	PRL18	32	32
A001 084Ch	VIC	Interrupt priority level storage register 19	PRL19	32	32
A001 0850h	VIC	Interrupt priority level storage register 20	PRL20	32	32
A001 0854h	VIC	Interrupt priority level storage register 21	PRL21	32	32
A001 0858h	VIC	Interrupt priority level storage register 22	PRL22	32	32
A001 085Ch	VIC	Interrupt priority level storage register 23	PRL23	32	32
A001 0860h	VIC	Interrupt priority level storage register 24	PRL24	32	32
A001 0864h	VIC	Interrupt priority level storage register 25	PRL25	32	32
A001 0868h	VIC	Interrupt priority level storage register 26	PRL26	32	32
A001 086Ch	VIC	Interrupt priority level storage register 27	PRL27	32	32
A001 0870h	VIC	Interrupt priority level storage register 28	PRL28	32	32
A001 0874h	VIC	Interrupt priority level storage register 29	PRL29	32	32
A001 0878h	VIC	Interrupt priority level storage register 30	PRL30	32	32
A001 087Ch	VIC	Interrupt priority level storage register 31	PRL31	32	32
A001 0880h	VIC	Interrupt priority level storage register 32	PRL32	32	32
A001 0884h	VIC	Interrupt priority level storage register 33	PRL33	32	32
A001 0888h	VIC	Interrupt priority level storage register 34	PRL34	32	32

Table 5.1 List of I/O Registers (Address Order) (17 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 088Ch	VIC	Interrupt priority level storage register 35	PRL35	32	32
A001 0890h	VIC	Interrupt priority level storage register 36	PRL36	32	32
A001 0894h	VIC	Interrupt priority level storage register 37	PRL37	32	32
A001 0898h	VIC	Interrupt priority level storage register 38	PRL38	32	32
A001 089Ch	VIC	Interrupt priority level storage register 39	PRL39	32	32
A001 08A0h	VIC	Interrupt priority level storage register 40	PRL40	32	32
A001 08A4h	VIC	Interrupt priority level storage register 41	PRL41	32	32
A001 08A8h	VIC	Interrupt priority level storage register 42	PRL42	32	32
A001 08ACh	VIC	Interrupt priority level storage register 43	PRL43	32	32
A001 08B0h	VIC	Interrupt priority level storage register 44	PRL44	32	32
A001 08B4h	VIC	Interrupt priority level storage register 45	PRL45	32	32
A001 08B8h	VIC	Interrupt priority level storage register 46	PRL46	32	32
A001 08BCh	VIC	Interrupt priority level storage register 47	PRL47	32	32
A001 08C0h	VIC	Interrupt priority level storage register 48	PRL48	32	32
A001 08C4h	VIC	Interrupt priority level storage register 49	PRL49	32	32
A001 08C8h	VIC	Interrupt priority level storage register 50	PRL50	32	32
A001 08CCh	VIC	Interrupt priority level storage register 51	PRL51	32	32
A001 08D0h	VIC	Interrupt priority level storage register 52	PRL52	32	32
A001 08D4h	VIC	Interrupt priority level storage register 53	PRL53	32	32
A001 08D8h	VIC	Interrupt priority level storage register 54	PRL54	32	32
A001 08DCh	VIC	Interrupt priority level storage register 55	PRL55	32	32
A001 08E0h	VIC	Interrupt priority level storage register 56	PRL56	32	32
A001 08E4h	VIC	Interrupt priority level storage register 57	PRL57	32	32
A001 08E8h	VIC	Interrupt priority level storage register 58	PRL58	32	32
A001 08ECh	VIC	Interrupt priority level storage register 59	PRL59	32	32
A001 08F0h	VIC	Interrupt priority level storage register 60	PRL60	32	32
A001 08F4h	VIC	Interrupt priority level storage register 61	PRL61	32	32
A001 08F8h	VIC	Interrupt priority level storage register 62	PRL62	32	32
A001 08FCh	VIC	Interrupt priority level storage register 63	PRL63	32	32
A001 0900h	VIC	Interrupt priority level storage register 64	PRL64	32	32
A001 0904h	VIC	Interrupt priority level storage register 65	PRL65	32	32
A001 0908h	VIC	Interrupt priority level storage register 66	PRL66	32	32
A001 090Ch	VIC	Interrupt priority level storage register 67	PRL67	32	32
A001 0910h	VIC	Interrupt priority level storage register 68	PRL68	32	32
A001 0914h	VIC	Interrupt priority level storage register 69	PRL69	32	32
A001 0918h	VIC	Interrupt priority level storage register 70	PRL70	32	32
A001 091Ch	VIC	Interrupt priority level storage register 71	PRL71	32	32
A001 0920h	VIC	Interrupt priority level storage register 72	PRL72	32	32
A001 0924h	VIC	Interrupt priority level storage register 73	PRL73	32	32
A001 0928h	VIC	Interrupt priority level storage register 74	PRL74	32	32
A001 092Ch	VIC	Interrupt priority level storage register 75	PRL75	32	32
A001 0930h	VIC	Interrupt priority level storage register 76	PRL76	32	32
A001 0934h	VIC	Interrupt priority level storage register 77	PRL77	32	32
A001 0938h	VIC	Interrupt priority level storage register 78	PRL78	32	32
A001 093Ch	VIC	Interrupt priority level storage register 79	PRL79	32	32
A001 0940h	VIC	Interrupt priority level storage register 80	PRL80	32	32
A001 0944h	VIC	Interrupt priority level storage register 81	PRL81	32	32
A001 0948h	VIC	Interrupt priority level storage register 82	PRL82	32	32

Table 5.1 List of I/O Registers (Address Order) (18 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 094Ch	VIC	Interrupt priority level storage register 83	PRL83	32	32
A001 0950h	VIC	Interrupt priority level storage register 84	PRL84	32	32
A001 0954h	VIC	Interrupt priority level storage register 85	PRL85	32	32
A001 0958h	VIC	Interrupt priority level storage register 86	PRL86	32	32
A001 095Ch	VIC	Interrupt priority level storage register 87	PRL87	32	32
A001 0960h	VIC	Interrupt priority level storage register 88	PRL88	32	32
A001 0964h	VIC	Interrupt priority level storage register 89	PRL89	32	32
A001 0968h	VIC	Interrupt priority level storage register 90	PRL90	32	32
A001 096Ch	VIC	Interrupt priority level storage register 91	PRL91	32	32
A001 0970h	VIC	Interrupt priority level storage register 92	PRL92	32	32
A001 0974h	VIC	Interrupt priority level storage register 93	PRL93	32	32
A001 0978h	VIC	Interrupt priority level storage register 94	PRL94	32	32
A001 097Ch	VIC	Interrupt priority level storage register 95	PRL95	32	32
A001 0980h	VIC	Interrupt priority level storage register 96	PRL96	32	32
A001 0984h	VIC	Interrupt priority level storage register 97	PRL97	32	32
A001 0988h	VIC	Interrupt priority level storage register 98	PRL98	32	32
A001 098Ch	VIC	Interrupt priority level storage register 99	PRL99	32	32
A001 0990h	VIC	Interrupt priority level storage register 100	PRL100	32	32
A001 0994h	VIC	Interrupt priority level storage register 101	PRL101	32	32
A001 0998h	VIC	Interrupt priority level storage register 102	PRL102	32	32
A001 099Ch	VIC	Interrupt priority level storage register 103	PRL103	32	32
A001 09A0h	VIC	Interrupt priority level storage register 104	PRL104	32	32
A001 09A4h	VIC	Interrupt priority level storage register 105	PRL105	32	32
A001 09A8h	VIC	Interrupt priority level storage register 106	PRL106	32	32
A001 09ACh	VIC	Interrupt priority level storage register 107	PRL107	32	32
A001 09B0h	VIC	Interrupt priority level storage register 108	PRL108	32	32
A001 09B4h	VIC	Interrupt priority level storage register 109	PRL109	32	32
A001 09B8h	VIC	Interrupt priority level storage register 110	PRL110	32	32
A001 09BCh	VIC	Interrupt priority level storage register 111	PRL111	32	32
A001 09C0h	VIC	Interrupt priority level storage register 112	PRL112	32	32
A001 09C4h	VIC	Interrupt priority level storage register 113	PRL113	32	32
A001 09C8h	VIC	Interrupt priority level storage register 114	PRL114	32	32
A001 09CCh	VIC	Interrupt priority level storage register 115	PRL115	32	32
A001 09D0h	VIC	Interrupt priority level storage register 116	PRL116	32	32
A001 09D4h	VIC	Interrupt priority level storage register 117	PRL117	32	32
A001 09D8h	VIC	Interrupt priority level storage register 118	PRL118	32	32
A001 09DCh	VIC	Interrupt priority level storage register 119	PRL119	32	32
A001 09E0h	VIC	Interrupt priority level storage register 120	PRL120	32	32
A001 09E4h	VIC	Interrupt priority level storage register 121	PRL121	32	32
A001 09E8h	VIC	Interrupt priority level storage register 122	PRL122	32	32
A001 09ECh	VIC	Interrupt priority level storage register 123	PRL123	32	32
A001 09F0h	VIC	Interrupt priority level storage register 124	PRL124	32	32
A001 09F4h	VIC	Interrupt priority level storage register 125	PRL125	32	32
A001 09F8h	VIC	Interrupt priority level storage register 126	PRL126	32	32
A001 09FCh	VIC	Interrupt priority level storage register 127	PRL127	32	32
A001 0A00h	VIC	Interrupt priority level storage register 128	PRL128	32	32
A001 0A04h	VIC	Interrupt priority level storage register 129	PRL129	32	32
A001 0A08h	VIC	Interrupt priority level storage register 130	PRL130	32	32

Table 5.1 List of I/O Registers (Address Order) (19 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0A0Ch	VIC	Interrupt priority level storage register 131	PRL131	32	32
A001 0A10h	VIC	Interrupt priority level storage register 132	PRL132	32	32
A001 0A14h	VIC	Interrupt priority level storage register 133	PRL133	32	32
A001 0A18h	VIC	Interrupt priority level storage register 134	PRL134	32	32
A001 0A1Ch	VIC	Interrupt priority level storage register 135	PRL135	32	32
A001 0A20h	VIC	Interrupt priority level storage register 136	PRL136	32	32
A001 0A24h	VIC	Interrupt priority level storage register 137	PRL137	32	32
A001 0A28h	VIC	Interrupt priority level storage register 138	PRL138	32	32
A001 0A2Ch	VIC	Interrupt priority level storage register 139	PRL139	32	32
A001 0A30h	VIC	Interrupt priority level storage register 140	PRL140	32	32
A001 0A34h	VIC	Interrupt priority level storage register 141	PRL141	32	32
A001 0A38h	VIC	Interrupt priority level storage register 142	PRL142	32	32
A001 0A3Ch	VIC	Interrupt priority level storage register 143	PRL143	32	32
A001 0A40h	VIC	Interrupt priority level storage register 144	PRL144	32	32
A001 0A44h	VIC	Interrupt priority level storage register 145	PRL145	32	32
A001 0A48h	VIC	Interrupt priority level storage register 146	PRL146	32	32
A001 0A4Ch	VIC	Interrupt priority level storage register 147	PRL147	32	32
A001 0A50h	VIC	Interrupt priority level storage register 148	PRL148	32	32
A001 0A54h	VIC	Interrupt priority level storage register 149	PRL149	32	32
A001 0A58h	VIC	Interrupt priority level storage register 150	PRL150	32	32
A001 0A5Ch	VIC	Interrupt priority level storage register 151	PRL151	32	32
A001 0A60h	VIC	Interrupt priority level storage register 152	PRL152	32	32
A001 0A64h	VIC	Interrupt priority level storage register 153	PRL153	32	32
A001 0A68h	VIC	Interrupt priority level storage register 154	PRL154	32	32
A001 0A6Ch	VIC	Interrupt priority level storage register 155	PRL155	32	32
A001 0A70h	VIC	Interrupt priority level storage register 156	PRL156	32	32
A001 0A74h	VIC	Interrupt priority level storage register 157	PRL157	32	32
A001 0A78h	VIC	Interrupt priority level storage register 158	PRL158	32	32
A001 0A7Ch	VIC	Interrupt priority level storage register 159	PRL159	32	32
A001 0A80h	VIC	Interrupt priority level storage register 160	PRL160	32	32
A001 0A84h	VIC	Interrupt priority level storage register 161	PRL161	32	32
A001 0A88h	VIC	Interrupt priority level storage register 162	PRL162	32	32
A001 0A8Ch	VIC	Interrupt priority level storage register 163	PRL163	32	32
A001 0A90h	VIC	Interrupt priority level storage register 164	PRL164	32	32
A001 0A94h	VIC	Interrupt priority level storage register 165	PRL165	32	32
A001 0A98h	VIC	Interrupt priority level storage register 166	PRL166	32	32
A001 0A9Ch	VIC	Interrupt priority level storage register 167	PRL167	32	32
A001 0AA0h	VIC	Interrupt priority level storage register 168	PRL168	32	32
A001 0AA4h	VIC	Interrupt priority level storage register 169	PRL169	32	32
A001 0AA8h	VIC	Interrupt priority level storage register 170	PRL170	32	32
A001 0AACh	VIC	Interrupt priority level storage register 171	PRL171	32	32
A001 0AB0h	VIC	Interrupt priority level storage register 172	PRL172	32	32
A001 0AB4h	VIC	Interrupt priority level storage register 173	PRL173	32	32
A001 0AB8h	VIC	Interrupt priority level storage register 174	PRL174	32	32
A001 0ABCh	VIC	Interrupt priority level storage register 175	PRL175	32	32
A001 0AC0h	VIC	Interrupt priority level storage register 176	PRL176	32	32
A001 0AC4h	VIC	Interrupt priority level storage register 177	PRL177	32	32
A001 0AC8h	VIC	Interrupt priority level storage register 178	PRL178	32	32

Table 5.1 List of I/O Registers (Address Order) (20 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0ACCh	VIC	Interrupt priority level storage register 179	PRL179	32	32
A001 0AD0h	VIC	Interrupt priority level storage register 180	PRL180	32	32
A001 0AD4h	VIC	Interrupt priority level storage register 181	PRL181	32	32
A001 0AD8h	VIC	Interrupt priority level storage register 182	PRL182	32	32
A001 0ADCh	VIC	Interrupt priority level storage register 183	PRL183	32	32
A001 0AE0h	VIC	Interrupt priority level storage register 184	PRL184	32	32
A001 0AE4h	VIC	Interrupt priority level storage register 185	PRL185	32	32
A001 0AE8h	VIC	Interrupt priority level storage register 186	PRL186	32	32
A001 0AECh	VIC	Interrupt priority level storage register 187	PRL187	32	32
A001 0AF0h	VIC	Interrupt priority level storage register 188	PRL188	32	32
A001 0AF4h	VIC	Interrupt priority level storage register 189	PRL189	32	32
A001 0AF8h	VIC	Interrupt priority level storage register 190	PRL190	32	32
A001 0AFCh	VIC	Interrupt priority level storage register 191	PRL191	32	32
A001 0B00h	VIC	Interrupt priority level storage register 192	PRL192	32	32
A001 0B04h	VIC	Interrupt priority level storage register 193	PRL193	32	32
A001 0B08h	VIC	Interrupt priority level storage register 194	PRL194	32	32
A001 0B0Ch	VIC	Interrupt priority level storage register 195	PRL195	32	32
A001 0B10h	VIC	Interrupt priority level storage register 196	PRL196	32	32
A001 0B14h	VIC	Interrupt priority level storage register 197	PRL197	32	32
A001 0B18h	VIC	Interrupt priority level storage register 198	PRL198	32	32
A001 0B1Ch	VIC	Interrupt priority level storage register 199	PRL199	32	32
A001 0B20h	VIC	Interrupt priority level storage register 200	PRL200	32	32
A001 0B24h	VIC	Interrupt priority level storage register 201	PRL201	32	32
A001 0B28h	VIC	Interrupt priority level storage register 202	PRL202	32	32
A001 0B2Ch	VIC	Interrupt priority level storage register 203	PRL203	32	32
A001 0B30h	VIC	Interrupt priority level storage register 204	PRL204	32	32
A001 0B34h	VIC	Interrupt priority level storage register 205	PRL205	32	32
A001 0B38h	VIC	Interrupt priority level storage register 206	PRL206	32	32
A001 0B3Ch	VIC	Interrupt priority level storage register 207	PRL207	32	32
A001 0B40h	VIC	Interrupt priority level storage register 208	PRL208	32	32
A001 0B44h	VIC	Interrupt priority level storage register 209	PRL209	32	32
A001 0B48h	VIC	Interrupt priority level storage register 210	PRL210	32	32
A001 0B4Ch	VIC	Interrupt priority level storage register 211	PRL211	32	32
A001 0B50h	VIC	Interrupt priority level storage register 212	PRL212	32	32
A001 0B54h	VIC	Interrupt priority level storage register 213	PRL213	32	32
A001 0B58h	VIC	Interrupt priority level storage register 214	PRL214	32	32
A001 0B5Ch	VIC	Interrupt priority level storage register 215	PRL215	32	32
A001 0B60h	VIC	Interrupt priority level storage register 216	PRL216	32	32
A001 0B64h	VIC	Interrupt priority level storage register 217	PRL217	32	32
A001 0B68h	VIC	Interrupt priority level storage register 218	PRL218	32	32
A001 0B6Ch	VIC	Interrupt priority level storage register 219	PRL219	32	32
A001 0B70h	VIC	Interrupt priority level storage register 220	PRL220	32	32
A001 0B74h	VIC	Interrupt priority level storage register 221	PRL221	32	32
A001 0B78h	VIC	Interrupt priority level storage register 222	PRL222	32	32
A001 0B7Ch	VIC	Interrupt priority level storage register 223	PRL223	32	32
A001 0B80h	VIC	Interrupt priority level storage register 224	PRL224	32	32
A001 0B84h	VIC	Interrupt priority level storage register 225	PRL225	32	32
A001 0B88h	VIC	Interrupt priority level storage register 226	PRL226	32	32

Table 5.1 List of I/O Registers (Address Order) (21 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 0B8Ch	VIC	Interrupt priority level storage register 227	PRL227	32	32
A001 0B90h	VIC	Interrupt priority level storage register 228	PRL228	32	32
A001 0B94h	VIC	Interrupt priority level storage register 229	PRL229	32	32
A001 0B98h	VIC	Interrupt priority level storage register 230	PRL230	32	32
A001 0B9Ch	VIC	Interrupt priority level storage register 231	PRL231	32	32
A001 0BA0h	VIC	Interrupt priority level storage register 232	PRL232	32	32
A001 0BA4h	VIC	Interrupt priority level storage register 233	PRL233	32	32
A001 0BA8h	VIC	Interrupt priority level storage register 234	PRL234	32	32
A001 0BACh	VIC	Interrupt priority level storage register 235	PRL235	32	32
A001 0BB0h	VIC	Interrupt priority level storage register 236	PRL236	32	32
A001 0BB4h	VIC	Interrupt priority level storage register 237	PRL237	32	32
A001 0BB8h	VIC	Interrupt priority level storage register 238	PRL238	32	32
A001 0BBCh	VIC	Interrupt priority level storage register 239	PRL239	32	32
A001 0BC0h	VIC	Interrupt priority level storage register 240	PRL240	32	32
A001 0BC4h	VIC	Interrupt priority level storage register 241	PRL241	32	32
A001 0BC8h	VIC	Interrupt priority level storage register 242	PRL242	32	32
A001 0BCCh	VIC	Interrupt priority level storage register 243	PRL243	32	32
A001 0BD0h	VIC	Interrupt priority level storage register 244	PRL244	32	32
A001 0BD4h	VIC	Interrupt priority level storage register 245	PRL245	32	32
A001 0BD8h	VIC	Interrupt priority level storage register 246	PRL246	32	32
A001 0BDCh	VIC	Interrupt priority level storage register 247	PRL247	32	32
A001 0BE0h	VIC	Interrupt priority level storage register 248	PRL248	32	32
A001 0BE4h	VIC	Interrupt priority level storage register 249	PRL249	32	32
A001 0BE8h	VIC	Interrupt priority level storage register 250	PRL250	32	32
A001 0BECh	VIC	Interrupt priority level storage register 251	PRL251	32	32
A001 0BF0h	VIC	Interrupt priority level storage register 252	PRL252	32	32
A001 0BF4h	VIC	Interrupt priority level storage register 253	PRL253	32	32
A001 0BF8h	VIC	Interrupt priority level storage register 254	PRL254	32	32
A001 0BFCh	VIC	Interrupt priority level storage register 255	PRL255	32	32
A001 1000h	VIC	IRQ status register 8	IRQS8	32	32
A001 1004h	VIC	IRQ status register 9	IRQS9	32	32
A001 1040h	VIC	Interrupt input status register 8	RAIS8	32	32
A001 1044h	VIC	Interrupt input status register 9	RAIS9	32	32
A001 1080h	VIC	Interrupt enable register 8	IEN8	32	32
A001 1084h	VIC	Interrupt enable register 9	IEN9	32	32
A001 10A0h	VIC	Interrupt enable clear register 8	IEC8	32	32
A001 10A4h	VIC	Interrupt enable clear register 9	IEC9	32	32
A001 1100h	VIC	Interrupt detection type selection register 8	PLS8	32	32
A001 1104h	VIC	Interrupt detection type selection register 9	PLS9	32	32
A001 1120h	VIC	Edge detection bit clear register 8	PIC8	32	32
A001 1124h	VIC	Edge detection bit clear register 9	PIC9	32	32
A001 11C0h	VIC	Interrupt priority level mask register 1	PRLM1	32	32
A001 11C4h	VIC	Interrupt priority level mask clear register 1	PRLC1	32	32
A001 11C8h	VIC	User mode enable register 1	UEN1	32	32
A001 1210h	VIC	Interrupt service status register 8	ISS8	32	32
A001 1214h	VIC	Interrupt service status register 9	ISS9	32	32
A001 1230h	VIC	Interrupt service current register 8	ISC8	32	32
A001 1234h	VIC	Interrupt service current register 9	ISC9	32	32

Table 5.1 List of I/O Registers (Address Order) (22 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 1400h	VIC	Interrupt address storage register 256	VAD256	32	32
A001 1404h	VIC	Interrupt address storage register 257	VAD257	32	32
A001 1408h	VIC	Interrupt address storage register 258	VAD258	32	32
A001 140Ch	VIC	Interrupt address storage register 259	VAD259	32	32
A001 1410h	VIC	Interrupt address storage register 260	VAD260	32	32
A001 1414h	VIC	Interrupt address storage register 261	VAD261	32	32
A001 1418h	VIC	Interrupt address storage register 262	VAD262	32	32
A001 141Ch	VIC	Interrupt address storage register 263	VAD263	32	32
A001 1420h	VIC	Interrupt address storage register 264	VAD264	32	32
A001 1424h	VIC	Interrupt address storage register 265	VAD265	32	32
A001 1428h	VIC	Interrupt address storage register 266	VAD266	32	32
A001 142Ch	VIC	Interrupt address storage register 267	VAD267	32	32
A001 1430h	VIC	Interrupt address storage register 268	VAD268	32	32
A001 1434h	VIC	Interrupt address storage register 269	VAD269	32	32
A001 1438h	VIC	Interrupt address storage register 270	VAD270	32	32
A001 143Ch	VIC	Interrupt address storage register 271	VAD271	32	32
A001 1440h	VIC	Interrupt address storage register 272	VAD272	32	32
A001 1444h	VIC	Interrupt address storage register 273	VAD273	32	32
A001 1448h	VIC	Interrupt address storage register 274	VAD274	32	32
A001 144Ch	VIC	Interrupt address storage register 275	VAD275	32	32
A001 1450h	VIC	Interrupt address storage register 276	VAD276	32	32
A001 1454h	VIC	Interrupt address storage register 277	VAD277	32	32
A001 1458h	VIC	Interrupt address storage register 278	VAD278	32	32
A001 145Ch	VIC	Interrupt address storage register 279	VAD279	32	32
A001 1460h	VIC	Interrupt address storage register 280	VAD280	32	32
A001 1464h	VIC	Interrupt address storage register 281	VAD281	32	32
A001 1468h	VIC	Interrupt address storage register 282	VAD282	32	32
A001 146Ch	VIC	Interrupt address storage register 283	VAD283	32	32
A001 1470h	VIC	Interrupt address storage register 284	VAD284	32	32
A001 1474h	VIC	Interrupt address storage register 285	VAD285	32	32
A001 1478h	VIC	Interrupt address storage register 286	VAD286	32	32
A001 147Ch	VIC	Interrupt address storage register 287	VAD287	32	32
A001 1480h	VIC	Interrupt address storage register 288	VAD288	32	32
A001 1484h	VIC	Interrupt address storage register 289	VAD289	32	32
A001 1488h	VIC	Interrupt address storage register 290	VAD290	32	32
A001 148Ch	VIC	Interrupt address storage register 291	VAD291	32	32
A001 1490h	VIC	Interrupt address storage register 292	VAD292	32	32
A001 1494h	VIC	Interrupt address storage register 293	VAD293	32	32
A001 1498h	VIC	Interrupt address storage register 294	VAD294	32	32
A001 149Ch	VIC	Interrupt address storage register 295	VAD295	32	32
A001 14A0h	VIC	Interrupt address storage register 296	VAD296	32	32
A001 14A4h	VIC	Interrupt address storage register 297	VAD297	32	32
A001 14A8h	VIC	Interrupt address storage register 298	VAD298	32	32
A001 14ACh	VIC	Interrupt address storage register 299	VAD299	32	32
A001 14B0h	VIC	Interrupt address storage register 300	VAD300	32	32
A001 1800h	VIC	Interrupt priority level storage register 256	PRL256	32	32
A001 1804h	VIC	Interrupt priority level storage register 257	PRL257	32	32
A001 1808h	VIC	Interrupt priority level storage register 258	PRL258	32	32

Table 5.1 List of I/O Registers (Address Order) (23 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A001 180Ch	VIC	Interrupt priority level storage register 259	PRL259	32	32
A001 1810h	VIC	Interrupt priority level storage register 260	PRL260	32	32
A001 1814h	VIC	Interrupt priority level storage register 261	PRL261	32	32
A001 1818h	VIC	Interrupt priority level storage register 262	PRL262	32	32
A001 181Ch	VIC	Interrupt priority level storage register 263	PRL263	32	32
A001 1820h	VIC	Interrupt priority level storage register 264	PRL264	32	32
A001 1824h	VIC	Interrupt priority level storage register 265	PRL265	32	32
A001 1828h	VIC	Interrupt priority level storage register 266	PRL266	32	32
A001 182Ch	VIC	Interrupt priority level storage register 267	PRL267	32	32
A001 1830h	VIC	Interrupt priority level storage register 268	PRL268	32	32
A001 1834h	VIC	Interrupt priority level storage register 269	PRL269	32	32
A001 1838h	VIC	Interrupt priority level storage register 270	PRL270	32	32
A001 183Ch	VIC	Interrupt priority level storage register 271	PRL271	32	32
A001 1840h	VIC	Interrupt priority level storage register 272	PRL272	32	32
A001 1844h	VIC	Interrupt priority level storage register 273	PRL273	32	32
A001 1848h	VIC	Interrupt priority level storage register 274	PRL274	32	32
A001 184Ch	VIC	Interrupt priority level storage register 275	PRL275	32	32
A001 1850h	VIC	Interrupt priority level storage register 276	PRL276	32	32
A001 1854h	VIC	Interrupt priority level storage register 277	PRL277	32	32
A001 1858h	VIC	Interrupt priority level storage register 278	PRL278	32	32
A001 185Ch	VIC	Interrupt priority level storage register 279	PRL279	32	32
A001 1860h	VIC	Interrupt priority level storage register 280	PRL280	32	32
A001 1864h	VIC	Interrupt priority level storage register 281	PRL281	32	32
A001 1868h	VIC	Interrupt priority level storage register 282	PRL282	32	32
A001 186Ch	VIC	Interrupt priority level storage register 283	PRL283	32	32
A001 1870h	VIC	Interrupt priority level storage register 284	PRL284	32	32
A001 1874h	VIC	Interrupt priority level storage register 285	PRL285	32	32
A001 1878h	VIC	Interrupt priority level storage register 286	PRL286	32	32
A001 187Ch	VIC	Interrupt priority level storage register 287	PRL287	32	32
A001 1880h	VIC	Interrupt priority level storage register 288	PRL288	32	32
A001 1884h	VIC	Interrupt priority level storage register 289	PRL289	32	32
A001 1888h	VIC	Interrupt priority level storage register 290	PRL290	32	32
A001 188Ch	VIC	Interrupt priority level storage register 291	PRL291	32	32
A001 1890h	VIC	Interrupt priority level storage register 292	PRL292	32	32
A001 1894h	VIC	Interrupt priority level storage register 293	PRL293	32	32
A001 1898h	VIC	Interrupt priority level storage register 294	PRL294	32	32
A001 189Ch	VIC	Interrupt priority level storage register 295	PRL295	32	32
A001 18A0h	VIC	Interrupt priority level storage register 296	PRL296	32	32
A001 18A4h	VIC	Interrupt priority level storage register 297	PRL297	32	32
A001 18A8h	VIC	Interrupt priority level storage register 298	PRL298	32	32
A001 18ACh	VIC	Interrupt priority level storage register 299	PRL299	32	32
A001 18B0h	VIC	Interrupt priority level storage register 300	PRL300	32	32
A004 0000h	USBh	HcRevision register	HcRevision	32	32
A004 0004h	USBh	HcControl register	HcControl	32	32
A004 0008h	USBh	HcCommandStatus register	HcCommandStatus	32	32
A004 000Ch	USBh	HcInterruptStatus register	HcIntStatus	32	32
A004 0010h	USBh	HcInterruptEnable register	HcIntEnable	32	32
A004 0014h	USBh	HcInterruptDisable register	HcIntDisable	32	32

Table 5.1 List of I/O Registers (Address Order) (24 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A004 0018h	USBh	HcHCCA register	HcHCCA	32	32
A004 001Ch	USBh	HcPeriodicCurrentED register	HcPeriodCurED	32	32
A004 0020h	USBh	HcControlHeadED register	HcContHeadED	32	32
A004 0024h	USBh	HcControlCurrentED register	HcContCurrentED	32	32
A004 0028h	USBh	HcBulkHeadED register	HcBulkHeadED	32	32
A004 002Ch	USBh	HcBulkCurrentED register	HcBulkCurrentED	32	32
A004 0030h	USBh	HcDoneHead register	HcDoneHead	32	32
A004 0034h	USBh	HcFmInterval register	HcFmInterval	32	32
A004 0038h	USBh	HcFmRemaining register	HcFmRemaining	32	32
A004 003Ch	USBh	HcFmNumber register	HcFmNumber	32	32
A004 0040h	USBh	HcPeriodicStart register	HcPeriodicStart	32	32
A004 0048h	USBh	HcRhDescriptorA register	HcRhDescriptorA	32	32
A004 004Ch	USBh	HcRhDescriptorB register	HcRhDescriptorB	32	32
A004 0050h	USBh	HcRhStatus register	HcRhStatus_A	32	32
A004 0050h	USBh	HcRhStatus register	HcRhStatus_B	32	32
A004 0054h	USBh	HcRhPortStatus1 register	HcRhPortStatus1_A	32	32
A004 0054h	USBh	HcRhPortStatus1 register	HcRhPortStatus1_B	32	32
A004 1000h	USBh	HCIVERSION / CAPLENGTH register	CAPL_VERSION	32	32
A004 1004h	USBh	HCSPARAMS register	HCSPARAMS	32	32
A004 1008h	USBh	HCCPARAMS register	HCCPARAMS	32	32
A004 100Ch	USBh	HCSP_PORTROUTE register	HCSP_PORTROUTE	32	32
A004 1020h	USBh	USBCMD register	USBCMD	32	32
A004 1024h	USBh	USBSTS register	USBSTS	32	32
A004 1028h	USBh	USBINTR register	USBINTR	32	32
A004 102Ch	USBh	FRINDEX register	FRINDEX	32	32
A004 1030h	USBh	CTRLDSSEGMENT register	CTRLDSSEGMENT	32	32
A004 1034h	USBh	PERIODICLISTBASE register	PERIODICLIST	32	32
A004 1038h	USBh	ASYNCLISTADDR register	ASYNCLISTADDR	32	32
A004 1060h	USBh	CONFIGFLAG register	CONFIGFLAG	32	32
A004 1064h	USBh	PORTSC1 register	PORTSC1	32	32
A005 0000h	USBh	PCI configuration register for OHCI	VID_DID_O	32	32
A005 0000h	USBh	PCI configuration register for AHB-PCI bridge	VID_DID_A	32	32
A005 0004h	USBh	PCI configuration register for OHCI	CMND_STS_O	32	32
A005 0004h	USBh	PCI configuration register for AHB-PCI bridge	CMND_STS_A	32	32
A005 0008h	USBh	PCI configuration register for OHCI	REVID_CC_O	32	32
A005 0008h	USBh	PCI configuration register for AHB-PCI bridge	REVID_CC_A	32	32
A005 000Ch	USBh	PCI configuration register for OHCI	CLS_LT_HT_BIST_O	32	32
A005 000Ch	USBh	PCI configuration register for AHB-PCI bridge	CLS_LT_HT_BIST_A	32	32
A005 0010h	USBh	PCI configuration register for OHCI	BASEAD_O	32	32
A005 0010h	USBh	PCI configuration register for AHB-PCI bridge	BASEAD_A	32	32
A005 0014h	USBh	PCI configuration register for AHB-PCI bridge	WIN1_BASEAD	32	32
A005 002Ch	USBh	PCI configuration register for OHCI	SSVID_SSID_O	32	32
A005 002Ch	USBh	PCI configuration register for AHB-PCI bridge	SSVID_SSID_A	32	32
A005 0030h	USBh	PCI configuration register for OHCI	EROM_BASEAD	32	32
A005 0034h	USBh	PCI configuration register for OHCI	CAPPTR	32	32
A005 003Ch	USBh	PCI configuration register for OHCI	INTR_LINE_PIN_O	32	32
A005 003Ch	USBh	PCI configuration register for AHB-PCI bridge	INTR_LINE_PIN_A	32	32
A005 0040h	USBh	PCI configuration register for OHCI	CAPID_NIP_PMCAP	32	32

Table 5.1 List of I/O Registers (Address Order) (25 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A005 0044h	USBh	PCI configuration register for OHCI	PMC_STS_PMCSR	32	32
A005 00E0h	USBh	PCI configuration register for OHCI	EXT1	32	32
A005 00E4h	USBh	PCI configuration register for OHCI	EXT2	32	32
A005 0100h	USBh	PCI configuration register for EHCI	VID_DID_E	32	32
A005 0104h	USBh	PCI configuration register for EHCI	CMND_STS_E	32	32
A005 0108h	USBh	PCI configuration register for EHCI	REVID_CC_E	32	32
A005 010Ch	USBh	PCI configuration register for EHCI	CLS_LT_HT_BIST_E	32	32
A005 0110h	USBh	PCI configuration register for EHCI	BASEAD_E	32	32
A005 012Ch	USBh	PCI configuration register for EHCI	SSVID_SSID_E	32	32
A005 0130h	USBh	PCI configuration register for EHCI	EROM_BASEAD_E	32	32
A005 0134h	USBh	PCI configuration register for EHCI	CAPPTR_E	32	32
A005 013Ch	USBh	PCI configuration register for EHCI	INTR_LINE_PIN_E	32	32
A005 0140h	USBh	PCI configuration register for EHCI	CAPID_NIP_PMCAP_E	32	32
A005 0144h	USBh	PCI configuration register for EHCI	PMC_STS_PMCSR_E	32	32
A005 0160h	USBh	PCI configuration register for EHCI	SBRN_FLADJ_PW	32	32
A005 01E0h	USBh	PCI configuration register for EHCI	EXT1_E	32	32
A005 01E4h	USBh	PCI configuration register for EHCI	EXT2_E	32	32
A005 0800h	USBh	PCIAHB_WIN1_CTR register	PCIAHB_WIN1_CTR	32	32
A005 0810h	USBh	AHBPCI_WIN1_CTR register	AHBPCI_WIN1_CTR	32	32
A005 0814h	USBh	AHBPCI_WIN2_CTR register	AHBPCI_WIN2_CTR	32	32
A005 0820h	USBh	PCI_INT_ENABLE register	PCI_INT_ENABLE	32	32
A005 0824h	USBh	PCI_INT_STATUS register	PCI_INT_STATUS	32	32
A005 0830h	USBh	AHB_BUS_CTR register	AHB_BUS_CTR	32	32
A005 0834h	USBh	USBCTR register	USBCTR	32	32
A005 0840h	USBh	PCI_ARBITER_CTR register	PCI_ARBITER_CTR	32	32
A005 0848h	USBh	PCI_UNIT_REV register	PCI_UNIT_REV	32	32
A006 0000h	USBf	System configuration control register 0	SYSCFG0	16	16
A006 0002h	USBf	System configuration control register 1	SYSCFG1	16	16
A006 0004h	USBf	System configuration status register	SYSSTS0	16	16
A006 0008h	USBf	Device state control register 0	DVSTCTR0	16	16
A006 000Ch	USBf	USB test mode register	TESTMODE	16	16
A006 0010h	USBf	DMA0-FIFO bus configuration register	D0FBCFG	16	16
A006 0012h	USBf	DMA1-FIFO bus configuration register	D1FBCFG	16	16
A006 0014h	USBf	CFIFO port register	CFIFO	32	8, 16, 32
A006 0018h	USBf	D0FIFO port register	D0FIFO	32	8, 16, 32
A006 001Ch	USBf	D1FIFO port register	D1FIFO	32	8, 16, 32
A006 0020h	USBf	CFIFO port select register	CFIFOSEL	16	16
A006 0022h	USBf	CFIFO port control register	CFIFOCTR	16	16
A006 0028h	USBf	D0FIFO port select register	D0FIFOSEL	16	16
A006 002Ah	USBf	D0FIFO port control register	D0FIFOCTR	16	16
A006 002Ch	USBf	D1FIFO port select register	D1FIFOSEL	16	16
A006 002Eh	USBf	D1FIFO port control register	D1FIFOCTR	16	16
A006 0030h	USBf	Interrupt enable register 0	INTENB0	16	16
A006 0036h	USBf	BRDY interrupt enable register	BRDYENB	16	16
A006 0038h	USBf	NRDY interrupt enable register	NRDYENB	16	16
A006 003Ah	USBf	BEMP interrupt enable register	BEMPENB	16	16
A006 003Ch	USBf	SOF pin configuration register	SOFCFG	16	16
A006 0040h	USBf	Interrupt status register 0	INTSTS0	16	16

Table 5.1 List of I/O Registers (Address Order) (26 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 0046h	USBf	BRDY interrupt status register	BRDYSTS	16	16
A006 0048h	USBf	NRDY interrupt status register	NRDYSTS	16	16
A006 004Ah	USBf	BEMP interrupt status register	BEMPSTS	16	16
A006 004Ch	USBf	Frame number register	FRMNUM	16	16
A006 004Eh	USBf	µ frame number register	UFRMNUM	16	16
A006 0050h	USBf	USB address register	USBADDR	16	16
A006 0054h	USBf	USB request type register	USBREQ	16	16
A006 0056h	USBf	USB request value register	USBVAL	16	16
A006 0058h	USBf	USB request index register	USBINDX	16	16
A006 005Ah	USBf	USB request length register	USBLENG	16	16
A006 005Eh	USBf	DCP max packet size register	DCPMAXP	16	16
A006 0060h	USBf	DCP control register	DCPCTR	16	16
A006 0064h	USBf	Pipe window select register	PIPESEL	16	16
A006 0068h	USBf	Pipe configuration register	PIPECFG	16	16
A006 006Ah	USBf	Pipe buffer specification register	PIPEBUF	16	16
A006 006Ch	USBf	Pipe max packet size register	PIPEMAXP	16	16
A006 006Eh	USBf	Pipe cycle control register	PIPEPERI	16	16
A006 0070h	USBf	PIPE1 control register	PIPE1CTR	16	16
A006 0072h	USBf	PIPE2 control register	PIPE2CTR	16	16
A006 0074h	USBf	PIPE3 control register	PIPE3CTR	16	16
A006 0076h	USBf	PIPE4 control register	PIPE4CTR	16	16
A006 0078h	USBf	PIPE5 control register	PIPE5CTR	16	16
A006 007Ah	USBf	PIPE6 control register	PIPE6CTR	16	16
A006 007Ch	USBf	PIPE7 control register	PIPE7CTR	16	16
A006 007Eh	USBf	PIPE8 control register	PIPE8CTR	16	16
A006 0080h	USBf	PIPE9 control register	PIPE9CTR	16	16
A006 0090h	USBf	PIPE1 transaction counter enable register	PIPE1TRE	16	16
A006 0092h	USBf	PIPE1 transaction counter register	PIPE1TRN	16	16
A006 0094h	USBf	PIPE2 transaction counter enable register	PIPE2TRE	16	16
A006 0096h	USBf	PIPE2 transaction counter register	PIPE2TRN	16	16
A006 0098h	USBf	PIPE3 transaction counter enable register	PIPE3TRE	16	16
A006 009Ah	USBf	PIPE3 transaction counter register	PIPE3TRN	16	16
A006 009Ch	USBf	PIPE4 transaction counter enable register	PIPE4TRE	16	16
A006 009Eh	USBf	PIPE4 transaction counter register	PIPE4TRN	16	16
A006 00A0h	USBf	PIPE5 transaction counter enable register	PIPE5TRE	16	16
A006 00A2h	USBf	PIPE5 transaction counter register	PIPE5TRN	16	16
A006 0102h	USBf	Low-power status register	LPSTS	16	16
A006 0160h	USBf	D0FIFO continuous transfer port register 0	D0FIFOB0	32	32
A006 0164h	USBf	D0FIFO continuous transfer port register 1	D0FIFOB1	32	32
A006 0168h	USBf	D0FIFO continuous transfer port register 2	D0FIFOB2	32	32
A006 016Ch	USBf	D0FIFO continuous transfer port register 3	D0FIFOB3	32	32
A006 0170h	USBf	D0FIFO continuous transfer port register 4	D0FIFOB4	32	32
A006 0174h	USBf	D0FIFO continuous transfer port register 5	D0FIFOB5	32	32
A006 0178h	USBf	D0FIFO continuous transfer port register 6	D0FIFOB6	32	32
A006 017Ch	USBf	D0FIFO continuous transfer port register 7	D0FIFOB7	32	32
A006 0180h	USBf	D1FIFO continuous transfer port register 0	D1FIFOB0	32	32
A006 0184h	USBf	D1FIFO continuous transfer port register 1	D1FIFOB1	32	32
A006 0188h	USBf	D1FIFO continuous transfer port register 2	D1FIFOB2	32	32

Table 5.1 List of I/O Registers (Address Order) (27 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 018Ch	USBf	D1FIFO continuous transfer port register 3	D1FIFOB3	32	32
A006 0190h	USBf	D1FIFO continuous transfer port register 4	D1FIFOB4	32	32
A006 0194h	USBf	D1FIFO continuous transfer port register 5	D1FIFOB5	32	32
A006 0198h	USBf	D1FIFO continuous transfer port register 6	D1FIFOB6	32	32
A006 019Ch	USBf	D1FIFO continuous transfer port register 7	D1FIFOB7	32	32
A006 01A0h	USBf	PHY configuration register 1	PHYSET1	16	16
A006 2000h	DMA0	Next 0 source address register 0	DMAC0_N0SA_0_N	32	32
A006 2000h	DMA0	Next 0 source address register 0	DMAC0_N0SA_0_W	32	32
A006 2004h	DMA0	Next 0 destination address register 0	DMAC0_N0DA_0	32	32
A006 2008h	DMA0	Next 0 transaction byte register 0	DMAC0_N0TB_0	32	32
A006 200Ch	DMA0	Next 1 source address register 0	DMAC0_N1SA_0_N	32	32
A006 200Ch	DMA0	Next 1 source address register 0	DMAC0_N1SA_0_W	32	32
A006 2010h	DMA0	Next 1 destination address register 0	DMAC0_N1DA_0	32	32
A006 2014h	DMA0	Next 1 transaction byte register 0	DMAC0_N1TB_0	32	32
A006 2018h	DMA0	Current source address register 0	DMAC0_CRSA_0	32	32
A006 201Ch	DMA0	Current destination address register 0	DMAC0_CRDA_0	32	32
A006 2020h	DMA0	Current transaction byte register 0	DMAC0_CRTB_0	32	32
A006 2024h	DMA0	Channel status register 0	DMAC0_CHSTAT_0	32	32
A006 2028h	DMA0	Channel control register 0	DMAC0_CHCTRL_0	32	32
A006 202Ch	DMA0	Channel configuration register 0	DMAC0_CHCFG_0	32	32
A006 2030h	DMA0	Channel interval register 0	DMAC0_CHITVL_0	32	32
A006 2038h	DMA0	Next link address register 0	DMAC0_NXLA_0	32	32
A006 203Ch	DMA0	Current link address register 0	DMAC0_CRLA_0	32	32
A006 2040h	DMA0	Next 0 source address register 1	DMAC0_N0SA_1_N	32	32
A006 2040h	DMA0	Next 0 source address register 1	DMAC0_N0SA_1_W	32	32
A006 2044h	DMA0	Next 0 destination address register 1	DMAC0_N0DA_1	32	32
A006 2048h	DMA0	Next 0 transaction byte register 1	DMAC0_N0TB_1	32	32
A006 204Ch	DMA0	Next 1 source address register 1	DMAC0_N1SA_1_N	32	32
A006 204Ch	DMA0	Next 1 source address register 1	DMAC0_N1SA_1_W	32	32
A006 2050h	DMA0	Next 1 destination address register 1	DMAC0_N1DA_1	32	32
A006 2054h	DMA0	Next 1 transaction byte register 1	DMAC0_N1TB_1	32	32
A006 2058h	DMA0	Current source address register 1	DMAC0_CRSA_1	32	32
A006 205Ch	DMA0	Current destination address register 1	DMAC0_CRDA_1	32	32
A006 2060h	DMA0	Current transaction byte register 1	DMAC0_CRTB_1	32	32
A006 2064h	DMA0	Channel status register 1	DMAC0_CHSTAT_1	32	32
A006 2068h	DMA0	Channel control register 1	DMAC0_CHCTRL_1	32	32
A006 206Ch	DMA0	Channel configuration register 1	DMAC0_CHCFG_1	32	32
A006 2070h	DMA0	Channel interval register 1	DMAC0_CHITVL_1	32	32
A006 2078h	DMA0	Current link address register 1	DMAC0_NXLA_1	32	32
A006 207Ch	DMA0	Next link address register 1	DMAC0_CRLA_1	32	32
A006 2080h	DMA0	Next 0 source address register 2	DMAC0_N0SA_2_N	32	32
A006 2080h	DMA0	Next 0 source address register 2	DMAC0_N0SA_2_W	32	32
A006 2084h	DMA0	Next 0 destination address register 2	DMAC0_N0DA_2	32	32
A006 2088h	DMA0	Next 0 transaction byte register 2	DMAC0_N0TB_2	32	32
A006 208Ch	DMA0	Next 1 source address register 2	DMAC0_N1SA_2_N	32	32
A006 208Ch	DMA0	Next 1 source address register 2	DMAC0_N1SA_2_W	32	32
A006 2090h	DMA0	Next 1 destination address register 2	DMAC0_N1DA_2	32	32
A006 2094h	DMA0	Next 1 transaction byte register 2	DMAC0_N1TB_2	32	32

Table 5.1 List of I/O Registers (Address Order) (28 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 2098h	DMA0	Current source address register 2	DMAC0_CRSA_2	32	32
A006 209Ch	DMA0	Current destination address register 2	DMAC0_CRDA_2	32	32
A006 20A0h	DMA0	Current transaction byte register 2	DMAC0_CRTB_2	32	32
A006 20A4h	DMA0	Channel status register 2	DMAC0_CHSTAT_2	32	32
A006 20A8h	DMA0	Channel control register 2	DMAC0_CHCTRL_2	32	32
A006 20ACh	DMA0	Channel configuration register 2	DMAC0_CHCFG_2	32	32
A006 20B0h	DMA0	Channel interval register 2	DMAC0_CHITVL_2	32	32
A006 20B8h	DMA0	Next link address register 2	DMAC0_NXLA_2	32	32
A006 20BCh	DMA0	Current link address register 2	DMAC0_CRLA_2	32	32
A006 20C0h	DMA0	Next 0 source address register 3	DMAC0_N0SA_3_N	32	32
A006 20C0h	DMA0	Next 0 source address register 3	DMAC0_N0SA_3_W	32	32
A006 20C4h	DMA0	Next 0 destination address register 3	DMAC0_N0DA_3	32	32
A006 20C8h	DMA0	Next 0 transaction byte register 3	DMAC0_N0TB_3	32	32
A006 20CCh	DMA0	Next 1 source address register 3	DMAC0_N1SA_3_N	32	32
A006 20CCh	DMA0	Next 1 source address register 3	DMAC0_N1SA_3_W	32	32
A006 20D0h	DMA0	Next 1 destination address register 3	DMAC0_N1DA_3	32	32
A006 20D4h	DMA0	Next 1 transaction byte register 3	DMAC0_N1TB_3	32	32
A006 20D8h	DMA0	Current source address register 3	DMAC0_CRSA_3	32	32
A006 20DCh	DMA0	Current destination address register 3	DMAC0_CRDA_3	32	32
A006 20E0h	DMA0	Current transaction byte register 3	DMAC0_CRTB_3	32	32
A006 20E4h	DMA0	Channel status register 3	DMAC0_CHSTAT_3	32	32
A006 20E8h	DMA0	Channel control register 3	DMAC0_CHCTRL_3	32	32
A006 20ECh	DMA0	Channel configuration register 3	DMAC0_CHCFG_3	32	32
A006 20F0h	DMA0	Channel interval register 3	DMAC0_CHITVL_3	32	32
A006 20F8h	DMA0	Next link address register 3	DMAC0_NXLA_3	32	32
A006 20FCh	DMA0	Current link address register 3	DMAC0_CRLA_3	32	32
A006 2100h	DMA0	Next 0 source address register 4	DMAC0_N0SA_4_N	32	32
A006 2100h	DMA0	Next 0 source address register 4	DMAC0_N0SA_4_W	32	32
A006 2104h	DMA0	Next 0 destination address register 4	DMAC0_N0DA_4	32	32
A006 2108h	DMA0	Next 0 transaction byte register 4	DMAC0_N0TB_4	32	32
A006 210Ch	DMA0	Next 1 source address register 4	DMAC0_N1SA_4_N	32	32
A006 210Ch	DMA0	Next 1 source address register 4	DMAC0_N1SA_4_W	32	32
A006 2110h	DMA0	Next 1 destination address register 4	DMAC0_N1DA_4	32	32
A006 2114h	DMA0	Next 1 transaction byte register 4	DMAC0_N1TB_4	32	32
A006 2118h	DMA0	Current source address register 4	DMAC0_CRSA_4	32	32
A006 211Ch	DMA0	Current destination address register 4	DMAC0_CRDA_4	32	32
A006 2120h	DMA0	Current transaction byte register 4	DMAC0_CRTB_4	32	32
A006 2124h	DMA0	Channel status register 4	DMAC0_CHSTAT_4	32	32
A006 2128h	DMA0	Channel control register 4	DMAC0_CHCTRL_4	32	32
A006 212Ch	DMA0	Channel configuration register 4	DMAC0_CHCFG_4	32	32
A006 2130h	DMA0	Channel interval register 4	DMAC0_CHITVL_4	32	32
A006 2138h	DMA0	Next link address register 4	DMAC0_NXLA_4	32	32
A006 213Ch	DMA0	Current link address register 4	DMAC0_CRLA_4	32	32
A006 2140h	DMA0	Next 0 source address register 5	DMAC0_N0SA_5_N	32	32
A006 2140h	DMA0	Next 0 source address register 5	DMAC0_N0SA_5_W	32	32
A006 2144h	DMA0	Next 0 destination address register 5	DMAC0_N0DA_5	32	32
A006 2148h	DMA0	Next 0 transaction byte register 5	DMAC0_N0TB_5	32	32
A006 214Ch	DMA0	Next 1 source address register 5	DMAC0_N1SA_5_N	32	32

Table 5.1 List of I/O Registers (Address Order) (29 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 214Ch	DMA0	Next 1 source address register 5	DMAC0_N1SA_5_W	32	32
A006 2150h	DMA0	Next 1 destination address register 5	DMAC0_N1DA_5	32	32
A006 2154h	DMA0	Next 1 transaction byte register 5	DMAC0_N1TB_5	32	32
A006 2158h	DMA0	Current source address register 5	DMAC0_CRSA_5	32	32
A006 215Ch	DMA0	Current destination address register 5	DMAC0_CRDA_5	32	32
A006 2160h	DMA0	Current transaction byte register 5	DMAC0_CRTB_5	32	32
A006 2164h	DMA0	Channel status register 5	DMAC0_CHSTAT_5	32	32
A006 2168h	DMA0	Channel control register 5	DMAC0_CHCTRL_5	32	32
A006 216Ch	DMA0	Channel configuration register 5	DMAC0_CHCFG_5	32	32
A006 2170h	DMA0	Channel interval register 5	DMAC0_CHITVL_5	32	32
A006 2178h	DMA0	Next link address register 5	DMAC0_NXLA_5	32	32
A006 217Ch	DMA0	Current link address register 5	DMAC0_CRLA_5	32	32
A006 2180h	DMA0	Next 0 source address register 6	DMAC0_N0SA_6_N	32	32
A006 2180h	DMA0	Next 0 source address register 6	DMAC0_N0SA_6_W	32	32
A006 2184h	DMA0	Next 0 destination address register 6	DMAC0_N0DA_6	32	32
A006 2188h	DMA0	Next 0 transaction byte register 6	DMAC0_N0TB_6	32	32
A006 218Ch	DMA0	Next 1 source address register 6	DMAC0_N1SA_6_N	32	32
A006 218Ch	DMA0	Next 1 source address register 6	DMAC0_N1SA_6_W	32	32
A006 2190h	DMA0	Next 1 destination address register 6	DMAC0_N1DA_6	32	32
A006 2194h	DMA0	Next 1 transaction byte register 6	DMAC0_N1TB_6	32	32
A006 2198h	DMA0	Current source address register 6	DMAC0_CRSA_6	32	32
A006 219Ch	DMA0	Current destination address register 6	DMAC0_CRDA_6	32	32
A006 21A0h	DMA0	Current transaction byte register 6	DMAC0_CRTB_6	32	32
A006 21A4h	DMA0	Channel status register 6	DMAC0_CHSTAT_6	32	32
A006 21A8h	DMA0	Channel control register 6	DMAC0_CHCTRL_6	32	32
A006 21ACh	DMA0	Channel configuration register 6	DMAC0_CHCFG_6	32	32
A006 21B0h	DMA0	Channel interval register 6	DMAC0_CHITVL_6	32	32
A006 21B8h	DMA0	Next link address register 6	DMAC0_NXLA_6	32	32
A006 21BCh	DMA0	Current link address register 6	DMAC0_CRLA_6	32	32
A006 21C0h	DMA0	Next 0 source address register 7	DMAC0_N0SA_7_N	32	32
A006 21C0h	DMA0	Next 0 source address register 7	DMAC0_N0SA_7_W	32	32
A006 21C4h	DMA0	Next 0 destination address register 7	DMAC0_N0DA_7	32	32
A006 21C8h	DMA0	Next 0 transaction byte register 7	DMAC0_N0TB_7	32	32
A006 21CCh	DMA0	Next 1 source address register 7	DMAC0_N1SA_7_N	32	32
A006 21CCh	DMA0	Next 1 source address register 7	DMAC0_N1SA_7_W	32	32
A006 21D0h	DMA0	Next 1 destination address register 7	DMAC0_N1DA_7	32	32
A006 21D4h	DMA0	Next 1 transaction byte register 7	DMAC0_N1TB_7	32	32
A006 21D8h	DMA0	Current source address register 7	DMAC0_CRSA_7	32	32
A006 21DCh	DMA0	Current destination address register 7	DMAC0_CRDA_7	32	32
A006 21E0h	DMA0	Current transaction byte register 7	DMAC0_CRTB_7	32	32
A006 21E4h	DMA0	Channel status register 7	DMAC0_CHSTAT_7	32	32
A006 21E8h	DMA0	Channel control register 7	DMAC0_CHCTRL_7	32	32
A006 21ECh	DMA0	Channel configuration register 7	DMAC0_CHCFG_7	32	32
A006 21F0h	DMA0	Channel interval register 7	DMAC0_CHITVL_7	32	32
A006 21F8h	DMA0	Next link address register 7	DMAC0_NXLA_7	32	32
A006 21FCh	DMA0	Current link address register 7	DMAC0_CRLA_7	32	32
A006 2200h	DMA0	Source continuous register 0	DMAC0_SCNT_0	32	32
A006 2204h	DMA0	Source skip register 0	DMAC0_SSKP_0	32	32

Table 5.1 List of I/O Registers (Address Order) (30 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 2208h	DMA0	Destination continuous register 0	DMAC0_DCNT_0	32	32
A006 220Ch	DMA0	Destination skip register 0	DMAC0_DSKP_0	32	32
A006 2220h	DMA0	Source continuous register 1	DMAC0_SCNT_1	32	32
A006 2224h	DMA0	Source skip register 1	DMAC0_SSKP_1	32	32
A006 2228h	DMA0	Destination continuous register 1	DMAC0_DCNT_1	32	32
A006 222Ch	DMA0	Destination skip register 1	DMAC0_DSKP_1	32	32
A006 2240h	DMA0	Source continuous register 2	DMAC0_SCNT_2	32	32
A006 2244h	DMA0	Source skip register 2	DMAC0_SSKP_2	32	32
A006 2248h	DMA0	Destination continuous register 2	DMAC0_DCNT_2	32	32
A006 224Ch	DMA0	Destination skip register 2	DMAC0_DSKP_2	32	32
A006 2260h	DMA0	Source continuous register 3	DMAC0_SCNT_3	32	32
A006 2264h	DMA0	Source skip register 3	DMAC0_SSKP_3	32	32
A006 2268h	DMA0	Destination continuous register 3	DMAC0_DCNT_3	32	32
A006 226Ch	DMA0	Destination skip register 3	DMAC0_DSKP_3	32	32
A006 2280h	DMA0	Source continuous register 4	DMAC0_SCNT_4	32	32
A006 2284h	DMA0	Source skip register 4	DMAC0_SSKP_4	32	32
A006 2288h	DMA0	Destination continuous register 4	DMAC0_DCNT_4	32	32
A006 228Ch	DMA0	Destination skip register 4	DMAC0_DSKP_4	32	32
A006 22A0h	DMA0	Source continuous register 5	DMAC0_SCNT_5	32	32
A006 22A4h	DMA0	Source skip register 5	DMAC0_SSKP_5	32	32
A006 22A8h	DMA0	Destination continuous register 5	DMAC0_DCNT_5	32	32
A006 22ACh	DMA0	Destination skip register 5	DMAC0_DSKP_5	32	32
A006 22C0h	DMA0	Source continuous register 6	DMAC0_SCNT_6	32	32
A006 22C4h	DMA0	Source skip register 6	DMAC0_SSKP_6	32	32
A006 22C8h	DMA0	Destination continuous register 6	DMAC0_DCNT_6	32	32
A006 22CCh	DMA0	Destination skip register 6	DMAC0_DSKP_6	32	32
A006 22E0h	DMA0	Source continuous register 7	DMAC0_SCNT_7	32	32
A006 22E4h	DMA0	Source skip register 7	DMAC0_SSKP_7	32	32
A006 22E8h	DMA0	Destination continuous register 7	DMAC0_DCNT_7	32	32
A006 22ECh	DMA0	Destination skip register 7	DMAC0_DSKP_7	32	32
A006 2300h	DMA0	DMA control register A	DMAC0_DCTRL_A	32	32
A006 2304h	DMA0	Descriptor interval register A	DMAC0_DSCITVL_A	32	32
A006 2310h	DMA0	DMA status EN register A	DMAC0_DST_EN_A	32	32
A006 2314h	DMA0	DMA status ER register A	DMAC0_DST_ER_A	32	32
A006 2318h	DMA0	DMA status END register A	DMAC0_DST_END_A	32	32
A006 2320h	DMA0	DMA status SUS register A	DMAC0_DST_SUS_A	32	32
A006 2400h	DMA0	Next 0 source address register 8	DMAC0_N0SA_8_N	32	32
A006 2400h	DMA0	Next 0 source address register 8	DMAC0_N0SA_8_W	32	32
A006 2404h	DMA0	Next 0 destination address register 8	DMAC0_N0DA_8	32	32
A006 2408h	DMA0	Next 0 transaction byte register 8	DMAC0_N0TB_8	32	32
A006 240Ch	DMA0	Next 1 source address register 8	DMAC0_N1SA_8_N	32	32
A006 240Ch	DMA0	Next 1 source address register 8	DMAC0_N1SA_8_W	32	32
A006 2410h	DMA0	Next 1 destination address register 8	DMAC0_N1DA_8	32	32
A006 2414h	DMA0	Next 1 transaction byte register 8	DMAC0_N1TB_8	32	32
A006 2418h	DMA0	Current source address register 8	DMAC0_CRSA_8	32	32
A006 241Ch	DMA0	Current destination address register 8	DMAC0_CRDA_8	32	32
A006 2420h	DMA0	Current transaction byte register 8	DMAC0_CRTB_8	32	32
A006 2424h	DMA0	Channel status register 8	DMAC0_CHSTAT_8	32	32

Table 5.1 List of I/O Registers (Address Order) (31 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 2428h	DMA0	Channel control register 8	DMAC0_CHCTRL_8	32	32
A006 242Ch	DMA0	Channel configuration register 8	DMAC0_CHCFG_8	32	32
A006 2430h	DMA0	Channel interval register 8	DMAC0_CHITVL_8	32	32
A006 2438h	DMA0	Next link address register 8	DMAC0_NXLA_8	32	32
A006 243Ch	DMA0	Current link address register 8	DMAC0_CRLA_8	32	32
A006 2440h	DMA0	Next 0 source address register 9	DMAC0_N0SA_9_N	32	32
A006 2440h	DMA0	Next 0 source address register 9	DMAC0_N0SA_9_W	32	32
A006 2444h	DMA0	Next 0 destination address register 9	DMAC0_N0DA_9	32	32
A006 2448h	DMA0	Next 0 transaction byte register 9	DMAC0_N0TB_9	32	32
A006 244Ch	DMA0	Next 1 source address register 9	DMAC0_N1SA_9_N	32	32
A006 244Ch	DMA0	Next 1 source address register 9	DMAC0_N1SA_9_W	32	32
A006 2450h	DMA0	Next 1 destination address register 9	DMAC0_N1DA_9	32	32
A006 2454h	DMA0	Next 1 transaction byte register 9	DMAC0_N1TB_9	32	32
A006 2458h	DMA0	Current source address register 9	DMAC0_CRSA_9	32	32
A006 245Ch	DMA0	Current destination address register 9	DMAC0_CRDA_9	32	32
A006 2460h	DMA0	Current transaction byte register 9	DMAC0_CRTB_9	32	32
A006 2464h	DMA0	Channel status register 9	DMAC0_CHSTAT_9	32	32
A006 2468h	DMA0	Channel control register 9	DMAC0_CHCTRL_9	32	32
A006 246Ch	DMA0	Channel configuration register 9	DMAC0_CHCFG_9	32	32
A006 2470h	DMA0	Channel interval register 9	DMAC0_CHITVL_9	32	32
A006 2478h	DMA0	Next link address register 9	DMAC0_NXLA_9	32	32
A006 247Ch	DMA0	Current link address register 9	DMAC0_CRLA_9	32	32
A006 2480h	DMA0	Next 0 source address register 10	DMAC0_N0SA_10_N	32	32
A006 2480h	DMA0	Next 0 source address register 10	DMAC0_N0SA_10_W	32	32
A006 2484h	DMA0	Next 0 destination address register 10	DMAC0_N0DA_10	32	32
A006 2488h	DMA0	Next 0 transaction byte register 10	DMAC0_N0TB_10	32	32
A006 248Ch	DMA0	Next 1 source address register 10	DMAC0_N1SA_10_N	32	32
A006 248Ch	DMA0	Next 1 source address register 10	DMAC0_N1SA_10_W	32	32
A006 2490h	DMA0	Next 1 destination address register 10	DMAC0_N1DA_10	32	32
A006 2494h	DMA0	Next 1 transaction byte register 10	DMAC0_N1TB_10	32	32
A006 2498h	DMA0	Current source address register 10	DMAC0_CRSA_10	32	32
A006 249Ch	DMA0	Current destination address register 10	DMAC0_CRDA_10	32	32
A006 24A0h	DMA0	Current transaction byte register 10	DMAC0_CRTB_10	32	32
A006 24A4h	DMA0	Channel status register 10	DMAC0_CHSTAT_10	32	32
A006 24A8h	DMA0	Channel control register 10	DMAC0_CHCTRL_10	32	32
A006 24ACh	DMA0	Channel configuration register 10	DMAC0_CHCFG_10	32	32
A006 24B0h	DMA0	Channel interval register 10	DMAC0_CHITVL_10	32	32
A006 24B8h	DMA0	Next link address register 10	DMAC0_NXLA_10	32	32
A006 24BCh	DMA0	Current link address register 10	DMAC0_CRLA_10	32	32
A006 24C0h	DMA0	Next 0 source address register 11	DMAC0_N0SA_11_N	32	32
A006 24C0h	DMA0	Next 0 source address register 11	DMAC0_N0SA_11_W	32	32
A006 24C4h	DMA0	Next 0 destination address register 11	DMAC0_N0DA_11	32	32
A006 24C8h	DMA0	Next 0 transaction byte register 11	DMAC0_N0TB_11	32	32
A006 24CCh	DMA0	Next 1 source address register 11	DMAC0_N1SA_11_N	32	32
A006 24CCh	DMA0	Next 1 source address register 11	DMAC0_N1SA_11_W	32	32
A006 24D0h	DMA0	Next 1 destination address register 11	DMAC0_N1DA_11	32	32
A006 24D4h	DMA0	Next 1 transaction byte register 11	DMAC0_N1TB_11	32	32
A006 24D8h	DMA0	Current source address register 11	DMAC0_CRSA_11	32	32

Table 5.1 List of I/O Registers (Address Order) (32 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 24DCh	DMA0	Current destination address register 11	DMAC0_CRDA_11	32	32
A006 24E0h	DMA0	Current transaction byte register 11	DMAC0_CRTB_11	32	32
A006 24E4h	DMA0	Channel status register 11	DMAC0_CHSTAT_11	32	32
A006 24E8h	DMA0	Channel control register 11	DMAC0_CHCTRL_11	32	32
A006 24ECh	DMA0	Channel configuration register 11	DMAC0_CHCFG_11	32	32
A006 24F0h	DMA0	Channel interval register 11	DMAC0_CHITVL_11	32	32
A006 24F8h	DMA0	Next link address register 11	DMAC0_NXLA_11	32	32
A006 24FCh	DMA0	Current link address register 11	DMAC0_CRLA_11	32	32
A006 2500h	DMA0	Next 0 source address register 12	DMAC0_N0SA_12_N	32	32
A006 2500h	DMA0	Next 0 source address register 12	DMAC0_N0SA_12_W	32	32
A006 2504h	DMA0	Next 0 destination address register 12	DMAC0_N0DA_12	32	32
A006 2508h	DMA0	Next 0 transaction byte register 12	DMAC0_N0TB_12	32	32
A006 250Ch	DMA0	Next 1 source address register 12	DMAC0_N1SA_12_N	32	32
A006 250Ch	DMA0	Next 1 source address register 12	DMAC0_N1SA_12_W	32	32
A006 2510h	DMA0	Next 1 destination address register 12	DMAC0_N1DA_12	32	32
A006 2514h	DMA0	Next 1 transaction byte register 12	DMAC0_N1TB_12	32	32
A006 2518h	DMA0	Current source address register 12	DMAC0_CRSA_12	32	32
A006 251Ch	DMA0	Current destination address register 12	DMAC0_CRDA_12	32	32
A006 2520h	DMA0	Current transaction byte register 12	DMAC0_CRTB_12	32	32
A006 2524h	DMA0	Channel status register 12	DMAC0_CHSTAT_12	32	32
A006 2528h	DMA0	Channel control register 12	DMAC0_CHCTRL_12	32	32
A006 252Ch	DMA0	Channel configuration register 12	DMAC0_CHCFG_12	32	32
A006 2530h	DMA0	Channel interval register 12	DMAC0_CHITVL_12	32	32
A006 2538h	DMA0	Next link address register 12	DMAC0_NXLA_12	32	32
A006 253Ch	DMA0	Current link address register 12	DMAC0_CRLA_12	32	32
A006 2540h	DMA0	Next 0 source address register 13	DMAC0_N0SA_13_N	32	32
A006 2540h	DMA0	Next 0 source address register 13	DMAC0_N0SA_13_W	32	32
A006 2544h	DMA0	Next 0 destination address register 13	DMAC0_N0DA_13	32	32
A006 2548h	DMA0	Next 0 transaction byte register 13	DMAC0_N0TB_13	32	32
A006 254Ch	DMA0	Next 1 source address register 13	DMAC0_N1SA_13_N	32	32
A006 254Ch	DMA0	Next 1 source address register 13	DMAC0_N1SA_13_W	32	32
A006 2550h	DMA0	Next 1 destination address register 13	DMAC0_N1DA_13	32	32
A006 2554h	DMA0	Next 1 transaction byte register 13	DMAC0_N1TB_13	32	32
A006 2558h	DMA0	Current source address register 13	DMAC0_CRSA_13	32	32
A006 255Ch	DMA0	Current destination address register 13	DMAC0_CRDA_13	32	32
A006 2560h	DMA0	Current transaction byte register 13	DMAC0_CRTB_13	32	32
A006 2564h	DMA0	Channel status register 13	DMAC0_CHSTAT_13	32	32
A006 2568h	DMA0	Channel control register 13	DMAC0_CHCTRL_13	32	32
A006 256Ch	DMA0	Channel configuration register 13	DMAC0_CHCFG_13	32	32
A006 2570h	DMA0	Channel interval register 13	DMAC0_CHITVL_13	32	32
A006 2578h	DMA0	Next link address register 13	DMAC0_NXLA_13	32	32
A006 257Ch	DMA0	Current link address register 13	DMAC0_CRLA_13	32	32
A006 2580h	DMA0	Next 0 source address register 14	DMAC0_N0SA_14_N	32	32
A006 2580h	DMA0	Next 0 source address register 14	DMAC0_N0SA_14_W	32	32
A006 2584h	DMA0	Next 0 destination address register 14	DMAC0_N0DA_14	32	32
A006 2588h	DMA0	Next 0 transaction byte register 14	DMAC0_N0TB_14	32	32
A006 258Ch	DMA0	Next 1 source address register 14	DMAC0_N1SA_14_N	32	32
A006 258Ch	DMA0	Next 1 source address register 14	DMAC0_N1SA_14_W	32	32

Table 5.1 List of I/O Registers (Address Order) (33 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 2590h	DMA0	Next 1 destination address register 14	DMAC0_N1DA_14	32	32
A006 2594h	DMA0	Next 1 transaction byte register 14	DMAC0_N1TB_14	32	32
A006 2598h	DMA0	Current source address register 14	DMAC0_CRSA_14	32	32
A006 259Ch	DMA0	Current destination address register 14	DMAC0_CRDA_14	32	32
A006 25A0h	DMA0	Current transaction byte register 14	DMAC0_CRTB_14	32	32
A006 25A4h	DMA0	Channel status register 14	DMAC0_CHSTAT_14	32	32
A006 25A8h	DMA0	Channel control register 14	DMAC0_CHCTRL_14	32	32
A006 25ACh	DMA0	Channel configuration register 14	DMAC0_CHCFG_14	32	32
A006 25B0h	DMA0	Channel interval register 14	DMAC0_CHITVL_14	32	32
A006 25B8h	DMA0	Next link address register 14	DMAC0_NXLA_14	32	32
A006 25BCh	DMA0	Current link address register 14	DMAC0_CRLA_14	32	32
A006 25C0h	DMA0	Next 0 source address register 15	DMAC0_N0SA_15_N	32	32
A006 25C0h	DMA0	Next 0 source address register 15	DMAC0_N0SA_15_W	32	32
A006 25C4h	DMA0	Next 0 destination address register 15	DMAC0_N0DA_15	32	32
A006 25C8h	DMA0	Next 0 transaction byte register 15	DMAC0_N0TB_15	32	32
A006 25CCh	DMA0	Next 1 source address register 15	DMAC0_N1SA_15_N	32	32
A006 25CCh	DMA0	Next 1 source address register 15	DMAC0_N1SA_15_W	32	32
A006 25D0h	DMA0	Next 1 destination address register 15	DMAC0_N1DA_15	32	32
A006 25D4h	DMA0	Next 1 transaction byte register 15	DMAC0_N1TB_15	32	32
A006 25D8h	DMA0	Current source address register 15	DMAC0_CRSA_15	32	32
A006 25DCh	DMA0	Current destination address register 15	DMAC0_CRDA_15	32	32
A006 25E0h	DMA0	Current transaction byte register 15	DMAC0_CRTB_15	32	32
A006 25E4h	DMA0	Channel status register 15	DMAC0_CHSTAT_15	32	32
A006 25E8h	DMA0	Channel control register 15	DMAC0_CHCTRL_15	32	32
A006 25ECh	DMA0	Channel configuration register 15	DMAC0_CHCFG_15	32	32
A006 25F0h	DMA0	Channel interval register 15	DMAC0_CHITVL_15	32	32
A006 25F8h	DMA0	Next link address register 15	DMAC0_NXLA_15	32	32
A006 25FCh	DMA0	Current link address register 15	DMAC0_CRLA_15	32	32
A006 2600h	DMA0	Source continuous register 8	DMAC0_SCNT_8	32	32
A006 2604h	DMA0	Source skip register 8	DMAC0_SSKP_8	32	32
A006 2608h	DMA0	Destination continuous register 8	DMAC0_DCNT_8	32	32
A006 260Ch	DMA0	Destination skip register 8	DMAC0_DSKP_8	32	32
A006 2620h	DMA0	Source continuous register 9	DMAC0_SCNT_9	32	32
A006 2624h	DMA0	Source skip register 9	DMAC0_SSKP_9	32	32
A006 2628h	DMA0	Destination continuous register 9	DMAC0_DCNT_9	32	32
A006 262Ch	DMA0	Destination skip register 9	DMAC0_DSKP_9	32	32
A006 2640h	DMA0	Source continuous register 10	DMAC0_SCNT_10	32	32
A006 2644h	DMA0	Source skip register 10	DMAC0_SSKP_10	32	32
A006 2648h	DMA0	Destination continuous register 10	DMAC0_DCNT_10	32	32
A006 264Ch	DMA0	Destination skip register 10	DMAC0_DSKP_10	32	32
A006 2660h	DMA0	Source continuous register 11	DMAC0_SCNT_11	32	32
A006 2664h	DMA0	Source skip register 11	DMAC0_SSKP_11	32	32
A006 2668h	DMA0	Destination continuous register 11	DMAC0_DCNT_11	32	32
A006 266Ch	DMA0	Destination skip register 11	DMAC0_DSKP_11	32	32
A006 2680h	DMA0	Source continuous register 12	DMAC0_SCNT_12	32	32
A006 2684h	DMA0	Source skip register 12	DMAC0_SSKP_12	32	32
A006 2688h	DMA0	Destination continuous register 12	DMAC0_DCNT_12	32	32
A006 268Ch	DMA0	Destination skip register 12	DMAC0_DSKP_12	32	32

Table 5.1 List of I/O Registers (Address Order) (34 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 26A0h	DMA0	Source continuous register 13	DMAC0_SCNT_13	32	32
A006 26A4h	DMA0	Source skip register 13	DMAC0_SSKP_13	32	32
A006 26A8h	DMA0	Destination continuous register 13	DMAC0_DCNT_13	32	32
A006 26ACh	DMA0	Destination skip register 13	DMAC0_DSKP_13	32	32
A006 26C0h	DMA0	Source continuous register 14	DMAC0_SCNT_14	32	32
A006 26C4h	DMA0	Source skip register 14	DMAC0_SSKP_14	32	32
A006 26C8h	DMA0	Destination continuous register 14	DMAC0_DCNT_14	32	32
A006 26CCh	DMA0	Destination skip register 14	DMAC0_DSKP_14	32	32
A006 26E0h	DMA0	Source continuous register 15	DMAC0_SCNT_15	32	32
A006 26E4h	DMA0	Source skip register 15	DMAC0_SSKP_15	32	32
A006 26E8h	DMA0	Destination continuous register 15	DMAC0_DCNT_15	32	32
A006 26ECh	DMA0	Destination skip register 15	DMAC0_DSKP_15	32	32
A006 2700h	DMA0	DMA control register B	DMAC0_DCTRL_B	32	32
A006 2704h	DMA0	Descriptor interval register B	DMAC0_DSCITVL_B	32	32
A006 2710h	DMA0	DMA status EN register B	DMAC0_DST_EN_B	32	32
A006 2714h	DMA0	DMA status ER register B	DMAC0_DST_ER_B	32	32
A006 2718h	DMA0	DMA status END register B	DMAC0_DST_END_B	32	32
A006 2720h	DMA0	DMA status SUS register B	DMAC0_DST_SUS_B	32	32
A006 3000h	DMA1	Next 0 source address register 0	DMAC1_N0SA_0_N	32	32
A006 3000h	DMA1	Next 0 source address register 0	DMAC1_N0SA_0_W	32	32
A006 3004h	DMA1	Next 0 destination address register 0	DMAC1_N0DA_0	32	32
A006 3008h	DMA1	Next 0 transaction byte register 0	DMAC1_N0TB_0	32	32
A006 300Ch	DMA1	Next 1 source address register 0	DMAC1_N1SA_0_N	32	32
A006 300Ch	DMA1	Next 1 source address register 0	DMAC1_N1SA_0_W	32	32
A006 3010h	DMA1	Next 1 destination address register 0	DMAC1_N1DA_0	32	32
A006 3014h	DMA1	Next 1 transaction byte register 0	DMAC1_N1TB_0	32	32
A006 3018h	DMA1	Current source address register 0	DMAC1_CRSA_0	32	32
A006 301Ch	DMA1	Current destination address register 0	DMAC1_CRDA_0	32	32
A006 3020h	DMA1	Current transaction byte register 0	DMAC1_CRTB_0	32	32
A006 3024h	DMA1	Channel status register 0	DMAC1_CHSTAT_0	32	32
A006 3028h	DMA1	Channel control register 0	DMAC1_CHCTRL_0	32	32
A006 302Ch	DMA1	Channel configuration register 0	DMAC1_CHCFG_0	32	32
A006 3030h	DMA1	Channel interval register 0	DMAC1_CHITVL_0	32	32
A006 3038h	DMA1	Next link address register 0	DMAC1_NXLA_0	32	32
A006 303Ch	DMA1	Current link address register 0	DMAC1_CRLA_0	32	32
A006 3040h	DMA1	Next 0 source address register 1	DMAC1_N0SA_1_N	32	32
A006 3040h	DMA1	Next 0 source address register 1	DMAC1_N0SA_1_W	32	32
A006 3044h	DMA1	Next 0 destination address register 1	DMAC1_N0DA_1	32	32
A006 3048h	DMA1	Next 0 transaction byte register 1	DMAC1_N0TB_1	32	32
A006 304Ch	DMA1	Next 1 source address register 1	DMAC1_N1SA_1_N	32	32
A006 304Ch	DMA1	Next 1 source address register 1	DMAC1_N1SA_1_W	32	32
A006 3050h	DMA1	Next 1 destination address register 1	DMAC1_N1DA_1	32	32
A006 3054h	DMA1	Next 1 transaction byte register 1	DMAC1_N1TB_1	32	32
A006 3058h	DMA1	Current source address register 1	DMAC1_CRSA_1	32	32
A006 305Ch	DMA1	Current destination address register 1	DMAC1_CRDA_1	32	32
A006 3060h	DMA1	Current transaction byte register 1	DMAC1_CRTB_1	32	32
A006 3064h	DMA1	Channel status register 1	DMAC1_CHSTAT_1	32	32
A006 3068h	DMA1	Channel control register 1	DMAC1_CHCTRL_1	32	32

Table 5.1 List of I/O Registers (Address Order) (35 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 306Ch	DMA1	Channel configuration register 1	DMAC1_CHCFG_1	32	32
A006 3070h	DMA1	Channel interval register 1	DMAC1_CHITVL_1	32	32
A006 3078h	DMA1	Next link address register 1	DMAC1_NXLA_1	32	32
A006 307Ch	DMA1	Current link address register 1	DMAC1_CRLA_1	32	32
A006 3080h	DMA1	Next 0 source address register 2	DMAC1_N0SA_2_N	32	32
A006 3080h	DMA1	Next 0 source address register 2	DMAC1_N0SA_2_W	32	32
A006 3084h	DMA1	Next 0 destination address register 2	DMAC1_N0DA_2	32	32
A006 3088h	DMA1	Next 0 transaction byte register 2	DMAC1_N0TB_2	32	32
A006 308Ch	DMA1	Next 1 source address register 2	DMAC1_N1SA_2_N	32	32
A006 308Ch	DMA1	Next 1 source address register 2	DMAC1_N1SA_2_W	32	32
A006 3090h	DMA1	Next 1 destination address register 2	DMAC1_N1DA_2	32	32
A006 3094h	DMA1	Next 1 transaction byte register 2	DMAC1_N1TB_2	32	32
A006 3098h	DMA1	Current source address register 2	DMAC1_CRSA_2	32	32
A006 309Ch	DMA1	Current destination address register 2	DMAC1_CRDA_2	32	32
A006 30A0h	DMA1	Current transaction byte register 2	DMAC1_CRTB_2	32	32
A006 30A4h	DMA1	Channel status register 2	DMAC1_CHSTAT_2	32	32
A006 30A8h	DMA1	Channel control register 2	DMAC1_CHCTRL_2	32	32
A006 30ACh	DMA1	Channel configuration register 2	DMAC1_CHCFG_2	32	32
A006 30B0h	DMA1	Channel interval register 2	DMAC1_CHITVL_2	32	32
A006 30B8h	DMA1	Next link address register 2	DMAC1_NXLA_2	32	32
A006 30BCh	DMA1	Current link address register 2	DMAC1_CRLA_2	32	32
A006 30C0h	DMA1	Next 0 source address register 3	DMAC1_N0SA_3_N	32	32
A006 30C0h	DMA1	Next 0 source address register 3	DMAC1_N0SA_3_W	32	32
A006 30C4h	DMA1	Next 0 destination address register 3	DMAC1_N0DA_3	32	32
A006 30C8h	DMA1	Next 0 transaction byte register 3	DMAC1_N0TB_3	32	32
A006 30CCh	DMA1	Next 1 source address register 3	DMAC1_N1SA_3_N	32	32
A006 30CCh	DMA1	Next 1 source address register 3	DMAC1_N1SA_3_W	32	32
A006 30D0h	DMA1	Next 1 destination address register 3	DMAC1_N1DA_3	32	32
A006 30D4h	DMA1	Next 1 transaction byte register 3	DMAC1_N1TB_3	32	32
A006 30D8h	DMA1	Current source address register 3	DMAC1_CRSA_3	32	32
A006 30DCh	DMA1	Current destination address register 3	DMAC1_CRDA_3	32	32
A006 30E0h	DMA1	Current transaction byte register 3	DMAC1_CRTB_3	32	32
A006 30E4h	DMA1	Channel status register 3	DMAC1_CHSTAT_3	32	32
A006 30E8h	DMA1	Channel control register 3	DMAC1_CHCTRL_3	32	32
A006 30ECh	DMA1	Channel configuration register 3	DMAC1_CHCFG_3	32	32
A006 30F0h	DMA1	Channel interval register 3	DMAC1_CHITVL_3	32	32
A006 30F8h	DMA1	Next link address register 3	DMAC1_NXLA_3	32	32
A006 30FCh	DMA1	Current link address register 3	DMAC1_CRLA_3	32	32
A006 3100h	DMA1	Next 0 source address register 4	DMAC1_N0SA_4_N	32	32
A006 3100h	DMA1	Next 0 source address register 4	DMAC1_N0SA_4_W	32	32
A006 3104h	DMA1	Next 0 destination address register 4	DMAC1_N0DA_4	32	32
A006 3108h	DMA1	Next 0 transaction byte register 4	DMAC1_N0TB_4	32	32
A006 310Ch	DMA1	Next 1 source address register 4	DMAC1_N1SA_4_N	32	32
A006 310Ch	DMA1	Next 1 source address register 4	DMAC1_N1SA_4_W	32	32
A006 3110h	DMA1	Next 1 destination address register 4	DMAC1_N1DA_4	32	32
A006 3114h	DMA1	Next 1 transaction byte register 4	DMAC1_N1TB_4	32	32
A006 3118h	DMA1	Current source address register 4	DMAC1_CRSA_4	32	32
A006 311Ch	DMA1	Current destination address register 4	DMAC1_CRDA_4	32	32

Table 5.1 List of I/O Registers (Address Order) (36 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 3120h	DMA1	Current transaction byte register 4	DMAC1_CRTB_4	32	32
A006 3124h	DMA1	Channel status register 4	DMAC1_CHSTAT_4	32	32
A006 3128h	DMA1	Channel control register 4	DMAC1_CHCTRL_4	32	32
A006 312Ch	DMA1	Channel configuration register 4	DMAC1_CHCFG_4	32	32
A006 3130h	DMA1	Channel interval register 4	DMAC1_CHITVL_4	32	32
A006 3138h	DMA1	Next link address register 4	DMAC1_NXLA_4	32	32
A006 313Ch	DMA1	Current link address register 4	DMAC1_CRLA_4	32	32
A006 3140h	DMA1	Next 0 source address register 5	DMAC1_N0SA_5_N	32	32
A006 3140h	DMA1	Next 0 source address register 5	DMAC1_N0SA_5_W	32	32
A006 3144h	DMA1	Next 0 destination address register 5	DMAC1_N0DA_5	32	32
A006 3148h	DMA1	Next 0 transaction byte register 5	DMAC1_N0TB_5	32	32
A006 314Ch	DMA1	Next 1 source address register 5	DMAC1_N1SA_5_N	32	32
A006 314Ch	DMA1	Next 1 source address register 5	DMAC1_N1SA_5_W	32	32
A006 3150h	DMA1	Next 1 destination address register 5	DMAC1_N1DA_5	32	32
A006 3154h	DMA1	Next 1 transaction byte register 5	DMAC1_N1TB_5	32	32
A006 3158h	DMA1	Current source address register 5	DMAC1_CRSA_5	32	32
A006 315Ch	DMA1	Current destination address register 5	DMAC1_CRDA_5	32	32
A006 3160h	DMA1	Current transaction byte register 5	DMAC1_CRTB_5	32	32
A006 3164h	DMA1	Channel status register 5	DMAC1_CHSTAT_5	32	32
A006 3168h	DMA1	Channel control register 5	DMAC1_CHCTRL_5	32	32
A006 316Ch	DMA1	Channel configuration register 5	DMAC1_CHCFG_5	32	32
A006 3170h	DMA1	Channel interval register 5	DMAC1_CHITVL_5	32	32
A006 3178h	DMA1	Next link address register 5	DMAC1_NXLA_5	32	32
A006 317Ch	DMA1	Current link address register 5	DMAC1_CRLA_5	32	32
A006 3180h	DMA1	Next 0 source address register 6	DMAC1_N0SA_6_N	32	32
A006 3180h	DMA1	Next 0 source address register 6	DMAC1_N0SA_6_W	32	32
A006 3184h	DMA1	Next 0 destination address register 6	DMAC1_N0DA_6	32	32
A006 3188h	DMA1	Next 0 transaction byte register 6	DMAC1_N0TB_6	32	32
A006 318Ch	DMA1	Next 1 source address register 6	DMAC1_N1SA_6_N	32	32
A006 318Ch	DMA1	Next 1 source address register 6	DMAC1_N1SA_6_W	32	32
A006 3190h	DMA1	Next 1 destination address register 6	DMAC1_N1DA_6	32	32
A006 3194h	DMA1	Next 1 transaction byte register 6	DMAC1_N1TB_6	32	32
A006 3198h	DMA1	Current source address register 6	DMAC1_CRSA_6	32	32
A006 319Ch	DMA1	Current destination address register 6	DMAC1_CRDA_6	32	32
A006 31A0h	DMA1	Current transaction byte register 6	DMAC1_CRTB_6	32	32
A006 31A4h	DMA1	Channel status register 6	DMAC1_CHSTAT_6	32	32
A006 31A8h	DMA1	Channel control register 6	DMAC1_CHCTRL_6	32	32
A006 31ACh	DMA1	Channel configuration register 6	DMAC1_CHCFG_6	32	32
A006 31B0h	DMA1	Channel interval register 6	DMAC1_CHITVL_6	32	32
A006 31B8h	DMA1	Next link address register 6	DMAC1_NXLA_6	32	32
A006 31BCh	DMA1	Current link address register 6	DMAC1_CRLA_6	32	32
A006 31C0h	DMA1	Next 0 source address register 7	DMAC1_N0SA_7_N	32	32
A006 31C0h	DMA1	Next 0 source address register 7	DMAC1_N0SA_7_W	32	32
A006 31C4h	DMA1	Next 0 destination address register 7	DMAC1_N0DA_7	32	32
A006 31C8h	DMA1	Next 0 transaction byte register 7	DMAC1_N0TB_7	32	32
A006 31CCh	DMA1	Next 1 source address register 7	DMAC1_N1SA_7_N	32	32
A006 31CCh	DMA1	Next 1 source address register 7	DMAC1_N1SA_7_W	32	32
A006 31D0h	DMA1	Next 1 destination address register 7	DMAC1_N1DA_7	32	32

Table 5.1 List of I/O Registers (Address Order) (37 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 31D4h	DMA1	Next 1 transaction byte register 7	DMAC1_N1TB_7	32	32
A006 31D8h	DMA1	Current source address register 7	DMAC1_CRSA_7	32	32
A006 31DCh	DMA1	Current destination address register 7	DMAC1_CRDA_7	32	32
A006 31E0h	DMA1	Current transaction byte register 7	DMAC1_CRTB_7	32	32
A006 31E4h	DMA1	Channel status register 7	DMAC1_CHSTAT_7	32	32
A006 31E8h	DMA1	Channel control register 7	DMAC1_CHCTRL_7	32	32
A006 31ECh	DMA1	Channel configuration register 7	DMAC1_CHCFG_7	32	32
A006 31F0h	DMA1	Channel interval register 7	DMAC1_CHITVL_7	32	32
A006 31F8h	DMA1	Next link address register 7	DMAC1_NXLA_7	32	32
A006 31FCh	DMA1	Current link address register 7	DMAC1_CRLA_7	32	32
A006 3200h	DMA1	Source continuous register 0	DMAC1_SCNT_0	32	32
A006 3204h	DMA1	Source skip register 0	DMAC1_SSKP_0	32	32
A006 3208h	DMA1	Destination continuous register 0	DMAC1_DCNT_0	32	32
A006 320Ch	DMA1	Destination skip register 0	DMAC1_DSKP_0	32	32
A006 3220h	DMA1	Source continuous register 1	DMAC1_SCNT_1	32	32
A006 3224h	DMA1	Source skip register 1	DMAC1_SSKP_1	32	32
A006 3228h	DMA1	Destination continuous register 1	DMAC1_DCNT_1	32	32
A006 322Ch	DMA1	Destination skip register 1	DMAC1_DSKP_1	32	32
A006 3240h	DMA1	Source continuous register 2	DMAC1_SCNT_2	32	32
A006 3244h	DMA1	Source skip register 2	DMAC1_SSKP_2	32	32
A006 3248h	DMA1	Destination continuous register 2	DMAC1_DCNT_2	32	32
A006 324Ch	DMA1	Destination skip register 2	DMAC1_DSKP_2	32	32
A006 3260h	DMA1	Source continuous register 3	DMAC1_SCNT_3	32	32
A006 3264h	DMA1	Source skip register 3	DMAC1_SSKP_3	32	32
A006 3268h	DMA1	Destination continuous register 3	DMAC1_DCNT_3	32	32
A006 326Ch	DMA1	Destination skip register 3	DMAC1_DSKP_3	32	32
A006 3280h	DMA1	Source continuous register 4	DMAC1_SCNT_4	32	32
A006 3284h	DMA1	Source skip register 4	DMAC1_SSKP_4	32	32
A006 3288h	DMA1	Destination continuous register 4	DMAC1_DCNT_4	32	32
A006 328Ch	DMA1	Destination skip register 4	DMAC1_DSKP_4	32	32
A006 32A0h	DMA1	Source continuous register 5	DMAC1_SCNT_5	32	32
A006 32A4h	DMA1	Source skip register 5	DMAC1_SSKP_5	32	32
A006 32A8h	DMA1	Destination continuous register 5	DMAC1_DCNT_5	32	32
A006 32ACh	DMA1	Destination skip register 5	DMAC1_DSKP_5	32	32
A006 32C0h	DMA1	Source continuous register 6	DMAC1_SCNT_6	32	32
A006 32C4h	DMA1	Source skip register 6	DMAC1_SSKP_6	32	32
A006 32C8h	DMA1	Destination continuous register 6	DMAC1_DCNT_6	32	32
A006 32CCh	DMA1	Destination skip register 6	DMAC1_DSKP_6	32	32
A006 32E0h	DMA1	Source continuous register 7	DMAC1_SCNT_7	32	32
A006 32E4h	DMA1	Source skip register 7	DMAC1_SSKP_7	32	32
A006 32E8h	DMA1	Destination continuous register 7	DMAC1_DCNT_7	32	32
A006 32ECh	DMA1	Destination skip register 7	DMAC1_DSKP_7	32	32
A006 3300h	DMA1	DMA control register A	DMAC1_DCTRL_A	32	32
A006 3304h	DMA1	Descriptor interval register A	DMAC1_DSCITVL_A	32	32
A006 3310h	DMA1	DMA status EN register A	DMAC1_DST_EN_A	32	32
A006 3314h	DMA1	DMA status ER register A	DMAC1_DST_ER_A	32	32
A006 3318h	DMA1	DMA status END register A	DMAC1_DST_END_A	32	32
A006 3320h	DMA1	DMA status SUS register A	DMAC1_DST_SUS_A	32	32

Table 5.1 List of I/O Registers (Address Order) (38 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 3400h	DMA1	Next 0 source address register 8	DMAC1_N0SA_8_N	32	32
A006 3400h	DMA1	Next 0 source address register 8	DMAC1_N0SA_8_W	32	32
A006 3404h	DMA1	Next 0 destination address register 8	DMAC1_N0DA_8	32	32
A006 3408h	DMA1	Next 0 transaction byte register 8	DMAC1_N0TB_8	32	32
A006 340Ch	DMA1	Next 1 source address register 8	DMAC1_N1SA_8_N	32	32
A006 340Ch	DMA1	Next 1 source address register 8	DMAC1_N1SA_8_W	32	32
A006 3410h	DMA1	Next 1 destination address register 8	DMAC1_N1DA_8	32	32
A006 3414h	DMA1	Next 1 transaction byte register 8	DMAC1_N1TB_8	32	32
A006 3418h	DMA1	Current source address register 8	DMAC1_CRSA_8	32	32
A006 341Ch	DMA1	Current destination address register 8	DMAC1_CRDA_8	32	32
A006 3420h	DMA1	Current transaction byte register 8	DMAC1_CRTB_8	32	32
A006 3424h	DMA1	Channel status register 8	DMAC1_CHSTAT_8	32	32
A006 3428h	DMA1	Channel control register 8	DMAC1_CHCTRL_8	32	32
A006 342Ch	DMA1	Channel configuration register 8	DMAC1_CHCFG_8	32	32
A006 3430h	DMA1	Channel interval register 8	DMAC1_CHITVL_8	32	32
A006 3438h	DMA1	Next link address register 8	DMAC1_NXLA_8	32	32
A006 343Ch	DMA1	Current link address register 8	DMAC1_CRLA_8	32	32
A006 3440h	DMA1	Next 0 source address register 9	DMAC1_N0SA_9_N	32	32
A006 3440h	DMA1	Next 0 source address register 9	DMAC1_N0SA_9_W	32	32
A006 3444h	DMA1	Next 0 destination address register 9	DMAC1_N0DA_9	32	32
A006 3448h	DMA1	Next 0 transaction byte register 9	DMAC1_N0TB_9	32	32
A006 344Ch	DMA1	Next 1 source address register 9	DMAC1_N1SA_9_N	32	32
A006 344Ch	DMA1	Next 1 source address register 9	DMAC1_N1SA_9_W	32	32
A006 3450h	DMA1	Next 1 destination address register 9	DMAC1_N1DA_9	32	32
A006 3454h	DMA1	Next 1 transaction byte register 9	DMAC1_N1TB_9	32	32
A006 3458h	DMA1	Current source address register 9	DMAC1_CRSA_9	32	32
A006 345Ch	DMA1	Current destination address register 9	DMAC1_CRDA_9	32	32
A006 3460h	DMA1	Current transaction byte register 9	DMAC1_CRTB_9	32	32
A006 3464h	DMA1	Channel status register 9	DMAC1_CHSTAT_9	32	32
A006 3468h	DMA1	Channel control register 9	DMAC1_CHCTRL_9	32	32
A006 346Ch	DMA1	Channel configuration register 9	DMAC1_CHCFG_9	32	32
A006 3470h	DMA1	Channel interval register 9	DMAC1_CHITVL_9	32	32
A006 3478h	DMA1	Next link address register 9	DMAC1_NXLA_9	32	32
A006 347Ch	DMA1	Current link address register 9	DMAC1_CRLA_9	32	32
A006 3480h	DMA1	Next 0 source address register 10	DMAC1_N0SA_10_N	32	32
A006 3480h	DMA1	Next 0 source address register 10	DMAC1_N0SA_10_W	32	32
A006 3484h	DMA1	Next 0 destination address register 10	DMAC1_N0DA_10	32	32
A006 3488h	DMA1	Next 0 transaction byte register 10	DMAC1_N0TB_10	32	32
A006 348Ch	DMA1	Next 1 source address register 10	DMAC1_N1SA_10_N	32	32
A006 348Ch	DMA1	Next 1 source address register 10	DMAC1_N1SA_10_W	32	32
A006 3490h	DMA1	Next 1 destination address register 10	DMAC1_N1DA_10	32	32
A006 3494h	DMA1	Next 1 transaction byte register 10	DMAC1_N1TB_10	32	32
A006 3498h	DMA1	Current source address register 10	DMAC1_CRSA_10	32	32
A006 349Ch	DMA1	Current destination address register 10	DMAC1_CRDA_10	32	32
A006 34A0h	DMA1	Current transaction byte register 10	DMAC1_CRTB_10	32	32
A006 34A4h	DMA1	Channel status register 10	DMAC1_CHSTAT_10	32	32
A006 34A8h	DMA1	Channel control register 10	DMAC1_CHCTRL_10	32	32
A006 34ACh	DMA1	Channel configuration register 10	DMAC1_CHCFG_10	32	32

Table 5.1 List of I/O Registers (Address Order) (39 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 34B0h	DMA1	Channel interval register 10	DMAC1_CHITVL_10	32	32
A006 34B8h	DMA1	Next link address register 10	DMAC1_NXLA_10	32	32
A006 34BCh	DMA1	Current link address register 10	DMAC1_CRLA_10	32	32
A006 34C0h	DMA1	Next 0 source address register 11	DMAC1_N0SA_11_N	32	32
A006 34C0h	DMA1	Next 0 source address register 11	DMAC1_N0SA_11_W	32	32
A006 34C4h	DMA1	Next 0 destination address register 11	DMAC1_N0DA_11	32	32
A006 34C8h	DMA1	Next 0 transaction byte register 11	DMAC1_N0TB_11	32	32
A006 34CCh	DMA1	Next 1 source address register 11	DMAC1_N1SA_11_N	32	32
A006 34CCh	DMA1	Next 1 source address register 11	DMAC1_N1SA_11_W	32	32
A006 34D0h	DMA1	Next 1 destination address register 11	DMAC1_N1DA_11	32	32
A006 34D4h	DMA1	Next 1 transaction byte register 11	DMAC1_N1TB_11	32	32
A006 34D8h	DMA1	Current source address register 11	DMAC1_CRSA_11	32	32
A006 34DCh	DMA1	Current destination address register 11	DMAC1_CRDA_11	32	32
A006 34E0h	DMA1	Current transaction byte register 11	DMAC1_CRTB_11	32	32
A006 34E4h	DMA1	Channel status register 11	DMAC1_CHSTAT_11	32	32
A006 34E8h	DMA1	Channel control register 11	DMAC1_CHCTRL_11	32	32
A006 34ECh	DMA1	Channel configuration register 11	DMAC1_CHCFG_11	32	32
A006 34F0h	DMA1	Channel interval register 11	DMAC1_CHITVL_11	32	32
A006 34F8h	DMA1	Next link address register 11	DMAC1_NXLA_11	32	32
A006 34FCh	DMA1	Current link address register 11	DMAC1_CRLA_11	32	32
A006 3500h	DMA1	Next 0 source address register 12	DMAC1_N0SA_12_N	32	32
A006 3500h	DMA1	Next 0 source address register 12	DMAC1_N0SA_12_W	32	32
A006 3504h	DMA1	Next 0 destination address register 12	DMAC1_N0DA_12	32	32
A006 3508h	DMA1	Next 0 transaction byte register 12	DMAC1_N0TB_12	32	32
A006 350Ch	DMA1	Next 1 source address register 12	DMAC1_N1SA_12_N	32	32
A006 350Ch	DMA1	Next 1 source address register 12	DMAC1_N1SA_12_W	32	32
A006 3510h	DMA1	Next 1 destination address register 12	DMAC1_N1DA_12	32	32
A006 3514h	DMA1	Next 1 transaction byte register 12	DMAC1_N1TB_12	32	32
A006 3518h	DMA1	Current source address register 12	DMAC1_CRSA_12	32	32
A006 351Ch	DMA1	Current destination address register 12	DMAC1_CRDA_12	32	32
A006 3520h	DMA1	Current transaction byte register 12	DMAC1_CRTB_12	32	32
A006 3524h	DMA1	Channel status register 12	DMAC1_CHSTAT_12	32	32
A006 3528h	DMA1	Channel control register 12	DMAC1_CHCTRL_12	32	32
A006 352Ch	DMA1	Channel configuration register 12	DMAC1_CHCFG_12	32	32
A006 3530h	DMA1	Channel interval register 12	DMAC1_CHITVL_12	32	32
A006 3538h	DMA1	Next link address register 12	DMAC1_NXLA_12	32	32
A006 353Ch	DMA1	Current link address register 12	DMAC1_CRLA_12	32	32
A006 3540h	DMA1	Next 0 source address register 13	DMAC1_N0SA_13_N	32	32
A006 3540h	DMA1	Next 0 source address register 13	DMAC1_N0SA_13_W	32	32
A006 3544h	DMA1	Next 0 destination address register 13	DMAC1_N0DA_13	32	32
A006 3548h	DMA1	Next 0 transaction byte register 13	DMAC1_N0TB_13	32	32
A006 354Ch	DMA1	Next 1 source address register 13	DMAC1_N1SA_13_N	32	32
A006 354Ch	DMA1	Next 1 source address register 13	DMAC1_N1SA_13_W	32	32
A006 3550h	DMA1	Next 1 destination address register 13	DMAC1_N1DA_13	32	32
A006 3554h	DMA1	Next 1 transaction byte register 13	DMAC1_N1TB_13	32	32
A006 3558h	DMA1	Current source address register 13	DMAC1_CRSA_13	32	32
A006 355Ch	DMA1	Current destination address register 13	DMAC1_CRDA_13	32	32
A006 3560h	DMA1	Current transaction byte register 13	DMAC1_CRTB_13	32	32

Table 5.1 List of I/O Registers (Address Order) (40 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 3564h	DMA1	Channel status register 13	DMAC1_CHSTAT_13	32	32
A006 3568h	DMA1	Channel control register 13	DMAC1_CHCTRL_13	32	32
A006 356Ch	DMA1	Channel configuration register 13	DMAC1_CHCFG_13	32	32
A006 3570h	DMA1	Channel interval register 13	DMAC1_CHITVL_13	32	32
A006 3578h	DMA1	Next link address register 13	DMAC1_NXLA_13	32	32
A006 357Ch	DMA1	Current link address register 13	DMAC1_CRLA_13	32	32
A006 3580h	DMA1	Next 0 source address register 14	DMAC1_N0SA_14_N	32	32
A006 3580h	DMA1	Next 0 source address register 14	DMAC1_N0SA_14_W	32	32
A006 3584h	DMA1	Next 0 destination address register 14	DMAC1_N0DA_14	32	32
A006 3588h	DMA1	Next 0 transaction byte register 14	DMAC1_N0TB_14	32	32
A006 358Ch	DMA1	Next 1 source address register 14	DMAC1_N1SA_14_N	32	32
A006 358Ch	DMA1	Next 1 source address register 14	DMAC1_N1SA_14_W	32	32
A006 3590h	DMA1	Next 1 destination address register 14	DMAC1_N1DA_14	32	32
A006 3594h	DMA1	Next 1 transaction byte register 14	DMAC1_N1TB_14	32	32
A006 3598h	DMA1	Current source address register 14	DMAC1_CRSA_14	32	32
A006 359Ch	DMA1	Current destination address register 14	DMAC1_CRDA_14	32	32
A006 35A0h	DMA1	Current transaction byte register 14	DMAC1_CRTB_14	32	32
A006 35A4h	DMA1	Channel status register 14	DMAC1_CHSTAT_14	32	32
A006 35A8h	DMA1	Channel control register 14	DMAC1_CHCTRL_14	32	32
A006 35ACh	DMA1	Channel configuration register 14	DMAC1_CHCFG_14	32	32
A006 35B0h	DMA1	Channel interval register 14	DMAC1_CHITVL_14	32	32
A006 35B8h	DMA1	Next link address register 14	DMAC1_NXLA_14	32	32
A006 35BCh	DMA1	Current link address register 14	DMAC1_CRLA_14	32	32
A006 35C0h	DMA1	Next 0 source address register 15	DMAC1_N0SA_15_N	32	32
A006 35C0h	DMA1	Next 0 source address register 15	DMAC1_N0SA_15_W	32	32
A006 35C4h	DMA1	Next 0 destination address register 15	DMAC1_N0DA_15	32	32
A006 35C8h	DMA1	Next 0 transaction byte register 15	DMAC1_N0TB_15	32	32
A006 35CCh	DMA1	Next 1 source address register 15	DMAC1_N1SA_15_N	32	32
A006 35CCh	DMA1	Next 1 source address register 15	DMAC1_N1SA_15_W	32	32
A006 35D0h	DMA1	Next 1 destination address register 15	DMAC1_N1DA_15	32	32
A006 35D4h	DMA1	Next 1 transaction byte register 15	DMAC1_N1TB_15	32	32
A006 35D8h	DMA1	Current source address register 15	DMAC1_CRSA_15	32	32
A006 35DCh	DMA1	Current destination address register 15	DMAC1_CRDA_15	32	32
A006 35E0h	DMA1	Current transaction byte register 15	DMAC1_CRTB_15	32	32
A006 35E4h	DMA1	Channel status register 15	DMAC1_CHSTAT_15	32	32
A006 35E8h	DMA1	Channel control register 15	DMAC1_CHCTRL_15	32	32
A006 35ECh	DMA1	Channel configuration register 15	DMAC1_CHCFG_15	32	32
A006 35F0h	DMA1	Channel interval register 15	DMAC1_CHITVL_15	32	32
A006 35F8h	DMA1	Next link address register 15	DMAC1_NXLA_15	32	32
A006 35FCh	DMA1	Current link address register 15	DMAC1_CRLA_15	32	32
A006 3600h	DMA1	Source continuous register 8	DMAC1_SCNT_8	32	32
A006 3604h	DMA1	Source skip register 8	DMAC1_SSKP_8	32	32
A006 3608h	DMA1	Destination continuous register 8	DMAC1_DCNT_8	32	32
A006 360Ch	DMA1	Destination skip register 8	DMAC1_DSKP_8	32	32
A006 3620h	DMA1	Source continuous register 9	DMAC1_SCNT_9	32	32
A006 3624h	DMA1	Source skip register 9	DMAC1_SSKP_9	32	32
A006 3628h	DMA1	Destination continuous register 9	DMAC1_DCNT_9	32	32
A006 362Ch	DMA1	Destination skip register 9	DMAC1_DSKP_9	32	32

Table 5.1 List of I/O Registers (Address Order) (41 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 3640h	DMA1	Source continuous register 10	DMAC1_SCNT_10	32	32
A006 3644h	DMA1	Source skip register 10	DMAC1_SSKP_10	32	32
A006 3648h	DMA1	Destination continuous register 10	DMAC1_DCNT_10	32	32
A006 364Ch	DMA1	Destination skip register 10	DMAC1_DSKP_10	32	32
A006 3660h	DMA1	Source continuous register 11	DMAC1_SCNT_11	32	32
A006 3664h	DMA1	Source skip register 11	DMAC1_SSKP_11	32	32
A006 3668h	DMA1	Destination continuous register 11	DMAC1_DCNT_11	32	32
A006 366Ch	DMA1	Destination skip register 11	DMAC1_DSKP_11	32	32
A006 3680h	DMA1	Source continuous register 12	DMAC1_SCNT_12	32	32
A006 3684h	DMA1	Source skip register 12	DMAC1_SSKP_12	32	32
A006 3688h	DMA1	Destination continuous register 12	DMAC1_DCNT_12	32	32
A006 368Ch	DMA1	Destination skip register 12	DMAC1_DSKP_12	32	32
A006 36A0h	DMA1	Source continuous register 13	DMAC1_SCNT_13	32	32
A006 36A4h	DMA1	Source skip register 13	DMAC1_SSKP_13	32	32
A006 36A8h	DMA1	Destination continuous register 13	DMAC1_DCNT_13	32	32
A006 36ACh	DMA1	Destination skip register 13	DMAC1_DSKP_13	32	32
A006 36C0h	DMA1	Source continuous register 14	DMAC1_SCNT_14	32	32
A006 36C4h	DMA1	Source skip register 14	DMAC1_SSKP_14	32	32
A006 36C8h	DMA1	Destination continuous register 14	DMAC1_DCNT_14	32	32
A006 36CCh	DMA1	Destination skip register 14	DMAC1_DSKP_14	32	32
A006 36E0h	DMA1	Source continuous register 15	DMAC1_SCNT_15	32	32
A006 36E4h	DMA1	Source skip register 15	DMAC1_SSKP_15	32	32
A006 36E8h	DMA1	Destination continuous register 15	DMAC1_DCNT_15	32	32
A006 36ECh	DMA1	Destination skip register 15	DMAC1_DSKP_15	32	32
A006 3700h	DMA1	DMA control register B	DMAC1_DCTRL_B	32	32
A006 3704h	DMA1	Descriptor interval register B	DMAC1_DSCITVL_B	32	32
A006 3710h	DMA1	DMA status EN register B	DMAC1_DST_EN_B	32	32
A006 3714h	DMA1	DMA status ER register B	DMAC1_DST_ER_B	32	32
A006 3718h	DMA1	DMA status END register B	DMAC1_DST_END_B	32	32
A006 3720h	DMA1	DMA status SUS register B	DMAC1_DST_SUS_B	32	32
A006 5000h	SCIFA0	Serial mode register	SMR	16	16
A006 5002h	SCIFA0	Bit rate register	BRR	8	8
A006 5002h	SCIFA0	Modulation duty register	MDDR	8	8
A006 5004h	SCIFA0	Serial control register	SCR	16	16
A006 5006h	SCIFA0	Transmit FIFO data register	FTDR	8	8
A006 5008h	SCIFA0	Serial status register	FSR	16	16
A006 500Ah	SCIFA0	Receive FIFO data register	FRDR	8	8
A006 500Ch	SCIFA0	FIFO control register	FCR	16	16
A006 500Eh	SCIFA0	FIFO data count register	FDR	16	16
A006 5010h	SCIFA0	Serial port register	SPTR	16	16
A006 5012h	SCIFA0	Line status register	LSR	16	16
A006 5014h	SCIFA0	Serial extended mode register	SEMR	8	8
A006 5016h	SCIFA0	FIFO trigger control register	FTCR	16	16
A006 5400h	SCIFA1	Serial mode register	SMR	16	16
A006 5402h	SCIFA1	Bit rate register	BRR	8	8
A006 5402h	SCIFA1	Modulation duty register	MDDR	8	8
A006 5404h	SCIFA1	Serial control register	SCR	16	16
A006 5406h	SCIFA1	Transmit FIFO data register	FTDR	8	8

Table 5.1 List of I/O Registers (Address Order) (42 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 5408h	SCIFA1	Serial status register	FSR	16	16
A006 540Ah	SCIFA1	Receive FIFO data register	FRDR	8	8
A006 540Ch	SCIFA1	FIFO control register	FCR	16	16
A006 540Eh	SCIFA1	FIFO data count register	FDR	16	16
A006 5410h	SCIFA1	Serial port register	SPTR	16	16
A006 5412h	SCIFA1	Line status register	LSR	16	16
A006 5414h	SCIFA1	Serial extended mode register	SEMR	8	8
A006 5416h	SCIFA1	FIFO trigger control register	FTCR	16	16
A006 5800h	SCIFA2	Serial mode register	SMR	16	16
A006 5802h	SCIFA2	Bit rate register	BRR	8	8
A006 5802h	SCIFA2	Modulation duty register	MDDR	8	8
A006 5804h	SCIFA2	Serial control register	SCR	16	16
A006 5806h	SCIFA2	Transmit FIFO data register	FTDR	8	8
A006 5808h	SCIFA2	Serial status register	FSR	16	16
A006 580Ah	SCIFA2	Receive FIFO data register	FRDR	8	8
A006 580Ch	SCIFA2	FIFO control register	FCR	16	16
A006 580Eh	SCIFA2	FIFO data count register	FDR	16	16
A006 5810h	SCIFA2	Serial port register	SPTR	16	16
A006 5812h	SCIFA2	Line status register	LSR	16	16
A006 5814h	SCIFA2	Serial extended mode register	SEMR	8	8
A006 5816h	SCIFA2	FIFO trigger control register	FTCR	16	16
A006 5C00h	SCIFA3	Serial mode register	SMR	16	16
A006 5C02h	SCIFA3	Bit rate register	BRR	8	8
A006 5C02h	SCIFA3	Modulation duty register	MDDR	8	8
A006 5C04h	SCIFA3	Serial control register	SCR	16	16
A006 5C06h	SCIFA3	Transmit FIFO data register	FTDR	8	8
A006 5C08h	SCIFA3	Serial status register	FSR	16	16
A006 5C0Ah	SCIFA3	Receive FIFO data register	FRDR	8	8
A006 5C0Ch	SCIFA3	FIFO control register	FCR	16	16
A006 5C0Eh	SCIFA3	FIFO data count register	FDR	16	16
A006 5C10h	SCIFA3	Serial port register	SPTR	16	16
A006 5C12h	SCIFA3	Line status register	LSR	16	16
A006 5C14h	SCIFA3	Serial extended mode register	SEMR	8	8
A006 5C16h	SCIFA3	FIFO trigger control register	FTCR	16	16
A006 6000h	SCIFA4	Serial mode register	SMR	16	16
A006 6002h	SCIFA4	Bit rate register	BRR	8	8
A006 6002h	SCIFA4	Modulation duty register	MDDR	8	8
A006 6004h	SCIFA4	Serial control register	SCR	16	16
A006 6006h	SCIFA4	Transmit FIFO data register	FTDR	8	8
A006 6008h	SCIFA4	Serial status register	FSR	16	16
A006 600Ah	SCIFA4	Receive FIFO data register	FRDR	8	8
A006 600Ch	SCIFA4	FIFO control register	FCR	16	16
A006 600Eh	SCIFA4	FIFO data count register	FDR	16	16
A006 6010h	SCIFA4	Serial port register	SPTR	16	16
A006 6012h	SCIFA4	Line status register	LSR	16	16
A006 6014h	SCIFA4	Serial extended mode register	SEMR	8	8
A006 6016h	SCIFA4	FIFO trigger control register	FTCR	16	16
A006 8000h	RSPI0	RSPI control register	SPCR	8	8

Table 5.1 List of I/O Registers (Address Order) (43 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 8001h	RSPI0	RSPI slave select polarity register	SSLP	8	8
A006 8002h	RSPI0	RSPI pin control register	SPPCR	8	8
A006 8003h	RSPI0	RSPI status register	SPSR	8	8
A006 8004h	RSPI0	RSPI data register	SPDR	32	16, 32
A006 8008h	RSPI0	RSPI sequence control register	SPSCR	8	8
A006 8009h	RSPI0	RSPI sequence status register	SPSSR	8	8
A006 800Ah	RSPI0	RSPI bit rate register	SPBR	8	8
A006 800Bh	RSPI0	RSPI data control register	SPDCR	8	8
A006 800Ch	RSPI0	RSPI clock delay register	SPCKD	8	8
A006 800Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8
A006 800Eh	RSPI0	RSPI next-access delay register	SPND	8	8
A006 800Fh	RSPI0	RSPI control register 2	SPCR2	8	8
A006 8010h	RSPI0	RSPI command register 0	SPCMD0	16	16
A006 8012h	RSPI0	RSPI command register 1	SPCMD1	16	16
A006 8014h	RSPI0	RSPI command register 2	SPCMD2	16	16
A006 8016h	RSPI0	RSPI command register 3	SPCMD3	16	16
A006 8018h	RSPI0	RSPI command register 4	SPCMD4	16	16
A006 801Ah	RSPI0	RSPI command register 5	SPCMD5	16	16
A006 801Ch	RSPI0	RSPI command register 6	SPCMD6	16	16
A006 801Eh	RSPI0	RSPI command register 7	SPCMD7	16	16
A006 8400h	RSPI1	RSPI control register	SPCR	8	8
A006 8401h	RSPI1	RSPI slave select polarity register	SSLP	8	8
A006 8402h	RSPI1	RSPI pin control register	SPPCR	8	8
A006 8403h	RSPI1	RSPI status register	SPSR	8	8
A006 8404h	RSPI1	RSPI data register	SPDR	32	16, 32
A006 8408h	RSPI1	RSPI sequence control register	SPSCR	8	8
A006 8409h	RSPI1	RSPI sequence status register	SPSSR	8	8
A006 840Ah	RSPI1	RSPI bit rate register	SPBR	8	8
A006 840Bh	RSPI1	RSPI data control register	SPDCR	8	8
A006 840Ch	RSPI1	RSPI clock delay register	SPCKD	8	8
A006 840Dh	RSPI1	RSPI slave select negation delay register	SSLND	8	8
A006 840Eh	RSPI1	RSPI next-access delay register	SPND	8	8
A006 840Fh	RSPI1	RSPI control register 2	SPCR2	8	8
A006 8410h	RSPI1	RSPI command register 0	SPCMD0	16	16
A006 8412h	RSPI1	RSPI command register 1	SPCMD1	16	16
A006 8414h	RSPI1	RSPI command register 2	SPCMD2	16	16
A006 8416h	RSPI1	RSPI command register 3	SPCMD3	16	16
A006 8418h	RSPI1	RSPI command register 4	SPCMD4	16	16
A006 841Ah	RSPI1	RSPI command register 5	SPCMD5	16	16
A006 841Ch	RSPI1	RSPI command register 6	SPCMD6	16	16
A006 841Eh	RSPI1	RSPI command register 7	SPCMD7	16	16
A006 8800h	RSPI2	RSPI control register	SPCR	8	8
A006 8801h	RSPI2	RSPI slave select polarity register	SSLP	8	8
A006 8802h	RSPI2	RSPI pin control register	SPPCR	8	8
A006 8803h	RSPI2	RSPI status register	SPSR	8	8
A006 8804h	RSPI2	RSPI data register	SPDR	32	16, 32
A006 8808h	RSPI2	RSPI sequence control register	SPSCR	8	8
A006 8809h	RSPI2	RSPI sequence status register	SPSSR	8	8

Table 5.1 List of I/O Registers (Address Order) (44 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 880Ah	RSPI2	RSPI bit rate register	SPBR	8	8
A006 880Bh	RSPI2	RSPI data control register	SPDCR	8	8
A006 880Ch	RSPI2	RSPI clock delay register	SPCKD	8	8
A006 880Dh	RSPI2	RSPI slave select negation delay register	SSLND	8	8
A006 880Eh	RSPI2	RSPI next-access delay register	SPND	8	8
A006 880Fh	RSPI2	RSPI control register 2	SPCR2	8	8
A006 8810h	RSPI2	RSPI command register 0	SPCMD0	16	16
A006 8812h	RSPI2	RSPI command register 1	SPCMD1	16	16
A006 8814h	RSPI2	RSPI command register 2	SPCMD2	16	16
A006 8816h	RSPI2	RSPI command register 3	SPCMD3	16	16
A006 8818h	RSPI2	RSPI command register 4	SPCMD4	16	16
A006 881Ah	RSPI2	RSPI command register 5	SPCMD5	16	16
A006 881Ch	RSPI2	RSPI command register 6	SPCMD6	16	16
A006 881Eh	RSPI2	RSPI command register 7	SPCMD7	16	16
A006 8C00h	RSPI3	RSPI control register	SPCR	8	8
A006 8C01h	RSPI3	RSPI slave select polarity register	SSLP	8	8
A006 8C02h	RSPI3	RSPI pin control register	SPPCR	8	8
A006 8C03h	RSPI3	RSPI status register	SPSR	8	8
A006 8C04h	RSPI3	RSPI data register	SPDR	32	16, 32
A006 8C08h	RSPI3	RSPI sequence control register	SPSCR	8	8
A006 8C09h	RSPI3	RSPI sequence status register	SPSSR	8	8
A006 8C0Ah	RSPI3	RSPI bit rate register	SPBR	8	8
A006 8C0Bh	RSPI3	RSPI data control register	SPDCR	8	8
A006 8C0Ch	RSPI3	RSPI clock delay register	SPCKD	8	8
A006 8C0Dh	RSPI3	RSPI slave select negation delay register	SSLND	8	8
A006 8C0Eh	RSPI3	RSPI next-access delay register	SPND	8	8
A006 8C0Fh	RSPI3	RSPI control register 2	SPCR2	8	8
A006 8C10h	RSPI3	RSPI command register 0	SPCMD0	16	16
A006 8C12h	RSPI3	RSPI command register 1	SPCMD1	16	16
A006 8C14h	RSPI3	RSPI command register 2	SPCMD2	16	16
A006 8C16h	RSPI3	RSPI command register 3	SPCMD3	16	16
A006 8C18h	RSPI3	RSPI command register 4	SPCMD4	16	16
A006 8C1Ah	RSPI3	RSPI command register 5	SPCMD5	16	16
A006 8C1Ch	RSPI3	RSPI command register 6	SPCMD6	16	16
A006 8C1Eh	RSPI3	RSPI command register 7	SPCMD7	16	16
A006 A000h	MTU3	Timer control register	TCR	8	8
A006 A001h	MTU4	Timer control register	TCR	8	8
A006 A002h	MTU3	Timer mode register 1	TMDR1	8	8
A006 A003h	MTU4	Timer mode register 1	TMDR1	8	8
A006 A004h	MTU3	Timer I/O control register H	TIORH	8	8
A006 A005h	MTU3	Timer I/O control register L	TIORL	8	8
A006 A006h	MTU4	Timer I/O control register H	TIORH	8	8
A006 A007h	MTU4	Timer I/O control register L	TIORL	8	8
A006 A008h	MTU3	Timer interrupt enable register	TIER	8	8
A006 A009h	MTU4	Timer interrupt enable register	TIER	8	8
A006 A00Ah	MTU	Timer output master enable register A	TOERA	8	8
A006 A00Dh	MTU	Timer gate control register A	TGCRA	8	8
A006 A00Eh	MTU	Timer output control register 1A	TOCR1A	8	8

Table 5.1 List of I/O Registers (Address Order) (45 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 A00Fh	MTU	Timer output control register 2A	TOCR2A	8	8
A006 A010h	MTU3	Timer counter	TCNT	16	16
A006 A012h	MTU4	Timer counter	TCNT	16	16
A006 A014h	MTU	Timer cycle data register A	TCDRA	16	16
A006 A016h	MTU	Timer dead time data register A	TDDRA	16	16
A006 A018h	MTU3	Timer general register A	TGRA	16	16
A006 A01Ah	MTU3	Timer general register B	TGRB	16	16
A006 A01Ch	MTU4	Timer general register A	TGRA	16	16
A006 A01Eh	MTU4	Timer general register B	TGRB	16	16
A006 A020h	MTU	Timer subcounter A	TCNTSA	16	16
A006 A022h	MTU	Timer cycle buffer register A	TCBRA	16	16
A006 A024h	MTU3	Timer general register C	TGRC	16	16
A006 A026h	MTU3	Timer general register D	TGRD	16	16
A006 A028h	MTU4	Timer general register C	TGRC	16	16
A006 A02Ah	MTU4	Timer general register D	TGRD	16	16
A006 A02Ch	MTU3	Timer status register	TSR	8	8
A006 A02Dh	MTU4	Timer status register	TSR	8	8
A006 A030h	MTU	Timer interrupt skipping set register 1A	TITCR1A	8	8
A006 A031h	MTU	Timer interrupt skipping counter 1A	TITCNT1A	8	8
A006 A032h	MTU	Timer buffer transfer set register A	TBTERA	8	8
A006 A034h	MTU	Timer dead time enable register A	TDERA	8	8
A006 A036h	MTU	Timer output level buffer register A	TOLBRA	8	8
A006 A038h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8
A006 A039h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8
A006 A03Ah	MTU	Timer interrupt skipping mode register A	TITMRA	8	8
A006 A03Bh	MTU	Timer interrupt skipping set register 2A	TITCR2A	8	8
A006 A03Ch	MTU	Timer interrupt skipping counter 2A	TITCNT2A	8	8
A006 A040h	MTU4	Timer A/D converter start request control register	TADCR	16	16
A006 A044h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16
A006 A046h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16
A006 A048h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16
A006 A04Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16
A006 A04Ch	MTU3	Timer control register 2	TCR2	8	8
A006 A04Dh	MTU4	Timer control register 2	TCR2	8	8
A006 A060h	MTU	Timer waveform control register A	TWCRA	8	8
A006 A070h	MTU	Timer mode register 2A	TMDR2A	8	8
A006 A072h	MTU3	Timer general register E	TGRE	16	16
A006 A074h	MTU4	Timer general register E	TGRE	16	16
A006 A076h	MTU4	Timer general register F	TGRF	16	16
A006 A080h	MTU	Timer start register A	TSTRA	8	8
A006 A081h	MTU	Timer synchronous register A	TSYRA	8	8
A006 A082h	MTU	Timer counter synchronous start register	TCSYSTR	8	8
A006 A084h	MTU	Timer read/write enable register A	TRWERA	8	8
A006 A090h	MTU0	Noise filter control register	NFCR0	8	8
A006 A091h	MTU1	Noise filter control register	NFCR1	8	8
A006 A092h	MTU2	Noise filter control register	NFCR2	8	8
A006 A093h	MTU3	Noise filter control register	NFCR3	8	8
A006 A094h	MTU4	Noise filter control register	NFCR4	8	8

Table 5.1 List of I/O Registers (Address Order) (46 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 A098h	MTU8	Noise filter control register	NFCR8	8	8
A006 A099h	MTU0	Noise filter control register	NFCRC	8	8
A006 A100h	MTU0	Timer control register	TCR	8	8
A006 A101h	MTU0	Timer mode register 1	TMDR1	8	8
A006 A102h	MTU0	Timer I/O control register H	TIORH	8	8
A006 A103h	MTU0	Timer I/O control register L	TIORL	8	8
A006 A104h	MTU0	Timer interrupt enable register	TIER	8	8
A006 A106h	MTU0	Timer counter	TCNT	16	16
A006 A108h	MTU0	Timer general register A	TGRA	16	16
A006 A10Ah	MTU0	Timer general register B	TGRB	16	16
A006 A10Ch	MTU0	Timer general register C	TGRC	16	16
A006 A10Eh	MTU0	Timer general register D	TGRD	16	16
A006 A120h	MTU0	Timer general register E	TGRE	16	16
A006 A122h	MTU0	Timer general register F	TGRF	16	16
A006 A124h	MTU0	Timer interrupt enable register 2	TIER2	8	8
A006 A126h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8
A006 A128h	MTU0	Timer control register 2	TCR2	8	8
A006 A180h	MTU1	Timer control register	TCR	8	8
A006 A181h	MTU1	Timer mode register 1	TMDR1	8	8
A006 A182h	MTU1	Timer I/O control register	TIOR	8	8
A006 A184h	MTU1	Timer interrupt enable register	TIER	8	8
A006 A185h	MTU1	Timer status register	TSR	8	8
A006 A186h	MTU1	Timer counter	TCNT	16	16
A006 A188h	MTU1	Timer general register A	TGRA	16	16
A006 A18Ah	MTU1	Timer general register B	TGRB	16	16
A006 A190h	MTU1	Timer input capture control register	TICCR	8	8
A006 A191h	MTU1	Timer mode register 3	TMDR3	8	8
A006 A194h	MTU1	Timer control register 2	TCR2	8	8
A006 A1A0h	MTU1	Timer longword counter	TCNTLW	32	32
A006 A1A4h	MTU1	Timer longword general register A	TGRALW	32	32
A006 A1A8h	MTU1	Timer longword general register B	TGRBLW	32	32
A006 A200h	MTU2	Timer control register	TCR	8	8
A006 A201h	MTU2	Timer mode register 1	TMDR1	8	8
A006 A202h	MTU2	Timer I/O control register	TIOR	8	8
A006 A204h	MTU2	Timer interrupt enable register	TIER	8	8
A006 A205h	MTU2	Timer status register	TSR	8	8
A006 A206h	MTU2	Timer counter	TCNT	16	16
A006 A208h	MTU2	Timer general register A	TGRA	16	16
A006 A20Ah	MTU2	Timer general register B	TGRB	16	16
A006 A20Ch	MTU2	Timer control register 2	TCR2	8	8
A006 A400h	MTU8	Timer control register	TCR	8	8
A006 A401h	MTU8	Timer mode register 1	TMDR1	8	8
A006 A402h	MTU8	Timer I/O control register H	TIORH	8	8
A006 A403h	MTU8	Timer I/O control register L	TIORL	8	8
A006 A404h	MTU8	Timer interrupt enable register	TIER	8	8
A006 A406h	MTU8	Timer control register 2	TCR2	8	8
A006 A408h	MTU8	Timer counter	TCNT	32	32
A006 A40Ch	MTU8	Timer general register A	TGRA	32	32

Table 5.1 List of I/O Registers (Address Order) (47 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 A410h	MTU8	Timer general register B	TGRB	32	32
A006 A414h	MTU8	Timer general register C	TGRC	32	32
A006 A418h	MTU8	Timer general register D	TGRD	32	32
A006 A800h	MTU6	Timer control register	TCR	8	8
A006 A801h	MTU7	Timer control register	TCR	8	8
A006 A802h	MTU6	Timer mode register 1	TMDR1	8	8
A006 A803h	MTU7	Timer mode register 1	TMDR1	8	8
A006 A804h	MTU6	Timer I/O control register H	TIORH	8	8
A006 A805h	MTU6	Timer I/O control register L	TIORL	8	8
A006 A806h	MTU7	Timer I/O control register H	TIORH	8	8
A006 A807h	MTU7	Timer I/O control register L	TIORL	8	8
A006 A808h	MTU6	Timer interrupt enable register	TIER	8	8
A006 A809h	MTU7	Timer interrupt enable register	TIER	8	8
A006 A80Ah	MTU	Timer output master enable register B	TOERB	8	8
A006 A80Eh	MTU	Timer output control register 1B	TOCR1B	8	8
A006 A80Fh	MTU	Timer output control register 2B	TOCR2B	8	8
A006 A810h	MTU6	Timer counter	TCNT	16	16
A006 A812h	MTU7	Timer counter	TCNT	16	16
A006 A814h	MTU	Timer cycle data register B	TCDRB	16	16
A006 A816h	MTU	Timer dead time data register B	TDDRB	16	16
A006 A818h	MTU6	Timer general register A	TGRA	16	16
A006 A81Ah	MTU6	Timer general register B	TGRB	16	16
A006 A81Ch	MTU7	Timer general register A	TGRA	16	16
A006 A81Eh	MTU7	Timer general register B	TGRB	16	16
A006 A820h	MTU	Timer subcounter B	TCNTSB	16	16
A006 A822h	MTU	Timer cycle buffer register B	TCBRB	16	16
A006 A824h	MTU6	Timer general register C	TGRC	16	16
A006 A826h	MTU6	Timer general register D	TGRD	16	16
A006 A828h	MTU7	Timer general register C	TGRC	16	16
A006 A82Ah	MTU7	Timer general register D	TGRD	16	16
A006 A82Ch	MTU6	Timer status register	TSR	8	8
A006 A82Dh	MTU7	Timer status register	TSR	8	8
A006 A830h	MTU	Timer interrupt skipping set register 1B	TITCR1B	8	8
A006 A831h	MTU	Timer interrupt skipping counter 1B	TITCNT1B	8	8
A006 A832h	MTU	Timer buffer transfer set register B	TBTERB	8	8
A006 A834h	MTU	Timer dead time enable register B	TDERB	8	8
A006 A836h	MTU	Timer output level buffer register B	TOLBRB	8	8
A006 A838h	MTU6	Timer buffer operation transfer mode register	TBTM	8	8
A006 A839h	MTU7	Timer buffer operation transfer mode register	TBTM	8	8
A006 A83Ah	MTU	Timer interrupt skipping mode register B	TITMRB	8	8
A006 A83Bh	MTU	Timer interrupt skipping set register 2B	TITCR2B	8	8
A006 A83Ch	MTU	Timer interrupt skipping counter 2B	TITCNT2B	8	8
A006 A840h	MTU7	Timer A/D converter start request control register	TADCR	16	16
A006 A844h	MTU7	Timer A/D converter start request cycle set register A	TADCORA	16	16
A006 A846h	MTU7	Timer A/D converter start request cycle set register B	TADCORB	16	16
A006 A848h	MTU7	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16
A006 A84Ah	MTU7	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16
A006 A84Ch	MTU6	Timer control register 2	TCR2	8	8

Table 5.1 List of I/O Registers (Address Order) (48 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 A84Dh	MTU7	Timer control register 2	TCR2	8	8
A006 A850h	MTU6	Timer synchronous clear register	TSYCR	8	8
A006 A860h	MTU	Timer waveform control register B	TWCRB	8	8
A006 A870h	MTU	Timer mode register 2B	TMDR2B	8	8
A006 A872h	MTU6	Timer general register E	TGRE	16	16
A006 A874h	MTU7	Timer general register E	TGRE	16	16
A006 A876h	MTU7	Timer general register F	TGRF	16	16
A006 A880h	MTU	Timer start register B	TSTRB	8	8
A006 A881h	MTU	Timer synchronous register B	TSYRB	8	8
A006 A884h	MTU	Timer read/write enable register B	TRWERB	8	8
A006 A893h	MTU6	Noise filter control register	NFCR6	8	8
A006 A894h	MTU7	Noise filter control register	NFCR7	8	8
A006 A895h	MTU5	Noise filter control register	NFCR5	8	8
A006 AA80h	MTU5	Timer counter U	TCNTU	16	16
A006 AA82h	MTU5	Timer general register U	TGRU	16	16
A006 AA84h	MTU5	Timer control register U	TCRU	8	8
A006 AA85h	MTU5	Timer control register 2U	TCR2U	8	8
A006 AA86h	MTU5	Timer I/O control register U	TIORU	8	8
A006 AA90h	MTU5	Timer counter V	TCNTV	16	16
A006 AA92h	MTU5	Timer general register V	TGRV	16	16
A006 AA94h	MTU5	Timer control register V	TCRV	8	8
A006 AA95h	MTU5	Timer control register 2V	TCR2V	8	8
A006 AA96h	MTU5	Timer I/O control register V	TIORV	8	8
A006 AAA0h	MTU5	Timer counter W	TCNTW	16	16
A006 AAA2h	MTU5	Timer general register W	TGRW	16	16
A006 AAA4h	MTU5	Timer control register W	TCRW	8	8
A006 AAA5h	MTU5	Timer control register 2W	TCR2W	8	8
A006 AAA6h	MTU5	Timer I/O control register W	TIORW	8	8
A006 AAB2h	MTU5	Timer interrupt enable register	TIER	8	8
A006 AAB4h	MTU5	Timer start register	TSTR	8	8
A006 AAB6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8
A006 C000h	GPT	General PWM timer software start register	GTSTR	16	16
A006 C002h	GPT	Noise filter control register	NFCR	16	16
A006 C004h	GPT	General PWM timer hardware source start/stop control register	GTHSCR	16	16
A006 C006h	GPT	General PWM timer hardware source clear control register	GTHCCR	16	16
A006 C008h	GPT	General PWM timer hardware start source select register	GTHSSR	16	16
A006 C00Ah	GPT	General PWM timer hardware stop/clear source select register	GTHPSR	16	16
A006 C00Ch	GPT	General PWM timer write-protection register	GTWP	16	16
A006 C00Eh	GPT	General PWM timer sync register	GTSYNC	16	16
A006 C010h	GPT	General PWM timer external trigger input interrupt register	GTETINT	16	16
A006 C014h	GPT	General PWM timer buffer operation disable register	GTBDR	16	16
A006 C018h	GPT	General PWM timer start write-protection register	GTSWP	16	16
A006 C100h	GPT0	General PWM timer I/O control register	GTIOR	16	16
A006 C102h	GPT0	General PWM timer interrupt output setting register	GTINTAD	16	16
A006 C104h	GPT0	General PWM timer control register	GTCR	16	16
A006 C106h	GPT0	General PWM timer buffer enable register	GTBER	16	16
A006 C108h	GPT0	General PWM timer count direction register	GTUDC	16	16
A006 C10Ah	GPT0	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	16

Table 5.1 List of I/O Registers (Address Order) (49 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 C10Ch	GPT0	General PWM timer status register	GTST	16	16
A006 C10Eh	GPT0	General PWM timer counter	GTCNT	16	16
A006 C110h	GPT0	General PWM timer compare capture register A	GTCCRA	16	16
A006 C112h	GPT0	General PWM timer compare capture register B	GTCCRB	16	16
A006 C114h	GPT0	General PWM timer compare capture register C	GTCCRC	16	16
A006 C116h	GPT0	General PWM timer compare capture register D	GTCCRD	16	16
A006 C118h	GPT0	General PWM timer compare capture register E	GTCCRE	16	16
A006 C11Ah	GPT0	General PWM timer compare capture register F	GTCCRF	16	16
A006 C11Ch	GPT0	General PWM timer cycle setting register	GTPR	16	16
A006 C11Eh	GPT0	General PWM timer cycle setting buffer register	GTPBR	16	16
A006 C120h	GPT0	General PWM timer cycle setting double-buffer register	GTPDBR	16	16
A006 C124h	GPT0	A/D converter start request timing register A	GTADTRA	16	16
A006 C126h	GPT0	A/D converter start request timing buffer register A	GTADTBRA	16	16
A006 C128h	GPT0	A/D Converter start request timing double-buffer register A	GTADTDBRA	16	16
A006 C12Ch	GPT0	A/D Converter start request timing register B	GTADTRB	16	16
A006 C12Eh	GPT0	A/D Converter start request timing buffer register B	GTADTBRB	16	16
A006 C130h	GPT0	A/D Converter start request timing double-buffer register B	GTADTDBRB	16	16
A006 C134h	GPT0	General PWM timer output negate control register	GTONCR	16	16
A006 C136h	GPT0	General PWM timer dead time control register	GTDTCR	16	16
A006 C138h	GPT0	General PWM timer dead time value register U	GTDVU	16	16
A006 C13Ah	GPT0	General PWM timer dead time value register D	GTDVD	16	16
A006 C13Ch	GPT0	General PWM timer dead time buffer register U	GTDBU	16	16
A006 C13Eh	GPT0	General PWM timer dead time buffer register D	GTDBD	16	16
A006 C140h	GPT0	General PWM timer output protection function status register	GTSOS	16	16
A006 C142h	GPT0	General PWM timer output protection function temporary release register	GTSOTR	16	16
A006 C180h	GPT1	General PWM timer I/O control register	GTIOR	16	16
A006 C182h	GPT1	General PWM timer interrupt output setting register	GTINTAD	16	16
A006 C184h	GPT1	General PWM timer control register	GTCR	16	16
A006 C186h	GPT1	General PWM timer buffer enable register	GTBER	16	16
A006 C188h	GPT1	General PWM timer count direction register	GTUDC	16	16
A006 C18Ah	GPT1	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	16
A006 C18Ch	GPT1	General PWM timer status register	GTST	16	16
A006 C18Eh	GPT1	General PWM timer counter	GTCNT	16	16
A006 C190h	GPT1	General PWM timer compare capture register A	GTCCRA	16	16
A006 C192h	GPT1	General PWM timer compare capture register B	GTCCRB	16	16
A006 C194h	GPT1	General PWM timer compare capture register C	GTCCRC	16	16
A006 C196h	GPT1	General PWM timer compare capture register D	GTCCRD	16	16
A006 C198h	GPT1	General PWM timer compare capture register E	GTCCRE	16	16
A006 C19Ah	GPT1	General PWM timer compare capture register F	GTCCRF	16	16
A006 C19Ch	GPT1	General PWM timer cycle setting register	GTPR	16	16
A006 C19Eh	GPT1	General PWM timer cycle setting buffer register	GTPBR	16	16
A006 C1A0h	GPT1	General PWM timer cycle setting double-buffer register	GTPDBR	16	16
A006 C1A4h	GPT1	A/D converter start request timing register A	GTADTRA	16	16
A006 C1A6h	GPT1	A/D converter start request timing buffer register A	GTADTBRA	16	16
A006 C1A8h	GPT1	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16
A006 C1ACh	GPT1	A/D converter start request timing register B	GTADTRB	16	16
A006 C1AEh	GPT1	A/D converter start request timing buffer register B	GTADTBRB	16	16

Table 5.1 List of I/O Registers (Address Order) (50 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 C1B0h	GPT1	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16
A006 C1B4h	GPT1	General PWM timer output negate control register	GTONCR	16	16
A006 C1B6h	GPT1	General PWM timer dead time control register	GTDTCR	16	16
A006 C1B8h	GPT1	General PWM timer dead time value register U	GTDVU	16	16
A006 C1BAh	GPT1	General PWM timer dead time value register D	GTDVD	16	16
A006 C1BCh	GPT1	General PWM timer dead time buffer register U	GTDBU	16	16
A006 C1BEh	GPT1	General PWM timer dead time buffer register D	GTDBD	16	16
A006 C1C0h	GPT1	General PWM timer output protection function status register	GTSOS	16	16
A006 C1C2h	GPT1	General PWM timer output protection function temporary release register	GTSOTR	16	16
A006 C200h	GPT2	General PWM timer I/O control register	GTIOR	16	16
A006 C202h	GPT2	General PWM timer interrupt output setting register	GTINTAD	16	16
A006 C204h	GPT2	General PWM timer control register	GTCR	16	16
A006 C206h	GPT2	General PWM timer buffer enable register	GTBER	16	16
A006 C208h	GPT2	General PWM timer count direction register	GTUDC	16	16
A006 C20Ah	GPT2	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	16
A006 C20Ch	GPT2	General PWM timer status register	GTST	16	16
A006 C20Eh	GPT2	General PWM timer counter	GTCNT	16	16
A006 C210h	GPT2	General PWM timer compare capture register A	GTCCRA	16	16
A006 C212h	GPT2	General PWM timer compare capture register B	GTCCRB	16	16
A006 C214h	GPT2	General PWM timer compare capture register C	GTCCRC	16	16
A006 C216h	GPT2	General PWM timer compare capture register D	GTCCRD	16	16
A006 C218h	GPT2	General PWM timer compare capture register E	GTCCRE	16	16
A006 C21Ah	GPT2	General PWM timer compare capture register F	GTCCRF	16	16
A006 C21Ch	GPT2	General PWM timer cycle setting register	GTPR	16	16
A006 C21Eh	GPT2	General PWM timer cycle setting buffer register	GTPBR	16	16
A006 C220h	GPT2	General PWM timer cycle setting double-buffer register	GTPDBR	16	16
A006 C224h	GPT2	A/D converter start request timing register A	GTADTRA	16	16
A006 C226h	GPT2	A/D converter start request timing buffer register A	GTADTBRA	16	16
A006 C228h	GPT2	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16
A006 C22Ch	GPT2	A/D converter start request timing register B	GTADTRB	16	16
A006 C22Eh	GPT2	A/D converter start request timing buffer register B	GTADTBRB	16	16
A006 C230h	GPT2	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16
A006 C234h	GPT2	General PWM timer output negate control register	GTONCR	16	16
A006 C236h	GPT2	General PWM timer dead time control register	GTDTCR	16	16
A006 C238h	GPT2	General PWM timer dead time value register U	GTDVU	16	16
A006 C23Ah	GPT2	General PWM timer dead time value register D	GTDVD	16	16
A006 C23Ch	GPT2	General PWM timer dead time buffer register U	GTDBU	16	16
A006 C23Eh	GPT2	General PWM timer dead time buffer register D	GTDBD	16	16
A006 C240h	GPT2	General PWM timer output protection function status register	GTSOS	16	16
A006 C242h	GPT2	General PWM timer output protection function temporary release register	GTSOTR	16	16
A006 C280h	GPT3	General PWM timer I/O control register	GTIOR	16	16
A006 C282h	GPT3	General PWM timer interrupt output setting register	GTINTAD	16	16
A006 C284h	GPT3	General PWM timer control register	GTCR	16	16
A006 C286h	GPT3	General PWM timer buffer enable register	GTBER	16	16
A006 C288h	GPT3	General PWM timer count direction register	GTUDC	16	16
A006 C28Ah	GPT3	General PWM timer interrupt and A/D converter start request skipping setting register	GTITC	16	16

Table 5.1 List of I/O Registers (Address Order) (51 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A006 C28Ch	GPT3	General PWM timer status register	GTST	16	16
A006 C28Eh	GPT3	General PWM timer counter	GTCNT	16	16
A006 C290h	GPT3	General PWM timer compare capture register A	GTCCRA	16	16
A006 C292h	GPT3	General PWM timer compare capture register B	GTCCRB	16	16
A006 C294h	GPT3	General PWM timer compare capture register C	GTCCRC	16	16
A006 C296h	GPT3	General PWM timer compare capture register D	GTCCRD	16	16
A006 C298h	GPT3	General PWM timer compare capture register E	GTCCRE	16	16
A006 C29Ah	GPT3	General PWM timer compare capture register F	GTCCRF	16	16
A006 C29Ch	GPT3	General PWM timer cycle setting register	GTPR	16	16
A006 C29Eh	GPT3	General PWM timer cycle setting buffer register	GTPBR	16	16
A006 C2A0h	GPT3	General PWM timer cycle setting double-buffer register	GTPDBR	16	16
A006 C2A4h	GPT3	A/D converter start request timing Register A	GTADTRA	16	16
A006 C2A6h	GPT3	A/D converter start request timing buffer register A	GTADTBRA	16	16
A006 C2A8h	GPT3	A/D converter start request timing double-buffer register A	GTADTDBRA	16	16
A006 C2ACh	GPT3	A/D converter start request timing register B	GTADTRB	16	16
A006 C2AEh	GPT3	A/D converter start request timing buffer register B	GTADTBRB	16	16
A006 C2B0h	GPT3	A/D converter start request timing double-buffer register B	GTADTDBRB	16	16
A006 C2B4h	GPT3	General PWM timer output negate control register	GTONCR	16	16
A006 C2B6h	GPT3	General PWM timer dead time control register	GTDTCR	16	16
A006 C2B8h	GPT3	General PWM timer dead time value register U	GTDVU	16	16
A006 C2BAh	GPT3	General PWM timer dead time value register D	GTDVD	16	16
A006 C2BCh	GPT3	General PWM timer dead time buffer register U	GTDBU	16	16
A006 C2BEh	GPT3	General PWM timer dead time buffer register D	GTDBD	16	16
A006 C2C0h	GPT3	General PWM timer output protection function status register	GTSOS	16	16
A006 C2C2h	GPT3	General PWM timer output protection function temporary release register	GTSOTR	16	16
A007 2000h	DSMIF	UVW control register	UVWCTL	32	32
A007 2004h	DSMIF	UVW status register	UVWSTA	32	32
A007 2008h	DSMIF	UVW overcurrent abnormality detection lower limit setting register	UVWIUNCMP	32	32
A007 200Ch	DSMIF	UVW overcurrent abnormality detection upper limit setting register	UVWIOVCMP	32	32
A007 2010h	DSMIF	UVW short abnormality detection 0 data input threshold setting register	UVWSCUNCMP	32	32
A007 2014h	DSMIF	UVW short abnormality detection 1 data input threshold setting register	UVWSCOVCMP	32	32
A007 2018h	DSMIF	UVW total current abnormality detection lower limit setting register	UVWIGUNCMP	32	32
A007 201Ch	DSMIF	UVW total current abnormality detection upper limit setting register	UVWIGOVCMP	32	32
A007 2020h	DSMIF	Channel U current value register 1	U1DATA	32	32
A007 2024h	DSMIF	Channel U current value crest trigger capture register 1	U1CDATA	32	32
A007 2028h	DSMIF	Channel U current value trough trigger capture register 1	U1VDATA	32	32
A007 202Ch	DSMIF	Channel U current value register 2	U2DATA	32	32
A007 2030h	DSMIF	Channel V current value register 1	V1DATA	32	32
A007 2034h	DSMIF	Channel V current value crest trigger capture register 1	V1CDATA	32	32
A007 2038h	DSMIF	Channel V current value trough trigger capture register 1	V1VDATA	32	32
A007 203Ch	DSMIF	Channel V current value register 2	V2DATA	32	32
A007 2040h	DSMIF	Channel W current value register 1	W1DATA	32	32
A007 2044h	DSMIF	Channel W current value crest trigger capture register 1	W1CDATA	32	32
A007 2048h	DSMIF	Channel W current value trough trigger capture register 1	W1VDATA	32	32
A007 204Ch	DSMIF	Channel W current value register 2	W2DATA	32	32
A007 2080h	DSMIF	XYZ control register	XYZCTL	32	32

Table 5.1 List of I/O Registers (Address Order) (52 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 2084h	DSMIF	XYZ status register	XYZSTA	32	32
A007 2090h	DSMIF	XYZ short abnormality detection 0 data input threshold setting register	XYZSCUNCMP	32	32
A007 2094h	DSMIF	XYZ short abnormality detection 1 data input threshold setting register	XYZSCOVCMP	32	32
A007 2098h	DSMIF	XYZ overcurrent abnormality detection lower limit setting register	XYZIUNCMP	32	32
A007 209Ch	DSMIF	XYZ overcurrent abnormality detection upper limit setting register	XYZIOVCMP	32	32
A007 20A0h	DSMIF	Channel X current value register 1	X1DATA	32	32
A007 20A4h	DSMIF	Channel X current value crest trigger capture register 1	X1CDATA	32	32
A007 20A8h	DSMIF	Channel X current value trough trigger capture register 1	X1VDATA	32	32
A007 20ACh	DSMIF	Channel X current value register 2	X2DATA	32	32
A007 8000h	RSCAN	Channel 0 configuration register	RSCAN0C0CFG	32	8, 16, 32
A007 8004h	RSCAN	Channel 0 control register	RSCAN0C0CTR	32	8, 16, 32
A007 8008h	RSCAN	Channel 0 status register	RSCAN0C0STS	32	8, 16, 32
A007 800Ch	RSCAN	Channel 0 error flag register	RSCAN0C0ERFL	32	8, 16, 32
A007 8010h	RSCAN	Channel 1 configuration register	RSCAN0C1CFG	32	8, 16, 32
A007 8014h	RSCAN	Channel 1 control register	RSCAN0C1CTR	32	8, 16, 32
A007 8018h	RSCAN	Channel 1 status register	RSCAN0C1STS	32	8, 16, 32
A007 801Ch	RSCAN	Channel 1 error flag register	RSCAN0C1ERFL	32	8, 16, 32
A007 8084h	RSCAN	Global configuration register	RSCAN0GCFG	32	8, 16, 32
A007 8088h	RSCAN	Global control register	RSCAN0GCTR	32	8, 16, 32
A007 808Ch	RSCAN	Global status register	RSCAN0GSTS	32	8, 16, 32
A007 8090h	RSCAN	Global error flag register	RSCAN0GERFL	32	8, 16, 32
A007 8094h	RSCAN	Global time stamp counter register	RSCAN0GTSC	32	16, 32
A007 8098h	RSCAN	Receive rule entry control register	RSCAN0GAFLECTR	32	8, 16, 32
A007 809Ch	RSCAN	Receive rule configuration register 0	RSCAN0GAFLCFG0	32	8, 16, 32
A007 80A4h	RSCAN	Reception buffer number register	RSCAN0RMNB	32	8, 16, 32
A007 80A8h	RSCAN	Reception buffer new data register 0	RSCAN0RMND0	32	8, 16, 32
A007 80B8h	RSCAN	Reception FIFO buffer configuration/control register 0	RSCAN0RFCC0	32	8, 16, 32
A007 80BCh	RSCAN	Reception FIFO buffer configuration/control register 1	RSCAN0RFCC1	32	8, 16, 32
A007 80C0h	RSCAN	Reception FIFO buffer configuration/control register 2	RSCAN0RFCC2	32	8, 16, 32
A007 80C4h	RSCAN	Reception FIFO buffer configuration/control register 3	RSCAN0RFCC3	32	8, 16, 32
A007 80C8h	RSCAN	Reception FIFO buffer configuration/control register 4	RSCAN0RFCC4	32	8, 16, 32
A007 80CCh	RSCAN	Reception FIFO buffer configuration/control register 5	RSCAN0RFCC5	32	8, 16, 32
A007 80D0h	RSCAN	Reception FIFO buffer configuration/control register 6	RSCAN0RFCC6	32	8, 16, 32
A007 80D4h	RSCAN	Reception FIFO buffer configuration/control register 7	RSCAN0RFCC7	32	8, 16, 32
A007 80D8h	RSCAN	Reception FIFO buffer status register 0	RSCAN0RFSTS0	32	8, 16, 32
A007 80DCh	RSCAN	Reception FIFO buffer status register 1	RSCAN0RFSTS1	32	8, 16, 32
A007 80E0h	RSCAN	Reception FIFO buffer status register 2	RSCAN0RFSTS2	32	8, 16, 32
A007 80E4h	RSCAN	Reception FIFO buffer status register 3	RSCAN0RFSTS3	32	8, 16, 32
A007 80E8h	RSCAN	Reception FIFO buffer status register 4	RSCAN0RFSTS4	32	8, 16, 32
A007 80ECh	RSCAN	Reception FIFO buffer status register 5	RSCAN0RFSTS5	32	8, 16, 32
A007 80F0h	RSCAN	Reception FIFO buffer status register 6	RSCAN0RFSTS6	32	8, 16, 32
A007 80F4h	RSCAN	Reception FIFO buffer status register 7	RSCAN0RFSTS7	32	8, 16, 32
A007 80F8h	RSCAN	Reception FIFO buffer pointer control register 0	RSCAN0RFPCTR0	32	8, 16, 32
A007 80FCh	RSCAN	Reception FIFO buffer pointer control register 1	RSCAN0RFPCTR1	32	8, 16, 32
A007 8100h	RSCAN	Reception FIFO buffer pointer control register 2	RSCAN0RFPCTR2	32	8, 16, 32
A007 8104h	RSCAN	Reception FIFO buffer pointer control register 3	RSCAN0RFPCTR3	32	8, 16, 32
A007 8108h	RSCAN	Reception FIFO buffer pointer control register 4	RSCAN0RFPCTR4	32	8, 16, 32
A007 810Ch	RSCAN	Reception FIFO buffer pointer control register 5	RSCAN0RFPCTR5	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (53 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8110h	RSCAN	Reception FIFO buffer pointer control register 6	RSCAN0RFPCTR6	32	8, 16, 32
A007 8114h	RSCAN	Reception FIFO buffer pointer control register 7	RSCAN0RFPCTR7	32	8, 16, 32
A007 8118h	RSCAN	Transmission/reception FIFO buffer configuration/control register 0	RSCAN0CFCC0	32	8, 16, 32
A007 811Ch	RSCAN	Transmission/reception FIFO buffer configuration/control register 1	RSCAN0CFCC1	32	8, 16, 32
A007 8120h	RSCAN	Transmission/reception FIFO buffer configuration/control register 2	RSCAN0CFCC2	32	8, 16, 32
A007 8124h	RSCAN	Transmission/reception FIFO buffer configuration/control register 3	RSCAN0CFCC3	32	8, 16, 32
A007 8128h	RSCAN	Transmission/reception FIFO buffer configuration/control register 4	RSCAN0CFCC4	32	8, 16, 32
A007 812Ch	RSCAN	Transmission/reception FIFO buffer configuration/control register 5	RSCAN0CFCC5	32	8, 16, 32
A007 8178h	RSCAN	Transmission/reception FIFO buffer status register 0	RSCAN0CFSTS0	32	8, 16, 32
A007 817Ch	RSCAN	Transmission/reception FIFO buffer status register 1	RSCAN0CFSTS1	32	8, 16, 32
A007 8180h	RSCAN	Transmission/reception FIFO buffer status register 2	RSCAN0CFSTS2	32	8, 16, 32
A007 8184h	RSCAN	Transmission/reception FIFO buffer status register 3	RSCAN0CFSTS3	32	8, 16, 32
A007 8188h	RSCAN	Transmission/reception FIFO buffer status register 4	RSCAN0CFSTS4	32	8, 16, 32
A007 818Ch	RSCAN	Transmission/reception FIFO buffer status register 5	RSCAN0CFSTS5	32	8, 16, 32
A007 81D8h	RSCAN	Transmission/reception FIFO buffer pointer control register 0	RSCAN0CFPCTR0	32	8, 16, 32
A007 81DCh	RSCAN	Transmission/reception FIFO buffer pointer control register 1	RSCAN0CFPCTR1	32	8, 16, 32
A007 81E0h	RSCAN	Transmission/reception FIFO buffer pointer control register 2	RSCAN0CFPCTR2	32	8, 16, 32
A007 81E4h	RSCAN	Transmission/reception FIFO buffer pointer control register 3	RSCAN0CFPCTR3	32	8, 16, 32
A007 81E8h	RSCAN	Transmission/reception FIFO buffer pointer control register 4	RSCAN0CFPCTR4	32	8, 16, 32
A007 81ECh	RSCAN	Transmission/reception FIFO buffer pointer control register 5	RSCAN0CFPCTR5	32	8, 16, 32
A007 8238h	RSCAN	FIFO empty status register	RSCAN0FESTS	32	8, 16, 32
A007 823Ch	RSCAN	FIFO full status register	RSCAN0FFSTS	32	8, 16, 32
A007 8240h	RSCAN	FIFO message lost status register	RSCAN0FMSTS	32	8, 16, 32
A007 8244h	RSCAN	Reception FIFO buffer interrupt flag status register	RSCAN0RFISTS	32	8, 16, 32
A007 8248h	RSCAN	Transmission/reception FIFO buffer Receive Interrupt Flag Status Register	RSCAN0CFRISTS	32	8, 16, 32
A007 824Ch	RSCAN	Transmission/reception FIFO buffer Transmit Interrupt Flag Status Register	RSCAN0CFTISTS	32	8, 16, 32
A007 8250h	RSCAN	Transmission buffer control register 0	RSCAN0TMC0	8	8
A007 8251h	RSCAN	Transmission buffer control register 1	RSCAN0TMC1	8	8
A007 8252h	RSCAN	Transmission buffer control register 2	RSCAN0TMC2	8	8
A007 8253h	RSCAN	Transmission buffer control register 3	RSCAN0TMC3	8	8
A007 8254h	RSCAN	Transmission buffer control register 4	RSCAN0TMC4	8	8
A007 8255h	RSCAN	Transmission buffer control register 5	RSCAN0TMC5	8	8
A007 8256h	RSCAN	Transmission buffer control register 6	RSCAN0TMC6	8	8
A007 8257h	RSCAN	Transmission buffer control register 7	RSCAN0TMC7	8	8
A007 8258h	RSCAN	Transmission buffer control register 8	RSCAN0TMC8	8	8
A007 8259h	RSCAN	Transmission buffer control register 9	RSCAN0TMC9	8	8
A007 825Ah	RSCAN	Transmission buffer control register 10	RSCAN0TMC10	8	8
A007 825Bh	RSCAN	Transmission buffer control register 11	RSCAN0TMC11	8	8
A007 825Ch	RSCAN	Transmission buffer control register 12	RSCAN0TMC12	8	8
A007 825Dh	RSCAN	Transmission buffer control register 13	RSCAN0TMC13	8	8
A007 825Eh	RSCAN	Transmission buffer control register 14	RSCAN0TMC14	8	8
A007 825Fh	RSCAN	Transmission buffer control register 15	RSCAN0TMC15	8	8
A007 8260h	RSCAN	Transmission buffer control register 16	RSCAN0TMC16	8	8
A007 8261h	RSCAN	Transmission buffer control register 17	RSCAN0TMC17	8	8
A007 8262h	RSCAN	Transmission buffer control register 18	RSCAN0TMC18	8	8
A007 8263h	RSCAN	Transmission buffer control register 19	RSCAN0TMC19	8	8
A007 8264h	RSCAN	Transmission buffer control register 20	RSCAN0TMC20	8	8

Table 5.1 List of I/O Registers (Address Order) (54 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8265h	RSCAN	Transmission buffer control register 21	RSCAN0TMC21	8	8
A007 8266h	RSCAN	Transmission buffer control register 22	RSCAN0TMC22	8	8
A007 8267h	RSCAN	Transmission buffer control register 23	RSCAN0TMC23	8	8
A007 8268h	RSCAN	Transmission buffer control register 24	RSCAN0TMC24	8	8
A007 8269h	RSCAN	Transmission buffer control register 25	RSCAN0TMC25	8	8
A007 826Ah	RSCAN	Transmission buffer control register 26	RSCAN0TMC26	8	8
A007 826Bh	RSCAN	Transmission buffer control register 27	RSCAN0TMC27	8	8
A007 826Ch	RSCAN	Transmission buffer control register 28	RSCAN0TMC28	8	8
A007 826Dh	RSCAN	Transmission buffer control register 29	RSCAN0TMC29	8	8
A007 826Eh	RSCAN	Transmission buffer control register 30	RSCAN0TMC30	8	8
A007 826Fh	RSCAN	Transmission buffer control register 31	RSCAN0TMC31	8	8
A007 82D0h	RSCAN	Transmission buffer status register 0	RSCAN0TMSTS0	8	8
A007 82D1h	RSCAN	Transmission buffer status register 1	RSCAN0TMSTS1	8	8
A007 82D2h	RSCAN	Transmission buffer status register 2	RSCAN0TMSTS2	8	8
A007 82D3h	RSCAN	Transmission buffer status register 3	RSCAN0TMSTS3	8	8
A007 82D4h	RSCAN	Transmission buffer status register 4	RSCAN0TMSTS4	8	8
A007 82D5h	RSCAN	Transmission buffer status register 5	RSCAN0TMSTS5	8	8
A007 82D6h	RSCAN	Transmission buffer status register 6	RSCAN0TMSTS6	8	8
A007 82D7h	RSCAN	Transmission buffer status register 7	RSCAN0TMSTS7	8	8
A007 82D8h	RSCAN	Transmission buffer status register 8	RSCAN0TMSTS8	8	8
A007 82D9h	RSCAN	Transmission buffer status register 9	RSCAN0TMSTS9	8	8
A007 82DAh	RSCAN	Transmission buffer status register 10	RSCAN0TMSTS10	8	8
A007 82DBh	RSCAN	Transmission buffer status register 11	RSCAN0TMSTS11	8	8
A007 82DCh	RSCAN	Transmission buffer status register 12	RSCAN0TMSTS12	8	8
A007 82DDh	RSCAN	Transmission buffer status register 13	RSCAN0TMSTS13	8	8
A007 82DEh	RSCAN	Transmission buffer status register 14	RSCAN0TMSTS14	8	8
A007 82DFh	RSCAN	Transmission buffer status register 15	RSCAN0TMSTS15	8	8
A007 82E0h	RSCAN	Transmission buffer status register 16	RSCAN0TMSTS16	8	8
A007 82E1h	RSCAN	Transmission buffer status register 17	RSCAN0TMSTS17	8	8
A007 82E2h	RSCAN	Transmission buffer status register 18	RSCAN0TMSTS18	8	8
A007 82E3h	RSCAN	Transmission buffer status register 19	RSCAN0TMSTS19	8	8
A007 82E4h	RSCAN	Transmission buffer status register 20	RSCAN0TMSTS20	8	8
A007 82E5h	RSCAN	Transmission buffer status register 21	RSCAN0TMSTS21	8	8
A007 82E6h	RSCAN	Transmission buffer status register 22	RSCAN0TMSTS22	8	8
A007 82E7h	RSCAN	Transmission buffer status register 23	RSCAN0TMSTS23	8	8
A007 82E8h	RSCAN	Transmission buffer status register 24	RSCAN0TMSTS24	8	8
A007 82E9h	RSCAN	Transmission buffer status register 25	RSCAN0TMSTS25	8	8
A007 82EAh	RSCAN	Transmission buffer status register 26	RSCAN0TMSTS26	8	8
A007 82EBh	RSCAN	Transmission buffer status register 27	RSCAN0TMSTS27	8	8
A007 82ECh	RSCAN	Transmission buffer status register 28	RSCAN0TMSTS28	8	8
A007 82EDh	RSCAN	Transmission buffer status register 29	RSCAN0TMSTS29	8	8
A007 82EEh	RSCAN	Transmission buffer status register 30	RSCAN0TMSTS30	8	8
A007 82EFh	RSCAN	Transmission buffer status register 31	RSCAN0TMSTS31	8	8
A007 8350h	RSCAN	Transmission buffer transmit request status register 0	RSCAN0TMTRSTS0	32	8, 16, 32
A007 8360h	RSCAN	Transmission buffer transmit abort request status register 0	RSCAN0TMTARSTS0	32	8, 16, 32
A007 8370h	RSCAN	Transmission buffer transmit complete status register 0	RSCAN0TMTCSTS0	32	8, 16, 32
A007 8380h	RSCAN	Transmission buffer transmit abort status register 0	RSCAN0TMTASTS0	32	8, 16, 32
A007 8390h	RSCAN	Transmission buffer interrupt enable configuration register 0	RSCAN0TMIEC0	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (55 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 83A0h	RSCAN	Transmission queue configuration/control register 0	RSCAN0TXQCC0	32	8, 16, 32
A007 83A4h	RSCAN	Transmission queue configuration/control register 1	RSCAN0TXQCC1	32	8, 16, 32
A007 83C0h	RSCAN	Transmission queue status register 0	RSCAN0TXQSTS0	32	8, 16, 32
A007 83C4h	RSCAN	Transmission queue status register 1	RSCAN0TXQSTS1	32	8, 16, 32
A007 83E0h	RSCAN	Transmission queue pointer control register 0	RSCAN0TXQPCTR0	32	8, 16, 32
A007 83E4h	RSCAN	Transmission queue pointer control register 1	RSCAN0TXQPCTR1	32	8, 16, 32
A007 8400h	RSCAN	Transmission history configuration/control register 0	RSCAN0THLCC0	32	8, 16, 32
A007 8404h	RSCAN	Transmission history configuration/control register 1	RSCAN0THLCC1	32	8, 16, 32
A007 8420h	RSCAN	Transmission history status register 0	RSCAN0THLSTS0	32	8, 16, 32
A007 8424h	RSCAN	Transmission history status register 1	RSCAN0THLSTS1	32	8, 16, 32
A007 8440h	RSCAN	Transmission history pointer control register 0	RSCAN0THLPCTR0	32	8, 16, 32
A007 8444h	RSCAN	Transmission history pointer control register 1	RSCAN0THLPCTR1	32	8, 16, 32
A007 8460h	RSCAN	Global TX interrupt status register 0	RSCAN0GTINTSTS0	32	8, 16, 32
A007 8468h	RSCAN	Global test configuration register	RSCAN0GTSTCFG	32	8, 16, 32
A007 846Ch	RSCAN	Global test control register	RSCAN0GTSTCTR	32	8, 16, 32
A007 847Ch	RSCAN	Global lock key register	RSCAN0GLOCKK	32	16, 32
A007 8500h	RSCAN	Receive rule ID register 0	RSCAN0GAFLID0	32	8, 16, 32
A007 8504h	RSCAN	Receive rule mask register 0	RSCAN0GAFLM0	32	8, 16, 32
A007 8508h	RSCAN	Receive rule pointer 0 register 0	RSCAN0GAFLP00	32	8, 16, 32
A007 850Ch	RSCAN	Receive rule pointer 1 register 0	RSCAN0GAFLP10	32	8, 16, 32
A007 8510h	RSCAN	Receive rule ID register 1	RSCAN0GAFLID1	32	8, 16, 32
A007 8514h	RSCAN	Receive rule mask register 1	RSCAN0GAFLM1	32	8, 16, 32
A007 8518h	RSCAN	Receive rule pointer 0 register 1	RSCAN0GAFLP01	32	8, 16, 32
A007 851Ch	RSCAN	Receive rule pointer 1 register 1	RSCAN0GAFLP11	32	8, 16, 32
A007 8520h	RSCAN	Receive rule ID register 2	RSCAN0GAFLID2	32	8, 16, 32
A007 8524h	RSCAN	Receive rule mask register 2	RSCAN0GAFLM2	32	8, 16, 32
A007 8528h	RSCAN	Receive rule pointer 0 register 2	RSCAN0GAFLP02	32	8, 16, 32
A007 852Ch	RSCAN	Receive rule pointer 1 register 2	RSCAN0GAFLP12	32	8, 16, 32
A007 8530h	RSCAN	Receive rule ID register 3	RSCAN0GAFLID3	32	8, 16, 32
A007 8534h	RSCAN	Receive rule mask register 3	RSCAN0GAFLM3	32	8, 16, 32
A007 8538h	RSCAN	Receive rule pointer 0 register 3	RSCAN0GAFLP03	32	8, 16, 32
A007 853Ch	RSCAN	Receive rule pointer 1 register 3	RSCAN0GAFLP13	32	8, 16, 32
A007 8540h	RSCAN	Receive rule ID register 4	RSCAN0GAFLID4	32	8, 16, 32
A007 8544h	RSCAN	Receive rule mask register 4	RSCAN0GAFLM4	32	8, 16, 32
A007 8548h	RSCAN	Receive rule pointer 0 register 4	RSCAN0GAFLP04	32	8, 16, 32
A007 854Ch	RSCAN	Receive rule pointer 1 register 4	RSCAN0GAFLP14	32	8, 16, 32
A007 8550h	RSCAN	Receive rule ID register 5	RSCAN0GAFLID5	32	8, 16, 32
A007 8554h	RSCAN	Receive rule mask register 5	RSCAN0GAFLM5	32	8, 16, 32
A007 8558h	RSCAN	Receive rule pointer 0 register 5	RSCAN0GAFLP05	32	8, 16, 32
A007 855Ch	RSCAN	Receive rule pointer 1 register 5	RSCAN0GAFLP15	32	8, 16, 32
A007 8560h	RSCAN	Receive rule ID register 6	RSCAN0GAFLID6	32	8, 16, 32
A007 8564h	RSCAN	Receive rule mask register 6	RSCAN0GAFLM6	32	8, 16, 32
A007 8568h	RSCAN	Receive rule pointer 0 register 6	RSCAN0GAFLP06	32	8, 16, 32
A007 856Ch	RSCAN	Receive rule pointer 1 register 6	RSCAN0GAFLP16	32	8, 16, 32
A007 8570h	RSCAN	Receive rule ID register 7	RSCAN0GAFLID7	32	8, 16, 32
A007 8574h	RSCAN	Receive rule mask register 7	RSCAN0GAFLM7	32	8, 16, 32
A007 8578h	RSCAN	Receive rule pointer 0 register 7	RSCAN0GAFLP07	32	8, 16, 32
A007 857Ch	RSCAN	Receive rule pointer 1 register 7	RSCAN0GAFLP17	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (56 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8580h	RSCAN	Receive rule ID register 8	RSCAN0GAFLID8	32	8, 16, 32
A007 8584h	RSCAN	Receive rule mask register 8	RSCAN0GAFLM8	32	8, 16, 32
A007 8588h	RSCAN	Receive rule pointer 0 register 8	RSCAN0GAFLP08	32	8, 16, 32
A007 858Ch	RSCAN	Receive rule pointer 1 register 8	RSCAN0GAFLP18	32	8, 16, 32
A007 8590h	RSCAN	Receive rule ID register 9	RSCAN0GAFLID9	32	8, 16, 32
A007 8594h	RSCAN	Receive rule mask register 9	RSCAN0GAFLM9	32	8, 16, 32
A007 8598h	RSCAN	Receive rule pointer 0 register 9	RSCAN0GAFLP09	32	8, 16, 32
A007 859Ch	RSCAN	Receive rule pointer 1 register 9	RSCAN0GAFLP19	32	8, 16, 32
A007 85A0h	RSCAN	Receive rule ID register 10	RSCAN0GAFLID10	32	8, 16, 32
A007 85A4h	RSCAN	Receive rule mask register 10	RSCAN0GAFLM10	32	8, 16, 32
A007 85A8h	RSCAN	Receive rule pointer 0 register 10	RSCAN0GAFLP010	32	8, 16, 32
A007 85ACh	RSCAN	Receive rule pointer 1 register 10	RSCAN0GAFLP110	32	8, 16, 32
A007 85B0h	RSCAN	Receive rule ID register 11	RSCAN0GAFLID11	32	8, 16, 32
A007 85B4h	RSCAN	Receive rule mask register 11	RSCAN0GAFLM11	32	8, 16, 32
A007 85B8h	RSCAN	Receive rule pointer 0 register 11	RSCAN0GAFLP011	32	8, 16, 32
A007 85BCh	RSCAN	Receive rule pointer 1 register 11	RSCAN0GAFLP111	32	8, 16, 32
A007 85C0h	RSCAN	Receive rule ID register 12	RSCAN0GAFLID12	32	8, 16, 32
A007 85C4h	RSCAN	Receive rule mask register 12	RSCAN0GAFLM12	32	8, 16, 32
A007 85C8h	RSCAN	Receive rule pointer 0 register 12	RSCAN0GAFLP012	32	8, 16, 32
A007 85CCh	RSCAN	Receive rule pointer 1 register 12	RSCAN0GAFLP112	32	8, 16, 32
A007 85D0h	RSCAN	Receive rule ID register 13	RSCAN0GAFLID13	32	8, 16, 32
A007 85D4h	RSCAN	Receive rule mask register 13	RSCAN0GAFLM13	32	8, 16, 32
A007 85D8h	RSCAN	Receive rule pointer 0 register 13	RSCAN0GAFLP013	32	8, 16, 32
A007 85DCh	RSCAN	Receive rule pointer 1 register 13	RSCAN0GAFLP113	32	8, 16, 32
A007 85E0h	RSCAN	Receive rule ID register 14	RSCAN0GAFLID14	32	8, 16, 32
A007 85E4h	RSCAN	Receive rule mask register 14	RSCAN0GAFLM14	32	8, 16, 32
A007 85E8h	RSCAN	Receive rule pointer 0 register 14	RSCAN0GAFLP014	32	8, 16, 32
A007 85ECh	RSCAN	Receive rule pointer 1 register 14	RSCAN0GAFLP114	32	8, 16, 32
A007 85F0h	RSCAN	Receive rule ID register 15	RSCAN0GAFLID15	32	8, 16, 32
A007 85F4h	RSCAN	Receive rule mask register 15	RSCAN0GAFLM15	32	8, 16, 32
A007 85F8h	RSCAN	Receive rule pointer 0 register 15	RSCAN0GAFLP015	32	8, 16, 32
A007 85FCh	RSCAN	Receive rule pointer 1 register 15	RSCAN0GAFLP115	32	8, 16, 32
A007 8600h	RSCAN	Reception buffer ID register 0	RSCAN0RMID0	32	8, 16, 32
A007 8604h	RSCAN	Reception buffer pointer register 0	RSCAN0RMPTR0	32	8, 16, 32
A007 8608h	RSCAN	Reception buffer data field 0 register 0	RSCAN0RMDF00	32	8, 16, 32
A007 860Ch	RSCAN	Reception buffer data field 1 register 0	RSCAN0RMDF10	32	8, 16, 32
A007 8610h	RSCAN	Reception buffer ID register 1	RSCAN0RMID1	32	8, 16, 32
A007 8614h	RSCAN	Reception buffer pointer register 1	RSCAN0RMPTR1	32	8, 16, 32
A007 8618h	RSCAN	Reception buffer data field 0 register 1	RSCAN0RMDF01	32	8, 16, 32
A007 861Ch	RSCAN	Reception buffer data field 1 register 1	RSCAN0RMDF11	32	8, 16, 32
A007 8620h	RSCAN	Reception buffer ID register 2	RSCAN0RMID2	32	8, 16, 32
A007 8624h	RSCAN	Reception buffer pointer register 2	RSCAN0RMPTR2	32	8, 16, 32
A007 8628h	RSCAN	Reception buffer data field 0 register 2	RSCAN0RMDF02	32	8, 16, 32
A007 862Ch	RSCAN	Reception buffer data field 1 register 2	RSCAN0RMDF12	32	8, 16, 32
A007 8630h	RSCAN	Reception buffer ID register 3	RSCAN0RMID3	32	8, 16, 32
A007 8634h	RSCAN	Reception buffer pointer register 3	RSCAN0RMPTR3	32	8, 16, 32
A007 8638h	RSCAN	Reception buffer data field 0 register 3	RSCAN0RMDF03	32	8, 16, 32
A007 863Ch	RSCAN	Reception buffer data field 1 register 3	RSCAN0RMDF13	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (57 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8640h	RSCAN	Reception buffer ID register 4	RSCAN0RMID4	32	8, 16, 32
A007 8644h	RSCAN	Reception buffer pointer register 4	RSCAN0RMPTR4	32	8, 16, 32
A007 8648h	RSCAN	Reception buffer data field 0 register 4	RSCAN0RMDF04	32	8, 16, 32
A007 864Ch	RSCAN	Reception buffer data field 1 register 4	RSCAN0RMDF14	32	8, 16, 32
A007 8650h	RSCAN	Reception buffer ID register 5	RSCAN0RMID5	32	8, 16, 32
A007 8654h	RSCAN	Reception buffer pointer register 5	RSCAN0RMPTR5	32	8, 16, 32
A007 8658h	RSCAN	Reception buffer data field 0 register 5	RSCAN0RMDF05	32	8, 16, 32
A007 865Ch	RSCAN	Reception buffer data field 1 register 5	RSCAN0RMDF15	32	8, 16, 32
A007 8660h	RSCAN	Reception buffer ID register 6	RSCAN0RMID6	32	8, 16, 32
A007 8664h	RSCAN	Reception buffer pointer register 6	RSCAN0RMPTR6	32	8, 16, 32
A007 8668h	RSCAN	Reception buffer data field 0 register 6	RSCAN0RMDF06	32	8, 16, 32
A007 866Ch	RSCAN	Reception buffer data field 1 register 6	RSCAN0RMDF16	32	8, 16, 32
A007 8670h	RSCAN	Reception buffer ID register 7	RSCAN0RMID7	32	8, 16, 32
A007 8674h	RSCAN	Reception buffer pointer register 7	RSCAN0RMPTR7	32	8, 16, 32
A007 8678h	RSCAN	Reception buffer data field 0 register 7	RSCAN0RMDF07	32	8, 16, 32
A007 867Ch	RSCAN	Reception buffer data field 1 register 7	RSCAN0RMDF17	32	8, 16, 32
A007 8680h	RSCAN	Reception buffer ID register 8	RSCAN0RMID8	32	8, 16, 32
A007 8684h	RSCAN	Reception buffer pointer register 8	RSCAN0RMPTR8	32	8, 16, 32
A007 8688h	RSCAN	Reception buffer data field 0 register 8	RSCAN0RMDF08	32	8, 16, 32
A007 868Ch	RSCAN	Reception buffer data field 1 register 8	RSCAN0RMDF18	32	8, 16, 32
A007 8690h	RSCAN	Reception buffer ID register 9	RSCAN0RMID9	32	8, 16, 32
A007 8694h	RSCAN	Reception buffer pointer register 9	RSCAN0RMPTR9	32	8, 16, 32
A007 8698h	RSCAN	Reception buffer data field 0 register 9	RSCAN0RMDF09	32	8, 16, 32
A007 869Ch	RSCAN	Reception buffer data field 1 register 9	RSCAN0RMDF19	32	8, 16, 32
A007 86A0h	RSCAN	Reception buffer ID register 10	RSCAN0RMID10	32	8, 16, 32
A007 86A4h	RSCAN	Reception buffer pointer register 10	RSCAN0RMPTR10	32	8, 16, 32
A007 86A8h	RSCAN	Reception buffer data field 0 register 10	RSCAN0RMDF010	32	8, 16, 32
A007 86ACh	RSCAN	Reception buffer data field 1 register 10	RSCAN0RMDF110	32	8, 16, 32
A007 86B0h	RSCAN	Reception buffer ID register 11	RSCAN0RMID11	32	8, 16, 32
A007 86B4h	RSCAN	Reception buffer pointer register 11	RSCAN0RMPTR11	32	8, 16, 32
A007 86B8h	RSCAN	Reception buffer data field 0 register 11	RSCAN0RMDF011	32	8, 16, 32
A007 86BCh	RSCAN	Reception buffer data field 1 register 11	RSCAN0RMDF111	32	8, 16, 32
A007 86C0h	RSCAN	Reception buffer ID register 12	RSCAN0RMID12	32	8, 16, 32
A007 86C4h	RSCAN	Reception buffer pointer register 12	RSCAN0RMPTR12	32	8, 16, 32
A007 86C8h	RSCAN	Reception buffer data field 0 register 12	RSCAN0RMDF012	32	8, 16, 32
A007 86CCh	RSCAN	Reception buffer data field 1 register 12	RSCAN0RMDF112	32	8, 16, 32
A007 86D0h	RSCAN	Reception buffer ID register 13	RSCAN0RMID13	32	8, 16, 32
A007 86D4h	RSCAN	Reception buffer pointer register 13	RSCAN0RMPTR13	32	8, 16, 32
A007 86D8h	RSCAN	Reception buffer data field 0 register 13	RSCAN0RMDF013	32	8, 16, 32
A007 86DCh	RSCAN	Reception buffer data field 1 register 13	RSCAN0RMDF113	32	8, 16, 32
A007 86E0h	RSCAN	Reception buffer ID register 14	RSCAN0RMID14	32	8, 16, 32
A007 86E4h	RSCAN	Reception buffer pointer register 14	RSCAN0RMPTR14	32	8, 16, 32
A007 86E8h	RSCAN	Reception buffer data field 0 register 14	RSCAN0RMDF014	32	8, 16, 32
A007 86ECh	RSCAN	Reception buffer data field 1 register 14	RSCAN0RMDF114	32	8, 16, 32
A007 86F0h	RSCAN	Reception buffer ID register 15	RSCAN0RMID15	32	8, 16, 32
A007 86F4h	RSCAN	Reception buffer pointer register 15	RSCAN0RMPTR15	32	8, 16, 32
A007 86F8h	RSCAN	Reception buffer data field 0 register 15	RSCAN0RMDF015	32	8, 16, 32
A007 86FCh	RSCAN	Reception buffer data field 1 register 15	RSCAN0RMDF115	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (58 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8700h	RSCAN	Reception buffer ID register 16	RSCAN0RMID16	32	8, 16, 32
A007 8704h	RSCAN	Reception buffer pointer register 16	RSCAN0RMPTR16	32	8, 16, 32
A007 8708h	RSCAN	Reception buffer data field 0 register 16	RSCAN0RMDF016	32	8, 16, 32
A007 870Ch	RSCAN	Reception buffer data field 1 register 16	RSCAN0RMDF116	32	8, 16, 32
A007 8710h	RSCAN	Reception buffer ID register 17	RSCAN0RMID17	32	8, 16, 32
A007 8714h	RSCAN	Reception buffer pointer register 17	RSCAN0RMPTR17	32	8, 16, 32
A007 8718h	RSCAN	Reception buffer data field 0 register 17	RSCAN0RMDF017	32	8, 16, 32
A007 871Ch	RSCAN	Reception buffer data field 1 register 17	RSCAN0RMDF117	32	8, 16, 32
A007 8720h	RSCAN	Reception buffer ID register 18	RSCAN0RMID18	32	8, 16, 32
A007 8724h	RSCAN	Reception buffer pointer register 18	RSCAN0RMPTR18	32	8, 16, 32
A007 8728h	RSCAN	Reception buffer data field 0 register 18	RSCAN0RMDF018	32	8, 16, 32
A007 872Ch	RSCAN	Reception buffer data field 1 register 18	RSCAN0RMDF118	32	8, 16, 32
A007 8730h	RSCAN	Reception buffer ID register 19	RSCAN0RMID19	32	8, 16, 32
A007 8734h	RSCAN	Reception buffer pointer register 19	RSCAN0RMPTR19	32	8, 16, 32
A007 8738h	RSCAN	Reception buffer data field 0 register 19	RSCAN0RMDF019	32	8, 16, 32
A007 873Ch	RSCAN	Reception buffer data field 1 register 19	RSCAN0RMDF119	32	8, 16, 32
A007 8740h	RSCAN	Reception buffer ID register 20	RSCAN0RMID20	32	8, 16, 32
A007 8744h	RSCAN	Reception buffer pointer register 20	RSCAN0RMPTR20	32	8, 16, 32
A007 8748h	RSCAN	Reception buffer data field 0 register 20	RSCAN0RMDF020	32	8, 16, 32
A007 874Ch	RSCAN	Reception buffer data field 1 register 20	RSCAN0RMDF120	32	8, 16, 32
A007 8750h	RSCAN	Reception buffer ID register 21	RSCAN0RMID21	32	8, 16, 32
A007 8754h	RSCAN	Reception buffer pointer register 21	RSCAN0RMPTR21	32	8, 16, 32
A007 8758h	RSCAN	Reception buffer data field 0 register 21	RSCAN0RMDF021	32	8, 16, 32
A007 875Ch	RSCAN	Reception buffer data field 1 register 21	RSCAN0RMDF121	32	8, 16, 32
A007 8760h	RSCAN	Reception buffer ID register 22	RSCAN0RMID22	32	8, 16, 32
A007 8764h	RSCAN	Reception buffer pointer register 22	RSCAN0RMPTR22	32	8, 16, 32
A007 8768h	RSCAN	Reception buffer data field 0 register 22	RSCAN0RMDF022	32	8, 16, 32
A007 876Ch	RSCAN	Reception buffer data field 1 register 22	RSCAN0RMDF122	32	8, 16, 32
A007 8770h	RSCAN	Reception buffer ID register 23	RSCAN0RMID23	32	8, 16, 32
A007 8774h	RSCAN	Reception buffer pointer register 23	RSCAN0RMPTR23	32	8, 16, 32
A007 8778h	RSCAN	Reception buffer data field 0 register 23	RSCAN0RMDF023	32	8, 16, 32
A007 877Ch	RSCAN	Reception buffer data field 1 register 23	RSCAN0RMDF123	32	8, 16, 32
A007 8780h	RSCAN	Reception buffer ID register 24	RSCAN0RMID24	32	8, 16, 32
A007 8784h	RSCAN	Reception buffer pointer register 24	RSCAN0RMPTR24	32	8, 16, 32
A007 8788h	RSCAN	Reception buffer data field 0 register 24	RSCAN0RMDF024	32	8, 16, 32
A007 878Ch	RSCAN	Reception buffer data field 1 register 24	RSCAN0RMDF124	32	8, 16, 32
A007 8790h	RSCAN	Reception buffer ID register 25	RSCAN0RMID25	32	8, 16, 32
A007 8794h	RSCAN	Reception buffer pointer register 25	RSCAN0RMPTR25	32	8, 16, 32
A007 8798h	RSCAN	Reception buffer data field 0 register 25	RSCAN0RMDF025	32	8, 16, 32
A007 879Ch	RSCAN	Reception buffer data field 1 register 25	RSCAN0RMDF125	32	8, 16, 32
A007 87A0h	RSCAN	Reception buffer ID register 26	RSCAN0RMID26	32	8, 16, 32
A007 87A4h	RSCAN	Reception buffer pointer register 26	RSCAN0RMPTR26	32	8, 16, 32
A007 87A8h	RSCAN	Reception buffer data field 0 register 26	RSCAN0RMDF026	32	8, 16, 32
A007 87ACh	RSCAN	Reception buffer data field 1 register 26	RSCAN0RMDF126	32	8, 16, 32
A007 87B0h	RSCAN	Reception buffer ID register 27	RSCAN0RMID27	32	8, 16, 32
A007 87B4h	RSCAN	Reception buffer pointer register 27	RSCAN0RMPTR27	32	8, 16, 32
A007 87B8h	RSCAN	Reception buffer data field 0 register 27	RSCAN0RMDF027	32	8, 16, 32
A007 87BCh	RSCAN	Reception buffer data field 1 register 27	RSCAN0RMDF127	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (59 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 87C0h	RSCAN	Reception buffer ID register 28	RSCAN0RMID28	32	8, 16, 32
A007 87C4h	RSCAN	Reception buffer pointer register 28	RSCAN0RMPTR28	32	8, 16, 32
A007 87C8h	RSCAN	Reception buffer data field 0 register 28	RSCAN0RMDF028	32	8, 16, 32
A007 87CCh	RSCAN	Reception buffer data field 1 register 28	RSCAN0RMDF128	32	8, 16, 32
A007 87D0h	RSCAN	Reception buffer ID register 29	RSCAN0RMID29	32	8, 16, 32
A007 87D4h	RSCAN	Reception buffer pointer register 29	RSCAN0RMPTR29	32	8, 16, 32
A007 87D8h	RSCAN	Reception buffer data field 0 register 29	RSCAN0RMDF029	32	8, 16, 32
A007 87DCh	RSCAN	Reception buffer data field 1 register 29	RSCAN0RMDF129	32	8, 16, 32
A007 87E0h	RSCAN	Reception buffer ID register 30	RSCAN0RMID30	32	8, 16, 32
A007 87E4h	RSCAN	Reception buffer pointer register 30	RSCAN0RMPTR30	32	8, 16, 32
A007 87E8h	RSCAN	Reception buffer data field 0 register 30	RSCAN0RMDF030	32	8, 16, 32
A007 87ECh	RSCAN	Reception buffer data field 1 register 30	RSCAN0RMDF130	32	8, 16, 32
A007 87F0h	RSCAN	Reception buffer ID register 31	RSCAN0RMID31	32	8, 16, 32
A007 87F4h	RSCAN	Reception buffer pointer register 31	RSCAN0RMPTR31	32	8, 16, 32
A007 87F8h	RSCAN	Reception buffer data field 0 register 31	RSCAN0RMDF031	32	8, 16, 32
A007 87FCh	RSCAN	Reception buffer data field 1 register 31	RSCAN0RMDF131	32	8, 16, 32
A007 8E00h	RSCAN	Reception FIFO buffer access ID register 0	RSCAN0RFID0	32	8, 16, 32
A007 8E04h	RSCAN	Reception FIFO buffer access pointer register 0	RSCAN0RFPTR0	32	8, 16, 32
A007 8E08h	RSCAN	Reception FIFO buffer access data field 0 register 0	RSCAN0RFDF00	32	8, 16, 32
A007 8E0Ch	RSCAN	Reception FIFO buffer access data field 1 register 0	RSCAN0RFDF10	32	8, 16, 32
A007 8E10h	RSCAN	Reception FIFO buffer access ID register 1	RSCAN0RFID1	32	8, 16, 32
A007 8E14h	RSCAN	Reception FIFO buffer access pointer register 1	RSCAN0RFPTR1	32	8, 16, 32
A007 8E18h	RSCAN	Reception FIFO buffer access data field 0 register 1	RSCAN0RFDF01	32	8, 16, 32
A007 8E1Ch	RSCAN	Reception FIFO buffer access data field 1 register 1	RSCAN0RFDF11	32	8, 16, 32
A007 8E20h	RSCAN	Reception FIFO buffer access ID register 2	RSCAN0RFID2	32	8, 16, 32
A007 8E24h	RSCAN	Reception FIFO buffer access pointer register 2	RSCAN0RFPTR2	32	8, 16, 32
A007 8E28h	RSCAN	Reception FIFO buffer access data field 0 register 2	RSCAN0RFDF02	32	8, 16, 32
A007 8E2Ch	RSCAN	Reception FIFO buffer access data field 1 register 2	RSCAN0RFDF12	32	8, 16, 32
A007 8E30h	RSCAN	Reception FIFO buffer access ID register 3	RSCAN0RFID3	32	8, 16, 32
A007 8E34h	RSCAN	Reception FIFO buffer access pointer register 3	RSCAN0RFPTR3	32	8, 16, 32
A007 8E38h	RSCAN	Reception FIFO buffer access data field 0 register 3	RSCAN0RFDF03	32	8, 16, 32
A007 8E3Ch	RSCAN	Reception FIFO buffer access data field 1 register 3	RSCAN0RFDF13	32	8, 16, 32
A007 8E40h	RSCAN	Reception FIFO buffer access ID register 4	RSCAN0RFID4	32	8, 16, 32
A007 8E44h	RSCAN	Reception FIFO buffer access pointer register 4	RSCAN0RFPTR4	32	8, 16, 32
A007 8E48h	RSCAN	Reception FIFO buffer access data field 0 register 4	RSCAN0RFDF04	32	8, 16, 32
A007 8E4Ch	RSCAN	Reception FIFO buffer access data field 1 register 4	RSCAN0RFDF14	32	8, 16, 32
A007 8E50h	RSCAN	Reception FIFO buffer access ID register 5	RSCAN0RFID5	32	8, 16, 32
A007 8E54h	RSCAN	Reception FIFO buffer access pointer register 5	RSCAN0RFPTR5	32	8, 16, 32
A007 8E58h	RSCAN	Reception FIFO buffer access data field 0 register 5	RSCAN0RFDF05	32	8, 16, 32
A007 8E5Ch	RSCAN	Reception FIFO buffer access data field 1 register 5	RSCAN0RFDF15	32	8, 16, 32
A007 8E60h	RSCAN	Reception FIFO buffer access ID register 6	RSCAN0RFID6	32	8, 16, 32
A007 8E64h	RSCAN	Reception FIFO buffer access pointer register 6	RSCAN0RFPTR6	32	8, 16, 32
A007 8E68h	RSCAN	Reception FIFO buffer access data field 0 register 6	RSCAN0RFDF06	32	8, 16, 32
A007 8E6Ch	RSCAN	Reception FIFO buffer access data field 1 register 6	RSCAN0RFDF16	32	8, 16, 32
A007 8E70h	RSCAN	Reception FIFO buffer access ID register 7	RSCAN0RFID7	32	8, 16, 32
A007 8E74h	RSCAN	Reception FIFO buffer access pointer register 7	RSCAN0RFPTR7	32	8, 16, 32
A007 8E78h	RSCAN	Reception FIFO buffer access data field 0 register 7	RSCAN0RFDF07	32	8, 16, 32
A007 8E7Ch	RSCAN	Reception FIFO buffer access data field 1 register 7	RSCAN0RFDF17	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (60 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 8E80h	RSCAN	Transmission/reception FIFO buffer access ID register 0	RSCAN0CFID0	32	8, 16, 32
A007 8E84h	RSCAN	Transmission/reception FIFO buffer access pointer register 0	RSCAN0CFPTR0	32	8, 16, 32
A007 8E88h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 0	RSCAN0CFDF00	32	8, 16, 32
A007 8E8Ch	RSCAN	Transmission/reception FIFO buffer access data field 1 register 0	RSCAN0CFDF10	32	8, 16, 32
A007 8E90h	RSCAN	Transmission/reception FIFO buffer access ID register 1	RSCAN0CFID1	32	8, 16, 32
A007 8E94h	RSCAN	Transmission/reception FIFO buffer access pointer register 1	RSCAN0CFPTR1	32	8, 16, 32
A007 8E98h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 1	RSCAN0CFDF01	32	8, 16, 32
A007 8E9Ch	RSCAN	Transmission/reception FIFO buffer access data field 1 register 1	RSCAN0CFDF11	32	8, 16, 32
A007 8EA0h	RSCAN	Transmission/reception FIFO buffer access ID register 2	RSCAN0CFID2	32	8, 16, 32
A007 8EA4h	RSCAN	Transmission/reception FIFO buffer access pointer register 2	RSCAN0CFPTR2	32	8, 16, 32
A007 8EA8h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 2	RSCAN0CFDF02	32	8, 16, 32
A007 8EACh	RSCAN	Transmission/reception FIFO buffer access data field 1 register 2	RSCAN0CFDF12	32	8, 16, 32
A007 8EB0h	RSCAN	Transmission/reception FIFO buffer access ID register 3	RSCAN0CFID3	32	8, 16, 32
A007 8EB4h	RSCAN	Transmission/reception FIFO buffer access pointer register 3	RSCAN0CFPTR3	32	8, 16, 32
A007 8EB8h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 3	RSCAN0CFDF03	32	8, 16, 32
A007 8EBCh	RSCAN	Transmission/reception FIFO buffer access data field 1 register 3	RSCAN0CFDF13	32	8, 16, 32
A007 8EC0h	RSCAN	Transmission/reception FIFO buffer access ID register 4	RSCAN0CFID4	32	8, 16, 32
A007 8EC4h	RSCAN	Transmission/reception FIFO buffer access pointer register 4	RSCAN0CFPTR4	32	8, 16, 32
A007 8EC8h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 4	RSCAN0CFDF04	32	8, 16, 32
A007 8ECCh	RSCAN	Transmission/reception FIFO buffer access data field 1 register 4	RSCAN0CFDF14	32	8, 16, 32
A007 8ED0h	RSCAN	Transmission/reception FIFO buffer access ID register 5	RSCAN0CFID5	32	8, 16, 32
A007 8ED4h	RSCAN	Transmission/reception FIFO buffer access pointer register 5	RSCAN0CFPTR5	32	8, 16, 32
A007 8ED8h	RSCAN	Transmission/reception FIFO buffer access data field 0 register 5	RSCAN0CFDF05	32	8, 16, 32
A007 8EDCh	RSCAN	Transmission/reception FIFO buffer access data field 1 register 5	RSCAN0CFDF15	32	8, 16, 32
A007 9000h	RSCAN	Transmission buffer ID register 0	RSCAN0TMID0	32	8, 16, 32
A007 9004h	RSCAN	Transmission buffer pointer register 0	RSCAN0TMPTR0	32	8, 16, 32
A007 9008h	RSCAN	Transmission buffer data field 0 register 0	RSCAN0TMDF00	32	8, 16, 32
A007 900Ch	RSCAN	Transmission buffer data field 1 register 0	RSCAN0TMDF10	32	8, 16, 32
A007 9010h	RSCAN	Transmission buffer ID register 1	RSCAN0TMID1	32	8, 16, 32
A007 9014h	RSCAN	Transmission buffer pointer register 1	RSCAN0TMPTR1	32	8, 16, 32
A007 9018h	RSCAN	Transmission buffer data field 0 register 1	RSCAN0TMDF01	32	8, 16, 32
A007 901Ch	RSCAN	Transmission buffer data field 1 register 1	RSCAN0TMDF11	32	8, 16, 32
A007 9020h	RSCAN	Transmission buffer ID register 2	RSCAN0TMID2	32	8, 16, 32
A007 9024h	RSCAN	Transmission buffer pointer register 2	RSCAN0TMPTR2	32	8, 16, 32
A007 9028h	RSCAN	Transmission buffer data field 0 register 2	RSCAN0TMDF02	32	8, 16, 32
A007 902Ch	RSCAN	Transmission buffer data field 1 register 2	RSCAN0TMDF12	32	8, 16, 32
A007 9030h	RSCAN	Transmission buffer ID register 3	RSCAN0TMID3	32	8, 16, 32
A007 9034h	RSCAN	Transmission buffer pointer register 3	RSCAN0TMPTR3	32	8, 16, 32
A007 9038h	RSCAN	Transmission buffer data field 0 register 3	RSCAN0TMDF03	32	8, 16, 32
A007 903Ch	RSCAN	Transmission buffer data field 1 register 3	RSCAN0TMDF13	32	8, 16, 32
A007 9040h	RSCAN	Transmission buffer ID register 4	RSCAN0TMID4	32	8, 16, 32
A007 9044h	RSCAN	Transmission buffer pointer register 4	RSCAN0TMPTR4	32	8, 16, 32
A007 9048h	RSCAN	Transmission buffer data field 0 register 4	RSCAN0TMDF04	32	8, 16, 32
A007 904Ch	RSCAN	Transmission buffer data field 1 register 4	RSCAN0TMDF14	32	8, 16, 32
A007 9050h	RSCAN	Transmission buffer ID register 5	RSCAN0TMID5	32	8, 16, 32
A007 9054h	RSCAN	Transmission buffer pointer register 5	RSCAN0TMPTR5	32	8, 16, 32
A007 9058h	RSCAN	Transmission buffer data field 0 register 5	RSCAN0TMDF05	32	8, 16, 32
A007 905Ch	RSCAN	Transmission buffer data field 1 register 5	RSCAN0TMDF15	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (61 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 9060h	RSCAN	Transmission buffer ID register 6	RSCAN0TMID6	32	8, 16, 32
A007 9064h	RSCAN	Transmission buffer pointer register 6	RSCAN0TMPTR6	32	8, 16, 32
A007 9068h	RSCAN	Transmission buffer data field 0 register 6	RSCAN0TMDF06	32	8, 16, 32
A007 906Ch	RSCAN	Transmission buffer data field 1 register 6	RSCAN0TMDF16	32	8, 16, 32
A007 9070h	RSCAN	Transmission buffer ID register 7	RSCAN0TMID7	32	8, 16, 32
A007 9074h	RSCAN	Transmission buffer pointer register 7	RSCAN0TMPTR7	32	8, 16, 32
A007 9078h	RSCAN	Transmission buffer data field 0 register 7	RSCAN0TMDF07	32	8, 16, 32
A007 907Ch	RSCAN	Transmission buffer data field 1 register 7	RSCAN0TMDF17	32	8, 16, 32
A007 9080h	RSCAN	Transmission buffer ID register 8	RSCAN0TMID8	32	8, 16, 32
A007 9084h	RSCAN	Transmission buffer pointer register 8	RSCAN0TMPTR8	32	8, 16, 32
A007 9088h	RSCAN	Transmission buffer data field 0 register 8	RSCAN0TMDF08	32	8, 16, 32
A007 908Ch	RSCAN	Transmission buffer data field 1 register 8	RSCAN0TMDF18	32	8, 16, 32
A007 9090h	RSCAN	Transmission buffer ID register 9	RSCAN0TMID9	32	8, 16, 32
A007 9094h	RSCAN	Transmission buffer pointer register 9	RSCAN0TMPTR9	32	8, 16, 32
A007 9098h	RSCAN	Transmission buffer data field 0 register 9	RSCAN0TMDF09	32	8, 16, 32
A007 909Ch	RSCAN	Transmission buffer data field 1 register 9	RSCAN0TMDF19	32	8, 16, 32
A007 90A0h	RSCAN	Transmission buffer ID register 10	RSCAN0TMID10	32	8, 16, 32
A007 90A4h	RSCAN	Transmission buffer pointer register 10	RSCAN0TMPTR10	32	8, 16, 32
A007 90A8h	RSCAN	Transmission buffer data field 0 register 10	RSCAN0TMDF010	32	8, 16, 32
A007 90ACh	RSCAN	Transmission buffer data field 1 register 10	RSCAN0TMDF110	32	8, 16, 32
A007 90B0h	RSCAN	Transmission buffer ID register 11	RSCAN0TMID11	32	8, 16, 32
A007 90B4h	RSCAN	Transmission buffer pointer register 11	RSCAN0TMPTR11	32	8, 16, 32
A007 90B8h	RSCAN	Transmission buffer data field 0 register 11	RSCAN0TMDF011	32	8, 16, 32
A007 90BCh	RSCAN	Transmission buffer data field 1 register 11	RSCAN0TMDF111	32	8, 16, 32
A007 90C0h	RSCAN	Transmission buffer ID register 12	RSCAN0TMID12	32	8, 16, 32
A007 90C4h	RSCAN	Transmission buffer pointer register 12	RSCAN0TMPTR12	32	8, 16, 32
A007 90C8h	RSCAN	Transmission buffer data field 0 register 12	RSCAN0TMDF012	32	8, 16, 32
A007 90CCh	RSCAN	Transmission buffer data field 1 register 12	RSCAN0TMDF112	32	8, 16, 32
A007 90D0h	RSCAN	Transmission buffer ID register 13	RSCAN0TMID13	32	8, 16, 32
A007 90D4h	RSCAN	Transmission buffer pointer register 13	RSCAN0TMPTR13	32	8, 16, 32
A007 90D8h	RSCAN	Transmission buffer data field 0 register 13	RSCAN0TMDF013	32	8, 16, 32
A007 90DCh	RSCAN	Transmission buffer data field 1 register 13	RSCAN0TMDF113	32	8, 16, 32
A007 90E0h	RSCAN	Transmission buffer ID register 14	RSCAN0TMID14	32	8, 16, 32
A007 90E4h	RSCAN	Transmission buffer pointer register 14	RSCAN0TMPTR14	32	8, 16, 32
A007 90E8h	RSCAN	Transmission buffer data field 0 register 14	RSCAN0TMDF014	32	8, 16, 32
A007 90ECh	RSCAN	Transmission buffer data field 1 register 14	RSCAN0TMDF114	32	8, 16, 32
A007 90F0h	RSCAN	Transmission buffer ID register 15	RSCAN0TMID15	32	8, 16, 32
A007 90F4h	RSCAN	Transmission buffer pointer register 15	RSCAN0TMPTR15	32	8, 16, 32
A007 90F8h	RSCAN	Transmission buffer data field 0 register 15	RSCAN0TMDF015	32	8, 16, 32
A007 90FCh	RSCAN	Transmission buffer data field 1 register 15	RSCAN0TMDF115	32	8, 16, 32
A007 9100h	RSCAN	Transmission buffer ID register 16	RSCAN0TMID16	32	8, 16, 32
A007 9104h	RSCAN	Transmission buffer pointer register 16	RSCAN0TMPTR16	32	8, 16, 32
A007 9108h	RSCAN	Transmission buffer data field 0 register 16	RSCAN0TMDF016	32	8, 16, 32
A007 910Ch	RSCAN	Transmission buffer data field 1 register 16	RSCAN0TMDF116	32	8, 16, 32
A007 9110h	RSCAN	Transmission buffer ID register 17	RSCAN0TMID17	32	8, 16, 32
A007 9114h	RSCAN	Transmission buffer pointer register 17	RSCAN0TMPTR17	32	8, 16, 32
A007 9118h	RSCAN	Transmission buffer data field 0 register 17	RSCAN0TMDF017	32	8, 16, 32
A007 911Ch	RSCAN	Transmission buffer data field 1 register 17	RSCAN0TMDF117	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (62 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 9120h	RSCAN	Transmission buffer ID register 18	RSCAN0TMID18	32	8, 16, 32
A007 9124h	RSCAN	Transmission buffer pointer register 18	RSCAN0TMPTR18	32	8, 16, 32
A007 9128h	RSCAN	Transmission buffer data field 0 register 18	RSCAN0TMDF018	32	8, 16, 32
A007 912Ch	RSCAN	Transmission buffer data field 1 register 18	RSCAN0TMDF118	32	8, 16, 32
A007 9130h	RSCAN	Transmission buffer ID register 19	RSCAN0TMID19	32	8, 16, 32
A007 9134h	RSCAN	Transmission buffer pointer register 19	RSCAN0TMPTR19	32	8, 16, 32
A007 9138h	RSCAN	Transmission buffer data field 0 register 19	RSCAN0TMDF019	32	8, 16, 32
A007 913Ch	RSCAN	Transmission buffer data field 1 register 19	RSCAN0TMDF119	32	8, 16, 32
A007 9140h	RSCAN	Transmission buffer ID register 20	RSCAN0TMID20	32	8, 16, 32
A007 9144h	RSCAN	Transmission buffer pointer register 20	RSCAN0TMPTR20	32	8, 16, 32
A007 9148h	RSCAN	Transmission buffer data field 0 register 20	RSCAN0TMDF020	32	8, 16, 32
A007 914Ch	RSCAN	Transmission buffer data field 1 register 20	RSCAN0TMDF120	32	8, 16, 32
A007 9150h	RSCAN	Transmission buffer ID register 21	RSCAN0TMID21	32	8, 16, 32
A007 9154h	RSCAN	Transmission buffer pointer register 21	RSCAN0TMPTR21	32	8, 16, 32
A007 9158h	RSCAN	Transmission buffer data field 0 register 21	RSCAN0TMDF021	32	8, 16, 32
A007 915Ch	RSCAN	Transmission buffer data field 1 register 21	RSCAN0TMDF121	32	8, 16, 32
A007 9160h	RSCAN	Transmission buffer ID register 22	RSCAN0TMID22	32	8, 16, 32
A007 9164h	RSCAN	Transmission buffer pointer register 22	RSCAN0TMPTR22	32	8, 16, 32
A007 9168h	RSCAN	Transmission buffer data field 0 register 22	RSCAN0TMDF022	32	8, 16, 32
A007 916Ch	RSCAN	Transmission buffer data field 1 register 22	RSCAN0TMDF122	32	8, 16, 32
A007 9170h	RSCAN	Transmission buffer ID register 23	RSCAN0TMID23	32	8, 16, 32
A007 9174h	RSCAN	Transmission buffer pointer register 23	RSCAN0TMPTR23	32	8, 16, 32
A007 9178h	RSCAN	Transmission buffer data field 0 register 23	RSCAN0TMDF023	32	8, 16, 32
A007 917Ch	RSCAN	Transmission buffer data field 1 register 23	RSCAN0TMDF123	32	8, 16, 32
A007 9180h	RSCAN	Transmission buffer ID register 24	RSCAN0TMID24	32	8, 16, 32
A007 9184h	RSCAN	Transmission buffer pointer register 24	RSCAN0TMPTR24	32	8, 16, 32
A007 9188h	RSCAN	Transmission buffer data field 0 register 24	RSCAN0TMDF024	32	8, 16, 32
A007 918Ch	RSCAN	Transmission buffer data field 1 register 24	RSCAN0TMDF124	32	8, 16, 32
A007 9190h	RSCAN	Transmission buffer ID register 25	RSCAN0TMID25	32	8, 16, 32
A007 9194h	RSCAN	Transmission buffer pointer register 25	RSCAN0TMPTR25	32	8, 16, 32
A007 9198h	RSCAN	Transmission buffer data field 0 register 25	RSCAN0TMDF025	32	8, 16, 32
A007 919Ch	RSCAN	Transmission buffer data field 1 register 25	RSCAN0TMDF125	32	8, 16, 32
A007 91A0h	RSCAN	Transmission buffer ID register 26	RSCAN0TMID26	32	8, 16, 32
A007 91A4h	RSCAN	Transmission buffer pointer register 26	RSCAN0TMPTR26	32	8, 16, 32
A007 91A8h	RSCAN	Transmission buffer data field 0 register 26	RSCAN0TMDF026	32	8, 16, 32
A007 91ACh	RSCAN	Transmission buffer data field 1 register 26	RSCAN0TMDF126	32	8, 16, 32
A007 91B0h	RSCAN	Transmission buffer ID register 27	RSCAN0TMID27	32	8, 16, 32
A007 91B4h	RSCAN	Transmission buffer pointer register 27	RSCAN0TMPTR27	32	8, 16, 32
A007 91B8h	RSCAN	Transmission buffer data field 0 register 27	RSCAN0TMDF027	32	8, 16, 32
A007 91BCh	RSCAN	Transmission buffer data field 1 register 27	RSCAN0TMDF127	32	8, 16, 32
A007 91C0h	RSCAN	Transmission buffer ID register 28	RSCAN0TMID28	32	8, 16, 32
A007 91C4h	RSCAN	Transmission buffer pointer register 28	RSCAN0TMPTR28	32	8, 16, 32
A007 91C8h	RSCAN	Transmission buffer data field 0 register 28	RSCAN0TMDF028	32	8, 16, 32
A007 91CCh	RSCAN	Transmission buffer data field 1 register 28	RSCAN0TMDF128	32	8, 16, 32
A007 91D0h	RSCAN	Transmission buffer ID register 29	RSCAN0TMID29	32	8, 16, 32
A007 91D4h	RSCAN	Transmission buffer pointer register 29	RSCAN0TMPTR29	32	8, 16, 32
A007 91D8h	RSCAN	Transmission buffer data field 0 register 29	RSCAN0TMDF029	32	8, 16, 32
A007 91DCh	RSCAN	Transmission buffer data field 1 register 29	RSCAN0TMDF129	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (63 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 91E0h	RSCAN	Transmission buffer ID register 30	RSCAN0TMID30	32	8, 16, 32
A007 91E4h	RSCAN	Transmission buffer pointer register 30	RSCAN0TMPTR30	32	8, 16, 32
A007 91E8h	RSCAN	Transmission buffer data field 0 register 30	RSCAN0TMDF030	32	8, 16, 32
A007 91ECh	RSCAN	Transmission buffer data field 1 register 30	RSCAN0TMDF130	32	8, 16, 32
A007 91F0h	RSCAN	Transmission buffer ID register 31	RSCAN0TMID31	32	8, 16, 32
A007 91F4h	RSCAN	Transmission buffer pointer register 31	RSCAN0TMPTR31	32	8, 16, 32
A007 91F8h	RSCAN	Transmission buffer data field 0 register 31	RSCAN0TMDF031	32	8, 16, 32
A007 91FCh	RSCAN	Transmission buffer data field 1 register 31	RSCAN0TMDF131	32	8, 16, 32
A007 9800h	RSCAN	Transmission history access register 0	RSCAN0THLACC0	32	8, 16, 32
A007 9804h	RSCAN	Transmission history access register 1	RSCAN0THLACC1	32	8, 16, 32
A007 9900h	RSCAN	RAM test page access register 0	RSCAN0RPGACC0	32	8, 16, 32
A007 9904h	RSCAN	RAM test page access register 1	RSCAN0RPGACC1	32	8, 16, 32
A007 9908h	RSCAN	RAM test page access register 2	RSCAN0RPGACC2	32	8, 16, 32
A007 990Ch	RSCAN	RAM test page access register 3	RSCAN0RPGACC3	32	8, 16, 32
A007 9910h	RSCAN	RAM test page access register 4	RSCAN0RPGACC4	32	8, 16, 32
A007 9914h	RSCAN	RAM test page access register 5	RSCAN0RPGACC5	32	8, 16, 32
A007 9918h	RSCAN	RAM test page access register 6	RSCAN0RPGACC6	32	8, 16, 32
A007 991Ch	RSCAN	RAM test page access register 7	RSCAN0RPGACC7	32	8, 16, 32
A007 9920h	RSCAN	RAM test page access register 8	RSCAN0RPGACC8	32	8, 16, 32
A007 9924h	RSCAN	RAM test page access register 9	RSCAN0RPGACC9	32	8, 16, 32
A007 9928h	RSCAN	RAM test page access register 10	RSCAN0RPGACC10	32	8, 16, 32
A007 992Ch	RSCAN	RAM test page access register 11	RSCAN0RPGACC11	32	8, 16, 32
A007 9930h	RSCAN	RAM test page access register 12	RSCAN0RPGACC12	32	8, 16, 32
A007 9934h	RSCAN	RAM test page access register 13	RSCAN0RPGACC13	32	8, 16, 32
A007 9938h	RSCAN	RAM test page access register 14	RSCAN0RPGACC14	32	8, 16, 32
A007 993Ch	RSCAN	RAM test page access register 15	RSCAN0RPGACC15	32	8, 16, 32
A007 9940h	RSCAN	RAM test page access register 16	RSCAN0RPGACC16	32	8, 16, 32
A007 9944h	RSCAN	RAM test page access register 17	RSCAN0RPGACC17	32	8, 16, 32
A007 9948h	RSCAN	RAM test page access register 18	RSCAN0RPGACC18	32	8, 16, 32
A007 994Ch	RSCAN	RAM test page access register 19	RSCAN0RPGACC19	32	8, 16, 32
A007 9950h	RSCAN	RAM test page access register 20	RSCAN0RPGACC20	32	8, 16, 32
A007 9954h	RSCAN	RAM test page access register 21	RSCAN0RPGACC21	32	8, 16, 32
A007 9958h	RSCAN	RAM test page access register 22	RSCAN0RPGACC22	32	8, 16, 32
A007 995Ch	RSCAN	RAM test page access register 23	RSCAN0RPGACC23	32	8, 16, 32
A007 9960h	RSCAN	RAM test page access register 24	RSCAN0RPGACC24	32	8, 16, 32
A007 9964h	RSCAN	RAM test page access register 25	RSCAN0RPGACC25	32	8, 16, 32
A007 9968h	RSCAN	RAM test page access register 26	RSCAN0RPGACC26	32	8, 16, 32
A007 996Ch	RSCAN	RAM test page access register 27	RSCAN0RPGACC27	32	8, 16, 32
A007 9970h	RSCAN	RAM test page access register 28	RSCAN0RPGACC28	32	8, 16, 32
A007 9974h	RSCAN	RAM test page access register 29	RSCAN0RPGACC29	32	8, 16, 32
A007 9978h	RSCAN	RAM test page access register 30	RSCAN0RPGACC30	32	8, 16, 32
A007 997Ch	RSCAN	RAM test page access register 31	RSCAN0RPGACC31	32	8, 16, 32
A007 9980h	RSCAN	RAM test page access register 32	RSCAN0RPGACC32	32	8, 16, 32
A007 9984h	RSCAN	RAM test page access register 33	RSCAN0RPGACC33	32	8, 16, 32
A007 9988h	RSCAN	RAM test page access register 34	RSCAN0RPGACC34	32	8, 16, 32
A007 998Ch	RSCAN	RAM test page access register 35	RSCAN0RPGACC35	32	8, 16, 32
A007 9990h	RSCAN	RAM test page access register 36	RSCAN0RPGACC36	32	8, 16, 32
A007 9994h	RSCAN	RAM test page access register 37	RSCAN0RPGACC37	32	8, 16, 32

Table 5.1 List of I/O Registers (Address Order) (64 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 9998h	RSCAN	RAM test page access register 38	RSCAN0RPGACC38	32	8, 16, 32
A007 999Ch	RSCAN	RAM test page access register 39	RSCAN0RPGACC39	32	8, 16, 32
A007 99A0h	RSCAN	RAM test page access register 40	RSCAN0RPGACC40	32	8, 16, 32
A007 99A4h	RSCAN	RAM test page access register 41	RSCAN0RPGACC41	32	8, 16, 32
A007 99A8h	RSCAN	RAM test page access register 42	RSCAN0RPGACC42	32	8, 16, 32
A007 99ACh	RSCAN	RAM test page access register 43	RSCAN0RPGACC43	32	8, 16, 32
A007 99B0h	RSCAN	RAM test page access register 44	RSCAN0RPGACC44	32	8, 16, 32
A007 99B4h	RSCAN	RAM test page access register 45	RSCAN0RPGACC45	32	8, 16, 32
A007 99B8h	RSCAN	RAM test page access register 46	RSCAN0RPGACC46	32	8, 16, 32
A007 99BCh	RSCAN	RAM test page access register 47	RSCAN0RPGACC47	32	8, 16, 32
A007 99C0h	RSCAN	RAM test page access register 48	RSCAN0RPGACC48	32	8, 16, 32
A007 99C4h	RSCAN	RAM test page access register 49	RSCAN0RPGACC49	32	8, 16, 32
A007 99C8h	RSCAN	RAM test page access register 50	RSCAN0RPGACC50	32	8, 16, 32
A007 99CCh	RSCAN	RAM test page access register 51	RSCAN0RPGACC51	32	8, 16, 32
A007 99D0h	RSCAN	RAM test page access register 52	RSCAN0RPGACC52	32	8, 16, 32
A007 99D4h	RSCAN	RAM test page access register 53	RSCAN0RPGACC53	32	8, 16, 32
A007 99D8h	RSCAN	RAM test page access register 54	RSCAN0RPGACC54	32	8, 16, 32
A007 99DCh	RSCAN	RAM test page access register 55	RSCAN0RPGACC55	32	8, 16, 32
A007 99E0h	RSCAN	RAM test page access register 56	RSCAN0RPGACC56	32	8, 16, 32
A007 99E4h	RSCAN	RAM test page access register 57	RSCAN0RPGACC57	32	8, 16, 32
A007 99E8h	RSCAN	RAM test page access register 58	RSCAN0RPGACC58	32	8, 16, 32
A007 99ECh	RSCAN	RAM test page access register 59	RSCAN0RPGACC59	32	8, 16, 32
A007 99F0h	RSCAN	RAM test page access register 60	RSCAN0RPGACC60	32	8, 16, 32
A007 99F4h	RSCAN	RAM test page access register 61	RSCAN0RPGACC61	32	8, 16, 32
A007 99F8h	RSCAN	RAM test page access register 62	RSCAN0RPGACC62	32	8, 16, 32
A007 99FCh	RSCAN	RAM test page access register 63	RSCAN0RPGACC63	32	8, 16, 32
A007 B000h	RSCAN	RSCAN ECC control register	ECCRCANCTL	32	8, 16, 32
A007 B010h	RSCAN	RSCAN ECC error address register 0	ECCRCANEAD0	32	8, 16, 32
A007 B014h	RSCAN	RSCAN ECC error address register 1	ECCRCANEAD1	32	8, 16, 32
A007 B018h	RSCAN	RSCAN ECC error address register 2	ECCRCANEAD2	32	8, 16, 32
A007 B01Ch	RSCAN	RSCAN ECC error address register 3	ECCRCANEAD3	32	8, 16, 32
A007 B020h	RSCAN	RSCAN ECC error address register 4	ECCRCANEAD4	32	8, 16, 32
A007 B024h	RSCAN	RSCAN ECC error address register 5	ECCRCANEAD5	32	8, 16, 32
A007 B028h	RSCAN	RSCAN ECC error address register 6	ECCRCANEAD6	32	8, 16, 32
A007 B02Ch	RSCAN	RSCAN ECC error address register 7	ECCRCANEAD7	32	8, 16, 32
A007 C000h	CRC	CRC data input register	CRCDIR	32	32
A007 C004h	CRC	CRC data output register	CRCDOR	32	32
A007 C020h	CRC	CRC control register	CRCCR	8	8
A007 D000h	ECMM	ECM master error set trigger register	ECMMESET	8	8
A007 D004h	ECMM	ECM master error clear trigger register	ECMMECLR	8	8
A007 D008h	ECMM	ECM master error source status register 0	ECMMESSTR0	32	32
A007 D00Ch	ECMM	ECM master error source status register 1	ECMMESSTR1	32	32
A007 D010h	ECMM	ECM master error source status register 2	ECMMESSTR2	32	32
A007 D014h	ECMM	ECM master protection command register	ECMMPCMD0	32	32
A007 D040h	ECMC	ECM checker error set trigger register	ECMCESET	8	8
A007 D044h	ECMC	ECM checker error clear trigger register	ECMCECLR	8	8
A007 D048h	ECMC	ECM checker error source status register 0	ECMCESSTR0	32	32
A007 D04Ch	ECMC	ECM checker error source status register 1	ECMCESSTR1	32	32

Table 5.1 List of I/O Registers (Address Order) (65 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A007 D050h	ECMC	ECM checker error source status register 2	ECMCESSTR2	32	32
A007 D054h	ECMC	ECM checker protection command register	ECMCPCMD0	32	32
A007 D080h	ECM	ECM error pulse configuration register	ECMEPCFG	8	8
A007 D084h	ECM	ECM maskable interrupt configuration register 0	ECMMICFG0	32	32
A007 D088h	ECM	ECM maskable interrupt configuration register 1	ECMMICFG1	32	32
A007 D08Ch	ECM	ECM maskable interrupt configuration register 2	ECMMICFG2	32	32
A007 D090h	ECM	ECM non-maskable interrupt configuration register 0	ECMNMICFG0	32	32
A007 D094h	ECM	ECM non-maskable interrupt configuration register 1	ECMNMICFG1	32	32
A007 D098h	ECM	ECM non-maskable interrupt configuration register 2	ECMNMICFG2	32	32
A007 D09Ch	ECM	ECM internal reset configuration register 0	ECMIRCFG0	32	32
A007 D0A0h	ECM	ECM internal reset configuration register 1	ECMIRCFG1	32	32
A007 D0A4h	ECM	ECM internal reset configuration register 2	ECMIRCFG2	32	32
A007 D0A8h	ECM	ECM error mask register 0	ECMEMK0	32	32
A007 D0ACh	ECM	ECM error mask register 1	ECMEMK1	32	32
A007 D0B0h	ECM	ECM error mask register 2	ECMEMK2	32	32
A007 D0B4h	ECM	ECM Error Source Status Clear Trigger Register 0	ECMESSTC0	32	32
A007 D0B8h	ECM	ECM Error Source Status Clear Trigger Register 1	ECMESSTC1	32	32
A007 D0BCh	ECM	ECM Error Source Status Clear Trigger Register 2	ECMESSTC2	32	32
A007 D0C0h	ECM	ECM protection command register	ECMPCMD1	32	32
A007 D0C4h	ECM	ECM protection status register	ECMPS	8	8
A007 D0C8h	ECM	ECM pseudo error trigger register 0	ECMPE0	32	32
A007 D0CCh	ECM	ECM pseudo error trigger register 1	ECMPE1	32	32
A007 D0D0h	ECM	ECM pseudo error trigger register 2	ECMPE2	32	32
A007 D0D4h	ECM	ECM delay timer control register	ECMDTMCTL	8	8
A007 D0D8h	ECM	ECM delay timer register	ECMDTMR	16	16
A007 D0DCh	ECM	ECM delay timer compare register	ECMDTMCMP	32	32
A007 D0E0h	ECM	ECM delay timer configuration register 0	ECMDTMCFG0	32	32
A007 D0E4h	ECM	ECM delay timer configuration register 1	ECMDTMCFG1	32	32
A007 D0E8h	ECM	ECM delay timer configuration register 2	ECMDTMCFG2	32	32
A007 D0ECh	ECM	ECM delay timer configuration register 3	ECMDTMCFG3	32	32
A007 D0F0h	ECM	ECM delay timer configuration register 4	ECMDTMCFG4	32	32
A007 D0F4h	ECM	ECM delay timer configuration register 5	ECMDTMCFG5	32	32
A007 D0F8h	ECM	ECM Error Output Clear Disable Configuration Register	ECMEOCCFG	32	32
A008 0000h	CMT	Compare match timer start register 0	CMSTR0	16	16
A008 0002h	CMT0	Compare match timer control register	CMCR	16	16
A008 0004h	CMT0	Compare match timer counter	CMCNT	16	16
A008 0006h	CMT0	Compare match timer constant register	CMCOR	16	16
A008 0008h	CMT1	Compare match timer control register	CMCR	16	16
A008 000Ah	CMT1	Compare match timer counter	CMCNT	16	16
A008 000Ch	CMT1	Compare match timer constant register	CMCOR	16	16
A008 0020h	CMT	Compare match timer start register 1	CMSTR1	16	16
A008 0022h	CMT2	Compare match timer control register	CMCR	16	16
A008 0024h	CMT2	Compare match timer counter	CMCNT	16	16
A008 0026h	CMT2	Compare match timer constant register	CMCOR	16	16
A008 0028h	CMT3	Compare match timer control register	CMCR	16	16
A008 002Ah	CMT3	Compare match timer counter	CMCNT	16	16
A008 002Ch	CMT3	Compare match timer constant register	CMCOR	16	16
A008 0040h	CMT	Compare match timer start register 2	CMSTR2	16	16

Table 5.1 List of I/O Registers (Address Order) (66 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 0042h	CMT4	Compare match timer control register	CMCR	16	16
A008 0044h	CMT4	Compare match timer counter	CMCNT	16	16
A008 0046h	CMT4	Compare match timer constant register	CMCOR	16	16
A008 0048h	CMT5	Compare match timer control register	CMCR	16	16
A008 004Ah	CMT5	Compare match timer counter	CMCNT	16	16
A008 004Ch	CMT5	Compare match timer constant register	CMCOR	16	16
A008 0100h	TPUA	Timer start register	TSTRA	8	8
A008 0101h	TPUA	Timer synchronous register	TSYRA	8	8
A008 0108h	TPU0	Noise filter control register	NFCR	8	8
A008 0109h	TPU1	Noise filter control register	NFCR	8	8
A008 010Ah	TPU2	Noise filter control register	NFCR	8	8
A008 010Bh	TPU3	Noise filter control register	NFCR	8	8
A008 010Ch	TPU4	Noise filter control register	NFCR	8	8
A008 010Dh	TPU5	Noise filter control register	NFCR	8	8
A008 0110h	TPU0	Timer control register	TCR	8	8
A008 0111h	TPU0	Timer mode register	TMDR	8	8
A008 0112h	TPU0	Timer I/O control register	TIORH	8	8
A008 0113h	TPU0	Timer I/O control register	TIORL	8	8
A008 0114h	TPU0	Timer interrupt enable register	TIER	8	8
A008 0115h	TPU0	Timer status register	TSR	8	8
A008 0116h	TPU0	Timer counter	TCNT	16	16
A008 0118h	TPU0	Timer general register A	TGRA	16	16
A008 011Ah	TPU0	Timer general register B	TGRB	16	16
A008 011Ch	TPU0	Timer general register C	TGRC	16	16
A008 011Eh	TPU0	Timer general register D	TGRD	16	16
A008 0120h	TPU1	Timer control register	TCR	8	8
A008 0121h	TPU1	Timer mode register	TMDR	8	8
A008 0122h	TPU1	Timer I/O control register	TIOR	8	8
A008 0124h	TPU1	Timer interrupt enable register	TIER	8	8
A008 0125h	TPU1	Timer status register	TSR	8	8
A008 0126h	TPU1	Timer counter	TCNT	16	16
A008 0128h	TPU1	Timer general register A	TGRA	16	16
A008 012Ah	TPU1	Timer general register B	TGRB	16	16
A008 0130h	TPU2	Timer control register	TCR	8	8
A008 0131h	TPU2	Timer mode register	TMDR	8	8
A008 0132h	TPU2	Timer I/O control register	TIOR	8	8
A008 0134h	TPU2	Timer interrupt enable register	TIER	8	8
A008 0135h	TPU2	Timer status register	TSR	8	8
A008 0136h	TPU2	Timer counter	TCNT	16	16
A008 0138h	TPU2	Timer general register A	TGRA	16	16
A008 013Ah	TPU2	Timer general register B	TGRB	16	16
A008 0140h	TPU3	Timer control register	TCR	8	8
A008 0141h	TPU3	Timer mode register	TMDR	8	8
A008 0142h	TPU3	Timer I/O control register	TIORH	8	8
A008 0143h	TPU3	Timer I/O control register	TIORL	8	8
A008 0144h	TPU3	Timer interrupt enable register	TIER	8	8
A008 0145h	TPU3	Timer status register	TSR	8	8
A008 0146h	TPU3	Timer counter	TCNT	16	16

Table 5.1 List of I/O Registers (Address Order) (67 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 0148h	TPU3	Timer general register A	TGRA	16	16
A008 014Ah	TPU3	Timer general register B	TGRB	16	16
A008 014Ch	TPU3	Timer general register C	TGRC	16	16
A008 014Eh	TPU3	Timer general register D	TGRD	16	16
A008 0150h	TPU4	Timer control register	TCR	8	8
A008 0151h	TPU4	Timer mode register	TMDR	8	8
A008 0152h	TPU4	Timer I/O control register	TIOR	8	8
A008 0154h	TPU4	Timer interrupt enable register	TIER	8	8
A008 0155h	TPU4	Timer status register	TSR	8	8
A008 0156h	TPU4	Timer counter	TCNT	16	16
A008 0158h	TPU4	Timer general register A	TGRA	16	16
A008 015Ah	TPU4	Timer general register B	TGRB	16	16
A008 0160h	TPU5	Timer control register	TCR	8	8
A008 0161h	TPU5	Timer mode register	TMDR	8	8
A008 0162h	TPU5	Timer I/O control register	TIOR	8	8
A008 0164h	TPU5	Timer interrupt enable register	TIER	8	8
A008 0165h	TPU5	Timer status register	TSR	8	8
A008 0166h	TPU5	Timer counter	TCNT	16	16
A008 0168h	TPU5	Timer general register A	TGRA	16	16
A008 016Ah	TPU5	Timer general register B	TGRB	16	16
A008 0180h	TPUA	Timer start register	TSTRB	8	8
A008 0181h	TPUA	Timer synchronous register	TSYRB	8	8
A008 0188h	TPU6	Noise filter control register	NFCR	8	8
A008 0189h	TPU7	Noise filter control register	NFCR	8	8
A008 018Ah	TPU8	Noise filter control register	NFCR	8	8
A008 018Bh	TPU9	Noise filter control register	NFCR	8	8
A008 018Ch	TPU10	Noise filter control register	NFCR	8	8
A008 018Dh	TPU11	Noise filter control register	NFCR	8	8
A008 0190h	TPU6	Timer control register	TCR	8	8
A008 0191h	TPU6	Timer mode register	TMDR	8	8
A008 0192h	TPU6	Timer I/O control register	TIORH	8	8
A008 0193h	TPU6	Timer I/O control register	TIORL	8	8
A008 0194h	TPU6	Timer interrupt enable register	TIER	8	8
A008 0195h	TPU6	Timer status register	TSR	8	8
A008 0196h	TPU6	Timer counter	TCNT	16	16
A008 0198h	TPU6	Timer general register A	TGRA	16	16
A008 019Ah	TPU6	Timer general register B	TGRB	16	16
A008 019Ch	TPU6	Timer general register C	TGRC	16	16
A008 019Eh	TPU6	Timer general register D	TGRD	16	16
A008 01A0h	TPU7	Timer control register	TCR	8	8
A008 01A1h	TPU7	Timer mode register	TMDR	8	8
A008 01A2h	TPU7	Timer I/O control register	TIOR	8	8
A008 01A4h	TPU7	Timer interrupt enable register	TIER	8	8
A008 01A5h	TPU7	Timer status register	TSR	8	8
A008 01A6h	TPU7	Timer counter	TCNT	16	16
A008 01A8h	TPU7	Timer general register A	TGRA	16	16
A008 01AAh	TPU7	Timer general register B	TGRB	16	16
A008 01B0h	TPU8	Timer control register	TCR	8	8

Table 5.1 List of I/O Registers (Address Order) (68 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 01B1h	TPU8	Timer mode register	TMDR	8	8
A008 01B2h	TPU8	Timer I/O control register	TIOR	8	8
A008 01B4h	TPU8	Timer interrupt enable register	TIER	8	8
A008 01B5h	TPU8	Timer status register	TSR	8	8
A008 01B6h	TPU8	Timer counter	TCNT	16	16
A008 01B8h	TPU8	Timer general register A	TGRA	16	16
A008 01BAh	TPU8	Timer general register B	TGRB	16	16
A008 01C0h	TPU9	Timer control register	TCR	8	8
A008 01C1h	TPU9	Timer mode register	TMDR	8	8
A008 01C2h	TPU9	Timer I/O control register	TIORH	8	8
A008 01C3h	TPU9	Timer I/O control register	TIORL	8	8
A008 01C4h	TPU9	Timer interrupt enable register	TIER	8	8
A008 01C5h	TPU9	Timer status register	TSR	8	8
A008 01C6h	TPU9	Timer counter	TCNT	16	16
A008 01C8h	TPU9	Timer general register A	TGRA	16	16
A008 01CAh	TPU9	Timer general register B	TGRB	16	16
A008 01CCh	TPU9	Timer general register C	TGRC	16	16
A008 01CEh	TPU9	Timer general register D	TGRD	16	16
A008 01D0h	TPU10	Timer control register	TCR	8	8
A008 01D1h	TPU10	Timer mode register	TMDR	8	8
A008 01D2h	TPU10	Timer I/O control register	TIOR	8	8
A008 01D4h	TPU10	Timer interrupt enable register	TIER	8	8
A008 01D5h	TPU10	Timer status register	TSR	8	8
A008 01D6h	TPU10	Timer counter	TCNT	16	16
A008 01D8h	TPU10	Timer general register A	TGRA	16	16
A008 01DAh	TPU10	Timer general register B	TGRB	16	16
A008 01E0h	TPU11	Timer control register	TCR	8	8
A008 01E1h	TPU11	Timer mode register	TMDR	8	8
A008 01E2h	TPU11	Timer I/O control register	TIOR	8	8
A008 01E4h	TPU11	Timer interrupt enable register	TIER	8	8
A008 01E5h	TPU11	Timer status register	TSR	8	8
A008 01E6h	TPU11	Timer counter	TCNT	16	16
A008 01E8h	TPU11	Timer general register A	TGRA	16	16
A008 01EAh	TPU11	Timer general register B	TGRB	16	16
A008 0200h	TPUSL	PWM feedback select register	PWMFBSLR	32	32
A008 0300h	CMTW0	Timer start register	CMWSTR	16	16
A008 0304h	CMTW0	Timer control register	CMWCR	16	16
A008 0308h	CMTW0	Timer I/O control register	CMWIOR	16	16
A008 0310h	CMTW0	Timer counter	CMWCNT	32	32
A008 0314h	CMTW0	Compare match constant register	CMWCOR	32	32
A008 0318h	CMTW0	Input capture register 0	CMWICR0	32	32
A008 031Ch	CMTW0	Input capture register 1	CMWICR1	32	32
A008 0320h	CMTW0	Output compare register 0	CMWOCR0	32	32
A008 0324h	CMTW0	Output compare register 1	CMWOCR1	32	32
A008 0380h	CMTW1	Timer start register	CMWSTR	16	16
A008 0384h	CMTW1	Timer control register	CMWCR	16	16
A008 0388h	CMTW1	Timer I/O control register	CMWIOR	16	16
A008 0390h	CMTW1	Timer counter	CMWCNT	32	32

Table 5.1 List of I/O Registers (Address Order) (69 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 0394h	CMTW1	Compare match constant register	CMWCOR	32	32
A008 0398h	CMTW1	Input capture register 0	CMWICR0	32	32
A008 039Ch	CMTW1	Input capture register 1	CMWICR1	32	32
A008 03A0h	CMTW1	Output compare register 0	CMWOCR0	32	32
A008 03A4h	CMTW1	Output compare register 1	CMWOCR1	32	32
A008 0400h	CMTW	Digital noise filter control register 0	NFCR0	32	32
A008 0404h	CMTW	Digital noise filter control register 1	NFCR1	32	32
A008 0410h	CMTW	ECM dynamic mode error output select register	ECDMESLR	32	32
A008 0506h	PPG0	PPG output control register	PCR	8	8
A008 0507h	PPG0	PPG output mode register	PMR	8	8
A008 0508h	PPG0	Next data enable register H	NDERH	8	8
A008 0509h	PPG0	Next data enable register L	NDERL	8	8
A008 050Ah	PPG0	Output data register H	PODRH	8	8
A008 050Bh	PPG0	Output data register L	PODRL	8	8
A008 050Ch	PPG0	Next data register H	NDRH	8	8
A008 050Dh	PPG0	Next data register L	NDRL	8	8
A008 050Eh	PPG0	Next data register H	NDRH2	8	8
A008 050Fh	PPG0	Next data register L	NDRL2	8	8
A008 0516h	PPG1	PPG output control register	PCR	8	8
A008 0517h	PPG1	PPG output mode register	PMR	8	8
A008 0518h	PPG1	Next data enable register H	NDERH	8	8
A008 0519h	PPG1	Next data enable register L	NDERL	8	8
A008 051Ah	PPG1	Output data register H	PODRH	8	8
A008 051Bh	PPG1	Output data register L	PODRL	8	8
A008 051Ch	PPG1	Next data register H	NDRH	8	8
A008 051Dh	PPG1	Next data register L	NDRL	8	8
A008 051Eh	PPG1	Next data register H	NDRH2	8	8
A008 051Fh	PPG1	Next data register L	NDRL2	8	8
A008 0520h	PPG1	PPG trigger select register	PTRSLR	8	8
A008 0600h	WDT0	WDT refresh register	WDTRR	8	8
A008 0602h	WDT0	WDT control register	WDTCR	16	16
A008 0604h	WDT0	WDT status register	WDTSR	16	16
A008 0606h	WDT0	WDT reset control register	WDTRCR	8	8
A008 0620h	WDT1*1	WDT refresh register	WDTRR	8	8
A008 0622h	WDT1*1	WDT control register	WDTCR	16	16
A008 0624h	WDT1*1	WDT status register	WDTSR	16	16
A008 0626h	WDT1*1	WDT reset control register	WDTRCR	8	8
A008 0700h	IWDT	IWDT refresh register	IWDTRR	8	8
A008 0702h	IWDT	IWDT control register	IWDTCR	16	16
A008 0704h	IWDT	IWDT status register	IWDTSR	16	16
A008 0706h	IWDT	IWDT reset control register	IWDTRCR	8	8
A008 0800h	POE3	Input level control/status register 1	ICSR1	16	16
A008 0802h	POE3	Output level control/status register 1	OCSR1	16	16
A008 0804h	POE3	Input level control/status register 2	ICSR2	16	16
A008 0806h	POE3	Output level control/status register 2	OCSR2	16	16
A008 0808h	POE3	Input level control/status register 3	ICSR3	16	16
A008 080Ah	POE3	Software port output enable register	SPOER	8	8
A008 080Bh	POE3	Port output enable control register 1	POECR1	8	8

Table 5.1 List of I/O Registers (Address Order) (70 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 080Ch	POE3	Port output enable control register 2	POECR2	16	16
A008 080Eh	POE3	Port output enable control register 3	POECR3	16	16
A008 0810h	POE3	Port output enable control register 4	POECR4	16	16
A008 0812h	POE3	Port output enable control register 5	POECR5	16	16
A008 0814h	POE3	Port output enable control register 6	POECR6	16	16
A008 0816h	POE3	Input level control/status register 4	ICSR4	16	16
A008 0818h	POE3	Input level control/status register 5	ICSR5	16	16
A008 081Ah	POE3	Active level register 1	ALR1	16	16
A008 081Ch	POE3	Input level control/status register 6	ICSR6	16	16
A008 0823h	POE3	GPT3 pin select register	G3SELR	8	8
A008 0824h	POE3	MTU0 pin select register 1	M0SELR1	8	8
A008 0825h	POE3	MTU0 pin select register 2	M0SELR2	8	8
A008 0826h	POE3	MTU3 pin select register	M3SELR	8	8
A008 0827h	POE3	MTU4 pin select register 1	M4SELR1	8	8
A008 0828h	POE3	MTU4 pin select register 2	M4SELR2	8	8
A008 0900h	RIIC0	I2C bus control register 1	ICCR1	8	8
A008 0901h	RIIC0	I2C bus control register 2	ICCR2	8	8
A008 0902h	RIIC0	I2C bus mode register 1	ICMR1	8	8
A008 0903h	RIIC0	I2C bus mode register 2	ICMR2	8	8
A008 0904h	RIIC0	I2C bus mode register 3	ICMR3	8	8
A008 0905h	RIIC0	I2C bus function enable register	ICFER	8	8
A008 0906h	RIIC0	I2C bus status enable register	ICSER	8	8
A008 0907h	RIIC0	I2C bus interrupt enable register	ICIER	8	8
A008 0908h	RIIC0	I2C bus status register 1	ICSR1	8	8
A008 0909h	RIIC0	I2C bus status register 2	ICSR2	8	8
A008 090Ah	RIIC0	Slave address register L0	ICSARL0	8	8
A008 090Bh	RIIC0	Slave address register U0	ICSARU0	8	8
A008 090Ch	RIIC0	Slave address register L1	ICSARL1	8	8
A008 090Dh	RIIC0	Slave address register U1	ICSARU1	8	8
A008 090Eh	RIIC0	Slave address register L2	ICSARL2	8	8
A008 090Fh	RIIC0	Slave address register U2	ICSARU2	8	8
A008 0910h	RIIC0	I2C bus bitrate low register	ICBRL	8	8
A008 0911h	RIIC0	I2C bus bitrate high register	ICBRH	8	8
A008 0912h	RIIC0	I2C bus transmit data register	ICDRT	8	8
A008 0913h	RIIC0	I2C bus receive data register	ICDRR	8	8
A008 0940h	RIIC1	I2C bus control register 1	ICCR1	8	8
A008 0941h	RIIC1	I2C bus control register 2	ICCR2	8	8
A008 0942h	RIIC1	I2C bus mode register 1	ICMR1	8	8
A008 0943h	RIIC1	I2C bus mode register 2	ICMR2	8	8
A008 0944h	RIIC1	I2C bus mode register 3	ICMR3	8	8
A008 0945h	RIIC1	I2C bus function enable register	ICFER	8	8
A008 0946h	RIIC1	I2C bus status enable register	ICSER	8	8
A008 0947h	RIIC1	I2C bus interrupt enable register	ICIER	8	8
A008 0948h	RIIC1	I2C bus status register 1	ICSR1	8	8
A008 0949h	RIIC1	I2C bus status register 2	ICSR2	8	8
A008 094Ah	RIIC1	Slave address register L0	ICSARL0	8	8
A008 094Bh	RIIC1	Slave address register U0	ICSARU0	8	8
A008 094Ch	RIIC1	Slave address register L1	ICSARL1	8	8

Table 5.1 List of I/O Registers (Address Order) (71 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 094Dh	RIIC1	Slave address register U1	ICSARU1	8	8
A008 094Eh	RIIC1	Slave address register L2	ICSARL2	8	8
A008 094Fh	RIIC1	Slave address register U2	ICSARU2	8	8
A008 0950h	RIIC1	I2C bus bitrate low register	ICBRL	8	8
A008 0951h	RIIC1	I2C bus bitrate high register	ICBRH	8	8
A008 0952h	RIIC1	I2C bus transmit data register	ICDRT	8	8
A008 0953h	RIIC1	I2C bus receive data register	ICDRR	8	8
A008 0A00h	TSN	Temperature sensor control register	TSCR	8	8
A008 0B00h	ELC	Event link control register	ELCR	8	8
A008 0B01h	ELC	Event link setting register 0	ELSR0	8	8
A008 0B04h	ELC	Event link setting register 3	ELSR3	8	8
A008 0B05h	ELC	Event link setting register 4	ELSR4	8	8
A008 0B08h	ELC	Event link setting register 7	ELSR7	8	8
A008 0B0Bh	ELC	Event link setting register 10	ELSR10	8	8
A008 0B0Ch	ELC	Event link setting register 11	ELSR11	8	8
A008 0B0Dh	ELC	Event link setting register 12	ELSR12	8	8
A008 0B0Eh	ELC	Event link setting register 13	ELSR13	8	8
A008 0B10h	ELC	Event link setting register 15	ELSR15	8	8
A008 0B11h	ELC	Event link setting register 16	ELSR16	8	8
A008 0B13h	ELC	Event link setting register 18	ELSR18	8	8
A008 0B14h	ELC	Event link setting register 19	ELSR19	8	8
A008 0B15h	ELC	Event link setting register 20	ELSR20	8	8
A008 0B16h	ELC	Event link setting register 21	ELSR21	8	8
A008 0B17h	ELC	Event link setting register 22	ELSR22	8	8
A008 0B18h	ELC	Event link setting register 23	ELSR23	8	8
A008 0B19h	ELC	Event link setting register 24	ELSR24	8	8
A008 0B1Ah	ELC	Event link setting register 25	ELSR25	8	8
A008 0B1Bh	ELC	Event link setting register 26	ELSR26	8	8
A008 0B1Ch	ELC	Event link setting register 27	ELSR27	8	8
A008 0B1Dh	ELC	Event link setting register 28	ELSR28	8	8
A008 0B1Fh	ELC	Event link option setting register A	ELOPA	8	8
A008 0B20h	ELC	Event link option setting register B	ELOPB	8	8
A008 0B21h	ELC	Event link option setting register C	ELOPC	8	8
A008 0B22h	ELC	Event link option setting register D	ELOPD	8	8
A008 0B23h	ELC	Port group setting register 1	PGR1	8	8
A008 0B24h	ELC	Port group setting register 2	PGR2	8	8
A008 0B25h	ELC	Port group control register 1	PGC1	8	8
A008 0B26h	ELC	Port group control register 2	PGC2	8	8
A008 0B27h	ELC	Port buffer register 1	PDBF1	8	8
A008 0B28h	ELC	Port buffer register 2	PDBF2	8	8
A008 0B29h	ELC	Event link port setting register 0	PEL0	8	8
A008 0B2Ah	ELC	Event link port setting register 1	PEL1	8	8
A008 0B2Bh	ELC	Event link port setting register 2	PEL2	8	8
A008 0B2Ch	ELC	Event link port setting register 3	PEL3	8	8
A008 0B2Dh	ELC	Event link software event generation register	ELSEGR	8	8
A008 0B31h	ELC	Event link setting register 33	ELSR33	8	8
A008 0B33h	ELC	Event link setting register 35	ELSR35	8	8
A008 0B34h	ELC	Event link setting register 36	ELSR36	8	8

Table 5.1 List of I/O Registers (Address Order) (72 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 0B35h	ELC	Event link setting register 37	ELSR37	8	8
A008 0B36h	ELC	Event link setting register 38	ELSR38	8	8
A008 0B39h	ELC	Event link setting register 41	ELSR41	8	8
A008 0B3Ah	ELC	Event link setting register 42	ELSR42	8	8
A008 0B3Bh	ELC	Event link setting register 43	ELSR43	8	8
A008 0B3Ch	ELC	Event link setting register 44	ELSR44	8	8
A008 0B3Dh	ELC	Event link setting register 45	ELSR45	8	8
A008 0B3Fh	ELC	Event link option setting register F	ELOPF	8	8
A008 0B41h	ELC	Event link option setting register H	ELOPH	8	8
A008 0B42h	ELC	Event link option setting register I	ELOPI	8	8
A008 0B43h	ELC	Event link option setting register J	ELOPJ	8	8
A008 1000h	SSI	Control register	SSICR	32	32
A008 1004h	SSI	Status register	SSISR	32	32
A008 1010h	SSI	FIFO control register	SSIFCR	32	32
A008 1014h	SSI	FIFO status register	SSIFSR	32	32
A008 1018h	SSI	Transmit FIFO data register	SSIFTDR	32	32
A008 101Ch	SSI	Receive FIFO data register	SSIFRDR	32	32
A008 1020h	SSI	TDM mode register	SSITDMR	32	32
A008 1200h	DOC	DOC control register	DOCR	8	8
A008 1202h	DOC	DOC data input register	DODIR	16	16
A008 1204h	DOC	DOC data setting register	DODSR	16	16
A008 C000h	S12ADC0	A/D control register	ADCSR	16	16
A008 C004h	S12ADC0	A/D channel select register A	ADANSA	16	16
A008 C008h	S12ADC0	A/D conversion value addition/average mode select register	ADADS	16	16
A008 C00Ch	S12ADC0	A/D conversion value addition/average number select register	ADADC	8	8
A008 C00Eh	S12ADC0	A/D control extended register	ADCER	16	16
A008 C010h	S12ADC0	A/D start trigger select register	ADSTRGR	16	16
A008 C012h	S12ADC0	A/D conversion extended input control register	ADEXICR	16	16
A008 C014h	S12ADC0	A/D channel select register B	ADANSB	16	16
A008 C018h	S12ADC0	A/D data duplicate register	ADDBLDR	16	16
A008 C01Ah	S12ADC0	A/D temperature sensor data register	ADTSDR	16	16
A008 C01Eh	S12ADC0	A/D self-diagnostic data register	ADRD	16	16
A008 C020h	S12ADC0	A/D data register 0	ADDR0	16	16
A008 C022h	S12ADC0	A/D data register 1	ADDR1	16	16
A008 C024h	S12ADC0	A/D data register 2	ADDR2	16	16
A008 C026h	S12ADC0	A/D data register 3	ADDR3	16	16
A008 C028h	S12ADC0	A/D data register 4	ADDR4	16	16
A008 C02Ah	S12ADC0	A/D data register 5	ADDR5	16	16
A008 C02Ch	S12ADC0	A/D data register 6	ADDR6	16	16
A008 C02Eh	S12ADC0	A/D data register 7	ADDR7	16	16
A008 C060h	S12ADC0	A/D sampling state register 0	ADSSTR0	8	8
A008 C066h	S12ADC0	A/D sampling state register control register	ADSHCR	16	16
A008 C070h	S12ADC0	A/D sampling state register T	ADSSTRT	8	8
A008 C073h	S12ADC0	A/D sampling state register 1	ADSSTR1	8	8
A008 C074h	S12ADC0	A/D sampling state register 2	ADSSTR2	8	8
A008 C075h	S12ADC0	A/D sampling state register 3	ADSSTR3	8	8
A008 C076h	S12ADC0	A/D sampling state register 4	ADSSTR4	8	8
A008 C077h	S12ADC0	A/D sampling state register 5	ADSSTR5	8	8

Table 5.1 List of I/O Registers (Address Order) (73 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 C078h	S12ADC0	A/D sampling state register 6	ADSSTR6	8	8
A008 C079h	S12ADC0	A/D sampling state register 7	ADSSTR7	8	8
A008 C07Ah	S12ADC0	A/D disconnection detect control register	ADDISCR	8	8
A008 C080h	S12ADC0	A/D group scan priority control register	ADGSPCR	16	16
A008 C084h	S12ADC0	A/D data duplicate register A	ADDBLDRA	16	16
A008 C086h	S12ADC0	A/D data duplicate register B	ADDBLDRB	16	16
A008 C090h	S12ADC0	A/D compare control register	ADCMPCR	8	8
A008 C092h	S12ADC0	A/D compare channel select extended register	ADCMPANSER	8	8
A008 C093h	S12ADC0	A/D compare level extended select register	ADCMPLER	8	8
A008 C094h	S12ADC0	A/D compare channel select register	ADCMPANSR	16	16
A008 C098h	S12ADC0	A/D compare level register	ADCMPLR	16	16
A008 C09Ch	S12ADC0	A/D compare data register 0	ADCMPDR0	16	16
A008 C09Eh	S12ADC0	A/D compare data register 1	ADCMPDR1	16	16
A008 C0A0h	S12ADC0	A/D compare status register	ADCMPSR	16	16
A008 C0A4h	S12ADC0	A/D compare status extended register	ADCMPSER	8	8
A008 C0C8h	S12ADC0	A/D pin level self-diagnosis control register	ADTDCR	8	8
A008 C0CAh	S12ADC0	A/D error control register	ADERCR	8	8
A008 C0CBh	S12ADC0	A/D error clear register	ADERCLR	8	8
A008 C0D2h	S12ADC0	A/D overwrite error register	ADOWER	16	16
A008 C0D6h	S12ADC0	A/D overwrite error extended register	ADOWEER	16	16
A008 C400h	S12ADC1	A/D control register	ADCSR	16	16
A008 C404h	S12ADC1	A/D channel select register A	ADANSA	16	16
A008 C408h	S12ADC1	A/D conversion value addition/average mode select register	ADADS	16	16
A008 C40Ch	S12ADC1	A/D conversion value addition/average number select register	ADADC	8	8
A008 C40Eh	S12ADC1	A/D control extended register	ADCER	16	16
A008 C410h	S12ADC1	A/D start trigger select register	ADSTRGR	16	16
A008 C412h	S12ADC1	A/D conversion extended input control register	ADEXICR	16	16
A008 C414h	S12ADC1	A/D channel select register B	ADANSB	16	16
A008 C418h	S12ADC1	A/D data duplicate register	ADDBLDR	16	16
A008 C41Eh	S12ADC1	A/D self-diagnostic data register	ADRD	16	16
A008 C420h	S12ADC1	A/D data register 0	ADDR0	16	16
A008 C422h	S12ADC1	A/D data register 1	ADDR1	16	16
A008 C424h	S12ADC1	A/D data register 2	ADDR2	16	16
A008 C426h	S12ADC1	A/D data register 3	ADDR3	16	16
A008 C428h	S12ADC1	A/D data register 4	ADDR4	16	16
A008 C42Ah	S12ADC1	A/D data register 5	ADDR5	16	16
A008 C42Ch	S12ADC1	A/D data register 6	ADDR6	16	16
A008 C42Eh	S12ADC1	A/D data register 7	ADDR7	16	16
A008 C430h	S12ADC1	A/D data register 8	ADDR8	16	16
A008 C432h	S12ADC1	A/D data register 9	ADDR9	16	16
A008 C434h	S12ADC1	A/D data register 10	ADDR10	16	16
A008 C436h	S12ADC1	A/D data register 11	ADDR11	16	16
A008 C438h	S12ADC1	A/D data register 12	ADDR12	16	16
A008 C43Ah	S12ADC1	A/D data register 13	ADDR13	16	16
A008 C43Ch	S12ADC1	A/D data register 14	ADDR14	16	16
A008 C43Eh	S12ADC1	A/D data register 15	ADDR15	16	16
A008 C460h	S12ADC1	A/D sampling state register 0	ADSSTR0	8	8
A008 C461h	S12ADC1	A/D sampling state register L	ADSSTRL	8	8

Table 5.1 List of I/O Registers (Address Order) (74 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A008 C473h	S12ADC1	A/D sampling state register 1	ADSSTR1	8	8
A008 C474h	S12ADC1	A/D sampling state register 2	ADSSTR2	8	8
A008 C475h	S12ADC1	A/D sampling state register 3	ADSSTR3	8	8
A008 C476h	S12ADC1	A/D sampling state register 4	ADSSTR4	8	8
A008 C477h	S12ADC1	A/D sampling state register 5	ADSSTR5	8	8
A008 C478h	S12ADC1	A/D sampling state register 6	ADSSTR6	8	8
A008 C479h	S12ADC1	A/D sampling state register 7	ADSSTR7	8	8
A008 C47Ah	S12ADC1	A/D disconnection detect control register	ADDISCR	8	8
A008 C480h	S12ADC1	A/D group scan priority control register	ADGSPCR	16	16
A008 C484h	S12ADC1	A/D data duplicate register A	ADDBLDRA	16	16
A008 C486h	S12ADC1	A/D data duplicate register B	ADDBLDRB	16	16
A008 C490h	S12ADC1	A/D compare control register	ADCMPCR	8	8
A008 C494h	S12ADC1	A/D compare channel select register	ADCMPANSR	16	16
A008 C498h	S12ADC1	A/D compare level register	ADCMPLR	16	16
A008 C49Ch	S12ADC1	A/D compare data register 0	ADCMPDR0	16	16
A008 C49Eh	S12ADC1	A/D compare data register 1	ADCMPDR1	16	16
A008 C4A0h	S12ADC1	A/D compare status register	ADCMPSR	16	16
A008 C4C8h	S12ADC1	A/D pin level self-diagnosis control register	ADTDCR	8	8
A008 C4CAh	S12ADC1	A/D error control register	ADERCR	8	8
A008 C4CBh	S12ADC1	A/D error clear register	ADERCLR	8	8
A008 C4D2h	S12ADC1	A/D overwrite error register	ADOWER	16	16
A008 C4D6h	S12ADC1	A/D overwrite error extended register	ADOWEER	16	16
A009 0000h	CLMA0	CLMA0 control register 0	CLMA0CTL0	8	8
A009 0008h	CLMA0	CLMA0 compare register L	CLMA0CMPL	16	16
A009 000Ch	CLMA0	CLMA0 compare register H	CLMA0CMPH	16	16
A009 0010h	CLMA0	CLMA0 command register	CLMA0PCMD	8	8
A009 0014h	CLMA0	CLMA0 protection status register	CLMA0PS	8	8
A009 0020h	CLMA1	CLMA1 control register 0	CLMA1CTL0	8	8
A009 0028h	CLMA1	CLMA1 compare register L	CLMA1CMPL	16	16
A009 002Ch	CLMA1	CLMA1 compare register H	CLMA1CMPH	16	16
A009 0030h	CLMA1	CLMA1 command register	CLMA1PCMD	8	8
A009 0034h	CLMA1	CLMA1 protection status register	CLMA1PS	8	8
A009 0040h	CLMA2	CLMA2 control register 0	CLMA2CTL0	8	8
A009 0048h	CLMA2	CLMA2 compare register L	CLMA2CMPL	16	16
A009 004Ch	CLMA2	CLMA2 compare register H	CLMA2CMPH	16	16
A009 0050h	CLMA2	CLMA2 command register	CLMA2PCMD	8	8
A009 0054h	CLMA2	CLMA2 protection status register	CLMA2PS	8	8
A009 4000h	DMA0	DMAC unit 0 source select register 0	DMA0SEL0	32	32
A009 4004h	DMA0	DMAC unit 0 source select register 1	DMA0SEL1	32	32
A009 4008h	DMA0	DMAC unit 0 source select register 2	DMA0SEL2	32	32
A009 400Ch	DMA0	DMAC unit 0 source select register 3	DMA0SEL3	32	32
A009 4010h	DMA0	DMAC unit 0 source select register 4	DMA0SEL4	32	32
A009 4014h	DMA0	DMAC unit 0 source select register 5	DMA0SEL5	32	32
A009 4018h	DMA0	DMAC unit 0 source select register 6	DMA0SEL6	32	32
A009 401Ch	DMA0	DMAC unit 0 source select register 7	DMA0SEL7	32	32
A009 4020h	DMA0	DMAC unit 0 source select register 8	DMA0SEL8	32	32
A009 4024h	DMA0	DMAC unit 0 source select register 9	DMA0SEL9	32	32
A009 4028h	DMA0	DMAC unit 0 source select register 10	DMA0SEL10	32	32

Table 5.1 List of I/O Registers (Address Order) (75 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A009 402Ch	DMA0	DMAC unit 0 source select register 11	DMA0SEL11	32	32
A009 4030h	DMA0	DMAC unit 0 source select register 12	DMA0SEL12	32	32
A009 4034h	DMA0	DMAC unit 0 source select register 13	DMA0SEL13	32	32
A009 4038h	DMA0	DMAC unit 0 source select register 14	DMA0SEL14	32	32
A009 403Ch	DMA0	DMAC unit 0 source select register 15	DMA0SEL15	32	32
A009 4040h	DMA1	DMAC unit 1 source select register 0	DMA1SEL0	32	32
A009 4044h	DMA1	DMAC unit 1 source select register 1	DMA1SEL1	32	32
A009 4048h	DMA1	DMAC unit 1 source select register 2	DMA1SEL2	32	32
A009 404Ch	DMA1	DMAC unit 1 source select register 3	DMA1SEL3	32	32
A009 4050h	DMA1	DMAC unit 1 source select register 4	DMA1SEL4	32	32
A009 4054h	DMA1	DMAC unit 1 source select register 5	DMA1SEL5	32	32
A009 4058h	DMA1	DMAC unit 1 source select register 6	DMA1SEL6	32	32
A009 405Ch	DMA1	DMAC unit 1 source select register 7	DMA1SEL7	32	32
A009 4060h	DMA1	DMAC unit 1 source select register 8	DMA1SEL8	32	32
A009 4064h	DMA1	DMAC unit 1 source select register 9	DMA1SEL9	32	32
A009 4068h	DMA1	DMAC unit 1 source select register 10	DMA1SEL10	32	32
A009 406Ch	DMA1	DMAC unit 1 source select register 11	DMA1SEL11	32	32
A009 4070h	DMA1	DMAC unit 1 source select register 12	DMA1SEL12	32	32
A009 4074h	DMA1	DMAC unit 1 source select register 13	DMA1SEL13	32	32
A009 4078h	DMA1	DMAC unit 1 source select register 14	DMA1SEL14	32	32
A009 407Ch	DMA1	DMAC unit 1 source select register 15	DMA1SEL15	32	32
A009 4080h	DMAC	DMAC software start register	DMASTG	32	32
A009 4200h	ICU	IRQ control register 0	IRQCR0	32	32
A009 4204h	ICU	IRQ control register 1	IRQCR1	32	32
A009 4208h	ICU	IRQ control register 2	IRQCR2	32	32
A009 420Ch	ICU	IRQ control register 3	IRQCR3	32	32
A009 4210h	ICU	IRQ control register 4	IRQCR4	32	32
A009 4214h	ICU	IRQ control register 5	IRQCR5	32	32
A009 4218h	ICU	IRQ control register 6	IRQCR6	32	32
A009 421Ch	ICU	IRQ control register 7	IRQCR7	32	32
A009 4220h	ICU	IRQ control register 8	IRQCR8	32	32
A009 4224h	ICU	IRQ control register 9	IRQCR9	32	32
A009 4228h	ICU	IRQ control register 10	IRQCR10	32	32
A009 422Ch	ICU	IRQ control register 11	IRQCR11	32	32
A009 4230h	ICU	IRQ control register 12	IRQCR12	32	32
A009 4234h	ICU	IRQ control register 13	IRQCR13	32	32
A009 4238h	ICU	IRQ control register 14	IRQCR14	32	32
A009 423Ch	ICU	IRQ control register 15	IRQCR15	32	32
A009 4240h	ICU	IRQ pin digital noise filter enable register	IRQFLTE	32	32
A009 4244h	ICU	IRQ pin digital noise filter setting register	IRQFLTC	32	32
A009 4248h	ICU	Non-maskable interrupt status register	NMISR	32	32
A009 424Ch	ICU	Non-maskable interrupt status clear register	NMICLR	32	32
A009 4250h	ICU	NMI pin interrupt control register	NMICR	32	32
A009 4254h	ICU	NMI pin digital noise filter enable register	NMIFLTE	32	32
A009 4258h	ICU	NMI pin digital noise filter setting register	NMIFLTC	32	32
A009 425Ch	ICU	Ethernet PHY control register 0	EPHYCR0	32	32
A009 4260h	ICU	Ethernet PHY control register 1	EPHYCR1	32	32
A009 4264h	ICU	Ethernet PHY control register 2	EPHYCR2	32	32

Table 5.1 List of I/O Registers (Address Order) (76 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A009 4268h	ICU	Ethernet PHY interrupt request pin digital noise filter enable register	EPHYFLTE	32	32
A009 426Ch	ICU	Ethernet PHY interrupt request pin digital noise filter setting register	EPHYFLTC	32	32
A009 4270h	ICU	External DMA request pin digital noise filter enable register	DREQFLTE	32	32
A009 4274h	ICU	External DMA request pin digital noise filter setting register	DREQFLTC	32	32
A009 4290h	ICU*1	Inter-CPU interrupt request register	CPUINT	32	32
A00B 0020h	SYSTEM	System clock control register	SCKCR	32	32
A00B 0024h	SYSTEM	System clock control register 2	SCKCR2	32	32
A00B 0028h	SYSTEM	Delta-sigma interface clock control register	DSCR	32	32
A00B 0034h	SYSTEM	PLL1 control register	PLL1CR	32	32
A00B 0038h	SYSTEM	PLL1 control register 2	PLL1CR2	32	32
A00B 0040h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	32	32
A00B 004Ch	SYSTEM	Oscillation stop detect control register	OSTDCR	32	32
A00B 0200h	SYSTEM	Reset status register 0	RSTSR0	32	32
A00B 0210h	SYSTEM	Software reset register	SWRR1	32	32
A00B 0220h	SYSTEM*1	Software reset register 2	SWRR2	32	32
A00B 0248h	SYSTEM	Module reset control register C	MRCTLC	32	32
A00B 0300h	SYSTEM	Module stop control register A	MSTPCRA	32	32
A00B 0304h	SYSTEM	Module stop control register B	MSTPCRB	32	32
A00B 0308h	SYSTEM	Module stop control register C	MSTPCRC	32	32
A00B 030Ch	SYSTEM	Module stop control register D	MSTPCRD	32	32
A00B 0310h	SYSTEM	Module stop control register E	MSTPCRE	32	32
A00B 0314h	SYSTEM	Module stop control register F	MSTPCRF	32	32
A00B 0800h	SYSTEM	ATCM wait control register	SYTATCMWAIT	32	32
A00B 0920h	SYSTEM*1	Semaphore enable register	SYTSEMFEN	32	32
A00B 0930h	SYSTEM*1	Semaphore register 0	SYTSEMF0	32	32
A00B 0934h	SYSTEM*1	Semaphore register 1	SYTSEMF1	32	32
A00B 0938h	SYSTEM*1	Semaphore register 2	SYTSEMF2	32	32
A00B 093Ch	SYSTEM*1	Semaphore register 3	SYTSEMF3	32	32
A00B 0940h	SYSTEM*1	Semaphore register 4	SYTSEMF4	32	32
A00B 0944h	SYSTEM*1	Semaphore register 5	SYTSEMF5	32	32
A00B 0948h	SYSTEM*1	Semaphore register 6	SYTSEMF6	32	32
A00B 094Ch	SYSTEM*1	Semaphore register 7	SYTSEMF7	32	32
A00B 0A00h	SYSTEM	Debug interface control register	DBGIFCNT	32	32
A00B 0A60h	SYSTEM	Mode monitor register	MDMONR	32	32
A00B 0A80h	SYSTEM	ECM mask control register	ECMMCNT	32	32
A00B 0B00h	SYSTEM	Protect register	PRCR	32	32
A00B F000h	ETHERC	Ethernet system protect command register	ETSPCMD	32	32
A00B F004h	ETHERC	MAC select register	MACSEL	32	32
A00B F008h	ETHERC	MII control register 0	MII_CTRL0	32	32
A00B F00Ch	ETHERC	MII control register 1	MII_CTRL1	32	32
A00B F010h	ETHERC	MII control register 2	MII_CTRL2	32	32
A00B F014h	ETHERSW	Ethernet PHY LINK mode register	ETHPHYLNK	32	32
A00B F100h	ECATC*1	EtherCAT PHY Offset Address Setting Register	CATOFFADD	32	32
A00B F104h	ECATC*1	EtherCAT Operation Mode Setting Register	CATEMMD	32	32
A00B F10Ch	ECATC*1	EtherCAT TXC Shift Setting Register	CATTXCSFT	32	32
A00B F110h	ETHERSW	Ethernet switch management TAG control register	ETHSWMTC	32	32
A00B F114h	ETHERSW	Ethernet switch operation mode setting register	ETHSWMD	32	32
A00B F118h	ETHERC	Ethernet peripheral reset register	ETHSFTRST	32	32

Table 5.1 List of I/O Registers (Address Order) (77 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00B F200h	ETHERSW	Timer output enable register	SWTMEN	32	32
A00B F204h	ETHERSW	Timer second start setting register	SWTMSTSEC	32	32
A00B F208h	ETHERSW	Timer nanosecond start setting register	SWTMSTNS	32	32
A00B F20Ch	ETHERSW	Timer second cycle setting register	SWTMPSEC	32	32
A00B F210h	ETHERSW	Timer nanosecond cycle setting register	SWTMPNS	32	32
A00B F214h	ETHERSW	Timer pulse width setting register	SWTMWTH	32	32
A00B F22Ch	ETHERSW	Timer second time holding register	SWTMLATSEC	32	32
A00B F230h	ETHERSW	Timer nanosecond time holding register	SWTMLATNS	32	32
A00C 0008h	ETHERSW	Port enable register	PORT_ENA	32	32
A00C 000Ch	ETHERSW	Unicast default mask register	UCAST_DEFAULT_MASK	32	32
A00C 0014h	ETHERSW	Broadcast default mask register	BCAST_DEFAULT_MASK	32	32
A00C 0018h	ETHERSW	Multicast default mask register	MCAST_DEFAULT_MASK	32	32
A00C 001Ch	ETHERSW	Input learning blocking register	INPUT_LEARN_BLOCK	32	32
A00C 0020h	ETHERSW	Management configuration register	MGMT_CONFIG	32	32
A00C 0024h	ETHERSW	Mode configuration register	MODE_CONFIG	32	32
A00C 0034h	ETHERSW	VLAN tag ID register	VLAN_TAG_ID	32	32
A00C 0080h	ETHERSW	Output queue management status register	OQMGR_STATUS	32	32
A00C 0084h	ETHERSW	Output queue minimum memory register	QMGR_MINCELLS	32	32
A00C 0088h	ETHERSW	Output queue minimum memory statistics register	QMGR_ST_MINCELLS	32	32
A00C 008Ch	ETHERSW	Output queue congestion status register	QMGR_CGS_STAT	32	32
A00C 0090h	ETHERSW	Queue internal interface status register	QMGR_IFACE_STAT	32	32
A00C 0094h	ETHERSW	Queue wait register	QMGR_WEIGHTS	32	32
A00C 0100h	ETHERSW	VLAN priority register 0	VLAN_PRIORITY0	32	32
A00C 0104h	ETHERSW	VLAN priority register 1	VLAN_PRIORITY1	32	32
A00C 0108h	ETHERSW	VLAN priority register 2	VLAN_PRIORITY2	32	32
A00C 0140h	ETHERSW	IP priority register 0	IP_PRIORITY0	32	32
A00C 0144h	ETHERSW	IP priority register 1	IP_PRIORITY1	32	32
A00C 0148h	ETHERSW	IP priority register 2	IP_PRIORITY2	32	32
A00C 0180h	ETHERSW	Priority configuration register 0	PRIORITY_CFG0	32	32
A00C 0184h	ETHERSW	Priority configuration register 1	PRIORITY_CFG1	32	32
A00C 0188h	ETHERSW	Priority configuration register 2	PRIORITY_CFG2	32	32
A00C 01C0h	ETHERSW	Hub control register	HUB_CONTROL	32	32
A00C 01C4h	ETHERSW	Hub status register	HUB_STATS	32	32
A00C 01C8h	ETHERSW	Hub input filter MAC address low register 0	HUB_FLT_MAC0lo	32	32
A00C 01CCh	ETHERSW	Hub input filter MAC address high register 0	HUB_FLT_MAC0hi	32	32
A00C 01D0h	ETHERSW	Hub input filter MAC address low register 1	HUB_FLT_MAC1lo	32	32
A00C 01D4h	ETHERSW	Hub input filter MAC address high register 1	HUB_FLT_MAC1hi	32	32
A00C 01D8h	ETHERSW	Hub input filter MAC address low register 2	HUB_FLT_MAC2lo	32	32
A00C 01DCh	ETHERSW	Hub input filter MAC address high register 2	HUB_FLT_MAC2hi	32	32
A00C 01E0h	ETHERSW	Hub input filter MAC address low register 3	HUB_FLT_MAC3lo	32	32
A00C 01E4h	ETHERSW	Hub input filter MAC address high register 3	HUB_FLT_MAC3hi	32	32
A00C 01E8h	ETHERSW	Hub input filter MAC address low register 4	HUB_FLT_MAC4lo	32	32
A00C 01ECh	ETHERSW	Hub input filter MAC address high register 4	HUB_FLT_MAC4hi	32	32
A00C 01F0h	ETHERSW	Hub input filter MAC address low register 5	HUB_FLT_MAC5lo	32	32
A00C 01F4h	ETHERSW	Hub input filter MAC address high register 5	HUB_FLT_MAC5hi	32	32
A00C 01F8h	ETHERSW	Hub input filter MAC address low register 6	HUB_FLT_MAC6lo	32	32

Table 5.1 List of I/O Registers (Address Order) (78 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00C 01FCh	ETHERSW	Hub input filter MAC address high register 6	HUB_FLT_MAC6hi	32	32
A00C 0300h	ETHERSW	Switch statistics counter	TOTAL_BYT_FRM	32	32
A00C 0304h	ETHERSW	Switch statistics counter	TOTAL_BYT_DISC	32	32
A00C 0308h	ETHERSW	Switch statistics counter	TOTAL_FRM	32	32
A00C 030Ch	ETHERSW	Switch statistics counter	TOTAL_DISC	32	32
A00C 0310h	ETHERSW	Switch statistics counter	ODISC0	32	32
A00C 0314h	ETHERSW	Switch statistics counter	IDISC_BLOCKED0	32	32
A00C 0318h	ETHERSW	Switch statistics counter	ODISC1	32	32
A00C 031Ch	ETHERSW	Switch statistics counter	IDISC_BLOCKED1	32	32
A00C 0320h	ETHERSW	Switch statistics counter	ODISC2	32	32
A00C 0324h	ETHERSW	Switch statistics counter	IDISC_BLOCKED2	32	32
A00C 0500h	ETHERSW	Learning record A register	LRN_REC_A	32	32
A00C 0504h	ETHERSW	Learning record B register	LRN_REC_B	32	32
A00C 0508h	ETHERSW	Learning data status register	LRN_STATUS	32	32
A00C 8008h	ETHERSW	Command configuration register 0	COMMAND_CONFIG0	32	32
A00C 8014h	ETHERSW	Maximum frame length register 0 (shared)	FRM_LENGTH0	32	32
A00C 801Ch	ETHERSW	FIFO buffer threshold register 0 (shared)	RX_SECTION_EMPTY0	32	32
A00C 8020h	ETHERSW	FIFO buffer threshold register 0 (shared)	RX_SECTION_FULL0	32	32
A00C 8024h	ETHERSW	FIFO buffer threshold register 0 (shared)	TX_SECTION_EMPTY0	32	32
A00C 8028h	ETHERSW	FIFO buffer threshold register 0 (shared)	TX_SECTION_FULL0	32	32
A00C 802Ch	ETHERSW	FIFO buffer threshold register 0 (shared)	RX_ALMOST_EMPTY0	32	32
A00C 8030h	ETHERSW	FIFO buffer threshold register 0 (shared)	RX_ALMOST_FULL0	32	32
A00C 8034h	ETHERSW	FIFO buffer threshold register 0 (shared)	TX_ALMOST_EMPTY0	32	32
A00C 8038h	ETHERSW	FIFO buffer threshold register 0 (shared)	TX_ALMOST_FULL0	32	32
A00C 8058h	ETHERSW	MAC status register 0 (shared)	MAC_STATUS0	32	32
A00C 805Ch	ETHERSW	Transmit IPG length register 0 (shared)	TX_IPG_LENGTH0	32	32
A00C 8100h	ETHERSW	MAC receive statistics counter	etherStatsOctets_0	32	32
A00C 8104h	ETHERSW	MAC receive statistics counter	OctetsOK_0	32	32
A00C 8108h	ETHERSW	MAC receive statistics counter	aAlignmentErrors_0	32	32
A00C 810Ch	ETHERSW	MAC receive statistics counter	aPAUSEMACCtrlFrames_0	32	32
A00C 8110h	ETHERSW	MAC receive statistics counter	FramesOK_0	32	32
A00C 8114h	ETHERSW	MAC receive statistics counter	CRCErrors_0	32	32
A00C 8118h	ETHERSW	MAC receive statistics counter	VLANOK_0	32	32
A00C 811Ch	ETHERSW	MAC receive statistics counter	ifInErrors_0	32	32
A00C 8120h	ETHERSW	MAC receive statistics counter	ifInUcastPkts_0	32	32
A00C 8124h	ETHERSW	MAC receive statistics counter	ifInMulticastPkts_0	32	32
A00C 8128h	ETHERSW	MAC receive statistics counter	ifInBroadcastPkts_0	32	32
A00C 812Ch	ETHERSW	MAC receive statistics counter	etherStatsDropEvents_0	32	32
A00C 8130h	ETHERSW	MAC receive statistics counter	etherStatsPkts_0	32	32
A00C 8134h	ETHERSW	MAC receive statistics counter	etherStatsUndersizePkts_0	32	32
A00C 8138h	ETHERSW	MAC receive statistics counter	etherStatsPkts64Octets_0	32	32
A00C 813Ch	ETHERSW	MAC receive statistics counter	etherStatsPkts65to127Octets_0	32	32
A00C 8140h	ETHERSW	MAC receive statistics counter	etherStatsPkts128to255Octets_0	32	32
A00C 8144h	ETHERSW	MAC receive statistics counter	etherStatsPkts256to511Octets_0	32	32

Table 5.1 List of I/O Registers (Address Order) (79 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00C 8148h	ETHERSW	MAC receive statistics counter	etherStatsPkts512to1023Octets_0	32	32
A00C 814Ch	ETHERSW	MAC receive statistics counter	etherStatsPkts1024to1518Octets_0	32	32
A00C 8150h	ETHERSW	MAC receive statistics counter	etherStatsPkts1519toMax_0	32	32
A00C 8154h	ETHERSW	MAC receive statistics counter	etherStatsOversizePkts_0	32	32
A00C 8158h	ETHERSW	MAC receive statistics counter	etherStatsJabbers_0	32	32
A00C 815Ch	ETHERSW	MAC receive statistics counter	etherStatsFragments_0	32	32
A00C 8160h	ETHERSW	MAC receive statistics counter	aMACControlFramesReceived_0	32	32
A00C 8164h	ETHERSW	MAC receive statistics counter	aFrameTooLong_0	32	32
A00C 816Ch	ETHERSW	MAC receive statistics counter	StackedVLANOK_0	32	32
A00C 8180h	ETHERSW	MAC transmit statistics counter	TXetherStatsOctets_0	32	32
A00C 8184h	ETHERSW	MAC transmit statistics counter	TxOctetsOK_0	32	32
A00C 818Ch	ETHERSW	MAC transmit statistics counter	TXaPAUSEMACCtrlFrames_0	32	32
A00C 8190h	ETHERSW	MAC transmit statistics counter	TxFramesOK_0	32	32
A00C 8194h	ETHERSW	MAC transmit statistics counter	TxCRCErrors_0	32	32
A00C 8198h	ETHERSW	MAC transmit statistics counter	TxVLANOK_0	32	32
A00C 819Ch	ETHERSW	MAC transmit statistics counter	ifOutErrors_0	32	32
A00C 81A0h	ETHERSW	MAC transmit statistics counter	ifUcastPkts_0	32	32
A00C 81A4h	ETHERSW	MAC transmit statistics counter	ifMulticastPkts_0	32	32
A00C 81A8h	ETHERSW	MAC transmit statistics counter	ifBroadcastPkts_0	32	32
A00C 81ACh	ETHERSW	MAC transmit statistics counter	TXetherStatsDropEvents_0	32	32
A00C 81B0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts_0	32	32
A00C 81B4h	ETHERSW	MAC transmit statistics counter	TXetherStatsUndersizePkts_0	32	32
A00C 81B8h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts64Octets_0	32	32
A00C 81BCh	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts65to127Octets_0	32	32
A00C 81C0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts128to255Octets_0	32	32
A00C 81C4h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts256to511Octets_0	32	32
A00C 81C8h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts512to1023Octets_0	32	32
A00C 81CCh	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts1024to1518Octets_0	32	32
A00C 81D0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts1519toMax_0	32	32
A00C 81D4h	ETHERSW	MAC transmit statistics counter	TXetherStatsOversizePkts_0	32	32
A00C 81D8h	ETHERSW	MAC transmit statistics counter	TXetherStatsJabbers_0	32	32
A00C 81DCh	ETHERSW	MAC transmit statistics counter	TXetherStatsFragments_0	32	32
A00C 81E0h	ETHERSW	MAC transmit statistics counter	aMACControlFrames_0	32	32
A00C 81E4h	ETHERSW	MAC transmit statistics counter	TXaFrameTooLong_0	32	32
A00C 81ECh	ETHERSW	MAC transmit statistics counter	aMultipleCollisions_0	32	32
A00C 81F0h	ETHERSW	MAC transmit statistics counter	aSingleCollisions_0	32	32
A00C 81F4h	ETHERSW	MAC transmit statistics counter	aLateCollisions_0	32	32
A00C 81F8h	ETHERSW	MAC transmit statistics counter	aExcessCollisions_0	32	32

Table 5.1 List of I/O Registers (Address Order) (80 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00C A008h	ETHERSW	Command configuration register 1	COMMAND_CONFIG1	32	32
A00C A014h	ETHERSW	Maximum frame length register 1 (shared)	FRM_LENGTH1	32	32
A00C A01Ch	ETHERSW	FIFO buffer threshold register 1 (shared)	RX_SECTION_EMPTY1	32	32
A00C A020h	ETHERSW	FIFO buffer threshold register 1 (shared)	RX_SECTION_FULL1	32	32
A00C A024h	ETHERSW	FIFO buffer threshold register 1 (shared)	TX_SECTION_EMPTY1	32	32
A00C A028h	ETHERSW	FIFO buffer threshold register 1 (shared)	TX_SECTION_FULL1	32	32
A00C A02Ch	ETHERSW	FIFO buffer threshold register 1 (shared)	RX_ALMOST_EMPTY1	32	32
A00C A030h	ETHERSW	FIFO buffer threshold register 1 (shared)	RX_ALMOST_FULL1	32	32
A00C A034h	ETHERSW	FIFO buffer threshold register 1 (shared)	TX_ALMOST_EMPTY1	32	32
A00C A038h	ETHERSW	FIFO buffer threshold register 1 (shared)	TX_ALMOST_FULL1	32	32
A00C A058h	ETHERSW	MAC status register 1 (shared)	MAC_STATUS1	32	32
A00C A05Ch	ETHERSW	Transmit IPG length register 1 (shared)	TX_IPG_LENGTH1	32	32
A00C A100h	ETHERSW	MAC receive statistics counter	etherStatsOctets_1	32	32
A00C A104h	ETHERSW	MAC receive statistics counter	OctetsOK_1	32	32
A00C A108h	ETHERSW	MAC receive statistics counter	aAlignmentErrors_1	32	32
A00C A10Ch	ETHERSW	MAC receive statistics counter	aPAUSEMACCtrlFrames_1	32	32
A00C A110h	ETHERSW	MAC receive statistics counter	FramesOK_1	32	32
A00C A114h	ETHERSW	MAC receive statistics counter	CRCErrors_1	32	32
A00C A118h	ETHERSW	MAC receive statistics counter	VLANOK_1	32	32
A00C A11Ch	ETHERSW	MAC receive statistics counter	ifInErrors_1	32	32
A00C A120h	ETHERSW	MAC receive statistics counter	ifInUcastPkts_1	32	32
A00C A124h	ETHERSW	MAC receive statistics counter	ifInMulticastPkts_1	32	32
A00C A128h	ETHERSW	MAC receive statistics counter	ifInBroadcastPkts_1	32	32
A00C A12Ch	ETHERSW	MAC receive statistics counter	etherStatsDropEvents_1	32	32
A00C A130h	ETHERSW	MAC receive statistics counter	etherStatsPkts_1	32	32
A00C A134h	ETHERSW	MAC receive statistics counter	etherStatsUndersizePkts_1	32	32
A00C A138h	ETHERSW	MAC receive statistics counter	etherStatsPkts64Octets_1	32	32
A00C A13Ch	ETHERSW	MAC receive statistics counter	etherStatsPkts65to127Octets_1	32	32
A00C A140h	ETHERSW	MAC receive statistics counter	etherStatsPkts128to255Octets_1	32	32
A00C A144h	ETHERSW	MAC receive statistics counter	etherStatsPkts256to511Octets_1	32	32
A00C A148h	ETHERSW	MAC receive statistics counter	etherStatsPkts512to1023Octets_1	32	32
A00C A14Ch	ETHERSW	MAC receive statistics counter	etherStatsPkts1024to1518Octets_1	32	32
A00C A150h	ETHERSW	MAC receive statistics counter	etherStatsPkts1519toMax_1	32	32
A00C A154h	ETHERSW	MAC receive statistics counter	etherStatsOversizePkts_1	32	32
A00C A158h	ETHERSW	MAC receive statistics counter	etherStatsJabbers_1	32	32
A00C A15Ch	ETHERSW	MAC receive statistics counter	etherStatsFragments_1	32	32
A00C A160h	ETHERSW	MAC receive statistics counter	aMACControlFramesReceived_1	32	32
A00C A164h	ETHERSW	MAC receive statistics counter	aFrameTooLong_1	32	32
A00C A16Ch	ETHERSW	MAC receive statistics counter	StackedVLANOK_1	32	32
A00C A180h	ETHERSW	MAC transmit statistics counter	TXetherStatsOctets_1	32	32
A00C A184h	ETHERSW	MAC transmit statistics counter	TxOctetsOK_1	32	32

Table 5.1 List of I/O Registers (Address Order) (81 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00C A18Ch	ETHERSW	MAC transmit statistics counter	TXaPAUSEMACCtrlFrames_1	32	32
A00C A190h	ETHERSW	MAC transmit statistics counter	TxFramesOK_1	32	32
A00C A194h	ETHERSW	MAC transmit statistics counter	TxCRCErrors_1	32	32
A00C A198h	ETHERSW	MAC transmit statistics counter	TxVLANOK_1	32	32
A00C A19Ch	ETHERSW	MAC transmit statistics counter	ifOutErrors_1	32	32
A00C A1A0h	ETHERSW	MAC transmit statistics counter	ifUcastPkts_1	32	32
A00C A1A4h	ETHERSW	MAC transmit statistics counter	ifMulticastPkts_1	32	32
A00C A1A8h	ETHERSW	MAC transmit statistics counter	ifBroadcastPkts_1	32	32
A00C A1ACh	ETHERSW	MAC transmit statistics counter	TXetherStatsDropEvents_1	32	32
A00C A1B0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts_1	32	32
A00C A1B4h	ETHERSW	MAC transmit statistics counter	TXetherStatsUndersizePkts_1	32	32
A00C A1B8h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts64Octets_1	32	32
A00C A1BCh	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts65to127Octets_1	32	32
A00C A1C0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts128to255Octets_1	32	32
A00C A1C4h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts256to511Octets_1	32	32
A00C A1C8h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts512to1023Octets_1	32	32
A00C A1CCh	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts1024to1518Octets_1	32	32
A00C A1D0h	ETHERSW	MAC transmit statistics counter	TXetherStatsPkts1519toMax_1	32	32
A00C A1D4h	ETHERSW	MAC transmit statistics counter	TXetherStatsOversizePkts_1	32	32
A00C A1D8h	ETHERSW	MAC transmit statistics counter	TXetherStatsJabbers_1	32	32
A00C A1DCh	ETHERSW	MAC transmit statistics counter	TXetherStatsFragments_1	32	32
A00C A1E0h	ETHERSW	MAC transmit statistics counter	aMACControlFrames_1	32	32
A00C A1E4h	ETHERSW	MAC transmit statistics counter	TXaFrameTooLong_1	32	32
A00C A1ECh	ETHERSW	MAC transmit statistics counter	aMultipleCollisions_1	32	32
A00C A1F0h	ETHERSW	MAC transmit statistics counter	aSingleCollisions_1	32	32
A00C A1F4h	ETHERSW	MAC transmit statistics counter	aLateCollisions_1	32	32
A00C A1F8h	ETHERSW	MAC transmit statistics counter	aExcessCollisions_1	32	32
A00C C004h	ETHERSW	Timer module configuration register	TSM_CONFIG	32	32
A00C C008h	ETHERSW	Timer interrupt status/acknowledge register	TSM_IRQ_STAT_ACK	32	32
A00C C020h	ETHERSW	Port timestamp control/status register 0	PORT0_CTRL	32	32
A00C C024h	ETHERSW	Port timestamp register 0	PORT0_TIME	32	32
A00C C028h	ETHERSW	Port timestamp control/status register 1	PORT1_CTRL	32	32
A00C C02Ch	ETHERSW	Port timestamp register 1	PORT1_TIME	32	32
A00C C120h	ETHERSW	Timer control register	ATIME_CTRL	32	32
A00C C124h	ETHERSW	Timer nanosecond register	ATIME	32	32
A00C C128h	ETHERSW	Timer offset correction register	ATIME_OFFSET	32	32
A00C C12Ch	ETHERSW	Timer cycle event generation register	ATIME_EVT_PERIOD	32	32
A00C C130h	ETHERSW	Timer drift correction register	ATIME_CORR	32	32
A00C C134h	ETHERSW	Timer increment register	ATIME_INC	32	32
A00C C138h	ETHERSW	Timer second register	ATIME_SEC	32	32
A00C C13Ch	ETHERSW	Timer offset correction count register	ATIME_OFFS_CORR	32	32

Table 5.1 List of I/O Registers (Address Order) (82 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00C E000h	ETHERSW	DLR control register	DLR_CONTROL	32	32
A00C E004h	ETHERSW	DLR status register	DLR_STATUS	32	32
A00C E008h	ETHERSW	DLR EtherType register	DLR_ETH_TYP	32	32
A00C E00Ch	ETHERSW	DLR interrupt control register	DLR_IRQ_CTRL	32	32
A00C E010h	ETHERSW	DLR interrupt status/acknowledge register	DLR_IRQ_STAT_ACK	32	32
A00C E014h	ETHERSW	DLR local MAC address low register	LOC_MAClo	32	32
A00C E018h	ETHERSW	DLR local MAC address high register	LOC_MAChi	32	32
A00C E020h	ETHERSW	DLR supervisor MAC address low register	SUPR_MAClo	32	32
A00C E024h	ETHERSW	DLR supervisor MAC address high register	SUPR_MAChi	32	32
A00C E028h	ETHERSW	DLR ring status/VLAN register	STATE_VLAN	32	32
A00C E02Ch	ETHERSW	DLR beacon timeout timer register	BEC_TMOUT	32	32
A00C E030h	ETHERSW	DLR beacon interval register	BEC_INTRVL	32	32
A00C E034h	ETHERSW	DLR supervisor IP address register	SUPR_IPADR	32	32
A00C E038h	ETHERSW	DLR sub-type/protocol version register	ETH_STYP_VER	32	32
A00C E03Ch	ETHERSW	DLR beacon illegal time-out timer register	INV_TMOUT	32	32
A00C E040h	ETHERSW	DLR sequence ID register	SEQ_ID	32	32
A00C E060h	ETHERSW	DLR MAC statistics counter	RX_STAT0	32	32
A00C E064h	ETHERSW	DLR MAC statistics counter	RX_ERR_STAT0	32	32
A00C E068h	ETHERSW	DLR MAC statistics counter	TX_STAT0	32	32
A00C E070h	ETHERSW	DLR MAC statistics counter	RX_STAT1	32	32
A00C E074h	ETHERSW	DLR MAC statistics counter	RX_ERR_STAT1	32	32
A00C E078h	ETHERSW	DLR MAC statistics counter	TX_STAT1	32	32
A00D 0000h	ECATC*1	Type Register	TYPE	8	8
A00D 0001h	ECATC*1	Revision Register	REVISION	8	8
A00D 0002h	ECATC*1	Build Register	BUILD	16	16
A00D 0004h	ECATC*1	FMMU Supported Register	FMMU_NUM	8	8
A00D 0005h	ECATC*1	SyncManager Supported Register	SYNC_MANAGER	8	8
A00D 0006h	ECATC*1	RAM Size Register	RAM_SIZE	8	8
A00D 0007h	ECATC*1	Port Descriptor Register	PORT_DESC	8	8
A00D 0008h	ECATC*1	ESC Features Supported Register	FEATURE	16	16
A00D 0010h	ECATC*1	Configured Station Address Register	STATION_ADR	16	16
A00D 0012h	ECATC*1	Configured Station Alias Register	STATION_ALIAS	16	16
A00D 0020h	ECATC*1	Write Register Enable Register	WR_REG_ENABLE	8	8
A00D 0021h	ECATC*1	Write Register Protection Register	WR_REG_PROTECT	8	8
A00D 0030h	ECATC*1	ESC Write Enable Register	ESC_WR_ENABLE	8	8
A00D 0031h	ECATC*1	ESC Write Protection Register	ESC_WR_PROTECT	8	8
A00D 0040h	ECATC*1	ESC Reset ECAT Register	ESC_RESET_ECAT	8	8
A00D 0041h	ECATC*1	ESC Reset PDI Register	ESC_RESET_PDI	8	8
A00D 0100h	ECATC*1	ESC DL Control Register	ESC_DL_CONTROL	32	32
A00D 0108h	ECATC*1	Physical Read/Write Offset Register	PHYSICAL_RW_OFFSET	16	16
A00D 0110h	ECATC*1	ESC DL Status Register	ESC_DL_STATUS	16	16
A00D 0120h	ECATC*1	AL Control Register	AL_CONTROL	16	16
A00D 0130h	ECATC*1	AL Status Register	AL_STATUS	16	16
A00D 0134h	ECATC*1	AL Status Code Register	AL_STATUS_CODE	16	16
A00D 0138h	ECATC*1	RUN LED Override Register	RUN_LED_OVERRIDE	8	8
A00D 0139h	ECATC*1	ERR LED Override Register	ERR_LED_OVERRIDE	8	8
A00D 0140h	ECATC*1	PDI Control Register	PDI_CONTROL	8	8
A00D 0141h	ECATC*1	ESC Configuration Register	ESC_CONFIG	8	8

Table 5.1 List of I/O Registers (Address Order) (83 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00D 0150h	ECATC*1	PDI Configuration Register	PDI_CONFIG	8	8
A00D 0151h	ECATC*1	SYNC/LATCH PDI Configuration Register	SYNC_LATCH_CONFIG	16	16
A00D 0152h	ECATC*1	Extended PDI Configuration Register	EXT_PDI_CONFIG	16	16
A00D 0200h	ECATC*1	ECAT Event Mask Register	ECAT_EVENT_MASK	16	16
A00D 0204h	ECATC*1	AL Event Mask Register	AL_EVENT_MASK	32	32
A00D 0210h	ECATC*1	ECAT Event Request Register	ECAT_EVENT_REQ	16	16
A00D 0220h	ECATC*1	AL Event Request Register	AL_EVENT_REQ	32	32
A00D 0300h + 0002h*n	ECATC*1	Rx Error Counter n Register	RX_ERR_COUNTn	16	16
A00D 0308h + 0001h*n	ECATC*1	Forwarded Rx Error Counter n Register	FWD_RX_ERR_COUNTn	8	8
A00D 030Ch	ECATC*1	ECAT Processing Unit Error Counter Register	ECAT_PROC_ERR_COUNT	8	8
A00D 030Dh	ECATC*1	PDI Error Counter Register	PDI_ERR_COUNT	8	8
A00D 0310h + 0001h*n	ECATC*1	Lost Link Counter n Register	LOST_LINK_COUNTn	8	8
A00D 0400h	ECATC*1	Watchdog Divider Register	WD_DIVIDE	16	16
A00D 0410h	ECATC*1	Watchdog Time PDI Register	WDT_PDI	16	16
A00D 0420h	ECATC*1	Watchdog Time Process Data Register	WDT_DATA	16	16
A00D 0440h	ECATC*1	Watchdog Status Process Data Register	WDS_DATA	16	16
A00D 0442h	ECATC*1	Watchdog Counter Process Data Register	WDC_DATA	8	8
A00D 0443h	ECATC*1	Watchdog Counter PDI Register	WDC_PDI	8	8
A00D 0500h	ECATC*1	EEPROM Configuration Register	EEP_CONF	8	8
A00D 0501h	ECATC*1	EEPROM PDI Access State Register	EEP_STATE	8	8
A00D 0502h	ECATC*1	EEPROM Control/Status Register	EEP_CONT_STAT	16	16
A00D 0504h	ECATC*1	EEPROM Address Register	EEP_ADR	32	32
A00D 0508h	ECATC*1	EEPROM Data Register	EEP_DATA	32	32
A00D 0510h	ECATC*1	MII Management Control/Status Register	MII_CONT_STAT	16	16
A00D 0512h	ECATC*1	PHY Address Register	PHY_ADR	8	8
A00D 0513h	ECATC*1	PHY Register Address Register	PHY_REG_ADR	8	8
A00D 0514h	ECATC*1	PHY Data Register	PHY_DATA	16	16
A00D 0516h	ECATC*1	MII Management ECAT Access State Register	MII_ECAT_ACS_STAT	8	8
A00D 0517h	ECATC*1	MII Management PDI Access State Register	MII_PDI_ACS_STAT	8	8
A00D 0600h + 0010h*m	ECATC*1	FMMU Logical Start Address m Register	FMMUm_L_START_ADR	32	32
A00D 0604h + 0010h*m	ECATC*1	FMMU Length m Register	FMMUm_LEN	16	16
A00D 0606h + 0010h*m	ECATC*1	FMMU Logical Start Bit m Register	FMMUm_L_START_BIT	8	8
A00D 0607h + 0010h*m	ECATC*1	FMMU Logical Stop Bit m Register	FMMUm_L_STOP_BIT	8	8
A00D 0608h + 0010h*m	ECATC*1	FMMU Physical Start Address m Register	FMMUm_P_START_ADR	16	16
A00D 060Ah + 0010h*m	ECATC*1	FMMU Physical Start Bit m Register	FMMUm_P_START_BIT	8	8
A00D 060Bh + 0010h*m	ECATC*1	FMMU Type m Register	FMMUm_TYPE	8	8
A00D 060Ch + 0010h*m	ECATC*1	FMMU Activate m Register	FMMUm_ACT	8	8
A00D 0800h + 0008h*m	ECATC*1	SyncManager Physical Start Address m Register	SMm_P_START_ADR	16	16
A00D 0802h + 0008h*m	ECATC*1	SyncManager Length m Register	SMm_LEN	16	16

Table 5.1 List of I/O Registers (Address Order) (84 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00D 0804h + 0008h*m	ECATC*1	SyncManager Control m Register	SMm_CONTROL	8	8
A00D 0805h + 0008h*m	ECATC*1	SyncManager Status m Register	SMm_STATUS	8	8
A00D 0806h + 0008h*m	ECATC*1	SyncManager Activate m Register	SMm_ACT	8	8
A00D 0807h + 0008h*m	ECATC*1	SyncManager PDI Control m Register	SMm_PDI_CONT	8	8
A00D 0900h	ECATC*1	Receive Time Port 0 Register	DC_RCV_TIME_PORT0	32	32
A00D 0904h	ECATC*1	Receive Time Port 1 Register	DC_RCV_TIME_PORT1	32	32
A00D 0910h	ECATC*1	System Time Register	DC_SYS_TIME	64	32
A00D 0918h	ECATC*1	Receive Time ECAT Processing Unit Register	DC_RCV_TIME_UNIT	64	32
A00D 0920h	ECATC*1	System Time Offset Register	DC_SYS_TIME_OFFSET	64	32
A00D 0928h	ECATC*1	System Time Delay Register	DC_SYS_TIME_DELAY	32	32
A00D 092Ch	ECATC*1	System Time Difference Register	DC_SYS_TIME_DIFF	32	32
A00D 0930h	ECATC*1	Speed Counter Start Register	DC_SPEED_COUNT_START	16	16
A00D 0932h	ECATC*1	Speed Counter Difference Register	DC_SPEED_COUNT_DIFF	16	16
A00D 0934h	ECATC*1	System Time Difference Filter Depth Register	DC_SYS_TIME_DIFF_FIL_DEPTH	8	8
A00D 0935h	ECATC*1	Speed Counter Filter Depth Register	DC_SPEED_COUNT_FIL_DEPTH	8	8
A00D 0980h	ECATC*1	Cyclic Unit Control Register	DC_CYC_CONT	8	8
A00D 0981h	ECATC*1	Activation Register	DC_ACT	8	8
A00D 0982h	ECATC*1	SYNC Signal Pulse Length Register	DC_PULSE_LEN	16	16
A00D 0984h	ECATC*1	Activation Status Register	DC_ACT_STAT	8	8
A00D 098Eh	ECATC*1	SYNC0 Status Register	DC_SYNC0_STAT	8	8
A00D 098Fh	ECATC*1	SYNC1 Status Register	DC_SYNC1_STAT	8	8
A00D 0990h	ECATC*1	Start Time Cyclic Operation/Next SYNC0 Pulse Register	DC_CYC_START_TIME	64	32
A00D 0998h	ECATC*1	Next SYNC1 Pulse Register	DC_NEXT_SYNC1_PULSE	64	32
A00D 09A0h	ECATC*1	SYNC0 Cycle Time Register	DC_SYNC0_CYC_TIME	32	32
A00D 09A4h	ECATC*1	SYNC1 Cycle Time Register	DC_SYNC1_CYC_TIME	32	32
A00D 09A8h	ECATC*1	Latch 0 Control Register	DC_LATCH0_CONT	8	8
A00D 09A9h	ECATC*1	Latch 1 Control Register	DC_LATCH1_CONT	8	8
A00D 09AEh	ECATC*1	Latch 0 Status Register	DC_LATCH0_STAT	8	8
A00D 09AFh	ECATC*1	Latch 1 Status Register	DC_LATCH1_STAT	8	8
A00D 09B0h	ECATC*1	Latch 0 Time Positive Edge Register	DC_LATCH0_TIME_POS	64	32
A00D 09B8h	ECATC*1	Latch 0 Time Negative Edge Register	DC_LATCH0_TIME_NEG	64	32
A00D 09C0h	ECATC*1	Latch 1 Time Positive Edge Register	DC_LATCH1_TIME_POS	64	32
A00D 09C8h	ECATC*1	Latch 1 Time Negative Edge Register	DC_LATCH1_TIME_NEG	64	32
A00D 09F0h	ECATC*1	Buffer Change Event Time Register	DC_ECAT_CNG_EV_TIME	32	32
A00D 09F8h	ECATC*1	PDI Buffer Start Event Time Register	DC_PDI_START_EV_TIME	32	32
A00D 09FCh	ECATC*1	PDI Buffer Change Event Time Register	DC_PDI_CNG_EV_TIME	32	32
A00D 0E00h	ECATC*1	Product ID Register	PRODUCT_ID	64	32
A00D 0E08h	ECATC*1	Vendor ID Register	VENDOR_ID	64	32

Table 5.1 List of I/O Registers (Address Order) (85 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00D 0F80h – A00D 0FFFh	ECATC*1	User RAM	USER_RAM	1024	8, 16, 32
A00D 1000h – A00D 2FFFh	ECATC*1	Process Data RAM	DATA_RAM	65536	8, 16, 32
A00E 0000h	ETHERC	Hardware function type register	C0TYPE	32	32
A00E 0008h	ETHERC	Hardware function state register	C0STAT	32	32
A00E F000h	ETHERC	Hardware Function System Call Register	SYSC	32	32
A00E F004h	ETHERC	Hardware function argument register 4	R4	32	32
A00E F008h	ETHERC	Hardware function argument register 5	R5	32	32
A00E F00Ch	ETHERC	Hardware function argument register 6	R6	32	32
A00E F010h	ETHERC	Hardware function argument register 7	R7	32	32
A00E F014h	ETHERC	Hardware Function Command Register	CMD	32	32
A00E F020h	ETHERC	Hardware function return value register 0	R0	32	32
A00E F024h	ETHERC	Hardware function return value register 1	R1	32	32
A00F 000Ch	ETHERC	TX ID register	GMAC_TXID	32	32
A00F 0010h	ETHERC	TX RESULT register	GMAC_TXRESULT	32	32
A00F 0020h	ETHERC	MODE register	GMAC_MODE	32	32
A00F 0024h	ETHERC	RX MODE register	GMAC_RXMODE	32	32
A00F 0028h	ETHERC	TX MODE register	GMAC_TXMODE	32	32
A00F 0030h	ETHERC	RESET register	GMAC_RESET	32	32
A00F 0080h	ETHERC	PAUSE packet data register 1	GMAC_PAUSE1	32	32
A00F 0084h	ETHERC	PAUSE packet data register 2	GMAC_PAUSE2	32	32
A00F 0088h	ETHERC	PAUSE packet data register 3	GMAC_PAUSE3	32	32
A00F 008Ch	ETHERC	PAUSE packet data register 4	GMAC_PAUSE4	32	32
A00F 0090h	ETHERC	PAUSE packet data register 5	GMAC_PAUSE5	32	32
A00F 0098h	ETHERC	RX FLOW CONTROL register	GMAC_FLWCTL	32	32
A00F 009Ch	ETHERC	PAUSE packet register	GMAC_PAUSPKT	32	32
A00F 00A0h	ETHERC	MIIM register	GMAC_MIIM	32	32
A00F 0100h	ETHERC	MAC address register 0A	GMAC_ADR0A	32	32
A00F 0104h	ETHERC	MAC address register 0B	GMAC_ADR0B	32	32
A00F 0108h	ETHERC	MAC address register 1A	GMAC_ADR1A	32	32
A00F 010ch	ETHERC	MAC address register 1B	GMAC_ADR1B	32	32
A00F 0110h	ETHERC	MAC address register 2A	GMAC_ADR2A	32	32
A00F 0114h	ETHERC	MAC address register 2B	GMAC_ADR2B	32	32
A00F 0118h	ETHERC	MAC address register 3A	GMAC_ADR3A	32	32
A00F 011ch	ETHERC	MAC address register 3B	GMAC_ADR3B	32	32
A00F 0120h	ETHERC	MAC address register 4A	GMAC_ADR4A	32	32
A00F 0124h	ETHERC	MAC address register 4B	GMAC_ADR4B	32	32
A00F 0128h	ETHERC	MAC address register 5A	GMAC_ADR5A	32	32
A00F 012ch	ETHERC	MAC address register 5B	GMAC_ADR5B	32	32
A00F 0130h	ETHERC	MAC address register 6A	GMAC_ADR6A	32	32
A00F 0134h	ETHERC	MAC address register 6B	GMAC_ADR6B	32	32
A00F 0138h	ETHERC	MAC address register 7A	GMAC_ADR7A	32	32
A00F 013Ch	ETHERC	MAC address register 7B	GMAC_ADR7B	32	32
A00F 0140h	ETHERC	MAC address register 8A	GMAC_ADR8A	32	32
A00F 0144h	ETHERC	MAC address register 8B	GMAC_ADR8B	32	32
A00F 0148h	ETHERC	MAC address register 9A	GMAC_ADR9A	32	32
A00F 014Ch	ETHERC	MAC address register 9B	GMAC_ADR9B	32	32
A00F 0150h	ETHERC	MAC address register 10A	GMAC_ADR10A	32	32

Table 5.1 List of I/O Registers (Address Order) (86 / 86)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size
A00F 0154h	ETHERC	MAC address register 10B	GMAC_ADR10B	32	32
A00F 0158h	ETHERC	MAC address register 11A	GMAC_ADR11A	32	32
A00F 015ch	ETHERC	MAC address register 11B	GMAC_ADR11B	32	32
A00F 0160h	ETHERC	MAC address register 12A	GMAC_ADR12A	32	32
A00F 0164h	ETHERC	MAC address register 12B	GMAC_ADR12B	32	32
A00F 0168h	ETHERC	MAC address register 13A	GMAC_ADR13A	32	32
A00F 016Ch	ETHERC	MAC address register 13B	GMAC_ADR13B	32	32
A00F 0170h	ETHERC	MAC address register 14A	GMAC_ADR14A	32	32
A00F 0174h	ETHERC	MAC address register 14B	GMAC_ADR14B	32	32
A00F 0178h	ETHERC	MAC address register 15A	GMAC_ADR15A	32	32
A00F 017Ch	ETHERC	MAC address register 15B	GMAC_ADR15B	32	32
A00F 0200h	ETHERC	RX FIFO status register	GMAC_RXFIFO	32	32
A00F 0204h	ETHERC	TX FIFO status register	GMAC_TXFIFO	32	32
A00F 0208h	ETHERC	TCPIPACC register	GMAC_ACC	32	32
A00F 0220h	ETHERC	RX MAC ENABLE register	GMAC_RXMAC_ENA	32	32
A00F 0224h	ETHERC	LPI mode control register	GMAC_LPI_MODE	32	32
A00F 0228h	ETHERC	LPI CLIENT timing control register	GMAC_LPI_TIMING	32	32
A00F 1100h	ETHERC	Reception buffer information register	BUFID	32	32
A00F 201Ch	ETHERC	Ethernet switch 10-Mbps/half-duplex mode setting register	ETHSW10HDEN	32	32
A00F 2100h	ETHERC	System protect command register	SPCMD	32	32
A00F 2110h	ETHERC	Ethernet MAC reset register	EMACRST	32	32
A00F 3000h	ECCRAM	Protection command register	RAMPCMD	32	32
A00F 3100h	ECCRAM	ECC decoder configuration register	RAMEDC	32	32
A00F 3104h	ECCRAM	ECC encoder configuration register	RAMEEC	32	32
A00F 3108h	ECCRAM	2-bit ECC error status register	RAMDBEST	32	32
A00F 310Ch	ECCRAM	2-bit ECC error address register	RAMDBEAD	32	32
A00F 3110h	ECCRAM	2-bit ECC error counter register	RAMDBECNT	32	32

Note 1. Optional

6. Reset

6.1 Overview

Available reset types are RES# pin reset, error control module (ECM) reset, software reset, and software reset 2. Table 6.1 lists the reset names and sources.

Table 6.1 Reset Names and Sources

Reset Name	Source
RES# pin reset	Voltage input to the RES# pin is low.
ECM reset	Reset request from the error control module (ECM)
Software reset	SWRR1 register setting
Software reset 2 (for products incorporating an R-IN engine)	SWRR2 register setting

The internal states and pins are initialized by reset.
Table 6.2 lists the reset targets to be initialized for each reset type. For details on reset control during debugging, see section 10.3.5, Reset Configuration and the Method of Connecting with the Emulator.

Table 6.2 Targets to Be Initialized for Each Reset Type (√: To be initialized, —: No change)

	Reset Source			
Reset Target	**RES# Pin Reset**	**ECM Reset**	**Software Reset**	**Software Reset 2*5**
RES# pin reset flag (RSTSR0.TRF)	—	√	√	—
ECM reset detect flag (RSTSR0.ECMRF)	√	—	√	—
Software reset detect flag (RSTSR0.SWRF1)	√	√	—	—
Pin state	√	√	√	—
Operation mode	√*1	—*2	—*2	—
Cortex-M3 (for products incorporating an R-IN engine)	√	√	√	√
WDTA (for Cortex-M3) (for products incorporating an R-IN engine)	√	√	√	√
ECM ECM master error source status registers 0 to 2 ECM checker error source status registers 0 to 2 ECM error output clear disable setting register	√	—	—	—
Registers other than the above, and internal state	√	√	√	—
RSTOUT# pin output	√ (Low)*3	√ (Low)*3	√ (Low)*3	—
ERROROUT# pin output	√ (Low)	*4	—	—

Note 1. An operation mode is selected according to the input level of the mode setting pin (MD2, MD1, or MD0) when the pin reset state (RES# and TRST# pins are both low) is released. For details on the operation mode, see section 3.2, Types and Selection of Operating Modes.
Note 2. The operating mode is not initialized in response to this type of reset and the chip will be in the operating mode that was selected following the previous release from the reset state applied by the low level on the RES#. For details, see section 3, Operating Modes.
Note 3. For the low output period, see section 6.3.6, Reset Output Pin (RSTOUT#).
Note 4. Depends on the ECM setting. For details, see section 42, Error Control Module (ECM).
Note 5. The initial setting of software reset register 2 (SWRR2) is to remain in the reset state. For details, see section 6.2.3, Software Reset Register 2 (SWRR2) (for products incorporating an R-IN engine).

Table 6.3 lists the input and output pins related to the reset.

Table 6.3 Input and Output Pins Related to Reset

Pin Name	I/O	Function
RES#	Input	Reset pin. Use this pin to reset the entire LSI except the debugging circuit and TAP (Test Access Port). Since the power-on reset circuit is not incorporated in RZ/T1, a reset circuit must be implemented outside this LSI. For an example of configuration of the external reset circuit, see section 10.3.5, Reset Configuration and the Method of Connecting with the Emulator.
TRST#	Input	Test reset pin. Use this pin to reset TAP. If you design a board which enables an emulator, set the TRST# pin to Low level during the same period as the RES# pin at the time of power-on. The TRST# pin should also be controllable independently. When unused, this pin must be set to low level or connected to the same signal as the RES# pin. For details, see section 10.3.5, Reset Configuration and the Method of Connecting with the Emulator.
RSTOUT#	Output	Reset output pin. This pin outputs low-level signal upon occurrence of reset. For details, see section 6.3.6, Reset Output Pin (RSTOUT#). This pin can be used for resetting the external device.

Note: For details on resetting the debugging circuit, see section 10, Debugging Interface.

6.2 Register Descriptions

The reset status register 0 contains bits assigned to respective reset types to indicate reset generation sources. RSTSR0 and SWRR1, and SWRR2 are protected by the register write protection function. To write these registers, clear the write protection bit 1 in the protect register (PRCR). For details on the register write protection, see section 11, Register Write Protection Function.

6.2.1 Reset Status Register 0 (RSTSR0)

RSTSR0 is the register that indicates reset generation sources.

Address(es): RSTSR0: A00B 0200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SWR1F	ECMRF	TRF	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	*1	*1	*1	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)
b1	TRF	RES# Pin Reset Detect Flag	0: RES# pin reset not detected 1: RES# pin reset detected [Setting condition] • When Low is input to the RES# pin. [Clearing conditions] • When a ECM reset or software reset occurs. • When “0000 0000h” is written to RSTSR0 after RSTSR0 is read.	R/(W)*2
b2	ECMRF	ECM Reset Detect Flag	0: ECM reset not detected 1: ECM reset detected [Setting condition] • When an error predefined as a reset source by ECM setting occurs. [Clearing conditions] • When an RES# pin reset or software reset occurs. • When “0000 0000h” is written to RSTSR0 after RSTSR0 is read.	R/(W)*2
b3	SWR1F	Software Reset Detect Flag	0: Software reset not detected. 1: Software reset detected. [Setting condition] • When a software reset occurs. [Clearing conditions] • When an RES# pin reset or ECM reset occurs. • When “0000 0000h” is written to RSTSR0 after RSTSR0 is read.	R/(W)*2
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag.

6.2.2 Software Reset Register (SWRR1)

SWRR1 is a register that controls the software reset.

Address(es): SWRR1: A00B 0210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SWRR1[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SWRR1[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SWRR1[31:0]	Software Reset	When “4321 A501h” is written, a software reset occurs. These bits are read as 0000 0000h.	R/W

6.2.3 Software Reset Register 2 (SWRR2) (for products incorporating an R-IN engine)

SWRR2 is a register that controls the software reset 2.

Address(es): SWRR2: A00B 0220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SWRR2[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SWRR2[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SWRR2[31:0]	Software Reset 2	These bits are used to control reset of Cortex-M3 and WDTA for Cortex-M3. When 4321 A50Fh is written, a software reset 2 occurs, and Cortex-M3 and WDTA for Cortex-M3 enter the reset state. To clear the reset, write 0000 0000h. These bits are read as 0000 0001h during reset, and as 0000 0000h when reset is released. Note: After an RES# pin reset, ECM reset, or software reset occurred, the reset state due to the software reset 2 takes place as the initial state. When it is necessary to release the software reset 2, write 0000 0000h to the SWRR2 register of Cortex-R4.	R/W

6.2.4 Module Reset Control Register C (MRCTLC)

MRCTLC is a register that controls the reset of peripheral modules.

Address(es): MRCTLC: A00B 0248h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MRUSBH	MRUSBF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MRUSBF	USB (Func) Reset Control	0: USB (Func) is released from reset. 1: USB (Func) is in the reset state.	R/W
b1	MRUSBH	USB (Host) Reset Control	0: USB (Host) is released from reset. 1: USB (Host) is in the reset state.	R/W
b31 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

6.3 Operation

6.3.1 RES# Pin Reset

This reset occurs when a signal arrives at the RES# pin from the externally connected reset circuit. When the signal becomes Low at the RES# pin, all the ongoing processes are aborted and the LSI enters the reset state. In order to reset the LSI without fail, the RES# pin should be held at Low level for the specified time after power-on. For details on the reset configuration, see section 10.3.5, Reset Configuration and the Method of Connecting with the Emulator.
After the reset is released, the CPU (Cortex-R4) starts reset exception handling.
When an RES# pin reset occurs, the RSTSR0.TRF flag is set to 1.

6.3.2 ECM Reset

This reset is generated in response to a reset request from ECM (Error Control Module).
ECM receives serious errors, such as oscillation stop detection, from individual modules in the LSI, and generates reset requests corresponding to respective errors. For details on the ECM operation, see section 42, Error Control Module (ECM). When an ECM reset occurs, all the ongoing processes are aborted and the LSI enters the reset state.
After the reset is released, the CPU (Cortex-R4) starts reset exception handling.
When an ECM reset occurs, the RSTSR0.ECMRF flag is set to 1.

6.3.3 Software Reset

The software reset occurs when “4321 A501h” is written to the SWRR1 register. When a software reset occurs, all the ongoing processes are aborted and the LSI enters the reset state.
After the reset is released, the CPU (Cortex-R4) starts reset exception handling.
When the software reset occurs, the RSTSR0.SWR1F flag is set to 1.

6.3.4 Software Reset 2 (for products incorporating an R-IN engine)

The software reset 2 applies to Cortex-M3 and WDTA for Cortex-M3. It occurs when 4321 A50Fh is written to the SWRR2 register. When an RES# pin reset, ECM reset, or software reset occurs, the software reset 2 becomes the reset state of the initial state.
To release the reset state of the software reset 2, write 0000 0000h to the SWRR2 register of Cortex-R4.

6.3.5 Determination of Reset Generation Source

Reading the RSTSR0 register determines which reset source was used for reset execution. Figure 6.1 shows an example of the flow to identify a reset generation source.

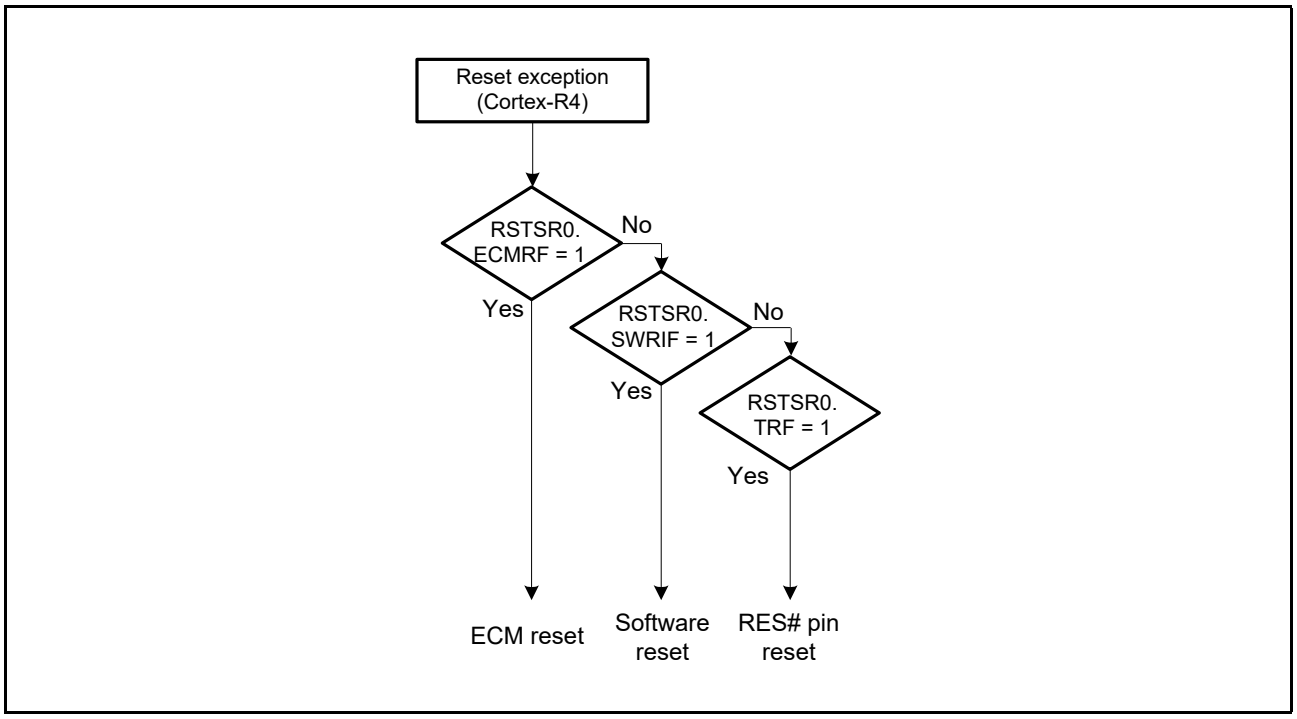


Figure 6.1 Example of Reset Generation Source Determination Flow

6.3.6 Reset Output Pin (RSTOUT#)

The reset output pin (RSTOUT#) outputs Low level upon occurrence of reset when the input level of the RES# pin is Low. It also outputs Low level upon occurrence of an ECM reset or software reset.

If the RES# pin remains Low for a specified time period and then changes to high, the reset output remains Low for 500 us (Typ.) and then changes to High. Similarly, when an ECM reset or software reset occurs, the reset output remains Low for 500 us (Typ.) and then changes to High.

6.3.7 Noise Cancellation for Reset Input

Noise cancellation using analog delay is applied to the RES# pin. This can eliminate noises within 100 ns (Min.).

6.4 Usage Note

6.4.1 Connection of Reset Output Pin (RSTOUT#)

The low level is output for a specified period of time on RSTOUT# after de-assertion of the signal on the RES# pin. This means that RSTOUT# should not be directly connected as a reset signal for a flash memory to be used in booting the LSI chip. Otherwise, release of the LSI chip itself from the reset state may precede that for the flash memory.
However, using RSTOUT# as the reset signal for external device is still possible as long as the timing requirement imposed by the output on the RSTOUT# pin is satisfied.
For details, see section 6.3.6, Reset Output Pin (RSTOUT#).

7. Clock Generation Circuit

7.1 Overview

This LSI incorporates a clock generation circuit.
Table 7.1 shows the specifications of the clock generation circuit. Figure 7.1, Figure 7.2 shows a block diagram of the clock generation circuit.

Table 7.1 Specifications of Clock Generation Circuit

Item	Specifications
Main clock oscillator	Resonator frequency: 25 MHz
	External clock input frequency: 25 MHz
	Connectable resonator or additional circuit: Ceramic resonator, crystal resonator Connection pin: EXTAL, XTAL
	Oscillation stop detection function: When an oscillation stop is detected with the main clock, the system clock source is switched to LOCO, and MTU3a and GPT output can be forcedly driven to the high-impedance.
PLL0 circuit	Input clock source: Main clock oscillator
	Input frequency: 25 MHz
	Frequency multiplication ratio: 48 multiplication
	Output clock frequency of the PLL0 circuit: 1200 MHz
	Oscillation abnormality detection function: When the CLMA0 detects an abnormality in oscillation of the PLL0, the system clock source is switched to main clock, and MTU3a and GPTa pins are placed in the high-impedance state.
PLL1 circuit	Input clock source: PLL0 clock divided by 80
	Input frequency: 15 MHz
	Frequency multiplication ratio: Selectable from 60 and 80
	Output clock frequency of the PLL1 circuit: 900 MHz, 1200 MHz
	Oscillation abnormality detection function: When the CLMA1 detects an abnormality in oscillation of the PLL1, the system clock source is switched to main clock, and MTU3a and GPTa pins are placed in the high-impedance state.
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz
	Oscillation abnormality detection function: The CLMA2 can detect an abnormality in oscillation of the LOCO.
External clock input for SSI (AUDIO_CLK)	Input frequency: 50 MHz (max.)
External clock input (TCK) for JTAG	Input frequency: 50 MHz (max.)

Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (1 / 2)

Item	Clock Source	Supplied to	Frequency
CPU clock (CPUCLK)	Selected from frequency-dividing clocks for PLL0 or PLL1	CPU (Cortex-R4)	150 MHz 300 MHz 450 MHz 600 MHz
System clock (ICLK)	Selected from frequency-dividing clocks for PLL0 or PLL1	CPU (Cortex-M3 (for products incorporating an R-IN engine)), DMAC, interrupt controller, on-chip extended SRAM	150 MHz
High-speed peripheral module clock (PCLKA)	Selected from frequency-dividing clocks for PLL0 or PLL1	Peripheral module	150 MHz
Low-speed peripheral module clock (PCLKB)	Selected from frequency-dividing clocks for PLL0 or PLL1	Peripheral module	75 MHz
High-speed peripheral module clock (PCLKC)	Frequency-dividing clock for PLL0	Peripheral modules (GPTa, MTU3a)	150 MHz
Low-speed peripheral module clock (PCLKD)	Frequency-dividing clock for PLL0	Peripheral modules (CRC, DOC, ECM, ELC, TPU, POE3, PPG, CMT, CMTW, and RIIC)	75 MHz
Low-speed peripheral module clock (PCLKE)	Frequency-dividing clock for PLL0	Peripheral module (WDTA)	Up to 75 MHz
Low-speed peripheral module clock (PCLKF)	Frequency-dividing clock for PLL0	Peripheral module (12-bit A/D converter Unit 0)	Up to 60 MHz
Low-speed peripheral module clock (PCLKG)	Frequency-dividing clock for PLL0	Peripheral module (12-bit A/D converter Unit 1)	Up to 60 MHz
Low-speed peripheral module clock (PCLKH)	Frequency-dividing clock for PLL0	Peripheral module (12-bit A/D converter, bus clock for units 0 and 1)	60 MHz
External bus clock (CKIO)	Frequency-dividing clock for PLL0 or PLL1	External bus	Up to 75 MHz
High-speed serial clock (SERICLK)	Frequency-dividing clock for PLL0	RSPIa, SCIFA	150 MHz, 120 MHz
USB clock M (USBMCLK)	Frequency-dividing clock for PLL0	USB PHY	50 MHz
USB clock P (USBPCLK)	Frequency-dividing clock for PLL0	USB	30 MHz
Ethernet clock A (ETCLKA)	Frequency-dividing clock for PLL0	EtherCAT (optional), Ethernet switch	100 MHz
Ethernet clock B (ETCLKB)	Frequency-dividing clock for PLL0	RMII converter	50 MHz
Ethernet clock C (ETCLKC)	Frequency-dividing clock for PLL0	Ethernet switch	200 MHz
Ethernet clock D (ETCLKD)	Frequency-dividing clock for PLL0	Ethernet MAC (MDC_CLK)	Up to 12.5 MHz
Ethernet clock E (ETCLKE)	Selected from main clock or frequency-dividing clock for PLL0	Ethernet PHY	25 MHz, 50 MHz
Ethernet clock F (ETCLKF)	Frequency-dividing clock for PLL0	EtherCAT (optional)	25 MHz
Ethernet clock G (ETCLKG)	Frequency-dividing clock for PLL0	Ethernet switch	125 MHz
Clock A for RSCAN (CANCLKA)	Frequency-dividing clock for PLL0	RSCAN	24 MHz
Clock B for RSCAN (CANCLKB)	Main clock	RSCAN	25 MHz
CLMAn sampling clock (CLMAMCLKA) (n = 1 or 0)	Main clock divided by 2	CLMA0, CLMA1	12.5 MHz
CLMA2 sampling clock (CLMAMCLKB)	Main clock divided by 256	CLMA2	97.6 kHz
CLMA2 monitor clock (CLMALCLK)	LOCO	CLMA2	240 kHz
CLMA0 monitor clock (CLMAPLCLK0)	PLL0 clock divided by 16	CLMA0	75 MHz

Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (2 / 2)

Item	Clock Source	Supplied to	Frequency
CLMA1 monitor clock (CLMAPLCLK1)	PLL1 clock divided by 16	CLMA1	75 MHz, 56.25 MHz*1
IWDT clock (IWDTCLK)	LOCO clock divided by 2	IWDT	120 kHz
ECM clock (ECMCKL)	LOCO	ECM	240 kHz
SSI clock (ACLK)	AUDIO_CLK	SSI	1 MHz to 50 MHz
Delta-sigma interface clock 0 (DSCLK0)	Frequency-dividing clock for PLL0	Delta-sigma interface (channels 0 to 2)	Up to 25 MHz
Delta-sigma interface clock 1 (DSCLK1)	Frequency-dividing clock for PLL0	Delta-sigma interface (channel 3)	Up to 25 MHz
JTAG clock (JTAGTCK)	TCK	JTAG	Up to 50 MHz
Trace interface clock (TCLK)	Selected from frequency-dividing clocks for PLL0 or PLL1	CoreSight TPIU	75 MHz

Note 1. Selecting 10b in the PLL1CR.CPUCKSEL[1:0] bits outputs 56.25 MHz. Selecting values other than 10b outputs 75 MHz.

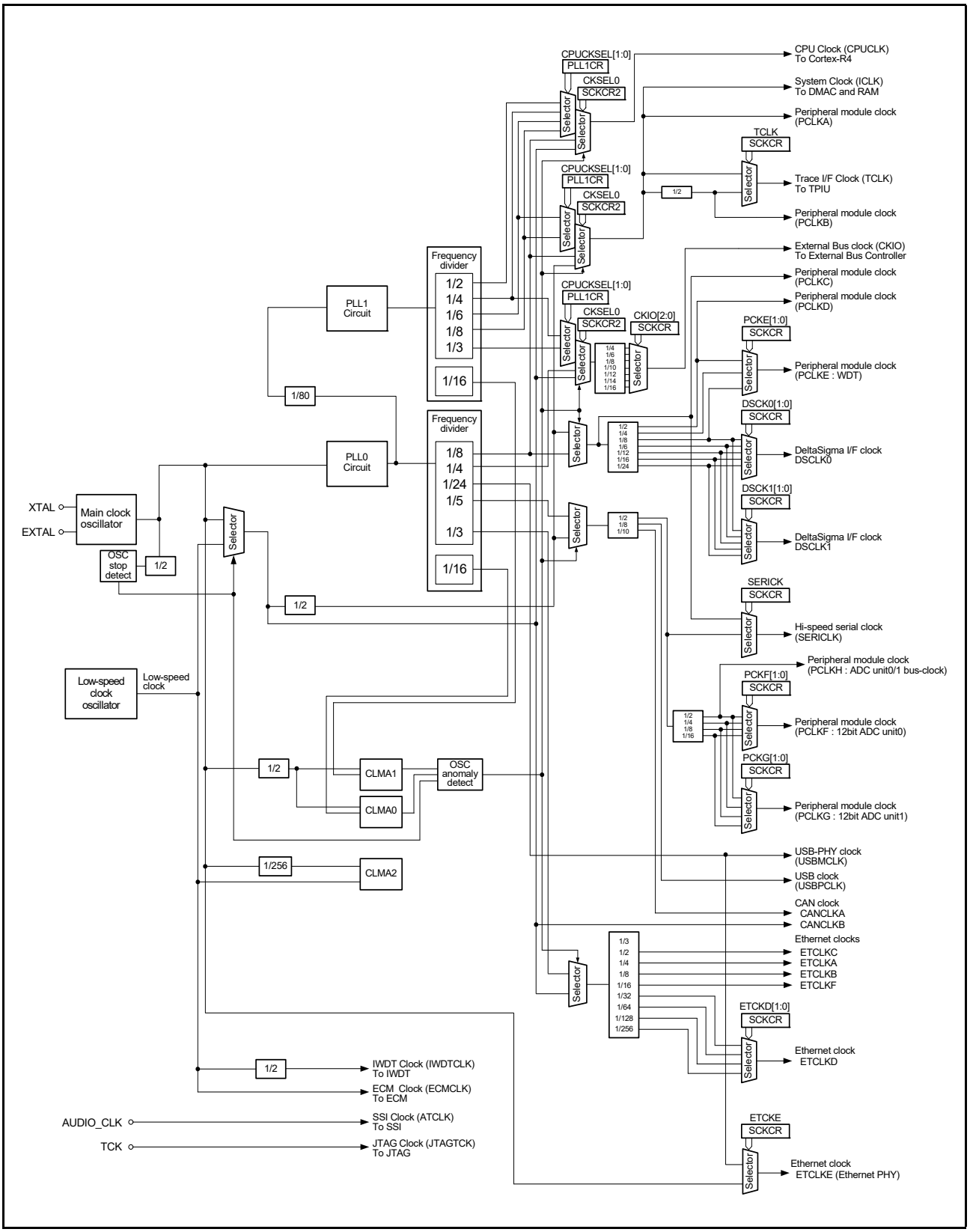


Figure 7.1 Block Diagram of Clock Generation Circuit

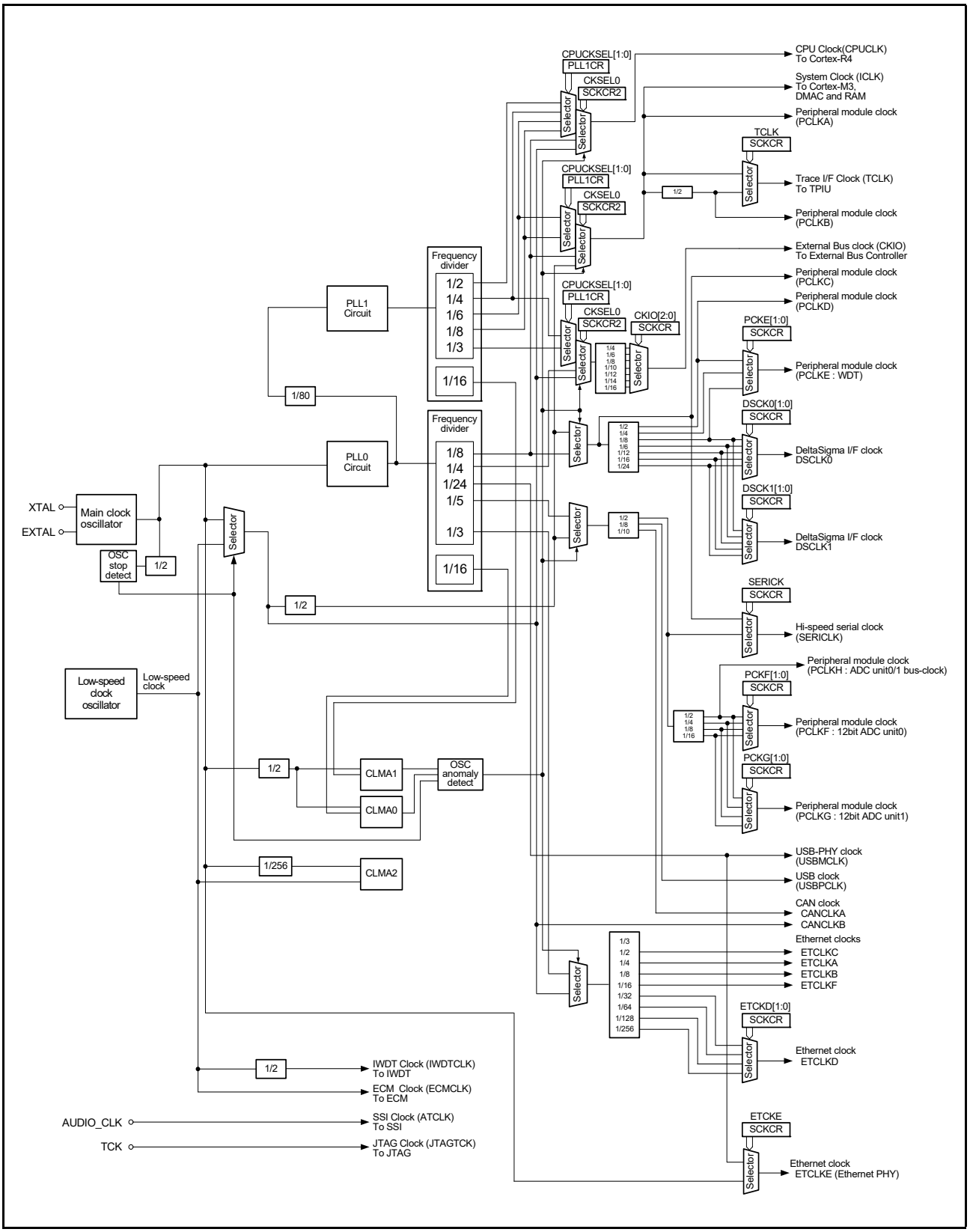


Figure 7.2 Block Diagram of Clock Generation Circuit (for products incorporating an R-IN engine)

Table 7.3 shows the input/output pins of the clock generation circuit.

Table 7.3 Pin Configuration of Clock Generation Circuit

Pin Name	I/O	Description
XTAL	Output	These pins are used to connect a crystal resonator. An external clock signal can also be input to the EXTAL pin. For details, see section 7.3.2, External Clock Input.
EXTAL	Input	
TCK	Input	This pin is used to input the clock for the JTAG.
AUDIO_CLK	Input	This pin is used to input the clock for the SSI.
CKIO	Output	This pin is used to supply the external bus clock (CKIO) to external devices.
OSCTH	Input	How to supply the clock signal to the main clock oscillator is specified based on the input level. Low: Connecting an oscillator High: External clock input
CLKOUT25M0	Output	This pin is used to supply Ethernet PHY0 with the main clock (25 MHz) or frequency-dividing clock of PLL0 (50 MHz).
CLKOUT25M1	Output	This pin is used to supply Ethernet PHY1 with the main clock (25 MHz) or frequency-dividing clock of PLL0 (50 MHz).
CLKOUT25M2	Output	This pin is used to supply Ethernet PHY2 with the main clock (25 MHz) or frequency-dividing clock of PLL0 (50 MHz).
MCLK0	I/O	Clock input/output pins for the delta-sigma interface. These pins are used as output pins when the clock is supplied to a delta-sigma modulator. These pins are used as input pins when the clock is supplied from the external clock generation circuit for the delta-sigma interface. For how to switch the clock, see section 7.2.3, Delta-Sigma Interface Clock Control Register (DSCR).
MCLK1	I/O	
MCLK2	I/O	
MCLK3	I/O	

7.2 Register Descriptions

The registers related to the clock generation circuit can be write-protected. To write to the registers, specify bit 0 of the Protect Register (PRCR) to cancel the write protection. For details, see section 11, Register Write Protection Function.

7.2.1 System Clock Control Register (SCKCR)

The SCKCR register is used to select the frequency for each of the delta-sigma interface clock (DSCLK), trace interface clock (TCLK), high-speed serial clock (SERICLK), Ethernet clocks (ETCLKD and ETCLKE), external bus clock (CKIO), peripheral module clocks (PCLKE, PCLKF, and PCLKG) and the clocks supplied to the delta-sigma interface.

Address(es): A00B 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	TCLK	—	—	—	SERICK
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ETCKD[1:0]		—	ETCKE	—	CKIO[2:0]			—	—	PCKE[1:0]		PCKF[1:0]		PCKG[1:0]	
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PCKG[1:0]	Peripheral Module Clock G (PCLKG) Select	Select the low-speed peripheral module clock PCLKG supplied to the 12-bit A/D converter unit 1. 00: 60 MHz 01: 30 MHz 10: 15 MHz 11: 7.5 MHz	R/W
b3, b2	PCKF[1:0]	Peripheral Module Clock F (PCLKF) Select	Select the low-speed peripheral module clock PCLKF supplied to the 12-bit A/D converter unit 0. 00: 60 MHz 01: 30 MHz 10: 15 MHz 11: 7.5 MHz	R/W
b5, b4	PCKE[1:0]	Peripheral Module Clock E (PCLKE) Select	Select the low-speed peripheral module clock PCLKE supplied to the WDTA. 00: 75 MHz 01: 37.5 MHz 10: 18.75 MHz Settings other than above are prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CKIO[2:0]	External Bus Clock (CKIO) Select	Select the frequency of the external bus clock CK10. 000: 75 MHz 001: 50 MHz 010: 37.5 MHz 011: 30 MHz 100: 25 MHz 101: 21.43 MHz 110: 18.75 MHz Settings other than above are prohibited.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b12	ETCKE	Ethernet Clock E (ETCLKE) Select	Selects the Ethernet clock ETCLKE supplied to Ethernet PHY. 0: Main clock (25 MHz) 1: Frequency-dividing clock of PLL0 (50 MHz)	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	ETCKD[1:0]	Ethernet Clock D (ETCLKD) Select	Select the Ethernet clock ETCLKD supplied to the Ethernet MAC. 00: 12.5 MHz 01: 6.25 MHz 10: 3.125 MHz 11: 1.563 MHz	R/W
b16	SERICK	High-Speed Serial Clock (SERICLK) Select	Selects the high-speed serial clock SERICLK supplied to RSPIa and SCIFA. 0: 150 MHz 1: 120 MHz	R/W
b19 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	TCLK	Trace interface clock (TCLK)	Selects the clock supplied to the trace I/F clock TCLK (CoreSight TPIU). 0: Setting prohibited 1: 75 MHz	R/W
b31 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

7.2.2 System Clock Control Register 2 (SCKCR2)

The SCKCR2 register is used to select PLL0 or PLL1 as the source of clocks supplied to the system clock.

Address(es): A00B 0024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CKSEL 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CKSEL0	System Clock Source Select	Selects the source of the CPU clock (CPUCLK), system clock (ICLK), high-speed peripheral module clock (PCLKA), low-speed peripheral module clock (PCLKB), and external bus clock (CKIO). Switching to a clock source which is not in operation is prohibited. 0: PLL0 is selected. 1: PLL1 is selected.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

7.2.3 Delta-Sigma Interface Clock Control Register (DSCR)

The DSCR register is used to select the clocks that are supplied to the delta-sigma interface.

Address(es): A00B 0028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	DSINV 1	DSCK1[2:0]			DSSEL 1
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	DSCHSEL	DSINV 0	DSCK0[2:0]			DSSEL 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	DSSEL0	Delta-Sigma Interface Clock 0 Supply Source Select (channels 0 to 2)	Selects the clock supplied to the delta-sigma interface (channels 0 to 2). 0: Supplied from outside the LSI (slave operation) 1: Supplied from the clock generation circuit (master operation)	R/W
b3 to b1	DSCK0[2:0]	Delta-Sigma Interface Clock 0 (DSCLK0) Frequency Select (channels 0 to 2)	Select the frequency of the delta-sigma interface clock output from the MCLKn pin (n = 0 to 2) when the delta-sigma interface operates as a master. The same clock frequency is used for the channels. 000: 25 MHz 001: 18.75 MHz 010: 12.5 MHz 011: 9.375 MHz 100: 6.25 MHz Settings other than above are prohibited.	R/W
b4	DSINV0	Delta-Sigma Interface Clock 0 (DSCLK0) Polarity Select (channels 0 to 2)	In master operation (DSSEL0 = 1): Selects whether to use the inverted internal operating clock for the delta-sigma interface clock output from the MCLKn pin (n = 0 to 2). In slave operation (DSSEL0 = 0): Selects whether to use the inverted internal operating clock for the delta-sigma interface clock input from the MCLKn pin (n = 0 to 2). Change the polarity to adjust the phase with the operating clock of external delta-sigma ADC. 0: Not inverted 1: Inverted	R/W
b5	DSCHSEL	Delta-Sigma Interface (channels 0 to 2) Supply Channel Select	Selects the path of the clock input to the MCLKn pin (n = 0 to 2) when the delta-sigma interface operates as a slave. If 0 is selected, the clocks input to the individual MCLKn pin are used. If 1 is selected, only the clock input to the MCLK0 pin is used. Select this when only one clock is supplied from outside the LSI. 0: Clocks input to the individual MCLKn pin are used. 1: The clock input to the MCLK0 pin is used.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DSSEL1	Delta-Sigma Interface Clock 1 Supply Source Select (channels 3)	Selects the source of the clock supplied to the delta-sigma interface (channels 3). 0: Supplied from outside the LSI (slave operation) 1: Supplied from the clock generation circuit (master operation)	R/W

Bit	Symbol	Bit Name	Description	R/W
b19 to b17	DSCK1[2:0]	Delta-Sigma Interface Clock 1 (DSCLK1) Frequency Select (channel 3)	Select the frequency of the delta-sigma interface clock output from the MCLK3 pin when the delta-sigma interface operates as a master. 000: 25 MHz 001: 18.75 MHz 010: 12.5 MHz 011: 9.375 MHz 100: 6.25 MHz Settings other than above are prohibited.	R/W
b20	DSINV1	Delta-Sigma Interface Clock 1 (DSCLK1) Polarity Select (channel 3)	In master operation (DSSEL1 = 1): Selects whether to use the inverted internal operating clock for the delta-sigma interface clock output from the MCLK3 pin. In slave operation (DSSEL1 = 0): Selects whether to use the inverted internal operating clock for the delta-sigma interface clock input from the MCLK3 pin. Change the polarity to adjust the phase with the operating clock of external delta-sigma ADC. 0: Not inverted 1: Inverted	R/W
b31 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

7.2.4 PLL1 Control Register (PLL1CR)

The PLL1CR register is used to set the CPU clock frequency.

Address(es): A00B 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUCKSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CPUCKSEL [1:0]	CPU Operating Frequency Select	Select the CPU clock frequency. After setting this bit to select the CPU operating frequency, use the PLL1CR2 register to control operation of the PLL1 circuit. For the procedure for changing the CPU frequency, see Figure 7.3. b1 b0 00: 150 MHz 01: 300 MHz 10: 450 MHz 11: 600 MHz	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Set the frequency within the allowable range for the electrical characteristics of the CPU frequency clock.
Note 2. The relationship between the PLL1 frequency multiplication ratio and clock division ratio specified with CPUCKSEL[1:0] is shown in Table 7.4.

Table 7.4 Relationship Between PLL1 Frequency Multiplication Ratio and Clock Division Ratio Specified with CPUCKSEL[1:0]

CPUCKSEL[1:0]	PLL1 Frequency Multiplication Ratio	Clock Division Ratio	CPU Operating Frequency
00	80	1/8	150 MHz
01	80	1/4	300 MHz
10	60	1/2	450 MHz
11	80	1/2	600 MHz

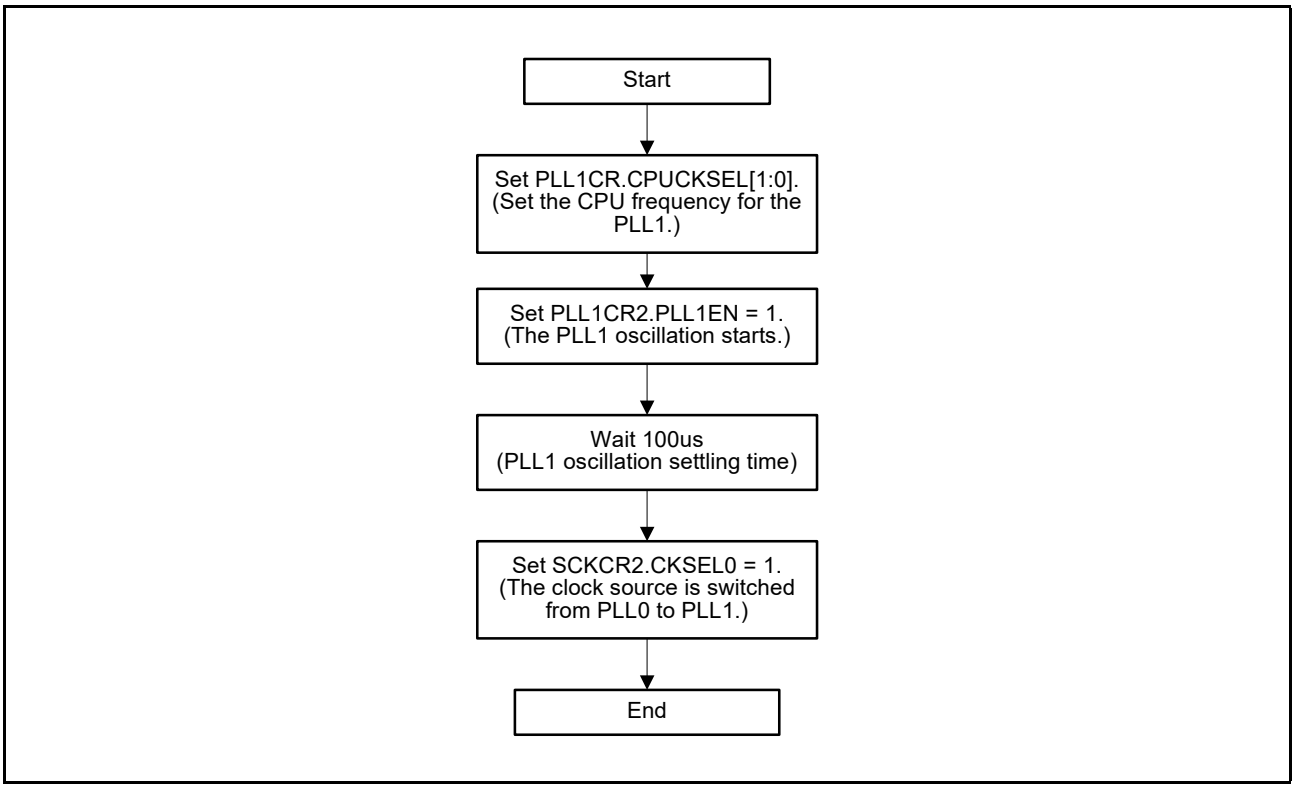


Figure 7.3 Changing the CPU Frequency

7.2.5 PLL1 Control Register 2 (PLL1CR2)

The PLL1CR2 register is used to control operation of the PLL1 circuit.

Address(es): A00B 0038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLL1EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PLL1EN	PLL1 Operation Control	Specifies whether to run or stop PLL1. 0: PLL1 stops 1: PLL1 runs If the PLL1EN bit is set to 1, 100 us of the PLL oscillation settling time must be counted by using loop processing in the CPU or by a timer. For details about how to change the CPU frequency, see Figure 7.3.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Before you attempt to set the CPU clock frequency by using the PLL1CR register, stop the PLL by setting the PLL1EN bit to 0.

7.2.6 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

LOCOCR is used to control operation of a low-speed on-chip oscillator.

Address(es): A00B 0040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	LCSTP	LOCO Stop	Specify whether to run or stop the low-speed on-chip oscillator (LOCO). 0: Run 1: Stop After setting this bit to run the LOCO, start using the LOCO clock after the LOCO oscillation stabilization time (t_{LOCOWT}) has elapsed.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To stop the LOCO and then run it again, wait at least the LOCO oscillation stabilization time (t_{LOCOWT}) is elapsed after setting the LCSTP bit to stop the LOCO, and then set the LCSTP bit to run the LOCO again.
To set the bit to stop the LOCO, make sure that the LOCO oscillation is stable.

Note 2. Writing of 1 to the LCSTP bit (stop the LOCO) is prohibited if the oscillation stop detection function is enabled by setting the OSTDCR.OSTDE bit.

7.2.7 Oscillation Stop Detection Control Register (OSTDCR)

The OSTDCR register is used to control the oscillation stop detection function of the main clock.

Address(es): A00B 004Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	Enable or disable the oscillation stop detection interrupt (OSTDI). This also specifies whether the oscillation stop detection is notified to the port output enable (POE). 0: Oscillation stop detection interrupt is disabled. Oscillation stop detection is not notified to the POE. 1: Oscillation stop detection interrupt is enabled. Oscillation stop detection is notified to the POE.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	Enable or disable the oscillation stop detection function. If the oscillation stop detection function is enabled, the LCSTP bit of the low-speed on-chip oscillator control register (LOCOCR) is also set to 0, and the low-speed on-chip oscillator operation starts.*1 0: The oscillation stop detection function is disabled. 1: The oscillation stop detection function is enabled.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The low-speed on-chip oscillator cannot be stopped while the oscillation stop detection function is enabled (OSTDE bit = 1). Writing 1 to the LOCOCR.LCSTP bit is ignored.

7.3 Selecting Input to Main Clock Oscillator

The clock signal is supplied to the main clock oscillator by connecting a resonator. The clock input mode is set based on the status of the OSCTH pin. For details about the settings, see Table 7.5.

Table 7.5 Clock Input Mode Selected for OSCTH Pin

OSCTH Pin	Clock Input Mode
Low	An oscillator is connected
High	External clock is input

7.3.1 Connecting a Crystal Resonator

Figure 7.4 shows an example of connecting a crystal resonator.
A damping resistor Rd should be added, if necessary. Because the resistor values vary depending on the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If use of an external feedback resistor (Rf) is directed by the resonator manufacturer, insert an Rf between EXTAL and XTAL by following the instruction.
When connecting a resonator to supply the clock, the frequency of the resonator should be in the frequency range of the resonator for the main clock oscillator described in Table 7.1.

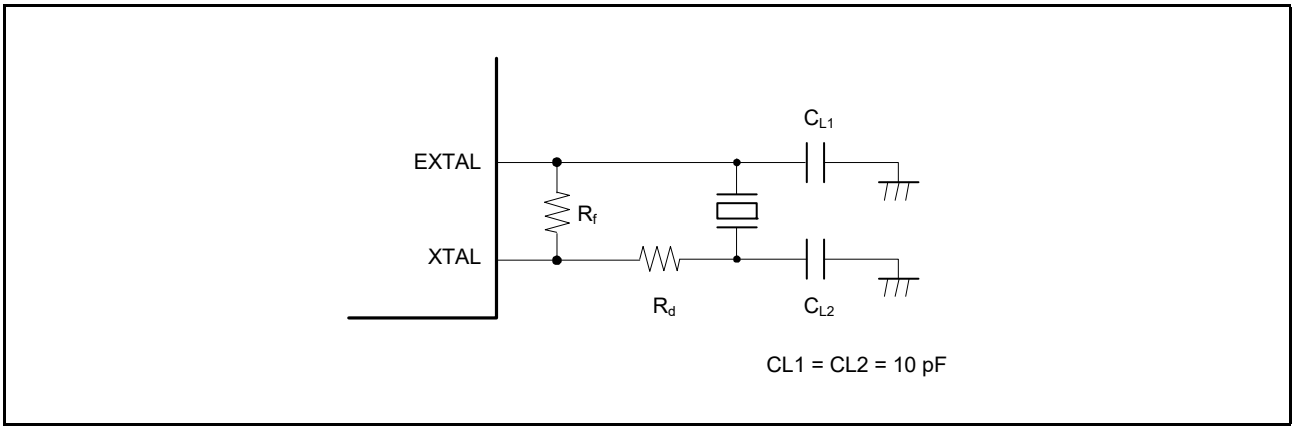


Figure 7.4 Example of Crystal Resonator Connection

Table 7.6 Damping Resistance (Reference Values)

Frequency (MHz)	25
Rd (Ω)	2.2K

Figure 7.5 shows an equivalent circuit of the crystal resonator. Use a crystal resonator that has the characteristics shown in Table 7.7.

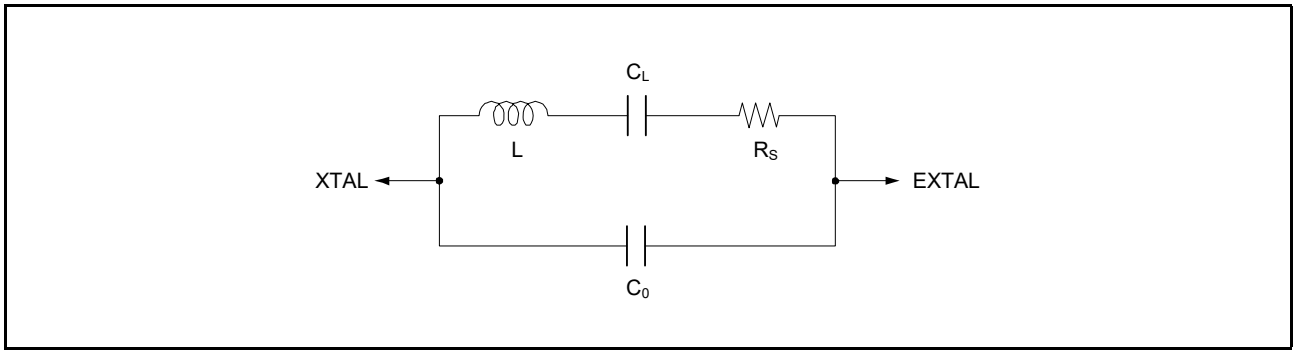


Figure 7.5 Equivalent Circuit of Crystal Resonator

Table 7.7 Crystal Resonator Characteristics (Reference Values)

Frequency (MHz)	25
R_S max (Ω)	100

7.3.2 External Clock Input

Figure 7.6 shows an example of connection of external clock input. To open the XTAL pin, make sure that the parasitic capacity is not more than 10 pF.

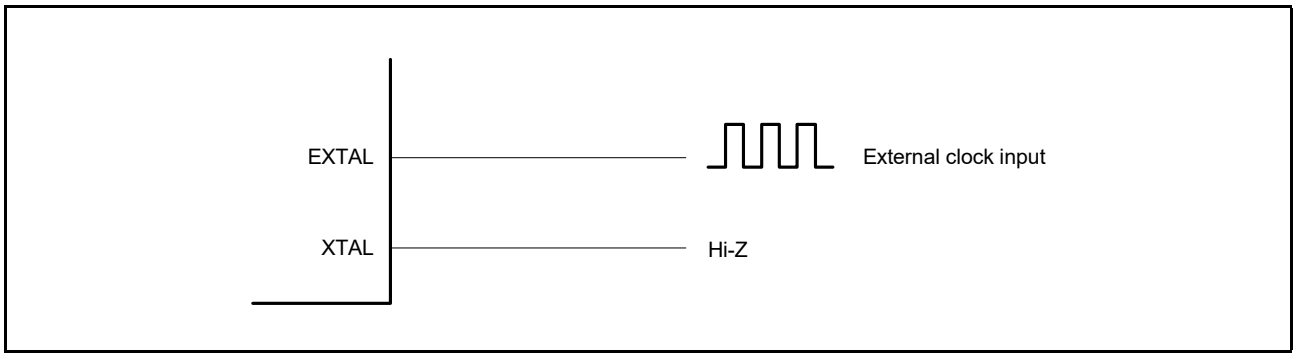


Figure 7.6 Example of External Clock Connection

7.4 Oscillation Stop Detection Function

7.4.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop and to supply LOCO clock pulses from the low-speed on-chip oscillator as the system clock source instead of the main clock, PLL0 clock, and PLL1 clock.
An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the MTU3a and GPTa output can be forcedly driven to the high-impedance on the detection. For details, see section 19, Multi-Function Timer Pulse Unit (MTU3a), section 20, Port Output Enable 3 (POE3), and section 21, General PWM Timer (GPTa).
This LSI detects a main clock oscillation stop when the input clock remains to be 0 or 1 for a certain period, for example, due to a malfunction of the main clock oscillator (see Table 47.40, Oscillation Stop Detection Circuit Characteristics, in section 47.8, Oscillation Stop Detection Timing).
When an oscillation stop is detected, clocks are switched to the LOCO clock.

After a reset is released, the oscillation stop detection function is disabled. To enable the oscillation stop detection function, set the OSTDCR.OSTDE bit to 1.
The clocks that are switched to the LOCO clock by the oscillation stop detection are the PLL0 clock, PLL1 clock, and clock B for RSCAN (CANCLKB).

7.4.2 Oscillation Stop Detection Interrupt

An oscillation-stop detection interrupt (OSTDI) will be generated if the oscillation-stop detection interrupt enable bit (OSTDCR.OSTDIE) is 1 (enabling interrupt generation on oscillation stop detection). At this time, the main clock oscillator stop is notified to the port output enable 3 (POE). On accepting the notification of the oscillation stop, the POE sets the OSTST high-impedance flag (POE.OSTSTF).
The oscillation stop detection interrupt is connected to the Error Control Module (ECM) as an error interrupt. Interrupts are disabled in the initial state after a reset release. To use oscillation stop detection interrupts, select maskable or non-maskable interrupt as the operation to be performed when the ECN detects an error interrupt. For details, see section 42, Error Control Module (ECM).

7.5 PLL Oscillation Abnormality Detection Function

The PLL oscillation abnormality detection function detects an abnormality in oscillation of the PLL0 or PLL1 by using the clock monitor circuits (CLMA0 and CLMA1) to monitor the frequency, and supplies the main clock instead of the PLL0 clock or PLL1 clock. For details about the CLMA, see section 8, Clock Monitor Circuit (CLMA).

7.6 Low-Speed On-Chip Oscillator Oscillation Abnormality Detection Function

The clock monitor circuit (CLMA2) can be used to detect an abnormality in oscillation of the low-speed on-chip oscillator. For details about the CLMA, see section 8, Clock Monitor Circuit (CLMA).

7.7 PLL Circuit

The PLL circuit has a function to multiply the frequency from the oscillator.

7.8 Internal Clock

Clock sources of internal clock signals are the main clock, LOCO clock, PLL0 clock, PLL1 clock, and the external clock for JTAG. The 14 types of internal clocks listed below are produced from these sources.

(1) Operating clock of the CPU: CPU clock (CPUCLK)
(2) Operating clock of DMAC, interrupt controller, and RAM with ECC: System clock (ICLK)
(3) Operating clocks of peripheral modules: Peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD, PCLKE, PCLKF, PCLKG, and PCLKH)
(4) Clock for the external bus controller and external pin output: External bus clock (CKIO)
(5) Operating clock for high-speed serial clock: High-speed serial clock (SERICLK)
(6) Operating clock for USB-PHY: USB clock M (USBMCLK)
(7) Operating clock for USB: USB clock P (USBPCLK)
(8) Operating clocks for Ethernet: Ethernet clocks (ETCLKA, ETCLKB, ETCLKC, ETCLKD, ETCLKE, ETCLKF, and ETCLKG)
(9) Operating clock for the CLMA module: CLMA clocks (CLMAMCLKA, CLMAMCLKB, CLMALCLK, CLMAPLCLK0, and CLMAPLCLK1)
(10) Operating clock for the IWDT module: IWDT-dedicated clock (IWDTCLK)
(11) Operating clock for SSI: SSI clock (ACLK)
(12) Operating clocks for delta-sigma interface: Delta-sigma interface clocks (DSCLK0 and DSCLK1)
(13) Operating clock for the JTAG module: JTAG clock (JTAGTCK)
(14) Operating clock for the trace interface: Trace interface clock (TCLK)

7.8.1 CPU Clock (CPUCLK)

The CPU clock (CPUCLK) is used as the operating clock of the CPU.
The CPU operating frequency is specified by the PLL1CR.CPUCKSEL[1:0] bits.

7.8.2 System Clock (ICLK)

The system clock (ICLK) is used as the operating clock of DMAC, interrupt controller, and on-chip extended SRAM with ECC.
The frequency of ICLK is fixed to 150 MHz. It cannot be specified by the user.

7.8.3 High-Speed Peripheral Module Clock (PCLKA)

The high-speed peripheral module clock (PCLKA) is used as the operating clock for high-speed peripheral modules.
The frequency of PCLKA is fixed to 150 MHz. It cannot be specified by the user.

7.8.4 Low-Speed Peripheral Module Clock (PCLKB)

The low-speed peripheral module clock (PCLKB) is used as the operating clock for low-speed peripheral modules.
The frequency of PCLKB is fixed to 75 MHz. It cannot be specified by the user.

7.8.5 High-Speed Peripheral Module Clock (PCLKC)

The high-speed peripheral module clock (PCLKC) is used as the operating clock for high-speed peripheral modules.
The frequency of PCLKC is fixed to 150 MHz. It cannot be specified by the user.

7.8.6 Low-Speed Peripheral Module Clocks (PCLKD, PCLKE, PCLKF, PCLKG, and PCLKH)

The unmodulated low-speed peripheral module clocks (PCLKD, PCLKE, PCLKF, PCLKG, and PCLKH) are operating clocks for use by low-speed peripheral modules. The frequencies of PCLKD and PCLKH are respectively fixed to 75 MHz and 60 MHz. They cannot be specified by the user. The frequency of PCLKE, PCLKF, and PCLKG is set by the SCKCR.PCKE[1:0], SCKCR.PCKF[1:0], and SCKCR.PCKG[1:0] bits, respectively.

7.8.7 External Bus Clock (CKIO)

The external bus clock (CK10) is used as an operating clock.
The CK10 operating frequency is specified by the SCKCR.CKIO[2:0] bits.

7.8.8 High-Speed Serial Clock (SERICLK)

The high-speed serial clock (SERICLK) is used as the operating clock for SCIFA and RSPIa.
The SERICLK operating frequency is specified by the SCKCR.SERICK bit.

7.8.9 USB Clock M (USBMCLK)

The USB M (USBMCLK) is used as the operating clock for USB PHY.
The frequency of USBMCLK is fixed to 50 MHz. It cannot be specified by the user.

7.8.10 USB Clock P (USBPCLK)

The clock P (USBPCLK) is used as the operating clock for USB.
The frequency of USBPCLK is fixed to 30 MHz. It cannot be specified by the user.

7.8.11 Ethernet Clocks (ETCLKA, ETCLKB, ETCLKC, ETCLKD, ETCLKE, ETCLKF, and ETCLKG)

Ethernet clocks (ETHCLKA to ETCLKF) are the operating clocks for use with EtherCAT.
The ETCLKD operating frequency is specified by the SCKCR.ETCKD[1:0] bits. The ETCLKE operating frequency is specified by the SCKCR.ETCKE bit.
Frequencies of the Ethernet clocks other than ETCLKD and ETCLKE are fixed. They cannot be specified by the user.

7.8.12 CLMA Clocks (CLMAMCLKA, CLMAMCLKB, CLMALCLK, CLMAPLCLK0, and CLMAPLCLK1)

The CLMA clocks (CLMAMCLKA, CLMAMCLKB, CLMALCLK, CLMAPLCLK0, and CLMAPLCLK1) are used as the operating clocks for the CLMA module.
CLMAMCLKA and CLMAMCLKB are obtained by frequency-dividing the main clock.
CMLAMCLK is generated by internal oscillation of the low-speed on-chip oscillator.
CMLAPLCLK0 and CLMAPLCLK1 are obtained by frequency-dividing the clocks which are generated by internal oscillation of PLL0 and PLL1 circuits.

7.8.13 IWDT Clock (IWDTCLK)

The IWDT clock (IWDTCLK) is used as the operating clock for the IWDT module.
IWDTCLK is a 1/2 clock internally generated by the low-speed on-chip oscillator.

7.8.14 ECM Clock (ECMCLK)

The ECM clock (ECMCLK) is used as the delay counter operating clock for the ECM module.
ECMCLK is generated by internal oscillation of the low-speed on-chip oscillator.

7.8.15 SSI Clock (ACLK)

The SSI clock (ACLK) is used as the operating clock for SSI.
ACLK is supplied from the external clock input for SSI (AUDIO_CLK).

7.8.16 Delta-Sigma Interface Clock 0 (DSCLK0)

The delta-sigma interface clock 0 (DSCLK0) is used as the operating clock for the delta-sigma interface (channels 0 to 2).
If the DSCR.DSSEL0 bit is 0, the clock generated by the external clock input for the delta-sigma interface is selected as DSCLK0. If the DSCR.DSSEL0 bit is 1, the clock generated by the clock generation circuit (PLL0) is selected.
When the clock generated by the clock generation circuit is used, the operating clock is specified by the DSCR.DSCK0[2:0] bits.

7.8.17 Delta-Sigma Interface Clock 1 (DSCLK1)

The delta-sigma interface clock 1 (DSCLK1) is used as the operating clock for the delta-sigma interface (channels 3).
If the DSCR.DSSEL1 bit is 0, the clock generated by the external clock input for the delta-sigma interface is selected as DSCLK1. If the DSCR.DSSEL1 bit is 1, the clock generated by the clock generation circuit (PLL0) is selected.
When the clock generated by the clock generation circuit is used, the operating clock is specified by the DSCR.DSCK1[2:0] bits.

7.8.18 JTAG Clock

The JTAG-dedicated clock (JTAGTCK) is the operating clock for the JTAG.
JTAGTCK is generated by the external clock for JTAG (TCK).

7.8.19 Trace Interface Clock (TCLK)

The trace interface clock (TCLK) is used as the operating clock for the trace interface within Coresight.
This clock is obtained by frequency-dividing the clock which is generated by internal oscillation within the PLL0 or PLL1 circuit.
This clock divided by two is output from the LSI as the trace clock for on-chip debugger (TRACECLK).

7.9 Usage Notes

7.9.1 Notes on Clock Generation Circuit

(1) Note that the operating frequency of the external bus clock (CKIO) and high-speed serial clock (SERICLK) that are supplied to the modules based on the SCKCR register settings varies before and after the frequency is changed.
(2) Do not change the clock frequency during access via the external bus. To start access via the external bus after the clock frequency is changed, confirm that the change to the frequency has been completed before you start access via the bus.
(3) After the clock source of CPUCLK is changed from PLL0 to PLL1, do not change the frequency specified in the PLL1CR.CPUCKSEL bit.
(4) Do not change the PCLKE clock frequency after the WDTA counting started. To start the WDTA counting after the clock frequency is changed, confirm that the change to the frequency has been completed before you start the WDTA counting.
(5) The ETCLKE frequency can be changed when the external Ethernet PHY is in the reset state. Do not change the frequency after release from the reset state.
(6) Do not change the ETCLKD clock frequency while the Ethernet MAC is operating. To cancel the module-stop state after the clock frequency is changed, confirm that the change to the frequency has been completed before you cancel the module-stop state.
(7) Do not change the SERICLK clock frequency while the RSPIa (channels 0 to 3) or SCIFA (channels 0 to 4) is operating. To cancel the module-stop state after the clock frequency is changed, confirm that the change to the frequency has been completed before you cancel the module-stop state.
(8) Do not change the DSCLK0 or DSCLK1 clock frequency or switch the clock while the delta-sigma interface is operating. To cancel the module-stop state after the clock frequency is changed or after the clock is switched, confirm that the change or switching has been completed before you cancel the module-stop state.
(9) In order to secure processing after the clock frequency is changed, dummy read the same register at least three times after writing to change the frequency, and only then proceed with the subsequent processing.

7.9.2 Notes on Resonator

Since various resonator characteristics relate closely to the user's board design, adequate evaluation is required on the user side before use, referencing the resonator connection example shown in this section. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Therefore, the circuit constants should be determined in full consultation with the resonator manufacturer. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

7.9.3 Notes on Designing the Board

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Other signal lines should be routed away from the oscillation circuit as shown in Figure 7.7. This prevents electromagnetic induction from interfering with correct oscillation.

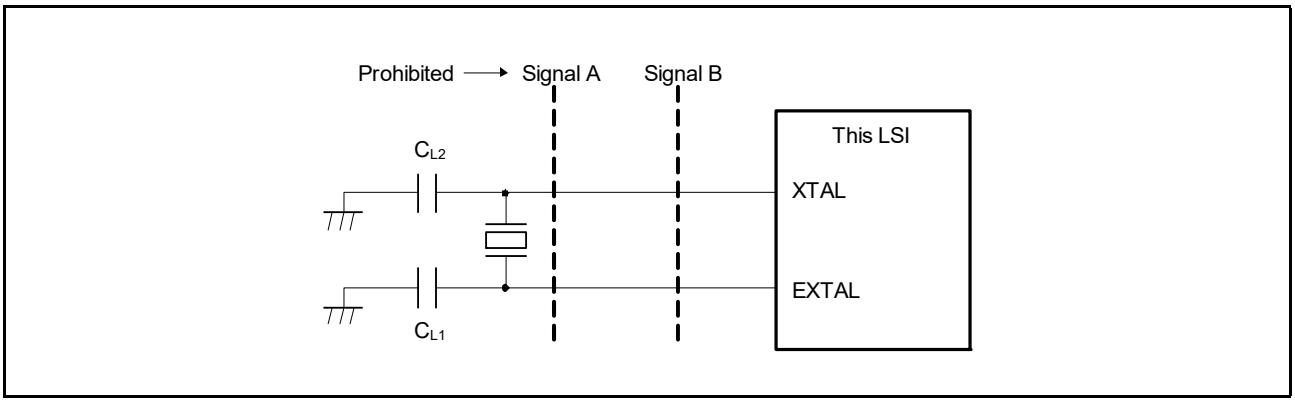


Figure 7.7 Notes on Board Design for Oscillation Circuit

8. Clock Monitor Circuit (CLMA)

A clock monitor circuit (CLMAn) (n = 2 to 0) detects a frequency error in PLL0 output, PLL1 output, or low-speed on-chip oscillator (LOCO) output, and then sends an error signal.

8.1 Overview

CLMAn (n = 2 to 0) can detect a frequency error in PLL0 output, PLL1 output, or on-chip oscillator (LOCO) output. During 16 cycles of the sampling clock, it counts the rising edges of the monitoring clock (frequency-dividing clock from PLL0, PLL1, or LOCO), and then compares the counter value with the compare register.

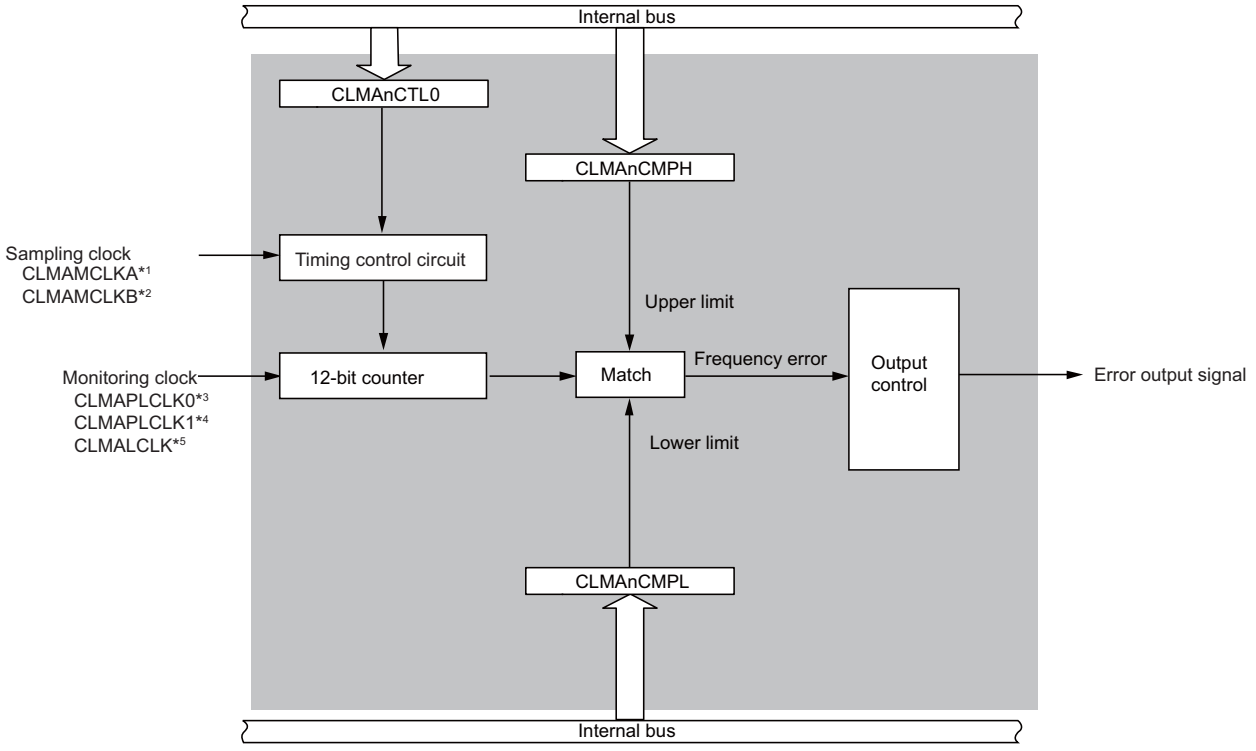
When CLMAn (n = 2 to 0) detects an error, it sends an error signal to the error control module (ECM). Besides, it switches the clock to supply the main clock instead of PLL0 or PLL1 output when it detects an error in PLL0 or PLL1 output.
For details on error signals, see section 42, Error Control Module (ECM).

Table 8.1 Specifications of CLMAn (n = 2 to 0)

Item	Specifications
Monitoring clock	The following monitoring clock frequency errors can be detected: • PLL0 output clock divided by 16 (CLMAPLCLK0, which is to be supplied to CLMA0): 75 MHz • PLL1 output clock divided by 16 (CLMAPLCLK1, which is to be supplied to CLMA1): 75 MHz / 56.25 MHz*1 • Low-speed on-chip oscillator (LOCO) output clock (CLMALCLK, which is to be supplied to CLMA2): 240 kHz
Sampling clock	The following clock frequency errors are monitored as the sampling clock: • Clock which equals to the main clock frequency divided by 2 (CLMAMCLKA, which is to be supplied to CLMA0): 12.5 MHz • Clock which equals to the main clock frequency divided by 2 (CLMAMCLKA, which is to be supplied to CLMA1): 12.5 MHz • Clock which equals to the main clock frequency divided by 256 (CLMAMCLKB, which is to be supplied to CLMA2): 97.66 kHz
Error signal output	When CLMAn detects a frequency error, it sends an error signal to the error control module (ECM). • CLMA0 oscillator-stopped detection error signal • CLMA1 oscillator-stopped detection error signal • CLMA2 oscillator-stopped detection error signal
Clock switching function when an error occurs	When an error is detected in PLL0 or PLL1 output, switches the clock to supply the main clock instead of PLL0 or PLL1 output.

Note 1. 56.25 MHz is selected when 10b is set for CPUCKSEL[1:0] of the PLL1CR register. When a value other than 10b is set, 75 MHz is selected. For details, see section 7, Clock Generation Circuit.

Figure 8.1 is a block diagram of CLMAn (n = 2 to 0).



Note 1. Main clock frequency divided by 2 to be supplied to CLMA0 and CLMA1
Note 2. Main clock frequency divided by 256 to be supplied to CLMA2
Note 3. PLL0 output clock divided by 16 to be supplied to CLMA0
Note 4. PLL1 output clock divided by 16 to be supplied to CLMA1
Note 5. Low-speed on-chip oscillator (LOCO) output clock to be supplied to CLMA2

Figure 8.1 Block Diagram of CLMAn (n = 2 to 0)

8.2 Register Descriptions

8.2.1 CLMAn Control Registers 0 (CLMAnCTL0) (n = 2 to 0)

The CLMAnCTL0 registers control operation of clock monitor circuit CLMAn.
Writing to these registers is protected by a specific command sequence. For details, see section 8.3.1, (1) Enabling operations.

Address(es): CLMA0CTL0: A009 0000h
CLMA1CTL0: A009 0020h
CLMA2CTL0: A009 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CLMAn CLME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CLMAnCLME	Clock Monitor Enable n	Enables or disables operation of clock monitor circuit CLMAn (n = 2 to 0). 0: Disables CLMAn operation. 1: Enables CLMAn operation.	R/W
b7 to b1	—	Reserved	These bits are always read as 0. The write value should be 0.	R/(W)

Note 1. Once the CLMAnCLME bit is set to 1, it cannot be cleared by any operation other than reset (except software reset 2).

8.2.2 CLMAn Compare Registers L (CLMAnCMPL) (n = 2 to 0)

The CLMAnCMPL registers set the lower limit for comparing frequency domains.
Values can be written to these registers when the CLMAnCLME bit is set to 0. When the CLMAnCLME bit is set to 1, writing to these registers has no effect.

Address(es): CLMA0CMPL: A009 0008h
CLMA1CMPL: A009 0028h
CLMA2CMPL: A009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CLMAnCMPL[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	CLMAnCMPL [11:0]	Clock Monitor Compare L	Specify the lower-limit threshold for the frequency domain.*1 • For details, see section 8.3.2, (2) Method of calculating threshold values, CLMAnCMPL.CLMAnCMPL[11:0] and CLMAnCMPH.CLMAnCMPH[11:0]. Recommended value: $f_{CLMATMON\ (min)} / f_{CLMATSMP\ (max)} \times 16 - 1$ $f_{CLMATMON}$: Monitoring clock frequency $f_{CLMATSMP}$: Sampling clock frequency • Minimum value: 0001h	R/W
b15 to b12	—	Reserved	These bits are always read as 0. The write value should be 0.	R/(W)

Note 1. To set the CLMAnCMPL registers, the following conditions must be met:
- 1 ≤ CLMAnCMPL
- CLMAnCMPL + 3 ≤ CLMAnCMPH

8.2.3 CLMAn Compare Registers H (CLMAnCMPH) (n = 2 to 0)

The CLMAnCMPH registers set the upper limit for comparing frequency domains.
Values can be written to the CLMAnCMPH registers when the CLMAnCLME bit is set to 0. When the CLMAnCLME bit is set to 1, writing to these registers has no effect.

Address(es): CLMA0CMPH: A009 000Ch
CLMA1CMPH: A009 002Ch
CLMA2CMPH: A009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CLMAnCMPH[11:0]											
Value after reset:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	CLMAnCMPH[11:0]	Clock Monitor Compare H	Specify the upper-limit threshold for the frequency domain*1. • For details, see section 8.3.2, (2) Method of calculating threshold values, CLMAnCMPL.CLMAnCMPL[11:0] and CLMAnCMPH.CLMAnCMPH[11:0]. Recommended value: $f_{CLMATMON\ (max)} / f_{CLMATSMP\ (min)} \times 16 + 1$ $f_{CLMATMON}$: Monitoring clock frequency $f_{CLMATSMP}$: Sampling clock frequency • Minimum value: CLMAnCMPL + 0003h	R/W
b15 to b12	—	Reserved	These bits are always read as 0. The write value should be 0.	R/(W)

Note 1. To set the CLMAnCMPH registers, the following conditions must be met:
- 1 ≤ CLMAnCMPL
- CLMAnCMPL + 3 ≤ CLMAnCMPH

8.2.4 CLMAn Command Registers (CLMAnPCMD) (n = 2 to 0)

The CLMAnPCMD registers control writing to the protected registers.
For details, see section 8.3.1, (1) Enabling operations.

Address(es): CLMA0PCMD: A009 0010h
CLMA1PCMD: A009 0030h
CLMA2PCMD: A009 0050h

	b7	b6	b5	b4	b3	b2	b1	b0
	CLMAnPR[7:0]							
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CLMAnPR[7:0]	CLMAn Protect Key Code	Write a specific command sequence.	W

8.2.5 CLMAn Protection Status Registers (CLMAnPS) (n = 2 to 0)

The CLMAnPS registers indicate whether writing to the protected register is performed correctly. If writing is not performed correctly, a protection error occurs, and the CLMAnPS.CLMAnPRERR bit is set to 1.
For details, see section 8.3.1, (1) Enabling operations.

Address(es): CLMA0PS: A009 0014h
CLMA1PS: A009 0034h
CLMA2PS: A009 0054h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CLMAn PRERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CLMAnPRERR	CLMAn Error	0: No protection error occurred. 1: A protection error occurred.	R
b7 to b1	—	Reserved	These bits are always read as 0.	R

8.3 Operation

8.3.1 CLMAn Operation

(1) Enabling operations

Setting the CLMAnCTL0.CLMAnCLME bit to 1 starts monitoring the monitoring clock (PLL0 output divided by 16, PLL1 output divided by 16, and LOCO output) by using clock monitor circuit CLMAn (n = 2 to 0) output. To write 1 in the CLMAnCTL0.CLMAnCLME bit, follow the following command sequence:

1. Write A5h to the CLMAnPCMD register.
2. Writing to CLMAnCTL0 is performed by the following sequence:
   - Write the target setting value (01h).
   - Write the reversed value of the target (FEh).
   - Write the target value (01h) again.
3. Read CLMAnCTL0.
   When the value of CLMAnCTL0 shows 01h, the operation of CLMAn is enabled.
   If it shows another value, check the value of CLMAn protection status register (CLMAnPS).

When CLMAnPS = 01h, the command sequence is not performed correctly. Execute the sequence again from step 1 to perform writing.

(2) Stopping operations

When a monitoring clock stops due to register operation, the corresponding clock monitor circuit (CLMAn) is disabled automatically. After that, when the monitoring clock starts oscillating again and stabilizes, the clock monitor circuit (CLMAn) resumes operation.

8.3.2 Detecting Error Clock Frequency

(1) Detection Method

1. During 16 cycles of the sampling clock, CLMAn counts the rising edge of the monitoring clock (PLL0 output divided by 16, PLL1 output divided by 16, and LOCO output), and compares the counter value with the set threshold (n = 2 to 0).
   - CLMAnCMPL.CLMAnCMPL[11:0] set the lower-limit threshold of the frequency domain.
   - CLMAnCMPH.CLMAnCMPH[11:0] set the upper-limit threshold of the frequency domain.
2. If the monitoring clock stops, or shows a value lower than the expected frequency, the counter value shows a value lower than the setting of CLMAnCMPL.CLMAnCMPL[11:0].
3. If the monitoring clock shows a value higher than the expected frequency, the counter value shows a value higher than the setting of CLMAnCMPH.CLMAnCMPH[11:0].

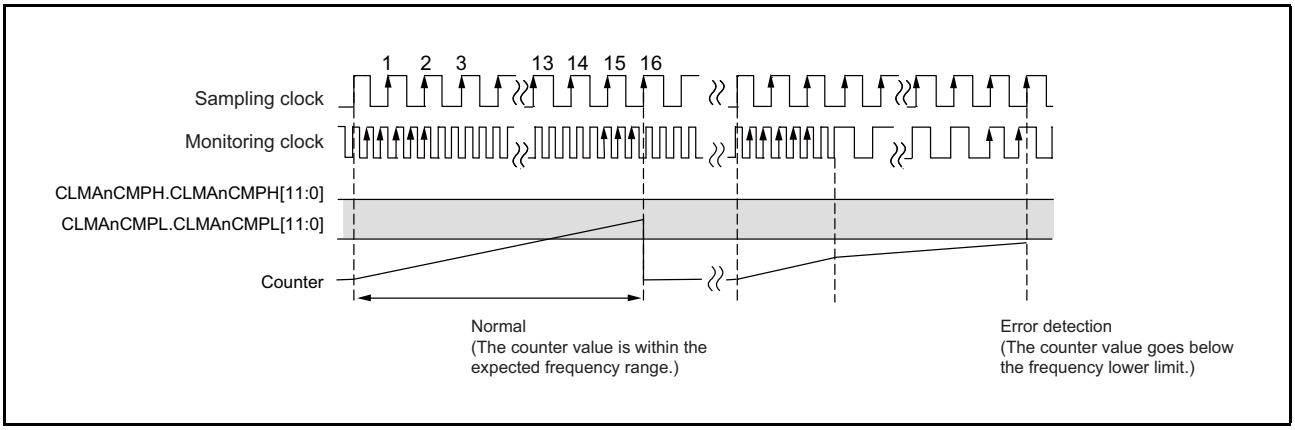


Figure 8.2 Example When the Monitoring Clock Shows a Value Lower Than the Expected Frequency

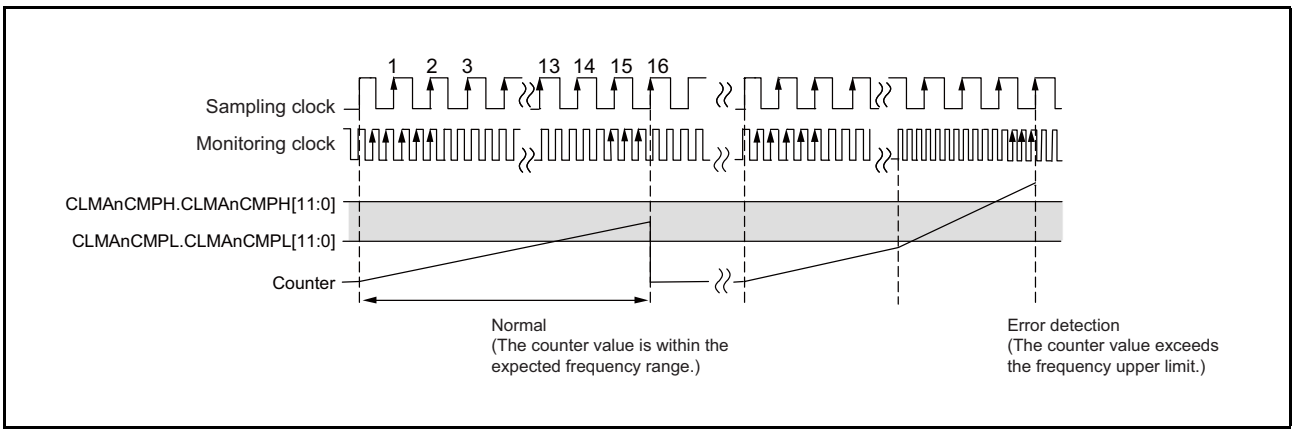


Figure 8.3 Example When the Monitoring Clock Shows a Value Higher Than the Expected Frequency

Note 1. No error is detected if the monitoring clock frequency changes within a sampling interval, and it stays within a valid counter value eventually. A monitoring clock error is detected after a sampling interval (16 cycles of the sampling clock).

(2) Method of calculating threshold values, CLMAnCMPL.CLMAnCMPL[11:0] and CLMAnCMPH.CLMAnCMPH[11:0]

For compare registers CLMAnCMPL and CLMAnCMPH, set the minimum and maximum values of the number of cycles (the number of rising edges) for the monitoring clock which is assumed to be normal within 16 cycles of the sampling clock (main clock frequency dividing clock).

$f_{CLMATSMP}$ indicates the sampling clock frequency, $f_{CLMATMON}$ indicates the monitoring clock frequency, and N indicates the number of cycles (rising edges) of the monitoring clock, which is expected within 16 cycles of the sampling clock.

$$\frac{16}{f_{CLMATSMP}} = \frac{N}{f_{CLMATMON}}$$

$$N = \frac{f_{CLMATMON}}{f_{CLMATSMP}} \times 16$$

Considering allowable frequency deviations for the monitoring clock and the sampling clock, use the following formula to calculate the threshold:

Lower-limit threshold $= N_{min}$

$$= \frac{f_{CLMATMON(min)}}{f_{CLMATSMP(max)}} \times 16 - 1$$

Upper-limit threshold $= N_{max}$

$$= \frac{f_{CLMATMON(max)}}{f_{CLMATSMP(min)}} \times 16 + 1$$

Note: Set the threshold within the following range:
CLMAnCMPL ≥ 0001_H
CLMAnCMPH ≥ CLMAnCMPL + 0003_H

Example: For CLMA0

For example, when the sampling clock equals to the main clock frequency divided by 2, $f_{CLMATSMP}$ = 12.5 MHz (±5%), or the monitoring clock equals to PLL0 output divided by 16, $f_{CLMATMON}$ = 75 MHz (±5%), the recommended threshold is calculated as follows:

$$N_{min} = f_{CLMATMON}(min) / f_{CLMATSMP}(max) = 71.25 / 13.125 \times 16 - 1$$
$$= 85.86$$

CLMAnCMPL = 86 = 0056h

$$N_{max} = f_{CLMATMON}(max) / f_{CLMATSMP}(min) = 78.75 / 11.875 \times 16 + 1$$
$$= 107.11$$

CLMAnCMPH = 107 = 006Bh

8.3.3 Detecting Error Clock Frequency

When the monitoring clock frequency (PLL0 output divided by 16, PLL1 output divided by 16, and LOCO output) is higher than the upper-limit threshold, or lower than the lower-limit threshold, any of the following signals is sent to the error control module (ECM):

- CLMA0 oscillator-stopped detection error signal
- CLMA1 oscillator-stopped detection error signal
- CLMA2 oscillator-stopped detection error signal

For details on error signals, see section 42, Error Control Module (ECM).

8.4 Notes on Using CLMAn

Do not use a clock for which CLMAn detected an error. If you use the clock, operation of the device is not guaranteed.

9. Low-Power Consumption Function

9.1 Overview

This LSI has several functions for reducing power consumption, including the Cortex-R4 standby function , Cortex-M3 (for products incorporating an R-IN engine) sleep function, and the module stop function that stops functions independently for each peripheral module. Power consumption by using clock control such as CLKOUT25Mn output control (n = 2 to 0) and CKIO output control is also possible.
Table 9.1 lists the specifications of low-power consumption functions. Table 9.2 describes how to stop each peripheral module and exit the stop state.

Table 9.1 Specifications of Low-Power Consumption Function

Item	Specifications
Low-power consumption mode	- Standby mode (Cortex-R4) - Sleep mode (Cortex-M3 (for products incorporating an R-IN engine))
Module-stop function	Functions can be stopped independently for each peripheral module.
CLKOUT25Mn (n = 2 to 0) output control function	CLKOUT25Mn (n = 2 to 0) clock output or stop (held at the low level) can be selected.
CKIO output control function	CKIO clock output or stop (held at the low level) can be selected.

Table 9.2 Stopping Peripheral Modules and Exiting Module-Stop State (1 / 2)

Module	How to Stop Operation and Exit the Stop State	Initial State*1
Cortex-R4	Stop condition: Execution of the Wait For Interrupt (WFI) instruction Condition for release from the stop-state: Interrupt	Operating
Cortex-M3 (for products incorporating an R-IN engine)	Stop condition: Execution of the Wait For Interrupt (WFI) instruction Condition for release from the stop-state: Interrupt	Operating
Internal bus	Always operating	Operating
Tightly Coupled Memory (ATCM or BTCM)	Operate only during access	Operate only during access
On-chip extended SRAM (with ECC)	Operate only during access	Operate only during access
Interrupt controller	Operation is always enabled.	Operating
Error control module (ECM)	Operation is always enabled.	Operating
Port output enable 3 (POE3)	Operation is always enabled.	Operating
Multifunction timer pulse unit 3 (MTU3a)	Set the control register to enter or exit the module-stop state.	Stop
General PWM timer (GPTa)	Set the control register to enter or exit the module-stop state.	Stop
16-bit timer pulse unit (TPUa)	Set the control register to enter or exit the module-stop state.	Stop
Programmable pulse generator (PPG)	Set the control register to enter or exit the module-stop state.	Stop
Compare match timer (CMT)	Set the control register to enter or exit the module-stop state.	Stop
Compare match timer W (CMTW)	Set the control register to enter or exit the module-stop state.	Stop
Ethernet switch	Set the control register to exit the module-stop state.*2	Stop
EtherCAT slave controller (EtherCAT) (optional)	Set the control register to exit the module-stop state.*2	Stop
Ethernet RMII	Set the control register to exit the module-stop state.*2	Stop
Ethernet MDIO	Set the control register to exit the module-stop state.*2	Stop

Table 9.2 Stopping Peripheral Modules and Exiting Module-Stop State (2 / 2)

Module	How to Stop Operation and Exit the Stop State	Initial State*1
Ethernet MAC/HW-RTOS (for products incorporating an R-IN engine)	Set the control register to exit the module-stop state*2.	Stop
Serial peripheral interface (RSPIa)	Set the control register to enter or exit the module-stop state.	Stop
Serial communication interface with FIFO (SCIFA)	Set the control register to enter or exit the module-stop state.	Stop
I2C bus interface (RIICa)	Set the control register to enter or exit the module-stop state.	Stop
CAN module (RSCAN)	Set the control register to enter or exit the module-stop state.	Stop
Clock monitor circuit (CLMA)	Set the control register to enter or exit the module-stop state.	Stop
CRC operation part (CRC)	Set the control register to enter or exit the module-stop state.	Stop
Data operation circuit (DOC)	Set the control register to enter or exit the module-stop state.	Stop
SPI multi I/O bus controller (SPIBSC)	Set the control register to enter or exit the module-stop state.	Stop*3
Bus state controller (BSC)	Set the control register to enter or exit the module-stop state.	Operating*3
Event link controller (ELC)	Set the control register to enter or exit the module-stop state.	Stop
12-bit A/D converter (S12ADCa)	Set the control register to enter or exit the module-stop state.	Stop
Temperature sensor	Set the control register to enter or exit the module-stop state.	Stop
Delta-sigma interface (DSMIF)	Set the control register to enter or exit the module-stop state.	Stop
USB	Set the control register to stop the module or exit the module stop state.	Stop
Serial sound interface (SSI)	Set the control register to enter or exit the module-stop state.	Stop
Direct memory access controller (DMAC)	Set the control register to stop the module or exit the module-stop state.	Operating
I/O port	Operation is always enabled.	Operating
Coresight	Set the control register to stop the module or exit the module-stop state.	Operating
Watchdog timer (WDTA (for Cortex-R4))	Operation is always enabled.	Operating
Watchdog timer (WDTA (for Cortex-M3) (for products incorporating an R-IN engine))	Operation is always enabled.	Operating
Independent watchdog timer (IWDTa)	Operation is always enabled.	Operating
Encode interface	Set the control register to enter or exit the module-stop state.	Stop

Note 1. Each module is returned to the initial state by means of the RES# pin reset, error control module (ECM) reset, or software reset. In addition to above, Cortex-M3 and WDT (for Cortex-M3) are set to the initial state when software reset 2 is generated.

Note 2. This module cannot be stopped by specifying the control register. For details, see section 9.2.2, Module Stop Control Register B (MSTPCRB).

Note 3. The state of the SPI multi I/O bus controller (SPIBSC) and bus state controller (BSC) after boot processing varies depending on the settings of the parameters for the loader. For details, see section 3, Operating Modes.

9.2 Register Descriptions

The registers are applicable to the register write protection function. For writing these registers, clear write protection for the target register by setting b1 of the Protect Register (PRCR). For details, see section 11, Register Write Protection Function.

9.2.1 Module Stop Control Register A (MSTPCRA)

The MSTPCRA register controls the module-stop state.
For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 0300h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTP CRA11	—	MSTP CRA9	MSTP CRA8	MSTP CRA7	MSTP CRA6	MSTP CRA5	MSTP CRA4	MSTP CRA3	MSTP CRA2	MSTP CRA1	MSTP CRA0
Value after reset:	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPCRA0	CMTW Unit 1 Module Stop	Target module: CMTW unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made.	R/W
b1	MSTPCRA1	CMTW Unit 0 Module Stop	Target module: CMTW unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b2	MSTPCRA2	CMT Unit 2 Module Stop	Target module: CMT unit 2 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b3	MSTPCRA3	CMT Unit 1 Module Stop	Target module: CMT unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b4	MSTPCRA4	CMT Unit 0 Module Stop	Target module: CMT unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b5	MSTPCRA5	PPG Unit 1 Module Stop	Target module: PPG unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made.	R/W
b6	MSTPCRA6	PPG Unit 0 Module Stop	Target module: PPG unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b7	MSTPCRA7	TPUa Unit 1 Module Stop	Target module: TPUa unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made.	R/W
b8	MSTPCRA8	TPUa Unit 0 Module Stop	Target module: TPUa unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b9	MSTPCRA9	GPTa Module Stop	Target module: GPTa 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	MSTPCRA11	MTU3a Module Stop	Target module: MTU3a 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

9.2.2 Module Stop Control Register B (MSTPCRB)

The MSTPCRB register controls the module-stop state.

For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 0304h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	MSTPCRB19	MSTPCRB18*1	MSTPCRB17	MSTPCRB16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPCRB15*1	MSTPCRB14	MSTPCRB13	MSTPCRB12	MSTPCRB11	MSTPCRB10	MSTPCRB9	MSTPCRB8	MSTPCRB7	MSTPCRB6	MSTPCRB5	—	MSTPCRB3	MSTPCRB2	MSTPCRB1	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Note 1. These bits are only for products incorporating an EtherCAT (optional).

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	MSTPCRB1	RSCAN Module Stop	Target module: RSCAN 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b2	MSTPCRB2	RIICa Channel 1 Module Stop	Target module: RIICa channel 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b3	MSTPCRB3	RIICa Channel 0 Module Stop	Target module: RIICa channel 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	MSTPCRB5	SCIFA Channel 4 Module Stop	Target module: SCIFA channel 4 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b6	MSTPCRB6	SCIFA Channel 3 Module Stop	Target module: SCIFA channel 3 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b7	MSTPCRB7	SCIFA Channel 2 Module Stop	Target module: SCIFA channel 2 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b8	MSTPCRB8	SCIFA Channel 1 Module Stop	Target module: SCIFA channel 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b9	MSTPCRB9	SCIFA Channel 0 Module Stop	Target module: SCIFA channel 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b10	MSTPCRB10	RSPIa Channel 3 Module Stop	Target module: RSPIa channel 3 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b11	MSTPCRB11	RSPIa Channel 2 Module Stop	Target module: RSPIa channel 2 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b12	MSTPCRB12	RSPIa Channel 1 Module Stop	Target module: RSPIa channel 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b13	MSTPCRB13	RSPIa Channel 0 Module Stop	Target module: RSPIa channel 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W

Bit	Symbol	Bit Name	Description	R/W
b14*1	MSTPCRB14	Ethernet Switch Module Stop	Target module: Ethernet Switch 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b15*1 *2	MSTPCRB15	EtherCAT Module Stop (optional)	Target module: EtherCAT 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b16*1	MSTPCRB16	Ethernet MDIO Module Stop	Target module: Ethernet MDIO 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b17*1	MSTPCRB17	Ethernet RMII Module Stop	Target module: Ethernet RMII 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b18*1*3	MSTPCRB18	Ethernet MAC/HW-RTOS Module Stop	Target module: Ethernet MAC, HW-RTOS 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b19*1	MSTPCRB19	CLKOUT25Mn (Ethernet PHY Clock Output) Stop (n = 2 to 0)	0: Clock output from the CLKOUT25Mn pin is permitted 1: Clock output from the CLKOUT25Mn pin is stopped (held at low level)	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Ethernet-related functions are stopped in the initial state. To use the functions, specify the MSTPCRB.MSTPCRB14 to MSTPCRB19 bits for release from the module-stop state. Note, however, that after release from the module-stop state, the module stop state cannot be set again. Operation is not guaranteed after release from the module-stop state is initiated the second time. After the modules are returned to the initial state (stop state) by a reset, they can be release from the module-stop state again.

Note 2. This bit is reserved for products other than those incorporating an EtherCAT (optional). It is read as 1. The write value should always be 1.

Note 3. Ethernet MAC/HW-RTOS is only the target of module stopping in products that incorporate an R-IN Engine. For other products, the MAC is the target of module stopping.

9.2.3 Module Stop Control Register C (MSTPCRC)

The MSTPCRC register controls the module-stop state.

For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 0308h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTP CRC14	MSTP CRC13	MSTP CRC12	MSTP CRC11	MSTP CRC10	MSTP CRC9	MSTP CRC8	MSTP CRC7	MSTP CRC6	MSTP CRC5	MSTP CRC4	MSTP CRC3	MSTP CRC2	MSTP CRC1	—
Value after reset:	0	1	1	1	1	1	1*1	1	0*1	1	1	1	1	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	MSTPCRC1	USB Module Stop	Target module: USB 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b2	MSTPCRC2	Delta-sigma interface Module Stop	Target module: Delta-sigma interface 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b3	MSTPCRC3	Temperature Sensor Module Stop	Target module: Temperature sensor 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b4	MSTPCRC4	ADC Unit 1 Module Stop	Target module: ADC unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b5	MSTPCRC5	ADC Unit 0 Module Stop	Target module: ADC unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b6	MSTPCRC6	ELC Module Stop	Target module: ELC 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b7	MSTPCRC7	BSC Module Stop	Target module: BSC 0: Release from the module-stop state 1: Transition to the module-stop state is made.	R/W
b8	MSTPCRC8	CKIO Stop	0: Clock output from the CKIO pin is permitted. 1: Clock output from the CKIO pin is stopped (retained at low level).	R/W
b9	MSTPCRC9	SPIBSC Module Stop	Target module: SPIBSC 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b10	MSTPCRC10	DOC Module Stop	Target module: DOC 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b11	MSTPCRC11	CRC Module Stop	Target module: CRC 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b12	MSTPCRC12	CLMA Unit 2 Module Stop	Target module: CLMA unit 2 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b13	MSTPCRC13	CLMA Unit 1 Module Stop	Target module: CLMA unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W

Bit	Symbol	Bit Name	Description	R/W
b14	MSTPCRC14	CLMA Unit 0 Module Stop	Target module: CLMA unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The state of the SPI multi I/O bus controller (SPIBSC) and bus state controller (BSC) after boot processing varies depending on the settings of the parameters for the loader. For details, see section 3, Operating Modes.

9.2.4 Module Stop Control Register D (MSTPCRD)

The MSTPCRD register controls the module stop state.

For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 030Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP CRD2	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPCRD2	SSI Module Stop	Target module: SSI 0: Release from the module-stop state 1: Transition to the module stop state is made	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

9.2.5 Module Stop Control Register E (MSTPCRE)

The MSTPCRE register controls the module-stop state.

For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 0310h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MSTP CRE5	MSTP CRE4	—	—	—	MSTP CRE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPCRE0*1	Encode interface Module Stop	Target module: Encode interface 0: Release from the module-stop state 1: Transition to the module stop state is made	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MSTPCRE4	DMAC Unit 1 Module Stop	Target module: DMAC unit 1 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b5	MSTPCRE5	DMAC Unit 0 Module Stop	Target module: DMAC unit 0 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Explicit software-driven release from the module-stop state by the setting of this bit is not required, because the encoder interface configuration library handles processing for release.

9.2.6 Module Stop Control Register F (MSTPCRF)

The MSTPCRF register controls the module-stop state.

For release from the module-stop state, see section 9.3.1, Module-Stop Function.

Address(es): A00B 0314h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP CRF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSTPCRF0	Coresight Module Stop	Target module: Coresight 0: Release from the module-stop state 1: Transition to the module-stop state is made	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

9.3 Operation

9.3.1 Module-Stop Function

The module-stop function can stop operation of each module of on-chip peripheral functions.
When the MSTPmi bit (m = A to F, i = 31 to 0) in the MSTPCRA to MSTPCRF registers is set to 1, the specified module stops operating and enters the module-stop state.
Clearing the MSTPmi bit (m = A to F, i = 31 to 0) to 0 leads to release from the module-stop state.
Follow the procedure given below when releasing any of the peripheral modules listed in Table 9.3 from the module-stop state. This procedure is not required for peripheral modules not listed in Table 9.3. However, release from the module-stop state should be in accord with the procedure for initialization described in the section for the given peripheral module.

[Procedures]

(1) Clear the corresponding bit in the relevant module stop control register (MSTPCRm; m = A to E) then immediately dummy-read the MSTPCRm register once.
(2) Dummy-read any register of the peripheral module which is being released from the module-stop state. After that, all registers of that peripheral module will be accessible.

Remarks: The MPU having set the access control attribute for the peripheral I/O register region to ‘Strongly-ordered’ or ‘Device’ is a prerequisite for the procedure.

<Example code>

```
volatile unsigned long dummy;                 //   Declared volatile to prevent optimization being applied

   SYSTEM.MSTPCRA.BIT.MSTPCRA0 = 0;           //   Setting to release CMTW unit 1 from the module-stop state
   dummy = SYSTEM.MSTPCRA.BIT.MSTPCRA0;       //   Step 1: Dummy-read the MSTPCRm register.

   dummy = CMTW1.CMWIOR.WORD;                 //   Step 2: Dummy-read any register of CMTW unit 1.
   CMTW1.CMWIOR.WORD = 0x81;                  //   The first setting for CMTW unit 1 (value is an example)
```

For details about the initial state after a release from the reset state, see Table 9.2, Stopping Peripheral Modules and Exiting Module-Stop State.

Note: Directly after a module is set to the module-stop state, writing might still be possible to the control register of that module.

Table 9.3 Peripheral Functions Requiring the above Procedure for Release from the Module-Stop State (1 / 2)

Peripheral Functions	Corresponding Module-Stop Control Register
CMTW unit 1	MSTPCRA register, MSTPCRA0 bit
CMTW unit 0	MSTPCRA register, MSTPCRA1 bit
CMT unit 2	MSTPCRA register, MSTPCRA2 bit
CMT unit 1	MSTPCRA register, MSTPCRA3 bit
CMT unit 0	MSTPCRA register, MSTPCRA4 bit
PPG unit 1	MSTPCRA register, MSTPCRA5 bit
PPG unit 0	MSTPCRA register, MSTPCRA6 bit
TPUa unit 1	MSTPCRA register, MSTPCRA7 bit
TPUa unit 0	MSTPCRA register, MSTPCRA8 bit
GPTa	MSTPCRA register, MSTPCRA9 bit

Table 9.3 Peripheral Functions Requiring the above Procedure for Release from the Module-Stop State (2 / 2)

Peripheral Functions	Corresponding Module-Stop Control Register
MTU3a	MSTPCRA register, MSTPCRA11 bit
RSCAN	MSTPCRB register, MSTPCRB1 bit
RIICa channel 1	MSTPCRB register, MSTPCRB2 bit
RIICa channel 0	MSTPCRB register, MSTPCRB3 bit
SCIFA channel 4	MSTPCRB register, MSTPCRB5 bit
SCIFA channel 3	MSTPCRB register, MSTPCRB6 bit
SCIFA channel 2	MSTPCRB register, MSTPCRB7 bit
SCIFA channel 1	MSTPCRB register, MSTPCRB8 bit
SCIFA channel 0	MSTPCRB register, MSTPCRB9 bit
RSPIa channel 3	MSTPCRB register, MSTPCRB10 bit
RSPIa channel 2	MSTPCRB register, MSTPCRB11 bit
RSPIa channel 1	MSTPCRB register, MSTPCRB12 bit
RSPIa channel 0	MSTPCRB register, MSTPCRB13 bit
$\Delta\sum$ interface	MSTPCRC register, MSTPCRC2 bit
Temperature sensor	MSTPCRC register, MSTPCRC3 bit
ADC unit 1	MSTPCRC register, MSTPCRC4 bit
ADC unit 0	MSTPCRC register, MSTPCRC5 bit
ELC	MSTPCRC register, MSTPCRC6 bit
BSC	MSTPCRC register, MSTPCRC7 bit
SPIBSC	MSTPCRC register, MSTPCRC9 bit
DOC	MSTPCRC register, MSTPCRC10 bit
CRC	MSTPCRC register, MSTPCRC11 bit
CLMA unit 2	MSTPCRC register, MSTPCRC12 bit
CLMA unit 1	MSTPCRC register, MSTPCRC13 bit
CLMA unit 0	MSTPCRC register, MSTPCRC14 bit
SSI	MSTPCRD register, MSTPCRD2 bit
Encoder interface	MSTPCRE register, MSTPCRE0 bit
DMAC unit 1	MSTPCRE register, MSTPCRE4 bit
DMAC unit 0	MSTPCRE register, MSTPCRE5 bit

9.3.2 Cortex-R4 Standby Mode and Cortex-M3 (for products incorporating an R-IN engine) Sleep Mode

9.3.2.1 Transition to Cortex-R4 Standby Mode and Cortex-M3 (for products incorporating an R-IN engine) Sleep Mode

Cortex-R4 enters standby mode and Cortex-M3 enters sleep mode by execution of a WFI instruction. In standby mode, Cortex-R4 and Cortex-M3 stop operating, thus reducing power consumption. For details, see the technical reference manual provided by Arm.

9.3.2.2 Release from Cortex-R4 Standby Mode and Cortex-M3 (for products incorporating an R-IN engine) Sleep Mode

Release from Cortex-R4 standby mode and Cortex-M3 sleep mode is initiated by any interrupt, the RES# pin reset, an ECM reset, or a software reset. Release from Cortex-M3 sleep mode is also initiated by software reset 2.

- Release triggered by an interrupt signal
  Generation of an interrupt in a CPU triggers release from standby mode or sleep mode of the CPU and the interrupt exception handling starts. Release is triggered by a non-maskable interrupt or a maskable interrupt that meets the following conditions:

  (1) The interrupt request is permitted by using the interrupt enable register.
  (2) Nothing has been assigned to DMAC by using the DMAC source selection register.

- Release by a reset
  After the RES# pin reset, ECM reset, or software reset is cleared, Cortex-R4 starts the reset exception handling. Even after the RES# pin reset, ECM reset, or software reset is cleared, Cortex-R4 is still in the reset state. To clear the reset, Cortex-R4 starts the reset exception handling after accessing the register and clearing software reset 2. For details about resets, see section 6, Reset.

9.4 Usage Notes

9.4.1 I/O Port State

To reduce I/O power consumption, pin processing based on I/O control is required. For details, see section 17, I/O Ports.

9.4.2 Module-Stop State of DMAC

Do not set a module-stop state while DMAC is operating. Make sure that the DMAC is inactive before you attempt to set the module-stop state.
For details, see section 15, DMA Controller (DMACAa).

9.4.3 On-Chip Peripheral Module Interrupts in Module-Stop State

Peripheral modules cannot interrupt in a module-stop state. Therefore, if the module-stop state is set during interrupt processing of the module or during DMA transfer by the DMAC, a CPU interrupt source or a DMAC or DTC startup source cannot be cleared. For this reason, disable the relevant interrupts before setting the module-stop state.

9.4.4 USB Low Power Consumption

For details about how to clear the USB module-stop state and how to enter the USB in low-power consumption mode, see section 31, USB2.0HS Host Module (USBh) and section 32, USB 2.0 HS Function Module (USBf).

9.4.5 Low Power Consumption for Ethernet-Related Functions

Ethernet-related functions are stopped in the initial state. To use the functions, specify the MSTPCRB.MSTPCRB14 to MSTPCRB19 bits for release from the module-stop state. Note, however, that after release from the module-stop state, the module stop state cannot be set again. Operation is not guaranteed after release from the module-stop state is initiated the second time. After the modules are returned to the initial state (stop state) by a reset, they can be released from the module-stop state again.

9.4.6 Write Protection Function

The module stop control registers (MSTPCRA to MSTPCRF) can be write-protected. To write to the MSTPCRA to MSTPCRF registers, specify bit 1 of the Protect Register (PRCR) to unlock the write protection. For details, see section 11, Register Write Protection Function.

10. Debugging Interface

This LSI has an internal debugging interface, which adopts an architecture in which Cortex-R4 and Cortex-M3 (for products incorporating an R-IN engine) are integrated by CoreSight. This LSI supports debugging functions, such as downloading, running, and breaking a program, and trace function, which outputs execution history of programs.

10.1 Overview

This LSI supports JTAG and SWD interfaces as interfaces for debugging, and trace port and SWV interfaces as interfaces for trace.

This LSI has TAP controllers for boundary scan and for CoreSight debugging, which can be selected by the input level of the BSCANP pin. To use debugging function, set the input level of the BSCANP pin to Low.

For details on boundary scan, see section 40, Boundary Scan.

Table 10.1 lists the specifications of CoreSight, and Figure 10.1 and Figure 10.2 are block diagrams of CoreSight. Moreover, Table 10.5 to Table 10.8 indicate the CoreSight address maps. For details on CoreSight, see Arm's technical reference manual.

Table 10.1 CoreSight Specifications

Item	Specifications
Debugging function	• JTAG interface • SWD (Serial Wire Debug) interface
Trace function	• Trace port interface 8 bits × 75 Mbps (37.5 MHz, DDR) trace data pin output Embedded Trace Buffer (ETB) 4 Kbytes • SWV (Serial Wire Viewer) interface

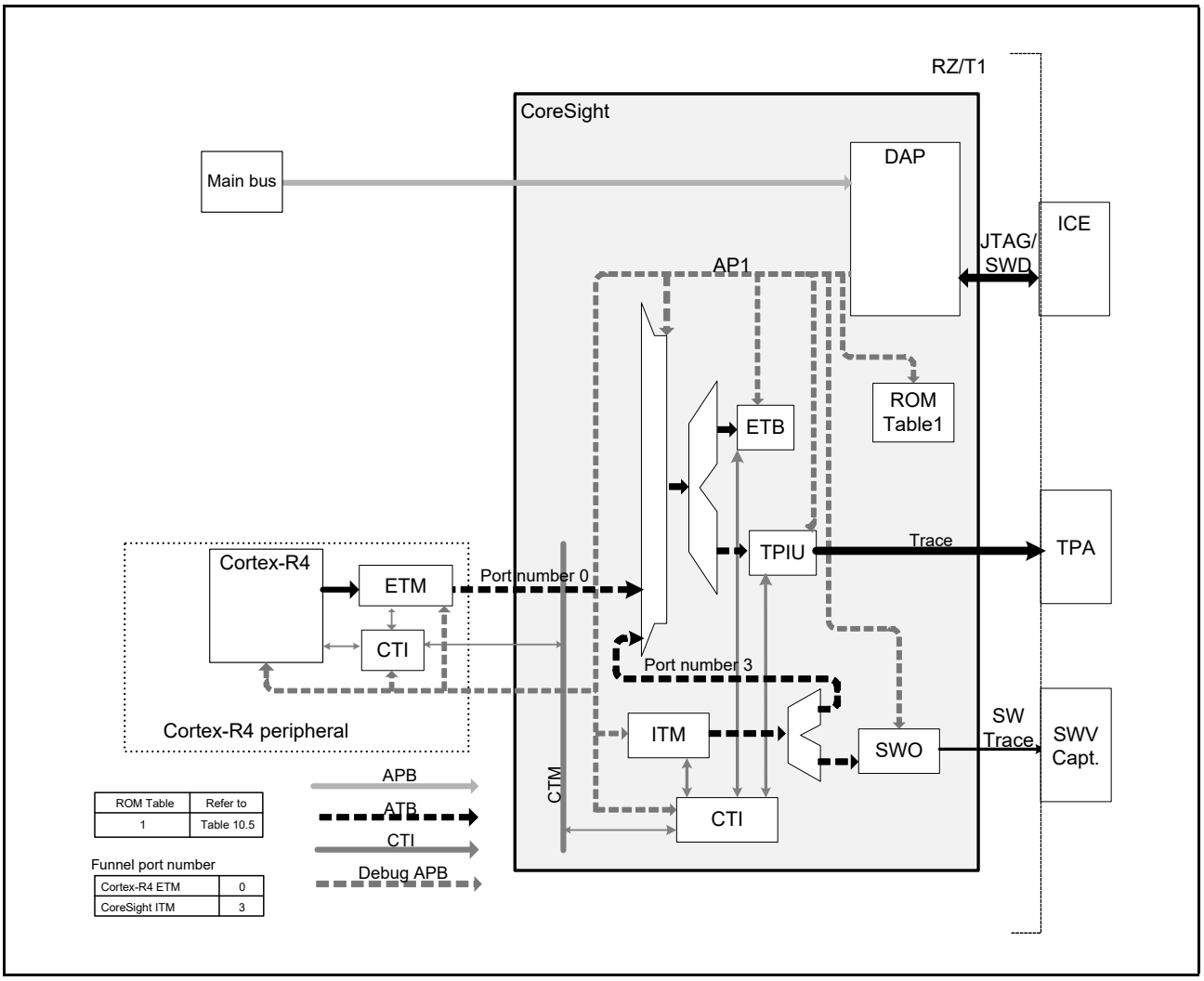


Figure 10.1 Block Diagram of CoreSight

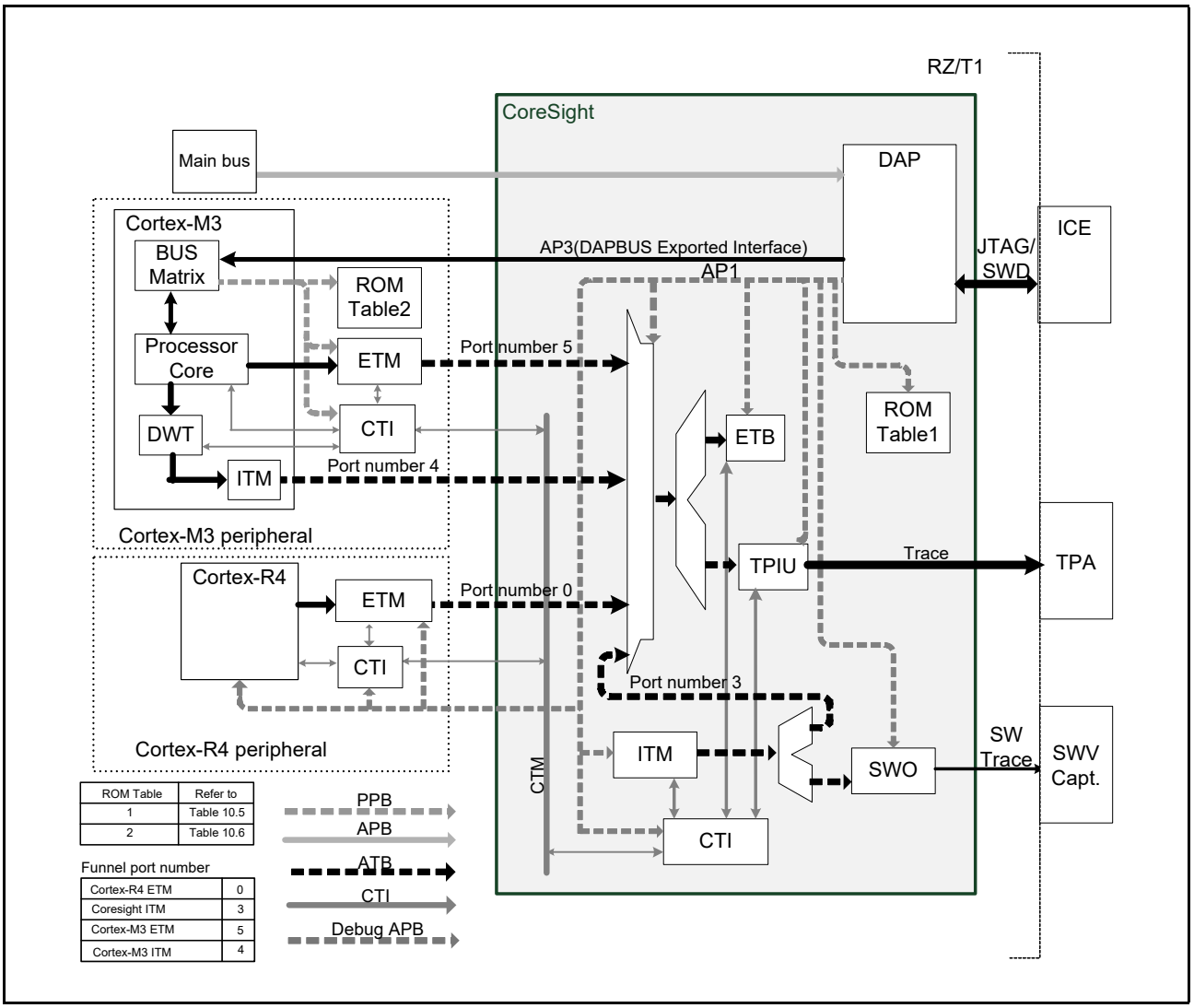


Figure 10.2 Block Diagram of CoreSight (for products incorporating an R-IN engine)

Table 10.2 CTI Trigger Input and Output (CoreSight)

CTI Input Pin	Source Device	Signal	CTI Output Pin	Destination Device	Signal
CTITRIGIN[0]	—	—	CTITRIGOUT[0]	ETB	FLUSHIN
CTITRIGIN[1]	—	—	CTITRIGOUT[1]	ETB	TRIGIN
CTITRIGIN[2]	ETB	FULL	CTITRIGOUT[2]	TPIU	FLUSHIN
CTITRIGIN[3]	ETB	ACQCOMP	CTITRIGOUT[3]	TPIU	TRIGIN
CTITRIGIN[4]	ITM	TRIGOUT	CTITRIGOUT[4]	—	—
CTITRIGIN[5]	—	—	CTITRIGOUT[5]	—	—
CTITRIGIN[6]	—	—	CTITRIGOUT[6]	—	—
CTITRIGIN[7]	—	—	CTITRIGOUT[7]	—	—

Table 10.3 CTI Trigger Input and Output (Cortex-R4)

CTI Input Pin	Source Device	Signal	CTI Output Pin	Destination Device	Signal
CTITRIGIN[0]	Cortex-R4	DBGTRIGGER	CTITRIGOUT[0]	Cortex-R4	EDBGRQ
CTITRIGIN[1]	Cortex-R4	nPMUIRQ	CTITRIGOUT[1]	ETM-R4	EXTIN[0]
CTITRIGIN[2]	ETM-R4	EXOUT[0]	CTITRIGOUT[2]	ETM-R4	EXTIN[1]
CTITRIGIN[3]	ETM-R4	EXOUT[1]	CTITRIGOUT[3]	VIC	TRIGINT
CTITRIGIN[4]	Cortex-R4	COMMRX	CTITRIGOUT[4]	—	—
CTITRIGIN[5]	Cortex-R4	COMMTX	CTITRIGOUT[5]	—	—
CTITRIGIN[6]	ETM-R4	TRIGGER	CTITRIGOUT[6]	—	—
CTITRIGIN[7]	—	—	CTITRIGOUT[7]	Cortex-R4	DBGRESTART

Table 10.4 CTI Trigger Input and Output (Cortex-M3) (only for products incorporating an R-IN engine)

CTI Input Pin	Source device	Signal	CTI Output Pin	Destination device	Signal
CTITRIGIN[0]	Core	HALTED	CTITRIGOUT[0]	Core	EDBGRQ
CTITRIGIN[1]	—	—	CTITRIGOUT[1]	—	—
CTITRIGIN[2]	—	—	CTITRIGOUT[2]	NVIC	INTISR[x]
CTITRIGIN[3]	—	—	CTITRIGOUT[3]	NVIC	INTISR[y]
CTITRIGIN[4]	DWT	ETMTRIGGER[0]	CTITRIGOUT[4]	ETM-M3	EXTIN[0]
CTITRIGIN[5]	DWT	ETMTRIGGER[1]	CTITRIGOUT[5]	ETM-M3	EXTIN[1]
CTITRIGIN[6]	DWT	ETMTRIGGER[2]	CTITRIGOUT[6]	—	—
CTITRIGIN[7]	ETM-M3	ETMTRIGOUT	CTITRIGOUT[7]	Core	DBGRESTART

Table 10.5 CoreSight Address Map (Debug-APB)

Cortex-R4 CPU View	Cortex-M3 CPU View (only for products incorporating an R-IN engine)	Debugger View*1 (AP = 1)	Module
H'E8000000 to H'E8000FFF	H'E8000000 to H'E8000FFF	H'00000000 to H'00000FFF	CoreSight / DAP ROM
H'E8001000 to H'E8001FFF	H'E8001000 to H'E8001FFF	H'00001000 to H'00001FFF	CoreSight / ETB
H'E8002000 to H'E8002FFF	H'E8002000 to H'E8002FFF	H'00002000 to H'00002FFF	CoreSight / CTI
H'E8003000 to H'E8003FFF	H'E8003000 to H'E8003FFF	H'00003000 to H'00003FFF	CoreSight / TPIU
H'E8004000 to H'E8004FFF	H'E8004000 to H'E8004FFF	H'00004000 to H'00004FFF	CoreSight / Funnel
H'E8005000 to H'E8005FFF	H'E8005000 to H'E8005FFF	H'00005000 to H'00005FFF	CoreSight / ITM
H'E8006000 to H'E8006FFF	H'E8006000 to H'E8006FFF	H'00006000 to H'00006FFF	CoreSight / SWO
H'E8007000 to H'E8007FFF	H'E8007000 to H'E8007FFF	H'00007000 to H'00007FFF	—
H'E8008000 to H'E8008FFF	H'E8008000 to H'E8008FFF	H'00008000 to H'00008FFF	Cortex-R4 / CPU
H'E8009000 to H'E8009FFF	H'E8009000 to H'E8009FFF	H'00009000 to H'00009FFF	Cortex-R4 / CTI
H'E800A000 to H'E800AFFF	H'E800A000 to H'E800AFFF	H'0000A000 to H'0000AFFF	Cortex-R4 / ETM-R4
H'E800B000 to H'E800BFFF	H'E800B000 to H'E800BFFF	H'0000B000 to H'0000BFFF	—
H'E800C000 to H'E800CFFF	H'E800C000 to H'E800CFFF	H'0000C000 to H'0000CFFF	—
H'E800D000 to H'E800DFFF	H'E800D000 to H'E800DFFF	H'0000D000 to H'0000DFFF	—
H'E800E000 to H'E800EFFF	H'E800E000 to H'E800EFFF	H'0000E000 to H'0000EFFF	—
H'E800F000 to H'E800FFFF	H'E800F000 to H'E800FFFF	H'0000F000 to H'0000FFFF	—

Note 1. When A31 (the most significant bit of the address) is set to 1, access without releasing the access lock becomes possible.

Table 10.6 CoreSight Address Map (DAPBUS Exported I/F) (only for products incorporating an R-IN engine)

Cortex-R4 CPU View	Cortex-M3 CPU View	Debugger View (AP = 3)	Module
Not accessible	H'E0000000 to H'E0000FFF	H'E0000000 to H'E0000FFF	Cortex-M3 / ITM
Not accessible	H'E0001000 to H'E0001FFF	H'E0001000 to H'E0001FFF	Cortex-M3 / DWT
Not accessible	H'E0002000 to H'E0002FFF	H'E0002000 to H'E0002FFF	Cortex-M3 / FPB
Not accessible	H'E0003000 to H'E0003FFF	H'E0003000 to H'E0003FFF	—
Not accessible	H'E000E000 to H'E000EFFF	H'E000E000 to H'E000EFFF	Cortex-M3 / SCS(NVIC)
Not accessible	H'E000F000 to H'E003FFFF	H'E000F000 to H'E003FFFF	—
Not accessible	H'E0040000 to H'E0040FFF	H'E0040000 to H'E0040FFF	—
Not accessible	H'E0041000 to H'E0041FFF	H'E0041000 to H'E0041FFF	Cortex-M3 / ETM-M3
Not accessible	H'E0042000 to H'E0042FFF	H'E0042000 to H'E0042FFF	Cortex-M3 / CTI
Not accessible	H'E0043000 to H'E0043FFF	H'E0043000 to H'E0043FFF	—
Not accessible	H'E00FF000 to H'E00FFFFF	H'E00FF000 to H'E00FFFFF	Cortex-M3 / ROM Table

Table 10.7 CoreSight Address Map

Cortex-R4 CPU View	Cortex-M3 CPU View (only for products incorporating an R-IN engine)	module
E800 0000h to E800 0FFFh	E800 0000h to E800 0FFFh	CoreSight / DAP ROM
E800 1000h to E800 1FFFh	E800 1000h to E800 1FFFh	CoreSight / ETB
E800 2000h to E800 2FFFh	E800 2000h to E800 2FFFh	CoreSight / CTI
E800 3000h to E800 3FFFh	E800 3000h to E800 3FFFh	CoreSight / TPIU
E800 4000h to E800 4FFFh	E800 4000h to E800 4FFFh	CoreSight / Funnel
E800 5000h to E800 5FFFh	E800 5000h to E800 5FFFh	CoreSight / ITM
E800 6000h to E800 6FFFh	E800 6000h to E800 6FFFh	CoreSight / SWO
E800 7000h to E800 7FFFh	E800 7000h to E800 7FFFh	—
E800 8000h to E800 8FFFh	E800 8000h to E800 8FFFh	Cortex-R4 / CPU
E800 9000h to E800 9FFFh	E800 9000h to E800 9FFFh	Cortex-R4 / CTI
E800 A000h to E800 AFFFh	E800 A000h to E800 AFFFh	Cortex-R4 / ETM-R4
E800 B000h to E800 BFFFh	E800 B000h to E800 BFFFh	—
E800 C000h to E800 CFFFh	E800 C000h to E800 CFFFh	—
E800 D000h to E800 DFFFh	E800 D000h to E800 DFFFh	—
E800 E000h to E800 EFFFh	E800 E000h to E800 EFFFh	—
E800 F000h to E800 FFFFh	E800 F000h to E800 FFFFh	—

Table 10.8 lists the input/output pins of the debugging interface.

Table 10.8 Configuration of Pins for the Debugging Interface

Name	Pin Name	I/O	Functions
Test Clock	TCK	Input	Data is serially supplied from the Test Data Input (TDI) pin to this module, synchronized with this clock, and output from the Test Data Output (TDO) pin. In SWD mode, this pin works as the SWDCLK pin.
Test Mode Select	TMS	Input/Output	Changing the level of this signal, by synchronizing with TCK, will determine the status of the TAP (Test Access Port) control circuit. The protocol conforms to the JTAG standard (IEEE Std.1149.1). In SWD mode, this pin works as the SWDIO pin.
Test Reset	TRST#*1	Input	This pin accepts input asynchronously with TCK. When the level of this pin is Low, TAP (Test Access Port) is reset. When the levels of the TRST# pin and RES# pin are both Low, TAP and the debugging circuit are reset.
Test Data Input	TDI	Input	Changing the level of this pin, by synchronizing with TCK, will send data to this module. This pin can also be used as a general-purpose port. The initial function is TDI.
Test Data Output	TDO	Output	Reading the level of this pin, by synchronizing with TCK, will read data from this module. This pin can also be selected as the output pin of SWV. This pin can also be used as a general-purpose port. The initial function is TDO.
Trace Clock Output	TRACECLK	Output	This pin is an output pin of the clock used for synchronizing trace data.
Trace Enable Output	TRACECTL	Output	This pin is an output pin of the enable signal for trace control. This pin can also be selected as the output pin of SWV.
Trace Data Output	TRACEDATA7 to TRACEDATA0	Output	This pin is an output pin of trace data. TRACEDATA0 can be selected as an output pin of SWV.
Boundary Scan Setting	BSCANP	Input	Input the high level when boundary scan test is performed. Input Low when debugging is performed by CoreSight. For details on boundary scan, see section 40, Boundary Scan.

Note 1. When you design a board on which an emulator can be used, set the TRST# pin to Low while the RES# pin is asserted at power up, and configure the board so that control is available by the TRST# pin only. When this pin is not used, fix it to Low, or connect it so that the same signal as that on the RES# pin is to be input. For details, see section 10.3.5, Reset Configuration and the Method of Connecting with the Emulator.

10.2 Register Descriptions

10.2.1 Debugging Interface Control Register (DBGIFCNT)

The DBGIFCNT register controls the pins used by the debugging interface.

Address(es): A00B 0A00h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWVSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SWVSEL[1:0]	SWV Output Select	Selects the pin for SWV (Serial Wire Viewer) output. b1 b0 0 0: SWV output is not output. 0 1: SWV output is output from the TDO pin. 1 0: SWV output is output from the TRACEDATA0 pin. 1 1: SWV output is output from the TRACECTL pin.	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)

10.3 Operation

10.3.1 JTAG Interface

The JTAG interface uses five signals (TCK, TMS, TDO, TDI, and TRST#) to communicate with the host machine (PC) via the emulator. Figure 10.3 shows an example connection, which includes the RES# pin connection.

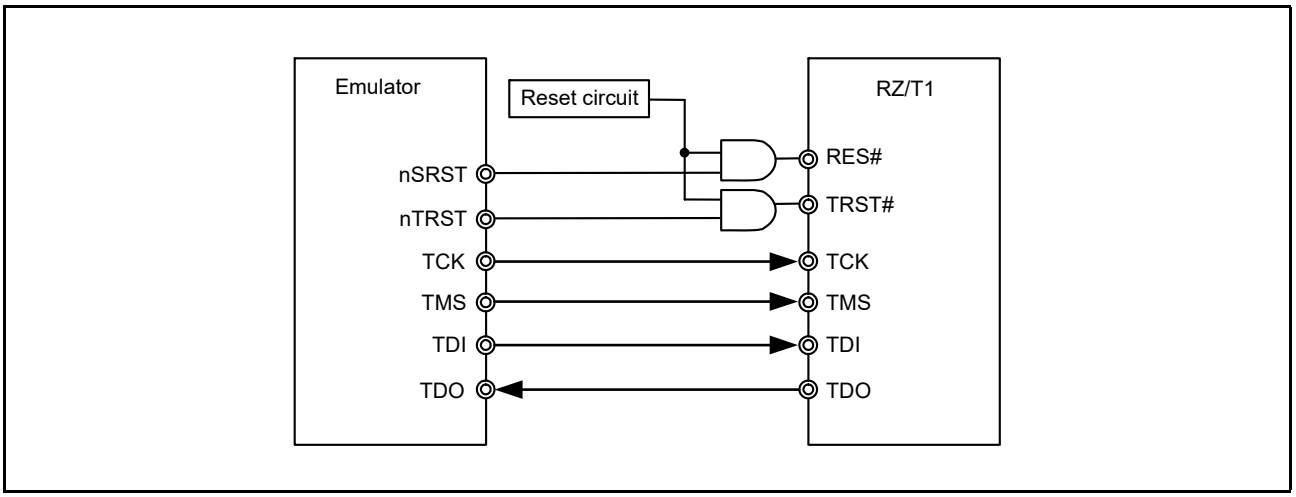


Figure 10.3 Example Connection of the JTAG Interface

10.3.2 SWD Interface

The SWD (Serial Wire Debug) interface uses two signals (SWCLK (TCK) and SWDIO (TMS)) to communicate with the host machine (PC) via the emulator. Figure 10.4 shows an example connection, which includes the RES# pin connection.

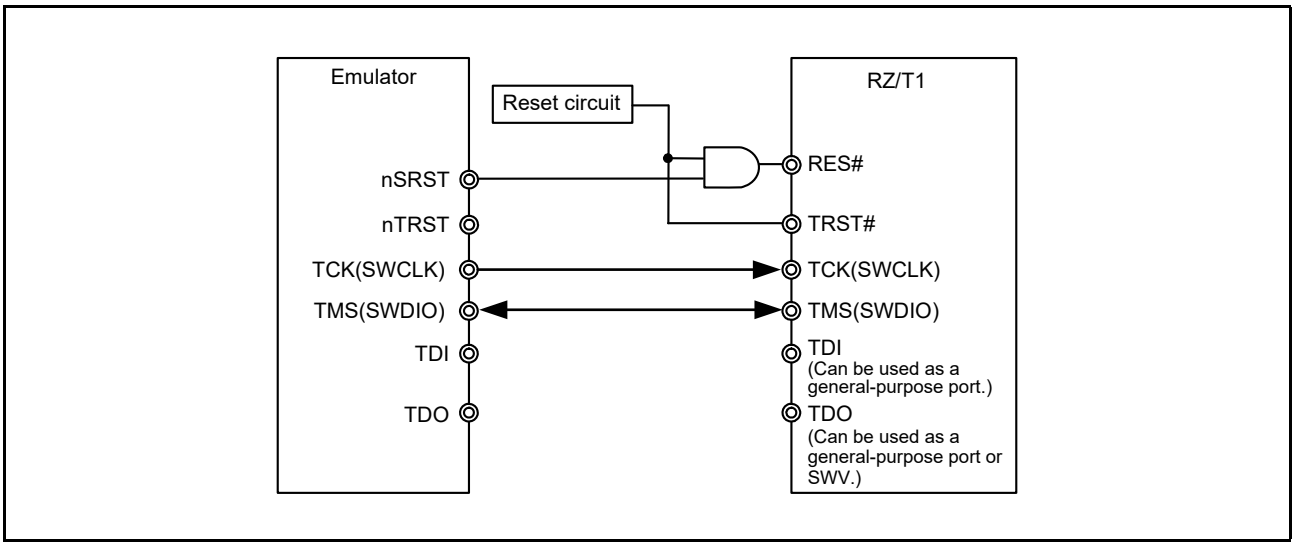


Figure 10.4 Example Connection of the SWD Interface

When the SWD interface is used for debugging, the TDI and TDO pins can be used as general-purpose ports. When you use these pins as general-purpose ports, perform pin settings by referring to section 18, Multi-Function Pin Controller (MPC).

Note: In the initial status of this LSI, the debugging interface is in JTAG mode. If you use the TDI and TDO pins as general-purpose ports and the emulator connection for debugging, switch the mode to SWD (Serial Wire Debug) mode by the control from the debugger, and then start debugging.

10.3.3 Trace Port Interface

The trace port interface uses ten signals (TRACECLK, TRACECTL, and TRACEDATA7 to TRACEDATA0) to output trace information. Information about branch instructions of the executed program (obtained by the ETM (Embedded Trace Macrocell) trace) is output from the trace port interface. After the debugger complements the information, you can know the branch source and destination at the time a branch occurred. For details on trace information, see the manual of each emulator vendor.

Only DDR clocking mode is supported for the synchronization relationship between the TRACECLK pin and TRACEDATA pin.

The maximum number of available TRACEDATA pins is 8. If the number of TRACEDATA pins is smaller than 8, the pins with smaller numbers are used (from TRACEDATA0). Set whether to connect the TRACECTL pin to TPA (Trace Port Analyzer), according to the specifications of the trace data transfer format of the TPA.

As the output frequency of the TRACECLK pin, 37.5 MHz (obtained by dividing the trace I/F clock (TCLK) by 2) can be set. For details, see section 7, Clock Generation Circuit.

In the initial status, different functions are assigned to the TRACECLK, TRACEDATA0 to TRACEDATA7, and TRACECTL pins. Perform pin settings by referring to section 18, Multi-Function Pin Controller (MPC).

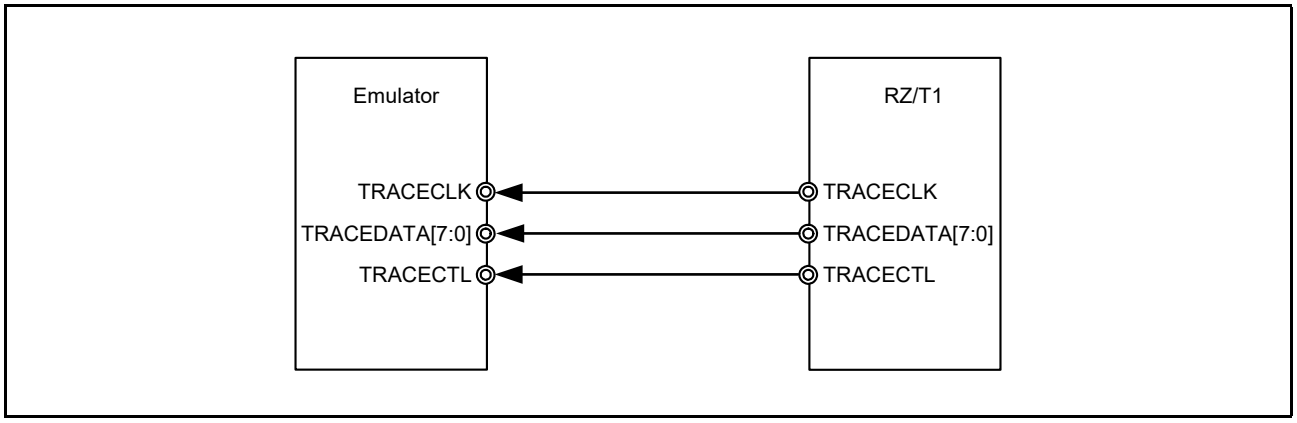


Figure 10.5 Example Connection of the Trace Port Interface

10.3.4 SWV Interface

The SWV (Serial Wire Viewer) interface is used to output trace information from the pin (TDO (SWV), TRACEDATA0 (SWV), or TRACECTL (SWV)) set by the DBGIFCNT register. When the JTAG interface is used, TDO (SWV) cannot be used. The SWV trace is a function that samples specified data at the specified sampling-cycle interval. For details on trace information, see the manual of each emulator vendor.

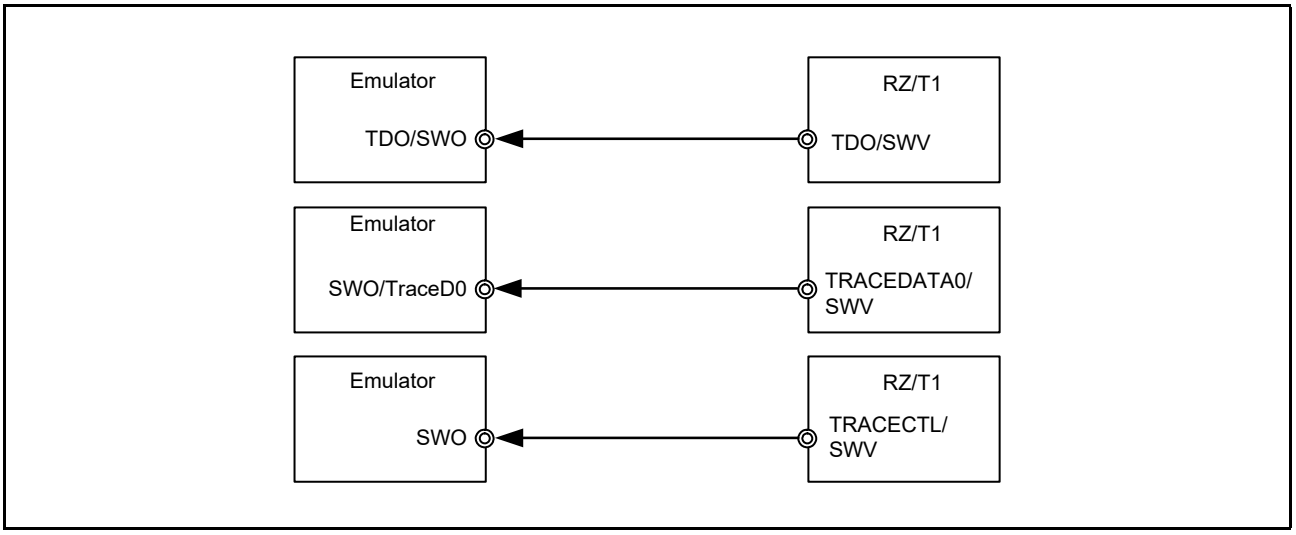


Figure 10.6 Example Connection of the SWV Interface

10.3.5 Reset Configuration and the Method of Connecting with the Emulator

When you design a board on which the emulator can be used, set the TRST# pin to Low while the RES# pin is asserted at power up. Also, configure the board so that control is available by the TRST# pin only.
When debugging is performed, if the initial level of the RES# and TRST# pins are both Low, the CPU and debugging section become the reset status. Then, setting the TRST# pin to High while the RES# pin is kept to Low will enable the debugging setting before CPU startup.
When the emulator is not connected, fix the TRST# pin to Low, or let the signal same as that on the RES# pin input to the TRST# pin.

Note: When debugging is performed by CoreSight, input Low to the BSCANP pin to disable the boundary scan function.

10.3.5.1 Example Connection of the Emulator That Cannot Drive the nTRST Output to High

Figure 10.7 shows an example of connection circuit when an emulator that cannot drive the nTRST output to High is used. The TRST# pin is pulled up, and is asserted to Low by the emulator. To perform debugging settings before CPU startup, follow the timing chart for when the emulator is connected (see Figure 10.7).

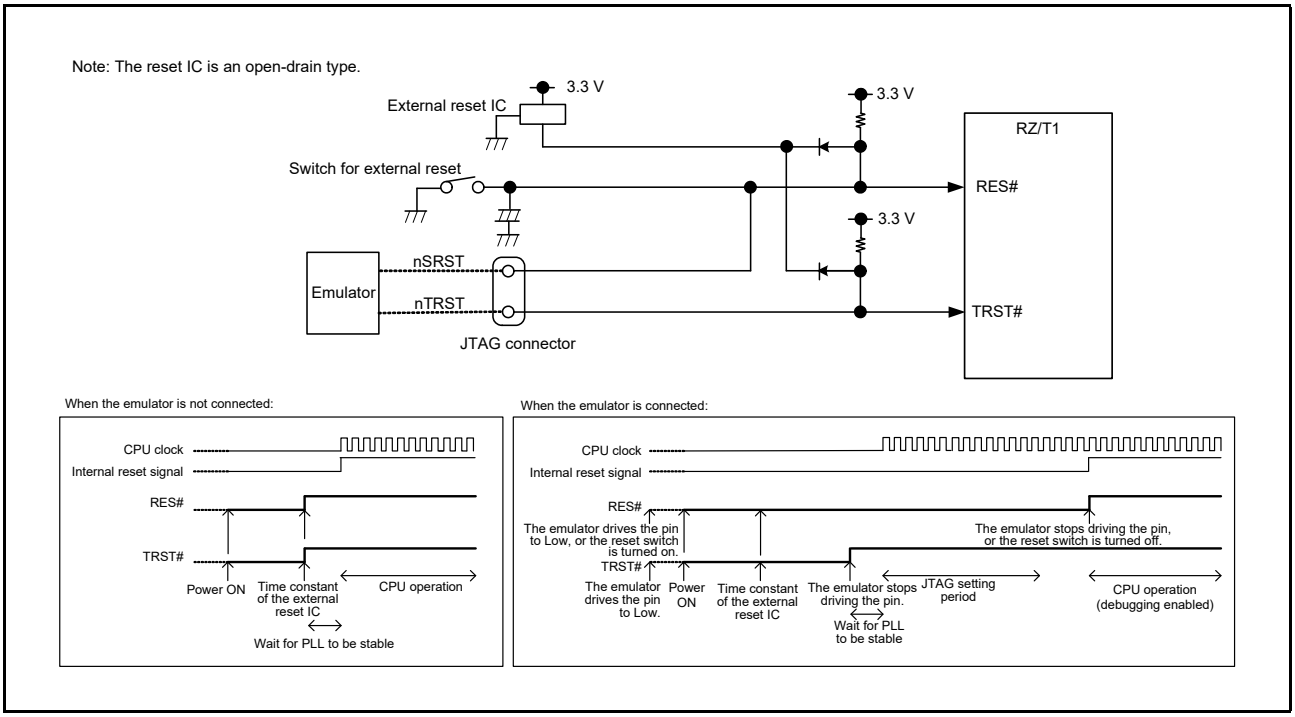


Figure 10.7 Example of Connection Circuit of an Emulator That Cannot Drive the nTRST Output to High

10.3.5.2 Example Connection of the Emulator That Can Drive the nTRST Output to High

Figure 10.8 shows an example of connection circuit when an emulator that can drive the nTRST output to High is used. The TRST# pin (High or Low) is controlled by the emulator. To perform debugging settings before CPU startup, follow the timing chart when the emulator is connected (see Figure 10.8).

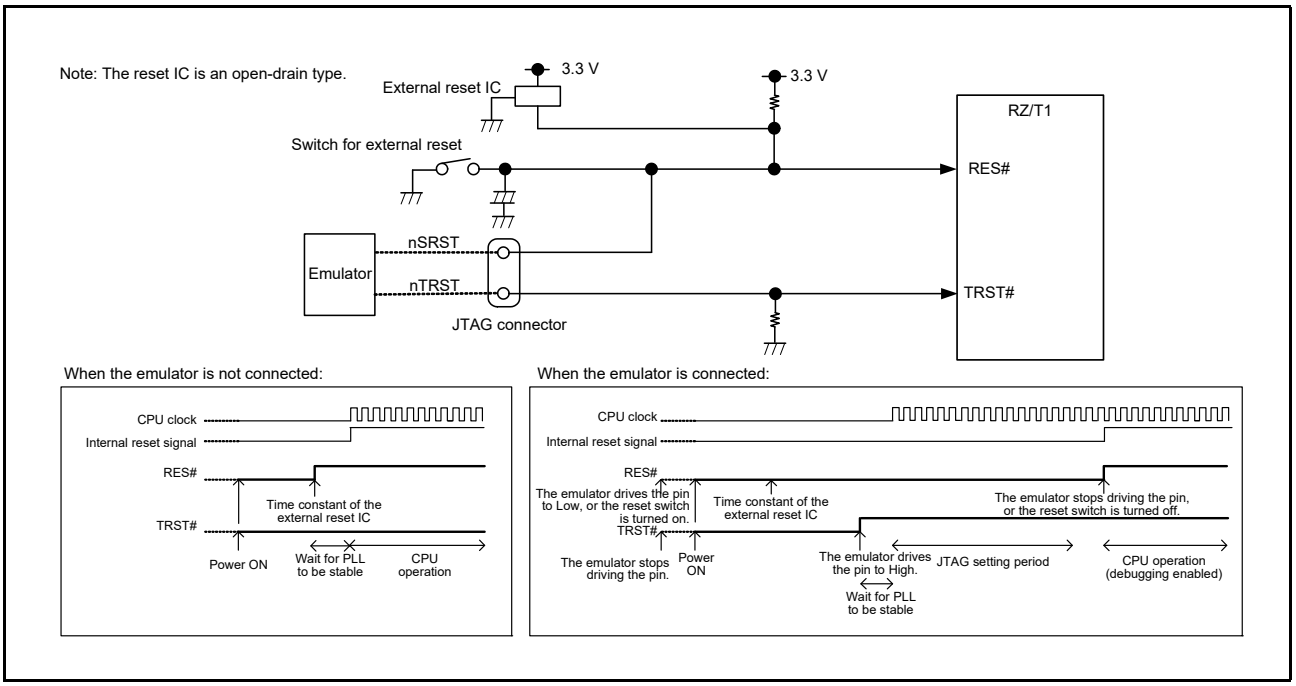


Figure 10.8 Example of Connection Circuit of an Emulator That Can Drive the nTRST Output to High

10.3.6 Handling of JTAG Pins When No Emulator Is Connected

If no emulator is connected, pin handling is required according to Table 10.9.

Table 10.9 Handling of JTAG Pins When No Emulator Is Connected

Pin Name	Handling
TCK	Pull down the pin.
TMS	Pull up the pin.
TDI	Pull up the pin (except when the port is used as a general-purpose port).
TDO	Open the pin (except when the port is used as a general-purpose port).
TRST#	Pull down the pin, or let the signal same as that on the RES# pin input.

10.3.7 Noise Reduction of the TRST# Pin

Analog delay noise reduction is performed for the TRST# pin. This measure against noise can remove noise that is within 100 ns at minimum.

10.3.8 Available Trace Functions

Table 10.10 lists the trace functions that are available via the respective debugging ports (trace port interface, SWV, and SWD or JTAG).

Table 10.10 Available Trace Functions

CPU Core	Debugging Port	Trace Functions
Cortex-R4 (CR4)	Trace Port interface	Full instruction tracing through the ETM of the Cortex-R4 Software tracing through the ITM among the CoreSight macrocells
	SWV	Only software tracing through the ITM among the CoreSight macrocells
	SWD/JTAG	The same information as for the trace port interface can be acquired via the ETB.
Cortex-M3 (CM3) (only for products incorporating an R-IN engine)	Trace Port interface	Full instruction tracing through the ETM of the Cortex-M3 Data tracing by the DWT through the ITM of the Cortex-M3 Software tracing through the ITM of the Cortex-M3
	SWV	Only software tracing through the ITM among the CoreSight macrocells
	SWD/JTAG	The same information as for the trace port interface can be acquired via the ETB.

When using software tracing through the ITM among the CoreSight macrocells, access the ITM by software from the CPU. For the address range of the ITM within the CoreSight registers, see Table 10.7.

10.4 Usage Note

10.4.1 SWV Interface

Due to the connection configuration in CoreSight, the ITM (including functions, such as watch point) output dedicated to Cortex-M3 (for products incorporating an R-IN engine) cannot be retrieved via the SWV (Serial Wire Viewer) interface. If you want to retrieve this output signal, use the trace port interface or the JTAG or SWD interface via ETB.

10.4.2 Access to the Main Bus

Access to the main bus by the DAP is via either the Cortex-R4 or Cortex-M3. When access is to be through the Cortex-M3, the setting of software reset register 2 (SWRR2) will have to be changed to release the Cortex-M3 from the reset state beforehand.
For details on software reset register 2, see section 6, Reset.

10.4.3 ROM Table

When using the ROM table to search for all debugging components including the Cortex-M3, search both the ROM table 1, which is connected to AP1 of the DAP, and ROM table 2, which is connected to the PPB via AP3.

11. Register Write Protection Function

11.1 Overview

The register write protection function protects important registers from being overwritten in case a program runs out of control. The registers to be protected are set with the protect register (PRCR).

Table 11.1 shows the correspondence between the PRCR register bits and the registers to be protected.

Table 11.1 Correspondence between PRCR Register Bits and Registers to be Protected

PRCR Register	Registers to be Protected
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, DSCR, PLL1CR, PLL1CR2, LOCOCR, OSTDCR
PRC1 bit	• Registers related to the low-power consumption functions: MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, MSTPCRE, MSTPCRF • Reset-related registers: RSTSR0, SWRR1, SWRR2, MRCTLC
PRC3 bit	• ATCM wait control register SYTATCMWAIT

11.2 Register Descriptions

11.2.1 Protect Register (PRCR)

The PRCR register controls writing to the protected registers.

Address(es): A00B 0B00h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PRC0	Protect 0	Enables writing to the registers related to the clock generation circuit. 0: Write disabled 1: Write enabled	R/W
b1	PRC1	Protect 1	Enables writing to the registers related to low-power consumption functions and reset. 0: Write disabled 1: Write enabled	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect 3	Enables writing to the ATCM wait control register. 0: Write disabled 1: Write enabled	R/W
b7 to 4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control permission and prohibition of writing to the PRCR register. To modify the PRCR register, write A5h to PRKEY[7:0]. When a value other than A5h is written to these bits, writing to the PRCR register has no effect.	R/(W)*1
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value written to these bits is not retained. These bits are always read as 00h.

PRCi Bits (Protect i) (i = 0, 1, 3)

These bits enable or disable writing to the corresponding registers to be protected.

Setting the PRCi bits to 1 and 0 enables and disables writing to the corresponding registers to be protected, respectively.

12. Interrupt Controller (ICUA)

12.1 Overview

Two types of interrupt controller, the vector interrupt controller (VIC) for the Cortex-R4 and the nested-type vector interrupt controller (NVIC) for the Cortex-M3 (for products incorporating an R-IN Engine) are provided. The interrupt controllers accept interrupt requests from peripheral modules, external pins including those from the Ethernet PHY, and the external DMA request pins. An interrupt accepted by the interrupt controller is set either as an interrupt for conveying to the CPU (the Cortex-R4 or Cortex-M3 (for products incorporating an R-IN engine)) or as an activating trigger signal for the DMAC.

Table 12.1 lists interrupt specifications, and Figure 12.1 and Figure 12.2 are block diagrams of the interrupt controller.

Table 12.1 Specifications of Interrupt Controller

Item		Description
Interrupts	Interrupt contact destinations	• Cortex-R4 • Two DMAC units (unit 0: 16ch., unit 1: 16ch.) • Cortex-M3 (for products incorporating an R-IN engine)
	Peripheral function interrupts	Interrupts from peripheral modules*1 Interrupt detection: Edge detection/level detection
	External pin interrupts	Interrupts from pins Ethernet PHY0 to 2, IRQ0 to IRQ15 Number of sources: 19 Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. Digital noise filter function: Supported
	Interrupts between the CPUs (for products incorporating an R-IN engine)	Mutual interrupts between Cortex-R4 and Cortex-M3 by software interrupts Number of sources: 1
	Interrupt priority level	For interrupts to the CPU, the priority level is set in 16 levels by the register.*2
	DMAC control	According to the interrupt source, DMAC can be activated. Switches interrupts from peripheral modules to DMA transfer completion interrupts.*3
	External DMA request	External DMA request pins (DREQ0 to DREQ2) can output DACK0 to DACK2, TEND0 to TEND2 according to DMA transfer to an external bus, and the request number. Number of sources: 3 Digital noise filter function: Supported
Non-maskable interrupts	NMI pin interrupts	Interrupts from the NMI pin Interrupt detection: Falling edge/rising edge Digital noise filter function: Supported
	For Cortex-R4	The following sources can be allocated as the non-maskable high-speed interrupt (FIQ) source. • Non-maskable interrupts from ECM (Error Control Module) • Non-maskable interrupts from the NMI pin
	For Cortex-M3 (for products incorporating an R-IN engine)	Allocate the following source to NMI input of NVIC. • Error interrupts of WDT for CM3 when a down-counter underflow occurs, or when a refresh error occurs
Restoration from the sleep status		Restoration due to non-maskable interrupt and all unmasked interrupt sources

Note 1. According to interrupt contact destinations, interrupt sources differ. For details on activation sources, see Table 12.3, Cortex-R4/DMAC Interrupt Vector Table and Table 12.6, CM3 Interrupt Vector Table.

Note 2. The 16 priority levels are valid for all sources with CR4 (VIC) vector numbers 1 to 255, and CM3 (for products incorporating an R-IN engine) (NVIC) vector numbers 1 to 127. Interrupt sources with CR4 (VIC) vector numbers 256 and later have priority lower than sources for vector numbers 1 to 255. For details, see section 12.4.6.1, Restrictions on VIC Priority Levels.

Note 3. When an interrupt signal is selected as the source for activating the DMAC, generation of the interrupt signal activates the DMAC but branching to interrupt handling does not proceed at this time. The DMAC generates a transfer completion interrupt when it completes the data transfer. For details, see section 12.3.1, Selecting Interrupt Request Destinations.

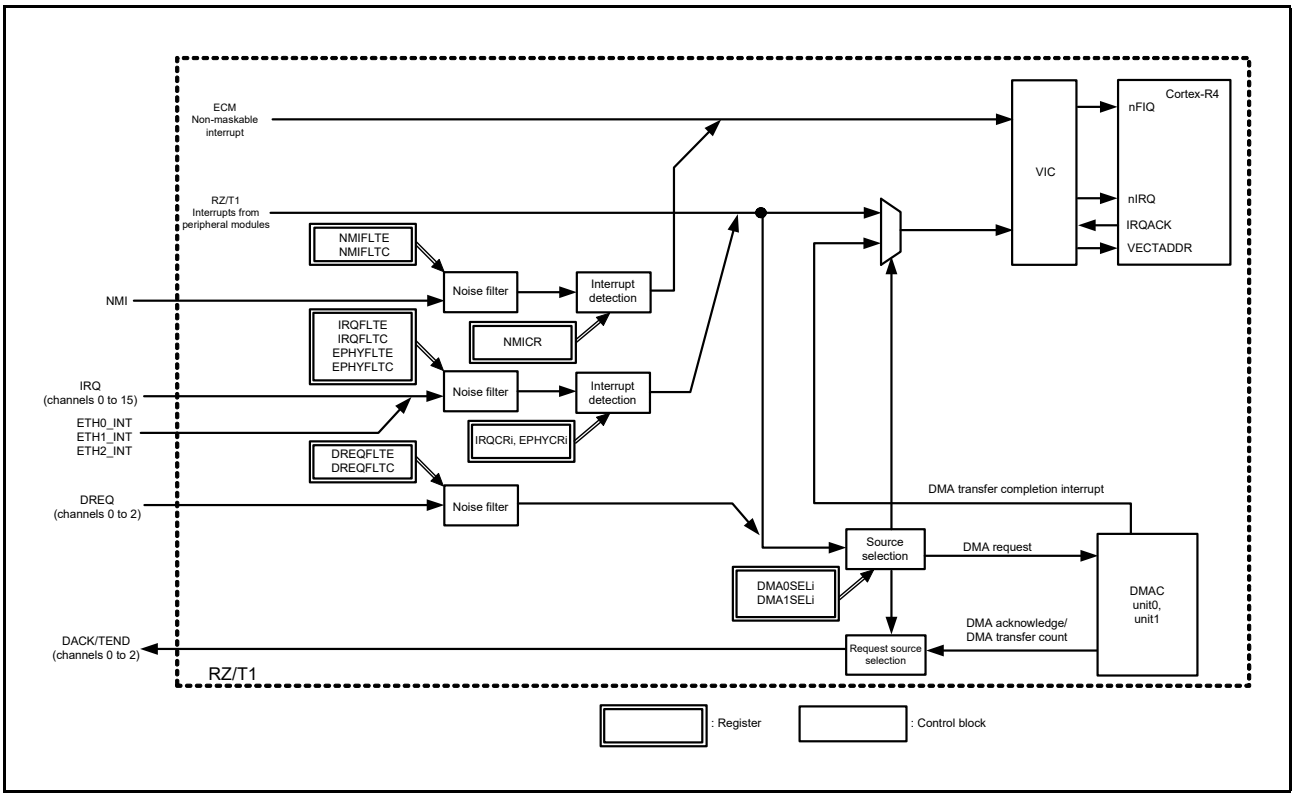


Figure 12.1 Block Diagram of Interrupt Controller

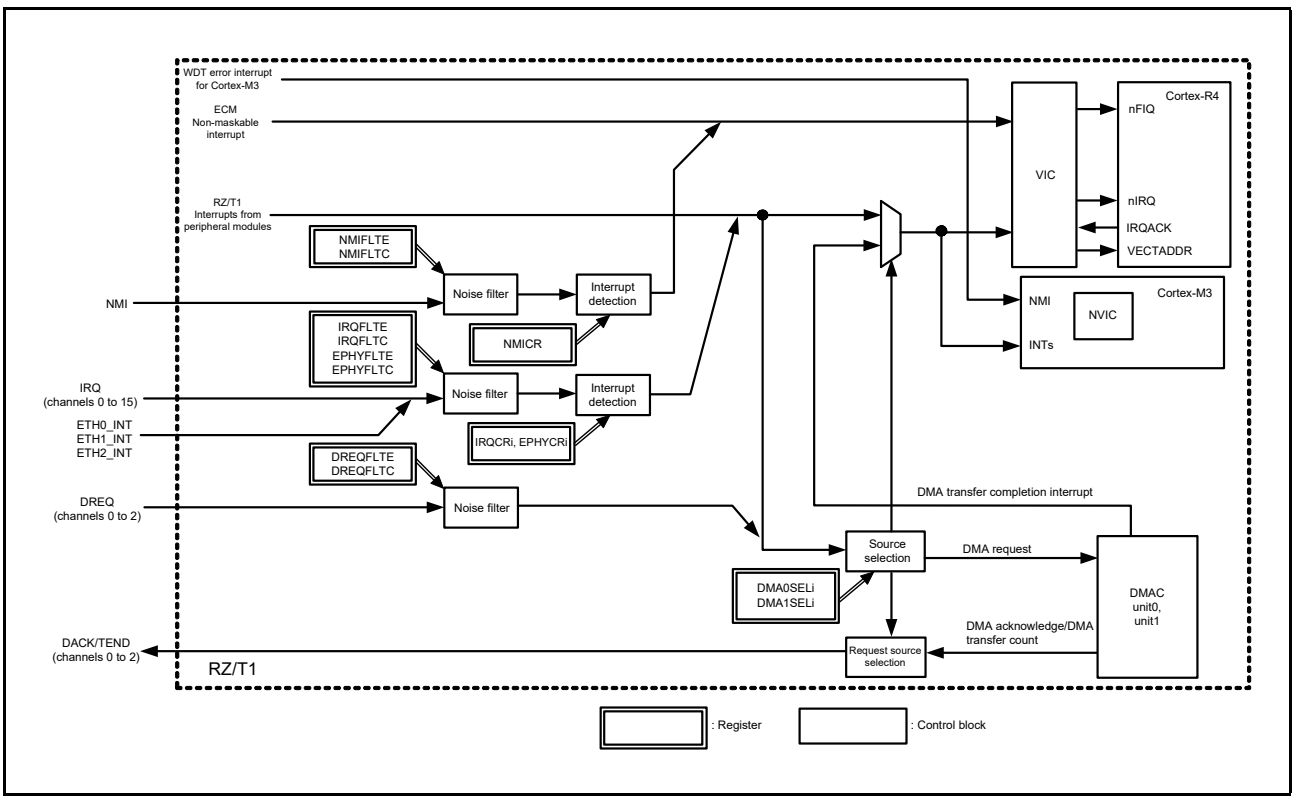


Figure 12.2 Block Diagram of Interrupt Controller (for products incorporating an R-IN engine)

Table 12.2 lists input/output pins that are used by interrupt controllers.

Table 12.2 Input/output Pins for Interrupt Controllers

Pin Name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ15	Input	Maskable interrupt request pin
ETH0_INT	Input	Ethernet PHY0 interrupt request pin
ETH1_INT	Input	Ethernet PHY1 interrupt request pin
ETH2_INT	Input	Ethernet PHY2 interrupt request pin
DREQ0 to DREQ2	Input	External DMA request
DACK0 to DACK2	Output	External DMA acknowledgment
TEND0 to TEND2	Output	External DMA transfer completion

12.2 Register Descriptions

12.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 15)

The IRQCRi register sets the method for detecting the external pin interrupt source (IRQ0 to IRQ15).

Address(es): ICU.IRQCR0 A009 4200h, ICU.IRQCR1 A009 4204h, ICU.IRQCR2 A009 4208h, ICU.IRQCR3 A009 420Ch, ICU.IRQCR4 A009 4210h, ICU.IRQCR5 A009 4214h, ICU.IRQCR6 A009 4218h, ICU.IRQCR7 A009 421Ch, ICU.IRQCR8 A009 4220h, ICU.IRQCR9 A009 4224h, ICU.IRQCR10 A009 4228h, ICU.IRQCR11 A009 422Ch, ICU.IRQCR12 A009 4230h, ICU.IRQCR13 A009 4234h, ICU.IRQCR14 A009 4238h, ICU.IRQCR15 A009 423Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	IRQMD[1:0]		—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3, b2	IRQMD[1:0]	IRQ Detection Sense Select	b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

IRQMD[1:0] Bits (IRQ Detection Sense Select)

These bits set the method for detecting the external pin interrupt source (IRQ0 to IRQ15).

For details on the methods for detecting external pin interrupt sources, see section 12.3.3, External Pin Interrupts.

Note: The same detection method should be set to the PLSn register of the VIC.

12.2.2 IRQ Pin Digital Noise Filter Enable Register (IRQFLTE)

The IRQFLTE register sets whether to use the digital noise filter for the external pin interrupt source (IRQ0 to IRQ15).

Address(es): ICU.IRQFLTE A009 4240h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN 15	FLTEN 14	FLTEN 13	FLTEN 12	FLTEN 11	FLTEN 10	FLTEN 9	FLTEN 8	FLTEN 7	FLTEN 6	FLTEN 5	FLTEN 4	FLTEN 3	FLTEN 2	FLTEN 1	FLTEN 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FLTEN0	IRQ0 Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b1	FLTEN1	IRQ1 Digital Noise Filter Enable		R/W
b2	FLTEN2	IRQ2 Digital Noise Filter Enable		R/W
b3	FLTEN3	IRQ3 Digital Noise Filter Enable		R/W
b4	FLTEN4	IRQ4 Digital Noise Filter Enable		R/W
b5	FLTEN5	IRQ5 Digital Noise Filter Enable		R/W
b6	FLTEN6	IRQ6 Digital Noise Filter Enable		R/W
b7	FLTEN7	IRQ7 Digital Noise Filter Enable		R/W
b8	FLTEN8	IRQ8 Digital Noise Filter Enable		R/W
b9	FLTEN9	IRQ9 Digital Noise Filter Enable		R/W
b10	FLTEN10	IRQ10 Digital Noise Filter Enable		R/W
b11	FLTEN11	IRQ11 Digital Noise Filter Enable		R/W
b12	FLTEN12	IRQ12 Digital Noise Filter Enable		R/W
b13	FLTEN13	IRQ13 Digital Noise Filter Enable		R/W
b14	FLTEN14	IRQ14 Digital Noise Filter Enable		R/W
b15	FLTEN15	IRQ15 Digital Noise Filter Enable		R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FLTENi Bit (IRQi Digital Noise Filter Enable) (i = 0 to 15)

This bit enables the digital noise filter used for the external pin interrupt source (IRQ0 to IRQ15).

When this bit is set to 1, the digital noise filter is enabled. When it is cleared to 0, the digital noise filter function is disabled.

The IRQi pin level is sampled at the sampling clock cycle specified with the IRQFLTC.FCLKSELi[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter.

12.2.3 IRQ Pin Digital Noise Filter Setting Register (IRQFLTC)

The IRQFLTC register sets the digital noise filter sampling clock for external pin interrupt request pins (IRQ0 to IRQ15).

Address(es): ICU.IRQFLTC A009 4244h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FCLKSEL15 [1:0]		FCLKSEL14 [1:0]		FCLKSEL13 [1:0]		FCLKSEL12 [1:0]		FCLKSEL11 [1:0]		FCLKSEL10 [1:0]		FCLKSEL9 [1:0]		FCLKSEL8 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FCLKSEL7 [1:0]		FCLKSEL6 [1:0]		FCLKSEL5 [1:0]		FCLKSEL4 [1:0]		FCLKSEL3 [1:0]		FCLKSEL2 [1:0]		FCLKSEL1 [1:0]		FCLKSEL0 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	FCLKSEL0[1:0]	IRQ0 Digital Noise Filter Sampling Clock Setting	Odd b Even b 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
b3, b2	FCLKSEL1[1:0]	IRQ1 Digital Noise Filter Sampling Clock Setting		R/W
b5, b4	FCLKSEL2[1:0]	IRQ2 Digital Noise Filter Sampling Clock Setting		R/W
b7, b6	FCLKSEL3[1:0]	IRQ3 Digital Noise Filter Sampling Clock Setting		R/W
b9, b8	FCLKSEL4[1:0]	IRQ4 Digital Noise Filter Sampling Clock Setting		R/W
b11, b10	FCLKSEL5[1:0]	IRQ5 Digital Noise Filter Sampling Clock Setting		R/W
b13, b12	FCLKSEL6[1:0]	IRQ6 Digital Noise Filter Sampling Clock Setting		R/W
b15, b14	FCLKSEL7[1:0]	IRQ9 Digital Noise Filter Sampling Clock Setting		R/W
b17, b16	FCLKSEL8[1:0]	IRQ8 Digital Noise Filter Sampling Clock Setting		R/W
b19, b18	FCLKSEL9[1:0]	IRQ9 Digital Noise Filter Sampling Clock Setting		R/W
b21, b20	FCLKSEL10[1:0]	IRQ10 Digital Noise Filter Sampling Clock Setting		R/W
b23, b22	FCLKSEL11[1:0]	IRQ11 Digital Noise Filter Sampling Clock Setting		R/W
b25, b24	FCLKSEL12[1:0]	IRQ12 Digital Noise Filter Sampling Clock Setting		R/W
b27, b26	FCLKSEL13[1:0]	IRQ13 Digital Noise Filter Sampling Clock Setting		R/W
b29, b28	FCLKSEL14[1:0]	IRQ14 Digital Noise Filter Sampling Clock Setting		R/W
b31, b30	FCLKSEL15[1:0]	IRQ15 Digital Noise Filter Sampling Clock Setting		R/W

FCLKSELi[1:0] Bits (IRQi Digital Noise Filter Sampling Clock Setting) (i = 0 to 15)

These bits select the digital noise filter sampling clock for external pin interrupt request pins (IRQ0 to IRQ15).

The sampling clock cycle can be selected from the PCLKB (every cycle), PCKLB/8 (once every eight cycles), PCKLB/32 (once every 32 cycles), and PCKLB/64 (once every 64 cycles).

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter. Note that even if the digital noise filter is disabled, PCLKB of which interrupts are to be sampled does not stop.

12.2.4 Non-maskable Interrupt Status Register (NMISR)

The NMISR register monitors the status of non-maskable interrupt sources. Writing to this register is ignored.
For information on non-maskable interrupt requests from ECM, read ECMm error source status register m (ECMmESSTRm, m = 0 to 2) for ECM, and check the error source.
Before ending non-maskable interrupt handler processing, read the NMISR register, and check the occurrence status of other non-maskable interrupts. Make sure all bits of the NMISR register are cleared to 0 before ending the interrupt handler processing.

Address(es): ICU.NMISR A009 4248h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECMST	NMIST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMIST	NMI Status Flag	0: NMI pin interrupt is not requested. 1: NMI pin interrupt is requested.	R
b1	ECMST	ECM Error Status Flag	0: ECM non-maskable interrupt is not requested. 1: ECM non-maskable interrupt is requested.	R
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R

NMIST Flag (NMI Status Flag)

This flag indicates whether NMI pin interrupts are requested.
The NMIST flag is read only, and it can be cleared to 0 with the NMICLR.NMICLR bit.
[Setting condition]

- When the edgeset for the NMICR.NMIMD bit is input for the NMI pin

[Clearing condition]

- When 1 is written to the NMICLR.NMICLR bit

ECMST Flag (ECM Error Status Flag)

This flag indicates whether ECM non-maskable interrupts are requested.
The ECMST flag is read only, and it can be cleared to 0 by the NMICLR.ECMCLR bit.
[Setting condition]

- When ECM non-maskable interrupts are generated

[Clearing condition]

- When 1 is written to the NMICLR.ECMCLR bit

12.2.5 Non-maskable Interrupt Status Clear Register (NMICLR)

The NMICLR register clears NMI or ECM non-maskable interrupt requests.

Address(es): ICU.NMICLR A009 424Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECMCLR	NMICLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NMICLR	NMI Clear	This bit is read as 0. Writing 1 clears the NMISR.NMIST flag. Writing 0 to this bit is disabled.	R/(W)*1
b1	ECMCLR	ECM Clear	This bit is read as 0. Writing 1 clears the NMISR.ECMST flag. Writing 0 to this bit is disabled.	R/(W)*1
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written.

12.2.6 NMI Pin Interrupt Control Register (NMICR)

The NMICR register sets the method for detecting the NMI pin interrupt.

Address(es): ICU.NMICR A009 4250h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	NMIMD	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	NMIMD	NMI Detection Setting	0: Falling edge 1: Rising edge	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NMIMD Bit (NMI Detection Setting)

This bit sets the method for detecting the NMI pin interrupt.

12.2.7 NMI Pin Digital Noise Filter Enable Register (NMIFLTE)

The NMIFLTE register sets whether to use the digital noise filter for NMI pin interrupts.

Address(es): ICU.NMIFLTE A009 4254h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NFLTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFLTEN	NMI Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFLTEN Bit (NMI Digital Noise Filter Enable)

This bit enables the digital noise filter used for NMI pin interrupts.

When this bit is set to 1, the digital noise filter is enabled. When it is cleared to 0, the digital noise filter function is disabled.

The NMI pin level is sampled at the sampling clock cycle specified with the NMIFLTC.NFCLKSEL[1:0] bits. When the sampled level matches three times, the output level from the digital noise filter changes.

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter.

12.2.8 NMI Pin Digital Noise Filter Setting Register (NMIFLTC)

The NMIFLTC register sets the digital noise filter sampling clock for the NMI pin interrupt.

Address(es): ICU.NMIFLTC A009 4258h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NFCLKSEL [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NFCLKSEL[1:0]	NMI Digital Noise Filter Sampling Clock Setting	b1 b0 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFCLKSEL[1:0] Bits (NMI Digital Noise Filter Sampling Clock Setting)

These bits set the digital noise filter sampling clock of the NMI pin interrupt.

The sampling clock cycle can be selected from the PCLKB (every cycle), PCKLB/8 (once every eight cycles), PCKLB/32 (once every 32 cycles), and PCKLB/64 (once every 64 cycles).

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter. Note that if the digital noise filter is disabled, PCLKB of which interrupts are to be sampled does not stop.

12.2.9 Ethernet PHY Control Register i (EPHYCRi) (i = 0 to 2)

The EPHYCRi register sets the method for detecting the Ethernet PHY interrupt source (ETH0_INT/ETH1_INT/ETH2_INT).

Address(es): ICU.EPHYCR0 A009 425Ch, ICU.EPHYCR1 A009 4260h, ICU.EPHYCR2 A009 4264h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	EPHYMD [1:0]		—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3, b2	EPHYMD[1:0]	Ethernet PHY interrupt Detection Setting	b3 b2 0 0: Low level 0 1: Falling edge 1 0: Rising edge 1 1: Rising and falling edges	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

EPHYMD[1:0] Bits (Ethernet PHY Interrupt Detection Setting)

These bits set the method for detecting the Ethernet PHY interrupt source (ETH0_INT/ETH1_INT/ETH2_INT). For details on the detection method of Ethernet PHY interrupt request, see section 12.3.3, External Pin Interrupts.

Note: Set the PLS register in the VIC to the same method of detection as is set in this register.

12.2.10 Ethernet PHY Interrupt Request Pin Digital Noise Filter Enable Register (EPHYFLTE)

The EPHYFLTE register enables the digital noise filter used for the Ethernet PHY interrupt source (ETH0_INT/ ETH1_INT/ETH2_INT).

Address(es): ICU.EPHYFLTE A009 4268h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EFLTEN2	EFLTEN1	EFLTEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EFLTEN0	Ethernet PHY0 Interrupt Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b1	EFLTEN1	Ethernet PHY1 Interrupt Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b2	EFLTEN2	Ethernet PHY2 Interrupt Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

EFLTENi Bit (Ethernet PHY Interrupt Digital Noise Filter Enable) (i = 0 to 2)

This bit enables the digital noise filter used for Ethernet PHY interrupt source (ETH0_INT/ETH1_INT/ETH2_INT). When this bit is set to 1, the digital noise filter is enabled. When it is cleared to 0, the digital noise filter function is disabled.

The ETH0_INT/ETH1_INT/ETH2_INT pin level is sampled at the sampling clock cycle specified with the EPHYFLTE.FLTENi[1:0] bits. When the sampled level matches three times, the output level from the digital noise filter changes.

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter.

12.2.11 Ethernet PHY Interrupt Request Pin Digital Noise Filter Setting Register (EPHYFLTC)

The EPHYFLTC register sets the digital noise filter sampling clock for the Ethernet PHY interrupt request pin (ETH0_INT/ETH1_INT/ETH2_INT).

Address(es): ICU.EPHYFLTC A009 426Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	EFCLKSEL2 [1:0]		EFCLKSEL1 [1:0]		EFCLKSEL0 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	EFCLKSEL0[1:0]	Ethernet PHY0 Interrupts Digital Noise Filter Sampling Clock Setting	Odd b Even b 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
b3, b2	EFCLKSEL1[1:0]	Ethernet PHY1 Interrupts Digital Noise Filter Sampling Clock Setting		R/W
b5, b4	EFCLKSEL2[1:0]	Ethernet PHY2 Interrupts Digital Noise Filter Sampling Clock Setting		R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

EFCLKSELi[1:0] Bits (Ethernet PHYi Interrupt Digital Noise Filter Sampling Clock Setting) (i = 0 to 2)

These bits select the digital noise filter sampling clock for Ethernet PHY interrupt request pin (ETH0_INT/ETH1_INT/ETH2_INT).

The sampling clock cycle can be selected from the PCLKB (every cycle), PCKLB/8 (once every eight cycles), PCKLB/32 (once every 32 cycles), and PCKLB/64 (once every 64 cycles).

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter. Note that if the digital noise filter is disabled, PCLKB of which interrupts are to be sampled does not stop.

12.2.12 External DMA Request Pin Digital Noise Enable Register (DREQFLTE)

The DREQFLTE register sets the usage of the digital noise filter for external DMA request pin interrupt sources (DREQ0 to DREQ2).

Address(es): ICU.DREQFLTE A009 4270h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DFLTEN2	DFLTEN1	DFLTEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLTEN0	DREQ0 Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b1	DFLTEN1	DREQ1 Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b2	DFLTEN2	DREQ2 Digital Noise Filter Enable	0: Digital noise filter is disabled. 1: Digital noise filter is enabled.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DFLTENi Bit (DREQi Digital Noise Filter Enable) (i = 0 to 2)

This bit enables the digital noise filter used for external DMA request pin interrupt sources (DREQ0 to DREQ2).
When this bit is set to 1, the digital noise filter is enabled. When it is cleared to 0, the digital noise filter function is disabled.
The DREQi# pin level is sampled at the sampling clock cycle specified with the DREQFLTC.DFCLKSELi[1:0] bits. When the sampled level matches three times, the output level from the digital filter changes.
For details on the digital noise filter, see section 12.3.2, Digital Noise Filter.

12.2.13 External DMA Request Pin Digital Noise Setting Register (DREQFLTC)

The DREQFLTC register selects the digital noise filter sampling clock for external DMA request pins (DREQ0 to DREQ2).

Address(es): ICU.DREQFLTC A009 4274h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	DFCLKSEL2 [1:0]		DFCLKSEL1 [1:0]		DFCLKSEL0 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DFCLKSEL0[1:0]	DREQ0 Digital Noise Filter Sampling Clock Setting	Odd b Even b 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64	R/W
b3, b2	DFCLKSEL1[1:0]	DREQ1 Digital Noise Filter Sampling Clock Setting		R/W
b5, b4	DFCLKSEL2 [1:0]	DREQ2 Digital Noise Filter Sampling Clock Setting		R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DFCLKSELi[1:0] Bits (DREQi Digital Noise Filter Sampling Clock Setting) (i = 0 to 2)

These bits select the digital noise filter sampling clock for external DMA request pins (DREQ0 to DREQ2).

The sampling clock cycle can be selected from the PCLKB (every cycle), PCKLB/8 (once every eight cycles), PCKLB/32 (once every 32 cycles), and PCKLB/64 (once every 64 cycles).

For details on the digital noise filter, see section 12.3.2, Digital Noise Filter. Note that if the digital noise filter is disabled, PCLKB of which interrupts are to be sampled does not stop.

12.2.14 Interrupts between the CPUs Request Register (CPUINT) (only for products incorporating an R-IN engine)

The CPUINT register requests interrupts to each CPU when Cortex-R4 requests interrupts to Cortex-M3, or when Cortex-M3 requests interrupts to Cortex-R4.

Address(es): ICU.CPUINT A009 4290h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CR4INT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CM3INT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CM3INT	Cortex-M3 Interrupt Request	1: Interrupts are requested to Cortex-M3. 0: Disabled (Interrupts are not requested). This bit is always read as 0.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	CR4INT	Cortex-R4 Interrupt Request	1: Interrupts are requested to Cortex-R4. 0: Disabled (Interrupts are not requested). This bit is always read as 0.	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CM3INT Bit (Cortex-M3 Interrupt Request)

This bit requests an interrupt to Cortex-M3.

When you want to request an interrupt to Cortex-M3, write 1. This interrupt request is assigned to Cortex-M3 interrupt vector number 1. If you write 0, no interrupt is performed. This bit is always read as 0.

CR4INT Bit (Cortex-R4 Interrupt Request)

This bit requests interrupt to Cortex-R4.

When you want to request an interrupt to Cortex-R4, write 1. This interrupt request is assigned to Cortex-R4 interrupt vector number 1. If you write 0, no interrupt is performed. This bit is always read as 0.

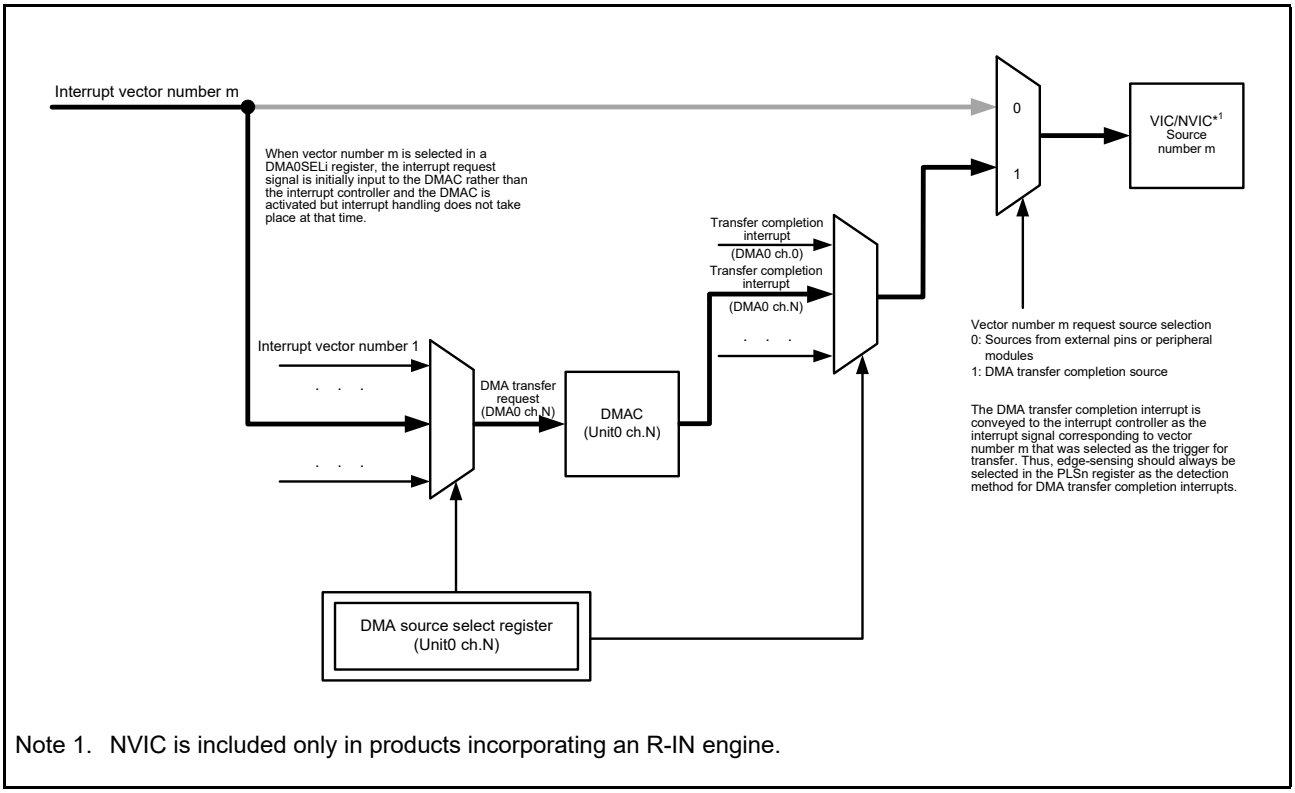
12.3 Operation

12.3.1 Selecting Interrupt Request Destinations

Table 12.3, Cortex-R4/DMAC Interrupt Vector Table, is a list of the requesting sources and indicates the source for which the CPU or DMAC is selectable as the destination. When the CPU is selected as the destination, the processing currently in progress branches to the interrupt handling routine in response to the interrupt request. When the DMAC is selected as the destination, DMA transfer starts in response to the interrupt request signal. In this case, a DMAC transfer completion interrupt is generated on completion of the transfer. Do not select interrupt request destinations that do not have the letter Y in the given request destination column in Table 12.3, Cortex-R4/DMAC Interrupt Vector Table.
Figure 12.3 shows the flow of selecting an interrupt source when vector number m is allocated to channel N of unit 0 as the DMA source. Vector numbers selected in the DMA source select register are not connected to an interrupt controller (VIC/NVIC)*1, but they are connected as DMA transfer requests to the corresponding channels of one of the DMACs. On completion of the DMA transfer, the transfer completion interrupt signal for the given channel of the DMAC is connected as the trigger for interrupt handling by the routine indicated by vector number m for the VIC/NVIC.
For example, when interrupt vector number 21 (compare match interrupt_ch.0 of CMT unit 0) is selected for IFC[7:0] of the DMAC unit 0 source select register 0 (DMA0SEL0), if this interrupt occurs, DMA transfer is requested on channel 0 of DMAC unit 0. After DMA transfer, if a DMA transfer completion interrupt is generated, the DMA transfer completion request for channel 0 of DMAC unit 0 is connected to the same interrupt vector number (21) for VIC/NVIC*1.
If vector number m is not selected by the source select register, interrupts from external pins and peripheral modules are connected to the interrupt controller VIC/NVIC*1 for the CPU (Figure 12.4).

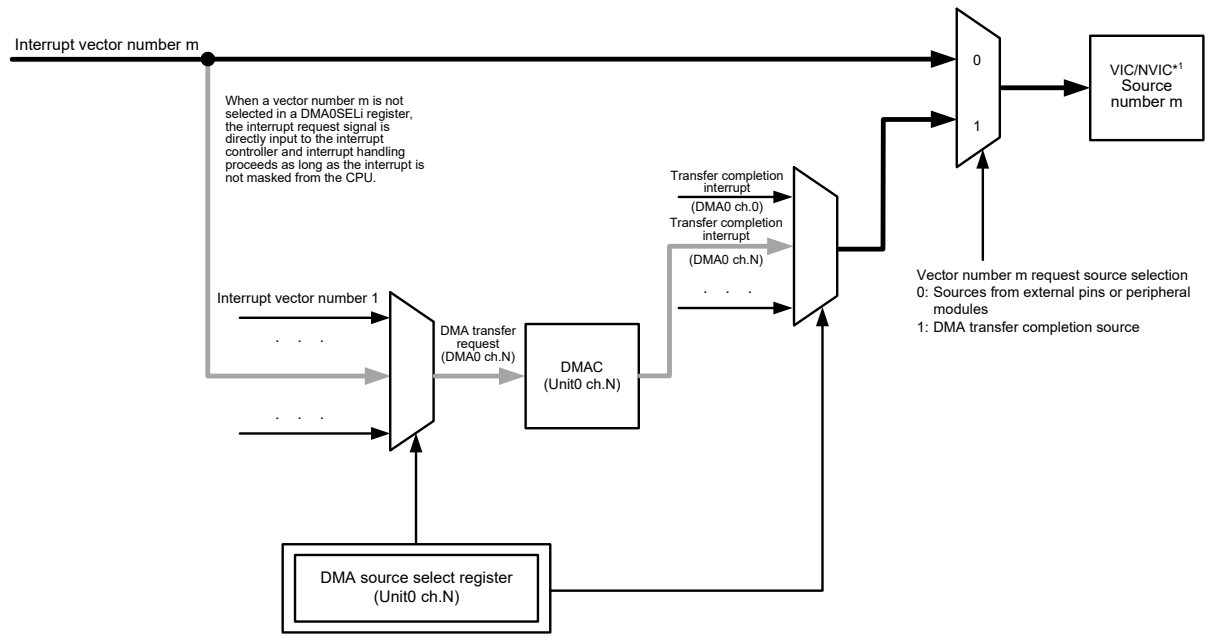
Note 1. NVIC is included only in products incorporating an R-IN engine.

Note: When the DMAC is selected as the destination for an interrupt request with vector number m, the DMA transfer completion interrupt signal is conveyed to the interrupt controller as the interrupt for vector number m on completion of the DMA transfer. This means that the detection type for an interrupt with vector number m whose destination is set as the DMAC should always be edge-sensing regardless of the vector number.



Note 1. NVIC is included only in products incorporating an R-IN engine.

Figure 12.3 DMAC as the Interrupt Request Destination



Note 1. NVIC is included only in products incorporating an R-IN engine.

Figure 12.4 CPU (Interrupt Controller) as the Interrupt Request Destination

12.3.2 Digital Noise Filter

The digital noise filter function is provided for the external interrupt request IRQi pins (i = 0 to 15), NMI pin interrupts, Ethernet PHY interrupt ETHn_INT pins (n = 0 to 2), and external DMA request DREQm pins (m = 0 to 2).
The digital noise filter samples input signals at the filter sampling clock (PCLKB) and pulses with levels that only match once or twice are removed.
To use the digital noise filter for the IRQi pins (IRQ0 to IRQ15), set the sampling clock cycle (PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64) with the IRQFLTC.FCLKSELi[1:0] bits (IRQ0 to IRQ15), and set the IRQFLTE.FLTENi bits (IRQ0 to IRQ15) to 1.
To use the digital noise filter for the NMI pin interrupt, set the sampling clock cycle (PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64) with the NMICR.NFCLKSEL[1:0] bits, and set the NMICR.NFLTEN bit to 1.
To use the digital noise filter for the Ethernet PHY interrupt ETHn_INT pins (n = 0 to 2), set the sampling clock cycle (PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64) with the EPHYFLTC.FCLKSELn[1:0] bits (n = 0 to 2), and set the EPHYFLTE.FLTENn bits (n = 0 to 2) to 1.
To use the digital noise filter for the external DMA request DREQm pins (m = 0 to 2), set the sampling clock cycle (PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64) with the DREQFLTC.DRmFCLKSEL[1:0] bits (m = 0 to 2), and set the DREQFLTE.DRmFLTEN bits (m = 0 to 2) to 1.
Figure 12.5 shows an example of digital noise filter operation.

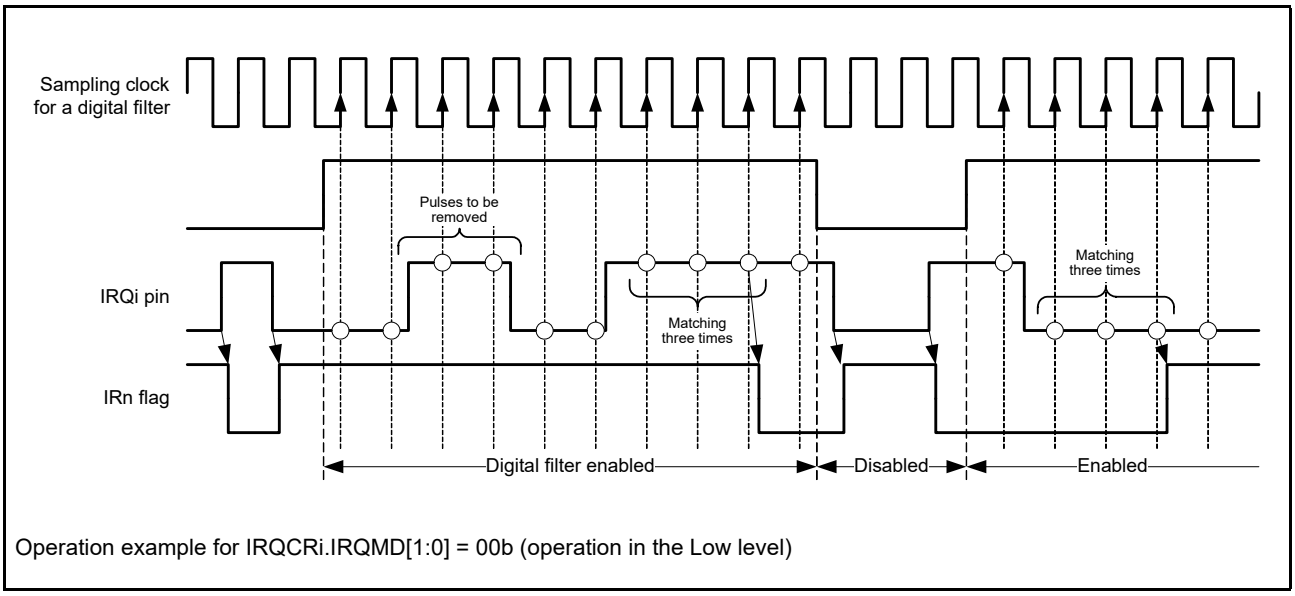


Figure 12.5 Digital Noise Filter Operation Example

12.3.3 External Pin Interrupts

The procedure for connecting an external pin interrupt to Cortex-R4 is shown below. For details on VIC, see section 12.4, Cortex-R4 Vector Interrupt Controller (VIC). To use the external pins at their falling edges or rising and falling edges, see section 12.6.1, Using “Falling-Edge” or “Rising and Falling Edges” Detection with the External Pin Interrupts.
For details on exception handing of Cortex-M3 (for products incorporating an R-IN engine), visit the following URL of Arm:
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

[For IRQ pins]

1. Clear the applicable IENn bit to 0 (set the IECn bit).
2. Clear the IRQFLTE.FLTENi bit to 0.*1
3. Set the digital noise filter sampling clock with the IRQFLTC.FCLKSEL[1:0] bits.*1
4. Set the Pmn I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).
5. Set the I/O port (PmnPFS.ISEL bit).
6. Set the method of detection with the IRQCRi.IRQMD[1:0] bits.
7. Set the IRQFLTE.FLTENi bit to 1.*1
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. This setting is only required when the digital noise filter is to be used.

[For ETH0_INT/ETH1_INT/ETH2_INT]

1. Set the applicable IENn bit to 0 (set the IECn bit).
2. Clear the EPHYFLTE.EFLTENi bit to 0.*1
3. Set the digital noise filter sampling clock with the EPHYFLTC.EFCLKSEL[1:0] bits.*1
4. Set the Pmn I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).
5. Set the I/O port (the PmnPFS.PSEL[5:0] bits and PMR register).
6. Set the method of detection with the EPHYCRi.EPHYMD[1:0] bits.
7. Set the EPHYFLTE.EFLTENi bit to 1.*1
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. This setting is only required when the digital noise filter is to be used.

12.3.4 NMI Pin Interrupts

Pins that can be used as NMI pins serve as general I/O ports after a reset. To use them as NMI pins, the following procedure is required.
Note that setting these pins to serve as general I/O ports after setting them to serve as the NMI pins is prohibited. To use the NMI pins at their falling edges, see section 12.6.2, Using Falling-Edge Detection with the NMI Pin.

1. Set the NMIFLTE.NFLTEN bit to 0.*1
2. Set the sampling clock of the digital noise filter with the NMIFLTC.NFCLKSEL[1:0] bits.*1
3. Set edge detection with the NMICR.NMIMD bit.
4. Set the NMICLR.NMICLR bit to 1 and clear the NMISR.NMIST flag to 0.
5. Set the NMIFLTE.NFLTEN bit to 1.*1
6. Set the P35 I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).
7. Set the I/O port (P35PFS.ISEL bit) and confirm the setting.

Note 1. This setting is only required when the digital noise filter is to be used.

12.4 Cortex-R4 Vector Interrupt Controller (VIC)

12.4.1 Overview

The RZ/T1 has the vector interrupt controller (VIC) to control interrupts for Cortex-R4. Non-maskable interrupt requests from the NMI pin or ECM are treated as FIQ interrupts and are always accepted at high-speed. Interrupts from external pins other than the NMI pin and those from on-chip peripheral modules are accepted as IRQ interrupts (maskable interrupts). The vector addresses of the individual IRQ interrupt sources are stored in the interrupt address storage registers (VADn). When an IRQ interrupt occurs, the interrupt controller provides the Cortex-R4 with the address in VADn as the destination for branching, so the program counter directly branches to the address set in VADn.

12.4.2 Register Descriptions

12.4.2.1 IRQ Status Register n (IRQSn) (n = 0 to 9)

The IRQSn (n = 0 to 9) register indicates the interrupt status after IRQ interrupt mask. This register is enabled when an interrupt is enabled (IENn = 1). Interrupt status is not reflected when an interrupt is disabled (IENn = 0).
This register can only be read in 32-bit units.
Before completing the level interrupt, use the register to make sure no interrupt is requested. (See section 12.4.4.3, (2) IRQ Interrupt (Level interrupt)).

- IRQS0

Address(es): VIC.IRQS0 A001 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ31	IRQ30	IRQ29	IRQ28	IRQ27	IRQ26	IRQ25	IRQ24	IRQ23	IRQ22	IRQ21	IRQ20	IRQ19	IRQ18	IRQ17	IRQ16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b31 to b1	IRQ[31:1]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

- IRQS1

Address(es): VIC.IRQS1 A001 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ63	IRQ62	IRQ61	IRQ60	IRQ59	IRQ58	IRQ57	IRQ56	IRQ55	IRQ54	IRQ53	IRQ52	IRQ51	IRQ50	IRQ49	IRQ48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ47	IRQ46	IRQ45	IRQ44	IRQ43	IRQ42	IRQ41	IRQ40	IRQ39	IRQ38	IRQ37	IRQ36	IRQ35	IRQ34	IRQ33	IRQ32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[63:32]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

IRQi Flag (Interrupt Status Flag) (i = 1 to 63)

This flag indicates the interrupt status after interrupt mask by the IEN registers.

- IRQS2

Address(es): VIC.IRQS2 A001 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ95	IRQ94	IRQ93	IRQ92	IRQ91	IRQ90	IRQ89	IRQ88	IRQ87	IRQ86	IRQ85	IRQ84	IRQ83	IRQ82	IRQ81	IRQ80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ79	IRQ78	IRQ77	IRQ76	IRQ75	IRQ74	IRQ73	IRQ72	IRQ71	IRQ70	IRQ69	IRQ68	IRQ67	IRQ66	IRQ65	IRQ64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[95:64]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

- IRQS3

Address(es): VIC.IRQS3 A001 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ127	IRQ126	IRQ125	IRQ124	IRQ123	IRQ122	IRQ121	IRQ120	IRQ119	IRQ118	IRQ117	IRQ116	IRQ115	IRQ114	IRQ113	IRQ112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ111	IRQ110	IRQ109	IRQ108	IRQ107	IRQ106	IRQ105	IRQ104	IRQ103	IRQ102	IRQ101	IRQ100	IRQ99	IRQ98	IRQ97	IRQ96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[127:96]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

IRQi Flag (Interrupt Status Flag) (i = 64 to 127)

This flag indicates the interrupt status after interrupt mask by the IEN registers.

- IRQS4

Address(es): VIC.IRQS4 A001 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ159	IRQ158	IRQ157	IRQ156	IRQ155	IRQ154	IRQ153	IRQ152	IRQ151	IRQ150	IRQ149	IRQ148	IRQ147	IRQ146	IRQ145	IRQ144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ143	IRQ142	IRQ141	IRQ140	IRQ139	IRQ138	IRQ137	IRQ136	IRQ135	IRQ134	IRQ133	IRQ132	IRQ131	IRQ130	IRQ129	IRQ128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[159:128]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

- IRQS5

Address(es): VIC.IRQS5 A001 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ191	IRQ190	IRQ189	IRQ188	IRQ187	IRQ186	IRQ185	IRQ184	IRQ183	IRQ182	IRQ181	IRQ180	IRQ179	IRQ178	IRQ177	IRQ176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ175	IRQ174	IRQ173	IRQ172	IRQ171	IRQ170	IRQ169	IRQ168	IRQ167	IRQ166	IRQ165	IRQ164	IRQ163	IRQ162	IRQ161	IRQ160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[191:160]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

IRQi Flag (Interrupt Status Flag) (i = 128 to 191)

This flag indicates the interrupt status after interrupt mask by the IEN registers.

- IRQS6

Address(es): VIC.IRQS6 A001 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ223	IRQ222	IRQ221	IRQ220	IRQ219	IRQ218	IRQ217	IRQ216	IRQ215	IRQ214	IRQ213	IRQ212	IRQ211	IRQ210	IRQ209	IRQ208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ207	IRQ206	IRQ205	IRQ204	IRQ203	IRQ202	IRQ201	IRQ200	IRQ199	IRQ198	IRQ197	IRQ196	IRQ195	IRQ194	IRQ193	IRQ192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[223:192]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

- IRQS7

Address(es): VIC.IRQS7 A001 001Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ255	IRQ254	IRQ253	IRQ252	IRQ251	IRQ250	IRQ249	IRQ248	IRQ247	IRQ246	IRQ245	IRQ244	IRQ243	IRQ242	IRQ241	IRQ240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ239	IRQ238	IRQ237	IRQ236	IRQ235	IRQ234	IRQ233	IRQ232	IRQ231	IRQ230	IRQ229	IRQ228	IRQ227	IRQ226	IRQ225	IRQ224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[255:224]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

IRQi Flag (Interrupt Status Flag) (i = 192 to 255)

This flag indicates the interrupt status after interrupt mask by the IEN registers.

- IRQS8

Address(es): VIC.IRQS8 A001 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IRQ287	IRQ286	IRQ285	IRQ284	IRQ283	IRQ282	IRQ281	IRQ280	IRQ279	IRQ278	IRQ277	IRQ276	IRQ275	IRQ274	IRQ273	IRQ272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQ271	IRQ270	IRQ269	IRQ268	IRQ267	IRQ266	IRQ265	IRQ264	IRQ263	IRQ262	IRQ261	IRQ260	IRQ259	IRQ258	IRQ257	IRQ256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IRQ[287:256]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R

- IRQS9

Address(es): VIC.IRQS9 A001 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IRQ300	IRQ299	IRQ298	IRQ297	IRQ296	IRQ295	IRQ294	IRQ293	IRQ292	IRQ291	IRQ290	IRQ289	IRQ288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	IRQ[300:288]	Interrupt Status Flag	0: IRQ interrupt is not requested. 1: IRQ interrupt is requested.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

IRQi Flag (Interrupt Status Flag) (i = 256 to 300)

This flag indicates the interrupt status after interrupt mask by the IEN registers.

12.4.2.2 Interrupt Input Status Register n (RAISn) (n = 0 to 9)

The RAISn (n = 0 to 9) register indicates the interrupt input status before IRQ (maskable) interrupt mask. The interrupt status is reflected to this register regardless of the IENn register setting (interrupt enabled or disabled).
This register can only be read in 32-bit units. The states of an interrupt source can be confirmed while the interrupt is disabled (the corresponding bit in IENn is 0) by, for example, polling the source bit (see section 12.4.4.6, Handling IRQ Interrupt Source Conditions by Polling).

- RAIS0

Address(es): VIC.RAIS0 A001 0040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI31	RAI30	RAI29	RAI28	RAI27	RAI26	RAI25	RAI24	RAI23	RAI22	RAI21	RAI20	RAI19	RAI18	RAI17	RAI16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI15	RAI14	RAI13	RAI12	RAI11	RAI10	RAI9	RAI8	RAI7	RAI6	RAI5	RAI4	RAI3	RAI2	RAI1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b31 to b1	RAI[31:1]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

- RAIS1

Address(es): VIC.RAIS1 A001 0044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI63	RAI62	RAI61	RAI60	RAI59	RAI58	RAI57	RAI56	RAI55	RAI54	RAI53	RAI52	RAI51	RAI50	RAI49	RAI48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI47	RAI46	RAI45	RAI44	RAI43	RAI42	RAI41	RAI40	RAI39	RAI38	RAI37	RAI36	RAI35	RAI34	RAI33	RAI32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[63:32]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

RAIi Flag (Interrupt Input Status Flag) (i = 1 to 63)

This flag indicates the interrupt request input status before interrupt mask.

- RAIS2

Address(es): VIC.RAIS2 A001 0048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI95	RAI94	RAI93	RAI92	RAI91	RAI90	RAI89	RAI88	RAI87	RAI86	RAI85	RAI84	RAI83	RAI82	RAI81	RAI80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI79	RAI78	RAI77	RAI76	RAI75	RAI74	RAI73	RAI72	RAI71	RAI70	RAI69	RAI68	RAI67	RAI66	RAI65	RAI64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[95:64]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

- RAIS3

Address(es): VIC.RAIS3 A001 004Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI127	RAI126	RAI125	RAI124	RAI123	RAI122	RAI121	RAI120	RAI119	RAI118	RAI117	RAI116	RAI115	RAI114	RAI113	RAI112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI111	RAI110	RAI109	RAI108	RAI107	RAI106	RAI105	RAI104	RAI103	RAI102	RAI101	RAI100	RAI99	RAI98	RAI97	RAI96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[127:96]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

RAIi Flag (Interrupt Input Status Flag) (i = 64 to 127)

This flag indicates the interrupt request input status before interrupt mask.

- RAIS4

Address(es): VIC.RAIS4 A001 0050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI159	RAI158	RAI157	RAI156	RAI155	RAI154	RAI153	RAI152	RAI151	RAI150	RAI149	RAI148	RAI147	RAI146	RAI145	RAI144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI143	RAI142	RAI141	RAI140	RAI139	RAI138	RAI137	RAI136	RAI135	RAI134	RAI133	RAI132	RAI131	RAI130	RAI129	RAI128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[159:128]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

- RAIS5

Address(es): VIC.RAIS5 A001 0054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI191	RAI190	RAI189	RAI188	RAI187	RAI186	RAI185	RAI184	RAI183	RAI182	RAI181	RAI180	RAI179	RAI178	RAI177	RAI176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI175	RAI174	RAI173	RAI172	RAI171	RAI170	RAI169	RAI168	RAI167	RAI166	RAI165	RAI164	RAI163	RAI162	RAI161	RAI160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[191:160]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

RAIi Flag (Interrupt Input Status Flag) (i = 128 to 191)

This flag indicates the interrupt request input status before interrupt mask.

- RAIS6

Address(es): VIC.RAIS6 A001 0058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI223	RAI222	RAI221	RAI220	RAI219	RAI218	RAI217	RAI216	RAI215	RAI214	RAI213	RAI212	RAI211	RAI210	RAI209	RAI208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI207	RAI206	RAI205	RAI204	RAI203	RAI202	RAI201	RAI200	RAI199	RAI198	RAI197	RAI196	RAI195	RAI194	RAI193	RAI192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[223:192]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

- RAIS7

Address(es): VIC.RAIS7 A001 005Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI255	RAI254	RAI253	RAI252	RAI251	RAI250	RAI249	RAI248	RAI247	RAI246	RAI245	RAI244	RAI243	RAI242	RAI241	RAI240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI239	RAI238	RAI237	RAI236	RAI235	RAI234	RAI233	RAI232	RAI231	RAI230	RAI229	RAI228	RAI227	RAI226	RAI225	RAI224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[255:224]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

RAIi Flag (Interrupt Input Status Flag) (i = 192 to 255)

This flag indicates the interrupt request input status before interrupt mask.

- RAIS8

Address(es): VIC.RAIS8 A001 1040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RAI287	RAI286	RAI285	RAI284	RAI283	RAI282	RAI281	RAI280	RAI279	RAI278	RAI277	RAI276	RAI275	RAI274	RAI273	RAI272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RAI271	RAI270	RAI269	RAI268	RAI267	RAI266	RAI265	RAI264	RAI263	RAI262	RAI261	RAI260	RAI259	RAI258	RAI257	RAI256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RAI[287:256]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R

- RAIS9

Address(es): VIC.RAIS9 A001 1044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RAI300	RAI299	RAI298	RAI297	RAI296	RAI295	RAI294	RAI293	RAI292	RAI291	RAI290	RAI289	RAI288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	RAI[300:288]	Interrupt Input Status Flag	0: Interrupt is not requested. 1: Interrupt is requested.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

RAIi Flag (Interrupt Input Status Flag) (i = 256 to 300)

This flag indicates the interrupt request input status before interrupt mask.

12.4.2.3 Interrupt Enable Register n (IENn) (n = 0 to 9)

The IENn (n = 0 to 9) register enables or masks IRQ interrupts. When it is reset, all interrupt requests are masked. When a bit of this register is set to 1, it cannot be cleared to 0. To clear the bit to 0, use interrupt enable clear register n (IECn).

This register can only be read and written in 32-bit units.

- IEN0

Address(es): VIC.IEN0 A001 0080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN31	IEN30	IEN29	IEN28	IEN27	IEN26	IEN25	IEN24	IEN23	IEN22	IEN21	IEN20	IEN19	IEN18	IEN17	IEN16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R/W
b31 to b1	IEN[31:1]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

- IEN1

Address(es): VIC.IEN1 A001 0084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN63	IEN62	IEN61	IEN60	IEN59	IEN58	IEN57	IEN56	IEN55	IEN54	IEN53	IEN52	IEN51	IEN50	IEN49	IEN48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN47	IEN46	IEN45	IEN44	IEN43	IEN42	IEN41	IEN40	IEN39	IEN38	IEN37	IEN36	IEN35	IEN34	IEN33	IEN32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[63:32]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

IENi Bit (Interrupt Request Enable) (i = 1 to 63)

This bit specifies interrupt request enable settings. When the bit is enabled, it cannot be masked with the IENn register. Perform interrupt mask with the IECn register.

- IEN2

Address(es): VIC.IEN2 A001 0088h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN95	IEN94	IEN93	IEN92	IEN91	IEN90	IEN89	IEN88	IEN87	IEN86	IEN85	IEN84	IEN83	IEN82	IEN81	IEN80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN79	IEN78	IEN77	IEN76	IEN75	IEN74	IEN73	IEN72	IEN71	IEN70	IEN69	IEN68	IEN67	IEN66	IEN65	IEN64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[95:64]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

- IEN3

Address(es): VIC.IEN3 A001 008Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN127	IEN126	IEN125	IEN124	IEN123	IEN122	IEN121	IEN120	IEN119	IEN118	IEN117	IEN116	IEN115	IEN114	IEN113	IEN112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN111	IEN110	IEN109	IEN108	IEN107	IEN106	IEN105	IEN104	IEN103	IEN102	IEN101	IEN100	IEN99	IEN98	IEN97	IEN96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[127:96]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

IENi Bit (Interrupt Request Enable) (i = 64 to 127)

This bit specifies interrupt request enable settings. When the bit is enabled, it cannot be masked with the IENn register. Perform interrupt mask with the IECn register.

- IEN4

Address(es): VIC.IEN4 A001 0090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN159	IEN158	IEN157	IEN156	IEN155	IEN154	IEN153	IEN152	IEN151	IEN150	IEN149	IEN148	IEN147	IEN146	IEN145	IEN144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN143	IEN142	IEN141	IEN140	IEN139	IEN138	IEN137	IEN136	IEN135	IEN134	IEN133	IEN132	IEN131	IEN130	IEN129	IEN128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[159:128]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

- IEN5

Address(es): VIC.IEN5 A001 0094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN191	IEN190	IEN189	IEN188	IEN187	IEN186	IEN185	IEN184	IEN183	IEN182	IEN181	IEN180	IEN179	IEN178	IEN177	IEN176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN175	IEN174	IEN173	IEN172	IEN171	IEN170	IEN169	IEN168	IEN167	IEN166	IEN165	IEN164	IEN163	IEN162	IEN161	IEN160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[191:160]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

IENi Bit (Interrupt Request Enable) (i = 128 to 191)

This bit specifies interrupt request enable settings. When the bit is enabled, it cannot be masked with the IENn register. Perform interrupt mask with the IECn register.

- IEN6

Address(es): VIC.IEN6 A001 0098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN223	IEN222	IEN221	IEN220	IEN219	IEN218	IEN217	IEN216	IEN215	IEN214	IEN213	IEN212	IEN211	IEN210	IEN209	IEN208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN207	IEN206	IEN205	IEN204	IEN203	IEN202	IEN201	IEN200	IEN199	IEN198	IEN197	IEN196	IEN195	IEN194	IEN193	IEN192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[223:192]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

- IEN7

Address(es): VIC.IEN7 A001 009Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN255	IEN254	IEN253	IEN252	IEN251	IEN250	IEN249	IEN248	IEN247	IEN246	IEN245	IEN244	IEN243	IEN242	IEN241	IEN240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN239	IEN238	IEN237	IEN236	IEN235	IEN234	IEN233	IEN232	IEN231	IEN230	IEN229	IEN228	IEN227	IEN226	IEN225	IEN224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[255:224]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

IENi Bit (Interrupt Request Enable) (i = 192 to 255)

This bit specifies interrupt request enable settings. When the bit is enabled, it cannot be masked with the IENn register. Perform interrupt mask with the IECn register.

- IEN8

Address(es): VIC.IEN8 A001 1080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEN287	IEN286	IEN285	IEN284	IEN283	IEN282	IEN281	IEN280	IEN279	IEN278	IEN277	IEN276	IEN275	IEN274	IEN273	IEN272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEN271	IEN270	IEN269	IEN268	IEN267	IEN266	IEN265	IEN264	IEN263	IEN262	IEN261	IEN260	IEN259	IEN258	IEN257	IEN256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEN[287:256]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W

- IEN9

Address(es): VIC.IEN9 A001 1084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IEN300	IEN299	IEN298	IEN297	IEN296	IEN295	IEN294	IEN293	IEN292	IEN291	IEN290	IEN289	IEN288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	IEN[300:288]	Interrupt Request Enable	0: Interrupt is masked (disabled). 1: Interrupt is enabled.	R/W
b31 to b13	—	Reserved	These bits are always read as 0. When written, always write 0.	R/W

IENi Bit (Interrupt Request Enable) (i = 256 to 300)

This bit specifies interrupt request enable settings. When the bit is enabled, it cannot be masked with the IENn register. Perform interrupt mask with the IECn register.

12.4.2.4 Interrupt Enable Clear Register n (IECn) (n = 0 to 9)

The IECn (n = 0 to 9) register clears a bit of the IENn register, and masks (disables) the applicable interrupt request. This register can only be written in 32-bit units.

If the value of the IECn register is to be changed, do so while interrupts are disabled. To disable interrupts, set the I bit in the CPSR register of the Arm CPU to 1.

- IEC0

Address(es): VIC.IEC0 A001 00A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC31	IEC30	IEC29	IEC28	IEC27	IEC26	IEC25	IEC24	IEC23	IEC22	IEC21	IEC20	IEC19	IEC18	IEC17	IEC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC15	IEC14	IEC13	IEC12	IEC11	IEC10	IEC9	IEC8	IEC7	IEC6	IEC5	IEC4	IEC3	IEC2	IEC1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The write value should be 0.	W
b31 to b1	IEC[31:1]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

- IEC1

Address(es): VIC.IEC1 A001 00A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC63	IEC62	IEC61	IEC60	IEC59	IEC58	IEC57	IEC56	IEC55	IEC54	IEC53	IEC52	IEC51	IEC50	IEC49	IEC48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC47	IEC46	IEC45	IEC44	IEC43	IEC42	IEC41	IEC40	IEC39	IEC38	IEC37	IEC36	IEC35	IEC34	IEC33	IEC32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[63:32]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

IECi Bit (Interrupt Request Clear) (i = 1 to 63)

This bit specifies settings for masking (disabling) interrupt requests. When 1 is set to a bit, the same bit of the IEN register is cleared to 0, and the interrupt request is masked (disabled).

- IEC2

Address(es): VIC.IEC2 A001 00A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC95	IEC94	IEC93	IEC92	IEC91	IEC90	IEC89	IEC88	IEC87	IEC86	IEC85	IEC84	IEC83	IEC82	IEC81	IEC80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC79	IEC78	IEC77	IEC76	IEC75	IEC74	IEC73	IEC72	IEC71	IEC70	IEC69	IEC68	IEC67	IEC66	IEC65	IEC64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[95:64]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

- IEC3

Address(es): VIC.IEC3 A001 00ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC127	IEC126	IEC125	IEC124	IEC123	IEC122	IEC121	IEC120	IEC119	IEC118	IEC117	IEC116	IEC115	IEC114	IEC113	IEC112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC111	IEC110	IEC109	IEC108	IEC107	IEC106	IEC105	IEC104	IEC103	IEC102	IEC101	IEC100	IEC99	IEC98	IEC97	IEC96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[127:96]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

IECi Bit (Interrupt Request Clear) (i = 64 to 127)

This bit specifies settings for masking (disabling) interrupt requests. When 1 is set to a bit, the same bit of the IEN register is cleared to 0, and the interrupt request is masked (disabled).

- IEC4

Address(es): VIC.IEC4 A001 00B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC159	IEC158	IEC157	IEC156	IEC155	IEC154	IEC153	IEC152	IEC151	IEC150	IEC149	IEC148	IEC147	IEC146	IEC145	IEC144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC143	IEC142	IEC141	IEC140	IEC139	IEC138	IEC137	IEC136	IEC135	IEC134	IEC133	IEC132	IEC131	IEC130	IEC129	IEC128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[159:128]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

- IEC5

Address(es): VIC.IEC5 A001 00B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC191	IEC190	IEC189	IEC188	IEC187	IEC186	IEC185	IEC184	IEC183	IEC182	IEC181	IEC180	IEC179	IEC178	IEC177	IEC176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC175	IEC174	IEC173	IEC172	IEC171	IEC170	IEC169	IEC168	IEC167	IEC166	IEC165	IEC164	IEC163	IEC162	IEC161	IEC160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[191:160]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

IECi Bit (Interrupt Request Clear) (i = 128 to 191)

This bit specifies settings for masking (disabling) interrupt requests. When 1 is set to a bit, the same bit of the IEN register is cleared to 0, and the interrupt request is masked (disabled).

- IEC6

Address(es): VIC.IEC6 A001 00B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC223	IEC222	IEC221	IEC220	IEC219	IEC218	IEC217	IEC216	IEC215	IEC214	IEC213	IEC212	IEC211	IEC210	IEC209	IEC208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC207	IEC206	IEC205	IEC204	IEC203	IEC202	IEC201	IEC200	IEC199	IEC198	IEC197	IEC196	IEC195	IEC194	IEC193	IEC192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[223:192]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

- IEC7

Address(es): VIC.IEC7 A001 00BCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC255	IEC254	IEC253	IEC252	IEC251	IEC250	IEC249	IEC248	IEC247	IEC246	IEC245	IEC244	IEC243	IEC242	IEC241	IEC240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC239	IEC238	IEC237	IEC236	IEC235	IEC234	IEC233	IEC232	IEC231	IEC230	IEC229	IEC228	IEC227	IEC226	IEC225	IEC224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[255:224]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

IECi Bit (Interrupt Request Clear) (i = 192 to 255)

This bit specifies settings for masking (disabling) interrupt requests. When 1 is set to a bit, the same bit of the IEN register is cleared to 0, and the interrupt request is masked (disabled).

- IEC8

Address(es): VIC.IEC8 A001 10A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IEC287	IEC286	IEC285	IEC284	IEC283	IEC282	IEC281	IEC280	IEC279	IEC278	IEC277	IEC276	IEC275	IEC274	IEC273	IEC272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IEC271	IEC270	IEC269	IEC268	IEC267	IEC266	IEC265	IEC264	IEC263	IEC262	IEC261	IEC260	IEC259	IEC258	IEC257	IEC256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	IEC[287:256]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W

- IEC9

Address(es): VIC.IEC9 A001 10A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IEC300	IEC299	IEC298	IEC297	IEC296	IEC295	IEC294	IEC293	IEC292	IEC291	IEC290	IEC289	IEC288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	IEC[300:288]	Interrupt Request Clear	0: Nothing is changed. 1: The applicable bit of the IEN register of which interrupt is masked (disabled) is cleared to 0.	W
b31 to b13	—	Reserved	The write value should be 0.	W

IECi Bit (Interrupt Request Clear) (i = 256 to 300)

This bit specifies settings for masking (disabling) interrupt requests. When 1 is set to a bit, the same bit of the IEN register is cleared to 0, and the interrupt request is masked (disabled).

12.4.2.5 Interrupt Detection Type Selection Register n (PLSn) (n = 0 to 9)

The PLSn (n = 0 to 9) register detects the edge or level for each interrupt input.
This register can only be read and written in 32-bit units.

- PLS0

Address(es): VIC.PLS0 A001 0100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS31	PLS30	PLS29	PLS28	PLS27	PLS26	PLS25	PLS24	PLS23	PLS22	PLS21	PLS20	PLS19	PLS18	PLS17	PLS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS15	PLS14	PLS13	PLS12	PLS11	PLS10	PLS9	PLS8	PLS7	PLS6	PLS5	PLS4	PLS3	PLS2	PLS1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b1	PLS[31:1]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

- PLS1

Address(es): VIC.PLS1 A001 0104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS63	PLS62	PLS61	PLS60	PLS59	PLS58	PLS57	PLS56	PLS55	PLS54	PLS53	PLS52	PLS51	PLS50	PLS49	PLS48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS47	PLS46	PLS45	PLS44	PLS43	PLS42	PLS41	PLS40	PLS39	PLS38	PLS37	PLS36	PLS35	PLS34	PLS33	PLS32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[63:32]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

PLSi Bit (Interrupt Input Detection Type Selection) (i = 1 to 63)

This bit selects the interrupt input detection type.
PLS[63:1] corresponds to vector numbers 63 to 1.

- PLS2

Address(es): VIC.PLS2 A001 0108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS95	PLS94	PLS93	PLS92	PLS91	PLS90	PLS89	PLS88	PLS87	PLS86	PLS85	PLS84	PLS83	PLS82	PLS81	PLS80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS79	PLS78	PLS77	PLS76	PLS75	PLS74	PLS73	PLS72	PLS71	PLS70	PLS69	PLS68	PLS67	PLS66	PLS65	PLS64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[95:64]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

- PLS3

Address(es): VIC.PLS3 A001 010Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS127	PLS126	PLS125	PLS124	PLS123	PLS122	PLS121	PLS120	PLS119	PLS118	PLS117	PLS116	PLS115	PLS114	PLS113	PLS112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS111	PLS110	PLS109	PLS108	PLS107	PLS106	PLS105	PLS104	PLS103	PLS102	PLS101	PLS100	PLS99	PLS98	PLS97	PLS96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[127:96]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

PLSi Bit (Interrupt Input Detection Type Selection) (i = 64 to 127)

This bit selects the interrupt input detection type.

PLS[127:64] corresponds to vector numbers 127 to 64.

- PLS4

Address(es): VIC.PLS4 A001 0110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS159	PLS158	PLS157	PLS156	PLS155	PLS154	PLS153	PLS152	PLS151	PLS150	PLS149	PLS148	PLS147	PLS146	PLS145	PLS144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS143	PLS142	PLS141	PLS140	PLS139	PLS138	PLS137	PLS136	PLS135	PLS134	PLS133	PLS132	PLS131	PLS130	PLS129	PLS128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[159:128]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

- PLS5

Address(es): VIC.PLS5 A001 0114h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS191	PLS190	PLS189	PLS188	PLS187	PLS186	PLS185	PLS184	PLS183	PLS182	PLS181	PLS180	PLS179	PLS178	PLS177	PLS176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS175	PLS174	PLS173	PLS172	PLS171	PLS170	PLS169	PLS168	PLS167	PLS166	PLS165	PLS164	PLS163	PLS162	PLS161	PLS160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[191:160]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

PLSi Bit (Interrupt Input Detection Type Selection) (i = 128 to 191)

This bit selects the interrupt input detection type.

PLS[191:128] corresponds to vector numbers 191 to 128.

- PLS6

Address(es): VIC.PLS6 A001 0118h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS223	PLS222	PLS221	PLS220	PLS219	PLS218	PLS217	PLS216	PLS215	PLS214	PLS213	PLS212	PLS211	PLS210	PLS209	PLS208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS207	PLS206	PLS205	PLS204	PLS203	PLS202	PLS201	PLS200	PLS199	PLS198	PLS197	PLS196	PLS195	PLS194	PLS193	PLS192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[223:192]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

- PLS7

Address(es): VIC.PLS7 A001 011Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS255	PLS254	PLS253	PLS252	PLS251	PLS250	PLS249	PLS248	PLS247	PLS246	PLS245	PLS244	PLS243	PLS242	PLS241	PLS240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS239	PLS238	PLS237	PLS236	PLS235	PLS234	PLS233	PLS232	PLS231	PLS230	PLS229	PLS228	PLS227	PLS226	PLS225	PLS224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[255:224]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

PLSi Bit (Interrupt Input Detection Type Selection) (i = 192 to 255)

This bit selects the interrupt input detection type.

PLS[255:192] corresponds to vector numbers 255 to 192.

- PLS8

Address(es): VIC.PLS8 A001 1100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PLS287	PLS286	PLS285	PLS284	PLS283	PLS282	PLS281	PLS280	PLS279	PLS278	PLS277	PLS276	PLS275	PLS274	PLS273	PLS272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PLS271	PLS270	PLS269	PLS268	PLS267	PLS266	PLS265	PLS264	PLS263	PLS262	PLS261	PLS260	PLS259	PLS258	PLS257	PLS256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PLS[287:256]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W

- PLS9

Address(es): VIC.PLS9 A001 1104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PLS300	PLS299	PLS298	PLS297	PLS296	PLS295	PLS294	PLS293	PLS292	PLS291	PLS290	PLS289	PLS288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	PLS[300:288]	Interrupt Input Detection Type Selection	0: Detects the level. 1: Detects the edge.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PLSi Bit (Interrupt Input Detection Type Selection) (i = 256 to 300)

This bit selects the interrupt input detection type.

PLS[300:256] corresponds to vector numbers 300 to 256.

12.4.2.6 Edge Detection Bit Clear Register n (PICn) (n = 0 to 9)

If you detect an edge, the interrupt detection status is retained for each interrupt input bit (See section 12.4, Cortex-R4 Vector Interrupt Controller (VIC) and section 12.4.4.3, (3) IRQ Interrupt (Edge Interrupt)).
The PICn (n = 0 to 9) register clears the edge detection circuit for the interrupt input bit of which edge was detected to 0. This register can only be written in 32-bit units.

- PIC0

Address(es): VIC.PIC0 A001 0120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC31	PIC30	PIC29	PIC28	PIC27	PIC26	PIC25	PIC24	PIC23	PIC22	PIC21	PIC20	PIC19	PIC18	PIC17	PIC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC15	PIC14	PIC13	PIC12	PIC11	PIC10	PIC9	PIC8	PIC7	PIC6	PIC5	PIC4	PIC3	PIC2	PIC1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The write value should be 0.	W
b31 to b1	PIC[31:1]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

- PIC1

Address(es): VIC.PIC1 A001 0124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC63	PIC62	PIC61	PIC60	PIC59	PIC58	PIC57	PIC56	PIC55	PIC54	PIC53	PIC52	PIC51	PIC50	PIC49	PIC48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC47	PIC46	PIC45	PIC44	PIC43	PIC42	PIC41	PIC40	PIC39	PIC38	PIC37	PIC36	PIC35	PIC34	PIC33	PIC32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[63:32]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

PICi Bit (Edge Detection Clear) (i = 1 to 63)

For interrupt requests of which edges were detected, this bit clears the edge detection circuit for each interrupt request.

- PIC2

Address(es): VIC.PIC2 A001 0128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC95	PIC94	PIC93	PIC92	PIC91	PIC90	PIC89	PIC88	PIC87	PIC86	PIC85	PIC84	PIC83	PIC82	PIC81	PIC80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC79	PIC78	PIC77	PIC76	PIC75	PIC74	PIC73	PIC72	PIC71	PIC70	PIC69	PIC68	PIC67	PIC66	PIC65	PIC64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[95:64]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

- PIC3

Address(es): VIC.PIC3 A001 012Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC127	PIC126	PIC125	PIC124	PIC123	PIC122	PIC121	PIC120	PIC119	PIC118	PIC117	PIC116	PIC115	PIC114	PIC113	PIC112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC111	PIC110	PIC109	PIC108	PIC107	PIC106	PIC105	PIC104	PIC103	PIC102	PIC101	PIC100	PIC99	PIC98	PIC97	PIC96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[127:96]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

PICi Bit (Edge Detection Clear) (i = 64 to 127)

For interrupt requests of which edges were detected, this bit clears the edge detection circuit for each interrupt request.

- PIC4

Address(es): VIC.PIC4 A001 0130h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC159	PIC158	PIC157	PIC156	PIC155	PIC154	PIC153	PIC152	PIC151	PIC150	PIC149	PIC148	PIC147	PIC146	PIC145	PIC144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC143	PIC142	PIC141	PIC140	PIC139	PIC138	PIC137	PIC136	PIC135	PIC134	PIC133	PIC132	PIC131	PIC130	PIC129	PIC128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[159:128]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

- PIC5

Address(es): VIC.PIC5 A001 0134h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC191	PIC190	PIC189	PIC188	PIC187	PIC186	PIC185	PIC184	PIC183	PIC182	PIC181	PIC180	PIC179	PIC178	PIC177	PIC176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC175	PIC174	PIC173	PIC172	PIC171	PIC170	PIC169	PIC168	PIC167	PIC166	PIC165	PIC164	PIC163	PIC162	PIC161	PIC160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[191:160]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

PICi Bit (Edge Detection Clear) (i = 128 to 191)

For interrupt requests of which edges were detected, this bit clears the edge detection circuit for each interrupt request.

- PIC6

Address(es): VIC.PIC6 A001 0138h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC223	PIC222	PIC221	PIC220	PIC219	PIC218	PIC217	PIC216	PIC215	PIC214	PIC213	PIC212	PIC211	PIC210	PIC209	PIC208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC207	PIC206	PIC205	PIC204	PIC203	PIC202	PIC201	PIC200	PIC199	PIC198	PIC197	PIC196	PIC195	PIC194	PIC193	PIC192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[223:192]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

- PIC7

Address(es): VIC.PIC7 A001 013Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC255	PIC254	PIC253	PIC252	PIC251	PIC250	PIC249	PIC248	PIC247	PIC246	PIC245	PIC244	PIC243	PIC242	PIC241	PIC240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC239	PIC238	PIC237	PIC236	PIC235	PIC234	PIC233	PIC232	PIC231	PIC230	PIC229	PIC228	PIC227	PIC226	PIC225	PIC224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[255:224]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

PICi Bit (Edge Detection Clear) (i = 192 to 255)

For interrupt requests of which edges were detected, this bit clears the edge detection circuit for each interrupt request.

- PIC8

Address(es): VIC.PIC8 A001 1120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PIC287	PIC286	PIC285	PIC284	PIC283	PIC282	PIC281	PIC280	PIC279	PIC278	PIC277	PIC276	PIC275	PIC274	PIC273	PIC272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIC271	PIC270	PIC269	PIC268	PIC267	PIC266	PIC265	PIC264	PIC263	PIC262	PIC261	PIC260	PIC259	PIC258	PIC257	PIC256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PIC[287:256]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W

- PIC9

Address(es): VIC.PIC9 A001 1124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PIC300	PIC299	PIC298	PIC297	PIC296	PIC295	PIC294	PIC293	PIC292	PIC291	PIC290	PIC289	PIC288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	PIC[300:288]	Edge Detection Clear	0: Nothing is changed. 1: Clears edge detection.	W
b31 to b13	—	Reserved	The write value should be 0.	W

PICi Bit (Edge Detection Clear) (i = 256 to 300)

For interrupt requests of which edges were detected, this bit clears the edge detection circuit for each interrupt request.

12.4.2.7 Interrupt Priority Level Mask Register 0 (PRLM0)

The PRLM0 register controls mask for interrupts to the interrupt priority level.
When a bit of this register is set to 1, it cannot be cleared to 0. To clear the bit to 0, use the interrupt priority level mask clear register 0 (PRLC0).
This register can only be read and written in 32-bit units.

Address(es): VIC.PRLM0 A001 01C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRLM15	PRLM14	PRLM13	PRLM12	PRLM11	PRLM10	PRLM9	PRLM8	PRLM7	PRLM6	PRLM5	PRLM4	PRLM3	PRLM2	PRLM1	PRLM0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	PRLM[15:0]	Interrupt Priority Level Setting	0: Nothing is changed. 1: Mask the same priority level as the corresponding bit number.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PRLMi Bit (Interrupt Priority Level Setting) (i = 0 to 15)

This is an interrupt priority level setting bit. For the sources with vector numbers 1 to 255, this bit sets mask of interrupts for the interrupt priority level.
The bit position of the register equals to the applicable priority level. When a bit is set to 1, the same priority level as the corresponding bit number is masked.

12.4.2.8 Interrupt Priority Level Mask Register 1 (PRLM1)

The PRLM1 register controls mask for interrupts to the interrupt priority level.
When a bit of this register is set to 1, it cannot be cleared to 0. To clear the bit to 0, use the interrupt priority level mask clear register 1 (PRLC1).
This register can only be read and written in 32-bit units.

Address(es): VIC.PRLM1 A001 11C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRLM15	PRLM14	PRLM13	PRLM12	PRLM11	PRLM10	PRLM9	PRLM8	PRLM7	PRLM6	PRLM5	PRLM4	PRLM3	PRLM2	PRLM1	PRLM0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	PRLM[15:0]	Interrupt Priority Level Setting	0: Nothing is changed. 1: Mask the same priority level as the corresponding bit number (PRLMi) + 16.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PRLMi Bit (Interrupt Priority Level Setting) (i = 0 to 15)

This is an interrupt priority level setting bit. For the sources with vector numbers 256 to 300, this bit sets mask of interrupts for the interrupt priority level.
When a bit is set to 1, the same priority level as the corresponding bit number (PRLMi) + 16 is masked.

12.4.2.9 Interrupt Priority Level Mask Clear Register 0 (PRLC0)

The PRLC0 register clears each bit of the PRLM0 register to 0.
This register can only be written in 32-bit units.

Address(es): VIC.PRLC0 A001 01C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRLC 15	PRLC 14	PRLC 13	PRLC 12	PRLC 11	PRLC 10	PRLC 9	PRLC8	PRLC7	PRLC6	PRLC5	PRLC4	PRLC3	PRLC2	PRLC1	PRLC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	PRLC[15:0]	Interrupt Priority Level Clear	0: Nothing is changed. 1: The bit corresponding to the bit number is cleared to 0.	W
b31 to b16	—	Reserved	The write value should be 0.	W

PRLCi Bit (Interrupt Priority Level Clear) (i = 0 to 15)

This is an interrupt priority level clear bit. For the sources with vector numbers 1 to 255, this bit clears interrupt priority level mask register 0 (PRLM0) to 0.
Once a bit is set to 1, the bit corresponding to the set bit number is cleared to 0.

12.4.2.10 Interrupt Priority Level Mask Clear Register 1 (PRLC1)

The PRLC1 register clears each bit of the PRLM1 register to 0.
The PRLC1 register can only be written in 32-bit units.

Address(es): VIC.PRLC1 A001 11C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRLC 15	PRLC 14	PRLC 13	PRLC 12	PRLC 11	PRLC 10	PRLC 9	PRLC8	PRLC7	PRLC6	PRLC5	PRLC4	PRLC3	PRLC2	PRLC1	PRLC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	PRLC[15:0]	Interrupt Priority Level Clear	0: Nothing is changed. 1: The bit corresponding to the bit number is cleared to 0.	W
b31 to b16	—	Reserved	The write value should be 0.	W

PRLCi Bit (Interrupt Priority Level Clear) (i = 0 to 15)

This is an interrupt priority level clear bit. For the sources with vector numbers 256 to 300, this bit clears interrupt priority level mask register 1 (PRLM1) to 0.
Once the bit is set to 1, the bit corresponding to the set bit number is cleared to 0.

12.4.2.11 User Mode Enable Register 0 (UEN0)

This register is used to enable or disable access to the interrupt control register (VIC control registers except UEN0 and UEN1 registers) in privilege mode.
When a bus master cannot generate protection information correctly, set the UE bit to 1 to enable access to the interrupt control register in user mode. The initial value of the UE bit is 1 and access to the interrupt control register in user mode is enabled.
The register can be read in 32-bit units.
Unlike other registers, the register can be written in 32-bit units only in privilege mode.

Address VIC.UEN0 A001 01C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UE*1	Interrupt Control Register Access Selection	0: Disables access in user mode. Enables access only in privilege mode. 1: Enables access in user mode. Access to interrupt control register in both user and privilege mode is possible (initial value).	W
b31 to b1	—	Reserved	The write value should be 0.	W

Note 1. Write access to the register is only possible in privilege mode.

UE Bit (Interrupt Control Register Access Selection)

This bit enables or disables access to the interrupt control register for sources corresponding to vector numbers 1 to 255.

12.4.2.12 User Mode Enable Register 1 (UEN1)

This register is used to enable or disable access to the interrupt control register (VIC control registers except UEN0 and UEN1 registers) in privilege mode.

When a bus master cannot generate protection information correctly, set the UE bit to 1 to enable access to the interrupt control register in user mode. The initial value of the UE bit is 1 and access to the interrupt control register in user mode is enabled.

The register can be read in 32-bit units.

Unlike other registers, the register can be written in 32-bit units only in privilege mode.

Address VIC.UEN1 A001 11C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UE*1	Interrupt Control Register Access Selection	0: Disables access in user mode. Enables access only in privilege mode. 1: Enables access in user mode. Access to interrupt control register in both user and privilege mode is possible (initial value).	W
b31 to b1	—	Reserved	The write value should be 0.	W

Note 1. Write access to the register is only possible in privilege mode.

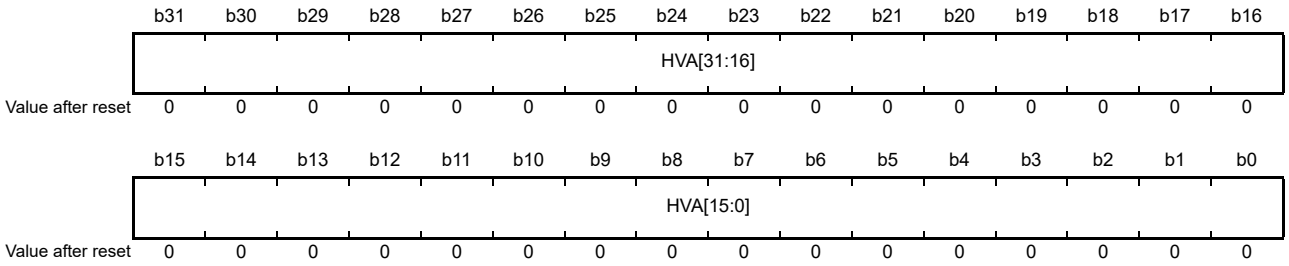
UE Bit (Interrupt Control Register Access Selection)

This bit enables or disables access to the interrupt control register for sources corresponding to vector numbers 256 to 300.

12.4.2.13 Interrupt Address Register (HVA0)

An arbitrary value must be written to the HVA0 register after being released from a reset in order to initialize the VIC. Also, an arbitrary value must be written to the HVA0 register at the end of an interrupt service routine (ISR). Writing to the HVA0 register causes the interrupt controller to recognize the completion of interrupt processing and clear the priority level of the stored interrupt. This leads to the processing of interrupts at the next priority level from that of the interrupt for which processing was just completed. The HVA0 register does not reflect values written to it.
Access to the register for any purpose other than initializing the VIC after it is released from a reset or ending interrupt processing is prohibited and attempting such access may result in incorrect interrupt operations.
This register can only be written in 32-bit units.

Address VIC.HVA0 A001 0200h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	HVA[31:0]	Interrupt Processing Ending Notification	These bits notify an end of interrupt processing (by writing an arbitrary value)	W

12.4.2.14 Interrupt Service Status Register n (ISSn) (n = 0 to 9)

The ISSn (n = 0 to 9) register indicates the service status of an IRQ interrupt.
This register stores information for which Cortex-R4 is executing or suspending an interrupt service routine (ISR).
This register can only be read in 32-bit units.

- ISS0

Address(es): VIC.ISS0 A001 0210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS31	ISS30	ISS29	ISS28	ISS27	ISS26	ISS25	ISS24	ISS23	ISS22	ISS21	ISS20	ISS19	ISS18	ISS17	ISS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS15	ISS14	ISS13	ISS12	ISS11	ISS10	ISS9	ISS8	ISS7	ISS6	ISS5	ISS4	ISS3	ISS2	ISS1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b31 to b1	ISS[31:1]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

- ISS1

Address(es): VIC.ISS1 A001 0214h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS63	ISS62	ISS61	ISS60	ISS59	ISS58	ISS57	ISS56	ISS55	ISS54	ISS53	ISS52	ISS51	ISS50	ISS49	ISS48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS47	ISS46	ISS45	ISS44	ISS43	ISS42	ISS41	ISS40	ISS39	ISS38	ISS37	ISS36	ISS35	ISS34	ISS33	ISS32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[63:32]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

ISSi Bit (IRQ Interrupt Request Service) (i = 1 to 63)

This flag indicates the service status of an IRQ interrupt request from vector numbers 1 to 63.

- ISS2

Address(es): VIC.ISS2 A001 0218h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS95	ISS94	ISS93	ISS92	ISS91	ISS90	ISS89	ISS88	ISS87	ISS86	ISS85	ISS84	ISS83	ISS82	ISS81	ISS80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS79	ISS78	ISS77	ISS76	ISS75	ISS74	ISS73	ISS72	ISS71	ISS70	ISS69	ISS68	ISS67	ISS66	ISS65	ISS64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[95:64]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

- ISS3

Address(es): VIC.ISS3 A001 021Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS127	ISS126	ISS125	ISS124	ISS123	ISS122	ISS121	ISS120	ISS119	ISS118	ISS117	ISS116	ISS115	ISS114	ISS113	ISS112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS111	ISS110	ISS109	ISS108	ISS107	ISS106	ISS105	ISS104	ISS103	ISS102	ISS101	ISS100	ISS99	ISS98	ISS97	ISS96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[127:96]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

ISSi Bit (IRQ Interrupt Request Service Flag) (i = 64 to 127)

This flag indicates the service status of an IRQ interrupt request from vector numbers 127 to 64.

- ISS4

Address(es): VIC.ISS4 A001 0220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS159	ISS158	ISS157	ISS156	ISS155	ISS154	ISS153	ISS152	ISS151	ISS150	ISS149	ISS148	ISS147	ISS146	ISS145	ISS144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS143	ISS142	ISS141	ISS140	ISS139	ISS138	ISS137	ISS136	ISS135	ISS134	ISS133	ISS132	ISS131	ISS130	ISS129	ISS128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[159:128]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

- ISS5

Address(es): VIC.ISS5 A001 0224h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS191	ISS190	ISS189	ISS188	ISS187	ISS186	ISS185	ISS184	ISS183	ISS182	ISS181	ISS180	ISS179	ISS178	ISS177	ISS176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS175	ISS174	ISS173	ISS172	ISS171	ISS170	ISS169	ISS168	ISS167	ISS166	ISS165	ISS164	ISS163	ISS162	ISS161	ISS160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[191:160]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

ISSi Bit (IRQ Interrupt Request Service Flag) (i = 128 to 191)

This flag indicates the service status of an IRQ interrupt request from vector numbers 191 to 128.

- ISS6

Address(es): VIC.ISS6 A001 0228h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS223	ISS222	ISS221	ISS220	ISS219	ISS218	ISS217	ISS216	ISS215	ISS214	ISS213	ISS212	ISS211	ISS210	ISS209	ISS208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS207	ISS206	ISS205	ISS204	ISS203	ISS202	ISS201	ISS200	ISS199	ISS198	ISS197	ISS196	ISS195	ISS194	ISS193	ISS192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[223:192]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

- ISS7

Address(es): VIC.ISS7 A001 022Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS255	ISS254	ISS253	ISS252	ISS251	ISS250	ISS249	ISS248	ISS247	ISS246	ISS245	ISS244	ISS243	ISS242	ISS241	ISS240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS239	ISS238	ISS237	ISS236	ISS235	ISS234	ISS233	ISS232	ISS231	ISS230	ISS229	ISS228	ISS227	ISS226	ISS225	ISS224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[255:224]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

ISSi Bit (IRQ Interrupt Request Service Flag) (i = 192 to 255)

This flag indicates the service status of IRQ interrupt request from vector numbers 255 to 192.

- ISS8

Address(es): VIC.ISS8 A001 1210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISS287	ISS286	ISS285	ISS284	ISS283	ISS282	ISS281	ISS280	ISS279	ISS278	ISS277	ISS276	ISS275	ISS274	ISS273	ISS272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISS271	ISS270	ISS269	ISS268	ISS267	ISS266	ISS265	ISS264	ISS263	ISS262	ISS261	ISS260	ISS259	ISS258	ISS257	ISS256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISS[287:256]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R

- ISS9

Address(es): VIC.ISS9 A001 1214h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

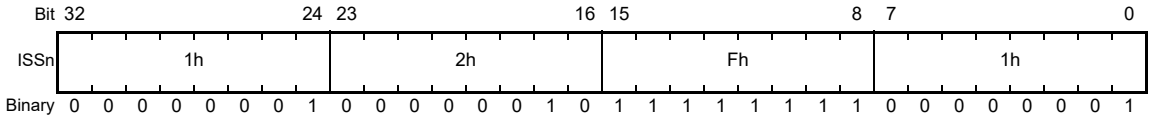
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ISS300	ISS299	ISS298	ISS297	ISS296	ISS295	ISS294	ISS293	ISS292	ISS291	ISS290	ISS289	ISS288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	ISS[300:288]	IRQ Interrupt Request Service Flag	0: The service is not executed. 1: The interrupt service routine (ISR) is being executed or suspended.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

ISSi Bit (IRQ Interrupt Request Service Flag) (i = 256 to 300)

This flag indicates the service status of IRQ interrupt request from vector numbers 300 to 256.

For example, if multiple interrupts are requested to the interrupt controller, the ISSn register shows the following status:



The figure indicates interrupts from vector numbers 24, 17, 15 to 8, and 0. Interrupt service routines (ISR) are serviced in descending order of priority which is set with the PRLm register. When the value of the PRLm is the same, the priority level of an interrupt with a smaller vector number is higher. When ISR finishes, the applicable bit of the ISSn register is cleared to 0, and then ISR that has the next highest priority level starts. In addition, if another interrupt is requested during ISR, the interrupt is also applied to this register.

12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9)

The ISCn (n = 0 to 9) register indicates the IRQ interrupt register with the highest priority level among IRQ interrupts which is set to 1 with interrupt service status register n (ISSn).
This register can only be read in 32-bit units.

- ISC0

Address(es): VIC.ISC0 A001 0230h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC31	ISC30	ISC29	ISC28	ISC27	ISC26	ISC25	ISC24	ISC23	ISC22	ISC21	ISC20	ISC19	ISC18	ISC17	ISC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC15	ISC14	ISC13	ISC12	ISC11	ISC10	ISC9	ISC8	ISC7	ISC6	ISC5	ISC4	ISC3	ISC2	ISC1	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b31 to b1	ISC[31:1]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

- ISC1

Address(es): VIC.ISC1 A001 0234h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC63	ISC62	ISC61	ISC60	ISC59	ISC58	ISC57	ISC56	ISC55	ISC54	ISC53	ISC52	ISC51	ISC50	ISC49	ISC48
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC47	ISC46	ISC45	ISC44	ISC43	ISC42	ISC41	ISC40	ISC39	ISC38	ISC37	ISC36	ISC35	ISC34	ISC33	ISC32
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[63:32]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

ISCi Bit (IRQ Interrupt Request Service Flag) (i = 1 to 63)

This flag indicates the service status of the IRQ interrupt request for interrupt service status register n (ISSn, n = 0 to 9).

- ISC2

Address(es): VIC.ISC2 A001 0238h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC95	ISC94	ISC93	ISC92	ISC91	ISC90	ISC89	ISC88	ISC87	ISC86	ISC85	ISC84	ISC83	ISC82	ISC81	ISC80
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC79	ISC78	ISC77	ISC76	ISC75	ISC74	ISC73	ISC72	ISC71	ISC70	ISC69	ISC68	ISC67	ISC66	ISC65	ISC64
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[95:64]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

- ISC3

Address(es): VIC.ISC3 A001 023Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC127	ISC126	ISC125	ISC124	ISC123	ISC122	ISC121	ISC120	ISC119	ISC118	ISC117	ISC116	ISC115	ISC114	ISC113	ISC112
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC111	ISC110	ISC109	ISC108	ISC107	ISC106	ISC105	ISC104	ISC103	ISC102	ISC101	ISC100	ISC99	ISC98	ISC97	ISC96
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[127:96]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

ISCi Bit (IRQ Interrupt Request Service Flag) (i = 64 to 127)

This flag indicates the service status of the IRQ interrupt request for interrupt service status register n (ISSn, n = 0 to 9).

- ISC4

Address(es): VIC.ISC4 A001 0240h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC159	ISC158	ISC157	ISC156	ISC155	ISC154	ISC153	ISC152	ISC151	ISC150	ISC149	ISC148	ISC147	ISC146	ISC145	ISC144
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC143	ISC142	ISC141	ISC140	ISC139	ISC138	ISC137	ISC136	ISC135	ISC134	ISC133	ISC132	ISC131	ISC130	ISC129	ISC128
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[159:128]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

- ISC5

Address(es): VIC.ISC5 A001 0244h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC191	ISC190	ISC189	ISC188	ISC187	ISC186	ISC185	ISC184	ISC183	ISC182	ISC181	ISC180	ISC179	ISC178	ISC177	ISC176
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC175	ISC174	ISC173	ISC172	ISC171	ISC170	ISC169	ISC168	ISC167	ISC166	ISC165	ISC164	ISC163	ISC162	ISC161	ISC160
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[191:160]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

ISCi Bit (IRQ Interrupt Request Service Flag) (i = 128 to 191)

This flag indicates the service status of the IRQ interrupt request for interrupt service status register n (ISSn, n = 0 to 9).

- ISC6

Address(es): VIC.ISC6 A001 0248h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC223	ISC222	ISC221	ISC220	ISC219	ISC218	ISC217	ISC216	ISC215	ISC214	ISC213	ISC212	ISC211	ISC210	ISC209	ISC208
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC207	ISC206	ISC205	ISC204	ISC203	ISC202	ISC201	ISC200	ISC199	ISC198	ISC197	ISC196	ISC195	ISC194	ISC193	ISC192
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[223:192]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

- ISC7

Address(es): VIC.ISC7 A001 024Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC255	ISC254	ISC253	ISC252	ISC251	ISC250	ISC249	ISC248	ISC247	ISC246	ISC245	ISC244	ISC243	ISC242	ISC241	ISC240
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC239	ISC238	ISC237	ISC236	ISC235	ISC234	ISC233	ISC232	ISC231	ISC230	ISC229	ISC228	ISC227	ISC226	ISC225	ISC224
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[255:224]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

ISCi Bit (IRQ Interrupt Request Service Flag) (i = 192 to 255)

This flag indicates the service status of the IRQ interrupt request for interrupt service status register n (ISSn, n = 0 to 9).

- ISC8

Address(es): VIC.ISC8 A001 1230h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ISC287	ISC286	ISC285	ISC284	ISC283	ISC282	ISC281	ISC280	ISC279	ISC278	ISC277	ISC276	ISC275	ISC274	ISC273	ISC272
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ISC271	ISC270	ISC269	ISC268	ISC267	ISC266	ISC265	ISC264	ISC263	ISC262	ISC261	ISC260	ISC259	ISC258	ISC257	ISC256
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	ISC[287:256]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R

- ISC9

Address(es): VIC.ISC9 A001 1234h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ISC300	ISC299	ISC298	ISC297	ISC296	ISC295	ISC294	ISC293	ISC292	ISC291	ISC290	ISC289	ISC288
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	ISC[300:288]	IRQ Interrupt Request Service Flag	0: The priority level is not the highest, or the interrupt service routine (ISR) is not executed. 1: An interrupt with the highest priority	R
b31 to b13	—	Reserved	These bits are read as 0.	R

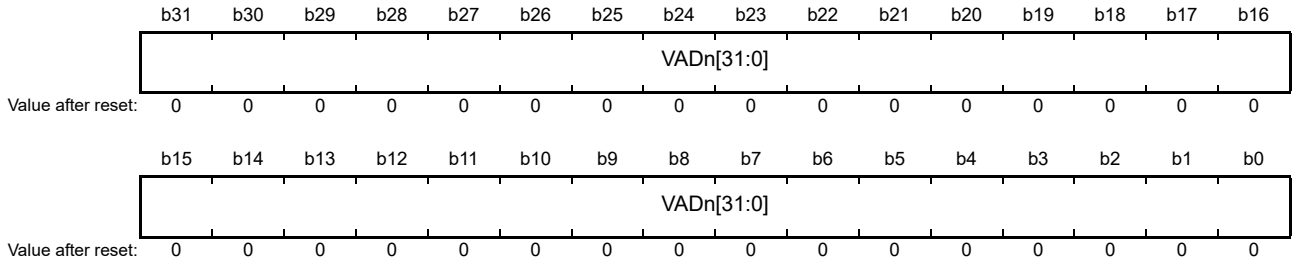
ISCi Bit (IRQ Interrupt Request Service Flag) (i = 256 to 300)

This flag indicates the service status of the IRQ interrupt request for interrupt service status register n (ISSn, n = 0 to 9).

12.4.2.16 Interrupt Address Store Register 0 (VADn) (n = 1 to 255)
Interrupt Address Store Register 1 (VADn) (n = 256 to 300)

The VADn (n = 1 to 300) register stores the vector address for each interrupt input.
This register can only be read and written in 32-bit units.

Address(es): VIC.VAD1 A001 0404h to VIC.VAD255 A001 07FCh
VIC.VAD256 A001 1400h to VIC.VAD300 A001 14B0h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	VADn[31:0]	Vector Address Store	VAD1 to VAD300 and vector numbers 1 to 300 are paired.	R/W

VADn[31:0] Bit (Vector Address Store) (n = 1 to 300)

This is a vector address store bit. VAD1 to VAD300 and bits of vector numbers 1 to 300 are paired.

- Connecting the CPU as the destination of interrupt requests
  Set the branch destination addresses of the interrupt handling routine to be run for interrupt requests n in these registers.
- Connecting a DMAC as the destination of interrupt requests
  The occurrence of interrupt requests n that have been set up to do so start DMA transfer. Set the branch destination addresses of the interrupt handling routines to be run for the DMA transfer completion interrupts in these registers.
  To connect a DMAC, set vector number n in the associated register as described in section 15.2.8, DMAC Unit 0 Source Select Register i (DMA0SELi) (i = 0 to 15), or section 15.2.9, DMAC Unit 1 Source Select Register i (DMA1SELi) (i = 0 to 15).

12.4.2.17 Interrupt Priority Level Store Register 0 (PRLn) (n = 1 to 255)

The PRLn (n = 1 to 255) register stores the interrupt priority level for each interrupt input.
This register can only be read and written in 32-bit units.

Address(es): VIC.PRL1 A001 0804h to VIC.PRL255 A001 0BFCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PRL3	PRL2	PRL1	PRL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PRL[3:0]	Interrupt Priority Level Store	The highest interrupt priority level is 0, and the lowest is 15.	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PRL[3:0] Bits (Interrupt Priority Level Store)

These bits store the interrupt priority level of vector numbers 1 to 255. The highest interrupt priority level is 0, and the lowest is 15.

12.4.2.18 Interrupt Priority Level Store Register 1 (PRLn) (n = 256 to 300)

The PRLn (n = 256 to 300) register stores the interrupt priority level for each interrupt input.
This register can only be read and written in 32-bit units.

Address(es): VIC.PRL256 A001 1800h to VIC.PRL300 A001 18B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PRL3	PRL2	PRL1	PRL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	PRL[3:0]	Interrupt Priority Level Store	The highest interrupt priority level is the value of PRLn+16. The highest is 16, and the lowest is 31.	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PRL[3:0] Bits (Interrupt Priority Level Store)

These bits store the interrupt priority level of vector numbers 256 to 300. The highest interrupt priority level is the value of PRLn+16. The highest is 16, and the lowest is 31.

12.4.2.19 Interrupt Level Control Register n (LVLCn) (n = 8, 9)

The LVLCn (n = 8, 9) register specifies the effective level for each interrupt input for the encoder I/F. Two bits are assigned for each interrupt input. High-level detection or low-level detection is specifiable.
This register can only be read and written in 32-bit units.

- LVLC8

Address(es): VIC.LVLC8 A001 01A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVC1431	LVC1430	LVC1421	LVC1420	LVC1411	LVC1410	LVC1401	LVC1400	LVC1391	LVC1390	LVC1381	LVC1380	LVC1371	LVC1370	LVC1361	LVC1360
Value after reset:	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVC1351	LVC1350	LVC1341	LVC1340	LVC1331	LVC1330	LVC1321	LVC1320	LVC1311	LVC1310	LVC1301	LVC1300	LVC1291	LVC1290	—	—
Value after reset:	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b1	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b3, b2	LVC[1291:1290]	Interrupt Effective Level Specification	Specify the effective level of vector number 129.	R/W
b5, b4	LVC[1301:1300]	Interrupt Effective Level Specification	Specify the effective level of vector number 130.	R/W
b7, b6	LVC[1311:1310]	Interrupt Effective Level Specification	Specify the effective level of vector number 131.	R/W
b9, b8	LVC[1321:1320]	Interrupt Effective Level Specification	Specify the effective level of vector number 132.	R/W
b11, b10	LVC[1331:1330]	Interrupt Effective Level Specification	Specify the effective level of vector number 133.	R/W
b13, b12	LVC[1341:1340]	Interrupt Effective Level Specification	Specify the effective level of vector number 134.	R/W
b15, b14	LVC[1351:1350]	Interrupt Effective Level Specification	Specify the effective level of vector number 135.	R/W
b17, b16	LVC[1361:1360]	Interrupt Effective Level Specification	Specify the effective level of vector number 136.	R/W
b19, b18	LVC[1371:1370]	Interrupt Effective Level Specification	Specify the effective level of vector number 137.	R/W
b21, b20	LVC[1381:1380]	Interrupt Effective Level Specification	Specify the effective level of vector number 138.	R/W
b23, b22	LVC[1391:1390]	Interrupt Effective Level Specification	Specify the effective level of vector number 139.	R/W
b25, b24	LVC[1401:1400]	Interrupt Effective Level Specification	Specify the effective level of vector number 140.	R/W
b27, b26	LVC[1411:1410]	Interrupt Effective Level Specification	Specify the effective level of vector number 141.	R/W
b29, b28	LVC[1421:1420]	Interrupt Effective Level Specification	Specify the effective level of vector number 142.	R/W
b31, b30	LVC[1431:1430]	Interrupt Effective Level Specification	Specify the effective level of vector number 143.	R/W

- LVLC9

Address(es): VIC.LVLC9 A001 01A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LVC1441	LVC1440
Value after reset:	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	LVC[1441:1440]	Interrupt Effective Level Specification	Specify the effective level of vector number 144.	R/W
b2	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b3	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b4	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b5	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b6	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b7	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b8	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b9	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b10	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b11	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b12	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b13	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b15	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b16	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b17	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b18	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b19	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b20	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W

Bit	Symbol	Bit Name	Description	R/W
b21	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b22	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b23	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b24	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b25	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b26	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b27	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b28	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b29	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b30	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b31	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W

LVCi Bits (Interrupt Effective Level Specification) (i = 1290 to 1441)

These bits specify the effective level for detection of interrupts with vector numbers 129 to 144.

LVCm1	LVCm0	Effective Level Specification
0	0	Setting prohibited
0	1	High level
1	0	Low level
1	1	Setting prohibited

12.4.3 Vector Table

12.4.3.1 Interrupt Vector Table

Table 12.3 describes the vector table for interrupts to Cortex-R4 and DMAC. Instead of an interrupt source from peripheral modules, transfer completion sources of DMAC channels selected by the DMAC source select register are connected to the vector number selected by the DMAC source select register.

For the interrupt source for vector numbers 42 to 44, interrupt sources are different between Cortex-R4 and DMAC. For Cortex-R4, the CPU interrupt source of the USB (func) is connected. Use vector numbers 43 and 44 as the DMA transfer sources for the USB (func). For details, see section 12.3.1, Selecting Interrupt Request Destinations. For details on interrupts from the USB, see section 31, USB2.0HS Host Module (USBh) and section 32, USB 2.0 HS Function Module (USBf).

The source of an interrupt for the Cortex-R4 and the same source as the trigger for DMAC activation may be detected in different ways. The Ethernet switch DLR interrupt (vector number 46) is one example. For details, see section 15, DMA Transfer Request, and the notes on DMA transfer.

The following table explains the items of the Cortex-R4/DMAC interrupt vector table.

Item	Description
Vector number	Indicates the vector number of the IRQ interrupt source in VIC for Cortex-R4.
Request source	Indicates the name of the interrupt request source.
Source	Indicates the interrupt name.
Detection type	Indicates the detection type for interrupts from peripheral modules. To connect a transfer completion interrupt from DMAC, the edge must be selected.
CR4	“Y” indicates the interrupt source for Cortex-R4 (VIC).
DMAC	“Y” indicates the DMAC activation source.

Note: An error signal of each module is not input to the CPU directly, but to the error control module (ECM). The signal is merged into other errors and conveyed as an error detection source to the CPU. For details, see section 42, Error Control Module (ECM).

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (1 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
1	System (CR4)	INTCR4	Interrupts between the CPU (CR4) (only for products incorporating an R-IN engine)	Edge	Y	N
2		INTCTI	CTI (Cross Trigger Interface) interrupt	Edge	Y	N
3		FPUEX	FPU exception	Level	Y	N
4	External	IRQ0	IRQ pin interrupt 0	Level / Edge	Y	Y
5		IRQ1	IRQ pin interrupt 1	Level / Edge	Y	Y
6		IRQ2	IRQ pin interrupt 2	Level / Edge	Y	Y
7		IRQ3	IRQ pin interrupt 3	Level / Edge	Y	Y
8		IRQ4	IRQ pin interrupt 4	Level / Edge	Y	Y
9		IRQ5	IRQ pin interrupt 5	Level / Edge	Y	Y
10		IRQ6	IRQ pin interrupt 6	Level / Edge	Y	Y
11		IRQ7	IRQ pin interrupt 7	Level / Edge	Y	Y
12		IRQ8	IRQ pin interrupt 8	Level / Edge	Y	Y
13		IRQ9	IRQ pin interrupt 9	Level / Edge	Y	Y
14		IRQ10	IRQ pin interrupt 10	Level / Edge	Y	Y
15		IRQ11	IRQ pin interrupt 11	Level / Edge	Y	Y
16		IRQ12	IRQ pin interrupt 12	Level / Edge	Y	Y
17		IRQ13	IRQ pin interrupt 13	Level / Edge	Y	Y
18		IRQ14	IRQ pin interrupt 14	Level / Edge	Y	Y
19		IRQ15	IRQ pin interrupt 15	Level / Edge	Y	Y
20	ECM	ERRD	Error detection (maskable)	Edge	Y	N
21	CMT unit 0	CMI0	Compare match interrupt_ch0	Edge	Y	Y
22		CMI1	Compare match interrupt_ch1	Edge	Y	Y
23	CMT unit 1	CMI2	Compare match interrupt_ch0	Edge	Y	Y
24		CMI3	Compare match interrupt_ch1	Edge	Y	Y
25	CMTW unit 0	CMWI0	Compare match interrupt	Edge	Y	Y
26		IC0I0	Input capture 0 interrupt	Edge	Y	Y
27		IC1I0	Input capture 1 interrupt	Edge	Y	Y
28		OC0I0	Output compare 0 interrupt	Edge	Y	Y
29		OC1I0	Output compare 1 interrupt	Edge	Y	Y
30	CMTW unit 1	CMWI1	Compare match interrupt	Edge	Y	Y
31		IC0I1	Input capture 0 interrupt	Edge	Y	Y
32		IC1I1	Input capture 1 interrupt	Edge	Y	Y
33		OC0I1	Output compare 0 interrupt	Edge	Y	Y
34		OC1I1	Output compare 1 interrupt	Edge	Y	Y
35	ADC unit 0	S12ADI0	AD conversion completion interrupt	Edge	Y	Y
36		S12GBADI0	Group B AD conversion completion interrupt	Edge	Y	Y
37		S12CMPI0	Compare condition not met	Level	Y	N
38	ADC unit 1	S12ADI1	AD conversion completion interrupt	Edge	Y	Y
39		S12GBADI1	Group B AD conversion completion interrupt	Edge	Y	Y
40		S12CMPI1	Compare condition met	Level	Y	N

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (2 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
41	USB	USBHI	USB (Host) CPU interrupt	Level	Y	N
42		USBFI	USB (Host) CPU interrupt	Level / Edge	Y	N
43		USBFDR1	USB (Func) DMA request 1	Level	N*3	Y
44		USBFDR2	USB (Func) DMA request 2	Level	N*3	Y
45	Switch with IEEE1588	ETHSWI	Ethernet switch interrupt	Level / Edge*1	Y	Y
46		ETHSWDLRI	Ethernet switch DLR interrupt	Level / Edge*1	Y	Y
47		ETHSWSOI	Ethernet switch SYNCOUT interrupt	Edge	Y	Y
48	Ethernet PHY	ETHPHYI0	Ethernet PHY interrupt 0	Level / Edge	Y	Y
49		ETHPHYI1	Ethernet PHY interrupt 1	Level / Edge	Y	Y
50		ETHPHYI2 (only for products incorporating an EtherCAT (optional))	Ethernet PHY interrupt 2	Level / Edge	Y	Y
51	Ethernet MAC	ETHDMAIR	Ethernet MACDMA reception completed	Level / Edge*1	Y	Y
52		ETHDMAIT	Ethernet MACDMA transmission completed	Edge	Y	Y
53		ETHRFI	Reception frame normal interrupt	Level / Edge*1	Y	Y
54	MTU3a	TGIA6	ch6 input capture/compare match A interrupt	Edge	Y	Y
55		TGIB6	ch6 input capture/compare match B interrupt	Edge	Y	Y
56		TGIC6	ch6 input capture/compare match C interrupt	Edge	Y	Y
57		TGID6	ch6 input capture/compare match D interrupt	Edge	Y	Y*6
58		TCIV6	ch6 overflow interrupt	Edge	Y	N
59		TGIA7	ch7 input capture/compare match A interrupt	Edge	Y	Y
60		TGIB7	ch7 input capture/compare match B interrupt	Edge	Y	Y
61		TGIC7	ch7 input capture/compare match C interrupt	Edge	Y	Y
62		TGID7	ch7 input capture/compare match D interrupt	Edge	Y	Y
63		TCIV7	ch7 overflow/underflow interrupt	Edge	Y	Y

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (3 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
64	Ethernet MAC	ETHMMAI	Ethernet MII management access completion interrupt	Edge	Y	Y
65		ETHPPIT	Ethernet pause packet transmission completed	Edge	Y	Y
66		ETHIT	Ethernet transmission completed interrupt	Edge	Y	Y
67		ETHRFIV	RX FIFO overflow	Edge	Y	N
68		ETHTFIU	TX FIFO underflow	Edge	Y	N
69		ETHTFIE	TX-FIFO error interrupt	Level	Y	N
70		ETHRFE	Ethernet reception frame error	Level	Y	N
71		ETHLPIST	LPI start notification interrupt from the MII	Edge	Y	N
72		ETHLPIEND	LPI end notification interrupt from the MII	Edge	Y	N
73	EtherCAT slave (optional)	ETHCSI0	EtherCAT Sync0 interrupt	Level / Edge*2	Y	Y
74		ETHCSI1	EtherCAT Sync1 interrupt	Level / Edge*2	Y	Y
75		ETHCI	EtherCAT interrupt	Level / Edge*1	Y	Y
76		ETHCSOFI	EtherCAT SOF interrupt	Edge	Y	Y
77		ETHCEOFI	EtherCAT EOF interrupt	Edge	Y	Y
78		ETHCWDTI	EtherCAT WDT interrupt	Edge	Y	N
79		ETHCRSTI	EtherCAT RESET interrupt	Edge	Y	N
80	RSPI ch0	SPRI0	Reception buffer full	Edge	Y	Y
81		SPTI0	Transmission buffer empty	Edge	Y	Y
82		SPEI0	Mode fault error/overrun error/parity error	Level	Y	N
83		SPII0	RSPI idle	Level	Y	N
84	RSPI ch1	SPRI1	Reception buffer full	Edge	Y	Y
85		SPTI1	Transmission buffer empty	Edge	Y	Y
86		SPEI1	Mode fault error/overrun error/parity error	Level	Y	N
87		SPII1	RSPI idle	Level	Y	N
88	RSPI ch2	SPRI2	Reception buffer full	Edge	Y	Y
89		SPTI2	Transmission buffer empty	Edge	Y	Y
90		SPEI2	Mode fault error/overrun error/parity error	Level	Y	N
91		SPII2	RSPI idle	Level	Y	N
92	RSPI ch3	SPRI3	Reception buffer full	Edge	Y	Y
93		SPTI3	Transmission buffer empty	Edge	Y	Y
94		SPEI3	Mode fault error/overrun error/parity error	Level	Y	N
95		SPII3	RSPI idle	Level	Y	N
96	SCIFA ch0	BRIF0	Break/overrun/framing error/parity error	Level	Y	N
97		RXIF0	Reception FIFO data full (RDF)	Level	Y	Y
98		TXIF0	Transmission FIFO data empty (TDFE)	Level	Y	Y
99		DRIF0	Transmit end/reception data ready	Level	Y	N

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (4 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
100	SCIFA ch1	BRIF1	Break/overrun/framing error/parity error	Level	Y	N
101		RXIF1	Reception FIFO data full (RDF)	Level	Y	Y
102		TXIF1	Transmission FIFO data empty (TDFE)	Level	Y	Y
103		DRIF1	Transmit end/reception data ready	Level	Y	N
104	RSCAN	CANRFI	CAN reception FIFO	Level	Y	N
105		CANFIR0	CAN0 transmission and reception FIFO transmission completed	Level	Y	N
106		CANTI0	CAN0 transmission	Level	Y	N
107		CANFIR1	CAN1 transmission and reception FIFO transmission completed	Level	Y	N
108		CANTI1	CAN1 transmission	Level	Y	N
109	SCIFA ch2	BRIF2	Break/overrun/framing error/parity error	Level	Y	N
110		RXIF2	Reception FIFO data full (RDF)	Level	Y	Y
111		TXIF2	Transmission FIFO data empty (TDFE)	Level	Y	Y
112		DRIF2	Transmit end/reception data ready	Level	Y	N
113	SCIFA ch3	BRIF3	Break/overrun/framing error/parity error	Level	Y	N
114		RXIF3	Reception FIFO data full (RDF)	Level	Y	Y
115		TXIF3	Transmission FIFO data empty (TDFE)	Level	Y	Y
116		DRIF3	Transmit end/reception data ready	Level	Y	N
117	SCIFA ch4	BRIF4	Break/overrun/framing error/parity error	Level	Y	N
118		RXIF4	Reception FIFO data full (RDF)	Level	Y	Y
119		TXIF4	Transmission FIFO data empty (TDFE)	Level	Y	Y
120		DRIF4	Transmit end/reception data ready	Level	Y	N
121	RIIC ch0	TEI0	Data transmission completed (TEND)	Level	Y	N
122		RXI0	Data reception completed (RDRF)	Edge	Y	Y
123		TXI0	Transmission data empty (TDRE)	Edge	Y	Y
124	RIIC ch1	TEI1	Data transmission completed (TEND)	Level	Y	N
125		RXI1	Data reception completed (RDRF)	Edge	Y	Y
126		TXI1	Transmission data empty (TDRE)	Edge	Y	Y
127	SSI	SSIRXI	Reception data full interrupt	Edge	Y	N
128		SSITXI	Transmission data empty interrupt	Edge	Y	N

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (5 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
129	Encoder I/F	ENCINT0	Encoder I/F interrupt 1	Level*5	Y	N
130		ENCINT1	Encoder I/F interrupt 2	Level*5	Y	N
131		ENCINT2	Encoder I/F interrupt 3	Level*5	Y	N
132		ENCINT3	Encoder I/F interrupt 4	Level*5	Y	N
133		ENCINT4	Encoder I/F interrupt 5	Level*5	Y	N
134		ENCINT5	Encoder I/F interrupt 6	Level*5	Y	N
135		ENCINT6	Encoder I/F interrupt 7	Level*5	Y	N
136		ENCINT7	Encoder I/F interrupt 8	Level*5	Y	N
137		ENCINT8	Encoder I/F interrupt 9	Level*5	Y	N
138		ENCINT9	Encoder I/F interrupt 10	Level*5	Y	N
139		ENCINT10	Encoder I/F interrupt 11	Level*5	Y	N
140		ENCINT11	Encoder I/F interrupt 12	Level*5	Y	N
141		ENCINT12	Encoder I/F interrupt 13	Level*5	Y	N
142		ENCINT13	Encoder I/F interrupt 14	Level*5	Y	N
143		ENCINT14	Encoder I/F interrupt 15	Level*5	Y	N
144		ENCINT15	Encoder I/F interrupt 16	Level*5	Y	N

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (6 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
145	MTU3a	TGIA0	ch0 input capture/compare match A interrupt	Edge	Y	Y
146		TGIB0	ch0 input capture/compare match B interrupt	Edge	Y	Y
147		TGIC0	ch0 input capture/compare match C interrupt	Edge	Y	Y
148		TGID0	ch0 input capture/compare match D interrupt	Edge	Y	Y
149		TGIE0	ch0 compare match E interrupt	Edge	Y	N
150		TGIF0	ch0 compare match F interrupt	Edge	Y	N
151		TCIV0	ch0 overflow interrupt	Edge	Y	N
152		TGIA1	ch1 input capture/compare match A interrupt	Edge	Y	Y
153		TGIB1	ch1 input capture/compare match B interrupt	Edge	Y	Y
154		TCIV1	ch1 overflow interrupt	Edge	Y	N
155		TCIU1	ch1 underflow interrupt	Edge	Y	N
156		TGIA2	ch2 input capture/compare match A interrupt	Edge	Y	Y
157		TGIB2	ch2 input capture/compare match B interrupt	Edge	Y	Y
158		TCIV2	ch2 overflow interrupt	Edge	Y	N
159		TCIU2	ch2 underflow interrupt	Edge	Y	N
160		TGIA3	ch3 input capture/compare match A interrupt	Edge	Y	Y
161		TGIB3	ch3 input capture/compare match B interrupt	Edge	Y	Y
162		TGIC3	ch3 input capture/compare match C interrupt	Edge	Y	Y
163		TGID3	ch3 input capture/compare match D interrupt	Edge	Y	Y
164		TCIV3	ch3 overflow interrupt	Edge	Y	N
165		TGIA4	ch4 input capture/compare match A interrupt	Edge	Y	Y
166		TGIB4	ch4 input capture/compare match B interrupt	Edge	Y	Y
167		TGIC4	ch4 input capture/compare match C interrupt	Edge	Y	Y
168		TGID4	ch4 input capture/compare match D interrupt	Edge	Y	Y
169		TCIV4	ch4 overflow/underflow interrupt	Edge	Y	Y
170		TGIU5	ch5 input capture/compare match U interrupt	Edge	Y	Y
171		TGIV5	ch5 input capture/compare match V interrupt	Edge	Y	Y
172		TGIW5	ch5 input capture/compare match W interrupt	Edge	Y	Y
173		TGIA8	ch8 input capture/compare match A interrupt	Edge	Y	Y
174		TGIB8	ch8 input capture/compare match B interrupt	Edge	Y	Y

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (7 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
175	MTU3a	TGIC8	ch8 input capture/compare match C interrupt	Edge	Y	Y
176		TGID8	ch8 input capture/compare match D interrupt	Edge	Y	Y
177		TCIV8	ch8 overflow interrupt	Edge	Y	N
178	GPTa	GTCIA0	ch0 input capture/compare match A interrupt	Edge	Y	Y
179		GTCIB0	ch0 input capture/compare match B interrupt	Edge	Y	Y
180		GTCIC0	ch0 compare match C interrupt	Edge	Y	Y
181		GTCID0	ch0 compare match D interrupt	Edge	Y	Y
182		GTCIE0	ch0 compare match E interrupt	Edge	Y	Y
183		GTCIF0	ch0 compare match F interrupt	Edge	Y	Y
184		GDTE0	ch0 dead time error input	Edge	Y	Y
185		GTCIV0	ch0 overflow interrupt	Edge	Y	Y
186		GTCIU0	ch0 underflow interrupt	Edge	Y	Y
187		GTCIA1	ch1 input capture/compare match A interrupt	Edge	Y	Y
188		GTCIB1	ch1 input capture/compare match B interrupt	Edge	Y	Y
189		GTCIC1	ch1 compare match C interrupt	Edge	Y	Y
190		GTCID1	ch1 compare match D interrupt	Edge	Y	Y
191		GTCIE1	ch1 compare match E interrupt	Edge	Y	Y
192		GTCIF1	ch1 compare match F interrupt	Edge	Y	Y
193		GDTE1	ch1 dead time error input	Edge	Y	Y
194		GTCIV1	ch1 overflow interrupt	Edge	Y	Y
195		GTCIU1	ch1 underflow interrupt	Edge	Y	Y
196		GTCIA2	ch2 input capture/compare match A interrupt	Edge	Y	Y
197		GTCIB2	ch2 input capture/compare match B interrupt	Edge	Y	Y
198		GTCIC2	ch2 compare match C interrupt	Edge	Y	Y
199		GTCID2	ch2 compare match D interrupt	Edge	Y	Y
200		GTCIE2	ch2 compare match E interrupt	Edge	Y	Y
201		GTCIF2	ch2 compare match F interrupt	Edge	Y	Y
202		GDTE2	ch2 dead time error input	Edge	Y	Y
203		GTCIV2	ch2 overflow interrupt	Edge	Y	Y
204		GTCIU2	ch2 underflow interrupt	Edge	Y	Y
205		GTCIA3	ch3 input capture/compare match A interrupt	Edge	Y	Y
206		GTCIB3	ch3 input capture/compare match B interrupt	Edge	Y	Y
207		GTCIC3	ch3 compare match C interrupt	Edge	Y	Y
208		GTCID3	ch3 compare match D interrupt	Edge	Y	Y
209		GTCIE3	ch3 compare match E interrupt	Edge	Y	Y
210		GTCIF3	ch3 compare match F interrupt	Edge	Y	Y
211		GDTE3	ch3 dead time error input	Edge	Y	Y
212		GTCIV3	ch3 overflow interrupt	Edge	Y	Y

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (8 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
213	GPTa	GTCIU3	ch3 underflow interrupt	Edge	Y	Y
214		ETGIN	External trigger input (falling edge detection) interrupt	Edge	Y	Y
215		ETGIP	External trigger input (rising edge detection) interrupt	Edge	Y	Y
216	TPUa unit 0	TGI0A	ch0 input capture/compare match A interrupt	Edge	Y	Y
217		TGI0B	ch0 input capture/compare match B interrupt	Edge	Y	Y
218		TGI0C	ch0 input capture/compare match C interrupt	Edge	Y	N
219		TGI0D	ch0 input capture/compare match D interrupt	Edge	Y	N
220		TCI0V	ch0 overflow interrupt	Edge	Y	N
221		TGI1A	ch1 input capture/compare match A interrupt	Edge	Y	Y
222		TGI1B	ch1 input capture/compare match B interrupt	Edge	Y	Y
223		TCI1V	ch1 overflow interrupt	Edge	Y	N
224		TCI1U	ch1 underflow interrupt	Edge	Y	N
225		TGI2A	ch2 input capture/compare match A interrupt	Edge	Y	Y
226		TGI2B	ch2 input capture/compare match B interrupt	Edge	Y	Y
227		TCI2V	ch2 overflow interrupt	Edge	Y	N
228		TCI2U	ch2 underflow interrupt	Edge	Y	N
229		TGI3A	ch3 input capture/compare match A interrupt	Edge	Y	Y
230		TGI3B	ch3 input capture/compare match B interrupt	Edge	Y	Y
231		TGI3C	ch3 input capture/compare match C interrupt	Edge	Y	N
232		TGI3D	ch3 input capture/compare match D interrupt	Edge	Y	N
233		TCI3V	ch3 overflow interrupt	Edge	Y	N
234		TGI4A	ch4 input capture/compare match A interrupt	Edge	Y	Y
235		TGI4B	ch4 input capture/compare match B interrupt	Edge	Y	Y
236		TCI4V	ch4 overflow interrupt	Edge	Y	N
237		TCI4U	ch4 underflow interrupt	Edge	Y	N
238		TGI5A	ch5 input capture/compare match A interrupt	Edge	Y	Y
239		TGI5B	ch5 input capture/compare match B interrupt	Edge	Y	Y
240		TCI5V	ch5 overflow interrupt	Edge	Y	N
241		TCI5U	ch5 underflow interrupt	Edge	Y	N
242	ELC	ELCIRQ1	Interrupt 1 (ELSR18)	Edge	Y	Y
243		ELCIRQ2	Interrupt 2 (ELSR19)	Edge	Y	Y

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (9 / 10)

Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
244	—	—	Reserved	—	—	—
245		—	Reserved	—	—	—
246	Ethernet MAC	ETHDRIE	MACDMA reception error interrupt	Edge	Y	N
247		ETHDTIE	MACDMA transmission error interrupt	Edge	Y	N
248	DMAC	DMAINT0	External DMA request 0 (DMAC) (can be connected to DMAC unit 0 only)	Level / Edge	N*3	Y
249		DMAINT1	External DMA request 1 (DMAC) (can be connected to DMAC unit 0 only)	Level / Edge	N*3	Y
250		DMAINT2	External DMA request 2 (DMAC) (can be connected to DMAC unit 1 only)	Level / Edge	N*3	Y
251		DMASRQ0	DMA transfer software activation (unit 0)	Edge	N*3	Y
252		DMASRQ1	DMA transfer software activation (unit 1)	Edge	N*3	Y
253	—	—	Reserved	—	—	—
254	CM3 (for products incorporating an R-IN engine)	SRQCM3	CM3 system reset request signal	Level	Y	N
255	—	—	Reserved	—	—	—
256	POE3	OEI1	POE0#Hi-Z request or output short (eMTU ch3, 4 or GPT ch0 to 2) interrupt	Level	Y	N
257		OEI2	POE4#Hi-Z request or output short (eMTU ch6, 7) interrupt	Level	Y	N
258		OEI3	POE8#Hi-Z request interrupt	Level	Y	N
259		OEI4	POE10# Hi-Z request interrupt	Level	Y	N
260	RIIC ch0	EEI0	Stop condition detection/Start condition detection/NACK detection/arbitration lost/time-out occurrence	Level	Y	N
261	RIIC ch1	EEI1	Stop condition detection/Start condition detection/NACK detection/arbitration lost/time-out occurrence	Level	Y	N
262	RSCAN	CANGE	CAN global error	Level	Y	N
263		CANIE0	CAN0 error	Level	Y	N
264		CANIE1	CAN1 error	Level	Y	N
265	BSC	BSCCMI	Compare match interrupt	Level	Y	N
266	SSI	SSIF	Transmission underflow interrupt/ transmission overflow interrupt/ reception underflow interrupt/reception overflow interrupt/Idle mode interrupt	Level	Y	N

Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (10 / 10)

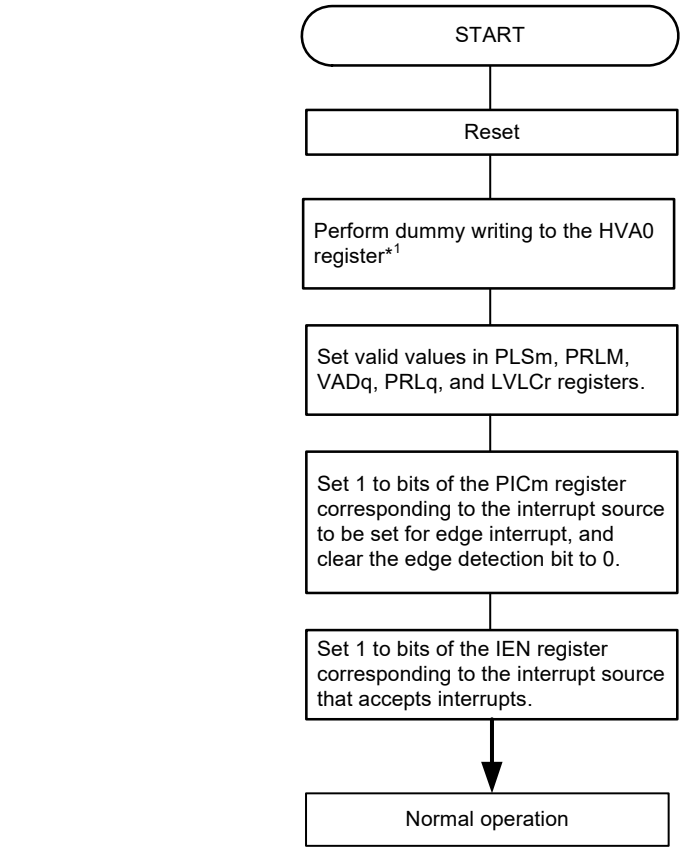
Vector Number	Request Source	Source		Detection Type	CR4	DMAC*4
267	TPUa unit 1	TGI6A	ch6 input capture/compare match A interrupt	Edge	Y	N
268		TGI6B	ch6 input capture/compare match B interrupt	Edge	Y	N
269		TGI6C	ch6 input capture/compare match C interrupt	Edge	Y	N
270		TGI6D	ch6 input capture/compare match D interrupt	Edge	Y	N
271		TCI6V	ch6 overflow interrupt	Edge	Y	N
272		TGI7A	ch7 input capture/compare match A interrupt	Edge	Y	N
273		TGI7B	ch7 input capture/compare match B interrupt	Edge	Y	N
274		TCI7V	ch7 overflow interrupt	Edge	Y	N
275		TCI7U	ch7 underflow interrupt	Edge	Y	N
276		TGI8A	ch8 input capture/compare match A interrupt	Edge	Y	N
277		TGI8B	ch8 input capture/compare match B interrupt	Edge	Y	N
278		TCI8V	ch8 overflow interrupt	Edge	Y	N
279		TCI8U	ch8 underflow interrupt	Edge	Y	N
280		TGI9A	ch9 input capture/compare match A interrupt	Edge	Y	N
281		TGI9B	ch9 input capture/compare match B interrupt	Edge	Y	N
282		TGI9C	ch9 input capture/compare match C interrupt	Edge	Y	N
283		TGI9D	ch9 input capture/compare match D interrupt	Edge	Y	N
284		TCI9V	ch9 overflow interrupt	Edge	Y	N
285		TGI10A	ch10 input capture/compare match A interrupt	Edge	Y	N
286		TGI10B	ch10 input capture/compare match B interrupt	Edge	Y	N
287		TCI10V	ch10 overflow interrupt	Edge	Y	N
288		TCI10U	ch10 underflow interrupt	Edge	Y	N
289		TGI11A	ch11 input capture/compare match A interrupt	Edge	Y	N
290		TGI11B	ch11 input capture/compare match B interrupt	Edge	Y	N
291		TCI11V	ch11 overflow interrupt	Edge	Y	N
292		TCI11U	ch11 underflow interrupt	Edge	Y	N
293	DMAC	DMAERR0	DMA transfer transfer error (unit 0)	Edge	Y	N
294		DMAERR1	DMA transfer transfer error (unit 1)	Edge	Y	N
295	—	—	Reserved	—	—	—
296		—	Reserved	—	—	—
297		—	Reserved	—	—	—
298		—	Reserved	—	—	—
299	CMT unit 2	CMI4	Compare match interrupt_ch0	Edge	Y	N
300		CMI5	Compare match interrupt_ch1	Edge	Y	N

Note: Do not select the interrupt request destinations that do not have Y for the request destination.
Note 1. Select level detection when using this source to generate interrupts for the CPU and edge detection when using it as a trigger for DMA activation.
Note 2. Select the level or edge detection when using this source to generate interrupts for the CPU, and edge detection when using it as a trigger for DMA activation.
Note 3. Though an interrupt serving as a DMA activating source is not generated as an interrupt, the interrupt handling routine with the vector number of the DMA transfer completion interrupt is executed on completion of DMA transfer. For details, see section 12.3.1, Selecting Interrupt Request Destinations, and section 15.4.2, DMA Transfer Completion Interrupts.
Note 4. When connecting the DMAC transfer completion interrupt, always select the same edge as that selected by the setting of interrupt detection type selection register n (PLSn). For details, see section 12.4.4.3, (1) Specifying Interrupt Detection Types.
Note 5. The active sense of the signal must be specified. For details, see section 12.4.4.3, Detecting Interrupts.
Note 6. Interrupts are generated in response to requests for DMA transfer, but there are no interrupts on completion of transfer. Poll the END bit of the CHSTAT_n register to confirm the completion of DMA transfer.

12.4.4 Operation

12.4.4.1 Initializing Registers of VIC

Figure 12.6 shows the procedure for initializing registers of VIC.
When you canceled reset, registers are not ready to operate due to interrupt priority level settings of VIC, or other reasons. For this reason, you must initialize the registers after a reset release.



m = 0 to 9, q = 1 to 300, r = 8, 9
Note 1. For initializing the VIC, write this register once after being released from a reset . Also, write this register at the end of each interrupt handling routine. For details, see section 12.4.2.13, Interrupt Address Register (HVA0).

Figure 12.6 Initializing Registers of VIC

12.4.4.2 Procedure for Rewriting the PLS, LVLC, PRLM, VAD, and PRL Registers

To rewrite the following registers while VIC is in operation, finish all interrupt processing, and then disable interrupts. To disable interrupts, set 1 to the I bit of the CPSR register for Cortex-R4.

- PLS (Interrupt detection type selection register)
- PRLM (Interrupt priority level mask register)
- LVLC (Interrupt level control register)
- VAD (Interrupt address storage register)
- PRL (Interrupt priority level storage register)

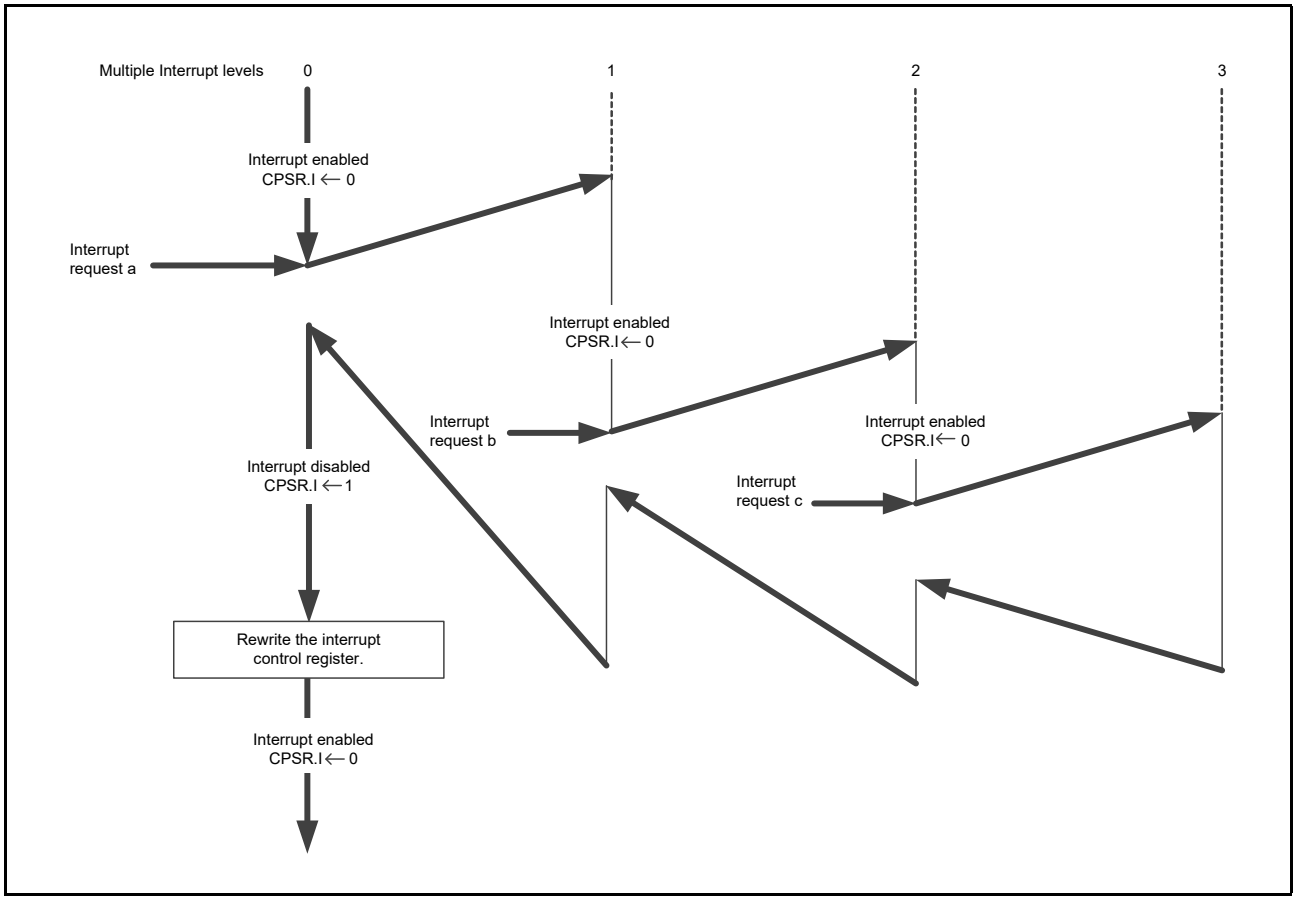


Figure 12.7 Period for Changing Register Settings

Follow the flow below to change register settings by using software.

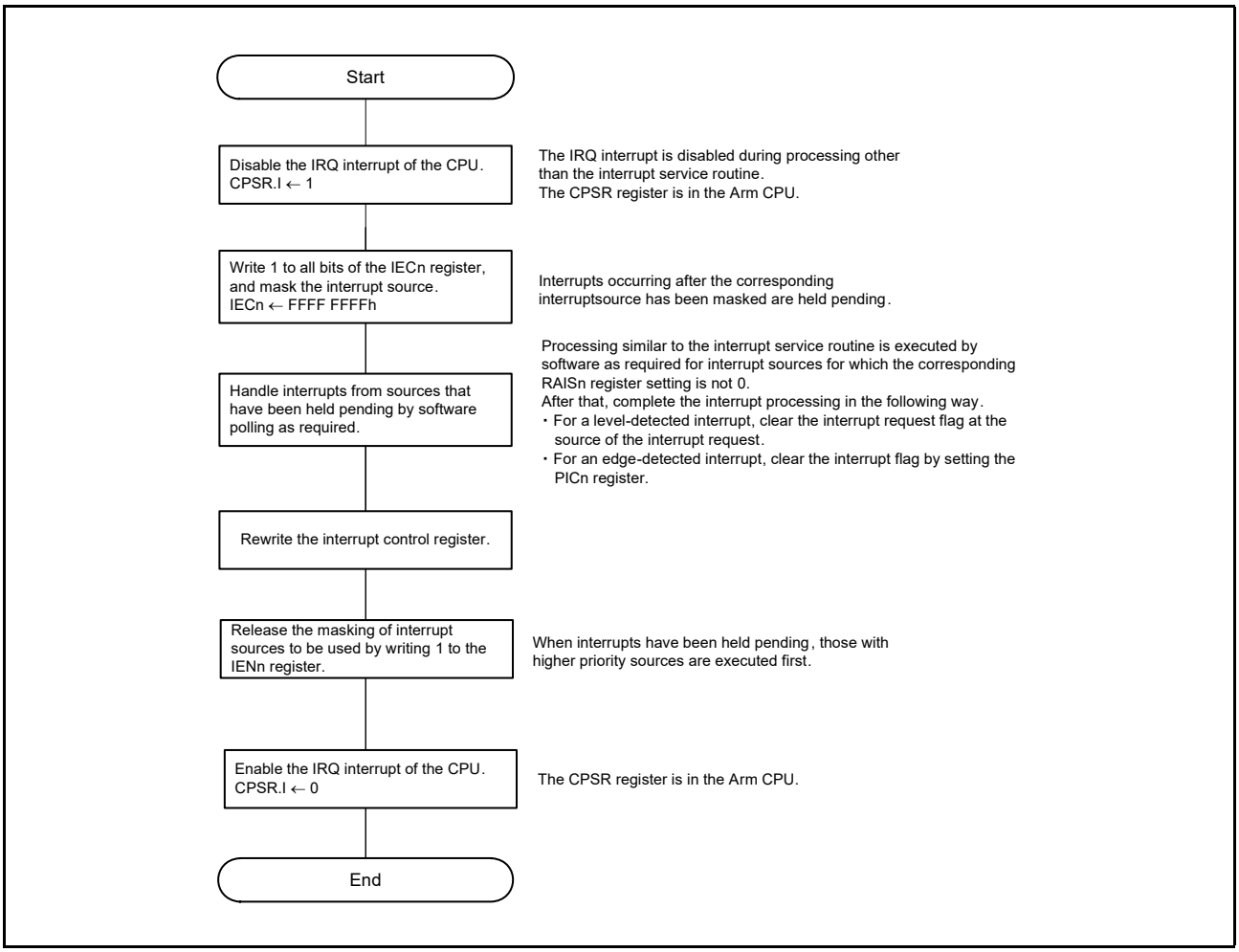


Figure 12.8 Register Rewrite Flow

12.4.4.3 Detecting Interrupts

(1) Specifying Interrupt Detection Types

When connecting external interrupts except interrupts from the NMI pin, and interrupts from on-chip peripheral modules to Cortex-R4, you must use VIC to select the edge or level detection with interrupt detection type selection register n (PLSn). You must also select the active sense of the signal in the corresponding interrupt level control register n (LVLCn). Table 12.4 lists settings of the interrupt detection type for VIC. When connecting transfer completion interrupt from DMAC, always select edge detection. For interrupt requests from the encoder interfaces, the type of detection and the active sense of interrupt signals have been specified for the individual modules, so set the given bits in the PLSn and LVLCn registers to match the specification.

Table 12.4 VIC Settings by Interrupt Detection Type

Interrupt Request Type	PLSm	LVCx1	LVCx0
Edge interrupt	1	Setting not required	Setting not required
Level interrupt	0	0/1	1/0

m: Interrupt vector number (0 to 300)
x: Interrupt vector number (129 to 144)

(2) IRQ Interrupt (Level interrupt)

Figure 12.9 shows level interrupt operation.

When you complete a level interrupt, stop interrupt output of the request source for the level interrupt. At that time, the applicable bit of IRQ status register n (IRQSn, n = 0 to 9) is cleared to 0. After that, make sure the interrupt is no longer requested. This operation is needed to prevent the same interrupt from being accepted after restoration because there is a delay before the interrupt output stop processing of the interrupt request source by the software is applied to the hardware. In addition, stop the interrupt output of the interrupt request source at the appropriate position of the service routine (ISR) according to the operation of the request source.

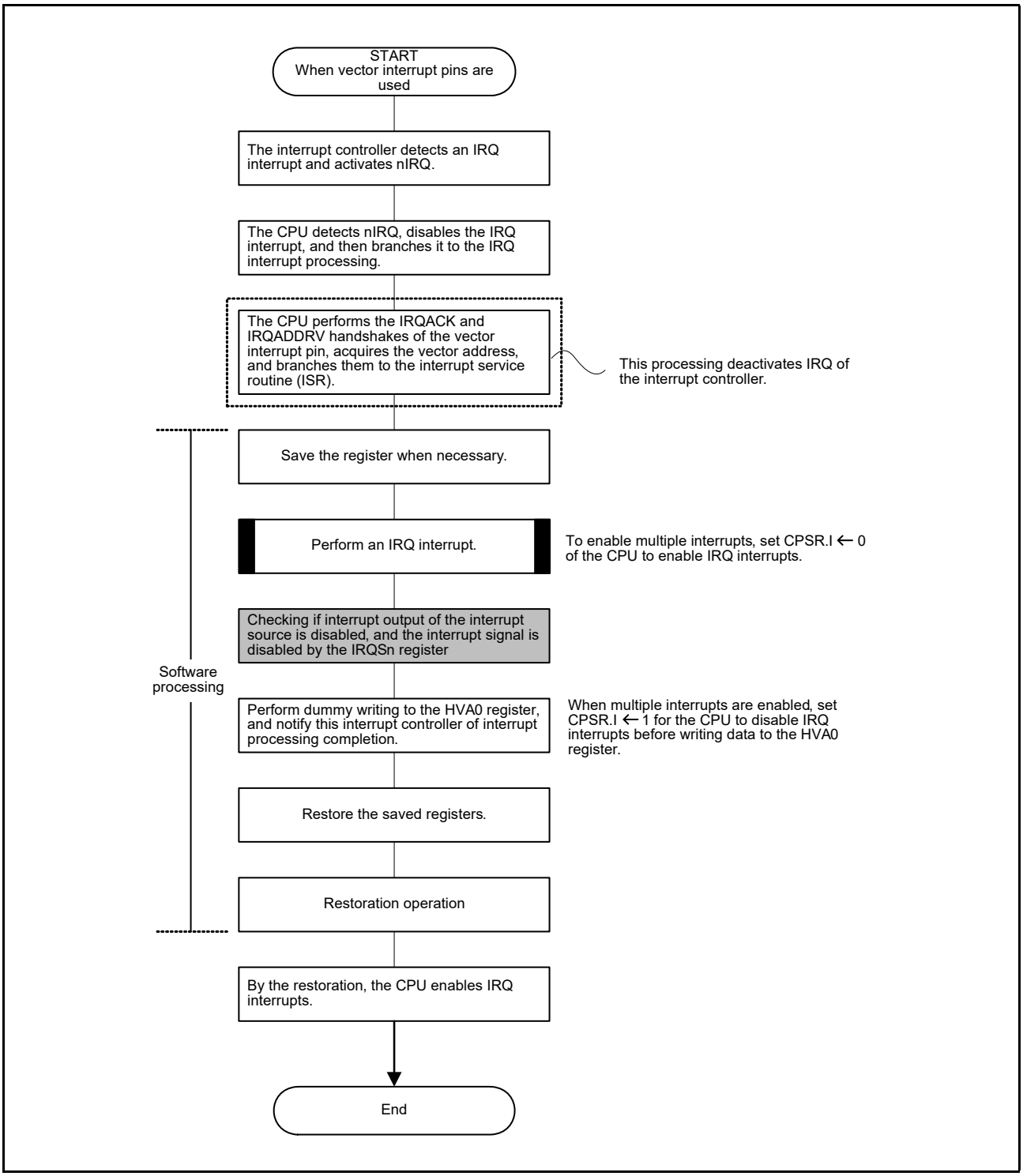


Figure 12.9 IRQ Interrupt Operation (Level Operations)

(3) IRQ Interrupt (Edge Interrupt)

Figure 12.10 shows edge interrupt operation.

Clear the edge interrupt request with edge detection bit clear register n (PICn, n = 0 to 9).

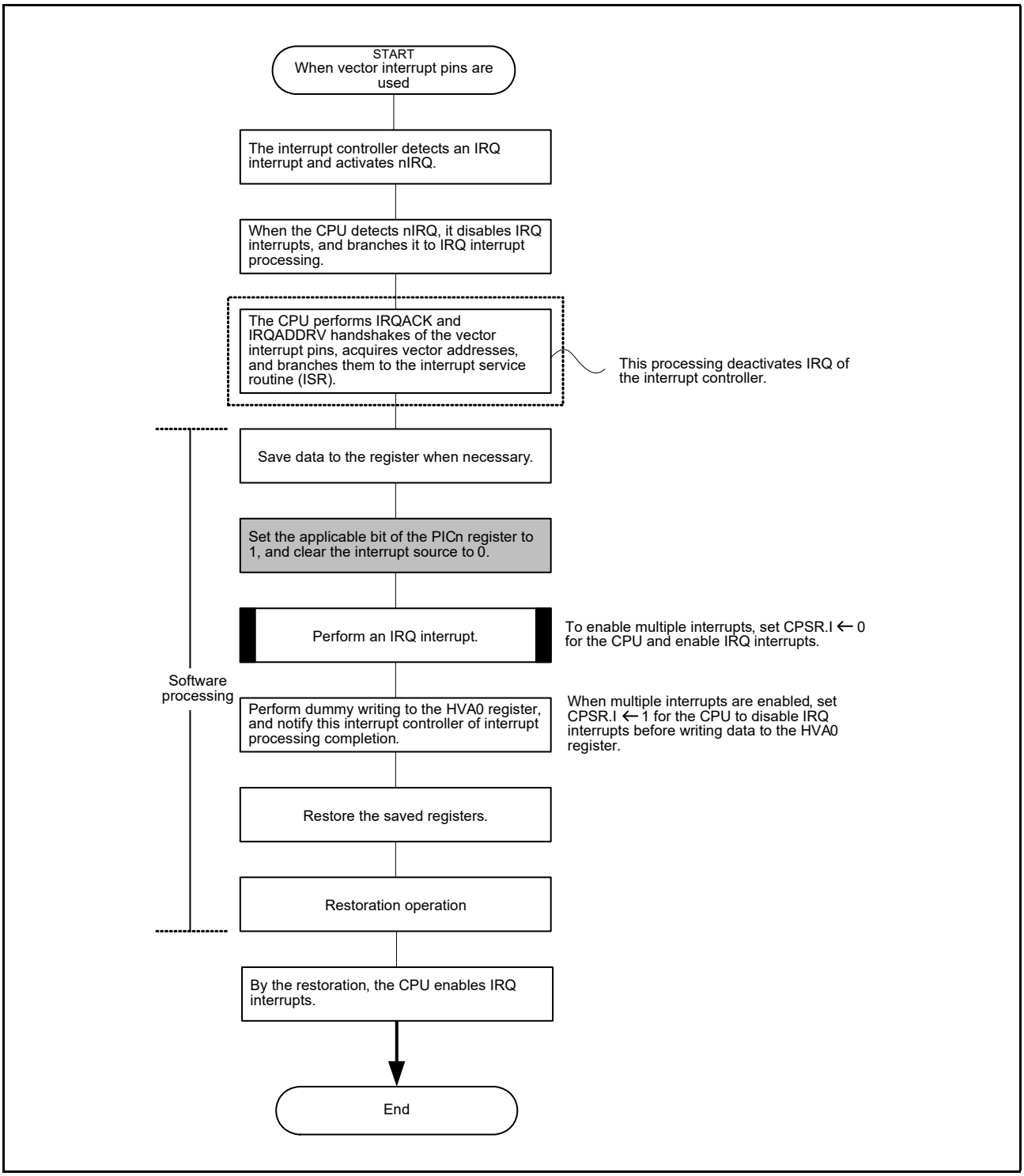


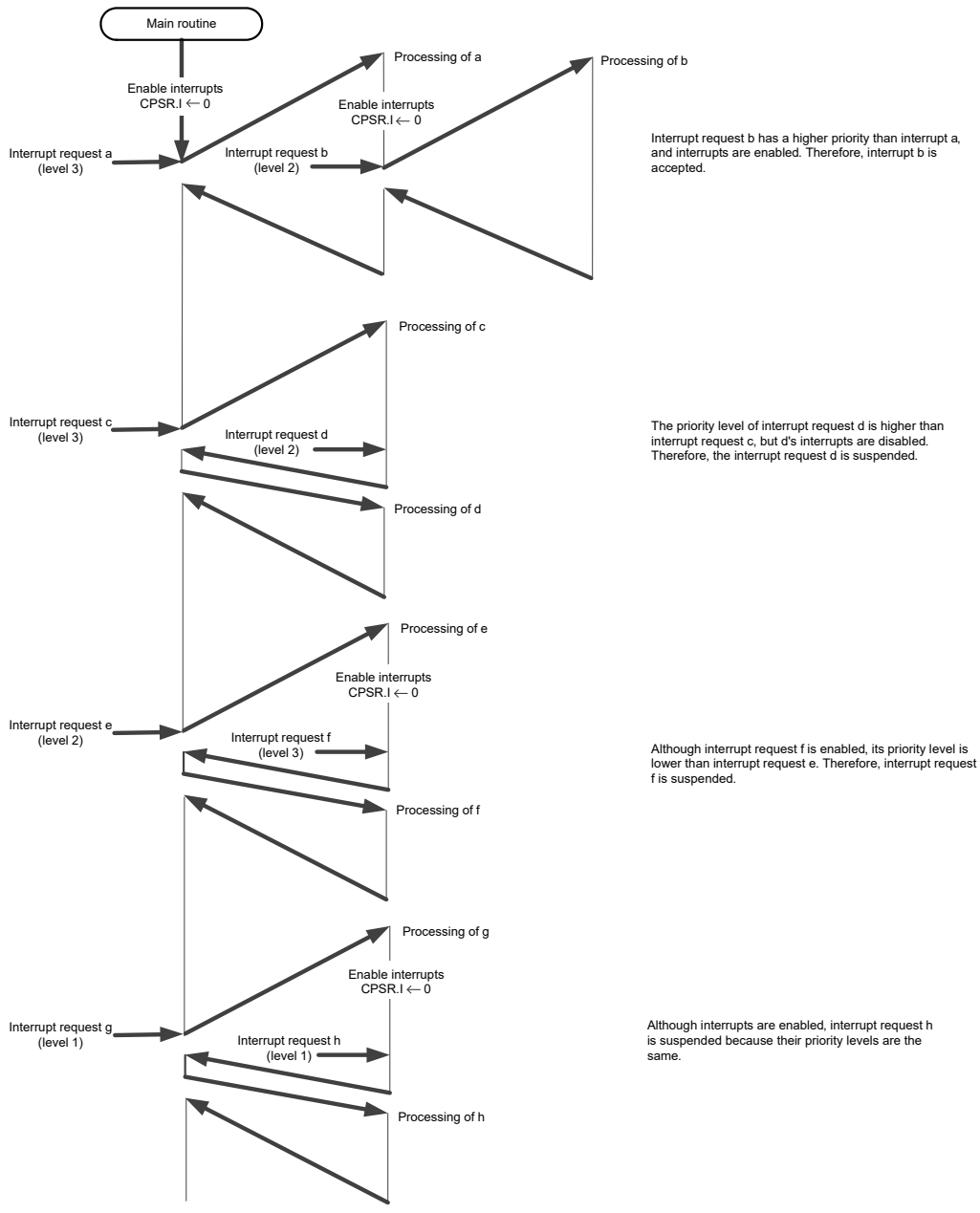
Figure 12.10 IRQ Interrupt Operation (Edge Interrupt)

12.4.4.4 Priority Level for Interrupt Multiple Control

If an interrupt is being handled (only when interrupt multiple control is being performed), only an interrupt that has higher priority than the interrupt which is being serviced is accepted. At that time, interrupts with lower priority than the currently serviced interrupt are suspended.

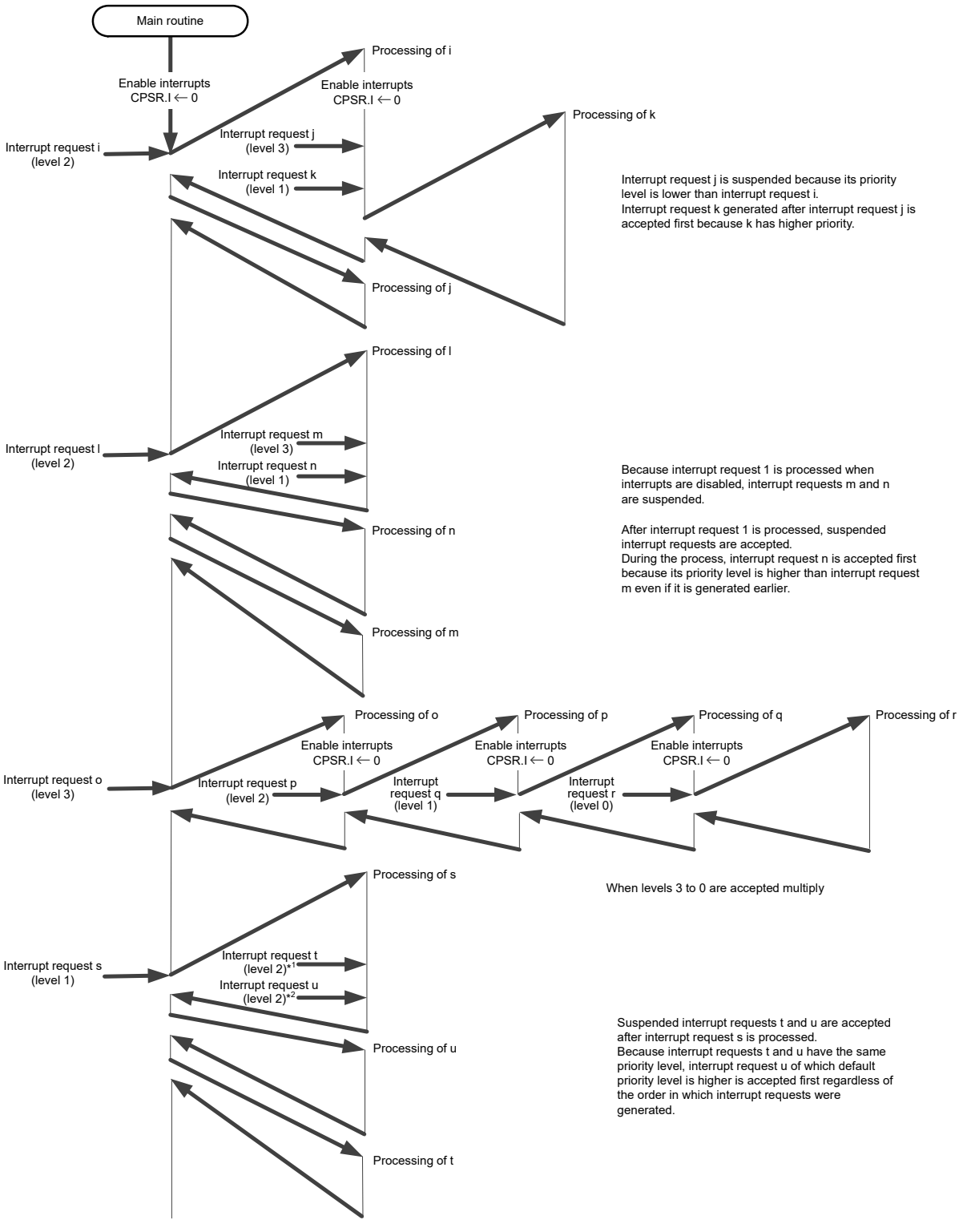
12.4.4.5 Handling Multiple Interrupts

Figure 12.11 provides an example of multiple interrupts that accept another interrupt when an interrupt is being handled.



a through u in the figure (including 2/2) are tentative names used to identify each interrupt request signal.
High/Low of the default priority level in the figure indicate the relative priority level between two interrupt request signals. The priorities are higher for smaller vector numbers, which means, if the same value is set in two interrupts by the PRLm register, the one with smaller vector number takes priority.

Figure 12.11 Concept of Multiple Interrupts (1 / 2)



Note 1. The default priority level is low.
Note 2. The default priority level is high.
The priorities are higher for smaller vector numbers, which means, if the same value is set in two interrupts by the PRLm register, the one with smaller vector number takes priority.

Figure 12.11 Concept of Multiple Interrupts (2 / 2)

12.4.4.6 Handling IRQ Interrupt Source Conditions by Polling

Figure 12.12 shows the procedure for handling IRQ interrupt source conditions by polling the interrupt status registers (RAISn).

That is, source conditions for IRQ interrupts can be detected by checking the bits of the interrupt input status registers (RAISn). This is useful when interrupts are masked by settings in the interrupt enable registers (IENn). This enables interrupt processing without hardware forcing branches to the interrupt service routines (ISRs).

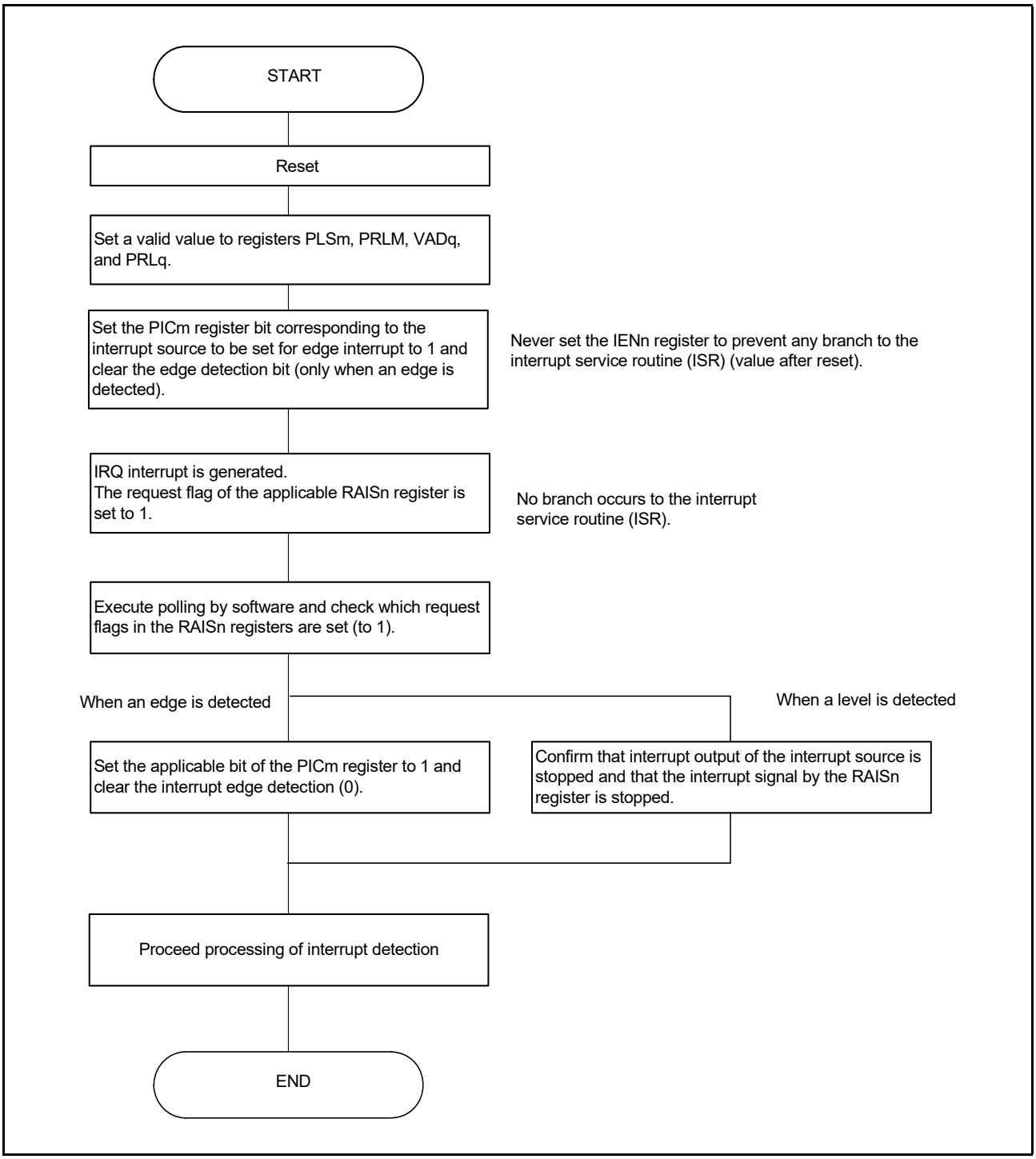


Figure 12.12 IRQ Interrupt Operation by Polling (Edge/Level Detection)

12.4.5 Return from Sleep Mode

If the interrupt controller is to return operation from sleep mode in response to an interrupt or non-maskable interrupt, make the following settings for the interrupt.

(1) The applicable interrupt request is enabled with the IENn bit.
(2) The DMAC source select register does not perform assignment to DMAC.

12.4.6 Usage Notes

12.4.6.1 Restrictions on VIC Priority Levels

VIC specifies the priority in 16 levels for each source with the interrupt priority level store register n (PRLn, n = 1 to 300). But lower priority levels are assigned to sources with vector numbers 256 and later compared to sources with vector numbers 1 to 255. Table 12.5 lists the relationship between vector numbers and priority levels.

Table 12.5 Relationship between Vector Numbers and Priority Levels

Vector Number	Priority Level*1
1 to 255	PRLn
256 to 300	PRLn + 16

n = 1 to 300
Note 1. The highest priority level is 0.

12.4.6.2 Notes on Accessing HVA0 Register

In cases of contention due to a vector interrupt being generated at the same time as writing to the HVA0 register, the AHB allows dummy-writing to the HVA0 register to proceed and blocks conveying of the IRQ interrupt to the CPU until a response to the write operation is returned so that processing to handle a new vector interrupt remains inactive over that time.
When writing to the HVA0 register, never fail to wait for the response indicating completion of the write operation before allowing IRQ interrupts to be sent to the CPU. Successful writing will be ensured by following the procedure illustrated in Figure 12.9 and executing a DMB instruction immediately after the write to the HVA0 register (as in the program example below).

- Program example

```
VIC.HVA0.LONG = 0x00000000;
asm(“dmb”);                    //DMB instruction
```

Note: The program format may vary according to the compiler. Confirm the applicable format for each compiler in the individual manuals.

12.4.6.3 Notes on Selecting Level Detection

When an interrupt request is set to level detection, do not cancel an interrupt request that was already generated except interrupt cancellation by the CPU. The correct vector address might not be output. For example, if level interrupt A is generated, the source for the output of interrupt A must be cleared by the service routine for interrupt A in a normal situation as shown in Figure 12.9 of section 12.4.4.3, Detecting Interrupts, but the source for the output of interrupt A may be transiently cleared if the service routine for another interrupt B has cleared or masked the source for the output of interrupt A.
When this interrupt controller accepts an interrupt, and the interrupt request is canceled before the CPU acquires the vector address, if another interrupt request is generated at the same time, 0000 0014h is output as the vector address. Therefore, to handle transitional cancellation of interrupt requests as mentioned above, it is recommended to use the return instruction only for 0000 0014h of the CPU (refer to the Example Program below).
In addition, if an interrupt request signal is transitionally withheld during the processing of an interrupt for which multiple interrupts are enabled, branching returns to the interrupt processing for which service is currently in progress. This interrupt handler writing to the HVA0 register causes the controller for this interrupt to recognize the completion of interrupt processing. Note that there is a gap between the actual interrupt source generating an interrupt request and the CPU recognizing the interrupt source.

- Example Program
  reserved_handler:
  subs pc, lr, #4 ; locate at 0000 0014h.

Note: The program format may differ for each complier. Confirm the applicable format for each in their manuals.

12.4.6.4 Notes when Rewriting the IECn Register

If the value of the IECn register is to be changed, do so while interrupts are disabled. To disable interrupts, set the I bit in the CPSR register of the Arm CPU to 1.

12.4.6.5 Notes on Vector Settings

In the specification of this product, use of the fixed vector by setting the SCTLR.[24]VE bit to 0 is prohibited. Only providing addresses from those of the VIC by setting SCTLR.[24]VE bit = 1 is possible. The addresses can be set by using the VADn registers (n: vector number).

12.5 Cortex-M3 Nested Vector Interrupt Controller (NVIC) (only for products incorporating an R-IN engine)

12.5.1 Overview

RZ/T1 uses NVIC embedded on Cortex-M3 as the interrupt controller of Cortex-M3. For details on the exceptional interrupt operations, visit the following URL of Arm:
http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

12.5.2 Vector Table

12.5.2.1 Interrupt Vector Table for CM3

Table 12.6 lists the vector table for interrupts to Cortex-M3. Interrupts specific to RZ/T1 are allocated to exception handling number 16 or later for Cortex-M3.
The source of an interrupt for the Cortex-M3 and the same source as the trigger for DMAC activation may be detected in different ways. The Ethernet switch DLR interrupt (vector number 107) is one example. For details, see section 15.3.4, DMA Transfer Request, and the notes on DMA transfer.
The following table explains the items of the CM3 interrupt vector table.

Item	Description
Vector Number	Indicates the vector number for NVIC of Cortex-M3.
Request source	Indicates the name of the interrupt request source.
Source	Indicates the interrupt name.
Detection type	Indicates the detection type for interrupts from peripheral modules. To connect a transfer completion interrupt from DMAC, the edge must be selected.
DMAC	Y indicates the DMAC activation source.
DMAC setting vector number	When the DMAC activation source is selected, the vector number to be set for the DMAC source select register is listed.

Table 12.6 CM3 Interrupt Vector Table (1 / 4)

Vector Number	Request Source	Source		Detection Type	DMAC	DMAC Setting Vector Number
1	System	INTCM3	Interrupts between the CPUs	Edge	N	—
2		—	Reserved	—	—	—
3		—	Reserved	—	—	—
4	External	IRQ0	IRQ pin interrupt 0	Level / Edge	Y	4 (4h)
5		IRQ1	IRQ pin interrupt 1	Level / Edge	Y	5 (5h)
6		IRQ2	IRQ pin interrupt 2	Level / Edge	Y	6 (6h)
7		IRQ3	IRQ pin interrupt 3	Level / Edge	Y	7 (7h)
8		IRQ4	IRQ pin interrupt 4	Level / Edge	Y	8 (8h)
9		IRQ5	IRQ pin interrupt 5	Level / Edge	Y	9 (9h)
10		IRQ6	IRQ pin interrupt 6	Level / Edge	Y	10 (Ah)
11		IRQ7	IRQ pin interrupt 7	Level / Edge	Y	11 (Bh)
12		IRQ8	IRQ pin interrupt 8	Level / Edge	Y	12 (Ch)
13		IRQ9	IRQ pin interrupt 9	Level / Edge	Y	13 (Dh)
14		IRQ10	IRQ pin interrupt 10	Level / Edge	Y	14 (Eh)
15		IRQ11	IRQ pin interrupt 11	Level / Edge	Y	15 (Fh)
16		IRQ12	IRQ pin interrupt 12	Level / Edge	Y	16 (10h)
17		IRQ13	IRQ pin interrupt 13	Level / Edge	Y	17 (11h)
18		IRQ14	IRQ pin interrupt 14	Level / Edge	Y	18 (12h)
19		IRQ15	IRQ pin interrupt 15	Level / Edge	Y	19 (13h)
20	—	—	Reserved	—	—	—
21	CMT unit 0	CMI0	Compare match interrupt_ch0	Edge	Y	21 (15h)
22		CMI1	Compare match interrupt_ch1	Edge	Y	22 (16h)
23	CMT unit 1	CMI2	Compare match interrupt_ch0	Edge	Y	23 (17h)
24		CMI3	Compare match interrupt_ch1	Edge	Y	24 (18h)
25	CMTW unit 0	CMWI0	Compare match interrupt	Edge	Y	25 (19h)
26		IC0I0	Input capture 0 interrupt	Edge	Y	26 (1Ah)
27		IC1I0	Input capture 1 interrupt	Edge	Y	27 (1Bh)
28		OC0I0	Output compare 0 interrupt	Edge	Y	28 (1Ch)
29		OC1I0	Output compare 1 interrupt	Edge	Y	29 (1Dh)
30	CMTW unit 1	CMWI1	Compare match interrupt	Edge	Y	30 (1Eh)
31		IC0I1	Input capture 0 interrupt	Edge	Y	31 (1Fh)
32		IC1I1	Input capture 1 interrupt	Edge	Y	32 (20h)
33		OC0I1	Output compare 0 interrupt	Edge	Y	33 (21h)
34		OC1I1	Output compare 1 interrupt	Edge	Y	34 (22h)
35	—	—	Reserved	—	—	—
36		—	Reserved	—	—	—
37		—	Reserved	—	—	—
38		—	Reserved	—	—	—
39	CMT unit 2	CMI4	Compare match interrupt_ch0	Edge	N	—
40		CMI5	Compare match interrupt_ch1	Edge	N	—

Table 12.6 CM3 Interrupt Vector Table (2 / 4)

Vector Number	Request Source	Source		Detection Type	DMAC	DMAC Setting Vector Number
41	DMAC	DMASRQ0	DMA transfer software activation (unit 0)	Edge	Y	251 (FBh)
42		DMASRQ1	DMA transfer software activation (unit 1)	Edge	Y	252 (FCh)
43		DMAERR0	DMA transfer transfer error (unit 0)	Edge	N	—
44		DMAERR1	DMA transfer transfer error (unit 1)	Edge	N	—
45	—	—	Reserved	—	—	—
46		—	Reserved	—	—	—
47		—	Reserved	—	—	—
48	Ethernet PHY	ETHPHYI0	Ethernet PHY interrupt 0	Level / Edge	Y	48 (30h)
49		ETHPHYI1	Ethernet PHY interrupt 1	Level / Edge	Y	49 (31h)
50		ETHPHYI2	Ethernet PHY interrupt 2	Level / Edge	Y	50 (32h)
51	—	—	Reserved	—	—	—
52		—	Reserved	—	—	—
53		—	Reserved	—	—	—
54		—	Reserved	—	—	—
55		—	Reserved	—	—	—
56		—	Reserved	—	—	—
57		—	Reserved	—	—	—
58		—	Reserved	—	—	—
59		—	Reserved	—	—	—
60	SCIFA ch0	BRIF0	Break/overrun/framing error/parity error	Level	N	—
61		RXIF0	Reception FIFO data full (RDF)	Level	Y	97 (61h)
62		TXIF0	Transmission FIFO data empty (TDFE)	Level	Y	98 (62h)
63		DRIF0	Transmit end/reception data ready	Level	N	—
64	SCIFA ch1	BRIF1	Break/overrun/framing error/parity error	Level	N	—
65		RXIF1	Reception FIFO data full (RDF)	Level	Y	101 (65h)
66		TXIF1	Transmission FIFO data empty (TDFE)	Level	Y	102 (66h)
67		DRIF1	Transmit end/reception data ready	Level	N	—
68	—	—	Reserved	—	—	—
69		—	Reserved	—	—	—
70		—	Reserved	—	—	—
71		—	Reserved	—	—	—
72	RIIC ch0	TEI0	Data transmission completed (TEND)	Level	N	—
73		RXI0	Data reception completed (RDRF)	Edge	Y	122 (7Ah)
74		TXI0	Transmission data empty (TDRE)	Edge	Y	123 (7Bh)
75		EEI0	Stop condition detection/start condition detection/ NACK detection/arbitration lost/time-out occurrence	Level	N	—
76	RIIC ch1	TEI1	Data transmission completed (TEND)	Level	N	—
77		RXI1	Data reception completed (RDRF)	Edge	Y	125 (7Dh)
78		TXI1	Transmission data empty (TDRE)	Edge	Y	126 (7Eh)
79		EEI1	Stop condition detection/start condition detection/ NACK detection/arbitration lost/time-out occurrence	Level	N	—

Table 12.6 CM3 Interrupt Vector Table (3 / 4)

Vector Number	Request Source	Source		Detection Type	DMAC	DMAC Setting Vector Number
80	RSPI ch0	SPRI0	Reception buffer full	Edge	Y	80 (50h)
81		SPTI0	Transmission buffer empty	Edge	Y	81 (51h)
82		SPEI0	Mode fault error/overrun error/parity error	Level	N	—
83		SPII0	RSPI idle	Level	N	—
84	RSPI ch1	SPRI1	Reception buffer full	Edge	Y	84 (54h)
85		SPTI1	Transmission buffer empty	Edge	Y	85 (55h)
86		SPEI1	Mode fault error/overrun error/parity error	Level	N	—
87		SPII1	RSPI idle	Level	N	—
88	RSCAN	CANRFI	CAN reception FIFO	Level	N	—
89		CANFIR0	CAN0 transmission and reception FIFO reception completed	Level	N	—
90		CANTI0	CAN0 transmission	Level	N	—
91		CANFIR1	CAN1 transmission and reception FIFO reception completed	Level	N	—
92		CANTI1	CAN1 transmission	Level	N	—
93		CANGE	CAN global error	Level	N	—
94		CANIE0	CAN0 error	Level	N	—
95		CANIE1	CAN1 error	Level	N	—
96	EtherCAT slave (optional)	HWRTOS	HW-RTOS interrupt	Level	N	—
97		ETHCSI0	EtherCAT Sync0 interrupt	Level / Edge*3	Y*4	73 (49h)
98		ETHCSI1	EtherCAT Sync1 interrupt	Level / Edge*3	Y*4	74 (4Ah)
99		ETHCI	EtherCAT interrupt	Level / Edge*2	Y*4	75 (4Bh)
100		ETHCSOFI	EtherCAT SOF interrupt	Edge	Y*4	76 (4Ch)
101		ETHCEOFI	EtherCAT EOF interrupt	Edge	Y*4	77 (4Dh)
102	Ethernet MAC	—	Reserved	—	—	—
103		ETHMMAI	Ethernet MII management access completion interrupt	Edge	Y*4	64 (40h)
104		ETHPPIT	Ethernet pause packet transmission completed	Edge	Y*4	65 (41h)
105		ETHIT	Ethernet transmission completed interrupt	Edge	Y*4	66 (42h)
106	Switch with IEEE1588	ETHSWI	Ethernet switch interrupt	Level / Edge*2	Y*4	45 (2Dh)
107		ETHSWDLRI	Ethernet switch DLR interrupt	Level / Edge*2	Y*4	46 (2Eh)
108		ETHSWSOI	Ethernet switch SYNCOUT interrupt	Edge	Y*4	47 (2Fh)
109	Ethernet MAC	ETHRFIV	RX FIFO overflow	Edge	N	—
110		ETHTFIU	TX FIFO underflow	Edge	N	—
111		ETHDMAIR	Ethernet MACDMA reception completed	Level / Edge*2	Y*4	51 (33h)
112		ETHDMAIT	Ethernet MACDMA transmission completed	Edge	Y*4	52 (34h)
113		ETHRFI	Reception frame normal interrupt	Level / Edge*2	Y*4	53 (35h)
114		—	Reserved	—	—	—
115		ETHTFIE	TX-FIFO error interrupt	Level	N	—
116		ETHRFE	Ethernet reception frame error	Level	N	—
117		ETHDRIE	MACDMA reception error interrupt	Edge	N	—
118		ETHDTIE	MACDMA transmission error interrupt	Edge	N	—
119		—	Reserved	—	—	—

Table 12.6 CM3 Interrupt Vector Table (4 / 4)

Vector Number	Request Source	Source		Detection Type	DMAC	DMAC Setting Vector Number
120	EtherCAT slave (optional)	ETHCRSTI	EtherCAT RESET interrupt	Edge	N	—
121		ETHCWDTI	EtherCAT WDT interrupt	Edge	N	—
122	Ethernet MAC	ETHLPIST	LPI start notification interrupt from the MII	Edge	N	—
123		ETHLPIEND	LPI end notification interrupt from the MII	Edge	N	—
124	RAM	ETHRSE1	1-bit ECC error interrupt from the on-chip extended SRAM*1	Edge	N	—
125		ETHRSE2	2-bit ECC error interrupt from the on-chip extended SRAM*1	Edge	N	—
126	System	ETHCTO0	CTI trigger output signal 0	Edge	N	—
127		ETHCTO1	CTI trigger output signal 1	Edge	N	—

Note: Do not select the interrupt request destinations that do not have Y for the request destination.
Note 1. Only in products with extended on-chip SRAM
Note 2. Select level detection when using this source to generate interrupts for the CPU and edge detection when using it as a trigger for DMA activation.
Note 3. Select the level or edge detection when using this source to generate interrupts for the CPU, and edge detection when using it as a trigger for DMA activation.
Note 4. Interrupts are generated in response to requests for DMA transfer, but there are no interrupts on completion of transfer. Poll the END bit of the CHSTAT_n register to confirm the completion of DMA transfer.

12.6 Usage Notes

12.6.1 Using “Falling-Edge” or “Rising and Falling Edges” Detection with the External Pin Interrupts

Since the internal level on external pin interrupts after a reset is high, when external pin interrupts are used with low as the initial input level and the detection of “falling edge” or “rising and falling edges”, follow the procedure below.
Otherwise, follow the procedures shown in section 12.3.3, External Pin Interrupts.
In addition, make sure that a falling edge is not input to the external pin interrupts before these settings are completed.

[For IRQ pins]

1. Clear the applicable IENn bit to 0 (set the IECn bit).
2. Set the Pmn I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).
3. Set and check (read) the I/O port (PmnPFS.ISEL bit).
4. Clear the IRQFLTE.FLTENi bit to 0.*1
5. Set the digital noise filter sampling clock with the IRQFLTC.FCLKSEL[1:0] bits.*1
6. Set the IRQFLTE.FLTENi bit to 1.*1
7. Select the edge for detection as “falling” or “rising and falling” by setting the IRQCRi.IRQMD[1:0] bits.
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. Setting is required only when the digital filter is used.

[For ETH0_INT/ETH1_INT/ETH2_INT pins]

1. Set the applicable IENn bit to 0 (set the IECn bit).
2. Set the Pmn I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).
3. Set the I/O port (the PmnPFS.PSEL[5:0] bits and PMR register), and check (read) the PmnPFS register.
4. Clear the EPHYFLTE.EFLTENi bit to 0.*1
5. Set the digital noise filter sampling clock with the EPHYFLTC.EFCLKSEL[1:0] bits.*1
6. Set the EPHYFLTE.EFLTENi bit to 1.*1
7. Select the edge for detection as “falling” or “rising and falling” by setting the EPHYCRi.EPHYMD[1:0] bits.
8. Set the applicable PICn register to 1 (when an edge is detected).
9. Set the applicable IENn bit to 1.

Note 1. Setting is required only when the digital filter is used.

12.6.2 Using Falling-Edge Detection with the NMI Pin

Since the internal level on the NMI pin after a reset is high, when the NMI pin is used with low as the initial input level and the detection of falling edges, follow the procedure below.
Otherwise, follow the procedure shown in section 12.3.4, NMI Pin Interrupts.
In addition, make sure that a falling edge is not input to the NMI pin before these settings are completed.

1. Select the edge for detection as rising by setting the NMICR.NMIMD bit to 1.
2. Set and check the I/O port pin (P35PFS.ISEL bit).
3. Clear the NMIFLTE.NFLTEN bit to 0.*1
4. Set the sampling clock cycle for the digital noise filter in the NMIFLTC.NFCLKSEL[1:0] bits.*1
5. Clear the NMICR.NMIMD bit to 0 (falling edge detection).
6. Set the NMICLR.NMICLR bit to 1, and clear the NMISR.NMIST flag to 0.
7. Set the NMIFLTE.NFLTEN bit to 1.*1
8. Set the P35 I/O select bit in the port direction register (PDR) of the I/O port to 10b (input).

Note 1. This setting is only required when the digital noise filter is to be used.

13. Internal Buses

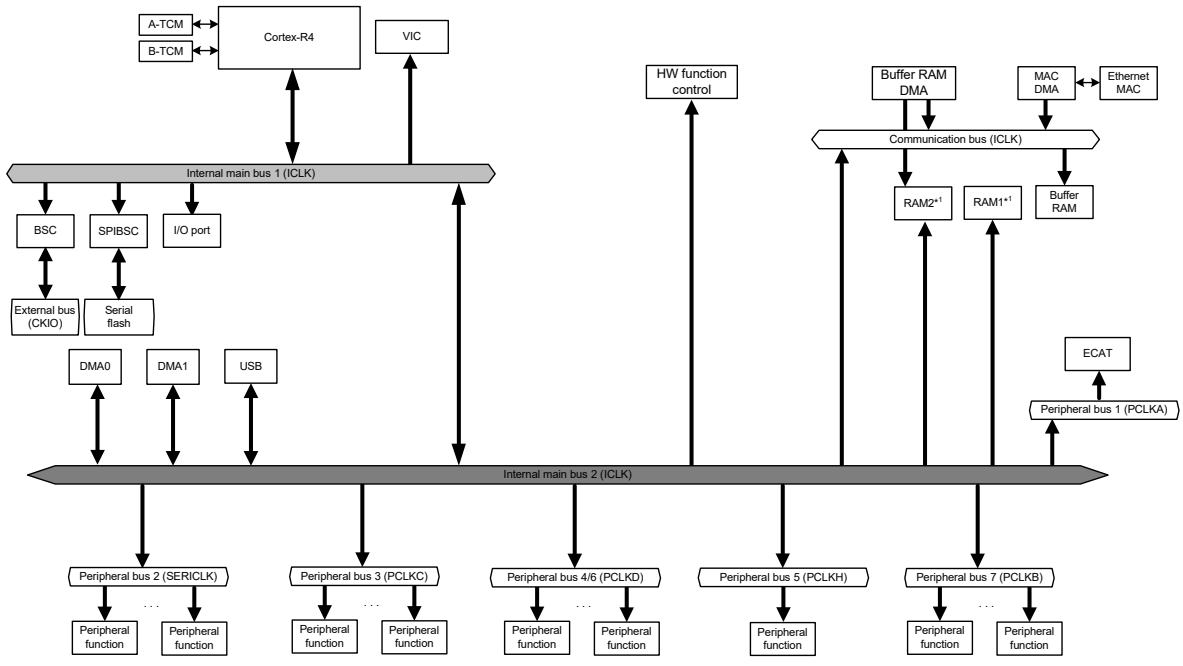
13.1 Overview

This product contains two internal memory buses, two memory buses, and multiple internal peripheral buses. Table 13.1 lists the specifications of internal buses and Figure 13.1 and Figure 13.2 show the internal bus configuration.

Table 13.1 Specifications of Internal Buses

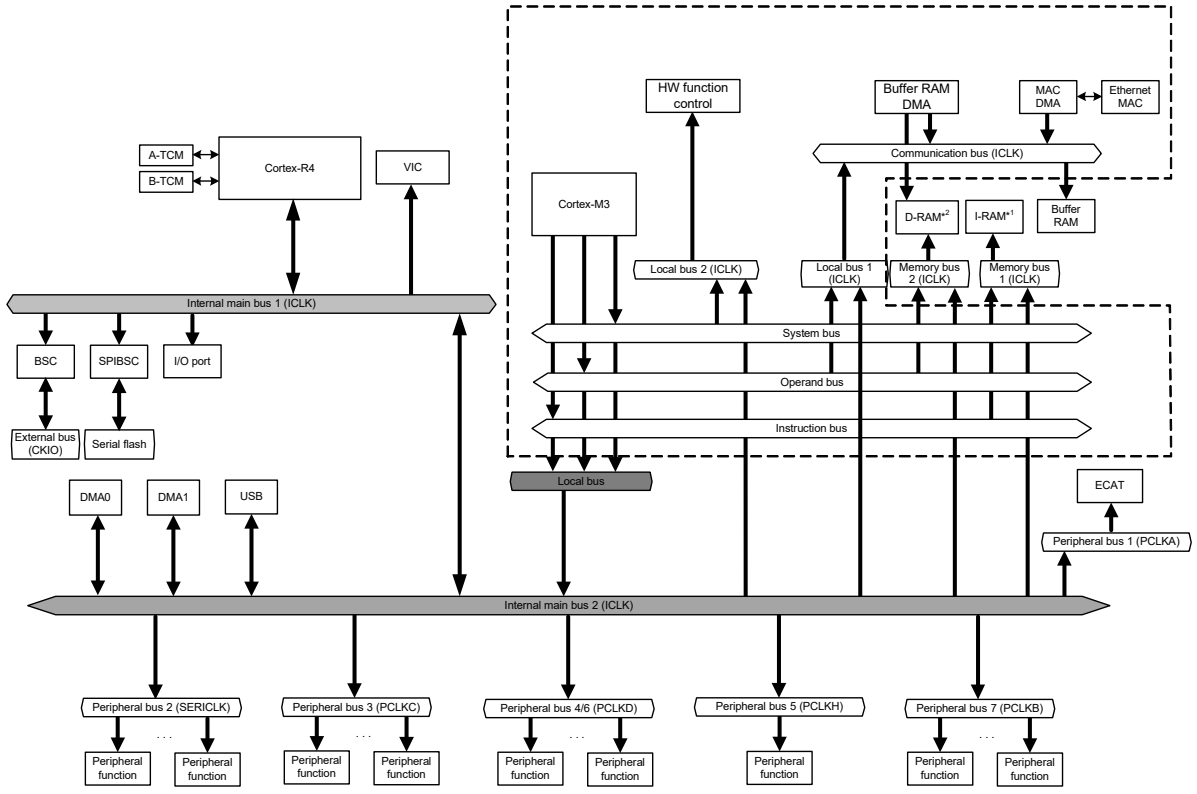
Internal Bus Type		Description
Internal main bus	Internal main bus 1	• Operates in synchronization with ICLK • Bus protocol: AMBA AXI • Priority order decision: Round-robin
	Internal main bus 2	• Operates in synchronization with ICLK • Bus protocol: AMBA AHB • Priority order decision: Round-robin with fixed priority order (DMA0 with top priority)
Memory buses 1 and 2 (only for products incorporating an R-IN engine)		Operates in synchronization with ICLK
Buses for Ethernet (buses other than the communication bus are only included in products incorporating an R-IN engine)	Instruction bus	Operates in synchronization with ICLK
	Operand bus	Operates in synchronization with ICLK
	System bus	Operates in synchronization with ICLK
	Communication bus	Operates in synchronization with ICLK
	Local bus 1	Operates in synchronization with ICLK
	Local bus 2	Operates in synchronization with ICLK
Peripheral bus 1 (only for products incorporating an EtherCAT (optional))	ECAT	Operates in synchronization with PCLKA
Peripheral bus 2	SCIFA, RSPIa	Operates in synchronization with SERICLK
Peripheral bus 3	GPTa, MTU3a	Operates in synchronization with PCLKC
Peripheral bus 4	CAN, CRC, ECM, DSMIF	Operates in synchronization with PCLKD
Peripheral bus 5	ADC	Operates in synchronization with PCLKH
Peripheral bus 6	ELC, TPU, POE3, PPG, CMT, CMTW, WDTA, IWDTa, RIIC, SSI, DOC, temperature sensor	Operates in synchronization with PCLKD
Peripheral bus 7	Clock generation circuit, CLMA	Operates in synchronization with PCLKB
External bus		Operates in synchronization with CKIO
External serial flash bus		Operates in synchronization with ICLK

Note: Peripheral bus 4 is divided internally into (CAN, CRC, ECM), and DSMIF. Moreover, peripheral buses 5, 6, and 7 are on the same slave layer, and are connected with internal main bus 2. Therefore, in products incorporating an R-IN Engine, even in case of simultaneous access to the CAN or DSMIF modules by both CPU cores, there will be no waiting. However, since the ADC (peripheral bus 5) and TPUa (peripheral bus 6) are on the same slave layer, there will be some waiting in case of simultaneous access by both CPU cores.



Note 1. Optional function depending on the product

Figure 13.1 Bus Configuration



Note 1. Instruction RAM (also accessible by the Cortex-R4)
Note 2. Data RAM (also accessible by the Cortex-R4)

Figure 13.2 Internal Bus Configuration (for products incorporating an R-IN engine)

13.2 Internal Main Bus

Internal main buses 1 and 2 of this LSI both have a multiple-layer structure. If bus masters request to access different bus slaves respectively, multiple accesses are processed in parallel. If bus masters request to access the same bus slave, priority order decision is performed and accesses are processed sequentially according to the priority order.
Table 13.2 lists the connection between the bus master and the bus slave for internal main bus 1, and Table 13.3 lists the bus master-slave connection for internal main bus 2.

Table 13.2 Internal Main Bus 1: Connection between Bus Master and Bus Slave

Bus Slave \ Bus Master	CPU (Cortex-R4)	Internal Main Bus 2
CPU (Cortex-R4)	A	A
I/O port	A	A
BSC	A	A
SPIBSC	A	A
VIC	A	A
Internal Main Bus 2	A	—

A: Accessible
—: Inaccessible

Table 13.3 Internal Main Bus 2: Connection between Bus Master and Bus Slave

Bus Slave \ Bus Master	Internal Main Bus 1	DMA0	DMA1	USB	CPU (Cortex-M3) (for products incorporating an R-IN engine)
Internal main bus 1	—	A	A	A	A
DMA0	A	—	—	—	A
DMA1	A	—	—	—	A
Instruction RAM	A	A	A	A	A
Data RAM	A	A	A	A	A
Buffer RAM	A	A	A	A	A
USB	A	A	A	—	A
Peripheral bus 1 (only for products incorporating an EtherCAT (optional))	A	A	A	—	A
Peripheral bus 2	A	A	A	—	A
Peripheral bus 3	A	A	A	—	A
Peripheral bus 4	A	A	A	—	A
Peripheral bus 5	A	A	A	—	A
Peripheral bus 6	A	A	A	—	A
Peripheral bus 7	A	A	A	—	A

A: Accessible
—: Inaccessible

14. Bus State Controller

The bus state controller outputs control signals for various types of memory and external devices that are connected to the external address space. The functions of this module enable this LSI to connect directly with SRAM, SDRAM, and other memory storage devices, and external devices.

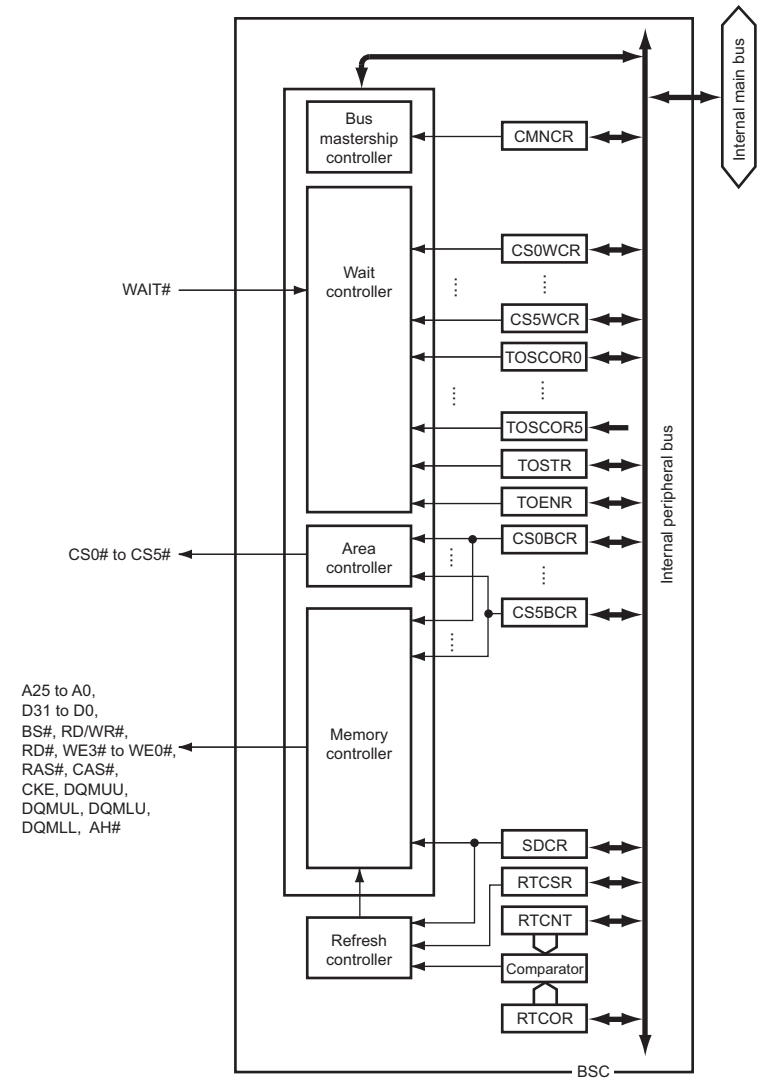
14.1 Features

Table 14.1 Bus State Controller Specifications

	Description
External address space	• A maximum of 64 Mbytes for each of areas CS0 to CS5. • Can specify the following for each CS space: SRAM interface, SRAM interface with byte selection, burst ROM (clocked synchronous or asynchronous), MPX-I/O, and SDRAM memory Data bus width (8, 16, or 32 bits) Insertion of wait cycles for each read access and write access. Can set independent idle cycles for the following five cases: Read-write (in same space/different spaces), read-read (in same space/different spaces), and the first cycle is a write access.
Various interfaces	SRAM interface Supports the interface that can directly connect to the SRAM.
	Burst ROM interface (clocked asynchronous) High-speed access to the ROM that has the page mode function.
	MPX-I/O interface Can directly connect to a peripheral LSI that needs an address/data multiplexing.
	SDRAM interface Can set the SDRAM in up to two areas.*1 Multiplex output for row address/column address. Efficient access by single read/single write. High-speed access in bank-active mode. Supports an auto-refresh and self-refresh. Supports a power-down mode. Issues MRS and EMRS commands.
	SRAM interface with byte selection Can connect directly to a SRAM with byte selection.
	Burst ROM interface (clocked synchronous) Can connect directly to a burst ROM of the clocked synchronous type.
Refresh function	Supports the auto-refresh and self-refresh functions. Specifies the refresh interval using the refresh counter and clock selection. Can execute concentrated refresh by specifying the refresh counts (1, 2, 4, 6, or 8). Usage as interval timer for refresh counter Generates an interrupt request at compare match.
External WAIT# pin	Detection of long wait state for access by the signal on the external WAIT# pin. A timeout detection condition is specifiable per CS space. Once timeout is detected, the external WAIT function is disabled and a timeout detection error request is issued.

Note 1. When connecting one SDRAM, set up the CS3 space for the SDRAM.

Figure 14.1 is a block diagram of the bus state controller.



CMNCR: Common control register*1
CSnWCR: CSn space wait control register (n = 0 to 5)
CSnBCR: CSn space bus control register (n = 0 to 5)
SDCR: SDRAM control register
RTCSR: Refresh timer control/status register
RTCNT: Refresh timer counter
RTCOR: Refresh time constant register
TOSCORn: Timeout cycle constant register (n = 0 to 5)
TOSTR: Timeout status register
TOENR: Timeout enable register

Note 1. For details of the CMNCR register, see section 15.2.11, Common Control Register (CMNCR).

Figure 14.1 Block Diagram of Bus State Controller

Table 14.2 lists the input/output pins of the bus state controller.

Table 14.2 Input/Output Pins of the Bus State Controller

Name	I/O	Function
A25 to A0	Output	Address output pins
D31 to D0	I/O	Data input/output pins
BS#	Output	Status signal output pin that indicates the start of the bus cycle
CS0# to CS5#	Output	Chip select signal output pins
RD/WR#	Output	Strobe signal output pin that indicates a read or write access Connect this pin to WE# pins when SDRAM or SRAM with byte selection is connected.
RD#	Output	Strobe signal output pin that indicates a read signal (read data output enable signal)
WE3#/DQMUU/AH#	Output	Write strobe signal output pin for D31 to D24 Connect this pin to the byte select pin when SRAM with byte selection is connected. Functions as the data mask enable signal output pin for D31 to D24 when SDRAM is connected. Functions as the address hold signal output pin when the MPX-I/O interface is used.
WE2#/DQMUL	Output	Write strobe signal output pin for D23 to D16 Connect this pin to the byte select pin when an SRAM with byte selection is connected. Functions as the data mask enable signal output pin for D23 to D16 when SDRAM is connected.
WE1#/DQMLU	Output	Write strobe signal output pin for D15 to D8 Connect this pin to the byte select pin when SRAM with byte selection is connected. Functions as the data mask enable signal output pin for D15 to D8 when SDRAM is connected.
WE0#/DQMLL	Output	Write strobe signal output pin for D7 to D0 Connect this pin to the byte select pin when SRAM with byte selection is connected. Functions as the data mask enable signal output pin for D7 to D0 when SDRAM is connected.
RAS#	Output	Low address strobe signal output pin for SDRAM. Connect this pin to RAS# pin of the SDRAM.
CAS#	Output	Column address strobe signal output pin for SDRAM. Connect this pin to CAS# pin of the SDRAM.
CKE	Output	Clock enable signal output pin for SDRAM. Connect this pin to CKE pin of the SDRAM.
WAIT#	Input	External wait control signal input pin used to insert a wait state into a bus cycle

14.2 Area Overview

14.2.1 Address Map

The kind of memory to be connected to the external address space and the data bus width are specified in each of CS0 to CS5 spaces. The address map for the external address space is listed below.

Table 14.3 Address Map

Internal Address	Space	Memory to be Connected
4000 0000h to 43FF FFFFh	CS0 mirror	SRAM interface, SRAM with byte selection, burst ROM (asynchronous or synchronous)
4400 0000h to 47FF FFFFh	CS1 mirror	SRAM interface, SRAM with byte selection
4800 0000h to 4BFF FFFFh	CS2 mirror	SRAM interface, SRAM with byte selection, SDRAM
4C00 0000h to 4FFF FFFFh	CS3 mirror	SRAM interface, SRAM with byte selection, SDRAM*1
5000 0000h to 53FF FFFFh	CS4 mirror	SRAM interface, SRAM with byte selection, burst ROM (asynchronous)
5400 0000h to 57FF FFFFh	CS5 mirror	SRAM interface, SRAM with byte selection, MPX-I/O
6000 0000h to 63FF FFFFh	CS0	SRAM interface, SRAM with byte selection, burst ROM (asynchronous or synchronous)
6400 0000h to 67FF FFFFh	CS1	SRAM interface, SRAM with byte selection
6800 0000h to 6BFF FFFFh	CS2	SRAM interface, SRAM with byte selection, SDRAM
6C00 0000h to 6FFF FFFFh	CS3	SRAM interface, SRAM with byte selection, SDRAM*1
7000 0000h to 73FF FFFFh	CS4	SRAM interface, SRAM with byte selection, burst ROM (asynchronous)
7400 0000h to 77FF FFFFh	CS5	SRAM interface, SRAM with byte selection, MPX-I/O

Note 1. When connecting one SDRAM, set up the CS3 space for the SDRAM.

14.2.2 Data Bus Width and Related Pin Setting for Each Area Depending on Boot Mode

The initial state of data bus width and settings of the pins related to this module depends on boot mode. For boot mode, refer to section 3, Operating Modes.

In 16-bit or 32-bit bus boot, the bus width of area 0 is automatically set to 16 or 32 bits, because this LSI is started up by the program stored in the ROM connected to area 0. For areas 1 to 5, the bus width and the memory to be connected can be changed by the program. Immediately after a power-on reset in these modes, some of the address and data-bus signals and the CS0# and RD# signals are automatically selected by default as the functions of the corresponding pins, since these signals are required to read ROM data from area 0. With the exception of these pins, the general purpose pin function is selected by default, and other required pin functions must be specified by software. Read access to area 0 is only permitted before the pin settings are completed.

In SPI boot modes, the state of areas 0 to 5 can be changed from the initial state by software, because the LSI is started by the program stored in the serial memory connected to the SPI space. Pin functions related to this module need to be set by software. Do not access external address spaces before the pin settings are completed.

Table 14.4 shows the initial state for individual boot modes and areas.

The sample access waveforms shown in this section include the pins such as BS#, RD/WR#, and WEn#. They are the waveforms when individual pin functions are enabled by the multi-function pin controller. For example, when 16-bit bus width is used in 32-bit bus boot mode, setting for pin A1 is needed. When 8-bit bus width is used, setting for pins A1 and A0 is also needed.

For details on pin function settings, see section 18, Multi-Function Pin Controller (MPC).

Table 14.4 Initial States for Individual Boot Modes and Areas

Boot Mode	Item	Area 0	Areas 1 to 5
16-bit bus boot	Data bus width	Fixed to 16 bits. Not changeable.	32 bits. Can be changed by program.
	Settings of pins related to this module	Pins A20 to A1, D15 to D0, CS0#, and RD# are set automatically. Other pins need to be set by program.	
32-bit bus boot	Data bus width	Fixed to 32 bits. Not changeable.	32 bits. Can be changed by program.
	Settings of pins related to this module	Pins A20 to A2, D31 to D0, CS0#, and RD# are set automatically. Other pins need to be set by program.	
SPI boot	Data bus width	32 bits. Can be changed by program.	
	Settings of pins related to this module	The initial value is the general I/O function. For external bus access, all the necessary pins need to be set by program.	

Note 1. In 16-bit bus boot or 32-bit bus boot, if an external memory that uses higher-order address lines than A21 is connected, the circuit board must include pull-down resistors for those address lines.

Note 2. The data-bus width may be limited by the type of memory in use. For details, see section 14.3.1, CSn Space Bus Control Register (CSnBCR) (n = 0 to 5).

14.3 Register Descriptions

14.3.1 CSn Space Bus Control Register (CSnBCR) (n = 0 to 5)

The CSnBCR register specifies the memory connected to each CS space, the number of idle cycles between bus cycles, and the bus width.

Do not access external memory for the corresponding area until CSnBCR initial setting and pin setting that are required for accessing the external memory are completed.

Idle cycles may be inserted even when they are not specified. For details, see section 14.4.10, Wait between Access Cycles.

Address(es): CS0BCR A000 2004h, CS1BCR A000 2008h, CS2BCR A000 200Ch, CS3BCR A000 2010h, CS4BCR A000 2014h, CS5BCR A000 2018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	IWW[2:0]			IWRWD[2:0]			IWRWS[2:0]			IWRRD[2:0]			IWRRS[2:0]		
Value after reset:	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	TYPE[2:0]			—	BSZ[1:0]		—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	1	1*1	0*1	0	0	0	0	0	0	0	0	0

Note 1. In 16-bit bus boot mode, 10b is set to the BSZ[1:0] bits of the CS0BCR register after a reset. In SPI boot mode and 32-bit bus boot mode, 11b is set. The BSZ[1:0] bits of the CSnBCR register (n = 1 to 5) after a reset is 11b.

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b10, b9	BSZ[1:0]	Data Bus Width Specification	Specify the data bus width of CS spaces. b10 b9 00: Reserved (setting prohibited) 01: 8-bit size 10: 16-bit size 11: 32-bit size For MPX-I/O, selects bus width by address Note 1. If area 5 is specified as MPX-I/O, setting these bits to 11b selects 8-bit or 16-bit bus width according to the address settings of the SZSEL bit in CS5WCR. Setting these bits to 01b or 10b selects the fixed bus with of 8-bit or 16-bit, respectively. Note 2. In 16-bit bus boot mode, 10b is automatically written to the BSZ[1:0] bits of the CS0BCR register. In 32-bit bus boot mode, 11b is automatically written. Note 3. If area 2 or area 3 is specified as SDRAM space, the bus width can be specified as either 16 bits or 32 bits. Note 4. If area 0 is specified as clocked synchronous burst ROM space, the bus width can be specified as either 16 bits or 32 bits.	R/W
b11	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W

Bit	Symbol	Bit Name	Description	R/W
b14 to b12	TYPE[2:0]	Memory Connected to a Space	Specify the type of memory connected to a CS space. b14 b12 000: Normal space 001: Burst ROM (clock asynchronous) 010: MPX-I/O 011: SRAM with byte selection 100: SDRAM 101: Reserved (setting prohibited) 110: Reserved (setting prohibited) 111: Burst ROM (clock synchronous) For details for memory type in each area, see Table 14.3. Note 1. When connecting the burst ROM to the CS0 space in 16-bit or 32-bit bus boot, change the CS0WCR register to the settings according to the burst ROM, and then set TYPE[2:0] to the burst ROM setting. In SPI boot mode, memory access should be performed after setting CS0BCR and CS0WCR. Note 2. Selecting SDRAM requires setting of the driving ability control register (DSCR) at the same time. For details, see section 17.3.6, Driving Ability Control Register (DSCR).	R/W
b15	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b18 to b16	IWRRS[2:0]	Idle State Insertion between Read-Read Cycles in the Same CS Space	Specify the number of idle cycles to be inserted after the access to an external memory that is connected to the CS space. The target cycle is a read-read cycle of which continuous access cycles are for the same CS space. b18 b16 000: No idle cycle inserted 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted	R/W
b21 to b19	IWRRD[2:0]	Idle State Insertion between Read-Read Cycles in Different CS Spaces	Specify the number of idle cycles to be inserted after the access to an external memory that is connected to the CS space. The target cycle is a read-read cycle of which continuous access cycles switch between different CS spaces. b21 b19 000: No idle cycle inserted 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted	R/W
b24 to b22	IWRWS[2:0]	Idle State Insertion between Read-Write Cycles in the Same CS Space	Specify the number of idle cycles to be inserted after the access to an external memory that is connected to the CS space. The target cycle is a read-write cycle of which continuous access cycles are for the same CS space. b24 b22 000: No idle cycle inserted 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted	R/W

Bit	Symbol	Bit Name	Description	R/W
b27 to b25	IWRWD[2:0]	Idle State Insertion between Read-Write Cycles in Different CS Spaces	Specify the number of idle cycles to be inserted after the access to an external memory that is connected to the CS space. The target access cycle is a read-write one in which continuous access cycles switch between different CS spaces. b27 b25 000: No idle cycle inserted 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted	R/W
b30 to b28	IWW[2:0]	Idle Cycles between Write-Read Cycles and Write-Write Cycles	These bits specify the number of idle cycles to be inserted after the access to an external memory that is connected to the CS space. The target access cycles are the write-read cycle and write-write cycle. b30 b28 000: No idle cycle inserted 001: 1 idle cycle inserted 010: 2 idle cycles inserted 011: 4 idle cycles inserted 100: 6 idle cycles inserted 101: 8 idle cycles inserted 110: 10 idle cycles inserted 111: 12 idle cycles inserted	R/W
b31	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W

14.3.2 CSn Space Wait Control Register (CSnWCR) (n = 0 to 5)

The CSnWCR register specifies various wait cycles for external memory access. The bit configuration of this register varies as shown below according to the memory type (TYPE2 to TYPE0) specified by the CSn space bus control register (CSnBCR). Specify CSnWCR before accessing the target area. Specify CSnBCR first, then specify CSnWCR.

(1) Normal Space, SRAM with Byte Selection, and MPX-I/O

- CS0WCR_0

Address(es): CS0WCR_0 A000 2028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—*1	BAS	—	—	—*1	—*1
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SW[1:0]		WR[3:0]				WM	—	—	—	—	HW[1:0]	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HW[1:0]	Delay States from RD#, WEn# Negation to Address, CS0# Negation	Specify the number of delay states from RD# and WEn# inactive to address and CS0# inactive. b1 b0 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles	R/W
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	WR[3:0]	Number of Access Waits	Specify the number of wait insertions that are necessary for read/write access. b10 b7 0000: No wait insertion 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b12, b11	SW[1:0]	Number of Delay Cycles from Address, CSn# Assertion to RD#, WEn# Assertion	Specify the number of delay cycle states from address and CS0# active to RD# and WEn# active. b12 b11 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	—*1	Reserved	Set these bits to 0 when the interfaces for SRAM or for SRAM with byte selection are used.	R/W
b19, b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b20	BAS	SRAM with Byte Selection Byte Access Select	Specifies the WE# and RD/WR# signal timing when the SRAM interface with byte selection is used. 0: Activates the WEn# signal at the read/write timing and activates the RD/WR# signal during the write access cycle. 1: Activates the WEn# signal during the read/write access cycle and activates the RD/WR# signal at the write timing.	R/W
b21	—*1	Reserved	Set this bit to 0 when the interfaces for SRAM or for SRAM with byte selection are used.	R/W
b31 to b22	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. In 16-bit or 32-bit bus boot mode, to connect the burst ROM to the CS0 space and switch to burst ROM interface after activation, set the TYPE[2:0] bits in CS0BCR after setting the burst number by the bits 20 and 21 and the burst wait cycle number by the bits 16 and 17. (For details on individual bits, see (2) and (4) of this section.) Do not write 1 to the reserved bits other than above bits.

- CS1WCR

Address(es): CS1WCR A000 202Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	BAS	—	WW[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SW[1:0]		WR[3:0]				WM	—	—	—	—	HW[1:0]	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HW[1:0]	Delay Cycles from RD#, WEn# Negation to Address, CS1# Negation	Specify the number of delay states from RD# and WEn# inactive to address and CS1# inactive. b1 b0 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles	R/W
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	WR[3:0]	Number of Read Access Waits	Specify the number of wait insertions that are necessary for read access. b10 b7 0000: No wait insertion 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b12, b11	SW[1:0]	Number of Delay Cycles from Address, CS1# Assertion to RD#, WEn# Assertion	Specify the number of delay states from address and CS1# active to RD# and WEn# active. b12 b11 00: 0.5 cycles 01: 1.5 cycles 10: 2.5 cycles 11: 3.5 cycles	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b18 to b16	WW[2:0]	Number of Write Access Waits	Specify the number of wait insertions that are necessary for write access. 000: The same as WR[3:0] setting (number of read access waits) b18 b16 001: No wait insertion 010: 1 cycle 011: 2 cycles 100: 3 cycles 101: 4 cycles 110: 5 cycles 111: 6 cycles	R/W
b19	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b20	BAS	SRAM with Byte Selection Byte Access Select	Specifies the WEn# and RD/WR# signal timing when the SRAM interface with byte selection is used. 0: Activates the WEn# signal at the read/write timing and activates the RD/WR# signal during the write access cycle. 1: Activates the WEn# signal during the read/write access cycle and activates the RD/WR# signal at the write timing.	R/W
b31 to b21	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

- CS2WCR_0, CS3WCR_0

Address(es): CS2WCR_0 A000 2030h, CS3WCR_0 A000 2034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	BAS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WR[3:0]				WM	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access waits is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	WR[3:0]	Number of Access Waits	Specify the number of waits that are necessary for read/write access. b10 b7 0000: No wait insertion 0001: 1 cycle 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles 0101: 5 cycles 0110: 6 cycles 0111: 8 cycles 1000: 10 cycles 1001: 12 cycles 1010: 14 cycles 1011: 18 cycles 1100: 24 cycles 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b19 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b20	BAS	SRAM with Byte Selection Byte Access Select	Specifies the WEn# and RD/WR# signal timing when the SRAM interface with byte selection is used. 0: Activates the WEn# signal at the read timing and activates the RD/WR# signal during the write access cycle. 1: Activates the WEn# signal during the read access cycle and activates the RD/WR# signal at the write timing.	R/W
b31 to b21	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

- CS4WCR_0

Address(es): CS4WCR_0 A000 2038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	BAS	—	WW[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SW[1:0]		WR[3:0]				WM	—	—	—	—	HW[1:0]	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HW[1:0]	Delay Cycles from RD#, WEn# Negation to Address, CS4# Negation	Specify the number of delay states from RD# and WEn# inactive to address and CS4# inactive. b1 b0 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access waits is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	WR[3:0]	Number of Read Access Waits	Specify the number of waits that are necessary for read access. b10 b7 0000: No wait insertion 0001: 1 wait 0010: 2 waits 0011: 3 waits 0100: 4 waits 0101: 5 waits 0110: 6 waits 0111: 8 waits 1000: 10 waits 1001: 12 waits 1010: 14 waits 1011: 18 waits 1100: 24 waits 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b12, b11	SW[1:0]	Number of Delay Cycles from Address, CS4# Assertion to RD#, WEn# Assertion	Specify the number of delay states from address and CS4# active to RD# and WEn# active. b12 b11 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b18 to b16	WW[2:0]	Number of Write Access Wait Cycles	Specify the number of wait inserts that are necessary for write access. b18 b16 000: The same as WR[3:0] setting (number of read access waits) 001: No wait insertion 010: 1 wait 011: 2 waits 100: 3 waits 101: 4 waits 110: 5 waits 111: 6 waits	R/W
b19	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b20	BAS	SRAM with Byte Selection Byte Access Select	Specifies the WEn# and RD/WR# signal timing when the SRAM interface with byte selection is used. 0: Activates the WEn# signal at the read timing and activates the RD/WR# signal during the write access cycle. 1: Activates the WEn# signal during the read access cycle and activates the RD/WR# signal at the write timing.	R/W
b31 to b21	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

- CS5WCR

Address(es): CS5WCR A000 203Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	SZSEL	MPXW/ BAS	—	WW[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SW[1:0]		WR[3:0]				WM	—	—	—	—	HW[1:0]	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HW[1:0]	Delay Cycles from RD#, WEn# to Address, CS5#	Specify the number of delay states from RD# and WEn# inactive to address and CS5# inactive when area 5 is specified as the SRAM interface or the SRAM interface with byte selection. When area 5 is specified as the MPX-I/O interface, these bits specify the number of delay states from RD# and WEn# inactive to CS5# inactive. b1 b0 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access waits is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	WR[3:0]	Number of Read Access Waits	Specify the number of waits that are necessary for read access. b10 b7 0000: No wait insertion 0001: 1 wait 0010: 2 waits 0011: 3 waits 0100: 4 waits 0101: 5 waits 0110: 6 waits 0111: 8 waits 1000: 10 waits 1001: 12 waits 1010: 14 waits 1011: 18 waits 1100: 24 waits 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W

Bit	Symbol	Bit Name	Description	R/W
b12, b11	SW[1:0]	Number of Delay Cycles from Address, CS5# Assertion to RD#, WEn# Assertion	Specify the number of delay states from address and CS5# active to RD# and WEn# active when area 5 is specified as the SRAM interface or the SRAM interface with byte selection. When area 5 is specified as the MPX-I/O interface, these bits specify the number of delay states from the end of the address cycle (Ta3) to RD# and WEn# active. b12 b11 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b18 to b16	WW[2:0]	Number of Write Access Waits	Specify the number of wait insertions that are necessary for write access. b18 b16 000: The same as WR[3:0] setting (number of read access waits) 001: No wait insertion 010: 1 wait 011: 2 waits 100: 3 waits 101: 4 waits 110: 5 waits 111: 6 waits	R/W
b19	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b20	MPXW	MPX-I/O Interface Address Cycle Wait	Specifies the address cycle wait for MPX-I/O interface. This bit setting is valid only when area 5 is specified as MPX-I/O. 0: Inserts no wait cycle 1: Inserts 1 wait cycle	R/W
	BAS	SRAM with Byte Selection Byte Access Select	Specifies the WEn# and RD/WR# signal timing when the SRAM interface with byte selection is used. This bit setting is valid only when area 5 is specified as SRAM with byte selection. 0: Activates the WEn# signal at the read timing and activates the RD/WR# signal during the write access cycle. 1: Activates the WEn# signal during the read access cycle and activates the RD/WR# signal at the write timing.	R/W
b21	SZSEL	MPX-I/O Interface Bus Width Specification	Specifies an address to select the bus width when the BSZ[1:0] of the CS5BCR register are specified as 11b. This bit is valid only when area 5 is specified as MPX-I/O. 0: Selects the bus width by address A14 1: Selects the bus width by address A21 The relationship between the SZSEL bit and bus width selected by A14 or A21 are summarized below.	R/W
b31 to b22	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

SZSEL	A14	A21	Bus Width
0	0	Not affected	8 bits
0	1	Not affected	16 bits
1	Not affected	0	8 bits
1	Not affected	1	16 bits

(2) Burst ROM (Clocked Asynchronous)

- CS0WCR_1

Address(es): CS0WCR_1 A000 2028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	BST[1:0]		—	—	BW[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	W[3:0]				WM	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access waits is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	W[3:0]	Number of Access Waits	Specify the number of waits to be inserted in the first access cycle. b10 b7 0000: No wait insertion 0001: 1 wait 0010: 2 waits 0011: 3 waits 0100: 4 waits 0101: 5 waits 0110: 6 waits 0111: 8 waits 1000: 10 waits 1001: 12 waits 1010: 14 waits 1011: 18 waits 1100: 24 waits 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b15 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	BW[1:0]	Number of Waits during Burst Access	Specify the number of waits to be inserted between the second or subsequent access cycles in burst access. b17 b16 00: No wait insertion 01: 1 wait 10: 2 waits 11: 3 waits	R/W
b19, b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

<table>
<tr><th>Bit</th><th>Symbol</th><th>Bit Name</th><th>Description</th><th>R/W</th></tr>
<tr><td>b21, b20</td><td>BST[1:0]</td><td>Burst Count Specification</td><td>Specify the burst count for 16-byte or more access. Do not set BST[1:0] to 11b.
<table><tr><th>Bus Width</th><th>BST[1:0]</th><th>Burst Count (16-Byte Access)</th></tr><tr><td>8 bits</td><td>00</td><td>16 burst × one time</td></tr><tr><td></td><td>01</td><td>4 burst × four times</td></tr><tr><td>16 bits</td><td>00</td><td>8 burst × one time</td></tr><tr><td></td><td>01</td><td>2 burst × four times</td></tr><tr><td></td><td>10</td><td>4-4 or 2-4-2 burst</td></tr><tr><td>32 bits</td><td>xx</td><td>4 burst × one time</td></tr></table>Note: For details, see Table 14.17, Relationship between Bus Width, Access Size, and Number of Bursts.</td><td>R/W</td></tr>
<tr><td>b31 to b22</td><td>—</td><td>Reserved</td><td>These bits are always read as 0. The write value should always be 0.</td><td>R/W</td></tr>
</table>

- CS4WCR_1

Address(es): CS4WCR_1 A000 2038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	BST[1:0]		—	—	BW[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SW[1:0]		W[3:0]				WM	—	—	—	—	HW[1:0]	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	HW[1:0]	Delay Cycles from RD#, WEn# to Address, CS4#	Specify the number of delay states from RD# and WEn# inactive to address and CS4# inactive. b1 b0 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b5 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access wait cycle is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	W[3:0]	Number of Access Waits	Specify the number of waits to be inserted in the first access cycle. b10 b7 0000: No wait insertion 0001: 1 wait 0010: 2 waits 0011: 3 waits 0100: 4 waits 0101: 5 waits 0110: 6 waits 0111: 8 waits 1000: 10 waits 1001: 12 waits 1010: 14 waits 1011: 18 waits 1100: 24 waits 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b12, b11	SW[1:0]	Number of Delay States from Address, CS4# Assertion to RD#, WEn# Assertion	Specify the number of delay states from address and CS4# active to RD# and WEn# active. b12 b11 00: 0.5 states 01: 1.5 states 10: 2.5 states 11: 3.5 states	R/W
b15 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	BW[1:0]	Number of Waits during Burst Access	Specify the number of waits to be inserted between the second or subsequent access cycles in burst access. b17 b16 00: No wait insertion 01: 1 wait 10: 2 waits 11: 3 waits	R/W

<table>
<tr><th>Bit</th><th>Symbol</th><th>Bit Name</th><th>Description</th><th>R/W</th></tr>
<tr><td>b19, b18</td><td>—</td><td>Reserved</td><td>These bits are always read as 0. The write value should always be 0.</td><td>R/W</td></tr>
<tr><td>b21, b20</td><td>BST[1:0]</td><td>Burst Count Specification</td><td>Specify the burst count for 16-byte or more access. Do not set these bits to 11b.
<table><tr><th>Bus Width</th><th>BST[1:0]</th><th>Burst Count (16-Byte Access)</th></tr><tr><td>8 bits</td><td>00</td><td>16 burst × one time</td></tr><tr><td></td><td>01</td><td>4 burst × four times</td></tr><tr><td>16 bits</td><td>00</td><td>8 burst × one time</td></tr><tr><td></td><td>01</td><td>2 burst × four times</td></tr><tr><td></td><td>10</td><td>4-4 or 2-4-2 burst</td></tr><tr><td>32 bits</td><td>xx</td><td>4 burst × one time</td></tr><tr><td>Note:</td><td colspan="2">For details, see Table 14.17, Relationship between Bus Width, Access Size, and Number of Bursts.</td></tr></table></td><td>R/W</td></tr>
<tr><td>b31 to b22</td><td>—</td><td>Reserved</td><td>These bits are always read as 0. The write value should always be 0.</td><td>R/W</td></tr>
</table>

(3) SDRAM*1

- CS2WCR_1

Address(es): CS2WCR_1 A000 2030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	A2CL[1:0]		—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8, b7	A2CL[1:0]	CAS Latency for Area 2	Specify the CAS latency for area 2. b8 b7 00: 1 01: 2 10: 3 11: 4	R/W
b9	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b10	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b31 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. If only one area is connected to the SDRAM, specify area 3. In this case, specify area 2 as normal space or SRAM with byte selection.

- CS3WCR_1

Address(es): CS3WCR_1 A000 2034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	WTRP[1:0]*1		—	WTRCD[1:0]*1		—	A3CL[1:0]		—	—	TRWL[1:0]*1		—	WTRC[1:0]*1	
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Note 1. If both areas 2 and 3 are specified as SDRAM, WTRP[1:0], WTRCD[1:0], TRWL[1:0], and WTRC[1:0] bit settings are used in both areas in common.

Bit	Symbol	Bit Name	Description	R/W
b1, b0	WTRC[1:0]*1	Number of Idle States from REF Command/Self-Refresh Release to ACTV/REF/MRS Command	Specify the number of minimum idle cycles in the periods shown below. • From the issuance of the REF command until the issuance of the ACTV/REF/MRS command • From releasing self-refresh until the issuance of the ACTV/REF/MRS command. The setting for areas 2 and 3 is common. b1 b0 00: 2 states 01: 3 states 10: 5 states 11: 8 states	R/W
b2	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b4, b3	TRWL[1:0]*1	Number of Auto-Precharge Startup Wait Cycles	Specify the number of minimum auto-precharge startup wait cycles as shown below. • State number from the issuance of the WRITA command by this LSI until the completion of auto-precharge in the SDRAM. Equivalent to the state number from the issuance of the WRITA command until the issuance of the ACTV command. Confirm that how many states are required between the WRITA command receive in the SDRAM and the auto-precharge activation, referring to each SDRAM data sheet. And set the state number so as not to exceed the state number specified by this bit. • State number from the issuance of the WRIT command until the issuance of the PRE command. This is the case when accessing another low address in the same bank in bank active mode. The setting for areas 2 and 3 is common. b4 b3 00: No wait insertion 01: 1 state 10: 2 states 11: 3 states	R/W
b6, b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8, b7	A3CL[1:0]	CAS Latency for Area 3	Specify the CAS latency for area 3. b8 b7 00: 1 01: 2 10: 3 11: 4	R/W
b9	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b11, b10	WTRCD [1:0]*1	Number of Waits between ACTV Command and READ(A)/WRIT(A) Command	Specify the minimum number of waits from issuing the ACTV command to issuing the READ(A)/WRIT(A) command. The setting for areas 2 and 3 is common. b11 b10 00: No wait insertion 01: 1 wait 10: 2 waits 11: 3 waits	R/W
b12	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14, b13	WTRP[1:0]*1	Number of Auto-Precharge Completion Wait States	Specify the number of minimum precharge completion wait states as shown below. • From the start of auto-precharge and issuing of ACTV command for the same bank • From issuing of the PRE/PALL command to issuing of the ACTV command for the same bank • Till entering the power-down mode or deep power-down mode • From the issuing of PALL command to issuing REF command in auto refresh mode • From the issuing of PALL command to issuing SELF command in self refresh mode The setting for areas 2 and 3 is common. b14 b13 00: No wait insertion 01: 1 state 10: 2 states 11: 3 states	R/W
b31 to b15	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note 1. If both areas 2 and 3 are specified as SDRAM, WTRP[1:0], WTRCD[1:0], TRWL[1:0], and WTRC[1:0] bit settings are used in both areas in common.
If only one area is connected to the SDRAM, specify area 3. In this case, specify area 2 as SRAM interface or SRAM with byte selection.

(4) Burst ROM (Clocked Synchronous)

- CS0WCR_2

Address(es): CS0WCR_2 A000 2028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BW[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	W[3:0]				WM	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b6	WM	External Wait Mask Specification	Specifies whether or not the external wait input is valid. The specification by this bit is valid even when the number of access waits is 0. 0: External wait input is valid 1: External wait input is ignored	R/W
b10 to b7	W[3:0]	Number of Access Waits	Specify the number of waits to be inserted in the first access cycle. b10 b7 0000: No wait insertion 0001: 1 wait 0010: 2 waits 0011: 3 waits 0100: 4 waits 0101: 5 waits 0110: 6 waits 0111: 8 waits 1000: 10 waits 1001: 12 waits 1010: 14 waits 1011: 18 waits 1100: 24 waits 1101: Reserved (setting prohibited) 1110: Reserved (setting prohibited) 1111: Reserved (setting prohibited)	R/W
b15 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	BW[1:0]	Number of Burst Wait Cycles	Specify the number of waits to be inserted between the second or subsequent access cycles in burst access. b17 b16 00: No wait insertion 01: 1 wait 10: 2 waits 11: 3 waits	R/W
b31 to b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.3 SDRAM Control Register (SDCR)

The SDCR register specifies the method to refresh and access SDRAM, and the types of SDRAMs to be connected.

Address(es): A000 204Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	A2ROW[1:0]		—	A2COL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DEEP	—	RFSH	RMODE	PDOWN	BACTV	—	—	—	A3ROW[1:0]		—	A3COL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	A3COL[1:0]	Number of Bits of Column Address for Area 3	Specify the number of bits of the column address for area 3. b1 b0 00: 8 bits 01: 9 bits 10: 10 bits 11: Reserved (setting prohibited)	R/W
b2	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b4, b3	A3ROW[1:0]	Number of Bits of Row Address for Area 3	Specify the number of bits of the row address for area 3. b4 b3 00: 11 bits 01: 12 bits 10: 13 bits 11: Reserved (setting prohibited)	R/W
b7 to b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	BACTV	Bank Active Mode	Specifies to access whether in auto-precharge mode (using READA and WRITA commands) or in bank active mode (using READ and WRIT commands). 0: Auto-precharge mode (using READA and WRITA commands) 1: Bank active mode (using READ and WRIT commands) Note: Bank active mode can be set only for area 3. When both areas 2 and 3 are set to SDRAM, specify the auto-precharge mode.	R/W
b9	PDOWN	Power-Down Mode	Specifies whether the SDRAM will enter the power-down mode after the access to the SDRAM. With this bit being set to 1, after the SDRAM is accessed, the CKE signal is driven low and the SDRAM enters the power-down mode. 0: The SDRAM does not enter the power-down mode after being accessed. 1: The SDRAM enters the power-down mode after being accessed.	R/W
b10	RMODE	Refresh Mode	Specifies whether to perform auto-refresh or self-refresh when the RFSH bit is 1. When the RFSH bit is 1 and this bit is 1, self-refresh starts immediately. When the RFSH bit is 1 and this bit is 0, auto-refresh starts according to the contents that are set in registers RTCSR, RTCNT, and RTCOR. 0: Auto-refresh is performed 1: Self-refresh is performed	R/W

Bit	Symbol	Bit Name	Description	R/W
b11	RFSH	Refresh Control	Specifies the refresh control for the SDRAM. 0: No refresh 1: Refresh	R/W
b12	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b13	DEEP	Deep Power-Down Mode	This bit is valid for low-power SDRAM. If the RFSH or RMODE bit is set to 1 while this bit is set to 1, the deep power-down entry command is issued and the low-power SDRAM enters the deep power-down mode. 0: Self-refresh mode 1: Deep power-down mode	R/W
b15, b14	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	A2COL[1:0]	Number of Bits of Column Address for Area 2	Specify the number of bits of column address for area 2. b17 b16 00: 8 bits 01: 9 bits 10: 10 bits 11: Reserved (setting prohibited)	R/W
b18	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b20, b19	A2ROW[1:0]	Number of Bits of Row Address for Area 2	Specify the number of bits of row address of the SDRAM connected to area 2. b20 b19 00: 11 bits 01: 12 bits 10: 13 bits 11: Reserved (setting prohibited)	R/W
b31 to b21	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.4 Refresh Timer Control/Status Register (RTCSR)

The RTCSR register specifies various items about refresh for SDRAM.
When RTCSR is written, the upper 16 bits of the write data must be A55Ah to cancel write protection.
The phase of the clock for incrementing the count in the refresh timer counter (RTCNT) is adjusted only by a power-on reset. Note that there is an error in the time until the compare match flag is set for the first time after the timer is started with the CKS[2:0] bits being set to a value other than 000b.

Address(es): A000 2050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMF	CMIE	CKS[2:0]			RRC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	RRC[2:0]	Refresh Count	Specify the number of continuous refresh cycles, when the refresh request occurs after the coincidence of the values of the refresh timer counter (RTCNT) and the refresh time constant register (RTCOR). These bits can make the period of occurrence of refresh long. b2 b0 000: 1 time 001: 2 times 010: 4 times 011: 6 times 100: 8 times 101: Reserved (setting prohibited) 110: Reserved (setting prohibited) 111: Reserved (setting prohibited)	R/W
b5 to b3	CKS[2:0]	Clock Select	Select the clock input to count-up the refresh timer counter (RTCNT). b5 b3 000: Stop the counting-up 001: CKIO/4 010: CKIO/16 011: CKIO/64 100: CKIO/256 101: CKIO/1024 110: CKIO/2048 111: CKIO/4096	R/W
b6	CMIE	Compare Match Interrupt Enable	Enables or disables CMF interrupt requests when the CMF bit in RTCSR is set to 1. 0: Disables CMF interrupt requests. 1: Enables CMF interrupt requests.	R/W
b7	CMF	Compare Match Flag	Indicates that a compare match occurs between the refresh timer counter (RTCNT) and refresh time constant register (RTCOR). This bit is set or cleared in the following conditions. 0: Clearing condition: When 0 is written in CMF after reading out RTCSR during CMF = 1. 1: Setting condition: When the condition RTCNT = RTCOR is satisfied.	R/W
b31 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.5 Refresh Timer Counter (RTCNT)

RTCNT is an 8-bit counter that increments using the clock selected by bits CKS[2:0] in RTCSR. When RTCNT matches RTCOR, RTCNT is cleared to 0. The value in RTCNT returns to 0 after counting up to 255. When the RTCNT is written, the upper 16 bits of the write data must be A55Ah to cancel write protection.

Address(es): A000 2054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0			8-Bit Counter	R/W
b31 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.6 Refresh Time Constant Register (RTCOR)

RTCOR is an 8-bit register. When RTCOR matches RTCNT, the CMF bit in RTCSR is set to 1 and RTCNT is cleared to 0.

When the RFSH bit in SDCR is 1, a memory refresh request is issued by this matching signal. This request is maintained until the refresh operation is performed. If the request is not processed when the next matching occurs, the previous request is ignored.

When the CMIE bit in RTCSR is set to 1, an interrupt request (BSCCMI) is issued by this matching signal. The request continues to be output until the CMF bit in RTCSR is cleared. Clearing the CMF bit only affects the interrupt request and does not clear the refresh request. Therefore, a combination of refresh request and interval timer interrupt can be specified so that the number of refresh requests are counted by using timer interrupts while refresh is performed periodically.

When RTCOR is written, the upper 16 bits of the write data must be A55Ah to cancel write protection.

Address(es): A000 2058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0			8-Bit Register	R/W
b31 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.7 Timeout Cycle Constant Register (TOSCORn) (n = 0 to 5)

TOSCORn is a 16-bit register the value of which is effective when the WM bit in the CSn space wait control register (CSnWCR) is 0 and the corresponding bit in the timeout enable register (TOENR) is 1. When the number of cycles of waiting due to the signal on the external wait input pin matches the setting of TOSCORn, the wait state is forcibly interrupted (external wait input is disabled) to end the cycle of access, the timeout status flag for the corresponding space in the timeout status register (TOSTR) is set, and a timeout detection error request from the external WAIT# pin is generated. The timeout detection error request is retained until the corresponding bit in the TOENR register is set to 0, or 0 is written to the timeout status flag for the corresponding space. Note that timeout detection is enabled even while the timeout status flag for the corresponding space in the TOSTR register is 1, and the wait state is forcibly interrupted (external wait input is disabled) to end the cycle of access in response to a further timeout.

Address(es): TOSCOR0: A000 2060h, TOSCOR1: A000 2064h, TOSCOR2: A000 2068h, TOSCOR3: A000 206Ch, TOSCOR4: A000 2070h, TOSCOR5: A000 2074h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0		16-Bit Register	When the number of external wait cycles matches the setting value of these bits, the timeout interrupt occurs and the wait state is forcibly interrupted to end the cycle of access. 0000h: 65536 (number of external wait cycles) 0001h: 1 : FFFFh: 65535	R/W
b31 to b16	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.8 Timeout Status Register (TOSTR)

This register is used for status of the external wait input. When the WM bit in the CSn space wait control register (CSnWCR) is 0 and the corresponding bit in the timeout enable register (TOENR) is 1 and the number of waits in response to the signal on the external wait input matches the setting of TOSCORn, the timeout status flag for the corresponding space is set and a timeout detection error request is generated. The only writable value for the timeout status flags is 0, which clears the flag. Writing 1 to a flag is ignored.

Address(es): A000 2080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CS5TOSTF	CS4TOSTF	CS3TOSTF	CS2TOSTF	CS1TOSTF	CS0TOSTF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CS0TOSTF	CS0 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS0 space has matched the setting of the CS0 space timeout cycle constant register (TOSCOR0). This bit is set or cleared in the following conditions. 0: Clearing condition When 0 is written in CS0TOSTF. 1: Setting condition When the WM bit in the CS0 space wait control register (CS0WCR) is 0 and the CS0TOEN bit in the timeout enable register (TOENR) is 1, the number of cycles of waiting due to the input on the external wait pin during access to the CS0 space has matched the setting of the TOSCOR0 register.	R/W
b1	CS1TOSTF	CS1 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS1 space has matched the setting of the CS1 space timeout cycle constant register (TOSCOR1). For the condition to set or clear this bit, refer to the description of CS0TOSTF.	R/W
b2	CS2TOSTF	CS2 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS2 space has matched the setting of the CS2 space timeout cycle constant register (TOSCOR2). For the condition to set or clear this bit, refer to the description of CS0TOSTF.	R/W
b3	CS3TOSTF	CS3 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS3 space has matched the setting of the CS3 space timeout cycle constant register (TOSCOR3). For the condition to set or clear this bit, refer to the description of CS0TOSTF.	R/W
b4	CS4TOSTF	CS4 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS4 space has matched the setting of the CS4 space timeout cycle constant register (TOSCOR4). For the condition to set or clear this bit, refer to the description of CS0TOSTF.	R/W

Bit	Symbol	Bit Name	Description	R/W
b5	CS5TOSTF	CS5 Space Timeout Status Flag	Status flag that indicates that the number of cycles of waiting due to the input on the external wait pin during access to the CS5 space has matched the setting of the CS5 space timeout cycle constant register (TOSCOR5). For the condition to set or clear this bit, refer to the description of CS0TOSTF.	R/W
b31 to b6	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.9 Timeout Enable Register (TOENR)

This register is used to enable or disable timeout detection function for each space.

Address(es): A000 2084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CS5TOEN	CS4TOEN	CS3TOEN	CS2TOEN	CS1TOEN	CS0TOEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CS0TOEN	CS0 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS0 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b1	CS1TOEN	CS1 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS1 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b2	CS2TOEN	CS2 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS2 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b3	CS3TOEN	CS3 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS3 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b4	CS4TOEN	CS4 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS4 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b5	CS5TOEN	CS5 Space Timeout Detection Enable	Specifies enabling or disabling the detection of timeout for waiting in the CS5 space. 0: The timeout detection is disabled. 1: The timeout detection is enabled.	R/W
b31 to b6	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

14.3.10 CKIO Control Register (CKIOSET)

This register should be left at its initial value. If the setting is to be changed, set the CKIOSET[3:0] bits to 0h.
The procedure for writing to CKIOSET is shown below. Execute the following access operations consecutively.
Write 1 byte with any value to register CKIOKEY.
Write 1 byte with any value to register CKIOKEY.
Write 0000 0000h to the CKIOSET[3:0] bits.

Address(es): A000 2C0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CKIOSET[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CKIOSET[3:0]		Set the CKIOSET[3:0] bits to 0h (the value after reset).	R/W
b31 to b4	—	Reserved	When writing, always write 0.	R/W

14.3.11 CKIOSET Protection Register (CKIOKEY)

This register is a protection register of the CKIOSET register. For how to access to CKIOSET, see section 14.3.10.

Address(es): A000 2CFCh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKIOKEY[7:0]							
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CKIOKEY[7:0]		CKIOSET protection register	W

14.4 Operation

14.4.1 Access Size and Data Alignment

This LSI supports little endian, in which the least significant byte (LSB) is that in the direction of the 0th address.
Data bus width can be selected from 8 bits, 16 bits, and 32 bits for the normal memory and SRAM with byte selection.
Data bus width can be selected from 16 bits and 32 bits for SDRAM. For MPX-I/O, the data bus width is fixed to either 8 or 16 bits, or made selectable as 8 bits or 16 bits by one of the address lines.
Data bus width varies depending on boot mode. For details, refer to section 14.2.2, Data Bus Width and Related Pin Setting for Each Area Depending on Boot Mode.
Data alignment is performed in accordance with the data bus width selected for the device. This also means that four read operations are required to read 32-bit data from a byte-width device. In this LSI, data alignment and conversion of data length is performed automatically between the respective interfaces.
Table 14.5 to Table 14.7 show the relationship between device data width and access unit.

Table 14.5 32-Bit External Device Access and Data Alignment in Little Endian

	Data Bus				Strobe Signals			
Operation	**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**	**WE3#, DQMUU**	**WE2#, DQMUL**	**WE1#, DQMLU**	**WE0#, DQMLL**
8-bit access at address 0	—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 1	—	—	Data 7 to 0	—	—	—	Active	—
8-bit access at address 2	—	Data 7 to 0	—	—	—	Active	—	—
8-bit access at address 3	Data 7 to 0	—	—	—	Active	—	—	—
16-bit access at address 0	—	—	Data 15 to 8	Data 7 to 0	—	—	Active	Active
16-bit access at address 2	Data 15 to 8	Data 7 to 0	—	—	Active	Active	—	—
32-bit access at address 0	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0	Active	Active	Active	Active

Table 14.6 16-Bit External Device Access and Data Alignment in Little Endian

		Data Bus				Strobe Signals			
Operation		**D31 to D24**	**D23 to D16**	**D15 to D8**	**D7 to D0**	**WE3#, DQMUU**	**WE2#, DQMUL**	**WE1#, DQMLU**	**WE0#, DQMLL**
8-bit access at address 0		—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 1		—	—	Data 7 to 0	—	—	—	Active	—
8-bit access at address 2		—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 3		—	—	Data 7 to 0	—	—	—	Active	—
16-bit access at address 0		—	—	Data 15 to 8	Data 7 to 0	—	—	Active	Active
16-bit access at address 2		—	—	Data 15 to 8	Data 7 to 0	—	—	Active	Active
32-bit access at address 0	1st access at address 0	—	—	Data 15 to 8	Data 7 to 0	—	—	Active	Active
	2nd access at address 2	—	—	Data 31 to 24	Data 23 to 16	—	—	Active	Active

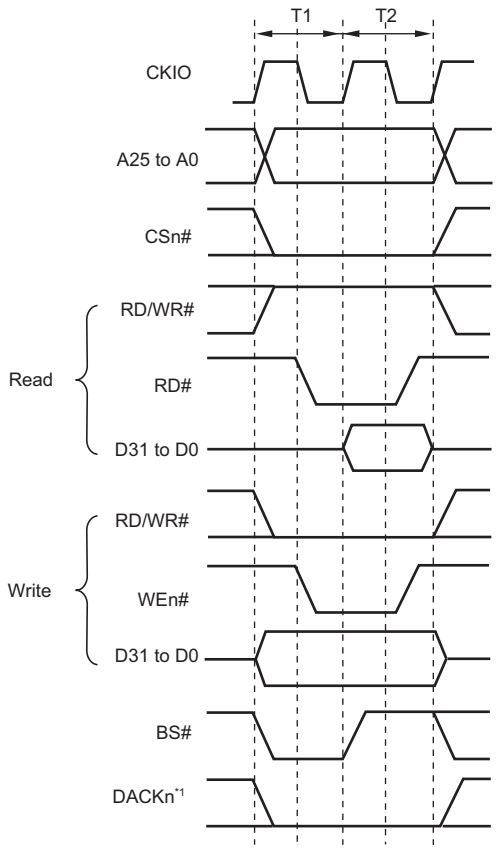
Table 14.7 8-Bit External Device Access and Data Alignment in Little Endian

Operation		Data Bus				Strobe Signals			
		D31 to D24	D23 to D16	D15 to D8	D7 to D0	WE3#, DQMUU	WE2#, DQMUL	WE1#, DQMLU	WE0#, DQMLL
8-bit access at address 0		—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 1		—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 2		—	—	—	Data 7 to 0	—	—	—	Active
8-bit access at address 3		—	—	—	Data 7 to 0	—	—	—	Active
16-bit access at address 0	1st access at address 0	—	—	—	Data 7 to 0	—	—	—	Active
	2nd access at address 1	—	—	—	Data 15 to 8	—	—	—	Active
16-bit access at address 2	1st access at address 0	—	—	—	Data 7 to 0	—	—	—	Active
	2nd access at address 1	—	—	—	Data 15 to 8	—	—	—	Active
32-bit access at address 0	1st access at address 0	—	—	—	Data 7 to 0	—	—	—	Active
	2nd access at address 1	—	—	—	Data 15 to 8	—	—	—	Active
	3rd access at address 2	—	—	—	Data 23 to 16	—	—	—	Active
	4th access at address 3	—	—	—	Data 31 to 24	—	—	—	Active

14.4.2 SRAM Interface

(1) Basic Timing

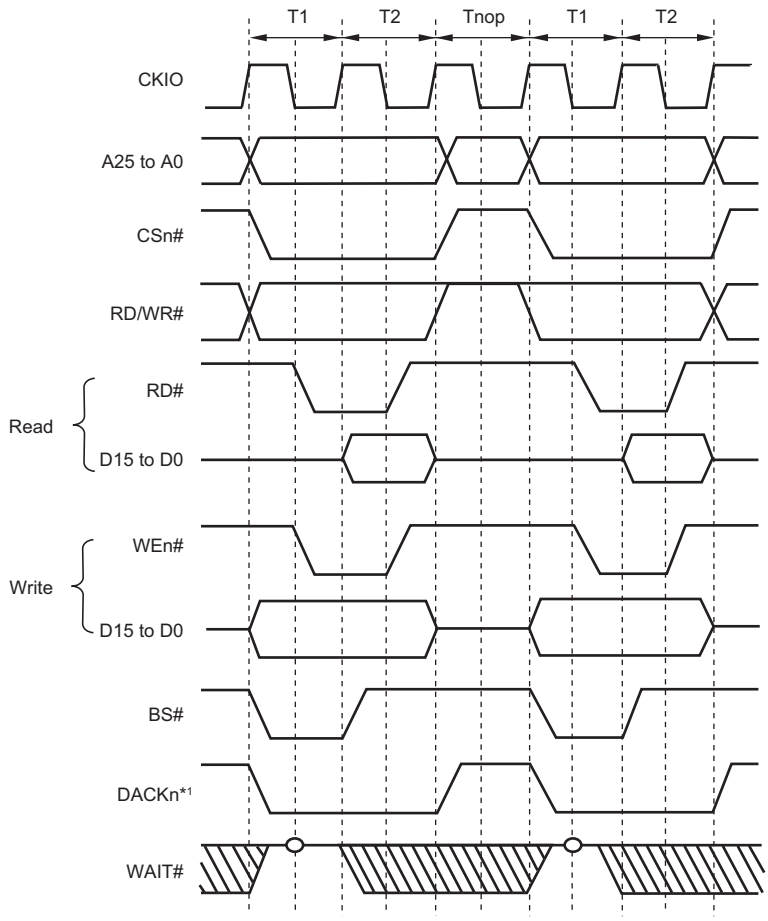
For access to an SRAM interface, this LSI uses strobe signal output in consideration of the fact that mainly static RAM will be directly connected. When using SRAM with a byte-selection pin, see section 14.4.8, SRAM Interface with Byte Selection. Figure 14.2 shows the basic timings of SRAM interface access. A no-wait normal access is completed in two cycles. The BS# signal is activated for one state to indicate the start of a bus cycle.



Note 1. The waveform for DACKn is when active low is specified.

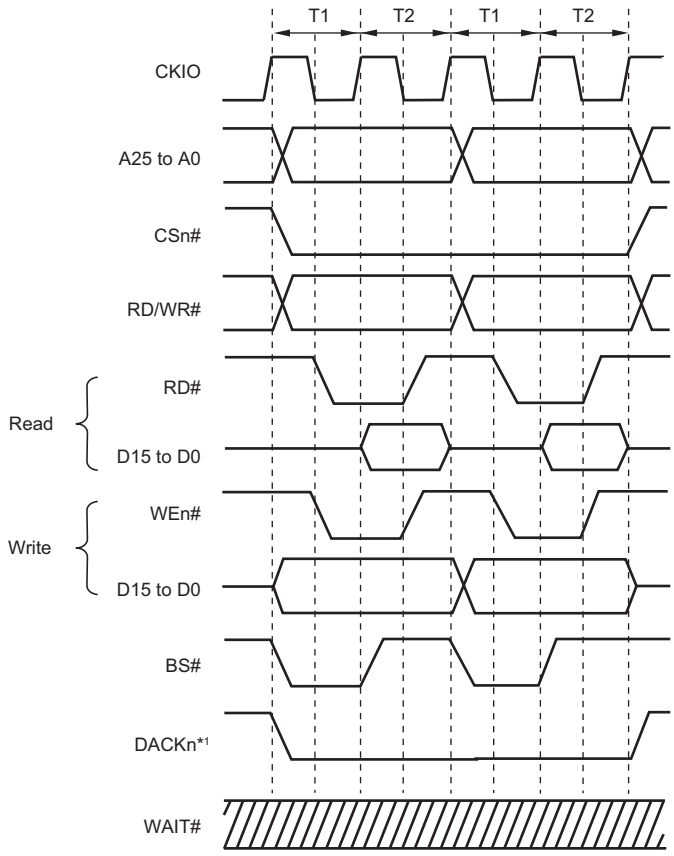
Figure 14.2 SRAM Interface Basic Access Timing (Access Wait 0)

There is no access size specification when reading. The correct access start address is output in the least significant bit of the address, but since there is no access size specification, 32 bits are always read in case of a 32-bit device. 16 bits are always read in case of a 16-bit device. When writing, only the WEn# signal for the byte to be written is activated.
It is necessary to output the data that has been read using RD# when a buffer is established in the data bus. The RD/WR# signal is in a read state (high output) when no access has been carried out. Therefore, care must be taken when controlling the external data buffer with this signal, to avoid output collision.
Figure 14.3 and Figure 14.4 show the basic timings in continuous access to the SRAM interface. If the WM bit in CSnWCR is cleared to 0, a Tnop cycle is inserted after the CSn space access to sample the external wait (Figure 14.3). If the WM bit in CSnWCR is set to 1, external waits are ignored and no Tnop cycle is inserted (Figure 14.4).



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.3 Continuous Access to the SRAM Interface (1)
Bus Width = 16 Bits, 32-Bit Access, CSnWCR.WM Bit = 0 (Access Wait = 0, Cycle Wait = 0)



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.4 Continuous Access to the SRAM Interface (2)
Bus Width = 16 Bits, 32-Bit Access, CSnWCR.WM Bit = 1 (Access Wait = 0, Cycle Wait = 0)

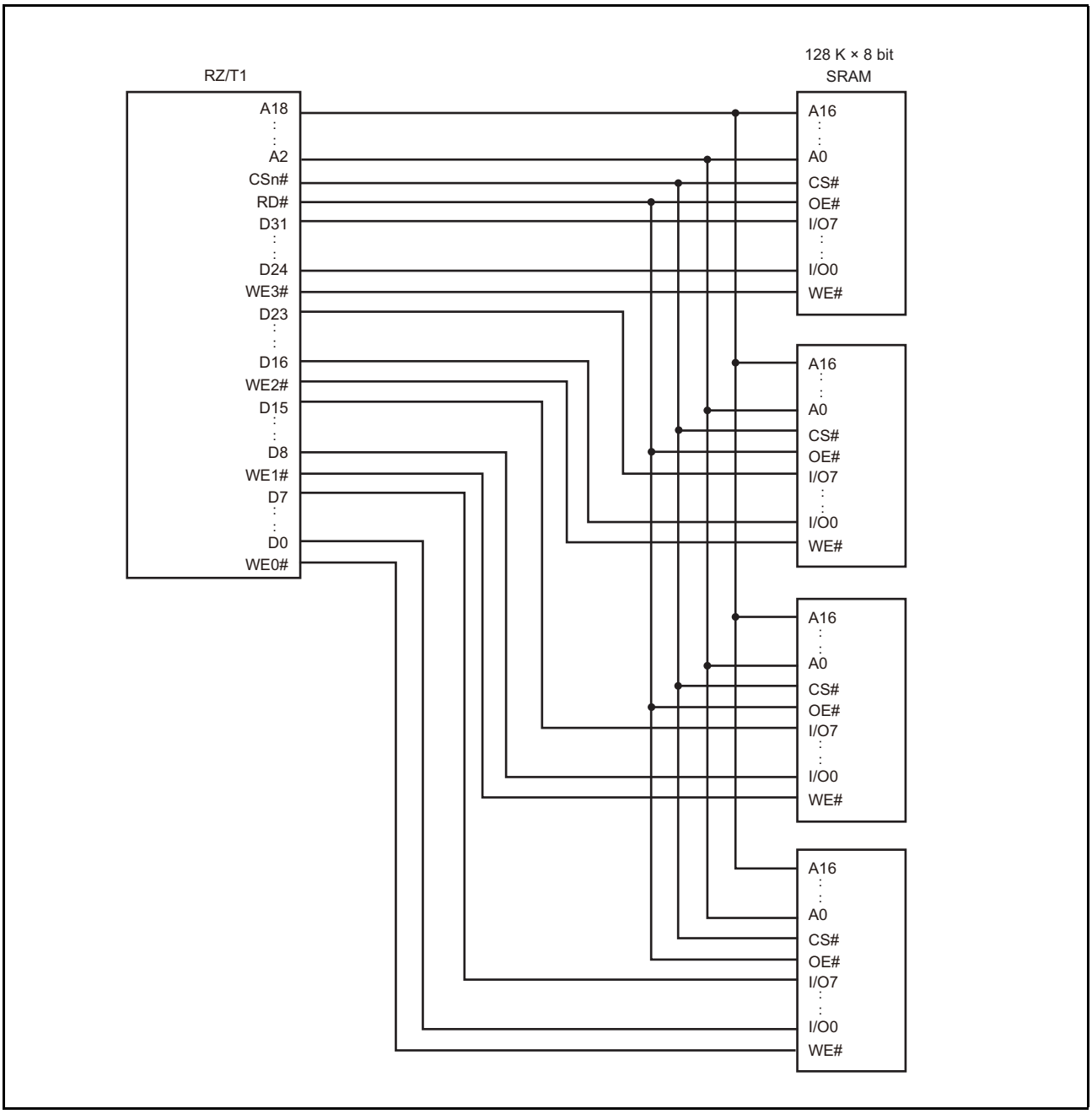


Figure 14.5 Example of 32-Bit Data-Width SRAM Connection

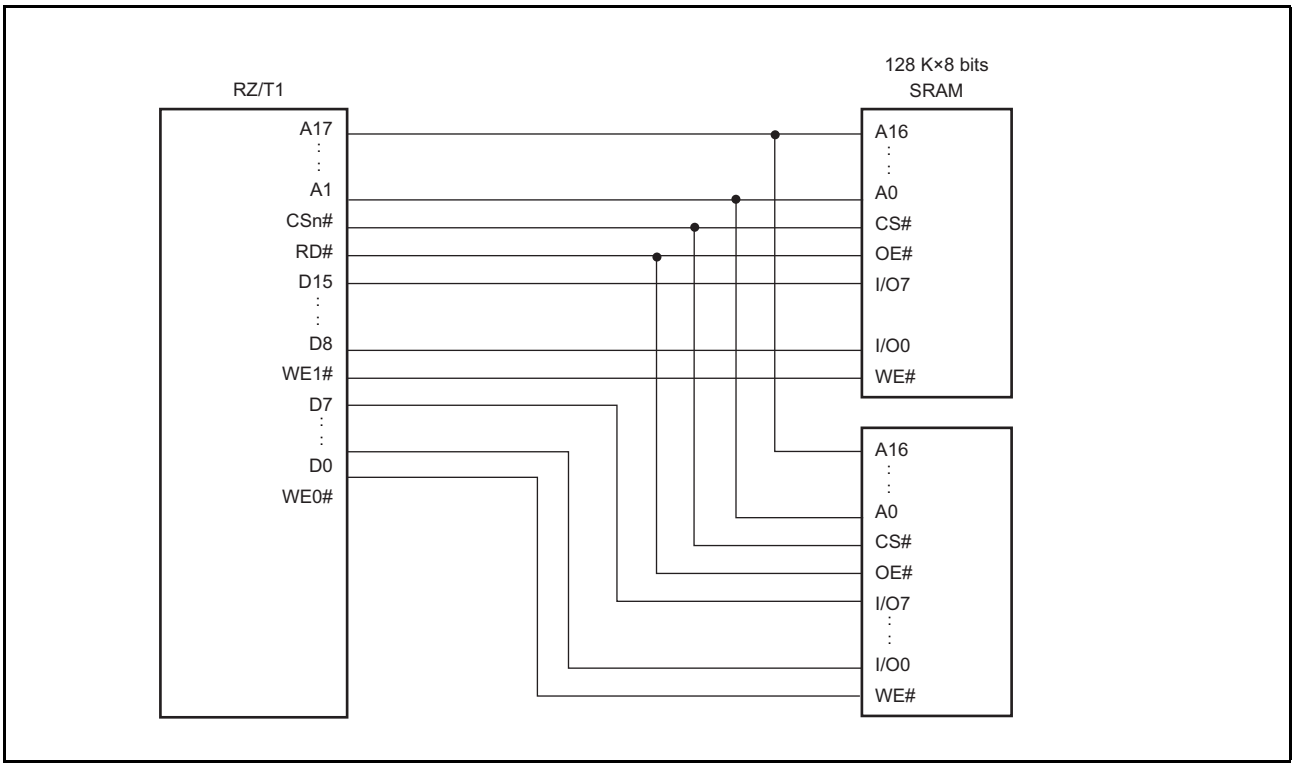


Figure 14.6 Example of 16-Bit Data-Width SRAM Connection

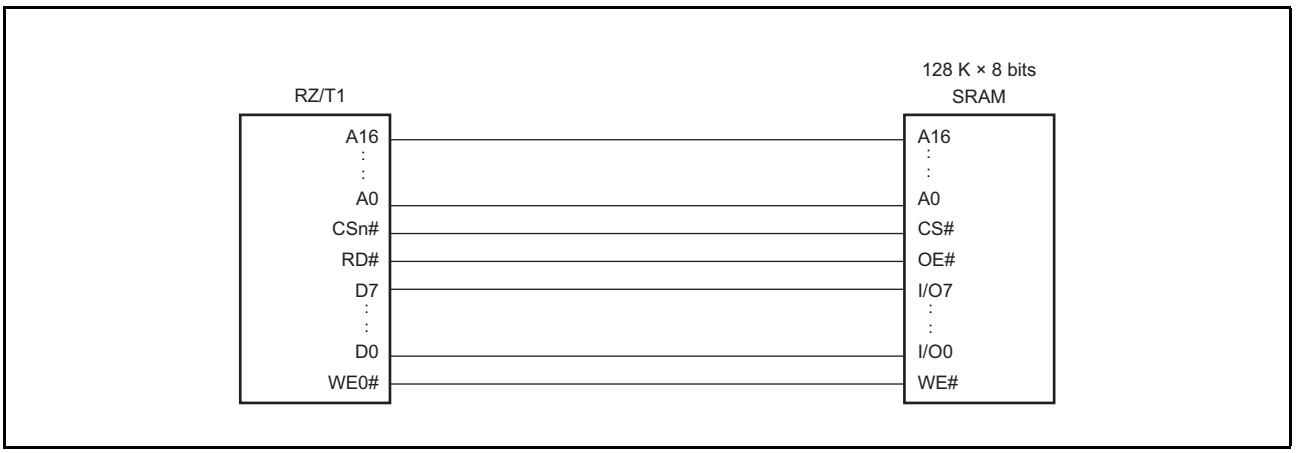
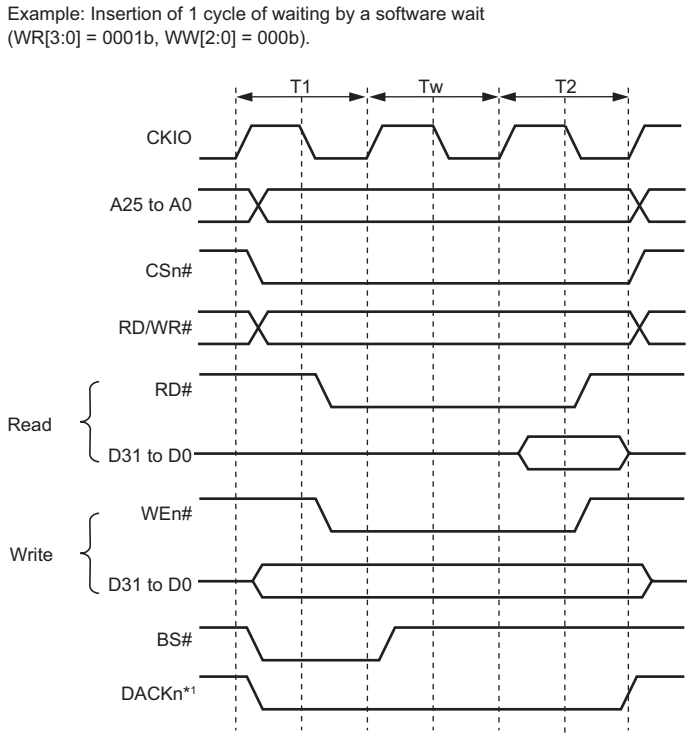


Figure 14.7 Example of 8-Bit Data-Width SRAM Connection

14.4.3 Access Wait Control

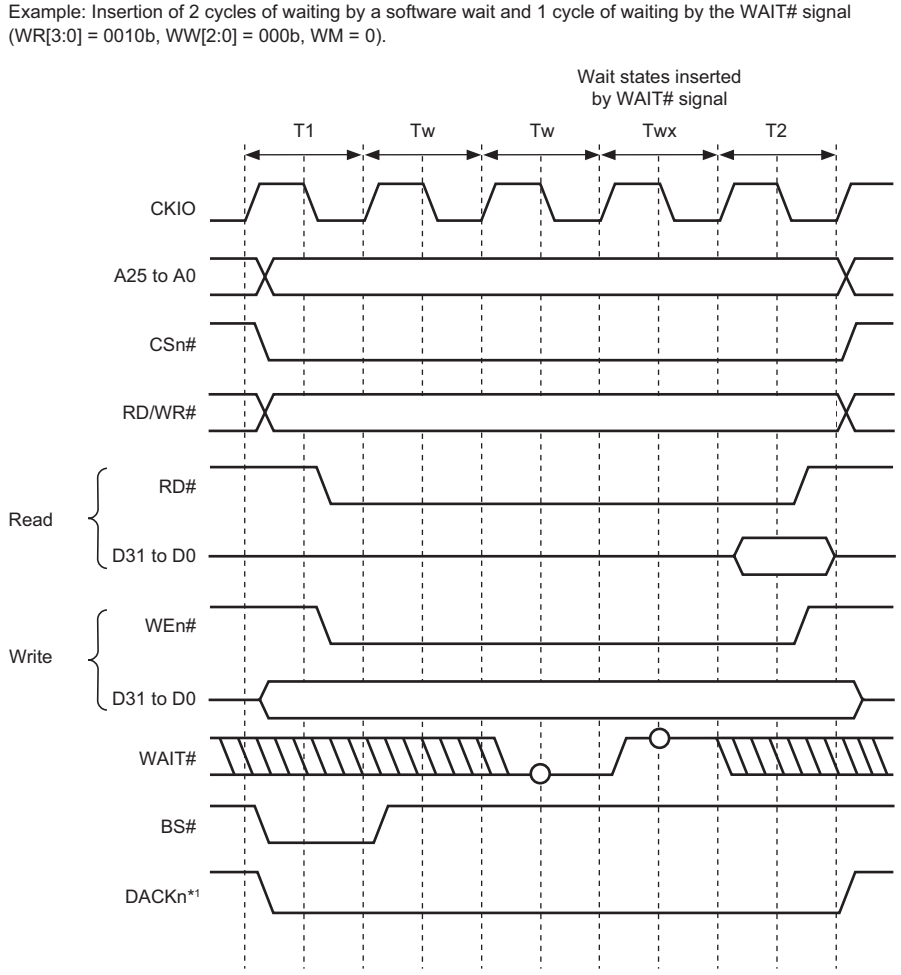
Wait insertion on a SRAM interface access can be controlled by the settings of bits WR3 to WR0 in CSnWCR. It is possible for areas 1, 4, and 5 to insert waits independently in read access and in write access. Areas 0, 2, and 3 have common access wait for read cycle and write cycle. The specified number of Tw states are inserted as waits in a SRAM interface access shown in Figure 14.8.



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.8 Wait Timing for SRAM Interface Access (Software Wait Only)

When the WM bit in the CSnWCR register is cleared to 0, the signal on the external WAIT# pin is also sampled. WAIT# pin sampling is shown in Figure 14.9. Two waits are specified as software waits. The WAIT# signal is sampled on the falling edge of the CKIO signal at the transition from the T1 or Tw cycle to the T2 cycle.

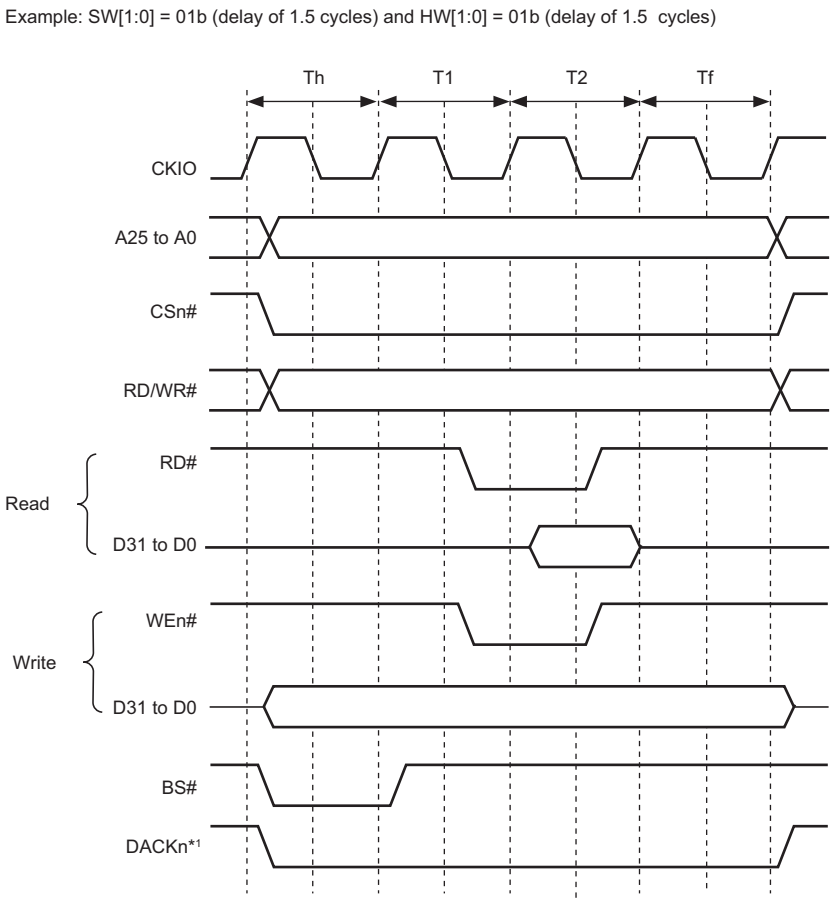


Note 1. The waveform for DACKn is when active low is specified.

Figure 14.9 Wait Cycle Timing for SRAM Interface Access (Wait Cycle Insertion Using WAIT# Signal)

14.4.4 CSn# Assert Period Expansion

The number of states from CSn# active to RD#, WEn# active can be specified by setting bits SW1 and SW0 in CSnWCR. The number of states from the inactive state of the RD# and WEn# signals to the inactive state of the CSn# signal can be specified by setting bits HW1 and HW0. Therefore, a flexible interface to an external device can be obtained. Figure 14.10 shows an example. A Th state and a Tf state are added before and after an ordinary cycle, respectively. In these states, the RD# and WEn# signals are not activated, while other signals are activated. The data output is prolonged to the Tf cycle, and this prolongation is useful for devices with slow writing operations.



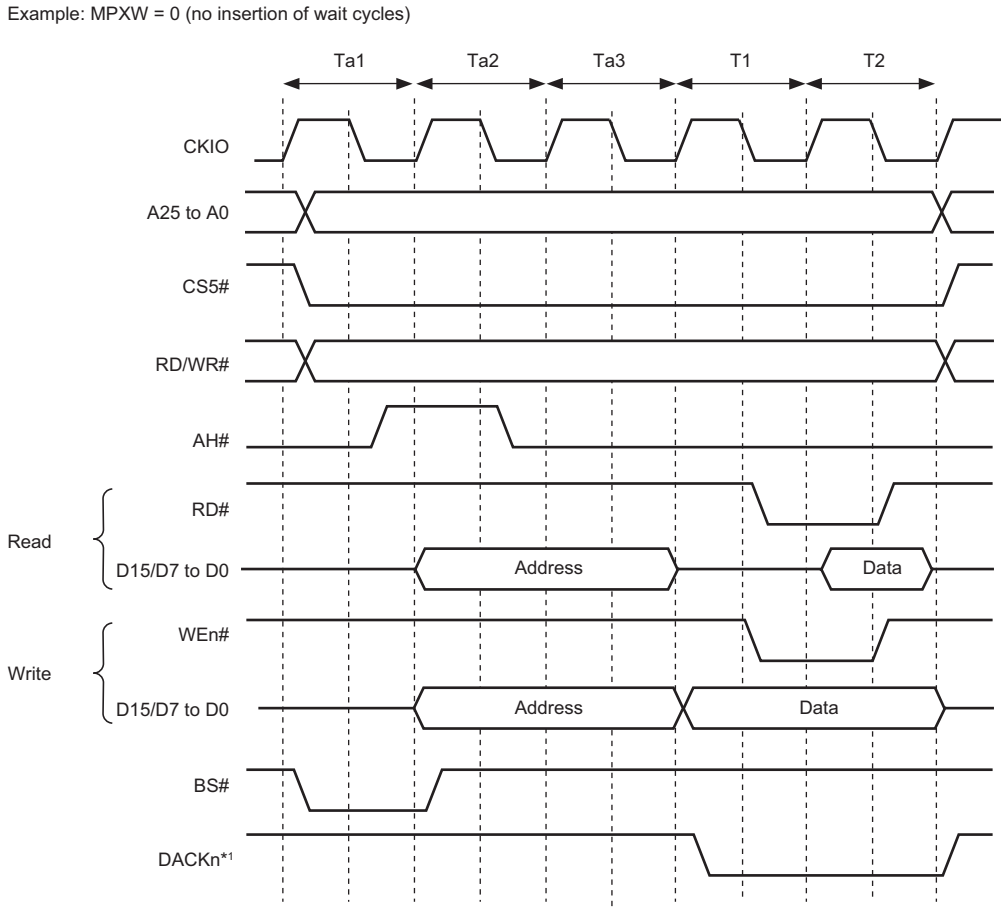
Note 1. The waveform for DACKn is when active low is specified.

Figure 14.10 Active Period Expansion for the CSn Signal

Note: For the CS2 and CS3 spaces, the active period cannot be extended.

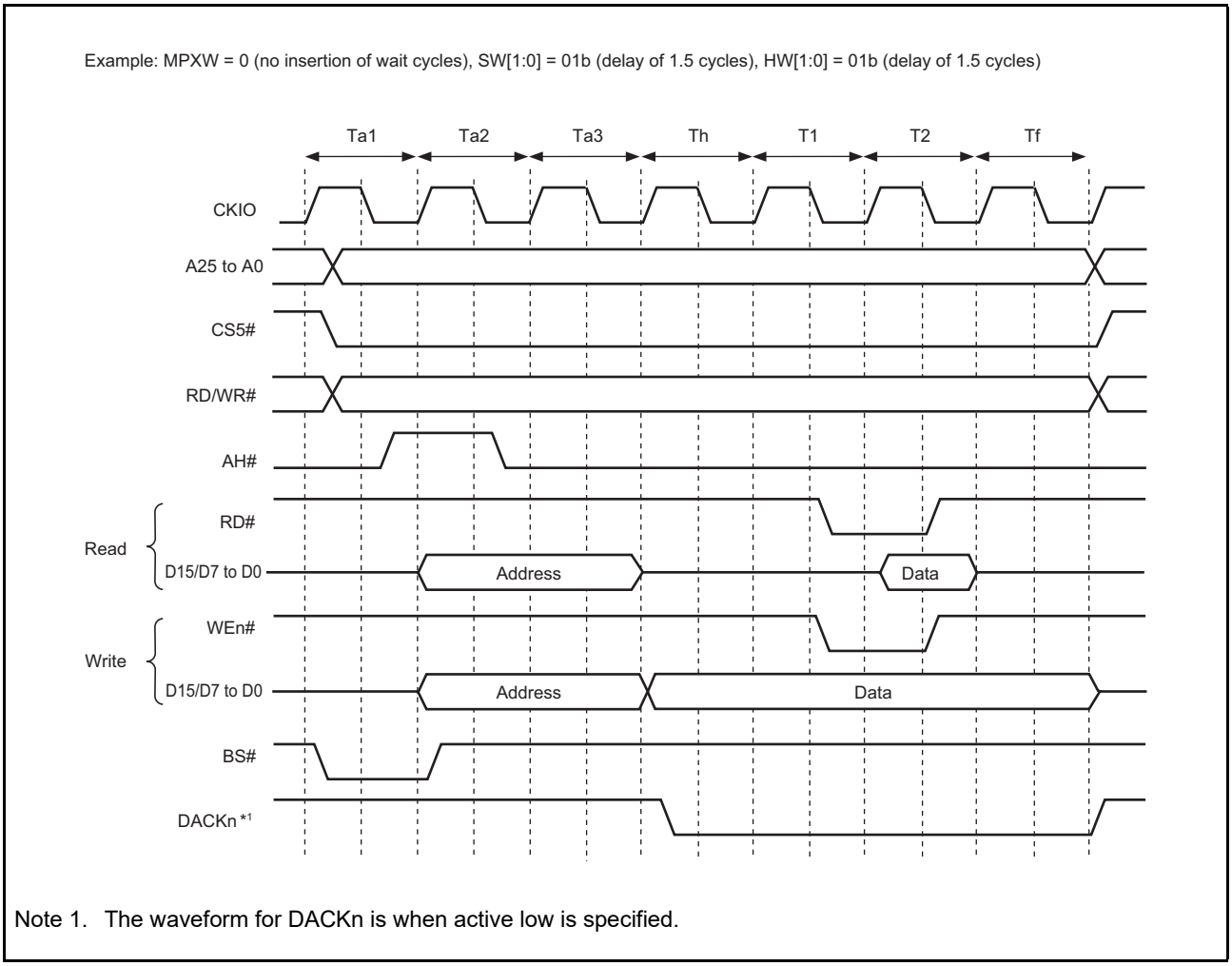
14.4.5 MPX-I/O Interface

Access timing for the MPX space is shown below. In the MPX space, CS5#, AH#, RD#, and WEn# signals control the accessing. The basic access for the MPX space consists of 2 cycles of address output followed by an access to an SRAM interface. The bus width for the address output cycle or the data input/output cycle is fixed to 8 bits or 16 bits. Alternatively, it can be 8 bits or 16 bits depending on the address to be accessed.
Output of the addresses D15 to D0 or D7 to D0 is performed from state Ta2 to state Ta3. Because state Ta1 has a high-impedance state, collisions of addresses and data can be avoided without inserting idle cycles, even in continuous access cycles. Address output is increased to 3 cycles by setting the MPXW bit in the CS5WCR register to 1.
The RD/WR# signal is output at the same time as the CS5# signal; it is high in the read cycle and low in the write cycle. The data cycle is the same as that in an SRAM interface access.
Delay cycles specified in the SW[1:0] bits of the CSnWCR register are inserted between the Ta3 state and the T1 state. Delay cycles specified in the HW[1:0] bits are added after the T2 state.
Timing charts are shown in Figure 14.11 to Figure 14.14.



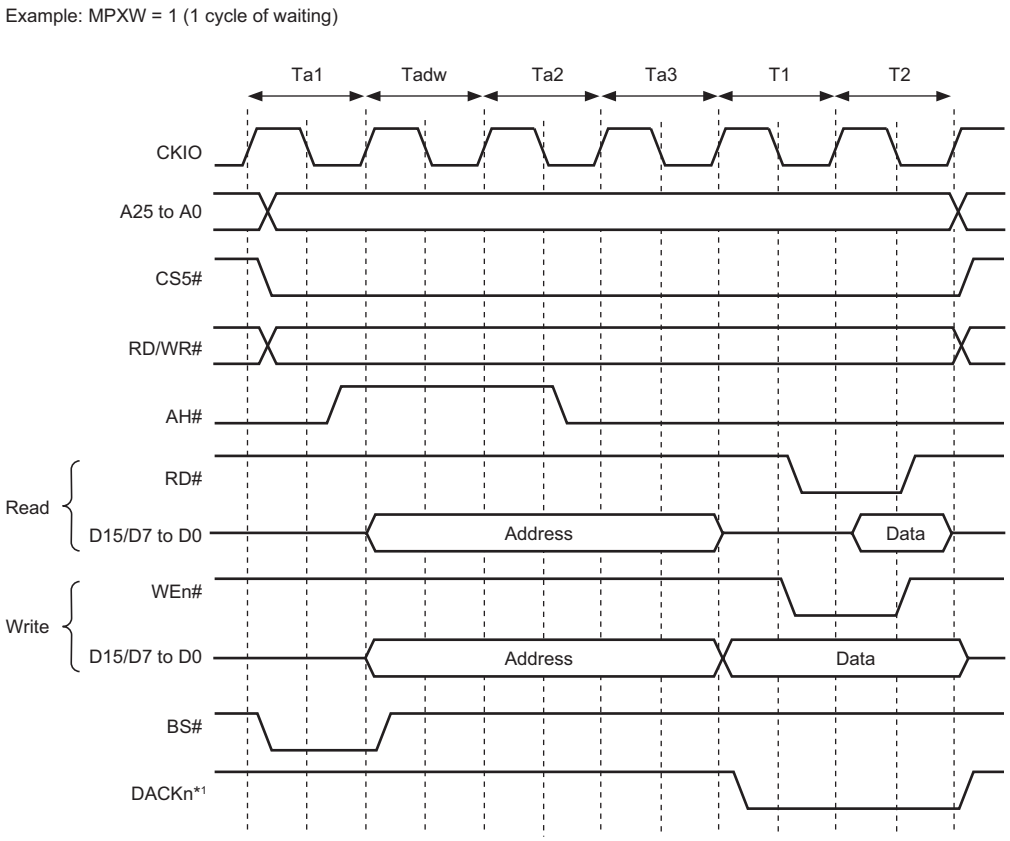
Note 1. The waveform for DACKn is when active low is specified.

Figure 14.11 Access Timing for MPX Space (1) (Address Cycle No Wait, Data Cycle No Wait)



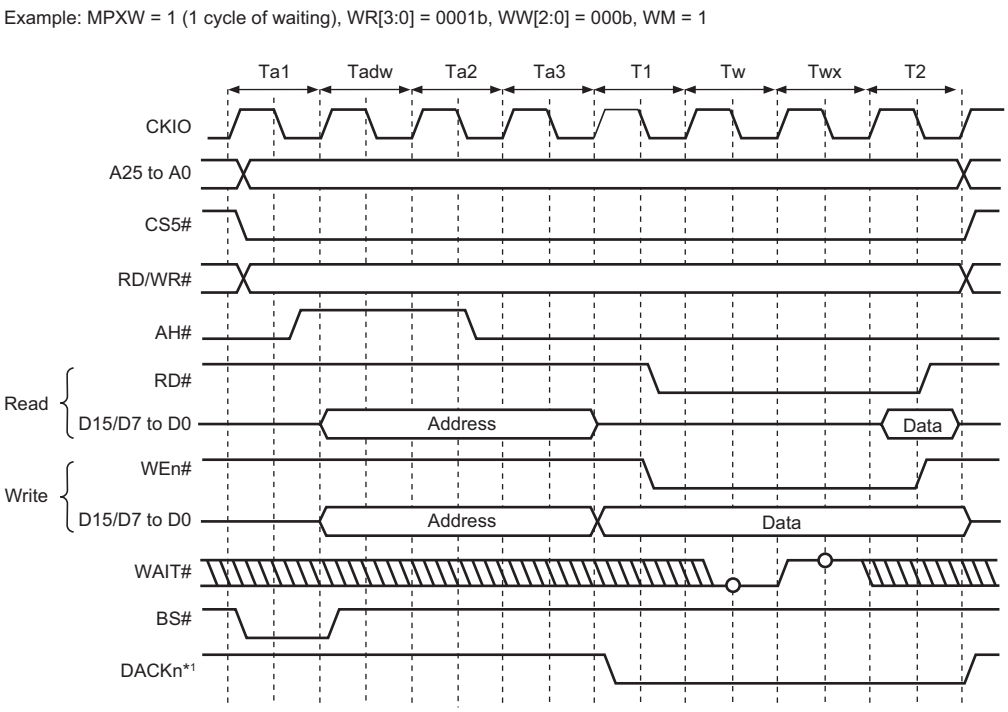
Note 1. The waveform for DACKn is when active low is specified.

Figure 14.12 Access Timing for MPX Space (2) (Address Cycle No Wait, 1.5 Assertion Delay States, Data Cycle No Wait, 1.5 Delay States)



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.13 Access Timing for MPX Space (3) (Address Cycle Wait 1, Data Cycle No Wait)



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.14 Access Timing for MPX Space (4) (Address Cycle Access Wait 1, Data Cycle Wait 1, External Wait 1)

14.4.6 SDRAM Interface

(1) SDRAM Direct Connection

The SDRAM that can be connected to this LSI is a product that has 11/12/13 bits of row address, 8/9/10 bits of column address, 4 or less banks, and uses the A10 pin for setting precharge mode in read and write command cycles.
The control signals for direct connection of SDRAM are RAS#, CAS#, RD/WR#, DQMUU, DQMUL, DQMLU, DQMLL, CKE, CS2#, and CS3#. All the signals other than CS2# and CS3# are common to all areas, and signals other than CKE are valid only when CS2# or CS3# is asserted. SDRAM can be connected to up to 2 spaces. The data bus width of the area that is connected to SDRAM is 16 bits or 32 bits.
Commands for SDRAM can be specified by RAS#, CAS#, RD/WR#, and specific address signals. These commands supports:

- NOP
- Auto-refresh (REF)
- Self-refresh (SELF)
- All banks pre-charge (PALL)
- Specified bank pre-charge (PRE)
- Bank active (ACTV)
- Read (READ)
- Read with pre-charge (READA)
- Write (WRIT)
- Write with pre-charge (WRITA)
- Write mode register (MRS, EMRS)

The byte to be accessed is specified by DQMUU, DQMUL, DQMLU, and DQMLL. Reading or writing is performed for a byte whose corresponding DQMxx is low. For details on the relationship between DQMxx and the byte to be accessed, see section 14.4.1, Access Size and Data Alignment (x = UU, UL, LU, LL).

Figure 14.15 and Figure 14.16 show examples of the connection of the SDRAM with this LSI.

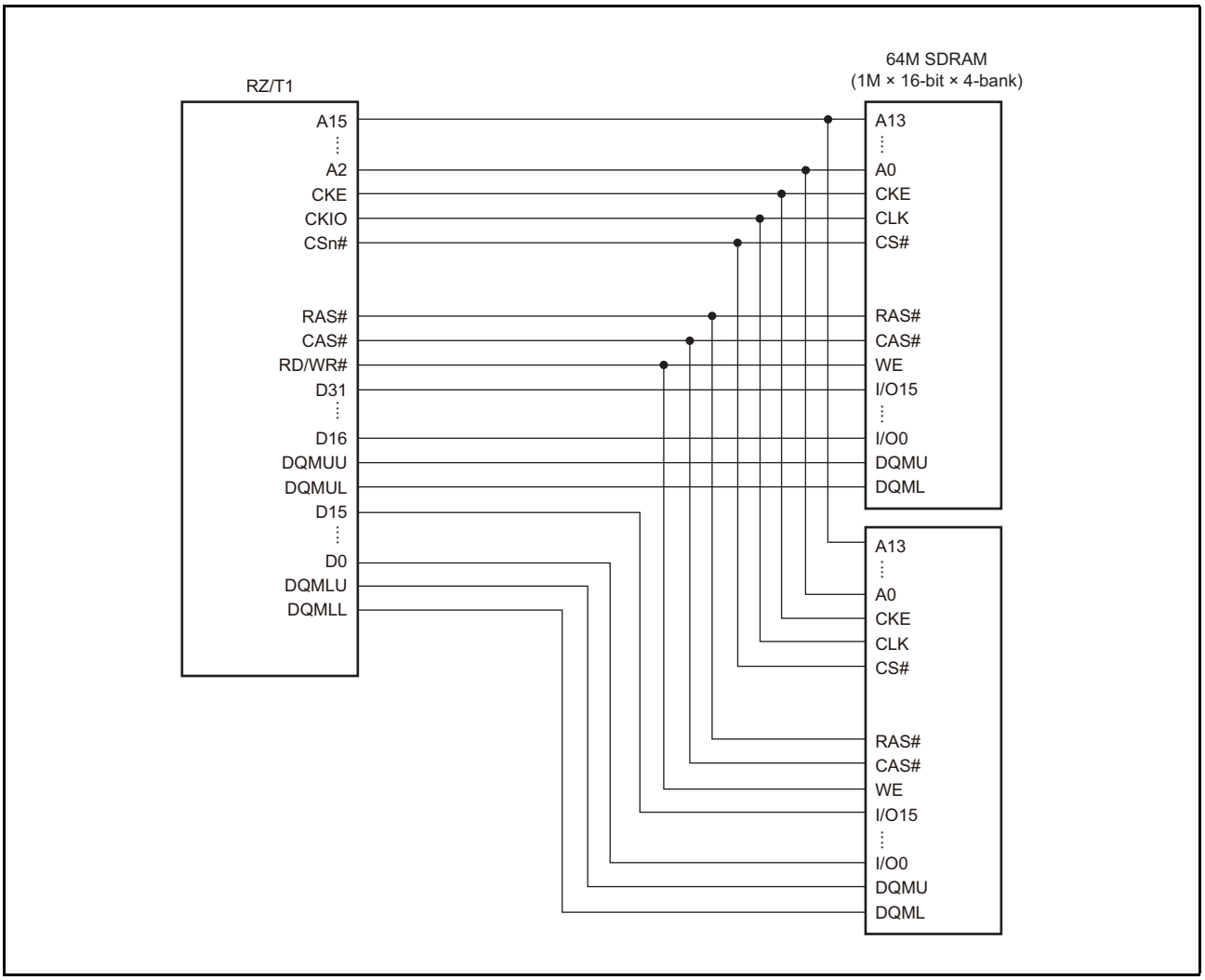


Figure 14.15 Example of 32-Bit Data Width SDRAM Connection

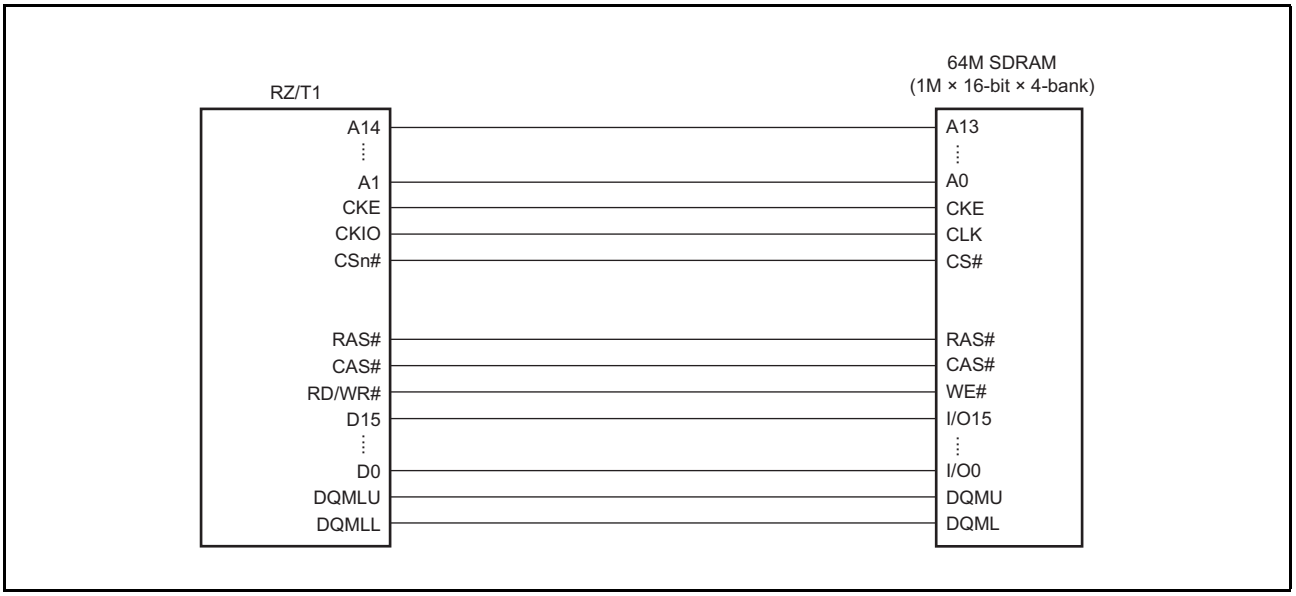


Figure 14.16 Example of 16-Bit Data Width SDRAM Connection

(2) Address Multiplexing

An address multiplexing is specified so that SDRAM can be connected without external multiplexing circuitry according to the setting of bits BSZ[1:0] in CSnBCR and bits A2ROW[1:0], A2COL[1:0], A3ROW[1:0], and A3COL[1:0] in SDCR. Table 14.8 to Table 14.13 show the relationship between the settings of bits BSZ[1:0], A2ROW[1:0], A2COL[1:0], A3ROW[1:0], and A3COL[1:0] and the bits output at the address pins. Do not specify those bits in the manner other than this table, otherwise the operation of this LSI is not guaranteed. A25 to A18 are not multiplexed and the original values of address are always output at these pins.

When the data bus width is 16 bits (BSZ1 and BSZ0 = 10b), A0 of SDRAM specifies a 16-bit address. Therefore, connect this A0 pin of SDRAM to the A1 pin of this LSI; the A1 pin of SDRAM to the A2 pin of the LSI, and so on.

When the data bus width is 32 bits (BSZ1 and BSZ0 = 11b), A0 of SDRAM specifies a 32-bit address. Therefore, connect this A0 pin of SDRAM to the A2 pin of this LSI; the A1 pin of SDRAM to the A3 pin of the LSI, and so on.

Table 14.8 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (1) (1/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**00 (11 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23	A15		
A14	A22*2	A22*2	A12 (BA1)	Specifies bank
A13	A21*2	A21*2	A11 (BA0)	
A12	A20	L/H*1	A10/AP	Specifies address/ precharge
A11	A19	A11	A9	Address
A10	A18	A10	A8	
A9	A17	A9	A7	
A8	A16	A8	A6	
A7	A15	A7	A5	
A6	A14	A6	A4	
A5	A13	A5	A3	
A4	A12	A4	A2	
A3	A11	A3	A1	
A2	A10	A2	A0	
A1	A9	A1		Unused
A0	A8	A0		
Example of connected memory				
64-Mbit product (512 Kwords × 32 bits × 4 banks, column 8 bits product): 1 16-Mbit product (512 Kwords × 16 bits × 2 banks, column 8 bits product): 2				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.8 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (1) (2/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23*2	A23*2	A13 (BA1)	Specifies bank
A14	A22*2	A22*2	A12 (BA0)	
A13	A21	A13	A11	Address
A12	A20	L/H*1	A10/AP	Specifies address/ precharge
A11	A19	A11	A9	Address
A10	A18	A10	A8	
A9	A17	A9	A7	
A8	A16	A8	A6	
A7	A15	A7	A5	
A6	A14	A6	A4	
A5	A13	A5	A3	
A4	A12	A4	A2	
A3	A11	A3	A1	
A2	A10	A2	A0	
A1	A9	A1		Unused
A0	A8	A0		
Example of connected memory				
128-Mbit product (1 Mwords × 32 bits × 4 banks, column 8 bits product): 1 64-Mbit product (1 Mwords × 16 bits × 4 banks, column 8 bits product): 2				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.9 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (2) (1/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16		
A15	A24*2	A24*2	A13 (BA1)	Specifies bank
A14	A23*2	A23*2	A12 (BA0)	
A13	A22	A13	A11	Address
A12	A21	L/H*1	A10/AP	Specifies address/ precharge
A11	A20	A11	A9	Address
A10	A19	A10	A8	
A9	A18	A9	A7	
A8	A17	A8	A6	
A7	A16	A7	A5	
A6	A15	A6	A4	
A5	A14	A5	A3	
A4	A13	A4	A2	
A3	A12	A3	A1	
A2	A11	A2	A0	
A1	A10	A1		Unused
A0	A9	A0		
Example of connected memory				
256-Mbit product (2 Mwords × 32 bits × 4 banks, column 9 bits product): 1 128-Mbit product (2 Mwords × 16 bits × 4 banks, column 9 bits product): 2				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.9 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (2) (2/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**01 (12 Bits)**	**10 (10 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25*2	A25*2	A13 (BA1)	Specifies bank
A14	A24*2	A24*2	A12 (BA0)	
A13	A23	A13	A11	Address
A12	A22	L/H*1	A10/AP	Specifies address/ precharge
A11	A21	A11	A9	Address
A10	A20	A10	A8	
A9	A19	A9	A7	
A8	A18	A8	A6	
A7	A17	A7	A5	
A6	A16	A6	A4	
A5	A15	A5	A3	
A4	A14	A4	A2	
A3	A13	A3	A1	
A2	A12	A2	A0	
A1	A11	A1		Unused
A0	A10	A0		
Example of connected memory				
512-Mbit product (4 Mwords × 32 bits × 4 banks, column 10 bits product): 1 256-Mbit product (4 Mwords × 16 bits × 4 banks, column 10 bits product): 2				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.10 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (3)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
11 (32 Bits)	**10 (13 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25*2	A25*2	A14 (BA1)	Specifies bank
A15	A24*2	A24*2	A13 (BA0)	
A14	A23	A14	A12	Address
A13	A22	A13	A11	
A12	A21	L/H*1	A10/AP	Specifies address/ precharge
A11	A20	A11	A9	Address
A10	A19	A10	A8	
A9	A18	A9	A7	
A8	A17	A8	A6	
A7	A16	A7	A5	
A6	A15	A6	A4	
A5	A14	A5	A3	
A4	A13	A4	A2	
A3	A12	A3	A1	
A2	A11	A2	A0	
A1	A10	A1		Unused
A0	A9	A0		
Example of connected memory				
512-Mbit product (4 Mwords × 32 bits × 4 banks, column 9 bits product): 1 256-Mbit product (4 Mwords × 16 bits × 4 banks, column 9 bits product): 2				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.11 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (4) (1/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**00 (11 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23	A15		
A14	A22	A14		
A13	A21	A21		
A12	A20*2	A20*2	A11 (BA0)	Specifies bank
A11	A19	L/H*1	A10/AP	Specifies address/ precharge
A10	A18	A10	A9	Address
A9	A17	A9	A8	
A8	A16	A8	A7	
A7	A15	A7	A6	
A6	A14	A6	A5	
A5	A13	A5	A4	
A4	A12	A4	A3	
A3	A11	A3	A2	
A2	A10	A2	A1	
A1	A9	A1	A0	
A0	A8	A0		Unused
Example of connected memory				
16-Mbit product (512 Kwords × 16 bits × 2 banks, column 8 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.11 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (4) (2/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**01 (12 Bits)**	**00 (8 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A25	A17		Unused
A16	A24	A16		
A15	A23	A15		
A14	A22*2	A22*2	A13 (BA1)	Specifies bank
A13	A21*2	A21*2	A12 (BA0)	
A12	A20	A12	A11	Address
A11	A19	L/H*1	A10/AP	Specifies address/ precharge
A10	A18	A10	A9	Address
A9	A17	A9	A8	
A8	A16	A8	A7	
A7	A15	A7	A6	
A6	A14	A6	A5	
A5	A13	A5	A4	
A4	A12	A4	A3	
A3	A11	A3	A2	
A2	A10	A2	A1	
A1	A9	A1	A0	
A0	A8	A0		Unused
Example of connected memory				
64-Mbit product (1 Mwords × 16 bits × 4 banks, column 8 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.12 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (5) (1/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**01 (12 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16		
A15	A24	A15		
A14	A23*2	A23*2	A13 (BA1)	Specifies bank
A13	A22*2	A22*2	A12 (BA0)	
A12	A21	A12	A11	Address
A11	A20	L/H*1	A10/AP	Specifies address/ precharge
A10	A19	A10	A9	Address
A9	A18	A9	A8	
A8	A17	A8	A7	
A7	A16	A7	A6	
A6	A15	A6	A5	
A5	A14	A5	A4	
A4	A13	A4	A3	
A3	A12	A3	A2	
A2	A11	A2	A1	
A1	A10	A1	A0	
A0	A9	A0		Unused
Example of connected memory				
128-Mbit product (2 Mwords × 16 bits × 4 banks, column 9 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.12 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (5) (2/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**01 (12 Bits)**	**10 (10 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25	A15		
A14	A24*2	A24*2	A13 (BA1)	Specifies bank
A13	A23*2	A23*2	A12 (BA0)	
A12	A22	A12	A11	Address
A11	A21	L/H*1	A10/AP	Specifies address/ precharge
A10	A20	A10	A9	Address
A9	A19	A9	A8	
A8	A18	A8	A7	
A7	A17	A7	A6	
A6	A16	A6	A5	
A5	A15	A5	A4	
A4	A14	A4	A3	
A3	A13	A3	A2	
A2	A12	A2	A1	
A1	A11	A1	A0	
A0	A10	A0		Unused
Example of connected memory				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 10 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.13 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (6) (1/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**10 (13 Bits)**	**01 (9 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A26	A17		Unused
A16	A25	A16		
A15	A24*2	A24*2	A14 (BA1)	Specifies bank
A14	A23*2	A23*2	A13 (BA0)	
A13	A22	A13	A12	Address
A12	A21	A12	A11	
A11	A20	L/H*1	A10/AP	Specifies address/ precharge
A10	A19	A10	A9	Address
A9	A18	A9	A8	
A8	A17	A8	A7	
A7	A16	A7	A6	
A6	A15	A6	A5	
A5	A14	A5	A4	
A4	A13	A4	A3	
A3	A12	A3	A2	
A2	A11	A2	A1	
A1	A10	A1	A0	
A0	A9	A0		Unused
Example of connected memory				
256-Mbit product (4 Mwords × 16 bits × 4 banks, column 9 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

Table 14.13 Relationship between BSZ[1:0], A2/3ROW[1:0], A2/3COL[1:0], and Address Multiplex Output (6) (2/2)

Setting				
BSZ[1:0]	**A2/3ROW[1:0]**	**A2/3COL[1:0]**		
10 (16 Bits)	**10 (13 Bits)**	**10 (10 Bits)**		
Output Pin of This LSI	**Row Address Output Cycle**	**Column Address Output Cycle**	**SDRAM Pin**	**Function**
A17	A27	A17		Unused
A16	A26	A16		
A15	A25*2	A25*2	A14 (BA1)	Specifies bank
A14	A24*2	A24*2	A13 (BA0)	
A13	A23	A13	A12	Address
A12	A22	A12	A11	
A11	A21	L/H*1	A10/AP	Specifies address/ precharge
A10	A20	A10	A9	Address
A9	A19	A9	A8	
A8	A18	A8	A7	
A7	A17	A7	A6	
A6	A16	A6	A5	
A5	A15	A5	A4	
A4	A14	A4	A3	
A3	A13	A3	A2	
A2	A12	A2	A1	
A1	A11	A1	A0	
A0	A10	A0		Unused
Example of connected memory				
512-Mbit product (8 Mwords × 16 bits × 4 banks, column 10 bits product): 1				

Note 1. L/H is a bit used in the command specification; it is fixed at L or H according to the access mode.
Note 2. Bank address specification

(3) Burst Read

A burst read occurs in the following cases with this LSI.

- Access size in reading is larger than data bus width.
- 16-, 32-, or 64-byte transfer

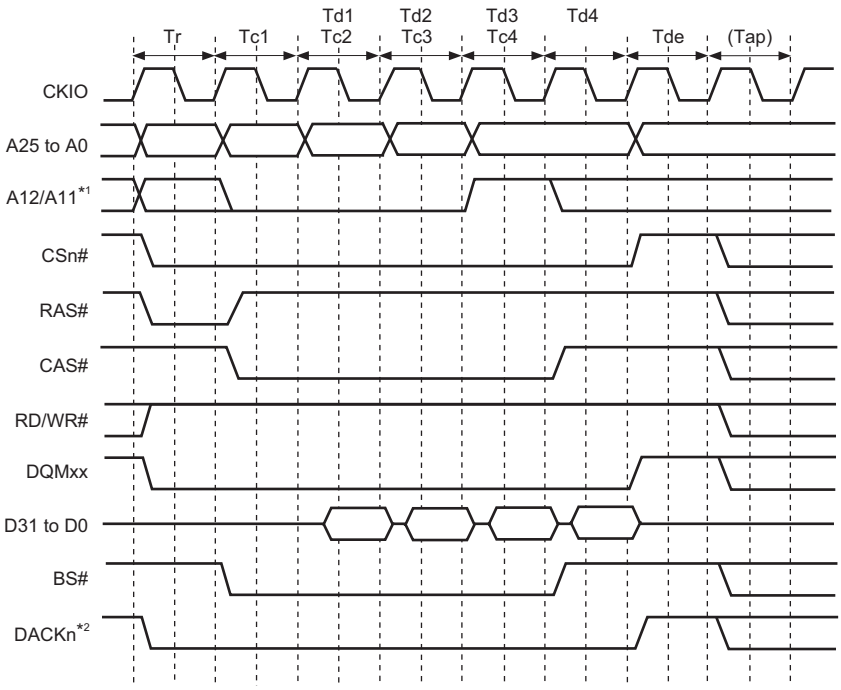
This LSI always accesses the SDRAM with burst length 1. For example, read access of burst length 1 is performed consecutively 8 times to read 16-byte continuous data from the SDRAM that is connected to a 16-bit data bus. This access is called the burst read with the burst number 8. Table 14.14 shows the relationship between the access size and the number of bursts.

Table 14.14 Relationship between Access Size and Number of Bursts

Bus Width	Access Size	Number of Bursts
16 bits	8 bits	1
	16 bits	1
	32 bits	2
	16 bytes	8
	32 bytes	16
	64 bytes	32
32 bits	8 bits	1
	16 bits	1
	32 bits	1
	16 bytes	4
	32 bytes	8
	64 bytes	16

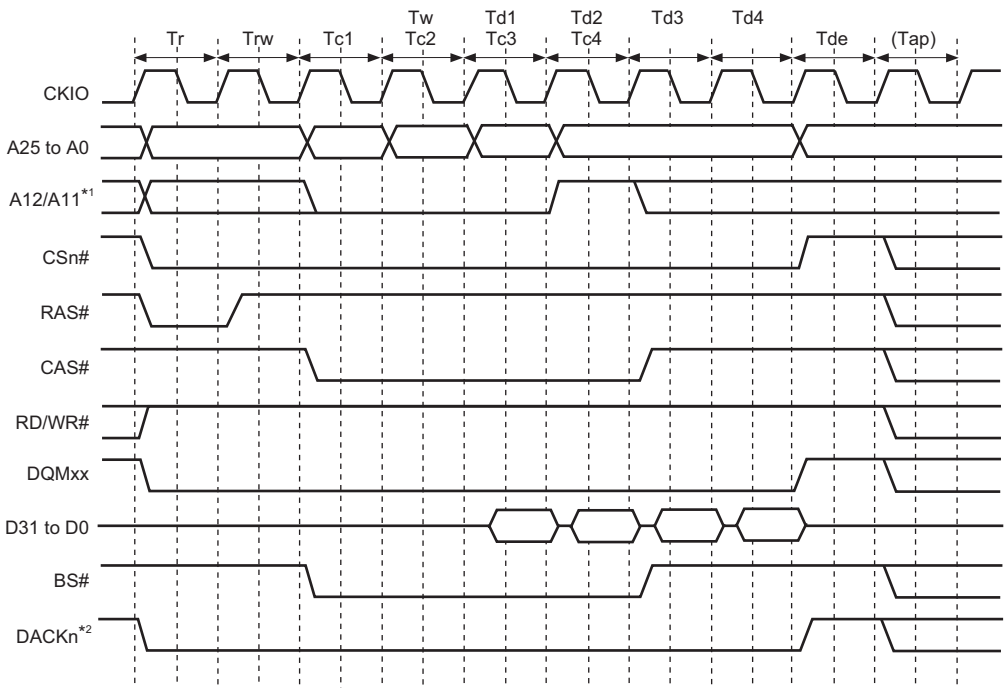
Figure 14.17 and Figure 14.18 show timing charts in burst read. In burst read, an ACTV command is output in the Tr cycle, the READ command is issued in the Tc1, Tc2, and Tc3 cycles, the READA command is issued in the Tc4 cycle, and the read data is received at the rising edge of the external clock (CKIO) in the Td1 to Td4 cycles. The Tap cycle is used to wait for the completion of an auto-precharge induced by the READA command in the SDRAM. In the Tap cycle, a new command will not be issued to the same bank. However, access to another CS space or another bank in the same SDRAM space is enabled. The number of Tap cycles is specified by the WTRP1 and WTRP0 bits in CS3WCR.

In this LSI, wait cycles can be inserted by specifying each bit in CS3WCR to connect the SDRAM in variable frequencies. Figure 14.18 shows an example in which wait cycles are inserted. The number of states from the Tr state where the ACTV command is output to the Tc1 state where the READ command is output can be specified using the WTRCD1 and WTRCD0 bits in the CS3WCR register. If the WTRCD1 and WTRCD0 bits specify one wait or more, a Trw state where the NOP command is issued is inserted between the Tr state and Tc1 state. The number of states from the Tc1 state where the READ command is output to the Td1 state where the read data is latched can be specified for the CS2 and CS3 spaces independently, using the A2CL1 and A2CL0 bits in the CS2WCR register or the A3CL1 and A3CL0 bits in the CS3WCR register. The number of states from Tc1 to Td1 corresponds to the SDRAM CAS latency. The CAS latency for the SDRAM is normally defined as up to three. However, the CAS latency in this LSI can be specified as 1 to 4. This CAS latency can be achieved by connecting a latch circuit between this LSI and the SDRAM.
A Tde state is an idle state required to transfer the read data into this LSI and occurs once for every burst read or every single read.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.17 Burst Read Basic Timing (CAS Latency 1, Auto Pre-Charge)



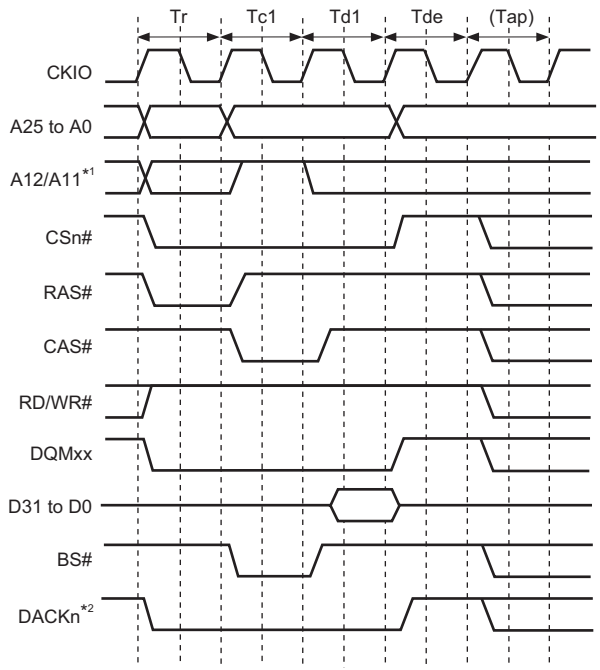
Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.18 Burst Read Wait Specification Timing (CAS Latency 2, WTRCD[1:0] = 1 Cycle, Auto Pre-Charge)

(4) Single Read

A read access ends in one cycle when the data bus width is larger than or equal to the access size. A read access that ends in one cycle is called single read.

Figure 14.19 shows the single read basic timing.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

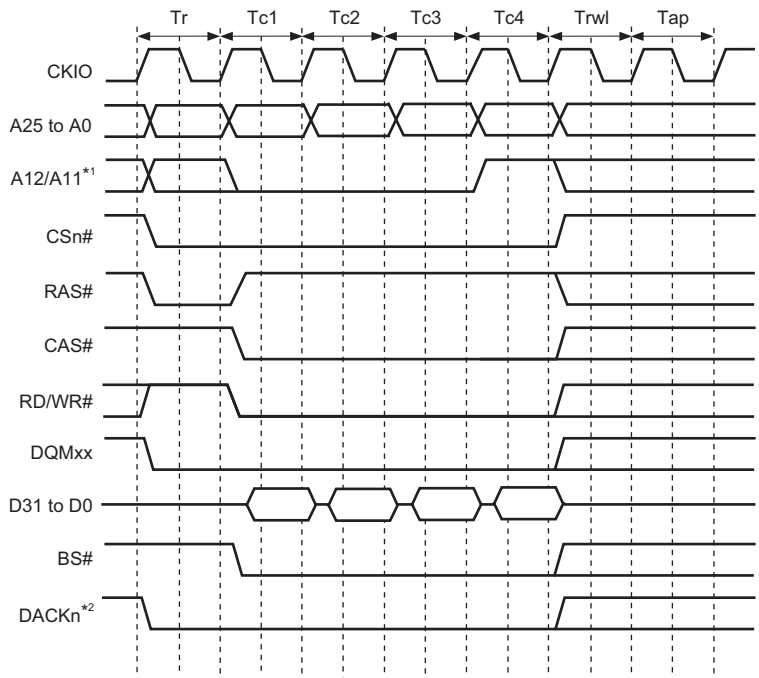
Figure 14.19 Basic Timing for Single Read (CAS Latency 1, Auto Pre-Charge)

(5) Burst Write

A burst write occurs in the following cases in this LSI.

- Access size in writing is larger than data bus width.
- 16-, 32-, or 64-byte transfer

This LSI always accesses SDRAM with burst length 1. For example, write access of burst length 1 is performed continuously 8 times to write 16-byte continuous data to the SDRAM that is connected to a 16-bit data bus. This access is called burst write with the burst number 8. The relationship between the access size and the number of bursts is shown in Table 14.14. Figure 14.20 shows a timing chart for burst writes. In burst write, an ACTV command is output in the Tr state, the WRIT command is issued in the Tc1, Tc2, and Tc3 states, and the WRITA command is issued to execute an auto-precharge in the Tc4 state. In the write cycle, the write data is output simultaneously with the write command. After the write command with the auto-precharge is output, the Trw1 state that waits for the auto-precharge initiation is followed by the Tap state that waits for completion of the auto-precharge induced by the WRITA command in the SDRAM. Between the Trwl and the Tap states, a new command will not be issued to the same bank. However, access to another CS space or another bank in the same SDRAM space is enabled. The number of Trw1 states is specified by the TRWL1 and TRWL0 bits in the CS3WCR register. The number of Tap states is specified by the WTRP1 and WTRP0 bits in the CS3WCR register.

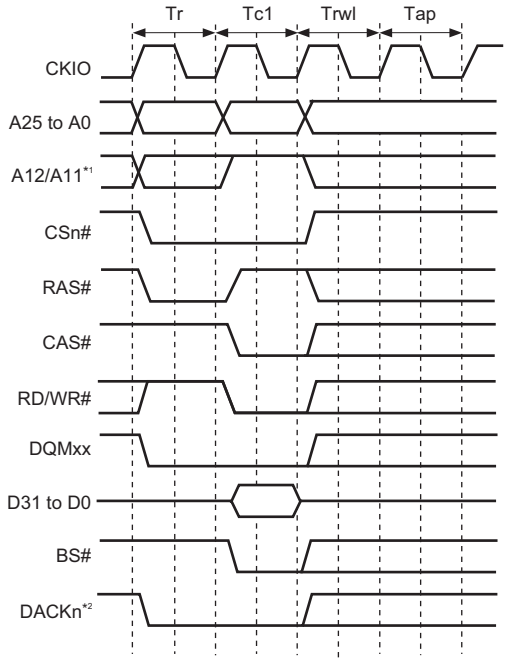


Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.20 Basic Timing for Burst Write (Auto Pre-Charge)

(6) Single Write

A write access ends in one cycle when the data bus width is larger than or equal to the access size. A write access that ends in one cycle is called single write. Figure 14.21 shows the basic timing of single-write operation.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.21 Single Write Basic Timing (Auto-Precharge)

(7) Bank Active

The SDRAM bank function can be used to support high-speed access to the same row address. When the BACTV bit in SDCR is 1, access is performed using commands without auto-precharge (READ or WRIT). This function is called bank-active function. This function is valid only for area 3. When area 3 is set to bank-active mode, area 2 should be set to normal space or SRAM with byte selection. When areas 2 and 3 are both set to SDRAM, auto precharge mode must be set.

When the bank-active function is used, precharging is not performed when the access ends. When accessing the same row address in the same bank, it is possible to issue the READ or WRIT command immediately, without issuing an ACTV command. As SDRAM is internally divided into several banks, it is possible to activate one row address in each bank. If the next access is to a different row address, a PRE command is first issued to precharge the relevant bank, then when precharging is completed, the access is performed by issuing an ACTV command followed by a READ or WRIT command. If this is followed by an access to a different row address, the access time will be longer because of the precharging performed after the access request is received. The number of states between issuance of the PRE command and the ACTV command is determined by the WTRP1 and WTPR0 bits in CS3WCR.

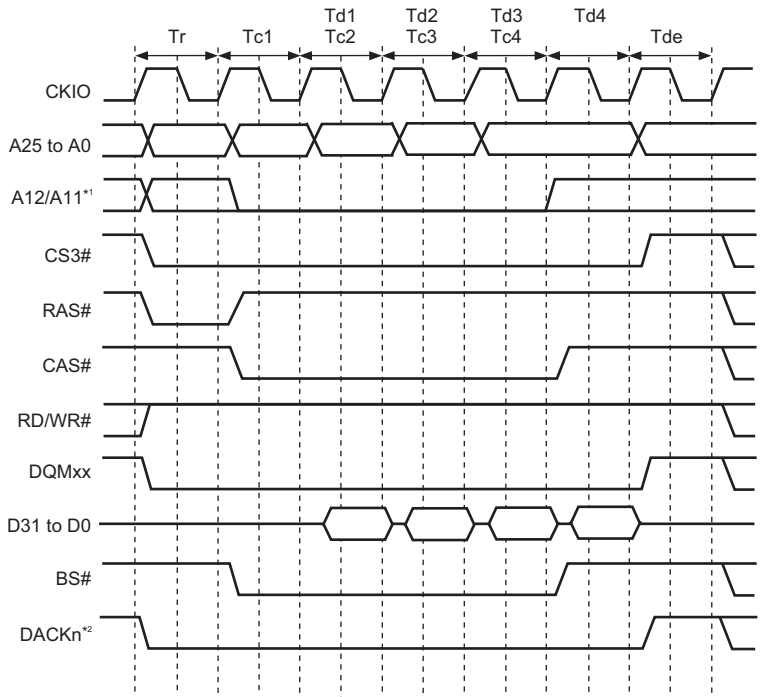
In a write, when an auto-precharge is performed, a command cannot be issued to the same bank for a period of Trwl + Tap states after issuance of the WRITA command. When bank active mode is used, READ or WRIT commands can be issued successively if the row address is the same. The number of cycles can thus be reduced by Trwl + Tap states for each write.

There is a limit on tRAS, the time for placing each bank in the active state. If there is no guarantee that there will not be a cache hit and another row address will be accessed within the period in which this value is maintained by program execution, it is necessary to set auto-refresh and set the refresh cycle to no more than the maximum value of tRAS.

A burst read cycle without auto-precharge is shown in Figure 14.22, a burst read cycle for the same row address in Figure 14.23, and a burst read cycle for different row addresses in Figure 14.24. Similarly, a single write cycle without auto-precharge is shown in Figure 14.25, a single write cycle for the same row address in Figure 14.26, and a single write cycle for different row addresses in Figure 14.27.

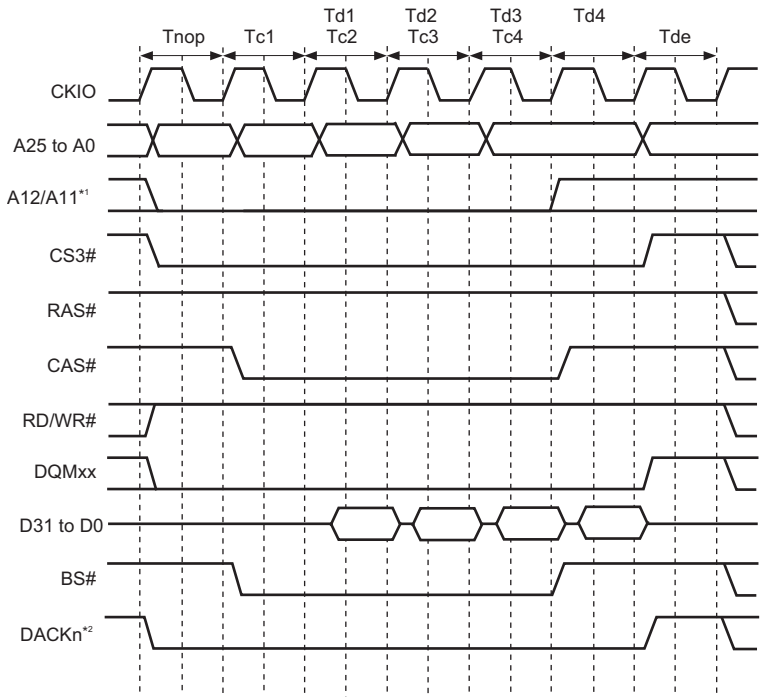
In Figure 14.23, a Tnop state in which no operation is performed is inserted before the Tc state that issues the READ command. The Tnop state is inserted to maintain latency 2 for the DQMxx signal that specifies the read byte in the data read from the SDRAM. If the CAS latency is specified as two or more, the Tnop state is not inserted because latency 2 can be maintained even if the DQMxx signal is activated after the Tc state.

When bank active mode is set, if only access cycles to the respective banks in the area 3 space are considered, as long as access cycles to the same row address continue, the operation starts with the cycle in Figure 14.22 or Figure 14.25, followed by repetition of the cycle in Figure 14.23 or Figure 14.26. An access to a different area during this time has no effect. If there is an access to a different row address in the bank active state, the bus cycle in Figure 14.24 or Figure 14.27 is executed instead of that in Figure 14.23 or Figure 14.26. In bank active mode, too, all banks become inactive after a refresh cycle.



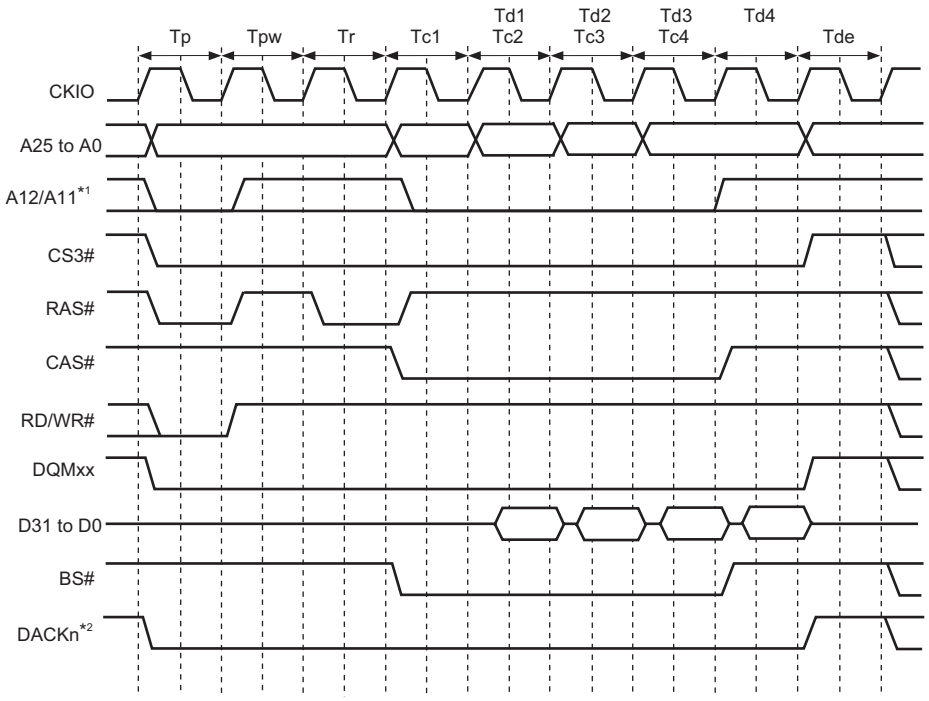
Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.22 Burst Read Timing (Bank Active, Different Bank, CAS Latency 1)



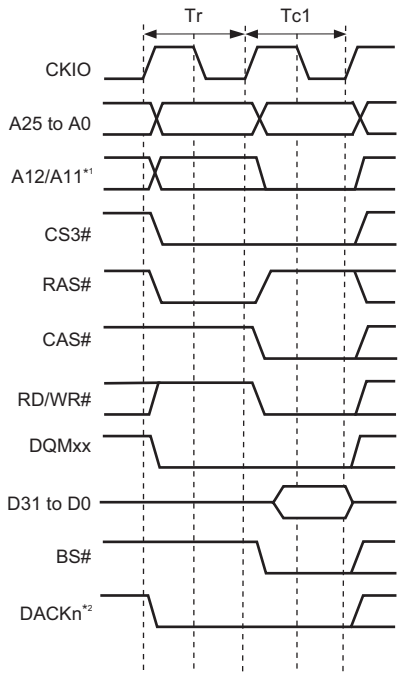
Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.23 Burst Read Timing (Bank Active, Same Row Addresses in the Same Bank, CAS Latency 1)



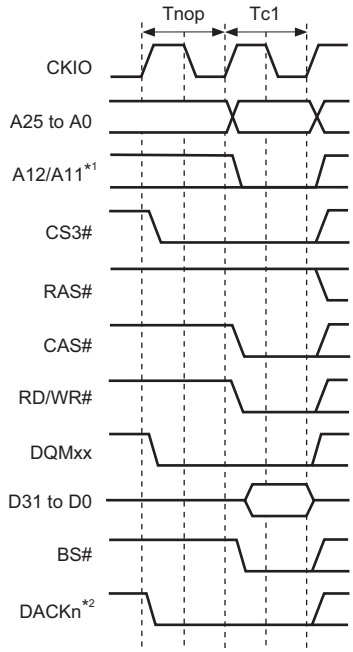
Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.24 Burst Read Timing (Bank Active, Different Row Addresses in the Same Bank, CAS Latency 1)



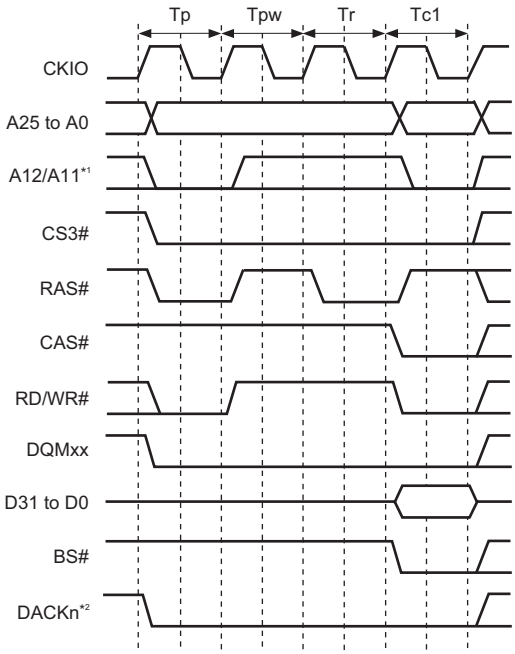
Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.25 Single Write Timing (Bank Active, Different Bank)



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.26 Single Write Timing (Bank Active, Same Row Addresses in the Same Bank)



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

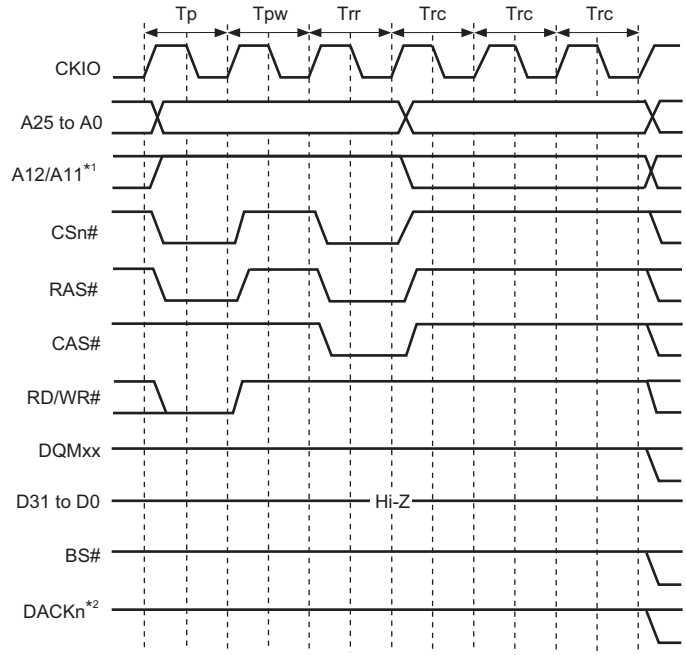
Figure 14.27 Single Write Timing (Bank Active, Different Row Addresses in the Same Bank)

(8) Refreshing

This module has a function for controlling SDRAM refreshing. Auto-refreshing can be performed by clearing the RMODE bit to 0 and setting the RFSH bit to 1 in SDCR. A continuous refreshing can be performed by setting the RRC2 to RRC0 bits in the RTCSR register. If SDRAM is not accessed for a long period, self-refresh mode, in which the power consumption for data retention is low, can be activated by setting both the RMODE bit and the RFSH bit to 1.

(a) Auto-refreshing

Refreshing is performed at intervals determined by the input clock selected by bits CKS2 to CKS0 in RTCSR, and the value set by in RTCOR. The value of bits CKS2 to CKS0 in RTCOR should be set so as to satisfy the refresh interval stipulation for the SDRAM used. First make the settings for RTCOR, RTCNT, and the RMODE and RFSH bits in SDCR, and then make the CKS2 to CKS0 and RRC2 to RRC0 settings. When the clock is selected by bits CKS2 to CKS0, RTCNT starts counting up from the value at that time. The RTCNT value is constantly compared with the RTCOR value, and if the two values are the same, a refresh request is generated and an auto-refresh is performed for the number of times specified by the RRC2 to RRC0. At the same time, RTCNT is cleared to zero and the count-up is restarted.
Figure 14.28 shows the auto-refresh cycle timing. After starting the auto refreshing, PALL command is issued in the Tp state to make all the banks to pre-charged state from active state when some bank is being pre-charged. Then REF command is issued in the Trr state after inserting idle states of which number is specified by the WTRP1 and WTRP0 bits in CS3WCR. A new command is not issued for the duration of the number of states specified by the WTRC1 and WTRC0 bits in CS3WCR after the Trr state. The WTRC1 and WTRC0 bits must be set so as to satisfy the SDRAM refreshing cycle time stipulation (tRC). An idle state is inserted between the Tp state and Trr state when the setting value of the WTRP1 and WTRP0 bits in CS3WCR is longer than or equal to 1 state.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.28 Auto-Refresh Timing

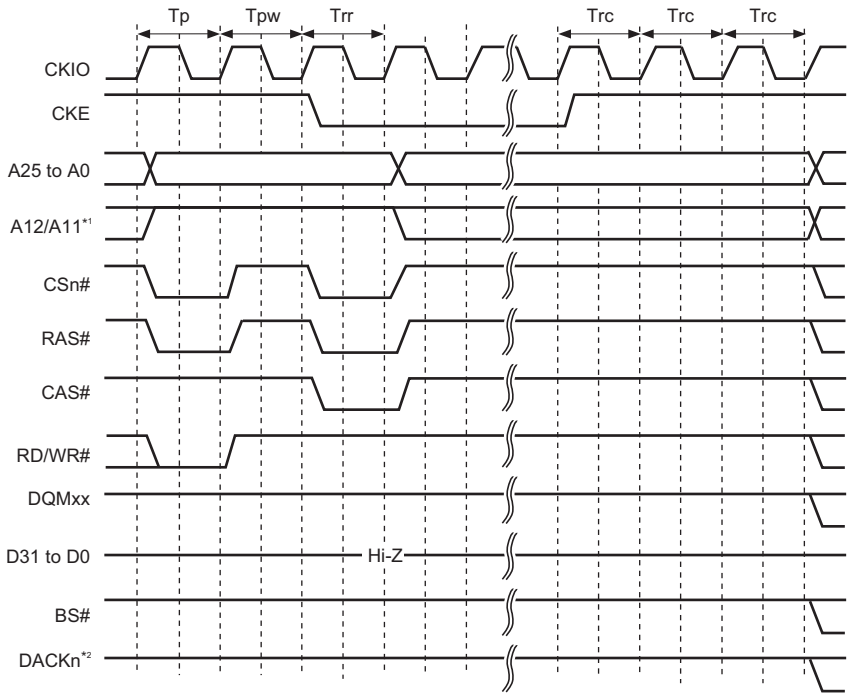
(b) Self-refreshing

Self-refresh mode is a kind of standby mode, in which the refresh timing and refresh addresses are generated within the SDRAM. This LSI enters self-refreshing by setting both the RMODE bit and the RFSH bit in SDCR to 1. After starting the self-refreshing, PALL command is issued in Tp state after the completion of the pre-charging bank. A SELF command is then issued after inserting idle states of which number is specified by the WTRP1 and WTRP0 bits in CS3WSR. SDRAM cannot be accessed while in the self-refresh state. Clearing the RMODE bit to 0 clears the self-refresh mode. After self-refresh mode has been cleared, command issuance is disabled for the number of states specified by the WTRC1 and WTRC0 bits in CS3WCR.

Self-refresh timing is shown in Figure 14.29. Settings must be made so that self-refresh clearing and data retention are performed correctly, and auto-refreshing is performed at the correct intervals. When self-refreshing is activated from the state in which auto-refreshing is set, auto-refreshing is restarted if the RFSH bit is set to 1 and the RMODE bit is cleared to 0 when self-refresh mode is cleared. If the transition from clearing of self-refresh mode to the start of auto-refreshing takes time, this time should be taken into consideration when setting the initial value of RTCNT. Making the RTCNT value 1 less than the RTCOR value will enable refreshing to be started immediately.

After self-refreshing has been set, the self-refresh state continues even if the chip standby state is entered using this LSI standby function, and is maintained even after recovery from standby mode due to an interrupt.

In case of a power-on reset, the bus state controller's registers are initialized, and therefore the self-refresh state is cleared.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

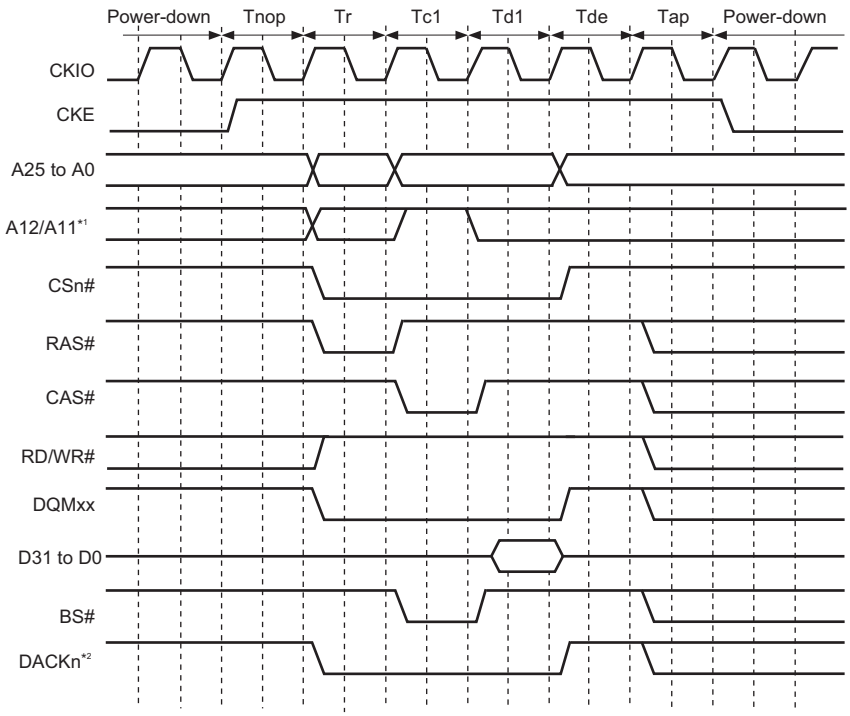
Figure 14.29 Self-Refresh Timing

(9) Relationship between Refresh Requests and Bus Cycles

If a refresh request occurs during bus cycle execution, the refresh cycle must wait for the bus cycle to be completed. If a new refresh request occurs while waiting for the previous refresh request, the previous refresh request is deleted. To refresh correctly, a bus cycle longer than the refresh interval must be prevented from occurring.

(10) Power-Down Mode

If the PDOWN bit in SDCR is set to 1 and the CKE signal is set to the low level after the access to the SDRAM, the SDRAM can enter the power-down mode. This power-down mode can effectively lower the power consumption in the non-access cycle. However, please note that if an access occurs in power-down mode, a state of overhead occurs because a state is needed to activate the CKE in order to cancel the power-down mode.
Figure 14.30 shows the access timing in power-down mode.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.30 Power-Down Mode Access Timing

(11) Power-On Sequence

In order to use SDRAM, mode setting must first be made for SDRAM after the pose interval specified for the SDRAM to be used after powering on. The pose interval should be obtained by a power-on reset generating circuit or software.
To perform SDRAM initialization correctly, the registers of this module must first be set, followed by a write to the SDRAM mode register. In SDRAM mode register setting, the address signal value at that time is latched by a combination of the CSn#, RAS#, CAS#, and RD/WR# signals. If the value to be set is X, the bus state controller provides for value X to be written to the SDRAM mode register by performing a 16-bit write to address A000 3000h + X for area 2 SDRAM, and to address A000 4000h + X for area 3 SDRAM. In this operation the data is ignored, but the mode write is performed as a byte-size access. To set burst read/single write or burst read/burst write (CAS latency 2 to 3, wrap type = sequential, and burst length 1) supported by this LSI, arbitrary data is written in 16 bits to the access addresses shown in Table 14.15. In this time 0 is output at the external address pins of A12 or later.

Table 14.15 Access Address in SDRAM Mode Register Write

- Setting for Area 2
  Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	A000 3440h	0000440h
	3	A000 3460h	0000460h
32 bits	2	A000 3880h	0000880h
	3	A000 38C0h	00008C0h

Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	A000 3040h	0000040h
	3	A000 3060h	0000060h
32 bits	2	A000 3080h	0000080h
	3	A000 30C0h	00000C0h

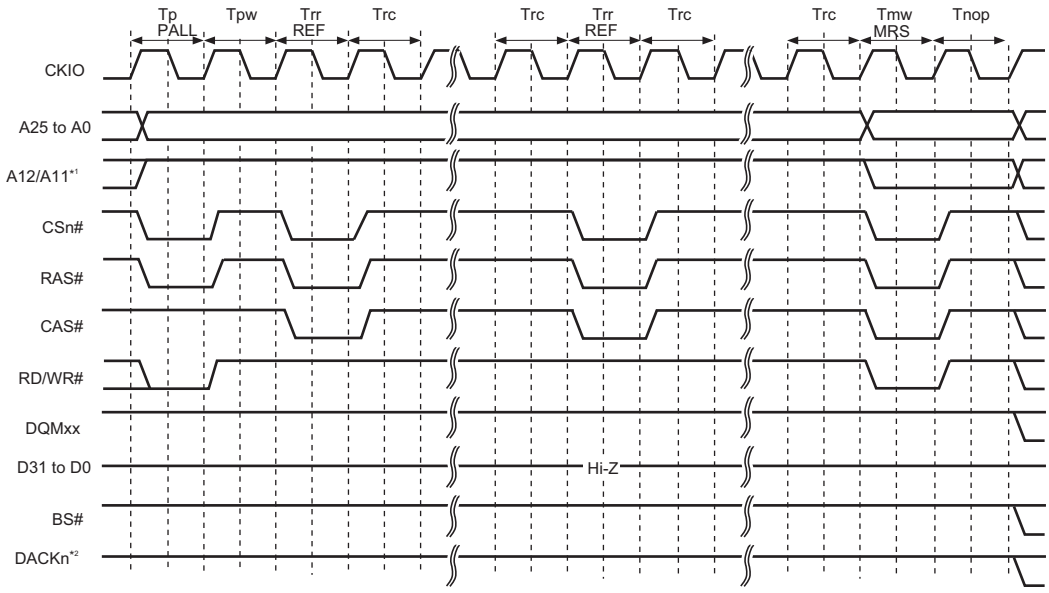
- Setting for Area 3
  Burst read/single write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	A000 4440h	0000440h
	3	A000 4460h	0000460h
32 bits	2	A000 4880h	0000880h
	3	A000 48C0h	00008C0h

Burst read/burst write (burst length 1):

Data Bus Width	CAS Latency	Access Address	External Address Pin
16 bits	2	A000 4040h	0000040h
	3	A000 4060h	0000060h
32 bits	2	A000 4080h	0000080h
	3	A000 40C0h	00000C0h

Mode register setting timing is shown in Figure 14.31. A PALL command (all bank pre-charge command) is firstly issued. A REF command (auto refresh command) is then issued 8 times. An MRS command (mode register write command) is finally issued. Idle states, of which number is specified by the WTRP1 and WTRP0 bits in CS3WCR, are inserted between the PALL and the first REF. Idle states, of which number is specified by the WTRC1 and WTRC0 bits in CS3WCR, are inserted between REF and REF, and between the 8th REF and MRS. One or more idle states are inserted between the MRS and a command to be issued next.
It is necessary to keep idle time of certain cycles for SDRAM before issuing PALL command after power-on. Refer to the manual of the SDRAM for the idle time to be needed. When the pulse width of the reset signal is longer than the idle time, mode register setting can be started immediately after the reset, but care should be taken when the pulse width of the reset signal is shorter than the idle time.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.31 SDRAM Mode Write Timing (Based on JEDEC)

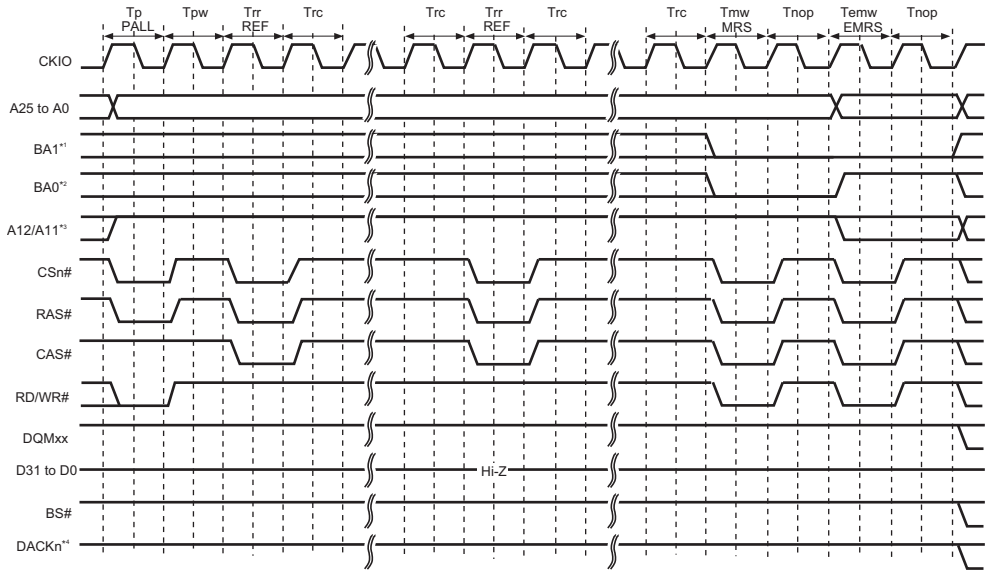
(12) Low-Power SDRAM

The low-power SDRAM can be accessed using the same protocol as the normal SDRAM.
The differences between the low-power SDRAM and normal SDRAM are that partial refresh takes place that puts only a part of the SDRAM in the self-refresh state during the self-refresh function, and that power consumption is low during refresh under user conditions such as the operating temperature. The partial refresh is effective in systems in which the data in a work area other than the specific area can be lost without severe repercussions. For details, please refer to the Data Sheet for the low-power SDRAM to be used.

The low-power SDRAM supports the extension mode register in addition to the mode registers as the normal SDRAM. This LSI supports issuing of the extension mode register write command (EMRS).
The EMRS command is issued according to Table 14.16. For example, if data 0YYY YYYYh is written to address A000 4XX0h in 32 bits, the commands are issued to the CS3 space in the following sequence: PALL -> REF × 8 -> MRS -> EMRS. In this case, the MRS and EMRS issue addresses are 0000XX0h and YYYYYYYh, respectively. If data 1YYY YYYYh is written to address A000 4XX0h in 32 bits, the commands are issued to the CS3 space in the following sequence: PALL -> MRS -> EMRS.

Table 14.16 Output Addresses when EMRS Command Is Issued

Command to be Issued	Access Address	Access Data	Write Access Size	MRS Command Issue Address	EMRS Command Issue Address
CS2 MRS	A000 3XX0h	**** ****h	16 bits	0000XX0h	-------h
CS3 MRS	A000 4XX0h	**** ****h	16 bits	0000XX0h	-------h
CS2 MRS + EMRS (with refresh)	A000 3XX0h	0YYY YYYYh	32 bits	0000XX0h	YYYYYYYh
CS3 MRS + EMRS (with refresh)	A000 4XX0h	0YYY YYYYh	32 bits	0000XX0h	YYYYYYYh
CS2 MRS + EMRS (without refresh)	A000 3XX0h	1YYY YYYYh	32 bits	0000XX0h	YYYYYYYh
CS3 MRS + EMRS (without refresh)	A000 4XX0h	1YYY YYYYh	32 bits	0000XX0h	YYYYYYYh

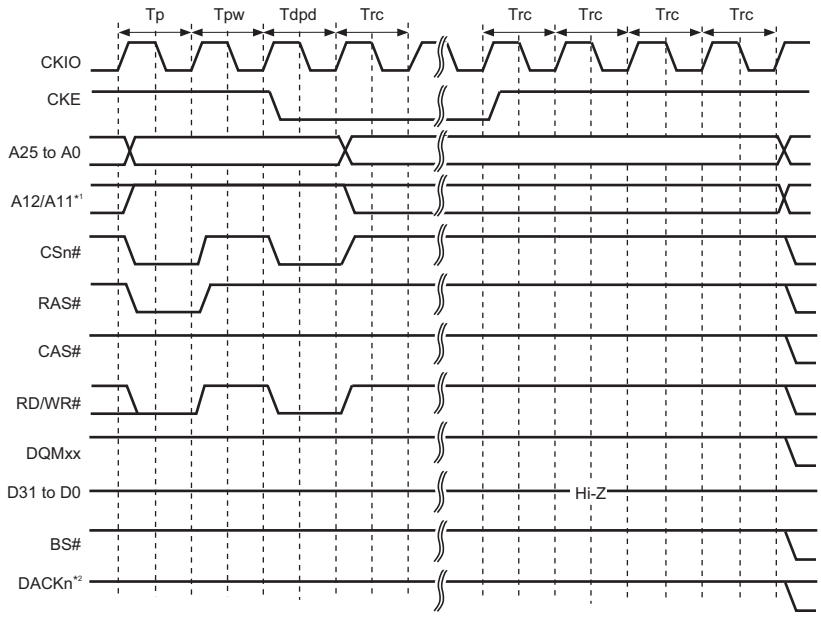


Note 1. Address pin to be connected to pin BA1 of SDRAM.
Note 2. Address pin to be connected to pin BA0 of SDRAM.
Note 3. Address pin to be connected to pin A10 of SDRAM.
Note 4. The waveform for DACKn is when active low is specified.

Figure 14.32 EMRS Command Issue Timing

- Deep power-down mode
  The low-power SDRAM supports the deep power-down mode as a low-power consumption mode. In the partial self-refresh function, self-refresh is performed on a specific area. In the deep power-down mode, self-refresh will not be performed on any memory area. This mode is effective in systems where all of the system memory areas are used as work areas.

If the RMODE bit in the SDCR is set to 1 while the DEEP and RFSH bits in the SDCR register are set to 1, the low-power SDRAM enters the deep power-down mode. If the RMODE bit is cleared to 0, the CKE signal is pulled high to cancel the deep power-down mode. Before executing an access after returning from the deep power-down mode, the power-up sequence must be re-executed.



Note 1. Address pin to be connected to pin A10 of SDRAM.
Note 2. The waveform for DACKn is when active low is specified.

Figure 14.33 Deep Power-Down Mode Transition Timing

14.4.7 Burst ROM (Clocked Asynchronous) Interface

The burst ROM (clocked asynchronous) interface is used to access a memory with a high-speed read function using a method of address switching called the burst mode or page mode. In a burst ROM (clocked asynchronous) interface, basically the same access as the SRAM interface is performed, but the 2nd and subsequent access cycles are performed only by changing the address, without inactivating the RD# signal at the end of the 1st cycle. In the 2nd and subsequent access cycles, addresses are changed at the falling edge of the CKIO signal.

For the 1st access cycle, the number of waits specified by the W3 to W0 bits in the CSnWCR register is inserted. For the 2nd and subsequent access cycles, the number of wait cycles specified by the BW1 and BW0 bits in the CSnWCR register is inserted.

In the access to the burst ROM (clocked asynchronous), the BS# signal is activated only to the first access cycle. An external wait input is valid only to the first access cycle.

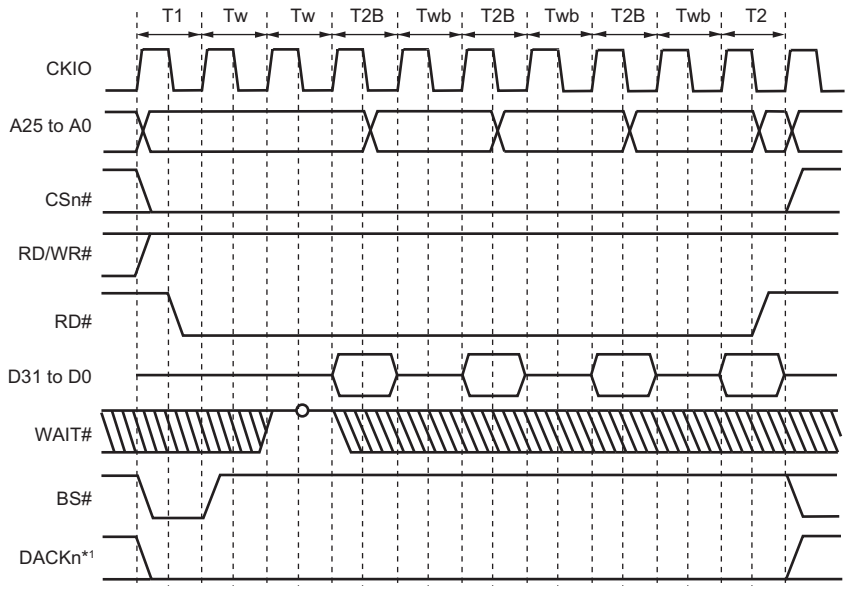
In the single access or write access that does not perform the burst operation in the burst ROM (clocked asynchronous) interface, access timing is same as an SRAM interface.

Table 14.17 lists a relationship between bus width, access size, and the number of bursts. Figure 14.34 shows a timing chart.

Table 14.17 Relationship between Bus Width, Access Size, and Number of Bursts

Bus Width	Access Size	CSnWCR.BST[1:0] Bits	Number of Bursts	Access Count
8 bits	8 bits	Not affected	1	1
	16 bits	Not affected	2	1
	32 bits	Not affected	4	1
	16 bytes	00	16	1
		01	4	4
	32 bytes	00	16	2
		01	4	8
	64 bytes	00	16	4
		01	4	16
16 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	2	1
	16 bytes	00	8	1
		01	2	4
		10*1	4	2
			2, 4, 2	3
	32 bytes	00	8	2
		01	2	8
		10*1	4	4
			2, 4, 2	6
	64 bytes	00	8	4
		01	2	16
		10*1	4	8
			2, 4, 2	12
32 bits	8 bits	Not affected	1	1
	16 bits	Not affected	1	1
	32 bits	Not affected	1	1
	16 bytes	Not affected	4	1
	32 bytes	Not affected	4	2
	64 bytes	Not affected	4	4

Note 1. When the bus width is 16 bits, the access size is 16 bits or more, and the BST[1:0] bits in CSnWCR are 10b, the number of bursts and access count depend on the access start address. At address xxx0h or xxx8h, 4-4 burst access is performed (burst numbers: 4,4 for a total of 2 rounds of access). At address xxx4h or xxxCh, 2-4-2 burst access is performed (burst numbers: 2, 4, 2 for a total of 3 rounds of access).



Note 1. The waveform for DACKn is when active low is specified.

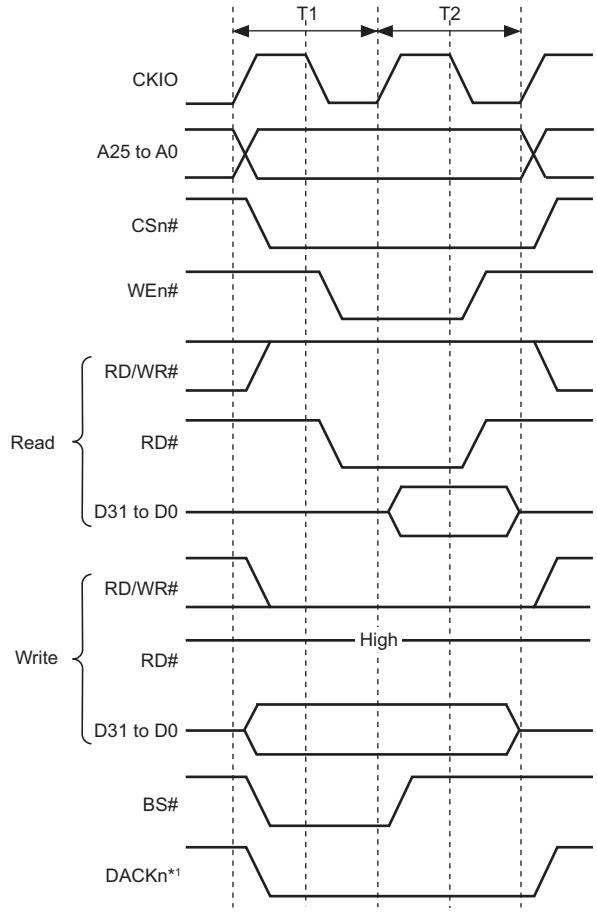
Figure 14.34 Burst ROM Access Timing (Clocked Asynchronous) (Bus Width = 32 Bits, 16-Byte Transfer (Number of Burst 4), Wait Cycles Inserted in First Access = 2, Wait Cycles Inserted in Second and Subsequent Access Cycles = 1)

14.4.8 SRAM Interface with Byte Selection

The SRAM interface with byte selection is a memory interface that outputs the byte selection signal (WEn#) in both read and write bus cycles. This interface has 16-bit data pins and accesses SRAMs having upper and lower byte selection pins, such as UB# and LB#.

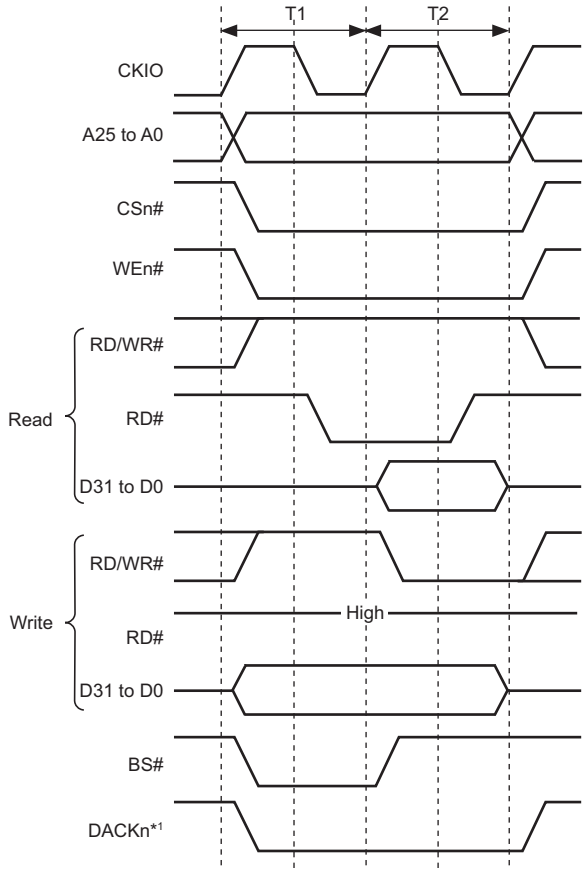
When the BAS bit in CSnWCR is cleared to 0 (value after reset), the write access timing of the SRAM interface with byte selection is the same as that for the SRAM interface. While in read access of a byte-selection SRAM interface, the byte-selection signal is output from the WEn# pin, which is different from that for the SRAM interface. The basic access timing is shown in Figure 14.35. In write access, data is written to the memory according to the timing of the byte-selection pin (WEn#). For details, please refer to the Data Sheet for the corresponding memory.

If the BAS bit in CSnWCR is set to 1, the WEn# pin and RD/WR# pin timings change. Figure 14.36 shows the basic access timing. In write access, data is written to the memory according to the timing of the write enable pin (RD/WR#). The data hold of write data at the timing of RD/WR# inactive must be acquired by setting the HW1 and HW0 bits in the CSnWCR register. Figure 14.37 shows the access timing when a software wait is specified.



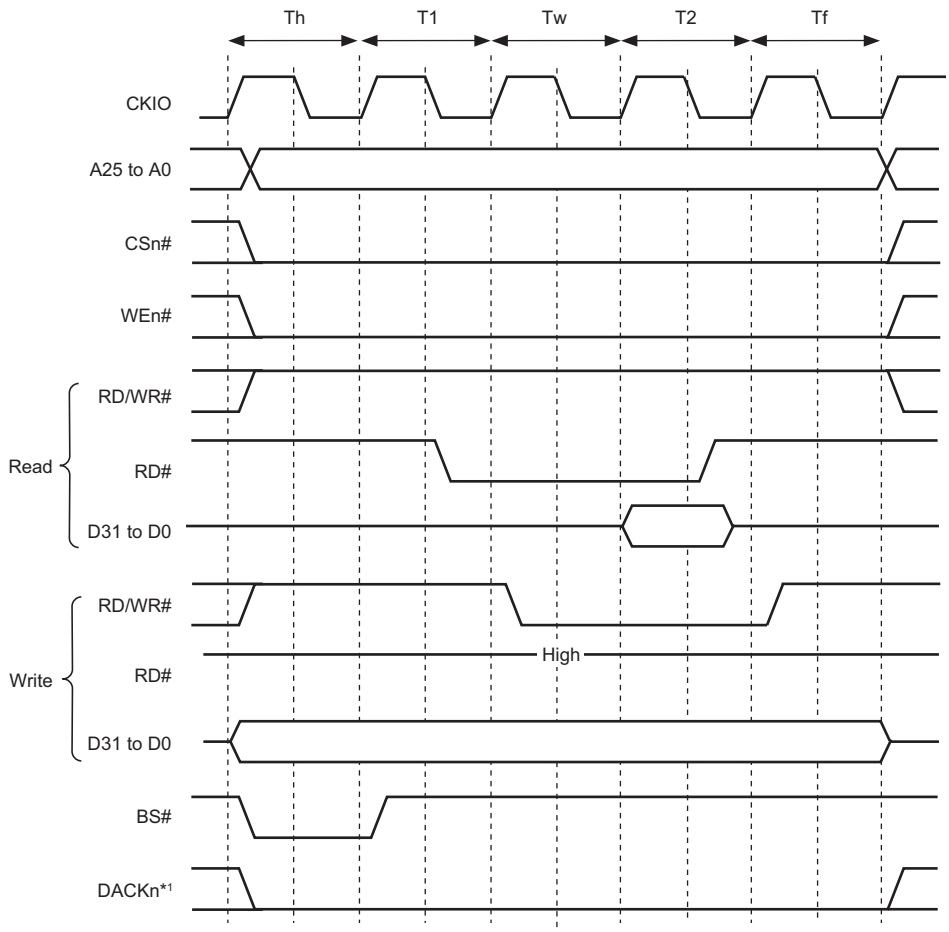
Note 1. The waveform for DACKn is when active low is specified.

Figure 14.35 Basic Access Timing for SRAM with Byte Selection (BAS = 0)



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.36 Basic Access Timing for SRAM with Byte Selection (BAS = 1)



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.37 Wait Timing for SRAM with Byte Selection (BAS = 1) (SW[1:0] = 01b, WR[3:0] = 0001b, HW[1:0] = 01b)

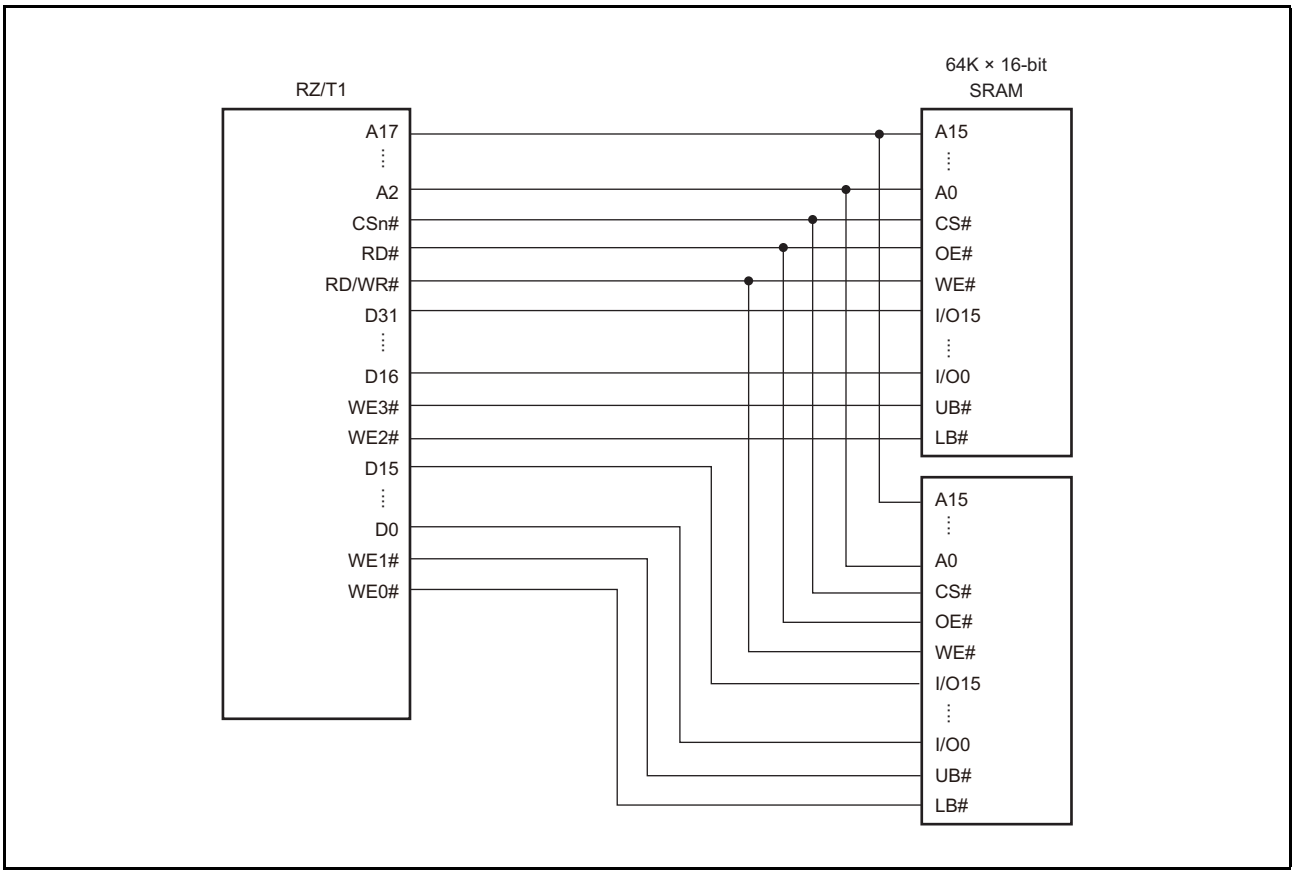


Figure 14.38 Example of Connection with 32-Bit Data-Width SRAM with Byte Selection

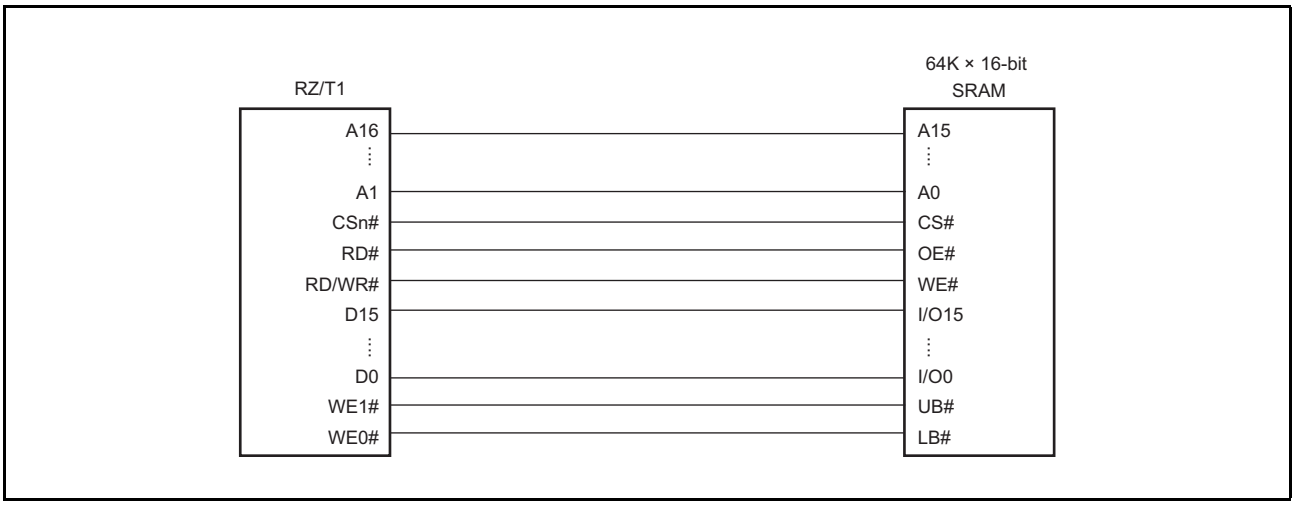


Figure 14.39 Example of Connection with 16-Bit Data-Width SRAM with Byte Selection

14.4.9 Burst ROM (Clocked Synchronous) Interface

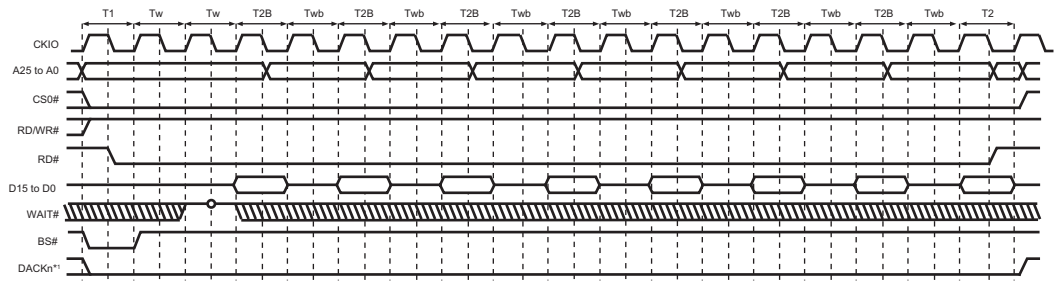
The burst ROM (clocked synchronous) interface is supported to access a ROM with a synchronous burst function at high speed. The burst ROM interface accesses the burst ROM in the same way as an SRAM interface. This interface is valid only for area 0.

In the first access cycle, wait cycles are inserted. In this case, the number of wait cycles to be inserted is specified by the W3 to W0 bits in CS0WCR. In the second and subsequent cycles, the number of wait cycles to be inserted is specified by the BW1 and BW0 bits in CS0WCR.

While the burst ROM (clocked synchronous) is accessed, the BS# signal is activated only for the first access cycle and an external wait input is also valid for the first access cycle.

When the bus width is 16 bits, the burst length must be specified as 8. When the bus width is 32 bits, the burst length must be specified as 4. The burst ROM interface does not support the 8-bit bus width for the burst ROM.

The burst ROM interface performs burst operations for all read access. For example, in a 32-bit access over a 16-bit bus, valid 16-bit data is read two times and invalid 16-bit data is read six times. These invalid data read cycles increase the memory access time and degrade the program execution speed and DMA transfer speed. To prevent this problem, it is recommended using a read in a 16-byte or more access size. The burst ROM interface performs write access in the same way as SRAM interface access.



Note 1. The waveform for DACKn is when active low is specified.

Figure 14.40 Burst ROM Access Timing (Clocked Synchronous) (Burst Length = 8, Wait Cycles Inserted in First Access = 2, Wait Cycles Inserted in Second and Subsequent Access Cycles = 1)

14.4.10 Wait between Access Cycles

As the operating frequency of LSIs becomes higher, the off-operation of the output data buffer for devices with slow access speed often collides with the data output for the next cycle. As a result of these collisions, the reliability of the device might be lowered or malfunctions might occur. Data collisions can be avoided by inserting idle (wait) cycles between continuous access cycles.
The number of idle states between access cycles can be set by the WM bit in CSnWCR, bits IWW2 to IWW0, IWRWD2 to IWRWD0, IWRWS2 to IWRWS0, IWRRD2 to IWRRD0, and IWRRS2 to IWRRS 0 in CSnBCR. The conditions for setting the idle cycles between access cycles are shown below.

1. Continuous access cycles are write-read or write-write
2. Continuous access cycles are read-write for different spaces
3. Continuous access cycles are read-write for the same space
4. Continuous access cycles are read-read for different spaces
5. Continuous access cycles are read-read for the same space

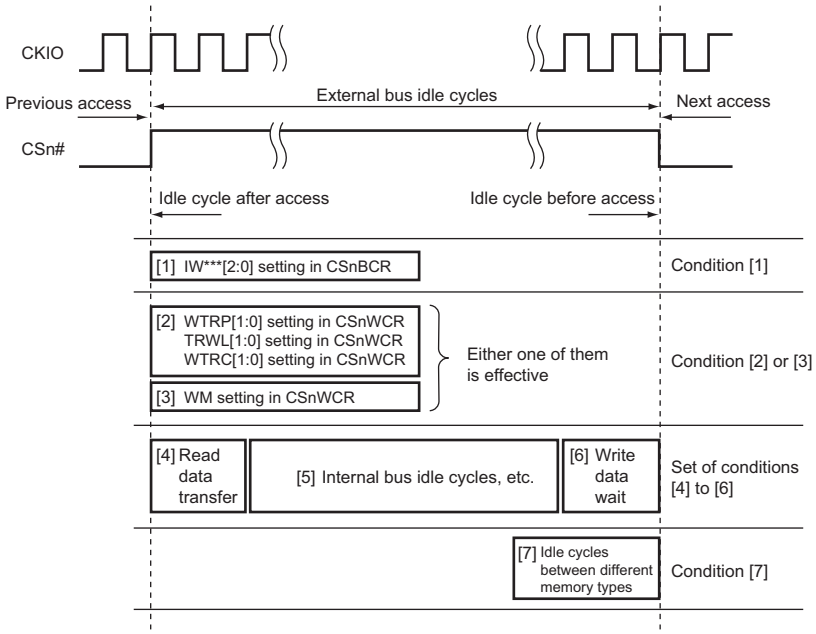
For the specification of the number of idle cycles between access cycles described above, refer to the description of each register.

Besides the idle states between access cycles specified by the registers, idle cycles must be inserted to interface with the internal bus or to obtain the minimum pulse width for a multiplexed pin (WEn#). The following gives detailed information about the idle cycles and describes how to estimate the number of idle cycles.
The number of idle cycles on the external bus from the inactive state of the CSn# signal to the active state of CSn# is described below.
There are seven conditions that determine the number of idle cycles on the external bus as shown in Table 14.18. The effects of these conditions are shown in Figure 14.41.

Table 14.18 Conditions for Determining Number of Idle Cycles

No.	Condition	Description	Range	Note
[1]	IW***[2:0] in CSnBCR	These bits specify the number of idle cycles for access. The number of idle cycles can be specified independently for each combination of the previous and next cycles. For example, in the case where reading CS1 space followed by reading other CS space, the bits IWRRD[2:0] in CS1BCR should be set to 100b to specify six or more idle cycles. This condition is effective only for access states other than single address transfer and generates idle states after the access is completed.	0 to 12	Do not set 0 for the number of idle cycles between memory types which are not allowed to be accessed successively.
[2]	SDRAM-related bits in CSnWCR	These bits specify precharge completion and startup wait states and idle states between commands for SDRAM access. This condition is effective only for SDRAM access and generates idle states after the access is completed	0 to 3	Specify these bits in accordance with the specification of the target SDRAM.
[3]	WM in CSnWCR	This bit enables or disables external WAIT# pin input for the memory types other than SDRAM. When this bit is cleared to 0 (external WAIT# enabled), one idle state is inserted to check the external WAIT# pin input after the access is completed. When this bit is set to 1 (disabled), no idle state is generated.	0 or 1	
[4]	Read data transfer cycle	One idle state is inserted after a read access is completed. This idle state is not generated for the first or middle cycles in divided access cycles. This is neither generated when the HW[1:0] bits in CSnWCR are not 00b.	0 or 1	One idle state is always inserted during a read cycle with SDRAM.
[5]	Internal bus idle cycles, etc.	External bus access requests from the CPU or the direct memory access controller (DMA) and their results are passed through the internal bus. The external bus enters idle state during internal bus idle cycles or while a bus other than the external bus is being accessed. This condition is not effective for divided access cycles, which are generated by the bus state controller when the access size is larger than the external data bus width.	0 or larger	The number of internal bus idle cycles may not become 0 depending on the CPU: internal bus: CKIO
[6]	Write data wait cycles	During write access, a write cycle is executed on the external bus only after the write data becomes ready. This write data wait period generates idle cycles before the write cycle. Note that when the previous cycle is a write cycle and the internal bus idle cycles are shorter than the previous write cycle, write data can be prepared in parallel with the previous write cycle and therefore, no idle cycle is generated (write buffer effect).	0 or 1	For write → write or write → read access cycles, successive access cycles without idle cycles may be available due to the write buffer effect described in the left column. If successive access cycles without idle cycles are not allowed, specify the minimum number of idle cycles between access cycles through the CSnBCR register.
[7]	Idle cycles between different memory types	To ensure the minimum pulse width on the multi-use pins, idle cycles may be inserted before access after memories are switched. For some memory types, idle cycles are inserted even when memory types are not switched.	0 to 2	The number of idle cycles depends on the target memory types. See Table 14.19.

In the above conditions, a total of four conditions, that is, condition [1], condition [2] or [3] (either one is effective), a set of conditions [4] to [6] (these are generated successively, and therefore the sum of them should be taken as one set of idle cycles), and condition [7] are generated at the same time. The maximum number of idle cycles among these four conditions become the number of idle cycles on the external bus. To ensure the minimum idle cycles, be sure to make register settings for condition [1].



Note: A total of four conditions (condition [1], condition [2] or [3], a set of conditions [4] to [6], and condition [7]) generate idle cycle at the same time. Accordingly, the maximum number of cycles among these four conditions become the number of idle cycles.

Figure 14.41 Idle Cycle Conditions

Table 14.19 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types

	Next Cycle						
Previous Cycle	**SRAM**	**Burst ROM (Asynchronous)**	**MPX-I/O**	**Byte SRAM (BAS = 0)**	**Byte SRAM (BAS = 1)**	**SDRAM**	**Burst ROM (Synchronous)**
SRAM	0	0	1	0	0/1*1	0/1*1	0
Burst ROM (asynchronous)	0	0	1	0	0/1*1	0/1*1	0
MPX-I/O	1	1	0	1	1	1	1
Byte SRAM (BAS = 0)	0	0	1	0	0/1*1	0/1*1	0
Byte SRAM (BAS = 1)	0/1*1	0/1*1	1/2*1	0/1*1	0	0	0/1*1
SDRAM	1	1	2	1	0	0	1
Burst ROM (synchronous)	0	0	1	0	1	1	0

Note 1. The number of idle cycles depends on the setting of the CSnWCR.HW[1:0] bits in the previous cycle. When HW[1:0] ≠ 00b, the number of idle cycles is the value on the left; when HM[1:0] = 00b, the number of idle cycles is the value on the right. If the CSnWCR.HW[1:0] bits were for a CSn space that does not exist in the previous cycle, the number of idle cycles is the value on the right.

14.4.11 Others

(1) Reset

This module can be initialized completely only at reset of the entire chip (pin reset, software reset, and ECM reset). When reset of the entire chip occurs, all signals are inactivated and data output buffers are turned off regardless of the bus cycle state after the internal reset is synchronized with the internal clock. All control registers are initialized. In the chip standby state, control registers of the bus state controller are not initialized.

(2) Caution on Write Buffer

Since the bus state controller incorporates a one-stage write buffer, it can execute an access via the internal bus before the previous external bus cycle is completed in a write cycle. If the on-chip module is read or written after the external low-speed memory is written, the on-chip module can be accessed before the completion of the external low-speed memory write cycle.

In read cycles, the CPU is placed in the wait state until read operation has been completed. To continue the process after the data write to the device has been completed, perform a dummy read to the same address to check for completion of the write before the next process to be executed.

The write buffer of the bus state controller functions in the same way for an access by a bus master other than the CPU such as the direct memory access controller (DMA). Accordingly, to perform DMA transfers, the next read cycle is initiated before the previous write cycle is completed. Note, however, that if both the DMA source and destination addresses exist in external memory space, the next read cycle will not be initiated until the previous write cycle is completed.

Changing the registers in this module while the write buffer is operating may disrupt correct write access. Therefore, do not change the registers in this module immediately after a write access. If this change becomes necessary, do it after executing a dummy read of the write data.

15. DMA Controller (DMACAa)

This LSI contains DMAC (Direct Memory Access Controller) consisting of two units, DMAC0 and DMAC1. DMAC transfers data without using the CPU. When a transfer is requested, DMAC transfers data stored at the transfer source address to the transfer destination address.

15.1 Overview

Table 15.1 lists specifications of DMAC.

Table 15.1 Specifications of DMAC

Item		Description	
		DMAC0	**DMAC1**
Number of channels		16 channels	16 channels
Address space		4 Gbytes	
DMAC activation source		External request (DREQ)/external interrupts (IRQ) On-chip peripheral module requests/software requests*1	
Channel priority		• Selectable from fixed priority or round-robin for channels 0 to 7 and for channels 8 to 15. • Round-robin arbitration between channels 0 to 7 and channels 8 to 15	
Transfer data unit		8, 16, 32, 128, 256, and 512 bits	8, 16, 32, and 128 bits
Maximum transfer size		$2^{32} - 1$ bytes	
Transfer mode	Single transfer	Performs DMA transfer for each DMA transfer request.	
	Block transfer	Performs DMA transfer of the specified size for a single DMAC activation request.	
DMA mode	Register mode	• DMA transfer setting value: Control register value within the DMA controller • DMA transfer to the source/destination specified by a register	
	Link mode	• DMA transfer setting value: Descriptors in the internal RAM or an external memory. • Various DMA transfers specified by descriptors can be performed (responsiveness: register mode > link mode).	
Interval function		The DMA transfer interval can be specified (bus occupation ratio can be adjusted).	
Skip function		• For the area to be accessed by DMA transfer, the continuous access size and the discrete access size (skip) can be set separately. • After the size of data specified for the continuous access is transferred, the specified number of addresses to be accessed next can be skipped.	
Suspending function		Current DMA transfer can be paused.	
Buffer flush function		When DMAC is stopped forcibly, data in the buffer can be flushed.	
Interrupt request		Each channel has the following interrupt requests: • Transfer completion: Indicates completion of transfer of the specified size; each channel has this source. • Transfer error: Indicates a bus error; total of two sources, one for unit 0 and the other for unit 1.	

Note 1. A software request is output as a source of an on-chip peripheral module request from the interrupt controller. For how to set a software request, see section 12, Interrupt Controller (ICUA).

Table 15.2 lists the input/output pins of the DMAC.

Table 15.2 Pin Configuration of the DMAC

Pin Name	I/O	Description
DREQ0	Input	DMA transfer request input from an external device to DMAC0
DREQ1	Input	DMA transfer request input from an external device to DMAC0
DREQ2	Input	DMA transfer request input from an external device to DMAC1
DACK0	Output	Output of DMAC transfer request acceptance from DMAC0 to an external device
DACK1	Output	Output of DMAC transfer request acceptance from DMAC0 to an external device
DACK2	Output	Output of DMAC transfer request acceptance from DMAC1 to an external device
TEND0	Output	Output of transfer completion from DMAC0 to an external device
TEND1	Output	Output of transfer completion from DMAC0 to an external device
TEND2	Output	Output of transfer completion from DMAC1 to an external device

Note: For details on active levels from DACK0 to DACK2, and TEND0 to TEND2, see section 15.2.11, Common Control Register (CMNCR) and section 15.3.5, DMA Acknowledge Output/DMA Transaction Completion Output Function.

15.2 Register Descriptions

15.2.1 Next Source Address Register n (N0SA_n_N, N0SA_n_W, N1SA_n_N, N1SA_n_W)

The N0SA_n and N1SA_n registers set the DMA transfer source address of DMA channel n (n = 15 to 0).
The N0SA_n register is for Next0 Register Set, and the N1SA_n register is for Next1 Register Set.
In write-only mode (CHCFG_n register WONLY = 1), this register is used to set writing data.

- For N0SA_n_N and N1SA_n_N (normal mode)

Address(es): DMAC0
N0SA_0_N: A006 2000h, N0SA_1_N: A006 2040h, N0SA_2_N: A006 2080h, N0SA_3_N: A006 20C0h,
N0SA_4_N: A006 2100h, N0SA_5_N: A006 2140h, N0SA_6_N: A006 2180h, N0SA_7_N: A006 21C0h,
N0SA_8_N: A006 2400h, N0SA_9_N: A006 2440h, N0SA_10_N: A006 2480h, N0SA_11_N: A006 24C0h,
N0SA_12_N: A006 2500h, N0SA_13_N: A006 2540h, N0SA_14_N: A006 2580h, N0SA_15_N: A006 25C0h
DMAC1
N0SA_0_N: A006 3000h, N0SA_1_N: A006 3040h, N0SA_2_N: A006 3080h, N0SA_3_N: A006 30C0h,
N0SA_4_N: A006 3100h, N0SA_5_N: A006 3140h, N0SA_6_N: A006 3180h, N0SA_7_N: A006 31C0h,
N0SA_8_N: A006 3400h, N0SA_9_N: A006 3440h, N0SA_10_N: A006 3480h, N0SA_11_N: A006 34C0h,
N0SA_12_N: A006 3500h, N0SA_13_N: A006 3540h, N0SA_14_N: A006 3580h, N0SA_15_N: A006 35C0h

DMAC0
N1SA_0_N: A006 200Ch, N1SA_1_N: A006 204Ch, N1SA_2_N: A006 208Ch, N1SA_3_N: A006 20CCh,
N1SA_4_N: A006 210Ch, N1SA_5_N: A006 214Ch, N1SA_6_N: A006 218Ch, N1SA_7_N: A006 21CCh,
N1SA_8_N: A006 240Ch, N1SA_9_N: A006 244Ch, N1SA_10_N: A006 248Ch, N1SA_11_N: A006 24CCh,
N1SA_12_N: A006 250Ch, N1SA_13_N: A006 254Ch, N1SA_14_N: A006 258Ch, N1SA_15_N: A006 25CCh
DMAC1
N1SA_0_N: A006 300Ch, N1SA_1_N: A006 304Ch, N1SA_2_N: A006 308Ch, N1SA_3_N: A006 30CCh,
N1SA_4_N: A006 310Ch, N1SA_5_N: A006 314Ch, N1SA_6_N: A006 318Ch, N1SA_7_N: A006 31CCh,
N1SA_8_N: A006 340Ch, N1SA_9_N: A006 344Ch, N1SA_10_N: A006 348Ch, N1SA_11_N: A006 34CCh,
N1SA_12_N: A006 350Ch, N1SA_13_N: A006 354Ch, N1SA_14_N: A006 358Ch, N1SA_15_N: A006 35CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SA[31:0] (Normal mode)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SA[31:0] (Normal mode)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SA[31:0] (Normal mode)	Source Address	Sets the start address of the DMA transfer source.	R/W

Note: During link mode transfer, descriptor read data is set to the N0SA_n_N register automatically.

- For N0SA_n_W and N1SA_n_W (write-only mode)

Address(es): DMAC0
N0SA_0_W: A006 2000h, N0SA_1_W: A006 2040h, N0SA_2_W: A006 2080h, N0SA_3_W: A006 20C0h,
N0SA_4_W: A006 2100h, N0SA_5_W: A006 2140h, N0SA_6_W: A006 2180h, N0SA_7_W: A006 21C0h,
N0SA_8_W: A006 2400h, N0SA_9_W: A006 2440h, N0SA_10_W: A006 2480h, N0SA_11_W: A006 24C0h,
N0SA_12_W: A006 2500h, N0SA_13_W: A006 2540h, N0SA_14_W: A006 2580h, N0SA_15_W: A006 25C0h
DMAC1
N0SA_0_W: A006 3000h, N0SA_1_W: A006 3040h, N0SA_2_W: A006 3080h, N0SA_3_W: A006 30C0h,
N0SA_4_W: A006 3100h, N0SA_5_W: A006 3140h, N0SA_6_W: A006 3180h, N0SA_7_W: A006 31C0h,
N0SA_8_W: A006 3400h, N0SA_9_W: A006 3440h, N0SA_10_W: A006 3480h, N0SA_11_W: A006 34C0h,
N0SA_12_W: A006 3500h, N0SA_13_W: A006 3540h, N0SA_14_W: A006 3580h, N0SA_15_W: A006 35C0h

DMAC0
N1SA_0_W: A006 200Ch, N1SA_1_W: A006 204Ch, N1SA_2_W: A006 208Ch, N1SA_3_W: A006 20CCh,
N1SA_4_W: A006 210Ch, N1SA_5_W: A006 214Ch, N1SA_6_W: A006 218Ch, N1SA_7_W: A006 21CCh,
N1SA_8_W: A006 240Ch, N1SA_9_W: A006 244Ch, N1SA_10_W: A006 248Ch, N1SA_11_W: A006 24CCh,
N1SA_12_W: A006 250Ch, N1SA_13_W: A006 254Ch, N1SA_14_W: A006 258Ch, N1SA_15_W: A006 25CCh
DMAC1
N1SA_0_W: A006 300Ch, N1SA_1_W: A006 304Ch, N1SA_2_W: A006 308Ch, N1SA_3_W: A006 30CCh,
N1SA_4_W: A006 310Ch, N1SA_5_W: A006 314Ch, N1SA_6_W: A006 318Ch, N1SA_7_W: A006 31CCh,
N1SA_8_W: A006 340Ch, N1SA_9_W: A006 344Ch, N1SA_10_W: A006 348Ch, N1SA_11_W: A006 34CCh,
N1SA_12_W: A006 350Ch, N1SA_13_W: A006 354Ch, N1SA_14_W: A006 358Ch, N1SA_15_W: A006 35CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	WD[31:0] (Write-only mode)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WD[31:0] (Write-only mode)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	WD[31:0] (Write-only mode)	Write Data	Sets write data for write-only mode.	R/W

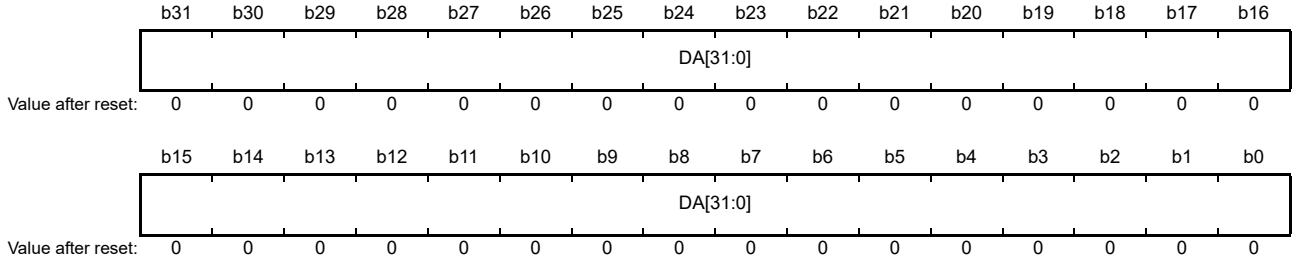
Note: During link mode transfer, descriptor read data is set to the N0SA_n_W register automatically.

15.2.2 Next Destination Address Register n (N0DA_n and N1DA_n)

The N0DA_n and N1DA_n registers set the DMA transfer destination address of DMA channel n (n = 15 to 0).
The N0DA_n register is for Next0 Register Set, and the N1DA_n register is for the Next1 Register Set.

Address(es): DMAC0
N0DA_0: A006 2004h, N0DA_1: A006 2044h, N0DA_2: A006 2084h, N0DA_3: A006 20C4h,
N0DA_4: A006 2104h, N0DA_5: A006 2144h, N0DA_6: A006 2184h, N0DA_7: A006 21C4h,
N0DA_8: A006 2404h, N0DA_9: A006 2444h, N0DA_10: A006 2484h, N0DA_11: A006 24C4h,
N0DA_12: A006 2504h, N0DA_13: A006 2544h, N0DA_14: A006 2584h, N0DA_15: A006 25C4h
DMAC1
N0DA_0: A006 3004h, N0DA_1: A006 3044h, N0DA_2: A006 3084h, N0DA_3: A006 30C4h,
N0DA_4: A006 3104h, N0DA_5: A006 3144h, N0DA_6: A006 3184h, N0DA_7: A006 31C4h,
N0DA_8: A006 3404h, N0DA_9: A006 3444h, N0DA_10: A006 3484h, N0DA_11: A006 34C4h,
N0DA_12: A006 3504h, N0DA_13: A006 3544h, N0DA_14: A006 3584h, N0DA_15: A006 35C4h

DMAC0
N1DA_0: A006 2010h, N1DA_1: A006 2050h, N1DA_2: A006 2090h, N1DA_3: A006 20D0h,
N1DA_4: A006 2110h, N1DA_5: A006 2150h, N1DA_6: A006 2190h, N1DA_7: A006 21D0h,
N1DA_8: A006 2410h, N1DA_9: A006 2450h, N1DA_10: A006 2490h, N1DA_11: A006 24D0h,
N1DA_12: A006 2510h, N1DA_13: A006 2550h, N1DA_14: A006 2590h, N1DA_15: A006 25D0h
DMAC1
N1DA_0: A006 3010h, N1DA_1: A006 3050h, N1DA_2: A006 3090h, N1DA_3: A006 30D0h,
N1DA_4: A006 3110h, N1DA_5: A006 3150h, N1DA_6: A006 3190h, N1DA_7: A006 31D0h,
N1DA_8: A006 3410h, N1DA_9: A006 3450h, N1DA_10: A006 3490h, N1DA_11: A006 34D0h,
N1DA_12: A006 3510h, N1DA_13: A006 3550h, N1DA_14: A006 3590h, N1DA_15: A006 35D0h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	DA[31:0]	Destination Address	Sets the start address of the DMA transfer destination.	R/W

Note: During link mode transfer, descriptor read data is set to the N0DA_n register automatically.

15.2.3 Next Transaction Byte Register n (N0TB_n and N1TB_n)

The N0TB_n and N1TB_n registers set the total number of transfer bytes of DMA channel n (n = 15 to 0).
The N0TB_n register is for Next0 Register Set, and the N1TB_n register is for Next1 Register Set.

Address(es): DMAC0
N0TB_0: A006 2008h, N0TB_1: A006 2048h, N0TB_2: A006 2088h, N0TB_3: A006 20C8h,
N0TB_4: A006 2108h, N0TB_5: A006 2148h, N0TB_6: A006 2188h, N0TB_7: A006 21C8h,
N0TB_8: A006 2408h, N0TB_9: A006 2448h, N0TB_10: A006 2488h, N0TB_11: A006 24C8h,
N0TB_12: A006 2508h, N0TB_13: A006 2548h, N0TB_14: A006 2588h, N0TB_15: A006 25C8h
DMAC1
N0TB_0: A006 3008h, N0TB_1: A006 3048h, N0TB_2: A006 3088h, N0TB_3: A006 30C8h,
N0TB_4: A006 3108h, N0TB_5: A006 3148h, N0TB_6: A006 3188h, N0TB_7: A006 31C8h,
N0TB_8: A006 3408h, N0TB_9: A006 3448h, N0TB_10: A006 3488h, N0TB_11: A006 34C8h,
N0TB_12: A006 3508h, N0TB_13: A006 3548h, N0TB_14: A006 3588h, N0TB_15: A006 35C8h

DMAC0
N1TB_0: A006 2014h, N1TB_1: A006 2054h, N1TB_2: A006 2094h, N1TB_3: A006 20D4h,
N1TB_4: A006 2114h, N1TB_5: A006 2154h, N1TB_6: A006 2194h, N1TB_7: A006 21D4h,
N1TB_8: A006 2414h, N1TB_9: A006 2454h, N1TB_10: A006 2494h, N1TB_11: A006 24D4h,
N1TB_12: A006 2514h, N1TB_13: A006 2554h, N1TB_14: A006 2594h, N1TB_15: A006 25D4h
DMAC1
N1TB_0: A006 3014h, N1TB_1: A006 3054h, N1TB_2: A006 3094h, N1TB_3: A006 30D4h,
N1TB_4: A006 3114h, N1TB_5: A006 3154h, N1TB_6: A006 3194h, N1TB_7: A006 31D4h,
N1TB_8: A006 3414h, N1TB_9: A006 3454h, N1TB_10: A006 3494h, N1TB_11: A006 34D4h,
N1TB_12: A006 3514h, N1TB_13: A006 3554h, N1TB_14: A006 3594h, N1TB_15: A006 35D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TB[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TB[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TB[31:0]	Transaction Byte	Sets the total number of transfer bytes. Note 1. Do not start DMA transfer when 0 is set.	R/W

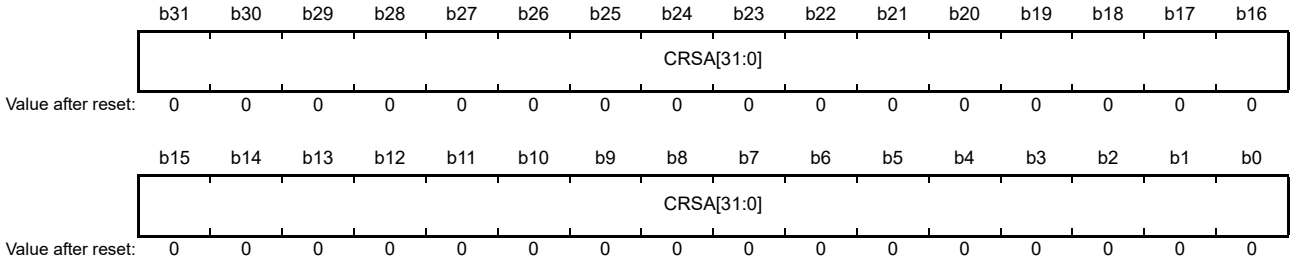
Note: During link mode transfer, descriptor read data is set to the N0TB_n register automatically.

15.2.4 Current Source Address Register (CRSA_n)

The CRSA_n register is a register that indicates the DMA transfer source address of DMA channel n (n = 15 to 0).

During DMA transfer, the value is incremented automatically (fixed when the SAD bit in the CHCFG_n register = 1, and not fixed when the WONLY bit in the CHCFG_n register = 1).

Address(es): DMAC0
CRSA_0: A006 2018h, CRSA_1: A006 2058h, CRSA_2: A006 2098h, CRSA_3: A006 20D8h,
CRSA_4: A006 2118h, CRSA_5: A006 2158h, CRSA_6: A006 2198h, CRSA_7: A006 21D8h,
CRSA_8: A006 2418h, CRSA_9: A006 2458h, CRSA_10: A006 2498h, CRSA_11: A006 24D8h,
CRSA_12: A006 2518h, CRSA_13: A006 2558h, CRSA_14: A006 2598h, CRSA_15: A006 25D8h
DMAC1
CRSA_0: A006 3018h, CRSA_1: A006 3058h, CRSA_2: A006 3098h, CRSA_3: A006 30D8h,
CRSA_4: A006 3118h, CRSA_5: A006 3158h, CRSA_6: A006 3198h, CRSA_7: A006 31D8h,
CRSA_8: A006 3418h, CRSA_9: A006 3458h, CRSA_10: A006 3498h, CRSA_11: A006 34D8h,
CRSA_12: A006 3518h, CRSA_13: A006 3558h, CRSA_14: A006 3598h, CRSA_15: A006 35D8h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRSA[31:0]	Current Source Address	Indicates the read address of the next DMA transfer.	R

The value after a reset is loaded from the following registers:

In register mode:
Loads the transfer source address from the Next0/1 register.

In link mode:
Loads the transfer source address from the descriptor read data (The hardware inputs descriptor read data to the N0SA_n register automatically, and loads it to the CRSA_n register when transfer starts).

The value is incremented when reading data from the transfer source is completed.

Read this register after DMA stops (when the TACT bit in the CHSTAT_n register = 0). (Handle the value during DMA operation as a reference value.)

15.2.5 Current Destination Address Register (CRDA_n)

The CRDA_n register indicates the DMA transfer destination address of DMA channel n (n = 15 to 0).
During DMA transfer, the value is incremented automatically (fixed when the DAD bit in the CHCFG_n register = 1).

Address(es): DMAC0
CRDA_0: A006 201Ch, CRDA_1: A006 205Ch, CRDA_2: A006 209Ch, CRDA_3: A006 20DCh,
CRDA_4: A006 211Ch, CRDA_5: A006 215Ch, CRDA_6: A006 219Ch, CRDA_7: A006 21DCh,
CRDA_8: A006 241Ch, CRDA_9: A006 245Ch, CRDA_10: A006 249Ch, CRDA_11: A006 24DCh,
CRDA_12: A006 251Ch, CRDA_13: A006 255Ch, CRDA_14: A006 259Ch, CRDA_15: A006 25DCh
DMAC1
CRDA_0: A006 301Ch, CRDA_1: A006 305Ch, CRDA_2: A006 309Ch, CRDA_3: A006 30DCh,
CRDA_4: A006 311Ch, CRDA_5: A006 315Ch, CRDA_6: A006 319Ch, CRDA_7: A006 31DCh,
CRDA_8: A006 341Ch, CRDA_9: A006 345Ch, CRDA_10: A006 349Ch, CRDA_11: A006 34DCh,
CRDA_12: A006 351Ch, CRDA_13: A006 355Ch, CRDA_14: A006 359Ch, CRDA_15: A006 35DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRDA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CRDA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRDA[31:0]	Current Destination Address	Indicates the write address of the next DMA transfer.	R

The value after a reset is loaded from the following registers:

In register mode:
Loads the transfer destination address from the Next0/1 register.

In link mode:
Loads the transfer destination address from the descriptor read data (The hardware inputs the descriptor read data to the N0DA_n register automatically, and loads it to the CRDA_n register when transfer starts).

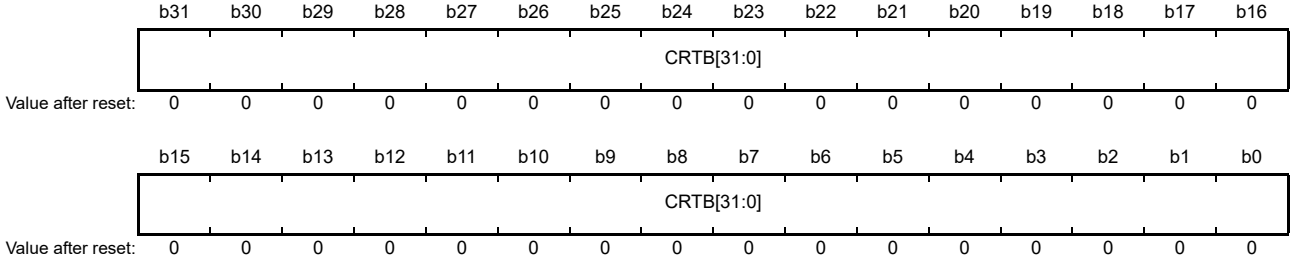
The value is incremented when writing data to the transfer destination completes.

Read this register after DMA stops (when the TACT bit in the CHSTAT_n register = 0). (Handle the value during DMA operation as a reference value.)

15.2.6 Current Transaction Byte Register (CRTB_n)

The CRTB_n register indicates the total number of transfer bytes of DMA channel n (n = 15 to 0). The value is cleared to 0 when transfer completes.
During DMA transfer, the value is decremented automatically.

Address(es): DMAC0
CRTB_0: A006 2020h, CRTB_1: A006 2060h, CRTB_2: A006 20A0h, CRTB_3: A006 20E0h,
CRTB_4: A006 2120h, CRTB_5: A006 2160h, CRTB_6: A006 21A0h, CRTB_7: A006 21E0h,
CRTB_8: A006 2420h, CRTB_9: A006 2460h, CRTB_10: A006 24A0h, CRTB_11: A006 24E0h,
CRTB_12: A006 2520h, CRTB_13: A006 2560h, CRTB_14: A006 25A0h, CRTB_15: A006 25E0h
DMAC1
CRTB_0: A006 3020h, CRTB_1: A006 3060h, CRTB_2: A006 30A0h, CRTB_3: A006 30E0h,
CRTB_4: A006 3120h, CRTB_5: A006 3160h, CRTB_6: A006 31A0h, CRTB_7: A006 31E0h,
CRTB_8: A006 3420h, CRTB_9: A006 3460h, CRTB_10: A006 34A0h, CRTB_11: A006 34E0h,
CRTB_12: A006 3520h, CRTB_13: A006 3560h, CRTB_14: A006 35A0h, CRTB_15: A006 35E0h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRTB[31:0]	Current Transaction Byte	Indicates the remaining number of transfer bytes that is currently performed.	R

The value after a reset is loaded from the following registers:

In register mode:
Loads the number of transfer bytes from the Next0/1 register.

In link mode:
Loads the number of transfer bytes from descriptor read data (The hardware inputs the descriptor read data to the N0TB_n register automatically, and loads it to the CRTB_n register when transfer starts).

The value is decremented when writing data to the transfer destination completes.

Read this register after DMA stops (when the TACT bit in the CHSTAT_n register = 0). (Handle the value during DMA operation as a reference value.)

15.2.7 Channel Status Register n (CHSTAT_n)

The CHSTAT_n register indicates the status of DMA channel n (n = 15 to 0).

Address(es): DMAC0
CHSTAT_0: A006 2024h, CHSTAT_1: A006 2064h, CHSTAT_2: A006 20A4h, CHSTAT_3: A006 20E4h,
CHSTAT_4: A006 2124h, CHSTAT_5: A006 2164h, CHSTAT_6: A006 21A4h, CHSTAT_7: A006 21E4h,
CHSTAT_8: A006 2424h, CHSTAT_9: A006 2464h, CHSTAT_10: A006 24A4h, CHSTAT_11: A006 24E4h,
CHSTAT_12: A006 2524h, CHSTAT_13: A006 2564h, CHSTAT_14: A006 25A4h, CHSTAT_15: A006 25E4h
DMAC1
CHSTAT_0: A006 3024h, CHSTAT_1: A006 3064h, CHSTAT_2: A006 30A4h, CHSTAT_3: A006 30E4h,
CHSTAT_4: A006 3124h, CHSTAT_5: A006 3164h, CHSTAT_6: A006 31A4h, CHSTAT_7: A006 31E4h,
CHSTAT_8: A006 3424h, CHSTAT_9: A006 3464h, CHSTAT_10: A006 34A4h, CHSTAT_11: A006 34E4h,
CHSTAT_12: A006 3524h, CHSTAT_13: A006 3564h, CHSTAT_14: A006 35A4h, CHSTAT_15: A006 35E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DNUM[7:0]								—	—	—	—	—	SWPRQ	DMARQM	INTM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MODE	DER	DW	DL	SR	—	END	ER	SUS	TACT	RQST	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EN	DMA Activation Enable	Indicates the status of operation enable/disable of DMA channel n. 0: Operation is disabled. 1: Operation is enabled. [Setting condition] • Writes 1 to the SETEN bit in the CHCTRL_n register. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLREN bit in the CHCTRL_n register. • When a bus error was reported during transfer • When all DMA transfers complete in register mode (transfers complete when the REN bit in the CHCFG_n register = 0) • In link mode, when DMA transfer (write back when WBD = 0) of the last descriptor (LE = 1) completes • When reading the descriptor in link mode stopped (when LV = 0, and DRRP in the CHCFG_n register = 0)	R

Bit	Symbol	Bit Name	Description	R/W
b1	RQST	DMA Transfer Request	This bit indicates that the transfer request is accepted. 0: The DMA transfer request is not accepted. 1: The DMA transfer request is accepted. [Setting condition] • The transfer request is accepted. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the SWRST bit in the CHCTRL_n register. • Writes 1 to the CLRRQ bit in the CHCTRL_n register. • In single transfer (the TM bit in the CHCFG_n register = 0) mode, the transfer specified in the REQD bit in the CHCFG_n register is performed • When all DMA transfers complete in register mode (transfer completes when the REN bit in the CHCFG_n register = 0) • In link mode, DMA transfer of the last descriptor (LE = 1) completes • In link mode, reading the descriptor is disabled (when LV = 0, and DRRP in the CHCFG_n register = 0) • In link mode, the DEM bit in the CHCFG_n register = 0, and DMA transfer completes. • When a buss error was reported to the master interface	R
b2	TACT	DMAC Operating Status	This bit indicates that DMAC is running. This bit is used to make sure the channel stops completely. For details, see section 15.3.9, DMA Transfer Status. 0: DMA in Channel_n stops. 1: DMA in Channel_n is running. [Setting condition] • Write 1 to the SETEN bit in the CHCTRL_n register (Reading the descriptor starts, or the DMA request is being waited). [Clearing condition] • When the internal state is idling (the EN bit in the CHSTAT_n register is cleared to 0, and all DMA transfer completes).	R
b3	SUS	Suspend	This bit indicates that the channel is suspended. For details, see section 15.3.10, Suspending a Transfer. 0: Channel_n is not suspended. 1: Channel_n is suspended. [Setting condition] • Writes 1 to the SETSUS bit in the CHCTRL_n register during DMA transfer of Channel_n, and the internal state is changed to the suspended state. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLRSUS bit in the CHCTRL_n register. • Writes 1 to the CLREN bit in the CHCTRL_n register. • Condition for clearing the EN bit in the CHSTAT_n register	R

Bit	Symbol	Bit Name	Description	R/W
b4	ER	DMA Error	This bit indicates that a DMA error interrupt is generated as a result of the bus error during DMA transfer. 0: No bus error occurred. 1: A bus error occurred. [Setting condition] • A buss error is reported to the bus cycle [Clearing condition] • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b5	END	DMA Transfer Completion Interrupt	This bit indicates that DMA transfer completes, and a DMA interrupt is generated. 0: DMA transfer is not completed. 1: DMA transfer is completed. [Setting conditions] When any of the following conditions is met: • The following conditions being met while the DEM bit in the CHCFG_n register = 0 (1) When a transfer for the total number of transfer bytes loaded to the CRTB register completes in register mode (2) When a transfer for the total number of transfer bytes loaded to the CRTB register completes in link mode while the WBD bit in the header of the descriptor is 1 (3) Completion of descriptor write-back in link mode while the WBD bit in the header of the descriptor is 0 • In link mode, the descriptor is read, LV of header = 0, and DRRP in the CHCFG_n register = 0, and DIM = 0. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLREND bit in the CHCTRL_n register. • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b6	—	Reserved	This bit is always read as 0.	R
b7	SR	Next Register Select	In register mode, indicates the selected register set. 0: Next0 Register Set 1: Next1 Register Set [Setting condition] • Set 1 to the RSEL bit in the CHCFG_n register. [Clearing condition] • Clears the RSEL bit in the CHCFG_n register to 0.	R

Bit	Symbol	Bit Name	Description	R/W
b8	DL	Descriptor Load	Indicates that the descriptor is being read. In addition, if a bus error is reported while the descriptor is being read, 1 is retained. 0: The descriptor is not being read. 1: (When ER = 0) The descriptor is being read in link mode. (When ER = 1) A buss error occurred while the descriptor is being read in link mode. [Setting condition] • Reading the descriptor in link mode is started [Clearing conditions] When any of the following conditions is met: • Reading the descriptor in link mode completes with the OK response. • Writes 1 to the SWRST bit in the CHCTRL_n register. (If 1 is retained for the bus error, it can be cleared to 0 only by the SWRST bit.)	R
b9	DW	Descriptor Write Back	Indicates that the descriptor is being written back. In addition, if a bus error is reported while the descriptor is written back, 1 is retained. 0: Header is not written back in link mode. 1: (The ER bit in the CHSTAT_n register = 0) Header is written back in link mode. (The ER bit in the CHSTAT_n register = 1) A buss error occurred when header is written back in link mode. [Setting condition] • Writing back of header in link mode started. [Clearing conditions] • Writing back of header in link mode completes with the OK response. • Writes 1 to the SWRST bit in the CHCTRL_n register (If 1 is retained due to the buss error, it can be cleared to 0 only by the SWRST bit).	R
b10	DER	Descriptor Error	Indicates that the read descriptor is invalid (LV = 0). (Does not depend on the value of the DIM bit in the CHCFG_n register.) 0: No descriptor error occurred. 1: Descriptor error occurred. [Setting condition] • In link mode, the DRRP bit in the CHCFG_n register = 0, and the read descriptor's LV is 0. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLRDE bit in the CHCTRL_n register. • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b11	MODE	DMA Mode	This bit indicates DMA mode. Indicates the setting value of the DMS bit in the CHCFG_n register. 0: Register mode 1: Link mode	R
b15 to b12	—	Reserved	These bits are always read as 0.	R

Bit	Symbol	Bit Name	Description	R/W
b16	INTM	Interrupt Request Mask	Indicates the temporary mask status of DMA interrupt output. 1: Temporary mask status 0: The temporary mask status is cleared. [Setting condition] • Writes 1 to the SETINTM bit in the CHCTRL_n register. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLRINTM bit in the CHCTRL_n register. • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b17	DMARQM	DMA Activation Request Mask	Indicates the temporary mask status of the DMA request. 1: Temporary mask status 0: Temporary mask status is cleared. [Setting condition] • Sets 1 to the SETDMARQM bit in the CHCTRL_n register. [Clearing conditions] When any of the following conditions is met: • Writes 1 to the CLRDMARQM bit in the CHCTRL_n register. • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b18	SWPRQ	Forced Ejection Request	Indicates the forced ejection request status. Indicates the software forced ejection request (a request activated by the SETSSWPRQ bit in the CHCTRL_n register). 1: Forced ejection is requested. 0: Forced ejection is not requested. [Setting condition] • Sets 1 to the SETSSWPRQ bit in the CHCTRL_n register. [Clearing conditions] When any of the following conditions is met: • The amount of data in the buffer becomes 0 because of forced ejection. • Writes 1 to the SWRST bit in the CHCTRL_n register.	R
b23 to b19	—	Reserved	These bits are always read as 0.	R
b31 to b24	DNUM	Amount of Data in the Buffer	These bits indicate the amount of valid data in the buffer. Read data from the DMA transfer source, and indicate the amount of data that is not written to the transfer destination (in bytes). [Increment condition] • When DMA read transfer completes [Decrement condition] • When DMA write transfer completes [Clearing conditions] When any of the following conditions is met: • Condition for clearing the EN bit • Writes 1 to the SWRST bit in the CHCTRL_n register.	R

Note 1. Handle the transfer when the ER bit in the CHSTAT_n register is set to 1 as invalid.
Note 2. To suspend DMA transfer, mask or clear the transfer request, or clear the EN bit in the CHSTAT_n register. See section 15.3.11, Aborting a Transfer for the procedure).
Note 3. To request a transfer by software, make sure that the previously requested DMA transfer operation completes (by checking Current Register), set the DMREQ bit in the DMAC software activation register (DMASTG), and then activate DMA.

15.2.8 DMAC Unit 0 Source Select Register i (DMA0SELi) (i = 0 to 15)

The DMA0SELi register selects the activation trigger source of channel i (i = 0 to 15) for DMAC unit 0. For details on numbers that are selected by this source selection, see the vector numbers listed in Table 12.3, Cortex-R4/DMAC Interrupt Vector Table. In addition, do not set the same source for multiple DMA0SELi and DMA1SELi registers. If the same source is set, the operation of this LSI cannot be guaranteed.

Address(es): DMA0.DMA0SEL0 A009 4000h, DMA0.DMA0SEL1 A009 4004h, DMA0.DMA0SEL2 A009 4008h, DMA0.DMA0SEL3 A009 400Ch, DMA0.DMA0SEL4 A009 4010h, DMA0.DMA0SEL5 A009 4014h, DMA0.DMA0SEL6 A009 4018h, DMA0.DMA0SEL7 A009 401Ch, DMA0.DMA0SEL8 A009 4020h, DMA0.DMA0SEL9 A009 4024h, DMA0.DMA0SEL10 A009 4028h, DMA0.DMA0SEL11 A009 402Ch, DMA0.DMA0SEL12 A009 4030h, DMA0.DMA0SEL13 A009 4034h, DMA0.DMA0SEL14 A009 4038h, DMA0.DMA0SEL15 A009 403Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IFC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	IFC0[7:0]	DMA channel source select	Select the trigger source of the DMA channel.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

15.2.9 DMAC Unit 1 Source Select Register i (DMA1SELi) (i = 0 to 15)

The DMA1SELi register selects the activation trigger source of channel i (i = 0 to 15) for DMAC unit 1. For details on numbers that are selected for this source selection, see the vector numbers listed in Table 12.3, Cortex-R4/DMAC Interrupt Vector Table. In addition, do not set the same source for multiple DMA0SELi and DMA1SELi registers. If the same source is set, the operation cannot be guaranteed.

Address(es): DMA1.DMA1SEL0 A009 4040h, DMA1.DMA1SEL1 A009 4044h, DMA1.DMA1SEL2 A009 4048h, DMA1.DMA1SEL3 A009 404Ch, DMA1.DMA1SEL4 A009 4050h, DMA1.DMA1SEL5 A009 4054h, DMA1.DMA1SEL6 A009 4058h, DMA1.DMA1SEL7 A009 405Ch, DMA1.DMA1SEL8 A009 4060h, DMA1.DMA1SEL9 A009 4064h, DMA1.DMA1SEL10 A009 4068h, DMA1.DMA1SEL11 A009 406Ch, DMA1.DMA1SEL12 A009 4070h, DMA1.DMA1SEL13 A009 4074h, DMA1.DMA1SEL14 A009 4078h, DMA1.DMA1SEL15 A009 407Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	IFC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	IFC1[7:0]	DMA channel source select	Select the trigger source of the DMA channel.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

15.2.10 DMAC Software Activation Register (DMASTG)

The DMASTG register controls activation of DMAC by software.

Address(es): DMAC.DMASTG A009 4080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMREQ1	DMREQ0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DMREQ0	DMA Unit 0 Software Activation	0: DMA transfer is not requested. 1: DMA transfer is requested.	W
b1	DMREQ1	DMA Unit 1 Software Activation	0: DMA transfer is not requested. 1: DMA transfer is requested.	W
b31 to b2	—	Reserved	The write value should be 0.	W

DMREQ0, DMREQ1 Bits (DMA Unit 0/1 Software Activation)

DMA transfer is requested if you select DMA activation by software for the DMA0SELi register and the DMA1SELi register (i = 0 to 15), and then write 1 to DMREQ0 and DMREQ1 bits.

These bits are write only. These bits are read as 0.

15.2.11 Common Control Register (CMNCR)

CMNCR is a 32-bit register that controls the common items for each area.

Address(es): A000 2000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TL2	TL1	TL0	—	AL2	AL1	AL0	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DPRTY[1:0]		—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b4, b3	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b8 to b5	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b10, b9	DPRTY[1:0]	DMA Burst Transfer Priority	Specify the priority for a refresh request during DMA burst transfer. 0x: Accepts a refresh request during DMA burst transfer. 10: Does not accept a refresh request during DMA burst transfer. 11: Reserved (setting prohibited)	R/W
b11	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b12	—	Reserved	This bit is always read as 1. The write value should always be 1.	R/W
b23 to b13	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b24	AL0	Acknowledge Level	Specifies the active level of the DACK0 signal. 0: Active-low output from DACK0 1: Active-high output from DACK0	R/W
b25	AL1	Acknowledge Level	Specifies the active level of the DACK1 signal. 0: Active-low output from DACK1 1: Active-high output from DACK1	R/W
b26	AL2	Acknowledge Level	Specifies the active level of the DACK2 signal. 0: Active-low output from DACK2 1: Active-high output from DACK2	R/W
b27	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b28	TL0	Transfer End Level	Specifies the active level of the TEND0 signal. 0: Active-low output from TEND0 1: Active-high output from TEND0	R/W
b29	TL1	Transfer End Level	Specifies the active level of the TEND1 signal. 0: Active-low output from TEND1 1: Active-high output from TEND1	R/W
b30	TL2	Transfer End Level	Specifies the active level of the TEND2 signal. 0: Active-low output from TEND2 1: Active-high output from TEND2	R/W
b31	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W

15.2.12 Channel Control Register n (CHCTRL_n)

The CHCTRL_n register controls DMA transfer of DMA channel n (n = 15 to 0).
This register is used to activate each function, and it does not retain the written value. These bits are always read as 0.
Only resources for channel n are masked temporary for forced ejection request and DMA transfer request inputs by the CLRDMARQM and SETDMARQM bits.

Address(es): DMAC0
CHCTRL_0: A006 2028h, CHCTRL_1: A006 2068h, CHCTRL_2: A006 20A8h, CHCTRL_3: A006 20E8h,
CHCTRL_4: A006 2128h, CHCTRL_5: A006 2168h, CHCTRL_6: A006 21A8h, CHCTRL_7: A006 21E8h,
CHCTRL_8: A006 2428h, CHCTRL_9: A006 2468h, CHCTRL_10: A006 24A8h, CHCTRL_11: A006 24E8h,
CHCTRL_12: A006 2528h, CHCTRL_13: A006 2568h, CHCTRL_14: A006 25A8h, CHCTRL_15: A006 25E8h
DMAC1
CHCTRL_0: A006 3028h, CHCTRL_1: A006 3068h, CHCTRL_2: A006 30A8h. CHCTRL_3: A006 30E8h,
CHCTRL_4: A006 3128h, CHCTRL_5: A006 3168h, CHCTRL_6: A006 31A8h, CHCTRL_7: A006 31E8h,
CHCTRL_8: A006 3428h, CHCTRL_9: A006 3468h, CHCTRL_10: A006 34A8h, CHCTRL_11: A006 34E8h,
CHCTRL_12: A006 3528h, CHCTRL_13: A006 3568h, CHCTRL_14: A006 35A8h, CHCTRL_15: A006 35E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	CLRDMARQM	SETDMARQM	CLRINTM	SETINTM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SETSSWPRQ	—	SETREN	—	—	CLRSUS	SETSUS	CLRDE	—	CLRENDD	CLRRQ	SWRST	—	CLREN	SETEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SETEN	DMA Activation Enable	Enables DMA transfer of DMA channel n. When this bit is set with the SWRST bit, clearing by the SWRST bit takes precedence, and a transfer does not start. This bit is always read as 0. 1: DMA transfer is enabled (The EN bit in the CHSTAT_n register is set). 0: Operation is not affected. Note: For resetting the DMA register, stop the ongoing DMA transfer by setting the CLREN bit and then set the SETEN bit.	R/W
b1	CLREN	DMA Activation Enable Clear	Clears the EN bit in the CHSTAT_n register (For details, see section 15.3.11, Aborting a Transfer). This bit is always read as 0. 1: DMA transfer is disabled (The EN bit in the CHSTAT_n register is cleared). 0: Operation is not affected.	R/W
b2	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W
b3	SWRST	Software Reset	Clears each bit in the CHSTAT_n register (For details on the bit to be cleared, see descriptions of the applicable bit). Set this bit to 0 when the EN bit and the TACT bit are cleared to 0. This bit is always read as 0. 1: Clears each bit in the CHSTAT_n register. 0: Operation is not affected.	R/W
b4	CLRRQ	DMA Transfer Request Clear	Clears the RQST bit in the CHSTAT_n register to 0. This bit is always read as 0. 1: Clears the RQST bit in the CHSTAT_n register. 0: Operation is not affected.	R/W
b5	CLREND	END Clear	Clears the END bit in the CHSTAT_n register to 0. This bit is always read as 0. 1: Clears the END bit. 0: Operation is not affected.	R/W
b6	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b7	CLRDE	DER Clear	Clears the descriptor error bit (DER) in the CHSTAT_n register to 0. This bit is always read as 0. 1: Clears the DER bit. 0: Operation is not affected.	R/W
b8	SETSUS	Suspend Request	If 1 is set to this bit when the EN bit in the CHSTAT_n register is 1, the current DMA transfer is suspended. This bit is always read as 0. 1: Suspends the current DMA transfer. 0: Operation is not affected.	R/W
b9	CLRSUS	Suspend Clear	If 1 is set to this bit when the SUS bit in the CHSTAT_n register is 1, the temporary suspend status is cleared. This bit is always read as 0. 1: Clears the temporary suspend status of the current DMA transfer. 0: Operation is not affected.	R/W
b11, b10	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b12	SETREN	REN Set Enable	Sets the register set enable bit (REN) in the CHCFG_n register. This bit is always read as 0. 1: Sets the REN bit in the CHCFG_n register. 0: Operation is not affected.	R/W
b13	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W
b14	SETSSWPRQ	Software Forced Ejection Request	Forcibly ejects data in the buffer to the transfer destination (See section 15.3.6, Forced Ejection Request). This bit is always read as 0. 1: Writes data in the buffer, which is not written, to the transfer destination. 0: Operation is not affected. Requests a hardware request on the destination side (when the RFQD bit in the CHCFGn register (n = 0 to 15) = 1), forced ejection cannot be used (disabled by the hardware).	R/W
b15	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W
b16	SETINTM	Interrupt Request Mask	Masks DMA transfer completion interrupt output temporary. Besides, the INTM bit in the CHSTATn register is set to 1. This bit is always read as 0. 1: Masks a DMA transfer completion interrupt temporary. 0: Operation is not affected.	R/W
b17	CLRINTM	Interrupt Request Mask Clear	Clears the mask status of DMA transfer completion interrupt output. Besides, the INTM bit in the CHSTATn register is cleared to 0. If the mask state is cleared when the LVINT bit in the DCTRL register = 1, and the END bit in the CHSTAT_n register = 1, DMA transfer completion interrupt is deactivated. (It is not activated when LVINT = 0.) This bit is always read as 0. 1: Clears the mask state set by the SETINTM bit. 0: Operation is not affected.	R/W
b18	SETDMARQM	DMA Activation Request Mask	Masks DMA transfer request input temporary. Besides, the DMARQM bit in the CHSTATn register is set to 1. This bit is always read as 0. 1: Masks DMA transfer request input. 0: Operation is not affected.	R/W
b19	CLRDMARQM	DMA Activation Request Mask Clear	Clears the mask state of DMA transfer request input. Besides, the DMARQM bit in the CHSTATn register is cleared to 0. This bit is always read as 0. 1: Clears the mask state set by the SETDMARQM bit. 0: Operation is not affected.	R/W
b31 to b20	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W

15.2.13 Channel Configuration Register n (CHCFG_n)

The CHCFG_n register controls DMA transfer of DMA channel n (n = 15 to 0).

Specify the detection method depending on the DMA transfer source to be used. For details on the DMA request signals, see section 15.3.4.1, Specifying Detection Operation of DMA Transfer Requests for Each Source.

Address(es): DMAC0
CHCFG_0: A006 202Ch, CHCFG_1: A006 206Ch, CHCFG_2: A006 20ACh, CHCFG_3: A006 20ECh,
CHCFG_4: A006 212Ch, CHCFG_5: A006 216Ch, CHCFG_6: A006 21ACh, CHCFG_7: A006 21ECh,
CHCFG_8: A006 242Ch, CHCFG_9: A006 246Ch, CHCFG_10: A006 24ACh, CHCFG_11: A006 24ECh,
CHCFG_12: A006 252Ch, CHCFG_13: A006 256Ch, CHCFG_14: A006 25ACh, CHCFG_15: A006 25ECh
DMAC1
CHCFG_0: A006 302Ch, CHCFG_1: A006 306Ch, CHCFG_2: A006 30ACh, CHCFG_3: A006 30ECh,
CHCFG_4: A006 312Ch, CHCFG_5: A006 316Ch, CHCFG_6: A006 31ACh, CHCFG_7: A006 31ECh,
CHCFG_C: A006 342Ch, CHCFG_9: A006 346Ch, CHCFG_10: A006 34ACh, CHCFG_11: A006 34ECh,
CHCFG_12: A006 352Ch, CHCFG_13: A006 356Ch, CHCFG_14: A006 35ACh, CHCFG_15: A006 35ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DMS	REN	RSW	RSEL	SBE	DIM	—	DEM	WONLY	TM	DAD	SAD	DDS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SDS[3:0]				DRRP	AM[2:0]			—	LVL	HIEN	LOEN	REQD	SEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SEL[2:0]	Pin Select	Sets channels of DMAC. Set the following values so that the channels of CHCFG_n (n = 0 to 15) and the channel set by SEL become the same: For example, set 001b to the SEL bit in CHCFG_1. Similarly, set 001b to the SEL bit in CHCFG_1. DMAC0/1 b2 b0 000: Channel 0/8 001: Channel 1/9 010: Channel 2/10 011: Channel 3/11 100: Channel 4/12 101: Channel 5/13 110: Channel 6/14 111: Channel 7/15	R/W
b3	REQD	DMA Activation Request Source Select	Specifies the DMA transfer request input source (internal modules or external devices that require DACK). The timing when DACK/TEND become active is determined by the setting of this bit. 0: Requested by a transfer source module. DACK/TEND output is activated when it is read (a value after a reset). 1: Requested by a transfer destination module. DACK/TEND output is activated when it is written.	R/W
b4	LOEN	L Detection Enable	Specifies the detection method of the DMA request signal. When LVL = 0 LOEN = 1: If DMA transfer request input detects a falling edge, it is regarded as requested. LOEN = 0: If the DMA transfer request input falls, the request is not recognized (a value after a reset). When LVL = 1 LOEN = 1: If DMA transfer request input detects the Low level, it is regarded as requested. LOEN = 0: If the DMA transfer request input is the Low level, the request is not recognized (a value after a reset).	R/W

Bit	Symbol	Bit Name	Description	R/W
b5	HIEN	H Detection Enable	Specifies the detection method of the DMA request signal. When LVL = 0 HIEN = 1: If DMA transfer request input detects a rising edge, it is regarded as requested. HIEN = 0: If the DMA transfer request input rises, the request is not recognized (a value after a reset). When LVL = 1 HIEN = 1: If DMA transfer request input detects the High level, it is regarded as requested. HIEN = 0: If the DMA transfer request input is the High level, the request is not recognized (a value after a reset).	R/W
b6	LVL	Level Detection Enable	Specifies the detection method of the DMA request signal. 0: Detects the edge (a value after a reset). 1: Detects the level.	R/W
b7	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W
b10 to b8	AM[2:0]	ACK Mode	Sets DACK/TEND output mode. b10 b8 000: Setting is prohibited (a value after a reset). At the initial setup, set a value other than 000b. 001: Level mode (Active until DMA transfer request input becomes inactive). 01x: Bus cycle mode (Active between DMA transfer cycles (Active if internal resources are the target)). 1xx: Masks DACK/TEND output. Note: For the conditions for outputting the DACK and TEND signals, see section 15.3.5, DMA Acknowledge Output/ DMA Transaction Completion Output Function.	R/W
b11	DRRP	Descriptor Reload Enable	Specifies the operation when LV of header = 0 while during descriptor read (see section 15.3.1.2, Link Mode (1) Operation flows in link mode). 0: Sets the DER bit in the CHSTAT_n register, and stops the operation (a value after a reset). 1: Continues reading the same descriptor until LV becomes 1. When LV becomes 1, DMA transfer using the descriptor value starts. The DSCITVL register controls the descriptor read interval.	R/W
b15 to b12	SDS[3:0]	Source Data Size	Sets the size of data in the transfer source to be transferred at a time. For a single transfer, the specified amount of data is transferred by a single request. For a block transfer, data is transferred as many times as the setting value × N times until the CRTB register is cleared to 0. For a transfer of 32 bits or more, 32 bits × N times burst transfers are performed. The SDS[3] bit switches between normal mode and skip mode. 0: Normal mode (a value after a reset). 1: Skip mode The SDS[2:0] bits set the transfer size. b14 b12 000: 8 bits (a value after a reset) 001: 16 bits 010: 32 bits 011: Setting is prohibited. 100: 128 bits*2 101: 256 bits (Can be set only for DMAC0) 110: 512 bits (Can be set only for DMAC0)*1 111: Setting is prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b19 to b16	DDS[3:0]	Destination Data Size	Sets the size of data in the transfer destination to be transferred at a time. The DDS[3] bit switches between normal mode and skip mode. 0: Normal mode (a value after a reset). 1: Skip mode The DDS[2:0] bits set the transfer size. b18 b16 000: 8 bits (a value after a reset) 001: 16 bits 010: 32 bits 011: Setting is prohibited. 100: 128 bits*2 101: 256 bits (Can be set only for DMAC0) 110: 512 bits (Can be set only for DMAC0)*1 111: Setting is prohibited.	R/W
b20	SAD	Source Address Count Direction	Sets the count direction of the transfer source address of DMA channel n. 0: Increment (a value after a reset) 1: Fixed To use SKIP mode on the transfer source, do not specify SAD = 1 (fixed). If SAD = 1 (fixed) is specified, the address of the transfer source should be aligned with a boundary of the size specified by the SDS[3:0] bits.	R/W
b21	DAD	Destination Address Count Direction	Sets the count direction of the transfer destination address of DMA channel n. 0: Increment (a value after a reset) 1: Fixed To use SKIP mode on the transfer destination, do not specify DAD = 1 (fixed). If DAD = 1 (fixed) is specified, the address of the transfer destination should be aligned with a boundary of the size specified by the DDS[3:0] bits.	R/W
b22	TM	Transfer Mode	Sets DMA transfer mode. 0: Single transfer mode (a value after a reset) 1: Block transfer mode	R/W
b23	WONLY	Write-Only Mode	Sets the write-only mode (see section 15.3.1.3, Write-Only Mode). 0: Normal mode (a value after a reset). 1: Write-only mode	R/W
b24	DEM	Transfer Completion Interrupt Mask	Masks DMA transfer completion interrupt detection. If this bit is set to 1 when DMA transfer completion interrupt is output, DMA transfer completion interrupt is not activated. Besides, the END bit in the CHSTAT_n register is not set. In register mode, the DEM bit is automatically cleared to 0. In link mode, it is not cleared. 0: Does not mask (a value after a reset). 1: Masks. [Clearing condition] DEM = 1, and DMA transfer completes.	R/W
b25	—	Reserved	This bit is always read as 0. The write value should be 0.	R/W
b26	DIM	Descriptor Interrupt Mask	Sets the DMA transfer completion interrupt mask if LV = 0 when header of the descriptor is read. 0: Does not mask a DMA transfer completion interrupt (a value after reset). 1: Masks a DMA transfer completion interrupt.	R/W

Bit	Symbol	Bit Name	Description	R/W
b27	SBE	Buffer Flush Enable	If the EN bit in the CHSTAT_n register is cleared to 0 during DMA transfer, selects whether to stop flushing (writing) data that is already read and stored in the buffer. Only when REQD = 0, flush mode can be used. 0: Stops transfer without flushing data in the buffer (a value after a reset). 1: Stops transfer after flushing data in the buffer.	R/W
b28	RSEL	Next Register Select	Selects the Next register set to be executed next. This bit is valid in register mode only. When RSW = 1, the value is reversed automatically (0 is reversed to 1, 1 is reversed to 0) after DMA transfer completes. 0: Executes Next0 Register Set (a value after a reset). 1: Executes Next1 Register Set. [Transition condition] RSW = 1, and DMA transfer completes.	R/W
b29	RSW	RSEL Reverse	When DMA transfer completes, the RSEL bit is automatically reversed (0 is reversed to 1, 1 is reversed to 0). This bit is valid in register mode only. 0: Does not reverse the RSEL bit when DMA transfer completes (a value after a reset). 1: Reverses the RSEL bit when DMA transfer completes.	R/W
b30	REN	Register Set Enable	When DMA transfer completes, performs DMA transfer of the Next register set selected by the RSEL bit accordingly. This bit is valid in register mode only. 0: Does not perform DMA transfer accordingly. 1: Performs DMA transfer accordingly. [Setting conditions] When any of the following conditions is met: • Writes 1 to this bit. • Writes 1 to the SETREN bit in the CHCTRL_n register. [Clearing conditions] • Writes 0 to this bit. • REN = 1, and DMA transfer completes. To reset the REN bit during DMA transfer, use the SETREN bit in the CHCTRL_n register. Also, reset the CHCFG_n.DEM bit to mask detection of DMA transfer completion interrupt.	R/W
b31	DMS	DMA Mode Select	Sets DMA mode. 0: Register mode (a value after a reset). 1: Link mode	R/W

Note 1. If the size is set to 512 bits, the address of the transfer source/destination should be aligned with 512-bit boundaries.
Note 2. If the size is set to 128 bits when DMAC1 is used, the address of the transfer source/destination should be aligned with 128-bit boundaries.

15.2.14 Channel Interval Register n (CHITVL_n)

The CHITVL_n register sets the DMA transfer interval of DMA channel n (n = 15 to 0).
For details, see section 15.3.7, Interval Count Function.

Address(es): DMAC0
CHITVL_0: A006 2030h, CHITVL_1: A006 2070h, CHITVL_2: A006 20B0h, CHITVL_3: A006 20F0h,
CHITVL_4: A006 2130h, CHITVL_5: A006 2170h, CHITVL_6: A006 21B0h, CHITVL_7: A006 21F0h,
CHITVL_8: A006 2430h, CHITVL_9: A006 2470h, CHITVL_10: A006 24B0h, CHITVL_11: A006 24F0h,
CHITVL_12: A006 2530h, CHITVL_13: A006 2570h, CHITVL_14: A006 25B0h, CHITVL_15: A006 25F0h
DMAC1
CHITVL_0: A006 3030h, CHITVL_1: A006 3070h, CHITVL_2: A006 30B0h, CHITVL_3: A006 30F0h,
CHITVL_4: A006 3130h, CHITVL_5: A006 3170h, CHITVL_6: A006 31B0h, CHITVL_7: A006 31F0h,
CHITVL_8: A006 3430h, CHITVL_9: A006 3470h, CHITVL_10: A006 34B0h, CHITVL_11: A006 34F0h,
CHITVL_12: A006 3530h, CHITVL_13: A006 3570h, CHITVL_14: A006 35B0h, CHITVL_15: A006 35F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ITVL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ITVL	Interval	These bits set the DMA transfer internal.	R/W
b31 to b16	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W

15.2.15 Next Link Address Register n (NXLA_n)

The NXLA_n register sets the link address of DMA channel n (n = 15 to 0).

Address(es): DMAC0
NXLA_0: A006 2038h, NXLA_1: A006 2078h, NXLA_2: A006 20B8h, NXLA_3: A006 20F8h,
NXLA_4: A006 2138h, NXLA_5: A006 2178h, NXLA_6: A006 21B8h, NXLA_7: A006 21F8h,
NXLA_8: A006 2438h, NXLA_9: A006 2478h, NXLA_10: A006 24B8h, NXLA_11: A006 24F8h,
NXLA_12: A006 2538h, NXLA_13: A006 2578h, NXLA_14: A006 25B8h, NXLA_15: A006 25F8h
DMAC1
NXLA_0: A006 3038h, NXLA_1: A006 3078h, NXLA_2: A006 30B8h, NXLA_3: A006 30F8h,
NXLA_4: A006 3138h, NXLA_5: A006 3178h, NXLA_6: A006 31B8h, NXLA_7: A006 31F8h,
NXLA_8: A006 3438h, NXLA_9: A006 3478h, NXLA_10: A006 34B8h, NXLA_11: A006 34F8h,
NXLA_12: A006 3538h, NXLA_13: A006 3578h, NXLA_14: A006 35B8h, NXLA_15: A006 35F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NXLA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NXLA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NXLA[31:0]	Next Link Address	Sets the address of the link destination. Because the two lower-order bits are fixed to 0, only word-aligned addresses can be set.	R/W
b31 to b2				R/W

15.2.16 Current Link Address Register n (CRLA_n)

The CRLA_n register sets the link address of DMA channel n (n = 15 to 0).

Address(es): DMAC0
CRLA_0: A006 203Ch, CRLA_1: A006 207Ch, CRLA_2: A006 20BCh, CRLA_3: A006 20FCh,
CRLA_4: A006 213Ch, CRLA_5: A006 217Ch, CRLA_6: A006 21BCh, CRLA_7: A006 21FCh,
CRLA_8: A006 243Ch, CRLA_9: A006 247Ch, CRLA_10: A006 24BCh, CRLA_11: A006 24FCh,
CRLA_12: A006 253Ch, CRLA_13: A006 257Ch, CRLA_14: A006 25BCh, CRLA_15: A006 25FCh
DMAC1
CRLA_0: A006 303Ch, CRLA_1: A006 307Ch, CRLA_2: A006 30BCh, CRLA_3: A006 30FCh,
CRLA_4: A006 313Ch, CRLA_5: A006 317Ch, CRLA_6: A006 31BCh, CRLA_7: A006 31FCh,
CRLA_8: A006 343Ch, CRLA_9: A006 347Ch, CRLA_10: A006 34BCh, CRLA_11: A006 34FCh,
CRLA_12: A006 353Ch, CRLA_13: A006 357Ch, CRLA_14: A006 35BCh, CRLA_15: A006 35FCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRLA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CRLA[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRLA[31:0]	Current Link Address	Indicates the address of the descriptor which is being executed.	R

15.2.17 Source Continuous Register n (SCNT_n)

The SCNT_n register sets the space size for continuous access during read access to the DMA transfer source (n = 15 to 0).

Use this register together with the SSKP_n register (see Figure 15.1).

When setting this register, set the SDS[3] bit in the CHCFG_n register to 1.

Address(es): DMAC0
SCNT_0: A006 2200h, SCNT_1: A006 2220h, SCNT_2: A006 2240h, SCNT_3: A006 2260h,
SCNT_4: A006 2280h, SCNT_5: A006 22A0h, SCNT_6: A006 22C0h, SCNT_7: A006 22E0h,
SCNT_8: A006 2600h, SCNT_9: A006 2620h, SCNT_10: A006 2640h, SCNT_11: A006 2660h,
SCNT_12: A006 2680h, SCNT_13: A006 26A0h, SCNT_14: A006 26C0h, SCNT_15: A006 26E0h
DMAC1
SCNT_0: A006 3200h, SCNT_1: A006 3220h, SCNT_2: A006 3240h, SCNT_3: A006 3260h,
SCNT_4: A006 3280h, SCNT_5: A006 32A0h, SCNT_6: A006 32C0h, SCNT_7: A006 32E0h,
SCNT_8: A006 3600h, SCNT_9: A006 3620h, SCNT_10: A006 3640h, SCNT_11: A006 3660h,
SCNT_12: A006 3680h, SCNT_13: A006 36A0h, SCNT_14: A006 36C0h, SCNT_15: A006 36E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SCNT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCNT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SCNT[31:0]	Source Continuous Access Size	Sets the size of the continuous access space during read access to the DMA transfer source in bytes.	R/W

When performing a skip transfer on the transfer source, do not set the SAD bit in the CHCFG_n register to 1 (fixed). In addition, do not perform a skip transfer when this register is set to 0000 0000h.

15.2.18 Source Skip Register n (SSKP_n)

The SSKP_n register sets the skip amount during read access to the DMA transfer source.
During read access to the DMA transfer source, after data of the size set by using the SCNT_n register is accessed, the next DMA transfer source address of the size set by using this register is skipped (n = 15 to 0).
Use this register together with the SCNT_n register (see Figure 15.1).
When setting this register, set the SDS[3] bit in the CHCFG_n register to 1.

Address(es): DMAC0
SSKP_0: A006 2204h, SSKP_1: A006 2224h, SSKP_2: A006 2244h, SSKP_3: A006 2264h,
SSKP_4: A006 2284h, SSKP_5: A006 22A4h, SSKP_6: A006 22C4h, SSKP_7: A006 22E4h,
SSKP_8: A006 2604h, SSKP_9: A006 2624h, SSKP_10: A006 2644h, SSKP_11: A006 2664h,
SSKP_12: A006 2684h, SSKP_13: A006 26A4h, SSKP_14: A006 26C4h, SSKP_15: A006 26E4h
DMAC1
SSKP_0: A006 3204h, SSKP_1: A006 3224h, SSKP_2: A006 3244h, SSKP_3: A006 3264h,
SSKP_4: A006 3284h, SSKP_5: A006 32A4h, SSKP_6: A006 32C4h, SSKP_7: A006 32E4h,
SSKP_8: A006 3604h, SSKP_9: A006 3624h, SSKP_10: A006 3644h, SSKP_11: A006 3664h,
SSKP_12: A006 3684h, SSKP_13: A006 36A4h, SSKP_14: A006 36C4h, SSKP_15: A006 36E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SSKP[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSKP[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SSKP[31:0]	Source Skip Size	Sets the skip amount during read access to the DMA transfer source in bytes.	R/W

When performing a skip transfer on the transfer source, do not set the SAD bit in the CHCFG_n register to 1 (fixed).

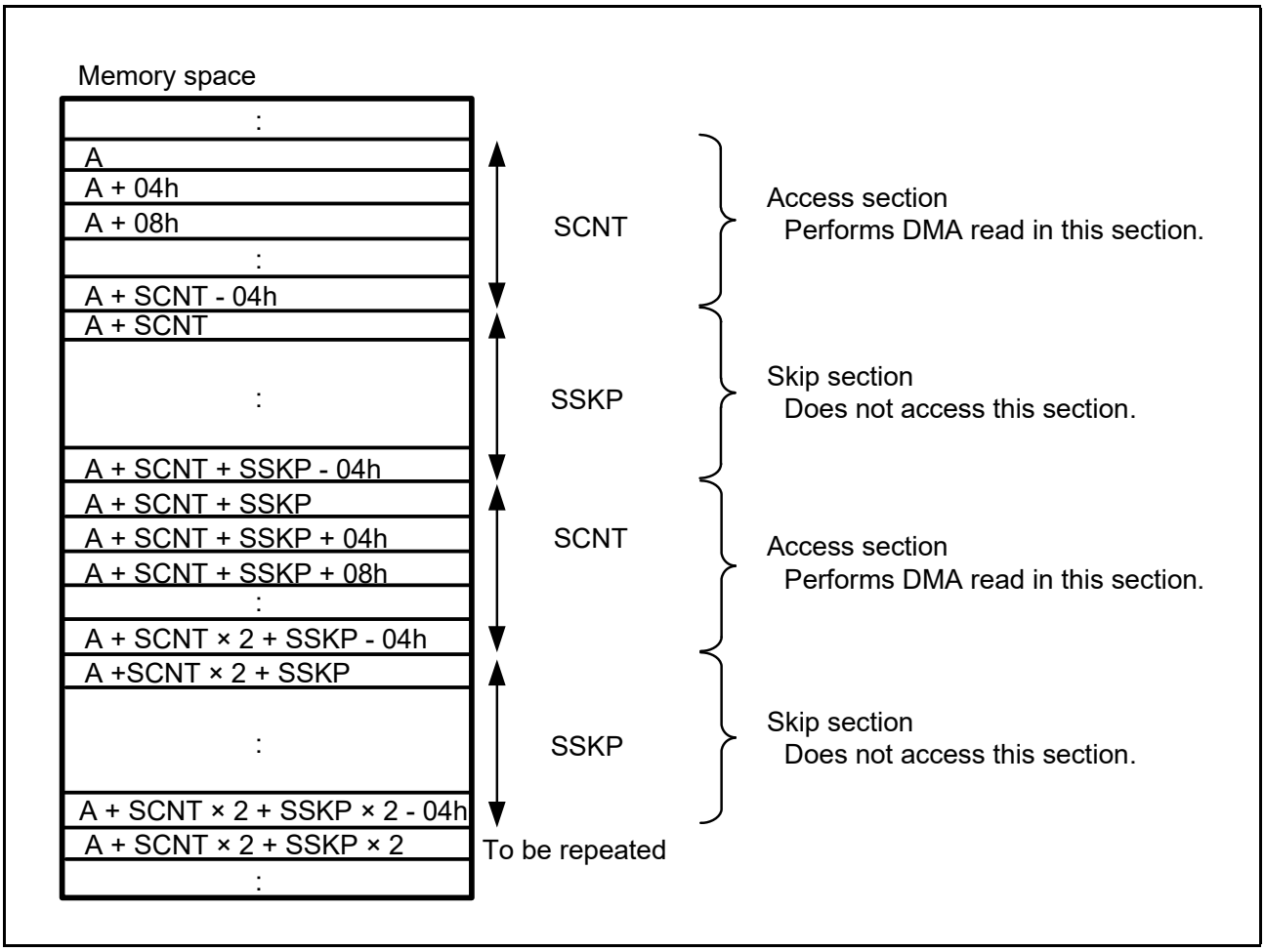


Figure 15.1 Relationship between SSKP and SCNT

Regardless of the source address and the setting value of the RDS field in the CHCFG_n register, the values for SCNT and SSKP can be set. DMAC accesses in the size set in the SDS field in the CHCFG_n register, and acquires the buffer of the valid data only.

15.2.19 Destination Continuous Register n (DCNT_n)

The DCNT_n register sets the space size for continuous access during write access to the DMA transfer destination (n = 15 to 0).

Use this register together with the DSKP_n register (see Figure 15.2).

To set this register, set the DDS[3] bit in the CHCFG_n register to 1.

Address(es): DMAC0
DCNT_0: A006 2208h, DCNT_1: A006 2228h, DCNT_2: A006 2248h, DCNT_3: A006 2268h,
DCNT_4: A006 2288h, DCNT_5: A006 22A8h, DCNT_6: A006 22C8h, DCNT_7: A006 22E8h,
DCNT_8: A006 2608h, DCNT_9: A006 2628h, DCNT_10: A006 2648h, DCNT_11: A006 2668h,
DCNT_12: A006 2688h, DCNT_13: A006 26A8h, DCNT_14: A006 26C8h, DCNT_15: A006 26E8h
DMAC1
DCNT_0: A006 3208h, DCNT_1: A006 3228h, DCNT_2: A006 3248h, DCNT_3: A006 3268h,
DCNT_4: A006 3288h, DCNT_5: A006 32A8h, DCNT_6: A006 32C8h, DCNT_7: A006 32E8h,
DCNT_8: A006 3608h, DCNT_9: A006 3628h, DCNT_10: A006 3648h, DCNT_11: A006 3668h,
DCNT_12: A006 3688h, DCNT_13: A006 36A8h, DCNT_14: A006 36C8h, DCNT_15: A006 36E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DCNT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DCNT[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	DCNT[31:0]	Destination Continuous Access Size	Sets the size of the continuous access space during write access to the DMA transfer destination in bytes.	R/W

When performing a skip transfer on the destination, do not set the DAD bit in the CHCFG_n register to 1 (fixed).

In addition, do not perform a skip transfer when this register is set to 0000 0000h.

15.2.20 Destination Skip Register n (DSKP_n)

The DSKP_n register sets the skip amount during write access to the DMA transfer destination.
During write access to the DMA transfer destination, accesses data of the size set with the DCNT_n register, and then skips the number of the next DMA transfer destination addresses set with this register (n = 15 to 0).
Use this register together with the DCNT_n register (see Figure 15.2).
To set this register, set the DDS[3] bit in the CHCFG_n register to 1.

Address(es): DMAC0
DSKP_0: A006 220Ch, DSKP_1: A006 222Ch, DSKP_2: A006 224Ch, DSKP_3: A006 226Ch,
DSKP_4: A006 228Ch, DSKP_5: A006 22ACh, DSKP_6: A006 22CCh, DSKP_7: A006 22ECh,
DSKP_8: A006 260Ch, DSKP_9: A006 262Ch, DSKP_10: A006 264Ch, DSKP_11: A006 266Ch,
DSKP_12: A006 268Ch, DSKP_13: A006 26ACh, DSKP_14: A006 26CCh, DSKP_15: A006 26ECh
DMAC1
DSKP_0: A006 320Ch, DSKP_1: A006 322Ch, DSKP_2: A006 324Ch, DSKP_3: A006 326Ch,
DSKP_4: A006 328Ch, DSKP_5: A006 32ACh, DSKP_6: A006 32CCh, DSKP_7: A006 32ECh,
DSKP_8: A006 360Ch, DSKP_9: A006 362Ch, DSKP_10: A006 364Ch, DSKP_11: A006 366Ch,
DSKP_12: A006 368Ch, DSKP_13: A006 36ACh, DSKP_14: A006 36CCh, DSKP_15: A006 36ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DSKP[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSKP[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	DSKP[31:0]	Destination Skip Size	Sets the skip amount during write access to the DMA transfer destination in bytes.	R/W

To perform skip transfer on the destination, do not set the DAD bit in the CHCFG_n register to 1 (fixed).

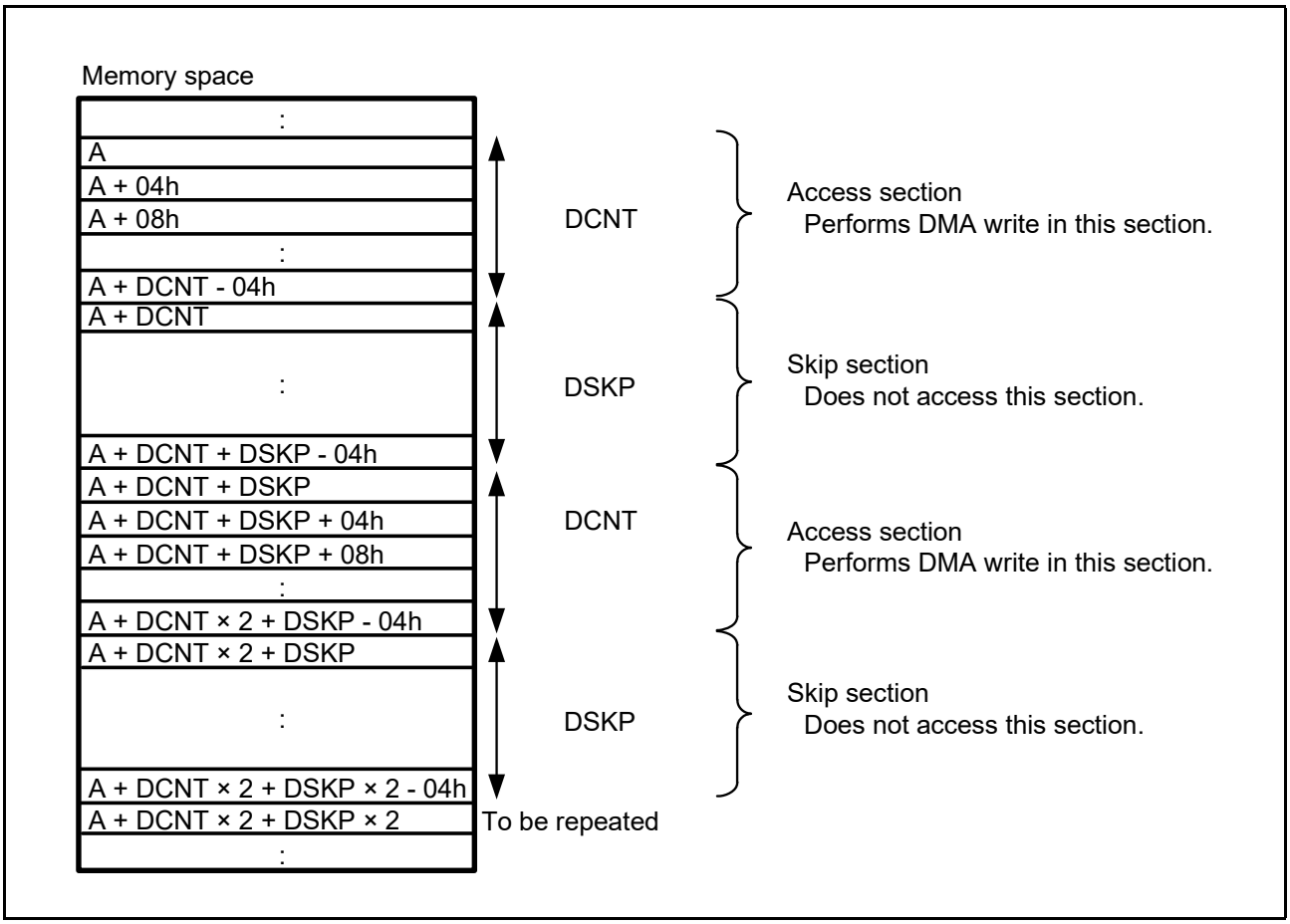


Figure 15.2 Relationship between DSKP and DCNT

Regardless of the destination address and the setting value of the DDS field in the CHCFG_n register, the values for DCNT and DSKP can be set. DMAC performs write access only to the specified space by the size equal to or smaller than the value set in the DDS field in the CHCFG_n register.

15.2.21 DMA Control Register (DCTRL_X (X = A or B))

The DCTRL_X register sets the arbitration between channels in all channels (DCTRL_A = channels 0 to 7, DCTRL_B = channels 8 to 15).

Address(es): DMAC0
DCTRL_A: A006 2300h, DCTRL_B: A006 2700h
DMAC1
DCTRL_A: A006 3300h, DCTRL_B: A006 3700h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PR	Priority Control Select	Sets the transfer priority control mode (see section 15.3.3, DMA Channel Priority Control). 0: Fixed priority mode 1: Round-robin mode	R/W
b31 to b1	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

15.2.22 Descriptor Interval Register n (DSCITVL_X (X = A or B))

The DSCITVL_X register sets the descriptor read interval in all channels (DSCITVL_A = channels 0 to 7, DSCITVL_B = channels 8 to 15).

By setting the DRRP bit in the CHCFG_n register to 1, the descriptor continues to read the descriptor until it reaches LV = 1. This register sets the read interval.

Address(es): DMAC0
DSCITVL_A: A006 2304h, DSCITVL_B: A006 2704h
DMAC1
DSCITVL_A: A006 3304h, DSCITVL_B: A006 3704h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DITVL								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W
b15 to b8	DITVL	Descriptor Interval	Sets the descriptor read interval. The descriptor is read again in the interval of (DITVL × 256) cycles. The descriptor read interval will be (the set value in the DITVL bit × 256 × ICLK) cycles.	R/W
b31 to b16	—	Reserved	These bits are always read as 0. The write value should be 0.	R/W

15.2.23 DMA Status EN Register (DST_EN_X (X = A or B))

The DST_EN_X register indicates the status for the EN bit of all channels (DST_EN_A = channels 0 to 7, DST_EN_B = channels 8 to 15).

Writing data to this register does not change the value of each bit.

Address(es): DMAC0
DST_EN_A: A006 2310h, DST_EN_B: A006 2710h
DMAC1
DST_EN_A: A006 3310h, DST_EN_B: A006 3710h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	EN 7/15	EN 6/14	EN 5/13	EN 4/12	EN 3/11	EN 2/10	EN 1/9	EN 0/8
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EN0/8	Channel 0/8EN	Indicates the status for the EN bit of DMA channel 0/8.	R
b1	EN1/9	Channel 1/9EN	Indicates the status for the EN bit of DMA channel 1/9.	R
b2	EN2/10	Channel 2/10EN	Indicates the status for the EN bit of DMA channel 2/10.	R
b3	EN3/11	Channel 3/11EN	Indicates the status for the EN bit of DMA channel 3/11.	R
b4	EN4/12	Channel 4/12EN	Indicates the status for the EN bit of DMA channel 4/12.	R
b5	EN5/13	Channel 5/13EN	Indicates the status for the EN bit of DMA channel 5/13.	R
b6	EN6/14	Channel 6/14EN	Indicates the status for the EN bit of DMA channel 6/14.	R
b7	EN7/15	Channel 7/15EN	Indicates the status for the EN bit of DMA channel 7/15.	R
b31 to b8	—	Reserved	These bits are always read as 0.	R

15.2.24 DMA Status ER Register (DST_ER_X (X = A or B))

The DST_ER_X register indicates the status for the ER bit of all channels (DST_ER_A = channels 0 to 7, DST_ER_B = channels 8 to 15).

Writing data to this register does not change the value of each bit.

Address(es): DMAC0
DST_ER_A: A006 2314h, DST_ER_B: A006 2714h
DMAC1
DST_ER_A: A006 3314h, DST_ER_B: A006 3714h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ER 7/15	ER 6/14	ER 5/13	ER 4/12	ER 3/11	ER 2/10	ER 1/9	ER 0/8
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ER0/8	Channel 0/8ER	Indicates the status for the ER bit of DMA channel 0/8.	R
b1	ER1/9	Channel 1/9ER	Indicates the status for the ER bit of DMA channel 1/9.	R
b2	ER2/10	Channel 2/10ER	Indicates the status for the ER bit of DMA channel 2/10.	R
b3	ER3/11	Channel 3/11ER	Indicates the status for the ER bit of DMA channel 3/11.	R
b4	ER4/12	Channel 4/12ER	Indicates the status for the ER bit of DMA channel 4/12.	R
b5	ER5/13	Channel 5/13ER	Indicates the status for the ER bit of DMA channel 5/13.	R
b6	ER6/14	Channel 6/14ER	Indicates the status for the ER bit of DMA channel 6/14.	R
b7	ER7/15	Channel 7/15ER	Indicates the status for the ER bit of DMA channel 7/15.	R
b31 to b8	—	Reserved	These bits are always read as 0.	R

15.2.25 DMA Status END Register (DST_END_X (X = A or B))

The DST_END_X register indicates the status for the END bit of all channels (DST_END_A = channels 0 to 7, DST_END_B = channels 8 to 15). Writing data to this register does not change the value of each bit.

Address(es): DMAC0
DST_END_A: A006 2318h, DST_END_B: A006 2718h
DMAC1
DST_END_A: A006 3318h, DST_END_B: A006 3718h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	END 7/15	END 6/14	END 5/13	END 4/12	END 3/11	END 2/10	END 1/9	END 0/8
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	END0/8	Channel 0/8END	Indicates the status for the END bit of DMA channel 0/8.	R
b1	END1/9	Channel 1/9END	Indicates the status for the END bit of DMA channel 1/9.	R
b2	END2/10	Channel 2/10END	Indicates the status for the END bit of DMA channel 2/10.	R
b3	END3/11	Channel 3/11END	Indicates the status for the END bit of DMA channel 3/11.	R
b4	END4/12	Channel 4/12END	Indicates the status for the END bit of DMA channel 4/12.	R
b5	END5/13	Channel 5/13END	Indicates the status for the END bit of DMA channel 5/13.	R
b6	END6/14	Channel 6/14END	Indicates the status for the END bit of DMA channel 6/14.	R
b7	END7/15	Channel 7/15END	Indicates the status for the END bit of DMA channel 7/15.	R
b31 to b8	—	Reserved	These bits are always read as 0.	R

15.2.26 DMA Status SUS Register (DST_SUS_X (X = A or B))

The DST_SUS_X register indicates the status for the SUS bit of all channels (DST_SUS_A = channels 0 to 7, DST_SUS_B = channels 8 to 15). Writing data to this register does not change the value of each bit.

Address(es): DMAC0
DST_SUS_A: A006 2320h, DST_SUS_B: A006 2720h
DMAC1
DST_SUS_A: A006 3320h, DST_SUS_B: A006 3720h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SUS 7/15	SUS 6/14	SUS 5/13	SUS 4/12	SUS 3/11	SUS 2/10	SUS 1/9	SUS 0/8
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SUS0/8	Channel 0/8SUS	Indicates the status for the SUS bit of DMA channel 0/8.	R
b1	SUS1/9	Channel 1/9SUS	Indicates the status for the SUS bit of DMA channel 1/9.	R
b2	SUS2/10	Channel 2/10SUS	Indicates the status for the SUS bit of DMA channel 2/10.	R
b3	SUS3/11	Channel 3/11SUS	Indicates the status for the SUS bit of DMA channel 3/11.	R
b4	SUS4/12	Channel 4/12SUS	Indicates the status for the SUS bit of DMA channel 4/12.	R
b5	SUS5/13	Channel 5/13SUS	Indicates the status for the SUS bit of DMA channel 5/13.	R
b6	SUS6/14	Channel 6/14SUS	Indicates the status for the SUS bit of DMA channel 6/14.	R
b7	SUS7/15	Channel 7/15SUS	Indicates the status for the SUS bit of DMA channel 7/15.	R
b31 to b8	—	Reserved	These bits are always read as 0.	R

15.3 Operation

15.3.1 DMA Mode

With the DMS bit in the CHCFG_n register, DMA mode can be switched between register mode and link mode.

Table 15.3 DMA Mode Setting

DMS (CHCFG_n)	Description	Applications
0	Register mode	With the values set for the next register set, performs a DMA transfer.
1	Link mode	Accesses the descriptor area, and performs a DMA transfer with the value set for the descriptor. Repeats descriptor read and DMA transfer unless you set the descriptor or use the control register to stop them.

15.3.1.1 Register Mode

In register mode, you can perform a DMA transfer with the value set in the internal register.
You can set two sets (Next0 Register Set and Next1 Register Set) of transfer source addresses, the transfer destination addresses, and the numbers of transfer bytes. You can select the next register set to perform a transfer, or transfer two next register sets successively.

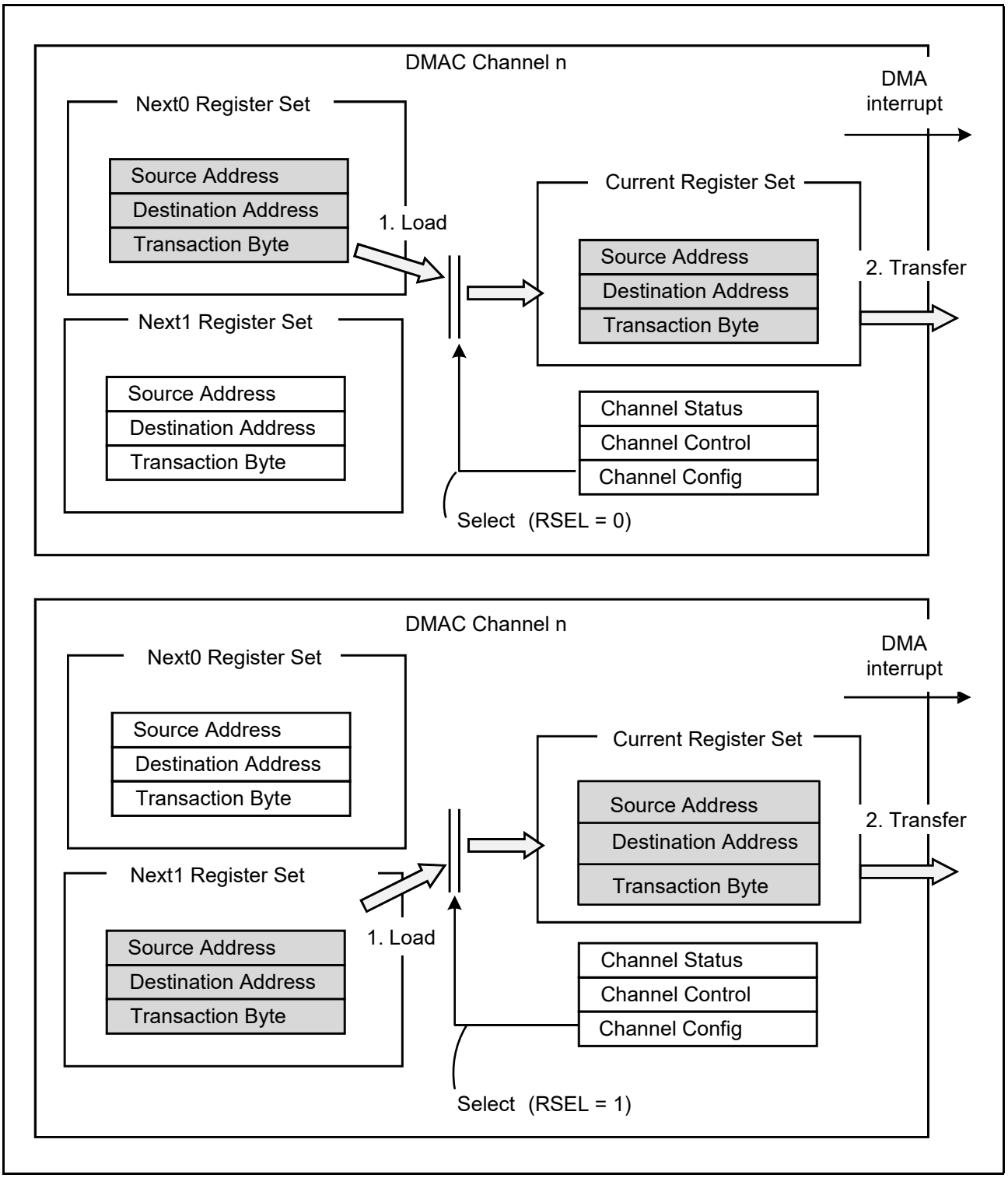


Figure 15.3 Overview of Register Normal Mode

Figure 15.3 illustrates operation when Next0 Register Set is executed (above), and when Next1 Register Set is executed (below).

(1) Operation Flow in Register Mode

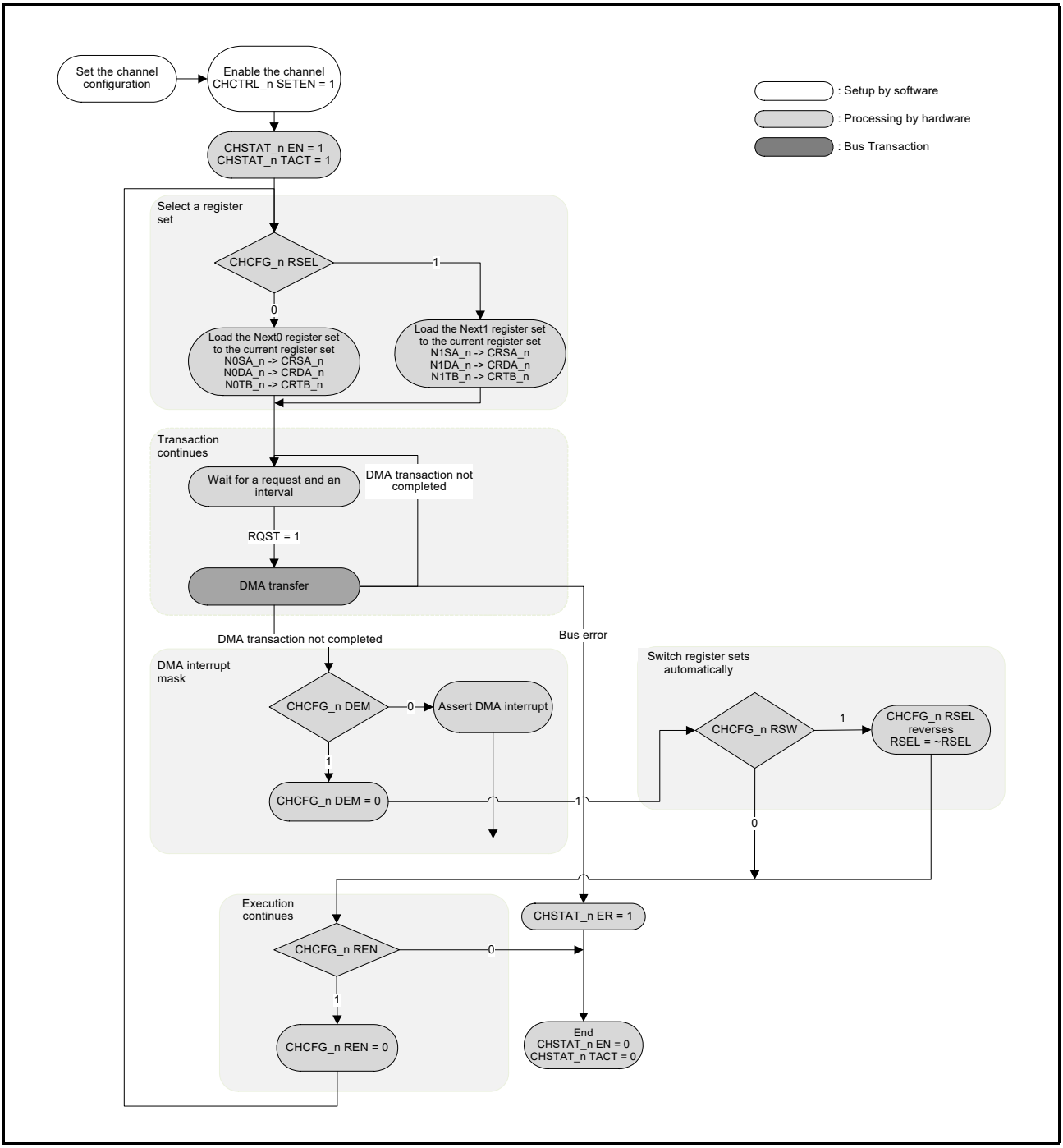


Figure 15.4 Register Mode Flow

<Register Mode Flow Description>

1. Channel Setting
   Set Next0 or Next1 Register Set (the transfer destination address, the transfer source address, and the total number of transfer bytes).
   In addition, use setting registers CHCTRL_n or CHCFG_n for each channel to set detection method of the DMA transfer request, output mode of the DACK/TEND signal, and the amount of data for a transfer.
2. Selecting the register set
   When 1 is written to the SETEN bit in the CHCTRL_n register, the EN bit and the TACT bit in the CHSTAT_n register are set to 1, and the setting value of the next register set selected by the RSEL bit in the CHCFG_n register is loaded to the current register set.
3. DMA Transfer
   According to the set value, a DMA transfer is performed. For details on the transfer, see from section 15.3.2, Transfer Mode to section 15.3.11, Aborting a Transfer.
4. DMA Transfer Completion Mask
   According to the value set for the DEM bit in the CHCFG_n register, the DMA transfer completion interrupt is masked. When DEM = 1, the DMA transfer completion interrupt is masked. Besides, immediately after the DMA transfer completion interrupt conditions are satisfied, the DEM bit is cleared to 0 automatically.
5. Switching Register Sets Automatically
   According to the value set for the RSW bit in the CHCFG_n register, the register set is switched to the other next register set.
6. Successive Execution
   According to the value set for the REN bit in the CHCFG_n register, DMA transfers are performed successively. When REN = 0, the EN bit and the TACT bit in the CHSTAT_n register are cleared to 0, and DMAC stops operation. When REN = 1, the DMA transfer is continued. Besides, immediately after the conditions for performing DMA transfer again are satisfied with the REN bit, the REN bit is cleared to 0 automatically.

(2) Setting the Register Mode

- Register mode settings
  Select the register set to execute.

Table 15.4 Register Mode Settings

DMS (CHCFG_n)	RSEL (CHCFG_n)	Description
0	0	Executes Next0 Register Set.
	1	Executes Next1 Register Set.

- DMA transfer completion interrupt mask settings
  DMA transfer completion interrupts can be masked.

Table 15.5 DMA Transfer Completion Interrupt Mask Settings

DEM (CHCFG_n)	Description
0	When a DMA transfer completes, the DMA transfer completion interrupt is generated.
1	Even if a DMA transfer completes, no DMA transfer completion interrupt is generated. When a DMA transfer completes, the DEM bit is cleared to 0 automatically.

- Settings for executing register sets automatically
  After a DMA transfer, another DMA transfer can be performed successively.

Table 15.6 Settings for Automatic Execution of Register Sets

REN (CHCFG_n)	Operation	Remarks
0	When a DMA transfer of the register set set for the RSEL bit completes, the EN bit is cleared to 0, and the DMA operation ends.	Set this value if you want to perform a DMA transfer once.
1	After a DMA transfer completes, a DMA transfer is performed for the register set that was selected to be performed successively. When the successive transfer is performed, the REN bit is cleared to 0.	Set this register if you want to perform register sets successively.

- Settings for switching register sets automatically
  When a DMA transfer completes, the register set can be switched to the next register set.

Table 15.7 Settings for Switching Register Sets Automatically

RSW (CHCFG_n)	Operation	Remarks
0	When a DMA transfer completes, register sets are not switched.	Set this value when you want to use one register set only.
1	When a DMA transfer completes, the RSEL bit is reversed automatically, and the other register set is selected.	Set this value if you want to switch register sets.

(3) Register Mode Setting Examples

- Using the Next0 register set only

Table 15.8 Register Mode Setting Example 1

DMS (CHCFG_n)	RSEL (CHCFG_n)	DEM (CHCFG_n)	RSW (CHCFG_n)	REN (CHCFG_n)
0 (register mode)	0 (Next0)	0 (Do not mask)	0 (Do not switch)	0 (Continuous execution not in progress)

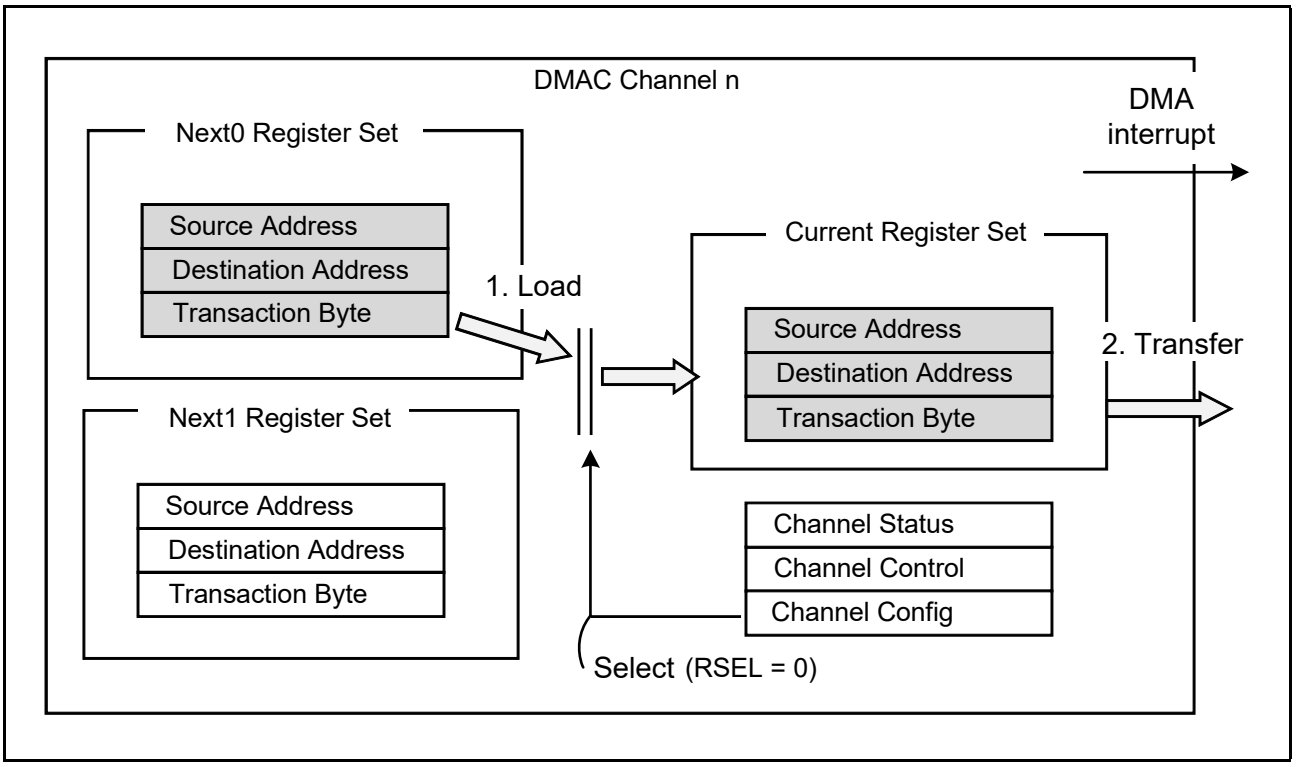


Figure 15.5 Register Mode Setting Example 1

1. Writing 1 to the SETEN bit in the CHCTRL_n register sets 1 to the EN bit in the CHSTAT_n register, and loads Next0 Register Set to the current register set.
2. According to the values set for the current register set and the channel register set, a DMA transfer is performed.
3. Because the DEM bit in the CHCFG_n register is 0, a DMA transfer completion interrupt is generated when a DMA transfer completes.
4. Because the REN bit in the CHCFG_n register is 0, the EN bit in the CHSTAT_n register is cleared to 0, and the operation ends.

- Using two register sets successively

Table 15.9 Register Mode Setting Example 2

DMS (CHCFG_n)	RSEL (CHCFG_n)	DEM (CHCFG_n)	RSW (CHCFG_n)	REN (CHCFG_n)
0 (Register mode)	0 (Next0)	1 (Mask)	1 (Switch)	1 (Continuous execution not in progress)

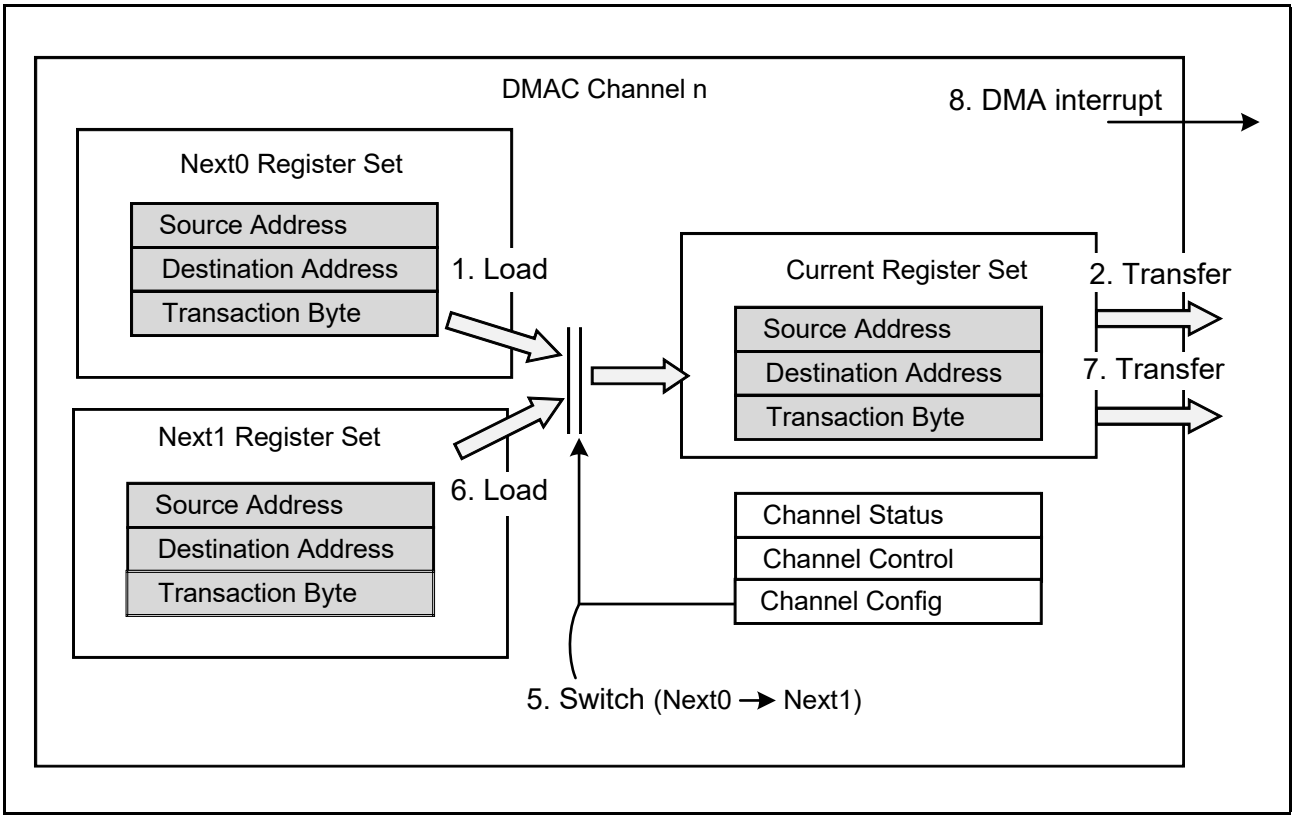


Figure 15.6 Register Mode Setting Example 2

1. Writing 1 to the SETEN bit in the CHCTRL_n register sets 1 to the EN bit in the CHSTAT_n register, and loads Next0 Register Set to the current register set.
2. According to the values set for the current register set and the channel register set, a DMA transfer is performed.
3. Because the DEM bit in the CHCFG_n register is 1, when the DMA transfer completes, no DMA transfer completion interrupt is generated. In addition, the DEM bit is cleared to 0 automatically.
4. Because the REN bit in the CHCFG_n register is 1, DMA transfers are performed successively. In addition, the REN bit is cleared to 0.
5. Because the RSW bit in the CHCFG_n register is 1, the register set to be executed next is switched (RSEL = 0 -> 1).
6. Loads Next1 Register Set to Current Register Set.
7. According to the values for Current Register Set and Channel Register Set, DMA transfers are performed.
8. Because the DEM bit in the CHCFG_n register is 0, a DMA transfer completion interrupt is generated when a DMA transfer completes.
9. Because the REN bit in the CHCFG_n register is 0, the EN bit in the CHSTAT_n register is cleared to 0 automatically.

15.3.1.2 Link Mode

In link mode, a DMA transfer is performed by reading a descriptor in the memory area outside the DMAC as the setting value. Within DMAC, each channel has the next link address (NXLA_n) register and the current link address (CRLA_n) register. Each of them is used to set the address of the descriptor to be executed next, and to indicate the descriptor address of the current DMA transfer respectively.

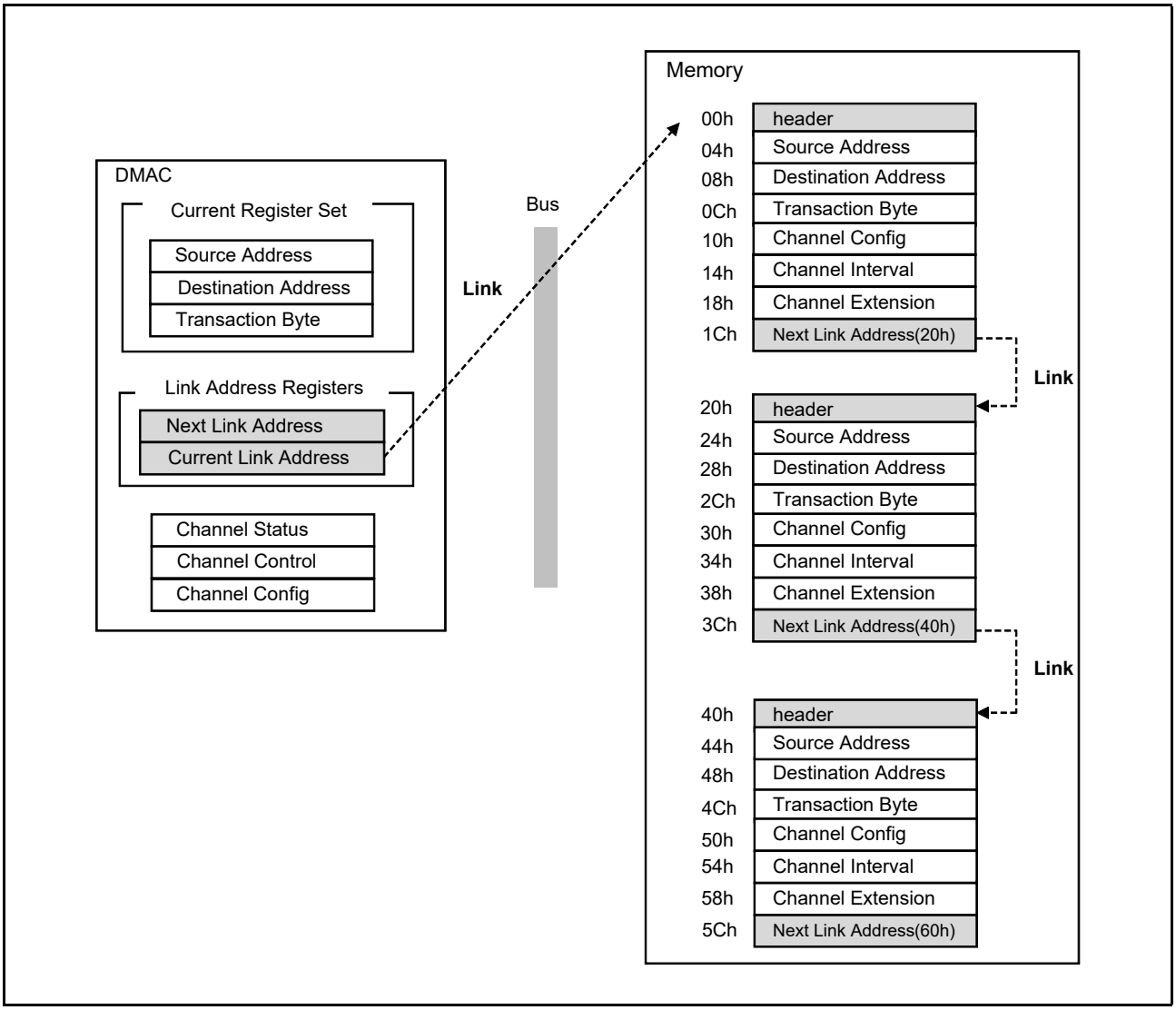


Figure 15.7 Link Mode Overview

(1) Operation flows in link mode

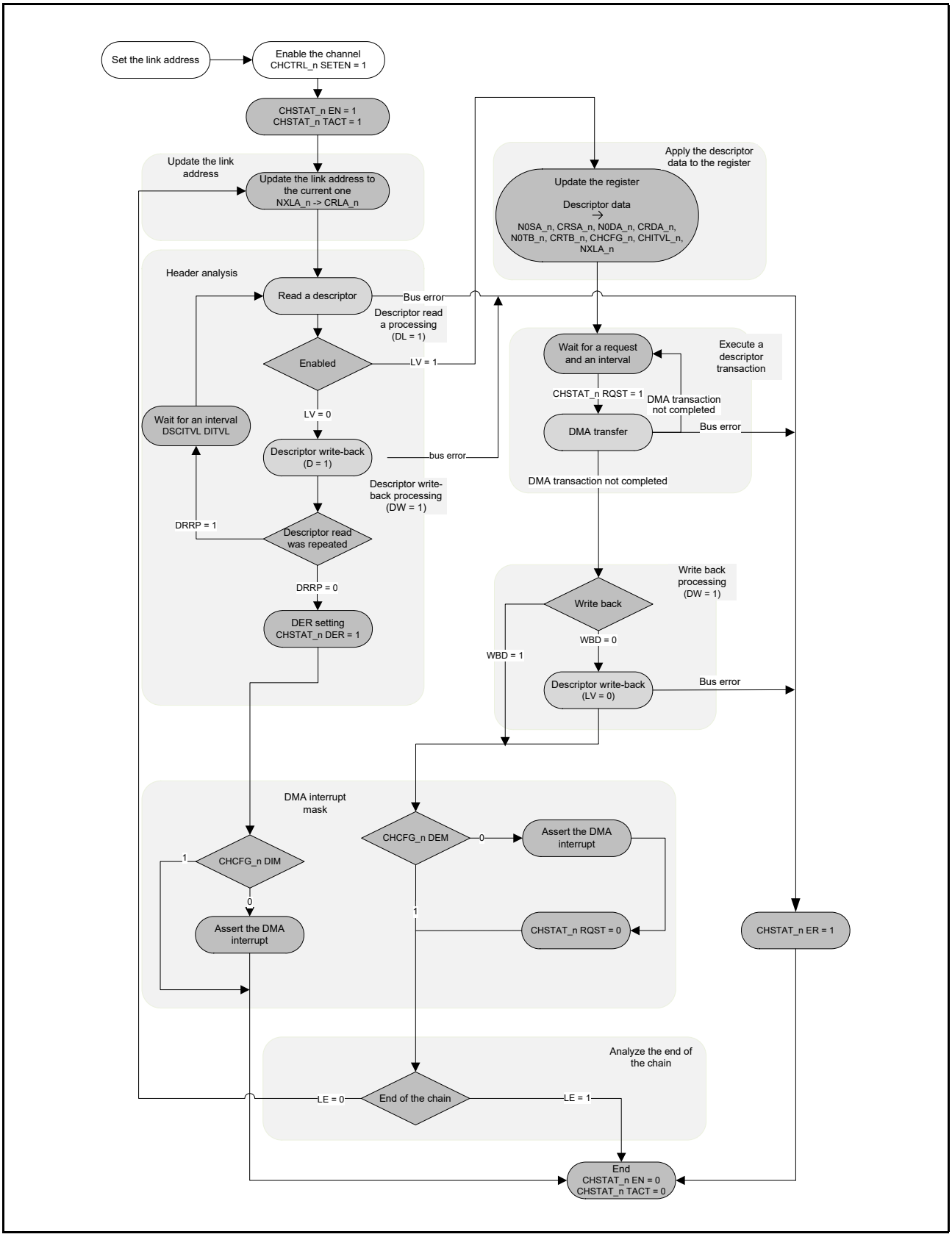


Figure 15.8 Link Mode Operation Flow

<Description of Link Mode Operation Flow>

1. Channel Setting
   Set the start address of the link destination in the NXLA_n register.
2. Updating the Link Address
   Writing 1 to the SETEN bit in the CHCTRL_n register sets 1 to the EN bit and the TACT bit in the CHSTAT_n register, and loads the link address set for the NXLA_n register to the CRLA_n register.
3. Descriptor Read and Header Judgment
   DMAC starts reading a descriptor, and checks the header contents. When LV = 0, 1 is written back to the D bit of header. After that, when the DRRP bit in the CHCFG_n register = 1, the same descriptor is read again after the number of cycles set in the DSCITVL register elapsed. When DRRP =0, DER in the CHSTAT_n register =1. This indicates the end state (the EN bit in the CHSTAT_n register = 0, and TACT = 0). At that time, if the DIM bit in the CHCFG_n register is 0, a DMA transfer completion interrupt is generated.
4. Descriptor Error
   When LV = 1, the read descriptor data is loaded to the current register set, and the channel register set. In addition, the next link destination is loaded to the NXLA_n register.
5. DMA Transfer
   According to the set value, a DMA transfer is performed. For details on the transfer, see from section 15.3.2, Transfer Mode to section 15.3.11, Aborting a Transfer.
6. Writing back of Header
   When WBD of header = 0, DMAC writes LV = 0 back to the header area.
7. DMA Interrupt Mask
   When the DEM bit in the CHCFG_n register is 0, a DMA transfer completion interrupt is generated.
8. Link End Judgment
   When LE of header = 1, the EN bit and the TACT bit in the CHSTAT_n register are cleared to 0, and DMAC stops operation. When LE = 0, the current register set is updated, and the next descriptor read is started.

(2) Register Settings

- Link mode settings
  When using link mode, set the DMS bit in the CHCFG_n register to 1.

Table 15.10 Link Mode Settings

DMS (CHCFG_n)	Description
1	Operates in link mode. This bit cannot be changed by using a descriptor.

- LINK address settings
  As registers that indicate the link destination, the next link address (NXLA_n) register, and the current link address (CRLA_n) register are available.
  To start link mode, set the link destination in the NXLA_n register.
  The NXLA_n register is updated to the next link after a descriptor is read. In addition, the CRLA_n register indicates the link address of the currently executed descriptor.

Table 15.11 Link Address Register Set

Register	Description
NXLA_n	Sets and indicates the next link destination. Before starting link mode, set the address of the link destination for this register.
CRLA_n	Indicates the currently executed link destination. This register is read-only.

(3) Descriptor settings

DMAC supports multiple descriptor formats.
To switch formats, use the DSCFM field of bits[31:28] in the first word (header) of a descriptor.
The following table describes the relationship between the value of the DSCFM bit and the descriptor format.

Table 15.12 Descriptor Format

DSCFM	Descriptor Size	Next Link Address	Channel Interval	Channel Config	Transaction Size	Destination Address	Source Address	Header
3	Four words	Y	— (reload)	— (reload)	— (header)	Y	Y	Y (with STS)
1	Eight words	Y	Y	Y	Y	Y	Y	Y (without STS)
Other than above	Setting prohibited							

Table 15.13 Description of activation in Table 15.12 Descriptor Format

Field	Availability	Description	Remarks
Header	Y (with STS)	Indicates the STS field of [15:0] for header is enabled. The value set in the STS field is used as the total number of transfer bytes (transaction size).	—
	Y (without STS)	The STS field of [15:0] for header is disabled. Use the transaction size of the descriptor as the total number of transfer bytes.	
Source Address	Y	Specifies the source address.	—
Destination Address	Y	Specifies the destination address.	—
Transaction Size	Y	Specifies the transaction size.	—
	— (header)	Omits the transaction size. Use the value set in the STS field of header as the total number of transfer bytes (transaction size).	Because the STS field is 16 bits, the maximum size you can set is 65,535 bytes.
Channel Config Channel Interval	Y	Specifies Channel Config and Channel Interval.	—
	— (reload)	Omits Channel Config and Channel Interval. Inherits the previous setting values (values of the CHCFG_n and CHITVL_n registers at that time).	—
Next Link Address	Y	Specifies the next descriptor address (next link address) that is read after a DMA transfer of this descriptor.	—

DMAC interprets data obtained through descriptor read in order. If a value less than eight words is specified in the DSCFM field, place descriptor data marked with Y in Table 15.12, Descriptor Format on memory.

Table 15.14 Descriptor Placement Example

	Address (Link Address + N)							
DSCFM	+1Ch	+18h	+14h	+10h	+0Ch	+08h	+04h	+00h
3h	—	—	—	—	Next Link Address	Destination Address	Source Address	Header
1h	Next Link Address	—	Interval	Config	Transaction Byte	Destination Address	Source Address	Header

- Header
  As shown below, header indicates descriptor states.
  This area is read by DMAC before starting a DMA transfer in link mode. In addition, after the DMA transfer, the transfer status is written back by DMAC.

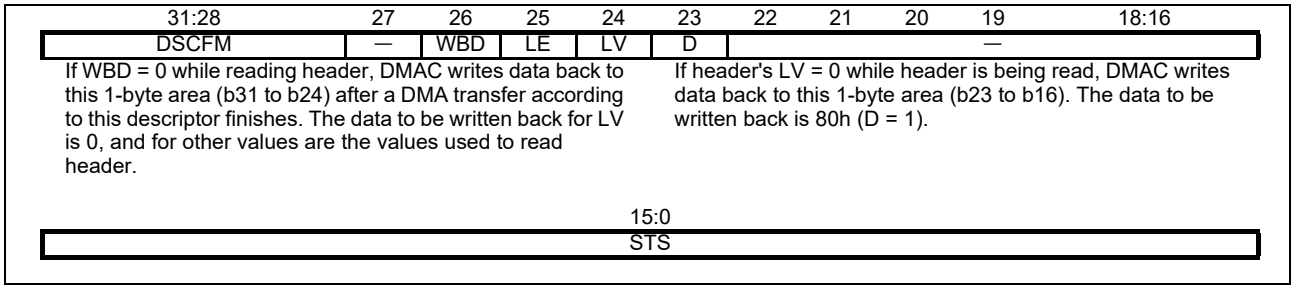


Figure 15.9 Header Area

Table 15.15 Header Area

Bit Position	Bit Name	Description
b15 to b0	STS	When DSCFM = 3, sets the transaction size in bytes. The maximum transfer bytes that can be set is 65,535 bytes. When DSCFM = 3, do not set 0 to the STS bit. If 0 is set, the operation is not guaranteed.
b22 to b16	—	A reserved area. Set 0.
b23	D	Indicates an access error of a descriptor. When LV = 0 while a descriptor is being read, DMAC writes 1 back to this bit. 0: No descriptor error 1: LV = 0 during descriptor read.
b24	LV	Indicates that this descriptor is enabled. When WBD = 0, DMAC writes 0 after the DMA transfer written in the descriptor. Set 1 when setting header. 0: The descriptor is disabled. 1: The descriptor is enabled.
b25	LE	Indicates that the link ends during DMA transfer of this descriptor. To indicate the end of the link, set this bit to 1. 0: The link continues. 1: The link ends.
b26	WBD	Masks write back execution of the LV bit. When this bit is 1, DMAC does not perform write-back operation. 0: The LV bit is written back to 0. 1: The LV bit is not written back.
b27	—	A reserved area. Set 0.
b31 to b28	DSCFM	Specifies the descriptor format (descriptor length, and combination). For details, see Table 15.12.

If you add a descriptor during DMA transfer completion processing (writing back to the descriptor), access of the CPU to set the LV bit to 1, and the access of DMAC to write 1 back to the D bit might conflict. Because of this, the data that was written first is overwritten with the data that was written later.
To avoid this problem, the byte lane of the D bit and the byte lane of the LV bit are placed differently. DMAC uses the byte write method for writing back the D bit. Therefore, to set LV = 1, also use the byte write method.

- Setting descriptors other than header
  Data in descriptors except header has the same specifications as an on-chip register. For details on the on-chip register specifications, see section 15.2, Register Descriptions.
  For descriptor setting examples, see section 15.5.4, Setting Example 4 (Link Mode).

- Descriptor areas and DMA transfer areas
  The following figure provides an overview of the descriptor area and the DMA transfer area to which DMAC accesses.

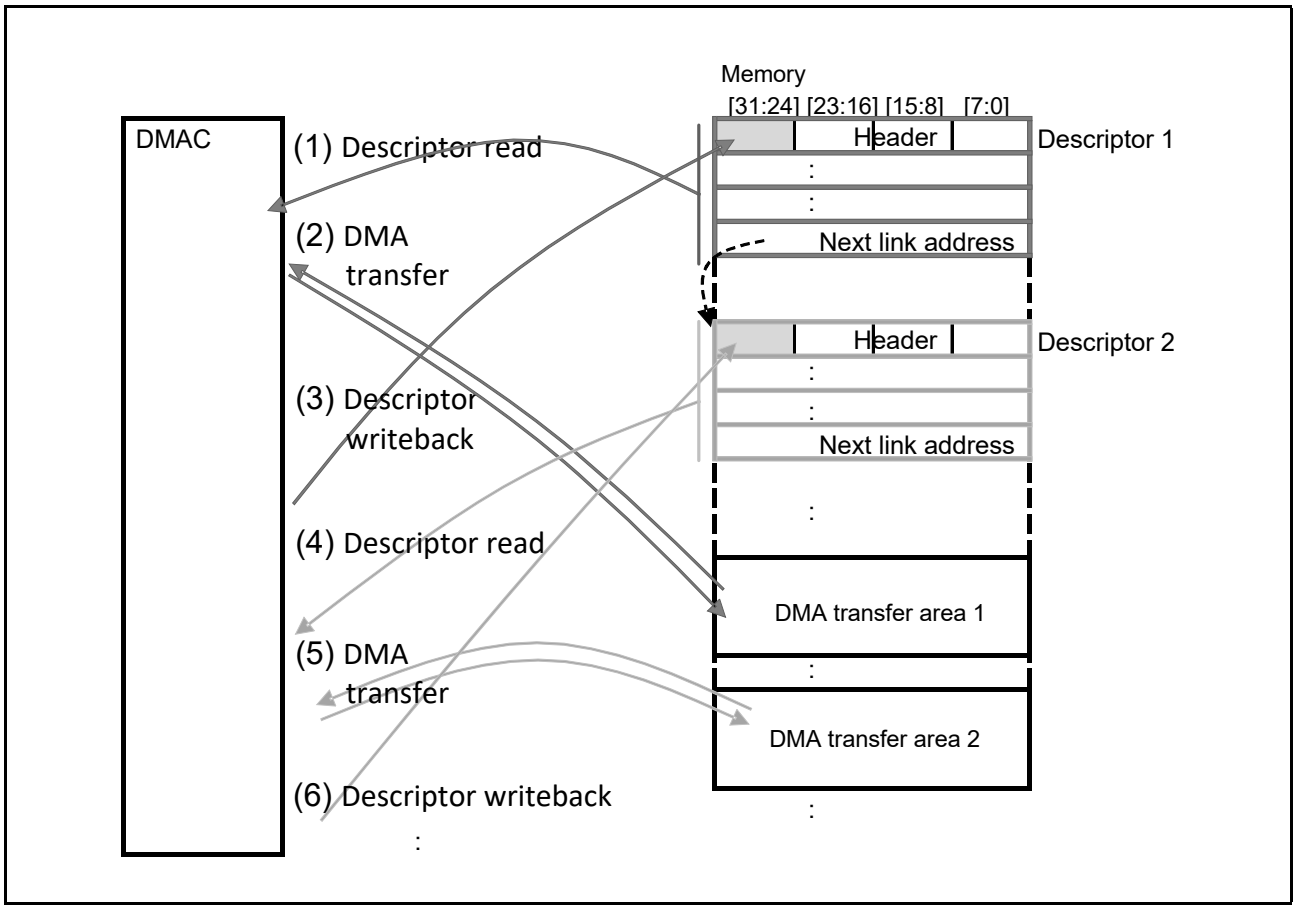


Figure 15.10 Header Area

(1) Descriptor read
Loads the value set for the on-chip NXLA_n register to the CRLA_n register, and then reads the descriptor from the memory space (descriptor 1) indicated by the CRLA_n register.

(2) DMA transfer
When the LV bit in header is 1, performs a DMA transfer according to the descriptor information.

(3) Descriptor write-back
After the DMA transfer for the set number of bytes, if the WBD bit in header is 0, the LV bit writes 0 and other fields writes the value read in step 1 as data back to header[31:24] of descriptor1 in bytes.

(4) Descriptor read
If the LE bit in header of the descriptor which was read previously (step 1) is 0, reads the next descriptor from the address (descriptor 2) indicated by the next link address in the descriptor.

(5) DMA transfer
When the LV bit in header is 1, performs a DMA transfer according to the descriptor information.

(6) Descriptor write-back
After the DMA transfer for the set number of bytes, if the WBD bit in header is 0, the LV bit writes 0 and other fields writes the value read in step 4 as data back to header[31:24] of descriptor2 in bytes.

Hereafter, repeats steps (4) through (6).

When LE of the header is 1 and WBD = 0, DMA transfer proceeds in accord with the descriptor settings, and 0 is written back to the LV bit of the header, after which operation ends.

When header's LE = 1, and WBD = 1, performs a DMA transfer with the setting, and ends the operation (no write-back is performed).

When header's LV = 0, writes 1 back to the D bit of header. And then, if the DRRP bit in the CHCFG_n register = 1, the descriptor is read again after the interval specified in the DITVL field in the DSCITVL_n register. When DRRP = 0, the operation stops.

- Notes on descriptors
  - In link mode, settings can be changed by reading a descriptor, but the timing for changing settings and for a hardware request cannot be synchronized. Because of this, if you want to issue a hardware request (DREQn pin input, and an external interrupt), set the AM, LVL, HIEN, LOEN, and SEL bits in the CHCFG_n register to 1 before setting the SETEN bit in the CHCTRL_n register. Besides, do not change these bits you set in a descriptor.

  - In a descriptor, the settings of the DMS field in the CHCFG_n register cannot be changed (always link mode). In addition, settings of the REN, RSW, and RSEL fields in the CHCFG_n register can be changed in the descriptor, but that does not affect the operation.

  - DMAC references the DSCFM field and the LV bit of header to determine if the descriptor is enabled or disabled. Therefore, initialize (DSCFM = 1 or 3, and LV = 1) the memory area equivalent to the LV bit of the DSCFM field before DMAC accesses it.

  - If you want to set the next descriptor on the memory while reading the transfer settings of DMA (during descriptor read), writes 1 to the LV bit after setting the descriptors after header (source address, destination address, ...next link address). This is to avoid DMA transfer using descriptor values (source address, destination address, and so on) before the setting if descriptor settings by the CPU and descriptor read of DMAC conflict, and DMAC's descriptor read interrupts descriptor settings by the CPU.

  - If you want to keep the information written back to the D bit of header, perform byte access to write 1 to the LV bit of header.

(4) LINK configuration examples

In link mode, descriptors can be configured as in the following figure.

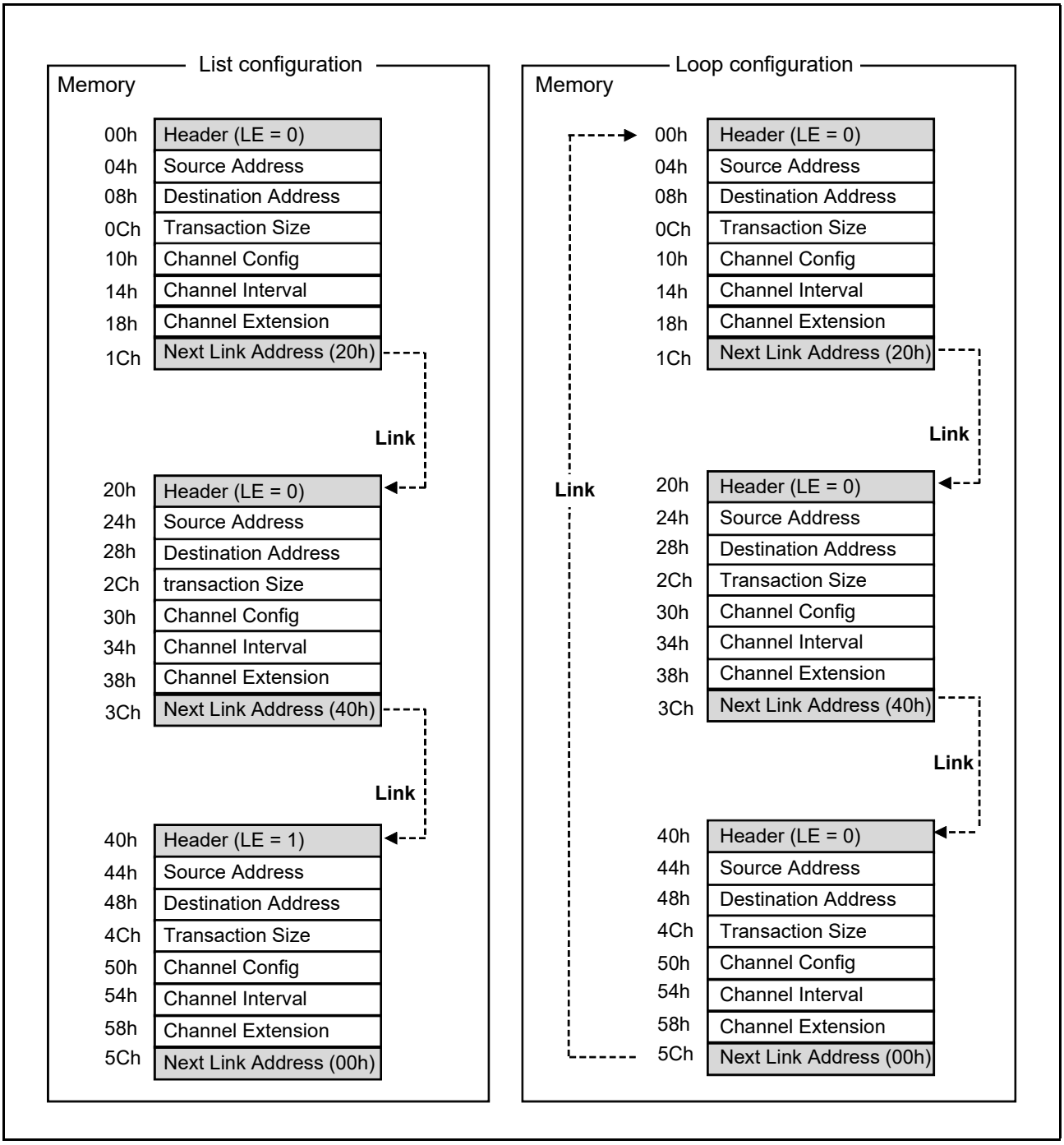


Figure 15.11 Header Area

- List configuration
  Setting 1 to the LE bit in header of the last descriptor ends the link.

- Loop configuration
  Setting the link destination of the last descriptor to the address of the previous descriptor configures the descriptors in a loop. To end the loop, change the LE bit of header to 1 before DMAC reads a descriptor, or follow the procedure to pause a transfer.

15.3.1.3 Write-Only Mode

Setting 1 to the WONLY bit in the CHCFG_n register falls in write-only mode.

Table 15.16 Write-Only Mode Settings

WONLY (CHCFG_n)	Mode	Description
0	Normal Mode	Performs a DMA transfer with the values set for the next register set
1	Write-Only Mode	Performs DMA write transfers only without performing DMA read transfers.

In write-only mode, read operation for DMA transfers is not performed (descriptor read is performed as same as in normal mode). In register mode, use the value set for the NxSA_n register (x = 0 when RSEL = 0, and x = 1 when RSEL = 1) as the write data. In link mode, use the value in the SA field of a descriptor as write data.
Use this mode for initializing a memory area.

15.3.2 Transfer Mode

Single transfer mode and block transfer mode are supported.
When selecting mode, use the TM bit in the CHCFG_n register for each channel.

Table 15.17 Basic Transfer Settings

Transfer Mode	TM (CHCFG_n)	Description
Single transfer	0	For one DMA request, performs a DMA transfer.
Block transfer	1	For one DMA request, performs transfers until a DMA transfer completes.

15.3.2.1 Single Transfer Mode

When a DMA transfer request is accepted, performs a DMA transfer on the side (transfer source or transfer destination) indicated by the REQD bit in the CHCFG_n register to activate DACK. Every time a transfer request is accepted, transfer proceeds. This operation is repeated until it reaches the transfer size loaded from the N0TB_n or N1TB_n register to the CRTB_n register (arbitration between channels is performed for each DMA transfer).
The DACK output timing differs depending on the setting for the REQD bit in the CHCFG_n register, or settings for the transfer size (DDS[2:0] and SDS[2:0] in the CHCFG_n register) bit setting. For details, see section 15.3.8, Differences in Operation According to the Transfer Data Size.
The TEND signal is activated when DACK output of the last DMA transfer is activated.

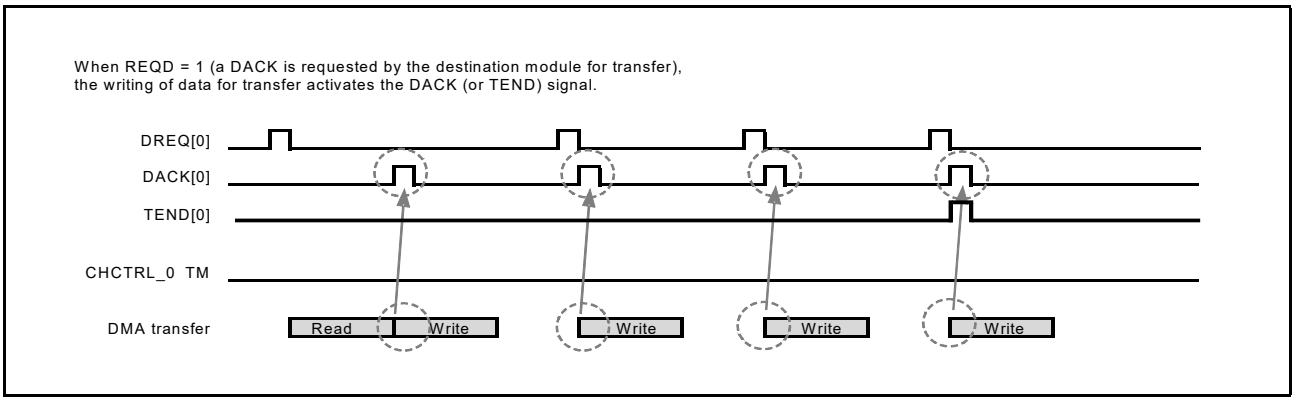


Figure 15.12 Single Transfer Mode (REQD = 1, SDS > DDS)

15.3.2.2 Block Transfer Mode

Once a DMA transfer request is accepted, the transfer continues until transfer of the number of bytes loaded from the N0TB_n or N1TB_n register to the DMA transfer byte register (CRTB_n register) is completed (DMA transfer completion; arbitration between channels is performed for each DMA transfer).
The TEND signal is activated when DACK output of the last DMA transfer is activated.

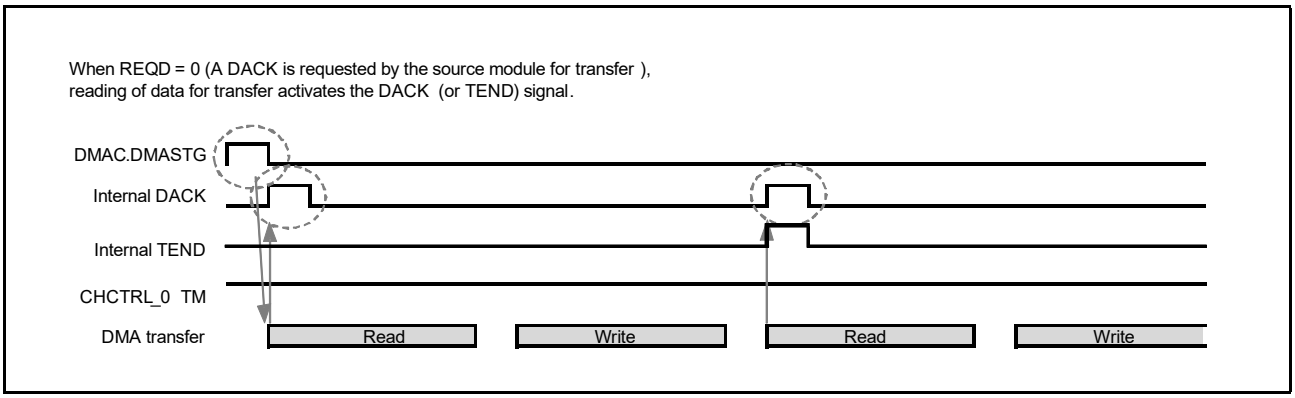


Figure 15.13 Block Transfer Mode (REQD = 0, SDS = DDS)

Note: If the interrupt source is DMAC.DMASTG, DACK and TEND are only active as internal signals and not output from the external pins. For details, see section 15.3.5, DMA Acknowledge Output/DMA Transaction Completion Output Function.

15.3.3 DMA Channel Priority Control

As an arbitration method between channels, fixed priority mode and round-robin mode are supported. To select mode, use the PR bit in the DCTRL register. When the PR bit is 0, fixed priority mode is selected. When the PR bit is set to 1, round-robin mode is selected.

Table 15.18 Priority Control Settings

Transfer Mode	PR (DCTRL)	Description	Applications
Fixed Priority	0	Channels 0 to 7, channels 8 to 15 are fixed priority mode. CH0 (CH8) > CH1 (CH9) > CH2 (CH10) > CH3 (CH11) > CH4 (CH12) > CH5 (CH13) > CH6 (CH14) > CH7 (CH15)	Select this mode if channels have priority.
Round-Robin	1	Controls requests in round-robin mode.	Select this mode if you want to execute requests equally.

15.3.3.1 Fixed Priority Mode

In fixed priority mode, the priority levels are fixed within the group of channels 0 to 7 and within the group of channels 8 to 15. In addition, the priority levels between the group of channels 0 to 7 and the group of channels 8 to 15 are in round-robin mode.
The priority levels immediately after a reset and transfer through DMA channel 0 are shown in Figure 15.14.

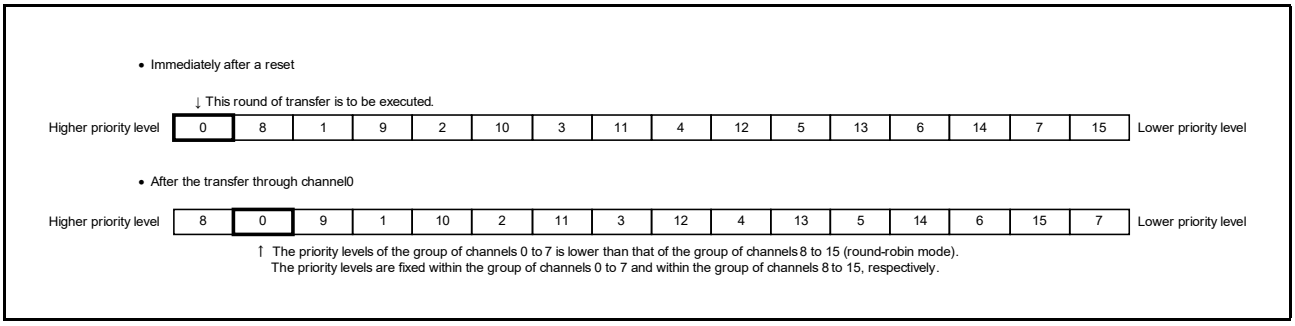


Figure 15.14 Priority Levels Immediately after a Reset and Transfer through DMA Channel 0

If DMA transfer requests are generated on multiple channels simultaneously, a DMA transfer request with a smaller channel number takes precedence.

The following figure provides an example when a DMA transfer is performed in fixed priority mode, if another DMA transfer with higher priority is requested.

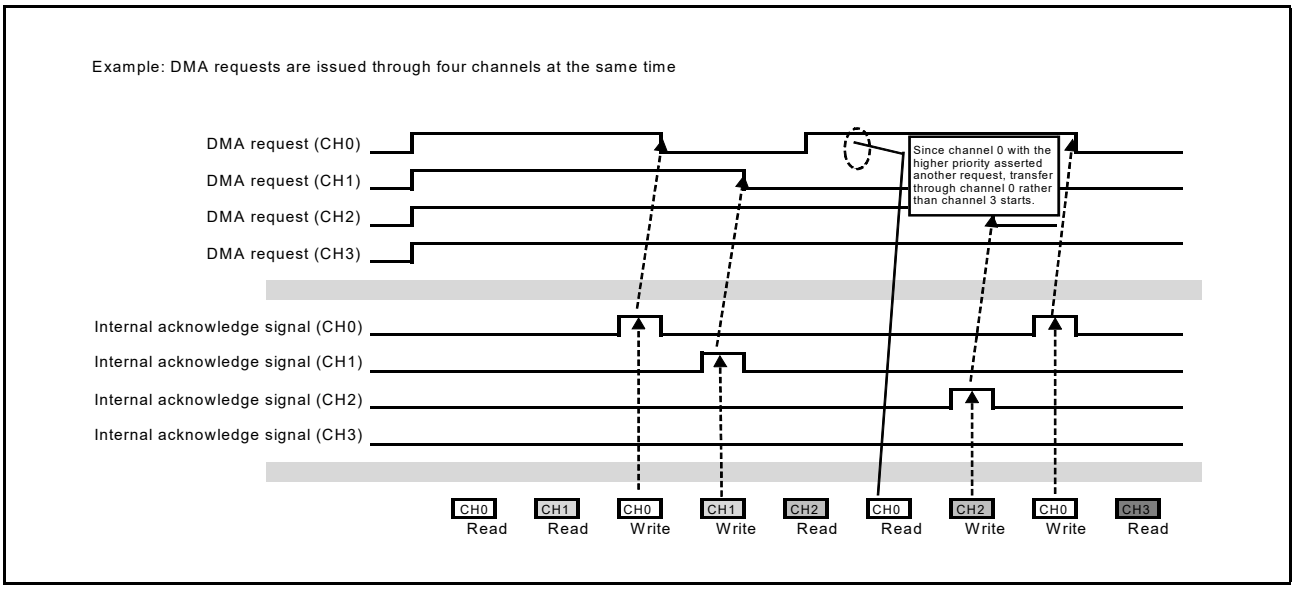


Figure 15.15 Fixed Priority Mode (Number of Channels Is 4, and REQD = 1)

Note: Channel 0 is handled with the highest priority, but the transfer with the next highest priority is performed because bus arbitration is performed after reading data from the transfer source of channel 0 finishes (Another read operation might interrupt the operation between reading data from and writing data to the same channel).

15.3.3.2 Round-Robin Mode

In round-robin mode, priority is changed every time a transfer of a channel is accepted so that the lowest priority is given to the channel in which the last transfer is performed.
The priority levels immediately after a reset and transfer through DMA channel 2 are shown in Figure 15.16.

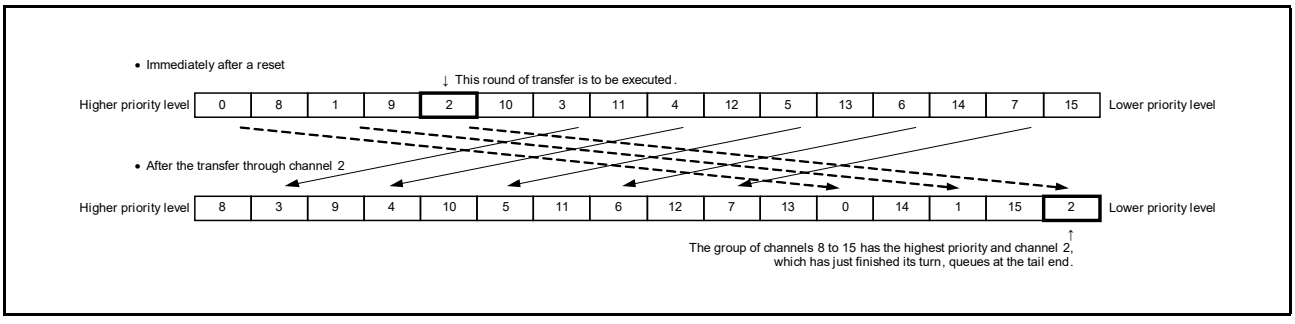


Figure 15.16 Priority Levels Immediately after a Reset and Transfer through DMA Channel 2

The following figure provides an example of a DMA transfer in round-robin mode.

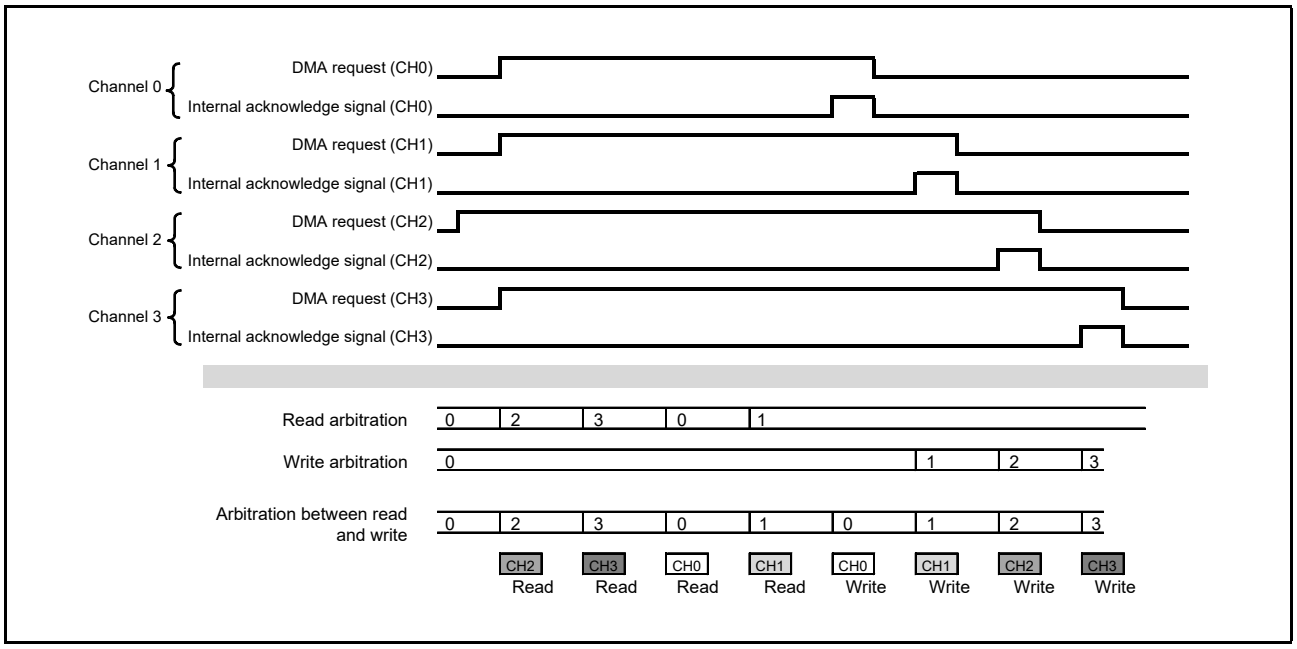


Figure 15.17 Round-Robin Mode (Number of Channels is 4, and REQD = 1)

Note: Within DMAC, arbitration between read channels, and arbitration between write channels are performed. As a result of those arbitrations, further arbitration is performed, and a bus access is issued.

15.3.4 DMA Transfer Request

DMA activation requests have four types including software requests, external requests, on-chip peripheral module requests, and external interrupts.
Select the transfer request source for an external request, on-chip peripheral module request, external interrupt, and software request with the DMAmSELn (m = 0 or 1, n = 0 to 15) register.
For details on the DMAmSELn (m = 0 or 1, n = 0 to 15) register, see section 15.2.8, DMAC Unit 0 Source Select Register i (DMA0SELi) (i = 0 to 15), and section 15.2.9, DMAC Unit 1 Source Select Register i (DMA1SELi) (i = 0 to 15).

15.3.4.1 Specifying Detection Operation of DMA Transfer Requests for Each Source

Detection methods for DMA transfer requests of external requests, on-chip peripheral module requests, external interrupts, and software requests might be specified according to sources.
For each DMA transfer source, set the LVL, HIEN, and LOEN bits in the CHCFG_n register according to Table 15.19, Table 15.20, and Table 15.21.
For details on edge detection operation, see Figure 15.18 and Figure 15.19. For information about level detection operation, see Figure 15.20 and Figure 15.21.

Table 15.19 Detection Operation Specification for Each Source of DMA Transfer Requests

DMA Transfer Request Source	Detection Operation Specification of DMA Transfer Requests	DMA Acknowledge Signal Specification
External request	Detects the rising edge. Detects the falling edge. Detects the high level. Detects the low level.	Depends on specifications of the DMA transfer request source.
On-chip peripheral module request	Depends on specifications of the DMA transfer request source. (See Table 15.21.)	Bus cycle mode
External interrupt	Detects the rising edge. Detects the high level.	Bus cycle mode
Software request	Detects the rising edge.	Bus cycle mode

Table 15.20 Method of Detecting DMA Transfer Request Signals

Mode	LVL (CHCFG_n)	HIEN (CHCFG_n)	LOEN (CHCFG_n)	Description
Edge detection	0	0	0	Disables detection.
			1	Detects the falling edge.
		1	0	Detects the rising edge.
			1	Setting prohibited
Level detection	1	0	0	Disables detection.
			1	Detects the low level.
		1	0	Detects the high level.
			1	Setting prohibited

Table 15.21 DMA Transfer Request Detection Operation Setting Table (1 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
External DMA Request	DREQ0	Arbitrary	Arbitrary	F8h	0/1	001/ 010/ 100	0/1	10/01		0/1	DMAC0 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	DREQ1	Arbitrary	Arbitrary	F9h							
	DREQ2	Arbitrary	Arbitrary	FAh							DMAC1 ch8: 0h ch9: 1h ch10: 2h ch11: 3h ch12: 4h ch13: 5h ch14: 6h ch15: 7h
External Interrupt	IRQ0	Arbitrary	Arbitrary	04h	0/1	010	0/1 *1	1*1	0*1	0/1	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	IRQ1			05h							
	IRQ2			06h							
	IRQ3			07h							
	IRQ4			08h							
	IRQ5			09h							
	IRQ6			0Ah							
	IRQ7			0Bh							
	IRQ8			0Ch							
	IRQ9			0Dh							
	IRQ10			0Eh							
	IRQ11			0Fh							
	IRQ12			10h							
	IRQ13			11h							
	IRQ14			12h							
	IRQ15			13h							
CMT Unit 0	Compare match 0	Arbitrary	Arbitrary	15h	0/1	010	0	1	0	0/1	
	Compare match 1			16h							
CMT Unit 1	Compare match 0	Arbitrary	Arbitrary	17h	0/1	010	0	1	0	0/1	
	Compare match 1			18h							

Table 15.21 DMA Transfer Request Detection Operation Setting Table (2 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
CMTW Unit 0	Compare match	Arbitrary	Arbitrary	19h	0/1	010	0	1	0	0/1	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	Input capture 0			1Ah							
	Input capture 1			1Bh							
	Output compare 0			1Ch							
	Output compare 1			1Dh							
CMTW Unit 1	Compare match	Arbitrary	Arbitrary	1Eh	0/1	010	0	1	0	0/1	
	Input capture 0			1Fh							
	Input capture 1			20h							
	Output compare 0			21h							
	Output compare 1			22h							
S12ADCa Unit 0	AD conversion completed	ADDRn	Arbitrary	23h	0/1	010	0	1	0	0	
	Group B Conversion completed	ADDRn		24h							
S12ADCa Unit 1	AD conversion completed	ADDRn	Arbitrary	26h	0/1	010	0	1	0	0	
	Group B Conversion completed	ADDRn		27h							
DMAC0	DMAC0 Software trigger	Arbitrary	Arbitrary	FBh	0/1	010	0	1	0	0/1	
DMAC1	DMAC1 Software trigger	Arbitrary	Arbitrary	FCh	0/1	010	0	1	0	0/1	
USB	FuncDMA request 1	Arbitrary (for transmission) / D0FIFO (for reception)	D0FIFO (for transmission) / Arbitrary (for reception)	2Bh	0	010 *3	1	1	0	0/1	
	Func DMA request 2			2Ch							
Ethernet switch with IEEE1588	Ethernet switch Interrupt	Arbitrary	Arbitrary	2Dh	0/1	010	0	1	0	0/1	
	Ethernet switch DLR Interrupt	Arbitrary	Arbitrary	2Eh							
	Ethernet switch SYNCOUT Interrupt	Arbitrary	Arbitrary	2Fh							
Ethernet PHY	Ethernet PHY Interrupt 0	Arbitrary	Arbitrary	30h	0/1	010	0/1	1	0	0/1	
	Ethernet PHY Interrupt 1	Arbitrary	Arbitrary	31h							
	Ethernet PHY Interrupt 2	Arbitrary	Arbitrary	32h							
Ethernet MAC	Ethernet MACDMA reception completed	Arbitrary	Arbitrary	33h	0/1	010	0	1	0	0/1	
	Ethernet MACDMA transmission completed	Arbitrary	Arbitrary	34h							
	Reception frame normal interrupt	Arbitrary	Arbitrary	35h							

Table 15.21 DMA Transfer Request Detection Operation Setting Table (3 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
MTU3a	TGIA6	Arbitrary	Arbitrary	36h	0/1	010	0	1	0	0/1	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	TGIB6			37h							
	TGIC6			38h							
	TGID6*4			39h							
	TGIA7			3Bh							
	TGIB7			3Ch							
	TGIC7			3Dh							
	TGID7			3Eh							
	TCIV7			3Fh							
Ethernet MAC	Ethernet MII management access completion Interrupt	Arbitrary	Arbitrary	40h	0/1	010	0	1	0	0/1	
	Ethernet pause packet transmission completion interrupt			41h							
	Ethernet transmission completed interrupt			42h							
EtherCAT Slave (optional)	Sync0 interrupt	Arbitrary	Arbitrary	49h	0/1	010	0	1	0	0/1	
	Sync1 interrupt			4Ah							
	EtherCAT interrupt			4Bh							
	SOF interrupt			4Ch							
	EOF interrupt			4Dh							
RSPI Channel 0	Reception buffer full	SPDR	Arbitrary	50h	0	010	0	1	0	0	
	Transmission buffer empty	Arbitrary	SPDR	51h	0	010	0	1	0	1	
RSPI Channel 1	Reception buffer full	SPDR	Arbitrary	54h	0	010	0	1	0	0	
	Transmission buffer empty	Arbitrary	SPDR	55h	0	010	0	1	0	1	
RSPI Channel 2	Reception buffer full	SPDR	Arbitrary	58h	0	010	0	1	0	0	
	Transmission buffer empty	Arbitrary	SPDR	59h	0	010	0	1	0	1	
RSPI Channel 3	Reception buffer full	SPDR	Arbitrary	5Ch	0	010	0	1	0	0	
	Transmission buffer empty	Arbitrary	SPDR	5Dh	0	010	0	1	0	1	
SCIFA Channel 0	Reception buffer full	FRDR	Arbitrary	61h	0	010	1	1	0	0	
	Transmission buffer empty	Arbitrary	FTDR	62h	0	010	1	1	0	1	
SCIFA Channel 1	Reception buffer full	FRDR	Arbitrary	65h	0	010	1	1	0	0	
	Transmission buffer empty	Arbitrary	FTDR	66h	0	010	1	1	0	1	
SCIFA Channel 2	Reception buffer full	FRDR	Arbitrary	6Eh	0	010	1	1	0	0	
	Transmission buffer empty	Arbitrary	FTDR	6Fh	0	010	1	1	0	1	
SCIFA Channel 3	Reception buffer full	FRDR	Arbitrary	72h	0	010	1	1	0	0	
	Transmission buffer empty	Arbitrary	FTDR	73h	0	010	1	1	0	1	

Table 15.21 DMA Transfer Request Detection Operation Setting Table (4 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n						
					TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
SCIFA Channel 4	Reception buffer full	FRDR	Arbitrary	76h	0	010	1	1	0	0	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	Transmission buffer empty	Arbitrary	FTDR	77h	0	010	1	1	0	1	
RIIC Channel 0	Data reception completed	ICDRR	Arbitrary	7Ah	0	010	0	1	0	0	
	Transmission data empty	Arbitrary	ICDRT	7Bh	0	010	0	1	0	1	
RIIC Channel 1	Data reception completed	ICDRR	Arbitrary	7Dh	0	010	0	1	0	0	
	Transmission data Empty	Arbitrary	ICDRT	7Eh	0	010	0	1	0	1	
MTU3a	TGIA0	Arbitrary	Arbitrary	91h	0/1	010	0	1	0	0/1	
	TGIB0			92h							
	TGIC0			93h							
	TGID0			94h							
	TGIA1			98h							
	TGIB1			99h							
	TGIA2			9Ch							
	TGIB2			9Dh							
	TGIA3			A0h							
	TGIB3			A1h							
	TGIC3			A2h							
	TGID3			A3h							
	TGIA4			A5h							
	TGIB4			A6h							
	TGIC4			A7h							
	TGID4			A8h							
	TCIV4			A9h							
	TGIU5			AAh							
	TGIV5			ABh							
	TGIW5			ACh							
	TGIA8			ADh							
	TGIB8			AEh							
	TGIC8			AFh							
	TGID8			B0h							

Table 15.21 DMA Transfer Request Detection Operation Setting Table (5 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n						
					TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
GPT	GTCIA0	Arbitrary	Arbitrary	B2h	0/1	010	0	1	0	0/1	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	GTCIB0			B3h							
	GTCIC0			B4h							
	GTCID0			B5h							
	GTCIE0			B6h							
	GTCIF0			B7h							
	GDTE0			B8h							
	GTCIV0			B9h							
	GTCIU0			BAh							
	GTCIA1			BBh							
	GTCIB1			BCh							
	GTCIC1			BDh							
	GTCID1			BEh							
	GTCIE1			BFh							
	GTCIF1			C0h							
	GDTE1			C1h							
	GTCIV1			C2h							
	GTCIU1			C3h							
	GTCIA2			C4h							
	GTCIB2			C5h							
	GTCIC2			C6h							
	GTCID2			C7h							
	GTCIE2			C8h							
	GTCIF2			C9h							
	GDTE2			CAh							
	GTCIV2			CBh							
	GTCIU2			CCh							
	GTCIA3			CDh							
	GTCIB3			CEh							
	GTCIC3			CFh							
	GTCID3			D0h							
	GTCIE3			D1h							
	GTCIF3			D2h							
	GDTE3			D3h							
	GTCIV3			D4h							
	GTCIU3			D5h							
	ETGIN			D6h							
	ETGIP			D7h							

Table 15.21 DMA Transfer Request Detection Operation Setting Table (6 / 6)

DMA Transfer Request Source	DMA Transfer Source	Transfer Source	Transfer Destination	DMAm SELn [7:0]	CHCFG_n TM	AM [2:0] *2	LVL	HIEN	LOEN	REQD	SEL[2:0]
TPUa Unit 0	TGI0A	Arbitrary	Arbitrary	D8h	0/1	010	0	1	0	0/1	DMAC0/1 ch0/8: 0h ch1/9: 1h ch2/10: 2h ch3/11: 3h ch4/12: 4h ch5/13: 5h ch6/14: 6h ch7/15: 7h
	TGI0B			D9h							
	TGI1A			DDh							
	TGI1B			DEh							
	TGI2A			E1h							
	TGI2B			E2h							
	TGI3A			E5h							
	TGI3B			E6h							
	TGI4A			EAh							
	TGI4B			EBh							
	TGI5A			EEh							
	TGI5B			EFh							
ELC	ELCIRQ1	Arbitrary	Arbitrary	F2h	0/1	010	0	1	0	0/1	
	ELCIRQ2			F3h							

Note 1. Set the LVL, HIEN, and LOEN bits of the external interrupt (IRQ0 to IRQ15) as follows.
For the setting of the IRQCRi (i = 0 to 15) register, see section 12.3.1, Selecting Interrupt Request Destinations.
LVL: Set according to the edge/level setting of the IRQCRi register.
HIEN: Set to 1 regardless of the detection level of the IRQCRi register.
LOEN: Set to 0 regardless of the detection level of the IRQCRi register.
Note 2. If the DACK/TEND signal is not used, specify any setting.
Note 3. Whether the DACK/TEND signal is used or not, make sure these bits are set to “010”.
Note 4. Interrupts are generated in response to requests for DMA transfer, but there are no interrupts on completion of transfer. Poll the END bit of the CHSTAT_n register to confirm the completion of DMA transfer.

Remarks: CHCFG_n register setting values
TM Bit
0: Single transfer
1: Block transfer
AM bit
001: DACK level output
010: DACK bus cycle output
100: Masks DACK output.
LVL bit
0: Detects the edge of a DMA request.
1: Detects the level of a DMA request.
REQD bit
0: DACK output during read operation.
1: DACK output during write operation.

Note: Instead of an interrupt source from peripheral modules, transfer completion sources of DMAC channels selected by the DMAC source select register are connected to the vector number selected by the DMAC source select register.
Note: Be sure to select edge detection with the PLSn register as the transfer completed interrupt detection type for the DMAC.

15.3.4.2 Edge Detection

Setting the LVL bit in the CHCFG_n register to 0 detects the edge.
Setting the HIEN bit in the CHCFG_n register to 1 detects the rising edge, and setting the LOEN bit in the CHCFG_n register to 1 detects the falling edge.
For DMA requests by the DREQn signal, request the next DMA transfer when the DACK or TEND signal is activated.

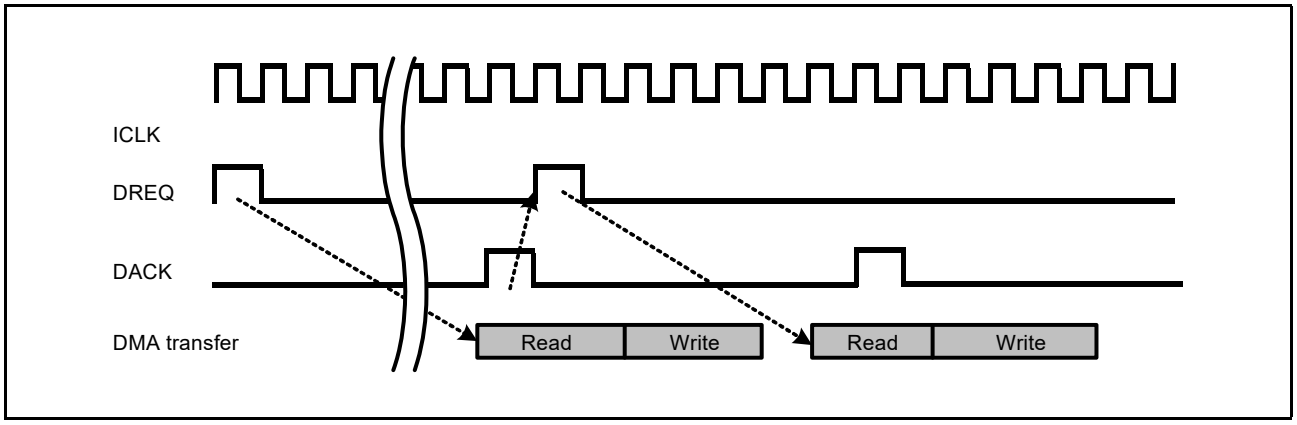


Figure 15.18 Edge Detection Timing (Rising Edge (HIEN = 1), DACK Output is Active during Reading (REQD = 0))

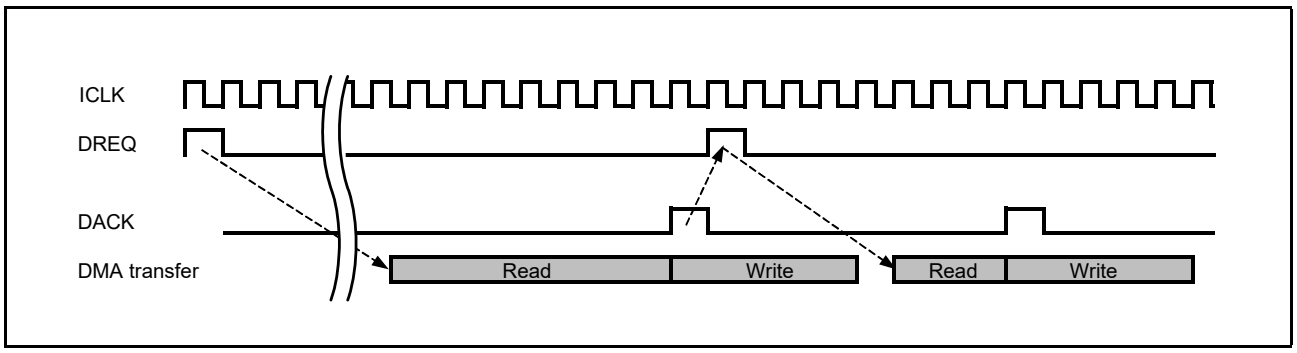


Figure 15.19 Edge Detection Timing (Rising Edge (HIEN = 1), DACK Output is Active during Writing (REQD = 1))

15.3.4.3 Level Detection

Setting the LVL bit in the CHCFG_n register to 1 detects the level.
If a DMA transfer request is active (according to HIEN or LOEN settings) for two consecutive clocks (ICLK) or more, it is recognized as a DMA request.

If the DACK/TEND signal output is set to level mode, the DACK/TEND signal output remains in the high level until the DMA transfer request is deactivated.
If you want to request the next DMA transfer, wait until the DACK/TEND signal is deactivated.

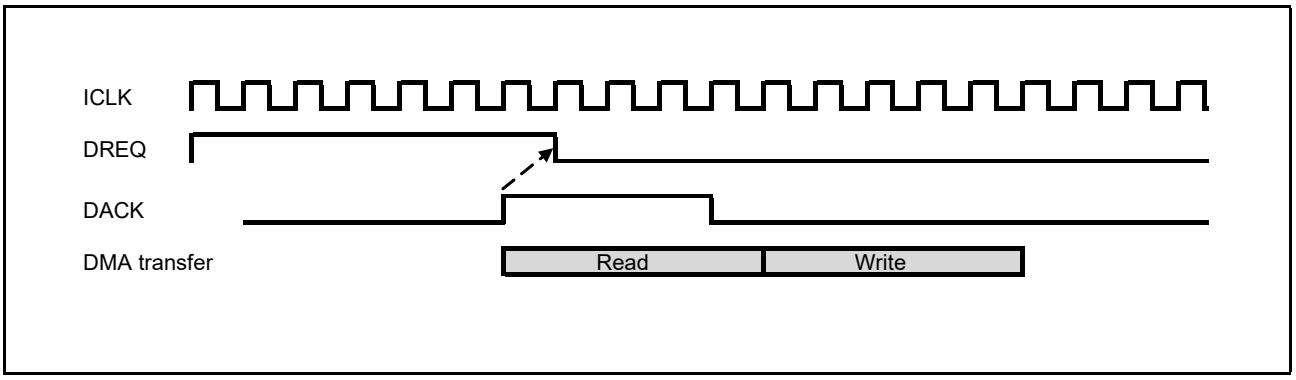


Figure 15.20 Level Detection Timing (High-Level Detection (HIEN = 1), DACK Output is Active during Reading (REQD = 0))

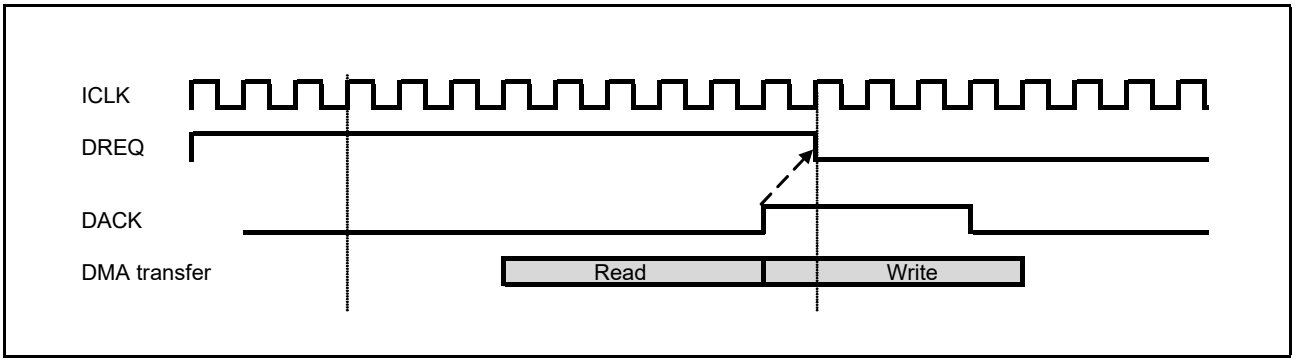


Figure 15.21 Level Detection Timing (High-Level Detection (HIEN = 1), DACK Output is Active during Writing (REQD = 1))

15.3.5 DMA Acknowledge Output/DMA Transaction Completion Output Function

As a reception response signal for a DMA transfer request, the DMA acknowledge signal (DACK) is output.
The DMA transfer completion signal (TEND) is output when the DACK signal for the last DMA transfer is output.
If you use the DREQn signal for a DMA transfer request, use DACKn as the DMA acknowledge signal, and use TENDn as the DMA transaction completion output signal.
Set the output mode of the DACKn and TENDn signals with the AM2 to AM0 bits of the channel configuration register (CHCFGn). Level output and bus cycle output are supported.
The outputs of DACK and TEND signals on the DACKn and TENDn pins are active only when the conditions given below are met. To use the DACKn and TENDn pins, make appropriate settings for the MPC.P#nPFS.PSEL (# = 0-9 and A-R, n = 0-7) bits and the port mode register (PMR) to use those pins as “peripheral functions”.
The conditions:

- The DREQn pin is set as the source for the DMA transfer request.
- The source and destination of the DMA transfer are set as follows:
  - DMA is set to be transferred from an external address space (CSn) to any destination while the CHCFG_n.REQD bit is set to 0 (requested from the source of transfer)
  - DMA is set to be transferred to an external address space (CSn) from any source while the CHCFG_n.REQD bit is set to 1 (requested from the destination of transfer)

The outputs on the pins are not active for the cases other than above. However, the internal signals become active according to the setting of the AM[2:0] bits.

Transfer Requested From	Source for DMA Transfer	Transferred From	Transferred To	CHCFG_n		External Pins Used for Outputting an Active Signal	
				AM[2:0]	REQD	DACK Signal	TEND Signal
Request from outside	DREQ0	External bus	Anywhere	001/010	0	DACK0	TEND0
		Anywhere	External bus		1	DACK0	TEND0
		Internal	Anywhere		0	—	—
		Anywhere	Internal bus		1	—	—
	DREQ1	External bus	Anywhere	001/010	0	DACK1	TEND1
		Anywhere	External bus		1	DACK1	TEND1
		Internal	Anywhere		0	—	—
		Anywhere	Internal bus		1	—	—
	DREQ2	External bus	Anywhere	001/010	0	DACK2	TEND2
		Anywhere	External bus		1	DACK2	TEND2
		Internal	Anywhere		0	—	—
		Anywhere	Internal bus		1	—	—
Other than above	Other than above	Anywhere	Anywhere	Any value	Any value	—	—

—: The outputs on the pin are always inactive. Inactive signal level is obtained by inverting the active level set by the bits which specify the acknowledge levels and transfer-end levels.
External bus refers to the CS0 to CS5 spaces and internal bus refers to the address spaces other than the external bus.

15.3.5.1 Specifying Mode of Acknowledge Signals/DMA Transaction Completion Signals for Each Source of DMA Transfer Requests

For the DMA acknowledge signal and DMA transaction completion signal, output mode might be specified according to the source.
For each DMA transfer request source, specify the correct operation with the AM[2:0] bits of the channel configuration register (CHCFGn) according to Table 15.19, Table 15.21, and Table 15.22.

For details on level output operation, see Figure 15.22, DACK/TEND Output Timing (AM[2:0] = 001, REQD = 0) and Figure 15.23, DACK/TEND Output Timing (AM[2:0] = 001, REQD = 1). For details on bus cycle output operation, see Figure 15.24, Bus Cycle Output Timing (REQD = 0) and Figure 15.25, Bus Cycle Output Timing (REQD = 1).

Table 15.22 DACKn/TENDn Pin Output Settings

Mode	AM[2] (CHCFG_n)	AM[1:0] (CHCFG_n)	REQD (CHCFG_n)	Applications
Level	0	01	0 (Activated during read operation)	In level mode, activate DACK/TEND. DACK/TEND output remains active until the DMA transfer request is deactivated. The TEND signal is activated when the final DMA transfer is performed.
			1 (Activated during write operation)	
Bus cycle	0	10 11	0 (Activated during read operation)	The DACK/TEND signal remains active during a bus cycle. Use this mode if you want to activate the DACK/TEND signal until a bus cycle ends. The TEND signal is activated when the last DMA transfer is performed.
			1 (Activated during write operation)	
Mask	1	—	—	Set DACK/TEND output to inactive (fixed). Use this mode if you do not want to notify the connection destination of DACK/TEND output.

15.3.5.2 Level Output

By setting the AM field in the CHCFG_n register to 001, the mode is switched to level output.
DACK output remains active until the DMA transfer request is deactivated. In addition, if it is the last DMA transfer, the TEND signal is output (level output) at the same timing as the DACK output.

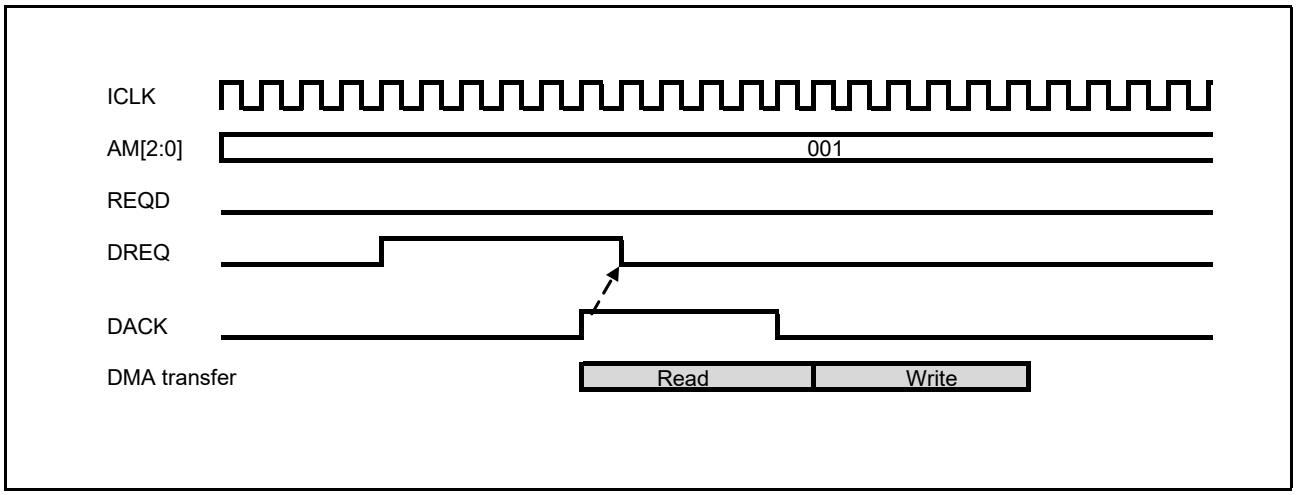


Figure 15.22 DACK/TEND Output Timing (AM[2:0] = 001, REQD = 0)

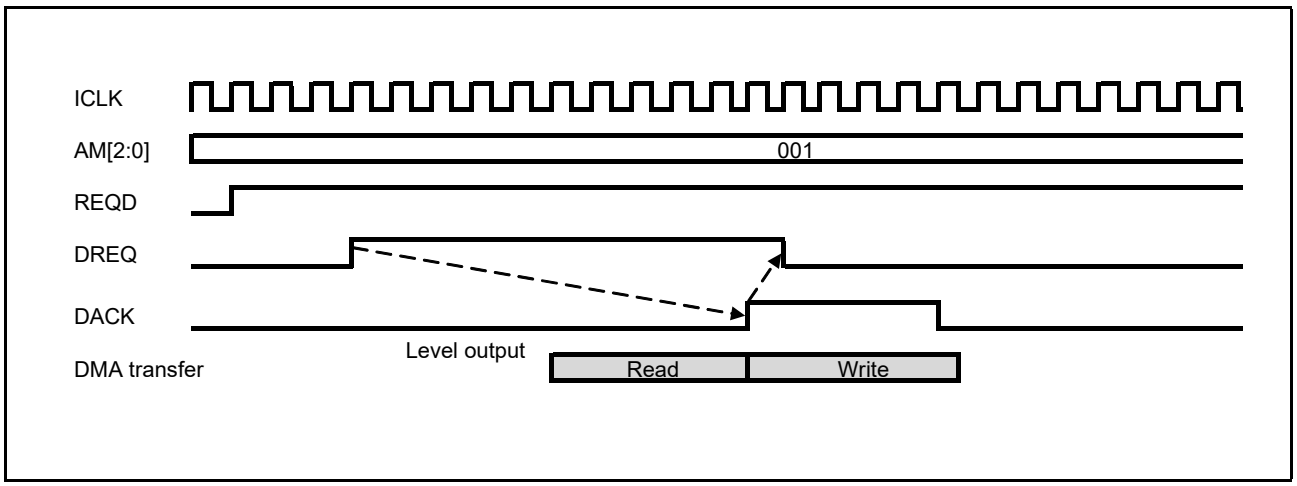


Figure 15.23 DACK/TEND Output Timing (AM[2:0] = 001, REQD = 1)

15.3.5.3 Bus Cycle Output

By setting the AM field in the CHCFG_n register to 010, the mode switches to bus cycle output. During a bus cycle, DACK output remains active. In addition, if it is the last DMA transfer, the TEND signal is output at the same timing as the DACK output during the bus cycle.
While the DACK/TEND signal is active, the DREQ signal is masked within the CPU. Therefore, if you set the DREQ signal to level detection, it is not necessary to deactivate the signal on the output side.

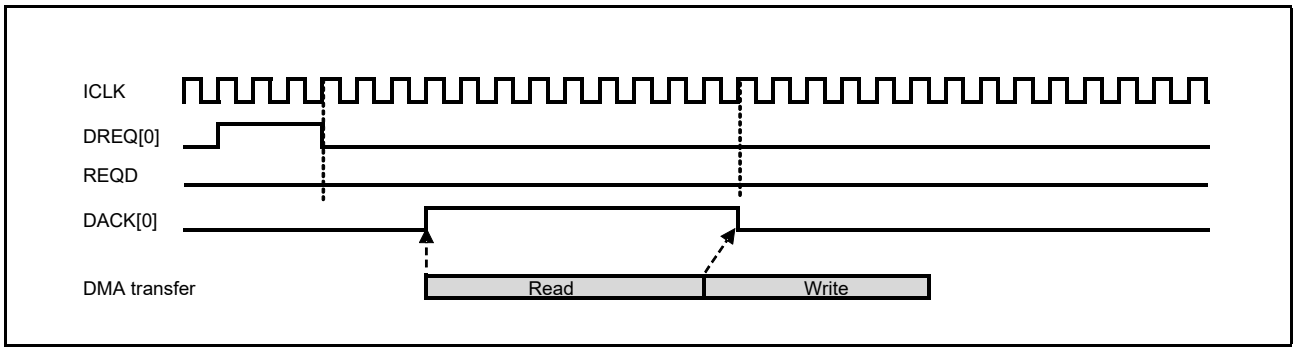


Figure 15.24 Bus Cycle Output Timing (REQD = 0)

- When the REQD bit in the CHCFG_n register = 0 (activated during read operation), DACK/TEND output remains active for the period from when a read request is output on a bus to when a cycle elapses after reading the last data.
- If DMA transfer request input is detected by level, DMA transfer request input is deactivated until the next cycle begins after a bus cycle ends.

The following signals trigger the rising and falling of DACK/TEND.

Rising: Starts a transfer.
Falling: Ends a transfer.

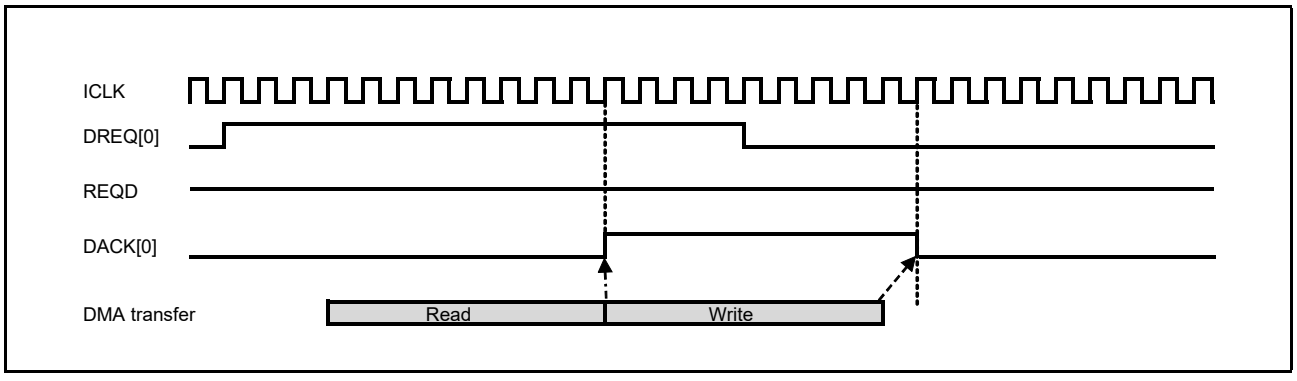


Figure 15.25 Bus Cycle Output Timing (REQD = 1)

- When the REQD bit in the CHCFG_n register = 1 (activated during write operation), the DACK/TEND signal remains active for the period from when a write request is output to when a clock (ICLK) elapses after responding to the last data.
- If DMA transfer request input is detected by level, DMA transfer request input is deactivated until the next cycle begins after a bus cycle ends.

The following signals trigger the rising and falling of DACK/TEND.

Rising: Starts a transfer.
Falling: Ends a transfer.

15.3.6 Forced Ejection Request

When a forced ejection request is input, data that is not yet transferred in a buffer is transferred to the DMA transfer destination address. After data is flushed, the DMA transfer resumes.

The following are notes on forced ejection requests:

- If a forced ejection request conflicts with DMA transfer request input, the forced ejection takes precedence, and then the DMA transfer is performed.

- For a system (the REQD bit in the CHCFG_n register = 1) in which the DMA transfer destination uses hardware requests through DMA transfer request input, the unit on the DMA transfer destination receives data even if the DMA transfer request is not activated. Therefore, a malfunction, such as buffer overflow, might occur. Because of this, when REQD =1, no forced ejection is performed by hardware.

- Differences from flush mode described in section 15.3.11.2, Aborting a Transfer (Buffer Flush: SBE = 1) (The EN bit is cleared to 0 when the SBE bit in the CHCFG_n register = 1).

Flush mode: DMAC stops operation after data in a buffer is written.
Forced ejection request: A DMA transfer continues after flush operation ends.

15.3.6.1 Software Forced Ejection Request

For software forced ejection requests, use the SETSSWPRQ bit in the CHCTRL_n register.
To request a forced ejection, set 1 to the SETSSWPRQ bit. DMAC outputs data in a buffer to the DMA transfer destination.

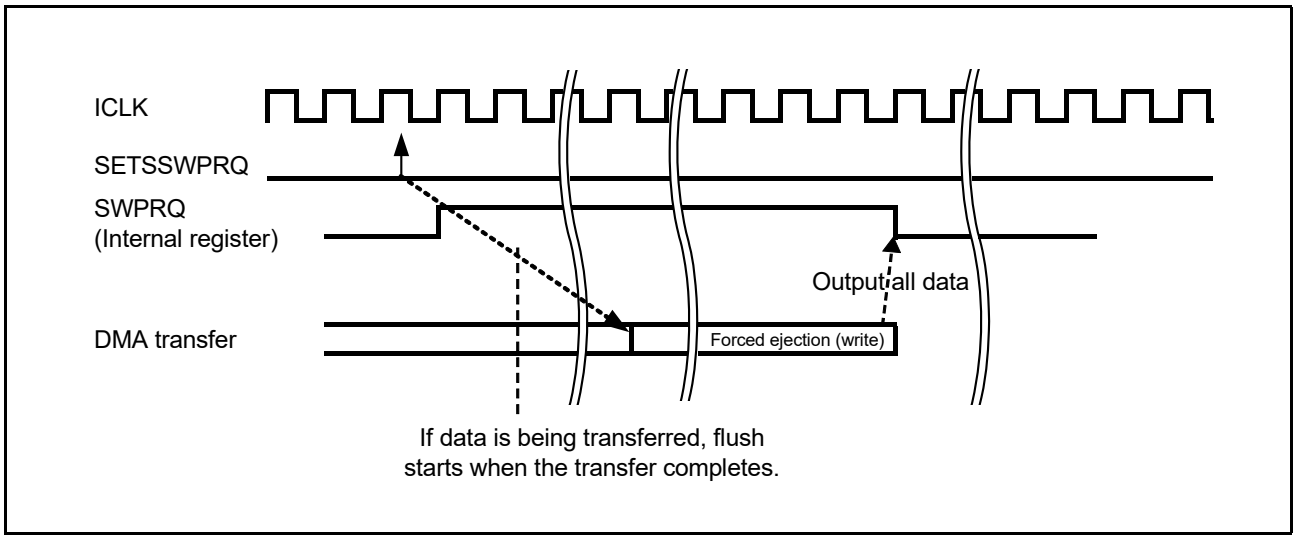


Figure 15.26 Software Forced Ejection Timing

15.3.7 Interval Count Function

By the setting for the ITVL field in the CHITVL_n register, the execution interval of DMA transfers can be adjusted. This function is used to avoid occupation of a bus by DMAC. Until the count value becomes 0, no DMA transfer for the next DMA request is performed.

The following figure provides an operation example.

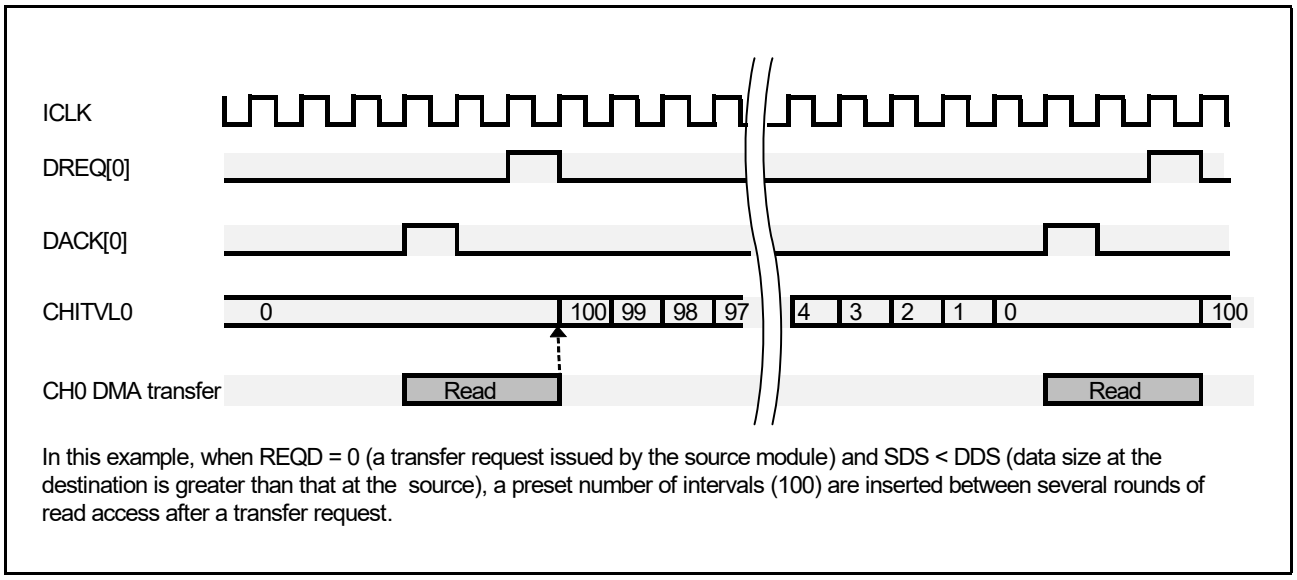


Figure 15.27 Interval Count (REQD = 0, SDS < DDS)

An interval is inserted after a transfer specified by the REQD bit in the CHCFG_n register.
The following figure shows the relationship between the setting values for the REQD, SDS, and DDS bits in the CHCFG_n register and the cycles to which intervals are applied.

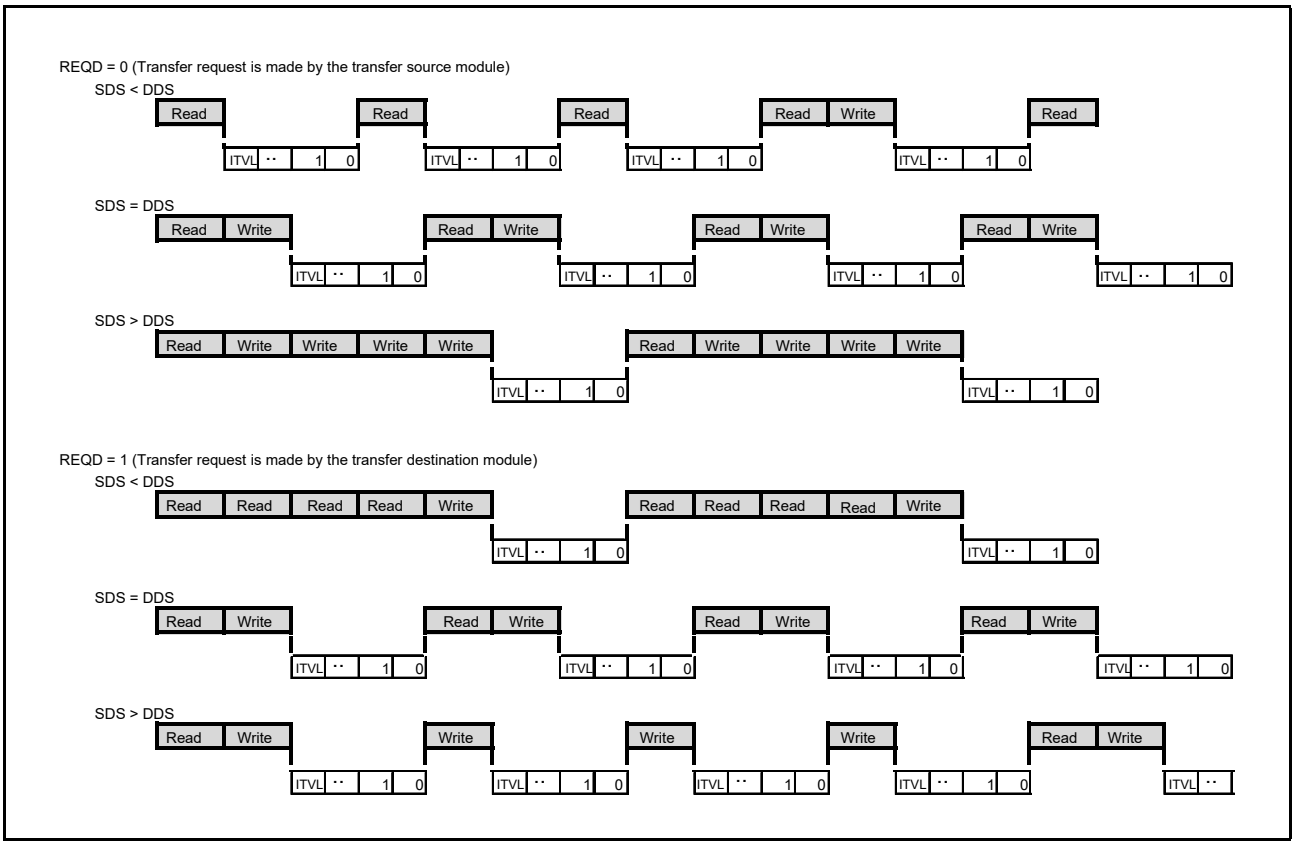


Figure 15.28 DMA Transfer Settings and Interval Counts

15.3.8 Differences in Operation According to the Transfer Data Size

15.3.8.1 When the Transfer Data Size on the Transfer Source is Small

As the transfer data size at the destination is large, reading from the source proceeds several times, and this is followed by writing to the destination.

The following figure shows the timing chart when the transfer source is 8 bits, and the transfer destination is 32 bits (SDS = 0 and DDS = 2 in the CHCFG_n register) for rising edge detection.

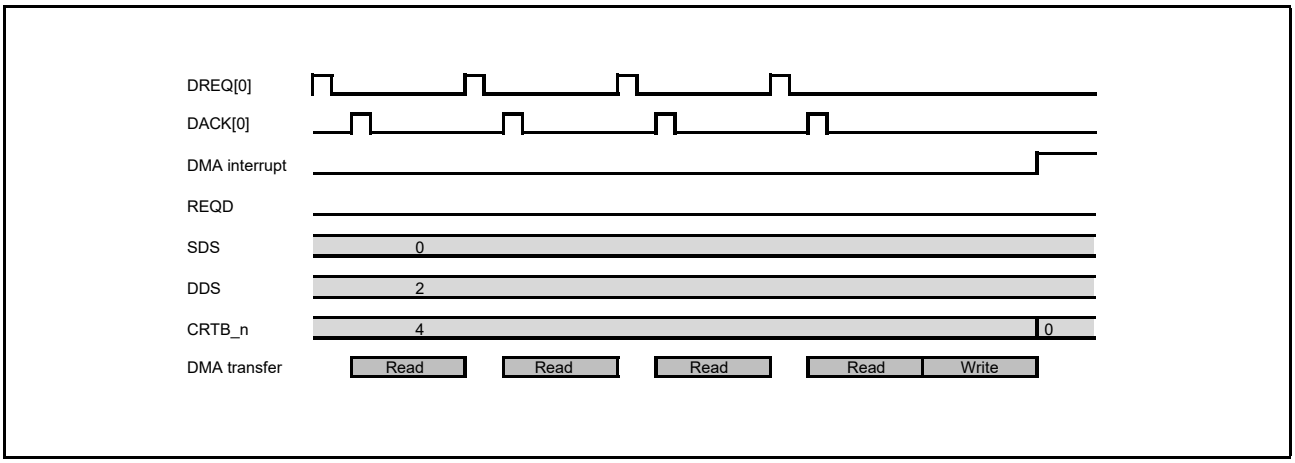


Figure 15.29 When the Size of Data on the Transfer Source is Small (LVL in CHCFGn = 0, HIEN = 1, REQD = 0, SDS < DDS)

15.3.8.2 When the Transfer Data Size on the Transfer Destination is Small

Because the transfer data size on the transfer source is large, after a single read operation, write operation to the transfer destination is performed a few times. The following figure shows the timing chart when the transfer source is 64 bits, and the transfer destination is 16 bits (SDS = 3 and DDS = 1 in the CHCFG_n register) for rising edge detection.

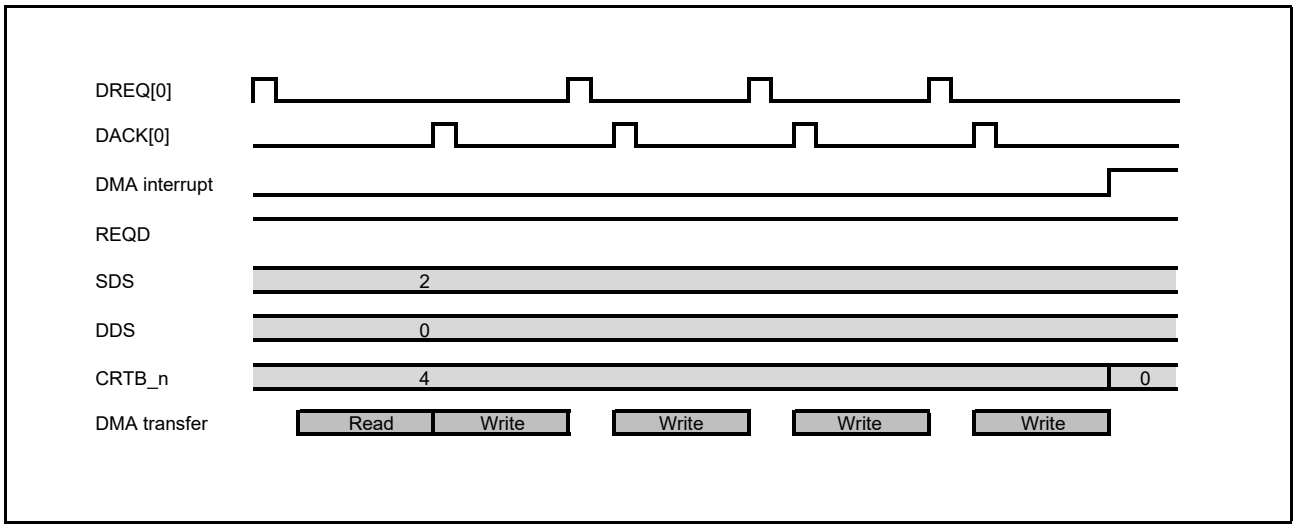


Figure 15.30 When the Size of Data on the Transfer Source is Small (LVL = 0, HIEN = 1, REQD = 1, and SDS > DDS in CHCFG_n)

15.3.8.3 When the Size of Transfer Data on the Transfer Destination and on the Transfer Destination is the Same

Every time a DMA transfer request is detected, read operation is performed on the transfer source, and write operation is performed on the transfer destination.
The following figure shows the timing chart when the transfer source and the transfer destination are 8 bits (SDS = 0 and DDS = 0 in the CHCFG_n register) for rising edge detection.

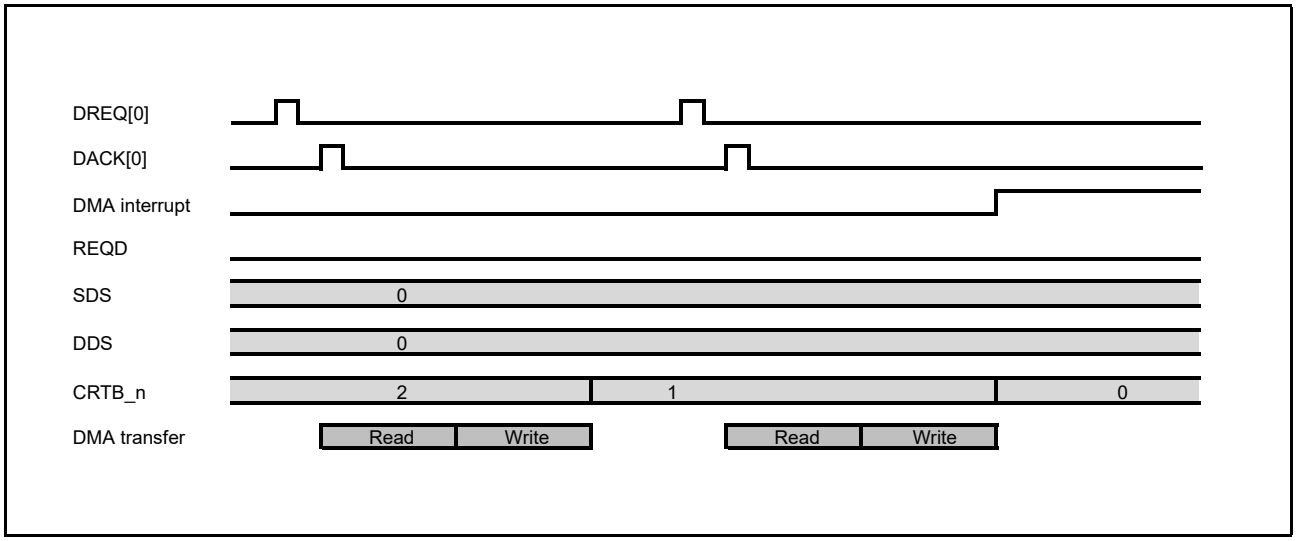


Figure 15.31 When the Sizes of Data on the Transfer Source and the Transfer Destination are the Same (LVL = 0, HIEN = 1, REQD = 0, and SDS = DDS in CHCFG_n)

15.3.9 DMA Transfer Status

The CHSTAT_n register indicates the DMA transfer status of each channel.
The TACT bit in the CHSTAT_n register indicates that DMA operation is being performed on channel n. Writing 1 to the SETEN bit in the CHCTRL_n register sets 1. The TACT bit remains 1 while accessing a descriptor, or waiting for a DMA request.
The TACT bit is cleared when the EN bit in the CHSTAT_n register is cleared (for details on clear conditions, see section 15.2.7, Channel Status Register n (CHSTAT_n)), and DMA transfers for the set number of times are finished.
The TACT bit is not cleared even when a DMA transfer finishes, but the EN bit is not cleared (when the REN bit in the CHCFG_n register = 1 in register mode, or the next descriptor access is performed in link mode).

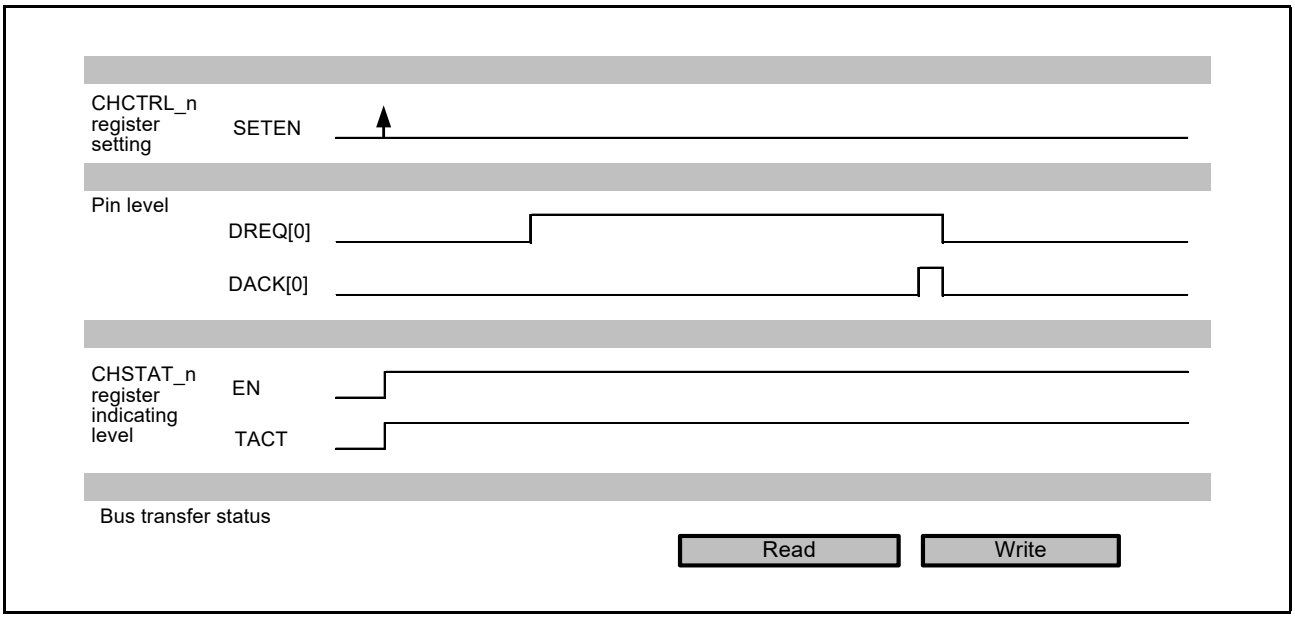


Figure 15.32 DMAC Status Example 1 (Hardware Request)

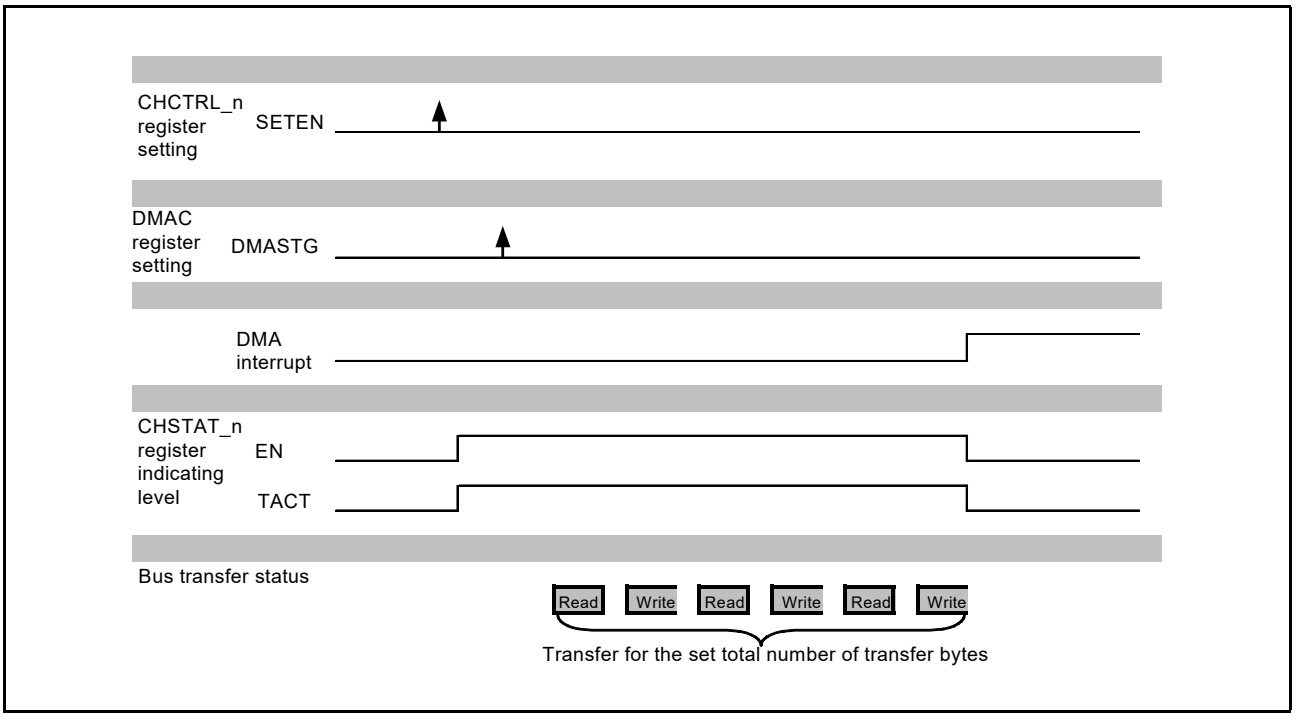


Figure 15.33 DMAC Status Example 2 (Software Request)

15.3.10 Suspending a Transfer

You can suspend a DMA transfer at the SETSUS bit in the CHCTRL_n register. At that time, if there is an already running bus cycle, waits for the cycle to end, and then suspends the transfer. Writing 1 to the CLRSUS bit in the CHCTRL_n register resumes from the suspended state.

To check if the transfer is suspended, set the SETSUS bit in the CHCTRL_n register, and then make sure that the SUS bit in the CHSTAT_n register, or the SUS bit in the DST_SUS register on the applicable channel is set to 1.

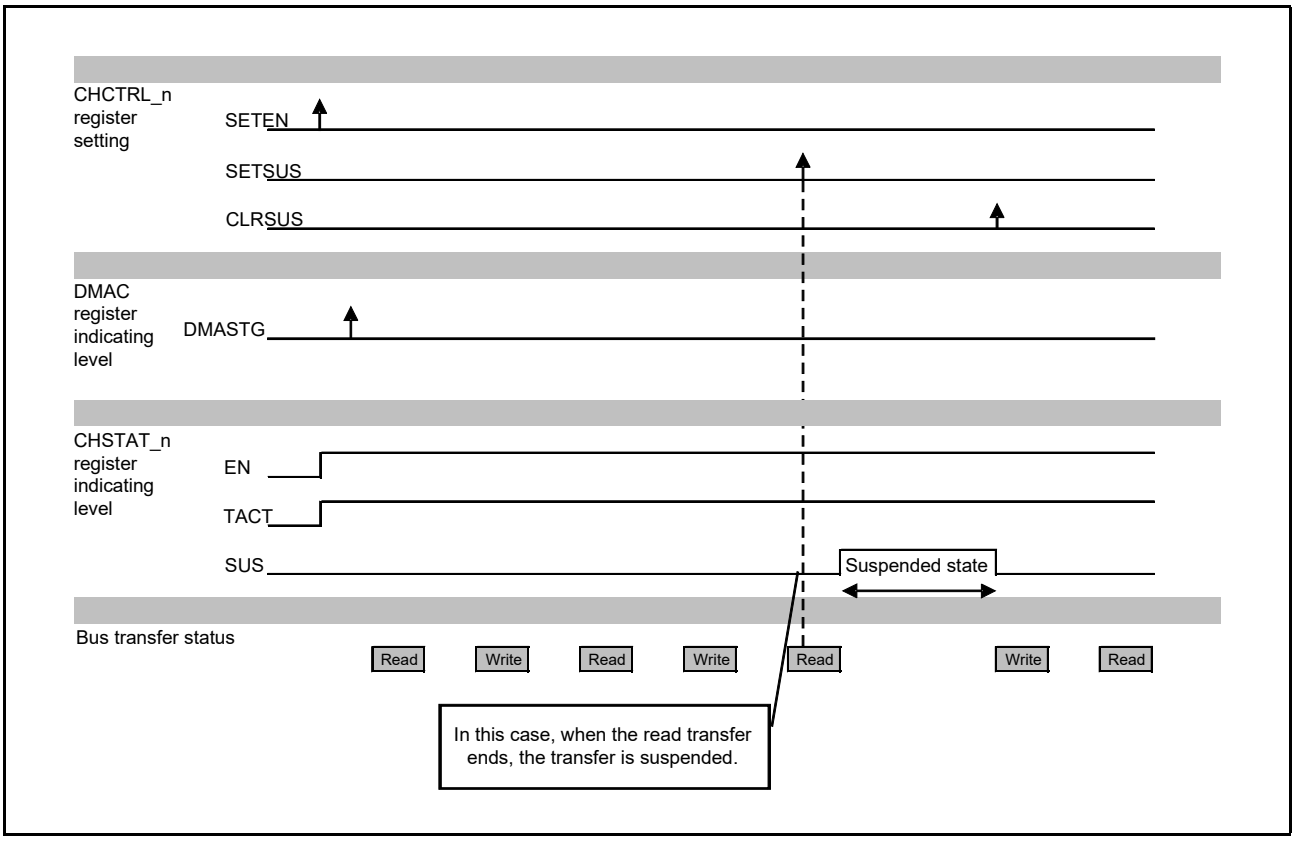


Figure 15.34 DMAC Suspended State (Software Request Block Transfer)

15.3.11 Aborting a Transfer

During a DMA transfer, if you write 1 to the CLREN bit in the CHCTRL_n register, you can abort the DMA transfer of the channel. As processing after aborting the transfer, you can use the SBE bit in the CHCFG_n register to determine whether to flush data remaining in a buffer when a transfer is suspended. By default, SBE = 0 (do not flush data) is selected.
When this mode (flush data) is activated, if a transfer which is being performed when the CLREN bit in the CHCTRL_n register = 1 is aborted, data remaining in the buffer of DMAC is flushed, and the operation stops.

15.3.11.1 Aborting a Transfer (No Buffer Flush: SBE = 0)

During a DMA transfer, if you write 1 to the CLREN bit in the CHCTRL_n register, you can abort and then stop the DMA transfer. The timing to stop the transfer depends on the value set for the REQD bit. After the transfer stops, write 1 to the SWRST bit in the CHCTRL_n register, and clear the contents within the DMAC before setting the next transfer.

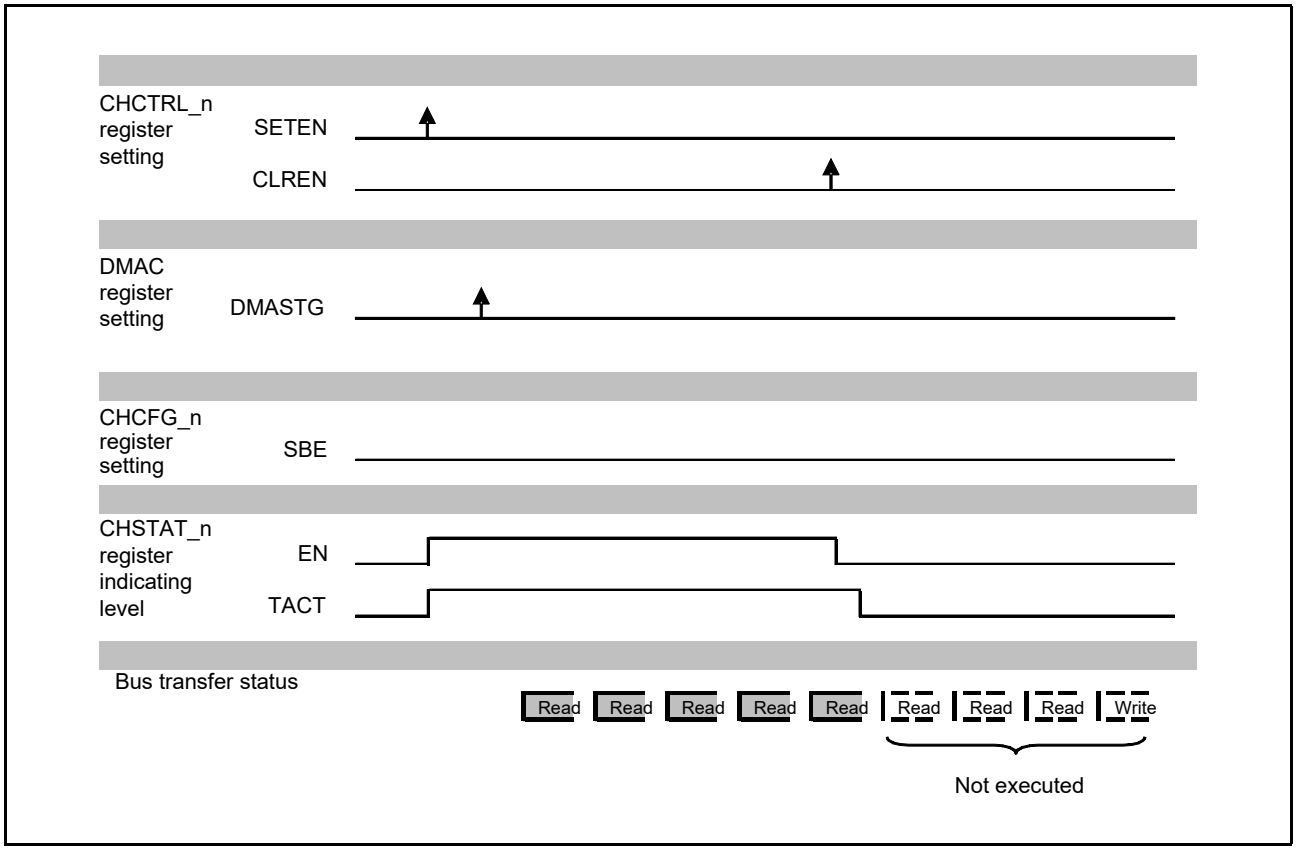


Figure 15.35 Aborting a DMA Transfer

- When the TACT bit in the CHSTAT_n register is cleared, you can confirm that the channel stops completely.
- If a DMA transfer is aborted, no DMA transfer completion interrupt is generated.
- When the REQD bit in the CHCFG_n register = 0, the transfer stops when the next read operation completes (Note that if there is data that can be written in the buffer, the transfer stops after the data is written).
- When the REQD bit in the CHCFG_n register = 1, the transfer stops when the next write operation completes.

15.3.11.2 Aborting a Transfer (Buffer Flush: SBE = 1)

During a DMA transfer, if you write 1 to the CLREN bit in the CHCTRL_n register, you can abort the DMA transfer. When the REQD bit in the CHCFG_n register = 0, already read data is flushed (written), and then the DMA transfer stops. When REQD = 1, flush mode cannot be used.
After the transfer stops, set the SWRST bit in the CHCTRL_n register, and clear the contents within the DMAC before setting the next transfer.

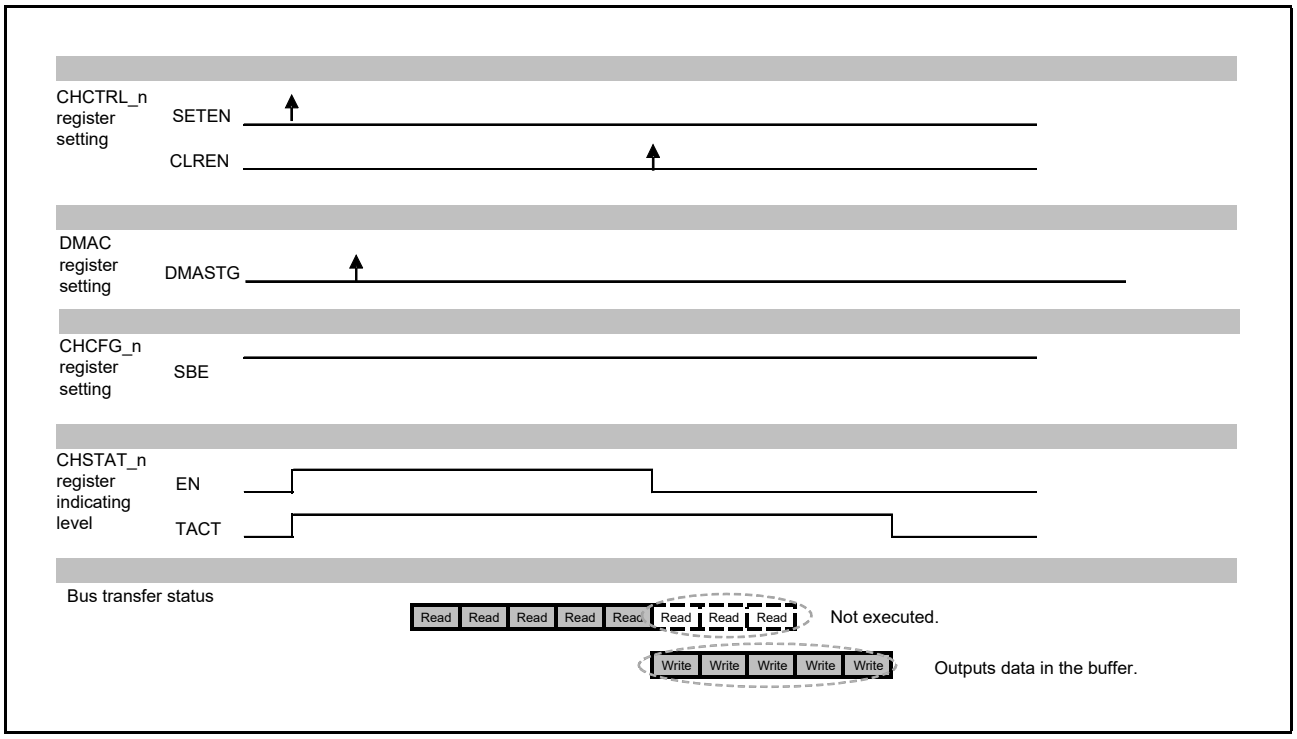


Figure 15.36 Aborting DMA Transfer (Buffer Flush Mode)

- The above figure shows an example when 1 is written to the CLREN bit in the CHCTRL_n register during the fifth read transfer in flush mode (the SBE bit in the CHCFG_n register = 1), and the transfer is aborted. It illustrates how read data is written, and the DMA transfer stops.
- When the TACT bit in the CHSTAT_n register is cleared to 0, you can confirm that the channel stops completely.

15.3.11.3 Checking If the Channel Stops

When 1 is written to the CLREN bit in the CHCTRL_n register, and the EN bit in the CHSTAT_n register is cleared to 0, if a transfer is already performed on a bus, DMAC cannot stop immediately. To check if DMA stops completely, make sure that the EN bit is cleared to 0, and the TACT bit in the CHSTAT_n register is cleared to 0.

15.3.11.4 Procedure for Aborting a Transfer

The following is the procedure for stopping a transfer:

1. Write 1 to the CLREN bit in the CHCTRL_n register.
2. When the SBE bit in the CHCFG_n register = 0, the transfer stops according to value for the REQD bit in the CHCFG_n register. At that time, if SBE = 1, flush mode is used.
3. By reading the CHSTAT_n register, make sure the TACT bit is cleared to 0. When TACT = 0, DMA stops completely. When TACT = 1, perform polling until the TACT bit is cleared to 0.
4. After a transfer is aborted, if you want to perform the next DMA transfer, you must set the SWRST (software reset) bit in the CHCTRL_n register immediately before the next transfer starts.

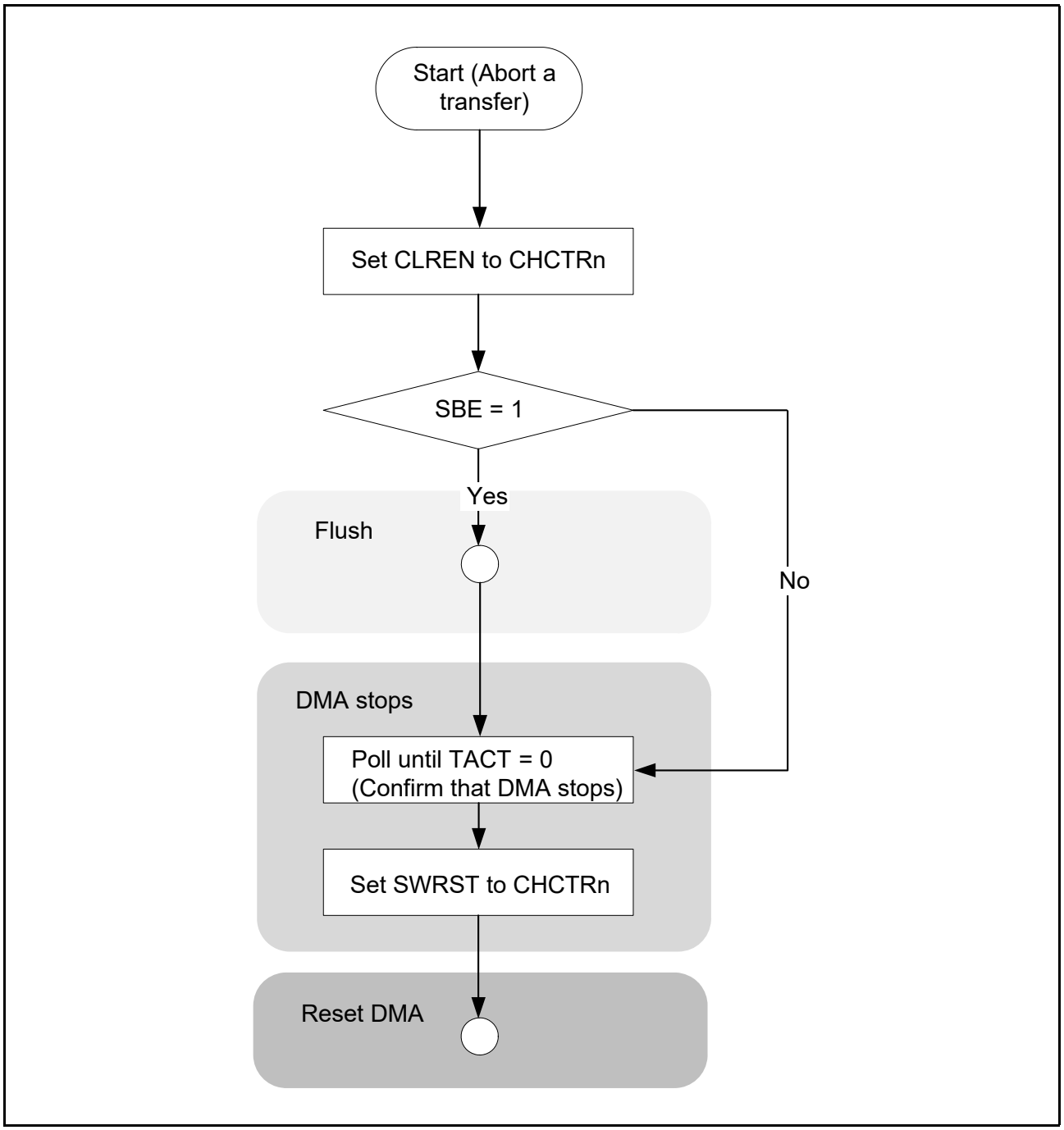


Figure 15.37 Operation Flow of Aborting a Transfer

15.4 Interrupts

15.4.1 Interrupt Sources

DMAC has two types of interrupt sources, such as DMA transfer completion interrupts and DMA error interrupts for each channel.
Table 15.23 shows the relationship among interrupt sources, enable bits, and status flags.

Table 15.23 Interrupt Sources of DMAC

Interrupt Source		Interrupt Enable Bit	Interrupt Status Flag	Output Condition
DMA transfer completion interrupt	DMA transfer completion	CHCFG_n.DEM	CHSTAT_n.END	When a transfer for the total number of transfer bytes loaded to the CRTB_n register completes (after a write back if write back is performed in link mode)
	Descriptor invalid	CHCFG_n.DIM		In link mode, when the DRRP and DIM bits in the CHCFG_n register = 0, and header of the read descriptor's LV = 0
DMA error interrupt		— (Mask disabled)	CHSTAT_n.ER	When a bus error occurs during a DMA transfer and descriptor access

15.4.2 DMA Transfer Completion Interrupts

A DMA transfer completion interrupt is an interrupt request signal indicating that the DMA transfer completes.
Each bit of the DMA transfer completion interrupt corresponds to each channel.

When the transfer of the total number of bytes for transfer loaded to the CRTB_n register is completed, the END bit in the CHSTAT_n register is set to 1. At that time, if the DEM bit in the CHCFG_n register = 0, a DMA transfer completion interrupt is generated (n = 15 to 0). To perform write back in link mode, an interrupt is generated after the write back.

In addition, when the DRRP bit in the CHCFG_n register = 0 in link mode, and header of the read descriptor is LV = 0, the DER bit in the CHSTAT_n register is set to 1. At that time, if the DIM bit in the CHCFG_n register = 0, a DMA transfer completion interrupt is generated.

Note: Instead of an interrupt source from peripheral modules, transfer completion sources of DMAC channels selected by the DMAC source select register are connected to the vector number selected by the DMAC source select registers (DMA0SELi, DMA1SELi). (The vector number selected by the DMA source selection register is handled as the vector number of the DMA transfer completed interrupt.)

Note: Be sure to select edge detection with the PLSn register as the transfer completed interrupt detection type for the DMAC.

For details, see section 12.3.1, Selecting Interrupt Request Destinations.

15.4.3 DMA Error Interrupt

If a bus error occurs during a DMA transfer or descriptor access, this module determines an error occurred, and stops the transfer. When a bus error occurs, the EN bit in the CHSTAT_n register for channel n where a transfer is performed is cleared to 0, and the ER bit is set to 1 (n = 15 to 0). In addition, a DMA error interrupt is generated.
DMA error interrupts cannot be masked.

Data for a series of error transfers cannot be guaranteed. You must perform the transfer from the beginning by using the following procedure.

1. Set the SWRST bit in the CHCTRL_n register to 1.
2. Set each register again.

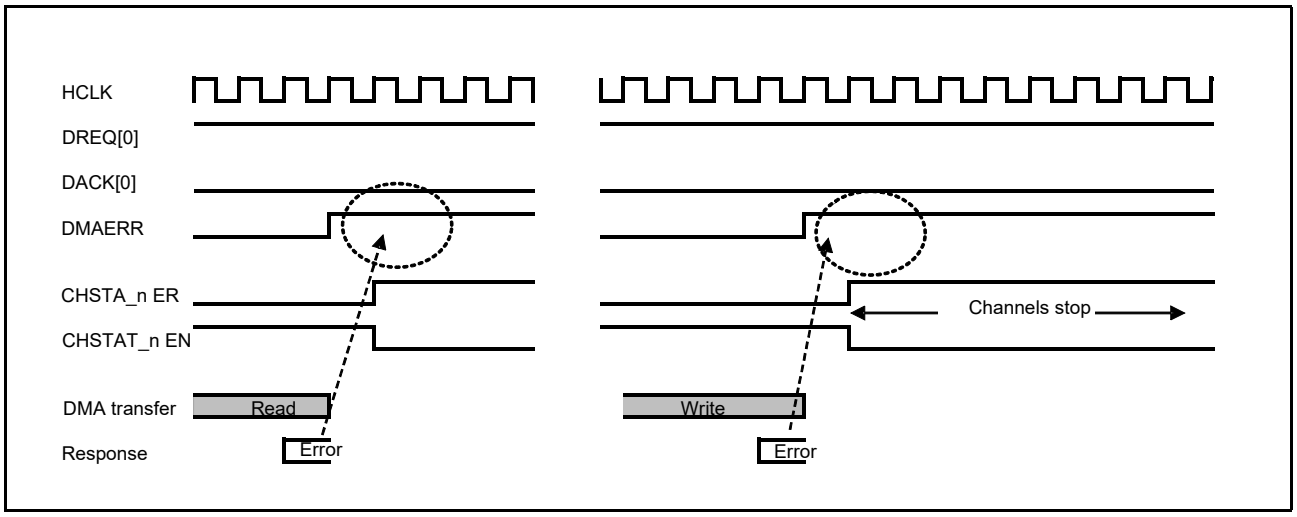


Figure 15.38 Stop Timing for Responding to a Bus Error

Note: When the CPU accesses a register of DMAC, if a bus error occurs, no DMA error interrupt is generated.

15.5 DMA Setting Examples

This section provides examples of DMA transfers. The following table lists the transfer conditions for the setting examples described in this section.

Table 15.24 List of Transfer Conditions for the DMA Transfer Setting Examples

Setting Example	DMA Mode	Transfer Mode	Transfer Request
Setting example 1	Register mode	Single transfer mode	Hardware
Setting example 2	Register mode	Block transfer mode	Software
Setting example 3	Register mode (continuous execution)	Block transfer mode	Software
Setting example 4	Link mode	Block transfer mode	Software

15.5.1 Setting Example 1 (Register Hardware Request)

This subsection provides setting examples of DMA transfers that use hardware requests in register mode.

Table 15.25 DMA Transfer Setting Example 1

Item		Description	
Channel to use		DMAC0 channel 3	
Priority control		Fixed priority	
DMA mode		Register mode	
Transfer mode		Single transfer mode	
Register set to use		Next0 register set	
Transfer source/transfer destination		**Transfer source**	**Transfer destination**
	Start address	6000 0000h	2000 0000h
	Address direction	Increment	Increment
	Data size	32 bits	32 bits
Number of DMA transfer bytes		64 bytes	
DMA transfer request		Detects the rising edge by hardware (DREQ0).	
Selection of the side which makes a DMA transfer request		Requested from the transfer-side module.	
DACK/TEND signal		Outputs by level during read operation.	
DMA transfer completion interrupt output mask		None	

Setting Example 1
N0SA = 6000 0000h (Transfer source address)
N0D = 2000 0000h (Transfer destination address)
N0TB = 0000 0040h (Number of transfer bytes)

CHCFG = 0002 2123h (Configuration)
CHITVL = 0000 0000h (Interval)

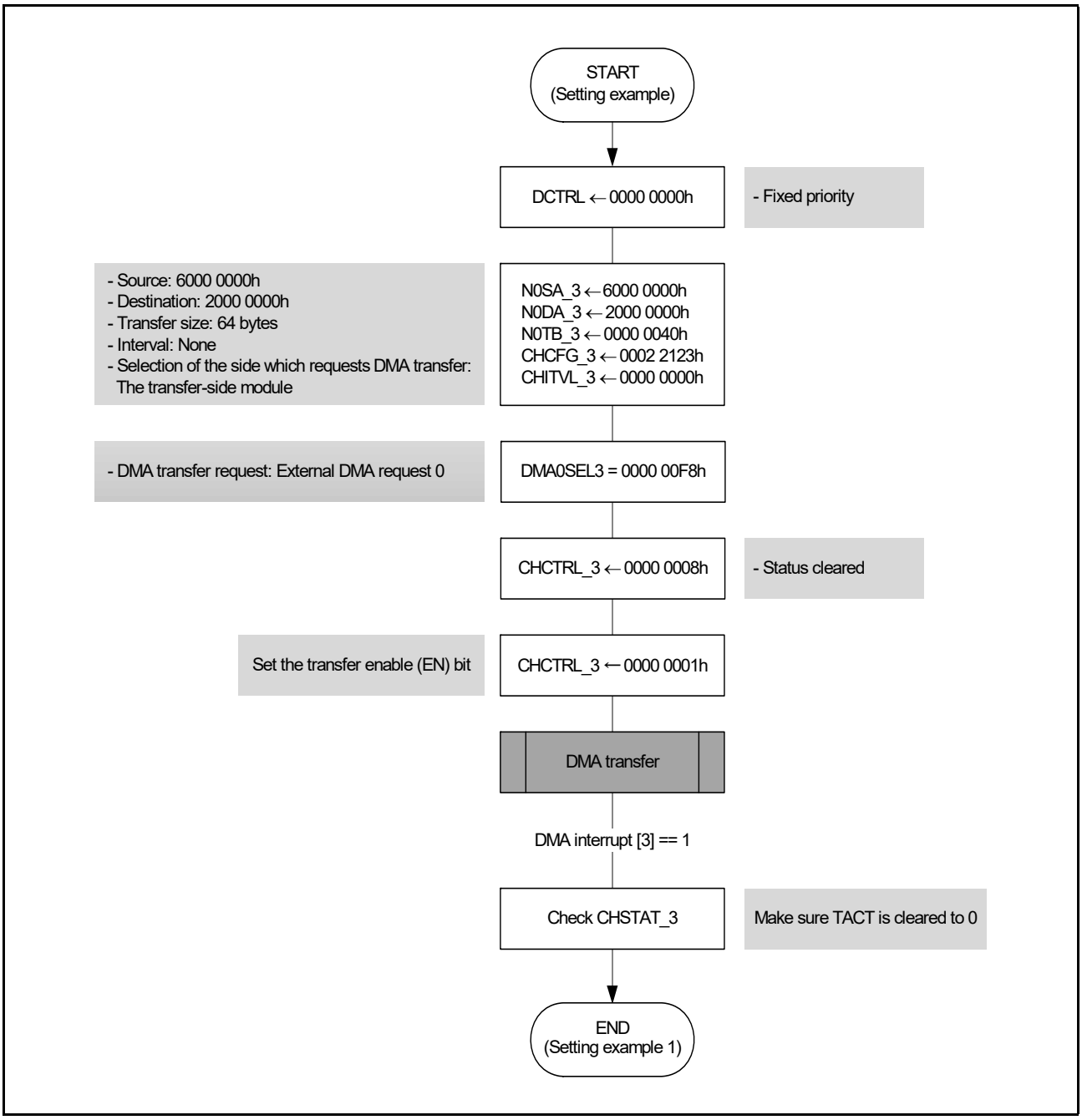


Figure 15.39 Setting Example 1

Note: DMA interrupt [3] indicates the interrupt source assigned to serve as the trigger for DMA transfer on channel 3.

15.5.2 Setting Example 2 (Register Mode Software Request)

This subsection provides a setting example of DMA transfers that use software requests in register mode.

Table 15.26 DMA Transfer Setting Example 2

Item		Description	
Channel to use		DMAC0 channel 2	
Priority control		Round-robin	
DMA mode		Register mode	
Transfer mode		Block transfer mode	
Register set to use		Next1 register set	
Transfer source/transfer destination		Transfer source	Transfer destination
	Start address	0400 0000h	2000 0000h
	Address direction	Increment	Increment
	Data size	8 bits	256 bits
Number of DMA transfer bytes		128 bytes	
DMA transfer request		Software request	
DACK/TEND signal		Mask	
DMA transfer completion interrupt output mask		None	

Setting Example 2
DCTRL = 0000 0001h (DMA setting)

N1SA = 0400 0000h (Transfer source address)
N1DA = 2000 0000h (Transfer destination address)
N1TB = 0000 0080h (Number of transfer bytes)

CHCFG = 1045 0222h (Configuration)
CHITVL = 0000 0000h (Interval)

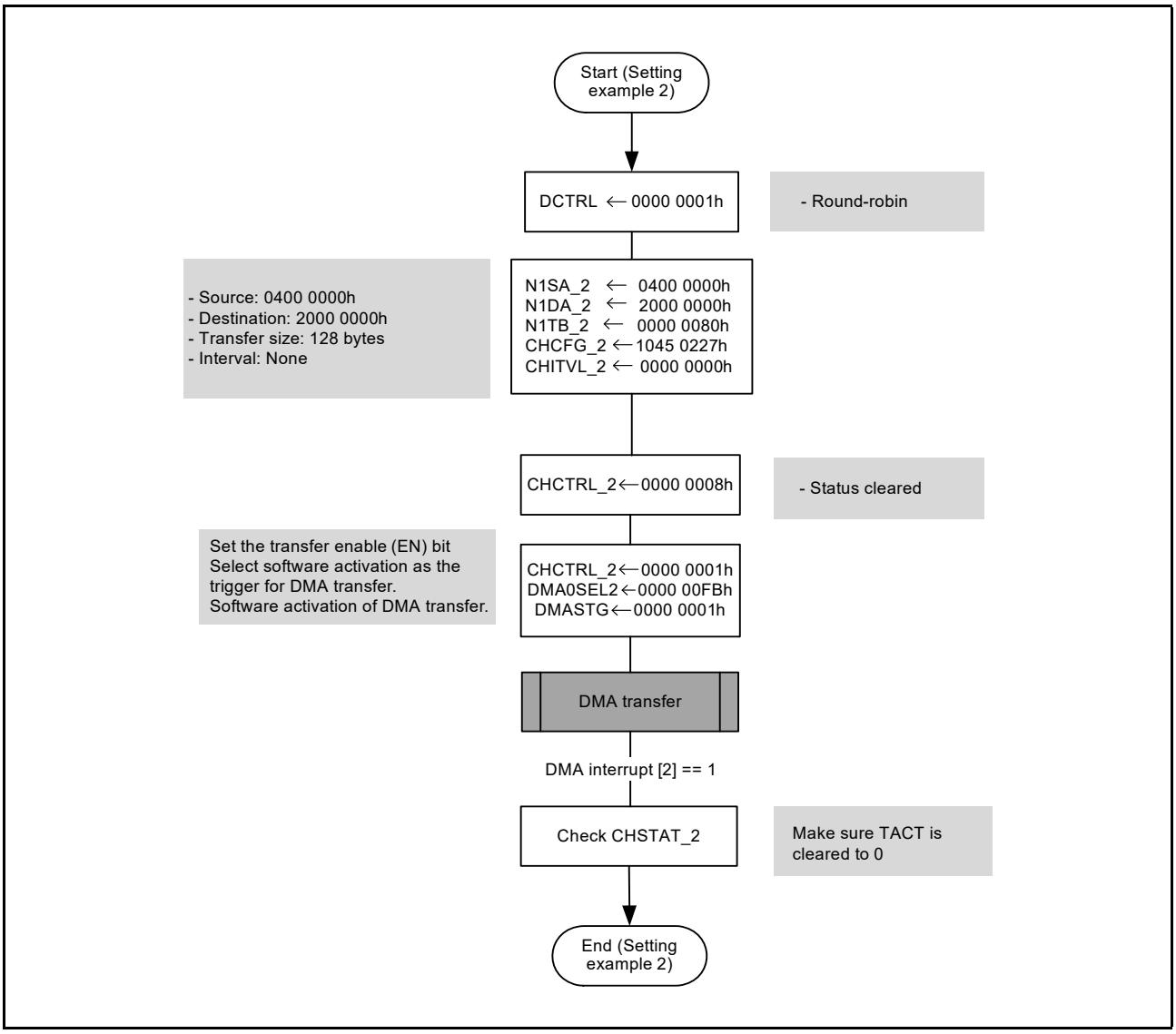


Figure 15.40 Setting Example 2

Note: DMA interrupt [2] indicates the interrupt source assigned to serve as the trigger for DMA transfer on channel 2.

15.5.3 Setting Example 3 (Register Mode Continuous Execution)

This subsection provides a setting example of DMA transfers that use Next0/1 Register Sets in series in register mode.

Table 15.27 DMA Transfer Setting Example 3

Item		Description	
Channel to use		DMAC0 channel 1	
Priority control		Round-robin	
DMA mode		Register mode	
Transfer mode		Block transfer mode	
Register set to use		Next0 register set -> Next1 register set in series	
Transfer source/transfer destination (Next0)		Transfer source	Transfer destination
	Start address	1111 0000h	2000 0000h
	Address direction	Fixed	Fixed
	Data size	32 bits	512 bits
	Number of DMA transfer bytes	512 bytes	
Transfer source/transfer destination (Next1)		Transfer source	Transfer destination
	Start address	0400 0000h	1000 0000h
	Address direction	Fixed	Fixed
	Data size	32 bits	512 bits
	Number of DMA transfer bytes	2,048 bytes	
DMA transfer request		Software request	
DACK/TEND signal		Mask	
DMA transfer completion interrupt output mask		Masks when Next0 completes.	

Setting Example 3
DCTR = 0000 0001h (DMA setting)

N0SA = 1111 0000h (Transfer source address)
N0DA = 2000 0000h (Transfer destination address)
N0TB = 0000 0200h (Number of transfer bytes)

N1SA = 0400 0000h (Transfer source address)
N1DA = 1000 0000h (Transfer destination address)
N1TB = 0000 0800h (Number of transfer bytes)

CHCFG = 6176 2007h (Configuration)
CHITVL = 0000 0000h (Interval)

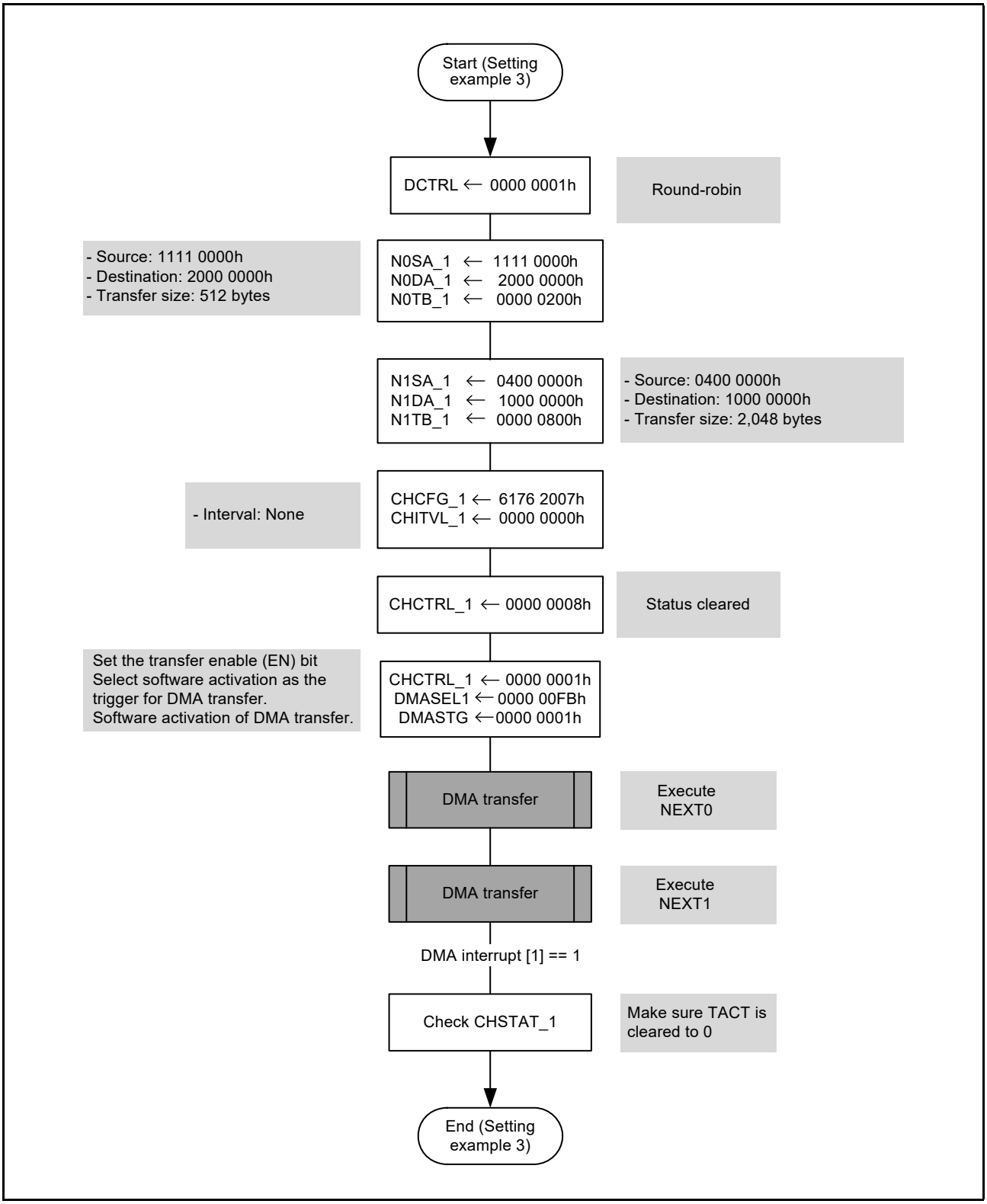


Figure 15.41 Setting Example 3

Note: DMA interrupt [1] indicates the interrupt source assigned to serve as the trigger for DMA transfer on channel 1.

15.5.4 Setting Example 4 (Link Mode)

This subsection provides a setting example when a DMA transfer is performed in link mode.

Table 15.28 DMA Transfer Setting Example 4

Item	Description
Channel to use	DMAC0 channel 0
Priority control	Round-robin
DMA mode	Link mode
Transfer mode	Block transfer mode
Descriptor start address	0080 0000h

Table 15.29 DMA Transfer Setting Example 4 (Descriptor 1)

Item		Description	
Descriptor start address		0080 0000h	
Next descriptor start address		0080 1000h	
Transfer mode		Block transfer mode	
Transfer source/transfer destination		Transfer source	Transfer destination
	Start address	1111 0000h	2000 0000h
	Address direction	Increment	Increment
	Data size	32 bits	32 bits
Number of DMA transfer bytes		2,048 bytes	
DMA transfer request		Software request	
DACK/TEND signal		Mask	
DMA transfer completion interrupt output mask		Masks when a DMA transfer on descriptor 1 completes.	
Descriptor format		1 (8 words)	
Descriptor header			
	Write back of the LV bit	Enable (WBD = 0)	
	Next link destination	Available (LE = 0)	
	Descriptor enabled	Enabled (LV = 1)	

Table 15.30 DMA Transfer Setting Example 4 (Descriptor 2)

Item		Item	
Descriptor start address		0080 1000h	
Next descriptor start address		0080 2000h	
Transfer mode		Block transfer mode	
Transfer source/transfer destination		Transfer source	Transfer destination
	Start address	0400 0000h	2000 0000h
	Address direction	Increment	Increment
	Data size	256 bits	256 bits
Number of DMA transfer bytes		1,024 bytes	
DMA transfer request		Software request	
DACK/TEND signal		Mask	
DMA transfer completion interrupt output mask		Masks when a DMA transfer on descriptor 2 completes.	
Descriptor format		1 (8 words)	
Descriptor header			
	Write back of the LV bit	Enable (WBD = 0)	
	Next link destination	Available (LE = 0)	
	Descriptor enabled	Enabled (LV = 1)	

Table 15.31 DMA Transfer Setting Example 4 (Descriptor 3)

Item		Item	
Descriptor start address		0080 2000h	
Next descriptor start address		—	
Transfer mode		Block transfer mode	
Transfer source/transfer destination		Transfer source	Transfer destination
	Start address	2000 0000h	0800 2000h
	Address direction	Increment	Increment
	Data size	512 bits	512 bits
Number of DMA transfer bytes		4,096 bytes	
DMA transfer request		Software request	
DACK/TEND signal		Mask	
DMA transfer completion interrupt output mask		Do not mask.	
Descriptor format		1 (8 words)	
Descriptor header			
	Write back of the LV bit	Enable (WBD = 0)	
	Next link destination	None (LE = 1)	
	Descriptor enabled	Enabled (LV = 1)	

Setting Example 4

DCTRL = 0000 0001h (DMA setting)

NXLA = 0080 0000h (Descriptor start address)

CHCFG = 8000 0000h (Configuration)

Table 15.32 Descriptor Settings

Item	Descriptor 1	Descriptor 2	Descriptor 3
Header	1100 0000h	1100 0000h	1300 0000h
SA (Source Address)	1111 0000h	0400 0000h	2000 0000h
DA (Destination Address)	2000 0000h	2000 0000h	0800 2000h
TB (Transaction Bytes)	0000 0800h	0000 0400h	0000 1000h
CFG (Configuration)	8142 2220h	8145 5220h	8046 6220h
ITVL (Interval)	0000 0000h	0000 0000h	0000 0000h
EXT (Extension)	0000 0000h	0000 0000h	0000 0000h
NXLA (Next Link Address)	0080 1000h	0080 2000h	0000 0000h

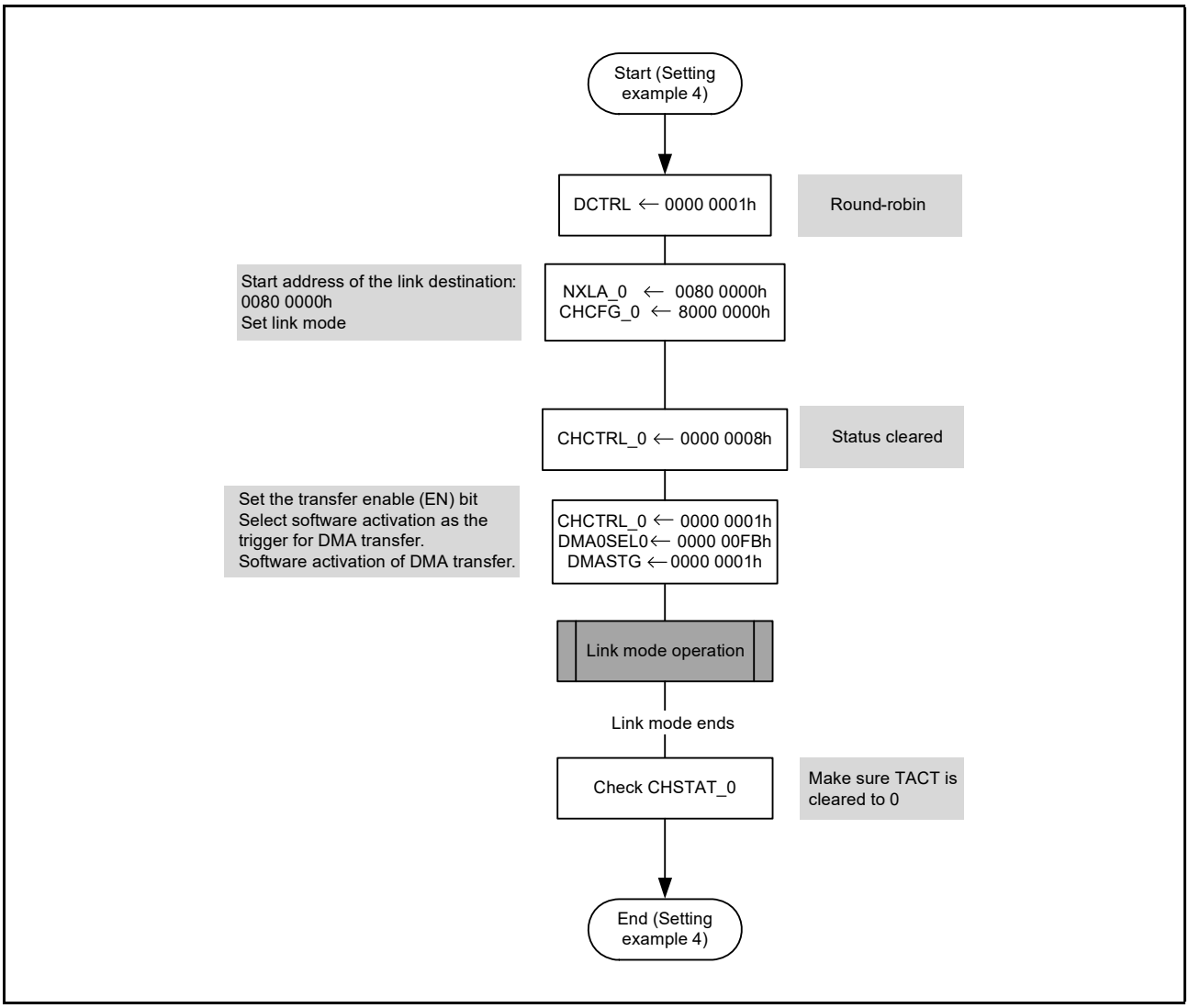


Figure 15.42 Setting Example 4

15.5.5 Next Register Continuous Execution Settings

The following figure shows a flow chart when using two Next register sets to continue DMA transfers in register mode. While performing a DMA transfer of a Next register, set the other Next register, and perform the DMA transfers in series.

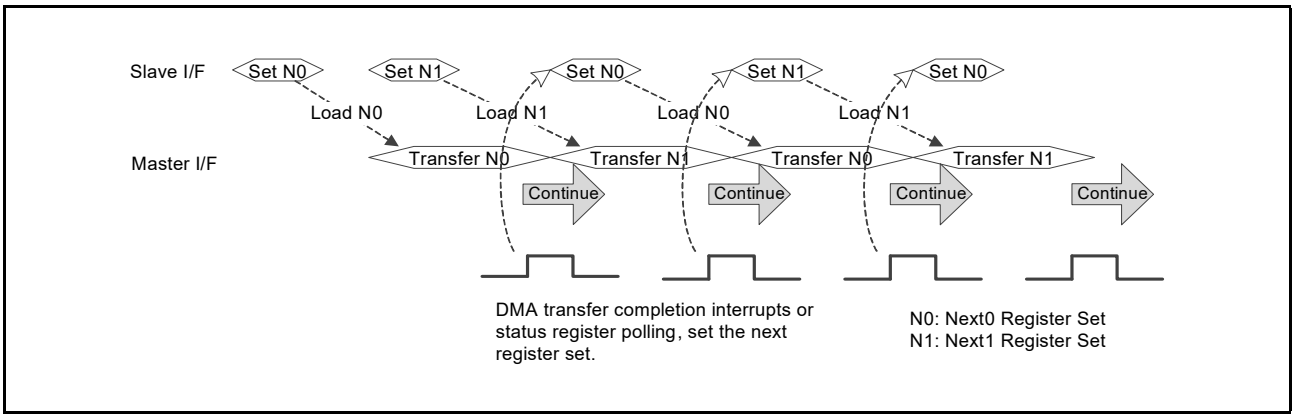


Figure 15.43 Next Register Continuous Execution Setting Image

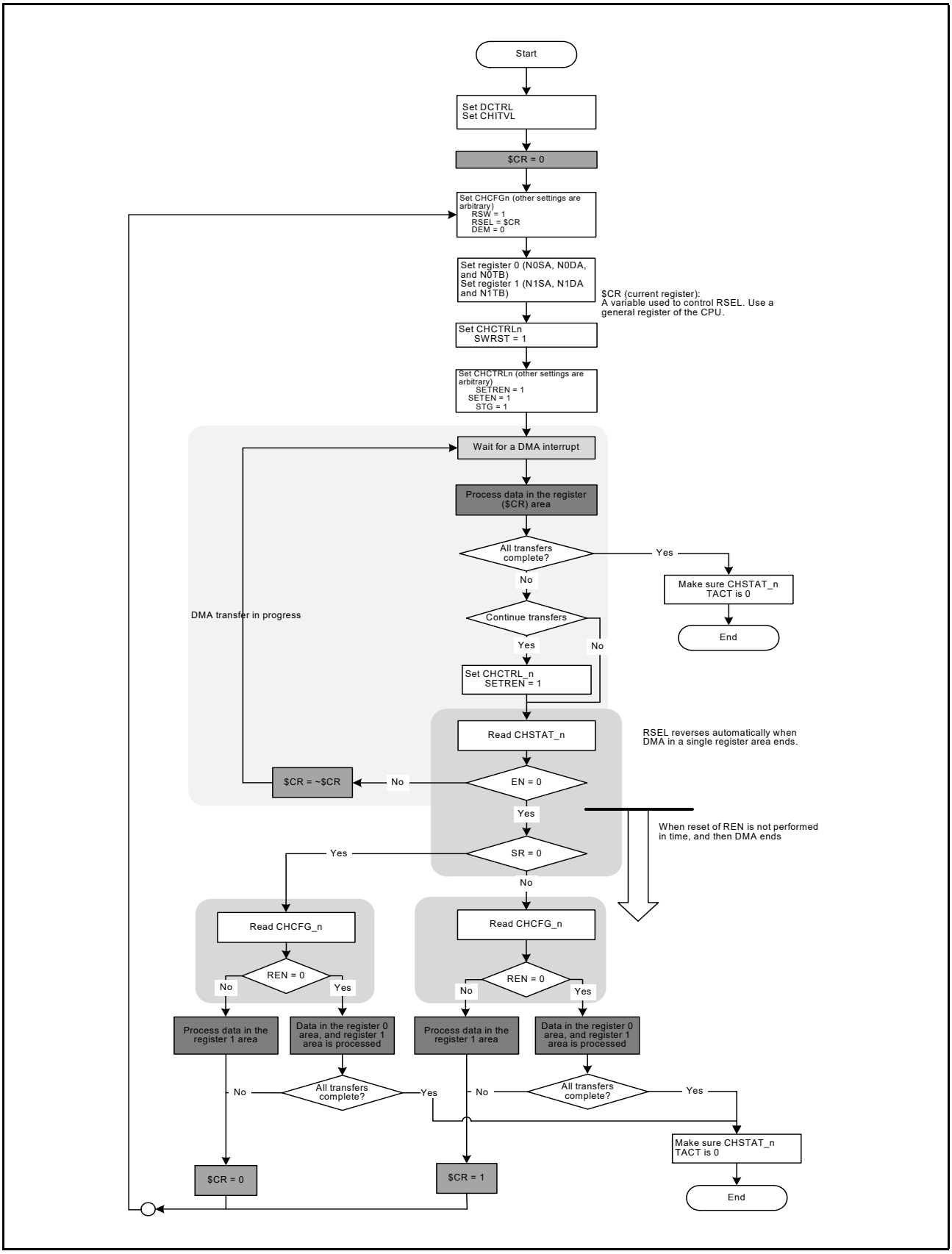


Figure 15.44 Setting Example of Next Register Continuous Execution

- Supplementary information:
  Save the register sets 0 (N0SA_n, N0DA_n, and N0TB_n registers) and 1 (N1SA_n, N1DA_n, and N1TB_n registers) in a general register (call this register value $CR for convenience).
  Every time a DMA transfer of a register set completes (a DMA transfer completion interrupt is generated), the REN bit in the CHCFG_n register is cleared to 0 automatically. To perform transfers in series, write 1 to the SETREN bit in the CHCTR_n register. By doing so, the REN bit in the CHCFG_n register is also set.

  In this mode, two Next registers are executed in series. However, if the SETREN bit is not set before a DMA transfer completes (before the next DMA transfer completion interrupt is generated), the continuous execution stops. In this case, by reading the SR and EN bits in the CHSTAT_n register, and the REN bit in the CHCFG_n register, you can check how far the transfer is performed. To resume the transfer, perform the procedure described in the above flow chart.

15.6 Usage Notes

This subsection provides notes on this module.

- When a transfer of which source and destination are in the same, or partially shared area is performed, consistency of data cannot be guaranteed. Therefore, do not perform a transfer of which source and destination address areas overlap.

- When DAD = 1 (fixed transfer source address), no skip transfer can be performed on the transfer destination. If a transfer is performed with this setting, operation cannot be guaranteed. Do not perform this type of transfers.

- When SAD = 1 (fixed transfer source address), no skip transfer can be performed on the transfer source. If a transfer is performed with this setting, operation cannot be guaranteed. Do not perform this type of transfers.

- For hardware activation, if REQD = 1 (the transfer destination issues a hardware request), SBE = 1 (flush mode) and the forced ejection function cannot be used. The transfer is deactivated by hardware.

- Since access to the region from A00E 0000h to A010 0000h within the peripheral I/O register region is not supported, locations or ranges within this region should never be set as sources or destinations for transfer.

15.6.1 When the DACK and TEND Signals Are Divided and Output

When four-byte or more data is transferred to an 8-bit or 16-bit external device, or two-byte or more data is transferred to an 8-bit external device, a DMA transfer unit is divided into multiple bus cycles. When a DMA transfer is divided into multiple bus cycles, and the CS signal is deactivated between bus cycles, DACK output and TEND output are divided in the same way as the CS signal.

Figure 15.45 provides an example of DACK0/TEND0.

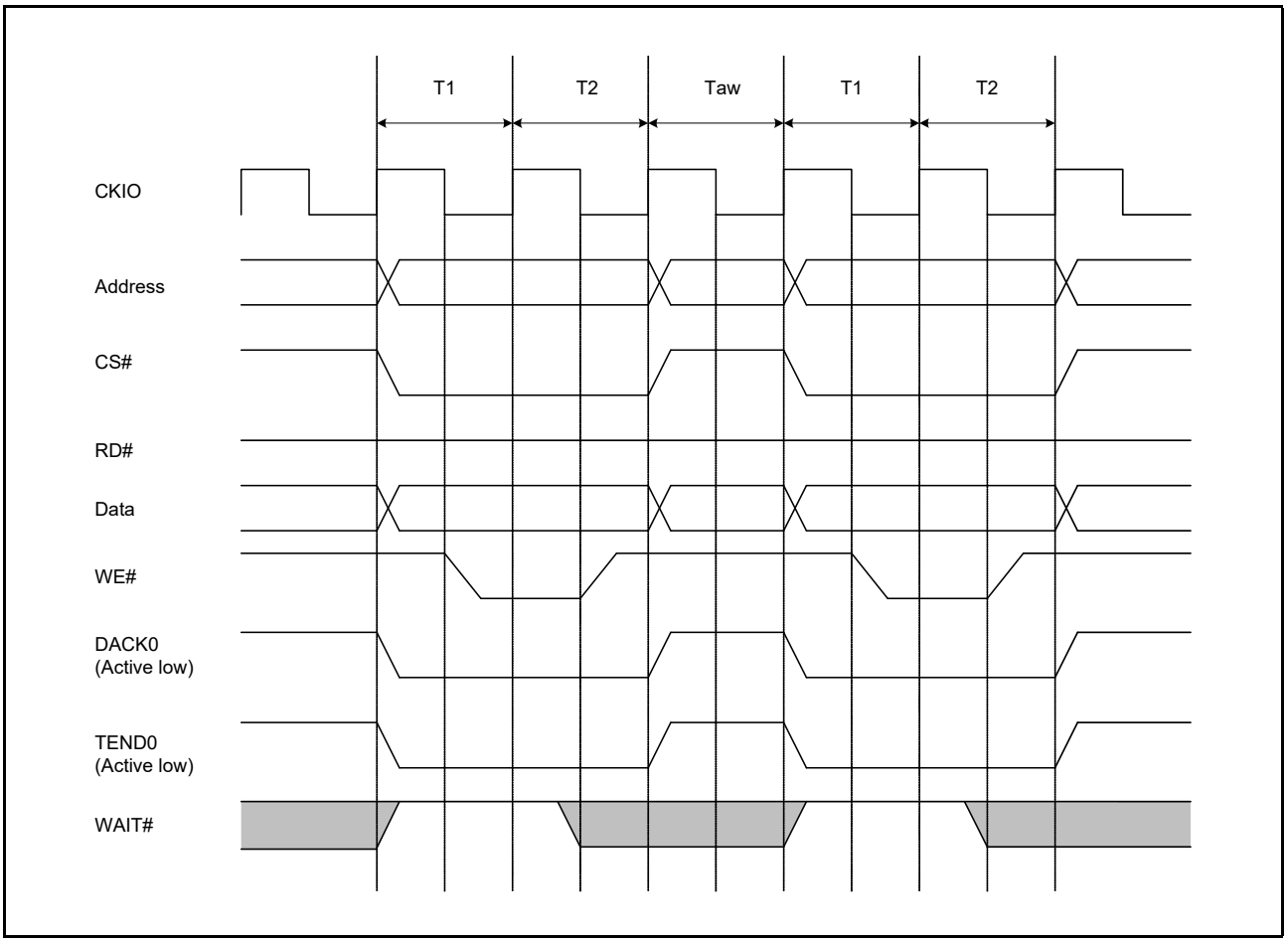


Figure 15.45 DACK/TEND Divided Output Example

15.6.2 When the TEND Signal is Not Output

Note that according to the combination of the DDS[3:0], SDS[3:0], and REQD bits in the CHCFG_n register, the TEND0 signal might not be output.

Table 15.33 shows combinations that are not output, and Figure 15.46 shows operation examples.

Table 15.33 TEND Signal Output Settings

CHCFG_n Register			
REQD	**DDS**	**SDS**	**TEND Output**
1	—	—	Output
0	DDS > SDS		Output
	DDS = SDS		Output
	DDS < SDS		Not output

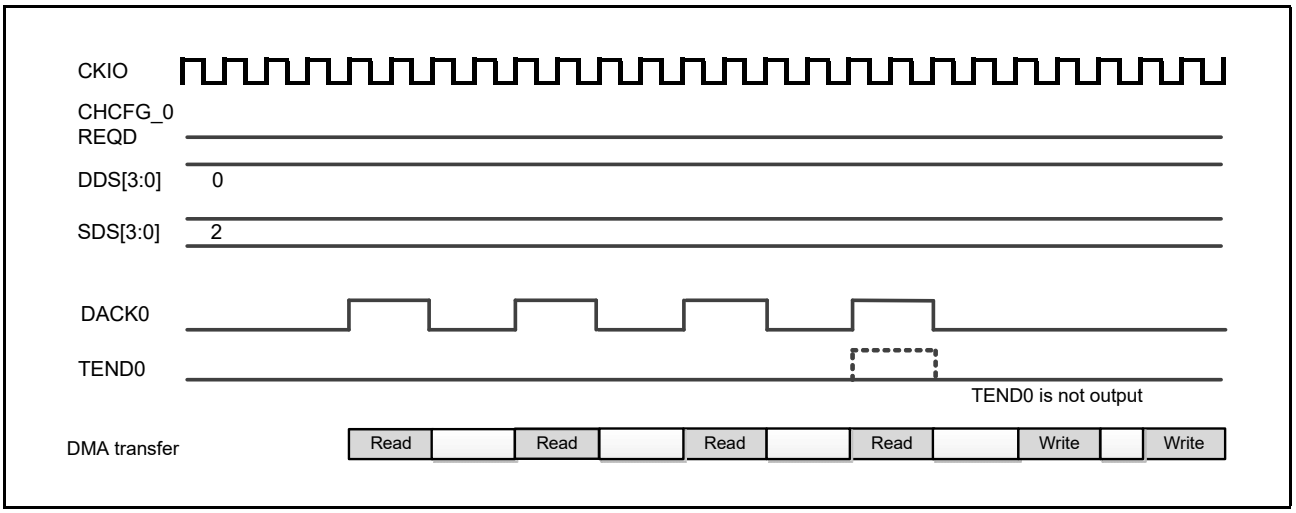


Figure 15.46 Example of TEND that is Not Output Yet

16. Event Link Controller (ELC)

16.1 Overview

The event link controller (ELC) connects (links) events generated by various peripheral modules to other modules. Event link allows direct cooperation among modules without CPU intervention.

Table 16.1 lists the specifications of the ELC, and Figure 16.1 shows a block diagram of the ELC.

Table 16.1 ELC Specifications

Item	Description
Event link function	• 103 types of event signals can be directly connected to modules. • The operation of timer modules can be selected when an event is input to the timer module. • Event link operation is possible for port B and port E. Single port*1: An event link can be set for a single bit specified in a port. Port group*1: An event link can be set for a group of single bits specified within eight I/O ports.
Low-power consumption function	Module-stop state can be set.

Note 1. The single port and port group specified as the input generate an event according to the change in the connected signal value.

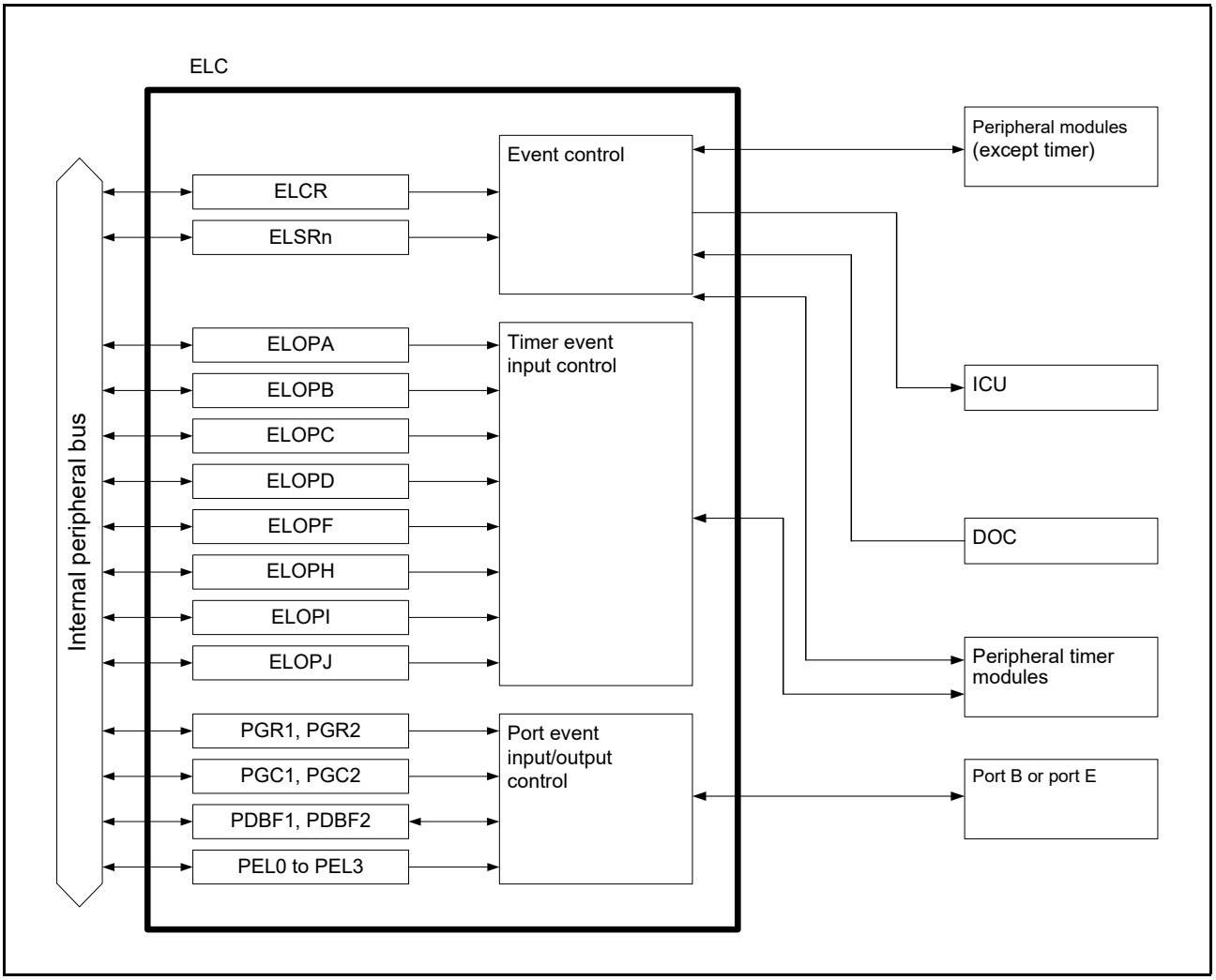


Figure 16.1 ELC Block Diagram (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 41 to 45)

16.2 Register Descriptions

16.2.1 Event Link Control Register (ELCR)

The ELCR register controls operation of the ELC.

Address(es): A008 0B00h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
Value after reset:	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	ELCON	All Event Link Enable	0: ELC function is disabled. 1: ELC function is enabled	R/W

16.2.2 Event Link Setting Register n (ELSRn) (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, 41 to 45)

The ELSRn register specifies an event signal to be linked to for each peripheral module. Table 16.2 shows the correspondence between the ELSRn register and the peripheral modules. Table 16.3 shows the correspondence between the event signal names set in the ELSRn register and the signal numbers.

Address(es): ELSR0 A008 0B01h, ELSR3 A008 0B04h, ELSR4 A008 0B05h, ELSR7 A008 0B08h, ELSR10 A008 0B0Bh, ELSR11 A008 0B0Ch, ELSR12 A008 0B0Dh, ELSR13 A008 0B0Eh, ELSR15 A008 0B10h, ELSR16 A008 0B11h*1, ELSR18 A008 0B13h, ELSR19 A008 0B14h, ELSR20 A008 0B15h, ELSR21 A008 0B16h, ELSR22 A008 0B17h, ELSR23 A008 0B18h, ELSR24 A008 0B19h, ELSR25 A008 0B1Ah, ELSR26 A008 0B1Bh, ELSR27 A008 0B1Ch, ELSR28 A008 0B1Dh*1, ELSR33 A008 0B31h, ELSR35 A008 0B33h, ELSR36 A008 0B34h, ELSR37 A008 0B35h, ELSR38 A008 0B36h, ELSR41 A008 0B39h, ELSR42 A008 0B3Ah, ELSR43 A008 0B3Bh, ELSR44 A008 0B3Ch, ELSR45 A008 0B3Dh

Note 1. Only for products incorporating an Encoder I/F.

	b7	b6	b5	b4	b3	b2	b1	b0
	ELS[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ELS[7:0]	Event Link Select	b7 b0 00000000: Event output to the corresponding peripheral module is disabled. 00000001 to 10111101: Set the number for the event signal to be linked. Settings other than above are prohibited.	R/W

Table 16.2 Correspondence between the ELSRn Register and the Peripheral Functions

Register Name	Peripheral Function (Module)
ELSR0	MTU0
ELSR3	MTU3
ELSR4	MTU4
ELSR7	CMT1
ELSR10	ΔΣIF unit 0 trigger 0*1
ELSR11	ΔΣIF unit 0 trigger 1*1
ELSR12	ΔΣIF unit 1 trigger 0*1
ELSR13	ΔΣIF unit 1 trigger 1*1
ELSR15	S12AD0
ELSR16	Encoder I/F trigger 0 (optional)
ELSR18	Interrupt 1 (ELCIRQ1)
ELSR19	Interrupt 2 (ELCIRQ2)
ELSR20	Output port group 1
ELSR21	Output port group 2
ELSR22	Input port group 1
ELSR23	Input port group 2
ELSR24	Single port 0
ELSR25	Single port 1
ELSR26	Single-port 2
ELSR27	Single-port 3
ELSR28	Encoder I/F trigger 1 (optional)
ELSR33	CMTW0
ELSR35	TPU0
ELSR36	TPU1
ELSR37	TPU2
ELSR38	TPU3
ELSR41	GPT0
ELSR42	GPT1
ELSR43	GPT2
ELSR44	GPT3
ELSR45	S12AD1

Note 1. Crest and trough trigger capturing can be used by selecting the crest or trough triggers of the PWM timers (MTU3a, GPTa) as event signals. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers (1 / 3)

ELS[7:0] Bit Value	Peripheral modules	Name of Event Signal Set in ELSRn
01h	Multifunction timer pulse unit 3	MTU0 compare match 0A
02h		MTU0 compare match 0B
03h		MTU0 compare match 0C
04h		MTU0 compare match 0D
05h		MTU0 compare match 0E
06h		MTU0 compare match 0F
07h		MTU0 overflow
10h		MTU3 compare match 3A
11h		MTU3 compare match 3B
12h		MTU3 compare match 3C
13h		MTU3 compare match 3D
14h		MTU3 overflow
15h		MTU4 compare match 4A
16h		MTU4 compare match 4B
17h		MTU4 compare match 4C
18h		MTU4 compare match 4D
19h		MTU4 overflow
1Ah		MTU4 underflow
1Fh	Compare match timer	CMT1 compare match 1
22h	Ethernet controller	Ether Switch SYNCOUT
23h		EtherCAT Sync0 (optional)
24h		EtherCAT Sync1 (optional)
25h	Encoder I/F	Encoder I/F event 1 (optional)
26h		Encoder I/F event 2 (optional)
27h		Encoder I/F event 3 (optional)
28h		Encoder I/F event 4 (optional)
29h		Encoder I/F event 5 (optional)
2Ah		Encoder I/F event 6 (optional)
2Bh		Encoder I/F event 7 (optional)
2Ch		Encoder I/F event 8 (optional)
4Eh	I^2C bus interface	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full
50h		RIIC0 transmit data empty
51h		RIIC0 transmit end
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error)
53h		RSPI0 idle
54h		RSPI0 receive data full
55h		RSPI0 transmit data empty
56h		RSPI0 transmit end
58h	12-bit A/D converter	S12AD0 A/D conversion end

Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers (2 / 3)

ELS[7:0] Bit Value	Peripheral modules	Name of Event Signal Set in ELSRn
63h	I/O ports	Input edge detection of input port group 1
64h		Input edge detection of input port group 2
65h		Input edge detection of single input port 0
66h		Input edge detection of single input port 1
67h		Input edge detection of single input port 2
68h		Input edge detection of single input port 3
69h	Event link controller	Software event
6Ah	Data operation circuit	DOC data operation condition met signal
6Ch	12-bit A/D converter	S12AD1 A/D conversion end
7Eh	Compare match timer W	CMTW channel 0 compare match
80h	General PWM timer	GPT0 compare match A
81h		GPT0 compare match B
82h		GPT0 compare match C
83h		GPT0 compare match D
86h		GPT0 overflow
87h		GPT0 underflow
88h		GPT1 compare match A
89h		GPT1 compare match B
8Ah		GPT1 compare match C
8Bh		GPT1 compare match D
8Eh		GPT1 overflow
8Fh		GPT1 underflow
90h		GPT2 compare match A
91h		GPT2 compare match B
92h		GPT2 compare match C
93h		GPT2 compare match D
96h		GPT2 overflow
97h		GPT2 underflow
98h		GPT3 compare match A
99h		GPT3 compare match B
9Ah		GPT3 compare match C
9Bh		GPT3 compare match D
9Eh		GPT3 overflow
9Fh		GPT3 underflow
A0h	Multifunction timer pulse unit3	MTU6 compare match 6A signal
A1h		MTU6 compare match 6B signal
A2h		MTU6 compare match 6C signal
A3h		MTU6 compare match 6D signal
A4h		MTU6 overflow signal
A5h		MTU7 compare match 7A signal
A6h		MTU7 compare match 7B signal
A7h		MTU7 compare match 7C signal
A8h		MTU7 compare match 7D signal
A9h		MTU7 overflow signal
AAh		MTU7 underflow signal

Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers (3 / 3)

ELS[7:0] Bit Value	Peripheral modules	Name of Event Signal Set in ELSRn
ACh	16-bit timer pulse unit	TPU0 compare match A
ADh		TPU0 compare match B
AEh		TPU0 compare match C
AFh		TPU0 compare match D
B0h		TPU0 overflow
B1h		TPU1 compare match A
B2h		TPU1 compare match B
B3h		TPU1 overflow
B4h		TPU1 underflow
B5h		TPU2 compare match A
B6h		TPU2 compare match B
B7h		TPU2 overflow
B8h		TPU2 underflow
B9h		TPU3 compare match A
BAh		TPU3 compare match B
BBh		TPU3 compare match C
BCh		TPU3 compare match D
BDh		TPU3 overflow
Settings other than above are prohibited.		

16.2.3 Event Link Option Setting Register A (ELOPA)

The ELOPA register determines the operation of MTU0 and MTU3 when an event is input. The event setting should be disabled when the ELC function is not used.

Address(es): A008 0B1Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	MTU3MD [1:0]		—	—	—	—	MTU0MD [1:0]	
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	MTU0MD [1:0]	MTU0 Operation Select	b1 b0 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*1 1 1: Event is disabled.	R/W
b5 to b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7, b6	MTU3MD [1:0]	MTU3 Operation Select	b7 b6 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*2 1 1: Event is disabled.	R/W

Note 1. The MTU0.TCNT value is captured into MTU0.TGRA.
Note 2. The MTU3.TCNT value is captured into MTU3.TGRA.

16.2.4 Event Link Option Setting Register B (ELOPB)

The ELOPB register determines the operation of MTU4 when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B20h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MTU4MD[1:0]	
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	MTU4MD[1:0]	MTU4 Operation Select	b1 b0 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*1 1 1: Event is disabled.	R/W
b7 to b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. The MTU4.TCNT value is captured into MTU4.TGRA.

16.2.5 Event Link Option Setting Register C (ELOPC)

The ELOPC register determines the operation of CMT1 when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B21h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMT1MD[1:0]		—	—
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b3, b2	CMT1MD[1:0]	CMT1 Operation Select	b3 b2 0 0: Counting is started. 0 1: The counter is cleared 1 0: Event counter 1 1: Event is disabled.	R/W
b7 to b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

16.2.6 Event Link Option Setting Register D (ELOPD)

The ELOPD register determines the operation of the ΔΣIF unit 0 trigger 0, the ΔΣIF unit 0 trigger 1, the ΔΣIF unit 1 trigger 0, and the ΔΣIF unit 1 trigger 1 when an event is input. The event setting should be disabled when the ELC function is not used.

Address(es): A008 0B22h

	b7	b6	b5	b4	b3	b2	b1	b0
	DSX1MD[1:0]		DSX0MD[1:0]		DSU1MD[1:0]		DSU0MD[1:0]	
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DSU0MD[1:0]	ΔΣIF Unit 0 Trigger 0 Event Link Select	b1 b0 0 0: Event link function enabled 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Event link function disabled	R/W
b3, b2	DSU1MD[1:0]	ΔΣIF Unit 0 Trigger 1 Event Link Select	b3 b2 0 0: Event link function enabled 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Event link function disabled	R/W
b5, b4	DSX0MD[1:0]	ΔΣIF Unit 1 Trigger 0 Event Link Select	b5 b4 0 0: Event link function enabled 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Event link function disabled	R/W
b7, b6	DSX1MD[1:0]	ΔΣIF Unit 1 Trigger 1 Event Link Select	b7 b6 0 0: Event link function enabled 0 1: Setting prohibited 1 0: Setting prohibited 1 1: Event link function disabled	R/W

16.2.7 Port Group Setting Register n (PGRn) (n = 1, 2)

The PGRn register specifies a group for I/O port bits. This register specifies each port bit in the same eight I/O ports as the member of a group. One to eight port bits can be specified as the members of the same group as required. Table 16.4 shows the PGRn register and corresponding ports.

Address(es): PGR1 A008 0B23h, PGR2 A008 0B24h

	b7	b6	b5	b4	b3	b2	b1	b0
	PGRn7	PGRn6	PGRn5	PGRn4	PGRn3	PGRn2	PGRn1	PGRn0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PGRn0	Port Group Setting n 0	0: The port bit is not specified as a member of the same group. 1: The port bit is specified as a member of the same group.	R/W
b1	PGRn1	Port Group Setting n 1		R/W
b2	PGRn2	Port Group Setting n 2		R/W
b3	PGRn3	Port Group Setting n 3		R/W
b4	PGRn4	Port Group Setting n 4		R/W
b5	PGRn5	Port Group Setting n 5		R/W
b6	PGRn6	Port Group Setting n 6		R/W
b7	PGRn7	Port Group Setting n 7		R/W

Table 16.4 Registers Related to Port Groups and Corresponding Port Numbers

Port Number	Port Group Setting Register (PGR)	Port Group Control Register (PGC)	Port Buffer Register (PDBF)
Port B	PGR1 register	PGC1 register	PDBF1 register
Port E	PGR2 register	PGC2 register	PDBF2 register

16.2.8 Port Group Control Register n (PGCn) (n = 1, 2)

For the output port group, the PGCn register specifies the form of outputting the signal externally via the port when the event signal is input. For the input port group, this register enables/disables overwriting of the PDBF register and specifies the conditions of event generation (edge of the externally input signal).
Refer to Table 16.4 for the PGRn register and corresponding ports.

Address(es): PGC1 A008 0B25h, PGC2 A008 0B26h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PGCOn[2:0]			—	PGCOVEn	PGCIn[1:0]	
Value after reset:	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PGCIn [1:0]	Event Output Edge Select	b1 b0 0 0: Event is generated upon detection of the rising edge of the external input signal. 0 1: Event is generated upon detection of the falling edge of the external input signal. 1 X: Event is generated upon detection of both the rising and falling edges of the external input signal.	R/W
b2	PGCOVEn	PDBF Overwrite	0: Overwriting PDBFn register is disabled. 1: Overwriting PDBFn register is enabled.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6 to b4	PGCOn [2:0]	Port Group Operation Select	b6 b4 0 0 0: 0 is output when the event is input. 0 0 1: 1 is output when the event is input. 0 1 0: The toggled (inverted) value is output when the event is input. 0 1 1: The buffer value is output when the event is input. 1 X X: The bit value is rotated out in the group (from MSB to LSB) when the event is input.	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

X: Don't care

16.2.9 Port Buffer Register n (PDBFn) (n = 1, 2)

The PDBFn register is an 8-bit readable/writable register used in combination with the PGRn register. Refer to section 16.3.5, I/O Port Operation upon Event Input and Event Generation for PDBFn register operations. Refer to Table 16.4 for the PDBFn register and corresponding ports.

Address(es): PDBF1 A008 0B27h, PDBF2 A008 0B28h

	b7	b6	b5	b4	b3	b2	b1	b0
	PDBFn 7	PDBFn 6	PDBFn 5	PDBFn 4	PDBFn 3	PDBFn 2	PDBFn 1	PDBFn 0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PDBFn0	Port Buffer n0	These bits handle the following operations in response to an input to or output from the port. • As an output port The value written to the PDBFn register is transferred to the PODR register. • As an input port The signal values on the external pins are transferred to the PDBFn register. Write access to the bit specified as a member of the input port group is invalid. For details, refer to section 16.3, Operation.	R/W
b1	PDBFn1	Port Buffer n1		R/W
b2	PDBFn2	Port Buffer n2		R/W
b3	PDBFn3	Port Buffer n3		R/W
b4	PDBFn4	Port Buffer n4		R/W
b5	PDBFn5	Port Buffer n5		R/W
b6	PDBFn6	Port Buffer n6		R/W
b7	PDBFn7	Port Buffer n7		R/W

16.2.10 Event Link Port Setting Register n (PELn) (n = 0 to 3)

The PELn register specifies the single port to which an event is to be linked, the port operation upon the event signal input, and the conditions of event generation. In this LSI, a total of 4 bits in port B or port E can be specified as single ports.

Address(es): PEL0 A008 0B29h, PEL1 A008 0B2Ah, PEL2 A008 0B2Bh, PEL3 A008 0B2Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PSMn[1:0]		PSPn[1:0]		PSBn[2:0]		
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	PSBn[2:0]	Bit Number Specification	A bit number in eight I/O ports is specified.	R/W
b4, b3	PSPn[1:0]	Port Number Specification	b4 b3 0 0: Setting prohibited 0 1: Port B (corresponding to PGR1) 1 0: Port E (corresponding to PGR2) 1 1 1: Setting prohibited	R/W
b6, b5	PSMn[1:0]	Event Link Specification	• For the output port, data to be output from the port is specified. b6 b5 0 0: 0 is output when the event is input. 0 1: 1 is output when the event is input. 1 X: The toggled (inverted) value is output when the event is input. • For the input port, the edge on which the event is to be output is specified. b6 b5 0 0: Event is output upon detection of the rising edge. 0 1: Event is output upon detection of the falling edge. 1 X: Event is output upon detection of both the rising and falling edges.	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

X: Don’t care

16.2.11 Event Link Software Event Generation Register (ELSEGR)

The ELSEGR register controls event generation by software.

Address(es): A008 0B2Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	1	1	1	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	SEG	Software Event Generation	0: Normal operation 1: Software event is generated.	W
b5 to b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b6	WE	SEG Bit Write Enable	0: Write to SEG bit is disabled. 1: Write to SEG bit is enabled.	R/W
b7	WI	ELSEGR Register Write Disable	0: Write to ELSEGR register is enabled. 1: Write to ELSEGR register is disabled.	W

SEG Bit (Software Event Generation)

When 1 is written to this bit while the WE bit is 1, a software event is generated.
This bit is read as 0. Even if 1 is written to this bit, the data will not be stored.

WE Bit (SEG Bit Write Enable)

The SEG bit can be written to only when the WE bit is 1.
[Setting condition]
If 1 is written to this bit while the WI bit is 0, this bit becomes 1.
[Clearing condition]
If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI Bit (ELSEGR Register Write Disable)

The ELSEGR register can be written to only when the value to be written to the WI bit is 0.
This bit is read as 1.

Note 1. The WE bit can only be updated by setting the WI bit and the WE bit at the same time.
Similarly, to update the SEG bit, the WI bit must be set at the same time; set WE = 1 by setting the WI bit and WE bit at the same time, and then set the WI bit and SEG bit. If WE = 1 when SEG is set, the WE bit retains the value 1.
However, setting the three bits at the same time while the current values are WI = 1, WE = 0, and SEG = 0 will not lead to the output of a software trigger. Since WE will only have the value 1 following the first time the three bits are set, a software trigger will only be generated by setting the three bits at the same time again.

16.2.12 Event Link Option Setting Register F (ELOPF)

The ELOPF register determines the operation of TPU0 to TPU3 when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B3Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TPU3MD[1:0]		TPU2MD[1:0]		TPU1MD[1:0]		TPU0MD[1:0]	
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TPU0MD[1:0]	TPU0 Operation Select	b1 b0 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*1 1 1: Event is disabled.	R/W
b3, b2	TPU1MD[1:0]	TPU1 Operation Select	b3 b2 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*2 1 1: Event is disabled.	R/W
b5, b4	TPU2MD[1:0]	TPU2 Operation Select	b5 b4 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*3 1 1: Event is disabled.	R/W
b7, b6	TPU3MD[1:0]	TPU3 Operation Select	b7 b6 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Input capture*4 1 1: Event is disabled.	R/W

Note 1. The TPU0.TCNT value is captured by TPU0.TGRA.
Note 2. The TPU1.TCNT value is captured by TPU1.TGRA.
Note 3. The TPU2.TCNT value is captured by TPU2.TGRA.
Note 4. The TPU3.TCNT value is captured by TPU3.TGRA

16.2.13 Event Link Option Setting Register H (ELOPH)

The ELOPH register determines the operation of channel 0 in CMTW when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B41h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMTW0MD[1:0]	
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CMTW0MD[1:0]	CMTW0 Operation Select	b1 b0 0 0: Counting is started. 0 1: Counting is cleared. 1 0: Event counter 1 1: Event is disabled.	R/W
b7 to b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

16.2.14 Event Link Option Setting Register I (ELOPI)

The ELOPI register determines the operation of GPT0 and GPT1 when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B42h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	GPT1MD[2:0]			—	GPT0MD[2:0]		
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	GPT0MD[2:0]	GPT0 Operation Select	b2 b0 0 0 0: Counting is started. 0 0 1: Counting is cleared. 0 1 0: Counting is stopped. 0 1 1: Input capture*1 1 1 1: Event is disabled. Settings other than above are prohibited.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6 to b4	GPT1MD[2:0]	GPT1 Operation Select	b6 b4 0 0 0: Counting is started. 0 0 1: Counting is cleared. 0 1 0: Counting is stopped. 0 1 1: Input capture*2 1 1 1: Event is disabled. Settings other than above are prohibited.	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note 1. The GPT0.GTCNT value is captured by GPT0.GTCCRA.
Note 2. The GPT1.GTCNT value is captured by GPT1.GTCCRA.

16.2.15 Event Link Option Setting Register J (ELOPJ)

The ELOPJ register determines the operation of GPT2 and GPT3 when an event is input. The event setting should be disabled when the ELC function is not to be used.

Address(es): A008 0B43h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	GPT3MD[2:0]			—	GPT2MD[2:0]		
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	GPT2MD[2:0]	GPT2 Operation Select	b2 b0 0 0 0: Counting is started. 0 0 1: Counting is cleared. 0 1 0: Counting is stopped. 0 1 1: Input capture*1 1 1 1: Event is disabled. Settings other than above are prohibited.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b6 to b4	GPT3MD[2:0]	GPT3 Operation Select	b6 b4 0 0 0: Counting is started. 0 0 1: Counting is cleared. 0 1 0: Counting is stopped. 0 1 1: Input capture*2 1 1 1: Event is disabled. Settings other than above are prohibited.	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note 1. The GPT2.GTCNT value is captured by GPT2.GTCCRA.
Note 2. The GPT3.GTCNT value is captured by GPT3.GTCCRA.

16.3 Operation

16.3.1 Relation between Interrupt Handling and Event Linking

The peripheral modules incorporated in this LSI are provided with the interrupt request status flags and the bits to enable/disable these interrupt requests. When an interrupt request is generated in a module, the corresponding interrupt request status flag is set. If the corresponding interrupt request is enabled then, the interrupt requested is issued to the CPU.
In contrast, the event link controller (ELC) uses the interrupt requests generated by various peripheral modules (excluding the Ethernet MAC and EtherCAT) as event signals to connect (link) them to different modules, allowing direct cooperation between the modules without CPU intervention. Event signals can be output regardless of the setting of the corresponding interrupt request enable bit. Because the Ethernet MAC and EtherCAT use interrupt signals as event signals, interrupt control must be permitted.
Figure 16.2 shows the relation between the interrupt handling and ELC.

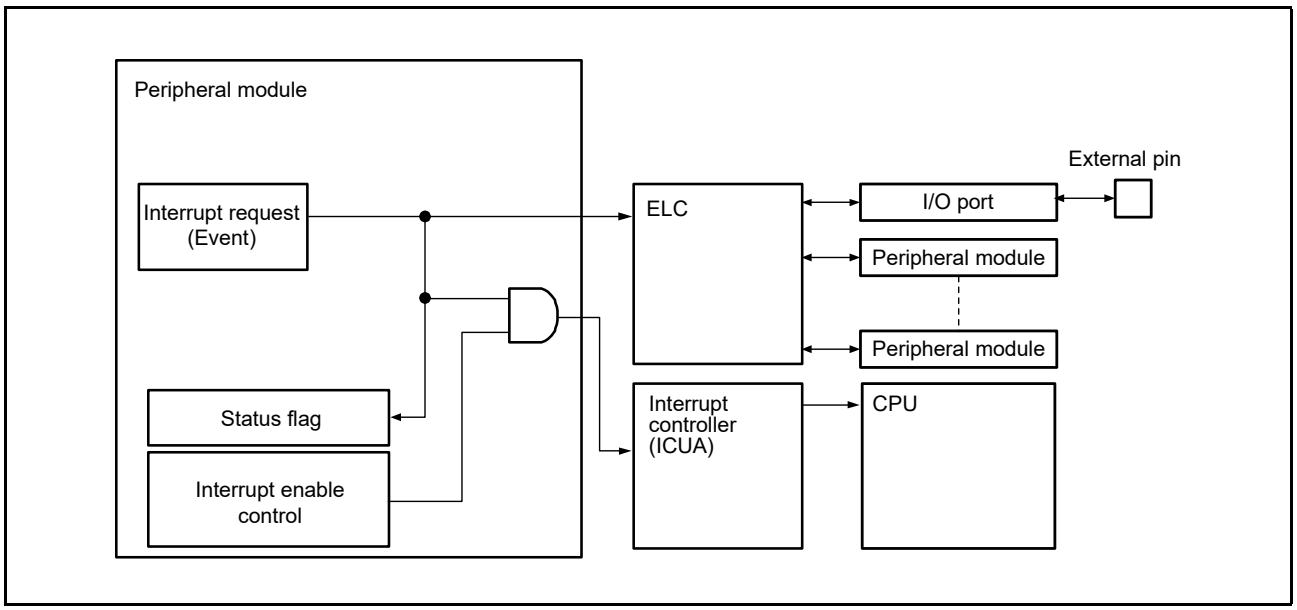


Figure 16.2 Relation between Interrupt Handling and ELC (excluding the Ethernet MAC and EtherCAT)

16.3.2 Event Linkage

Set an event to the ELSRn register of the module to which the event is to be linked. On occurrence of the specified event, the link destination module performs the operation set in the ELOPm register (m = A to D, F, H to J). Only one type of event can be connected with one module. For detailed procedure for setting desired operation, see section 16.3.6, Example of Procedure for Linking Events. Table 16.5 lists the operations of modules when an event is input.

Table 16.5 Operations of Modules When Event is Input

Module	Operations When Event is Input	
MTU CMT CMTW TPU GPT	Each module operates as follows, depending on the setting of the ELOPm register (m = A to C, F, H to J) . • Starts counting when an event signal is input (MTU, CMT, CMTW, TPU, GPT). • Clears counting when an event signal is input (MTU, CMT, CMTW, TPU, GPT). Restarting counting is possible when the start bit of the timer is 1. • Counts the input events (CMT, CMTW). • Performs input-capture operation when an event signal is input (MTU, TPU, GPT). • Stops counting when an event signal is input (GPT).	
A/D converter	Starts A/D conversion when an event signal is input.	
DSMIF	Crest/trough trigger capture function*1	
I/O ports (output)	Port group	• Changes the PODR value to the value specified in the PGCn register. • Transfers the PDBFn value to the PODR register. • Rotates out the bit value.
	Single port	Changes the PODR value to the value specified in the PELn register.
I/O ports (input)	Port group	Transfers the signal value of the external pin to the PDBFn register.
	Single port	Event connection is not possible.
Interrupt controller	Issues an interrupt request to the CPU and starts DMAC data transfer.	
Encoder I/F	Even operation set by the encoder I/F	

Note 1. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

16.3.3 Operation of Peripheral Timer Modules When Event is Input

The operation when an event signal is input is set by the ELOPm register (m = A to C, F, H to J).

(1) Counting Start Operation

When an event is input, the timer starts counting, which sets the count start bit*1 in each timer control register to 1. An event that is input while the count start bit is 1 is invalid.

(2) Counting Clear Operation

When an event is input, the timer counter is initialized. If the count start bit*1 in each timer control register is set to 1, the counting continues, thus, counting restarts.

(3) Event Counter Operation

Event input is selected as the timer clock source and the timer counts events.

(4) Input Capture Operation

When an event is input, the timer performs input-capture operation.

(5) Stopping Counting

The counter stops counting in response to the input of an event signal

Note 1. Refer to the register descriptions on starting the timer in the relevant peripheral timer module section.

16.3.4 Operation of A/D Converter When Event is Input

The A/D converter starts A/D conversion when the ADCSR.ADST bit*1 is set to 1.

Note 1. Refer to the register descriptions on the A/D converter section.

16.3.5 I/O Port Operation upon Event Input and Event Generation

The I/O port operation to be performed upon event input to the port can be set and the operation causing the port to generate an event can be set.

(1) Single ports and Port Groups

There are two event link modes: event link to single ports and event link to port groups. In the former mode, events can be connected to eight I/O ports. In the latter mode, events can be connected to port groups consisting of any two or more bits in the same eight I/O ports.
A single port can be set by specifying any bit in the I/O port*1 to which an event can be connected using the PELn register. A port group can be set by specifying any one or more bits in the I/O port*1 to which an event can be connected using the PGRn register. One input port group and one output port group can be set in the same I/O port.
If the I/O port bit is specified as both a single port and a member of a port group, both functions are enabled when the relevant port is input, whereas only the port group function is enabled when the relevant port is output.
Set the PDR register to select the direction of the I/O ports.

Note 1. Port B and port E

(2) Single Input Port Operation upon Event Generation

A single input port which is specified by the PDR register generates an event when the signal value of the external pin connected to the relevant port changes. The event generation condition is specified using PELn register. An example of event linking operation by a single input port is shown as [1] in Figure 16.3.

(3) Single Output Port Operation upon Event Input

When an event is input to a single output port which is specified by the PDR register, the signal of the external pin connected to the relevant port changes according to the settings of PELn register. This changes the signal value of the external pin connected to the relevant port. An example of event linking operation by a single output port is shown as [2] in Figure 16.3.

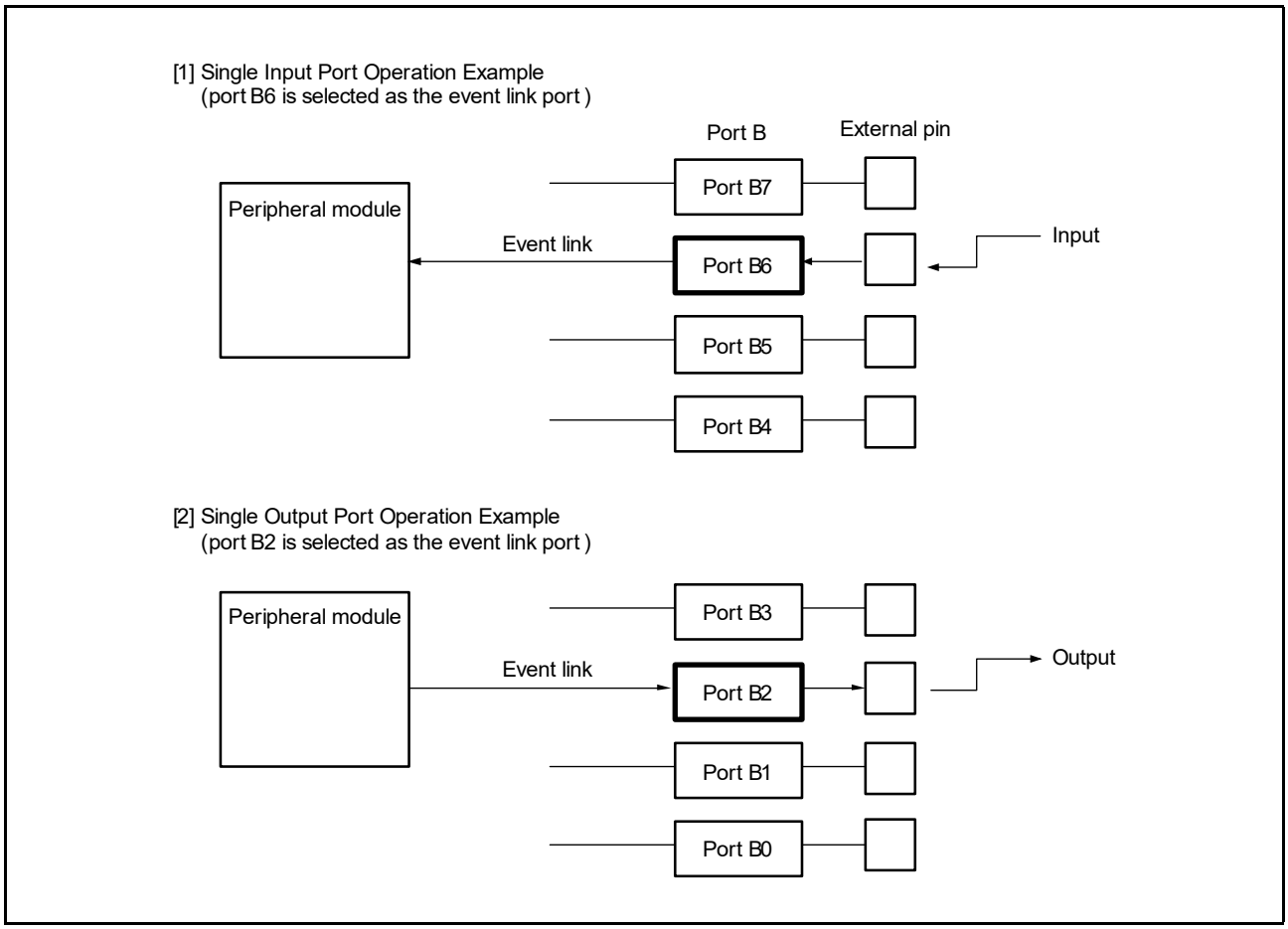


Figure 16.3 Event Linkage Related to Single Ports (Port B)

(4) Input Port Group Operation upon Event Generation

An input port group which is specified by the PDR register generates an event when the signal value of any one of the external pins connected to the relevant port group changes. The event generation condition is specified using the PCIn bit of the PGCn register.

(5) Input Port Group Operation upon Event Input

When an event is input to an input port group, the signal value of the external pin of the bit specified as a member of the input port group is transferred to the PDBFn register. If another event is input to the input port group in this state, operations are performed depending on the PGCn.PGCOVE bit setting as described below. Figure 16.4 shows the input port group operation upon an event input.

- PGCn.PGCOVEn = 0 (overwriting is disabled)
  If the value that was transferred to the PDBFn register upon the previous event input has already been read by the CPU, the signal value of the external pin is transferred to the PDBFn register. If not read, the signal value of the external pin is not transferred to the PDBFn register and the input event is invalid.
- PGCn.PGCOVEn = 1 (overwriting is enabled)
  When another event is input to an input port group, the signal value of the external pin is transferred to the PDBFn register.

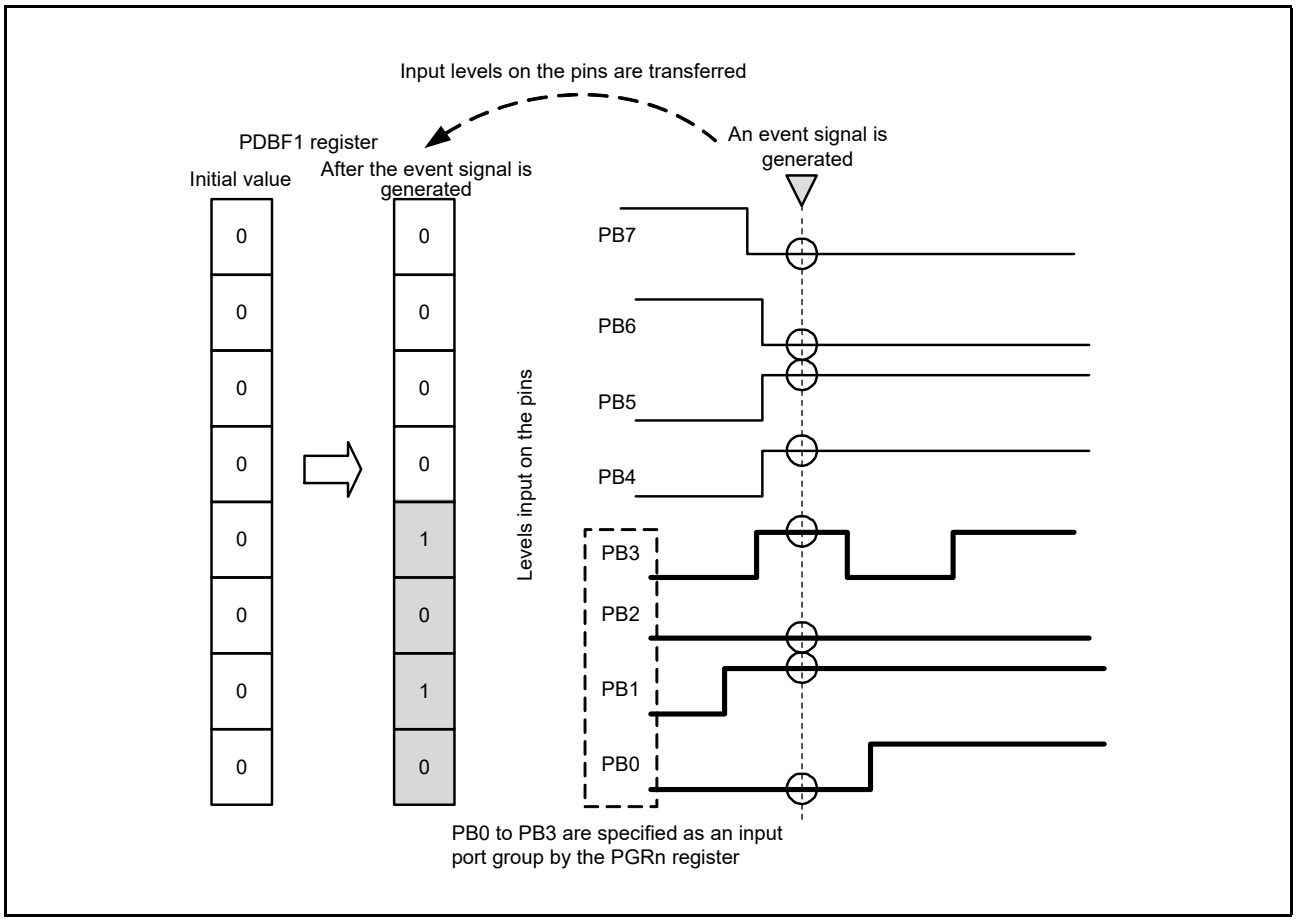


Figure 16.4 Input Port Group Operation upon Event Input (Port B)

(6) Output Port Group Operation upon Event Input

When an event is input to an output port group, the following operations are performed depending on the PGCn.PGCOn bit setting as described below.

- If an event is input to an output port group while the PGCn.PGCOn bit being 000b, 001b, or 010b, the PODR value is changed to the value which was specified in the PGCn register.
- If an event is input to an output port group while the PGCn.PGCOn bit being 011b, the PDBFn value is transferred to the PODR register of the port which was specified in the PGRn register. Example of operation of the output port group upon an event input (when PGCn.PGCOn = 011b) is shown in Figure 16.5.
- If an event is input to the output port group while the PGCn.PGCOn bit being 1XXb, the PDBFn value is transferred to the PODR register of the port which was specified in the PGRn register, and then the PODR value is rotated bit by bit from MSB to LSB. The initial value to be output to the port group should be provided in the PDBFn register in advance. Examples of bit-rotating operation of output port groups upon an event input (when PGCn.PGCOn = 1XXb) is shown in Figure 16.6.

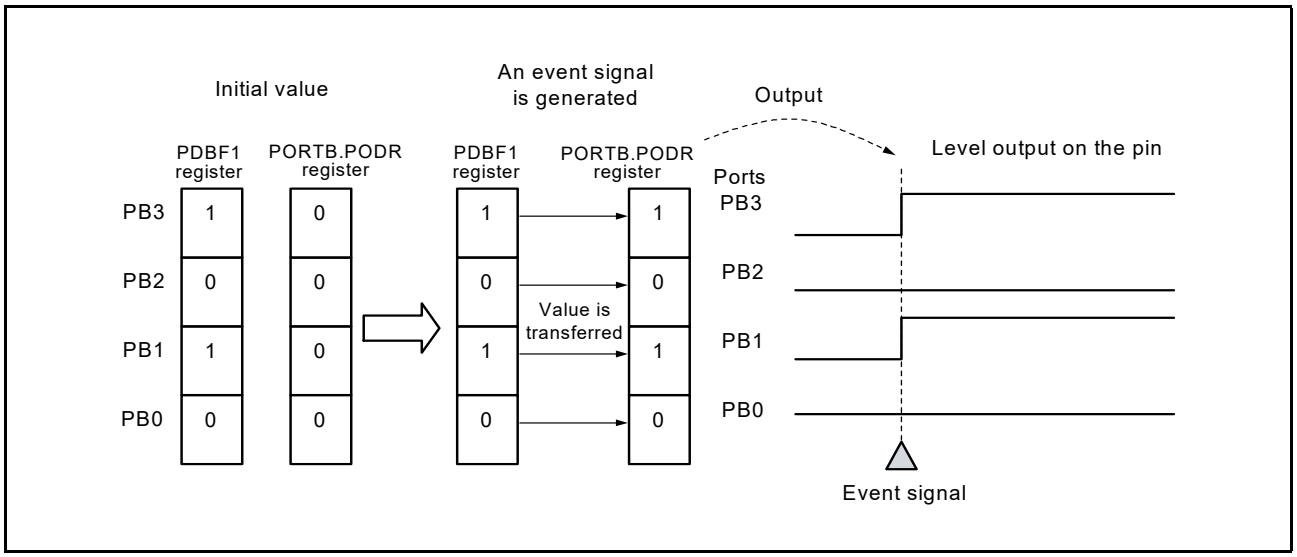


Figure 16.5 Event Linkage Operation of Output Port Group (Port B)

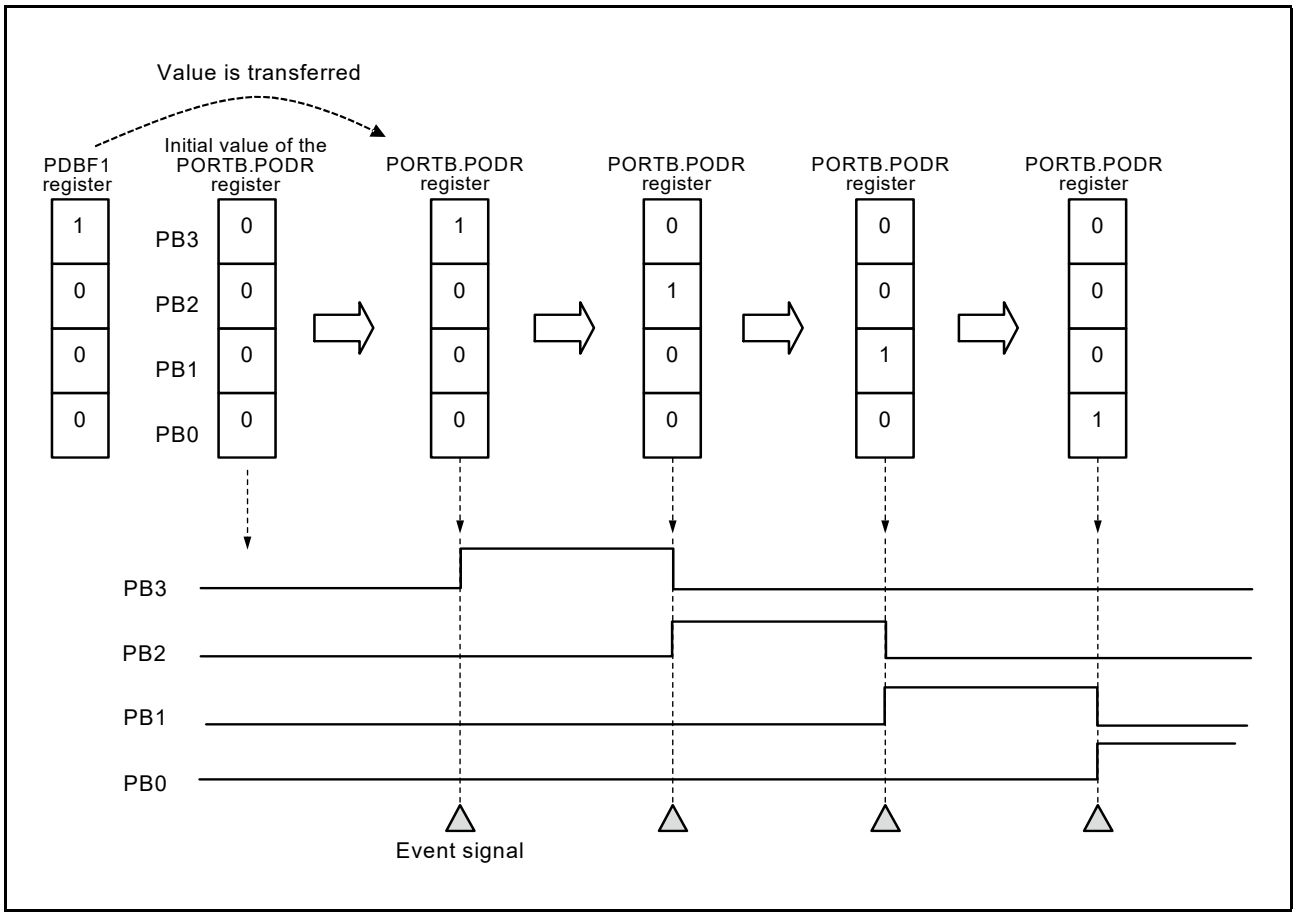


Figure 16.6 Bit-Rotating Operation of Output Port Groups (Port B)

(7) Restrictions on Writing to PODR and PDBFn Registers by a CPU

For event linkage through the I/O ports, following restrictions apply when a CPU writes the PODR and PDBFn registers.

- If port bits are specified as members of the input port group, write access to the relevant bits in the PDBFn register is invalid.
- If port bits are specified as members of the output port group, write access to the relevant bits in the PODR register is invalid.
- If a port bit is specified as a single output port and the event linkage is set (by the ELSRn register) for the port, write access to the relevant bit in the PODR register is invalid.

16.3.6 Example of Procedure for Linking Events

The following describes the procedure for linking events.

1. Set the operation of the module to which an event is to be linked.
2. If events are linked to ports, set the registers corresponding to the ports as below.

- I/O port setting
  PODR: Set the initial values of the output ports.
  PDR: Set the I/O direction of the ports.
- ELC setting
  PGRn: If ports are used as a port group, set the ports (in bit units) to be grouped.
  PGCn: Set the operation of the port group.
  PELn: If ports are used as single ports, set the ports, the operation of the ports when an event is input, and the condition when an event is generated.

Note: Setting the PDBFn register
(1) Output port groups
Set the PGCn register before setting the PDBFn register.
The value of the PGCn register can be changed if this precedes an event trigger which causes the value of the PODR register to change.
(2) Input port groups
Setting the PDBFn is not required. However, since the value after a reset is 00h, if the PDBFn register is used to confirm changes from H to L due to an event input, set the PDBFn bit for the pin for which you wish to confirm this to 1.

3. To the ELSRn register corresponding to the module to which an event signal is to be linked, set the number of the event signal.
4. If events are to be linked to timer modules, set the ELOPm registers (m = A to C, F, H to J) corresponding to the timers as required. If the module to which an event is to be linked is ΔΣIF, set the corresponding ELOPD register as required.
5. Set the ELCR.ELCON bit to 1, which enables linkage of all the events.
6. Set the operation of the module from which an event is output, and activate the module. This allows the event output from the module to start the module to which an event is linked as preset.
7. To stop event linkage of independent modules, set 0000 0000b to the ELSRn.ELS[7:0] bits corresponding to the modules. To stop linkage of all the events, set the ELCR.ELCON bit to 0.

16.4 Usage Notes

16.4.1 Setting ELSR18 and ELSR19 Registers

For event linkage to an interrupt controller, specify the event signals to be set in the ELSR18 and ELSR19 registers from 63h to BDh. Setting any other values is prohibited.

16.4.2 Setting Bit-Rotating Operation of Output Port Groups

When the values of the PDBFn register are changed in the bit-rotating operation mode of the output port group, set the ELSRn register again after changing the PDBFn register value.

16.4.3 Setting Clocks

To link events, it is necessary for the ELC and the related modules to be enabled. The modules cannot operate if the related modules are in the module-stop state or if the low-power consumption mode causes the modules to stop (all-module stop mode).

16.4.4 Module Stop Function Setting

ELC operation can be disabled or enabled using module stop control register C (MSTPCRC). The initial setting allows the ELC to be stopped. Register access is enabled by canceling the module-stop state. For details, see section 9, Low-Power Consumption Function.

17. I/O Ports

17.1 Overview

The pins of an I/O port function as general I/O port pins, I/O pins for peripheral modules, or interrupt input pins.
Each pin is also configurable as an I/O pin of a peripheral module or an input pin for an interrupt. All pins are set to non-use immediately after a reset (Hi-Z input protection), and pin functions can be switched by register settings. The setting of each pin is specified by the registers for the corresponding I/O port and peripheral modules.
Each port has the port direction register (PDR) that selects non-use, input, or output, the port output data register (PODR) that holds data for output, the port input register (PIDR) that indicates the pin states, the pull-up/pull-down control register (PCR) that controls enabling and disabling of the input pull-up/pull-down resistor, and the port mode register (PMR) that specifies the pin function of each port. For details on PMR, refer to section 18, Multi-Function Pin Controller (MPC).
The configuration of the I/O ports differs depending on the package. Table 17.1 shows the specifications of I/O ports, and Table 17.2 lists the port functions.

Table 17.1 Specifications of I/O Ports

	Package		Package	
Port	**320 Pins**	**Number of Pins**	**176 Pins**	**Number of Pins**
PORT0	P00 to P07	8	P00 to P07	8
PORT1	P10 to P17	8	P10, P13 to P17	6
PORT2	P20 to P27	8	P20 to P27	8
PORT3	P30 to P37	8	P30, P33 to P37	6
PORT4	P40 to P47	8	P40, P42, P43, P47	4
PORT5	P50 to P56	7	P51, P54, P56	3
PORT6	P60 to P67	8	P60 to P65	6
PORT7	P70 to P77	8	P70 to P77	8
PORT8	P80 to P87	8	P82, P85 to P87	4
PORT9	P90 to P97	8	Not provided	0
PORTA	PA0 to PA7	8	PA0 to PA7	8
PORTB	PB0 to PB7	8	PB0 to PB7	8
PORTC	PC0 to PC7	8	PC0 to PC3	4
PORTD	PD0 to PD7	8	PD5 to PD7	3
PORTE	PE0 to PE7	8	PE0 to PE7	8
PORTF	PF5 to PF7	3	PF5 to PF6	2
PORTG	PG0 to PG7	8	PG0 to PG7	8
PORTH	PH0 to PH7	8	PH0 to PH7	8
PORTJ	PJ0 to PJ7	8	Not provided	0
PORTK	PK0 to PK7	8	Not provided	0
PORTL	PL0 to PL7	8	Not provided	0
PORTM	PM0 to PM7	8	Not provided	0
PORTN	PN0 to PN7	8	Not provided	0
PORTP	PP0 to PP7	8	Not provided	0
PORTR	PR0 to PR7	8	Not provided	0
PORTS	PS0 to PS7	8	Not provided	0
PORTT	PT0 to PT7	8	Not provided	0
PORTU	PU0 to PU7	8	Not provided	0
	Total of pins	218	Total of pins	102

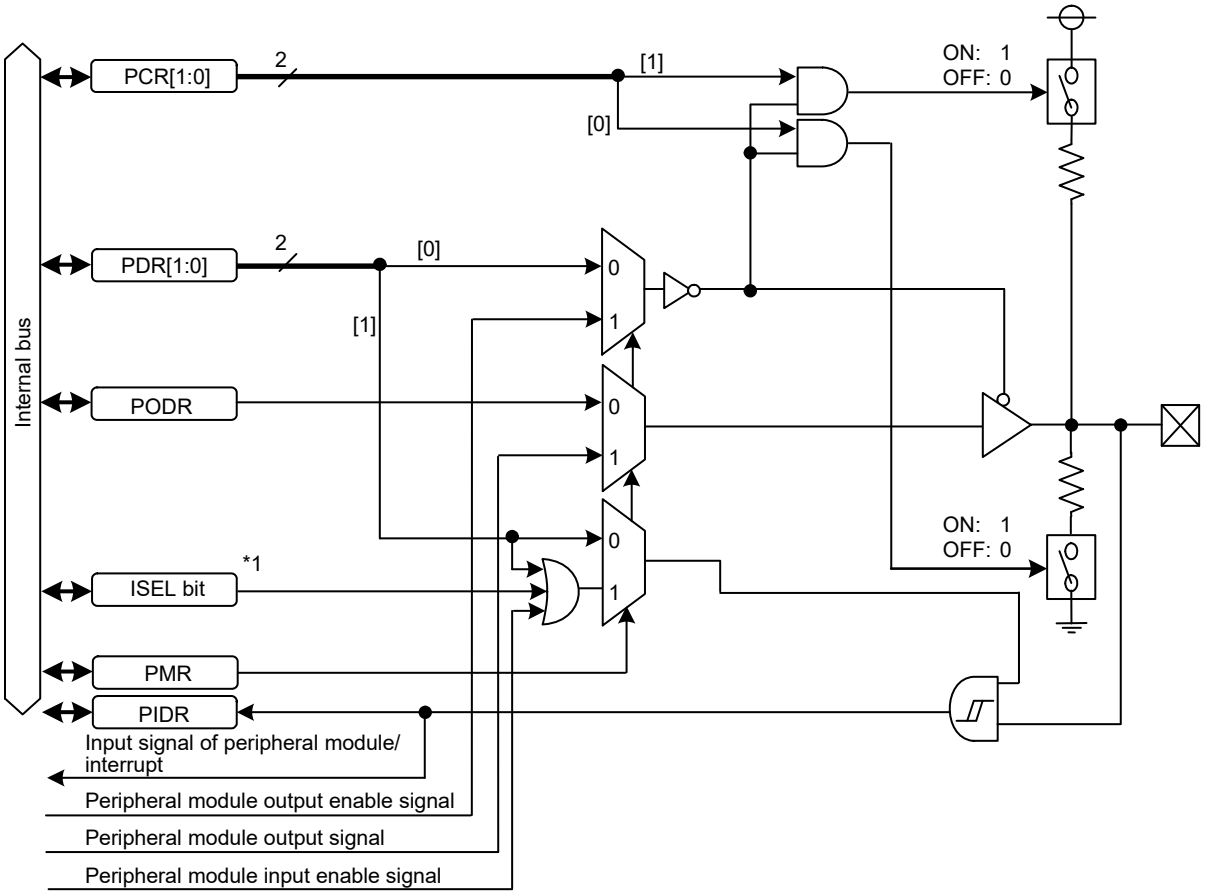
Table 17.2 Port Functions

Port	Pin	Input Pull-Up/Pull-Down	Switching of Driving Ability	5-V Tolerant	Schmitt Input
PORT0	P00 to P07	√	—	—	—
PORT1	P10	√	√	—	√
	P11 to P17	√	—	—	√
PORT2	P20 to P27	√	—	—	√
PORT3	P30	—	—	√	√
	P31 to P33, P35 to P37	√	—	—	√
	P34	√	—	—	—
PORT4	P40 to P47	√	—	—	√
PORT5	P50 to P56	√	—	—	√
PORT6	P60 to P67	√	—	—	√
PORT7	P70 to P77	√	—	—	—
PORT8	P80 to P85	√	—	—	√
	P86, P87	√	—	—	√
PORT9	P90 to P97	√	—	—	√
PORTA	PA0 to PA7	√	—	—	—
PORTB	PB0 to PB7	√	—	—	√
PORTC	PC0 to PC7	—	—	√	√
PORTD	PD0 to PD7	√	—	—	√
PORTE	PE0 to PE7	√	—	—	—
PORTF	PF5 to PF7	√	—	—	√
PORTG	PG0 to PG7	√	—	—	√
PORTH	PH0 to PH7	√	—	—	√
PORTJ	PJ0 to PJ7	√	—	—	√
PORTK	PK0 to PK7	√	—	—	√
PORTL	PL0 to PL7	√	—	—	√
PORTM	PM0 to PM7	√	—	—	√
PORTN	PN0 to PN7	√	—	—	√
PORTP	PP0 to PP7	√	—	—	√
PORTR	PR0 to PR7	√	—	—	√
PORTS	PS0 to PS7	√	—	—	√
PORTT	PT0 to PT7	√	—	—	√
PORTU	PU0 to PU7	√	—	—	√

Specifying input pull-up/pull-down or switching of driving ability is available for other signals on pins that also function as general I/O pins.

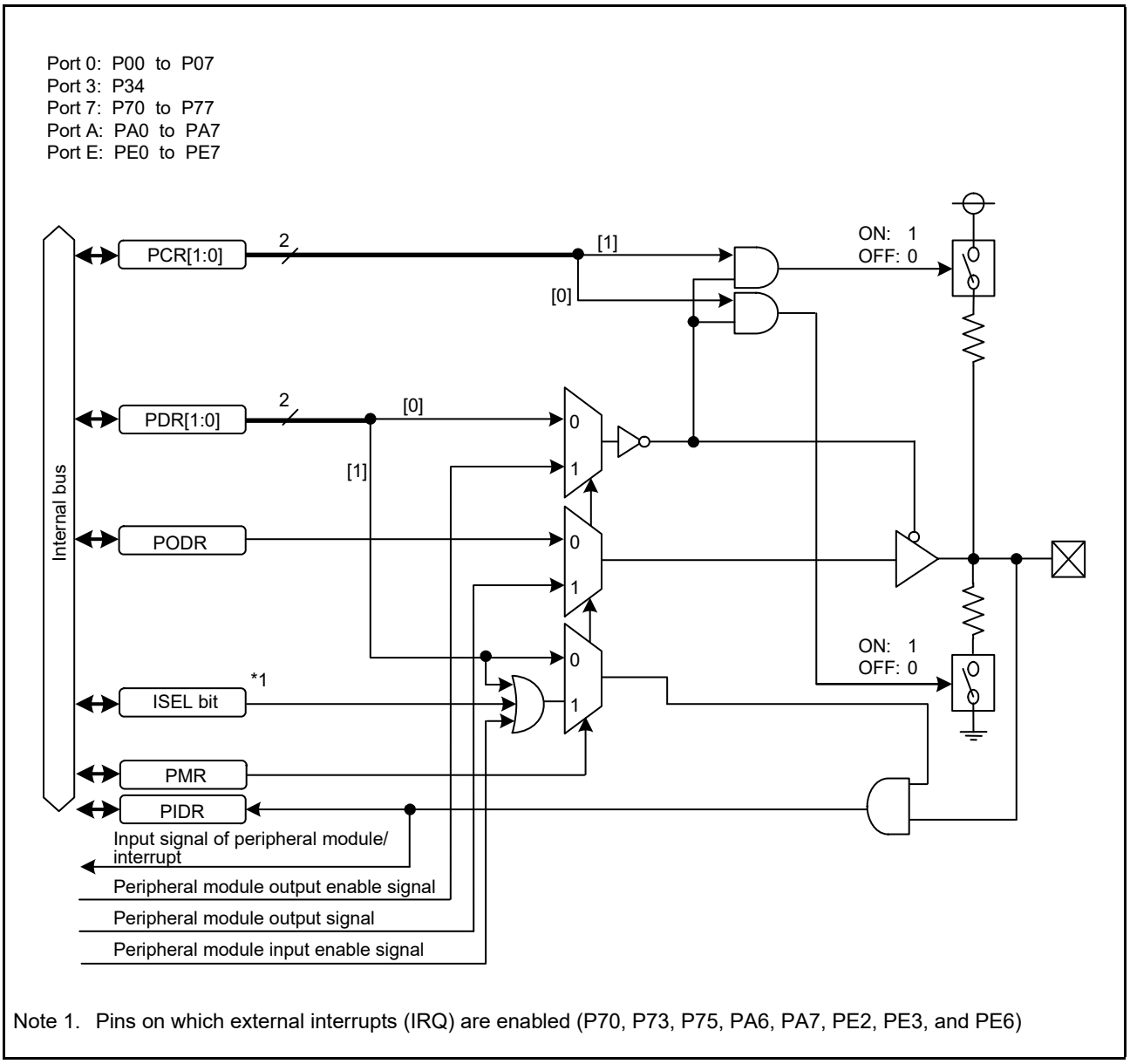
17.2 I/O Port Configuration

Port 1: P11 to P17
Port 2: P20 to P27
Port 3: P31 to P33, P35 to P37
Port 4: P40 to P47
Port 5: P50 to P56
Port 6: P60 to P67
Port 8: P80 to P85
Port B: PB0 to PB7
Port F: PF5 to PF7
Port G: PG0 to PG7
Port H: PH0 to PH7
Port J: PJ0 to PJ7
Port K: PK0 to PK7
Port L: PL0 to PL7
Port M: PM0 to PM7
Port N: PN0 to PN7
Port P: PP0 to PP7
Port R: PR0 to PR7
Port S: PS0 to PS7
Port T: PT0 to PT7
Port U: PU0 to PU7



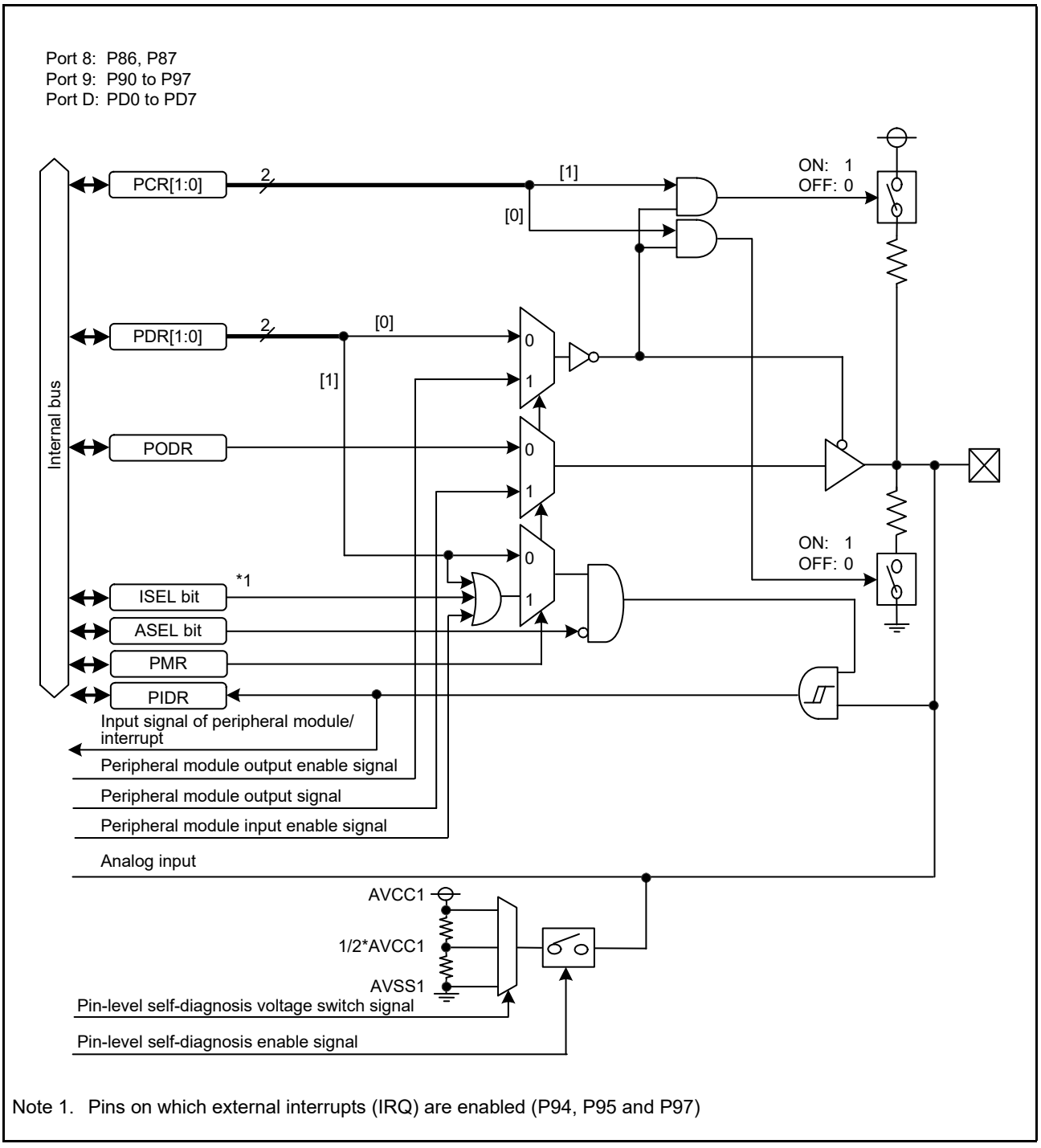
Note 1. Pins on which external interrupts (NMI, IRQ) are enabled (P11, P21, P22, P24, P32, P35, P44, P50, P51, P55, P66, P67, P80, P83, P85, PB3, PF7, PH4, PJ0, PJ2, PJ3, PJ6, PJ7, PL4, PL7, PM6, PN2, PN4, PN5, PR1, PS1, PS6, PT0, PT3, PU2, and PU5)

Figure 17.1 I/O Port Configuration (1)



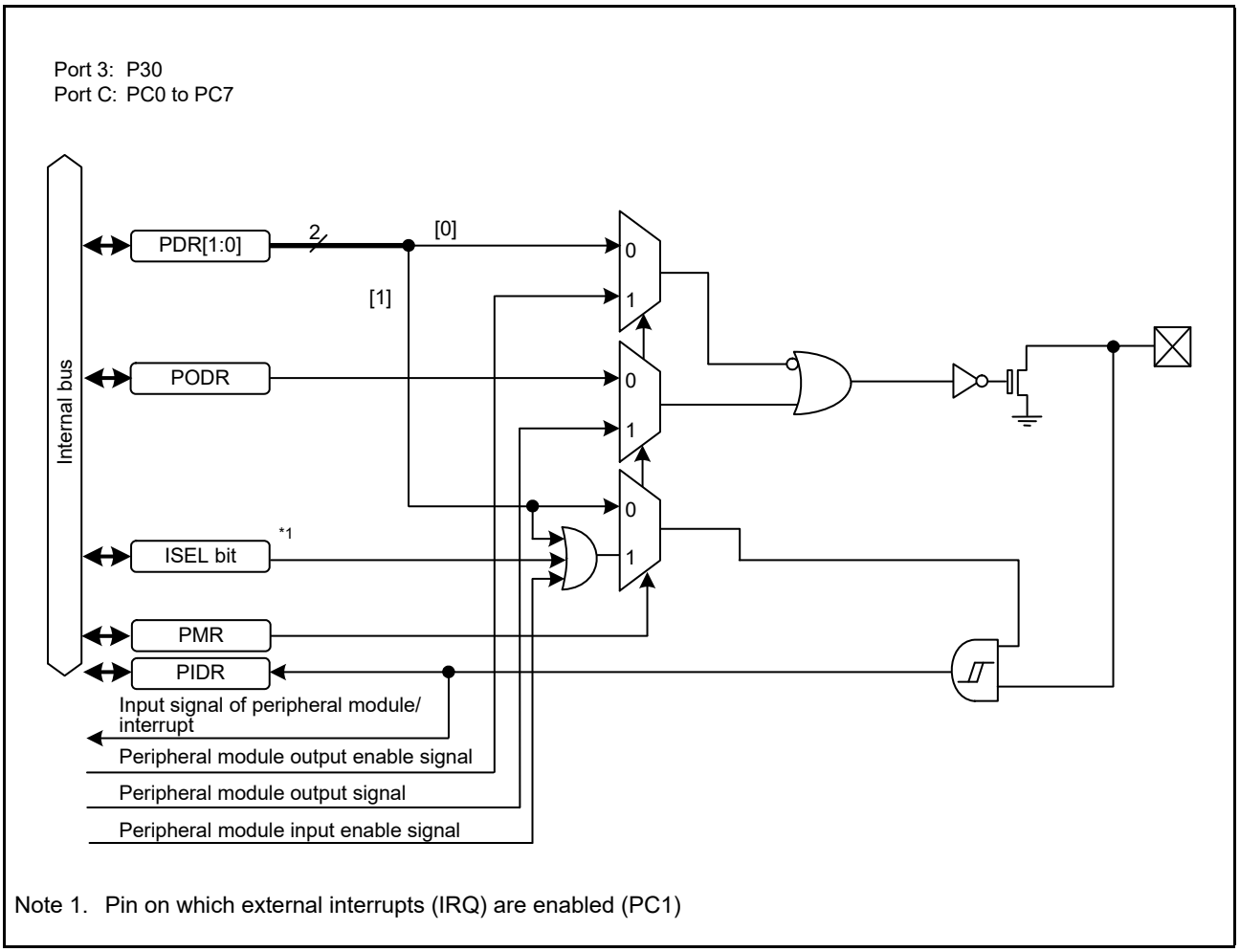
Note 1. Pins on which external interrupts (IRQ) are enabled (P70, P73, P75, PA6, PA7, PE2, PE3, and PE6)

Figure 17.2 I/O Port Configuration (2)



Note 1. Pins on which external interrupts (IRQ) are enabled (P94, P95 and P97)

Figure 17.3 I/O Port Configuration (3)



Note 1. Pin on which external interrupts (IRQ) are enabled (PC1)

Figure 17.4 I/O Port Configuration (4)

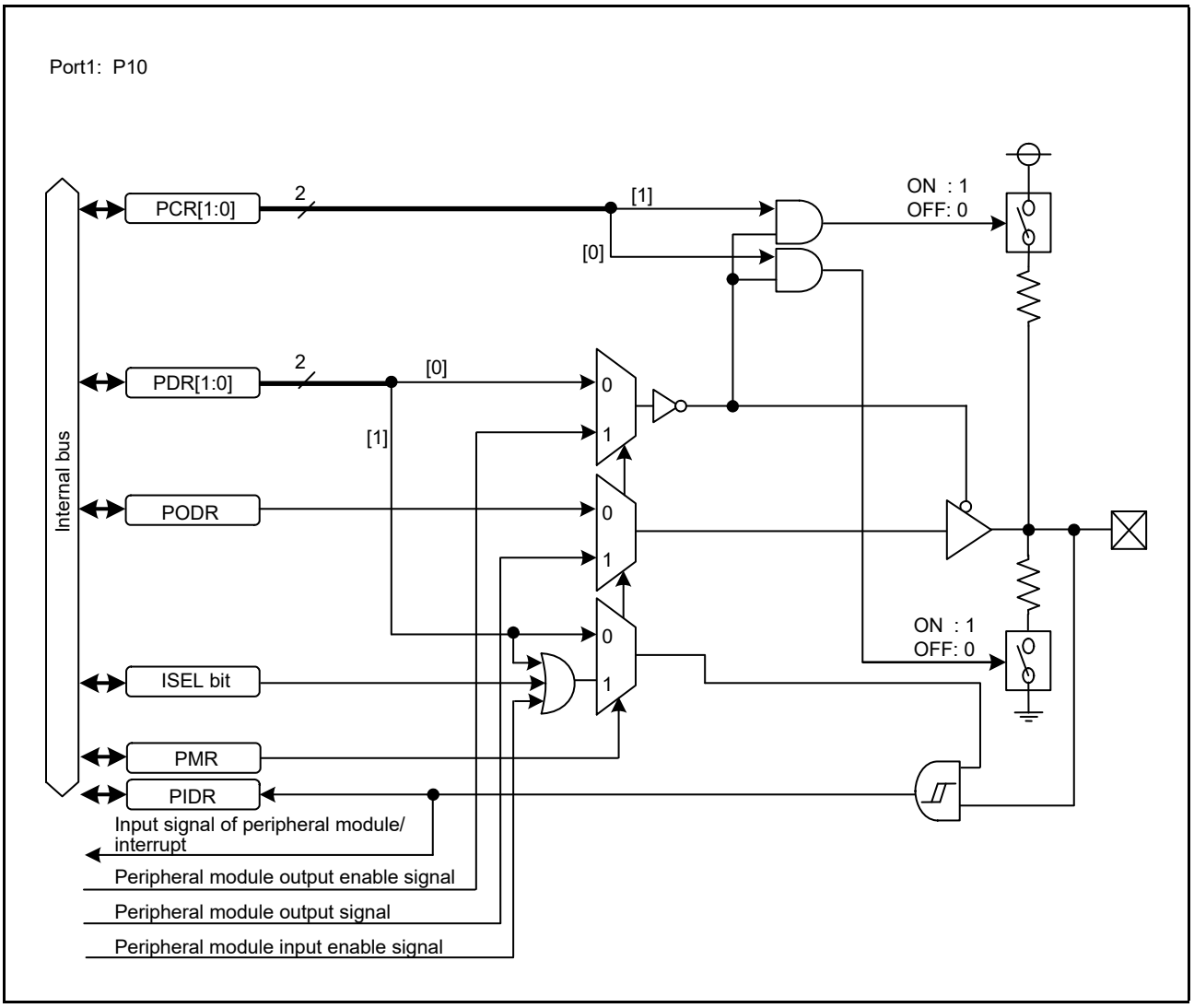


Figure 17.5 I/O Port Configuration (5)

17.3 Register Descriptions

17.3.1 Port Direction Register (PDR)

The PDR register is used to select non-use, input, or output (input enable) for individual pins of the corresponding port when the pins are configured as the general I/O pins. When 00 (non-use) is set to this register, this LSI can be protected from input Hi-Z state.

Address(es): PORT0.PDR A000 0000h, PORT1.PDR A000 0002h, PORT2.PDR A000 0004h, PORT3.PDR A000 0006h, PORT4.PDR A000 0008h, PORT5.PDR A000 000Ah, PORT6.PDR A000 000Ch, PORT7.PDR A000 000Eh, PORT8.PDR A000 0010h, PORT9.PDR A000 0012h, PORTA.PDR A000 0014h, PORTB.PDR A000 0016h, PORTC.PDR A000 0018h, PORTD.PDR A000 001Ah, PORTE.PDR A000 001Ch, PORTF.PDR A000 001Eh, PORTG.PDR A000 0020h, PORTH.PDR A000 0022h, PORTJ.PDR A000 0024h, PORTK.PDR A000 0026h, PORTL.PDR A000 0028h, PORTM.PDR A000 002Ah, PORTN.PDR A000 002Ch, PORTP.PDR A000 002Eh, PORTR.PDR A000 0030h, PORTS.PDR A000 0032h, PORTT.PDR A000 0034h, PORTU.PDR A000 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	B7[1:0]		B6[1:0]		B5[1:0]		B4[1:0]		B3[1:0]		B2[1:0]		B1[1:0]		B0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	B0[1:0]	Pm0 I/O Select	Odd bit Even bit 0 0: Non-use (Hi-Z input protection) 0 1: Setting prohibited 1 0: Input (functions as an input pin) 1 1: Output (functions as an output pin (port read enable))	R/W
b3, b2	B1[1:0]	Pm1 I/O Select		R/W
b5, b4	B2[1:0]	Pm2 I/O Select		R/W
b7, b6	B3[1:0]	Pm3 I/O Select		R/W
b9, b8	B4[1:0]	Pm4 I/O Select		R/W
b11, b10	B5[1:0]	Pm5 I/O Select		R/W
b13, b12	B6[1:0]	Pm6 I/O Select		R/W
b15, b14	B7[1:0]	Pm7 I/O Select		R/W

m = 0 to 9, A to H, J to N, P, and R to U

Each bit of PORTm.PDR corresponds to each pin of port m; pin function can be specified in 2-bit units. However, set the bits that correspond to ports m (ports 9, J to N, P, and R to U) to 00 (non-use) on the 176-pin product.
Write 00 (non-use) or 10 (input) to the PORT3.PDR.B0 and PORTC.PDR.Bn (n = 0 to 7) bits because the P30 and PC0 to PC7 pins are input only.
The bit corresponding to a pin that does not exist is also reserved. A reserved bit is always read as 0. The write value should always be 0.

17.3.2 Port Output Data Register (PODR)

The PODR register holds the data to be output from the pins used for general I/O.

Address(es): PORT0.PODR A000 0040h, PORT1.PODR A000 0041h, PORT2.PODR A000 0042h, PORT3.PODR A000 0043h, PORT4.PODR A000 0044h, PORT5.PODR A000 0045h, PORT6.PODR A000 0046h, PORT7.PODR A000 0047h, PORT8.PODR A000 0048h, PORT9.PODR A000 0049h, PORTA.PODR A000 004Ah, PORTB.PODR A000 004Bh, PORTC.PODR A000 004Ch, PORTD.PODR A000 004Dh, PORTE.PODR A000 004Eh, PORTF.PODR A000 004Fh, PORTG.PODR A000 0050h, PORTH.PODR A000 0051h, PORTJ.PODR A000 0052h, PORTK.PODR A000 0053h, PORTL.PODR A000 0054h, PORTM.PODR A000 0055h, PORTN.PODR A000 0056h, PORTP.PODR A000 0057h, PORTR.PODR A000 0058h, PORTS.PODR A000 0059h, PORTT.PODR A000 005Ah, PORTU.PODR A000 005Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Output Data Store	0: Low output 1: High output	R/W
b1	B1	Pm1 Output Data Store		R/W
b2	B2	Pm2 Output Data Store		R/W
b3	B3	Pm3 Output Data Store		R/W
b4	B4	Pm4 Output Data Store		R/W
b5	B5	Pm5 Output Data Store		R/W
b6	B6	Pm6 Output Data Store		R/W
b7	B7	Pm7 Output Data Store		R/W

m = 0 to 9, A to H, J to N, P, and R to U

Bits that correspond to ports m (ports 9, J to N, P, and R to U) on the 176-pin product are reserved. Be sure to write 0 (low output) to these bits.

The PORT3.PODR.B0 and PORTC.PODR.Bn (n = 0 to 7) bits are reserved because the P30 and PC0 to PC7 pins are input only. The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

17.3.3 Port Input Data Register (PIDR)

The PIDR register reflects the states of the individual input port pins.

Address(es): PORT0.PIDR A000 0060h, PORT1.PIDR A000 0061h, PORT2.PIDR A000 0062h, PORT3.PIDR A000 0063h, PORT4.PIDR A000 0064h, PORT5.PIDR A000 0065h, PORT6.PIDR A000 0066h, PORT7.PIDR A000 0067h, PORT8.PIDR A000 0068h, PORT9.PIDR A000 0069h, PORTA.PIDR A000 006Ah, PORTB.PIDR A000 006Bh, PORTC.PIDR A000 006Ch, PORTD.PIDR A000 006Dh, PORTE.PIDR A000 006Eh, PORTF.PIDR A000 006Fh, PORTG.PIDR A000 0070h, PORTH.PIDR A000 0071h, PORTJ.PIDR A000 0072h, PORTK.PIDR A000 0073h, PORTL.PIDR A000 0074h, PORTM.PIDR A000 0075h, PORTN.PIDR A000 0076h, PORTP.PIDR A000 0077h, PORTR.PIDR A000 0078h, PORTS.PIDR A000 0079h, PORTT.PIDR A000 007Ah, PORTU.PIDR A000 007Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0	0: Low input 1: High input	R
b1	B1	Pm1		R
b2	B2	Pm2		R
b3	B3	Pm3		R
b4	B4	Pm4		R
b5	B5	Pm5		R
b6	B6	Pm6		R
b7	B7	Pm7		R

m = 0 to 9, A to H, J to N, P, and R to U

If PORTm.PDR is set to 10 or 11, the pin states of ports m can be read with PORTm.PIDR, regardless of the values of PORTm.PMR.

The bit corresponding to a pin that does not exist is reserved. A reserved bit is read as undefined, and cannot be modified.

17.3.4 Port Mode Register (PMR)

The PMR register specifies the function of the pins of the port.

Address(es): PORT0.PMR A000 0080h, PORT1.PMR A000 0081h, PORT2.PMR A000 0082h, PORT3.PMR A000 0083h, PORT4.PMR A000 0084h, PORT5.PMR A000 0085h, PORT6.PMR A000 0086h, PORT7.PMR A000 0087h, PORT8.PMR A000 0088h, PORT9.PMR A000 0089h, PORTA.PMR A000 008Ah, PORTB.PMR A000 008Bh, PORTC.PMR A000 008Ch, PORTD.PMR A000 008Dh, PORTE.PMR A000 008Eh, PORTF.PMR A000 008Fh, PORTG.PMR A000 0090h, PORTH.PMR A000 0091h, PORTJ.PMR A000 0092h, PORTK.PMR A000 0093h, PORTL.PMR A000 0094h, PORTM.PMR A000 0095h, PORTN.PMR A000 0096h, PORTP.PMR A000 0097h, PORTR.PMR A000 0098h, PORTS.PMR A000 0099h, PORTT.PMR A000 009Ah, PORTU.PMR A000 009Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	B7	B6	B5	B4	B3	B2	B1	B0
Value after reset: *1	0	0	0	0	0	0	0	0

Note 1. The PMR register value for port 3 after a reset is 18h.

Bit	Symbol	Bit Name	Description	R/W
b0	B0	Pm0 Pin Mode Control	0: Uses the pin as a general I/O pin 1: Uses the pin as an I/O port for peripheral functions	R/W
b1	B1	Pm1 Pin Mode Control		R/W
b2	B2	Pm2 Pin Mode Control		R/W
b3	B3	Pm3 Pin Mode Control		R/W
b4	B4	Pm4 Pin Mode Control		R/W
b5	B5	Pm5 Pin Mode Control		R/W
b6	B6	Pm6 Pin Mode Control		R/W
b7	B7	Pm7 Pin Mode Control		R/W

m = 0 to 9, A to H, J to N, P, and R to U

Each bit of PORTm.PMR corresponds to each pin of port m; pin function can be specified in 1-bit units. Bits that correspond to ports m (ports 9, J to N, P, and R to U) on the 176-pin product are reserved. Be sure to write 0 (general I/O port) to these bits. The bit corresponding to a pin that does not exist is reserved. A reserved bit is always read as 0. The write value should always be 0.

17.3.5 Pull-Up/Pull-Down Control Register (PCR)

The PCR register enables or disables an input pull-up or pull-down resistor for each pin of the port.
When a pin for the general port or peripheral module is in the input state, the input pull-up resistor connected to the pin with the corresponding bit in PORTm.PCR set to 10 is enabled, and the input pull-down resistor connected to the pin with the corresponding bit in PORTm.PCR set to 01 is enabled.
When a pin is set as a general port output pin or a peripheral module output pin, the pull-up resistor for the pin is disabled regardless of the settings of PCR. Note that the P30 and PC0 to PC7 pins do not have his function.
The pull-up and pull-down resistors are also disabled in the reset state.

Address(es): PORT0.PCR A000 0100h, PORT1.PCR A000 0102h, PORT2.PCR A000 0104h, PORT3.PCR A000 0106h, PORT4.PCR A000 0108h, PORT5.PCR A000 010Ah, PORT6.PCR A000 010Ch, PORT7.PCR A000 010Eh, PORT8.PCR A000 0110h, PORT9.PCR A000 0112h, PORTA.PCR A000 0114h, PORTB.PCR A000 0116h, PORTD.PCR A000 011Ah, PORTE.PCR A000 011Ch, PORTF.PCR A000 011Eh, PORTG.PCR A000 0120h, PORTH.PCR A000 0122h, PORTJ.PCR A000 0124h, PORTK.PCR A000 0126h, PORTL.PCR A000 0128h, PORTM.PCR A000 012Ah, PORTN.PCR A000 012Ch, PORTP.PCR A000 012Eh, PORTR.PCR A000 0130h, PORTS.PCR A000 0132h, PORTT.PCR A000 0134h, PORTU.PCR A000 0136h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	B7[1:0]		B6[1:0]		B5[1:0]		B4[1:0]		B3[1:0]		B2[1:0]		B1[1:0]		B0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	B0[1:0]	Pm0 Input Pull-Up/Pull-Down Resistor Control	Odd bit Even bit 0 0: Disables an input pull-up and pull-down resistors 0 1: Enables an input pull-down resistor 1 0: Enables an input pull-up resistor 1 1: Setting prohibited	R/W
b3, b2	B1[1:0]	Pm1 Input Pull-Up/Pull-Down Resistor Control		R/W
b5, b4	B2[1:0]	Pm2 Input Pull-Up/Pull-Down Resistor Control		R/W
b7, b6	B3[1:0]	Pm3 Input Pull-Up/Pull-Down Resistor Control		R/W
b9, b8	B4[1:0]	Pm4 Input Pull-Up/Pull-Down Resistor Control		R/W
b11, b10	B5[1:0]	Pm5 Input Pull-Up/Pull-Down Resistor Control		R/W
b13, b12	B6[1:0]	Pm6 Input Pull-Up/Pull-Down Resistor Control		R/W
b15, b14	B7[1:0]	Pm7 Input Pull-Up/Pull-Down Resistor Control		R/W

m = 0 to 9, A to H, J to N, P, and R to U

The bit corresponding to a pin that does not exist is also reserved. A reserved bit is always read as 00b. The write value should always be 00b.

17.3.6 Driving Ability Control Register (DSCR)

The DSCR register controls driving ability of the ports.
Set the CKIO pin to high-drive output by this register if SDRAM (TYPE[2:0] = 100b) is to be selected in the CSn space bus control register (CSnBCR).

Address(es): PORT1.DSCR A000 0142h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	B0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	B0	P10 Driving Ability Control	0: Normal output 1: High-drive output	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The bit corresponding to a pin that does not exist is also reserved. A reserved bit is always read as 0. The write value should always be 0.

Note: Select high-drive output when connecting the SDRAM.

17.4 Handling of Unused Pins

Table 17.3 lists the details of handling of unused pins.

Table 17.3 Handling of Unused Pins

Pin Name	Handling
MD0, MD1, MD2	— (Use this as a mode pin.)
BSCANP	— (Use this as a boundary scan enable pin.)
OSCTH	— (Use this as a clock input mode pin.)
EXTAL	— (Use this as a crystal oscillator connection pin or external clock input pin.)
XTAL	Keep this pin open.
ERROROUT#	Keep this pin open.
RSTOUT#	Keep this pin open.
TRST#	Connect these pins to VSS via a resistor (pulling down), or input the same signal as that on the RES# pin.
TCK	Connect these pins to VSS via a resistor (pulling down).
TMS	Connect this pin to VCCQ33 via a resistor (pulling up).
Port 34 (TDI)	Connect this pin to VCCQ33 via a resistor (pulling up).
Port 0 to Port 9, Port A to Port H, Port J to Port N, Port P, and Port R to Port U (except Port 34)*1	Keep these pins open, connect them to VCCQ33 via a resistor (pulling up), or connect them to VSS via a resistor (pulling down).
USB0_DP USB0_DM	Keep these pins open.
USB_RREF	Keep this pin open.
VREFH0	Connect this pin to AVCC0.
VREFL0	Connect this pin to AVSS0.
VREFH1	Connect this pin to AVCC1.
VREFL1	Connect this pin to AVSS1.
AN000 to AN007	Connect these pins to AVSS0 via a resistor (pulling down).

Note 1. When handling them as unused pins, set the corresponding bits of the port direction register (PDR) to “Non-use (Hi-Z input protection)” which is the value after reset release.

18. Multi-Function Pin Controller (MPC)

18.1 Overview

This LSI configures an I/O pin or an interrupt pin of peripheral functions to be multiplexed with multiple ports. The multi-function pin controller (MPC) is a module that selects I/O pins and interrupt pins for the peripheral function to use from multiple ports, and then assigns the function to the selected pins.
Table 18.1 lists the multiplexed pin configurations.Y and N in the table indicate whether the pin is available or unavailable for the package. Selecting a single function for multiple pins is prohibited.

Table 18.1 List of Multiplexed Pin Configurations (1 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Debugging interface		TDI (input)	P34	Y	Y
		TDO (output)	P33	Y	Y
		TRACECLK (output)	P10	Y	Y
			P70	Y	Y
			PP7	Y	N
		TRACECTL (output)	P00	Y	Y
			P71	Y	Y
			PP6	Y	N
		TRACEDATA0 (output)	P72	Y	Y
			PE0	Y	Y
			PR0	Y	N
		TRACEDATA1 (output)	P73	Y	Y
			PE1	Y	Y
			PR1	Y	N
		TRACEDATA2 (output)	P74	Y	Y
			PE2	Y	Y
			PR2	Y	N
		TRACEDATA3 (output)	P75	Y	Y
			PE3	Y	Y
			PR3	Y	N
		TRACEDATA4 (output)	P76	Y	Y
			PE4	Y	Y
			PR4	Y	N
		TRACEDATA5 (output)	P77	Y	Y
			PE5	Y	Y
			PR5	Y	N
		TRACEDATA6 (output)	PA0	Y	Y
			PE6	Y	Y
			PR6	Y	N
		TRACEDATA7 (output)	PA1	Y	Y
			PE7	Y	Y
			PR7	Y	N

Table 18.1 List of Multiplexed Pin Configurations (2 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
External bus controller		A0 (output)	P23	Y	Y
		A1 (output)	PG0	Y	Y
		A2 (output)	PG1	Y	Y
		A3 (output)	PG2	Y	Y
		A4 (output)	PG3	Y	Y
		A5 (output)	PG4	Y	Y
		A6 (output)	PG5	Y	Y
		A7 (output)	PG6	Y	Y
		A8 (output)	PG7	Y	Y
		A9 (output)	PH0	Y	Y
		A10 (output)	PH1	Y	Y
		A11 (output)	PH2	Y	Y
		A12 (output)	PH3	Y	Y
		A13 (output)	PH4	Y	Y
		A14 (output)	PH5	Y	Y
		A15 (output)	PH6	Y	Y
		A16 (output)	PH7	Y	Y
		A17 (output)	P20	Y	Y
		A18 (output)	P25	Y	Y
		A19 (output)	P26	Y	Y
		A20 (output)	P27	Y	Y
		A21 (output)	PA6	Y	Y
			PD5	Y	Y
			PT6	Y	N
		A22 (output)	PA7	Y	Y
			PD6	Y	Y
			PT7	Y	N
		A23 (output)	P87	Y	Y
			PK2	Y	N
		A24 (output)	P55	Y	N
			PB4	Y	Y
			PK3	Y	N
		A25 (output)	P97	Y	N
			PF7	Y	N
		D0 (input/output)	P00	Y	Y
		D1 (input/output)	P01	Y	Y
		D2 (input/output)	P02	Y	Y
		D3 (input/output)	P03	Y	Y
		D4 (input/output)	P04	Y	Y
		D5 (input/output)	P05	Y	Y
		D6 (input/output)	P06	Y	Y
		D7 (input/output)	P07	Y	Y
		D8 (input/output)	PE0	Y	Y
		D9 (input/output)	PE1	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (3 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
External bus controller		D10 (input/output)	PE2	Y	Y
		D11 (input/output)	PE3	Y	Y
		D12 (input/output)	PE4	Y	Y
		D13 (input/output)	PE5	Y	Y
		D14 (input/output)	PE6	Y	Y
		D15 (input/output)	PE7	Y	Y
		D16 (input/output)	P70	Y	Y
		D17 (input/output)	P71	Y	Y
		D18 (input/output)	P72	Y	Y
		D19 (input/output)	P73	Y	Y
		D20 (input/output)	P74	Y	Y
		D21 (input/output)	P75	Y	Y
		D22 (input/output)	P76	Y	Y
		D23 (input/output)	P77	Y	Y
		D24 (input/output)	PA0	Y	Y
		D25 (input/output)	PA1	Y	Y
		D26 (input/output)	PA2	Y	Y
		D27 (input/output)	PA3	Y	Y
		D28 (input/output)	PA4	Y	Y
		D29 (input/output)	PA5	Y	Y
		D30 (input/output)	PA6	Y	Y
		D31 (input/output)	PA7	Y	Y
		CKIO (output)	P10	Y	Y
		CS0# (output)	P21	Y	Y
		CS1# (output)	P50	Y	N
			PB3	Y	Y
			PD1	Y	N
		CS2# (output)	P16	Y	Y
			P45	Y	N
		CS3# (output)	P15	Y	Y
			PT4	Y	N
		CS4# (output)	P16	Y	Y
			PD0	Y	N
		CS5# (output)	P17	Y	Y
			P92	Y	N
			PK1	Y	N
		RD# (output)	P22	Y	Y
		RD/WR# (output)	P24	Y	Y
		BS# (output)	P41	Y	N
			P56	Y	Y
			PT5	Y	N
		WAIT# (input)	P44	Y	N
			PC0	Y	Y
			PD2	Y	N

Table 18.1 List of Multiplexed Pin Configurations (4 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
External bus controller		WE0#/DQMLL (output)	P36	Y	Y
		WE1#/DQMLU (output)	P37	Y	Y
		WE2#/DQMUL (output)	P43	Y	Y
		WE3#/DQMUU/AH# (output)	P47	Y	Y
		RAS# (output)	P13	Y	Y
			P90	Y	N
		CAS# (output)	P14	Y	Y
			P91	Y	N
			PK0	Y	N
		CKE (output)	P15	Y	Y
			P46	Y	N
Direct memory access controller	DMAC0	DREQ0 (input)	P65	Y	Y
			PC6	Y	N
			PN7	Y	N
		DACK0 (output)	P61	Y	Y
			P66	Y	N
			PP1	Y	N
		TEND0 (output)	P60	Y	Y
			P67	Y	N
			PP0	Y	N
	DMAC1	DREQ1 (input)	P26	Y	Y
			PR0	Y	N
		DACK1 (output)	P23	Y	Y
			PP7	Y	N
		TEND1 (output)	P25	Y	Y
			PR1	Y	N
	DMAC2	DREQ2 (input)	PA2	Y	Y
			PT6	Y	N
		DACK2 (output)	PA3	Y	Y
			PT7	Y	N
		TEND2 (output)	PA4	Y	Y
			PT5	Y	N

Table 18.1 List of Multiplexed Pin Configurations (5 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Interrupt	NMI	NMI (input)	P35	Y	Y
	IRQ0	IRQ0 (input)	P10	Y	Y
			P70	Y	Y
			PT0	Y	N
	IRQ1	IRQ1 (input)	P21	Y	Y
			P51	Y	Y
			PS1	Y	N
	IRQ2	IRQ2 (input)	P22	Y	Y
			PE2	Y	Y
			PU2	Y	N
	IRQ3	IRQ3 (input)	P73	Y	Y
			PB3	Y	Y
			PE3	Y	Y
	IRQ4	IRQ4 (input)	P94	Y	N
			PH4	Y	Y
			PL4	Y	N
	IRQ5	IRQ5 (input)	P55	Y	N
			P85	Y	Y
			PN5	Y	N
	IRQ6	IRQ6 (input)	PA6	Y	Y
			PE6	Y	Y
			PM6	Y	N
	IRQ7	IRQ7 (input)	P97	Y	N
			PA7	Y	Y
			PF7	Y	N

Table 18.1 List of Multiplexed Pin Configurations (6 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Interrupt	IRQ8	IRQ8 (input)	P50	Y	N
			P80	Y	N
			PJ0	Y	N
	IRQ9	IRQ9 (input)	P11	Y	N
			PC1	Y	Y
			PR1	Y	N
	IRQ10	IRQ10 (input)	P32	Y	N
			PJ2	Y	N
			PN2	Y	N
	IRQ11	IRQ11 (input)	P83	Y	N
			PJ3	Y	N
			PT3	Y	N
	IRQ12	IRQ12 (input)	P24	Y	Y
			P44	Y	N
			PN4	Y	N
	IRQ13	IRQ13 (input)	P75	Y	Y
			P95	Y	N
			PU5	Y	N
	IRQ14	IRQ14 (input)	P66	Y	N
			PJ6	Y	N
			PS6	Y	N
	IRQ15	IRQ15 (input)	P67	Y	N
			PJ7	Y	N
			PL7	Y	N
Multi-function timer unit 3	MTU0	MTIOC0A (input/output)	PE6	Y	Y
			PP4	Y	N
		MTIOC0B (input/output)	PE4	Y	Y
			PP3	Y	N
		MTIOC0C (input/output)	PE5	Y	Y
			PP2	Y	N
		MTIOC0D (input/output)	PE3	Y	Y
			PP1	Y	N
	MTU1	MTIOC1A (input/output)	P72	Y	Y
			P93	Y	N
			PB2	Y	Y
		MTIOC1B (input/output)	PE0	Y	Y
			PH3	Y	Y
	MTU2	MTIOC2A (input/output)	P07	Y	Y
			PH2	Y	Y
		MTIOC2B (input/output)	P06	Y	Y
			PH1	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (7 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Multi-function timer unit 3	MTU3	MTIOC3A (input/output)	P05	Y	Y
			PN7	Y	N
		MTIOC3B (input/output)	P16	Y	Y
			PA2	Y	Y
			PB7	Y	Y
		MTIOC3C (input/output)	P04	Y	Y
			PN6	Y	N
		MTIOC3D (input/output)	P15	Y	Y
			PA1	Y	Y
			PF6	Y	Y
	MTU4	MTIOC4A (input/output)	P14	Y	Y
			PA0	Y	Y
			PF5	Y	Y
		MTIOC4B (input/output)	P12	Y	N
			P76	Y	Y
			P86	Y	Y
		MTIOC4C (input/output)	P13	Y	Y
			P77	Y	Y
			P87	Y	Y
		MTIOC4D (input/output)	P11	Y	N
			P75	Y	Y
			PD7	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (8 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Multi-function timer unit 3	MTU5	MTIC5U (input)	P03	Y	Y
			P23	Y	Y
		MTIC5V (input)	P02	Y	Y
			P21	Y	Y
		MTIC5W (input)	P01	Y	Y
			PH7	Y	Y
	MTU6	MTIOC6A (input/output)	P00	Y	Y
			PN5	Y	N
		MTIOC6B (input/output)	PA7	Y	Y
			PS5	Y	N
		MTIOC6C (input/output)	P47	Y	Y
			PN4	Y	N
		MTIOC6D (input/output)	P70	Y	Y
			PS4	Y	N
	MTU7	MTIOC7A (input/output)	PE7	Y	Y
			PS3	Y	N
		MTIOC7B (input/output)	P22	Y	Y
			PS1	Y	N
		MTIOC7C (input/output)	P42	Y	Y
			PS2	Y	N
		MTIOC7D (input/output)	PH6	Y	Y
			PS0	Y	N
	MTU8	MTIOC8A (input/output)	P40	Y	Y
			PN3	Y	N
		MTIOC8B (input/output)	P43	Y	Y
			PN2	Y	N
		MTIOC8C (input/output)	P27	Y	Y
			PN1	Y	N
		MTIOC8D (input/output)	P26	Y	Y
			PN0	Y	N
	MTU	MTCLKA (input)	P74	Y	Y
			P95	Y	N
			PB1	Y	Y
		MTCLKB (input)	P73	Y	Y
			P94	Y	N
			PB0	Y	Y
		MTCLKC (input)	P25	Y	Y
			PE2	Y	Y
		MTCLKD (input)	P20	Y	Y
			PE1	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (9 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Port output enable 3	POE0	POE0# (input)	P71	Y	Y
			P96	Y	N
			PB5	Y	Y
	POE4	POE4# (input)	PR1	Y	N
	POE8	POE8# (input)	PE7	Y	Y
			PP0	Y	N
	POE10	POE10# (input)	P71	Y	Y
			P96	Y	N
			PB5	Y	Y
General PWM timer	GPT0	GTIOC0A (input/output)	P16	Y	Y
			PA2	Y	Y
			PB7	Y	Y
		GTIOC0B (input/output)	P15	Y	Y
			PA1	Y	Y
			PF6	Y	Y
	GPT1	GTIOC1A (input/output)	P14	Y	Y
			PA0	Y	Y
			PF5	Y	Y
		GTIOC1B (input/output)	P13	Y	Y
			P77	Y	Y
			P87	Y	Y
	GPT2	GTIOC2A (input/output)	P12	Y	N
			P76	Y	Y
			P86	Y	Y
		GTIOC2B (input/output)	P11	Y	N
			P75	Y	Y
			PD7	Y	Y
	GPT3	GTIOC3A (input/output)	P66	Y	N
			PA6	Y	Y
		GTIOC3B (input/output)	P67	Y	N
			PA7	Y	Y
	GPT	GTETRG (input)	PC0	Y	Y
			PA3	Y	Y
16-bit timer pulse unit	TPU0 (unit 0)	TIOCA0 (input/output)	P10	Y	Y
			PT3	Y	N
		TIOCB0 (input/output)	P06	Y	Y
			P27	Y	Y
			PT3	Y	N
		TIOCC0 (input/output)	P81	Y	N
			PE4	Y	Y
		TIOCD0 (input/output)	P22	Y	Y
			PE6	Y	Y
			PJ5	Y	N

Table 18.1 List of Multiplexed Pin Configurations (10 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
16-bit timer pulse unit	TPU1 (unit 0)	TIOCA1 (input/output)	P00	Y	Y
			PT2	Y	N
		TIOCB1 (input/output)	P07	Y	Y
			P21	Y	Y
			PT2	Y	N
	TPU2 (unit 0)	TIOCA2 (input/output)	P01	Y	Y
			PA3	Y	Y
			PT1	Y	N
		TIOCB2 (input/output)	PE0	Y	Y
			PT1	Y	N
	TPU3 (unit 0)	TIOCA3 (input/output)	P02	Y	Y
			PA4	Y	Y
			PT0	Y	N
		TIOCB3 (input/output)	PE1	Y	Y
			PT0	Y	N
		TIOCC3 (input/output)	P80	Y	N
			PE5	Y	Y
		TIOCD3 (input/output)	P82	Y	Y
			PE7	Y	Y
	TPU4 (unit 0)	TIOCA4 (input/output)	P03	Y	Y
			PA5	Y	Y
			PS7	Y	N
		TIOCB4 (input/output)	PE2	Y	Y
			PS7	Y	N
	TPU5 (unit 0)	TIOCA5 (input/output)	P04	Y	Y
			P90	Y	N
			PS6	Y	N
		TIOCB5 (input/output)	PE3	Y	Y
			PS6	Y	N
	TPU (unit 0)	TCLKA (input)	PB6	Y	Y
			PG5	Y	Y
		TCLKB (input)	PB5	Y	Y
			PG6	Y	Y
		TCLKC (input)	PB1	Y	Y
			PC6	Y	N
			PP3	Y	N
		TCLKD (input)	P44	Y	N
			PB0	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (11 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
16-bit timer pulse unit	TPU6 (unit 1)	TIOCA6 (input/output)	PL2	Y	N
			PR7	Y	N
		TIOCB6 (input/output)	PK6	Y	N
			PR7	Y	N
		TIOCC6 (input/output)	PN4	Y	N
			PU5	Y	N
		TIOCD6 (input/output)	PN7	Y	N
			PU3	Y	N
	TPU7 (unit 1)	TIOCA7 (input/output)	PL3	Y	N
			PR6	Y	N
		TIOCB7 (input/output)	PK7	Y	N
			PR6	Y	N
	TPU8 (unit 1)	TIOCA8 (input/output)	PL5	Y	N
			PR5	Y	N
		TIOCB8 (input/output)	PK5	Y	N
			PR5	Y	N
	TPU9 (unit 1)	TIOCA9 (input/output)	PL6	Y	N
			PR4	Y	N
		TIOCB9 (input/output)	PL0	Y	N
			PR4	Y	N
		TIOCC9 (input/output)	PU4	Y	N
			PN6	Y	N
		TIOCD9 (input/output)	PU2	Y	N
			PN5	Y	N
	TPU10 (unit 1)	TIOCA10 (input/output)	PR3	Y	N
			PU0	Y	N
		TIOCB10 (input/output)	PL1	Y	N
			PR3	Y	N
	TPU11 (unit 1)	TIOCA11 (input/output)	PP6	Y	N
			PR2	Y	N
			PU1	Y	N
		TIOCB11 (input/output)	PK4	Y	N
			PR2	Y	N
	TPU (unit 1)	TCLKE (input)	PM2	Y	N
			PR0	Y	N
		TCLKF (input)	PP7	Y	N
			PU6	Y	N
		TCLKG (input)	PC5	Y	N
			PR0	Y	N
		TCLKH (input)	PC4	Y	N
			PP2	Y	N
			PP7	Y	N

Table 18.1 List of Multiplexed Pin Configurations (12 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Programmable pulse generator	PPG0	PO0 (output)	P36	Y	Y
		PO1 (output)	P37	Y	Y
		PO2 (output)	PG0	Y	Y
		PO3 (output)	PG1	Y	Y
		PO4 (output)	PG2	Y	Y
		PO5 (output)	PG3	Y	Y
		PO6 (output)	PG4	Y	Y
		PO7 (output)	PG5	Y	Y
		PO8 (output)	PG6	Y	Y
		PO9 (output)	PG7	Y	Y
		PO10 (output)	PH0	Y	Y
		PO11 (output)	PH1	Y	Y
		PO12 (output)	PH2	Y	Y
		PO13 (output)	PH3	Y	Y
		PO14 (output)	PH4	Y	Y
		PO15 (output)	PH5	Y	Y
	PPG1	PO16 (output)	PM3	Y	N
		PO17 (output)	PM4	Y	N
		PO18 (output)	PM5	Y	N
		PO19 (output)	PM6	Y	N
		PO20 (output)	PM7	Y	N
		PO21 (output)	PN1	Y	N
		PO22 (output)	PP5	Y	N
		PO23 (output)	PS6	Y	N
		PO24 (output)	PS7	Y	N
		PO25 (output)	PT0	Y	N
		PO26 (output)	PT1	Y	N
		PO27 (output)	PT2	Y	N
		PO28 (output)	PT3	Y	N
		PO29 (output)	PT4	Y	N
		PO30 (output)	PT5	Y	N
		PO31 (output)	PK0	Y	N

Table 18.1 List of Multiplexed Pin Configurations (13 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Compare match timer W	CMTW0	TOC0 (output)	PD7	Y	Y
			PG2	Y	Y
		TIC0 (input)	PC7	Y	N
			PD5	Y	Y
	CMTW1	TOC1 (output)	P86	Y	Y
			PG4	Y	Y
		TIC1 (input)	PD6	Y	Y
			PG3	Y	Y
	CMTW2	TOC2 (output)	P71	Y	Y
			PF6	Y	Y
		TIC2 (input)	P72	Y	Y
			PF5	Y	Y
	CMTW3	TOC3 (output)	P92	Y	N
			PB7	Y	Y
		TIC3 (input)	P93	Y	N
			PB0	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (14 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Serial Communications Interface with FIFO (SCIFA)	SCI0	RXD0 (input)	P24	Y	Y
			P42	Y	Y
		TXD0 (output)	P23	Y	Y
			P40	Y	Y
		SCK0 (input/output)	P22	Y	Y
			P41	Y	N
		CTS0# (input/output)	P21	Y	Y
			P44	Y	N
		RTS0# (output)	P27	Y	Y
			PH6	Y	Y
	SCI1	RXD1 (input)	P73	Y	Y
			PE6	Y	Y
			PP6	Y	N
		TXD1 (output)	P72	Y	Y
			PE5	Y	Y
			PR0	Y	N
		SCK1 (input/output)	P71	Y	Y
			PE7	Y	Y
			PP7	Y	N
		CTS1# (input/output)	P74	Y	Y
			PE3	Y	Y
			PR1	Y	N
		RTS1# (output)	P70	Y	Y
			PE4	Y	Y
			PR2	Y	N
	SCI2	RXD2 (input)	P92	Y	N
			PA4	Y	Y
			PS6	Y	N
		TXD2 (output)	P91	Y	N
			PA5	Y	Y
			PS7	Y	N
		SCK2 (input/output)	P93	Y	N
			PA3	Y	Y
			PT0	Y	N
		CTS2# (input/output)	P95	Y	N
			PA6	Y	Y
			PT3	Y	N
		RTS2# (output)	P94	Y	N
			PA7	Y	Y
			PT1	Y	N

Table 18.1 List of Multiplexed Pin Configurations (15 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Serial Communications Interface with FIFO (SCIFA)	SCI3	RXD3 (input)	PB4	Y	Y
			PJ5	Y	N
			PU2	Y	N
		TXD3 (output)	PB3	Y	Y
			PJ4	Y	N
			PU3	Y	N
		SCK3 (input/output)	PB6	Y	Y
			PJ6	Y	N
			PU1	Y	N
		CTS3# (input/output)	PB5	Y	Y
			PJ7	Y	N
			PU4	Y	N
		RTS3# (output)	P82	Y	Y
			PF7	Y	N
			PU5	Y	N
	SCI4	RXD4 (input)	P84	Y	N
			PC3	Y	Y
			PU7	Y	N
		TXD4 (output)	P83	Y	N
			P85	Y	Y
			P90	Y	N
			PM0	Y	N
		SCK4 (input/output)	P82	Y	Y
			P85	Y	Y
			PM1	Y	N
		CTS4# (input/output)	P81	Y	N
			PB1	Y	Y
			PU6	Y	N
		RTS4# (output)	P80	Y	N
			PB6	Y	Y
			PM2	Y	N
I^2C bus interface	RIIC0	SCL0 (input/output)	PC3	Y	Y
			PC4	Y	N
		SDA0 (input/output)	PC2	Y	Y
			PC5	Y	N
	RIIC1	SCL1 (input/output)	PC0	Y	Y
			PC6	Y	N
		SDA1 (input/output)	PC1	Y	Y
			PC7	Y	N

Table 18.1 List of Multiplexed Pin Configurations (16 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Ethernet controller	Ether0	CLKOUT25M0 (output)	P85	Y	Y
		ETH0_TXC (input)	PC2	Y	Y
		ETH0_TXEN (output)	P82	Y	Y
		ETH0_TXER (output)	PF7	Y	N
		ETH0_TXD0 (output)	PD5	Y	Y
			PJ3	Y	N
		ETH0_TXD1 (output)	PD6	Y	Y
			PJ2	Y	N
		ETH0_TXD2 (output)	PJ1	Y	N
		ETH0_TXD3 (output)	PJ0	Y	N
		ETH0_INT (input)	P52	Y	N
			PA5	Y	Y
		ETH0_RXC (input)	PC3	Y	Y
		ETH0_RXDV (input)	P80	Y	N
			PC3	Y	Y
		ETH0_RXER (input)	P81	Y	N
			PB4	Y	Y
		ETH0_RXD0 (input)	P87	Y	Y
			PJ4	Y	N
		ETH0_RXD1 (input)	PB2	Y	Y
			PJ5	Y	N
		ETH0_RXD2 (input)	PJ6	Y	N
		ETH0_RXD3 (input)	PJ7	Y	N
		ETH0_CRS (input)	P83	Y	N
		ETH0_COL (input)	P84	Y	N
		PHYLINK0 (input)	P50	Y	N
			PC1	Y	Y
		ETH_MDC (output)	PB6	Y	Y
		ETH_MDIO (input/output)	PB5	Y	Y
		ETHSWSECOUT (output)	P55	Y	N
			PA3	Y	Y
		PHYRESETOUT# (output)	P17	Y	Y
			PB3	Y	Y
			PU6	Y	N

Table 18.1 List of Multiplexed Pin Configurations (17 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Ethernet controller	Ether1	CLKOUT25M1 (output)	P54	Y	Y
		ETH1_TXC (input)	P87	Y	Y
		ETH1_TXEN (output)	PF5	Y	Y
		ETH1_TXER (output)	P17	Y	Y
			P56	Y	Y
			PA5	Y	Y
		ETH1_TXD0 (output)	P86	Y	Y
		ETH1_TXD1 (output)	PD7	Y	Y
		ETH1_TXD2 (output)	PD6	Y	Y
		ETH1_TXD3 (output)	PD5	Y	Y
		ETH1_INT (input)	P53	Y	N
			PA4	Y	Y
		ETH1_RXC (input)	PB2	Y	Y
		ETH1_RXDV (input)	PB0	Y	Y
		ETH1_RXER (input)	PB1	Y	Y
		ETH1_RXD0 (input)	PF6	Y	Y
		ETH1_RXD1 (input)	PB7	Y	Y
		ETH1_RXD2 (input)	PC0	Y	Y
			PC2	Y	Y
		ETH1_RXD3 (input)	PC1	Y	Y
		ETH1_CRS (input)	P82	Y	Y
			PB3	Y	Y
		ETH1_COL (input)	PB4	Y	Y
		PHYLINK1 (input)	P51	Y	Y
	Ether2	CLKOUT25M2 (output)	PM0	Y	N
		ETH2_TXC (input)	PL1	Y	N
		ETH2_TXEN (output)	PL2	Y	N
		ETH2_TXER (output)	PK4	Y	N
		ETH2_TXD0 (output)	PL0	Y	N
		ETH2_TXD1 (output)	PK5	Y	N
		ETH2_TXD2 (output)	PK7	Y	N
		ETH2_TXD3 (output)	PK6	Y	N
		ETH2_INT (input)	PD4	Y	N
		ETH2_RXC (input)	PU1	Y	N
		ETH2_RXDV (input)	PL7	Y	N
		ETH2_RXER (input)	PU0	Y	N
		ETH2_RXD0 (input)	PL3	Y	N
		ETH2_RXD1 (input)	PL4	Y	N
		ETH2_RXD2 (input)	PL5	Y	N
		ETH2_RXD3 (input)	PL6	Y	N
		ETH2_CRS (input)	PU2	Y	N
		ETH2_COL (input)	PU3	Y	N
		MII2_MDC (output)	PU4	Y	N
		MII2_MDIO (input/output)	PU5	Y	N
		PHYRESETOUT2# (output)	PD3	Y	N

Table 18.1 List of Multiplexed Pin Configurations (18 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
EtherCAT slave controller (optional)	Ether0	CATLEDRUN (output)	PJ7	Y	N
			PM4	Y	N
		CATIRQ (output)	PJ6	Y	N
			PU7	Y	N
		CATLEDSTER (output)	PJ1	Y	N
			PM5	Y	N
		CATLEDERR (output)	PJ0	Y	N
			PM1	Y	N
		CATLINKACT0 (output)	P83	Y	N
			PM6	Y	N
		CATLINKACT1 (output)	P84	Y	N
			PM7	Y	N
		CATSYNC1 (output)	PB2	Y	N
			PM2	Y	N
		CATSYNC0 (output)	PB4	Y	N
			PM3	Y	N
		CATLATCH1 (input)	PB2	Y	N
			PM2	Y	N
		CATLATCH0 (input)	PB4	Y	N
			PM3	Y	N
		CATI2CCLK (input/output)	PC3	Y	N
			PC4	Y	N
		CATI2CDATA (input/output)	PC2	Y	N
			PC5	Y	N
USB2.0 host/ function module	USB	USB_VBUSIN (input)	P30	Y	Y
			PC6	Y	N
		USB_VBUSEN (output)	P31	Y	N
			P43	Y	Y
			P66	Y	N
			P85	Y	Y
		USB_OVRCUR (input)	P32	Y	N
			P67	Y	N
			P70	Y	Y
			P82	Y	Y
CAN module	CAN0	CRXD0 (input)	P30	Y	Y
			PC6	Y	N
		CTXD0 (output)	P60	Y	Y
			P67	Y	N
	CAN1	CRXD1 (input)	PC3	Y	Y
			PC7	Y	N
		CTXD1 (output)	P61	Y	Y
			P66	Y	N
			PB3	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (19 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Serial peripheral interface	RSPI0	RSPCK0 (input/output)	P77	Y	Y
			PE7	Y	Y
		MOSI0 (input/output)	PA0	Y	Y
			PE5	Y	Y
		MISO0 (input/output)	PA1	Y	Y
			PE6	Y	Y
		SSL00 (input/output)	P75	Y	Y
			PE4	Y	Y
		SSL01 (output)	P76	Y	Y
			PE3	Y	Y
		SSL02 (output)	PA2	Y	Y
			PE2	Y	Y
		SSL03 (output)	P74	Y	Y
			PE1	Y	Y
	RSPI1	RSPCK1 (input/output)	PG2	Y	Y
			PN3	Y	N
		MOSI1 (input/output)	PG4	Y	Y
			PN2	Y	N
		MISO1 (input/output)	PG3	Y	Y
			PN1	Y	N
		SSL10 (input/output)	PG5	Y	Y
			PN0	Y	N
		SSL11 (output)	PG6	Y	Y
			PN4	Y	N
	RSPI2	RSPCK2 (input/output)	P51	Y	Y
			P86	Y	Y
		MOSI2 (input/output)	P54	Y	Y
			PK4	Y	N
		MISO2 (input/output)	P53	Y	N
			PD6	Y	Y
		SSL20 (input/output)	P52	Y	N
			PD5	Y	Y
	RSPI3	RSPCK3 (input/output)	PB5	Y	Y
			PJ1	Y	N
		MOSI3 (input/output)	PJ0	Y	N
			PB4	Y	Y
		MISO3 (input/output)	PB6	Y	Y
			PJ2	Y	N
		SSL30 (input/output)	PB2	Y	Y
			PF7	Y	N

Table 18.1 List of Multiplexed Pin Configurations (20 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Quad serial peripheral interface		SPBCLK (output)	P62	Y	Y
		SPBMO/SPBIO0 (input/output)	P63	Y	Y
		SPBMI/SPBIO1 (input/output)	P64	Y	Y
		SPBIO2 (input/output)	P65	Y	Y
		SPBIO3 (input/output)	P61	Y	Y
		SPBSSL (output)	P60	Y	Y
Serial sound interface	SSI0	SSISCK0 (input/output)	P74	Y	Y
			PS1	Y	N
		SSIWS0 (input/output)	P76	Y	Y
			PS2	Y	N
		SSITXD0 (output)	P72	Y	Y
			PS4	Y	N
		SSIRXD0 (input)	P73	Y	Y
			PS3	Y	N
		AUDIO_CLK (input)	PA1	Y	Y
			PS0	Y	N
ΔΣ interface		MCLK0 (input/output)	PB3	Y	Y
			PP4	Y	N
			PA7	Y	Y
		MDAT0 (input)	PB4	Y	Y
			PP5	Y	N
			PA6	Y	Y
		MCLK1 (input/output)	P87	Y	Y
			PP2	Y	N
			PA5	Y	Y
		MDAT1 (input)	PB2	Y	Y
			PP3	Y	N
			PA4	Y	Y
		MCLK2 (input/output)	PD6	Y	Y
			PP0	Y	N
			PA3	Y	Y
		MDAT2 (input)	PC1	Y	Y
			PP1	Y	N
			PA2	Y	Y
		MCLK3 (input/output)	PD5	Y	Y
			PN6	Y	N
			PA1	Y	Y
		MDAT3 (input)	PC0	Y	Y
			PN7	Y	N
			PA0	Y	Y

Table 18.1 List of Multiplexed Pin Configurations (21 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
12-bit A/D converter	Unit 0	ADTRG0 (input)	P17	Y	Y
			P44	Y	N
			PA4	Y	Y
			PJ3	Y	N
	Unit 1	AN100 (input)*1	P90	Y	N
		AN101 (input)*1	P91	Y	N
		AN102 (input)*1	P92	Y	N
		AN103 (input)*1	P93	Y	N
		AN104 (input)*1	P94	Y	N
		AN105 (input)*1	P95	Y	N
		AN106 (input)*1	P96	Y	N
		AN107 (input)*1	P97	Y	N
		AN108 (input)*1	PD0	Y	N
		AN109 (input)*1	PD1	Y	N
		AN110 (input)*1	PD2	Y	N
		AN111 (input)*1	PD3	Y	N
		AN112 (input)*1	PD4	Y	N
		AN113 (input)*1	PD5	Y	Y
		AN114 (input)*1	PD6	Y	N
		AN115 (input)*1	PD7	Y	N
		AN1_ANEX0 (output)*1	P86	Y	N
		AN1_ANEX1 (input)*1	P87	Y	N
		ADTRG1 (input)	P00	Y	N
			P97	Y	N
			PL2	Y	N
Encoder I/F		ENCIF12 (input/output)	P16	Y	N
			PK1	Y	N
			PN7	Y	N
		ENCIF11 (input/output)	P15	Y	N
			PK0	Y	N
			PN6	Y	N
		ENCIF10 (input/output)	P14	Y	N
			PT7	Y	N
			PN5	Y	N
		ENCIF09 (input/output)	P96	Y	N
			PT3	Y	N
			PN1	Y	N
		ENCIF08 (input/output)	P94	Y	N
			PT1	Y	N
			PR1	Y	N
		ENCIF07 (input/output)	P93	Y	N
			PT0	Y	N
			PR0	Y	N

Table 18.1 List of Multiplexed Pin Configurations (22 / 22)

Module/Function	Channel	Pin Function	Allocation Port	Package	
				320-pin	176-pin
Encoder I/F		ENCIF06 (input/output)	P91	Y	N
			PS6	Y	N
			PP6	Y	N
		ENCIF05 (input/output)	PA2	Y	N
			PR7	Y	N
		ENCIF04 (input/output)	P75	Y	N
			PR6	Y	N
		ENCIF03 (input/output)	P73	Y	N
			PR5	Y	N
		ENCIF02 (input/output)	P72	Y	N
			PR4	Y	N
		ENCIF01 (input/output)	P71	Y	N
			PR3	Y	N
		ENCIF00 (input/output)	P70	Y	N
			PR2	Y	N

Note 1. To use this pin, make the applicable pin unavailable, and configure it as a general input/output port (by setting the PORTm.PDR.Bn bit to 00, and the PORTm.PMR.Bn bit to 0).

18.2 Register Descriptions

The registers and bits of unsupported pins, depending on the package, are reserved. The write value to the reserved bits is the value after a reset.

18.2.1 Write-Protect Register (PWPR)

The PWPR register enables or disables writing to the PFS register and the PFSWE bit of the PWPR register.

Address(es): A000 02FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PFS Register Write Enable	0: Writing to the PFS register is disabled. 1: Writing to the PFS register is enabled.	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled. 1: Writing to the PFSWE bit is disabled.	R/W

PFSWE Bit (PFS Register Write Enable)

Writing to the PmnPFS register (m = 0 to 9, A to H, J to N, P, R to U, and n = 0 to 7) is enabled only when the PFSWE bit is set to 1.

To set the PFSWE bit to 1, write 0 to the B0WI bit, and then set 1 to the PFSWE bit.

B0WI Bit (PFSWE Bit Write Disable)

Only when the B0WI bit is set to 0, writing to the PFSWE bit is enabled.

18.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 7)

The P0n pin function control register (P0nPFS) selects the function of the pin to use.
The P0nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection.

Address(es): P00PFS A000 0200h, P01PFS A000 0201h, P02PFS A000 0202h, P03PFS A000 0203h, P04PFS A000 0204h, P05PFS A000 0205h, P06PFS A000 0206h, P07PFS A000 0207h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.2.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

Table 18.2 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	P00	P01	P02	P03	P04	P05	P06	P07
000000b (Value after reset)	Hi-Z							
000001b	MTIOC6A	MTIC5W	MTIC5V	MTIC5U	MTIOC3C	MTIOC3A	MTIOC2B	MTIOC2A
000011b	TIOCA1	TIOCA2	TIOCA3	TIOCA4	TIOCA5	—	TIOCB0	TIOCB1
001001b	ADTRG1	—	—	—	—	—	—	—
100010b	D0	D1	D2	D3	D4	D5	D6	D7
100111b	TRACECTL	—	—	—	—	—	—	—

Note: —: Do not set.

18.2.3 P1n Pin Function Control Register (P1nPFS) (n = 0 to 7)

The P1n pin function control register (P1nPFS) selects the function of the pin to use.
The P1nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P10PFS A000 0208h, P11PFS A000 0209h, P12PFS A000 020Ah, P13PFS A000 020Bh, P14PFS A000 020Ch, P15PFS A000 020Dh, P16PFS A000 020Eh, P17PFS A000 020Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.3, and Table 18.4.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ input pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.3 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	P10	P11	P12	P13	P14	P15	P16	P17
000000b (Value after reset)	Hi-Z							
000001b	—	MTIOC4D	MTIOC4B	MTIOC4C	MTIOC4A	MTIOC3D	MTIOC3B	—
000011b	TIOCA0	—	—	—	—	—	—	—
001001b	—	—	—	—	—	—	—	ADTRG0
010010b	—	—	—	—	—	—	—	ETH1_TXER
010110b	—	—	—	—	—	—	—	PHYRESETOUT#
011110b	—	GTIOC2B	GTIOC2A	GTIOC1B	GTIOC1A	GTIOC0B	GTIOC0A	—
100010b	CKIO	—	—	RAS#	CAS#	CS3#	CS4#	CS5#
100011b	—	—	—	—	—	CKE	CS2#	—
100111b	TRACECLK	—	—	—	—	—	—	—
101011b	—	—	—	—	ENCIF10	ENCIF11	ENCIF12	—

Note: —: Do not set.

Table 18.4 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin					
	P10	P13	P14	P15	P16	P17
000000b (Value after reset)	Hi-Z					
000001b	—	MTIOC4C	MTIOC4A	MTIOC3D	MTIOC3B	—
000011b	TIOCA0	—	—	—	—	—
001001b	—	—	—	—	—	ADTRG0
010010b	—	—	—	—	—	ETH1_TXER
010110b	—	—	—	—	—	PHYRESETOUT#
011110b	—	GTIOC1B	GTIOC1A	GTIOC0B	GTIOC0A	—
100010b	CKIO	RAS#	CAS#	CS3#	CS4#	CS5#
100011b	—	—	—	CKE	CS2#	—
100111b	TRACECLK	—	—	—	—	—

Note: —: Do not set.

18.2.4 P2n Pin Function Control Register (P2nPFS) (n = 0 to 7)

The P2n pin function control register (P2nPFS) selects the function of the pin to use. The P2nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P20PFS A000 0210h, P21PFS A000 0211h, P22PFS A000 0212h, P23PFS A000 0213h, P24PFS A000 0214h, P25PFS A000 0215h, P26PFS A000 0216h, P27PFS A000 0217h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.5.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.5 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	P20	P21	P22	P23	P24	P25	P26	P27
000000b (Value after reset)	Hi-Z							
000001b	MTCLKD	MTIC5V	—	MTIC5U	—	MTCLKC	MTIOC8D	MTIOC8C
000010b	—	—	MTIOC7B	—	—	—	—	—
000011b	—	TIOCB1	TIOCD0	—	—	—	—	TIOCB0
001010b	—	—	—	—	—	—	—	RTS0#
001011b	—	CTS0#	SCK0	TXD0	RXD0	—	—	—
011000b	—	—	—	DACK1	—	TEND1	DREQ1	—
100010b	A17	CS0#	RD#	A0	RD/WR#	A18	A19	A20

Note: —: Do not set.

18.2.5 P3n Pin Function Control Register (P3nPFS) (n = 0 to 7)

The P3n pin function control register (P3nPFS) selects the function of the pin to use. The P3nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written. No peripheral functions are assigned to P35. To use P35 as the NMI pin, see section 12.3.4, NMI Pin Interrupts.

Address(es): P30PFS A000 0218h, P31PFS A000 0219h, P32PFS A000 021Ah, P33PFS A000 021Bh, P34PFS A000 021Ch, P35PFS A000 021Dh, P36PFS A000 021Eh, P37PFS A000 021Fh

	b7	b6	b5	b4	b3	b2	b1	b0	
	—	ISEL	PSEL[5:0]						
Value after reset:	0	0	0	0	0	0	0	0	*1
	0	0	1	0	0	1	1	1	*2

Note 1. Other than P33PFS and P34PFS
Note 2. P33PFS, P34PFS

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.6 and Table 18.7.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin or NMI input pin. 1: Use as the IRQn input pin or NMI input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ input pin or the NMI input pin (P35). This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins. To use the pin as the NMI pin, see section 12.3.4, NMI Pin Interrupts.

Table 18.6 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin						
	P30	P31	P32	P33	P34	P36	P37
000000b (Value after reset) *1	Hi-Z						
000110b	—	—	—	—	—	PO0	PO1
010000b	CRXD0	—	—	—	—	—	—
011001b	USB_VBUSIN	USB_VBUSEN	USB_OVRCUR	—	—	—	—
100010b	—	—	—	—	—	WE0#/DQMLL	WE1#/DQMLU
100111b (Value after reset) *2	—	—	—	TDO	TDI	—	—

Note 1. For pins other than P33 and P34.
Note 2. For pins P33 and P34 only.
Note: —: Do not set.

Table 18.7 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin				
	P30	P33	P34	P36	P37
000000b	Hi-Z				
000110b	—	—	—	PO0	PO1
010000b	CRXD0	—	—	—	—
011001b	USB_VBUSIN	—	—	—	—
100010b	—	—	—	WE0#/DQMLL	WE1#/DQMLU
100111b (Value after reset)	—	TDO	TDI	—	—

Note: —: Do not set.

18.2.6 P4n Pin Function Control Register (P4nPFS) (n = 0 to 7)

The P4n pin function control register (P4nPFS) selects the function of the pin to use. The P4nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P40PFS A000 0220h, P41PFS A000 0221h, P42PFS A000 0222h, P43PFS A000 0223h, P44PFS A000 0224h, P45PFS A000 0225h, P46PFS A000 0226h, P47PFS A000 0227h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.8 and Table 18.9.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.8 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	P40	P41	P42	P43	P44	P45	P46	P47
000000b (Value after reset)	Hi-Z							
000001b	MTIOC8A	—	—	MTIOC8B	—	—	—	MTIOC6C
000010b	—	—	MTIOC7C	—	—	—	—	—
000011b	—	—	—	—	TCLKD	—	—	—
001001b	—	—	—	—	ADTRG0	—	—	—
001010b	TXD0	SCK0	RXD0	—	CTS0#	—	—	—
011001b	—	—	—	USB_VBUSEN	—	—	—	—
100010b	—	—	—	WE2#/DQMUL	—	CS2#	CKE	WE3#/DQMUU/AH#
100011b	—	BS#	—	—	WAIT#	—	—	—

Note: —: Do not set.

Table 18.9 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin			
	P40	P42	P43	P47
000000b (Value after reset)	Hi-Z			
000001b	MTIOC8A	—	MTIOC8B	MTIOC6C
000010b	—	MTIOC7C	—	—
001010b	TXD0	RXD0	—	—
011001b	—	—	USB_VBUSEN	—
100010b	—	—	WE2#/DQMUL	WE3#/DQMUU/AH#

Note: —: Do not set.

18.2.7 P5n Pin Function Control Register (P5nPFS) (n = 0 to 6)

The P5n pin function control register (P5nPFS) selects the function of the pin to use. The P5nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P50PFS A000 0228h, P51PFS A000 0229h, P52PFS A000 022Ah, P53PFS A000 022Bh, P54PFS A000 022Ch, P55PFS A000 022Dh, P56PFS A000 022Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.10 and Table 18.11.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.10 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin						
	P50	P51	P52	P53	P54	P55	P56
000000b (Value after reset)	Hi-Z						
001101b	—	RSPCK2	—	—	MOSI2	—	—
001110b	—	—	SSL20	MISO2	—	—	—
010001b	PHYLINK0	PHYLINK1	ETH0_INT	ETH1_INT	CLKOUT25M1	ETHSWSECOUT	ETH1_TXER
100010b	—	—	—	—	—	—	BS#
100011b	CS1#	—	—	—	—	A24	—

Note: —: Do not set.

Table 18.11 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin		
	P51	P54	P56
000000b (Value after reset)	Hi-Z		
001101b	RSPCK2	MOSI2	—
010001b	PHYLINK1	CLKOUT25M1	ETH1_TXER
100010b	—	—	BS#

Note: —: Do not set.

18.2.8 P6n Pin Function Control Register (P6nPFS) (n = 0 to 7)

The P6n pin function control register (P6nPFS) selects the function of the pin to use. The P6nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P60PFS A000 0230h, P61PFS A000 0231h, P62PFS A000 0232h, P63PFS A000 0233h, P64PFS A000 0234h, P65PFS A000 0235h, P66PFS A000 0236h, P67PFS A000 0237h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.12 and Table 18.13.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.12 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	P60	P61	P62	P63	P64	P65	P66	P67
000000b (Value after reset)	Hi-Z							
010000b	CTXD0	CTXD1	—	—	—	—	CTXD1	CTXD0
011000b	TEND0	DACK0	—	—	—	DREQ0	DACK0	TEND0
011001b	—	—	—	—	—	—	USB_VBUSEN	USB_OVRCUR
011011b	SPBSSL	SPBIO3	SPBCLK	SPBMO/ SPBIO0	SPBMI/ SPBIO1	SPBIO2	—	—
011110b	—	—	—	—	—	—	GTIOC3A	GTIOC3B

Note: —: Do not set.

Table 18.13 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin					
	P60	P61	P62	P63	P64	P65
000000b (Value after reset)	Hi-Z					
010000b	CTXD0	CTXD1	—	—	—	—
011000b	TEND0	DACK0	—	—	—	DREQ0
011011b	SPBSSL	SPBIO3	SPBCLK	SPBMO/ SPBIO0	SPBMI/SPBIO1	SPBIO2

Note: —: Do not set.

18.2.9 P7n Pin Function Control Register (P7nPFS) (n = 0 to 7)

The P7n pin function control register (P7nPFS) selects the function of the pin to use. The P7nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): P70PFS A000 0238h, P71PFS A000 0239h, P72PFS A000 023Ah,P73PFS A000 023Bh, P74PFS A000 023Ch, P75PFS A000 023Dh, P76PFS A000 023Eh, P77PFS A000 023Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.14.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.14 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	P70	P71	P72	P73	P74	P75	P76	P77
000000b (Value after reset)	Hi-Z							
000001b	—	—	MTIOC1A	MTCLKB	MTCLKA	MTIOC4D	MTIOC4B	MTIOC4C
000010b	MTIOC6D	—	—	—	—	—	—	—
000111b	—	POE0#	—	—	—	—	—	—
001000b	—	POE10#	—	—	—	—	—	—
001010b	RTS1#	SCK1	TXD1	RXD1	CTS1#	—	—	—
001101b	—	—	—	—	SSL03	SSL00	SSL01	RSPCK0
010111b	—	—	SSITXD0	SSIRXD0	SSISCK0	—	SSIWS0	—
011001b	USB_OVRCUR	—	—	—	—	—	—	—
011101b	—	TOC2	TIC2	—	—	—	—	—
011110b	—	—	—	—	—	GTIOC2B	GTIOC2A	GTIOC1B
100010b	D16	D17	D18	D19	D20	D21	D22	D23
100111b	TRACECLK	TRACECTL	TRACEDATA0	TRACEDATA1	TRACEDATA2	TRACEDATA3	TRACEDATA4	TRACEDATA5
101011b	ENCIF00	ENCIF01	ENCIF02	ENCIF03	—	ENCIF04	—	—

Note: —: Do not set.

18.2.10 P8n Pin Function Control Register (P8nPFS) (n = 0 to 7)

The P8n pin function control register (P8nPFS) selects the function of the pin to use. The P8nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of a pin without the IRQn function, and the ASEL bit of a pin without the analog input function are reserved. A value after a reset must be written.

Address(es): P80PFS A000 0240h, P81PFS A000 0241h, P82PFS A000 0242h, P83PFS A000 0243h, P84PFS A000 0244h, P85PFS A000 0245h, P86PFS A000 0246h, P87PFS A000 0247h

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.15 and Table 18.16.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	ASEL	Analog Input Function Select	0: Do not use as an analog input. 1: Use as an analog input.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins. If the setting of the ASEL bit is 1, the given pin does not function as an IRQn input pin even if this bit is set to 1.

ASEL Bit (Analog Input Function Select)

Set this bit to 1 to use the given pin as an analog pin. To set the ASEL bit as an analog pin, select the general input/output port by the port mode register (PORTm.PMR), and disable it by the port direction register (PORTm.PDR). At that time, the pin status cannot be read.

Table 18.15 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	P80	P81	P82	P83	P84	P85	P86	P87
000000b (Value after reset)	Hi-Z							
000001b	—	—	—	—	—	—	MTIOC4B	MTIOC4C
000011b	TIOCC3	TIOCC0	TIOCD3	—	—	—	—	—
001010b	RTS4#	CTS4#	SCK4	—	—	TXD4	—	—
001011b	—	—	RTS3#	TXD4	RXD4	SCK4	—	—
001110b	—	—	—	—	—	—	RSPCK2	—
010001b	ETH0_RXDV	ETH0_RXER	ETH0_TXEN	ETH0_CRS	ETH0_COL	CLKOUT25M0	ETH1_TXD0	ETH1_TXC
010010b	—	—	ETH1_CRS	—	—	—	—	ETH0_RXD0
010101b	—	—	—	CATLINKACT0 *1	CATLINKACT1 *1	—	—	—
011001b	—	—	USB_OVRCUR	—	—	USB_VBUSEN	—	—
011101b	—	—	—	—	—	—	TOC1	—
011110b	—	—	—	—	—	—	GTIOC2A	GTIOC1B
100010b	—	—	—	—	—	—	—	A23
101000b	—	—	—	—	—	—	—	MCLK1

Note: —: Do not set.
Note 1. Only for products incorporating an EtherCAT (optional)

Table 18.16 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin			
	P82	P85	P86	P87
000000b (Value after reset)	Hi-Z			
000001b	—	—	MTIOC4B	MTIOC4C
000011b	TIOCD3	—	—	—
001010b	SCK4	TXD4	—	—
001011b	RTS3#	SCK4	—	—
001110b	—	—	RSPCK2	—
010001b	ETH0_TXEN	CLKOUT25M0	ETH1_TXD0	ETH1_TXC
010010b	ETH1_CRS	—	—	ETH0_RXD0
011001b	USB_OVRCUR	USB_VBUSEN	—	—
011101b	—	—	TOC1	—
011110b	—	—	GTIOC2A	GTIOC1B
100010b	—	—	—	A23
101000b	—	—	—	MCLK1

Note: —: Do not set.

18.2.11 P9n Pin Function Control Register (P9nPFS) (n = 0 to 7)

The P9n pin function control register (P9nPFS) selects the function of the pin to use. The P9nPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of a pin without the IRQn function, and the ASEL bit of a pin without the analog input function are reserved. A value after a reset must be written.

Address(es): P90PFS A000 0248h, P91PFS A000 0249h, P92PFS A000 024Ah, P93PFS A000 024Bh, P94PFS A000 024Ch, P95PFS A000 024Dh, P96PFS A000 024Eh, P97PFS A000 024Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.17.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	ASEL	Analog Input Function Select	0: Do not use as an analog input. 1: Use as an analog input.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as an IRQ input pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.
If the setting of the ASEL bit is 1, the given pin does not function as an IRQn input pin even if this bit is set to 1.

ASEL Bit (Analog Input Function Select)

Set this bit to 1 to use the given pin as an analog pin. To set the ASEL bit as an analog pin, select the general input/output port by the port mode register (PORTm.PMR), and then disable it by the port direction register (PORTm.PDR). At that time, the pin status cannot be read.

Table 18.17 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	P90	P91	P92	P93	P94	P95	P96	P97
000000b (Value after reset)	Hi-Z							
000001b	—	—	—	MTIOC1A	MTCLKB	MTCLKA	—	—
000011b	TIOCA5	—	—	—	—	—	—	—
000111b	—	—	—	—	—	—	POE0#	—
001000b	—	—	—	—	—	—	POE10#	—
001001b	—	—	—	—	—	—	—	ADTRG1
001011b	—	TXD2	RXD2	SCK2	RTS2#	CTS2#	—	—
001100b	TXD4	—	—	—	—	—	—	—
011101b	—	—	TOC3	TIC3	—	—	—	—
100011b	RAS#	CAS#	CS5#	—	—	—	—	A25
101011b	—	ENCIF06	—	ENCIF07	ENCIF08	—	ENCIF09	—

Note: —: Do not set.

18.2.12 PAn Pin Function Control Register (PAnPFS) (n = 0 to 7)

The PAn pin function control register (PAnPFS) selects the function of the pin to use. The PAnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PA0PFS A000 0250h, PA1PFS A000 0251h, PA2PFS A000 0252h, PA3PFS A000 0253h, PA4PFS A000 0254h, PA5PFS A000 0255h, PA6PFS A000 0256h, PA7PFS A000 0257h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.18.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.18 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	PA0	PA1	PA2	PA3	PA4	PA5	PA6	PA7
000000b (Value after reset)	Hi-Z							
000001b	MTIOC4A	MTIOC3D	MTIOC3B	—	—	—	—	—
000010b	—	—	—	—	—	—	—	MTIOC6B
000011b	—	—	—	TIOCA2	TIOCA3	TIOCA4	—	—
001001b	—	—	—	—	ADTRG0	—	—	—
001010b	—	—	—	SCK2	RXD2	TXD2	CTS2#	RTS2#
001101b	MOSI0	MISO0	SSL02	—	—	—	—	—
010001b	—	—	—	—	—	ETH0_INT	—	—
010010b	—	—	—	ETHSWSECOUT	ETH1_INT	ETH1_TXER	—	—
010111b	—	AUDIO_CLK	—	—	—	—	—	—
011000b	—	—	DREQ2	DACK2	TEND2	—	—	—
011110b	GTIOC1A	GTIOC0B	GTIOC0A	GTETRG	—	—	GTIOC3A	GTIOC3B
100010b	D24	D25	D26	D27	D28	D29	D30	D31
100011b	—	—	—	—	—	—	A21	A22
101000b	MDAT3	MCLK3	MDAT2	MCLK2	MDAT1	MCLK1	MDAT0	MCLK0
100111b	TRACEDATA6	TRACEDATA7	—	—	—	—	—	—
101011b	—	—	ENCIF05	—	—	—	—	—

Note: —: Do not set.

18.2.13 PBn Pin Function Control Register (PBnPFS) (n = 0 to 7)

The PBn pin function control register (PBnPFS) selects the function of the pin to use. The PBnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PB0PFS A000 0258h, PB1PFS A000 0259h, PB2PFS A000 025Ah, PB3PFS A000 025Bh, PB4PFS A000 025Ch, PB5PFS A000 025Dh, PB6PFS A000 025Eh, PB7PFS A000 025Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.19.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.19 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	PB0	PB1	PB2	PB3	PB4	PB5	PB6	PB7
000000b (Value after reset)	Hi-Z							
000001b	MTCLKB	MTCLKA	MTIOC1A	—	—	—	—	MTIOC3B
000011b	TCLKD	TCLKC	—	—	—	TCLKB	TCLKA	—
000111b	—	—	—	—	—	POE0#	—	—
001000b	—	—	—	—	—	POE10#	—	—
001010b	—	—	—	TXD3	RXD3	CTS3#	SCK3	—
001011b	—	CTS4#	—	—	—	—	RTS4#	—
001110b	—	—	SSL30	—	MOSI3	RSPCK3	MISO3	—
010000b	—	—	—	CTXD1	—	—	—	—
010001b	ETH1_RXDV	ETH1_RXER	ETH1_RXC	ETH1_CRS	ETH1_COL	ETH_MDIO	ETH_MDC	ETH1_RXD1
010010b	—	—	ETH0_RXD1	—	ETH0_RXER	—	—	—
010101b	—	—	CATSYNC1*1, *2	PHYRESETOUT#	CATSYNC0*1, *2	—	—	—
010110b	—	—	CATLATCH1*1, *2	—	CATLATCH0*1, *2	—	—	—
011101b	TIC3	—	—	—	—	—	—	TOC3
011110b	—	—	—	—	—	—	—	GTIOC0A
100010b	—	—	—	CS1#	A24	—	—	—
101000b	—	—	MDAT1	MCLK0	MDAT0	—	—	—

Note: —: Do not set.
Note 1. Not supported for the 176-pin products
Note 2. Only for products incorporating an EtherCAT (optional)

18.2.14 PCn Pin Function Control Register (PCnPFS) (n = 0 to 7)

The PCn pin function control register (PCnPFS) selects the function of the pin to use. The PCnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PC0PFS A000 0260h, PC1PFS A000 0261h, PC2PFS A000 0262h, PC3PFS A000 0263h, PC4PFS A000 0264h, PC5PFS A000 0265h, PC6PFS A000 0266h, PC7PFS A000 0267h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.20 and Table 18.21.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.20 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PC0	PC1	PC2	PC3	PC4	PC5	PC6	PC7
000000b (Value after reset)	Hi-Z							
000011b	—	—	—	—	TCLKH	TCLKG	TCLKC	—
001010b	—	—	—	RXD4	—	—	—	—
001111b	SCL1	SDA1	SDA0	SCL0	SCL0	SDA0	SCL1	SDA1
010000b	—	—	—	CRXD1	—	—	CRXD0	CRXD1
010001b	ETH1_RXD2	ETH1_RXD3	ETH0_TXC	ETH0_RXC	—	—	—	—
010010b	—	PHYLINK0	ETH1_RXD2	ETH0_RXDV	—	—	—	—
010101b	—	—	CATI2CDATA *1	CATI2CCLK *1	—	—	—	—
010110b	—	—	—	—	CATI2CCLK *1	CATI2CDATA *1	—	—
011000b	—	—	—	—	—	—	DREQ0	—
011001b	—	—	—	—	—	—	USB_VBUSIN	—
011101b	—	—	—	—	—	—	—	TIC0
011110b	GTETRG	—	—	—	—	—	—	—
100010b	WAIT#	—	—	—	—	—	—	—
101000b	MDAT3	MDAT2	—	—	—	—	—	—

Note: —: Do not set.
Note 1. Only for products incorporating an EtherCAT (optional)

Table 18.21 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

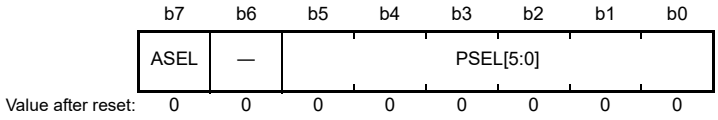
PSEL[5:0] Setting	Pin			
	PC0	PC1	PC2	PC3
000000b (Value after reset)	Hi-Z			
001010b	—	—	—	RXD4
001111b	SCL1	SDA1	SDA0	SCL0
010000b	—	—	—	CRXD1
010001b	ETH1_RXD2	ETH1_RXD3	ETH0_TXC	ETH0_RXC
010010b	—	PHYLINK0	ETH1_RXD2	ETH0_RXDV
011110b	GTETRG	—	—	—
100010b	WAIT#	—	—	—
101000b	MDAT3	MDAT2	—	—

Note: —: Do not set.

18.2.15 PDn Pin Function Control Register (PDnPFS) (n = 0 to 7)

The PDn pin function control register (PDnPFS) selects the function of the pin to use. The PDnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ASEL bit of a pin without analog input function is reserved. A value after a reset must be written.

Address(es): PD0PFS A000 0268h, PD1PFS A000 0269h, PD2PFS A000 026Ah, PD3PFS A000 026Bh, PD4PFS A000 026Ch, PD5PFS A000 026Dh, PD6PFS A000 026Eh, PD7PFS A000 026Fh



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.22 and Table 18.23.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	ASEL	Analog Input Function Select	0: Do not use as an analog input. 1: Use as an analog input.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ASEL Bit (Analog Input Function Select)

Set this bit to 1 to use the given pin as an analog pin. To set the ASEL bit as an analog pin, select the general input/output port by the port mode register (PORTm.PMR), and then disable it by the port direction register (PORTm.PDR). At that time, the pin status cannot be read.

Table 18.22 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
000000b (Value after reset)	Hi-Z							
000010b	—	—	—	—	—	—	—	MTIOC4D
001101b	—	—	—	—	—	SSL20	MISO2	—
010001b	—	—	—	—	—	ETH1_TXD3	ETH1_TXD2	ETH1_TXD1
010010b	—	—	—	—	—	ETH0_TXD0	ETH0_TXD1	—
010100b	—	—	—	PHYRESETOUT2#	ETH2_INT	—	—	—
011101b	—	—	—	—	—	TIC0	TIC1	TOC0
011110b	—	—	—	—	—	—	—	GTIOC2B
100010b	—	—	—	—	—	A21	A22	—
100011b	CS4#	CS1#	WAIT#	—	—	—	—	—
101000b	—	—	—	—	—	MCLK3	MCLK2	—

Note: —: Do not set.

Table 18.23 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin		
	PD5	PD6	PD7
000000b (Value after reset)	Hi-Z		
000010b	—	—	MTIOC4D
001101b	SSL20	MISO2	—
010001b	ETH1_TXD3	ETH1_TXD2	ETH1_TXD1
010010b	ETH0_TXD0	ETH0_TXD1	—
011101b	TIC0	TIC1	TOC0
011110b	—	—	GTIOC2B
100010b	A21	A22	—
101000b	MCLK3	MCLK2	—

Note: —: Do not set.

18.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 7)

The PEn pin function control register (PEnPFS) selects the function of the pin to use. The PEnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PE0PFS A000 0270h, PE1PFS A000 0271h, PE2PFS A000 0272h, PE3PFS A000 0273h, PE4PFS A000 0274h, PE5PFS A000 0275h, PE6PFS A000 0276h, PE7PFS A000 0277h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.24.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as an IRQ input pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.24 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	PE0	PE1	PE2	PE3	PE4	PE5	PE6	PE7
000000b (Value after reset)	Hi-Z							
000001b	MTIOC1B	MTCLKD	MTCLKC	MTIOC0D	MTIOC0B	MTIOC0C	MTIOC0A	—
000010b	—	—	—	—	—	—	—	MTIOC7A
000011b	TIOCB2	TIOCB3	TIOCB4	TIOCB5	TIOCC0	TIOCC3	TIOCD0	TIOCD3
000111b	—	—	—	—	—	—	—	POE8#
001100b	—	—	—	CTS1#	RTS1#	TXD1	RXD1	SCK1
001110b	—	SSL03	SSL02	SSL01	SSL00	MOSI0	MISO0	RSPCK0
100010b	D8	D9	D10	D11	D12	D13	D14	D15
100111b	TRACEDATA0	TRACEDATA1	TRACEDATA2	TRACEDATA3	TRACEDATA4	TRACEDATA5	TRACEDATA6	TRACEDATA7

Note: —: Do not set.

18.2.17 PFn Pin Function Control Register (PFnPFS) (n = 5 to 7)

The PFn pin function control register (PFnPFS) selects the function of the pin to use. The PFnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PF5PFS: A000 027Dh, PF6PFS: A000 027Eh, PF7PFS: A000 027Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each pin function, see Table 18.25 and Table 18.26.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.25 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin		
	PF5	PF6	PF7
000000b (Value after reset)	Hi-Z		
000001b	MTIOC4A	MTIOC3D	—
001010b	—	—	RTS3#
001101b	—	—	SSL30
010001b	ETH1_TXEN	ETH1_RXD0	ETH0_TXER
011101b	TIC2	TOC2	—
011110b	GTIOC1A	GTIOC0B	—
100010b	—	—	A25

Note: —: Do not set.

Table 18.26 Register Settings for the Input/Output Function in the 176-pin HLFQFP Pin

PSEL[5:0] Setting	Pin	
	PF5	PF6
000000b (Value after reset)	Hi-Z	
000001b	MTIOC4A	MTIOC3D
010001b	ETH1_TXEN	ETH1_RXD0
011101b	TIC2	TOC2
011110b	GTIOC1A	GTIOC0B

18.2.18 PGn Pin Function Control Register (PGnPFS) (n = 0 to 7)

The PGn pin function control register (PGnPFS) selects the function of the pin to use. The PGnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection.

Address(es): PG0PFS A000 0280h, PG1PFS A000 0281h, PG2PFS A000 0282h, PG3PFS A000 0283h, PG4PFS A000 0284h, PG5PFS A000 0285h, PG6PFS A000 0286h, PG7PFS A000 0287h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.27.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

Table 18.27 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	PG0	PG1	PG2	PG3	PG4	PG5	PG6	PG7
000000b (Value after reset)	Hi-Z							
000011b	—	—	—	—	—	TCLKA	TCLKB	—
000110b	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9
001101b	—	—	RSPCK1	MISO1	MOSI1	SSL10	SSL11	—
011101b	—	—	TOC0	TIC1	TOC1	—	—	—
100010b	A1	A2	A3	A4	A5	A6	A7	A8

Note: —: Do not set.

18.2.19 PHn Pin Function Control Register (PHnPFS) (n = 0 to 7)

The PHn pin function control register (PHnPFS) selects the function of the pin to use. The PHnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PH0PFS A000 0288h, PH1PFS A000 0289h, PH2PFS A000 028Ah, PH3PFS A000 028Bh, PH4PFS A000 028Ch, PH5PFS A000 028Dh, PH6PFS A000 028Eh, PH7PFS A000 028Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.28.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.28 Register Settings for the Input/Output Function in the 320-pin FBGA and 176-pin HLFQFP Pins

PSEL[5:0] Setting	Pin							
	PH0	PH1	PH2	PH3	PH4	PH5	PH6	PH7
000000b (Value after reset)	Hi-Z							
000001b	—	MTIOC2B	MTIOC2A	MTIOC1B	—	—	—	MTIC5W
000010b	—	—	—	—	—	—	MTIOC7D	—
000110b	PO10	PO11	PO12	PO13	PO14	PO15	—	—
001011b	—	—	—	—	—	—	RTS0#	—
100010b	A9	A10	A11	A12	A13	A14	A15	A16

Note: —: Do not set.

18.2.20 PJn Pin Function Control Register (PJnPFS) (n = 0 to 7)

The PJn pin function control register (PJnPFS) selects the function of the pin to use. The PJnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PJ0PFS A000 0290h, PJ1PFS A000 0291h, PJ2PFS A000 0292h, PJ3PFS A000 0293h, PJ4PFS A000 0294h, PJ5PFS A000 0295h, PJ6PFS A000 0296h, PJ7PFS A000 0297h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.29.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.29 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

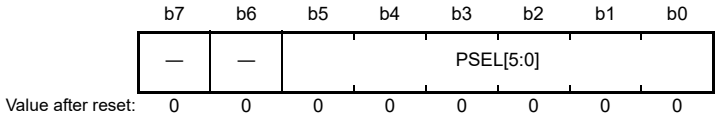
PSEL[5:0] Setting	Pin							
	PJ0	PJ1	PJ2	PJ3	PJ4	PJ5	PJ6	PJ7
000000b (Value after reset)	Hi-Z							
000011b	—	—	—	—	—	TIOCD0	—	—
001001b	—	—	—	ADTRG0	—	—	—	—
001011b	—	—	—	—	TXD3	RXD3	SCK3	CTS3#
001101b	MOSI3	RSPCK3	MISO3	—	—	—	—	—
010001b	ETH0_TXD3	ETH0_TXD2	ETH0_TXD1	ETH0_TXD0	ETH0_RXD0	ETH0_RXD1	ETH0_RXD2	ETH0_RXD3
010101b	CATLEDERR *1	CATLEDSTER *1	—	—	—	—	CATIRQ*1	CATLEDRUN *1

Note: —: Do not set.
Note 1. Only for products incorporating an EtherCAT (optional)

18.2.21 PKn Pin Function Control Register (PKnPFS) (n = 0 to 7)

The PKn pin function control register (PKnPFS) selects the function of the pin to use. The PKnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection.

Address(es): PK0PFS A000 0298h, PK1PFS A000 0299h, PK2PFS A000 029Ah, PK3PFS A000 029Bh, PK4PFS A000 029Ch, PK5PFS A000 029Dh, PK6PFS A000 029Eh, PK7PFS A000 029Fh



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.30.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

Table 18.30 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PK0	PK1	PK2	PK3	PK4	PK5	PK6	PK7
000000b (Value after reset)	Hi-Z							
000011b	—	—	—	—	TIOCB11	TIOCB8	TIOCB6	TIOCB7
000110b	PO31	—	—	—	—	—	—	—
001110b	—	—	—	—	MOSI2	—	—	—
010100b	—	—	—	—	ETH2_TXER	ETH2_TXD1	ETH2_TXD3	ETH2_TXD2
100011b	CAS#	CS5#	A23	A24	—	—	—	—
101011b	ENCIF11	ENCIF12	—	—	—	—	—	—

Note: —: Do not set.

18.2.22 PLn Pin Function Control Register (PLnPFS) (n = 0 to 7)

The PLn pin function control register (PLnPFS) selects the function of the pin to use. The PLnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PL0PFS A000 02A0h, PL1PFS A000 02A1h, PL2PFS A000 02A2h, PL3PFS A000 02A3h, PL4PFS A000 02A4h, PL5PFS A000 02A5h, PL6PFS A000 02A6h, PL7PFS A000 02A7h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.31.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.31 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PL0	PL1	PL2	PL3	PL4	PL5	PL6	PL7
000000b (Value after reset)	Hi-Z							
000011b	TIOCB9	TIOCB10	TIOCA6	TIOCA7	—	TIOCA8	TIOCA9	—
001001b	—	—	ADTRG1	—	—	—	—	—
010100b	ETH2_TXD0	ETH2_TXC	ETH2_TXEN	ETH2_RXD0	ETH2_RXD1	ETH2_RXD2	ETH2_RXD3	ETH2_RXDV

Note: —: Do not set.

18.2.23 PMn Pin Function Control Register (PMnPFS) (n = 0 to 7)

The PMn pin function control register (PMnPFS) selects the function of the pin to use. The PMnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PM0PFS A000 02A8h, PM1PFS A000 02A9h, PM2PFS A000 02AAh, PM3PFS A000 02ABh, PM4PFS A000 02ACh, PM5PFS A000 02ADh, PM6PFS A000 02AEh, PM7PFS A000 02AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.32.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.32 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

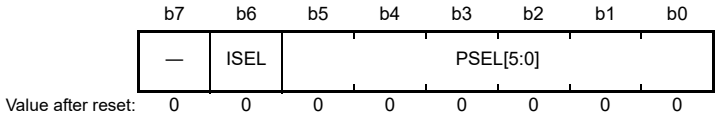
PSEL[5:0] Setting	Pin							
	PM0	PM1	PM2	PM3	PM4	PM5	PM6	PM7
000000b (Value after reset)	Hi-Z							
000011b	—	—	TCLKE	—	—	—	—	—
000110b	—	—	—	PO16	PO17	PO18	PO19	PO20
001100b	TXD4	SCK4	RTS4#	—	—	—	—	—
010100b	CLKOUT25M2	—	—	—	—	—	—	—
010101b	—	—	CATSYNC1*1	CATSYNC0*1	—	—	—	—
010110b	—	CATLEDERR *1	CATLATCH1 *1	CATLATCH0 *1	CATLEDRUN *1	CATLEDSTER *1	CATLINKACT0 *1	CATLINKACT1 *1

Note: —: Do not set.
Note 1. Only for products incorporating an EtherCAT (optional)

18.2.24 PNn Pin Function Control Register (PNnPFS) (n = 0 to 7)

The PNn pin function control register (PNnPFS) selects the function of the pin to use. The PNnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PN0PFS A000 02B0h, PN1PFS A000 02B1h, PN2PFS A000 02B2h, PN3PFS A000 02B3h, PN4PFS A000 02B4h, PN5PFS A000 02B5h, PN6PFS A000 02B6h, PN7PFS A000 02B7h



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.33.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.33 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

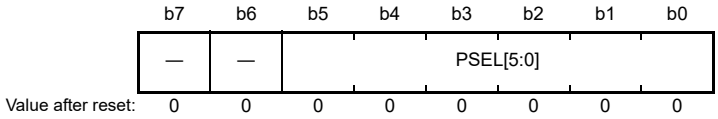
PSEL[5:0] Setting	Pin							
	PN0	PN1	PN2	PN3	PN4	PN5	PN6	PN7
000000b (Value after reset)	Hi-Z							
000001b	MTIOC8D	MTIOC8C	MTIOC8B	MTIOC8A	MTIOC6C	MTIOC6A	MTIOC3C	MTIOC3A
000011b	—	—	—	—	TIOCC6	TIOCD9	TIOCC9	TIOCD6
000110b	—	PO21	—	—	—	—	—	—
001110b	SSL10	MISO1	MOSI1	RSPCK1	SSL11	—	—	—
011000b	—	—	—	—	—	—	—	DREQ0
101000b	—	—	—	—	—	—	MCLK3	MDAT3
101011b	—	ENCIF09	—	—	—	ENCIF10	ENCIF11	ENCIF12

Note: —: Do not set.

18.2.25 PPn Pin Function Control Register (PPnPFS) (n = 0 to 7)

The PPn pin function control register (PPnPFS) selects the function of the pin to use. The PPnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection.

Address(es): PP0PFS A000 02B8h, PP1PFS A000 02B9h, PP2PFS A000 02BAh, PP3PFS A000 02BBh, PP4PFS A000 02BCh, PP5PFS A000 02BDh, PP6PFS A000 02BEh, PP7PFS A000 02BFh



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.34.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

Table 18.34 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PP0	PP1	PP2	PP3	PP4	PP5	PP6	PP7
000000b (Value after reset)	Hi-Z							
000010b	—	MTIOC0D	MTIOC0C	MTIOC0B	MTIOC0A	—	—	—
000011b	—	—	TCLKH	TCLKC	—	—	TIOCA11	TCLKF
000100b	—	—	—	—	—	—	—	TCLKH
000110b	—	—	—	—	—	PO22	—	—
000111b	POE8#	—	—	—	—	—	—	—
001011b	—	—	—	—	—	—	RXD1	SCK1
011000b	TEND0	DACK0	—	—	—	—	—	DACK1
100111b	—	—	—	—	—	—	TRACECTL	TRACECLK
101000b	MCLK2	MDAT2	MCLK1	MDAT1	MCLK0	MDAT0	—	—
101011b	—	—	—	—	—	—	ENCIF06	—

Note: —: Do not set.

18.2.26 PRn Pin Function Control Register (PRnPFS) (n = 0 to 7)

The PRn pin function control register (PRnPFS) selects the function of the pin to use. The PRnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PR0PFS A000 02C0h, PR1PFS A000 02C1h, PR2PFS A000 02C2h, PR3PFS A000 02C3h, PR4PFS A000 02C4h, PR5PFS A000 02C5h, PR6PFS A000 02C6h, PR7PFS A000 02C7h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.35.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.35 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PR0	PR1	PR2	PR3	PR4	PR5	PR6	PR7
000000b (Value after reset)	Hi-Z							
000011b	TCLKE	—	TIOCA11	TIOCA10	TIOCA9	TIOCA8	TIOCA7	TIOCA6
000100b	TCLKG	—	TIOCB11	TIOCB10	TIOCB9	TIOCB8	TIOCB7	TIOCB6
000111b	—	POE4#	—	—	—	—	—	—
001011b	TXD1	CTS1#	RTS1#	—	—	—	—	—
011000b	DREQ1	TEND1	—	—	—	—	—	—
100111b	TRACEDATA0	TRACEDATA1	TRACEDATA2	TRACEDATA3	TRACEDATA4	TRACEDATA5	TRACEDATA6	TRACEDATA7
101011b	ENCIF07	ENCIF08	ENCIF00	ENCIF01	ENCIF02	ENCIF03	ENCIF04	ENCIF05

Note: —: Do not set.

18.2.27 PSn Pin Function Control Register (PSnPFS) (n = 0 to 7)

The PSn pin function control register (PSnPFS) selects the function of the pin to use. The PSnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PS0PFS A000 02C8h, PS1PFS A000 02C9h, PS2PFS A000 02CAh, PS3PFS A000 02CBh, PS4PFS A000 02CCh, PS5PFS A000 02CDh, PS6PFS A000 02CEh, PS7PFS A000 02CFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.36.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.36 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PS0	PS1	PS2	PS3	PS4	PS5	PS6	PS7
000000b (Value after reset)	Hi-Z							
000010b	MTIOC7D	MTIOC7B	MTIOC7C	MTIOC7A	MTIOC6D	MTIOC6B	—	—
000011b	—	—	—	—	—	—	TIOCA5	TIOCA4
000100b	—	—	—	—	—	—	TIOCB5	TIOCB4
000110b	—	—	—	—	—	—	PO23	PO24
001100b	—	—	—	—	—	—	RXD2	TXD2
010111b	AUDIO_CLK	SSISCK0	SSIWS0	SSIRXD0	SSITXD0	—	—	—
101011b	—	—	—	—	—	—	ENCIF06	—

Note: —: Do not set.

18.2.28 PTn Pin Function Control Register (PTnPFS) (n = 0 to 7)

The PTn pin function control register (PTnPFS) selects the function of the pin to use. The PTnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PT0PFS A000 02D0h, PT1PFS A000 02D1h, PT2PFS A000 02D2h, PT3PFS A000 02D3h, PT4PFS A000 02D4h, PT5PFS A000 02D5h, PT6PFS A000 02D6h, PT7PFS A000 02D7h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.37.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.37 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PT0	PT1	PT2	PT3	PT4	PT5	PT6	PT7
000000b (Value after reset)	Hi-Z							
000011b	TIOCA3	TIOCA2	TIOCA1	TIOCA0	—	—	—	—
000100b	TIOCB3	TIOCB2	TIOCB1	TIOCB0	—	—	—	—
000110b	PO25	PO26	PO27	PO28	PO29	PO30	—	—
001100b	SCK2	RTS2#	—	CTS2#	—	—	—	—
011000b	—	—	—	—	—	TEND2	DREQ2	DACK2
100011b	—	—	—	—	CS3#	BS#	A21	A22
101011b	ENCIF07	ENCIF08	—	ENCIF09	—	—	—	ENCIF10

Note: —: Do not set.

18.2.29 PUn Pin Function Control Register (PUnPFS) (n = 0 to 7)

The PUn pin function control register (PUnPFS) selects the function of the pin to use. The PUnPFS register is protected by the write protect register (PWPR). Modifications to this register can only be made after releasing protection. The ISEL bit of the pin without the IRQn function is reserved. A value after a reset must be written.

Address(es): PU0PFS A000 02D8h, PU1PFS A000 02D9h, PU2PFS A000 02DAh, PU3PFS A000 02DBh, PU4PFS A000 02DCh, PU5PFS A000 02DDh, PU6PFS A000 02DEh, PU7PFS A000 02DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	ISEL	PSEL[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	PSEL[5:0]	Pin Function Select	These bits select the peripheral function. For details on each function, see Table 18.38.	R/W
b6	ISEL	Interrupt Input Function Select	0: Do not use as the IRQn input pin. 1: Use as the IRQn input pin.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PSEL[5:0] Bits (Pin Function Select)

These bits select the peripheral function to assign to a pin.

ISEL Bit (Interrupt Input Function Select)

Set this bit to 1 to use the given pin as the IRQ pin. This bit can be used with peripheral functions. Note that IRQn (external pin interrupt) with the same number cannot be enabled for two or more pins.

Table 18.38 Register Settings for the Input/Output Function in the 320-pin FBGA Pin

PSEL[5:0] Setting	Pin							
	PU0	PU1	PU2	PU3	PU4	PU5	PU6	PU7
000000b (Value after reset)	Hi-Z							
000011b	TIOCA10	TIOCA11	TIOCD9	TIOCD6	TIOCC9	TIOCC6	TCLKF	—
001100b	—	SCK3	RXD3	TXD3	CTS3#	RTS3#	CTS4#	RXD4
010100b	ETH2_RXER	ETH2_RXC	ETH2_CRS	ETH2_COL	MII2_MDC	MII2_MDIO	—	—
010110b	—	—	—	—	—	—	PHYRESETOUT#	CATIRQ *1

Note: —: Do not set.
Note 1. Only for products incorporating an EtherCAT (optional)

18.3 Usage Notes

18.3.1 Procedure for Specifying the Pin Input/Output Function

To specify the pin input/output function:

1. Set the port direction register (PDR) of the applicable pin to 00, and clear the port mode register (PMR) to 0 to set them as a general I/O port.
2. For each peripheral module, set the I/O signal to assign to the applicable pin.
3. Clear the PWPR.B0WI bit to 0, and then set the PWPR.PFSWE bit to 1. By doing so, make the Pmn pin function control register (PmnPFS) (m = 0 to 9, A to H, J to N, P, R to U, n = 0 to 7) writable.
4. By using the PmnPFS.PSEL[5:0] bits, set the pin input/output function.
5. Clear the PWPR.PFSWE bit to 0 to disable writing to the PmnPFS register.
6. Set the applicable bit of the PMR register corresponding to the selected pin to 1 as necessary to switch to the pin input/output function of the peripheral function.
7. Set the PDR register to 10 as necessary to enable reading the port status.

18.3.2 Notes on MPC Register Setting

1. Settings of the Pmn pin function control register (PmnPFS) (m = 0 to 9, A to H, J to N, P, R to U, n = 0 to 7) should be made only while the PMR register for the target pin is cleared to 0. If the PmnPFS is set while the applicable bit of the PMR register is 1, unexpected edges might be input for the input function. Besides, unexpected pulses might be output for the output function.
2. When setting the PmnPFS.ISEL bit to use the IRQ or NMI pin interrupt, follow the procedure described in [For IRQ pins] of section 12.3.3, External Pin Interrupts and section 12.3.4, NMI Pin Interrupts. If the PmnPFS.ISEL bit is set using a different procedure, unexpected edges may be input, leading to malfunction.
3. Only the allowed functions should be specified for the PmnPFS register. If a value that is not allowed for the register is specified, correct operation is not guaranteed.
4. Do not assign a single function to multiple pins through the MPC settings.
5. Ports 8 (P86 and P87 only), 9, and D also function as analog input/output pins for the A/D converter. When using these ports as analog input/output pins, disable the pin by clearing the bit of the corresponding pin in the port mode register (PMR) to 0, and setting the port direction register (PDR) to 00, and set the PmnPFS.ASEL bit to 1, and then setting the PmnPFS.ASEL bit to 1 to avoid degradation of accuracy.
6. Points to note regarding the port mode register (PMR), port direction register (PDR), and Pmn pin function control register (PmnPFS) settings for pins that have multiplexed pin functions are listed in Table 18.39. The pin states are readable if the value of the ASEL bit of the Pmn pin is 0. Ensure that the bit corresponding to the applicable pin of the PMR register is 0 when changes to the PSEL[5:0] bits are made.

Table 18.39 Register Settings

Item	PMR.Bn	PDR.Bn[1:0]	PmnPFS			Note
			ASEL	ISEL	PSEL[5:0]	
After a reset is canceled	0 *1	00	0	0	000000b *1	In the disabled (Hi-z input protection) state after a reset is canceled.
Not used	0	00	0	0	N	
General I/O port	0	10/11 *2	0	0/1 *3	N	Set the PmnPFS.ISEL bit to 1 if these are multiplexed with interrupt inputs.
Peripheral functions	1	00/10 *4	0	0/1 *3	Peripheral functions (See Table 18.2 to Table 18.38.)	Set the PmnPFS.ISEL bit to 1 if it is multiplexed with interrupt inputs. Set the PDR.Bn[1:0] bits to 10 if it is multiplexed with the port read function (reading the pin status of the port in the PIDR.Bn bit).
Interrupt input (NMI, IRQ0 to IRQ15)	0	10	0	1	N	
Analog inputs	0	00	1	N *5	N	For use as analog input, set the given pin to “non-use” by setting the associated bits of the port mode register (PMR) and the port direction register (PDR) to 0 and 00, respectively. After that, set the PmnPFS.ASEL bit to 1. This procedure avoids deterioration of the precision of values.

N: Setting is not required.

Note 1. Values after reset for PORT3.PMR, P33PFS.PSEL[5:0], and P34PFS.PSEL[5:0] are different.
For details on the PSEL[5:0] bits, see section 18.2.5, P3n Pin Function Control Register (P3nPFS) (n = 0 to 7).
For details on PORT3.PMR, see section 17.3.4, Port Mode Register (PMR).

Note 2. Setting the PDR.Bn[1:0] bits to 10 makes the register function as a general input port.
Setting the PDR.Bn[1:0] bits to 11 makes the register function as a general output port.

Note 3. If the PmnPFS.ISEL bit is set to 0, the register does not function as an IRQ pin.
Setting the PmnPFS.ISEL bit to 1 makes the register function as an IRQ pin (when the IRQ function is multiplexed).

Note 4. If the PDR.Bn[1:0] bits is set to 00, the port read function (reading the pin status of the port with the PIDR.Bn bit) cannot be used.
Setting the PDR.Bn[1:0] bits to 10 enables reading of the port pin status.

Note 5. Setting the PmnPFS.ISEL bit to 1 does not make the register function as an IRQn input pin.

18.3.3 Usage Notes on Port Read Function

When a peripheral module for a pin which is bidirectional or an output is in use and the value of the PDR bits for the given pin is changed from 00 (initial value) to 10 (input enabled), the state of the pin can be read (port read function) from the PIDR register while the peripheral function is in use.

When a peripheral module for a pin which is an input or any of the input/output pin functions listed in Table 18.40 is in use, input is always enabled and the pin function can be used in parallel with port reading without changing the setting of the PDR register.

A shoot-through current flows when an external pin enters the Hi-Z state. An external pin must be pulled down or up when in the Hi-Z state.

When the pin functions in Table 18.41 are in use with an external bus controller, setting the PDR register to 10 (input enabled) is prohibited because the external bus controller controls enabling and disabling of input to the pins.

Table 18.40 List of Modules and Associated Pin Functions for Which Input is Always Enabled (1 / 4)

Module/Function	Channel	Pin Function
Multi-function timer unit 3*1	MTU0	MTIOC0A (Input/output)
		MTIOC0B (Input/output)
		MTIOC0C (Input/output)
	MTU1	MTIOC1A (Input/output)
		MTIOC1B (Input/output)
	MTU2	MTIOC2A (Input/output)
		MTIOC2B (Input/output)
	MTU3	MTIOC3A (Input/output)
		MTIOC3B (Input/output)
		MTIOC3C (Input/output)
		MTIOC3D (Input/output)
	MTU4	MTIOC4A (Input/output)
		MTIOC4B (Input/output)
		MTIOC4C (Input/output)
		MTIOC4D (Input/output)
	MTU6	MTIOC6A (Input/output)
		MTIOC6B (Input/output)
		MTIOC6C (Input/output)
		MTIOC6D (Input/output)
	MTU7	MTIOC7A (Input/output)
		MTIOC7B (Input/output)
		MTIOC7C (Input/output)
		MTIOC7D (Input/output)
	MTU8	MTIOC8A (Input/output)
		MTIOC8B (Input/output)
		MTIOC8C (Input/output)
		MTIOC8D (Input/output)

Table 18.40 List of Modules and Associated Pin Functions for Which Input is Always Enabled (2 / 4)

Module/Function	Channel	Pin Function
General PWM timer*1	GPT0	GTIOC0A (Input/output)
		GTIOC0B (Input/output)
	GPT1	GTIOC1A (Input/output)
		GTIOC1B (Input/output)
	GPT2	GTIOC2A (Input/output)
		GTIOC2B (Input/output)
	GPT3	GTIOC3A (Input/output)
		GTIOC3B (Input/output)
16-bit timer pulse unit	TPU0 (unit 0)	TIOCA0 (Input/output)
		TIOCB0 (Input/output)
		TIOCC0 (Input/output)
		TIOCD0 (Input/output)
	TPU1 (Unit 0)	TIOCA1 (Input/output)
		TIOCB1 (Input/output)
	TPU2 (Unit 0)	TIOCA2 (Input/output)
		TIOCB2 (Input/output)
	TPU3 (Unit 0)	TIOCA3 (Input/output)
		TIOCB3 (Input/output)
		TIOCC3 (Input/output)
		TIOCD3 (Input/output)
	TPU4 (Unit 0)	TIOCA4 (Input/output)
		TIOCB4 (Input/output)
	TPU5 (Unit 0)	TIOCA5 (Input/output)
		TIOCB5 (Input/output)
	TPU6 (Unit 1)	TIOCA6 (Input/output)
		TIOCB6 (Input/output)
		TIOCC6 (Input/output)
		TIOCD6 (Input/output)
	TPU7 (Unit 1)	TIOCA7 (Input/output)
		TIOCB7 (Input/output)
	TPU8 (Unit 1)	TIOCA8 (Input/output)
		TIOCB8 (Input/output)
	TPU9 (Unit 1)	TIOCA9 (Input/output)
		TIOCB9 (Input/output)
		TIOCC9 (Input/output)
		TIOCD9 (Input/output)
	TPU10 (Unit 1)	TIOCA10 (Input/output)
		TIOCB10 (Input/output)
	TPU11 (Unit 1)	TIOCA11 (Input/output)
		TIOCB11 (Input/output)

Table 18.40 List of Modules and Associated Pin Functions for Which Input is Always Enabled (3 / 4)

Module/Function	Channel	Pin Function
Serial Communications Interface with FIFO (SCIFA)	SCI0	RXD0 (Input)
		SCK0 (Input/output)
		CTS0# (Input/output)
		RTS0# (Output)
	SCI1	RXD1 (Input)
		SCK1 (Input/output)
		CTS1# (Input/output)
		RTS1# (Output)
	SCI2	RXD2 (Input)
		SCK2 (Input/output)
		CTS2# (Input/output)
		RTS2# (Output)
	SCI3	RXD3 (Input)
		SCK3 (Input/output)
		CTS3# (Input/output)
		RTS3# (Output)
	SCI4	RXD4 (Input)
		SCK4 (Input/output)
		CTS4# (Input/output)
		RTS4# (Output)
Ethernet controller	Ether0	ETH_MDIO (Input/output)
	Ether2	MII2_MDIO (Input/output)
EtherCAT slave controller (optional)	EtherCAT	CATI2CCLK (Input/output)
Serial peripheral interface	RSPI0	RSPCK0 (Input/output)
		MOSI0 (Input/output)
		MISO0 (Input/output)
		SSL00 (Input/output)
	RSPI1	RSPCK1 (Input/output)
		MOSI1 (Input/output)
		MISO1 (Input/output)
		SSL10 (Input/output)
		SSL11 (Output)
	RSPI2	RSPCK2 (Input/output)
		MOSI2 (Input/output)
		MISO2 (Input/output)
		SSL20 (Input/output)
	RSPI3	RSPCK3 (Input/output)
		MOSI3 (Input/output)
		MISO3 (Input/output)
		SSL30 (Input/output)
SPI multi I/O bus controller		SPBMO/SPBIO0 (Input/output)
		SPBMI/SPBIO1 (Input/output)
		SPBIO2 (Input/output)
		SPBIO3 (Input/output)

Table 18.40 List of Modules and Associated Pin Functions for Which Input is Always Enabled (4 / 4)

Module/Function	Channel	Pin Function
Serial sound interface	SSI0	SSISCK0 (Input/output)
		SSIWS0 (Input/output)
ΔΣ interface		MCLK0 (Input/output)
		MCLK1 (Input/output)
		MCLK2 (Input/output)
		MCLK3 (Input/output)

Note 1. When the POE places a pin in the Hi-Z state, input to the pin is disabled. An external pin being in the Hi-Z state thus does not create a problem.

Table 18.41 List of PDR Setting Prohibited Function

Module/Function	Pin Function
External bus controller	D0 (Input/output)
	D1 (Input/output)
	D2 (Input/output)
	D3 (Input/output)
	D4 (Input/output)
	D5 (Input/output)
	D6 (Input/output)
	D7 (Input/output)
	D8 (Input/output)
	D9 (Input/output)
	D10 (Input/output)
	D11 (Input/output)
	D12 (Input/output)
	D13 (Input/output)
	D14 (Input/output)
	D15 (Input/output)
	D16 (Input/output)
	D17 (Input/output)
	D18 (Input/output)
	D19 (Input/output)
	D20 (Input/output)
	D21 (Input/output)
	D22 (Input/output)
	D23 (Input/output)
	D24 (Input/output)
	D25 (Input/output)
	D26 (Input/output)
	D27 (Input/output)
	D28 (Input/output)
	D29 (Input/output)
	D30 (Input/output)
	D31 (Input/output)
	WAIT# (Input)

18.3.4 Notes on Port Settings for MTU and GPT

(1) MTU

If a set of pins capable of 6-phase PWM output is being used with the MTU in complementary PWM mode or reset-synchronized PWM mode, some restrictions apply to the port settings for the pins in use as MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, and MTIOC4D. For details on the individual port settings, see section 19.6.28, Notes on Port Settings in Complementary PWM Mode or Reset-Synchronized PWM Mode, of section 19, Multi-Function Timer Pulse Unit (MTU3a).

(2) GPT

If a set of pins capable of 6-phase PWM output pins is being used with channels 0, 1, or 2 of the GPT, some restrictions apply to the port settings for the pins in use as GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B. For details on the individual port settings, see section 21.9.5, Notes on Port Settings in PWM Output Operating Mode, of section 21, General PWM Timer (GPTa).

19. Multi-Function Timer Pulse Unit (MTU3a)

19.1 Overview

This LSI has an on-chip multi-function timer pulse unit (MTU3a), consisting of eight 16-bit timer channels and one 32-bit timer channel.

Table 19.1 shows the specifications of the MTU and Table 19.2 lists the functions of the MTU. Figure 19.1 and Figure 19.2 are block diagrams of the MTU.

Table 19.1 Specifications of the MTU

Item	Description
Pulse input/output	28 lines maximum
Pulse input	3 lines
Count clock	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU1 and 2, and 10 clocks for channel 5)
Operating frequency	PCLKC (150 MHz)
Available operations	[MTU0 to MTU4, MTU6, MTU7, and MTU8] • Waveform output on compare match • Input capture function (noise filter setting available) • Counter-clearing operation • Simultaneous writing to multiple timer counters (TCNT) (excluding MTU8) • Simultaneous clearing on compare match or input capture (excluding MTU8) • Simultaneous input and output to registers in synchronization with counter operations (excluding MTU8) • Up to 12-phase PWM output in combination with synchronous operation (excluding MTU8)
	[MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8] • Buffer operation specifiable
	[MTU1, MTU2] • Phase counting mode specifiable independently (noise filter setting available for external clock input) • Cascade connection operation available (as a 32-bit counter)
	[MTU3, MTU4, MTU6, and MTU7] • Through interlocked operation of MTU3/MTU4 and MTU6/MTU7, the positive and negative signals in six phases (12 phases in total) can be output in complementary-PWM and reset-PWM operation. • In complementary PWM mode, transfer of values from buffer registers to temporary registers on crests and troughs of the timer-counter values or writing to the buffer registers (MTU4.TGRD and MTU7.TGRD) • Double-buffering selectable in complementary PWM mode
	[MTU3 and MTU4] • Through interlocking with channel 0, a mode for driving AC synchronous motors (brushless DC motors) by using complementary PWM output and reset PWM output is settable and allows the selection of two types of waveform output (chopping or level)
	[MTU5] • Capable of operation as a dead-time compensation counter
	[MTU0/MTU5, MTU1, MTU2, and MTU8] 32-bit phase counting mode specifiable by combining MTU1 and MTU2 and through interlocked operation with MTU0/MTU5 and MTU8
Interrupt-skipping function in complementary PWM mode	In complementary PWM mode, interrupts on crests and troughs of counter values and triggers to start conversion by the A/D converter can be skipped
Interrupt sources	43 sources
Buffer operation	Automatic transfer of register data (transfer from the buffer register to the timer register)
Trigger generation	A/D converter start triggers can be generated
	A/D converter start request delaying function enables A/D converter to be started with any desired timing and to be synchronized with PWM output
Low-power consumption function	Module stop mode can be set

Table 19.2 Functions of the MTU (1 / 3)

Item		MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7	MTU8
Count clock*1		PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB MTCLKC MTCLKD MTIOC1A	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB MTCLKC	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTIOC1A	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB	PCLKC/1 PCLKC/2 PCLKC/4 PCLKC/8 PCLKC/16 PCLKC/32 PCLKC/64 PCLKC/256 PCLKC/1024 MTCLKA MTCLKB
General registers (TGR)		TGRA TGRB TGRE	TGRA TGRB TGRALW TGRBLW	TGRA TGRB	TGRA TGRB	TGRA TGRB	TGRU TGRV TGRW	TGRA TGRB	TGRA TGRB	TGRA TGRB
General registers/ buffer registers		TGRC TGRD TGRF	—	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF	—	TGRC TGRD TGRE	TGRC TGRD TGRE TGRF	TGRC TGRD
I/O pins		MTIOC0A MTIOC0B MTIOC0C MTIOC0D	MTIOC1A MTIOC1B	MTIOC2A MTIOC2B	MTIOC3A MTIOC3B MTIOC3C MTIOC3D	MTIOC4A MTIOC4B MTIOC4C MTIOC4D	MTIC5U MTIC5V MTIC5W	MTIOC6A MTIOC6B MTIOC6C MTIOC6D	MTIOC7A MTIOC7B MTIOC7C MTIOC7D	MTIOC8A MTIOC8B MTIOC8C MTIOC8D
Counter clear function		TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture	TGR compare match or input capture
Compare match output	0 output	√	√	√	√	√	—	√	√	√
	1 output	√	√	√	√	√	—	√	√	√
	Toggle output	√	√	√	√	√	—	√	√	√
Input capture function		√	√	√	√	√	√	√	√	√
Synchronous operation		√	√	√	√	√	—	√	√	—
PWM mode 1		√	√	√	√	√	—	√	√	—
PWM mode 2		√	√	√	—	—	—	—	—	—
Complementary PWM mode		—	—	—	√	√	—	√	√	—
Reset-synchronized PWM mode		—	—	—	√	√	—	√	√	—
AC synchronous motor drive mode		√	—	—	√	√	—	—	—	—
Phase counting mode		—	√	√	—	—	—	—	—	—
Buffer operation		√	—	—	√	√	—	√	√	√
Dead time compensation counter function		—	—	—	—	—	√	—	—	—

Table 19.2 Functions of the MTU (2 / 3)

Item	MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7	MTU8
DMAC activation	TGRm compare match or input capture (m = A to D)	TGRm compare match or input capture (m = A, B)	TGRm compare match or input capture (m = A, B)	TGRm compare match or input capture (m = A to D)	TGRm compare match or input capture (m = A to D) and TCNT overflow/ underflow (only in complementary PWM mode)	TGRm compare match or input capture (m = U, V, W)	TGRm compare match or input capture (m = A to D)	TGRm compare match or input capture (m = A to D) and TCNT overflow/ underflow (only in complementary PWM mode)	TGRm compare match or input capture (m = A to D)
A/D converter start trigger	TGRA compare match or input capture TGRE compare match	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture, or TCNT underflow (trough) in complementary PWM mode	—	TGRA compare match or input capture	TGRA compare match or input capture, or TCNT underflow (trough) in complementary PWM mode	—
Interrupt sources	Seven sources • Compare match or input capture 0A • Compare match or input capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Compare match0E • Compare match0F • Overflow	Four sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow • Underflow	Four sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow • Underflow	Five sources • Compare match or input capture 3A • Compare match or input capture 3B • Compare match or input capture 3C • Compare match or input capture 3D • Overflow	Five sources • Compare match or input capture 4A • Compare match or input capture 4B • Compare match or input capture 4C • Compare match or input capture 4D • Overflow or underflow (only in complementary PWM mode)	Three sources • Compare match or input capture 5U • Compare match or input capture 5V • Compare match or input capture 5W	Five sources • Compare match or input capture 6A • Compare match or input capture 6B • Compare match or input capture 6C • Compare match or input capture 6D • Overflow	Five sources • Compare match or input capture 7A • Compare match or input capture 7B • Compare match or input capture 7C • Compare match or input capture 7D • Overflow or underflow (only in complementary PWM mode)	Five sources • Compare match or input capture 8A • Compare match or input capture 8B • Compare match or input capture 8C • Compare match or input capture 8D • Overflow
Event link function (output)	Seven sources • Compare match 0A • Compare match 0B • Compare match 0C • Compare match 0D • Compare match 0E • Compare match 0F • Overflow	—	—	Five sources • Compare match 3A • Compare match 3B • Compare match 3C • Compare match 3D • Overflow	Six sources • Compare match 4A • Compare match 4B • Compare match 4C • Compare match 4D • Overflow • Underflow (only in complementary PWM mode)	—	Five sources • Compare match 6A • Compare match 6B • Compare match 6C • Compare match 6D • Overflow	Six sources • Compare match 7A • Compare match 7B • Compare match 7C • Compare match 7D • Overflow • Underflow (only in complementary PWM mode)	—
Event link function (input)	• Start counting • Input capture (to be captured in the TGRA) • Clear [Restart] counting	—	—	• Start counting • Input capture (to be captured in the TGRA) • Clear [Restart] counting	• Start counting • Input capture (to be captured in the TGRA) • Clear [Restart] counting	—	—	—	—

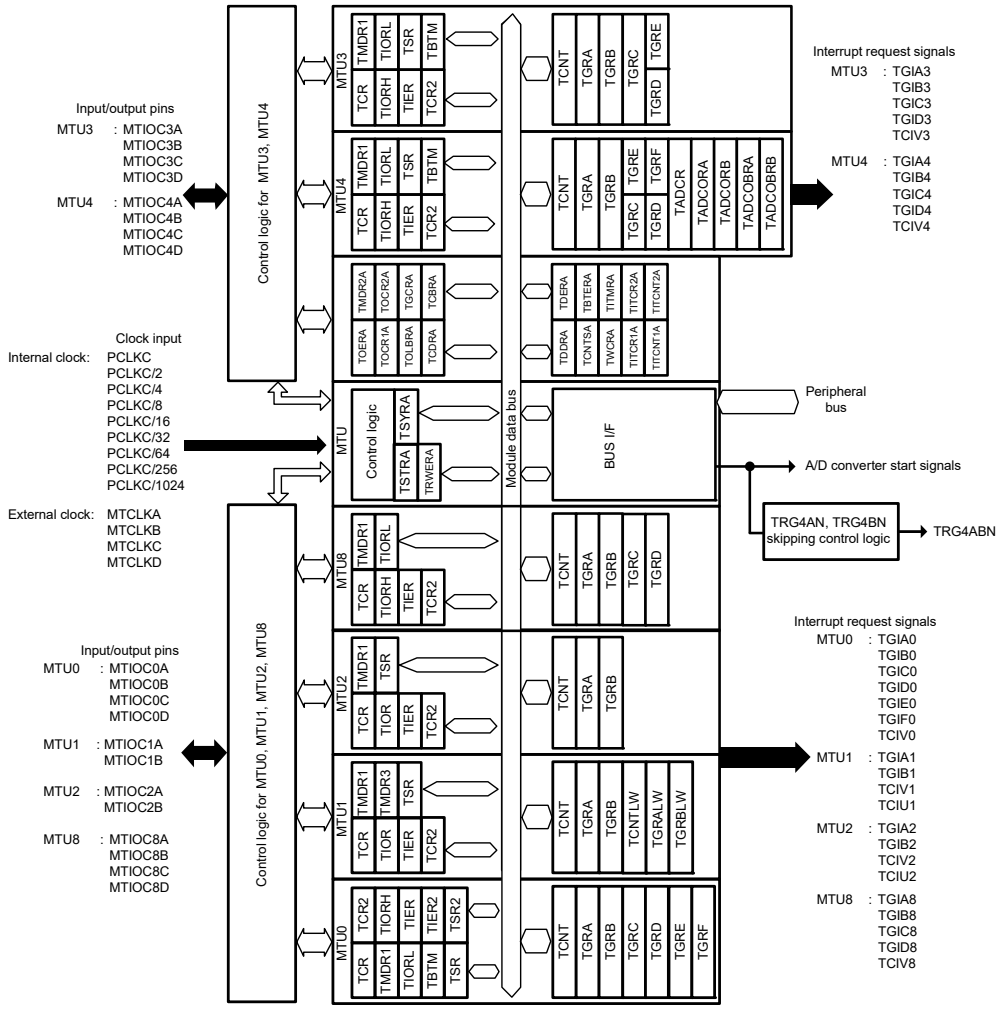
Table 19.2 Functions of the MTU (3 / 3)

Item	MTU0	MTU1	MTU2	MTU3	MTU4	MTU5	MTU6	MTU7	MTU8
A/D converter start request delaying function	—	—	—	—	A/D converter start request at a match between TADCORA and TCNT or A/D converter start request at a match between TADCORB and TCNT	—	—	A/D converter start request at a match between TADCORA and TCNT or A/D converter start request at a match between TADCORB and TCNT	—
Interrupt skipping	—	—	—	Skips TGRA compare match interrupts	Skips TCIV interrupts	—	Skips TGRA compare match interrupts	Skips TCIV interrupts	—
Interrupt skipping 2	—	—	—	—	Skipping in compare count between TADCORA and TCNT, and TADCORB and TCNT	—	—	Skipping in compare count between TADCORA and TCNT, and TADCORB and TCNT	—
Module stop function	Module stop setting by the MSTPCRA.MSTPCRA11 bit*2								

√: Possible —: Not possible

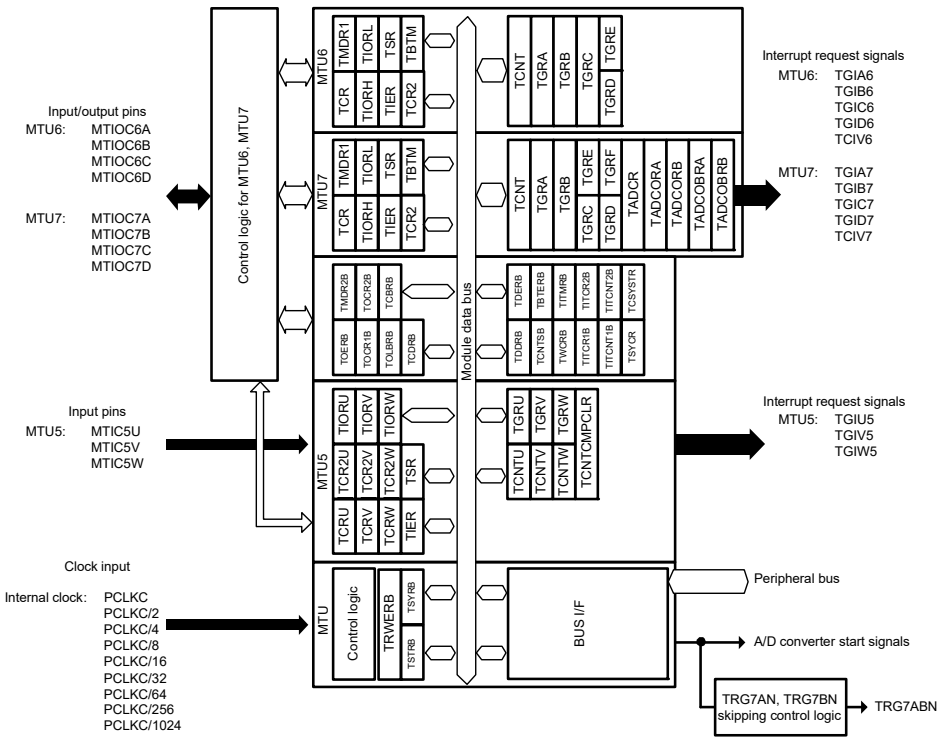
Note 1. The external count clocks not listed in this table are available in phase-counting mode. For details, see section 19.3.6, Phase Counting Mode.

Note 2. For details on the module stop function, see section 9, Low-Power Consumption Function.



TCR: Timer control register
TCR2: Timer control register 2
TMDR1: Timer mode register 1
TMDR2A: Timer mode register 2
TMDR3: Timer mode register 3
TIOR: Timer I/O control register
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIER: Timer interrupt enable register
TIER2: Timer interrupt enable register 2
TSR: Timer status register
TSR2: Timer status register 2
TBTM: Timer buffer operation transfer mode register
TCNT: Timer counter
TCNTLW: Timer longword counter
TGRA: Timer general register A
TGRALW: Timer longword general register A
TGRB: Timer general register B
TGRBLW: Timer longword general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TSTRA: Timer start register
TSYRA: Timer synchronous register
TRWERA: Timer read/write enable register
TOERA: Timer output master enable register
TOCR1A: Timer output control register 1
TOCR2A: Timer output control register 2
TOLBRA: Timer output level buffer register
TGCRA: Timer gate control register A
TCNTSA: Timer subcounter
TCDRA: Timer cycle data register
TCBRA: Timer cycle buffer register
TDDRA: Timer dead time data register
TDERA: Timer dead time enable register
TBTERA: Timer buffer transfer set register
TWCRA: Timer waveform control register
TICCR: Timer input capture control register
TADCR: Timer A/D converter start request control register
TADCORA: Timer A/D converter start request cycle set register A
TADCORB: Timer A/D converter start request cycle set register B
TADCOBRA: Timer A/D converter start request cycle set buffer register A
TADCOBRB: Timer A/D converter start request cycle set buffer register B
TITMRA: Timer interrupt skipping mode register
TITCR1A: Timer interrupt skipping set register 1
TITCR2A: Timer interrupt skipping set register 2
TITCNT1A: Timer interrupt skipping counter 1
TITCNT2A: Timer interrupt skipping counter 2

Figure 19.1 Block Diagram of MTU (MTU0 to MTU4, MTU8)



TCR: Timer control register
TCRU: Timer control register U
TCR2U: Timer control register 2U
TCRV: Timer control register V
TCR2V: Timer control register 2V
TCRW: Timer control register W
TCR2W: Timer control register 2W
TMDR1: Timer mode register 1
TMDR2B: Timer mode register 2
TIORH: Timer I/O control register H
TIORL: Timer I/O control register L
TIORU: Timer I/O control register U
TIORV: Timer I/O control register V
TIORW: Timer I/O control register W
TIER: Timer interrupt enable register
TSR: Timer status register
TCNT: Timer counter
TCNTU: Timer counter U
TCNTV: Timer counter V
TCNTW: Timer counter W
TGRA: Timer general register A
TGRB: Timer general register B
TGRC: Timer general register C
TGRD: Timer general register D
TGRE: Timer general register E
TGRF: Timer general register F
TGRU: Timer general register U
TGRV: Timer general register V
TGRW: Timer general register W
TCNTCMPCLR: Timer compare match clear register

TSTRB: Timer start register
TSYRB: Timer synchronous register
TSYCR: Timer synchronous clear register
TCSYSTR: Timer counter synchronous start register
TRWERB: Timer read/write enable register
TOERB: Timer output master enable register
TOCR1B: Timer output control register 1
TOCR2B: Timer output control register 2
TOLBRB: Timer output level buffer register
TCDRB: Timer cycle data register
TCBRB: Timer cycle buffer register
TDDRB: Timer dead time data register
TDERB: Timer dead time enable register
TCNTSB: Timer subcounter
TBTERB: Timer buffer transfer set register
TWCRB: Timer waveform control register
TADCR: Timer A/D converter start request control register
TADCORA: Timer A/D converter start request cycle set register A
TADCORB: Timer A/D converter start request cycle set register B
TADCOBRA: Timer A/D converter start request cycle set buffer register A
TADCOBRB: Timer A/D converter start request cycle set buffer register B
TITMRB: Timer interrupt skipping mode register
TITCR1B: Timer interrupt skipping set register 1
TITCR2B: Timer interrupt skipping set register 2
TITCNT1B: Timer interrupt skipping counter 1
TITCNT2B: Timer interrupt skipping counter 2

Figure 19.2 Block Diagram of MTU (MTU5 to MTU7)

Table 19.3 shows the configuration of pins for the MTU.

Table 19.3 Pin Configuration of the MTU

Channel	Pin Name	I/O	Function
MTU	MTCLKA	Input	External clock A input pin (MTU1/MTU2 phase counting mode A phase input)
	MTCLKB	Input	External clock B input pin (MTU1/MTU2 phase counting mode B phase input)
	MTCLKC	Input	External clock C input pin (MTU1 phase counting mode A phase input)
	MTCLKD	Input	External clock D input pin (MTU2 phase counting mode B phase input)
MTU0	MTIOC0A	I/O	MTU0 TGRA input capture input/output compare output/PWM output pin
	MTIOC0B	I/O	MTU0 TGRB input capture input/output compare output/PWM output pin
	MTIOC0C	I/O	MTU0 TGRC input capture input/output compare output/PWM output pin
	MTIOC0D	I/O	MTU0 TGRD input capture input/output compare output/PWM output pin
MTU1	MTIOC1A	I/O	MTU1 TGRA input capture input/output compare output/PWM output pin
	MTIOC1B	I/O	MTU1 TGRB input capture input/output compare output/PWM output pin
MTU2	MTIOC2A	I/O	MTU2 TGRA input capture input/output compare output/PWM output pin
	MTIOC2B	I/O	MTU2 TGRB input capture input/output compare output/PWM output pin
MTU3	MTIOC3A	I/O	MTU3 TGRA input capture input/output compare output/PWM output pin
	MTIOC3B	I/O	MTU3 TGRB input capture input/output compare output/PWM output pin
	MTIOC3C	I/O	MTU3 TGRC input capture input/output compare output/PWM output pin
	MTIOC3D	I/O	MTU3 TGRD input capture input/output compare output/PWM output pin
MTU4	MTIOC4A	I/O	MTU4 TGRA input capture input/output compare output/PWM output pin
	MTIOC4B	I/O	MTU4 TGRB input capture input/output compare output/PWM output pin
	MTIOC4C	I/O	MTU4 TGRC input capture input/output compare output/PWM output pin
	MTIOC4D	I/O	MTU4 TGRD input capture input/output compare output/PWM output pin
MTU5	MTIC5U	Input	MTU5 TGRU input capture input/external pulse input pin
	MTIC5V	Input	MTU5 TGRV input capture input/external pulse input pin
	MTIC5W	Input	MTU5 TGRW input capture input/external pulse input pin
MTU6	MTIOC6A	I/O	MTU6 TGRA input capture input/output compare output/PWM output pin
	MTIOC6B	I/O	MTU6 TGRB input capture input/output compare output/PWM output pin
	MTIOC6C	I/O	MTU6 TGRC input capture input/output compare output/PWM output pin
	MTIOC6D	I/O	MTU6 TGRD input capture input/output compare output/PWM output pin
MTU7	MTIOC7A	I/O	MTU7 TGRA input capture input/output compare output/PWM output pin
	MTIOC7B	I/O	MTU7 TGRB input capture input/output compare output/PWM output pin
	MTIOC7C	I/O	MTU7 TGRC input capture input/output compare output/PWM output pin
	MTIOC7D	I/O	MTU7 TGRD input capture input/output compare output/PWM output pin
MTU8	MTIOC8A	I/O	MTU8.TGRA input capture input/output compare output pin
	MTIOC8B	I/O	MTU8.TGRB input capture input/output compare output pin
	MTIOC8C	I/O	MTU8.TGRC input capture input/output compare output pin
	MTIOC8D	I/O	MTU8.TGRD input capture input/output compare output pin

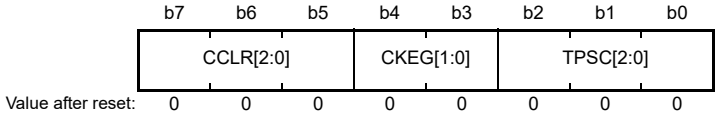
19.2 Register Descriptions

19.2.1 Timer Control Register (TCR)

The TCR register controls the TCNT operation for each channel in combination with the TCR2 register. The MTU has a total of 11 TCR registers, one each for MTU0 to MTU4, MTU 6, MTU7, and MTU8 and three (TCRU, TCRV, and TCRW) for MTU5. TCR values should be specified only while TCNT operation is stopped.

- MTU0, MTU1, MTU2, MTU3, MTU4, MTU6, MTU7, MTU8

Address(es): MTU0.TCR A006 A100h, MTU1.TCR A006 A180h, MTU2.TCR A006 A200h, MTU3.TCR A006 A000h, MTU4.TCR A006 A001h, MTU6.TCR A006 A800h, MTU7.TCR A006 A801h, MTU8.TCR A006 A400h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Time Prescaler Select	See Table 19.6 to Table 19.9.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Count at rising edge 0 1: Count at falling edge 1 x: Count at both edges	R/W
b7 to b5	CCLR[2:0]	Counter Clear Source Select	See Table 19.4 and Table 19.5.	R/W

x: Don't care

TPSC[2:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See Table 19.6 to Table 19.9 for details.

CKEG[1: 0] Bits (Clock Edge Select)

These bits select the input clock edge, including the MTIOC1A pin. When the input clock is counted at both edges, the input clock period is halved (e.g. PCLKC/4 at both edges = PCLKC/2 at rising edge). If phase counting mode is used on MTU1 and MTU2, the setting of these bits is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is PCLKC/2 or slower. When PCLKC/1 or the overflow/underflow in another channel is selected for the input clock, a value can be written to these bits but counter operation compiles with the initial value.

CCLR[2:0] Bits (Counter Clear Source Select)

These bits select the TCNT counter clearing source. See Table 19.4 and Table 19.5 for details.

- MTU5

Address(es): MTU5.TCRU A006 AA84h, MTU5.TCRV A006 AA94h, MTU5.TCRW A006 AAA4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TPSC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TPSC[1:0]	Time Prescaler Select	See Table 19.10.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TPSC[1:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. See Table 19.10 for details.

19.2.2 Timer Control Register 2 (TCR2)

The TCR2 register controls the TCNT operation for each channel in combination with the TCR register. The MTU has a total of 11 TCR registers, one each for MTU0 to MTU4, MTU 6, MTU7, and MTU8 and three (TCR2U, TCR2V, and TCR2W) for MTU5. TCR values should be specified only while TCNT operation is stopped.

- MTU0, MTU3, MTU4, MTU6, MTU7, MTU8

Address(es): MTU0.TCR2 A006 A128h, MTU3.TCR2 A006 A04Ch, MTU4.TCR2 A006 A04Dh, MTU6.TCR2 A006 A84Ch, MTU7.TCR2 A006 A84Dh, MTU8.TCR2 A006 A406h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

- MTU1, MTU2

Address(es): MTU1.TCR2 A006 A194h, MTU2.TCR2 A006 A20Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCB[1:0]		TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC2[2:0]	Time Prescaler Select	See Table 19.6 to Table 19.9.	R/W
b4, b3	PCB[1:0]	Phase Counting Mode Function Expansion Control	Controls expansion of functionality to modes 2, 3, and 5 of phase-counting mode	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

TPSC2[2:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. The clock source can be selected independently for each channel. See Table 19.6 to Table 19.9 for details.

PCB[1:0] Bits (Functional Expansion Control for Phase Counting Modes 2, 3, and 5)

These bits control extended functions for phase counting mode 2, 3, and 5 in MTU1 and MTU2. For details, see section 19.3.6, Phase Counting Mode.

- MTU5

Address(es): MTU5.TCR2U A006 AA85h, MTU5.TCR2V A006 AA95h, MTU5.TCR2W A006 AAA5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CKEG[1:0]		TPSC2[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC2[2:0]	Time Prescaler Select	See Table 19.10.	R/W
b4, b3	CKEG[1:0]	Clock Edge Select	b4 b3 0 0: Counts at the rising edge. 0 1: Counts at the falling edge. 1 x: Counts at both edges.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TPSC2[2:0] Bits (Time Prescaler Select)

These bits select the TCNT counter clock. See Table 19.10 for details.

CKEG[1:0] bits (Clock Edge Select)

These bits select the edge of the counter clock signal output from the MTIOC1A pin.

Table 19.4 CCLR[2:0] (MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8)

	Bit 7	Bit 6	Bit 5	
Channel	CCLR2	CCLR1	CCLR0	Description
MTU0 MTU3 MTU4 MTU6 MTU7 MTU8	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/ synchronous operation*1
	1	0	0	TCNT clearing disabled
	1	0	1	TCNT cleared by TGRC compare match/input capture*2
	1	1	0	TCNT cleared by TGRD compare match/input capture*2
	1	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/ synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC or TSYRB.SYNC bit to 1. However, MTU8 is excluded.
Note 2. When TGRC or TGRD is used as a buffer register, TCNT is not cleared because the buffer register setting has priority and compare match/input capture does not occur.

Table 19.5 CCLR[2:0] (MTU1 and MTU2)

	Bit 7	Bit 6	Bit 5	
Channel	Reserved*2	CCLR1	CCLR0	Description
MTU1 MTU2	0	0	0	TCNT clearing disabled
	0	0	1	TCNT cleared by TGRA compare match/input capture
	0	1	0	TCNT cleared by TGRB compare match/input capture
	0	1	1	TCNT cleared by counter clearing in another channel performing synchronous clearing/synchronous operation*1

Note 1. Synchronous operation is selected by setting the TSYRA.SYNC and TSYRB.SYNC bits to 1.
Note 2. Bit 7 is reserved in MTU1 and MTU2. The bit is read as 0. The write value is ignored.

Table 19.6 TPSC[2:0],TPSC2[2:0] (MTU0)

	TCR2[2:0]			TCR[2:0]			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC22	TPSC21	TPSC20	TPSC2	TPSC1	TPSC0	Description
MTU0	0	0	0	0	0	0	Internal clock: counts on PCLKC/1
	0	0	0	0	0	1	Internal clock: counts on PCLKC/4
	0	0	0	0	1	0	Internal clock: counts on PCLKC/16
	0	0	0	0	1	1	Internal clock: counts on PCLKC/64
	0	0	0	1	0	0	External clock: counts on MTCLKA
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	External clock: counts on MTCLKC pin input
	0	0	0	1	1	1	External clock: counts on MTCLKD pin input
	0	0	1	×	×	×	Internal clock: counts on PCLKC/2
	0	1	0	×	×	×	Internal clock: counts on PCLKC/8
	0	1	1	×	×	×	Internal clock: counts on PCLKC/32
	1	0	0	×	×	×	Internal clock: counts on PCLKC/256
	1	0	1	×	×	×	Internal clock: counts on PCLKC/1024
	1	1	0	×	×	×	Setting prohibited
	1	1	1	×	×	×	External clock: counts on MTIOC1A pin input

×: Don't care

Table 19.7 TPSC[2:0], TPSC2[2:0] (MTU1)

	TCR2[2:0]			TCR[2:0]			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC22	TPSC21	TPSC20	TPSC2	TPSC1	TPSC0	Description
MTU1	0	0	0	0	0	0	Internal clock: counts on PCLKC/1
	0	0	0	0	0	1	Internal clock: counts on PCLKC/4
	0	0	0	0	1	0	Internal clock: counts on PCLKC/16
	0	0	0	0	1	1	Internal clock: counts on PCLKC/64
	0	0	0	1	0	0	External clock: counts on MTCLKA pin input
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	Internal clock: counts on PCLKC/256
	0	0	0	1	1	1	Overflow/underflow of MTU2.TCNT
	0	0	1	×	×	×	Internal clock: counts on PCLKC/2
	0	1	0	×	×	×	Internal clock: counts on PCLKC/8
	0	1	1	×	×	×	Internal clock: counts on PCLKC/32
	1	0	0	×	×	×	Internal clock: counts on PCLKC/1024
	1	0	1	×	×	×	Setting prohibited
	1	1	0	×	×	×	Setting prohibited
	1	1	1	×	×	×	Setting prohibited

×: Don't care

Note: This setting has no effect when MTU1 is in phase-counting mode.

Table 19.8 TPSC[2:0], TPSC2[2:0] (MTU2)

	TCR2[2:0]			TCR[2:0]			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC22	TPSC21	TPSC20	TPSC2	TPSC1	TPSC0	Description
MTU2	0	0	0	0	0	0	Internal clock: counts on PCLKC/1
	0	0	0	0	0	1	Internal clock: counts on PCLKC/4
	0	0	0	0	1	0	Internal clock: counts on PCLKC/16
	0	0	0	0	1	1	Internal clock: counts on PCLKC/64
	0	0	0	1	0	0	External clock: counts on MTCLKA pin input
	0	0	0	1	0	1	External clock: counts on MTCLKB pin input
	0	0	0	1	1	0	External clock: counts on MTCLKC pin input
	0	0	0	1	1	1	Internal clock: counts on PCLKC/1024
	0	0	1	×	×	×	Internal clock: counts on PCLKC/2
	0	1	0	×	×	×	Internal clock: counts on PCLKC/8
	0	1	1	×	×	×	Internal clock: counts on PCLKC/32
	1	0	0	×	×	×	Internal clock: counts on PCLKC/256
	1	0	1	×	×	×	Setting prohibited
	1	1	0	×	×	×	Setting prohibited
	1	1	1	×	×	×	Setting prohibited

×: Don't care

Note: When the MTU2 is in phase counting mode, this setting is invalid.

Table 19.9 TPSC[2:0], TPSC2[2:0] (MTU3, MTU4, MTU6, MTU7, and MTU8)

	TCR2[2:0]			TCR[2:0]			
	Bit 2	Bit 1	Bit 0	Bit 2	Bit 1	Bit 0	
Channel	TPSC22	TPSC21	TPSC20	TPSC2	TPSC1	TPSC0	Description
MTU3 MTU4 MTU6 MTU7 MTU8	0	0	0	0	0	0	Internal clock: counts on PCLKC/1
	0	0	0	0	0	1	Internal clock: counts on PCLKC/4
	0	0	0	0	1	0	Internal clock: counts on PCLKC/16
	0	0	0	0	1	1	Internal clock: counts on PCLKC/64
	0	0	0	1	0	0	Internal clock: counts on PCLKC/256
	0	0	0	1	0	1	Internal clock: counts on PCLKC/1024
	0	0	0	1	1	0	External clock: counts on MTCLKA pin input
	0	0	0	1	1	1	External clock: counts on MTCLKB pin input
	0	0	1	×	×	×	Internal clock: counts on PCLKC/2
	0	1	0	×	×	×	Internal clock: counts on PCLKC/8
	0	1	1	×	×	×	Internal clock: counts on PCLKC/32
	1	0	0	×	×	×	Setting prohibited
	1	0	1	×	×	×	Setting prohibited
	1	1	0	×	×	×	Setting prohibited
	1	1	1	×	×	×	Setting prohibited

×: Don't care

Table 19.10 TPSC2[2:0], TPSC[1:0] (MTU5)

	TCR2[2:0]			TCR[1:0]		
	Bit 2	Bit 1	Bit 0	Bit 1	Bit 0	
Channel	TPSC22	TPSC21	TPSC20	TPSC1	TPSC0	Description
MTU5	0	0	0	0	0	Internal clock: counts on PCLKC/1
	0	0	0	0	1	Internal clock: counts on PCLKC/4
	0	0	0	1	0	Internal clock: counts on PCLKC/16
	0	0	0	1	1	Internal clock: counts on PCLKC/64
	0	0	1	×	×	Internal clock: counts on PCLKC/2
	0	1	0	×	×	Internal clock: counts on PCLKC/8
	0	1	1	×	×	Internal clock: counts on PCLKC/32
	1	0	0	×	×	Internal clock: counts on PCLKC/256
	1	0	1	×	×	Internal clock: counts on PCLKC/1024
	1	1	0	×	×	Setting prohibited
	1	1	1	×	×	Internal clock: counts on MTIOC1A pin input

Note: Bits 7 to 2 in the TCR register are reserved for MTU5. These bits are read as 0. The write value should be 0.

19.2.3 Timer Mode Register 1 (TMDR1)

The TMDR1 register specifies the operating mode of each channel. The MTU has a total of eight TMDR1 registers, one each for MTU0 to MTU4, MTU 6, MTU7, and MTU8. TMDR1 register values should be specified only while TCNT operation is stopped.

- MTU0.TMDR1

Address(es): MTU0.TMDR1 A006 A101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BFE	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU1.TMDR1, MTU2.TMDR1

Address(es): MTU1.TMDR1 A006 A181h, MTU2.TMDR1 A006 A201h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TMDR1, MTU4.TMDR1, MTU6.TMDR1, MTU7.TMDR1, MTU8.TMDR1

Address(es): MTU3.TMDR1 A006 A002h, MTU4.TMDR1 A006 A003h, MTU6.TMDR1 A006 A802h, MTU7.TMDR1 A006 A803h, MTU8.TMDR1 A006 A401h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	These bits specify the timer operating mode. See Table 19.11 for details.	R/W
b4	BFA	Buffer Operation A	0: TGRA and TGRC operate normally 1: TGRA and TGRC used together for buffer operation	R/W
b5	BFB	Buffer Operation B	0: TGRB and TGRD operate normally 1: TGRB and TGRD used together for buffer operation	R/W
b6	BFE	Buffer Operation E	0: MTU0.TGRE and MTU0.TGRF operate normally 1: MTU0.TGRE and MTU0.TGRF used together for buffer operation	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

MD[3:0] Bits (Mode Select)

These bits specifies the operating mode of the timer. See Table 19.11.

BFA Bit (Buffer Operation A)

This bit specifies whether to operate TGRA in the normal way or to use TGRA and TGRC together for buffer operation. When TGRC is used as a buffer register, TGRC input capture/output compare does not take place in a mode other than complementary PWM mode, but TGRC compare match takes place in complementary PWM mode. If MTU4 compare match takes place in the Tb interval of complementary PWM mode, clear the TGIEC bit in the timer interrupt enable register (MTU4.TIER) to 0.

In reset synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFA bit of MTU3.TMDR1 (MTU6.TMDR1). The BFA bit of MTU4.TMDR1 (MTU7.TMDR1) should be set to 0.

In MTU1 and MTU2, which have no TGRC, this bit is reserved. It is read as 0. The write value should be 0. For details about the Tb interval of complementary PWM mode, see Figure 19.50.

BFB Bit (Buffer Operation B)

This bit specifies whether to operate TGRB in the normal way or to use TGRB and TGRD together for buffer operation. When TGRD is used as a buffer register, TGRD input capture/output compare does not usually take place, but TGRD compare match takes place in complementary PWM mode. If MTU4 compare match takes place in the Tb interval of complementary PWM mode, clear the TGIED bit in the timer interrupt enable register (MTU4.TIER) to 0.

In reset synchronized PWM mode or complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in the BFB bit of MTU3.TMDR1 (MTU6.TMDR1). The BFB bit of MTU4.TMDR1 (MTU7.TMDR1) should be set to 0.

In MTU1 and MTU2, which have no TGRD, this bit is reserved. It is read as 0. The write value should be 0. For details about the Tb interval of complementary PWM mode, see Figure 19.50.

BFE Bit (Buffer Operation E)

This bit specifies whether to operate MTU0.TGRE and MTU0.TGRF in the normal way or to use them together for buffer operation. TGRF compare match takes place even when TGRF is used as a buffer register.

In MTU1 to MTU4, MTU6, MTU7, and MTU8, this bit is reserved. It is read as 0. The write value should be 0.

Table 19.11 Operating Mode Setting by MD[3:0] Bits (MTU0 to MTU4, MTU6 to MTU8)

Bit 3	Bit 2	Bit 1	Bit 0		MTU0	MTU1	MTU2	MTU3	MTU4	MTU6	MTU7	MTU8
MD3	MD2	MD1	MD0	Description								
0	0	0	0	Normal operation (normal mode)	√	√	√	√	√	√	√	√
0	0	0	1	Setting prohibited								
0	0	1	0	PWM mode 1	√	√	√	√	√	√	√	
0	0	1	1	PWM mode 2	√	√	√					
0	1	0	0	Phase counting mode 1		√	√					
0	1	0	1	Phase counting mode 2		√	√					
0	1	1	0	Phase counting mode 3		√	√					
0	1	1	1	Phase counting mode 4		√	√					
1	0	0	0	Reset-synchronized PWM mode*1				√		√		
1	0	0	1	Phase counting mode 5		√	√					
1	0	1	x	Setting prohibited								
1	1	0	0	Setting prohibited								
1	1	0	1	Complementary PWM mode 1 (transfer at crest)*1				√		√		
1	1	1	0	Complementary PWM mode 2 (transfer at trough)*1				√		√		
1	1	1	1	Complementary PWM mode 3 (transfer at crest and trough)*1				√		√		

x: Don't care

Note 1. Reset-synchronized PWM mode and complementary PWM mode can only be set for MTU3 and MTU6. When MTU3 or MTU6 is set to reset-synchronized PWM mode or complementary PWM mode, the MTU4 or MTU7 settings become ineffective and automatically conform to the MTU3 or MTU6 setting, respectively. MTU4 and MTU7 should be set to the initial values (normal operation).

19.2.4 Timer Mode Registers 2 (TMDR2A, TMDR2B)

TMDR2 specifies the double buffer function in complementary PWM mode 3 (transfer at the crest and trough of the counter value). The MTU has two TMDR2 registers, one each for MTU3 (TMDR2A) and MTU6 (TMDR2B). TMDR2A and TMDR2B values should be specified only while TCNT operation is stopped.

Address(es): MTU.TMDR2A A006 A070h, MTU.TMDR2B A006 A870h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DRS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DRS	Double Buffer Select	0: Double buffer function is disabled 1: Double buffer function is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DRS Bit (Double Buffer Select)

This bit enables or disables the double buffer function in complementary PWM mode.

19.2.5 Timer Mode Register 3 (TMDR3)

The TMDR3 register controls access in longword units to the combination of MTU1 and MTU2, and there is only one register, which is in MTU1.
Such access can proceed when the LWA bit is set in the ways listed inTable 19.12.

Address(es): MTU1.TMDR3 A006 A191h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PHCKSEL	LWA
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	LWA	MTU1/MTU2 Combination Long-word Access Control	0: 16-bit access is enabled. 1: 32-bit access is enabled.	R/W
b1	PHCKSEL	External Input Phase Clock Select	Selects the external clock pin for phase counting mode. 0: MTCLKA and MTCLKB are selected for the external phase clock. 1: MTCLKC and MTCLKD are selected for the external phase clock.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

LWA Bit (Longword Access Control)

This bit selects a 32-bit access in combination of MTU1 and MTU2. Set this bit only in 32-bit phase counting mode.
When LWA is cleared to 0, the MTU1.TCNTLW, MTU1.TGRALW, and MTU1.TGRBLW registers cannot be accessed. This bit is read as 0000 0000h.
When LWA is set to 1, the MTU1.TCNT, MTU2.TCNT, MTU1.TGRA, MTU2.TGRA, MTU1.TGRB, and MTU2.TGRB registers cannot be accessed. This bit is read as 0000 0000h.
The settings of the control registers (TCR, TCR2, TIOR, and TMDR1) in MTU1 take priority because MTU1 and MTU2 operates together while LWA = 1.
In this case, the settings of the control registers in MTU2 are ignored. Furthermore, MTU2 input capture and compare match are disabled, which in turn disables any linked operation with the ELC.
Initialize the counters and general registers in MTU1 and MTU2 prior to rewriting to the LWA bit.

PHCKSEL Bit (External Input Phase Clock Select)

When the MTU1 and MTU2 registers are combined for 32-bit phase counting mode or MTU2 phase counting mode, this bit selects the external input clock pin on which A- or B-phase signal is to be input. See Table 19.66, Clock Input Pins in Phase Counting Mode for details.

Table 19.12 Setting and Combination of the TMDR3 Register

	TMDR3.LWA = 0		TMDR3.LWA = 1	
Register	**Symbol**	**Access mode**	**Symbol**	**Access mode**
Counter in MTU1*1	MTU1.TCNT	Word	MTU1.TCNTLW	Longword
Counter in MTU2	MTU2.TCNT	Word		
General register A in MTU1	MTU1.TGRA	Word	MTU1.TGRALW	Longword
General register A in MTU2	MTU2.TGRA	Word		
General register B in MTU1	MTU1.TGRB	Word	MTU1.TGRBLW	Longword
General register B in MTU2	MTU2.TGRB	Word		

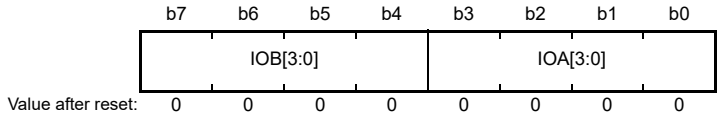
Note 1. When the LWA bit is set to 1, setting the counter clock for MTU1 as MTU2.TCNT overflow/underflow is not required.

19.2.6 Timer I/O Control Register (TIOR)

The TIOR register controls the TGR register. The MTU has a total of 17 TIOR registers, two each for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8, one each for MTU1 and MTU2, and three (MTU5.TIORU/V/W) for MTU5.
Note that TIOR is affected by the TMDR1 setting.
The initial output specified by TIOR is valid when the counter is stopped (the CST bit in TSTRA and the CST bit in TSTRB are cleared to 0). In PWM mode 2, the output when the counter is cleared to 0 is specified.
When TGRC or TGRD is designated for buffer operation, this setting is invalid and the register operates as a buffer register.

- MTU0.TIORH, MTU1.TIOR, MTU2.TIOR, MTU3.TIORH, MTU4.TIORH, MTU6.TIORH, MTU7.TIORH, MTU8.TIORH

Address(es): MTU0.TIORH A006 A102h, MTU1.TIOR A006 A182h, MTU2.TIOR A006 A202h, MTU3.TIORH A006 A004h, MTU4.TIORH A006 A006h, MTU6.TIORH A006 A804h, MTU7.TIORH A006 A806h, MTU8.TIORH A006 A402h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOA[3:0]	I/O Control A*1	See the following tables. MTU0.TIORH: Table 19.27 MTU1.TIOR: Table 19.29 MTU2.TIOR: Table 19.30 MTU3.TIORH: Table 19.31 MTU4.TIORH: Table 19.33 MTU6.TIORH: Table 19.35 MTU7.TIORH: Table 19.37 MTU8.TIORH: Table 19.39	R/W
b7 to b4	IOB[3:0]	I/O Control B*1	See the following tables. MTU0.TIORH: Table 19.13 MTU1.TIOR: Table 19.15 MTU2.TIOR: Table 19.16 MTU3.TIORH: Table 19.17 MTU4.TIORH: Table 19.19 MTU6.TIORH: Table 19.21 MTU7.TIORH: Table 19.23 MTU8.TIORH: Table 19.25	R/W

Note 1. When the value of IOn[3:0] (n = A, B) is changed to the output-prohibited state (0000b or 0100b) during low, high, or toggle output at compare match, this register is in Hi-Z.

- MTU0.TIORL, MTU3.TIORL, MTU4.TIORL, MTU6.TIORL, MTU7.TIORL, MTU8.TIORL

Address(es): MTU0.TIORL A006 A103h, MTU3.TIORL A006 A005h, MTU4.TIORL A006 A007h, MTU6.TIORL A006 A805h, MTU7.TIORL A006 A807h, MTU8.TIORL A006 A403h

	b7	b6	b5	b4	b3	b2	b1	b0
	IOD[3:0]				IOC[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOC[3:0]	I/O Control C*1	See the following tables. MTU0.TIORL: Table 19.28 MTU3.TIORL: Table 19.32 MTU4.TIORL: Table 19.34 MTU6.TIORL: Table 19.36 MTU7.TIORL: Table 19.38 MTU8.TIORL: Table 19.40	R/W
b7 to b4	IOD[3:0]	I/O Control D*1	See the following tables. MTU0.TIORL: Table 19.14 MTU3.TIORL: Table 19.18 MTU4.TIORL: Table 19.20 MTU6.TIORL: Table 19.22 MTU7.TIORL: Table 19.24 MTU8.TIORL: Table 19.26	R/W

Note 1. When the value of IOn[3:0] (n = C, D) is changed to the output-prohibited state (0000b or 0100b) during low, high, or toggle output at compare match, this register is in Hi-Z.

- MTU5.TIORU, MTU5.TIORV, MTU5.TIORW

Address(es): MTU5.TIORU A006 AA86h, MTU5.TIORV A006 AA96h, MTU5.TIORW A006 AAA6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IOC[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	IOC[4:0]	I/O Control C	See the following table. MTU5.TIORU, MTU5.TIORV, MTU5.TIORW: Table 19.41	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.13 TIORH (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU0.TGRB Function**	**MTIOC0B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)

x: Don't care

Table 19.14 TIORL (MTU0)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	**IOD2**	**IOD1**	**IOD0**	**MTU0.TGRD Function**	**MTIOC0D Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)

x: Don't care

Note 1. When the MTU0.TMDR1.BFB is set to 1 and MTU0.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.15 TIOR (MTU1)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	IOB2	IOB1	IOB0	MTU1.TGRB Function	MTIOC1B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	0	0		Input capture at occurrence of compare match or input capture in the MTU0.TGRC register
1	1	1	x		Input capture on generation of compare match with MTU8.TGRC

x: Don't care

Table 19.16 TIOR (MTU2)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	IOB2	IOB1	IOB0	MTU2.TGRB Function	MTIOC2B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.17 TIORH (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU3.TGRB Function**	**MTIOC3B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.18 TIORL (MTU3)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	**IOD2**	**IOD1**	**IOD0**	**MTU3.TGRD Function**	**MTIOC3D Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU3.TMDR1 is set to 1 and MTU3.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.19 TIORH (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU4.TGRB Function**	**MTIOC4B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.20 TIORL (MTU4)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	**IOD2**	**IOD1**	**IOD0**	**MTU4.TGRD Function**	**MTIOC4D Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU4.TMDR1 is set to 1 and MTU4.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.21 TIORH (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU6.TGRB Function**	**MTIOC6B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.22 TIORL (MTU6)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	**IOD2**	**IOD1**	**IOD0**	**MTU6.TGRD Function**	**MTIOC6D Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU6.TMDR1 is set to 1 and MTU6.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.23 TIORH (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	IOB2	IOB1	IOB0	MTU7.TGRB Function	MTIOC7B Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.24 TIORL (MTU7)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	IOD2	IOD1	IOD0	MTU7.TGRD Function	MTIOC7D Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFB bit in MTU7.TMDR1 is set to 1 and MTU7.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.25 TIORH (MTU8)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOB3	**IOB2**	**IOB1**	**IOB0**	**MTU8.TGRB Function**	**MTIOC8B Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)

x: Don't care

Table 19.26 TIORL (MTU8)

Bit 7	Bit 6	Bit 5	Bit 4	Description	
IOD3	**IOD2**	**IOD1**	**IOD0**	**MTU8.TGRD Function**	**MTIOC8D Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU8.TMDR1.BFB bit is set to 1 and the MTU8.TGRD register is used as a buffer register, this setting is not effective and the input capture or output compare operation does not proceed.

Table 19.27 TIORH (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU0.TGRA Function**	**MTIOC0A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	0	0		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)
1	1	1	x		Input capture on generation of compare match with MTU8.TGRC

x: Don't care

Table 19.28 TIORL (MTU0)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	**IOC2**	**IOC1**	**IOC0**	**MTU0.TGRC Function**	**MTIOC0C Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register*1	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Capture input source is the clock source for counting in MTU1. Input capture on counting up or down by MTU1.TCNT (LWA = 0) or MTU1.TCNTLW (LWA = 1)

x: Don't care

Note 1. When the BFA bit in MTU0.TMDR1 is set to 1 and MTU0.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.29 TIOR (MTU1)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU1.TGRA Function**	**MTIOC1A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	0	1	x		Input capture at both edges.
1	1	x	x		Input capture at generation of MTU0.TGRA compare match/input capture.

x: Don't care

Table 19.30 TIOR (MTU2)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU2.TGRA Function**	**MTIOC2A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.31 TIORH (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU3.TGRA Function**	**MTIOC3A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.32 TIORL (MTU3)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	IOC2	IOC1	IOC0	MTU3.TGRC Function	MTIOC3C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU3.TMDR1 is set to 1 and MTU3.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.33 TIORH (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	IOA2	IOA1	IOA0	MTU4.TGRA Function	MTIOC4A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match
0	0	1	0		Initial output is low. High output at compare match
0	0	1	1		Initial output is low. Toggle output at compare match
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match
0	1	1	0		Initial output is high. High output at compare match
0	1	1	1		Initial output is high. Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
1	x	0	1		Input capture at falling edge
1	x	1	x		Input capture at both edges

x: Don't care

Table 19.34 TIORL (MTU4)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	**IOC2**	**IOC1**	**IOC0**	**MTU4.TGRC Function**	**MTIOC4C Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match
0	0	1	0		Initial output is low. High output at compare match
0	0	1	1		Initial output is low. Toggle output at compare match
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match
0	1	1	0		Initial output is high. High output at compare match
0	1	1	1		Initial output is high. Toggle output at compare match
1	x	0	0	Input capture register*1	Input capture at rising edge
1	x	0	1		Input capture at falling edge
1	x	1	x		Input capture at both edges

x: Don't care

Note 1. When the BFA bit in MTU4.TMDR1 is set to 1 and MTU4.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.35 TIORH (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU6.TGRA Function**	**MTIOC6A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.36 TIORL (MTU6)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	**IOC2**	**IOC1**	**IOC0**	**MTU6.TGRC Function**	**MTIOC6C Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU6.TMDR1 is set to 1 and MTU6.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.37 TIORH (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	**IOA2**	**IOA1**	**IOA0**	**MTU7.TGRA Function**	**MTIOC7A Pin Function**
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.38 TIORL (MTU7)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	IOC2	IOC1	IOC0	MTU7.TGRC Function	MTIOC7C Pin Function
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the BFA bit in MTU7.TMDR1 is set to 1 and MTU7.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 19.39 TIORH (MTU8)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOA3	IOA2	IOA1	IOA0	MTU8.TGRA Function	MTIOC8A Pin Function
0	0	0	0	Output compare register	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	0	0	0	Input capture register	Input capture at rising edge.
1	0	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Table 19.40 TIORL (MTU8)

Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC3	**IOC2**	**IOC1**	**IOC0**	**MTU8.TGRC Function**	**MTIOC8C Pin Function**
0	0	0	0	Output compare register*1	Output prohibited
0	0	0	1		Initial output is low. Low output at compare match.
0	0	1	0		Initial output is low. High output at compare match.
0	0	1	1		Initial output is low. Toggle output at compare match.
0	1	0	0		Output prohibited
0	1	0	1		Initial output is high. Low output at compare match.
0	1	1	0		Initial output is high. High output at compare match.
0	1	1	1		Initial output is high. Toggle output at compare match.
1	x	0	0	Input capture register*1	Input capture at rising edge.
1	x	0	1		Input capture at falling edge.
1	x	1	x		Input capture at both edges.

x: Don't care

Note 1. When the MTU8.TMDR1.BFA bit is set to 1 and the MTU8.TGRC register is used as a buffer register, this setting is not effective and the input capture or output compare operation does not proceed.

Table 19.41 TIORU, TIORV, and TIORW (MTU5)

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	
IOC4	IOC3	IOC2	IOC1	IOC0	MTU5.TGRU, MTU5.TGRV, MTU5.TGRW Function	MTIC5U, MTIC5V, MTIC5W Pin Function
0	0	0	0	0	Output compare register	No function
0	0	0	0	1		Setting prohibited
0	0	0	1	x		Setting prohibited
0	0	1	x	x		Setting prohibited
0	1	x	x	x		Setting prohibited
1	0	0	0	0	Input capture register	Setting prohibited
1	0	0	0	1		Input capture at rising edge.
1	0	0	1	0		Input capture at falling edge.
1	0	0	1	1		Input capture at both edges.
1	0	1	x	x		Input capture on generation of compare match with MTU8.TGRC
1	1	0	0	0		Setting prohibited
1	1	0	0	1		Measurement of low pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	0	1	0		Measurement of low pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	0	1	1		Measurement of low pulse width of external input signal. Capture at crest and trough of complementary PWM mode.
1	1	1	0	0		Setting prohibited
1	1	1	0	1		Measurement of high pulse width of external input signal. Capture at trough in complementary PWM mode.
1	1	1	1	0		Measurement of high pulse width of external input signal. Capture at crest of complementary PWM mode.
1	1	1	1	1		Measurement of high pulse width of external input signal. Capture at crest and trough of complementary PWM mode.

x: Don't care

19.2.7 Timer Compare Match Clear Register (TCNTCMPCLR)

TCNTCMPCLR specifies requests to clear MTU5.TCNTU, MTU5.TCNTV, and MTU5.TCNTW. The MTU has one TCNTCMPCLR (on MTU5).

Address(es): MTU5.TCNTCMPCLR A006 AAB6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CMPCLR5U	CMPCLR5V	CMPCLR5W
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPCLR5W	TCNT Compare Clear 5W	0: Disables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture 1: Enables MTU5.TCNTW to be cleared to 0000h at MTU5.TCNTW and MTU5.TGRW compare match or input capture	R/W
b1	CMPCLR5V	TCNT Compare Clear 5V	0: Disables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture 1: Enables MTU5.TCNTV to be cleared to 0000h at MTU5.TCNTV and MTU5.TGRV compare match or input capture	R/W
b2	CMPCLR5U	TCNT Compare Clear 5U	0: Disables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture 1: Enables MTU5.TCNTU to be cleared to 0000h at MTU5.TCNTU and MTU5.TGRU compare match or input capture	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCLR5n Bits (TCNT Compare Clear 5n) (n = U, V, W)

These bits are used to enable or disable requests to clear MTU5.TCNTn on compare match or input capture for MTU5.TCNTn and MTU5.TGRn.

19.2.8 Timer Interrupt Enable Register (TIER)

The TIER register enables or disables interrupt requests from each channel. The MTU has a total of ten TIER registers, two for MTU0 and one each for MTU1 to MTU8.

- TIER (MTU1, MTU2)

Address(es): MTU1.TIER A006 A184h, MTU2.TIER A006 A204h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- TIER (MTU0, MTU3, MTU6)

Address(es): MTU0.TIER A006 A104h, MTU3.TIER A006 A008h, MTU6.TIER A006 A808h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- TIER (MTU4, MTU7)

Address(es): MTU4.TIER A006 A009h, MTU7.TIER A006 A809h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

- TIER (MTU8)

Address(es): MTU8.TIER A006 A404hh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEA	TGR Interrupt Enable A	0: Interrupt requests (TGIA) disabled 1: Interrupt requests (TGIA) enabled	R/W
b1	TGIEB	TGR Interrupt Enable B	0: Interrupt requests (TGIB) disabled 1: Interrupt requests (TGIB) enabled	R/W
b2	TGIEC	TGR Interrupt Enable C	0: Interrupt requests (TGIC) disabled 1: Interrupt requests (TGIC) enabled	R/W
b3	TGIED	TGR Interrupt Enable D	0: Interrupt requests (TGID) disabled 1: Interrupt requests (TGID) enabled	R/W
b4	TCIEV	Overflow Interrupt Enable	0: Interrupt requests (TCIV) disabled 1: Interrupt requests (TCIV) enabled	R/W
b5	TCIEU	Underflow Interrupt Enable	0: Interrupt requests (TCIU) disabled 1: Interrupt requests (TCIU) enabled	R/W
b6	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by MTUn.TCNT underflow (trough) disabled 1: A/D converter start request generation by MTUn.TCNT underflow (trough) enabled	R/W
b7	TTGE	A/D Converter Start Request Enable	0: A/D converter start request generation disabled 1: A/D converter start request generation enabled	R/W

n = 4 or 7

TGIEA and TGIEB Bits (TGR Interrupt Enable A and B)

Each bit enables or disables the interrupt request (TGIn) (n = A or B).

TGIEC and TGIED Bits (TGR Interrupt Enable C and D)

Each bit enables or disables the interrupt request (TGIn) (n = C or D).
In MTU1 and MTU2, these bits are reserved. They are always read as 0. The write value should be 0.

TCIEV Bit (Overflow Interrupt Enable)

This bit enables or disables the interrupt request (TCIV).

TCIEU Bit (Underflow Interrupt Enable)

This bit enables or disables the interrupt request (TCIU).
In MTU0, MTU3, MTU4, MTU5, MTU6, MTU7, and MTU8, this bit is reserved. It is always read as 0. The write value should be 0.

TTGE2 Bit (A/D Converter Start Request Enable 2)

This bit enables or disables generation of A/D converter start requests by MTUn.TCNT underflow (trough) in complementary PWM mode (n = 4 or 7).
In MTU0 to MTU3, MTU6, and MTU8, this bit is reserved. It is always read as 0. The write value should be 0.

TTGE Bit (A/D Converter Start Request Enable)

This bit enables or disables generation of A/D converter start requests by TGRA input capture/compare match.
MTU8 is a reserved bit. It is always read as 0. The write value should be 0.

- TIER2 (MTU0)

Address(es): MTU0.TIER2 A006 A124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE2	—	—	—	—	—	TGIEF	TGIEE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEE	TGR Interrupt Enable E	0: Interrupt requests (TGIE) disabled 1: Interrupt requests (TGIE) enabled	R/W
b1	TGIEF	TGR Interrupt Enable F	0: Interrupt requests (TGIF) disabled 1: Interrupt requests (TGIF) enabled	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TTGE2	A/D Converter Start Request Enable 2	0: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE disabled 1: A/D converter start request generation by compare match between MTU0.TCNT and MTU0.TGRE enabled	R/W

TGIEE and TGIEF Bits (TGR Interrupt Enable E and F)

Each bit enables or disables interrupt requests by compare match between MTU0.TCNT and MTU0.TGRn (n = E or F).

TTGE2 Bit (A/D Converter Start Request Enable 2)

Each bit enables or disables interrupt requests by compare match between MTU0.TCNT and MTU0.TGRE.

- TIER (MTU5)

Address(es): MTU5.TIER A006 AAB2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TGIE5U	TGIE5V	TGIE5W
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TGIE5W	TGR Interrupt Enable 5W	0: Interrupt requests TGIW5 disabled 1: Interrupt requests TGIW5 enabled	R/W
b1	TGIE5V	TGR Interrupt Enable 5V	0: Interrupt requests TGIV5 disabled 1: Interrupt requests TGIV5 enabled	R/W
b2	TGIE5U	TGR Interrupt Enable 5U	0: Interrupt requests TGIU5 disabled 1: Interrupt requests TGIU5 enabled	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TGIE5n Bits (TGR Interrupt Enable 5n)

Each bit enables or disables the interrupt request (TGIn5) (n = U, V, or W).

19.2.9 Timer Status Register (TSR)

The TSR register indicates the state of each channel. The MTU has a total of six TSR registers, one each for MTU1 to MTU7 (excluding MTU5).

- TSR (MTU1, MTU2)

Address(es): MTU1.TSR A006 A185h, MTU2.TSR A006 A205h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

- TSR (MTU3, MTU4, MTU6, MTU7)

Address(es): MTU3.TSR A006 A02Ch, MTU4.TSR A006 A02Dh, MTU6.TSR A006 A82Ch, MTU7.TSR A006 A82Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGFA	Input Capture/Output Compare Flag A	0: TGRA input capture or compare match has not occurred. 1: TGRA input capture or compare match has occurred.	R/W*1
b1	TGFB	Input Capture/Output Compare Flag B	0: TGRB input capture or compare match has not occurred. 1: TGRB input capture or compare match has occurred.	R/W*1
b2	TGFC	Input Capture/Output Compare Flag C	0: TGRC input capture or compare match has not occurred. 1: TGRC input capture or compare match has occurred.	R/W*1
b3	TGFD	Input Capture/Output Compare Flag D	0: TGRD input capture or compare match has not occurred. 1: TGRD input capture or compare match has occurred.	R/W*1
b4	TCFV	Overflow Flag	0: TCNT overflow has not occurred. 1: TCNT overflow has occurred.	R/W*1
b5	TCFU	Underflow Flag	0: A TCNT underflow has not occurred in MTU1 and MTU2 when they are in phase-counting mode. 1: A TCNT underflow has occurred in MTU1 and MTU2 when they are in phase-counting mode.	R/W*1
b6	—	Reserved	This bit is read as 1.	R
b7	TCFD	Count Direction Flag	0: TCNT counts down 1: TCNT counts up	R

Note 1. Only writing 0 to this bit after reading 1 from this bit in order to clear the flag is possible. After 1 is read from this bit, if the next flag is set before 0 is written to this bit, writing 0 to this bit does not clear the flag. In this case, read 1 again from this bit, and then write 0 to this bit.

TGFA Flag (Input Capture/Output Compare Flag A)

This status flag indicates generation of TGRA input capture or compare match. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TGFA = 1, the TGFA flag is read, and then 0 is written to the TGFA flag.

[Setting conditions]

- TCNT = TGRA when the TGRA register functions as an output compare register.
- The value of TCNT is transferred to TGRA due to the input capture signal when the TGRA register functions as an input capture register.

TGFB Flag (Input Capture/Output Compare Flag B)

This status flag indicates generation of TGRB input capture or compare match. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TGFB = 1, the TGFB flag is read, and then 0 is written to the TGFB flag.

[Setting conditions]

- TCNT = TGRB when the TGRB register functions as an output compare register.
- The value of TCNT is transferred to the TGRB register due to the input capture signal when the TGRB register functions as an input capture register.

TGFC Flag (Input Capture/Output Compare Flag C)

This status flag indicates generation of TGRC input capture or compare match for MTU3, MTU4, MTU6, or MTU7. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TGFC = 1, the TGFC flag is read, and then 0 is written to the TGFC flag.

[Setting conditions]

- TCNT = TGRC when the TGRC register functions as an output compare register.
- The value of TCNT is transferred to the TGRC register due to the input capture signal when the TGRC register functions as an input capture register.

This bit is reserved for MTU1 and MTU2. This bit is read as 0. The write value should be 0.

TGFD Flag (Input Capture/Output Compare Flag D)

This status flag indicates generation of TGRD input capture or compare match for MTU3, MTU4, MTU6, or MTU7. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TGFD = 1, the TGFD flag is read, and then 0 is written to the TGFD flag.

[Setting conditions]

- TCNT = TGRD when the TGRD register functions as the output compare register.
- The value of TCNT is transferred to the TGRD register due to the input capture signal when the TGRD register functions as an input capture register.

This bit is reserved for MTU1 and MTU2. This bit is read as 0. The write value should be 0.

TCFV Flag (Overflow Flag)

This status flag indicates generation of TCNT overflow. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TCFV = 1, the TCFV flag is read, and then 0 is written to the TCFV flag.

[Setting condition]

- The value of TCNT overflows (changed from FFFFh to 0000h).

For MTU4 or MUTU7, the TCFV flag is also set to 1 when the value of TCNT of MTU4 or MTU7 underflows (changed from 0001h to 0000h) in complementary PWM mode.

TCFU Flag (Underflow Flag)

This status flag indicates generation of TCNT underflow when MTU1 and MTU2 are in phase counting mode. Only writing 0 to this bit in order to clear the flag is possible.

[Clearing condition]

- When TCFU = 1, TCFU is read, and then 0 is written to TCFU.

[Setting condition]

- The value of TCNT underflows (changed from 0000h to FFFFh).

This bit is reserved for MTU3, MTU4, MTU6, and MTU7. This bit is read as 0. The write value should be 0.

TCFD Flag (Count Direction Flag)

Status flag that indicates the direction in which TCNT is counting in MTU1 to MTU4, MTU6, and MTU7.

19.2.10 Timer Buffer Operation Transfer Mode Register (TBTM)

TBTM specifies the timing for transferring data from the buffer register to the timer general register in PWM mode. The MTU has a total of five TBTM registers, one each for MTU0, MTU3, MTU4, MTU6, and MTU7.

- MTU0.TBTM

Address(es): MTU0.TBTM A006 A126h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TTSE	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

- MTU3.TBTM, MTU4.TBTM, MTU6.TBTM, MTU7.TBTM

Address(es): MTU3.TBTM A006 A038h, MTU4.TBTM A006 A039h, MTU6.TBTM A006 A838h, MTU7.TBTM A006 A839h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TTSB	TTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TTSA	Timing Select A	0: When compare match A occurs in each channel, data is transferred from TGRC to TGRA 1: When TCNT is cleared in each channel, data is transferred from TGRC to TGRA	R/W
b1	TTSB	Timing Select B	0: When compare match B occurs in each channel, data is transferred from TGRD to TGRB 1: When TCNT is cleared in each channel, data is transferred from TGRD to TGRB	R/W
b2	TTSE	Timing Select E	0: When compare match E occurs in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE 1: When MTU0.TCNT is cleared in MTU0, data is transferred from MTU0.TGRF to MTU0.TGRE	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TTSA Bit (Timing Select A)

This bit specifies the timing for transferring data from TGRC to TGRA in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSA bit in the channel to 1.

TTSB Bit (Timing Select B)

This bit specifies the timing for transferring data from TGRD to TGRB in each channel when they are used together for buffer operation. When a channel is not set to PWM mode, do not set the TTSB bit in the channel to 1.

TTSE Bit (Timing Select E)

This bit specifies the timing for transferring data from MTU0.TGRF to MTU0.TGRE when they are used together for buffer operation.
In MTU3, MTU4, MTU6, and MTU7, this bit is reserved. It is read as 0 and the write value should be 0. When a channel is not set to PWM mode, do not set the TTSE bit in the channel to 1.

19.2.11 Timer Input Capture Control Register (TICCR)

TICCR specifies input capture conditions when MTU1.TCNT and MTU2.TCNT are cascaded. The MTU has one TICCR for MTU1.

Address(es): MTU1.TICCR A006 A190h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	I2BE	I2AE	I1BE	I1AE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	I1AE	Input Capture Enable	0: Does not include the MTIOC1A pin in the MTU2.TGRA input capture conditions 1: Includes the MTIOC1A pin in the MTU2.TGRA input capture conditions	R/W
b1	I1BE	Input Capture Enable	0: Does not include the TMTIOC1B pin in the MTU2.TGRB input capture conditions 1: Includes the MTIOC1B pin in the MTU2.TGRB input capture conditions	R/W
b2	I2AE	Input Capture Enable	0: Does not include the MTIOC2A pin in the MTU1.TGRA input capture conditions 1: Includes the MTIOC2A pin in the MTU1.TGRA input capture conditions	R/W
b3	I2BE	Input Capture Enable	0: Does not include the MTIOC2B pin in the MTU1.TGRB input capture conditions 1: Includes the MTIOC2B pin in the MTU1.TGRB input capture conditions	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

I1AE Bit (Input Capture Enable)

This bit selects or deselects the signal on the MTIOC1A pin as a condition for input capture to MTU2.TGRA.

I1BE Bit (Input Capture Enable)

This bit selects or deselects the signal on the MTIOC1B pin as a condition for input capture to MTU2.TGRB.

I2AE Bit (Input Capture Enable)

This bit selects or deselects the signal on the MTIOC2A pin as a condition for input capture to MTU1.TGRA.

I2BE Bit (Input Capture Enable)

This bit selects or deselects the signal on the MTIOC2B pin as a condition for input capture to MTU1.TGRB.

19.2.12 Timer Synchronous Clear Register (TSYCR)

The TSYCR register specifies synchronous clear conditions for MTU6.TCNT and MTU7.TCNT. The MTU has one TSYCR for MTU6.

Address(es): MTU6.TSYCR A006 A850h

	b7	b6	b5	b4	b3	b2	b1	b0
	CE0A	CE0B	CE0C	CE0D	CE1A	CE1B	CE2A	CE2B
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CE2B	Clear Enable 2B	0: Disables counter clearing by the MTU2.TGIB2 interrupt generation timing. 1: Enables counter clearing by the MTU2.TGIB2 interrupt generation timing.	R/W
b1	CE2A	Clear Enable 2A	0: Disables counter clearing by the MTU2.TGIA2 interrupt generation timing*1. 1: Enables counter clearing by the MTU2.TGIA2 interrupt generation timing*1.	R/W
b2	CE1B	Clear Enable 1B	0: Disables counter clearing by the MTU1.TGIB1 interrupt generation timing*1. 1: Enables counter clearing by the MTU1.TGIB1 interrupt generation timing*1.	R/W
b3	CE1A	Clear Enable 1A	0: Disables counter clearing by the MTU1.TGIA1 interrupt generation timing*1. 1: Enables counter clearing by the MTU1.TGIA1 interrupt generation timing*1.	R/W
b4	CE0D	Clear Enable 0D	0: Disables counter clearing by the MTU0.TGID0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGID0 interrupt generation timing*1.	R/W
b5	CE0C	Clear Enable 0C	0: Disables counter clearing by the MTU0.TGIC0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIC0 interrupt generation timing*1.	R/W
b6	CE0B	Clear Enable 0B	0: Disables counter clearing by the MTU0.TGIB0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIB0 interrupt generation timing*1.	R/W
b7	CE0A	Clear Enable 0A	0: Disables counter clearing by the MTU0.TGIA0 interrupt generation timing*1. 1: Enables counter clearing by the MTU0.TGIA0 interrupt generation timing*1.	R/W

Note 1. This does not depend on the TIERn.TGIEm bit setting. (n = 0, 1, or 2; m = A, B, C, or D)

CEnm Bits (Clear Enable nm) (n = 0, 1, 2; m = A, B, C, D)

These bits enable or disable counter clearing by the MTUn.TGImn interrupt generation timing.

19.2.13 Timer Counter (TCNT)

TCNT of each MTU0 to MTU7 is a 16-bit readable/writable register. TCNT of MTU8 is a 32-bit readable/writable register. The MTU has a total of 11 TCNT counters, one each for MTU0 to MTU4, MTU6, MTU7, and MTU8 and three (MTU5.TCNTU, TCNTUV, and TCNTUW) for MTU5.
The TCNT counters in MTU0 to MTU4, MTU6, and MTU7 are initialized to 0000h by a reset, and, and the MTU8.TCNT counter is initialized to 0000 0000h by a reset.
In MTU0 to MTU4, MTU6, and MTU7, the TCNT counters must not be accessed in 8-bit units; they should always be accessed in 16-bit units. The MTU8.TCNT counter must not be accessed in 8- or 16-bit units; it should always be accessed in 32-bit units.

- MTU0.TCNT to MTU7.TCNT

Address(es): MTU0.TCNT A006 A106h, MTU1.TCNT A006 A186h, MTU2.TCNT A006 A206h, MTU3.TCNT A006 A010h, MTU4.TCNT A006 A012h, MTU6.TCNT A006 A810h, MTU7.TCNT A006 A812h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNT must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

- MTU8.TCNT

Address(es): MTU8.TCNT A006 A408h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNT must not be accessed in 8- or 16-bit units; they should always be accessed in 32-bit units.

19.2.14 Timer Longword Counter (TCNTLW)

The TCNTLW counter is a 32-bit readable/writable counter. Only one counter of this type is provided, and is formed by combining MTU1.TCNT and MTU2.TCNT. Such operation is only effective when the setting of TMDR3.LWA is 1.
The TCNTLW counter is initialized to 0000 0000h by a reset. See section 19.2.5, Timer Mode Register 3 (TMDR3) for details. This register can only be used in 32-bit phase counting mode.

Address(es): MTU1.TCNTLW A006 A1A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

19.2.15 Timer General Register (TGR)

The TGR registers in MTU0 to MTU7 are 16-bit readable/writable registers; the MTU8.TGR register is a 32-bit readable/writable register. The MTU has a total of 39 TGR registers, six for MTU0, two each for MTU1 and MTU2, five each for MTU3 and MTU6, six each for MTU4 and MTU7, three for MTU5 and four for MTU8.
The TGRA, TGRB, TGRC, and TGRD registers function as either output compare or input capture registers. The TGRC and TGRD registers for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8 can also be designated for operation as buffer registers. TGR buffer register combinations are TGRA and TGRC, and TGRB and TGRD.
MTU0.TGRE and MTU0.TGRF function as compare registers. When the MTU0.TCNT count matches the MTU0.TGRE value, an A/D converter start request can be issued. The TGRF register can also be designated for operation as a buffer register. TGR buffer register combination is TGRE and TGRF. MTU5.TGRU, MTU5.TGRV, and MTU5.TGRW function as compare match, input capture, or external pulse width measurement registers.

Address(es): MTU0.TGRA A006 A108h, MTU0.TGRB A006 A10Ah, MTU0.TGRC A006 A10Ch, MTU0.TGRD A006 A10Eh, MTU0.TGRE A006 A120h, MTU0.TGRF A006 A122h,
MTU1.TGRA A006 A188h, MTU1.TGRB A006 A18Ah,
MTU2.TGRA A006 A208h, MTU2.TGRB A006 A20Ah,
MTU3.TGRA A006 A018h, MTU3.TGRB A006 A01Ah, MTU3.TGRC A006 A024h, MTU3.TGRD A006 A026h, MTU3.TGRE A006 A072h
MTU4.TGRA A006 A01Ch, MTU4.TGRB A006 A01Eh, MTU4.TGRC A006 A028h, MTU4.TGRD A006 A02Ah, MTU4.TGRE A006 A074h, MTU4.TGRF A006 A076h,
MTU5.TGRU A006 AA82h, MTU5.TGRV A006 AA92h, MTU5.TGRW A006 AAA2h,
MTU6.TGRA A006 A818h, MTU6.TGRB A006 A81Ah, MTU6.TGRC A006 A824h, MTU6.TGRD A006 A826h, MTU6.TGRE A006 A872h,
MTU7.TGRA A006 A81Ch, MTU7.TGRB A006 A81Eh, MTU7.TGRC A006 A828h, MTU7.TGRD A006 A82Ah, MTU7.TGRE A006 A874h,
MTU7.TGRF A006 A876h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Access to TGR in 8-bit units is prohibited. Always access this register in 16-bit units. The initial value of TGR is FFFFh.

Address(es): MTU8.TGRA A006 A40Ch, MTU8.TGRB A006 A410h, MTU8.TGRC A006 A414h, MTU8.TGRD A006 A418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: For cycle setting, see section 19.6.3, Note on Cycle Setting.

19.2.16 Timer Longword General Register n (TGRnLW) (n = A, B)

The TGRnLW register is a 32-bit readable/writable register. Two general registers of this type are provided, and are formed by combining MTU1.TGRn and MTU2.TGRn. Such operation is only effective when the setting of TMDR3.LWA is 1.

See section 19.2.5, Timer Mode Register 3 (TMDR3) for details.

The TGRnLW register functions as an output compare or input capture register when TMDR3.LWA is 1.

This register can only be used in 32-bit phase counting mode.

Address(es): MTU1.TGRALW A006 A1A4h, MTU1.TGRBLW A006 A1A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

19.2.17 Timer Start Register (TSTR)

TSTRA starts or stops TCNT operation in MTU0 to MTU4 and MTU8.
TSTRB starts or stops TCNT operation in MTU6 and MTU7.
TSTR starts or stops TCNT operation in MTU5.
Before setting the operating mode in TMDR1 or setting the TCNT count clock in TCR, be sure to stop the TCNT counter.

- TSTRA (MTU0 to MTU4 and MTU8)

Address(es): MTU.TSTRA A006 A080h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST4	CST3	—	—	CST8	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	Counter Start 0	0: MTU0.TCNT count operation is stopped 1: MTU0.TCNT performs count operation	R/W
b1	CST1	Counter Start 1	0: MTU1.TCNT count operation is stopped 1: MTU1.TCNT performs count operation	R/W
b2	CST2	Counter Start 2	0: MTU2.TCNT count operation is stopped 1: MTU2.TCNT performs count operation	R/W
b3	CST8	Counter Start 8	0: MTU8.TCNT count operation is stopped. 1: MTU8.TCNT performs count operation.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CST3	Counter Start 3	0: MTU3.TCNT count operation is stopped 1: MTU3.TCNT performs count operation	R/W
b7	CST4	Counter Start 4	0: MTU4.TCNT count operation is stopped 1: MTU4.TCNT performs count operation	R/W

Note: When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRA is also set to 1 automatically.

CSTn Bits (Counter Start n) (n = 0, 1, 2, 3, 4, 8)

Each bit starts or stops TCNT in the corresponding channel.
If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- TSTRB (MTU6, MTU7)

Address(es): MTU.TSTRB A006 A880h

	b7	b6	b5	b4	b3	b2	b1	b0
	CST7	CST6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CST6	Counter Start 6	0: MTU6.TCNT count operation is stopped 1: MTU6.TCNT performs count operation	R/W
b7	CST7	Counter Start 7	0: MTU7.TCNT count operation is stopped 1: MTU7.TCNT performs count operation	R/W

Note: When 1 is written to a bit in TCSYSTR, the corresponding bit in TSTRB is also set to 1 automatically.

CSTn Bits (Counter Start n) (n = 6 or 7)

Each bit starts or stops TCNT in the corresponding channel.
If 0 is written to the CSTn bit during operation with the MTIOC pin designated for output, the counter stops but the output compare signal level from the MTIOC pin is retained. If TIOR is written to while the CSTn bit is 0, the pin output level will be changed to the specified initial output value.

- TSTR (MTU5)

Address(es): MTU5.TSTR A006 AAB4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSTU5	CSTV5	CSTW5
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CSTW5	Counter Start W5	0: MTU5.TCNTW count operation is stopped 1: MTU5.TCNTW performs count operation	R/W
b1	CSTV5	Counter Start V5	0: MTU5.TCNTV count operation is stopped 1: MTU5.TCNTV performs count operation	R/W
b2	CSTU5	Counter Start U5	0: MTU5.TCNTU count operation is stopped 1: MTU5.TCNTU performs count operation	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CSTn5 Bits (Counter Start n5) (n = U, V, W)

These bits cause the respective TCNT registers to stop or run.

19.2.18 Timer Synchronous Register (TSYR)

TSYRA selects independent operation or synchronous operation of TCNT in MTU0 to MTU4.
TSYRB selects independent operation or synchronous operation of TCNT in MTU6 and MTU7.
A channel performs synchronous operation when the corresponding bit in TSYR is set to 1.

- TSYRA (MTU0, MTU1, MTU2, MTU3, MTU4)

Address(es): MTU.TSYRA A006 A081h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC4	SYNC3	—	—	—	SYNC2	SYNC1	SYNC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SYNC0	Timer Synchronous Operation 0	0: MTU0.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU0.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b1	SYNC1	Timer Synchronous Operation 1	0: MTU1.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU1.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b2	SYNC2	Timer Synchronous Operation 2	0: MTU2.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU2.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SYNC3	Timer Synchronous Operation 3	0: MTU3.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU3.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b7	SYNC4	Timer Synchronous Operation 4	0: MTU4.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU4.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W

SYNCn Bits (Timer Synchronous Operation n) (n = 0 to 4)

Each bit selects whether operation is independent of or synchronized with other channels.
When synchronous operation is selected, the TCNT synchronous presetting of multiple channels and synchronous clearing by counter clearing on another channel are possible.
To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits TCR.CCLR[2:0].

- TSYRB (MTU6, MTU7)

Address(es): MTU.TSYRB A006 A881h

	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC7	SYNC6	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SYNC6	Timer Synchronous Operation 6	0: MTU6.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU6.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W
b7	SYNC7	Timer Synchronous Operation 7	0: MTU7.TCNT operates independently (TCNT presetting/ clearing is not related to other channels). 1: MTU7.TCNT performs synchronous operation. (TCNT synchronous presetting/synchronous clearing is enabled.)	R/W

SYNCn Bits (Timer Synchronous Operation n) (n = 6 or 7)

Each bit selects whether operation is independent of or synchronized with other channels.

When synchronous operation is selected, the TCNT synchronous presetting of multiple channels and synchronous clearing by counter clearing on another channel are possible.

To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits TCR.CCLR[2:0].

19.2.19 Timer Counter Synchronous Start Register (TCSYSTR)

TCSYSTR specifies synchronous start of the counters.

Address(es): MTU.TCSYSTR A006 A082h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCH0	SCH1	SCH2	SCH3	SCH4	—	SCH6	SCH7
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SCH7	Synchronous Start 7	0: Does not specify synchronous start for MTU7.TCNT 1: Specifies synchronous start for MTU7.TCNT	R/W *1
b1	SCH6	Synchronous Start 6	0: Does not specify synchronous start for MTU6.TCNT 1: Specifies synchronous start for MTU6.TCNT	R/W *1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	SCH4	Synchronous Start 4	0: Does not specify synchronous start for MTU4.TCNT 1: Specifies synchronous start for MTU4.TCNT	R/W *1
b4	SCH3	Synchronous Start 3	0: Does not specify synchronous start for MTU3.TCNT 1: Specifies synchronous start for MTU3.TCNT	R/W *1
b5	SCH2	Synchronous Start 2	0: Does not specify synchronous start for MTU2.TCNT 1: Specifies synchronous start for MTU2.TCNT	R/W *1
b6	SCH1	Synchronous Start 1	0: Does not specify synchronous start for MTU1.TCNT 1: Specifies synchronous start for MTU1.TCNT	R/W *1
b7	SCH0	Synchronous Start 0	0: Does not specify synchronous start for MTU0.TCNT 1: Specifies synchronous start for MTU0.TCNT	R/W *1

Note 1. Only 1 can be written to this bit, and doing so sets the register.
TCSYSTR is automatically cleared to 0 after 1 is written to.

SCH7 Bit (Synchronous Start 7)

This bit controls synchronous start of MTU7.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST7 bit while SCH7 = 1

SCH6 Bit (Synchronous Start 6)

This bit controls synchronous start of MTU6.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST6 bit while SCH6 = 1

SCH4 Bit (Synchronous Start 4)

This bit controls synchronous start of MTU4.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST4 bit while SCH4 = 1

SCH3 Bit (Synchronous Start 3)

This bit controls synchronous start of MTU3.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST3 bit while SCH3 = 1

SCH2 Bit (Synchronous Start 2)

This bit controls synchronous start of MTU2.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST2 bit while SCH2 = 1

SCH1 Bit (Synchronous Start 1)

This bit controls synchronous start of MTU1.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST1 bit while SCH1 = 1

SCH0 Bit (Synchronous Start 0)

This bit controls synchronous start of MTU0.TCNT.

[Clearing condition]

- When 1 is set to the TSTRA.CST0 bit while SCH0 = 1

19.2.20 Timer Read/Write Enable Registers (TRWERA, TRWERB)

TRWERA enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU3 and MTU4.
TRWERB enables or disables access to the registers and counters that have write-protection capability against accidental modification in MTU6 and MTU7.

Address(es): MTU.TRWERA A006 A084h, MTU.TRWERB A006 A884h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RWE
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RWE	Read/Write Enable	0: Read/write access to the registers is disabled 1: Read/write access to the registers is enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RWE Bit (Read/Write Enable)

This bit enables or disables access to the registers that have write-protection capability against accidental modification.
[Clearing condition]

- When 0 is written to the RWE bit after reading RWE = 1

- Registers and counters having write-protection capability against accidental modification (TRWERA)
  24 registers: MTUn.TCR, MTUn.TCR2, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, TOERA, TOCR1A, TOCR2A, TGCRA, TCDRA, TDDRA, and MTUn.TCNT (n = 3 or 4)
- Registers and counters having write-protection capability against accidental modification (TRWERB)
  23 registers: MTUn.TCR, MTUn.TCR2, MTUn.TMDR1, MTUn.TIORH, MTUn.TIORL, MTUn.TIER, MTUn.TGRA, MTUn.TGRB, TOERB, TOCR1B, TOCR2B, TCDRB, TDDRB, and MTUn.TCNT (n = 6 or 7)

19.2.21 Timer Output Master Enable Register (TOER)

TOERA enables or disables output settings for output pins MTIOC4D, MTIOC4C, MTIOC3D, MTIOC4B, MTIOC4A, and MTIOC3B.
TOERB enables or disables output settings for output pins MTIOC7D, MTIOC7C, MTIOC6D, MTIOC7B, MTIOC7A, and MTIOC6B.
These pins do not output correctly if the TOER bits have not been set. In MTU3, MTU4, MTU6, and MTU7, set TOER prior to setting TIOR.
Set MTU.TOERA after clearing the CST3 and CST4 bits in MTU.TSTRA to 0.
Set MTU.TOERB after clearing the CST0 and CST1 bits in MTU.TSTRB to 0 (see Figure 19.44 and Figure 19.48).

- TOERA

Address(es): MTU.TOERA A006 A00Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE3B	Master Enable MTIOC3B	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b1	OE4A	Master Enable MTIOC4A	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b2	OE4B	Master Enable MTIOC4B	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b3	OE3D	Master Enable MTIOC3D	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b4	OE4C	Master Enable MTIOC4C	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b5	OE4D	Master Enable MTIOC4D	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. The non-active level depends on the setting of the timer output control register 1 or 2 (TOCR 1/2). See section 19.2.22, Timer Output Control Registers 1 (TOCR1A, TOCR1B) and section 19.2.23, Timer Output Control Registers 2 (TOCR2A, TOCR2B) for details. When MTU output is in a mode other than complementary PWM mode or reset-synchronized PWM mode, set the relevant bit to 1. If the setting is 0, the non-active level will be output due to this setting of the timer output control register.

OEnm Bits (Master Enable MTIOCnm) (n = 3 or 4, m = A to D)

These bits enable or disable the output setting for MTIOCnm output pin of MTU.

- TOERB

Address(es): MTU.TOERB A006 A80Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OE7D	OE7C	OE6D	OE7B	OE7A	OE6B
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OE6B	Master Enable MTIOC6B	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b1	OE7A	Master Enable MTIOC7A	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b2	OE7B	Master Enable MTIOC7B	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b3	OE6D	Master Enable MTIOC6D	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b4	OE7C	Master Enable MTIOC7C	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b5	OE7D	Master Enable MTIOC7D	0: MTU output is disabled (non-active level)*1 1: MTU output is enabled	R/W
b7, b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. The non-active level depends on the setting of the timer output control register 1 or 2 (TOCR 1/2). See section 19.2.22, Timer Output Control Registers 1 (TOCR1A, TOCR1B) and section 19.2.23, Timer Output Control Registers 2 (TOCR2A, TOCR2B) for details. When MTU output is in a mode other than complementary PWM mode or reset-synchronized PWM mode, set the relevant bit to 1. If the setting is 0, the non-active level will be output due to this setting of the timer output control register.

OEnm Bits (Master Enable MTIOCnm) (n = 6 or 7, m = A to D)

These bits enable or disable the output setting for MTIOCnm output pin of MTU.

19.2.22 Timer Output Control Registers 1 (TOCR1A, TOCR1B)

TOCR1A is used to configure the MTU3 and MTU4 for use in complementary PWM mode and reset synchronous PWM mode.
TOCR1B is used to configure the MTU6 and MTU7 for use in complementary PWM mode and reset synchronous PWM mode.

Address(es): MTU.TOCR1A A006 A00Eh, MTU.TOCR1B A006 A80Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP
Value after reset:	0	0	0	0	0*4	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSP	Output Level Select P*1, *3	See Table 19.42.	R/W
b1	OLSN	Output Level Select N*1, *3	See Table 19.43.	R/W
b2	TOCS	TOC Select	0: TOCR1j setting is selected (j = A or B) 1: TOCR2j setting is selected	R/W
b3	TOCL	TOC Register Write Protection*2, *4	0: Write access to the TOCS, OLSN, and OLSP bits is enabled 1: Write access to the TOCS, OLSN, and OLSP bits is disabled	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PSYE	PWM Synchronous Output Enable	0: Toggle output is disabled 1: Toggle output is enabled	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Clearing the TOCR1j.TOCS bit to 0 makes this bit setting valid.
Note 2. Setting the TOCR1j.TOCL bit to 1 prevents accidental modification when the CPU goes out of control.
Note 3. If dead-time is not generated, the negative-phase output is always the exact inverse of the positive-phase output. In this case, only the OLSP bit is valid.
Note 4. This bit can be set to 1 only once after a reset. After 1 is written, 0 cannot be written to the bit.

OLSP Bit (Output Level Select P)

This bit selects the positive-phase output level in reset-synchronized PWM mode and complementary PWM mode.

OLSN Bit (Output Level Select N)

This bit selects the negative-phase output level in reset-synchronized PWM mode and complementary PWM mode.

TOCS Bit (TOC Select)

This bit selects either the TOCR1j or TOCR2j (j = A or B) setting to be used for the output level in complementary PWM mode and reset-synchronized PWM mode.

TOCL Bit (TOC Register Write Protection)

This bit enables or disables write access to the TOCS, OLSN, and OLSP bits in TOCR1j (j = A or B).

PSYE Bit (PWM Synchronous Output Enable)

This bit enables or disables toggle output synchronized with the PWM cycle.

Table 19.42 Output Level Select Function

Bit 0			Function	
			Compare Match Output	
OLSP	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

Table 19.43 Output Level Select Function

Bit 1			Function	
			Compare Match Output	
OLSN	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Figure 19.3 shows an example of output in complementary PWM mode (one phase) when OLSN = 1 and OLSP = 1.

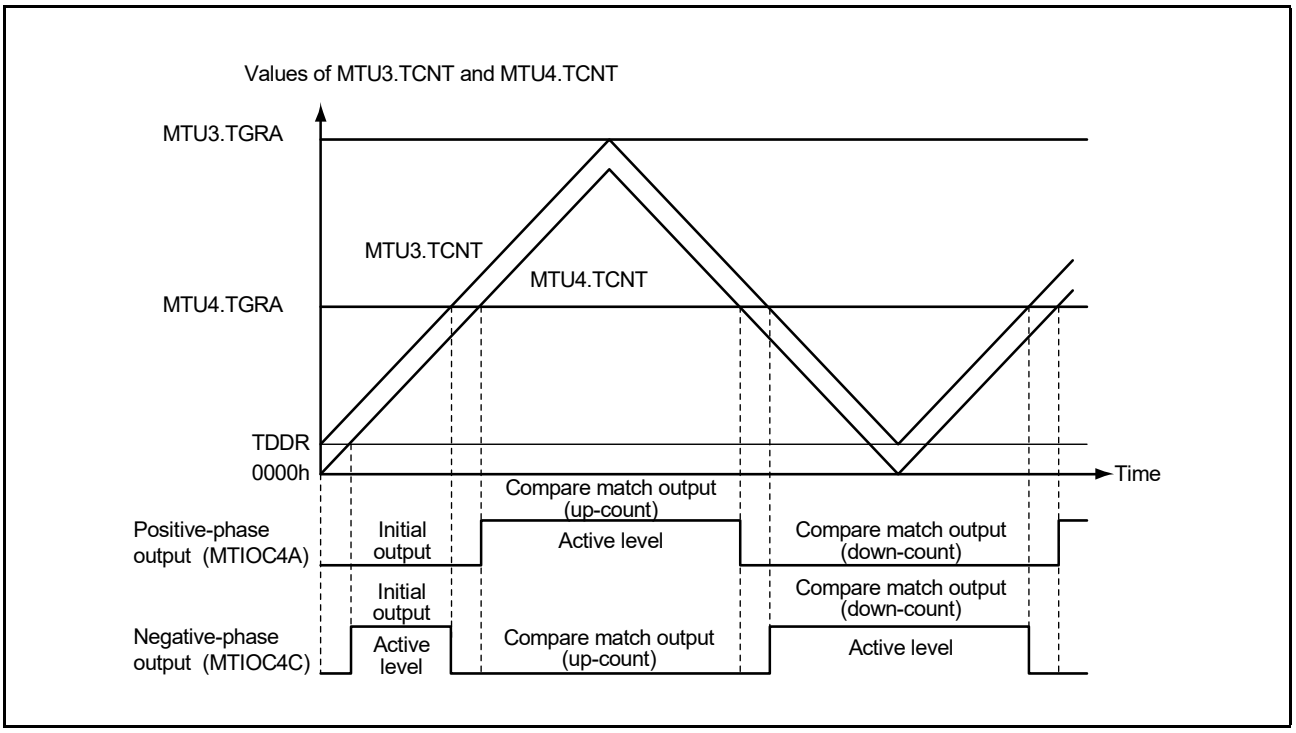


Figure 19.3 Example of Output in Complementary PWM Mode

19.2.23 Timer Output Control Registers 2 (TOCR2A, TOCR2B)

TOCR2A and TOCR2B control inversion of PWM output level in complementary PWM mode and reset-synchronized PWM mode.

Address(es): MTU.TOCR2A A006 A00Fh, MTU.TOCR2B A006 A80Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P*1, *2	This bit selects the output level on MTIOC3B or MTIOC6B in reset-synchronized PWM mode and complementary PWM mode. See Table 19.44.	R/W
b1	OLS1N	Output Level Select 1N*1, *2	This bit selects the output level on MTIOC3D or MTIOC6D in reset-synchronized PWM mode and complementary PWM mode. See Table 19.45.	R/W
b2	OLS2P	Output Level Select 2P*1, *2	This bit selects the output level on MTIOC4A or MTIOC7Ain reset-synchronized PWM mode and complementary PWM mode. See Table 19.46.	R/W
b3	OLS2N	Output Level Select 2N*1, *2	This bit selects the output level on MTIOC4C or MTIOC7C in reset-synchronized PWM mode and complementary PWM mode. See Table 19.47.	R/W
b4	OLS3P	Output Level Select 3P*1, *2	This bit selects the output level on MTIOC4B or MTIOC7B in reset-synchronized PWM mode and complementary PWM mode. See Table 19.48.	R/W
b5	OLS3N	Output Level Select 3N*1, *2	This bit selects the output level on MTIOC4D or MTIOC7D in reset-synchronized PWM mode and complementary PWM mode. See Table 19.49.	R/W
b7, b6	BF[1:0]	TOLBR Buffer Transfer Timing Select	These bits select the timing for transferring data from TOLBRj to TOCR2j. See Table 19.50 for details.	R/W

j = A or B

Note 1. Setting the TOCR1j.TOCS bit to 1 makes this bit setting valid.

Note 2. If dead-time is not generated, the negative-phase output is always the exact inverse of the positive-phase output. In this case, only the OLSiP bits are valid (i = 1 to 3).

Table 19.44 MTIOCmB Output Level Select Function

Bit 0	Function			
			Compare Match Output	
OLS1P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 3 or 6

Table 19.45 MTIOCmD Output Level Select Function

Bit 1	Function			
			Compare Match Output	
OLS1N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 3 or 6

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 19.46 MTIOCmA Output Level Select Function

Bit 2	Function			
			Compare Match Output	
OLS2P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 4 or 7

Table 19.47 MTIOCmC Output Level Select Function

Bit 3	Function			
			Compare Match Output	
OLS2N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 4 or 7

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 19.48 MTIOCmB Output Level Select Function

Bit 4	Function			
			Compare Match Output	
OLS3P	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	Low level	High level
1	Low level	High level	High level	Low level

m = 4 or 7

Table 19.49 MTIOCmD Output Level Select Function

Bit 5	Function			
			Compare Match Output	
OLS3N	Initial Output	Active Level	Up-Counting	Down-Counting
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

m = 4 or 7

Note: The initial output value of negative-phase waveform changes to an active level after the dead time has passed since counting starts.

Table 19.50 Setting of TOCR2j.BF[1:0] Bits

Bit 7	Bit 6	Description	
BF1	**BF0**	**Complementary PWM Mode**	**Reset-Synchronized PWM Mode**
0	0	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.	Does not transfer data from the buffer register (TOLBRj) to TOCR2j.
0	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest of the MTUn.TCNT count.	Transfers data from the buffer register (TOLBRj) to TOCR2j when MTUm.TCNT or MTUn.TCNT is cleared.
1	0	Transfers data from the buffer register (TOLBRj) to TOCR2j at the trough of the MTUn.TCNT count.	Setting prohibited
1	1	Transfers data from the buffer register (TOLBRj) to TOCR2j at the crest and trough of the MTUn.TCNT count.	Setting prohibited

n = 4 or 7, m = 3 or 6, j = A or B

19.2.24 Timer Output Level Buffer Registers (TOLBRA, TOLBRB)

TOLBRA and TOLBRB are buffer registers for TOCR2A and TOCR2B and specify the PWM output level in complementary PWM mode and reset-synchronized PWM mode.

Address(es): MTU.TOLBRA A006 A036h, MTU.TOLBRB A006 A836h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLS1P	Output Level Select 1P	Specify the buffer value to be transferred to the OLS1P bit in TOCR2j.	R/W
b1	OLS1N	Output Level Select 1N	Specify the buffer value to be transferred to the OLS1N bit in TOCR2j.	R/W
b2	OLS2P	Output Level Select 2P	Specify the buffer value to be transferred to the OLS2P bit in TOCR2j.	R/W
b3	OLS2N	Output Level Select 2N	Specify the buffer value to be transferred to the OLS2N bit in TOCR2j.	R/W
b4	OLS3P	Output Level Select 3P	Specify the buffer value to be transferred to the OLS3P bit in TOCR2j.	R/W
b5	OLS3N	Output Level Select 3N	Specify the buffer value to be transferred to the OLS3N bit in TOCR2j.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

j = A or B

Figure 19.4 shows an example of the PWM output level setting procedure in buffer operation.

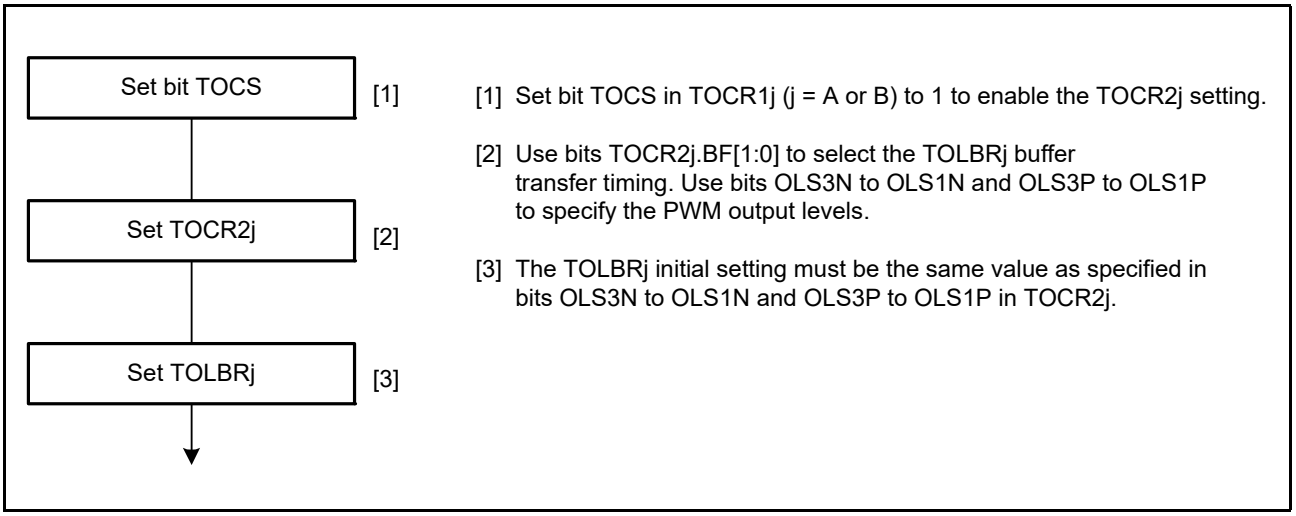


Figure 19.4 Example of PWM Output Level Setting Procedure in Buffer Operation

19.2.25 Timer Gate Control Register A (TGCRA)

TGCRA controls the output waveform necessary for brushless DC motor control in reset-synchronized PWM mode and complementary PWM mode. TGCRA register settings are ineffective for anything other than complementary PWM mode and reset-synchronized PWM mode.

Address(es): MTU.TGCRA A006 A00Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	BDC	N	P	FB	WF	VF	UF
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	UF	Output Phase Switch	These bits turn on or off the positive-phase/negative-phase output. The setting of these bits is valid only when the TGCRA.FB bit s set to 1. In this case, the setting of b0 to b2 is used instead of the external input. See Table 19.51.	R/W
b1	VF			R/W
b2	WF			R/W
b3	FB	External Feedback Signal Enable	0: Output is switched by external input (input sources are TGRA, TGRB, and TGRC input capture signals in MTU0) 1: Output is switched by software (TGCRA's UF, VF, and WF settings)	R/W
b4	P	Positive-Phase Output (P) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b5	N	Negative-Phase Output (N) Control	0: Level output 1: Reset-synchronized PWM or complementary PWM output	R/W
b6	BDC	Brushless DC Motor	0: Ordinary output 1: Functions of this register are made effective	R/W
b7	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

UF, VF, and WF Bits (Output Phase Switch)

These bits are used to switch output of the positive- and negative-phase signals on or off.

FB Bit (External Feedback Signal Enable)

This bit selects whether the positive-/negative-phase output is switched automatically with the TGRA, TGRB, and TGRC input capture signals in MTU0 or by writing 0 or 1 to bits 2 to 0 in TGCRA.

P Bit (Positive-Phase Output (P) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the positive-phase output pins (MTIOC3B, MTIOC4A, and MTIOC4B pins).

N Bit (Negative-Phase Output (N) Control)

This bit selects the level output or the reset-synchronized PWM/complementary PWM output for the negative-phase output pins (MTIOC3D, MTIOC4C, and MTIOC4D pins).

BDC Bit (Brushless DC Motor)

This bit selects whether to make the functions of TGCRA effective or ineffective.

Table 19.51 Output Level Select Function

Bit 2	Bit 1	Bit 0	Function					
			MTIOC3B	MTIOC4A	MTIOC4B	MTIOC3D	MTIOC4C	MTIOC4D
WF	VF	UF	U Phase	V Phase	W Phase	U Phase	V Phase	W Phase
0	0	0	OFF	OFF	OFF	OFF	OFF	OFF
0	0	1	ON	OFF	OFF	OFF	OFF	ON
0	1	0	OFF	ON	OFF	ON	OFF	OFF
0	1	1	OFF	ON	OFF	OFF	OFF	ON
1	0	0	OFF	OFF	ON	OFF	ON	OFF
1	0	1	ON	OFF	OFF	OFF	ON	OFF
1	1	0	OFF	OFF	ON	ON	OFF	OFF
1	1	1	OFF	OFF	OFF	OFF	OFF	OFF

19.2.26 Timer Subcounters (TCNTSA, TCNTSB)

TCNTSA and TCNTSB are 16-bit read-only counters that are used only in complementary PWM mode.
The initial value of TCNTSA and TCNTSB after a reset is 0000h.

Address(es): MTU.TCNTSA A006 A020h, MTU.TCNTSB A006 A820h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: TCNTSA and TCNTSB must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

19.2.27 Timer Cycle Data Registers (TCDRA, TCDRB)

TCDRA and TCDRB are 16-bit readable/writable registers used only in complementary PWM mode. Set half the PWM carrier cycle as the TCDRA and TCDRB values. The TCDRA and TCDRB registers are always compared with the TCNTSA and TCNTSB counters respectively, in complementary PWM mode. When they match, the TCNTSA or TCNTSB counter switches the count direction (from down-count to up-count).
The initial value of TCDRA and TCDRB after a reset is FFFFh.

Address(es): MTU.TCDRA A006 A014h, MTU.TCDRB A006 A814h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TCDRA and TCDRB must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

19.2.28 Timer Cycle Buffer Registers (TCBRA, TCBRB)

TCBRA and TCBRB are 16-bit readable/writable registers, used only in complementary PWM mode, that function as buffer registers for TCDRA and TCDRB. The TCBRA and TCBRB values are transferred to TCDRA and TCDRB with the transfer timing set in TMDR1.
The initial value of TCBRA and TCBRB after a reset is FFFFh.

Address(es): MTU.TCBRA A006 A022h, MTU.TCBRB A006 A822h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TCBRA and TCBRB must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

19.2.29 Timer Dead Time Data Registers (TDDRA, TDDRB)

TDDRA and TDDRB are 16-bit readable/writable registers, used only in complementary PWM mode, that specify the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counter offset value. In complementary PWM mode, when the MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT) counters are cleared and then restarted, the TDDRA (TDDRB) value is loaded into the MTU3.TCNT (MTU6.TCNT) counter and the count operation starts. The initial value of TDDRA and TDDRB after a reset is FFFFh.

Address(es): MTU.TDDRA A006 A016h, MTU.TDDRB A006 A816h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TDDRA and TDDRB must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

19.2.30 Timer Dead Time Enable Registers (TDERA, TDERB)

TDERA and TDERB control dead time generation in complementary PWM mode. The MTU has one TDER each for MTU3 and MTU6. TDERA and TDERB should be modified only while TCNT stops.

Address(es): MTU.TDERA A006 A034h, MTU.TDERB A006 A834h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDER
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TDER	Dead Time Enable	0: No dead time is generated. 1: Dead time is generated.*1	R/(W)
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. TDDRA and TDDRB must be set to 1 or a larger value.

TDER Bit (Dead Time Enable)

This bit specifies whether to generate dead time.

[Clearing condition]

- When 0 is written to TDER after reading TDER = 1

19.2.31 Timer Buffer Transfer Set Registers (TBTERA, TBTERB)

TBTERA and TBTERB enable or disable transfer from the buffer registers used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping 1 operation.

Address(es): MTU.TBTERA A006 A032h, MTU.TBTERB A006 A832h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BTE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BTE[1:0]	Buffer Transfer Disable and Interrupt Skipping Link Setting	These bits enable or disable transfer from the buffer registers*1 used in complementary PWM mode to the temporary registers, and specify whether to link the transfer with interrupt skipping function 1. For details, see Table 19.52.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Applicable buffer registers (TBTERA):
MTU3.TGRC, MTU3.TGRD, MTU4.TGRC, MTU4.TGRD, and TCBRA
Applicable buffer registers (TBTER_B):
MTU6.TGRC, MTU6.TGRD, MTU7.TGRC, MTU7.TGRD, and TCBRB

Table 19.52 Setting of TBTER.BTE[1:0] Bits

Bit 1	Bit 0	
BTE1	BTE0	Description
0	0	Enables transfer from the buffer registers to the temporary registers*1 and does not link the transfer with interrupt skipping function 1.
0	1	Disables transfer from the buffer registers to the temporary registers.
1	0	Links transfer from the buffer registers to the temporary registers with interrupt skipping function 1.*2
1	1	Setting prohibited

Note 1. Data is transferred according to the MD3 to MD0 bit setting in TMDR1. For details, see section 19.3.8, Complementary PWM Mode.

Note 2. When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits are cleared to 0 in the timer interrupt skipping set register (TITCR1A (TITCR1B)) or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), be sure to disable link of buffer transfer with interrupt skipping (clear the BTE1 bit in the timer buffer transfer set register (TBTERA (TBTERB)) to 0). If link with interrupt skipping is enabled while interrupt skipping is disabled, buffer transfer will not be performed.

19.2.32 Timer Waveform Control Registers (TWCRA, TWCRB)

TWCRA and TWCRB control the output waveform when synchronous counter clearing occurs in MTU3.TNCT and MTU4.TNCT (MTU6.TNCT and MTU7.TNCT) in complementary PWM mode and specifies whether to clear the counters at MTU3.TGRA (MTU6.TGRA) compare match.
The CCE bit and WRE bit in TWCRA and TWCRB should be modified only while TCNT stops.

Address(es): MTU.TWCRA A006 A060h, MTU.TWCRB A006 A860h

	b7	b6	b5	b4	b3	b2	b1	b0
	CCE	—	—	—	—	—	SCC	WRE
Value after reset:	0*2	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WRE	Waveform Retain Enable	0: Initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output 1: Initial output is inhibited	R/(W)*3
b1	SCC*1, *3	Synchronous Clearing Control	(Only valid in register TWCRB) 0: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is enabled. 1: Clearing of MTU6.TCNT and MTU7.TCNT in response to synchronous clearing for MTU0, MTU1, MTU2–MTU6, MTU7 is disabled.	R/(W)
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CCE*2	Compare Match Clear Enable	0: Counters are not cleared at MTU3.TGRA (MTU6.TGRA) compare match 1: Counters are cleared at MTU3.TGRA (MTU6.TGRA) compare match	R/(W)

Note 1. This bit is only valid in register TWCRB and is a reserved bit in register TWCRA.
Note 2. Do not set to 1 when complementary PWM mode 1 is not selected.
Note 3. Do not set to 1 when complementary PWM mode is not selected.

WRE Bit (Waveform Retain Enable)

This bit selects the waveform output when synchronous counter clearing occurs in complementary PWM mode.
The initial output is inhibited with this function only when synchronous clearing occurs within the Tb interval at the trough in complementary PWM mode. When synchronous clearing occurs outside this interval, the initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are output regardless of the WRE bit setting. The initial values specified in TOCR1A and TOCR2A (TOCR1B and TOCR2B) are also output when synchronous clearing occurs in the Tb interval at the trough immediately after MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start operation.
For the Tb interval at the trough in complementary PWM mode, see Figure 19.50.
[Setting condition]

- When 1 is written to WRE after reading WRE = 0

SCC Bit (Synchronous Clearing Control) (Only valid in register TWCRB)

The setting of this bit selects whether MTU6.TCNT and MTU7.TCNT are or are not cleared when counter-synchronous clearing is generated for MTU0, MTU1, MTU2 to MTU6, and MTU7 in complementary PWM mode.
Make the complementary PWM mode settings for MTU6 and MTU7 when this function is in use. When writing a new value to the SCC bit while the counter is operating, do so in such a way that the values of the CCE and WRE bits are not changed.
Synchronous clearing from the MTU module only becomes disabled due to the setting of the SCC bit when synchronous clearing is generated outside the Tb interval in the trough. If synchronous clearing is generated within the Tb interval in the trough including immediately after the value at which MTU6.TCNT and MTU7.TCNT start, MTU6.TCNT and MTU7.TCNT are cleared.
Regarding the Tb interval in the trough in complementary PWM mode, see Figure 19.50.
[Setting condition]

- Writing of 1 to the SCC bit after reading it as 0

The corresponding bit in register TWCRA is reserved and is always read as 0. When writing to TWCRA, always write 0 to this bit.

CCE Bit (Compare Match Clear Enable)

This bit specifies whether to clear counters at MTU3.TGRA (MTU6.TGRA) compare match in complementary PWM mode.
[Setting condition]

- When 1 is written to CCE after reading CCE = 0

19.2.33 Noise Filter Control Register n (NFCRn) (n = 0 to 4, 6, 7, 8, C)

NFCRn controls noise filtering for the input pins of MTUn (n = 0 to 4, 6, 7, or 8). NFCRC controls noise filtering for the external clock input pins of the MTU.

- NFCRn (n = 0 to 4, 6, 7, 8)

Address(es): MTU0.NFCR0 A006 A090h, MTU1.NFCR1 A006 A091h, MTU2.NFCR2 A006 A092h, MTU3.NFCR3 A006 A093h, MTU4.NFCR4 A006 A094h, MTU6.NFCR6 A006 A893h, MTU7.NFCR7 A006 A894h, MTU8.NFCR8 A006 A098h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		NFDEN	NFCEN	NFBEN	NFAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFAEN	Noise Filter A Enable Bit	0: The noise filter for the MTIOCnA pin is disabled. 1: The noise filter for the MTIOCnA pin is enabled.	R/W
b1	NFBEN	Noise Filter B Enable Bit	0: The noise filter for the MTIOCnB pin is disabled. 1: The noise filter for the MTIOCnB pin is enabled.	R/W
b2	NFCEN	Noise Filter C Enable Bit	0: The noise filter for the MTIOCnC pin is disabled. 1: The noise filter for the MTIOCnC pin is enabled.	R/W*1
b3	NFDEN	Noise Filter D Enable Bit	0: The noise filter for the MTIOCnD pin is disabled. 1: The noise filter for the MTIOCnD pin is enabled.	R/W*1
b5, b4	NFCS[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKC/1 0 1: PCLKC/8 1 0: PCLKC/32 1 1: Clock source for counting	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits are reserved in the NFCR1 and NFCR2 registers. These bits are read as 0 and writing to them is not effective.

NFAEN Bit (Noise Filter A Enable)

This bit enables or disables the noise filter for input from the MTIOCnA pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFBEN Bit (Noise Filter B Enable)

This bit enables or disables the noise filter for input from the MTIOCnB pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFCEN Bit (Noise Filter C Enable)

This bit enables or disables the noise filter for input from the MTIOCnC pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFDEN Bit (Noise Filter D Enable)

This bit enables or disables the noise filter for input from the MTIOCnD pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register or set the TMDR.MD[3:0] bits to a value other than that for normal mode (0000b) before doing so.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. When setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval before setting the input-capture function. When the NFCS[1:0] bits are set to 11b, i.e. selecting the external clock as the source to drive counting, wait for two cycles of the external clock before setting the input capture function.

- NFCRC

Address(es): MTU0.NFCRC A006 A099h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCSC[1:0]		NFDEN	NFCEN	NFBEN	NFAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFAEN	Noise Filter A Enable Bit	0: The noise filter for the MTCLKA pin is disabled. 1: The noise filter for the MTCLKA pin is enabled.	R/W
b1	NFBEN	Noise Filter B Enable Bit	0: The noise filter for the MTCLKB pin is disabled. 1: The noise filter for the MTCLKB pin is enabled.	R/W
b2	NFCEN	Noise Filter C Enable Bit	0: The noise filter for the MTCLKC pin is disabled. 1: The noise filter for the MTCLKC pin is enabled.	R/W
b3	NFDEN	Noise Filter D Enable Bit	0: The noise filter for the MTCLKD pin is disabled. 1: The noise filter for the MTCLKD pin is enabled.	R/W
b5, b4	NFCSC[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKC/1 0 1: PCLKC/2 1 0: PCLKC/8 1 1: PCLKC/32	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFAEN Bit (Noise Filter A Enable)

This bit enables or disables the noise filter for input from the MTCLKA pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFBEN Bit (Noise Filter B Enable)

This bit enables or disables the noise filter for input from the MTCLKB pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFCEN Bit (Noise Filter C Enable)

This bit enables or disables the noise filter for input from the MTCLKC pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFDEN Bit (Noise Filter D Enable)

This bit enables or disables the noise filter for input from the MTCLKD pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, do so after stopping the internal counter.

NFCSC[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. After setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval to set the input capture function.

19.2.34 Noise Filter Control Register 5 (NFCR5)

NFCR5 controls noise filtering for the input pins of MTU5.

Address(es): MTU5.NFCR5 A006 A895h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		—	NFWEN	NFVEN	NFUEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFUEN	Noise Filter U Enable Bit	0: The noise filter for the MTIOC5U pin is disabled. 1: The noise filter for the MTIOC5U pin is enabled.	R/W
b1	NFVEN	Noise Filter V Enable Bit	0: The noise filter for the MTIOC5V pin is disabled. 1: The noise filter for the MTIOC5V pin is enabled.	R/W
b2	NFWEN	Noise Filter W Enable Bit	0: The noise filter for the MTIOC5W pin is disabled. 1: The noise filter for the MTIOC5W pin is enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	NFCS[1:0]	Noise Filter Clock Select	b5 b4 0 0: PCLKC/1 0 1: PCLKC/8 1 0: PCLKC/32 1 1: Clock source for counting	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NFUEN Bit (Noise Filter U Enable)

This bit enables or disables the noise filter for input from the MTIOC5U pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFVEN Bit (Noise Filter V Enable)

This bit enables or disables the noise filter for input from the MTIOC5V pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFWEN Bit (Noise Filter W Enable)

This bit enables or disables the noise filter for input from the MTIOC5W pin. Since unexpected edges may be internally generated when the value of this bit is changed, select the output compare function for the relevant pin in the timer I/O control register.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits set the sampling interval for the noise filters. When setting the NFCS[1:0] bits, wait for two cycles of the selected sampling interval before setting the input-capture function.

19.2.35 Timer A/D Converter Start Request Control Register (TADCR)

TADCR enables or disables A/D converter start requests and specifies whether to link A/D converter start requests with interrupt skipping function. The MTU has one TADCR each for MTU4 and MTU7.

- TADCR (MTU4)

Address(es): MTU.TADCR A006 A040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT4AE	DT4AE	UT4BE	DT4BE	ITA3AE	ITA4VE	ITB3AE	ITB4VE
Value after reset:	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB4VE*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TCI4V interrupt skipping 1 are linked	R/W
b1	ITB3AE*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4BN and TGI3A interrupt skipping 1 are linked	R/W
b2	ITA4VE*4	TCIV4 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TCI4V interrupt skipping 1 are linked	R/W
b3	ITA3AE*4	TGIA3 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG4AN and TGI3A interrupt skipping 1 are linked	R/W
b4	DT4BE*4	Down-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT down-count operation	R/W
b5	UT4BE	Up-Count TRG4BN Enable	0: A/D converter start requests (TRG4BN) disabled during MTU4.TCNT up-count operation 1: A/D converter start requests (TRG4BN) enabled during MTU4.TCNT up-count operation	R/W
b6	DT4AE*4	Down-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT down-count operation 1: A/D converter start requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b7	UT4AE	Up-Count TRG4AN Enable	0: A/D converter start requests (TRG4AN) disabled during MTU4.TCNT up-count operation 1: A/D converter up requests (TRG4AN) enabled during MTU4.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU4.TADCOBRA/B Transfer Timing Select	See Table 19.53 for details. These bits specify the transfer timing from MTU4.TADCOBRA and MTU4.TADCOBRB to MTU4.TADCORA and MTU4.TADCORB.	R/W

Note 1. MTU4.TADCR must not be accessed in 8-bit units; it should always be accessed in 16-bit units.
Note 2. When interrupt skipping is disabled (the T3AEN and T4VEN bits in TITCR1A are cleared to 0 or the T3ACOR and T4VCOR bits in TITCR1A are cleared to 0), do not link A/D converter start requests with interrupt skipping function 1 (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in MUT3_4.TADCR to 0).
Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 4. Do not set to 1 when complementary PWM mode is not selected.

Table 19.53 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU4)

Bit 15	Bit 14	
BF1	**BF0**	**Description**
0	0	Does not transfer data from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB).
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the MTU4.TCNT count.*1
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the MTU4.TCNT count.*2
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the MTU4.TCNT count.*2

Note 1. Data is transferred from the cycle set buffer register (MTU4.TADCOBRA, MTU4.TADCOBRB) to the cycle set register (MTU4.TADCORA, MTU4.TADCORB) when the crest of the MTU4.TCNT count is reached or the MTU4.TGRD is written to in complementary PWM mode, when a compare match occurs between MTU3.TCNT and MTU3.TGRA in reset-synchronized PWM mode, or when a compare match occurs between MTU4.TCNT and MTU4.TGRA in PWM mode 1 or normal operation mode.

Note 2. These settings are prohibited when complementary PWM mode is not selected.

- TADCR (MTU7)

Address(es): MTU7, TADCR A006 A840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BF[1:0]		—	—	—	—	—	—	UT7AE	DT7AE	UT7BE	DT7BE	ITA6AE	ITA7VE	ITB6AE	ITB7VE
Value after reset:	0	0	0	0	0	0	0	0	0	0*4	0	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit Name	Description	R/W
b0	ITB7VE*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TCI7V interrupt skipping 1 are linked	R/W
b1	ITB6AE*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7BN and TGI6A interrupt skipping 1 are linked	R/W
b2	ITA7VE*4	TCIV7 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TCI7V interrupt skipping 1 are linked	R/W
b3	ITA6AE*4	TGIA6 Interrupt Skipping Link Enable	0: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are not linked 1: A/D converter start request signal TRG7AN and TGI6A interrupt skipping 1 are linked	R/W
b4	DT7BE*4	Down-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT down-count operation	R/W
b5	UT7BE	Up-Count TRG7BN Enable	0: A/D converter start requests (TRG7BN) disabled during MTU7.TCNT up-count operation 1: A/D converter start requests (TRG7BN) enabled during MTU7.TCNT up-count operation	R/W
b6	DT7AE*4	Down-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT down-count operation 1: A/D converter start requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b7	UT7AE	Up-Count TRG7AN Enable	0: A/D converter start requests (TRG7AN) disabled during MTU7.TCNT up-count operation 1: A/D converter up requests (TRG7AN) enabled during MTU7.TCNT down-count operation	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	BF[1:0]	MTU7.TADCOBRA/B Transfer Timing Select	See Table 19.54 for details. These bits specify the transfer timing from MTU7.TADCOBRA and MTU7.TADCOBRB to MTU7.TADCORA and MTU7.TADCORB.	R/W

Note 1. MTU7.TADCR must not be accessed in 8-bit units; it should always be accessed in 16-bit units.
Note 2. When interrupt skipping is disabled (the T6AEN and T7VEN bits in TITCR1B are cleared to 0 or the T6ACOR and T7VCOR bits in TITCR1B are cleared to 0), do not link A/D converter start requests with interrupt skipping function 1 (clear the ITA6AE, ITA7VE, ITB6AE, and ITB7VE bits in MUT3_7.TADCR to 0).
Note 3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
Note 4. Do not set to 1 when complementary PWM mode is not selected.

Table 19.54 Setting of Transfer Timing by TADCR.BF[1:0] Bits (MTU7)

Bit 15	Bit 14	
BF1	**BF0**	**Description**
0	0	Does not transfer data from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB).
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the MTU7.TCNT count.*1
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the MTU7.TCNT count.*2
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the MTU7.TCNT count.*2

Note 1. Data is transferred from the cycle set buffer register (MTU7.TADCOBRA, MTU7.TADCOBRB) to the cycle set register (MTU7.TADCORA, MTU7.TADCORB) when the crest of the MTU7.TCNT count is reached or the MTU7.TGRD is written to in complementary PWM mode, when a compare match occurs between MTU6.TCNT and MTU6.TGRA in reset-synchronized PWM mode, or when a compare match occurs between MTU7.TCNT and MTU7.TGRA in PWM mode 1 or normal operation mode.

Note 2. These settings are prohibited when complementary PWM mode is not selected.

19.2.36 Timer A/D Converter Start Request Cycle Set Registers (TADCORA, TADCORB)

TADCORA and TADCORB are 16-bit readable/writable registers that issue a corresponding A/D converter start request when the MTUn.TCNT (n = 4 or 7) count reaches the value in TADCORA or TADCORB.
MTUn.TADCORA and TADCORB are initialized to FFFFh by a reset.

Address(es): MTU4.TADCORA A006 A044h, MTU4.TADCORB A006 A046h, MTU7.TADCORA A006 A844h, MTU7.TADCORB A006 A846h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: MTUn.TADCORA and MTUn.TADCORB (n = 4 or 7) must not be accessed in 8-bit units; they should always be accessed in 16-bit units.

Note 1. When the A/D converter start request delaying function linked with skipping function 1 (for details, see section 19.3.9 (4), A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1) is used, the value of this register should be 0002h to TCDRA setting - 2 in MTU4 and 0002h to TCDRB setting - 2 in MTU7.

Note 2. When interrupt skipping function 2 is used and the difference between the MTUn.TADCORA value and the MTUn.TADCORB value is small, the skipping count may not be counted correctly and the A/D converter start request may not be generated with the expected timing in some cases. The TADCORA and TADCORB values should satisfy the following conditions.

(1) When skipping function 2 is specified with the skipping count set to 0

- The difference between the MTUn.TADCORA and MTUn.TADCORB values should be equal to or greater than 4.
- The MTUn.TADCORA compare interval should be equal to or greater than 4 PCLKC cycles (the MTUn.TADCORA update value should be the previous value + 4 or greater, or previous value - 4 or smaller).
- The MTUn.TADCORB compare interval should be equal to or greater than 4 PCLKC cycles (the MTUn.TADCORB update value should be the previous value + 4 or greater, or previous value - 4 or smaller).

(2) When skipping function 2 is specified with the skipping count set to 1 or greater

- The difference between the MTUn.TADCORA and MTUn.TADCORB values should be equal to or greater than 2.
- The MTUn.TADCORB compare interval should be equal to or greater than 2 PCLKC cycles (the MTUn.TADCOR update value should be the previous value + 2 or greater, or previous value - 2 or smaller)

19.2.37 Timer A/D Converter Start Request Cycle Set Buffer Registers (TADCOBRA, TADCOBRB)

TADCOBRA and TADCOBRB are 16-bit readable/writable registers whose values are transferred to TADCORA and TADCORB, respectively, when the crest or trough of the MTUn.TCNT count is reached.
TADCOBRA and TADCOBRB are initialized to FFFFh by a reset.

Address(es): MTU4.TADCORA A006 A048h, MTU4.TADCORB A006 A04Ah, MTU7.TADCORA A006 A848h, MTU7.TADCORB A006 A84Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: TADCOBRA and TADCOBRB must not be accessed in 8-bit units; it should always be accessed in 16-bit units.

19.2.38 Timer Interrupt Skipping Mode Registers (TITMRA, TITMRB)

TITMRA and TITMRB are used to select either of two skipping functions for the TITMRA and TITMRB registers.

Address(es): MTU.TITMRA A006 A03Ah, MTU.TITMRB A006 A83Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TITM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TITM	Interrupt Skipping Function Select	Selects one of the two types of interrupt skipping functions shown in Table 19.55.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.55 Interrupt Skipping Function Selected through TITM Bit

Bit 0	
TITM	**Description**
0	Selects interrupt skipping function 1*1
1	Selects interrupt skipping function 2*2

Note 1. TITCR1A or TITCR1B enables interrupt skipping function 1.
Note 2. TITCR2A or TITCR2B enables interrupt skipping function 2.

19.2.39 Timer Interrupt Skipping Set Registers 1 (TITCR1A, TITCR1B)

TITCR1A and TITCR1B enable or disable interrupt skipping and specify the interrupt skipping count. This setting is valid only while TITMRA or TITMRB is set to 0; when TITMRA or TITMRB is set to 1, the setting in the corresponding TITCR1 register is cleared.

- TITCR1A

Address(es): MTU.TITMRA A006 A030h

	b7	b6	b5	b4	b3	b2	b1	b0
	T3AEN		T3ACOR[2:0]			T4VEN	T4VCOR[2:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCOR[2:0]	TCIV4 Interrupt Skipping Count Setting	These bits specify the TCIV4 interrupt skipping count within the range from 0 to 7.*1 For details, see Table 19.56.	R/W
b3	T4VEN	T4VEN	0: TCIV4 interrupt skipping disabled 1: TCIV4 interrupt skipping enabled	R/W
b6 to b4	T3ACOR[2:0]	TGIA3 Interrupt Skipping Count Setting	These bits specify the TGIA3 interrupt skipping count within the range from 0 to 7.*1 For details, see Table 19.57.	R/W
b7	T3AEN	T3AEN	0: TGIA3 interrupt skipping disabled 1: TGIA3 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0 to clear the skipping counter (TITCNT1A).

- TITCR1B

Address(es): MTU.TITCR1B A006 A830h

	b7	b6	b5	b4	b3	b2	b1	b0
	T6AEN		T6ACOR[2:0]			T7VEN	T7VCOR[2:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCOR[2:0]	TCIV7 Interrupt Skipping Count Setting	These bits specify the TCIV7 interrupt skipping count within the range from 0 to 7.*1 For details, see Table 19.58.	R/W
b3	T7VEN	T7VEN	0: TCIV7 interrupt skipping disabled 1: TCIV7 interrupt skipping enabled	R/W
b6 to b4	T6ACOR[2:0]	TGIA6 Interrupt Skipping Count Setting	These bits specify the TGIA6 interrupt skipping count within the range from 0 to 7.*1 For details, see Table 19.59.	R/W
b7	T6AEN	T6AEN	0: TGIA6 interrupt skipping disabled 1: TGIA6 interrupt skipping enabled	R/W

Note 1. When 0 is specified for the interrupt skipping count, no interrupt skipping will be performed.
Before changing the interrupt skipping count, be sure to clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0 to clear the skipping counter (TITCNT1B).

Table 19.56 Setting of Interrupt Skipping Count by T4VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	
T4VCOR2	T4VCOR1	T4VCOR0	Description
0	0	0	Does not skip TCIV4 interrupts.
0	0	1	Sets the TCIV4 interrupt skipping count to 1.
0	1	0	Sets the TCIV4 interrupt skipping count to 2.
0	1	1	Sets the TCIV4 interrupt skipping count to 3.
1	0	0	Sets the TCIV4 interrupt skipping count to 4.
1	0	1	Sets the TCIV4 interrupt skipping count to 5.
1	1	0	Sets the TCIV4 interrupt skipping count to 6.
1	1	1	Sets the TCIV4 interrupt skipping count to 7.

Table 19.57 Setting of Interrupt Skipping Count by T3ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T3ACOR2	T3ACOR1	T3ACOR0	Description
0	0	0	Does not skip TGIA3 interrupts.
0	0	1	Sets the TGIA3 interrupt skipping count to 1.
0	1	0	Sets the TGIA3 interrupt skipping count to 2.
0	1	1	Sets the TGIA3 interrupt skipping count to 3.
1	0	0	Sets the TGIA3 interrupt skipping count to 4.
1	0	1	Sets the TGIA3 interrupt skipping count to 5.
1	1	0	Sets the TGIA3 interrupt skipping count to 6.
1	1	1	Sets the TGIA3 interrupt skipping count to 7.

Table 19.58 Setting of Interrupt Skipping Count by T7VCOR[2:0] Bits

Bit 2	Bit 1	Bit 0	
T7VCOR2	T7VCOR1	T7VCOR0	Description
0	0	0	Does not skip TCIV7 interrupts.
0	0	1	Sets the TCIV7 interrupt skipping count to 1.
0	1	0	Sets the TCIV7 interrupt skipping count to 2.
0	1	1	Sets the TCIV7 interrupt skipping count to 3.
1	0	0	Sets the TCIV7 interrupt skipping count to 4.
1	0	1	Sets the TCIV7 interrupt skipping count to 5.
1	1	0	Sets the TCIV7 interrupt skipping count to 6.
1	1	1	Sets the TCIV7 interrupt skipping count to 7.

Table 19.59 Setting of Interrupt Skipping Count by T6ACOR[2:0] Bits

Bit 6	Bit 5	Bit 4	
T6ACOR2	T6ACOR1	T6ACOR0	Description
0	0	0	Does not skip TGIA6 interrupts.
0	0	1	Sets the TGIA6 interrupt skipping count to 1.
0	1	0	Sets the TGIA6 interrupt skipping count to 2.
0	1	1	Sets the TGIA6 interrupt skipping count to 3.
1	0	0	Sets the TGIA6 interrupt skipping count to 4.
1	0	1	Sets the TGIA6 interrupt skipping count to 5.
1	1	0	Sets the TGIA6 interrupt skipping count to 6.
1	1	1	Sets the TGIA6 interrupt skipping count to 7.

19.2.40 Timer Interrupt Skipping Counters 1 (TITCNT1A, TITCNT1B)

TITCNT1A and TITCNT1B are 8-bit readable/writable counters. TITCNTA and TITCNTB retain their values even after stopping the count operation of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

- TITCNT1A

Address(es): MTU.TITCNT1A A006 A031h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	T3ACNT[2:0]			—	T4VCNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T4VCNT[2:0]	TCIV4 Interrupt Counter	While the T4VEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TCIV4 interrupt occurs.	R
b3	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b6 to b4	T3ACNT[2:0]	TGIA3 Interrupt Counter	While the T3AEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TGIA3 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1A, clear the TITCR1A.T3AEN and TITCR1A.T4VEN bits to 0.

T4VCNT[2:0] Bits (TCIV4 Interrupt Counter)

While the T4VEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TCIV4 interrupt occurs.
[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T4VEN bit in TITCR1A is cleared to 0
- When the T4VCOR[2:0] bits in TITCR1A are cleared to 000b
- When the T4VCNT[2:0] bits in TITCNT1A match the T4VCOR[2:0] bits in TITCR1A

T3ACNT[2:0] Bits (TGIA3 Interrupt Counter)

While the T3AEN bit in TITCR1A is set to 1, the count in these bits is incremented every time a TGIA3 interrupt occurs.
[Clearing conditions]

- When the TITM bit in TITMRA is 1
- When the T3AEN bit in TITCR1A is cleared to 0
- When the T3ACOR[2:0] bits in TITCR1A are cleared to 000b
- When the T3ACNT[2:0] bits in TITCNT1A match the T3ACOR[2:0] bits in TITCR1A

- TITCNT1B

Address(es): MTU.TITCNT1B A006 A831h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	T6ACNT[2:0]			—	T7VCNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	T7VCNT[2:0]	TCIV7 Interrupt Counter	While the T7VEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TCIV7 interrupt occurs.	R
b3	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b6 to b4	T6ACNT[2:0]	TGIA6 Interrupt Counter	While the T6AEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TGIA6 interrupt occurs.	R
b7	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. To clear the TITCNT1B, clear the TITCR1B.T6AEN and TITCR1B.T7VEN bits to 0.

T7VCNT[2:0] Bits (TCIV7 Interrupt Counter)

While the T7VEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TCIV7 interrupt occurs.
[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T7VEN bit in TITCR1B is cleared to 0
- When the T7VCOR[2:0] bits in TITCR1B are cleared to 000b
- When the T7VCNT[2:0] bits in TITCNT1B match the T7VCOR[2:0] bits in TITCR1B

T6ACNT[2:0] Bits (TGIA6 Interrupt Counter)

While the T6AEN bit in TITCR1B is set to 1, the count in these bits is incremented every time a TGIA6 interrupt occurs.
[Clearing conditions]

- When the TITM bit in TITMRB is 1
- When the T6AEN bit in TITCR1B is cleared to 0
- When the T6ACOR[2:0] bits in TITCR1B are cleared to 000b
- When the T6ACNT[2:0] bits in TITCNT1B match the T6ACOR[2:0] bits in TITCR1B

19.2.41 Timer Interrupt Skipping Set Registers 2 (TITCR2A, TITCR2B)

TITCR2A and TITCR2B specify the interrupt skipping count for TRG4AN and TRG4BN (TRG7AN and TRG7BN). This setting is valid only while TITMRA or TITMRB is set to 1.

- TITCR2A

Address(es): MTU.TITCR2A A006 A03Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG4COR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4COR [2:0]	TRG4AN/TRG4BN Interrupt Skipping Count Setting	These bits specify the TRG4AN/TRG4BN interrupt skipping count within the range from 0 to 7. For details, see Table 19.60.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.60 Setting of Interrupt Skipping Count by TRG4COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG4COR2	TRG4COR1	TRG4COR0	Description
0	0	0	Does not skip TRG4AN and TRG4BN interrupts.
0	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 1.
0	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 2.
0	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 3.
1	0	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 4.
1	0	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 5.
1	1	0	Sets the TRG4AN and TRG4BN interrupt skipping count to 6.
1	1	1	Sets the TRG4AN and TRG4BN interrupt skipping count to 7.

- TITCR2B

Address(es): MTU.TITCR2B A006 A83Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7COR[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7COR [2:0]	TRG7AN/TRG7BN Interrupt Skipping Count Setting	These bits specify the TRG7AN/TRG7BN interrupt skipping count within the range from 0 to 7. For details, see Table 19.61.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 19.61 Setting of Interrupt Skipping Count by TRG7COR[2:0] Bits

Bit 2	Bit 1	Bit 0	
TRG7COR2	TRG7COR1	TRG7COR0	Description
0	0	0	Does not skip TRG7AN and TRG7BN interrupts.
0	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 1.
0	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 2.
0	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 3.
1	0	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 4.
1	0	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 5.
1	1	0	Sets the TRG7AN and TRG7BN interrupt skipping count to 6.
1	1	1	Sets the TRG7AN and TRG7BN interrupt skipping count to 7.

19.2.42 Timer Interrupt Skipping Counters 2 (TITCNT2A, TITCNT2B)

TITCNT2A and TITCNT2B start counting from the values set in the TRG4COR[2:0] and TRG7COR[2:0] bits and the count decrements every time TRG4AN or TRG4BN (TITCNT2A) is generated or TRG7AN or TRG7BN (TITCNT2B) is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts or the TRG7AN and TRG7BN interrupts become valid.

- TITCNT2A

Address(es): MTU.TITCNT2A A006 A03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG4CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG4CNT [2:0]	TRG4AN/TRG4BN Interrupt Counter	These bits start counting from the value set in TRG4COR[2:0] and the count decrements every time TRG4AN or TRG4BN is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to this bit has no effect.	R

TRG4CNT[2:0] Bits (TRG4AN/TRG4BN Interrupt Counter)

These bits start counting from the value set in the TRG4COR[2:0] bits and the count decrements every time a TRG4AN or TRG4BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG4AN and TRG4BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRA is 0
- When the TRG4COR[2:0] bits in TITCR2A are cleared to 000b
- When the count of TRG4AN and TRG4BN occurrence matches the TRG4COR[2:0] value in TITCR2A

- TITCNT2B

Address(es): MTU.TITCNT2B A006 A83Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TRG7CNT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TRG7CNT [2:0]	TRG7AN/TRG7BN Interrupt Counter	These bits start counting from the value set in TRG7COR[2:0] and the count decrements every time TRG7AN or TRG7BN is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.	R
b7 to b3	—	Reserved	These bits are read as 0. Writing to this bit has no effect.	R

TRG7CNT[2:0] Bits (TRG7AN/TRG7BN Interrupt Counter)

These bits start counting from the value set in the TRG7COR[2:0] bits and the count decrements every time a TRG7AN or TRG7BN interrupt is generated. When the count reaches 0 and is reloaded, the TRG7AN and TRG7BN interrupts become valid.

[Clearing conditions]

- When the TITM bit in TITMRB is 0
- When the TRG7COR[2:0] bits in TITCR2B are cleared to 000b
- When the count of TRG7AN and TRG7BN occurrence matches the TRG7COR[2:0] value in TITCR2B

19.2.43 Bus Master Interface

The timer counter (MTU8.TCNT), general registers (MTU8.TGRn) for MTU8, and MTU1.TCNTLW, MTU1.TGRALW, and MTU1.TGRBLW registers when TMDR3.LWA = 1 are 32-bit registers. A 32-bit data bus to the bus master enables 32-bit read/write access. 8- and 16-bit read/write are not allowed. Always access these registers in 32-bit units.

The timer counters (MTU0.TCNT to MTU7.TCNT) excluding MTU8, general registers (MTU0.TGRn to MTU7.TGRn), timer subcounters (TCNTSA and TCNTSB), timer cycle buffer registers (TCBRA and TCBRB), timer dead time data registers (TDDRA and TDDRB), timer cycle data registers (TCDRA and TCDRB), timer A/D converter start request control registers (MTU4.TADCR and MTU7.TADCR), timer A/D converter start request cycle set registers (MTU4.TADCORA, MTU4.TADCORB, MTU7.TADCORA, and MTU7.TADCORB), and timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA, MTU4.TADCOBRB, MTU7.TADCOBRA, and MTU7.TADCOBRB) are 16-bit registers. A 16-bit data bus to the bus master enables 16-bit read/write access. 8-bit read/write is not allowed. Always access the registers in 16-bit units.

All registers other than the above registers are 8-bit registers. A 16-bit data bus to the CPU enables 16-bit read/write access. These registers can also be accessed in 8-bit units.

19.3 Operation

19.3.1 Basic Functions

Each channel has TCNT and TGR. TCNT performs up-counting, and is also capable of free-running operation, periodic counting, and external event counting.
Each TGR can be used as an input capture register or an output compare register.

(1) Counter Operation

When one of bits CST0 to CST4 and CST8 in TSTRA, bits CST6 and CST7 in TSTRB, and bits CSTU5, CSTV5, and CSTW5 in MTU5.TSTR is set to 1, TCNT for the corresponding channel begins counting. TCNT can operate as a free-running counter, periodic counter, for example.

(a) Example of Count Operation Setting Procedure

Figure 19.5 shows an example of the count operation setting procedure.

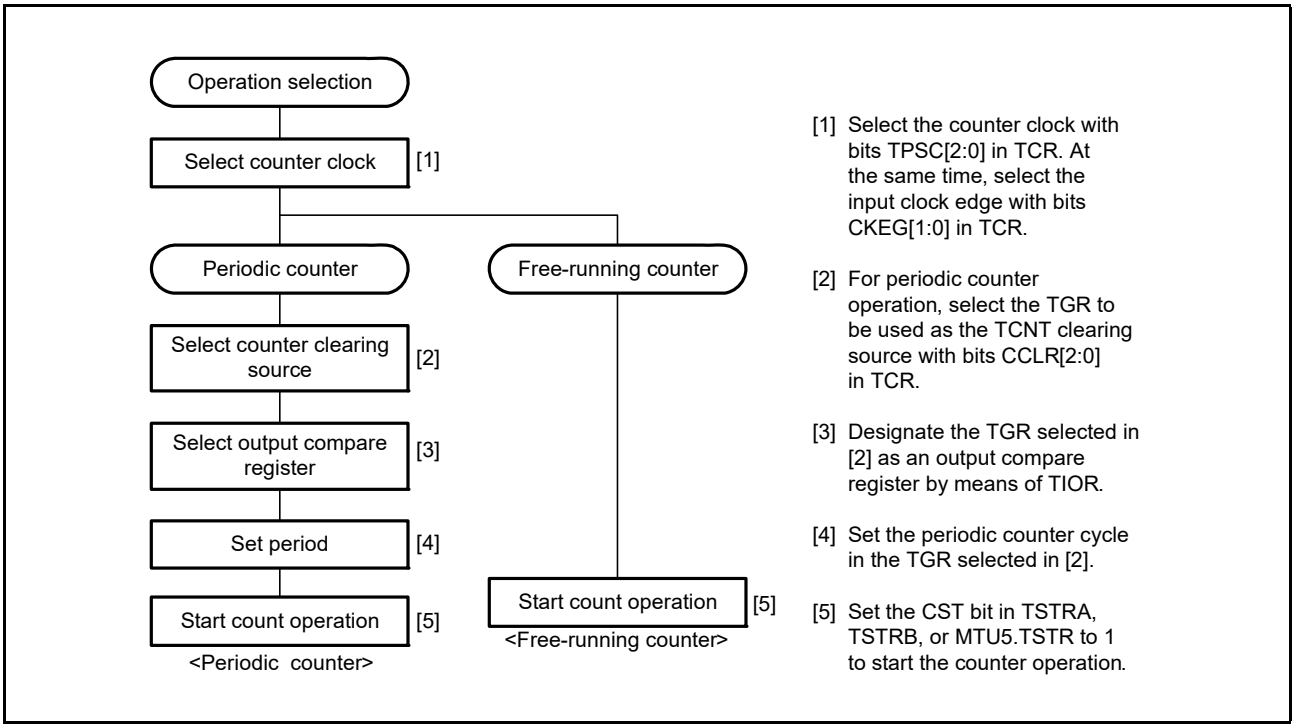


Figure 19.5 Example of Counter Operation Setting Procedure

(b) Free-Running Count Operation and Periodic Count Operation

Immediately after a reset, the MTU's TCNT counters are all designated as free-running counters. When the relevant bit in TSTRA, TSTRB, or MTU5.TSTR is set to 1, the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from FFFFh to 0000h), if the corresponding TIER.TCIEV bit is 1, the MTU requests an interrupt. After an overflow, TCNT starts counting up again from 0000h.
Figure 19.6 illustrates free-running counter operation.

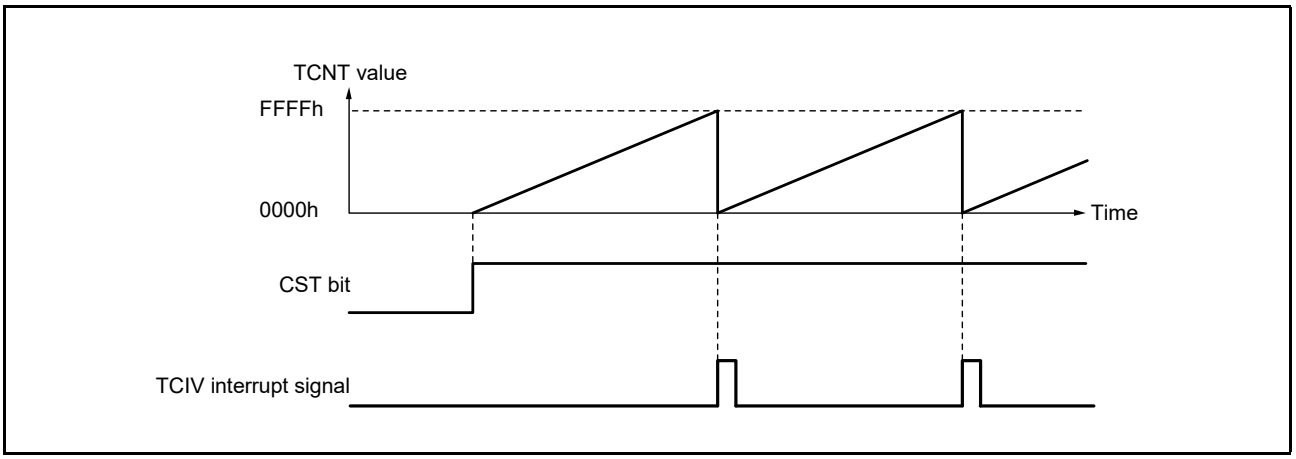


Figure 19.6 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, TCNT for the relevant channel performs periodic count operation. TGR for setting the cycle is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR[2:0] in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTRA, TSTRB or MTU5.TSTR is set to 1. When the count matches the value in TGR, TCNT is cleared to 0000h.
If the value of the corresponding TIER.TGIE bit is 1 at this point, the MTU requests an interrupt. After a compare match, TCNT starts counting up again from 0000h.
Figure 19.7 illustrates periodic counter operation.

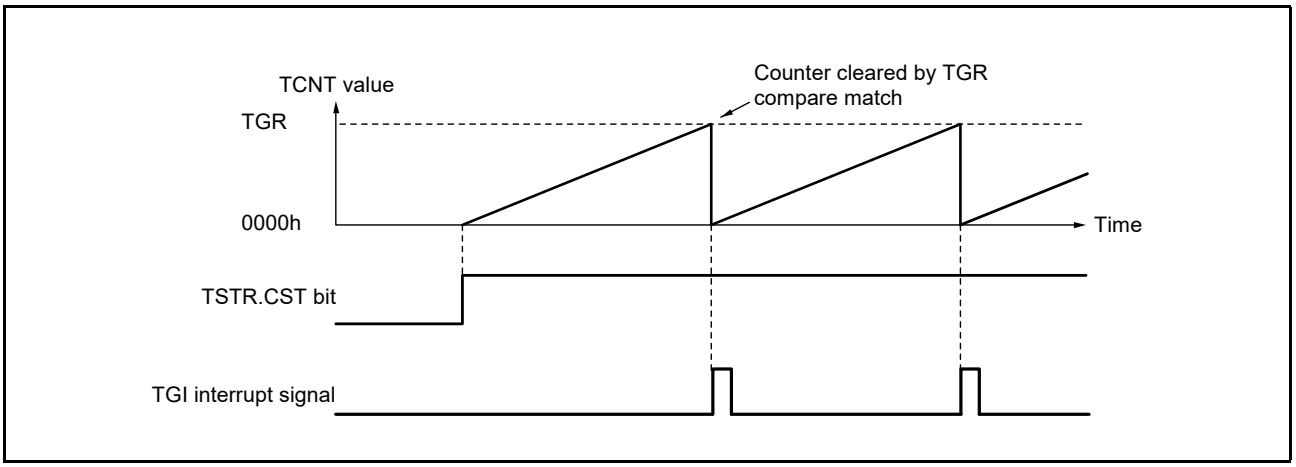


Figure 19.7 Periodic Counter Operation

(2) Waveform Output by Compare Match

The MTU can output low or high or toggles output from the corresponding output pin using compare match. Note that MTU5 cannot output compare-match signals.

(a) Example of Procedure for Setting Waveform Output by Compare Match

Figure 19.8 shows an example of the procedure for setting waveform output by compare match

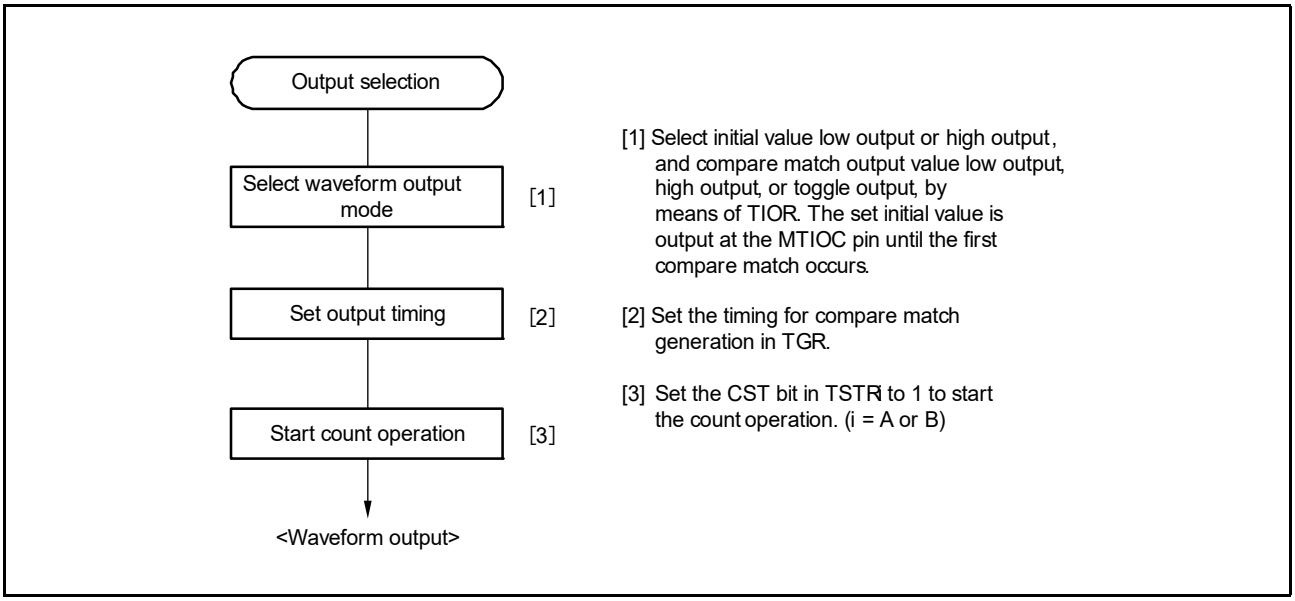


Figure 19.8 Example of Procedure for Setting Waveform Output by Compare Match

(b) Examples of Waveform Output Operation

Figure 19.9 shows an example of low output and high output.
In this example, TCNT has been designated as a free-running counter, and settings have been made so that high is output by compare match A and low is output by compare match B. When the pin level is the same as the specified level, the pin level does not change.

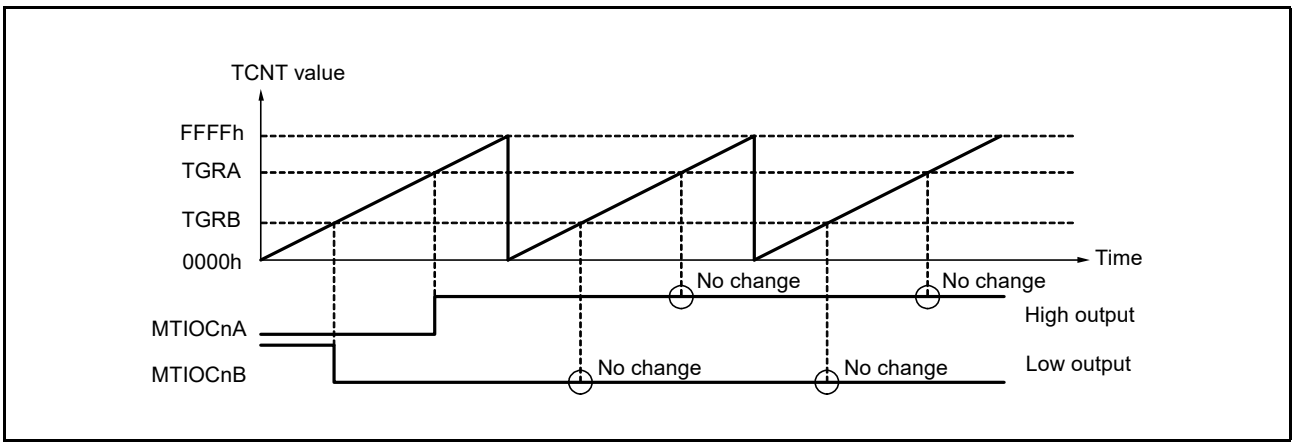


Figure 19.9 Example of low output and high output Operation

Figure 19.10 shows an example of toggle output.
In this example, TCNT has been designated as a periodic counter (with counter clearing on compare match B), and settings have been made so that the output is toggled by both compare match A and compare match B.

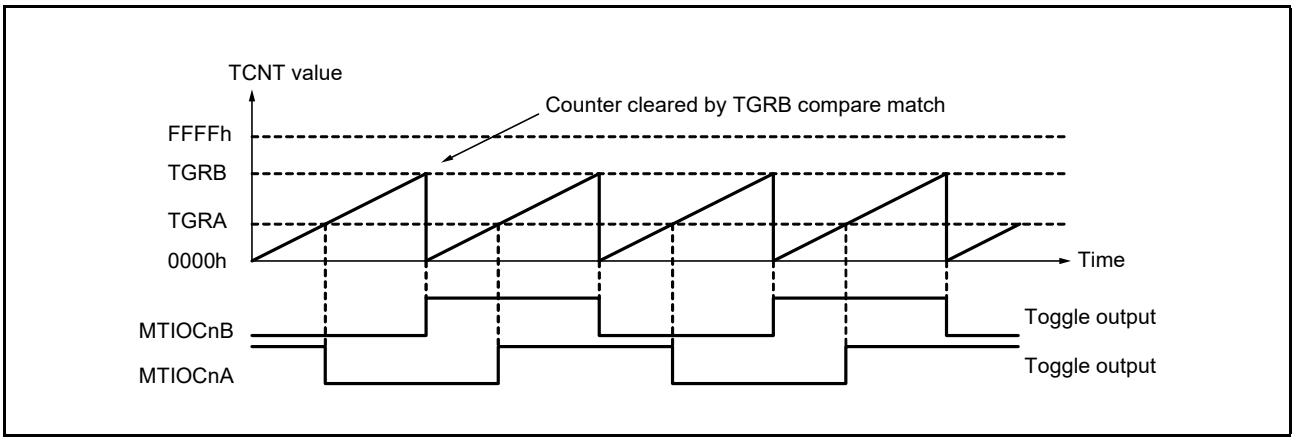


Figure 19.10 Example of Toggle Output Operation

(3) Input Capture Function

The TCNT value can be transferred to TGR on detection of an edge input on the MTIOCnm (n = 0 to 4, 6, 7, or 8, m = A to D), MTIC5U, MTIC5V, or MTIC5W pin.

The rising edge, falling edge, or both edges can be selected as the detection edge. For MTU0 and MTU1, another channel's counter input clock or compare match signal can also be specified as the input capture source.

Note: When another channel's counter input clock is used as the input capture input for MTU0 and MTU1, PCLKC/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if PCLKC/1 is selected.

(a) Example of Input Capture Operation Setting Procedure

Figure 19.11 shows an example of the input capture operation setting procedure.

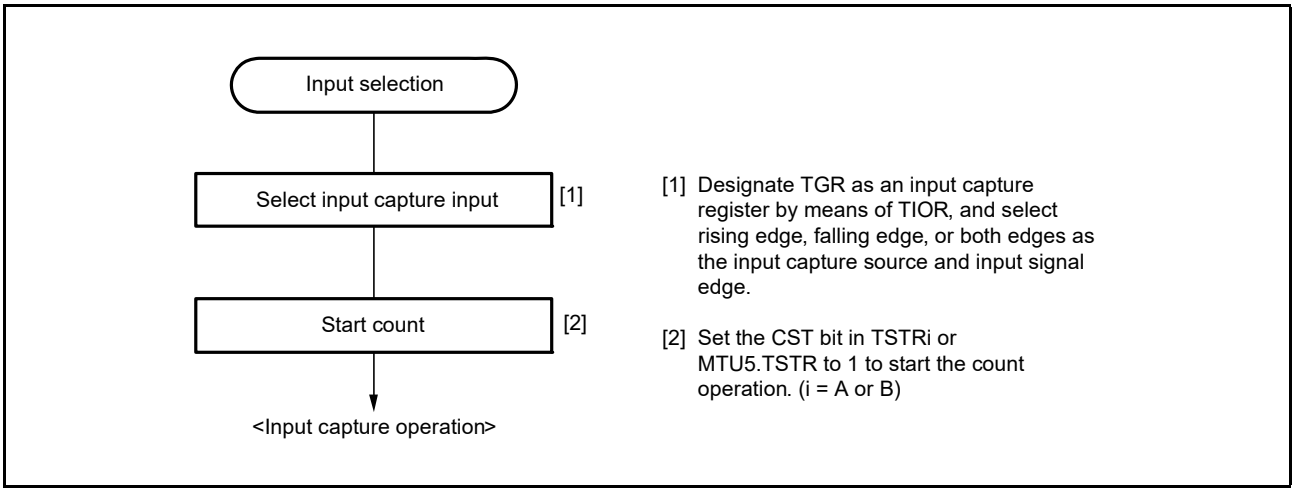


Figure 19.11 Example of Input Capture Operation Setting Procedure

(b) Example of Input Capture Operation

Figure 19.12 shows an example of input capture operation.
In this example, both rising and falling edges have been selected as the MTIOCnA pin input capture input edge, the falling edge has been selected as the MTIOCnB pin input capture input edge, and counter clearing by TGRB input capture has been designated for TCNT (n = 0 to 4, 6, 7, or 8).

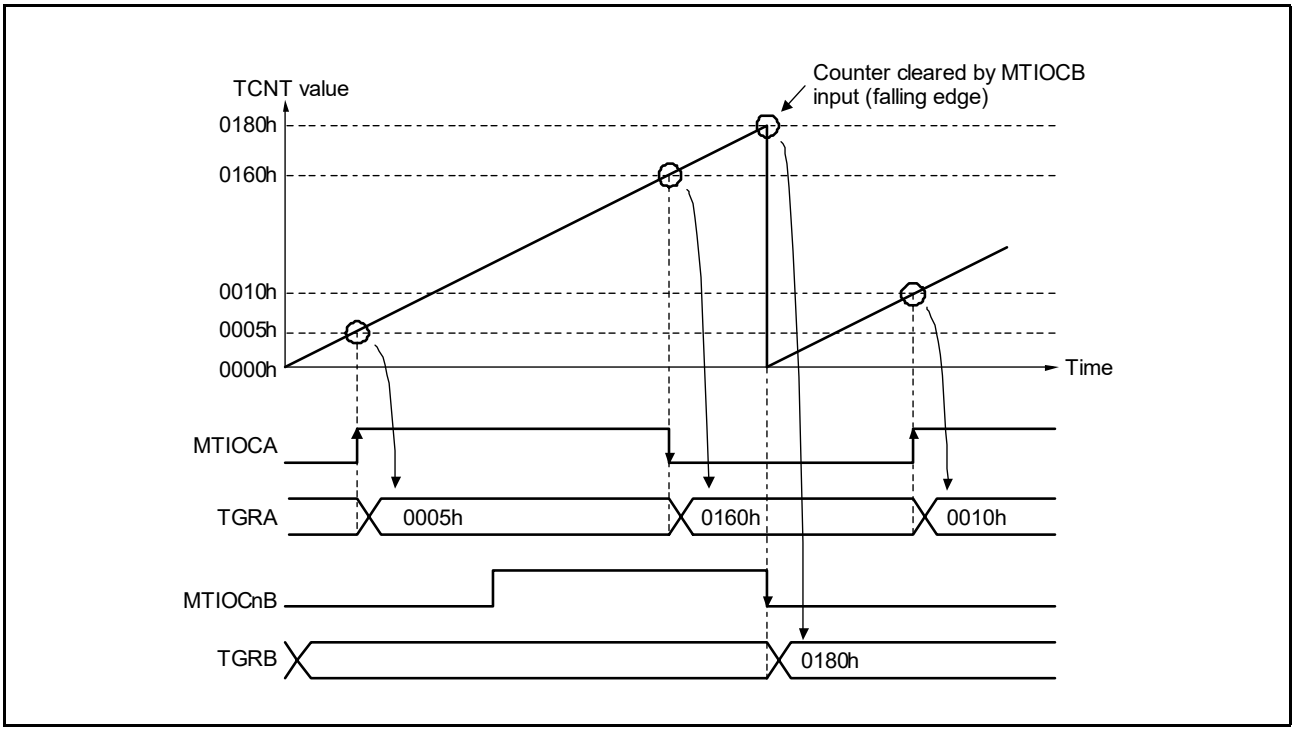


Figure 19.12 Example of Input Capture Operation (n = 0 to 4, 6, 7, or 8)

19.3.2 Synchronous Operation

In synchronous operation, the values in multiple TCNT counters can be modified simultaneously (synchronous presetting). In addition, multiple TCNT counters can be cleared simultaneously (synchronous clearing) by making the appropriate setting in TCR.
Synchronous operation increases the number of TGR registers assigned to a single time base.
MTU0 to MTU4, MTU6, and MTU7 can all be designated for synchronous operation.
MTU5 and MTU8 cannot be used for synchronous operation.

(1) Example of Synchronous Operation Setting Procedure

Figure 19.13 shows an example of the synchronous operation setting procedure.

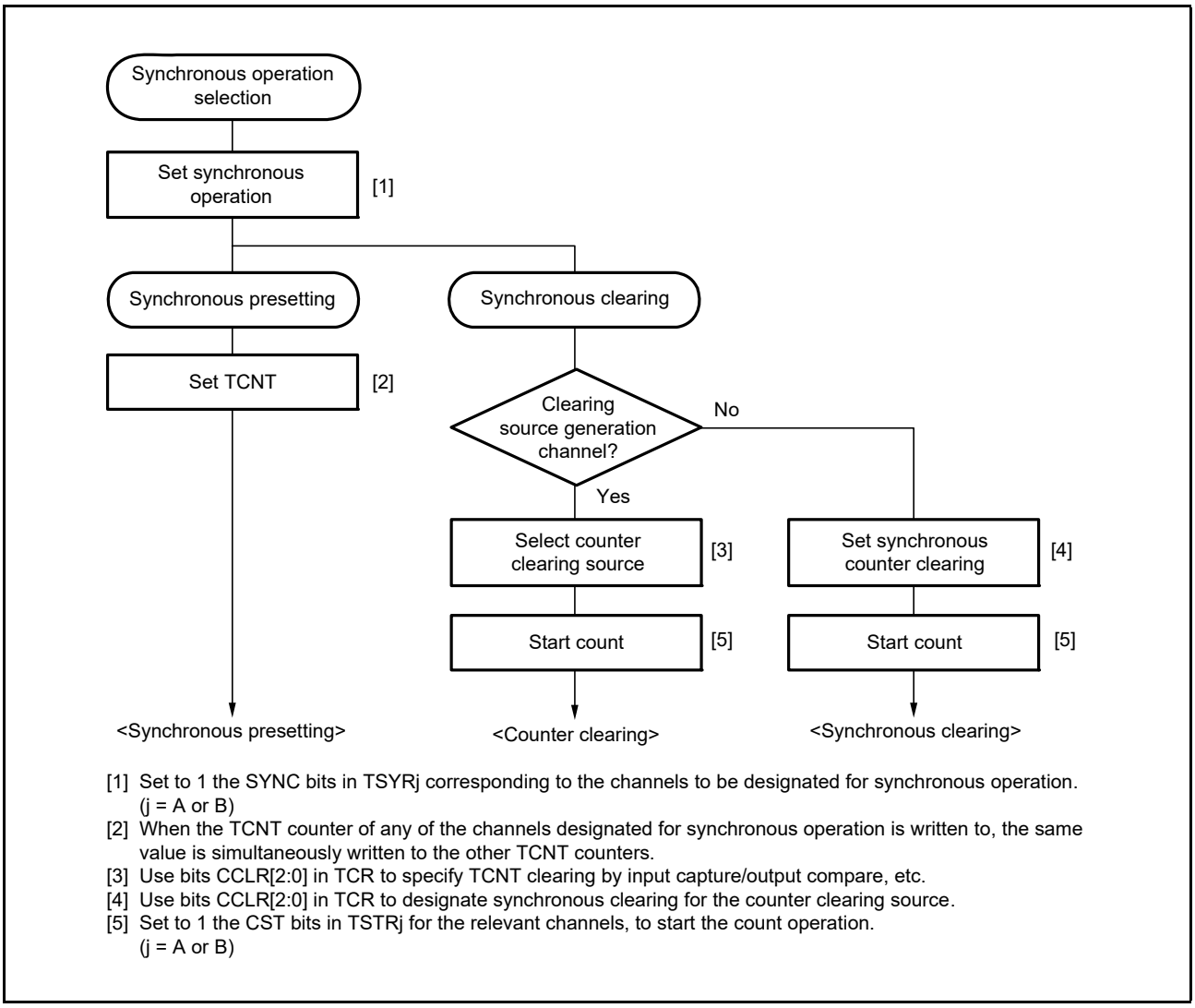


Figure 19.13 Example of Synchronous Operation Setting Procedure

(2) Example of Synchronous Operation

Figure 19.14 shows an example of synchronous operation.
In this example, synchronous operation and PWM mode 1 have been designated for MTU0 to MTU2, MTU0.TGRB compare match has been set as the counter clearing source in MTU0, and synchronous clearing has been set for the counter clearing source in MTU1 and MTU2.
Three-phase PWM waveforms are output from pins MTIOC0A, MTIOC1A, and MTIOC2A. At this time, synchronous presetting and synchronous clearing by MTU0.TGRB compare match are performed for the TCNT counters in MTU0 to MTU2, and the data set in MTU0.TGRB is used as the PWM cycle.
For details of PWM modes, see section 19.3.5, PWM Modes.

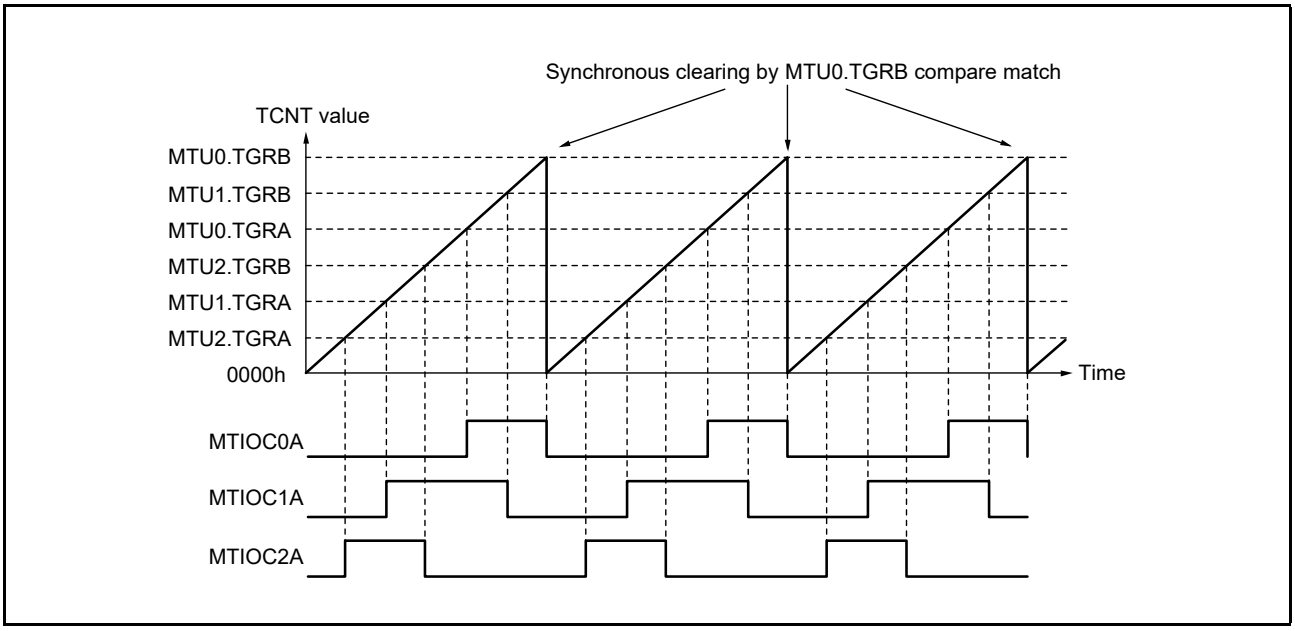


Figure 19.14 Example of Synchronous Operation

19.3.3 Buffer Operation

Buffer operation, provided for MTU0, MTU3, MTU4, MTU6, MTU7, and MTU8, enables TGRC and TGRD to be used as buffer registers. In MTU0, TGRF can also be used as a buffer register.
Buffer operation differs depending on whether TGR has been designated as an input capture register or as a compare match register.

Note: MTU0.TGRE cannot be designated as an input capture register and can only operate as a compare match register.

Table 19.62 shows the register combinations used in buffer operation.

Table 19.62 Register Combinations in Buffer Operation

Channel	Timer General Register	Buffer Register
MTU0	TGRA	TGRC
	TGRB	TGRD
	TGRE	TGRF
MTU3	TGRA	TGRC
	TGRB	TGRD
MTU4	TGRA	TGRC
	TGRB	TGRD
MTU6	TGRA	TGRC
	TGRB	TGRD
MTU7	TGRA	TGRC
	TGRB	TGRD
MTU8	TGRA	TGRC
	TGRB	TGRD

- When TGR is an output compare register

When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.
This operation is illustrated in Figure 19.15.

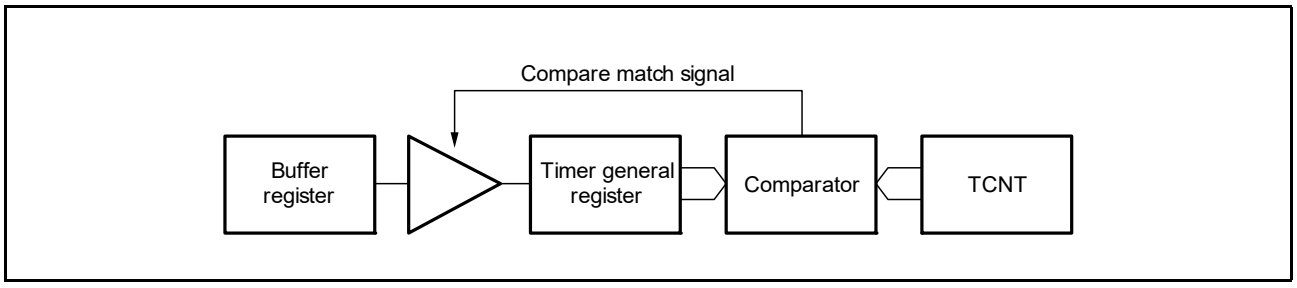


Figure 19.15 Compare Match Buffer Operation

- When TGR is an input capture register

When an input capture occurs, the value in TCNT is transferred to TGR and the value previously held in TGR is transferred to the buffer register.
This operation is illustrated in Figure 19.16.

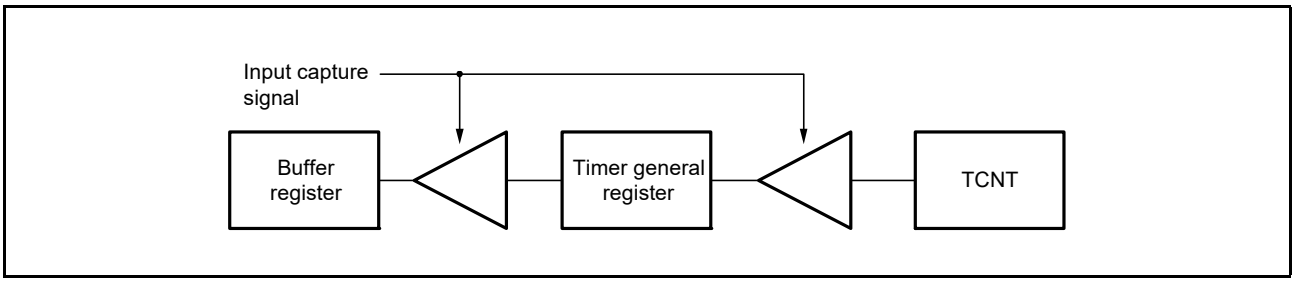


Figure 19.16 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 19.17 shows an example of the buffer operation setting procedure.

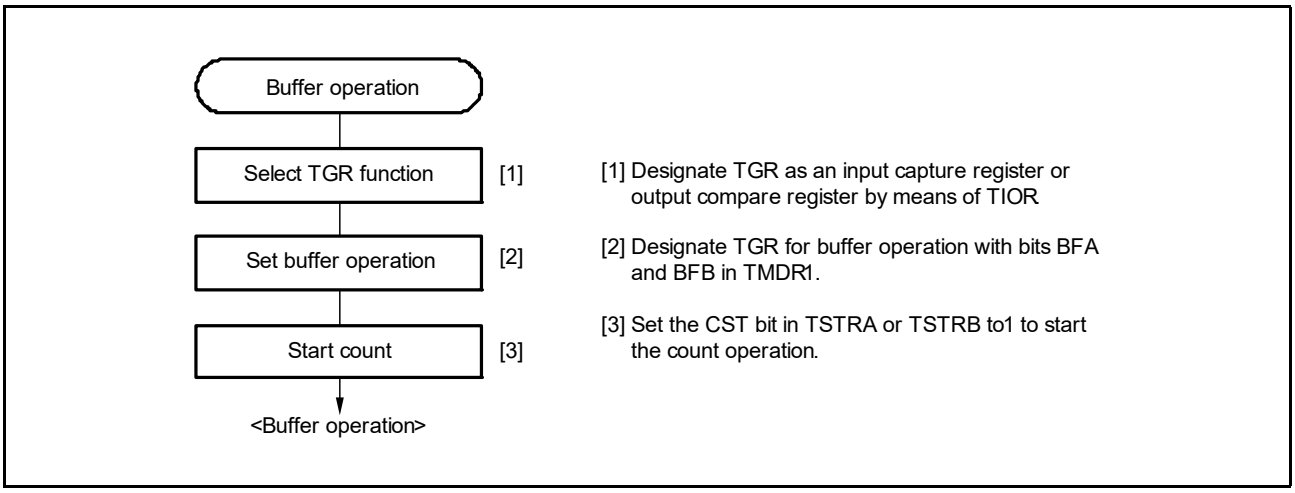


Figure 19.17 Example of Buffer Operation Setting Procedure

(2) Examples of Buffer Operation

(a) When TGR is an Output Compare Register

Figure 19.18 shows an operation example in which PWM mode 1 has been designated for MTU0, and TGRC has been designated as a buffer register for TGRA. The settings used in this example are TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. In this example, the TTSA bit in TBTM is cleared to 0.

As buffer operation has been set, when compare match A occurs, the output changes and the value in buffer register TGRC is simultaneously transferred to timer general register TGRA. This operation is repeated each time compare match A occurs.

For details of PWM modes, see section 19.3.5, PWM Modes.

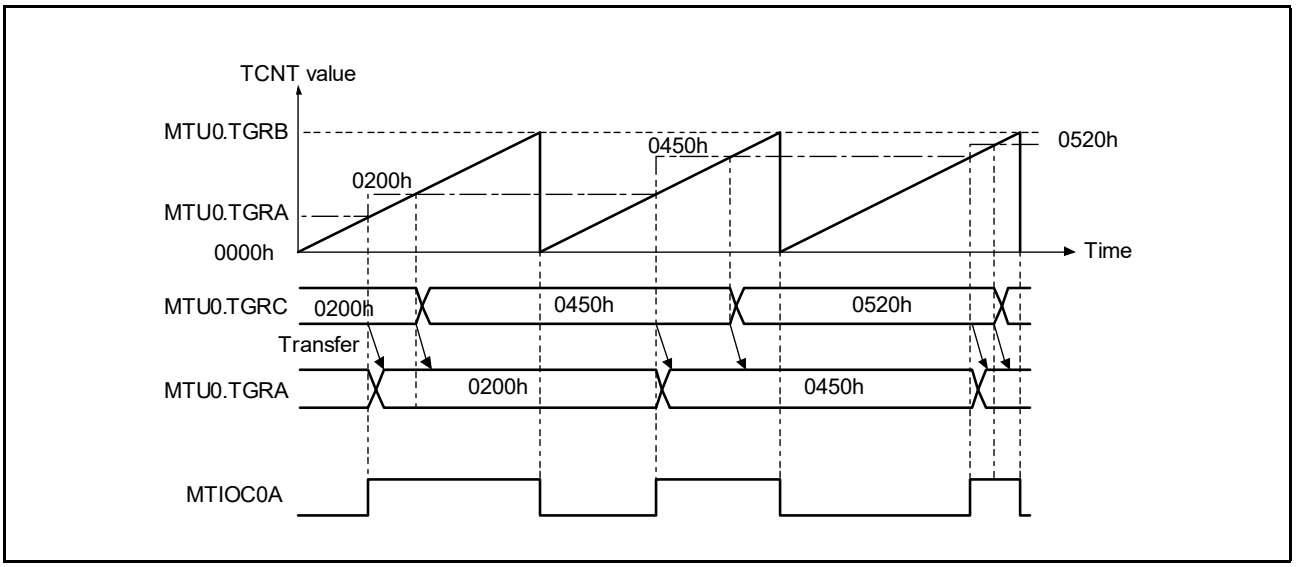


Figure 19.18 Example of Buffer Operation (1)

(b) When TGR is an Input Capture Register

Figure 19.19 shows an operation example in which TGRA has been designated as an input capture register, and TGRC has been designated as a buffer register for TGRA.
Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the MTIOCnA pin input capture input edge (n = 0 to 4, 6, 7, or 8).
As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

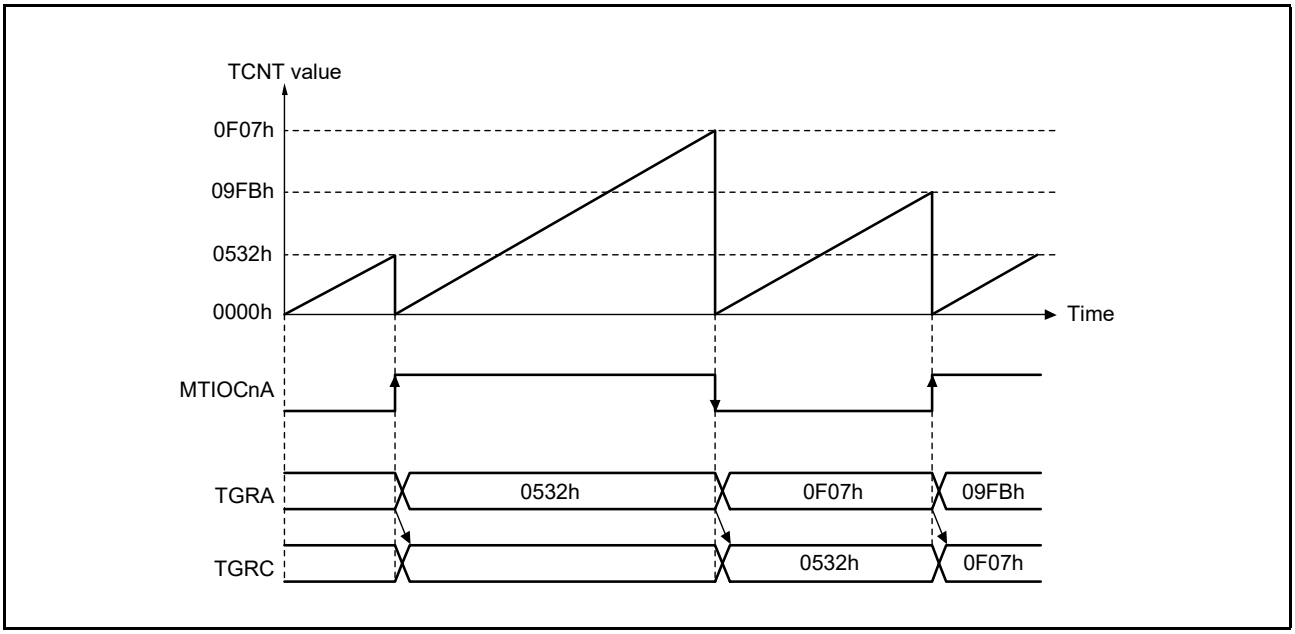


Figure 19.19 Example of Buffer Operation (2) (n = 0 to 4, 6, 7, or 8)

(3) Selecting Timing for Transfer from Buffer Registers to Timer General Registers in PWM Mode

The timing for transfer from buffer registers to timer general registers can be selected in PWM mode only by setting the buffer operation transfer mode registers (MTUn.TBTM (n = 0, 3, 4, 6, or 7)). The timing for transfer can be selected in PWM mode 1 or 2 for MTU0, or in PWM mode 1 for MTU3, MTU4, MTU6, and MTU7. Either compare match (value after reset) or TCNT clearing can be selected for the transfer timing. TCNT clearing as transfer timing is one of the following cases.

- When TCNT overflows (FFFFh to 0000h)
- When 0000h is written to TCNT during counting
- When TCNT is cleared to 0000h under the condition specified in the CCLR[2:0] bits in TCR

Note: TBTM must be modified only while TCNT stops.

Figure 19.20 shows an operation example in which PWM mode 1 is designated for MTU0 and buffer operation is designated for MTU0.TGRA and MTU0.TGRC. The settings used in this example are MTU0.TCNT clearing by compare match B, high output at compare match A, and low output at compare match B. The TTSA bit in MTU0.TBTM is set to 1.

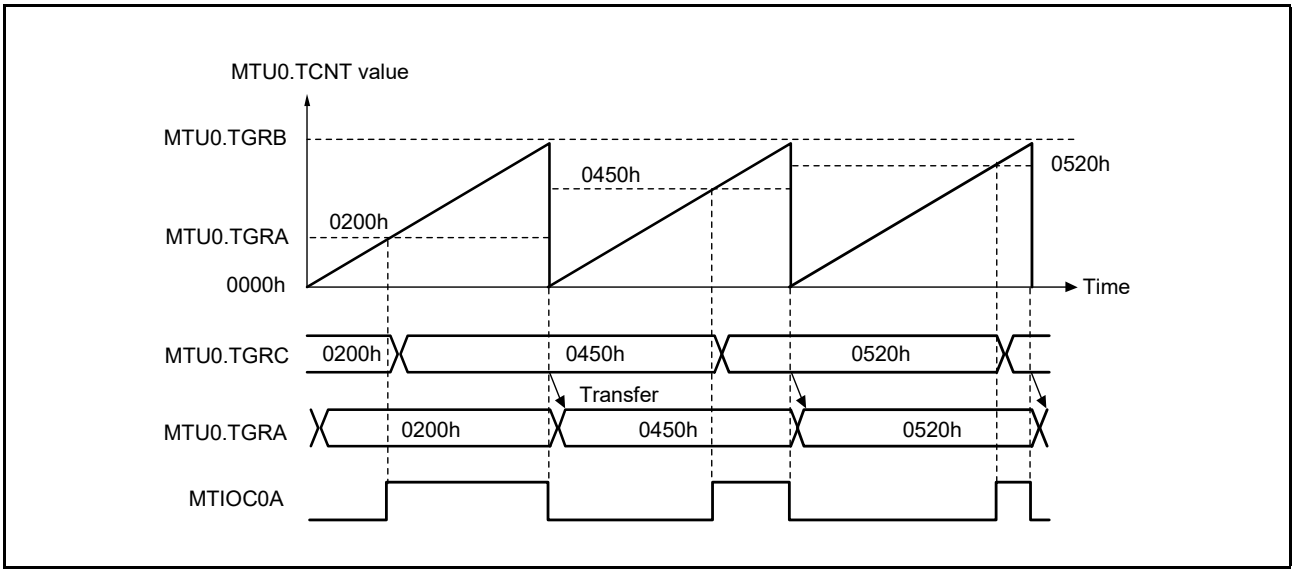


Figure 19.20 Example of Buffer Operation When MTU0.TCNT Clearing is Selected for MTU0.TGRC-to-MTU0.TGRA Transfer Timing

19.3.4 Cascaded Operation

In cascaded operation, two 16-bit counters in different channels are used together as a 32-bit counter. The following describes operation when the MTU1.TMDR3.LWA bit is set to 0.

This function works when overflow/underflow of MTU2.TCNT is selected as the counter clock for MTU1 through the TCR.TPSC[2:0] bits.

Underflow occurs only when the lower 16 bits of TCNT is in phase counting mode.

Table 19.63 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for MTU1, the counter clock setting is invalid and the counters operate independently in phase counting mode.

Table 19.63 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
MTU1 and MTU2	MTU1.TCNT	MTU2.TCNT

For simultaneous input capture of MTU1.TCNT and MTU2.TCNT during cascaded operation, additional input capture input pins can be specified by the input capture control register (TICCR). The input-capture condition is of edges in the signal produced by taking the logical OR of the input level on the main input pin and the input level on the added input pin. Accordingly, if either is at the high level, a change in the level of the other will not produce an edge for detection. For details, see (4), Cascaded Operation Example (c). For input capture in cascade connection, see section 19.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection.

Table 19.64 shows the TICCR setting and input capture input pins.

Table 19.64 TICCR Setting and Input Capture Input Pins

Target Input Capture	TICCR Setting	Input Capture Input Pin
Input capture from MTU1.TCNT to MTU1.TGRA	I2AE bit = 0 (initial value)	MTIOC1A
	I2AE bit = 1	MTIOC1A, MTIOC2A
Input capture from MTU1.TCNT to MTU1.TGRB	I2BE bit = 0 (initial value)	MTIOC1B
	I2BE bit = 1	MTIOC1B, MTIOC2B
Input capture from MTU2.TCNT to MTU2.TGRA	I1AE bit = 0 (initial value)	MTIOC2A
	I1AE bit = 1	MTIOC2A, MTIOC1A
Input capture from MTU2.TCNT to MTU2.TGRB	I1BE bit = 0 (initial value)	MTIOC2B
	I1BE bit = 1	MTIOC2B, MTIOC1B

(1) Example of Cascaded Operation Setting Procedure

Figure 19.21 shows an example of the cascaded operation setting procedure.

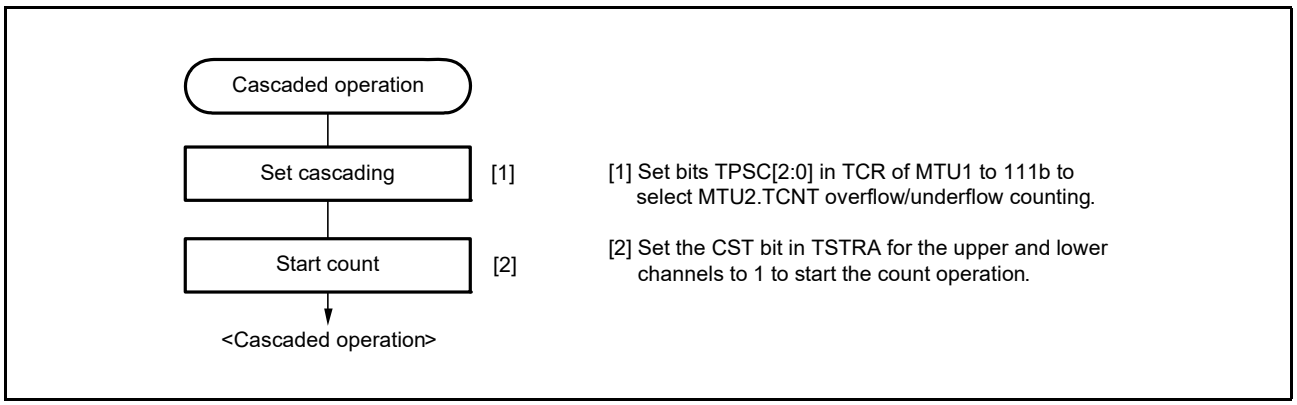


Figure 19.21 Cascaded Operation Setting Procedure

(2) Cascaded Operation Example (a)

Figure 19.22 illustrates the operation when MTU2.TCNT overflow/underflow counting has been set for MTU1.TCNT and phase counting mode has been designated for MTU2.
MTU1.TCNT is incremented by MTU2.TCNT overflow and decremented by MTU2.TCNT underflow.

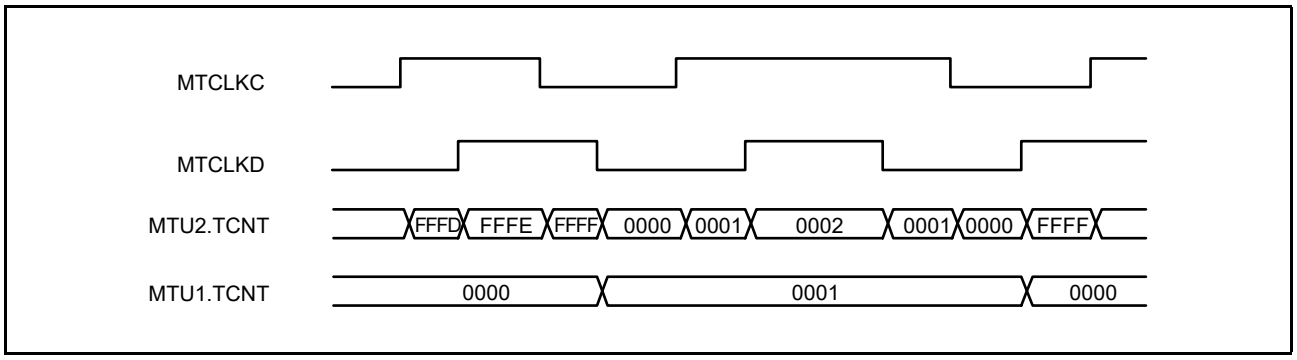


Figure 19.22 Cascaded Operation Example (a)

(3) Cascaded Operation Example (b)

Figure 19.23 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the I2AE bit in TICCR has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the MTU1.TIOR.IOA[3:0] bits have selected the MTIOC1A rising edge for the input capture timing while the MTU2.TIOR.IOA[3:0] bits have selected the MTIOC2A rising edge for the input capture timing.
Under these conditions, the rising edge of both MTIOC1A and MTIOC2A is used for the MTU1.TGRA input capture condition. For the MTU2.TGRA input capture condition, the MTIOC2A rising edge is used.

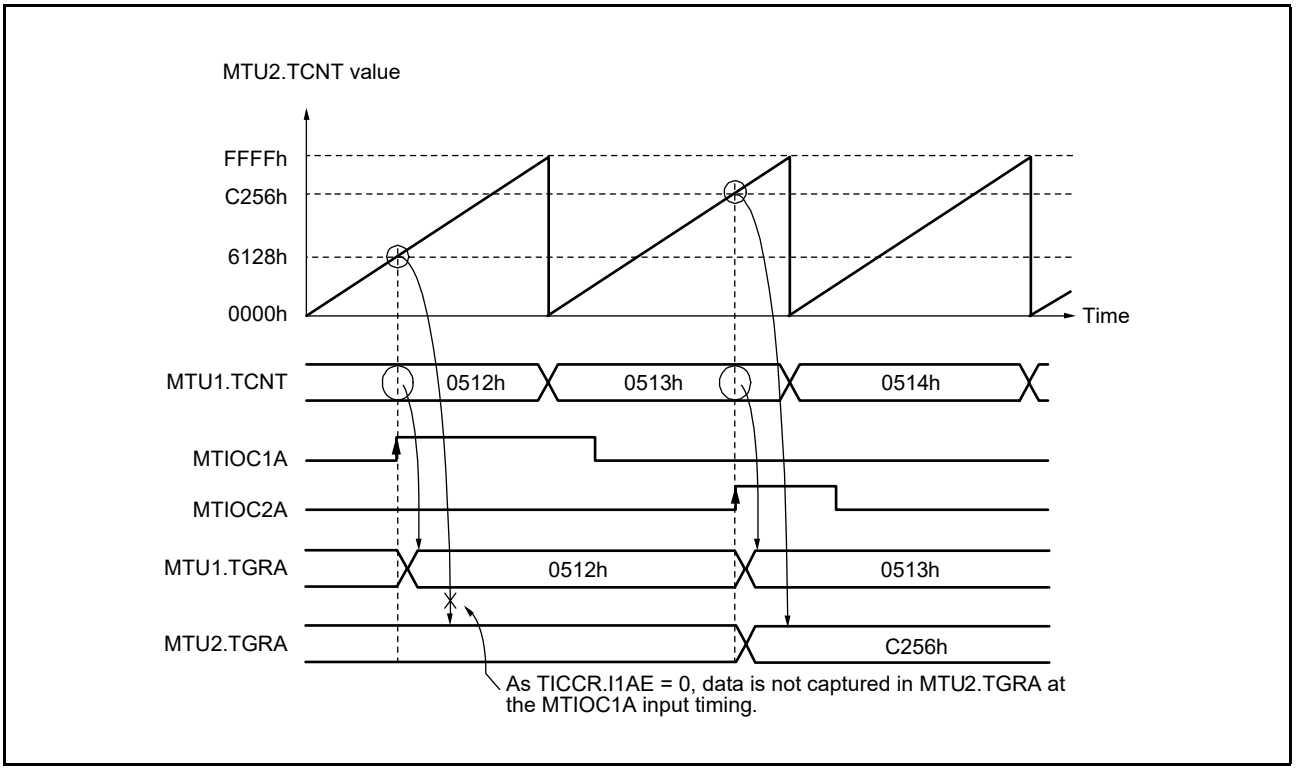
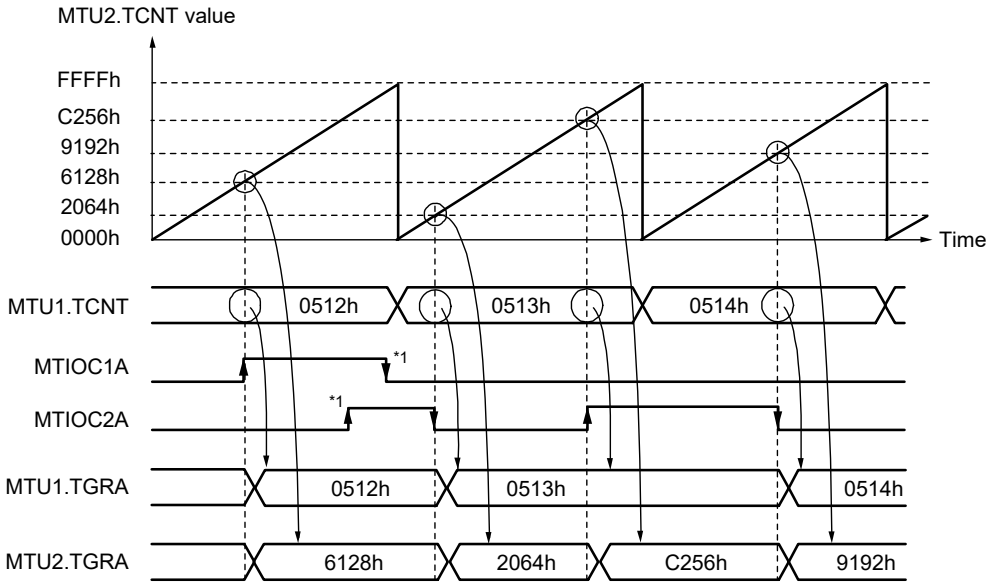


Figure 19.23 Cascaded Operation Example (b)

(4) Cascaded Operation Example (c)

Figure 19.24 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE and I1AE bits have been set to 1 to include the MTIOC2A and MTIOC1A pins in the MTU1.TGRA and MTU2.TGRA input capture conditions, respectively. In this example, the IOA[3:0] bits in both MTU1.TIOR and MTU2.TIOR have selected both the rising and falling edges for the input capture timing. Under these conditions, the ORed result of MTIOC1A and MTIOC2A input is used for the MTU1.TGRA and MTU2.TGRA input capture conditions.



Note 1. When either of the input signals is driven high, the selected edge of the other cannot act as the input capture condition.

Figure 19.24 Cascaded Operation Example (c)

(5) Cascaded Operation Example (d)

Figure 19.25 illustrates the operation when MTU1.TCNT and MTU2.TCNT have been cascaded and the TICCR.I2AE bit has been set to 1 to include the MTIOC2A pin in the MTU1.TGRA input capture conditions. In this example, the IOA[3:0] bits in MTU1.TIOR have selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing while the IOA[3:0] bits in MTU2.TIOR have selected the MTIOC2A rising edge for the input capture timing.

Under these conditions, as MTU1.TIOR has selected occurrence of MTU0.TGRA compare match or input capture for the input capture timing, the MTIOC2A edge is not used for MTU1.TGRA input capture condition although the I2AE bit in TICCR has been set to 1.

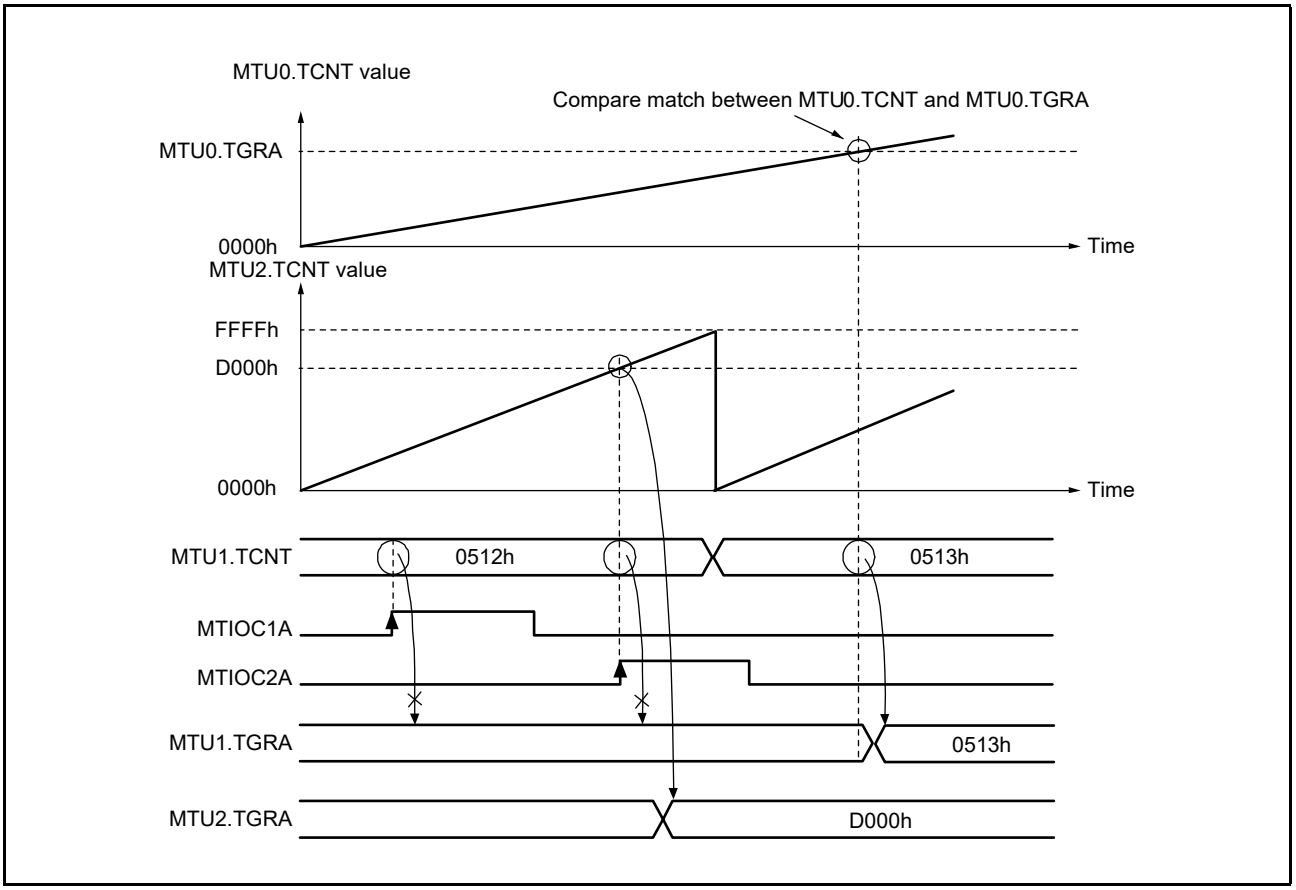


Figure 19.25 Cascaded Operation Example (d)

19.3.5 PWM Modes

PWM modes are provided to output PWM waveforms from the external pins. The output level can be selected as low, high, or toggle output in response to a compare match of each TGR.
PWM waveforms in the range of 0% to 100% duty cycle can be output according to the TGR settings.
By designating TGR compare match as the counter clearing source, the PWM cycle can be specified in that register.
Every channel can be set to PWM mode independently. Synchronous operation is also possible.
There are two PWM modes as described below.

(a) PWM Mode 1

PWM waveforms are output from the MTIOCnA and MTIOCnC pins by pairing TGRA with TGRB and TGRC with TGRD. The levels specified by the TIOR.IOA[3:0] and TIOR.IOC[3:0] bits are output from the MTIOCnA and MTIOCnC pins at compare matches A and C, and the level specified by the TIOR.IOB[3:0] and TIOR.IOD[3:0] bits are output at compare matches B and D (n = 0 to 4, 6, or 7). The initial output value is set in TGRA or TGRC. If the values set in paired TGRs are identical, the output value does not change even when a compare match occurs.
In PWM mode 1, PWM waveforms in up to 12 phases can be output.

(b) PWM Mode 2

PWM waveform output is generated using one TGR as the cycle register and the others as duty registers. The level specified in TIOR is output at compare matches. Upon counter clearing by a cycle register compare match, the initial value set in TIOR is output from each pin. If the values set in the cycle and duty registers are identical, the output value does not change even when a compare match occurs.

In PWM mode 2, up to eight phases of PWM waveforms can be output when using synchronous operation in combination.

The correspondence between PWM output pins and registers is shown in Table 19.65.

Table 19.65 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Register**	**PWM Mode 1**	**PWM Mode 2**
MTU0	TGRA	MTIOC0A	MTIOC0A
	TGRB		MTIOC0B
	TGRC	MTIOC0C	MTIOC0C
	TGRD		MTIOC0D
MTU1	TGRA	MTIOC1A	MTIOC1A
	TGRB		MTIOC1B
MTU2	TGRA	MTIOC2A	MTIOC2A
	TGRB		MTIOC2B
MTU3	TGRA	MTIOC3A	Setting prohibited
	TGRB		
	TGRC	MTIOC3C	
	TGRD		
MTU4	TGRA	MTIOC4A	
	TGRB		
	TGRC	MTIOC4C	
	TGRD		
MTU6	TGRA	MTIOC6A	
	TGRB		
	TGRC	MTIOC6C	
	TGRD		
MTU7	TGRA	MTIOC7A	
	TGRB		
	TGRC	MTIOC7C	
	TGRD		

Note: In PWM mode 2, PWM waveform output is not possible for the TGR register in which the PWM cycle is set.

(1) Example of PWM Mode Setting Procedure

Figure 19.26 shows an example of the PWM mode setting procedure.

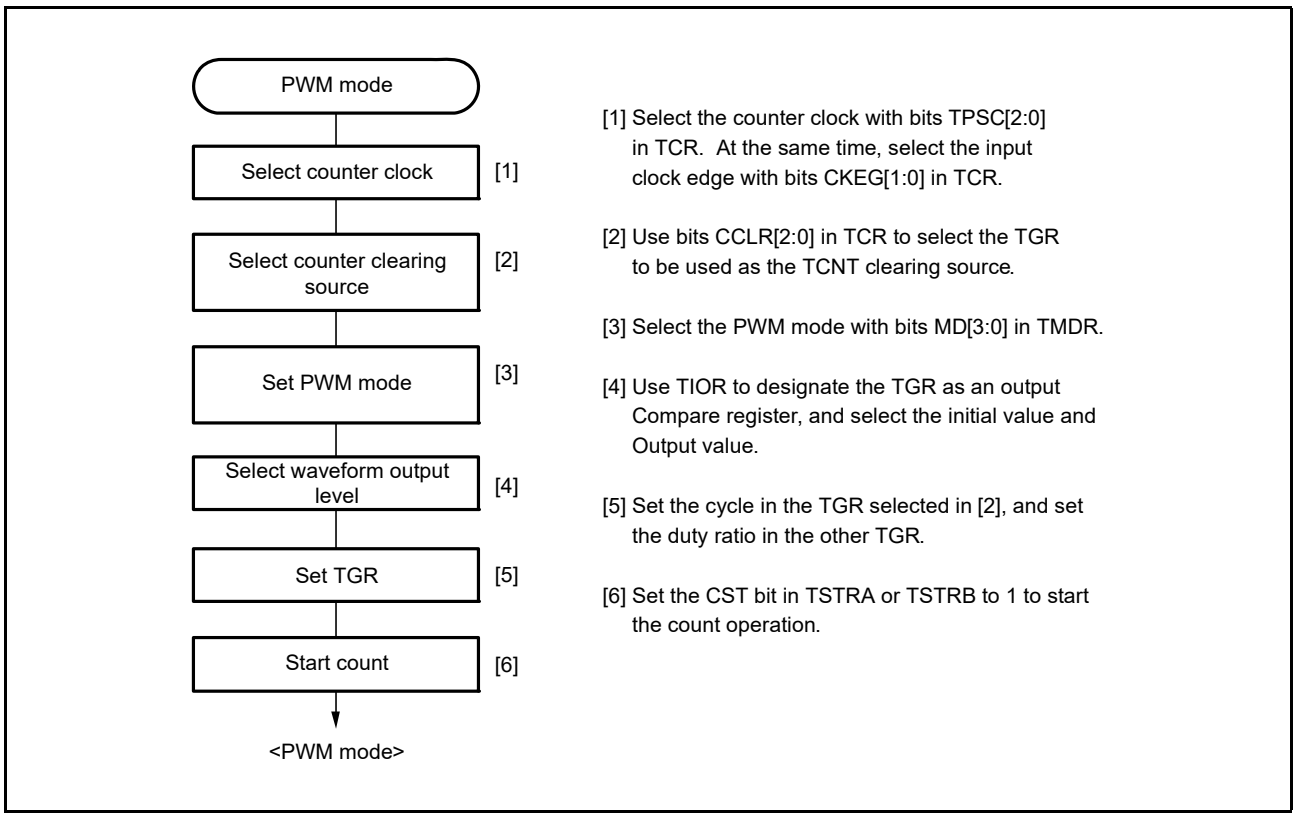


Figure 19.26 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 19.27 shows an example of operation in PWM mode 1.
In this example, TGRA compare match is set as the TCNT clearing source, 0 is set as the initial output value and output value for TGRA, and 1 is set as the output value for TGRB.
In this case, the value set in TGRA is used as the cycle, and the value set in TGRB is used as the duty ratio.

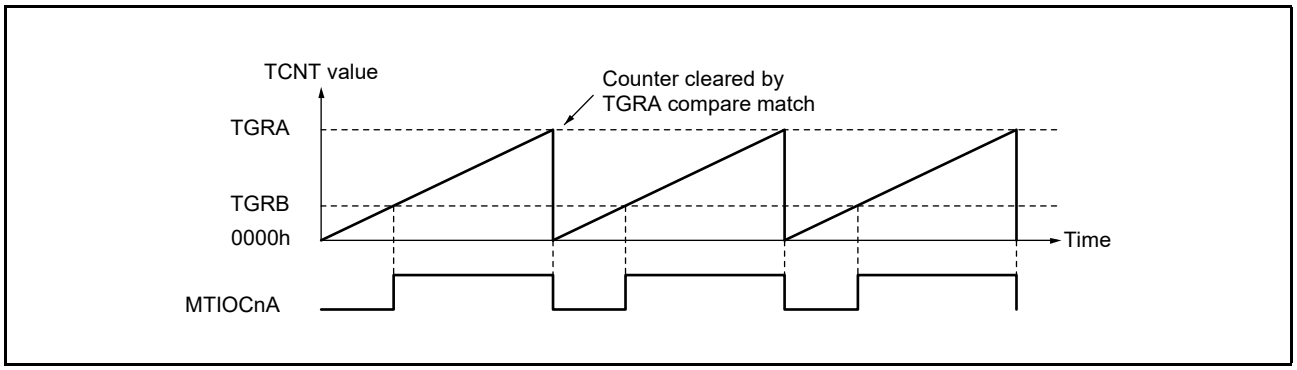


Figure 19.27 Example of PWM Mode 1 Operation (n = 0 to 4, 6, or 7)

Figure 19.28 shows an example of operation in PWM mode 2.
In this example, synchronous operation is designated for MTU0 and MTU1, MTU1.TGRB compare match is set as the TCNT clearing source, and Low is set as the initial output value and High as the output value for the other TGR registers (MTU0.TGRA to MTU0.TGRD and MTU1.TGRA), outputting 5-phase PWM waveforms.
In this case, the value set in MTU1.TGRB is used as the cycle, and the values set in the other TGRs are used as the duty ratio.

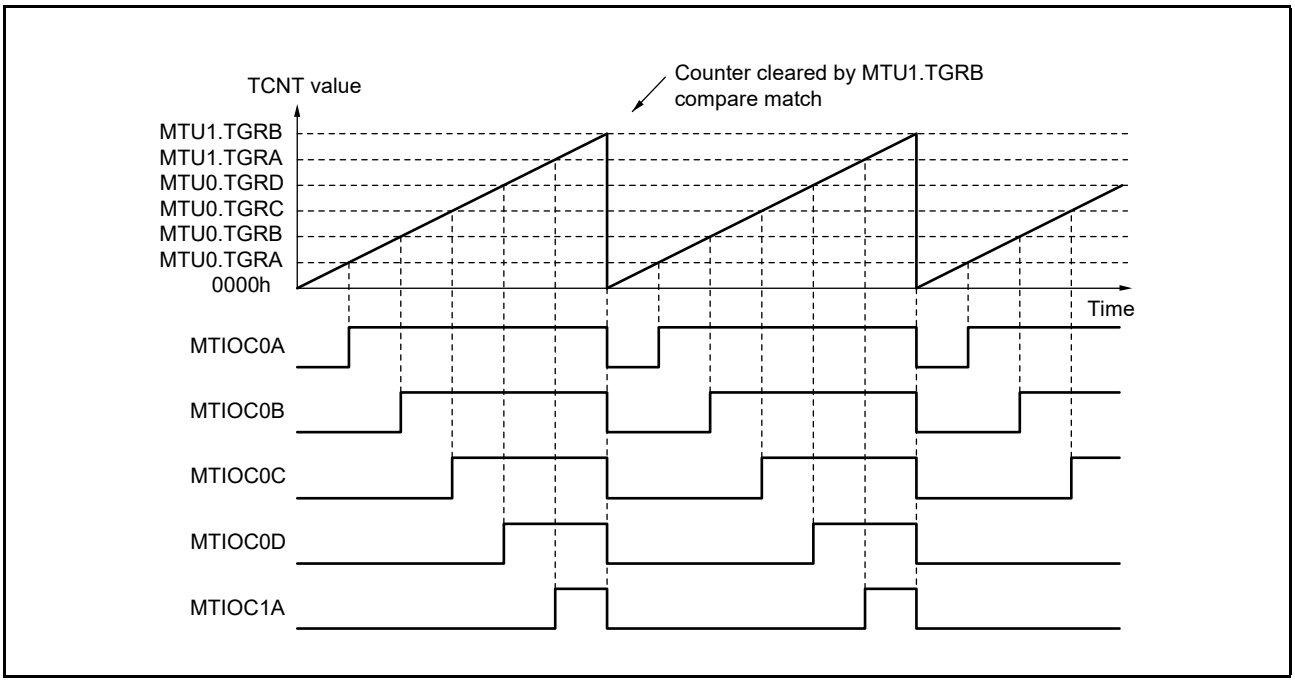


Figure 19.28 Example of PWM Mode 2 Operation

Figure 19.29 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

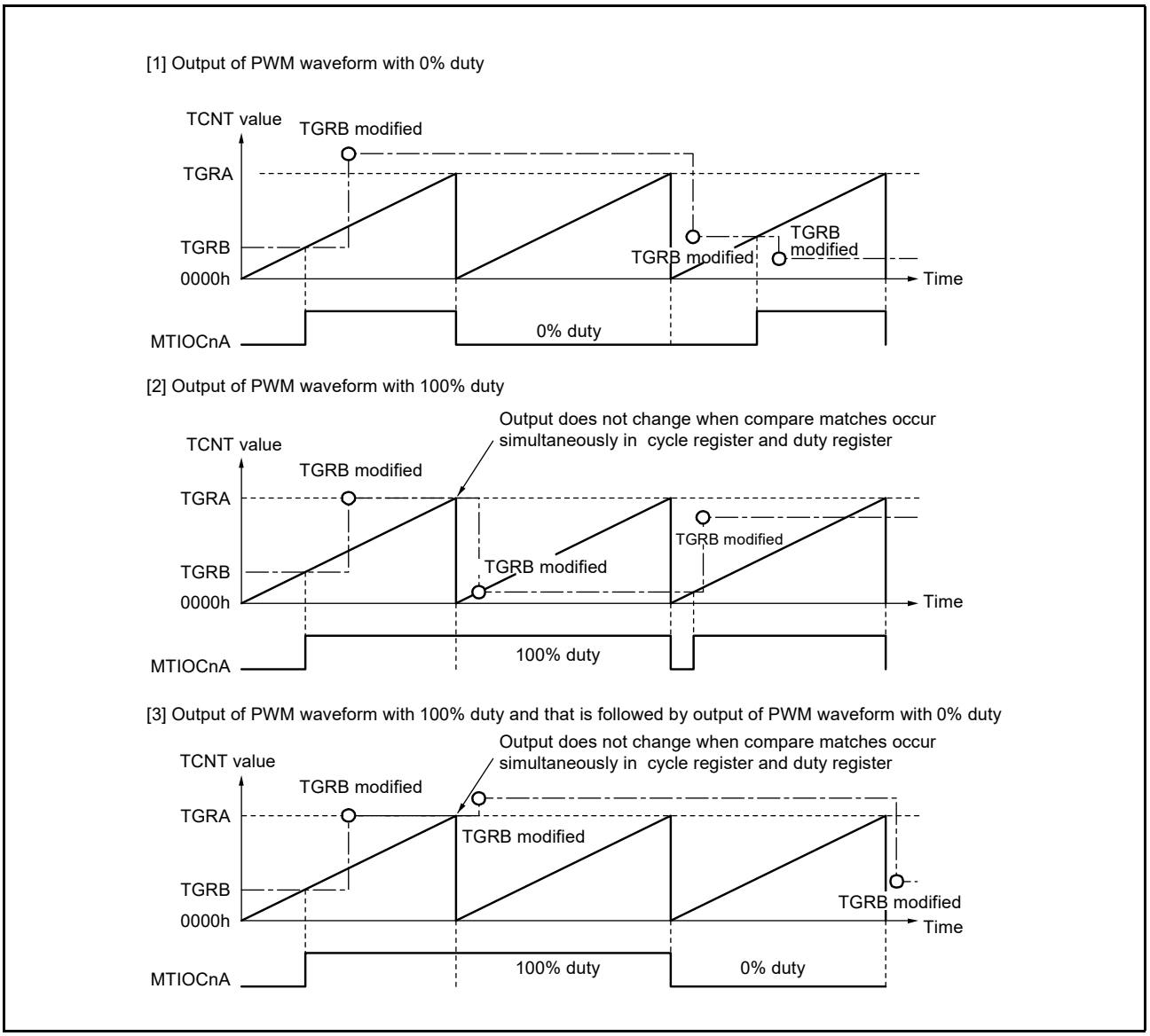


Figure 19.29 Examples of PWM Mode Operation (PWM Waveform Output with 0% Duty and 100% Duty) (n = 0 to 4, 6, or 7)

19.3.6 Phase Counting Mode

In phase counting mode, the phase difference between two external input clocks is detected and TCNT is incremented or decremented accordingly. This mode can be set for MTU1 and MTU2.

When phase counting mode is specified, an external clock is selected as the counter input clock and TCNT operates as an up-counter/down-counter regardless of the setting of the TCR.TPSC[2:0], TCR2.TPSC2[2:0], and TCR2.CKEG[1:0] bits. However, the functions of bits CCLR[1:0] in TCR and of TIOR, TIER, and TGR are valid, and input capture/compare match and interrupt functions can be used.

This can be used for two-phase encoder pulse input.

If an overflow occurs while TCNT is counting up, a TCIV interrupt is generated if the TCIEV bit in the TIER register is 1. If an underflow occurs while TCNT is counting down, a TCIU interrupt is generated if the TCIEU bit in the TIER register is 1.

The TCFD flag in TSR is the count direction flag. Read the TCFD flag to check whether TCNT is counting up or down.

This module operates in two phase counting mode: 16- and 32-bit modes. In 16-bit phase counting mode, MTU1 and MTU2 independently operate. In 32-bit phase counting mode, meanwhile, MTU1 and MTU2 jointly operate when the MTU1.TMDR3.LWA bit is set to 1. In 32-bit phase counting mode, the TCR, TCR2, TIOR, TIER, TMDR1, and TSR registers control MTU1. See Figure 19.43 for the procedure of selecting 32-bit phase counting mode.

Table 19.66 shows the correspondence between external clock pins and channels. In 32-bit phase counting mode, the TCR, TCR2, TIOR, TIER, TMDR1, and TSR registers are controlled by MTU1.

Table 19.66 Clock Input Pins in Phase Counting Mode

			External Clock Input Pins	
16-/32-bit mode	**Channel**	**TMDR3.PHCKSEL bit**	**A-Phase**	**B-Phase**
16-bit	MTU1	× (Don't care)	MTCLKA	MTCLKB
	MTU2	0	MTCLKA	MTCLKB
		1 (initial value)	MTCLKC	MTCLKD
32-bit	MTU1 and MTU2	0	MTCLKA	MTCLKB
		1 (initial value)	MTCLKC	MTCLKD

(1) Example of Phase Counting Mode Setting Procedure

Figure 19.30 shows an example of the phase counting mode setting procedure.

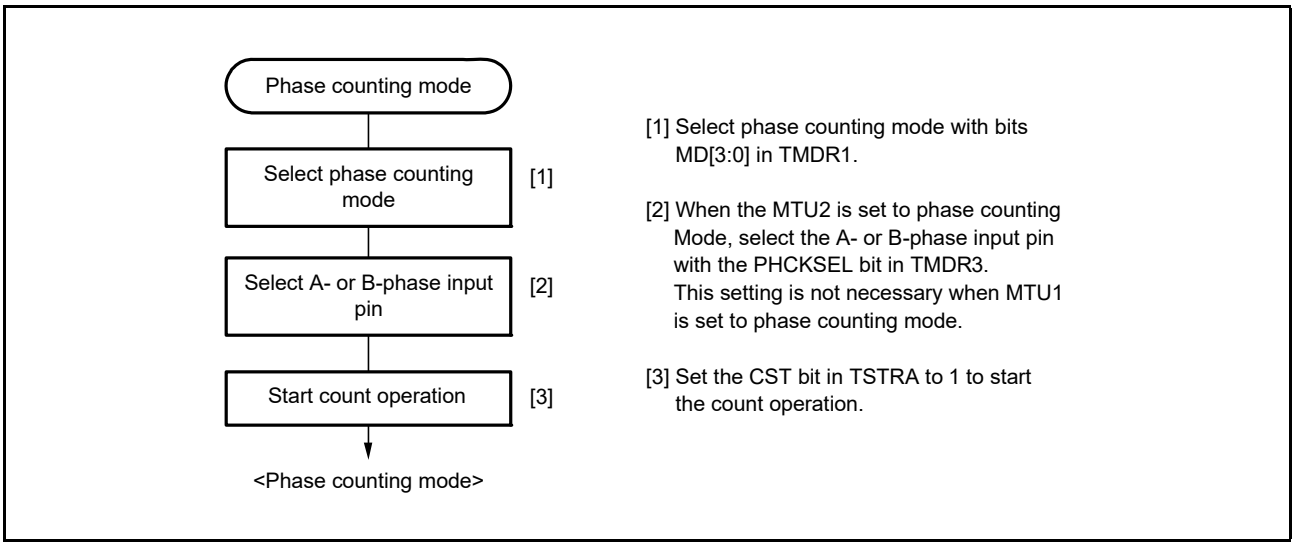


Figure 19.30 Example of Phase Counting Mode Setting Procedure

(2) Examples of Phase Counting Mode Operation

In phase counting mode, TCNT is incremented or decremented according to the phase difference between two external clocks. There are five modes according to the count conditions.
Operation in each mode is described by giving an example of 16-bit phase counting mode where the PHCKSEL bit in TMDR3 is 1 (the phase clock for MTU1 is MTCLKA or MTCLKB and that for MTU2 is MTCLKC or MTCLKD).

(a) Phase Counting Mode 1

Figure 19.31 shows an example of operation in phase counting mode 1, and Table 19.67 summarizes the TCNT up-/down-count conditions.

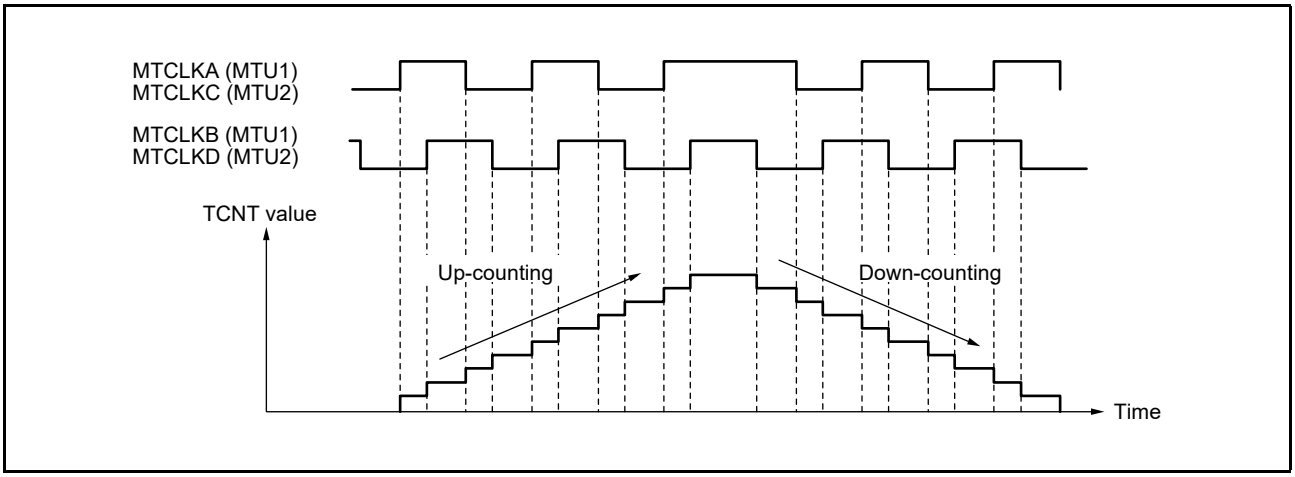


Figure 19.31 Example of Operation in Phase Counting Mode 1

Table 19.67 Up-/Down-Count Conditions in Phase Counting Mode 1

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	
↓	Low	

↑ : Rising edge

↓ : Falling edge

(b) Phase Counting Mode 2

Figure 19.32 to Figure 19.34 show the examples of operation in phase counting mode 2 and Table 19.68 summarizes the TCNT up- and down-counting conditions.

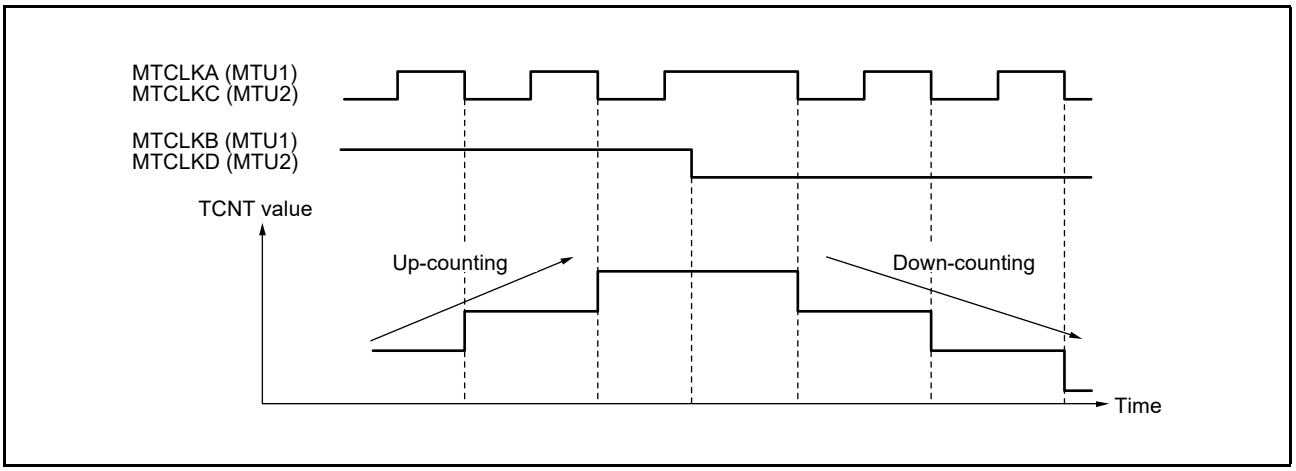


Figure 19.32 Example of Operation in Phase Counting Mode 2 (when MTUn.TCR2.PCB[1:0] is 00 (n = 1, 2))

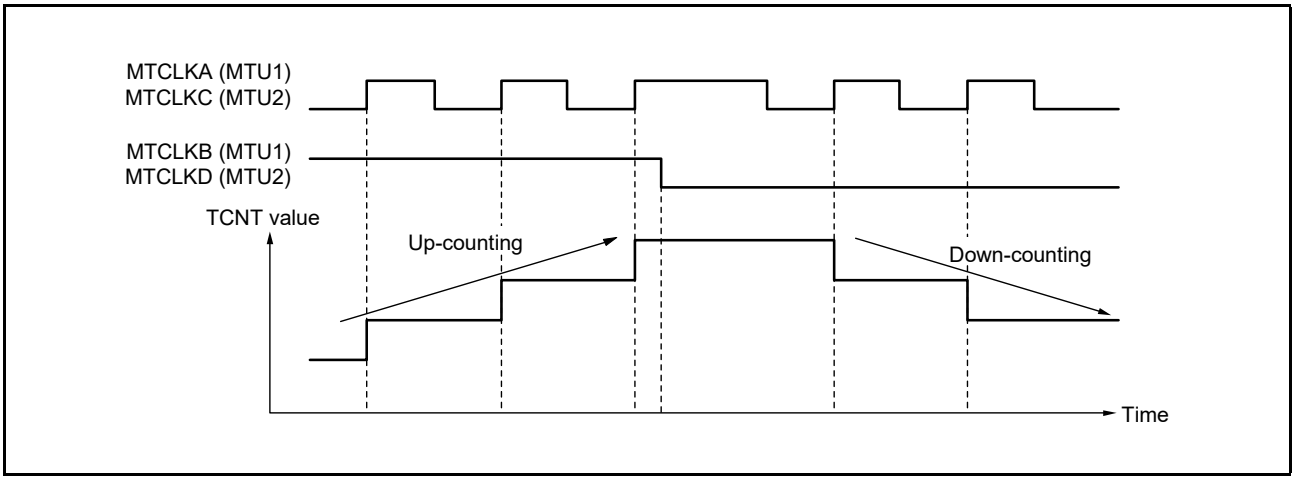


Figure 19.33 Example of Operation in Phase Counting Mode 2 (when MTUn.TCR2.PCB[1:0] is 01 (n = 1, 2))

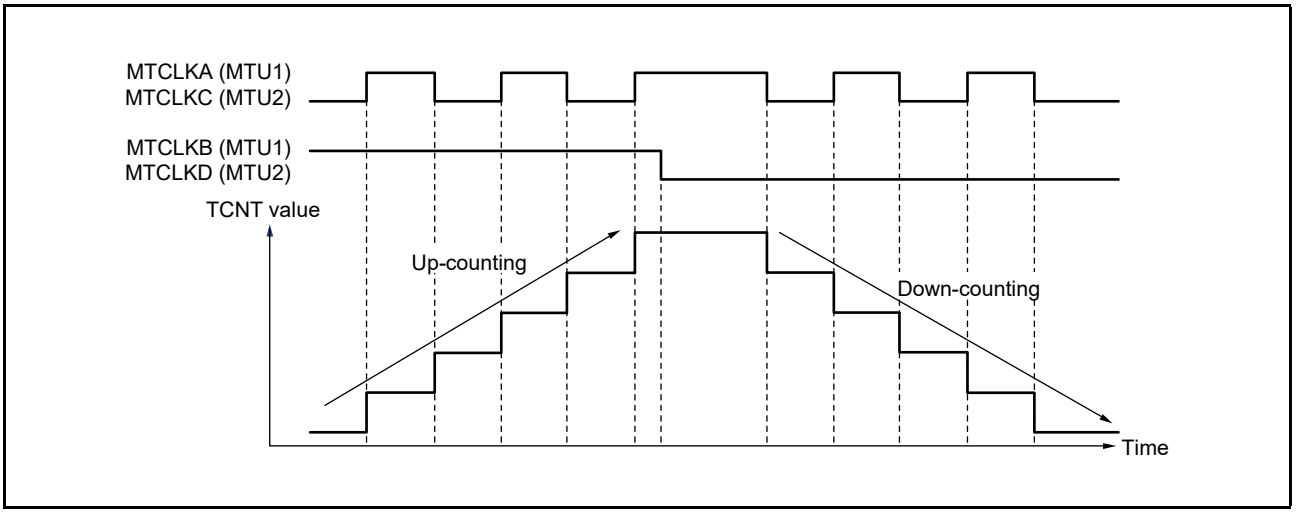


Figure 19.34 Example of Operation in Phase Counting Mode 2 (when MTUn.TCR2.PCB[1:0] is 1x (n = 1, 2))

Table 19.68 Up-/Down-Count Conditions in Phase Counting Mode 2

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
00	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	
	↓	Low	Down-counting
01	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	Down-counting
	↓	High	Not counted (Don't care)
	High	↓	
	Low	↑	
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)
1x	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	Down-counting
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	Up-counting
	↓	Low	Down-counting

↑ : Rising edge

↓ : Falling edge

(c) Phase Counting Mode 3

Figure 19.35 to Figure 19.37 show the examples of operation in phase counting mode 3 and Table 19.69 summarizes the TCNT up- and down-counting conditions.

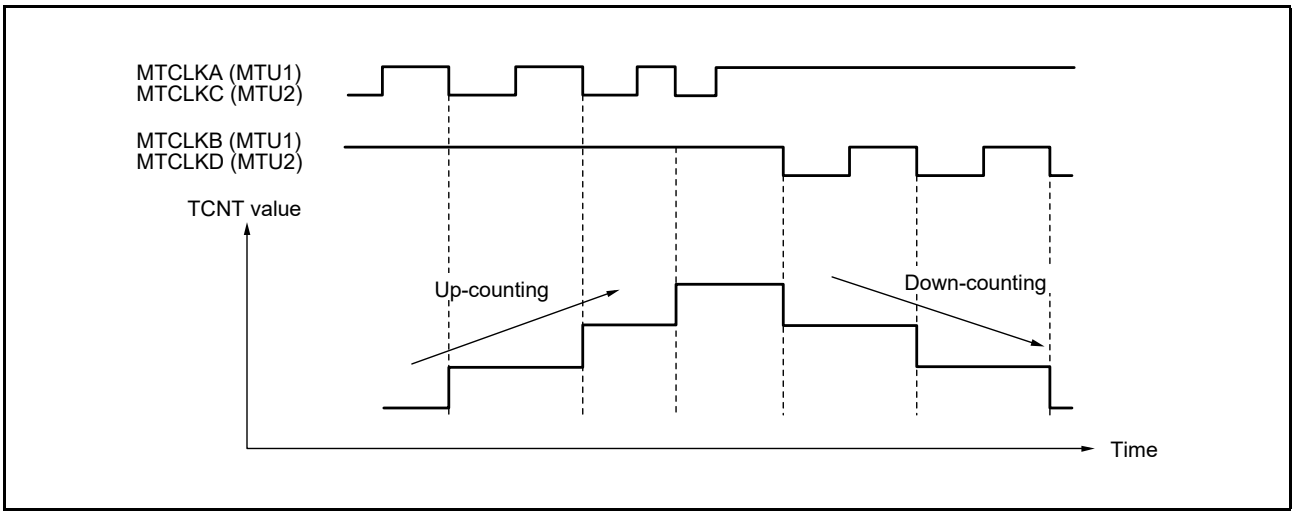


Figure 19.35 Example of Operation in Phase Counting Mode 3 (when MTUn.TCR2.PCB[1:0] is 00 (n = 1, 2))

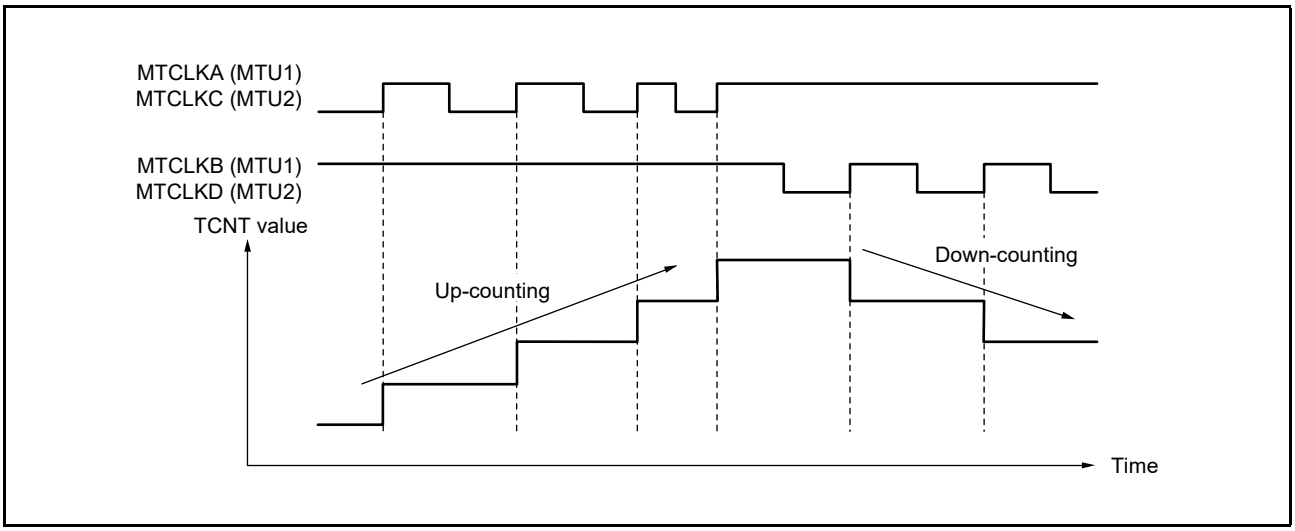


Figure 19.36 Example of Operation in Phase Counting Mode 3 (when MTUn.TCR2.PCB[1:0] is 01 (n = 1, 2))

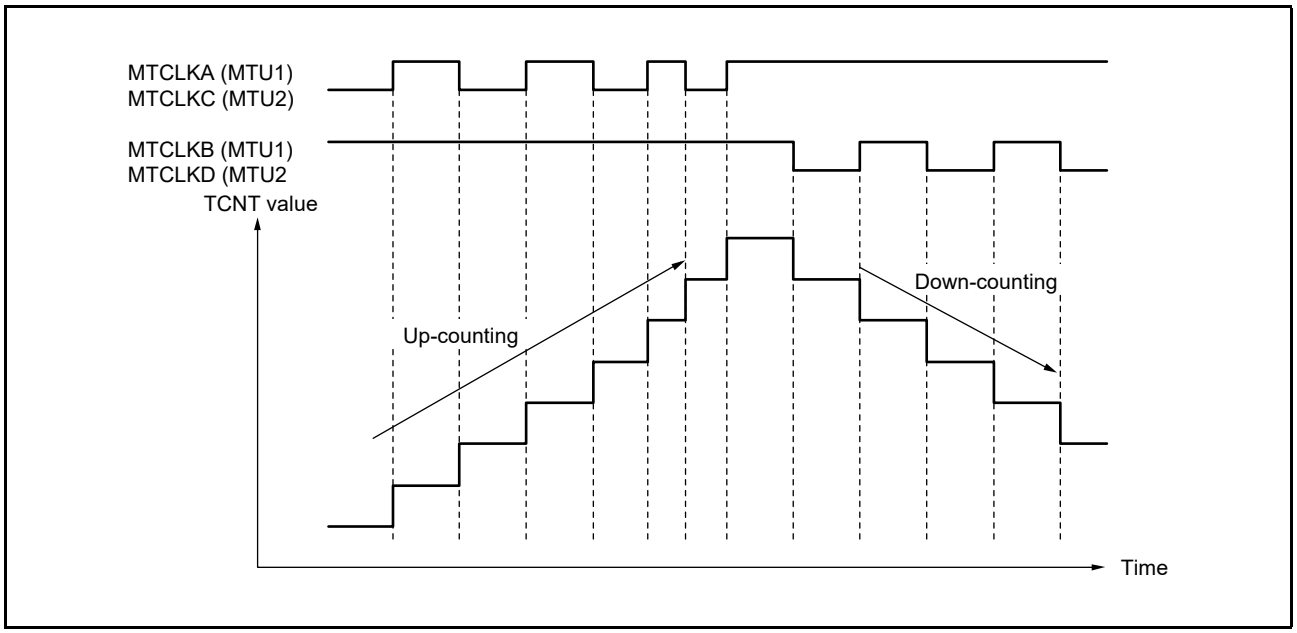


Figure 19.37 Example of Operation in Phase Counting Mode 3 (when MTUn.TCR2.PCB[1:0] is 1x (n = 1, 2))

Table 19.69 Up-/Down-Count Conditions in Phase Counting Mode 3

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
00	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Down-counting
	Low	↑	Not counted (Don't care)
	↑	High	
	↓	Low	
01	High	↑	Down-counting
	Low	↓	Not counted (Don't care)
	↑	Low	
	↓	High	
	High	↓	
	Low	↑	
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)
1x	High	↑	Down-counting
	Low	↓	Not counted (Don't care)
	↑	Low	
	↓	High	Up-counting
	High	↓	Down-counting
	Low	↑	Not counted (Don't care)
	↑	High	Up-counting
	↓	Low	Not counted (Don't care)

↑ : Rising edge

↓ : Falling edge

(d) Phase Counting Mode 4

Figure 19.38 shows an example of operation in phase counting mode 4, and Table 19.70 summarizes the TCNT up-/down-count conditions.

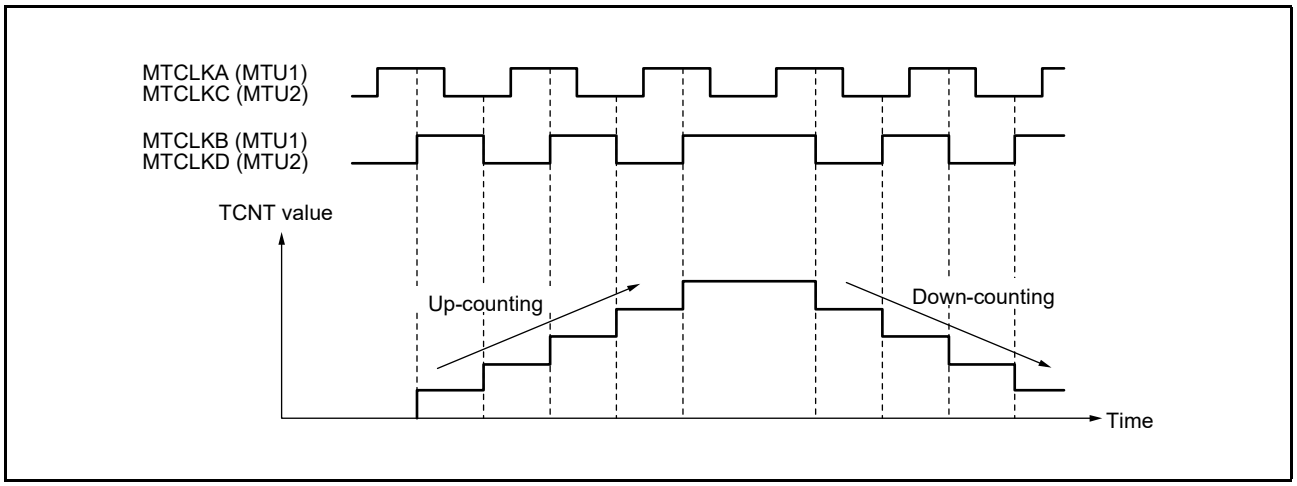


Figure 19.38 Example of Operation in Phase Counting Mode 4

Table 19.70 Up-/Down-Count Conditions in Phase Counting Mode 4

MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
High	↑	Up-counting
Low	↓	
↑	Low	Not counted (Don't care)
↓	High	
High	↓	Down-counting
Low	↑	
↑	High	Not counted (Don't care)
↓	Low	

↑ : Rising edge

↓ : Falling edge

(e) Phase Counting Mode 5

Figure 19.39 and Figure 19.40 show the examples of operation in phase counting mode 5 and Table 19.71 summarizes the TCNT up- and down-counting conditions.

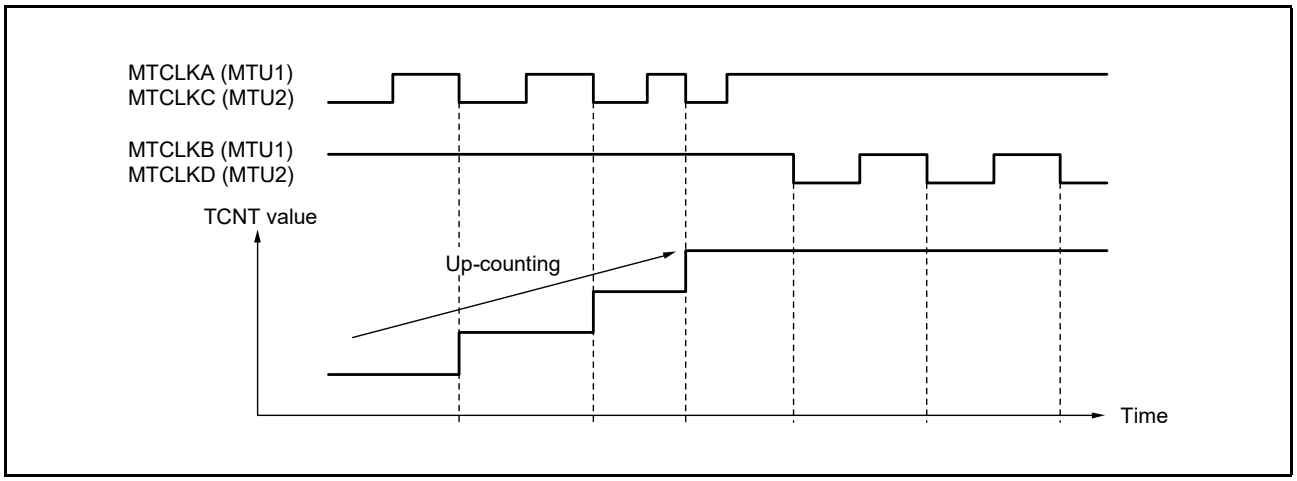


Figure 19.39 Example of Operation in Phase Counting Mode 5 (when MTUn.TCR2.PCB1 is 0 (n = 1, 2))

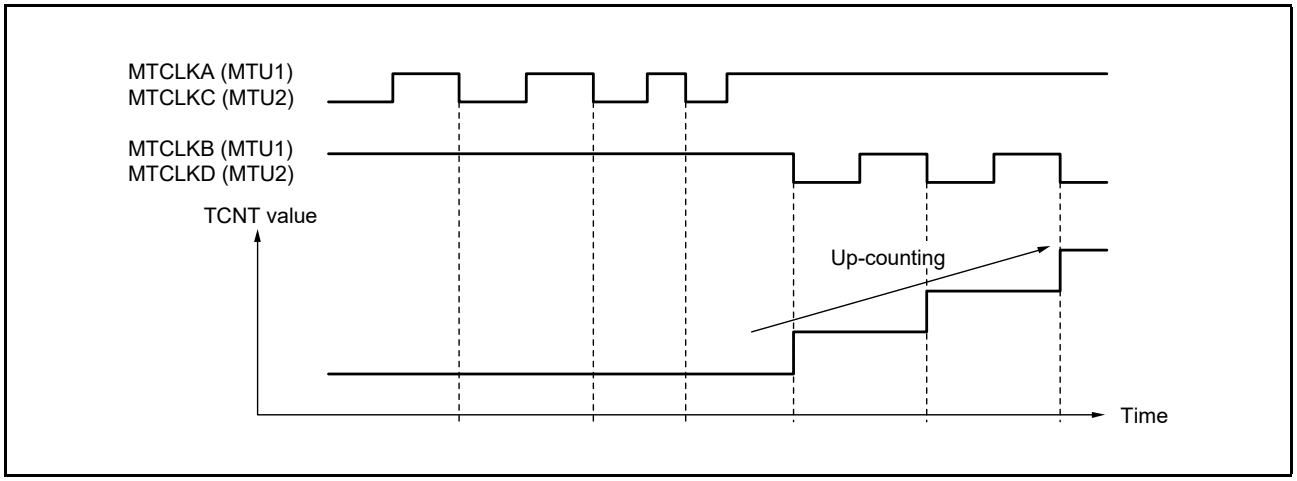


Figure 19.40 Example of Operation in Phase Counting Mode 5 (when MTUn.TCR2.PCB1 is 1 (n = 1, 2))

Table 19.71 Up-/Down-Count Conditions in Phase Counting Mode 5

PCB[1:0]	MTCLKA (MTU1) MTCLKC (MTU2)	MTCLKB (MTU1) MTCLKD (MTU2)	Operation
0x	High	↑	Not counted (Don't care)
	Low	↓	
	↑	Low	
	↓	High	Up-counting
	High	↓	Not counted (Don't care)
	Low	↑	
	↑	High	
	↓	Low	Up-counting
1x	High	↑	Not counted (Don't care)
	Low	↓	Up-counting
	↑	Low	Not counted (Don't care)
	↓	High	
	High	↓	Up-counting
	Low	↑	Not counted (Don't care)
	↑	High	
	↓	Low	

↑ : Rising edge

↓ : Falling edge

(3) 16-bit Phase Counting Mode Application Example

Figure 19.41 shows an example in which MTU1 is in phase counting mode, and MTU1 is coupled with MTU0 to input 2-phase encoder pulses of a servo motor in order to detect position or speed.
MTU1 is set to phase counting mode 1, and the encoder pulse A-phase and B-phase are input to MTCLKA and MTCLKB.
In MTU0, MTU0.TGRC compare match is specified as the TCNT clearing source and MTU0.TGRA and MTU0.TGRC are used for the compare match function and are set with the speed control cycle and position control cycle.
MTU0.TGRB is used for input capture, with MTU0.TGRB and MTU0.TGRD operating in buffer mode.
The MTU1 counter input clock is designated as the MTU0.TGRB input capture source, and the widths of 2-phase encoder 4-multiplication pulses are detected.
MTU1.TGRA and MTU1.TGRB for MTU1 are designated for the input capture function and MTU0.TGRA and MTU0.TGRC compare matches in MTU0 are selected as the input capture sources to store the up/down-counter values for the control cycles.
This procedure enables the accurate detection of position and speed.

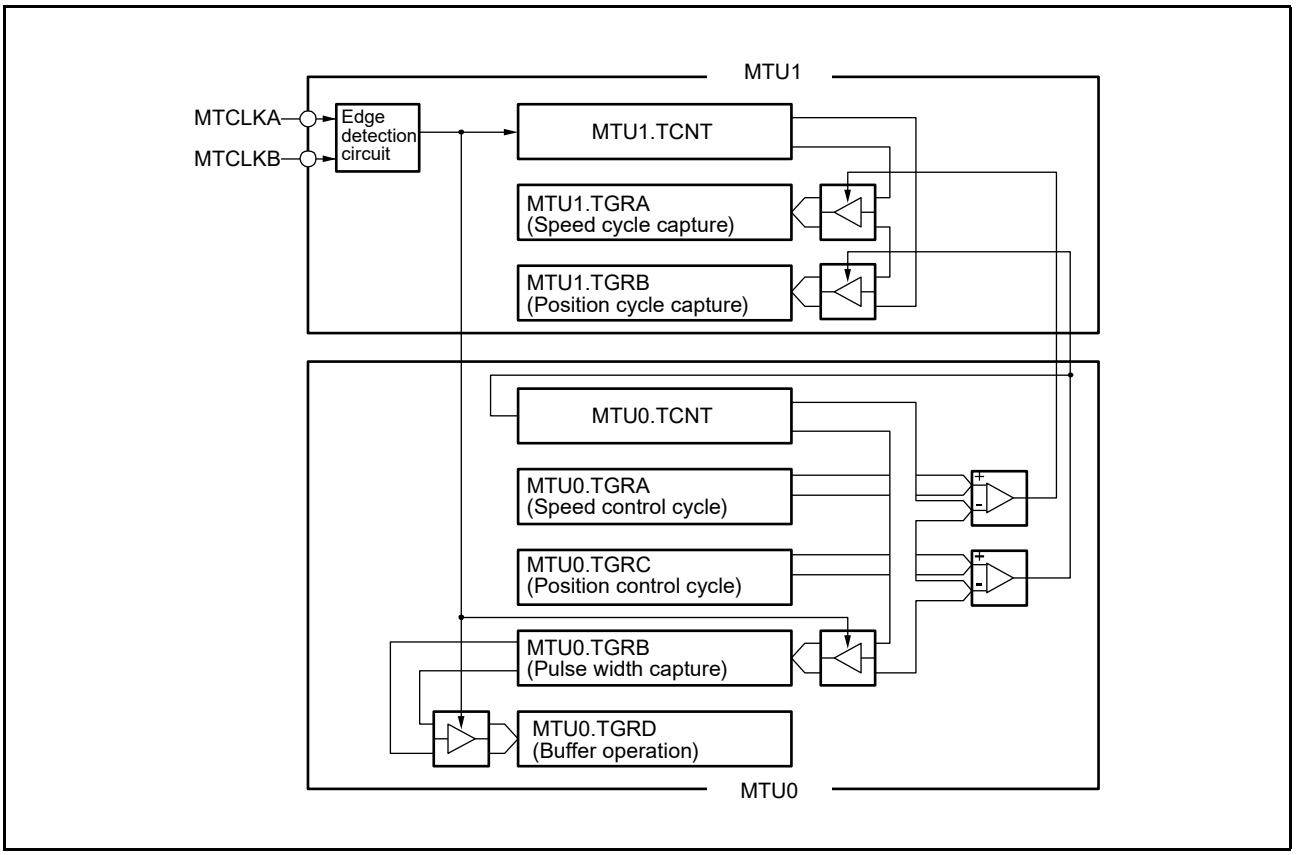


Figure 19.41 Phase Counting Mode Application Example

(4) 32-bit Phase Counting Mode Application Example

When MTU1 is set to phase counting mode by setting MTU1.TMDR3.LWA = 1, MTU1 and MTU2 are connected to operate in cascade connection 32-bit phase counting mode as shown in Figure 19.42. When this mode is used, the TCR, TCR2, TIOR, TIER, TMDR1, and TSR registers are controlled by MTU1 and the settings of MTU2 are disabled. Refer to Figure 19.43 for the procedure for setting cascade connection 32-bit phase counting mode.

In this mode, three-phase (A, B, and Z) signals can be input. As an encoder pulse signal, the external input phase clocks MTCLKA and MTCLKB or MTCLKC and MTCLKD can be selected for A-phase and B-phase, and MTIOC1A can be selected for Z-phase, respectively. Refer to Table 19.70 for selecting external clock input of A-phase and B-phase. A counter event is generated using an A-phase or B-phase pulse and counted by the 32-bit counter MTU1.TCNTLW.

An input capture can also be generated using a Z-phase signal; thus the angular velocity can be measured using the captured value in the general register (MTU1.TGRALW, MTU1.TGRBLW).

Furthermore, MTU8 can be used as a channel for measuring a control period interval, and a compare match signal can be output at a control period interval to the MTU1 and MTU2, which operate in cascade connection 32-bit phase counting mode. That is, a compare match signal of MTU8 is used as a capture signal of MTU1 and MTU2, and the number of A-phase and B-phase pulses for a control period can be measured.

When MTU0 or MTU5 is specified as the channel for measuring a Z-phase signal pulse, this compare match signal of MTU8.TGRC can be output as a capture signal or clear signal to MTU0 or MTU5, thus the Z-phase count at a control period interval can be measured.

In addition, a counter event signal of combined MTU1 and MTU2 can be used as a capture signal of MTU8.TGRD, and measurement can be performed including the intervals of A, B, or both phase pulses. In this case, the general register for measurement (MTU8.TGRD) should be set to a register for buffer operation.

Refer to section 19.3.4, Cascaded Operation, for details on the cascade connection function for connecting MTU1 and MTU2 in a mode other than cascade connection 32-bit phase counting mode.

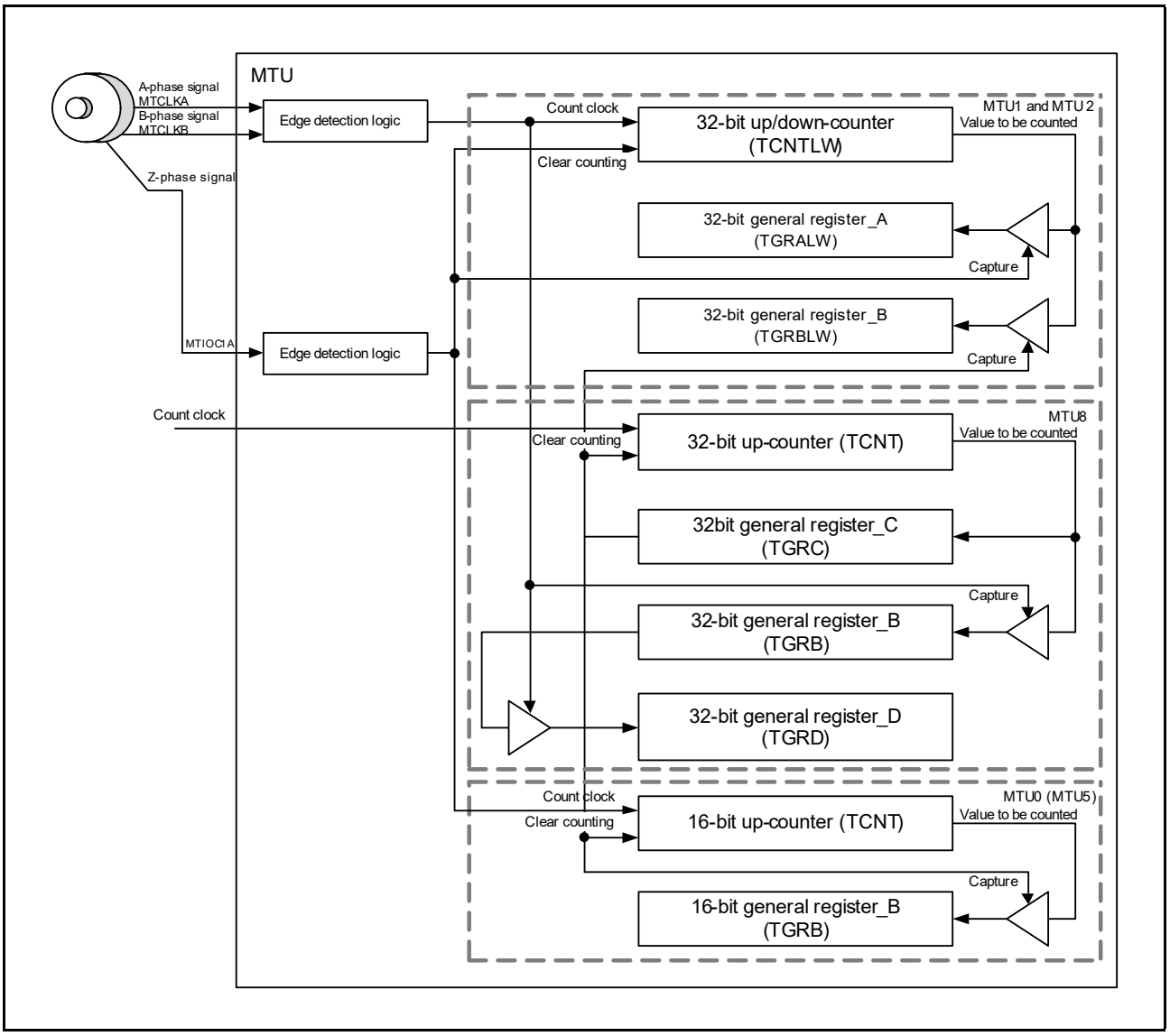
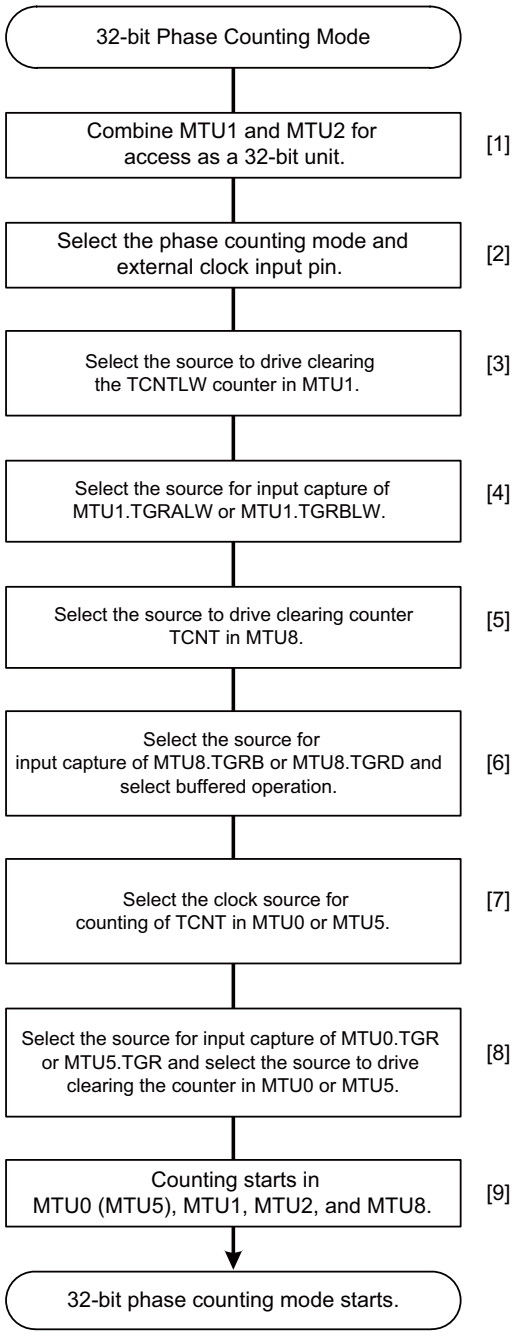


Figure 19.42 32-bit Phase Counting Mode Application Example



[1] Set the LWA bit in MTU1.TMDR3 to 1 and combine MTU1 and MTU2 for access as a 32-bit unit.

[2] Select phase counting mode with the MD[3:0] bits in MTU1.TMDR1 and select the external clock input pin with the PHCKSEL bits in MTU1.TMDR3.

[3] Set the CCLR[2:0] bits in MTU1.TCR to 001b to select input capture of MTU1.TGRALW as the source of the signal to drive clearing counter TCNTLW in MTU1.

[4] Set the IOA[3:0] bits in MTU1.TIOR to select the effective edge (rising, falling or both) of the signal produced by input capture of TGRALW in MTU1. After that, set the IOB[3:0] bits in MTU1.TIOR to 1110b to select the compare match signal of MTU8.TGRC as the source to drive input capture of MTU1.TGRBLW.

[5] Set the CCLR[2:0] bits in MTU8.TCR to 101b to select the compare match signal of MTU8.TGRC as the source to drive clearing counter TCNT in MTU8.

[6] Select the source for input capture of MTU8.TGRB as the clock source for counting of TCNTLW in MTU1 by setting the IOB[3:0] bits in MTU8.TIORH to 1110b. At the same time, select buffered operation for TGRB and TGRD by setting the BFB bit in MTU8.TMDR1 to 1.

[7] Set the TPSC2[2:0] bits in MTU0.TCR2 to 111b to select the MTIOC1A pin as the clock source for counting of TCNT in MTU0.
(When using TCNT in MTU5, set the TPSC2[2:0] bits in MTU5.TCR2 to 111b).

[8] Select the compare match signal of MTU8.TGRC as the source to drive input capture of MTU0.TGRA by setting the IOA[3:0] bits in MTU0.TIORH to 1110b.
(When using TCNT in MTU5, set the TIORU, TIORV, or TIORW bit in MTU5 is set to 10100b).
After that, select input capture of MTU0.TGRA as the source to drive clearing counter TCNT in MTU0 by setting the CCLR[2:0] bits in MTU0.TCR to 001b.

[9] Start counting in MTU0, MTU1, MTU2, and MTU8 by setting the TSTRA bit to 00001111b.
(When using TCNT in MTU5, set the counter corresponding to TSTR in MTU5 to 1).

Note: When the LWA bit in MTU1.TMDR3 is set to 1, the TCR, TCR2, TMDR1, and TIOR registers in MTU1 are effective in controlling cascaded operation. In this case, the settings of these registers in MTU2 are ignored.

Figure 19.43 Procedure of Selecting 32-bit Phase Counting Mode

19.3.7 Reset-Synchronized PWM Mode

In reset-synchronized PWM mode, three phases of positive and negative PWM waveforms (six phases in total) that share a common wave transition point can be output by combining MTU3 and MTU4 and MTU6 and MTU7.
When set for reset-synchronized PWM mode, the MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D pins function as PWM output pins and timer counters 3 and 6 (MTU3.TCNT and MTU6.TCNT) functions as an up-counter.
Table 19.72 shows the PWM output pins used. Table 19.73 shows the settings of the registers.

Table 19.72 Output Pins for Reset-Synchronized PWM Mode

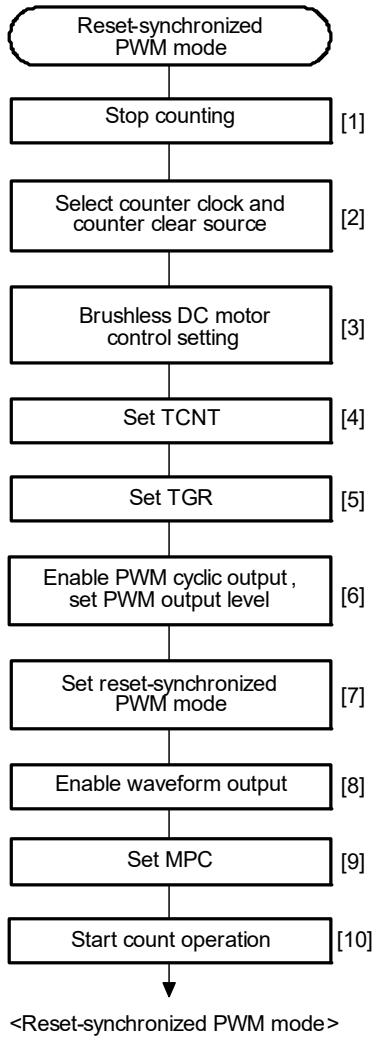
Channel	Output Pin	Description
MTU3	MTIOC3B	PWM output pin 1
	MTIOC3D	PWM output pin 1' (negative-phase waveform of PWM output 1)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (negative-phase waveform of PWM output 2)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (negative-phase waveform of PWM output 3)
MTU6	MTIOC6B	PWM output pin 4
	MTIOC6D	PWM output pin 4' (negative-phase waveform of PWM output 4)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (negative-phase waveform of PWM output 5)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (negative-phase waveform of PWM output 6)

Table 19.73 Register Settings for Reset-Synchronized PWM Mode

Register	Setting
MTU3.TCNT	Initial setting (0000h)
MTU4.TCNT	Initial setting (0000h)
MTU3.TGRA	Set the count cycle for MTU3.TCNT
MTU3.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC3B and MTIOC3D pins
MTU4.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC4A and MTIOC4C pins
MTU4.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC4B and MTIOC4D pins
MTU6.TCNT	Initial setting (0000h)
MTU7.TCNT	Initial setting (0000h)
MTU6.TGRA	Set the count cycle for MTU6.TCNT
MTU6.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC6B and MTIOC6D pins
MTU7.TGRA	Set the transition point of the PWM waveform to be output from the MTIOC7A and MTIOC7C pins
MTU7.TGRB	Set the transition point of the PWM waveform to be output from the MTIOC7B and MTIOC7D pins

(1) Example of Procedure for Setting Reset-Synchronized PWM Mode

Figure 19.44 shows an example of procedure for setting the reset-synchronized PWM mode.



[1] Clear the CST3 and CST4 bits in TSTRA to 0 to stop the TCNT operation. Specify the reset-synchronized PWM mode while MTU3.TCNT and MTU4.TCNT are stopped.

[2] Set bits TPSC[2:0] and CKEG[1:0] in MTU3.TCR to select the counter clock and clock edge for MTU3. Set bits CCLR[2:0] to select TGRA compare match as a counter clear source.

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCRA) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set MTU3.TCNT and MTU4.TCNT to 0000h.

[5] MTU3.TGRA is the cycle register. Set the waveform cycle value in MTU3.TGRA. Set the transition timing of the PWM output waveforms in MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB. The set value should be within the range of compare match between MTU3.TCNT and MTU3.TGRA.

$X \leq$ MTU3.TGRA (X: Set value)

[6] Enable or disable toggle output synchronized with the PMW cycle using bit PSYE in TOCR1A, and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBRA as a buffer for TOCR2A, see Figure 19.3.

[7] Set bits MD[3:0] in MTU3.TMDR1 to 1000b to select the reset-synchronized PWM mode. In addition, specify the buffer operation of the MTU3.TGRA (BFA = 1) and MTU3.TGRC (BFB = 1) when necessary. Set the MTU4.TMDR1 to the initial value (normal operation; BFA = 0 and BFB = 0).

[8] Set the enabling/disabling of the PWM waveform output pin in TOERA.

[9] Set the port control register and the port I/O register.

[10] Set the CST3 bit in the TSTRA to 1 to start the count operation.

Note: The output waveform starts to toggle at the point of MTU3.TCNT = MTU3.TGRA = X by setting X = MTU3.TGRA, i.e., cycle = duty ratio.

Figure 19.44 Procedure for Selecting Reset-Synchronized PWM Mode

(2) Example of Reset-Synchronized PWM Mode Operation

Figure 19.45 shows an example of operation in the reset-synchronized PWM mode.
MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) operate as up-counters. The counters are cleared when a compare match occurs between MTU3.TCNT (MTU6.TCNT) and MTU3.TGRA (MTU6.TGRA), and then begin incrementing from 0000h. The output from the PWM pins toggles every time a compare match occurs in MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB) and the counters are cleared.

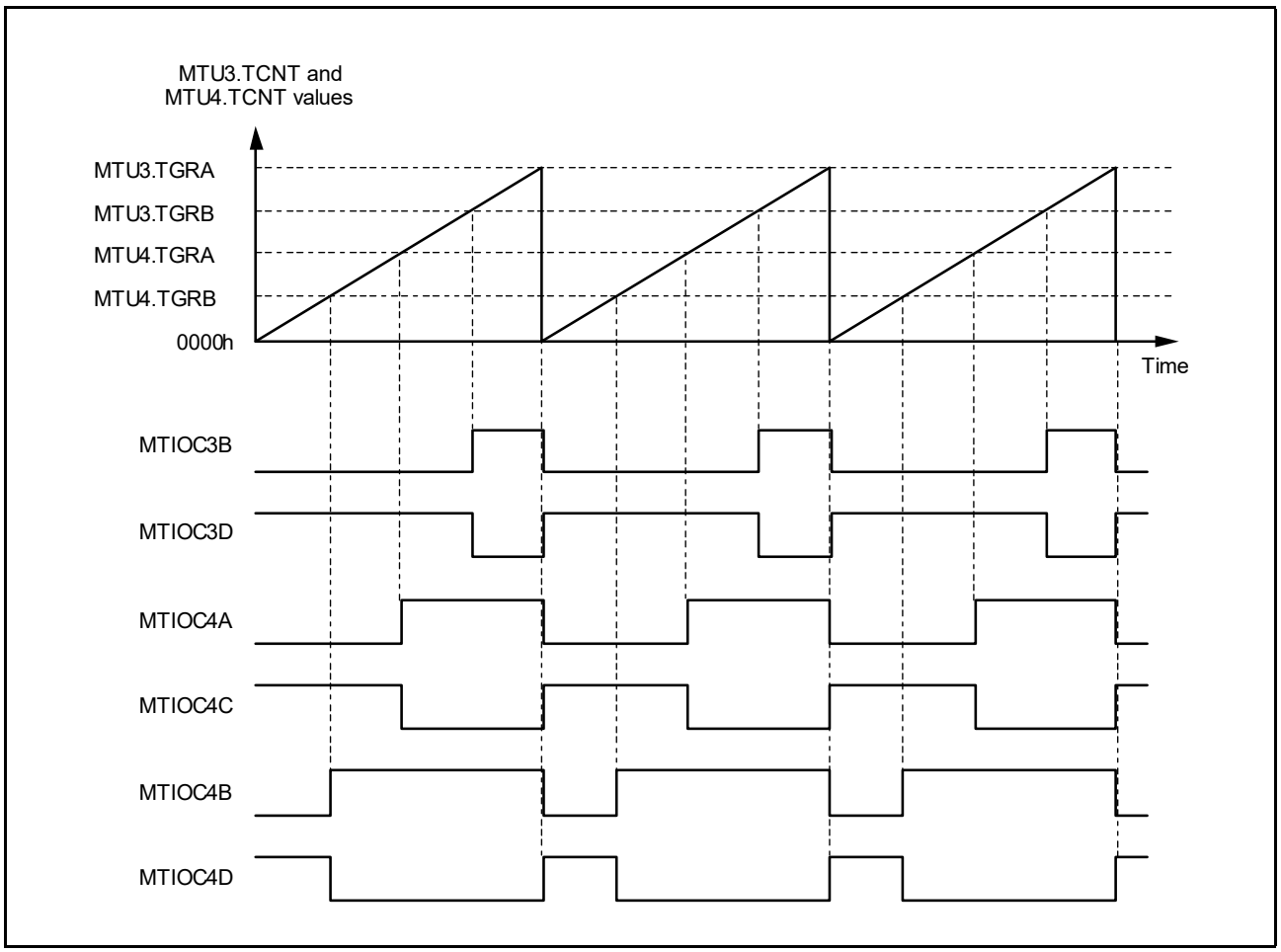


Figure 19.45 Example of Reset-Synchronized PWM Mode Operation (When TOCR1A's OLSN = 1 and OLSP = 1 in MTU3 and MTU4)

19.3.8 Complementary PWM Mode

In complementary PWM mode, the dead time can be set for the output PWM waveforms. The dead time is a period during which both the upper and lower arm transistors are set to the non-active level to prevent a short circuit of the arm. PWM waveforms can be output in six positive and inverse phases (12 phases in total) with dead time by combining MTU3 and MTU4 and MTU6 and MTU7. PWM waveforms without dead time can also be output.
In complementary PWM mode, MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D pins function as PWM output pins, and the MTIOC3A and MTIOC6A pins can be set for toggle output synchronized with the PWM cycle.
MTU3.TCNT, MTU4.TCNT, MTU6.TCNT, and MTU7.TCNT function as up/down-counters.
Table 19.74 shows the PWM output pins used. Table 19.75 shows the settings of the registers used.
A function to directly cut off the PWM output by using an external signal is supported as a port function.

Table 19.74 Output Pins for Complementary PWM Mode

Channel	Output Pin	Description
MTU3	MTIOC3A	Toggle output synchronized with PWM cycle (or I/O port)
	MTIOC3B	PWM output pin 1
	MTIOC3C	I/O port*1
	MTIOC3D	PWM output pin 1' (Negative-phase waveform of PWM output 1 is output.)
MTU4	MTIOC4A	PWM output pin 2
	MTIOC4C	PWM output pin 2' (Negative-phase waveform of PWM output 2 is output.)
	MTIOC4B	PWM output pin 3
	MTIOC4D	PWM output pin 3' (Negative-phase waveform of PWM output 3 is output.)
MTU6	MTIOC6A	Toggle output synchronized with PWM cycle (or I/O port)
	MTIOC6B	PWM output pin 4
	MTIOC6C	I/O port*1
	MTIOC6D	PWM output pin 4' (non-overlapping negative-phase waveform of PWM output 4; PWM output without non-overlapping interval is also available)
MTU7	MTIOC7A	PWM output pin 5
	MTIOC7C	PWM output pin 5' (non-overlapping negative-phase waveform of PWM output 5; PWM output without non-overlapping interval is also available)
	MTIOC7B	PWM output pin 6
	MTIOC7D	PWM output pin 6' (non-overlapping negative-phase waveform of PWM output 6; PWM output without non-overlapping interval is also available)

Note 1. Avoid setting the MTIOC3C and MTIOC6C pins as timer I/O pins in complementary PWM mode.

Table 19.75 Register Settings for Complementary PWM Mode (1/2)

Channel	Counter/ Register	Description	Read/Write from CPU
MTU3	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERA setting*1
	TGRA	Set MTU3.TCNT upper limit value (1/2 carrier cycle + dead time)	Maskable by TRWERA setting*1
	TGRB	PWM output 1 compare register	Maskable by TRWERA setting*1
	TGRC	MTU3.TGRA buffer register	Readable/writable
	TGRD	PWM output 1/MTU3.TGRB buffer register	Readable/writable
	TGRE	MTU3.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU4	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERA setting*1
	TGRA	PWM output 2 compare register	Maskable by TRWERA setting*1
	TGRB	PWM output 3 compare register	Maskable by TRWERA setting*1
	TGRC	PWM output 2/MTU4.TGRA buffer register	Readable/writable
	TGRD	PWM output 3/MTU4.TGRB buffer register	Readable/writable
	TGRE	MTU4.TGRA buffer register B (when double buffer function is used)	Readable/writable
	TGRF	MTU4.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU6	TCNT	Starts up-counting from the value set in the dead time register	Maskable by TRWERB setting*2
	TGRA	Set MTU6.TCNT upper limit value (1/2 carrier cycle + dead time)	Maskable by TRWERB setting*2
	TGRB	PWM output 4 compare register	Maskable by TRWERB setting*2
	TGRC	MTU6.TGRA buffer register	Readable/writable
	TGRD	PWM output 4/MTU6.TGRB buffer register	Readable/writable
	TGRE	MTU6.TGRB buffer register B (when double buffer function is used)	Readable/writable
MTU7	TCNT	Starts up-counting after being initialized to 0000h	Maskable by TRWERB setting*2
	TGRA	PWM output 5 compare register	Maskable by TRWERB setting*2
	TGRB	PWM output 6 compare register	Maskable by TRWERB setting*2
	TGRC	PWM output 5/MTU7.TGRA buffer register	Readable/writable
	TGRD	PWM output 6/MTU7.TGRB buffer register	Readable/writable
	TGRE	MTU7.TGRA buffer register B (when double buffer function is used)	Readable/writable
	TGRF	MTU7.TGRB buffer register B (when double buffer function is used)	Readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

Table 19.75 Register Settings for Complementary PWM Mode (2/2)

Channel	Counter/ Register	Description	Read/Write from CPU
Timer dead time data register A (TDDRA)		Set MTU4.TCNT and MTU3.TCNT offset value (dead time value)	Maskable by TRWERA setting*1
Timer dead time data register B (TDDRB)		Set MTU7.TCNT and MTU6.TCNT offset value (dead time value)	Maskable by TRWERB setting*2
Timer cycle data register A (TCDRA)		Set MTU4.TCNT upper limit value (1/2 carrier cycle)	Maskable by TRWERA setting*1
Timer cycle data register B (TCDRB)		Set MTU7.TCNT upper limit value (1/2 carrier cycle)	Maskable by TRWERB setting*2
Timer cycle buffer register A (TCBRA)		TCDRA buffer register	Readable/writable
Timer cycle buffer register B (TCBRB)		TCDRB buffer register	Readable/writable
Subcounter A (TCNTSA)		Subcounter A for dead time generation	Read-only
Subcounter B (TCNTSB)		Subcounter B for dead time generation	Read-only
Temporary register 1A (TEMP1A)		PWM output 1/MTU3.TGRB temporary register A	Not readable/writable
Temporary register 1B (TEMP1B)		PWM output 1/MTU3.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 2A (TEMP2A)		PWM output 2/MTU4.TGRA temporary register A	Not readable/writable
Temporary register 2B (TEMP2B)		PWM output 2/MTU4.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 3A (TEMP3A)		PWM output 3/MTU4.TGRB temporary register A	Not readable/writable
Temporary register 3B (TEMP3B)		PWM output 3/MTU4.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 4A (TEMP4A)		PWM output 4/MTU6.TGRB temporary register A	Not readable/writable
Temporary register 4B (TEMP4B)		PWM output 4/MTU6.TGRB temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 5A (TEMP5A)		PWM output 5/MTU7.TGRA temporary register A	Not readable/writable
Temporary register 5B (TEMP5B)		PWM output 5/MTU7.TGRA temporary register B (when double buffer function is used)	Not readable/writable
Temporary register 6A (TEMP6A)		PWM output 6/MTU7.TGRB temporary register A	Not readable/writable
Temporary register 6B (TEMP6B)		PWM output 6/MTU7.TGRB temporary register B (when double buffer function is used)	Not readable/writable

Note 1. Access can be enabled or disabled according to the setting in TRWERA (timer read/write enable register A).
Note 2. Access can be enabled or disabled according to the setting in TRWERB (timer read/write enable register B).

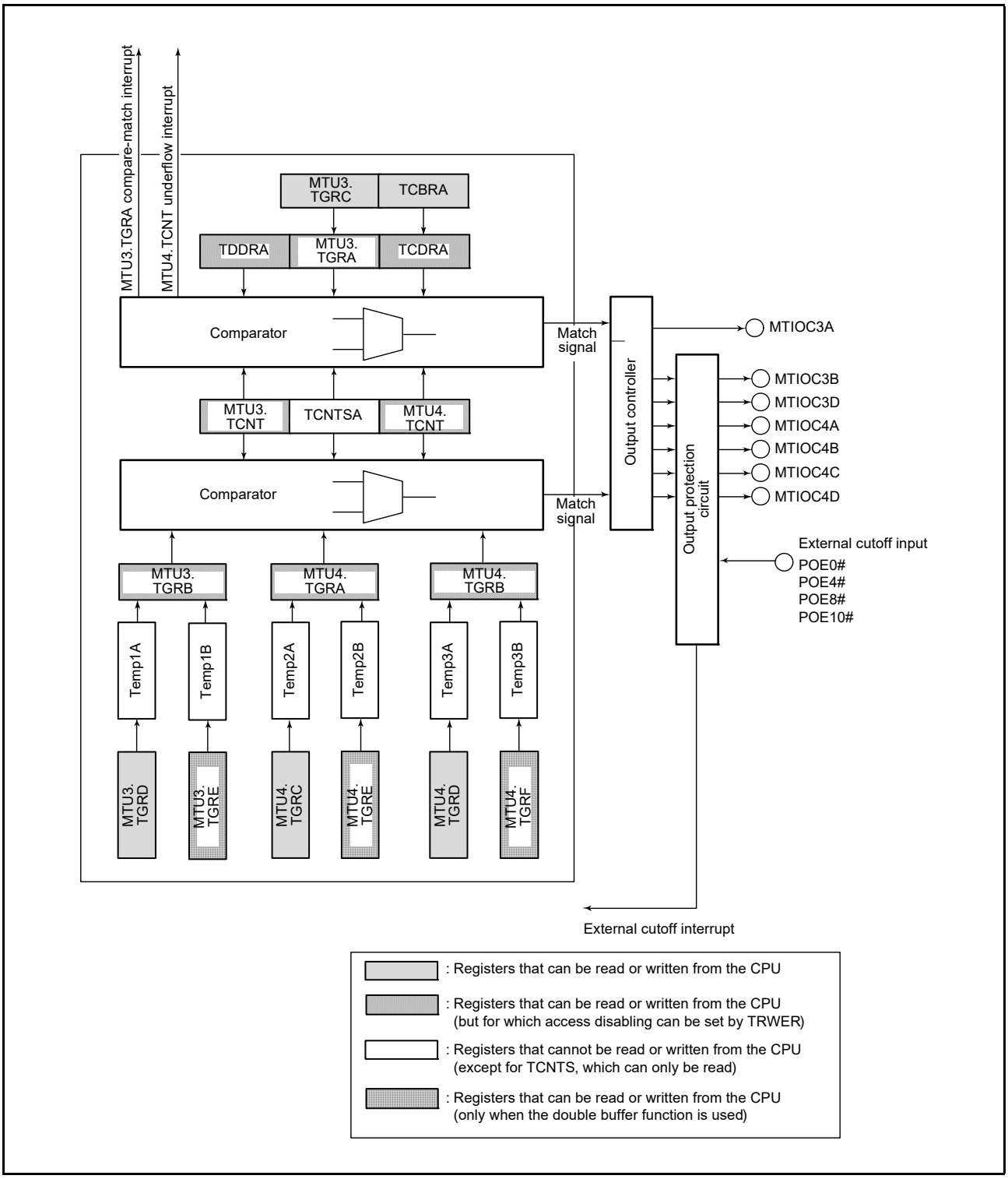


Figure 19.46 Block Diagram of MTU3 and MTU4 in Complementary PWM Mode

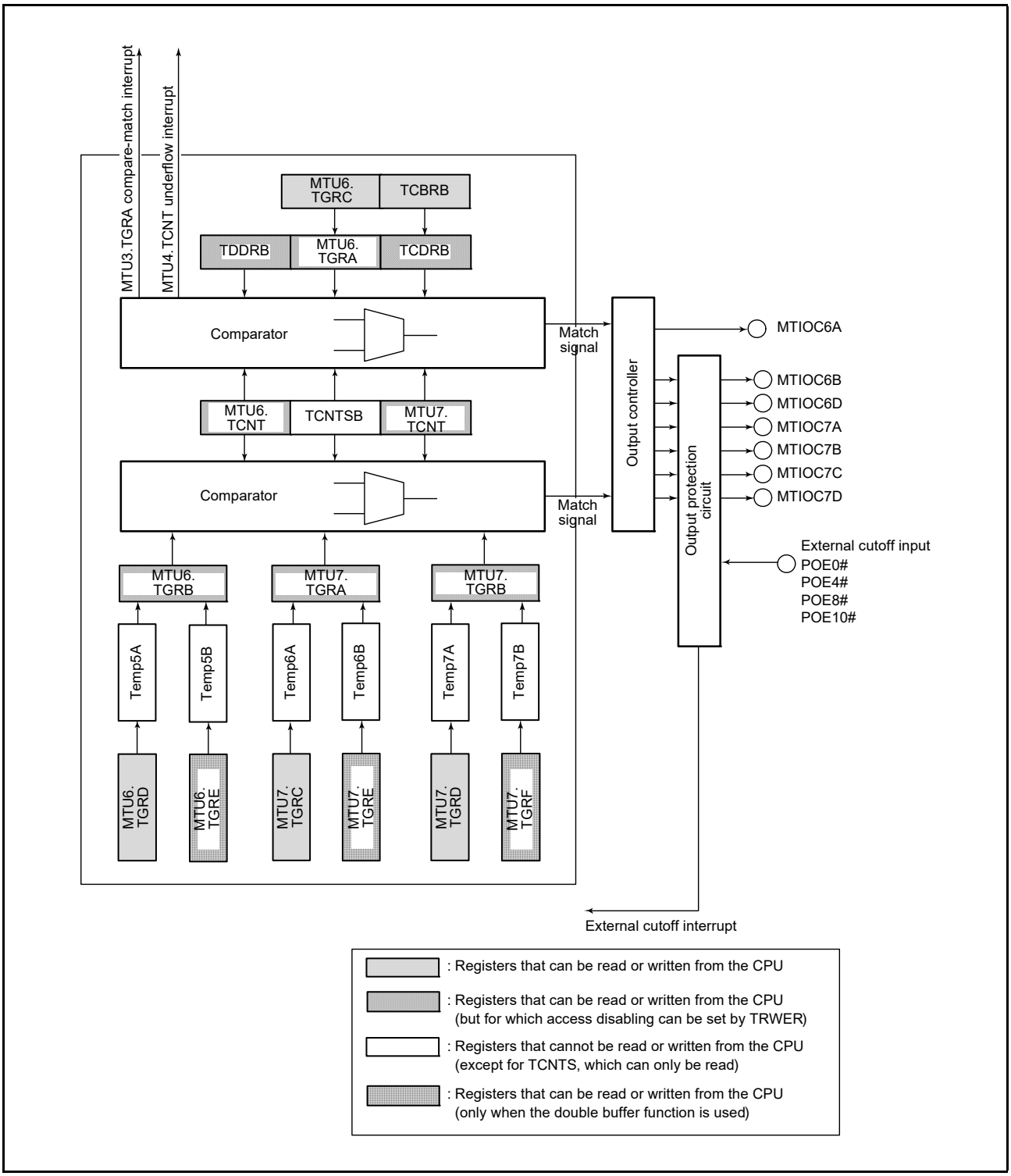
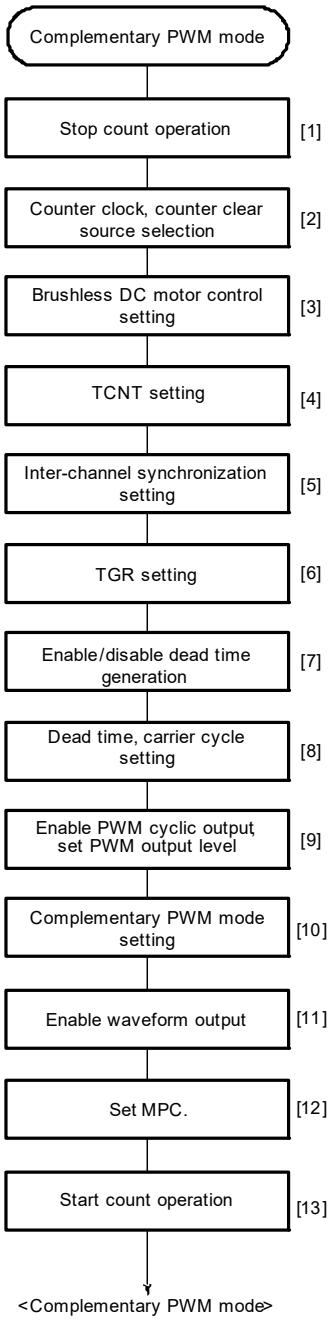


Figure 19.47 Block Diagram of MTU6 and MTU7 in Complementary PWM Mode

(1) Example of Complementary PWM Mode Setting Procedure

Figure 19.48 shows an example of the complementary PWM mode setting procedure.



[1] Clear bits CST3 and CST4 in the timer start register (TSTRA) to 0 to stop timer counter (TCNT) operation. Specify complementary PWM mode while MTU3.TCNT and MTU4.TCNT are stopped.

[2] Set the same counter clock and clock edge for MTU3 and MTU4 with bits TPSC[2:0] and bits CKEG[1:0] in the timer control register (TCR). Use bits CCLR[2:0] to set synchronous clearing only when restarting by synchronous clearing with another channel during complementary PWM mode operation.

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCRA) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set the dead time in MTU3.TCNT. Set MTU4.TCNT to 0000h.

[5] Set only when restarting by synchronous clearing with another channel during complementary PWM mode operation. In this case, synchronize the channel generating the synchronous clear with MTU3 and MTU4 using the timer synchronous register (TSYRA).

[6] Set the output PWM duty cycles in the duty registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB) and buffer registers (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD). Be sure to set the same value in each pair of duty register and buffer register. Only when using the double buffer function, set the output PWM duty value - 1 in the buffer registers (MTU3.TGRDE, MTU4.TGRCE, MTU4.TGRDF).

[7] This setting is necessary only when no dead time should be generated. Make appropriate settings in the timer dead time enable register (TDERA) so that no dead time is generated.

[8] Set the dead time in the dead time register (TDDRA), 1/2 the carrier cycle in the timer cycle data register (TCDRA) and timer cycle buffer register (TCBRA), and 1/2 the carrier cycle plus the dead time in MTU3. TGRA and MTU3.TGRC. When no dead time generation is selected, set 1 in TDDRA and 1/2 the carrier cycle + 1 in MTU3.TGRA and MTU3.TGRC.

[9] Enable or disable toggle output synchronized with the PWM cycle using bit PSYE in the timer output control register 1 (TOCR1A), and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBRA as a buffer for TOCR2A, see Figure 19.3.

[10] Select complementary PWM mode in the timer mode register1 (MTU3.TMDR1). In addition, specify the buffer operation of the MTU3.TGRA (BFA = 1) and MTU3.TGRC (BFB = 1) when necessary. Enable the double buffer operation with the TMDR2 register only when the double buffer function is used.

[11] Set enabling/disabling of PWM waveform output pin output in the timer output master enable register (TOERA).

[12] Set the MPC and port mode registers (PMR) of the I/O ports.

[13] Set bits CST3 and CST4 in TSTRA to 1 simultaneously to start the count operation.

Figure 19.48 Example of Complementary PWM Mode Setting Procedure

(2) Outline of Complementary PWM Mode Operation

In complementary PWM mode, six waveforms of three-phase PWM can be output. Figure 19.49 illustrates counter operation in complementary PWM mode (MTU3 and MTU4), and Figure 19.50 shows an example of operation in complementary PWM mode.

(a) Counter Operation

In complementary PWM mode, three counters—MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) —in each unit perform up-/down-count operations.
MTU3.TCNT (MTU6.TCNT) is automatically initialized to the value set in TDDRA (TDDRB) when complementary PWM mode is selected and the CST bit in TSTRA (TSTRB) is 0. When the CST bit is set to 1, MTU3.TCNT (MTU6.TCNT) counts up to the value set in MTU3.TGRA (MTU6.TGRA), then switches to down-counting when it matches MTU3.TGRA (MTU6.TGRA). When the MTU4.TCNT (MTU7.TCNT) value matches 0000h, MTU3.TCNT (MTU6.TCNT) switches to up-counting, and the operation is repeated in this way.
MTU4.TCNT (MTU7.TCNT) should be initialized to 0000h after a reset. When the CST bit is set to 1, MTU4.TCNT (MTU7.TCNT) counts up in synchronization with MTU3.TCNT (MTU6.TCNT), and switches to down-counting when MTU3.TCNT (MTU6.TCNT) matches MTU3.TGRA (MTU6.TGRA). On reaching 0000h, MTU4.TCNT (MTU7.TCNT) switches to up-counting, and the operation is repeated in this way.
TCNTSA (TCNTSB) is a read-only counter. It does not need to be initialized after a reset. In counting up by MTU3.TCNT and MTU4.TCNT (or MTU6.TCNT and MTU7.TCNT), MTU3.TCNT (or MTU6.TCNT) starts counting up when it matches TCDRA (or TCDRB) and switches to counting down when it matches MTU3.TGRA (or MTU6.TGRA).
Furthermore, when MTU4.TCNT (or MTU7.TCNT) matches TDDRA (or TDDRB), TCNTSA (or TCNTSB) is set to the value in MTU3.TGRA (or MTU6.TGRA) and counting is stopped.When MTU4.TCNT (MTU7.TCNT) matches TDDRA (TDDRB) during down-counting of MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT), TCNTSA (TCNTSB) starts up-counting, and when MTU4.TCNT (MTU7.TCNT) matches 0000h, the operation switches to down-counting.
When MTU3.TCNT (MTU6.TCNT) matches TCDRA (TCDRB), TCNTSA (TCNTSB) is cleared to 0000h and stops counting.
TCNTSA (TCNTSB) is compared with the compare register and temporary register, in which the PWM duty is specified, only during the count operation.

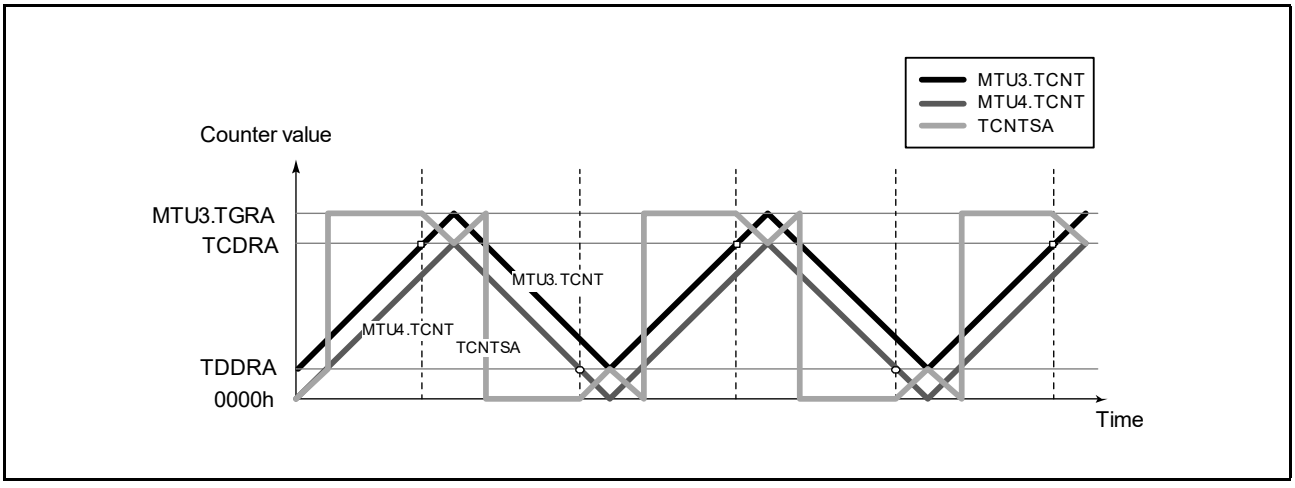


Figure 19.49 Counter Operation in Complementary PWM Mode (MTU3, MTU4)

(b) Register Operation

In complementary PWM mode, nine registers (compare registers, buffer registers, and temporary registers) are used for each unit. Figure 19.50 shows an example of operation in complementary PWM mode (MTU3 and MTU4).
MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB) are compared with the counters to generate PWM waveforms. When these registers match the counter, the value set in bits OLSN and OLSP in the timer output control register (TOCR1) is output.
MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD) are buffer registers for these compare registers.
When the double buffer function is used, MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF) are also used as buffer registers B. For details of double buffer operation, see section 19.3.8 (2) (s) Double Buffer Function in Complementary PWM Mode.
To update data in a compare register, write the data to be updated to the corresponding buffer register. Buffer registers are always readable and writable.
Data in a compare register can be changed by writing new data to the corresponding buffer register. The buffer registers can be read or written at any time.
The data written to a buffer register is constantly transferred to the temporary register in the Ta interval. Data is not transferred to the temporary register in the Tb interval. Data written to a buffer register in this interval is transferred to the temporary register at the end of the Tb interval.
The value transferred to a temporary register is transferred to the compare register when TCNTSA (TCNTSB) for which the Tb interval ends matches MTU3.TGRA (MTU6.TGRA) while TCNTSA (TCNTSB) is counting up, or 0000h while counting down. The timing for transfer from the temporary register to the compare register can be selected with bits MD[3:0] in the timer mode register 1 (TMDR1). Figure 19.50 shows an example in which the trough is selected for the transfer timing.
In the Tb interval in which data is not transferred to the temporary register (Tb1 in Figure 19.50), the temporary register has the same function as the compare register and is compared with the counter. In this interval, therefore, there are two compare match registers for one output phase; the compare register contains the pre-change data and the temporary register contains new data. In this interval, three counters MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) and two registers (compare register and temporary register) are compared, and PWM output is controlled accordingly.

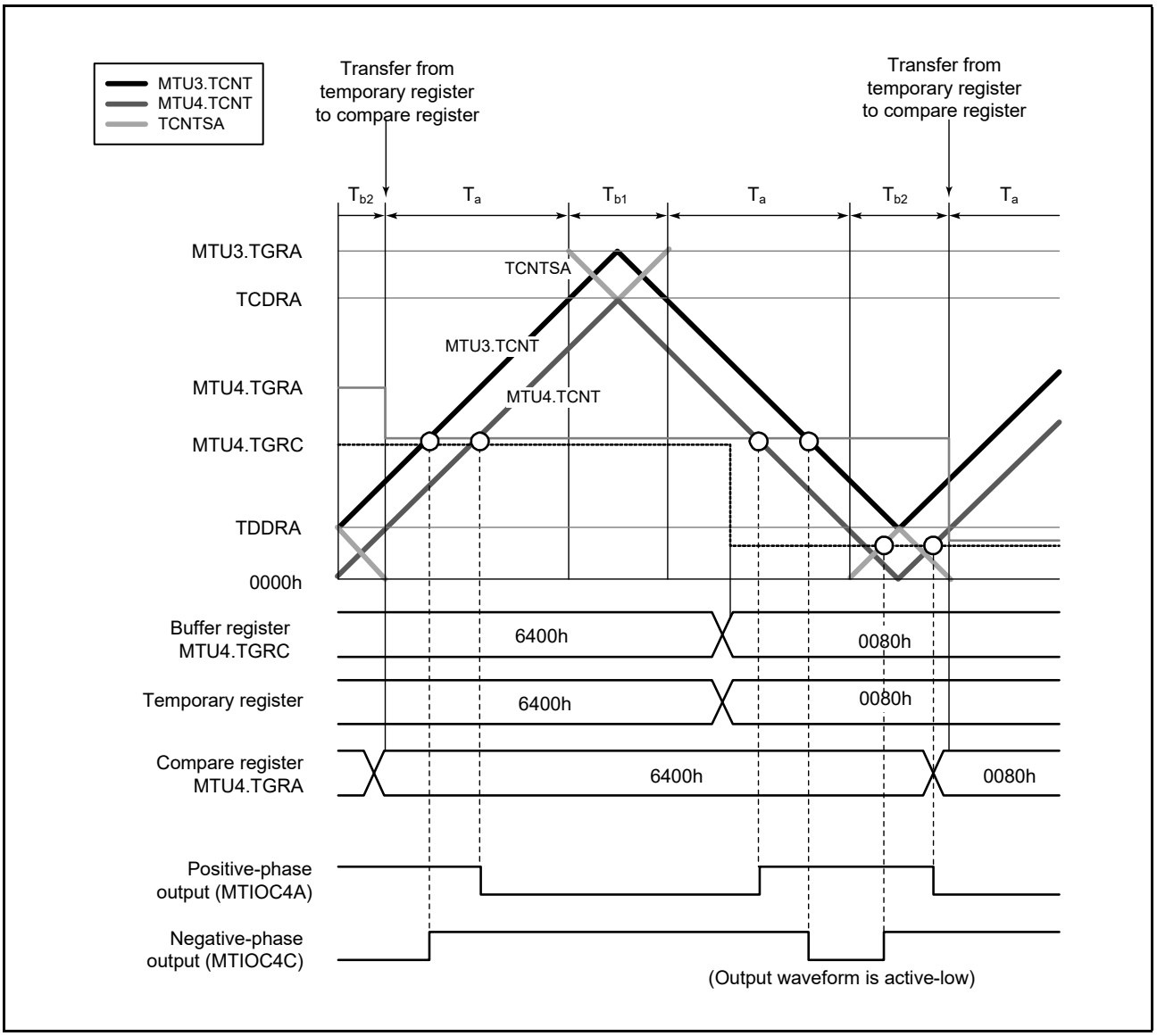


Figure 19.50 Example of Operation in Complementary PWM Mode (MTU3 and MTU4)

(c) Initial Setting

In complementary PWM mode, there are six registers that require initial setting. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).
Before setting complementary PWM mode with bits MD[3:0] in the timer mode register 1 (TMDR1), initial values should be set in the following registers.
MTU3.TGRC (MTU6.TGRC) operates as the buffer register for MTU3.TGRA (MTU6.TGRA), and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBRA or TCBRB) operates as the buffer register for the timer cycle data register (TCDRA or TCDRB), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDRA or TDDRB).
When dead time is not needed, the TDER bit in the timer dead time enable register (TDERA or TDERB) should be cleared to 0, MTU3.TGRC and MTU3.TGRA (MTU6.TGRC and MTU6.TGRA) should be set to 1/2 the PWM carrier cycle + 1, and TDDRA (TDDRB) should be set to 1.
Set the respective initial PWM duty values in three buffer registers A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD (MTU6.TGRD, MTU7.TGRC, and MTU7.TGRD)).
Set the respective (initial PWM duty – 1) values in three buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF (MTU6.TGRE, MTU7.TGRE, and MTU7.TGRF)) only when the double buffer function is used.
The values set in the five buffer registers excluding TDDRA (TDDRB) are transferred to the corresponding compare registers as soon as complementary PWM mode is set.
Set MTU4.TCNT (MTU7.TCNT) to 0000h before setting complementary PWM mode.

Table 19.76 Registers and Counters Requiring Initial Setting

Register and Counter	Setting
MTU3.TGRC MTU6.TGRC	1/2 PWM carrier cycle + dead time Td (1/2 PWM carrier cycle + 1 when dead time generation is disabled by TDERA or TDERB)
TDDRA, TDDRB	Dead time Td (1 when dead time generation is disabled by TDERA or TDERB)
TCBRA, TCBRB	1/2 PWM carrier cycle
MTU3.TGRD, MTU4.TGRC, MTU4.TGRD MTU6.TGRD, MTU7.TGRC, MTU7.TGRD	Initial PWM duty ratio value for each phase
MTU3.TGRE, MTU4.TGRE, MTU4.TGRF MTU6.TGRE, MTU7.TGRE, MTU7.TGRF	Initial PWM duty ratio – 1 value for each phase (only when double buffer function is used)
MTU4.TCNT MTU7.TCNT	0000h

Note: The value set in MTU3.TGRC (MTU6.TGRC) should be the sum of 1/2 the PWM carrier cycle set in TCBRA (TCBRB) and dead time Td set in TDDRA (TDDRB). When dead time generation is disabled by TDERA (TDERB), TGRC should be set to 1/2 the PWM carrier cycle + 1.

(d) PWM Output Level Setting

In complementary PWM mode, the PWM pulse output level is set with bits OLSN and OLSP in timer output control register 1 (TOCR1A or TOCR1B) or bits OLS1P to OLS3P and OLS1N to OLS3N in timer output control register 2 (TOCR2A or TOCR2B).
The output level can be set for each of the three positive phases and three negative phases of 6-phase output.
Complementary PWM mode should be cleared before setting or changing output levels.

(e) Dead Time Setting

In complementary PWM mode, the dead time can be set for the output PWM waveforms.
The dead time is set in the timer dead time data register (TDDRA or TDDRB). The value set in TDDRA (TDDRB) is used as the MTU3.TCNT (MTU6.TCNT) counter start value and creates a non-overlapping interval between MTU3.TCNT (MTU6.TCNT) and MTU4.TCNT (MTU7.TCNT). Complementary PWM mode should be cleared before changing the contents of TDDRA (TDDRB).

(f) Dead Time Suppressing

Dead time generation is suppressed by clearing the TDER bit in the timer dead time enable register (TDERA or TDERB) to 0. TDERA (TDERB) can be cleared to 0 only when 0 is written to it after reading TDER = 1.
MTU3.TGRA and MTU4.TGRC (MTU6.TGRA and MTU7.TGRC) should be set to 1/2 PWM carrier cycle + 1 and the timer dead time data register (TDDRA or TDDRB) should be set to 1.
By the above settings, PWM waveforms without dead time can be obtained. Figure 19.51 shows an example of operation without dead time (MTU3 and MTU4).

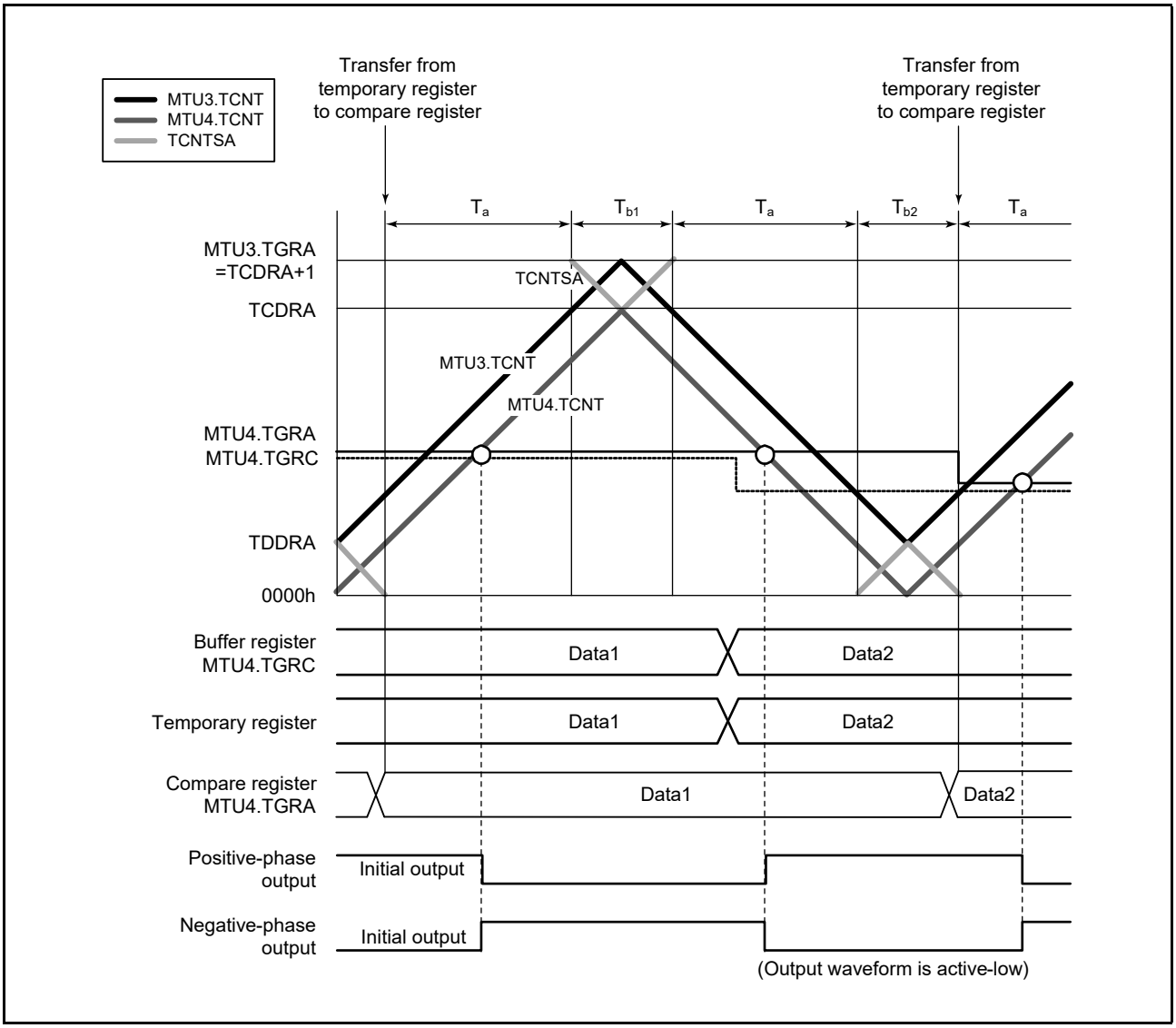


Figure 19.51 Example of Operation without Dead Time (MTU3 and MTU4)

(g) PWM Cycle Setting

In complementary PWM mode, the PWM pulse cycle is set in two registers—MTU3.TGRA (MTU6.TGRA), in which the MTU3.TCNT (MTU6.TCNT) upper limit value is set, and TCDRA (TCDRB), in which the MTU4.TCNT (MTU7.TCNT) upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:

With dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + TDDRA (TDDRB) setting
Without dead time: MTU3.TGRA (MTU6.TGRA) setting = TCDRA (TCDRB) setting + 1

In addition, the settings should be made so as to achieve the following relationship between the TCDRA (TCDRB) register and the TDDRA (TDDRB) register:
TCDRA (TCDRB) setting value > TDDRA (TDDRB) setting value × 2 + 2

The MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) settings are made by setting values in buffer registers MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB). The values set in MTU3.TGRC and TCBRA (MTU6.TGRC and TCBRB) are transferred simultaneously to MTU3.TGRA and TCDRA (MTU6.TGRA and TCDRB) with the transfer timing selected with bits MD[3:0] in the timer mode register 1 (TMDR1).
The new PWM cycle is reflected from the next cycle when data is updated at the crest, or from the current cycle when updated in the trough. Figure 19.52 illustrates the operation when the PWM cycle is updated at the crest.
See the following section, (h) Register Data Updating, for the method of updating the data in each buffer register.

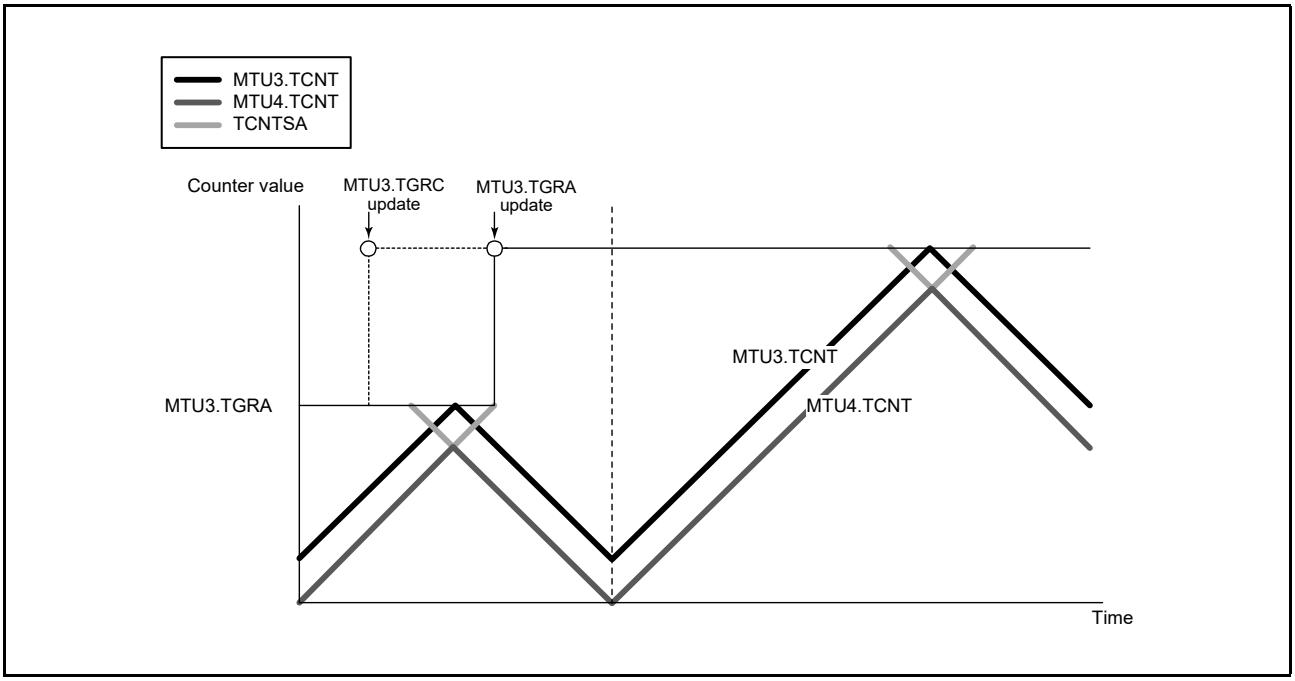


Figure 19.52 Example of PWM Cycle Updating (MTU3 and MTU4)

(h) Register Data Updating

In complementary PWM mode, the buffer register is used to update the data in a compare register. The update data can be written to the buffer register at any time. There are five registers (PWM duty and carrier cycle registers) that have buffer registers and can be updated during operation.

There is a temporary register between each of these registers and its buffer register. While subcounter TCNTSA (TCNTSB) is not counting, if buffer register data is updated, the temporary register value also changes. Data is not transferred from buffer registers to temporary registers while TCNTSA (TCNTSB) is counting; in this case, the value written to a buffer register is transferred after TCNTSA (TCNTSB) halts.

The temporary register value is transferred to the compare register at the data update timing set with bits MD[3:0] in the timer mode register 1 (TMDR1). Figure 19.53 shows an example of data updating in complementary PWM mode (MTU3 and MTU4). This example shows the mode in which data is updated at both the counter crest and trough.

When updating buffer register data, be sure to write to MTU4.TGRD (MTU7.TGRD) at the end of the update. Data is transferred from buffer registers to the temporary registers simultaneously for all five registers after the write to MTU4.TGRD (MTU7.TGRD).

Even when not updating all five registers or when not updating the MTU4.TGRD (MTU7.TGRD) data, be sure to write to MTU4.TGRD (MTU7.TGRD) after writing data to the registers to be updated. In this case, the data written to MTU4.TGRD (MTU7.TGRD) should be the same as the data prior to the write operation.

See section 19.3.8 (2) (s) Double Buffer Function in Complementary PWM Mode, for data updating when the double buffer function is used.

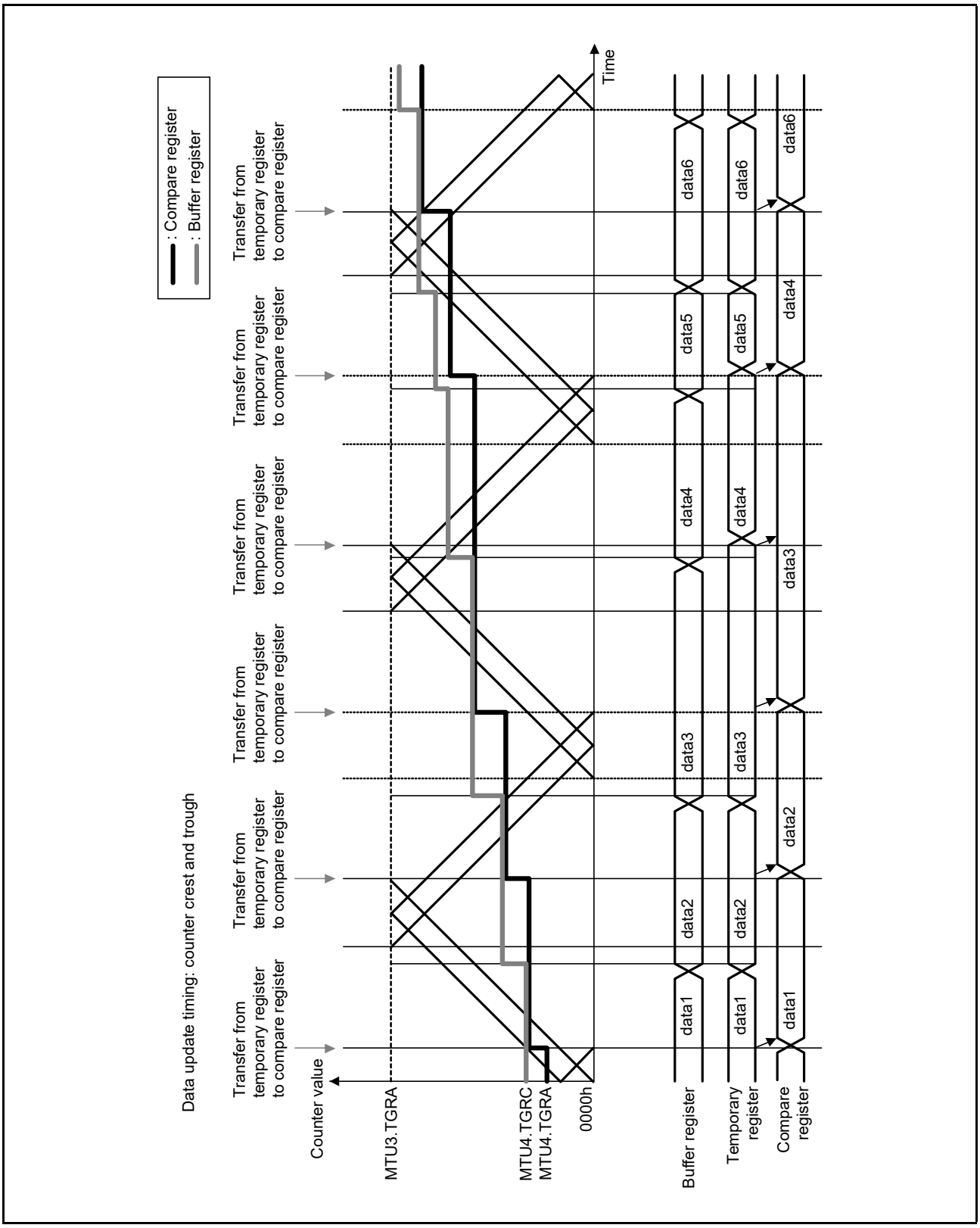


Figure 19.53 Example of Data Updating in Complementary PWM Mode (MTU3 and MTU4)

(i) Initial Output in Complementary PWM Mode

In complementary PWM mode, the initial output is determined by the setting of bits OLSN and OLSP in timer output control register 1 (TOCR1A or TOCR1B) or bits OLS1N to OLS3N and OLS1P to OLS3P in timer output control register 2 (TOCR2A or TOCR2B).

This initial output is the non-active level of the PWM pulse and continues from when complementary PWM mode is set with the timer mode register 1 (TMDR1) until MTU4.TCNT (MTU7.TCNT) exceeds the value set in the dead time register (TDDRA or TDDRB). Figure 19.54 shows an example of the initial output in complementary PWM mode. An example of the waveform when the initial PWM duty ratio value is smaller than the TDDRA (TDDRB) value is shown in Figure 19.55.

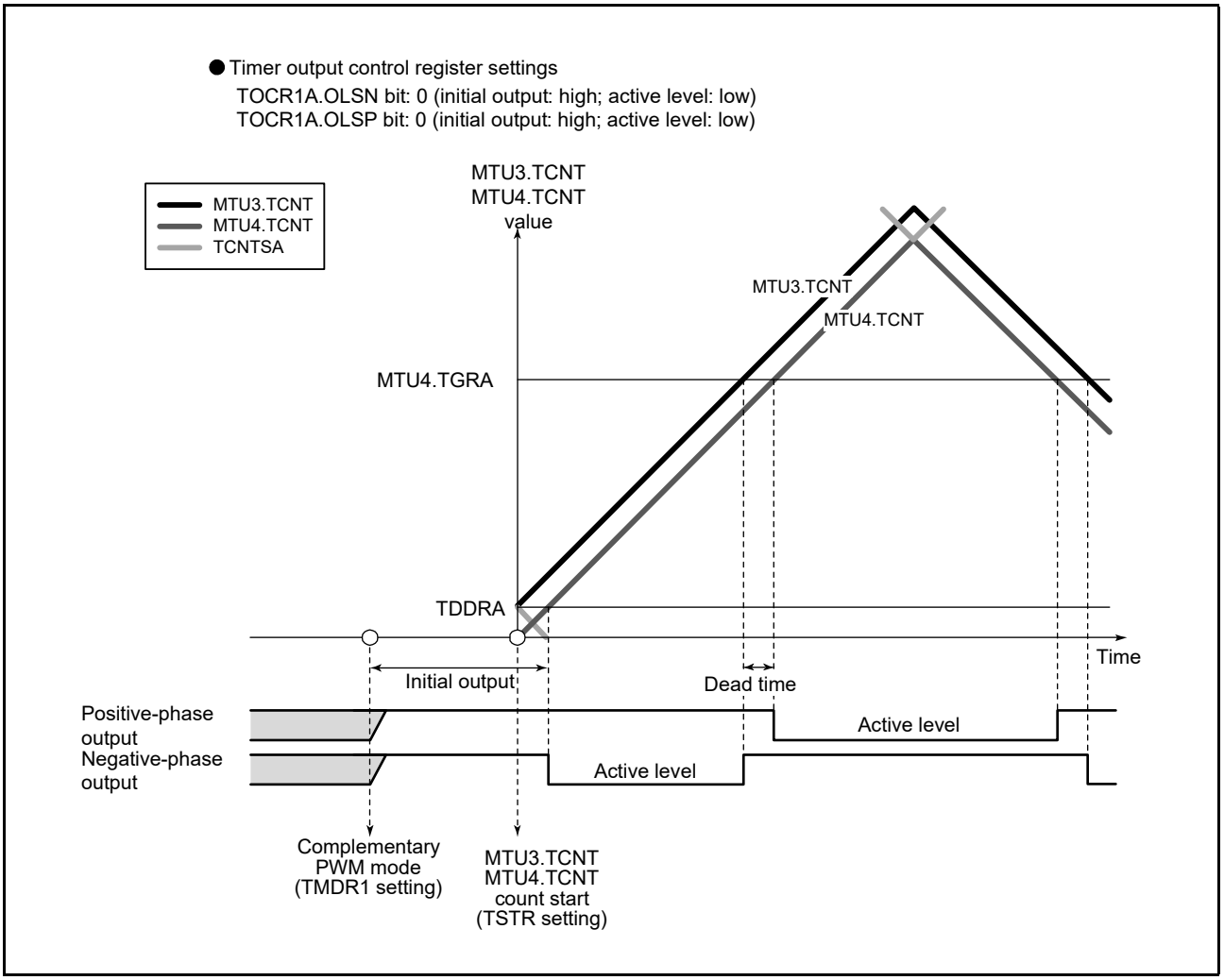


Figure 19.54 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (1)

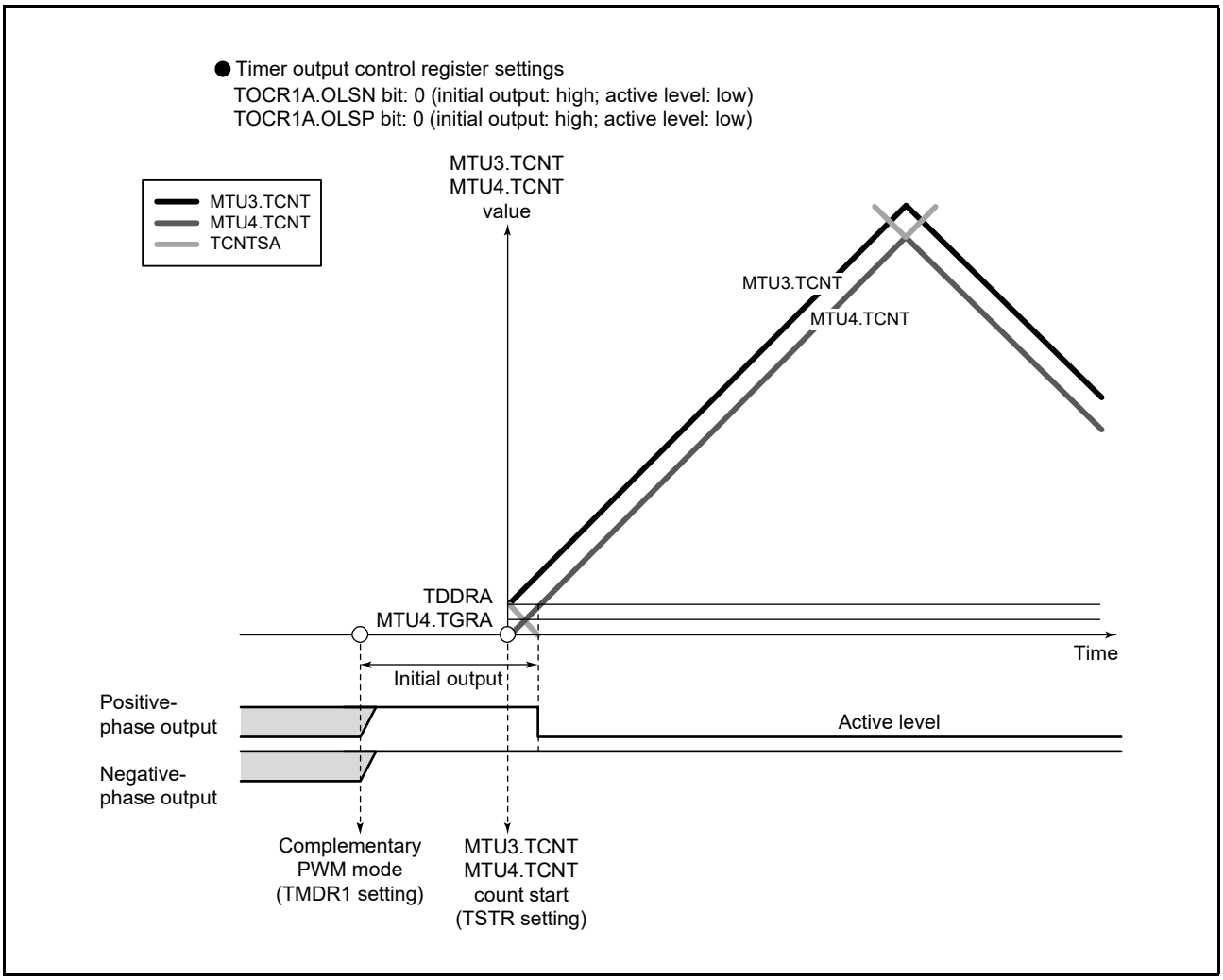


Figure 19.55 Example of Initial Output in Complementary PWM Mode (MTU3 and MTU4) (2)

(j) Method for Generating PWM Output in Complementary PWM Mode

In complementary PWM mode, six waveforms of three-phase PWM are output. The dead time can be set for the output PWM waveforms.

A PWM waveform is generated by output of the level selected in the timer output control register in the event of a compare match between a counter and a compare register. While TCNTSA (TCNTSB) is counting, the compare register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of turn-on and turn-off compare match occurrence may vary, but the compare match that turns off each phase takes precedence to secure the dead time and ensure that the positive-phase and negative-phase turn-on times do not overlap. Figure 19.56 to Figure 19.58 show examples of waveform generation in complementary PWM mode.

The positive-phase and negative-phase turn-off timing is generated by a compare match with the counter value indicated in MTU3.TCNT in the figure, and the turn-on timing by a compare match with the counter indicated in MTU4.TCNT, which operates with a delay of the dead time behind the MTU3.TCNT counter. In the T1 period, compare match a that turns off the negative phase has the highest priority, and compare matches before a are ignored. In the T2 period, compare match c that turns off the positive phase has the highest priority, and compare matches before c are ignored.

In most cases, compare matches occur in the order a → b → c → d (or c → d → a' → b') as shown in Figure 19.56.

If compare matches deviate from the a → b → c → d order, since the time for which the negative phase is off is shorter than twice the dead time, the positive phase is not turned on. If compare matches deviate from the c → d → a' → b' order, since the time for which the positive phase is off is shorter than twice the dead time, the negative phase is not turned on.

As shown in Figure 19.57, if compare match c follows compare match a before compare match b, compare match b is ignored and the negative phase is turned on by compare match d. This is because turning off the positive phase has priority due to the occurrence of compare match c (positive-phase off timing) before compare match b (positive-phase on timing) (consequently, the waveform does not change because the positive phase goes from off to off).

Similarly, in the example in Figure 19.58, compare match a' with new data in the temporary register occurs before compare match c, but until compare match c, which turns off the positive phase, other compare matches are ignored. As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare matches at turn-off timings take precedence, and turn-on timing compare matches that occur before a turn-off timing compare match are ignored.

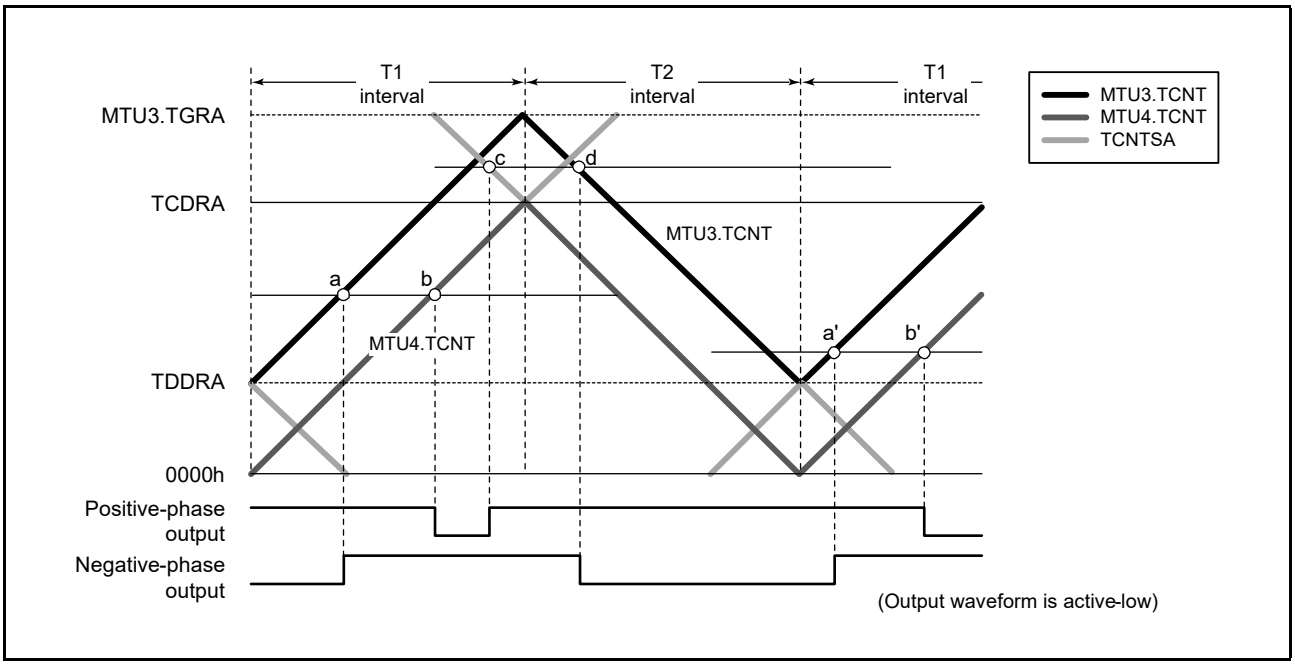


Figure 19.56 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

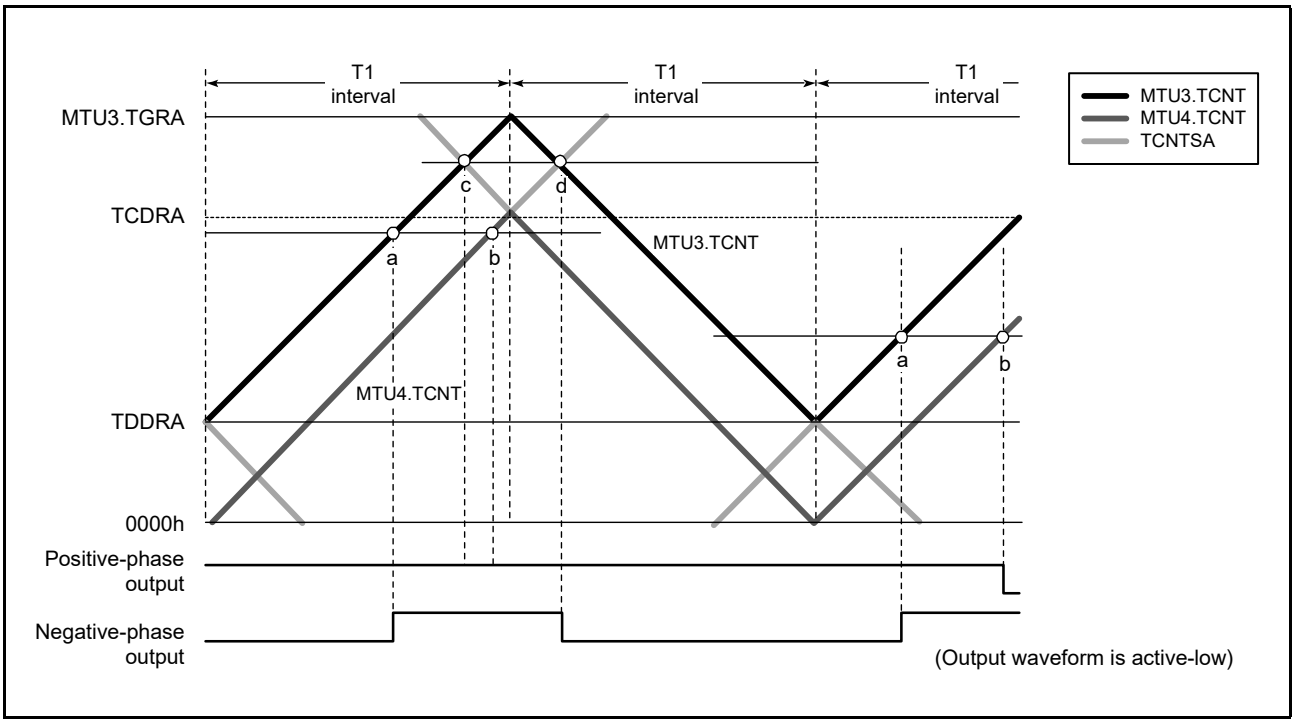


Figure 19.57 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

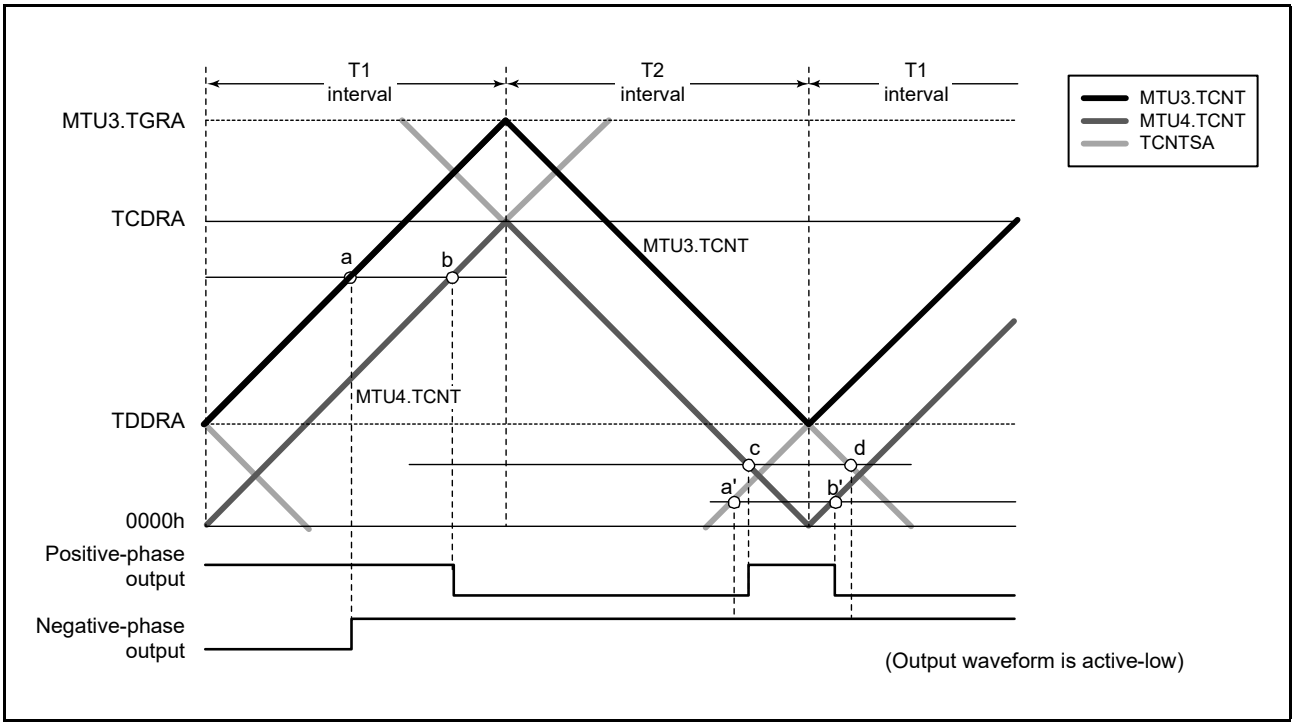


Figure 19.58 Example of Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

(k) 0% and 100% Duty Ratio Output in Complementary PWM Mode

In complementary PWM mode, 0% and 100% duty PWM waveforms can be output as required. Figure 19.59 to Figure 19.63 show output examples.

A 100% duty waveform is output when the compare register value is set to 0000h. The waveform in this case has a positive phase with a 100% on-state. A 0% duty waveform is output when the compare register value is set to the same value as MTU3.TGRA (MTU6.TGRA). The waveform in this case has a positive phase with a 100% off-state.

On and off compare matches occur simultaneously, but if a turn-on compare match and turn-off compare match for the same phase occur simultaneously, both compare matches are ignored and the waveform does not change.

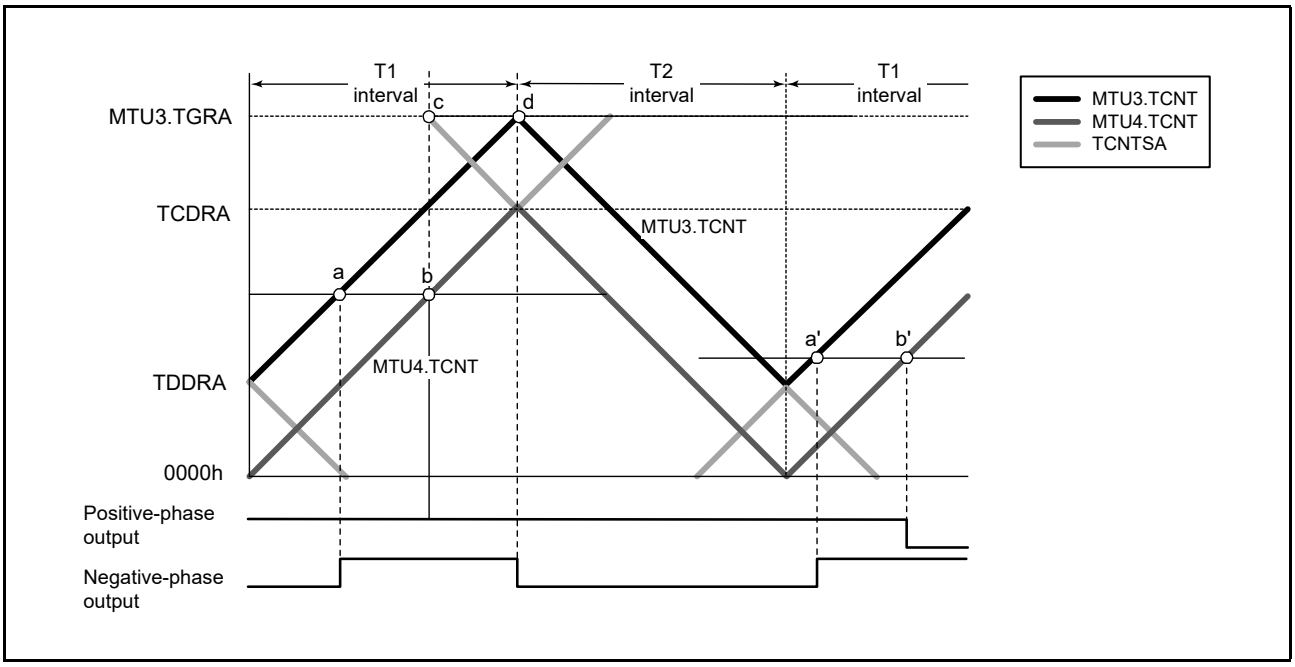


Figure 19.59 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (1)

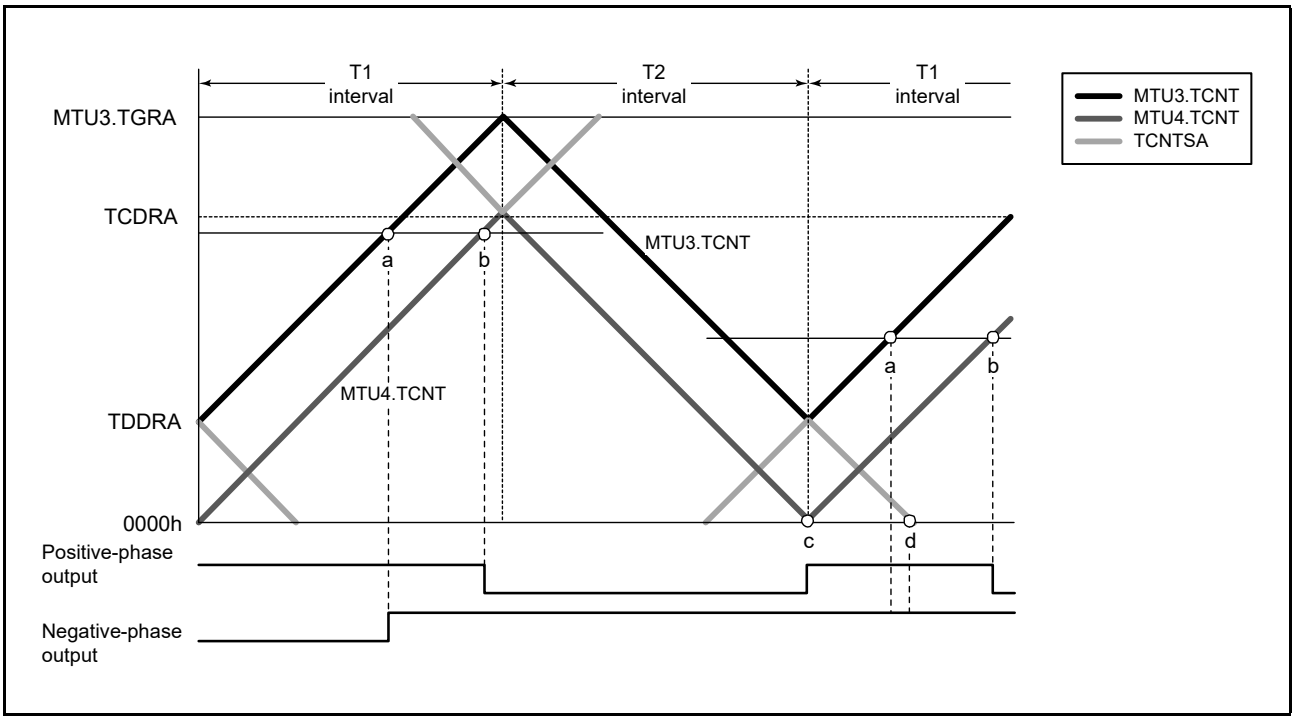


Figure 19.60 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (2)

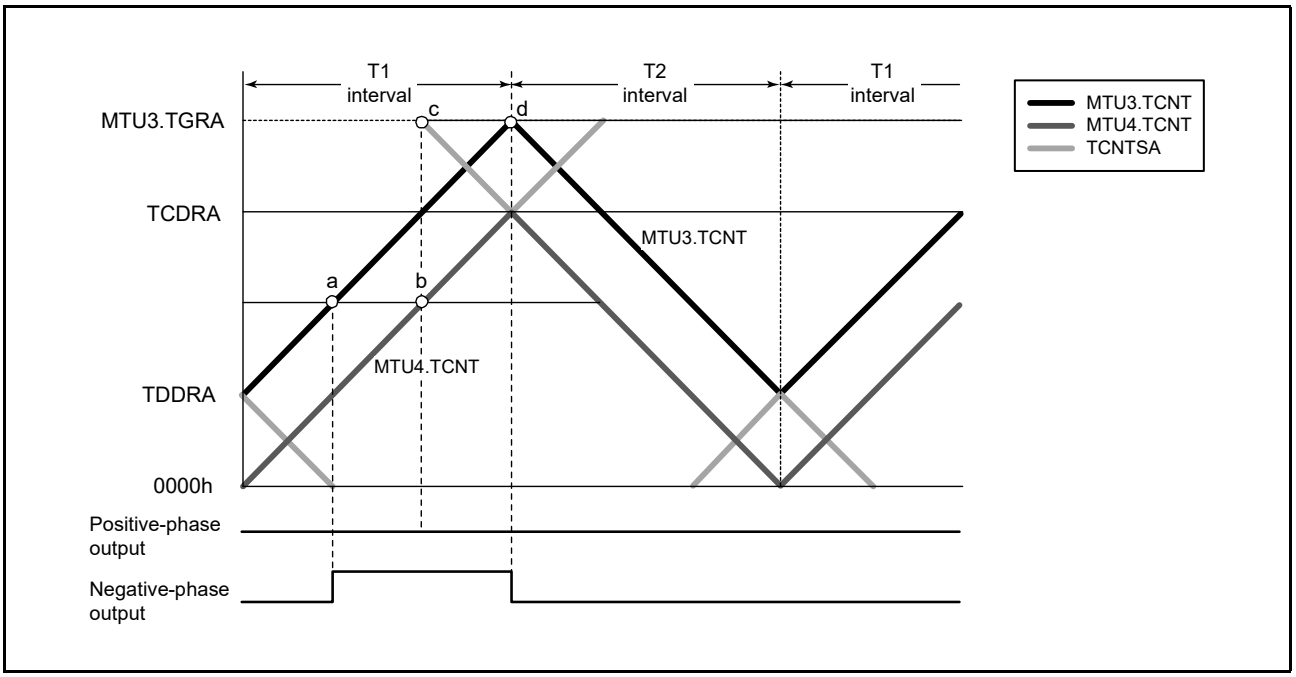


Figure 19.61 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (3)

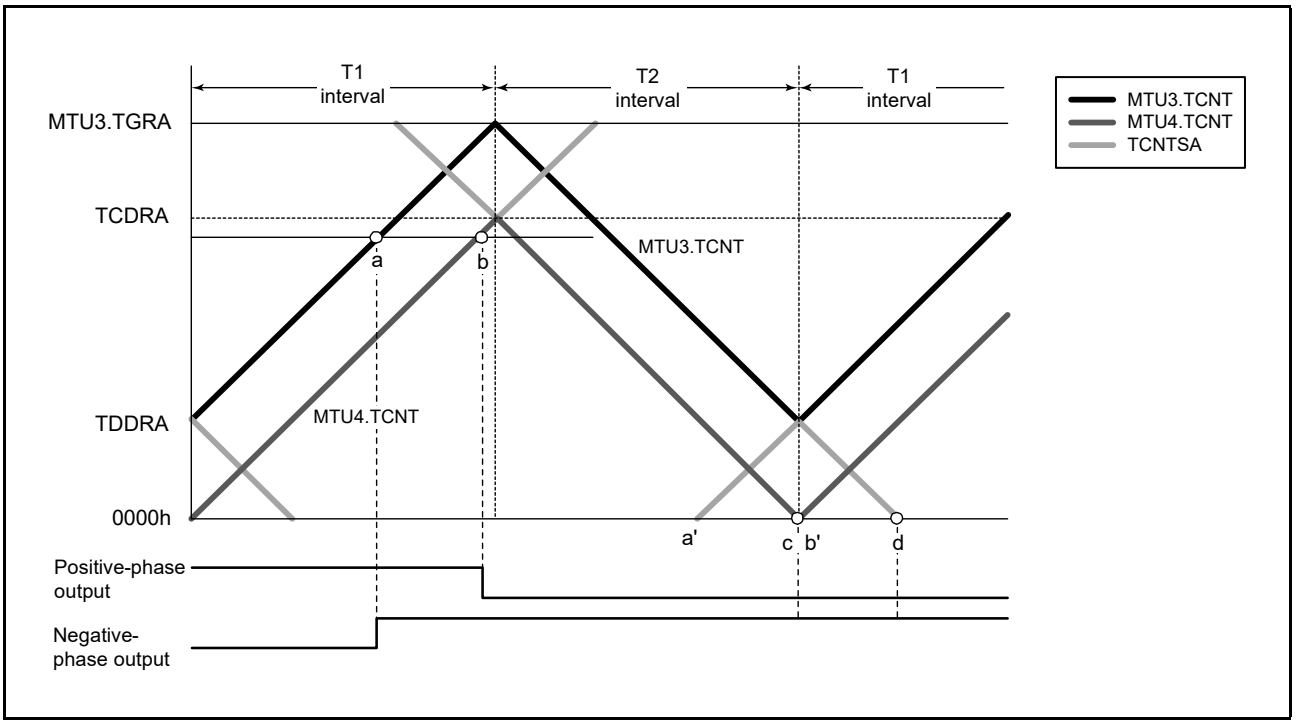


Figure 19.62 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (4)

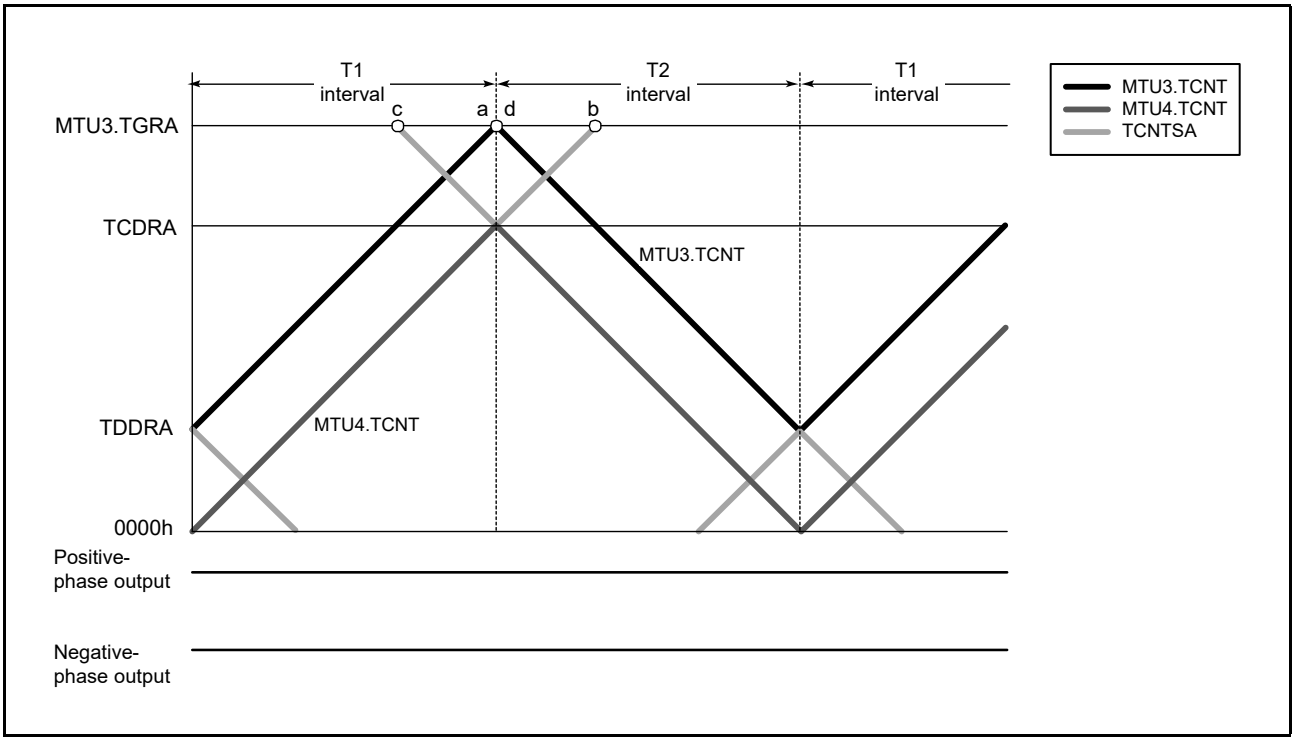


Figure 19.63 Example of 0% and 100% Waveform Output in Complementary PWM Mode (MTU3 and MTU4) (5)

(l) Toggle Output Synchronized with PWM Cycle

In complementary PWM mode, toggle output in synchronization with the PWM carrier cycle can be generated by setting the PSYE bit to 1 in the timer output control register 1 (TOCR1A or TOCR1B). An example of a toggle output waveform is shown in Figure 19.64.

This output is toggled by a compare match between MTU3.TCNT and MTU3.TGRA (MTU6.TCNT and MTU6.TGRA) and a compare match between MTU4.TCNT (MTU7.TCNT) and 0000h.

The MTIOC3A (MTIOC6A) pin is assigned for this toggle output. The initial output is High.

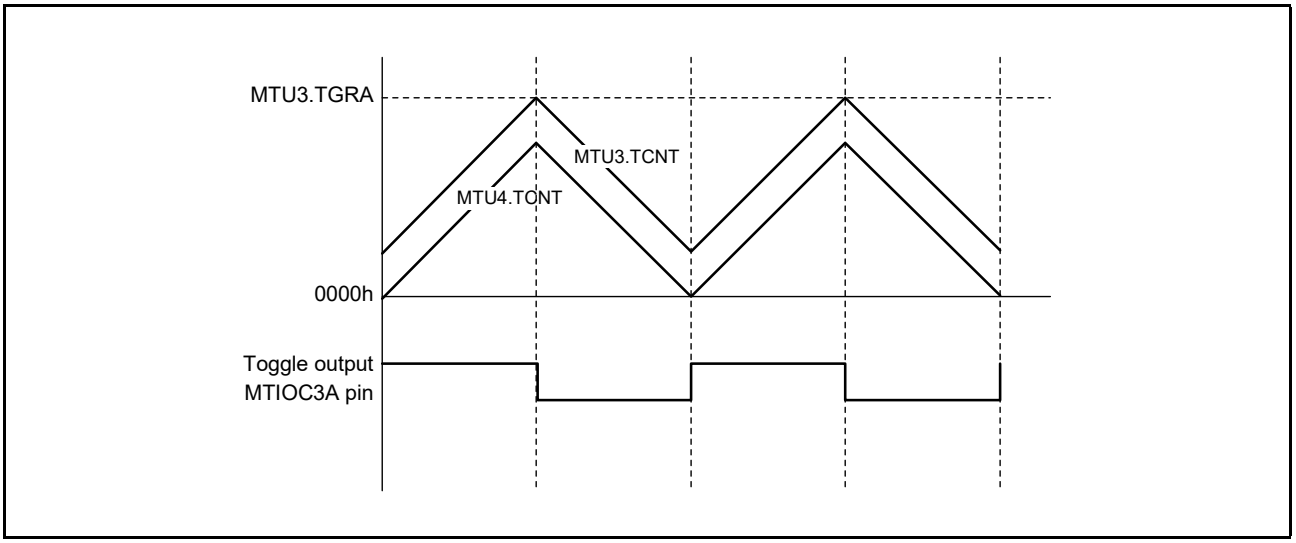


Figure 19.64 Example of Toggle Output Waveform Synchronized with PWM Output (MTU3 and MTU4)

(m) Counter Clearing by Another Channel

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by another channel when a mode for synchronization with another channel is specified through the timer synchronous register (TSYRA or TSYRB) and synchronous clearing is selected with bits CCLR[2:0] in the timer control register (TCR).

Figure 19.65 illustrates an example of this operation.

Use of this function enables a counter to be cleared and restarted through an external signal.

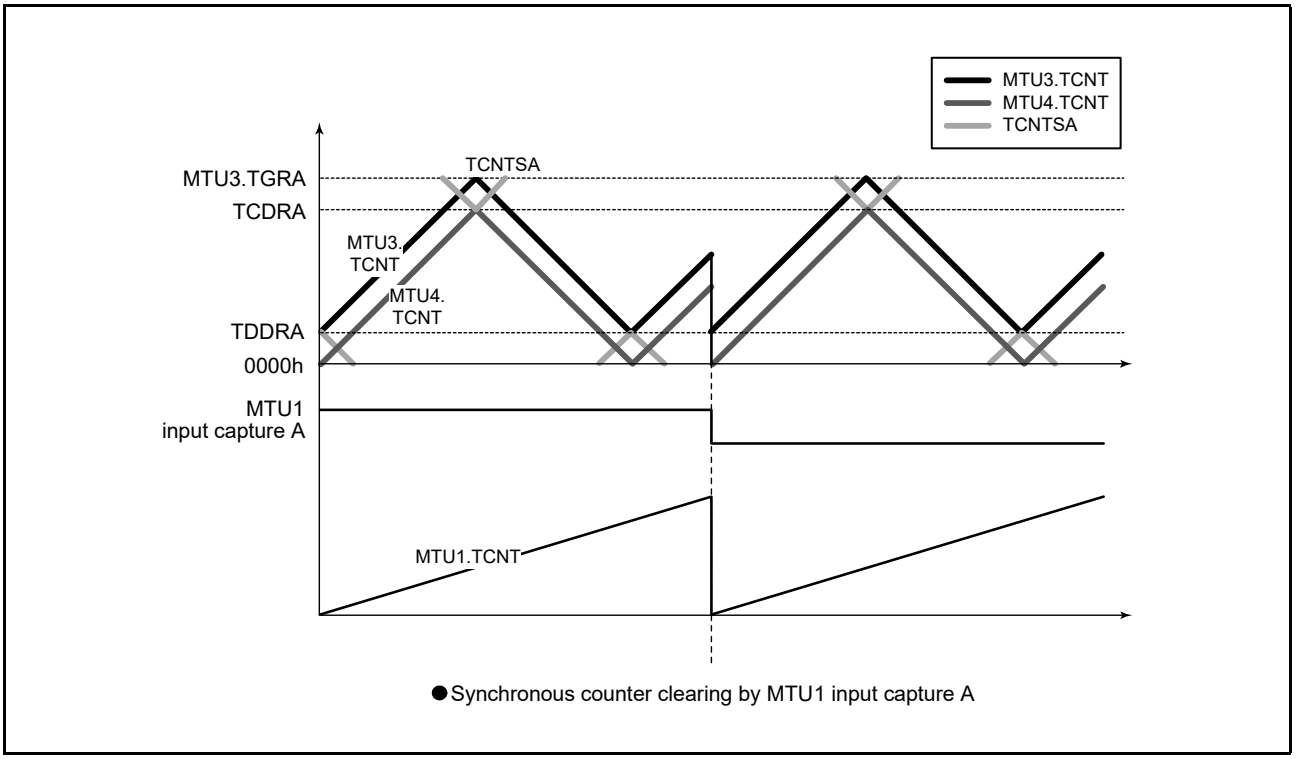


Figure 19.65 Counter Clearing Synchronized with Another Channel (MTU3 and MTU4)

(n) Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Setting the WRE bit in TWCRA (TWCRB) to 1 suppresses initial output when synchronous counter clearing occurs in the Tb interval at the trough in complementary PWM mode and controls abrupt change in duty cycle at synchronous counter clearing.

Initial output suppression through the WRE bit = 1 is applicable only when synchronous clearing occurs in the Tb interval at the trough as indicated by (10) or (11) in Figure 19.66. When synchronous clearing occurs outside that interval, the initial value specified by the OLSN and OLSP bits in TOCR1A (TOCR1B) is output. Even in the Tb interval at the trough, if synchronous clearing occurs in the initial value output period (indicated by (1) in Figure 19.66) immediately after the counters start operation, initial value output is not suppressed.

This function can be used in both channel combinations of MTU 3 and MTU4, or MTU6 and MTU7. In MTU3 and MTU4, synchronous clearing generated in MTU0 to MTU2 can cause counter clearing; in MTU6 and MTU7, compare match or input capture generated in MTU0 to MTU2 can cause counter clearing.

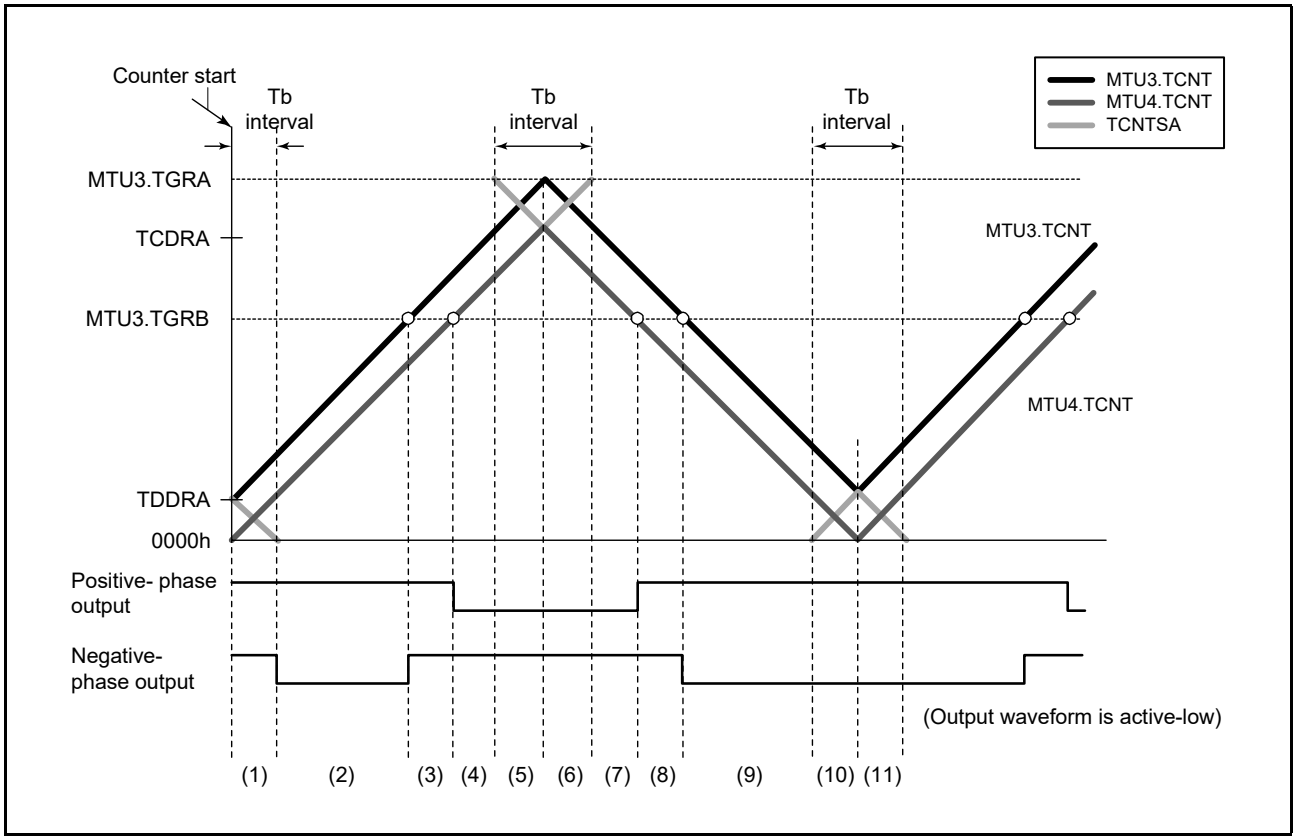


Figure 19.66 Timing for Synchronous Counter Clearing (MTU3 and MTU4)

- Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode.

An example of the procedure for setting output waveform control at synchronous counter clearing in complementary PWM mode is shown in Figure 19.67.

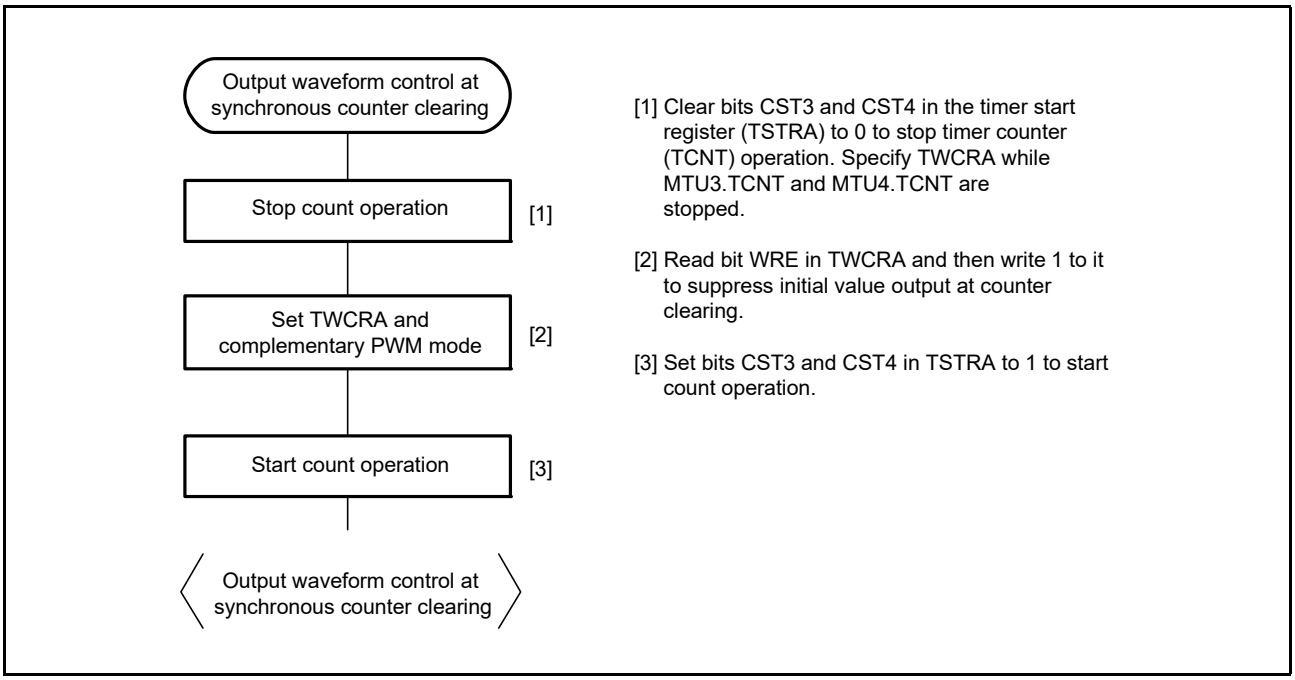


Figure 19.67 Example of Procedure for Setting Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode (MTU3 and MTU4)

- Examples of Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Figure 19.68 to Figure 19.71 show examples of output waveform control in which MTU3 and MTU4 operate in complementary PWM mode and synchronous counter clearing is generated while the WRE bit in TWCRA is set to 1. In the examples shown in Figure 19.68 to Figure 19.71, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 19.66, respectively.

In MTU6 and MTU7, these examples are equivalent to the cases when MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing is generated while the SCC bit is cleared to 0 and the WRE bit is set to 1 in TWCRB.

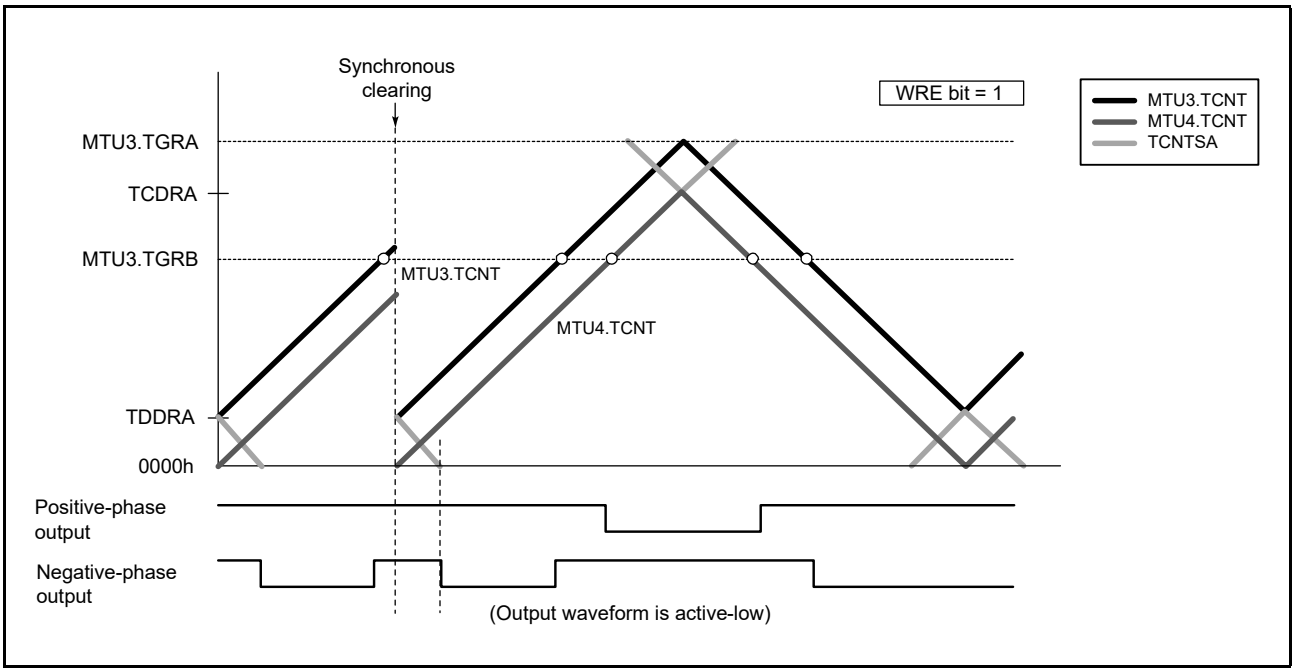


Figure 19.68 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 19.66; Bit WRE of TWCRA is 1)

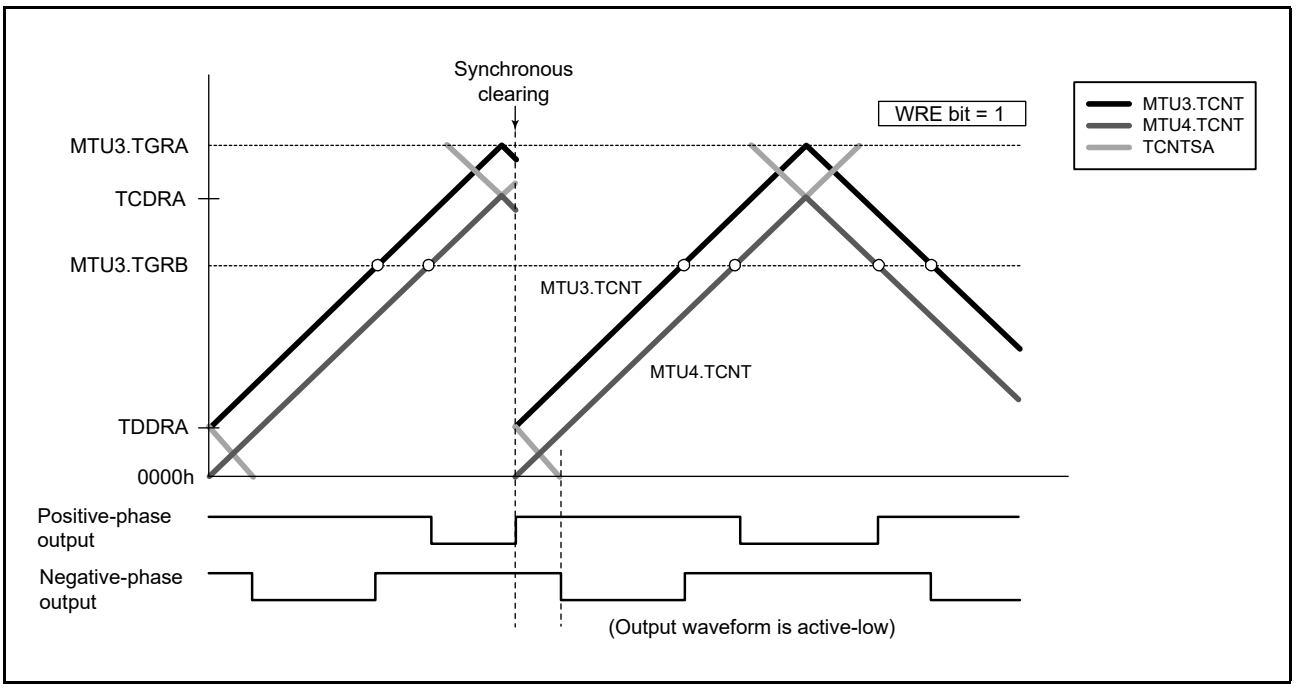


Figure 19.69 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 19.66; Bit WRE of TWCRA is 1)

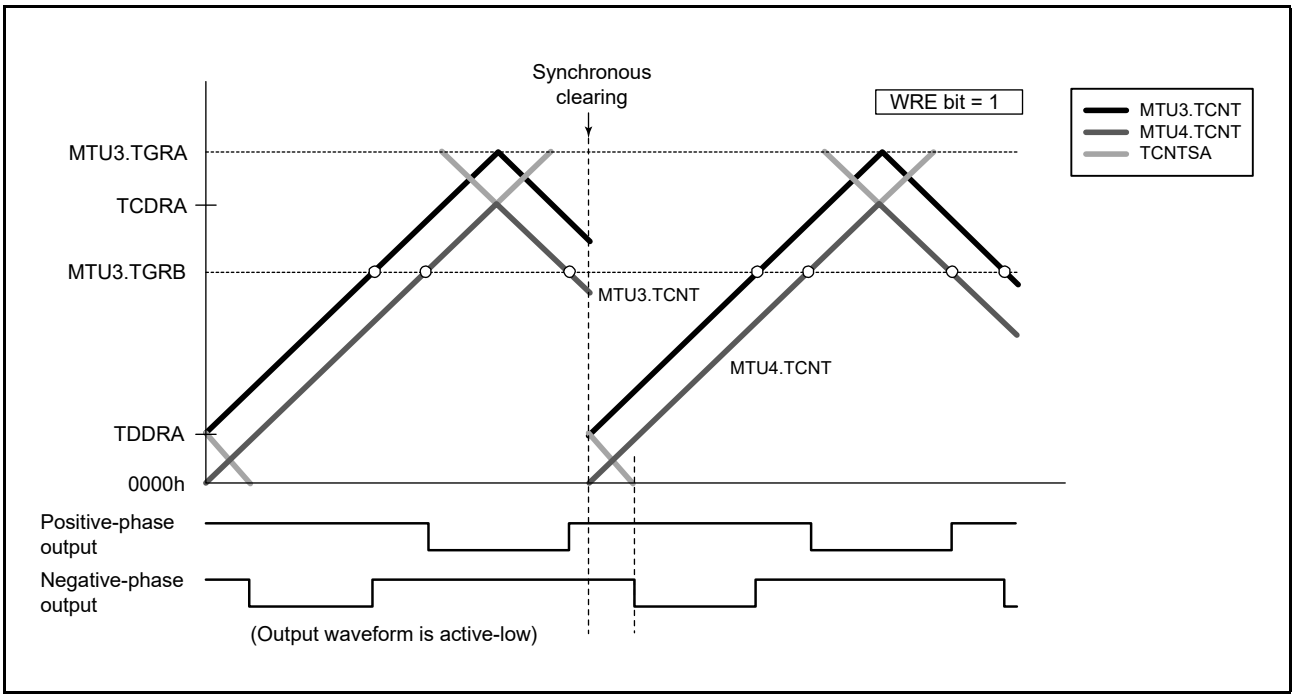


Figure 19.70 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 19.66; Bit WRE of TWCRA is 1)

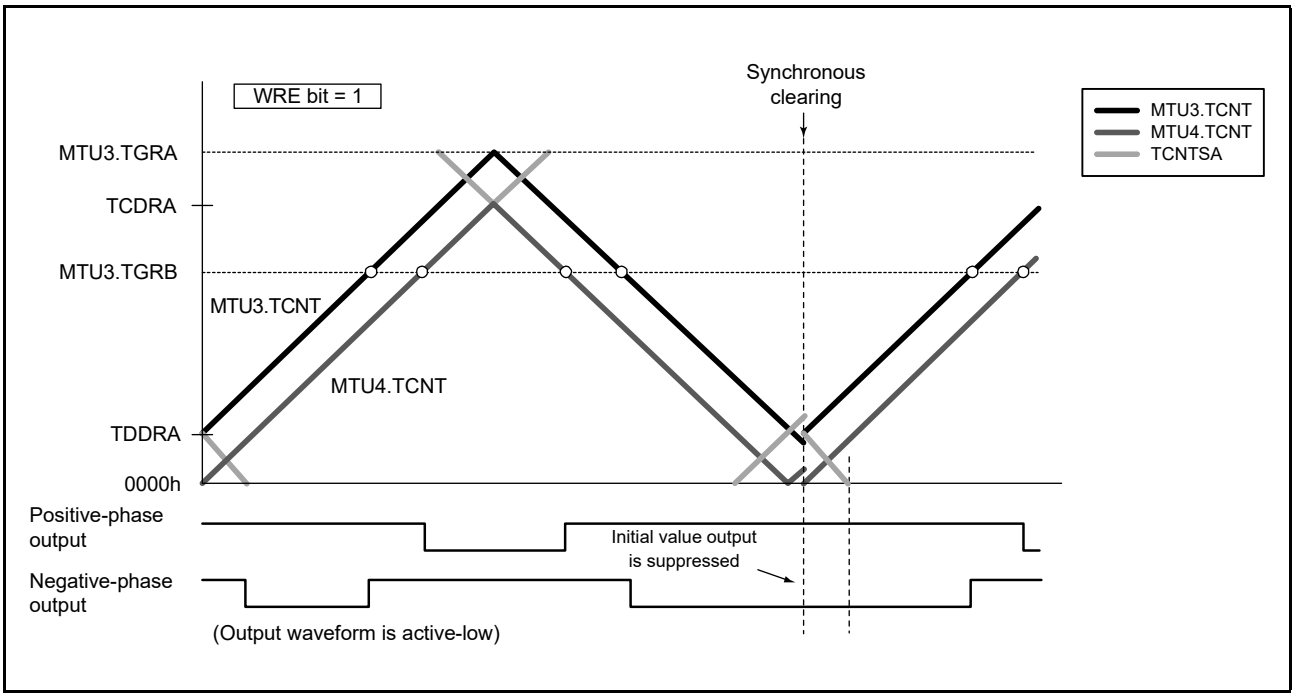


Figure 19.71 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 19.66; Bit WRE of TWCRA is 1)

(o) Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

In MTU6 and MTU7, setting the SCC bit in TWCRB to 1 suppresses synchronous counter clearing caused by MTU0, MTU1, and MTU2.

Synchronous counter clearing caused by MTU0, MTU1, and MTU2 is suppressed only within the interval shown in Figure 19.72.

When using this function, MTU6 and MTU7 should be set to complementary PWM mode.

For details of synchronous clearing caused by MTU0, MTU1, and MTU2, see section 19.3.10 (2) Synchronous Counter Clearing for MTU6 and MTU7.

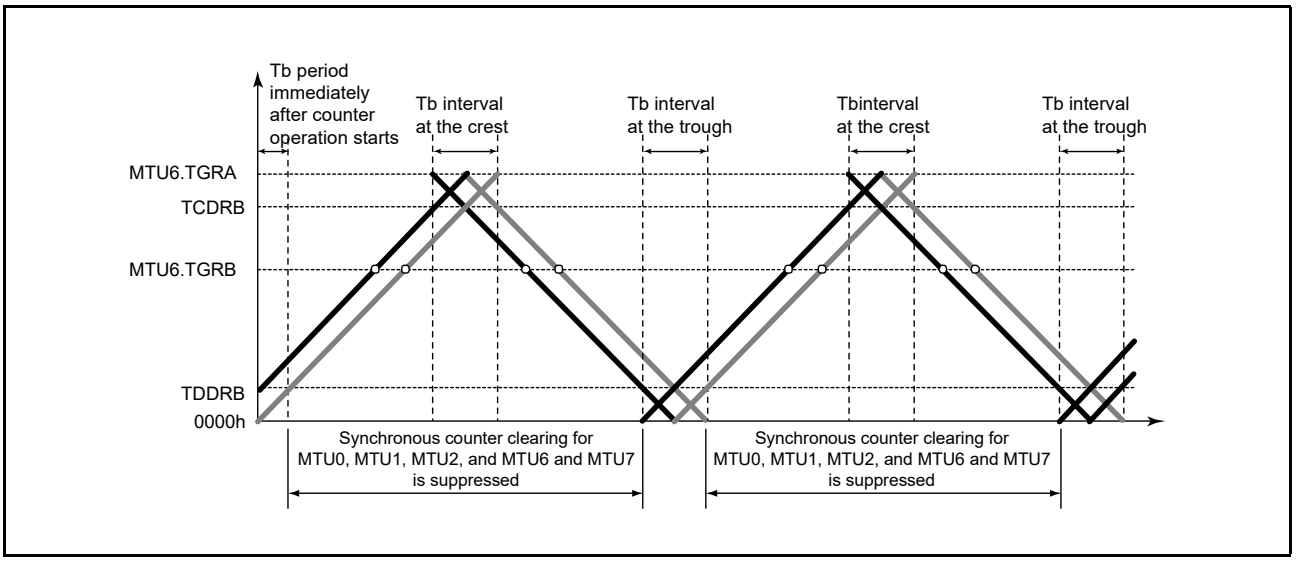
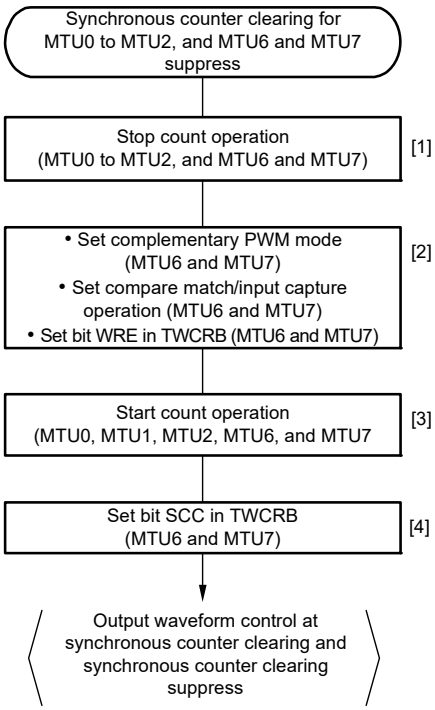


Figure 19.72 Synchronous Clearing-Suppressed Interval Specified by SCC Bit in TWCRB for MTU0 to MTU2, and MTU6 and MTU7

- Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

An example of the procedure for suppressing synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7 is shown in Figure 19.73.



[1] Clear bits CST of the timer start register (TSTRB) in MTU6 and MTU7 to 0, and stop count operation. Clear bits CST of TSTRA in MTU0, MTU1, and MTU2 to 0, and stop count operation.

[2] Set the complementary PWM mode in MTU6 and MTU7 and compare match/input capture operation in MTU0, MTU1, and MTU2. When bit WRE in TWCRA or TWCRB should be set, make appropriate setting here.

[3] Set bits CST6 and CST7 in MTU6 and MTU7 to 1 to start count operation. For synchronous counter clearing for MTU0, MTU1, MTU2 to MTU6, and MTU7, set bits CST of TSTRA in MTU0, MTU1, and MTU2 to 1 to start count operation in any one of MTU0.TCNT to MTU2.TCNT.

[4] Read TWCRB and then set bit SCC in TWCRB to 1 to suppress synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7*1. Here, do not modify the CCE and WRE bit values in TWCRB of MTU6 and MTU7. Synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7 is suppressed in the synchronous counter clearing-suppressed periods.

Note 1. The TWCRB.SCC bit value can be modified during counter operation. However, if a synchronous clearing occurs when bit TWCRB.SCC is modified from 0 to 1, the synchronous clearing may not be suppressed. If a synchronous clearing occurs when bit TWCRB.SCC is modified from 1 to 0, the synchronous clearing may be suppressed.

Figure 19.73 Example of Procedure for Suppressing Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

- Examples of Suppression of Synchronous Counter Clearing for MTU0 to MTU2, and MTU6 and MTU7

Figure 19.74 to Figure 19.77 show examples of operation in which MTU6 and MTU7 operate in complementary PWM mode and synchronous counter clearing for MTU0 to MTU2, and MTU6 and MTU7 is suppressed by setting the SCC bit in TWCRB in MTU6 and MTU7 to 1. In the examples shown in Figure 19.74 to Figure 19.77, synchronous counter clearing occurs at timing (3), (6), (8), and (11) shown in Figure 19.66, respectively. In these examples, the WRE bit in TWCRB in MTU6 and MTU7 is set to 1.

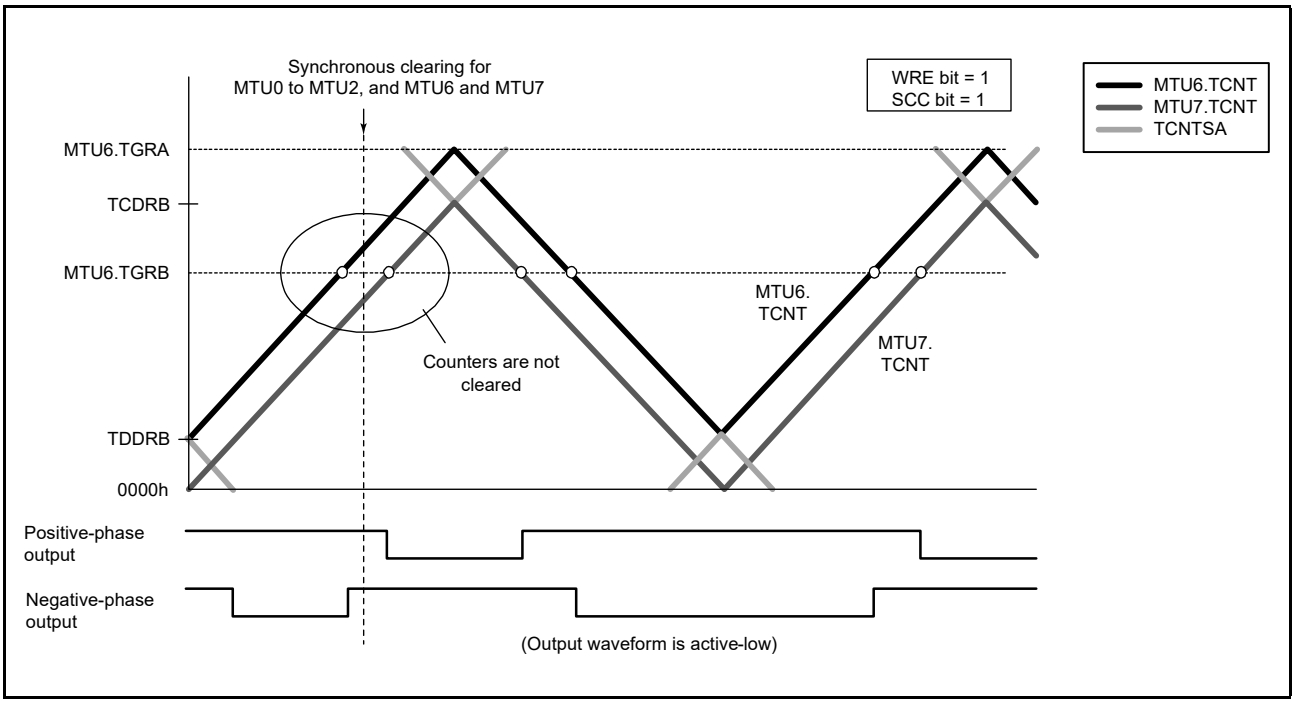


Figure 19.74 Example of Synchronous Clearing in Dead Time during Up-Counting (Timing (3) in Figure 19.66; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

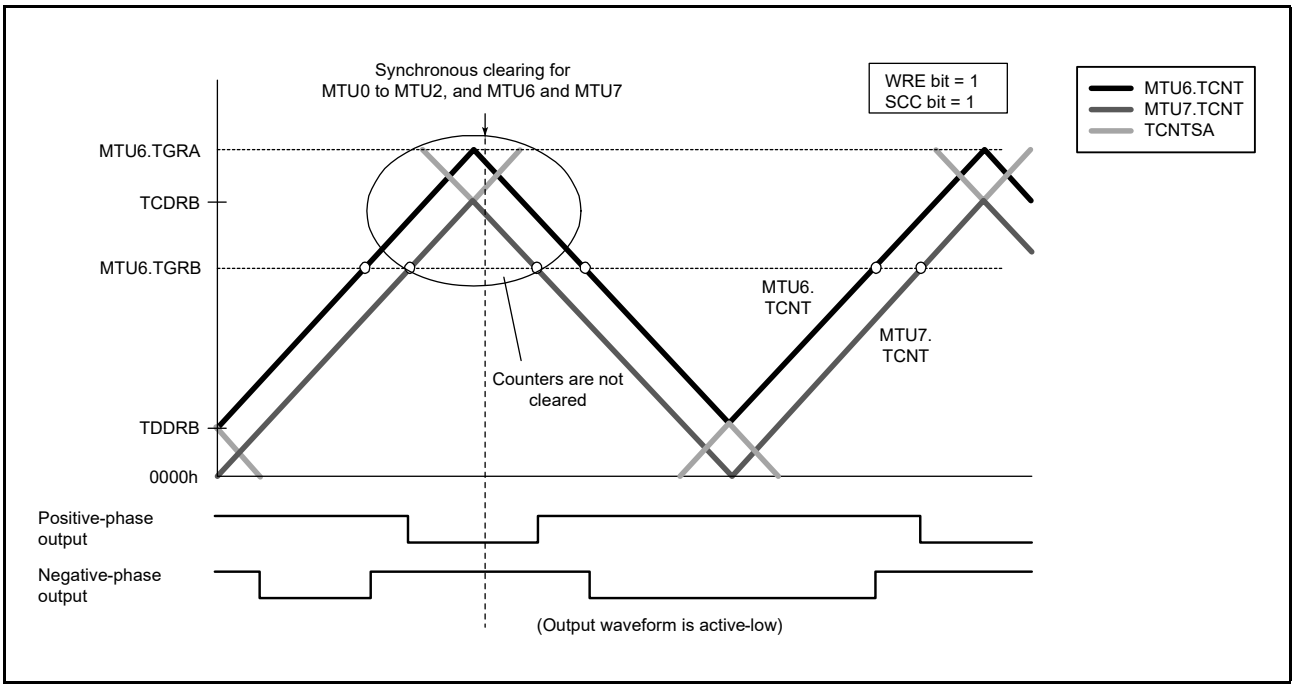


Figure 19.75 Example of Synchronous Clearing in Interval Tb at Crest (Timing (6) in Figure 19.66; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

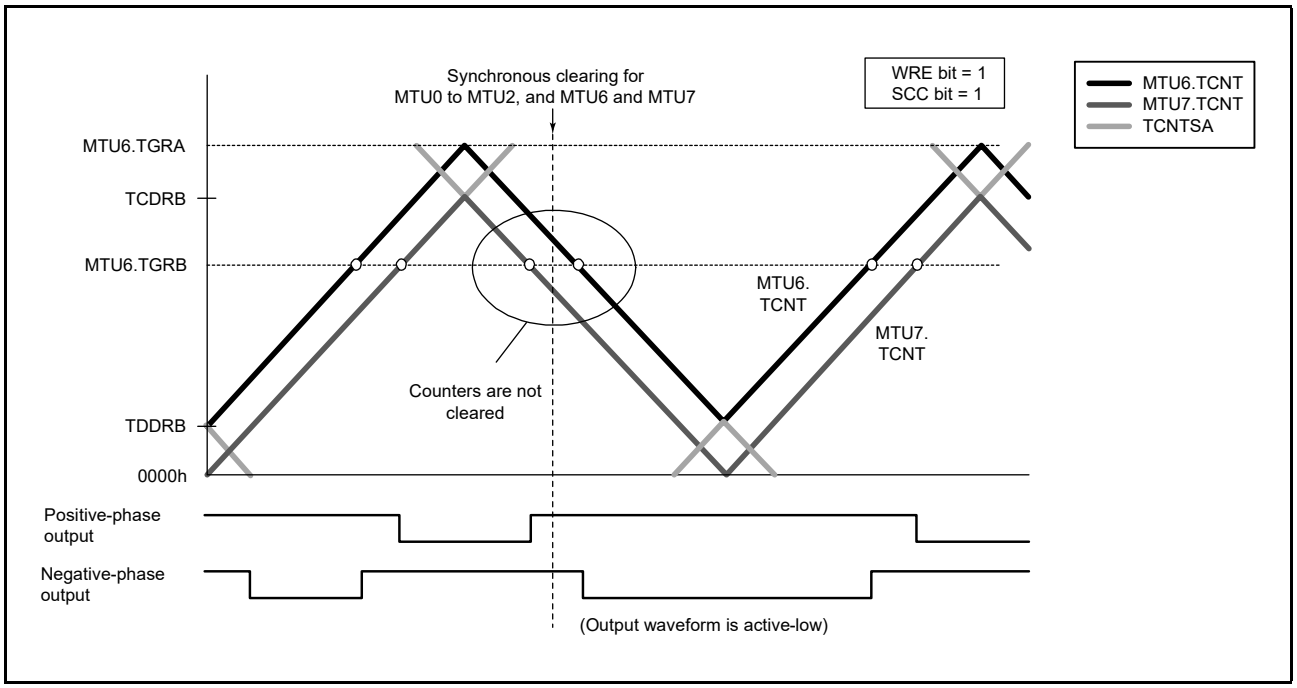


Figure 19.76 Example of Synchronous Clearing in Dead Time during Down-Counting (Timing (8) in Figure 19.66; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

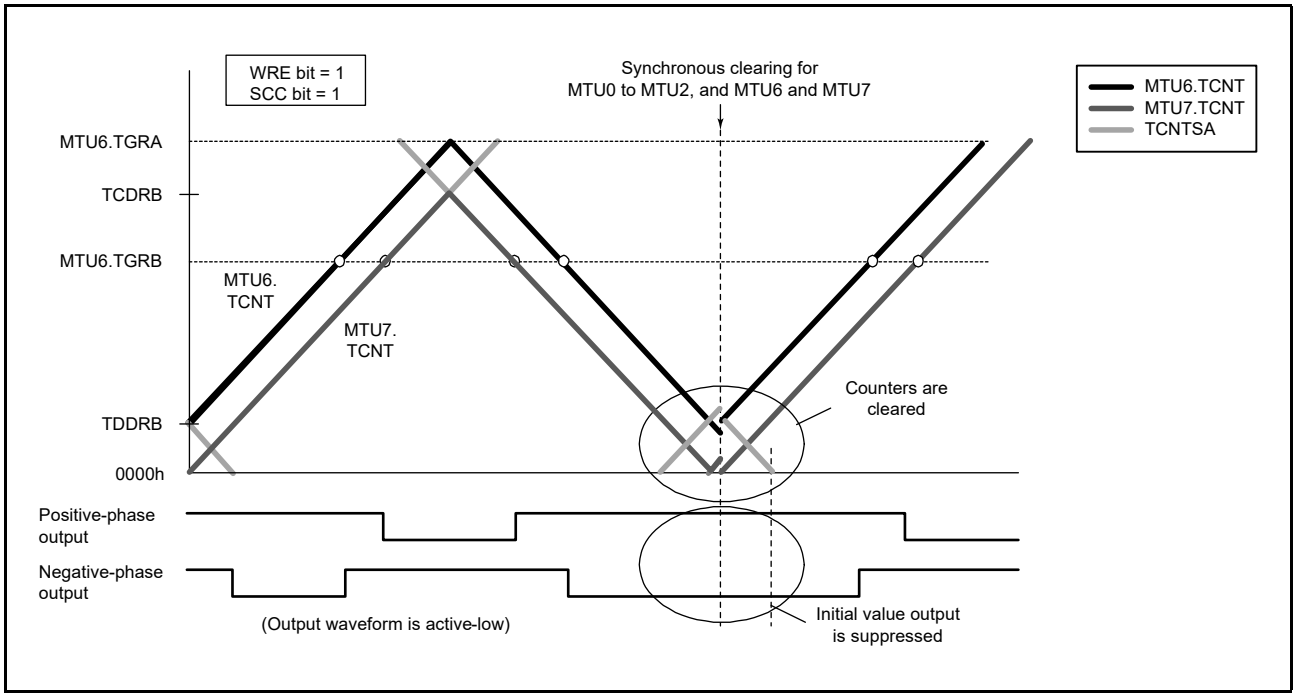


Figure 19.77 Example of Synchronous Clearing in Interval Tb at Trough (Timing (11) in Figure 19.66; Bit WRE is 1 and Bit SCC is 1 in TWCRB in MTU6 and MTU7)

(p) Counter Clearing by MTU3.TGRA (MTU6.TGRA) Compare Match

In complementary PWM mode, MTU3.TCNT, MTU4.TCNT, and TCNTSA (MTU6.TCNT, MTU7.TCNT, and TCNTSB) can be cleared by MTU3.TGRA (MTU6.TGRA) compare match when the CCE bit is set in the timer waveform control register (TWCRA or TWCRB).
Figure 19.78 illustrates an operation example.

Note 1. Use this function only in complementary PWM mode 1 (transfer at crest).
Note 2. Do not specify synchronous clearing by another channel (do not set 1 in the SYNC0 to SYNC4 or SYNC6 to SYNC7 bits in the timer synchronous register (TSYRA or TSYRB) and the CE0A to CE0D, CE1A and CE1B, or CE2A and CE2B bits in TSYCR).
Note 3. Do not set the PWM duty value to 0000h.
Note 4. Do not set the PSYE bit in timer output control register 1 (TOCR1A or TOCR1B) to 1.

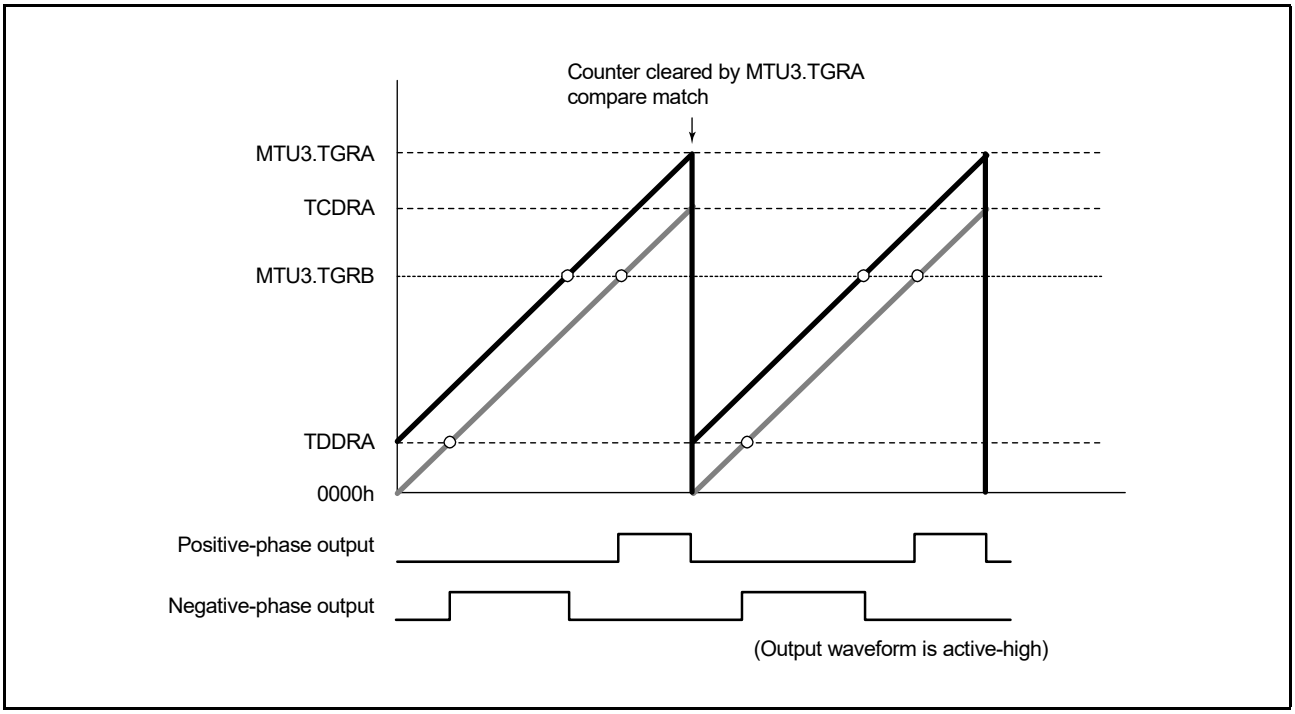


Figure 19.78 Example of Counter Clearing Operation by MTU3.TGRA Compare Match

(q) Example of Waveform Output for Driving AC Synchronous Motor (Brushless DC Motor)

In complementary PWM mode, a brushless DC motor can easily be controlled using the timer gate control register (TGCRA). Figure 19.79 to Figure 19.82 show examples of brushless DC motor driving waveforms created using TGCRA.

To switch the output phases for a 3-phase brushless DC motor by means of external signals detected with a Hall element, etc., clear the TGCRA.FB bit to 0. In this case, the external signals indicating the magnetic pole position should be input to timer input pins MTIOC0A, MTIOC0B, and MTIOC0C in MTU0 (make appropriate settings with the MPC and port mode registers (PMR) of the I/O ports). When an edge is detected at pin MTIOC0A, MTIOC0B, or MTIOC0C, the output on/off state is switched automatically.

When the TGCRA.FB bit is 1, the output on/off state is switched when the UF, VF, or WF bit in TGCRA is cleared to 0 or set to 1.

The driving waveforms are output from the 6-phase output pins for complementary PWM mode.

With this 6-phase output, while the output is turned on, chopping output is available through complementary PWM mode output function by setting the N bit or P bit in TGCRA to 1. When the N bit or P bit is 0, the level output is selected.

The active level of the 6-phase output (on output level) can be set with the OLSN and OLSP bits in the timer output control register 1A (TOCR1A) regardless of the setting of the N and P bits.

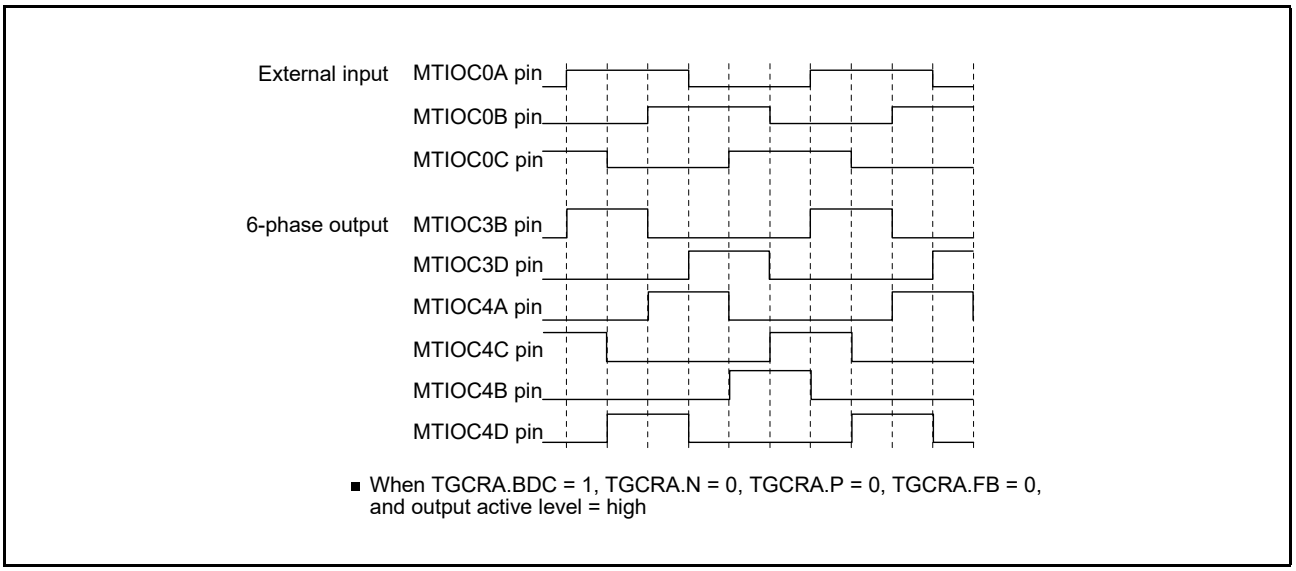


Figure 19.79 Example of Output Phase Switching by External Input (1)

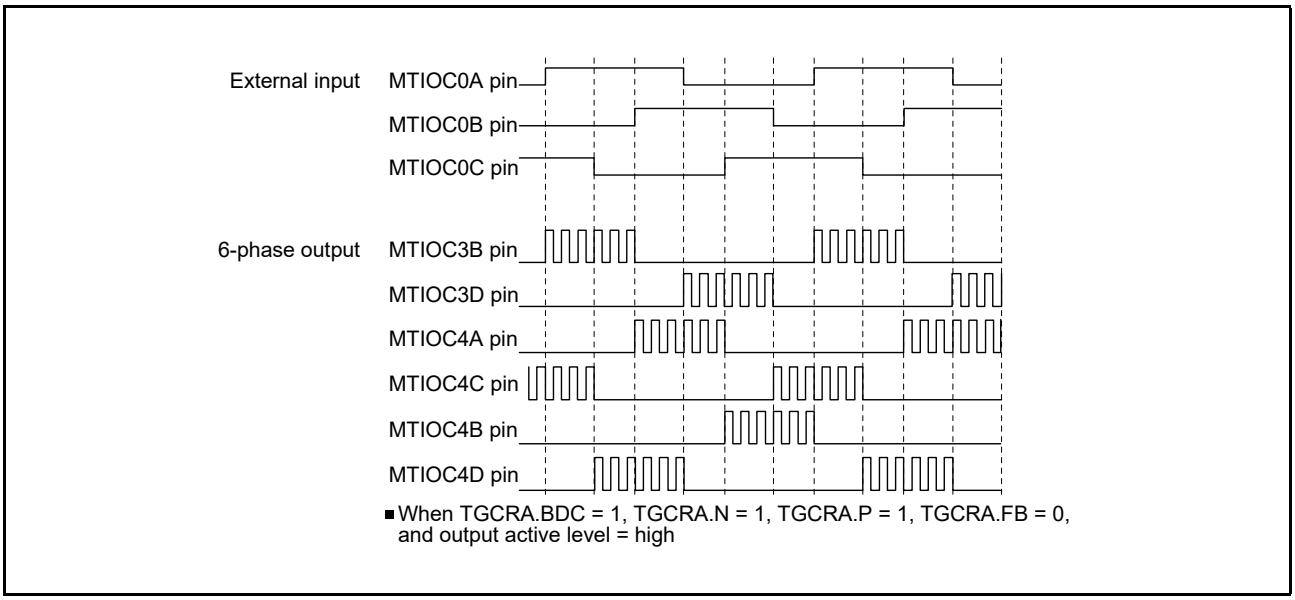


Figure 19.80 Example of Output Phase Switching by External Input (2)

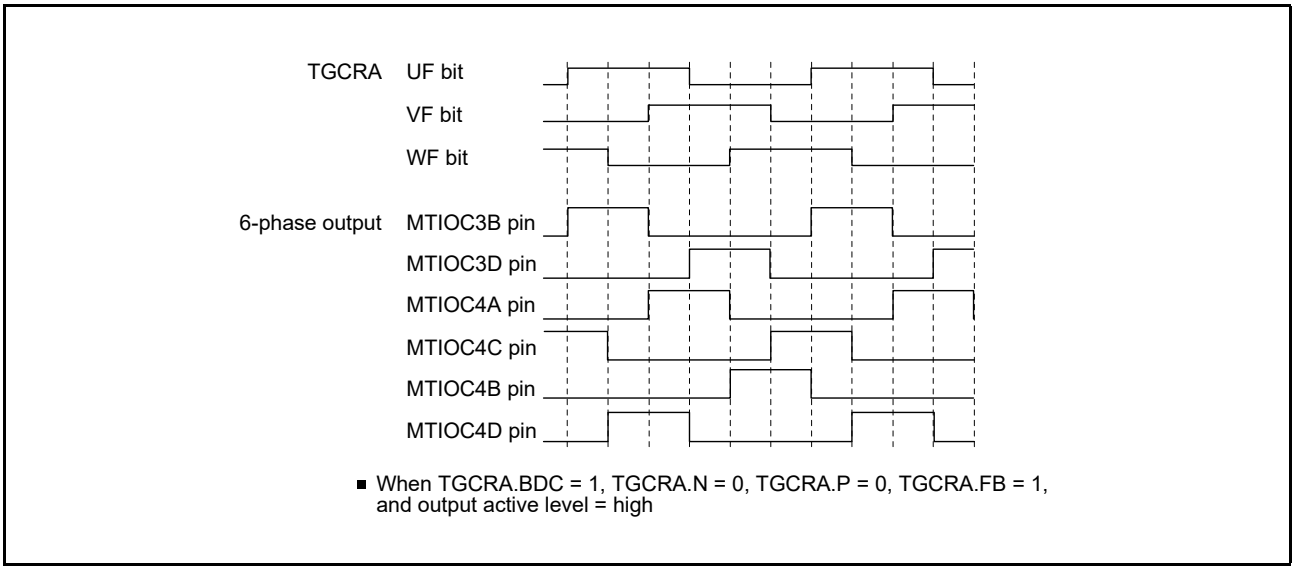


Figure 19.81 Example of Output Phase Switching through UF, VF, and WF Bit Settings (1)

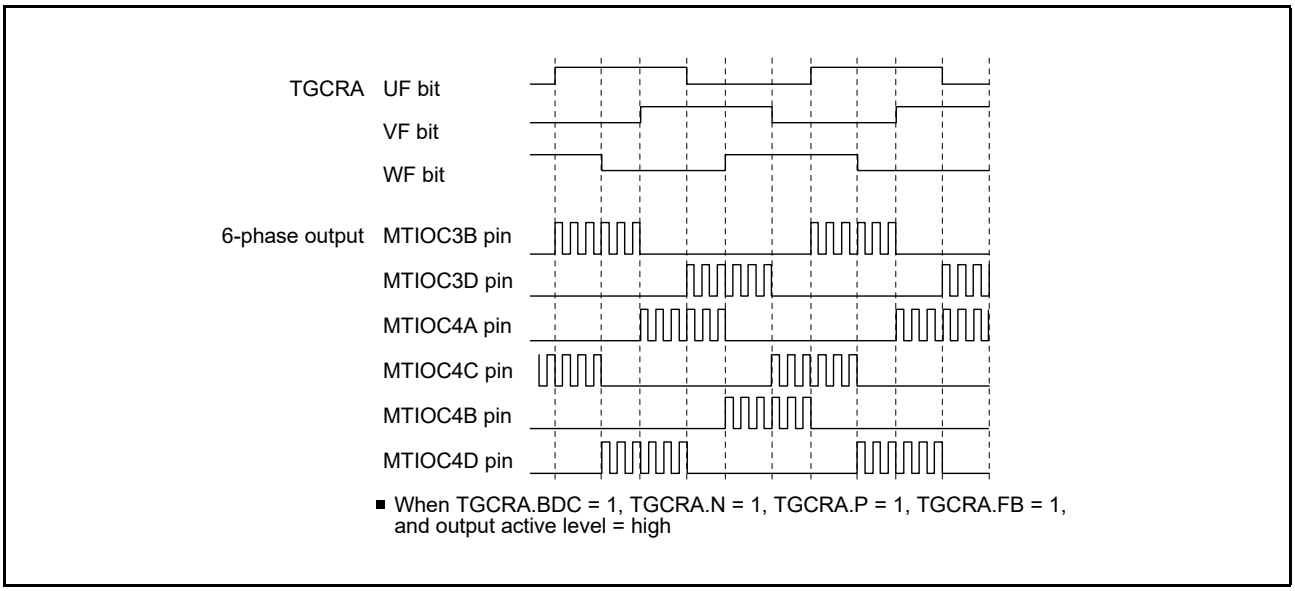


Figure 19.82 Example of Output Phase Switching through UF, VF, and WF Bit Settings (2)

(r) A/D Converter Start Request Setting

In complementary PWM mode, an A/D converter start request can be issued using MTU3.TGRA (MTU6.TGRA) compare match, MTU4.TCNT (MTU7.TCNT) underflow (trough), or compare match on a channel other than MTU3 and MTU4 (MTU6 and MTU7).
When start requests using MTU3.TGRA (MTU6.TGRA) compare match are specified, A/D conversion can be started at the crest of the MTU3.TCNT (MTU6.TCNT) count.
A/D converter start requests can be specified by setting the TTGE bit to 1 in the timer interrupt enable register (TIER).
To issue an A/D converter start request at an MTU4.TCNT (MTU7.TCNT) underflow (trough), set the TTGE2 bit in MTU4.TIER (MTU7.TIER) to 1.

(s) Double Buffer Function in Complementary PWM Mode

In complementary PWM mode 3 (transfer at the crest and trough), the PWM output setting resolution can be improved from ±2 to ±1 by setting the DRS bit in timer mode register 2 (TMDR2A or TMDR2B) to 1.
When setting buffer registers A (MTU3.TGRD, MTU4.TGRC, and MTU4.TGRD), set also buffer registers B (MTU3.TGRE, MTU4.TGRE, and MTU4.TGRF) at the same time. Each buffer register B should be set to the buffer register A value or (buffer register A value – 1). For details of the setting procedure, see section 19.3.8 (1) Example of Complementary PWM Mode Setting Procedure.

Note: When a buffer register B is set to the buffer register A value, symmetric PWM waveforms are output. When a buffer register B is set to (buffer register A value – 1), asymmetric PWM waveforms are output.

Figure 19.83 shows an example of double buffer operation.
Each register data is transferred as follows.

- After MTU4.TGRD (buffer A) is written to, data is transferred from MTU4.TGRD (buffer A) to Temp3A (temporary A) and from MTU4.TGRF (buffer B) to Temp3B (temporary B).
- With timing (1) in the figure, data is transferred from Temp3A (temporary A) to MTU4.TGRB (compare).
- With timing (2) in the figure, data is transferred from Temp3B (temporary B) to MTU4.TGRB (compare).

In the crest interval (Tb interval at crest), the compare register and temporary register A are valid; in the trough interval (Tb interval at trough), the compare register and temporary register B are valid.

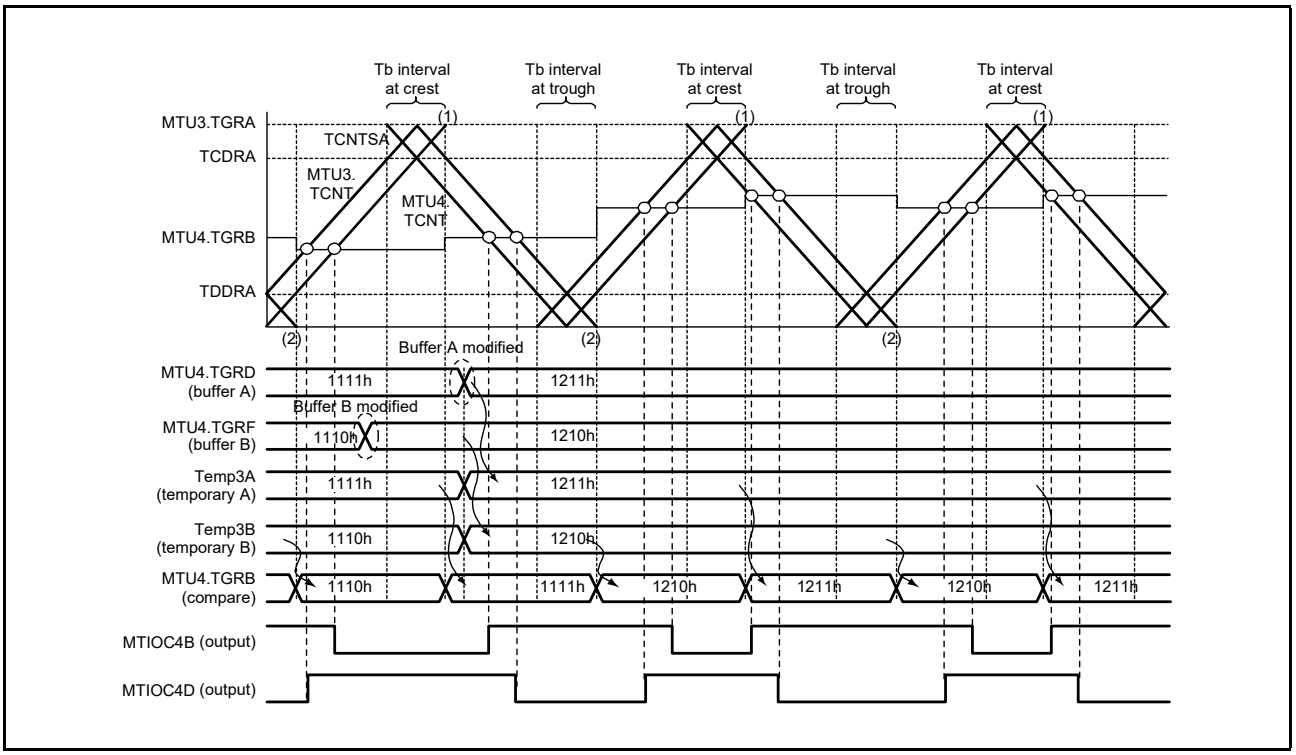


Figure 19.83 Example of Double Buffer Operation

Figure 19.84 shows an example when the buffer write value is smaller than the TDDRA value, and Figure 19.85 shows an example when the write value is greater than TCDRA.
In the crest interval, the output is controlled according to the compare match with the compare register or temporary register A; in the trough interval, the output is controlled according to the compare match with the compare register or temporary register B.

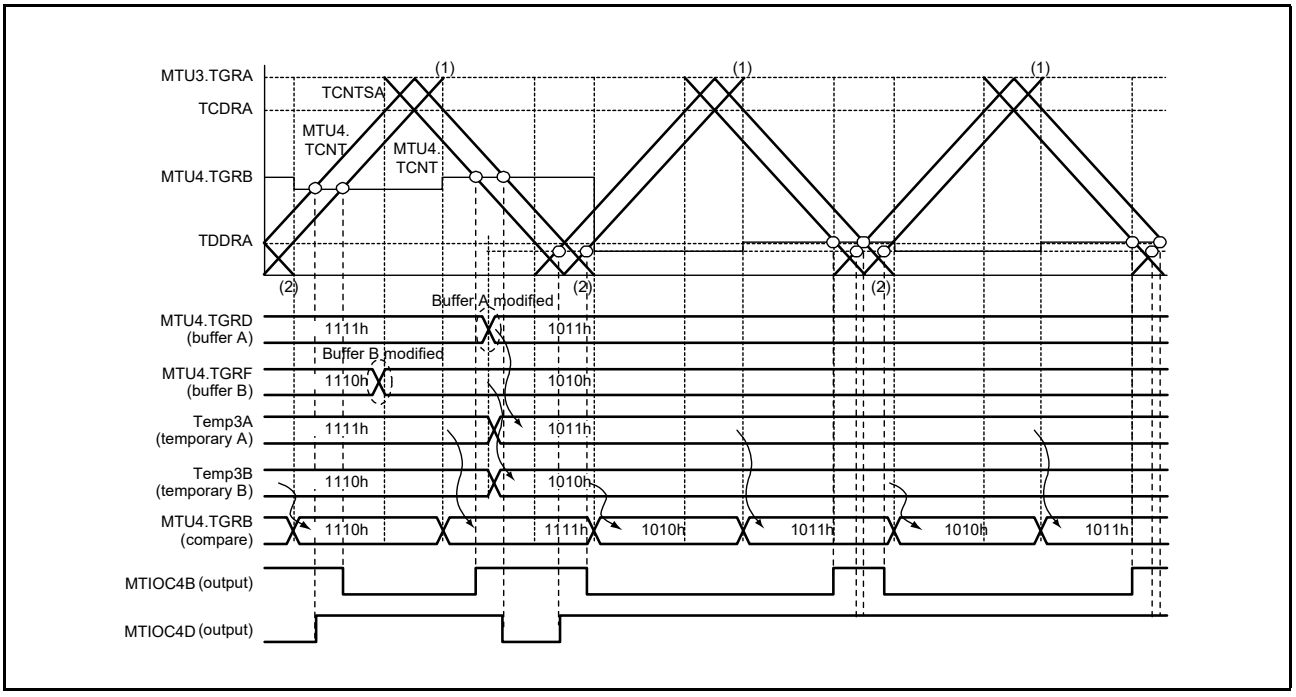


Figure 19.84 Example of Double Buffer Operation (Buffer Write Value is Smaller than TDDRA)

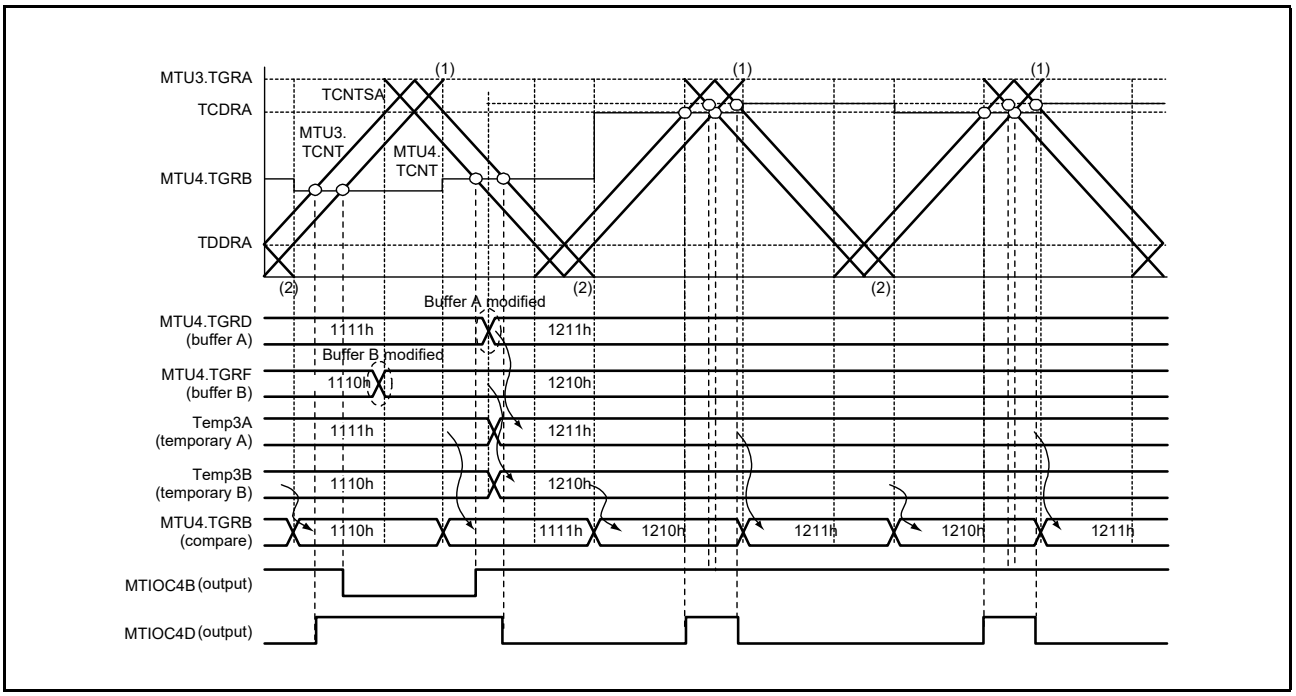


Figure 19.85 Example of Double Buffer Operation (Buffer Write Value is Greater than TCDRA)

(3) Interrupt Skipping Function 1 in Complementary PWM Mode

Interrupts TGIA3 (TGIA6) (at the crest) and TCIV4 (TCIV7) (at the trough) in MTU3 and MTU4 (MTU6 and MTU7) can be skipped up to seven times by making settings in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B).

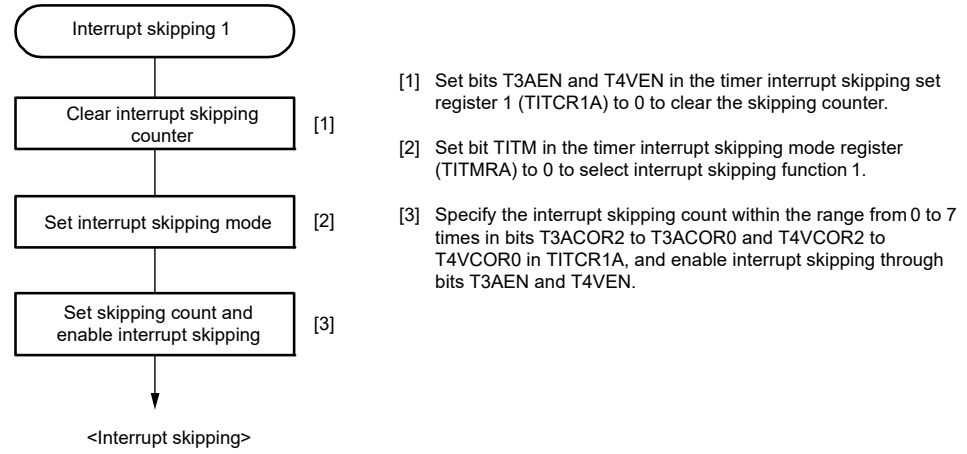
Transfers from a buffer register to a temporary register or a compare register can be skipped in coordination with interrupt skipping by making settings in the timer buffer transfer register (TBTERA or TBTERB). For the linkage with buffer registers, see section (c), Buffer Transfer Control Linked with Interrupt Skipping below.

A/D converter start requests generated by the A/D converter start request delaying function can also be skipped in coordination with interrupt skipping by making settings in the timer A/D converter request control register (MTU4.TADCR or MTU7.TADCR). For the linkage with the A/D converter start request delaying function, see section 19.3.9, A/D Converter Start Request Delaying Function.

The timer interrupt skipping setting register 1 (TITCR1A or TITCR1B) should be set while interrupt skipping function 1 is selected by setting the TITM bit to 0 in the timer interrupt skipping mode register (TITMRA or TITMRB), TGIA3 (TGIA6) and TCIV4 (TCIV7) interrupt requests are disabled by the settings of MTU3.TIER and MTU4.TIER (MTU6.TIER and MTU7.TIER), and a compare match is not generated. Before changing the skipping count, be sure to clear the T3AEN (T6AEN) and T4VEN (T7VEN) bits to 0 to clear the skipping counter.

(a) Example of Interrupt Skipping Function 1 Setting Procedure

Figure 19.86 shows an example of the interrupt skipping function 1 setting procedure. Figure 19.87 shows the periods during which interrupt skipping count can be changed.



Note: The setting of TITCR1A must be done while the TGIA3 and TCIV4 interrupt requests are disabled by the settings of MTU3.TIER and MTU4.TIER under the conditions in which a compare match is not generated. Before changing the skipping count, be sure to clear the T3AEN and T4VEN bits to 0 to clear the skipping counter.

Figure 19.86 Example of Interrupt Skipping Function 1 Setting Procedure

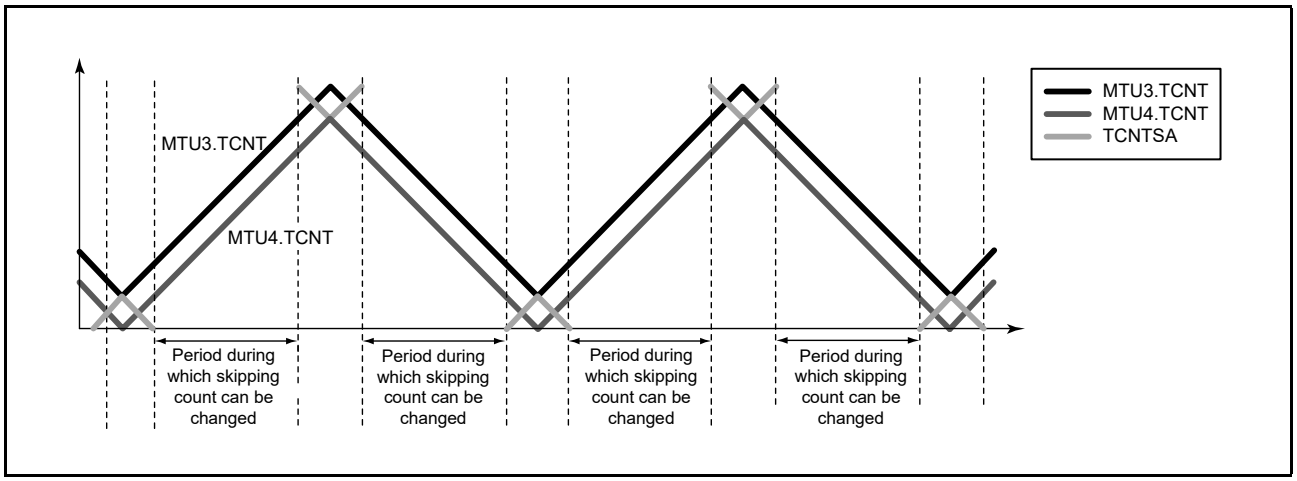


Figure 19.87 Periods during which Interrupt Skipping Count can be Changed

(b) Example of Interrupt Skipping Function 1

Figure 19.88 shows an example of TGIA3 (TGIA6) interrupt skipping in which the interrupt skipping count is set to three by the T3ACOR (T6ACOR) bits and the T3AEN (T6AEN) bit is set to 1 in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B).

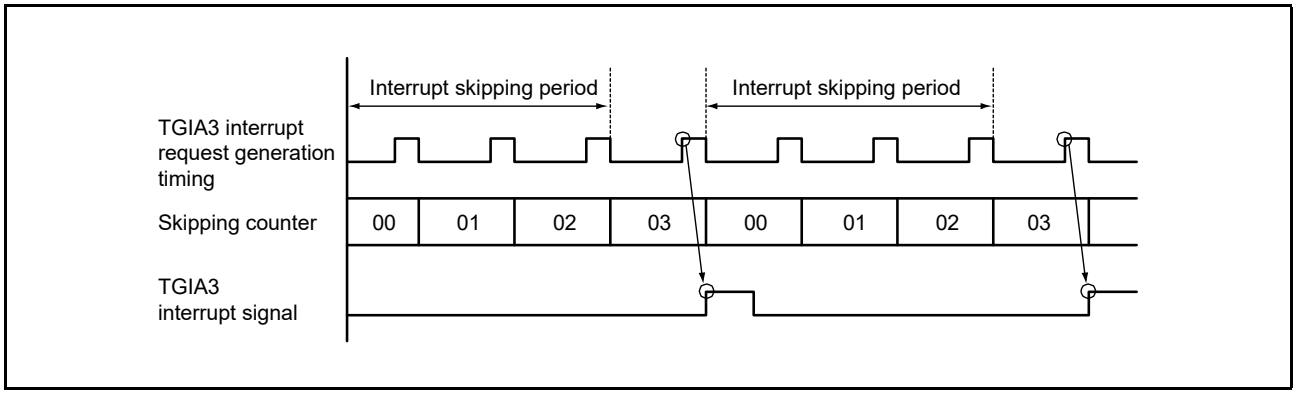


Figure 19.88 Example of Interrupt Skipping Function 1

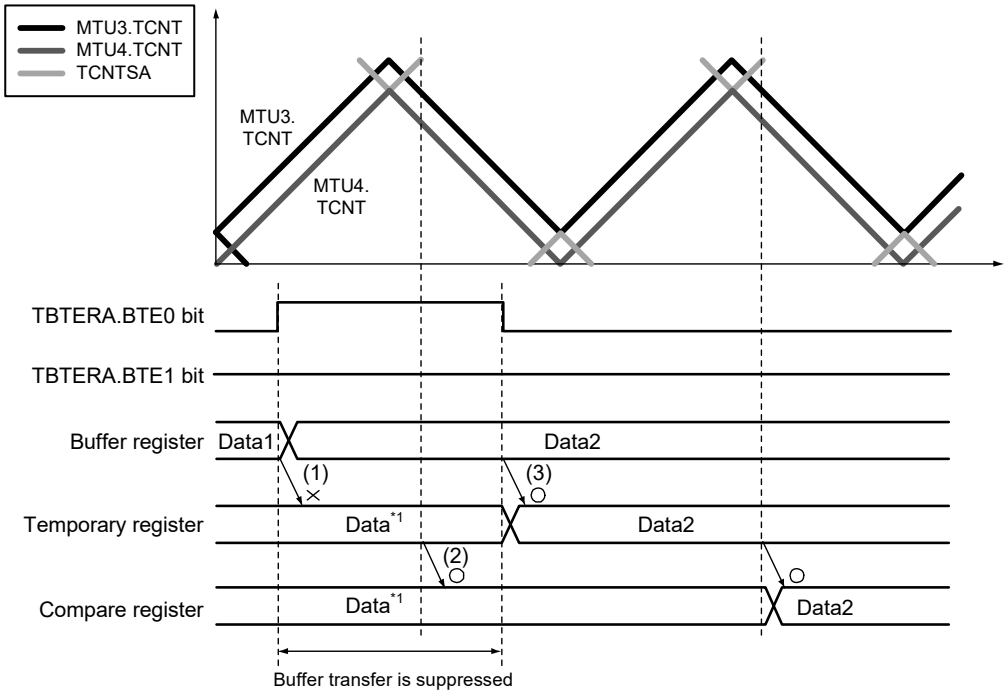
(c) Buffer Transfer Control Linked with Interrupt Skipping

In complementary PWM mode, whether to transfer data from a buffer register to a temporary register and whether to link the transfer with interrupt skipping can be specified with the BTE[1:0] bits in the timer buffer transfer set register (TBTERA or TBTERB).

Figure 19.89 shows an example of operation when buffer transfer is disabled (BTE[1:0] = 01b). While this setting is valid, data is not transferred from the buffer register to the temporary register.

Figure 19.90 shows an example of operation when buffer transfer is linked with interrupt skipping (BTE[1:0] = 10b). While this setting is valid, data is not transferred from the buffer register outside the buffer transfer-enabled period. Note that the buffer transfer-enabled period depends on the T3AEN (T6AEN) and T4VEN (T7VEN) bit settings in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B). Figure 19.91 shows the relationship between the T3AEN (T6AEN) and T4VEN (T7VEN) bit settings in TITCR1A (TITCR1B) and buffer transfer-enabled period.

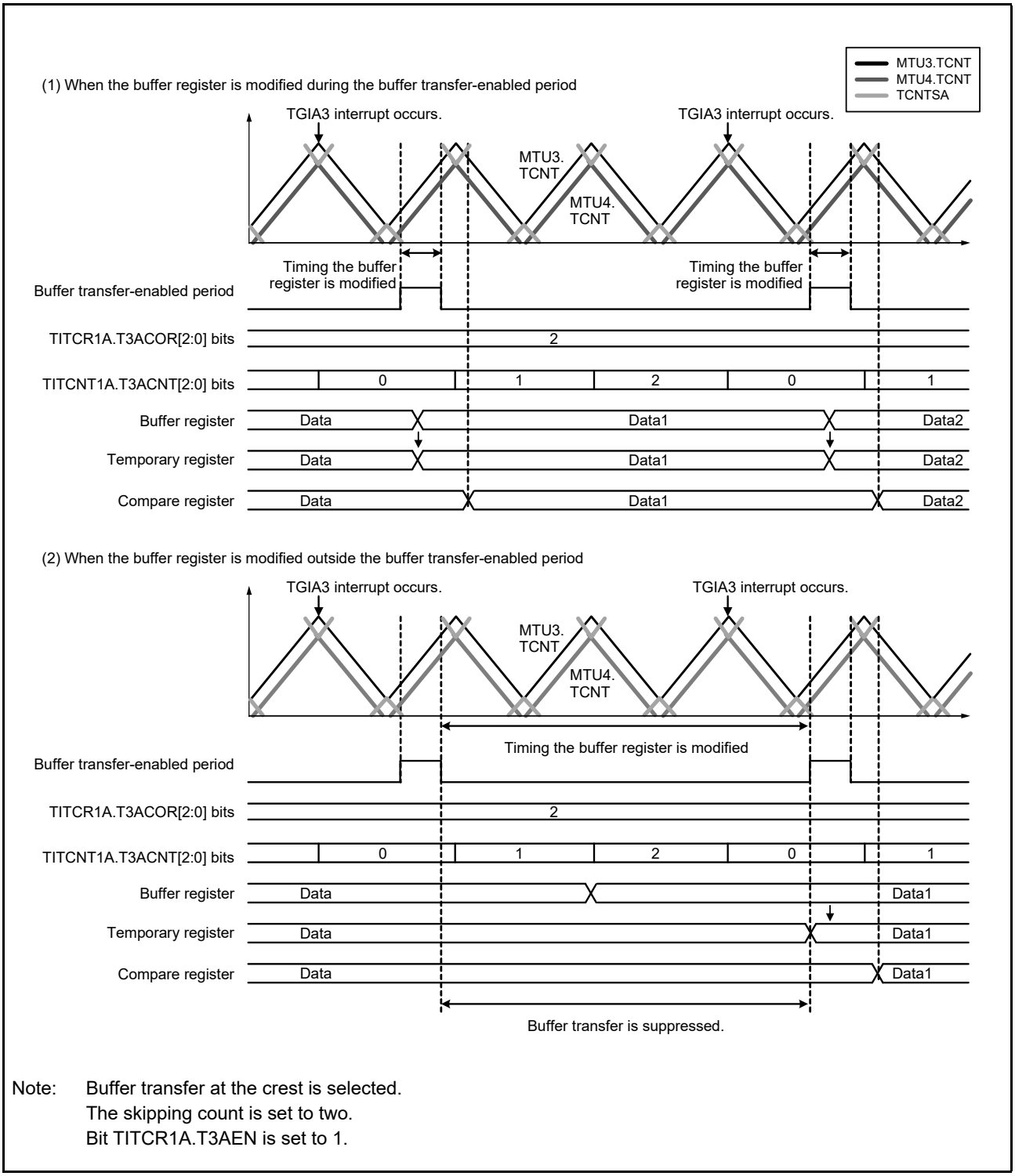
Note: This function must always be used in combination with interrupt skipping function 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register 1 (TITCR1A or TITCR1B) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that buffer transfer is not linked with interrupt skipping (clear the BTE1 bit in TBTERA or TBTERB to 0).
If buffer transfer is linked with interrupt skipping while interrupt skipping is disabled, buffer transfer is never performed.



[Legend]
(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE[1:0] in TBTERA are set to 01b).
(2) Data is transferred from the temporary register to the compare register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

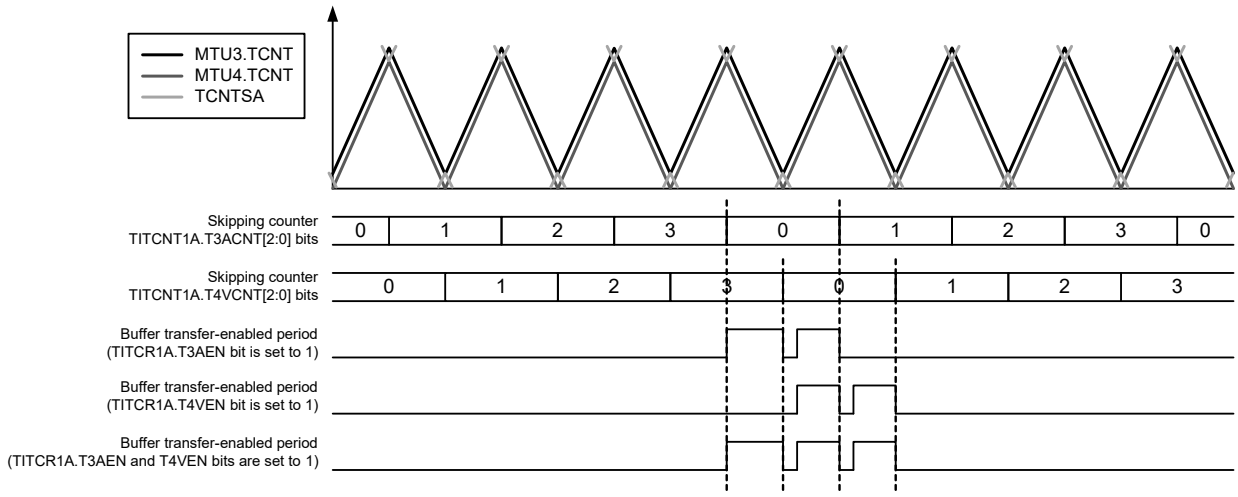
Note 1. When buffer transfer at the crest is selected.

Figure 19.89 Example of Operation when Buffer Transfer is Disabled (BTE[1:0] = 01b)



Note: Buffer transfer at the crest is selected.
The skipping count is set to two.
Bit TITCR1A.T3AEN is set to 1.

Figure 19.90 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE[1:0] = 10b)



Note: The skipping count is set to three.
Buffer transfer at the crest and trough is selected.

Figure 19.91 Relationship between Bits T3AEN and T4VEN in TITCR1A and Buffer Transfer-Enabled Period

(4) Complementary PWM Mode Output Protection Functions

The MTU provides the following protection functions for complementary PWM mode output.

(a) Register and Counter Miswrite Prevention Function

With the exception of the buffer registers, which can be modified, access by the CPU can be enabled or disabled for the mode registers, control registers, compare registers, and counters used in complementary PWM mode by means of the RWE bit in the timer read/write enable register (TRWERA or TRWERB). The applicable registers are some of the registers in MTU3, MTU4, MTU6, and MTU7 shown below:

43 registers in total
MTU3.TCR, MTU4.TCR, MTU3.TMDR1, MTU4.TMDR1, MTU3.TIORH,
MTU4.TIORH, MTU3.TIORL, MTU4.TIORL, MTU3.TIER, MTU4.TIER,
MTU3.TCNT, MTU4.TCNT, MTU3.TGRA, MTU4.TGRA, MTU3.TGRB, MTU4.TGRB,
TOERA, TOCR1A, TOCR2A, TGCRA, TCDRA, TDDRA
MTU6.TCR, MTU7.TCR, MTU6.TMDR1, MTU7.TMDR1, MTU6.TIORH, MTU7.TIORH,
MTU6.TIORL, MTU7.TIORL, MTU6.TIER, MTU7.TIER, MTU6.TCNT, MTU7.TCNT,
MTU6.TGRA, MTU7.TGRA, MTU6.TGRB, MTU7.TGRB,
TOERB, TOCR1B, TOCR2B, TCDRB, and TDDRB

This function can disable CPU access to the mode registers, control registers, and counters to prevent miswriting due to CPU runaway. In the access-disabled state, the applicable registers are read as undefined and writing to these registers is ignored.

(b) Halting of PWM Output by External Signal

The 6-phase PWM output pins can be set to the high-impedance state automatically by inputting specified external signals.

See section 20, Port Output Enable 3 (POE3), for details.

(c) Halting of PWM Output when Oscillator is Stopped

Upon detecting that the clock input to this MCU has stopped, the 6-phase PWM output pins are automatically set to the high-impedance state. Note that the pin states are not guaranteed when the clock is restarted.

See section 7.4, Oscillation Stop Detection Function.

19.3.9 A/D Converter Start Request Delaying Function

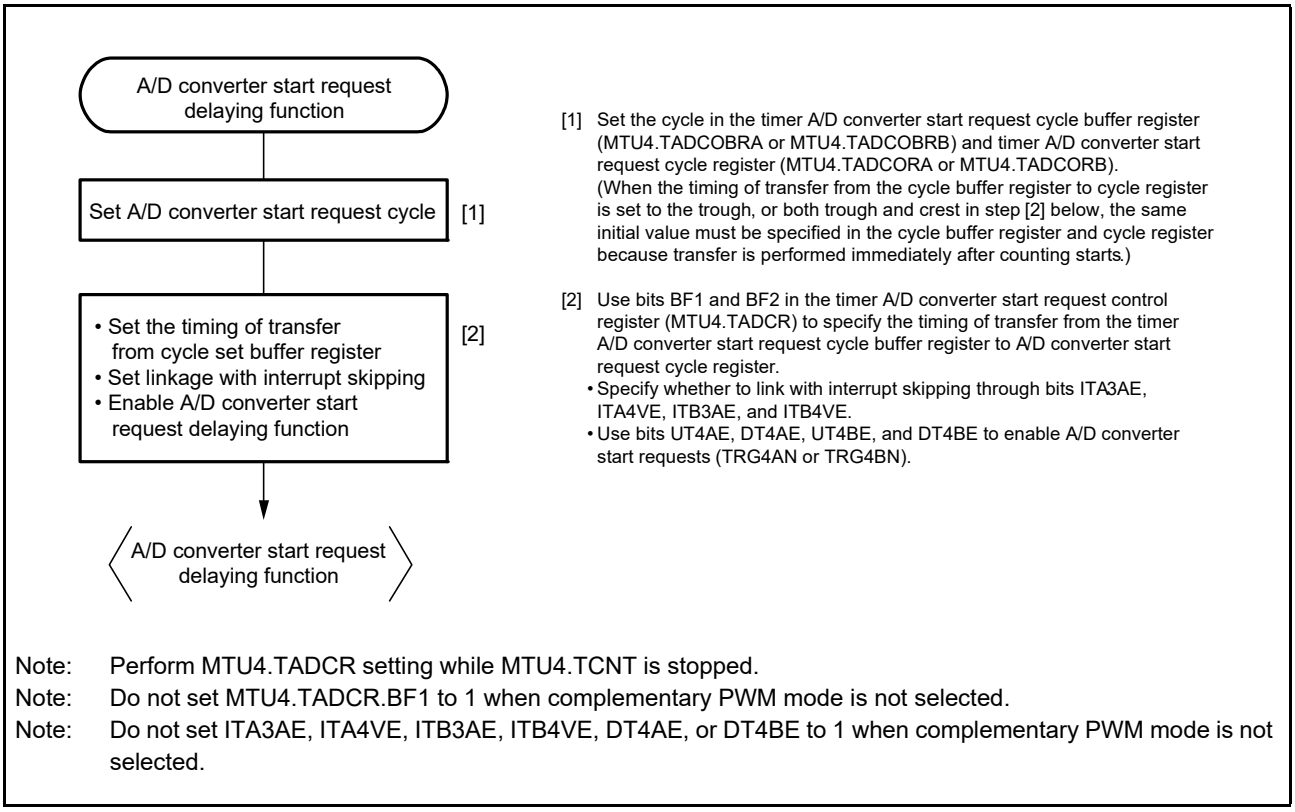
A/D converter start requests can be issued in MTU4 or MTU7 by making settings in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR), timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB), and timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB).

The A/D converter start request delaying function compares MTU4.TCNT with MTU4.TADCORA or MTU4.TADCORB (MTU7.TCNT with MTU7.TADCORA or MTU7.TADCORB), and when their values match, the function issues a respective A/D converter start request (TRG4AN or TRG4BN (TRG7AN or TRG7BN)).

A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be skipped in coordination with interrupt skipping by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in MTU4.TADCR (the ITA6AE, ITA7VE, ITB6AE, and ITB7VE bits in MTU7.TADCR).

(1) Example of Procedure for Specifying A/D Converter Start Request Delaying Function

Figure 19.92 shows an example of procedure for specifying the A/D converter start request delaying function.



Note: Perform MTU4.TADCR setting while MTU4.TCNT is stopped.
Note: Do not set MTU4.TADCR.BF1 to 1 when complementary PWM mode is not selected.
Note: Do not set ITA3AE, ITA4VE, ITB3AE, ITB4VE, DT4AE, or DT4BE to 1 when complementary PWM mode is not selected.

Figure 19.92 Example of Procedure for Specifying A/D Converter Start Request Delaying Function (MTU3 and MTU4)

(2) Basic Example of A/D Converter Start Request Delaying Function Operation

Figure 19.93 shows a basic example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when the trough of MTU4.TCNT (MTU7.TCNT) is specified for the buffer transfer timing and an A/D converter start request signal is output during MTU4.TCNT (MTU7.TCNT) down-counting.

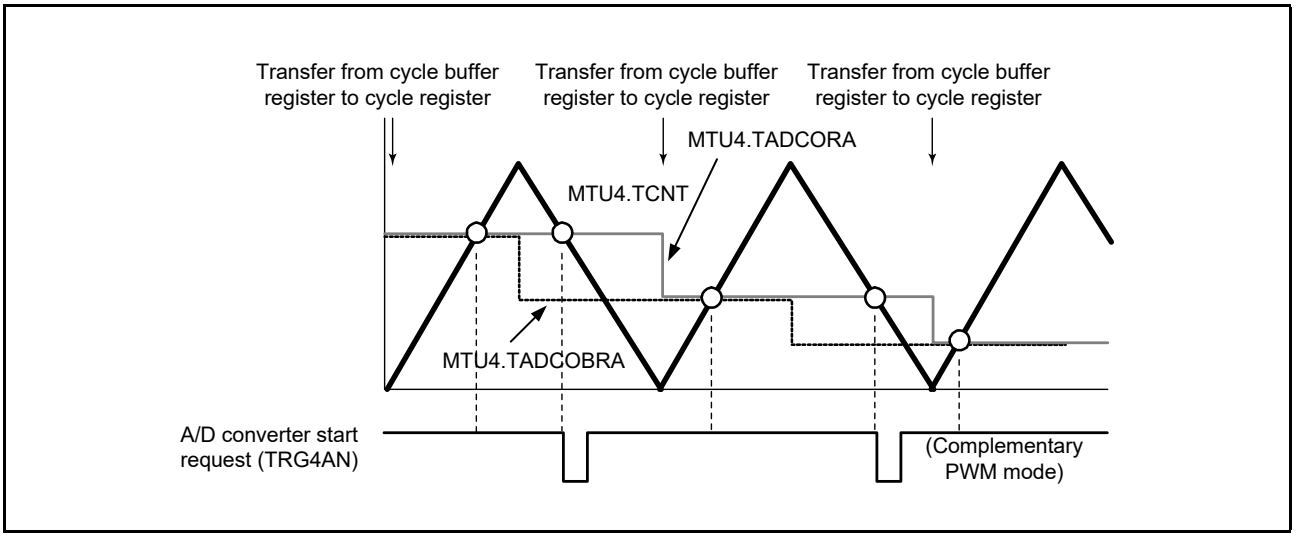


Figure 19.93 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation

(3) Buffer Transfer

The data in the timer A/D converter start request cycle set registers (MTU4.TADCORA and MTU4.TADCORB, or MTU7.TADCORA and MTU7.TADCORB) is updated by writing data to the timer A/D converter start request cycle set buffer registers (MTU4.TADCOBRA and MTU4.TADCOBRB, or MTU7.TADCOBRA and MTU7.TADCOBRB). Data is transferred from the buffer registers to the respective cycle set registers at the timing selected with the BF[1:0] bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).
In complementary PWM mode, data is also transferred from the timer A/D converter start request cycle set buffer registers to the timer A/D converter start request cycle set registers when timer general register D (MTU4.TGRD or MTU7.TGRD) is updated.

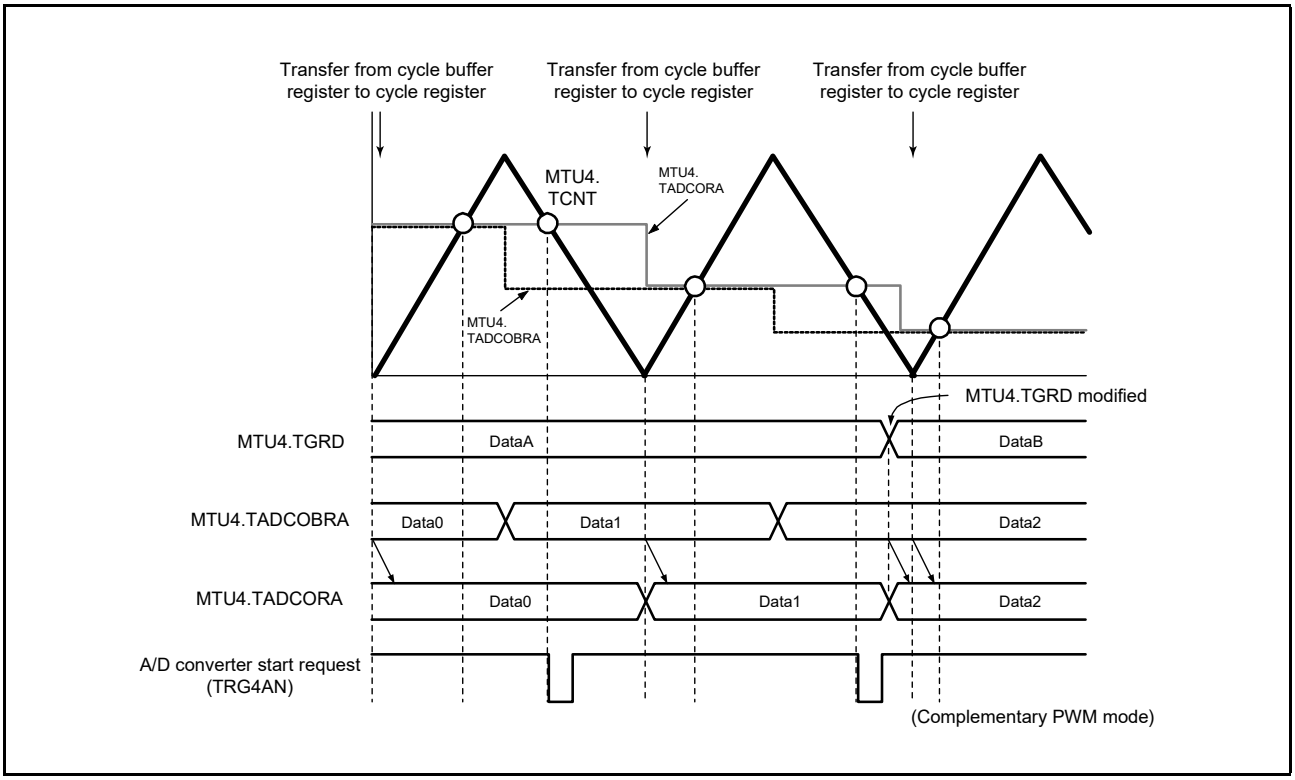
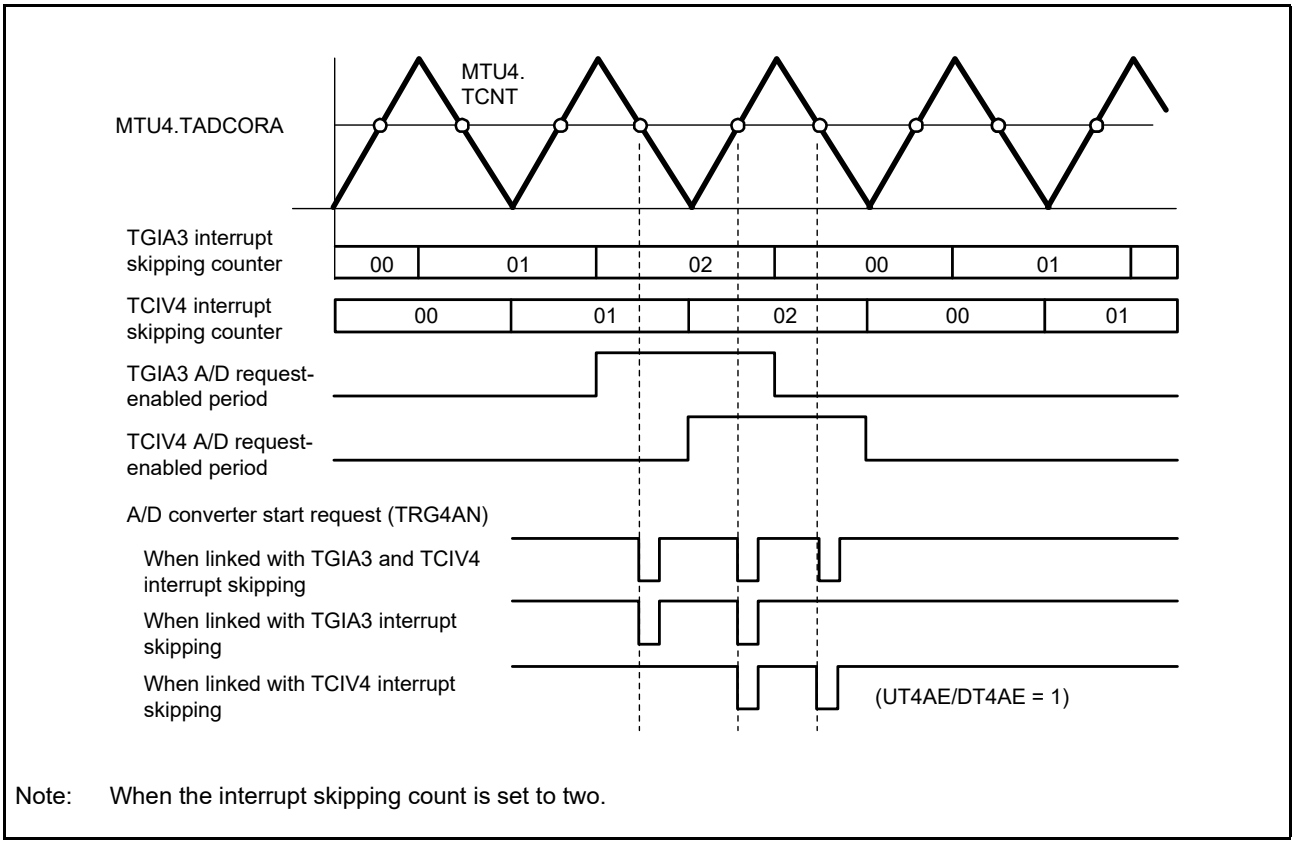


Figure 19.94 Example of A/D Converter Start Request Signal (TRG4AN) and Buffer Transfer Operation

(4) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 1

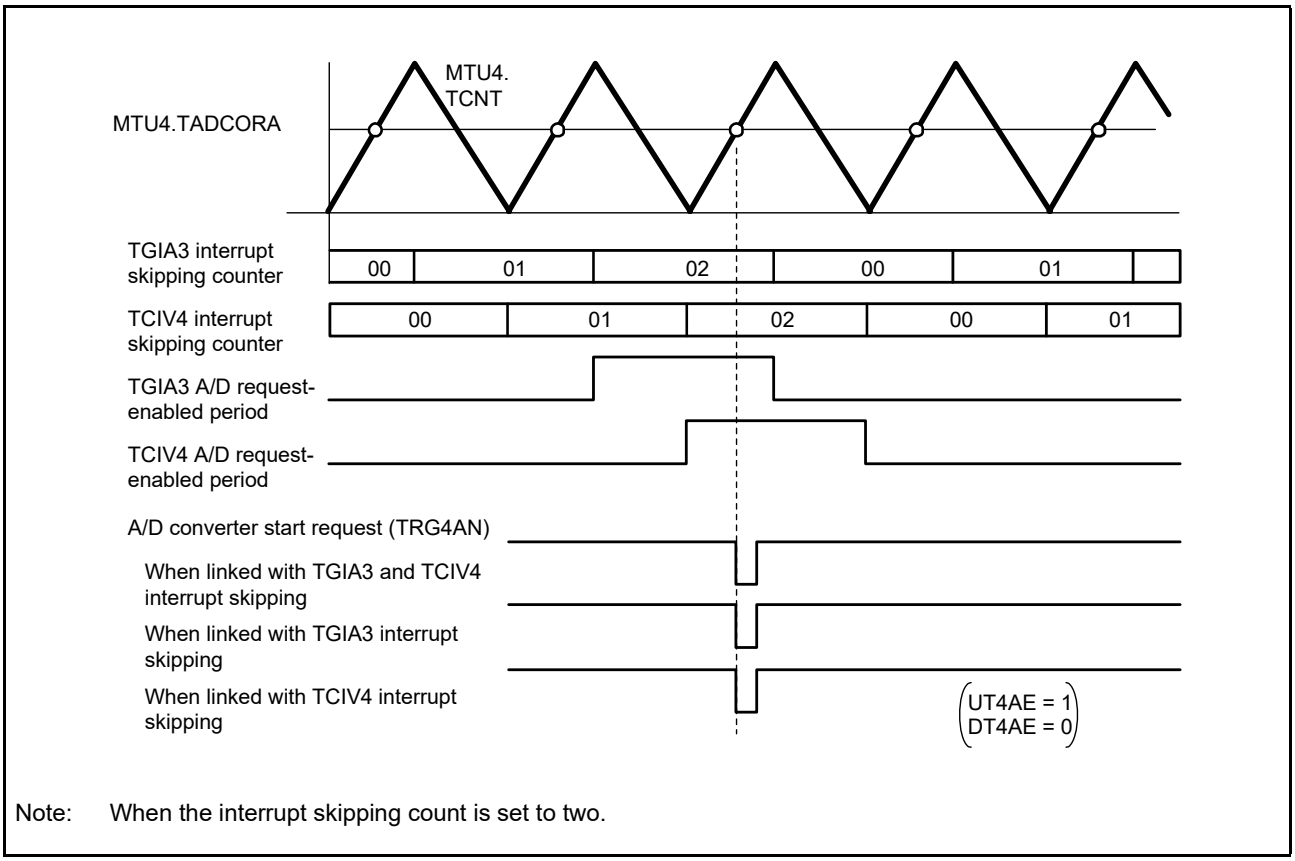
A/D converter start requests (TRG4AN and TRG4BN (TRG7AN and TRG7BN)) can be issued in coordination with interrupt skipping 1 by making settings in the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR or MTU7.TADCR).
Figure 19.95 shows an example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and down-counting and A/D converter start requests are linked with interrupt skipping 1.
Figure 19.96 shows another example of A/D converter start request signal (TRG4AN (TRG7AN)) operation when TRG4AN (TRG7AN) output is enabled during MTU4.TCNT (MTU7.TCNT) up-counting and A/D converter start requests are linked with interrupt skipping 1.

Note: This function should be used in combination with interrupt skipping 1.
When interrupt skipping is disabled (the T3AEN and T4VEN (T6AEN and T7VEN) bits in the timer interrupt skipping set register (TITCR1A (TITCR1B)) are cleared to 0 or the skipping count set bits (T3ACOR and T4VCOR (T6ACOR and T7VCOR)) in TITCR1A (TITCR1B) are cleared to 0), make sure that A/D converter start requests are not linked with interrupt skipping 1 (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE (ITA6AE, ITA7VE, ITB6AE, and ITB7VE) bits in the timer A/D converter start request control register (MTU4.TADCR (MTU7.TADCR)) to 0).
When this function is used, MTU4.TADCORA and MTU4.TADCORB (MTU7.TADCORA and MTU7.TADCORB) should be set with the value ranging 0002h to the value set in TCDRA minus 2 (value set in TCDRB minus 2).



Note: When the interrupt skipping count is set to two.

Figure 19.95 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE and DT4AE = 1)



Note: When the interrupt skipping count is set to two.

Figure 19.96 Example of A/D Converter Start Request Signal (TRG4AN) Operation Linked with Interrupt Skipping Function 1 (UT4AE = 1, DT4AE = 0)

(5) A/D Converter Start Request Delaying Function Linked with Interrupt Skipping Function 2

By setting the TITM bit to 1 in the timer interrupt skipping mode register (TITMRA or TITMRB), the counter starts down-counting from the value (0 to 7) set in the TRG4COR[2:0] (TRG7COR[2:0]) bits in timer interrupt skipping set register 2 (TITCR2A (TITCR2B)) every time an A/D converter start trigger (TGR4AN or TRG4BN (TGR7AN or TRG7BN)) is generated. When the counter value reaches 0 and is reloaded, the TRG4AN and TRG4BN (TRG7AN and TRG7BN) interrupts become valid and an A/D converter start request signal (TRG4ABN (TRG7ABN)) is output.
This function is valid only when the A/D converter request delaying function is enabled.

(a) Example of Procedure for Setting Interrupt Skipping Function 2

Figure 19.97 shows an example of procedure for setting interrupt skipping function 2.

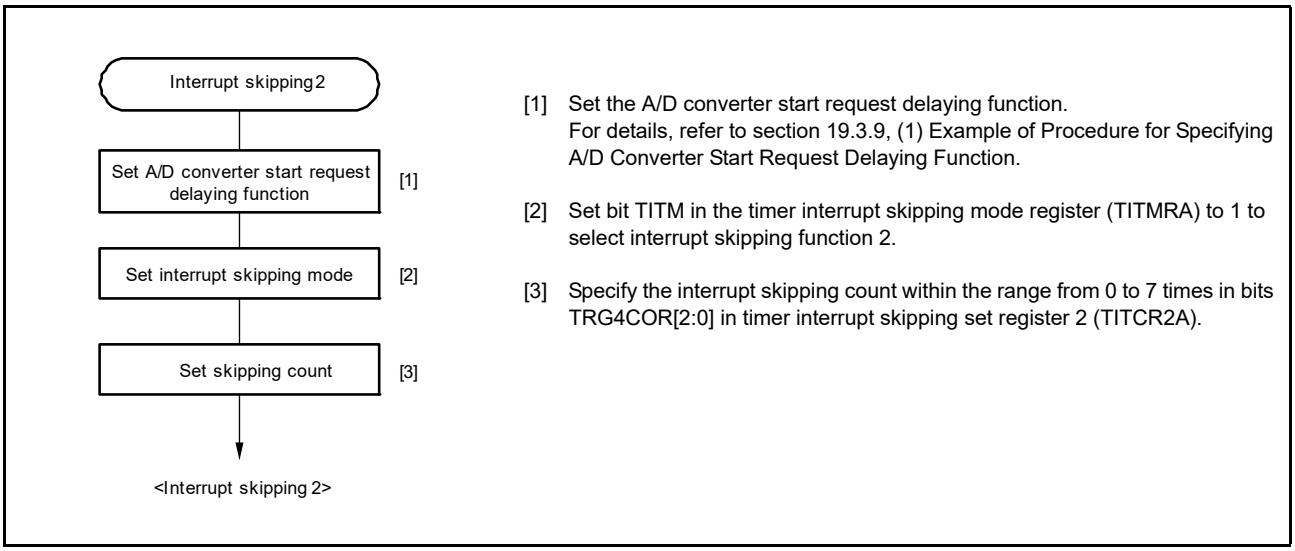


Figure 19.97 Example of Procedure for Setting Interrupt Skipping Function 2

(b) Example of Interrupt Skipping Function 2 Operation

Figure 19.98 shows an example of interrupt skipping 2 operation.

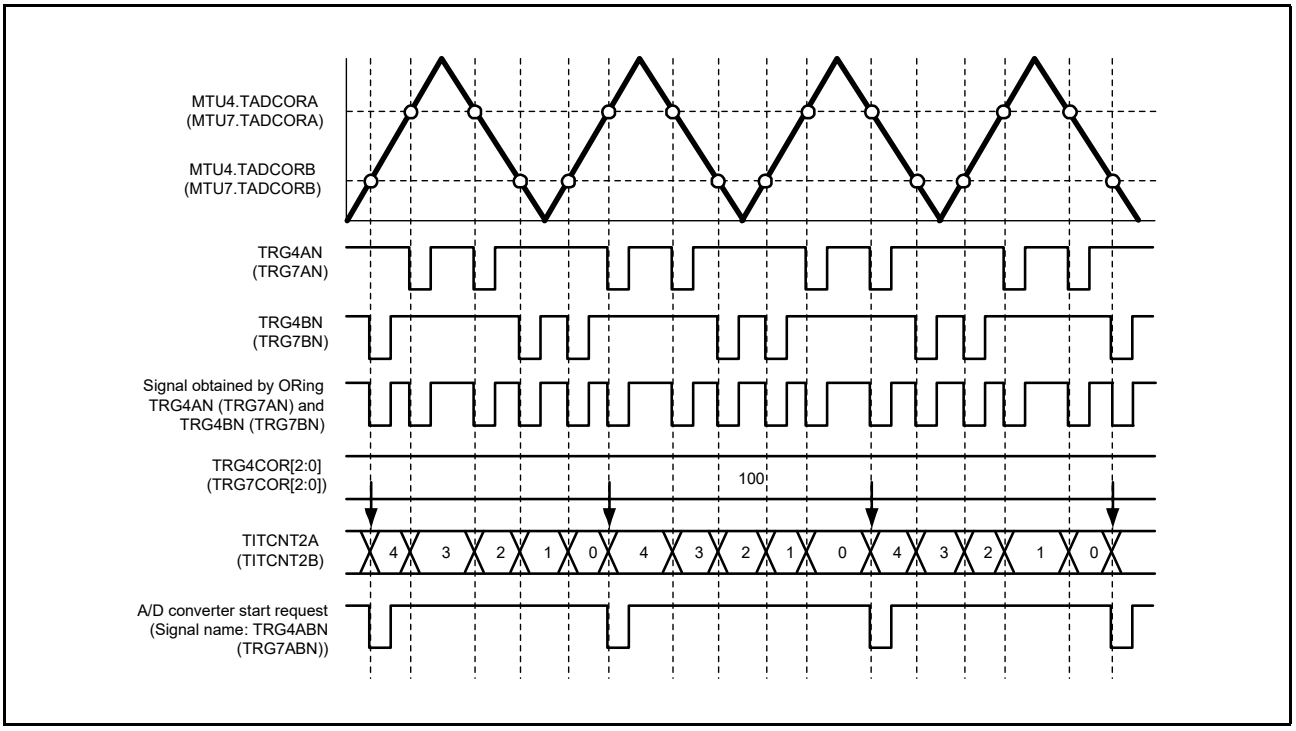


Figure 19.98 Example of Interrupt Skipping 2 Operation (Skipping Count is Set to Four)

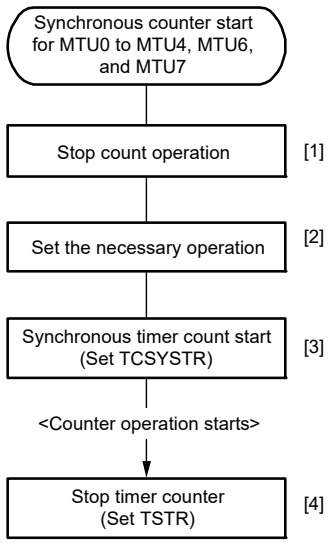
19.3.10 Synchronous Operation of MTU0 to MTU4, MTU6, and MTU7

(1) Synchronous Counter Start for MTU0 to MTU4, MTU6, and MTU7

The counters in MTU0 to MTU4, MTU6, and MTU7 can be started synchronously by making the TCSYSTR settings.

(a) Example of Procedure for Setting Synchronous Counter Start for MTU0 to MTU 4, MTU6, and MTU7

Figure 19.99 shows an example of synchronous counter start setting procedure.



[1] Set TSTRA and TSTRB to stop the counters used for synchronous start operation.

[2] Specify the necessary operation with appropriate registers such as TCR, TMDR1, and TMDR2.

[3] In TCSYSTR, set the bits corresponding to the counters to be started synchronously to 1 at the same time. When TCSYSTR is set, TSTRA and TSTRB for the target timer counters are automatically set appropriately, the counters start synchronously, and TCSYSTR is automatically cleared.

[4] To stop a timer counter, set the bit in TSTRA or TSTRB that corresponds to the counter to 0.

Note: Even if a bit in TCSYSTR corresponding to an operating counter is cleared to 0, the counter will not stop.

Note: To start counters synchronously in reset-synchronized PWM mode or complementary PWM mode using MTU3 and MTU4 or MTU6 and MTU7, set the bits in TCSYSTR that correspond to MTU 3, MTU4, MTU6, and MTU7 to 1 at the same time.

Figure 19.99 Example of Synchronous Counter Start Setting Procedure

(b) Examples of Synchronous Counter Start Operation

Figure 19.100 shows an example of synchronous counter start operation for MTU0 to MTU4, MTU6, and MTU7.

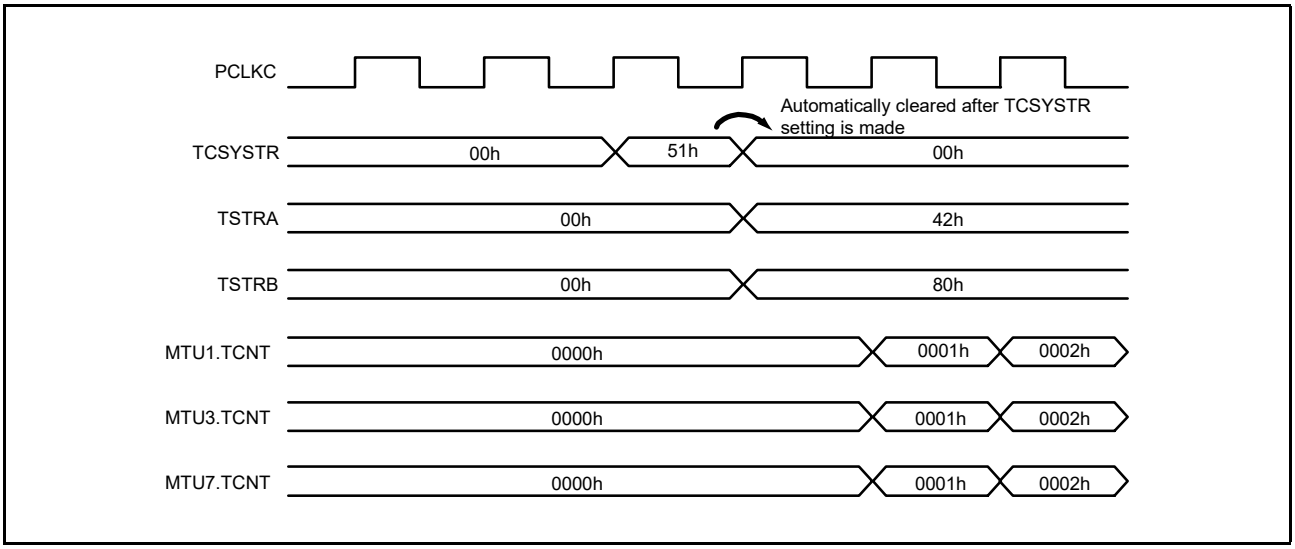


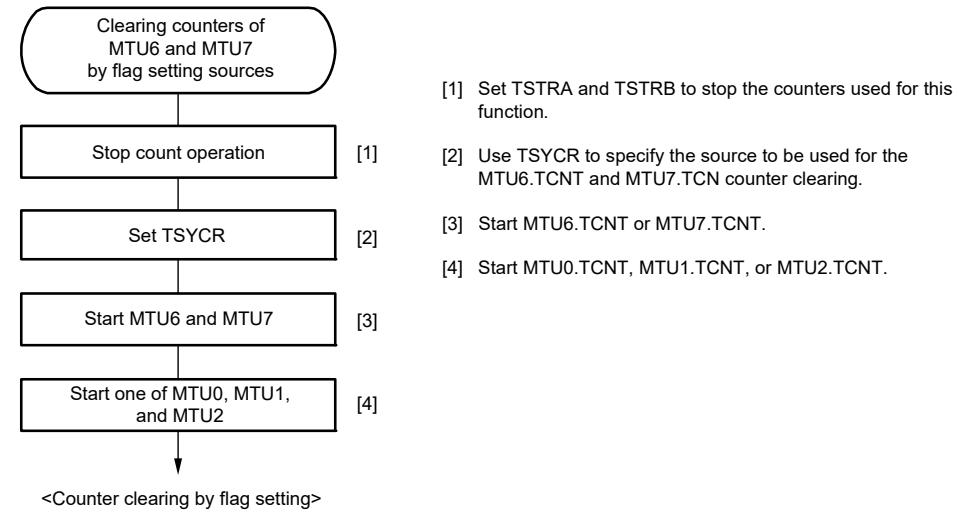
Figure 19.100 Example of Synchronous Counter Start Operation

(2) Synchronous Counter Clearing for MTU6 and MTU7

The counters in MTU6 and MTU7 can be cleared by the TGImn interrupt generation timing (m = A to D; n = 0 to 2) through the TSYCR setting.

(a) Example of Procedure for Specifying Synchronous Counter Clearing for MTU6 and MTU7

Figure 19.101 shows an example of procedure for specifying synchronous counter clearing for MTU6 and MTU7 by flag setting sources.



Note: The TSYCR setting is ignored while the counter is stopped. The setting becomes valid after MTU6.TCNT or MTU7.TCNT is started.

Figure 19.101 Example of Procedure for Specifying Synchronous Counter Clearing for MTU6 and MTU7

(b) Examples of Synchronous Counter Clearing for MTU6 and MTU7

Figure 19.102 and Figure 19.103 show examples of synchronous counter clearing for MTU6 and MTU7 by flag setting sources.

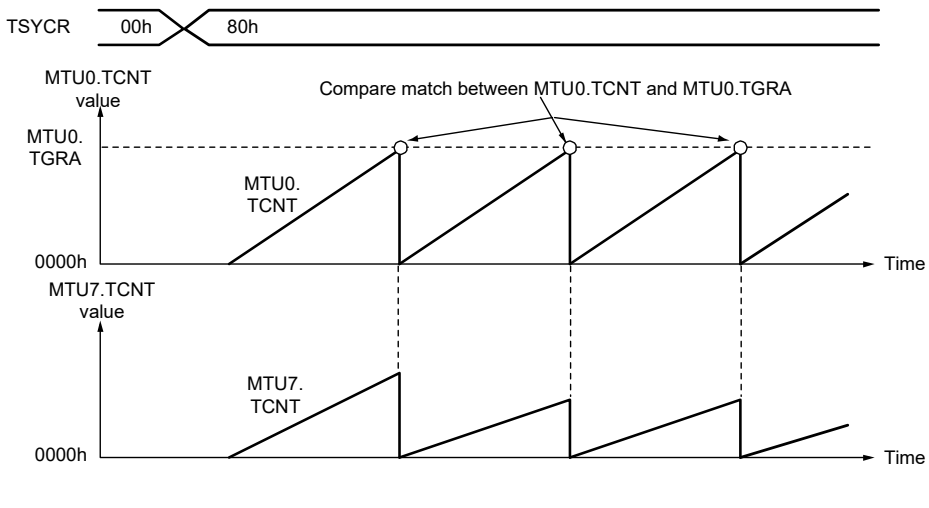


Figure 19.102 Example of Synchronous Counter Clearing for MTU6 and MTU7 (1)

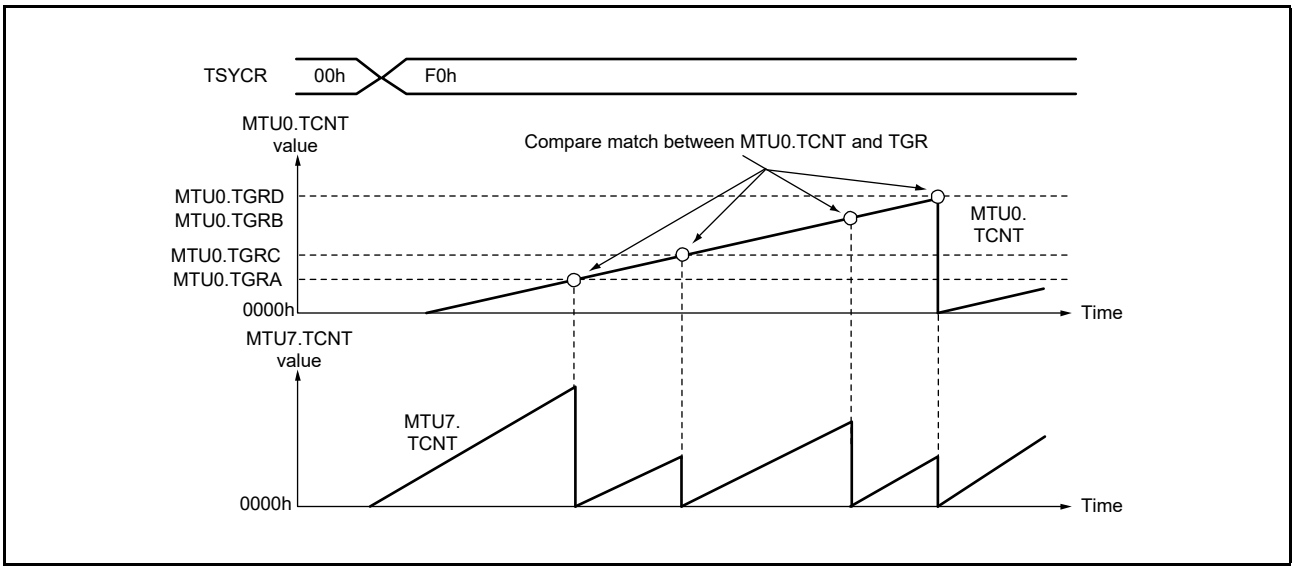
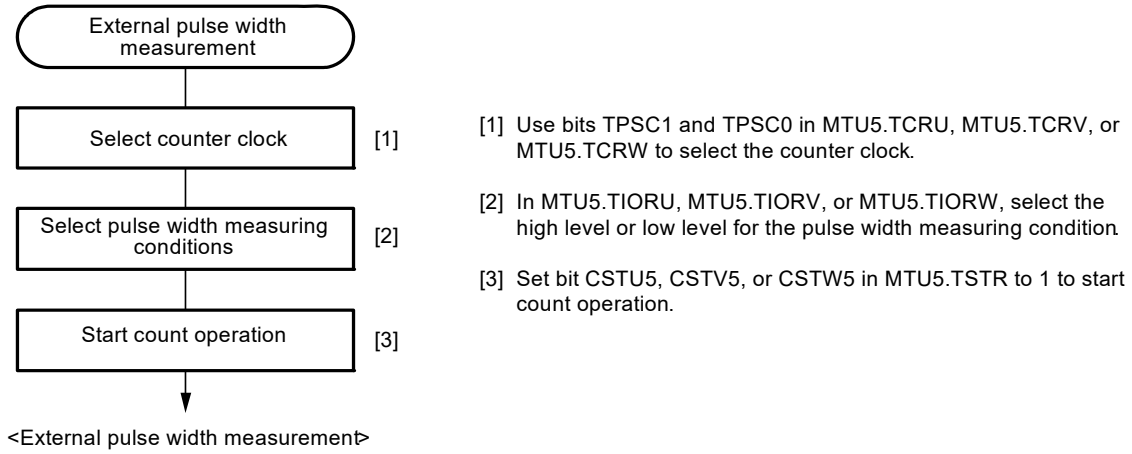


Figure 19.103 Example of Synchronous Counter Clearing for MTU6 and MTU7 (2)

19.3.11 External Pulse Width Measurement

The pulse widths of up to three external input lines can be measured in MTU5.

(1) Example of External Pulse Width Measurement Setting Procedure



Note: Do not set bit CMPCLR5U, CMPCLR5V, or CMPCLR5W in TCNTCMPCLR to 1.
Note: Do not set bit TGIE5U, TGIE5V, or TGIE5W in MTU5.TIER to 1.
Note: The value in TCNT is not captured in TGR.

Figure 19.104 Example of External Pulse Width Measurement Setting Procedure

(2) Example of External Pulse Width Measurement

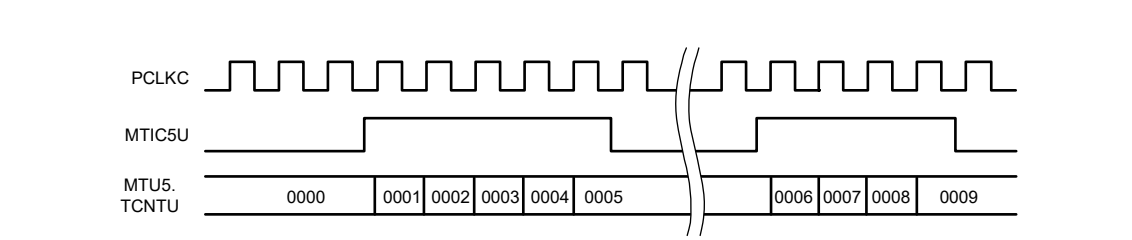


Figure 19.105 Example of External Pulse Width Measurement (Measuring High Pulse Width)

19.3.12 Dead Time Compensation

By measuring the delay of the output waveform and reflecting it to duty ratio, the external pulse width measurement function can be used as the dead time compensation function while the complementary PWM is in operation.

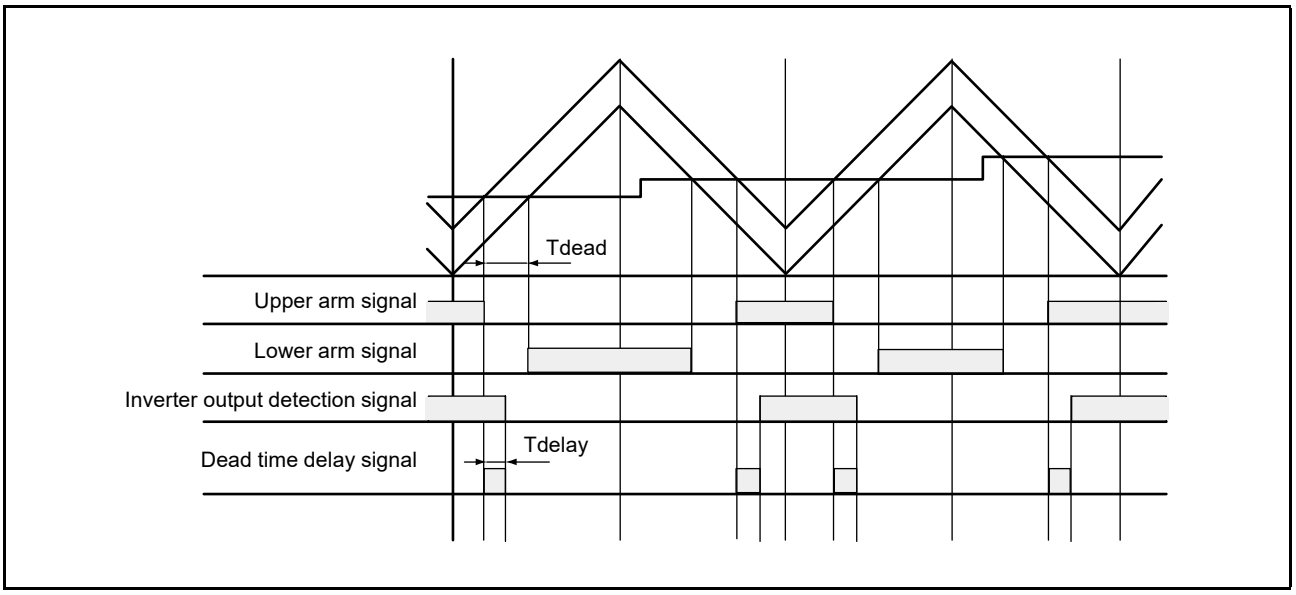
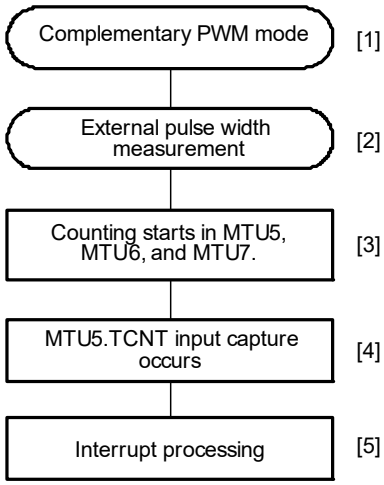


Figure 19.106 Delay in Dead Time in Complementary PWM Operation

(1) Example of Dead Time Compensation Setting Procedure

Figure 19.107 shows an example of dead time compensation setting procedure by using three counters in MTU5.



[1] Set MTU6 and MTU7 to complementary PWM mode.
For details, refer to section 19.3.8, Complementary PWM Mode.

[2] Specify the external pulse width measurement function for the target TIOR in MTU5. For details, refer to section 19.3.11, External Pulse Width Measurement.

[3] Set bits CST6 and CST7 in TSTRB and bits CSTU5, CSTV5, and CSTW5 in MTU5.TSTR to 1 to start count operation.

[4] When the capture condition specified in TIOR is satisfied, the MTU5.TCNT value is captured in MTU5.TGR. To prevent the generation of the MTU5.TGIm5 interrupt (m = U, V, W) request under the capture condition specified in TIOR, do not enable interrupt requests in MTU5.TIER.

[5] For U-phase dead time compensation, when an interrupt is generated at the crest (TGIA6) or trough (TCIV7) in complementary PWM mode, read the MTU5.TGRU value, calculate the difference in time between MTU6.TGRB and MTU5.TGRU, and write the corrected value to MTU6.TGRD in the interrupt processing. For the V phase and W phase, read the MTU5.TGRV and MTU5.TGRW values and write the corrected values to MTU7.TGRC and TGRD, respectively, in the same way as for U-phase compensation. The MTU5.TCNT value should be cleared through the TCNTCMPCLR setting or by software.

Note: The MPC and port mode registers (PMR) of the I/O ports should be set up in advance. Do not set MTU5.TIER to enable interrupt requests because the interrupt flag is set when the capture conditions set in TIOR are satisfied.

Figure 19.107 Example of Dead Time Compensation Setting Procedure

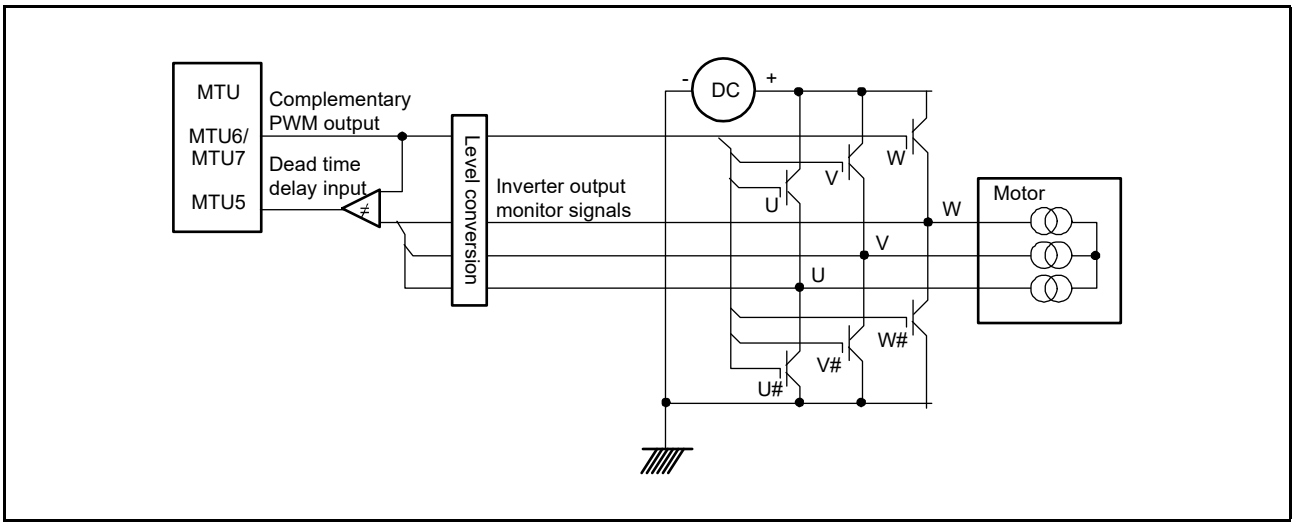


Figure 19.108 Example of Motor Control Circuit Configuration

19.3.13 TCNT Capture at Crest and/or Trough in Complementary PWM Operation

The TCNT value is captured in TGR at either the crest or trough or at both the crest and trough during complementary PWM operation. The timing for capturing in TGR can be selected by TIOR.

Figure 19.109 is an operating example in which TCNT is used as a free-running counter without being cleared, and the TCNT value is captured in TGR at the specified timing (either crest or trough, or both crest and trough).

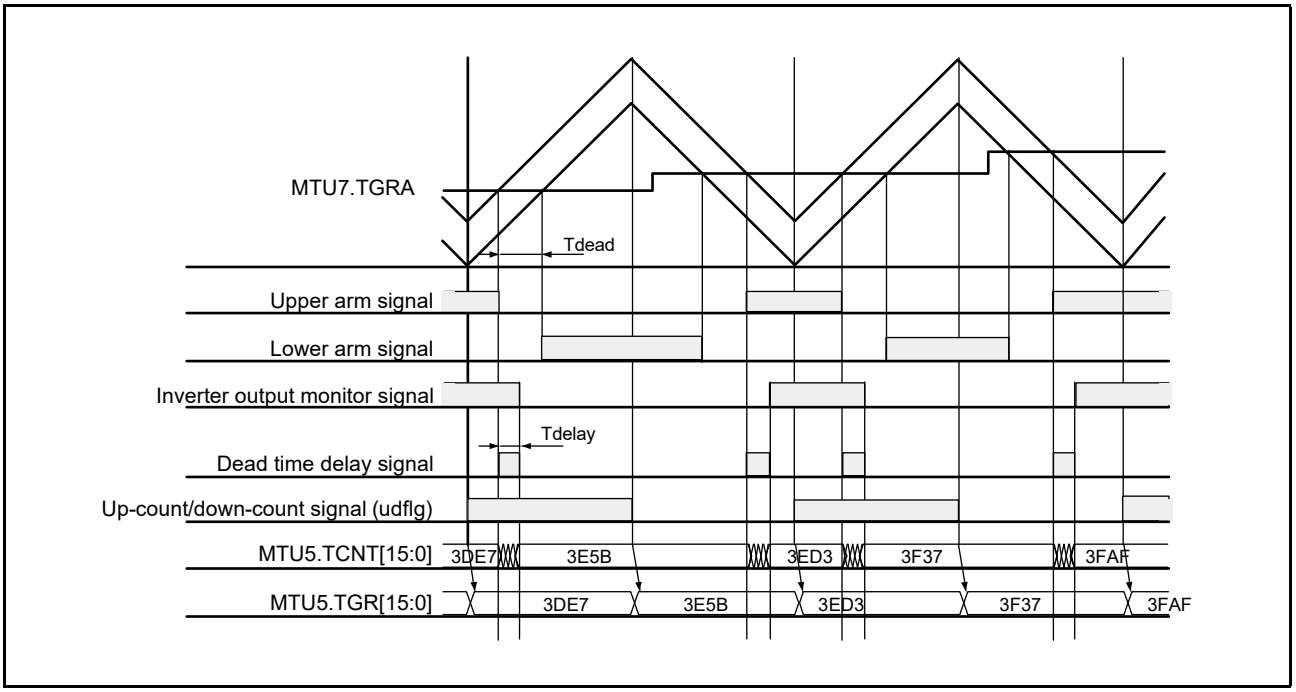


Figure 19.109 TCNT Capture at Crest and/or Trough in Complementary PWM Operation

19.3.14 Noise Filtering Function

The input capture input pins and external clock input pins have a noise filtering function. Use the NFCRn register (n = 0 to 8, or C) to enable or disable noise filtering and to set the sampling clock. Noise filtering can be enabled or disabled for each pin, and the sampling clock can be set for each channel. Figure 19.110 shows the timing of noise filtering.

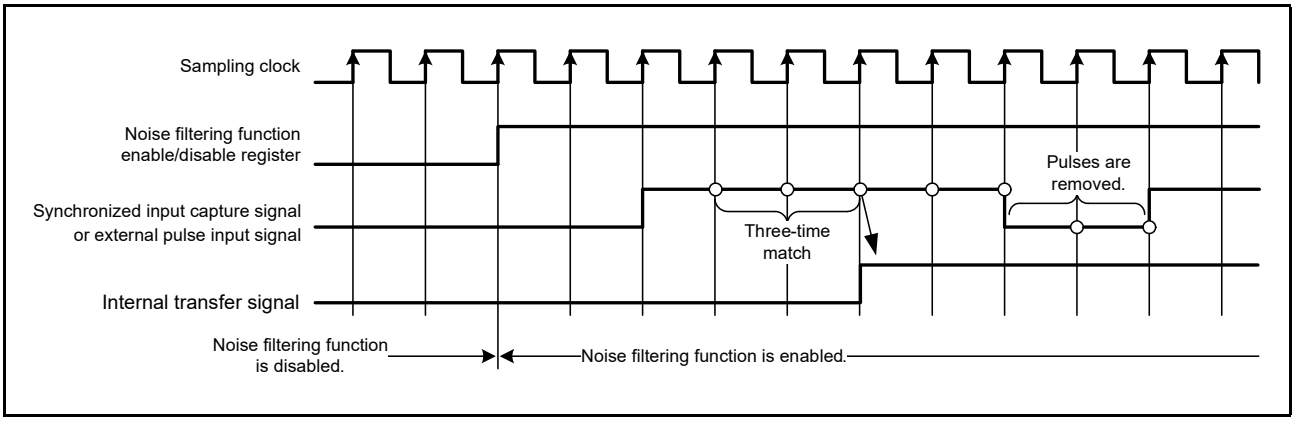


Figure 19.110 Timing of Noise Filtering

19.4 Interrupt Sources

19.4.1 Interrupt Sources and Priorities

There are three kinds of MTU interrupt source; TGR input capture/compare match, TCNT overflow, and TCNT underflow. Each interrupt source has its own enable/disable bit, allowing the generation of interrupt request signals to be enabled or disabled individually.

When an interrupt source is generated, if the corresponding enable/disable bit in TIER is set to 1, an interrupt is requested.

Relative interrupt priorities can be changed by the interrupt controller. For details, see section 12, Interrupt Controller (ICUA). Table 19.77 lists the MTU interrupt sources.

Table 19.77 MTU Interrupt Sources

Channel	Name	Interrupt Source	DMAC Activation	Priority
MTU0	TGIA0	ch0 input capture/compare match A interrupt	Possible	High
	TGIB0	ch0 input capture/compare match B interrupt	Possible	
	TGIC0	ch0 input capture/compare match C interrupt	Possible	
	TGID0	ch0 input capture/compare match D interrupt	Possible	
	TCIV0	ch0 overflow interrupt	Not possible	
	TGIE0	ch0 compare match E interrupt	Not possible	
	TGIF0	ch0 compare match F interrupt	Not possible	
MTU1	TGIA1	ch1 input capture/compare match A interrupt	Possible	
	TGIB1	ch1 input capture/compare match B interrupt	Possible	
	TCIV1	ch1 overflow interrupt	Not possible	
	TCIU1	ch1 underflow interrupt	Not possible	
MTU2	TGIA2	ch2 input capture/compare match A interrupt	Possible	
	TGIB2	ch2 input capture/compare match B interrupt	Possible	
	TCIV2	ch2 overflow interrupt	Not possible	
	TCIU2	ch2 underflow interrupt	Not possible	
MTU3	TGIA3	ch3 input capture/compare match A interrupt	Possible	
	TGIB3	ch3 input capture/compare match B interrupt	Possible	
	TGIC3	ch3 input capture/compare match C interrupt	Possible	
	TGID3	ch3 input capture/compare match D interrupt	Possible	
	TCIV3	ch3 overflow interrupt	Not possible	
MTU4	TGIA4	ch4 input capture/compare match A interrupt	Possible	
	TGIB4	ch4 input capture/compare match B interrupt	Possible	
	TGIC4	ch4 input capture/compare match C interrupt	Possible	
	TGID4	ch4 input capture/compare match D interrupt	Possible	
	TCIV4	ch4 overflow/underflow interrupt*1	Possible	
MTU5	TGIU5	ch5 input capture/compare match U interrupt	Possible	
	TGIV5	ch5 input capture/compare match V interrupt	Possible	
	TGIW5	ch5 input capture/compare match W interrupt	Possible	
MTU6	TGIA6	ch6 input capture/compare match A interrupt	Possible	
	TGIB6	ch6 input capture/compare match B interrupt	Possible	
	TGIC6	ch6 input capture/compare match C interrupt	Possible	
	TGID6	ch6 input capture/compare match D interrupt	Possible*2	
	TCIV6	ch6 overflow interrupt	Not possible	
MTU7	TGIA7	ch7 input capture/compare match A interrupt	Possible	
	TGIB7	ch7 input capture/compare match B interrupt	Possible	
	TGIC7	ch7 input capture/compare match C interrupt	Possible	
	TGID7	ch7 input capture/compare match D interrupt	Possible	
	TCIV7	ch7 overflow/underflow interrupt*1	Possible	
MTU8	TGIA8	ch8 input capture/compare match A interrupt	Possible	
	TGIB8	ch8 input capture/compare match B interrupt	Possible	
	TGIC8	ch8 input capture/compare match C interrupt	Possible	
	TGID8	ch8 input capture/compare match D interrupt	Possible	
	TCIV8	ch8 overflow interrupt	Not Possible	Low

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

Note 1. Only in complementary PWM mode
Note 2. Interrupts are generated in response to requests for DMA transfer, but there are no interrupts on completion of transfer. Poll the END bit of the CHSTAT_n register to confirm the completion of DMA transfer.

(1) Input Capture/Compare Match Interrupt

If the TIER.TGIE bit is set to 1 when a TGR input capture/compare match occurs on a channel, an interrupt is requested. The MTU has 33 input capture/compare match interrupts (six for MTU0, four each for MTU3, MTU4, MTU6, MTU7, and MTU8, two each for MTU1 and MTU2, and three for MTU5). The MTU0.TGFE and MTU0.TGFF flags in MTU0 are not set to 1 by the occurrence of an input capture.

(2) Overflow Interrupt

If the TIER.TCIEV bit is set to 1 when a TCNT overflow occurs on a channel, an interrupt is requested. The MTU has eight overflow interrupts one for each channel.

(3) Underflow Interrupt

If the TIER.TCIEU bit is set to 1 when a TCNT underflow occurs on a channel, an interrupt is requested. The MTU has two underflow interrupts (one each for MTU1 and MTU2).

19.4.2 DMAC Activation

(1) DMAC Activation

The DMAC can be activated by the TGRA input capture/compare match interrupt and the overflow interrupt in MTU4 and MTU7. For details, see section 15, DMA Controller (DMACAa).
The MTU provides a total of 33 input capture/compare match interrupts that can be used as DMAC activation sources: four each for MTU0, MTU3, MTU6, and MTU8, two each for MTU1 and MTU2, five each for MTU4 and MTU7, and three for MTU5.

19.4.3 A/D Converter Activation

The A/D converter can be activated by one of the following three methods in the MTU. Table 19.78 shows the relationship between interrupt sources and A/D converter start request signals.

(1) A/D Converter Activation by MTUn.TGRA (n = 0 to 4, 6, 7) Input Capture/Compare Match or at MTUm.TCNT (m = 4 or 7) Trough in Complementary PWM Mode

The A/D converter can be activated by the occurrence of a TGRA input capture/compare match in channels 0 to 4, 6, and 7. In addition, if complementary PWM operation is performed while the TTGE2 bit in MTUm.TIER is set to 1, the A/D converter can be activated at the trough of MTUm.TCNT count (MTUm.TCNT = 0000h) (m = 4 or 7).
A/D converter start request signal TRGAnN is issued to the A/D converter under either of the following conditions (n = 0 to 4, 6, or 7).

- When a TGRA input capture/compare match occurs on a channel while the TIER.TTG bit is set to 1
- When the MTUm.TCNT count reaches the trough (MTUm.TCNT = 0000h) during complementary PWM operation while the TTGE2 bit in MTUm.TIER is set to 1

When either condition is satisfied, if A/D converter start signal TRGAnN from the MTU is selected as the trigger in the A/D converter, A/D conversion will start.

(2) A/D Converter Activation by Compare Match between MTU0.TCNT and MTU0.TGRE

A/D converter start request signal TRG0N is issued to the A/D converter when a compare match occurs between MTU0.TCNT and MTU0.TGRE in MTU0.
When a compare match occurs between MTU0.TCNT and MTU0.TGRE in MTU0 while the TTGE2 bit in MTU0.TIER2 is set to 1, A/D converter start request TGR0N is issued to the A/D converter. If A/D converter start signal TRG0N from the MTU is selected as the trigger in the A/D converter, A/D conversion will start.

(3) A/D Converter Activation by A/D Converter Start Request Delaying Function (MTU4 and MTU7)

The A/D converter can be activated by generating TRGmAN or TRGmBN when the MTUm.TCNT count matches the MTUm.TADCORA or MTUm.TADCORB value if the UTmAE, DTmAE, UTmBE, or DTmBE bit in the A/D converter start request control register (MTUm.TADCR) is set to 1 (m = 4 or 7). The A/D converter can also be activated by outputting TRGmABN when TRGmAN or TRGmBN is generated, or by outputting TRG4ABN (TRG7ABN) when TRG4AN (TRG7AN) or TRG4BN (TRG7BN) is generated. For details, see section 19.3.9, A/D Converter Start Request Delaying Function.
A/D conversion will start when TRGmAN is generated if A/D converter start signal TRGmAN from the MTU is selected as the trigger in the A/D converter, when TRGmBN is generated if TRGmBN from the MTU is selected as the trigger in the A/D converter, or when TRGmABN is generated if TRGmABN from the MTU is selected as the trigger in the A/D converter (m = 4 or 7).

Table 19.78 Interrupt Sources and A/D Converter Start Request Signals

Target Registers	Interrupt Source	A/D Converter Start Request Signal
MTU0.TGRA and MTU0.TCNT	Input capture/compare match	TRGA0N
MTU1.TGRA and MTU1.TCNT		TRGA1N
MTU2.TGRA and MTU2.TCNT		TRGA2N
MTU3.TGRA and MTU3.TCNT		TRGA3N
MTU4.TGRA and MTU4.TCNT*1		TRGA4N
MTU4.TCNT	MTU4.TCNT trough in complementary PWM mode	
MTU6.TGRA and MTU6.TCNT	Input capture/compare match	TRGA6N
MTU7.TGRA and MTU7.TCNT*1		TRGA7N
MTU7.TCNT	MTU7.TCNT trough in complementary PWM mode	
MTU0.TGRE and MTU0.TCNT	Compare match	TRG0N
MTU4.TADCORA and MTU4.TCNT	Compare match	TRG4AN
MTU4.TADCORB and MTU4.TCNT		TRG4BN
MTU7.TADCORA and MTU7.TCNT		TRG7AN
MTU7.TADCORB and MTU7.TCNT		TRG7BN
MTU4.TADCORA and MTU4.TCNT, MTU4.TADCORB and MTU4.TCNT	Compare match (interrupt skipping function 2)	TRG4ABN
MTU7.TADCORA and MTU7.TCNT, MTU7.TADCORB and MTU7.TCNT		TRG7ABN

Note 1. Since PWM waveforms are generated in complementary PWM mode, MTU4.TGRA (MTU7.TGRA) compare match not only with MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) is detected. Accordingly, when compare match with MTU3.TCNT (MTU6.TCNT) and TCNTSA (TCNTSB) occurs, TRGA4N (TRGA7N) is also generated. When MTU3 and MTU 4 (MTU 6 and MTU7) are made to operate in complementary PWM mode for generating an A/D converter start request, use the A/D converter start request by compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA/B (MTU7.TADCORA/B).

19.5 Operation Timing

19.5.1 Input/Output Timing

(1) TCNT Count Timing

Figure 19.111 and Figure 19.112 show the TCNT count timing in internal clock operation, Figure 19.113 shows the TCNT count timing in external clock operation (normal mode), and Figure 19.114 shows the TCNT count timing in external clock operation (phase counting mode).

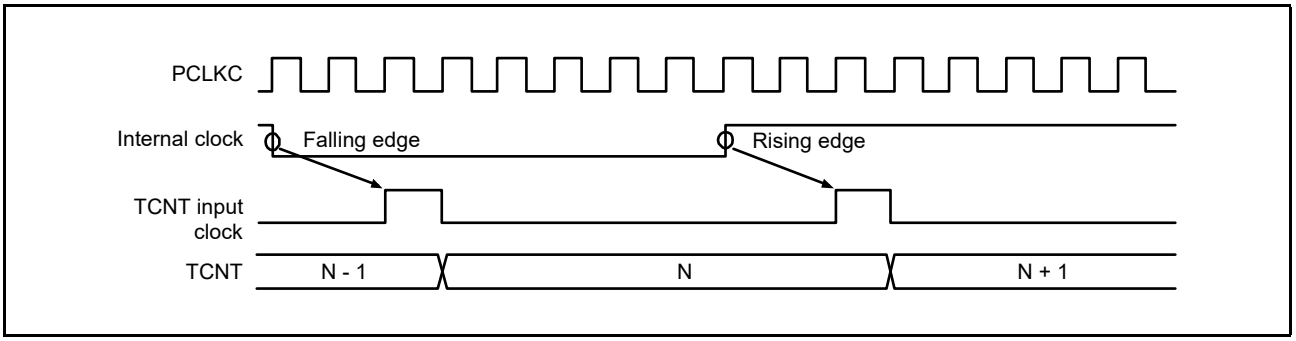


Figure 19.111 Count Timing in Internal Clock Operation (MTU0 to MTU4 and MTU6 to MTU8)

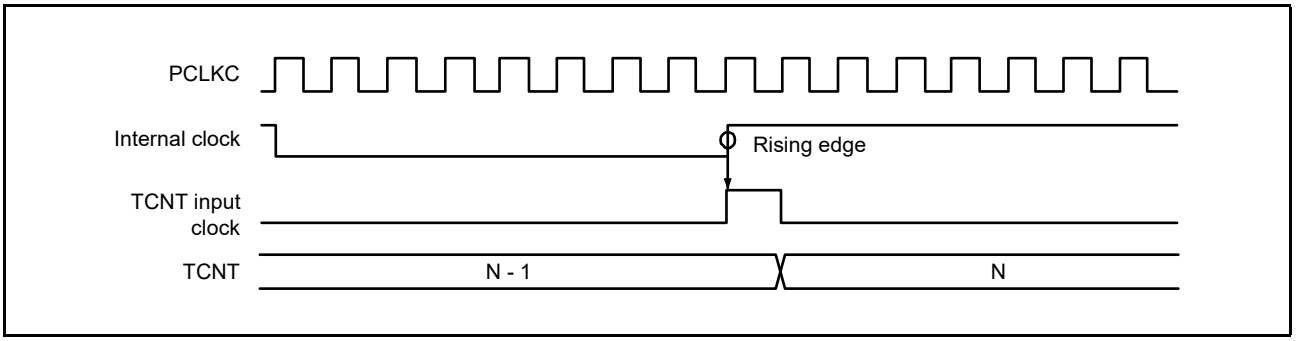


Figure 19.112 Count Timing in Internal Clock Operation (MTU5)

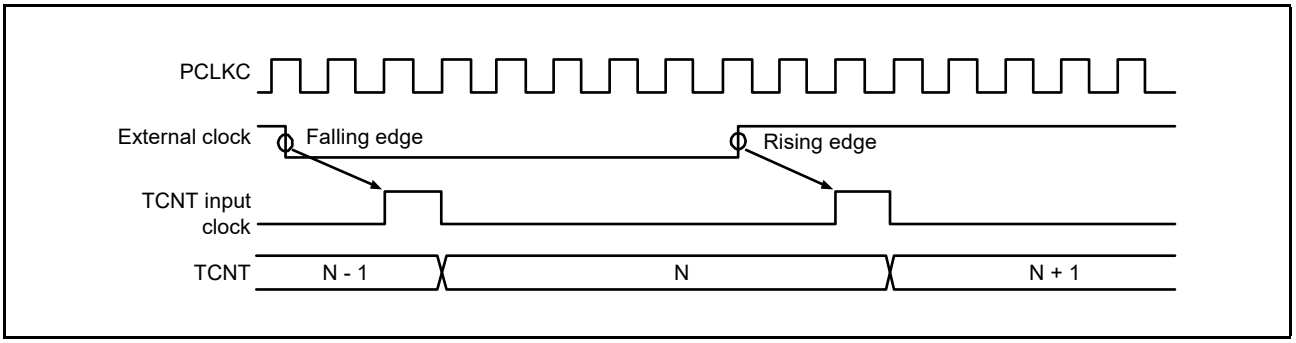


Figure 19.113 Count Timing in External Clock Operation (MTU0 to MTU4 and MTU8)

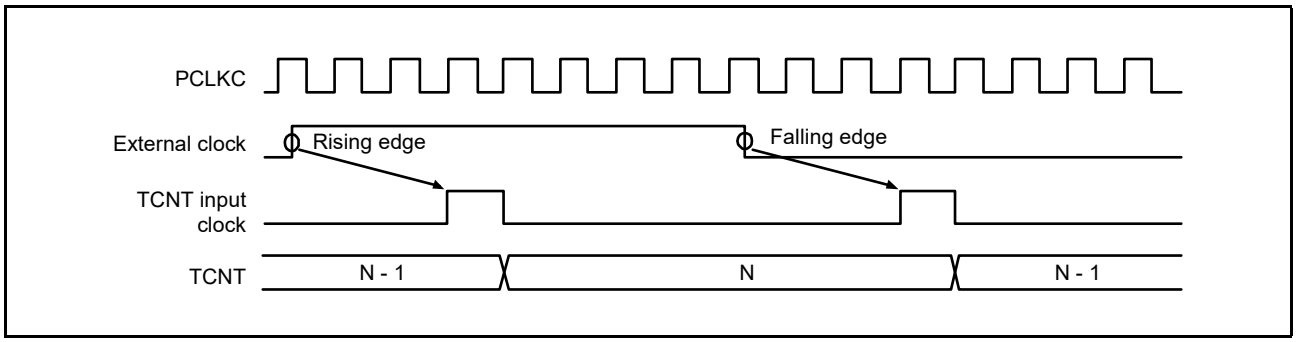


Figure 19.114 Count Timing in External Clock Operation (Phase Counting Mode)

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TCNT and TGR match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the value set in TIOR is output from the MTIOCnm pin (n = 0 to 4, 6, 7, or 8; m = A to D). After a match between TCNT and TGR, the compare match signal is not generated until the TCNT input clock is generated.

Figure 19.115 shows the output compare output timing (normal mode or PWM mode) and Figure 19.116 shows the output compare output timing (complementary PWM mode or reset-synchronized PWM mode).

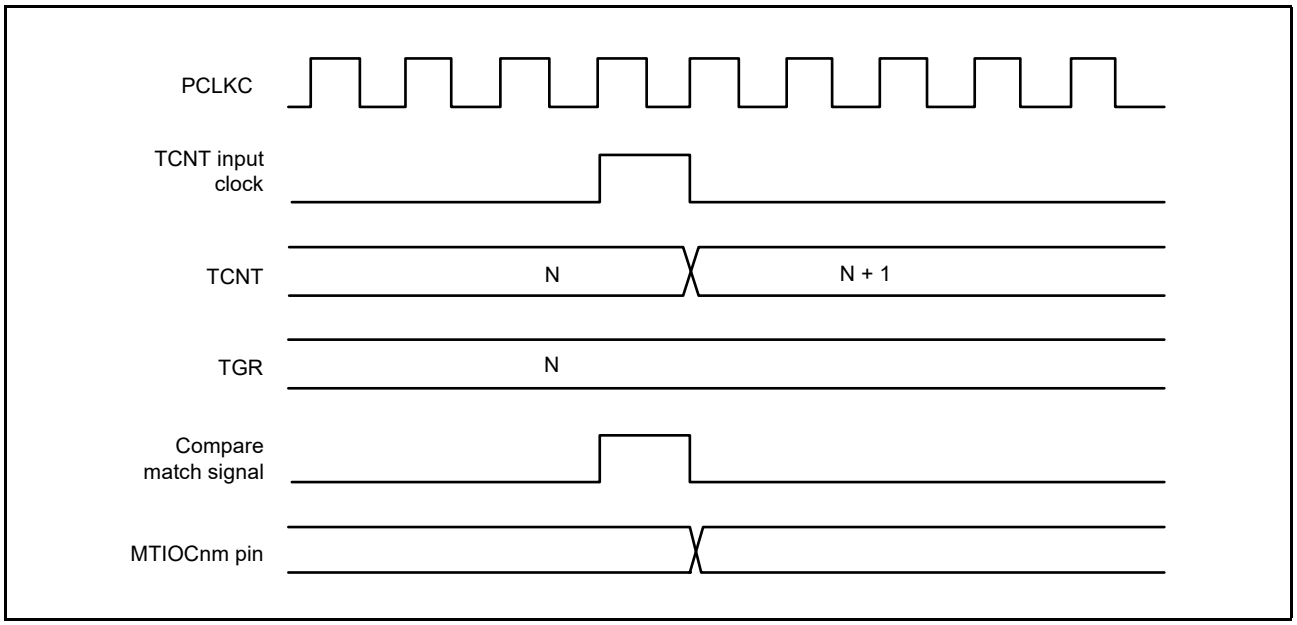


Figure 19.115 Output Compare Output Timing (Normal Mode or PWM Mode) (n = 0 to 4, 6, 7, or 8, m = A to D)

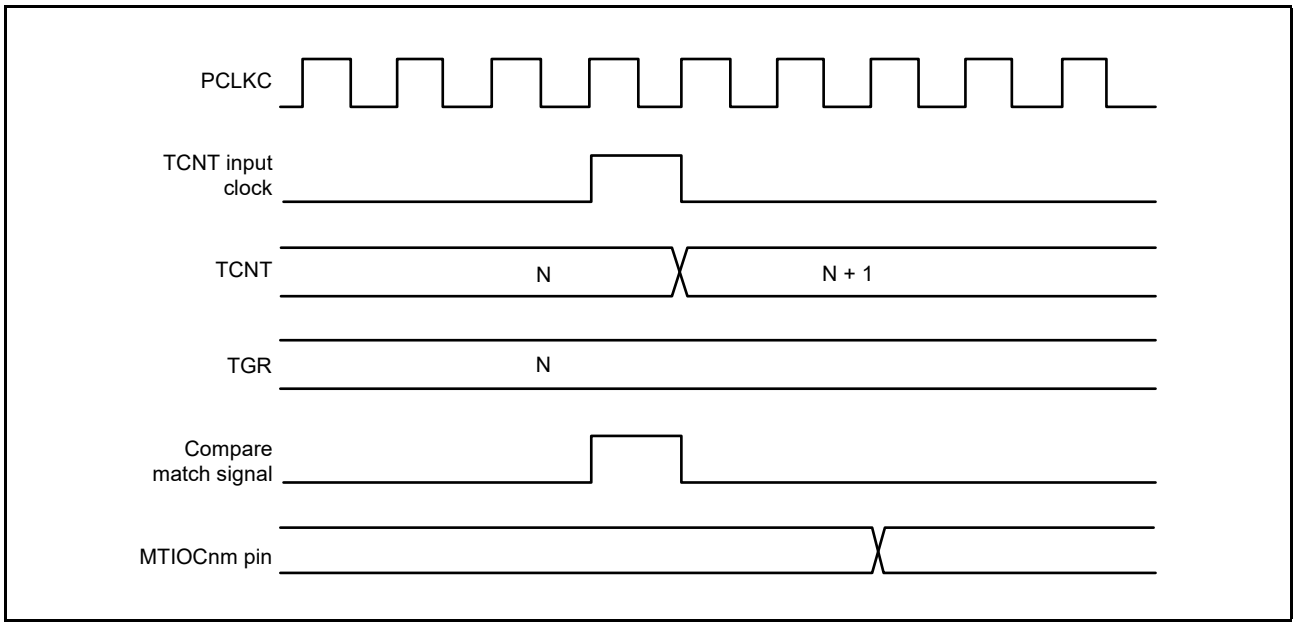


Figure 19.116 Output Compare Output Timing (Complementary PWM Mode or Reset-Synchronized PWM Mode) (n = 0 to 4, 6, 7, or 8, m = A to D)

(3) Input Capture Signal Timing

Figure 19.117 shows the input capture signal timing.

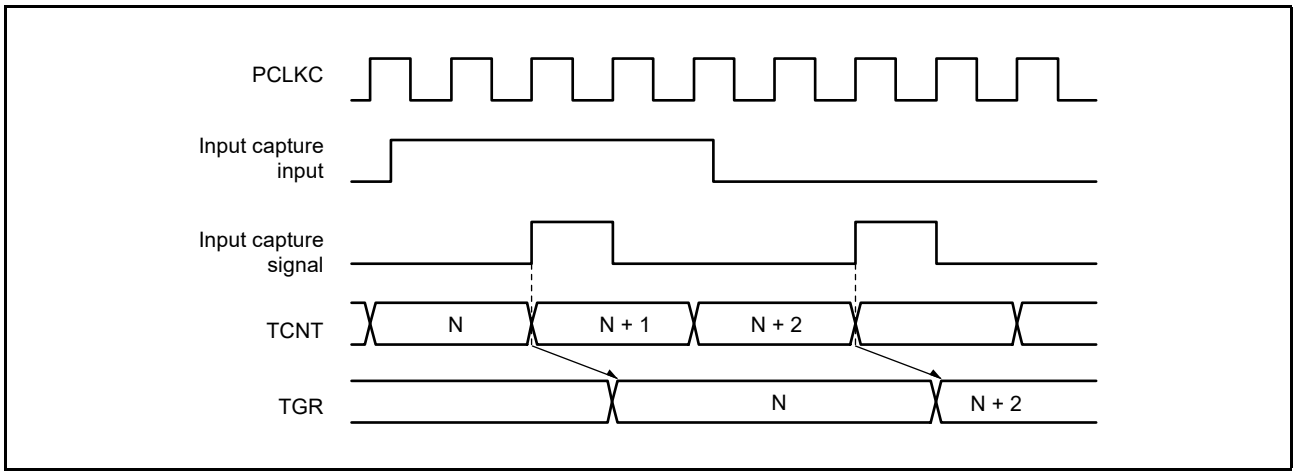


Figure 19.117 Input Capture Input Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

Figure 19.118 and Figure 19.119 show the timing when counter clearing on compare match is specified, and Figure 19.120 shows the timing when counter clearing on input capture is specified.

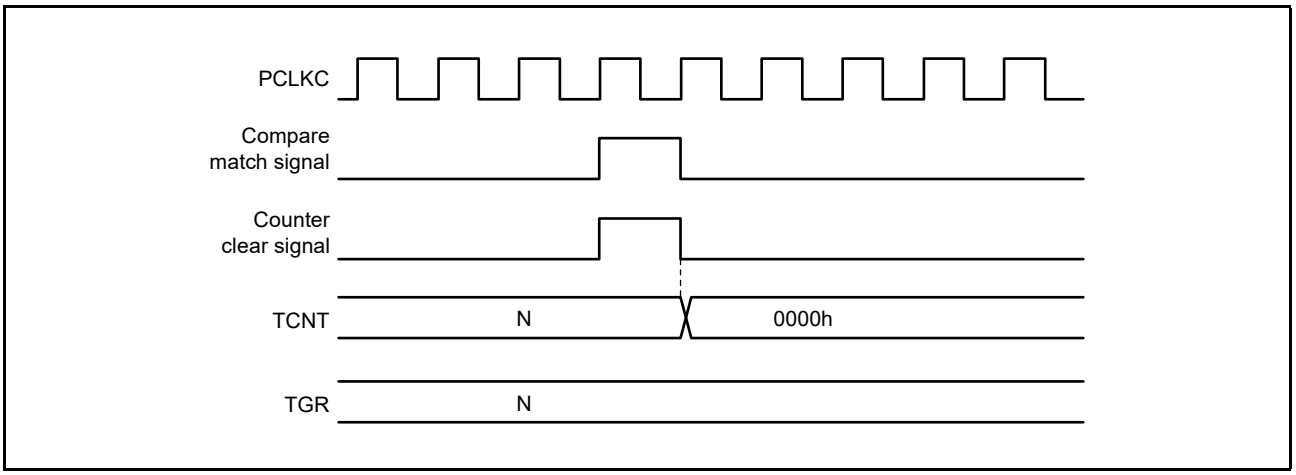


Figure 19.118 Counter Clear Timing (Compare Match) (MTU0 to MTU4 and MTU6 to MTU8)

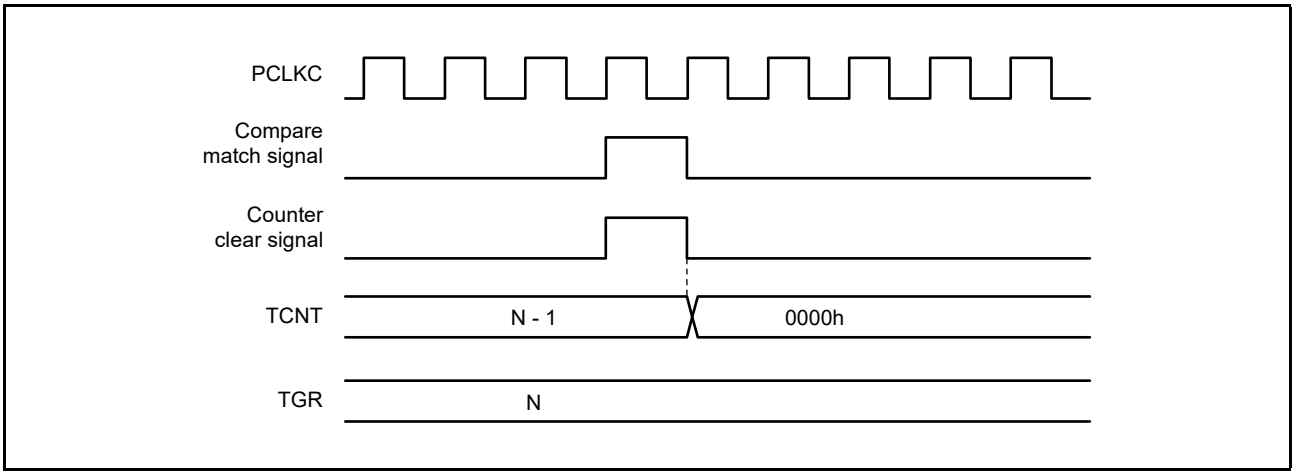


Figure 19.119 Counter Clear Timing (Compare Match) (MTU5)

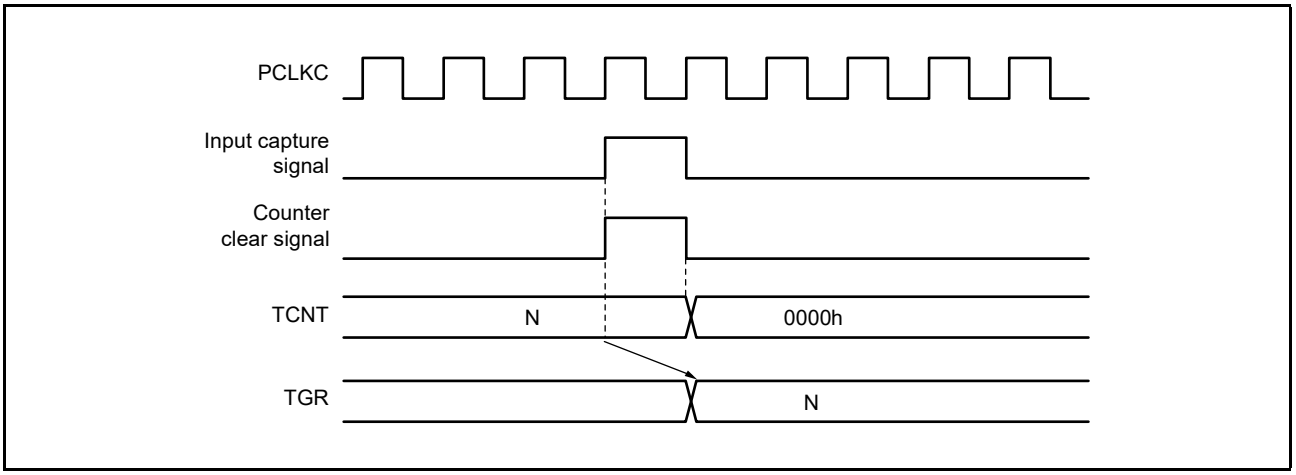


Figure 19.120 Counter Clear Timing (Input Capture) (MTU0 to MTU8)

(5) Buffer Operation Timing

Figure 19.121 to Figure 19.123 show the timing in buffer operation.

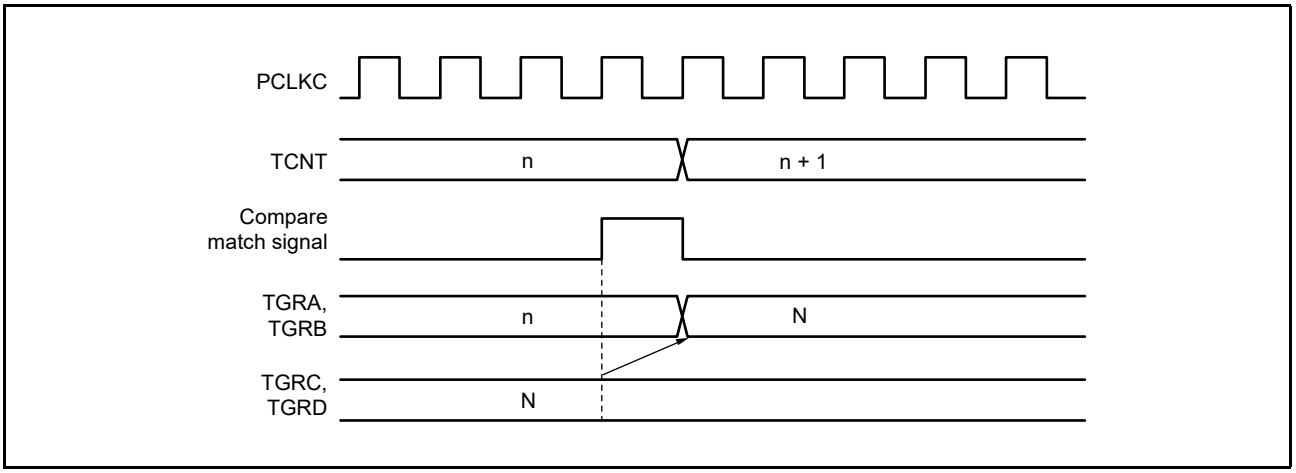


Figure 19.121 Buffer Operation Timing (Compare Match)

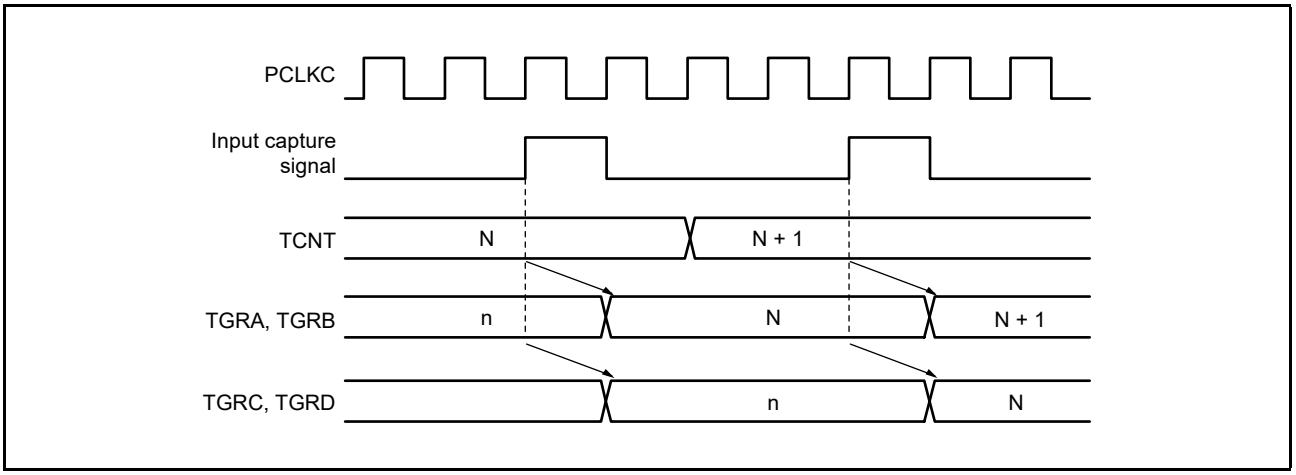


Figure 19.122 Buffer Operation Timing (Input Capture)

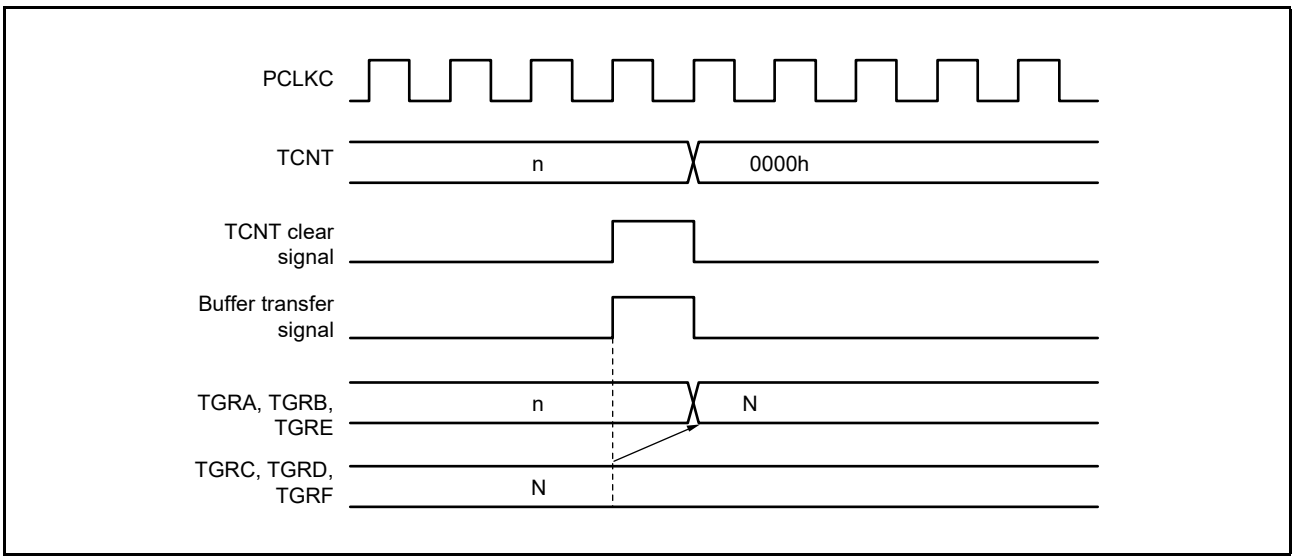


Figure 19.123 Buffer Operation Timing (when TCNT Cleared)

(6) Buffer Transfer Timing (Complementary PWM Mode)

Figure 19.124 to Figure 19.126 show the buffer transfer timing in complementary PWM mode.

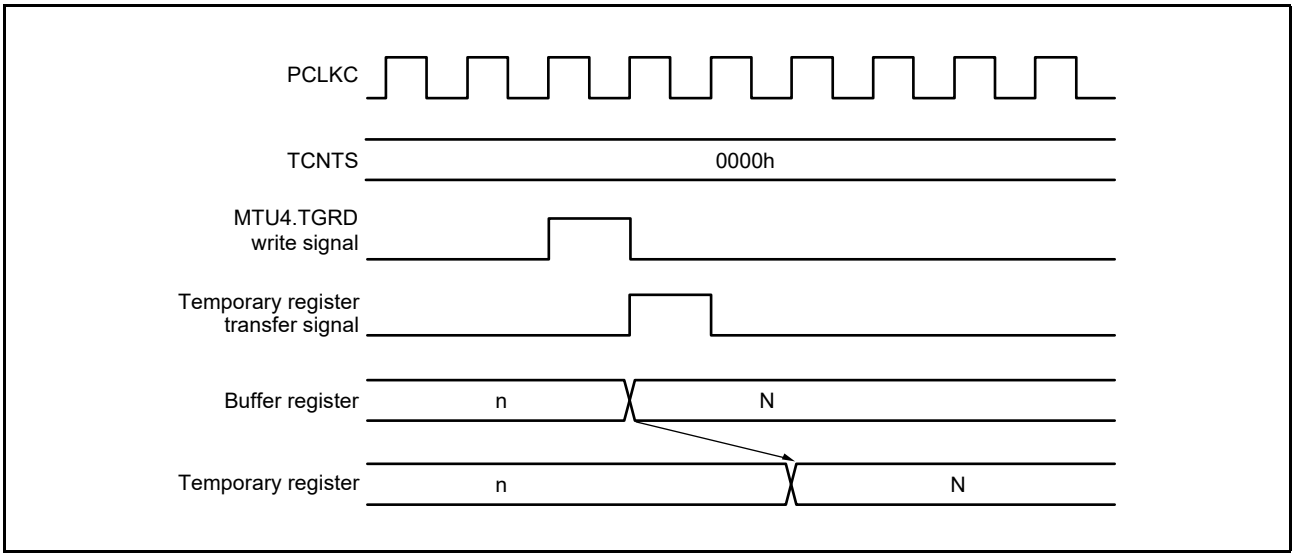


Figure 19.124 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Stopped)

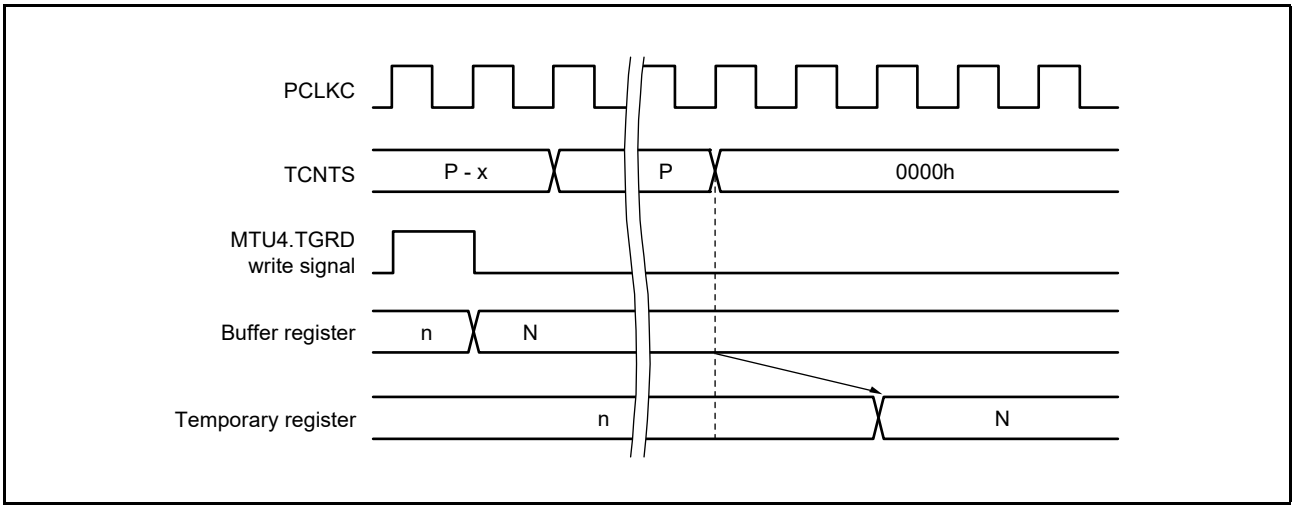


Figure 19.125 Transfer Timing from Buffer Register to Temporary Register (TCNTSA Operating)

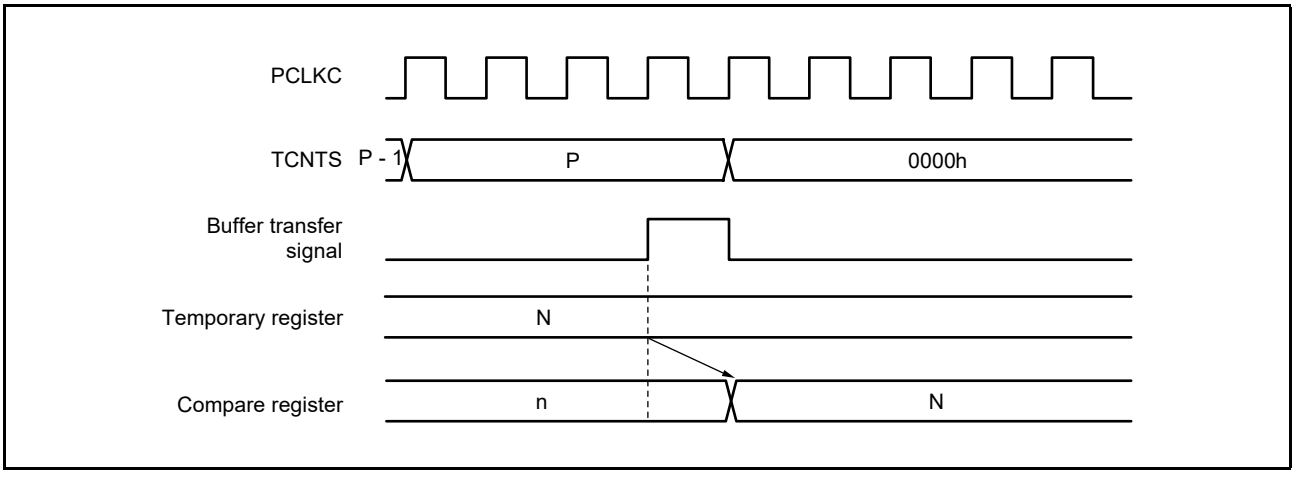


Figure 19.126 Transfer Timing from Temporary Register to Compare Register

19.5.2 Interrupt Signal Timing

(1) TGI Interrupt Timing by Compare Match

Figure 19.127 and Figure 19.128 show the TGI interrupt request signal timing when a compare match occurs.

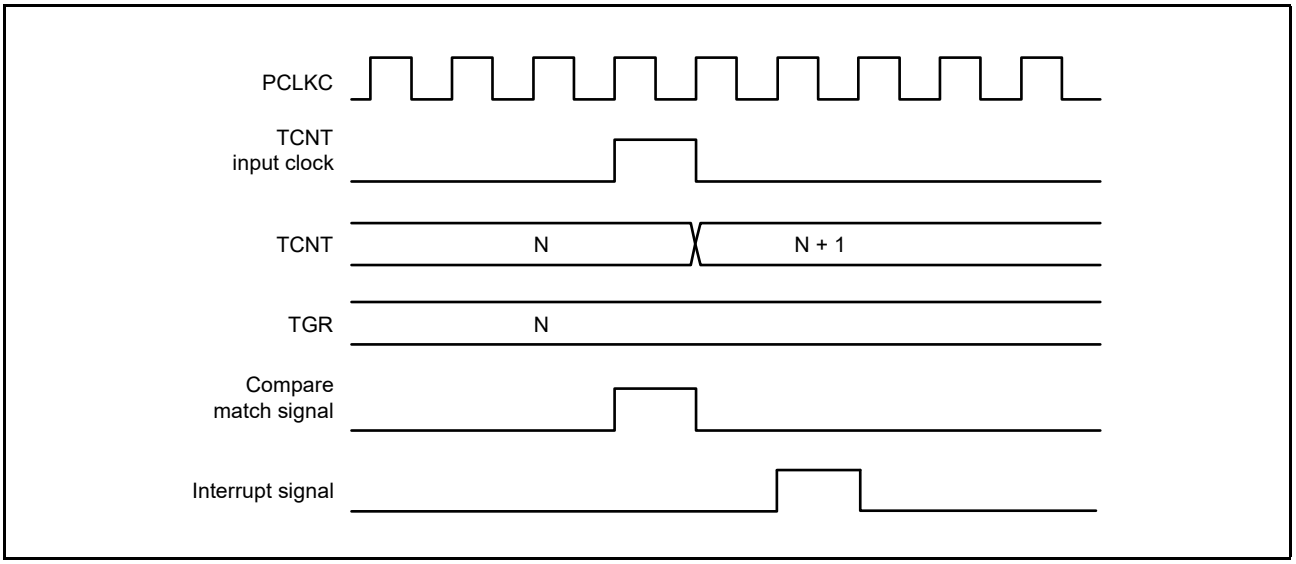


Figure 19.127 TGI Interrupt Timing (Compare Match) (MTU0 to MTU4 and MTU6 to MTU8)

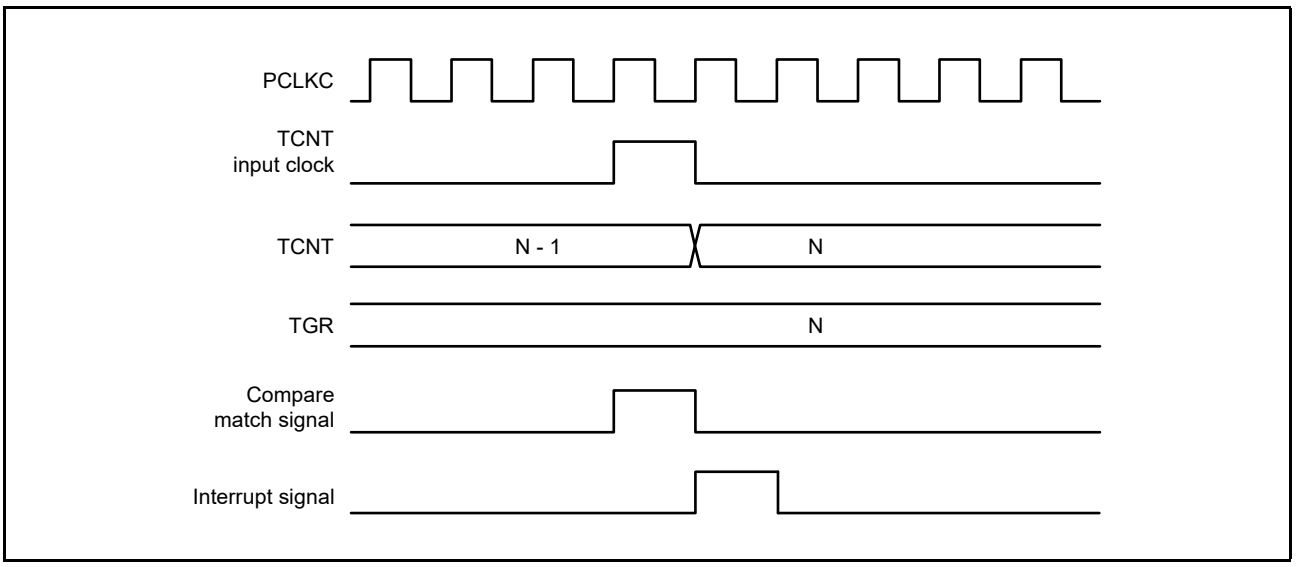


Figure 19.128 TGI Interrupt Timing (Compare Match) (MTU5)

(2) TGI Interrupt Timing by Input Capture

Figure 19.129 and Figure 19.130 show the TGI interrupt request signal timing when an input capture occurs.

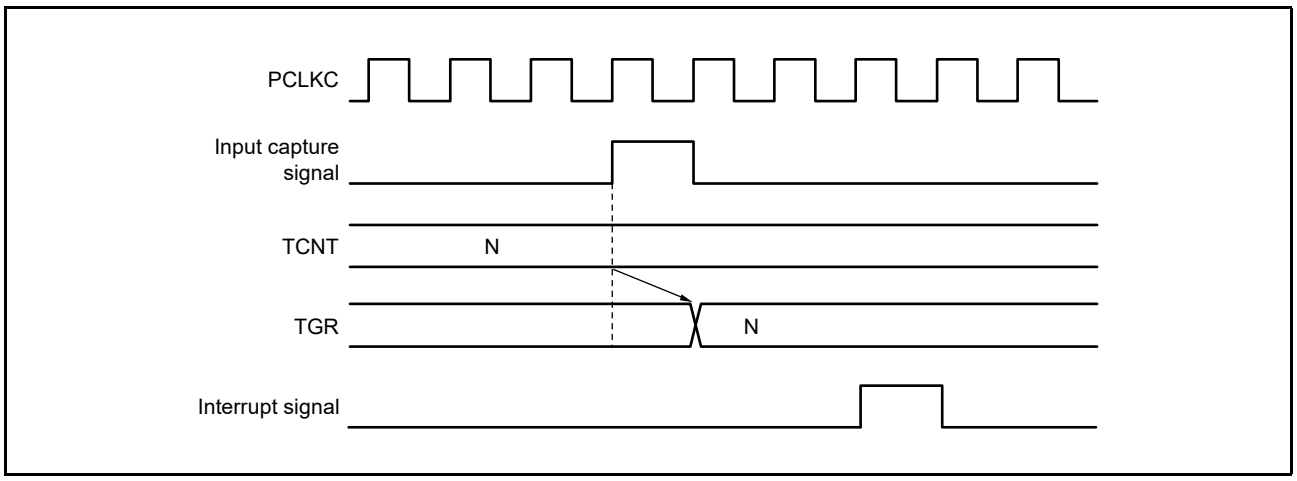


Figure 19.129 TGI Interrupt Timing (Input Capture) (MTU0 to MTU4 and MTU6 to MTU8)

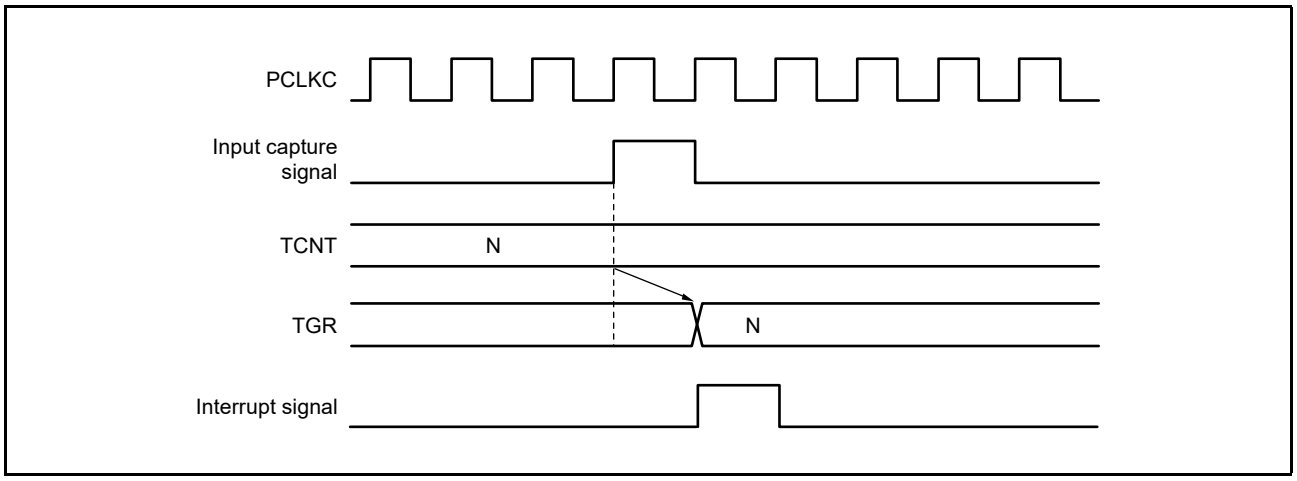


Figure 19.130 TGI Interrupt Timing (Input Capture) (MTU5)

(3) TCFV and TCFU Interrupt Request Timing on Overflow/Underflow

Figure 19.131 shows the TCIV interrupt request signal timing when an overflow is generated.
Figure 19.132 shows the TCIU interrupt request signal timing when an underflow is generated.

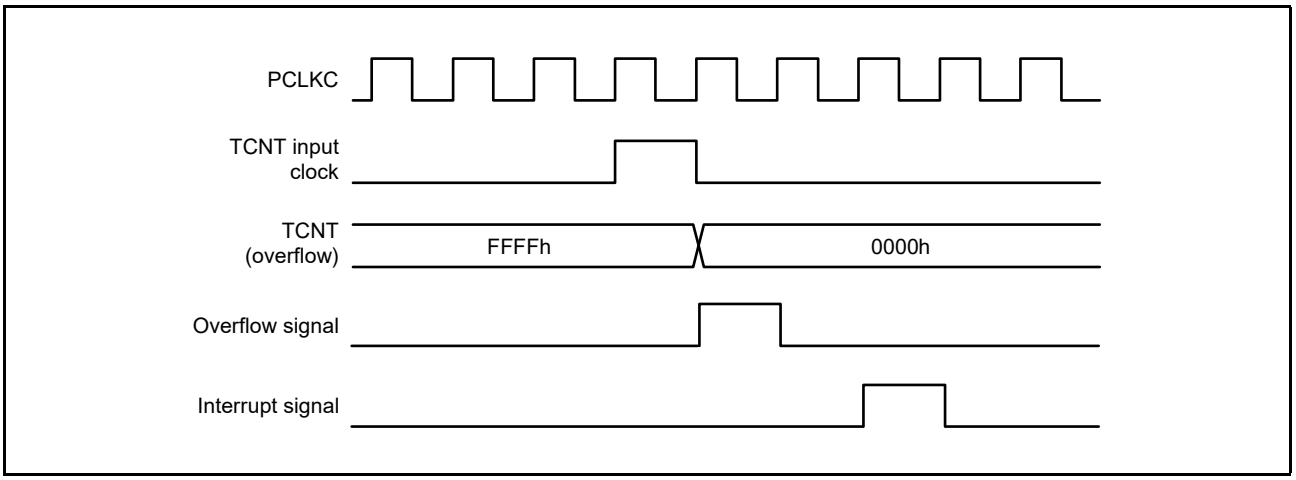


Figure 19.131 TCIV Interrupt Timing

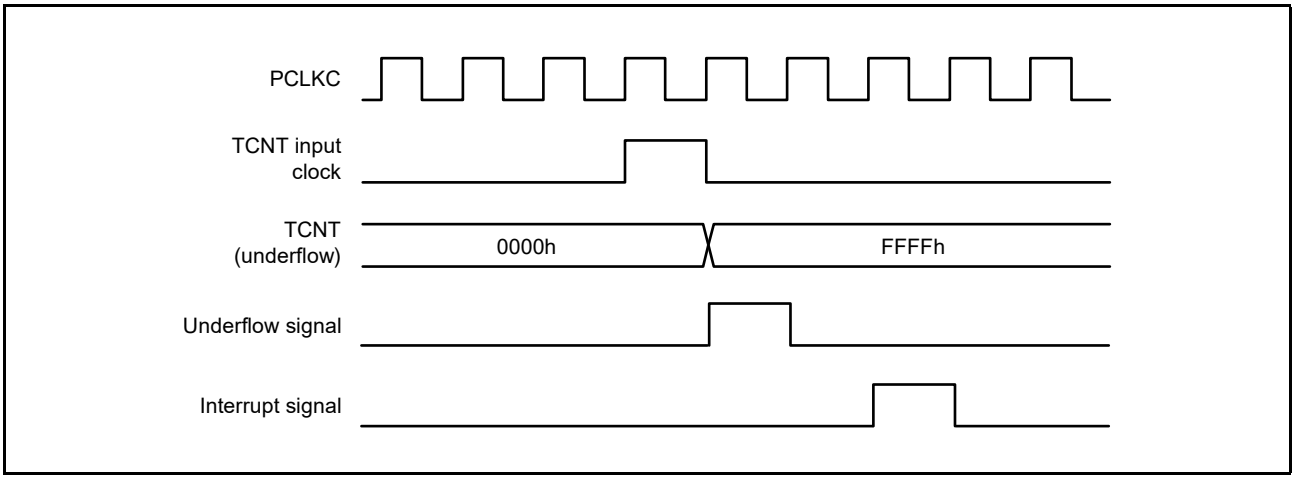


Figure 19.132 TCIU Interrupt Timing

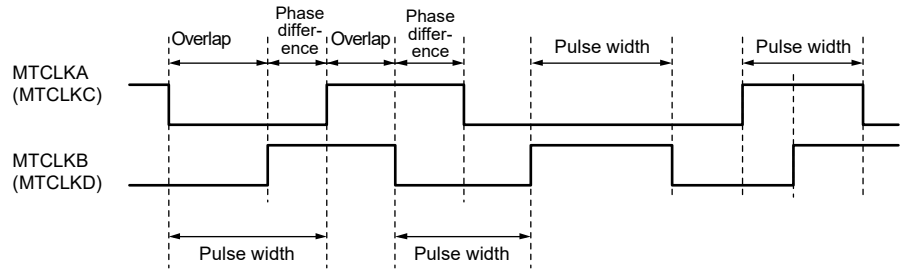
19.6 Usage Notes

19.6.1 Module Stop Function Setting

MTU operation can be disabled or enabled using the module stop control register. MTU operation is stopped with the initial setting. Register access is enabled by clearing the module clock stop status. For details, see section 9, Low-Power Consumption Function.

19.6.2 Input Clock Restrictions

The input clock pulse width must be at least 3 cycles of the PCLKC clock for single-edge detection, and at least 5 cycles of the PCLKC clock for both-edge detection. The MTU will not operate properly at narrower pulse widths.
In phase counting mode, the phase difference and overlap between the 2 input clocks must be at least 3 cycles of the PCLKC clock, and the pulse width must be at least 5 cycles of the PCLKC clock. Figure 19.133 shows the input clock conditions in phase counting mode.



Note: Phase difference and overlap: 3 PCLKC cycles or more
Pulse width: 5 PCLKC cycles or more

Figure 19.133 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

19.6.3 Note on Cycle Setting

When counter clearing on compare match is set, TCNT is cleared in the final state in which it matches the TGR value (the point at which TCNU updates the matched count value). Consequently, the actual counter frequency is given by the following formula:

- MTU0 to MTU4 and MTU6 to MTU8

$$f = \frac{CNTCLK}{(N + 1)}$$

- MTU5

$$f = \frac{CNTCLK}{N}$$

f: Counter frequency
CNTCLK: The counter-clock frequency set by TCR.TPSC[2:0] and TCR2.TPSC2[2:0]
N: TGR setting

19.6.4 Contention between TCNT Write and Clear Operations

If the counter clear signal is generated in the T2 state of a TCNT write cycle, TCNT clearing takes precedence and TCNT write operation is not performed.

Figure 19.134 shows the timing in this case.

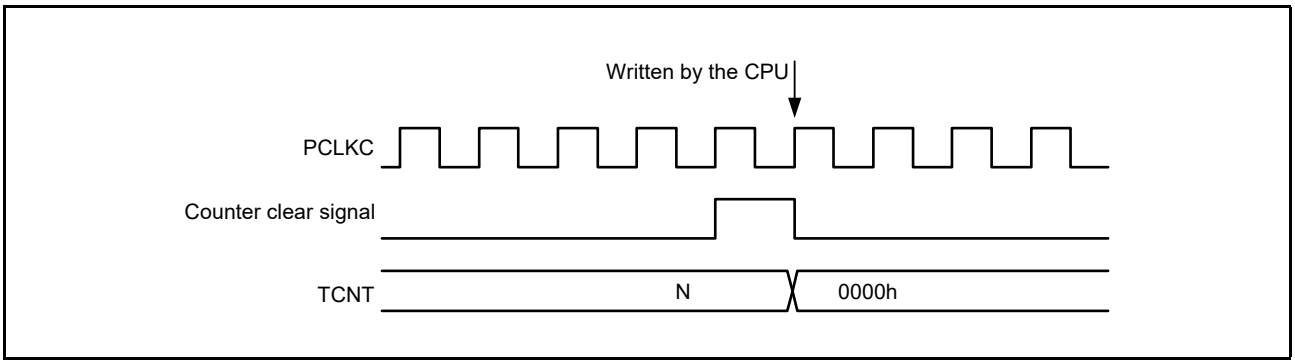


Figure 19.134 Contention between TCNT Write and Clear Operations

19.6.5 Contention between TCNT Write and Increment Operations

If incrementing occurs in the T2 state of a TCNT write cycle, TCNT write operation takes precedence and TCNT is not incremented.

Figure 19.135 shows the timing in this case.

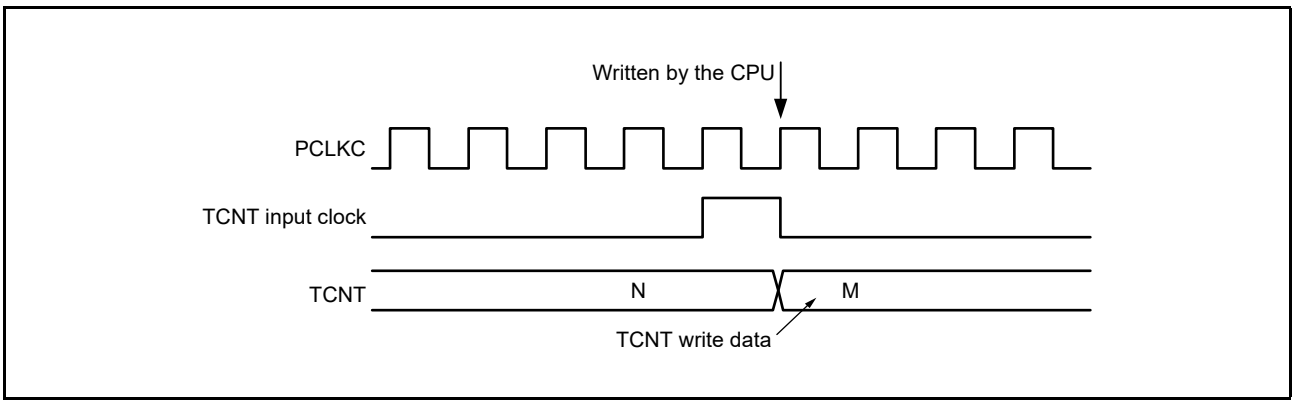


Figure 19.135 Contention between TCNT Write and Clear Operations

19.6.6 Contention between TGR Write Operation and Compare Match

If a compare match occurs in a TGR write cycle, TGR write operation is executed and the compare match signal is also generated.

Figure 19.136 shows the timing in this case.

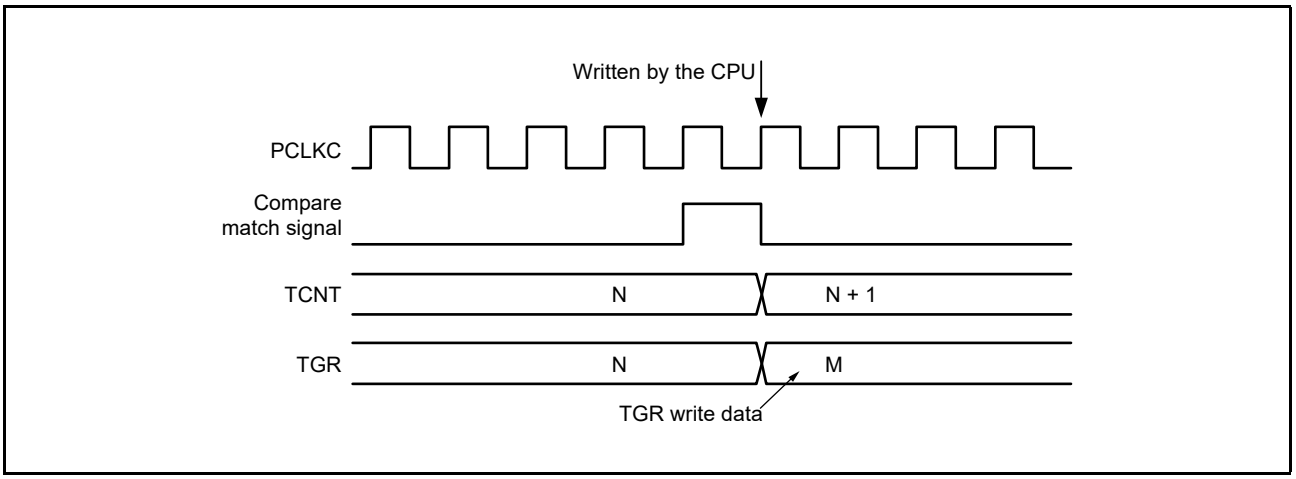


Figure 19.136 Contention between TGR Write Operation and Compare Match

19.6.7 Contention between Buffer Register Write Operation and Compare Match

If a compare match occurs in a TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.

Figure 19.137 shows the timing in this case.

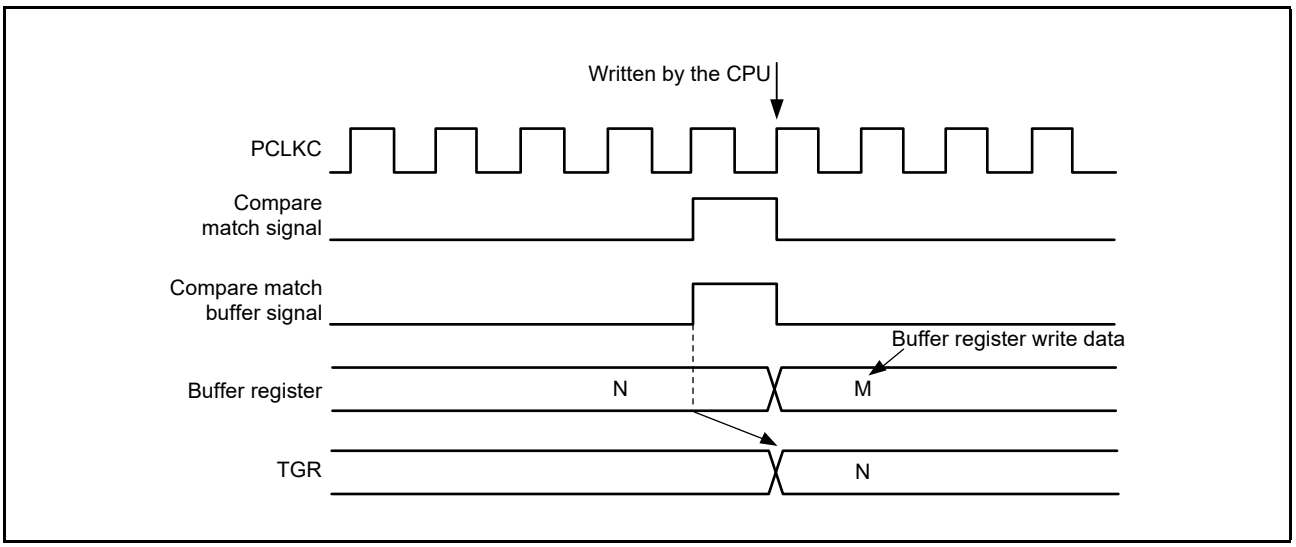


Figure 19.137 Contention between Buffer Register Write Operation and Compare Match

19.6.8 Contention between Buffer Register Write and TCNT Clear Operations

When the buffer transfer timing is set at the TCNT clear timing by the timer buffer operation transfer mode register (TBTM), if TCNT clearing occurs in the T2 state in a TGR write cycle, the data before write operation is transferred to TGR by the buffer operation.

Figure 19.138 shows the timing in this case.

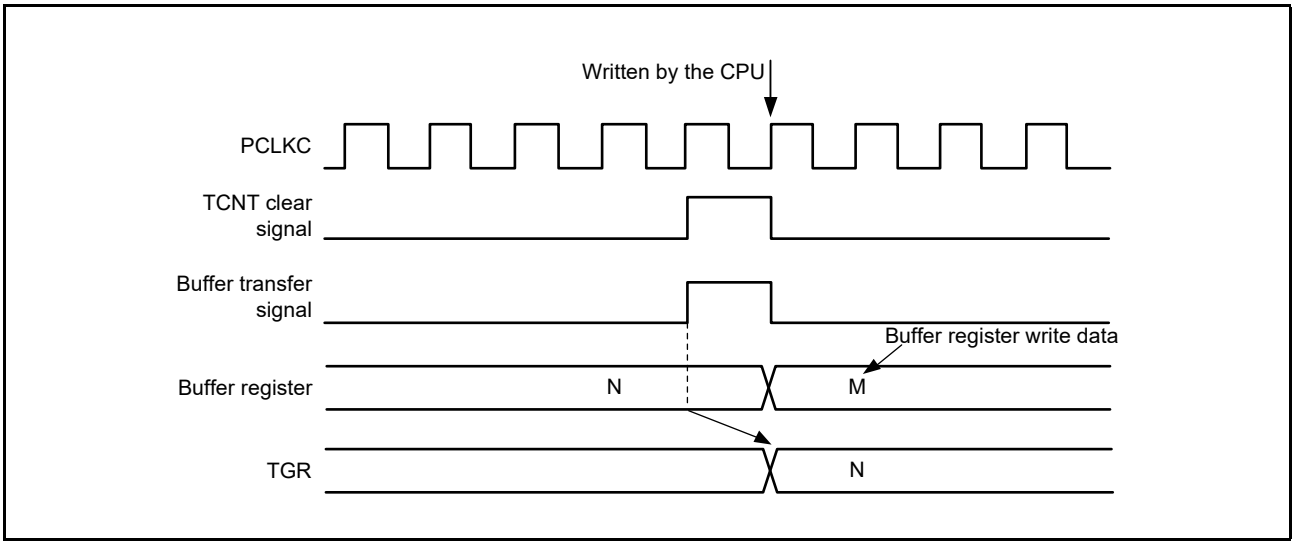


Figure 19.138 Contention between Buffer Register Write and TCNT Clear Operations

19.6.9 Contention between TGR Read Operation and Input Capture

If an input capture signal is generated in the T1 state in a TGR read cycle, the data before input capture transfer is read. Figure 19.139 shows the timing in this case.

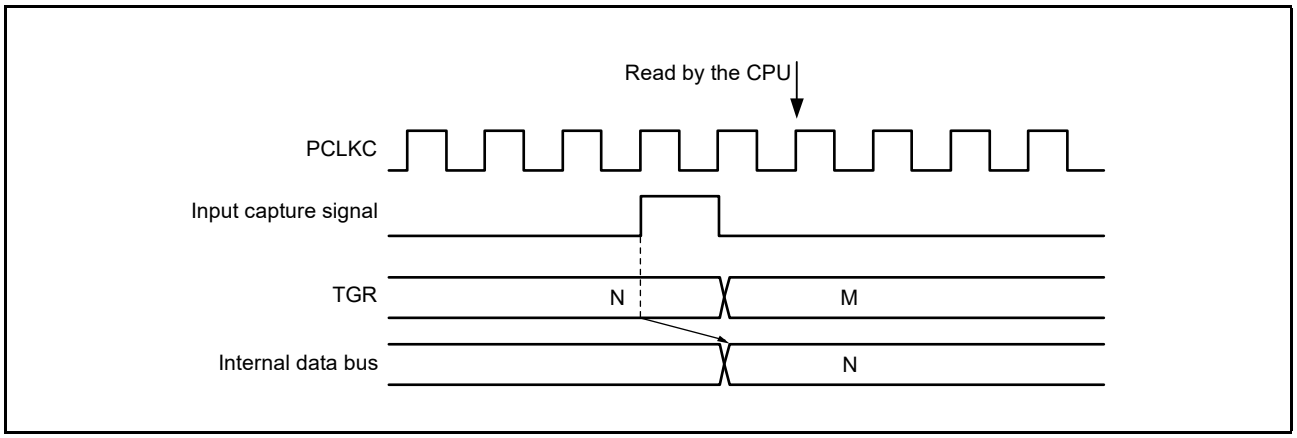


Figure 19.139 Contention between TGR Read Operation and Input Capture (MTU0 to MTU8)

19.6.10 Contention between TGR Write Operation and Input Capture

If an input capture signal is generated in a TGR write cycle, the input capture operation takes precedence and the TGR write operation is not performed in MTU0 to MTU4 and MTU6 to MTU8. In MTU5, the TGR write operation is performed and the input capture signal is generated.
Figure 19.140 and Figure 19.141 show the timing in this case.

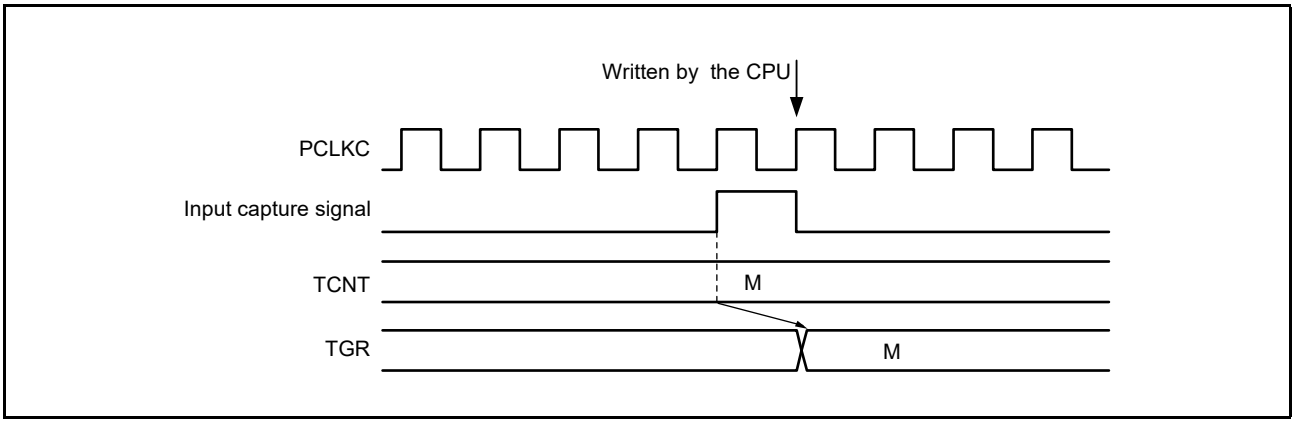


Figure 19.140 Contention between TGR Write Operation and Input Capture (MTU0 to MTU4 and MTU6 to MTU8)

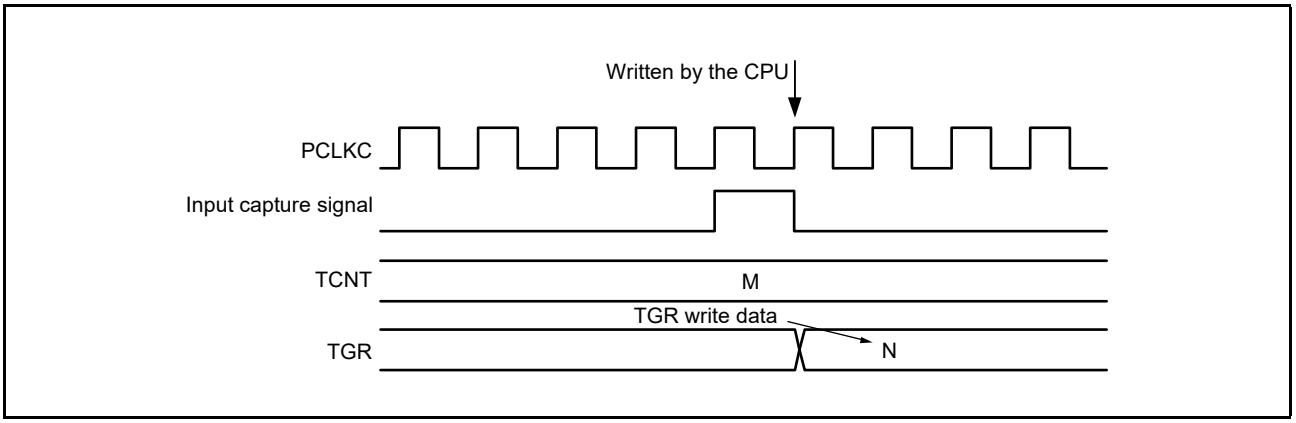


Figure 19.141 Contention between TGR Write Operation and Input Capture (MTU5)

19.6.11 Contention between Buffer Register Write Operation and Input Capture

If an input capture signal is generated in a buffer register write cycle, the buffer operation takes precedence and the buffer register write operation is not performed.

Figure 19.142 shows the timing in this case.

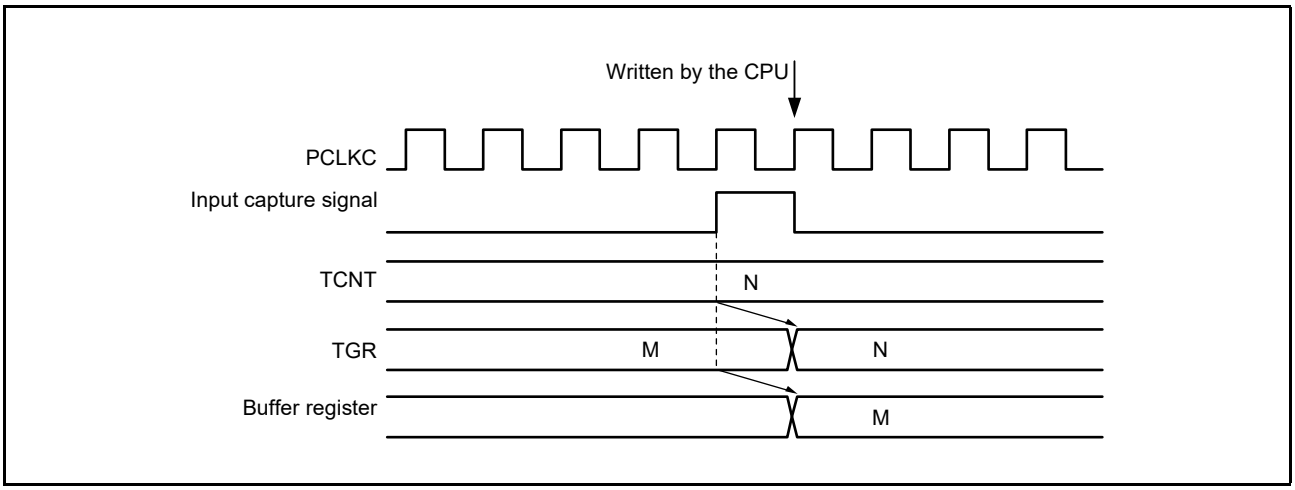


Figure 19.142 Contention between Buffer Register Write Operation and Input Capture

19.6.12 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

With timer counters MTU1.TCNT and MTU2.TCNT in a cascade, when a contention occurs between MTU1.TCNT counting (an MTU2.TCNT overflow/underflow) and the MTU2.TCNT writing, the MTU2.TCNT write operation is performed and the MTU1.TCNT count signal is disabled. In this case, if MTU1.TGRA works as a compare match register and there is a match between the MTU1.TGRA and MTU1.TCNT values, a compare match signal is issued. Furthermore, when the MTU1.TCNT count clock is selected as the input capture source of MTU0, MTU0.TGRA to MTU0.TGRD work in input capture mode. In addition, when the MTU0.TGRC compare match/input capture is selected as the input capture source of MTU1.TGRB, MTU1.TGRB works in input capture mode.

Figure 19.143 shows the timing in this case.

When setting the TCNT clearing function in cascaded operation, be sure to synchronize MTU1 and MTU2.

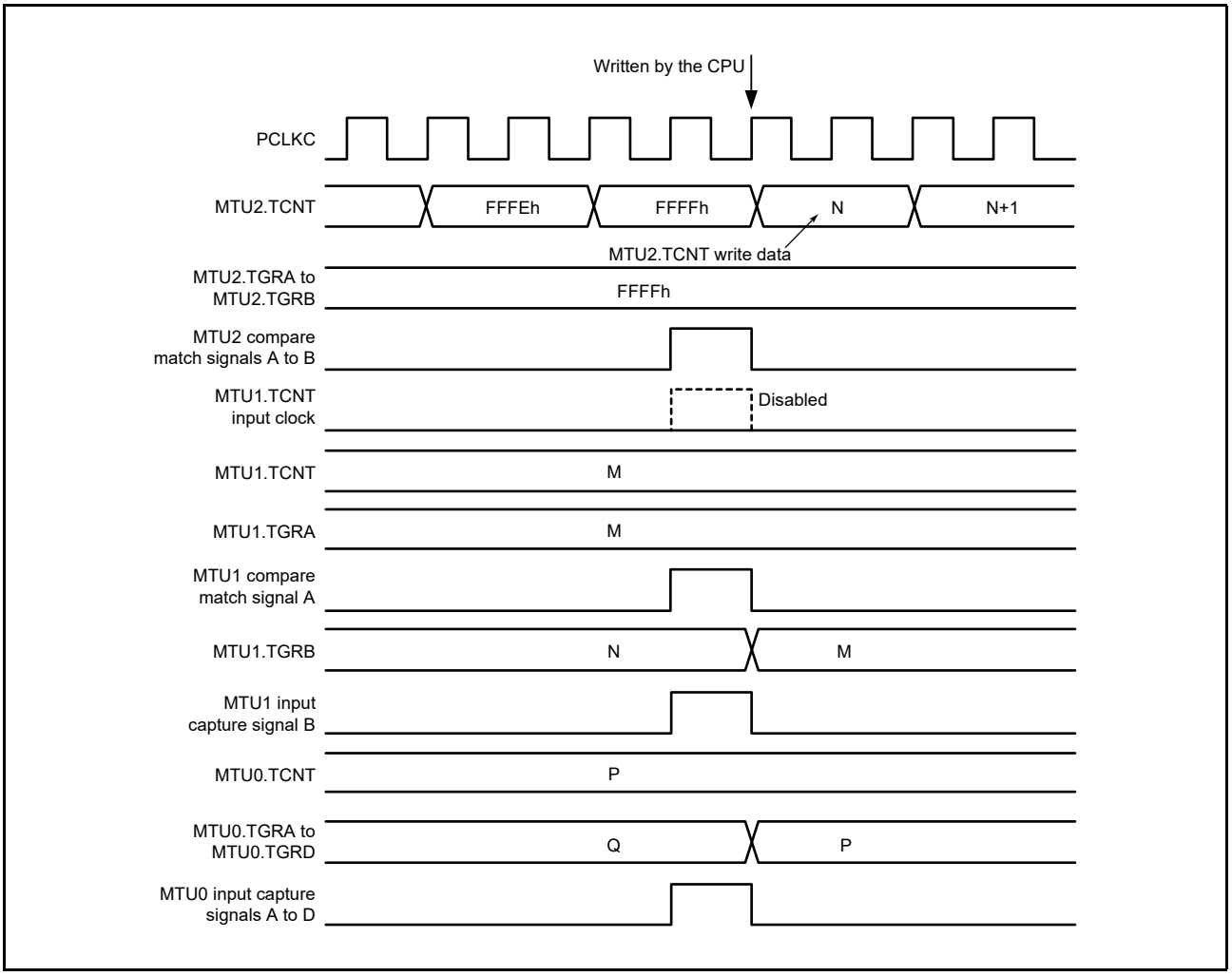


Figure 19.143 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation

19.6.13 Counter Value when Stopped in Complementary PWM Mode

When counting operation in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) is stopped in complementary PWM mode, the MTU3.TCNT (MTU6.TCNT) value is set to the timer dead time register (TDDRA (TDDRB)) value and MTU4.TCNT (MTU7.TCNT) is set to 0000h.
When operation is restarted in complementary PWM mode, counting begins automatically from the initial setting state. Figure 19.144 shows this operation.
When counting begins in another operating mode, be sure to make initial settings in MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT).

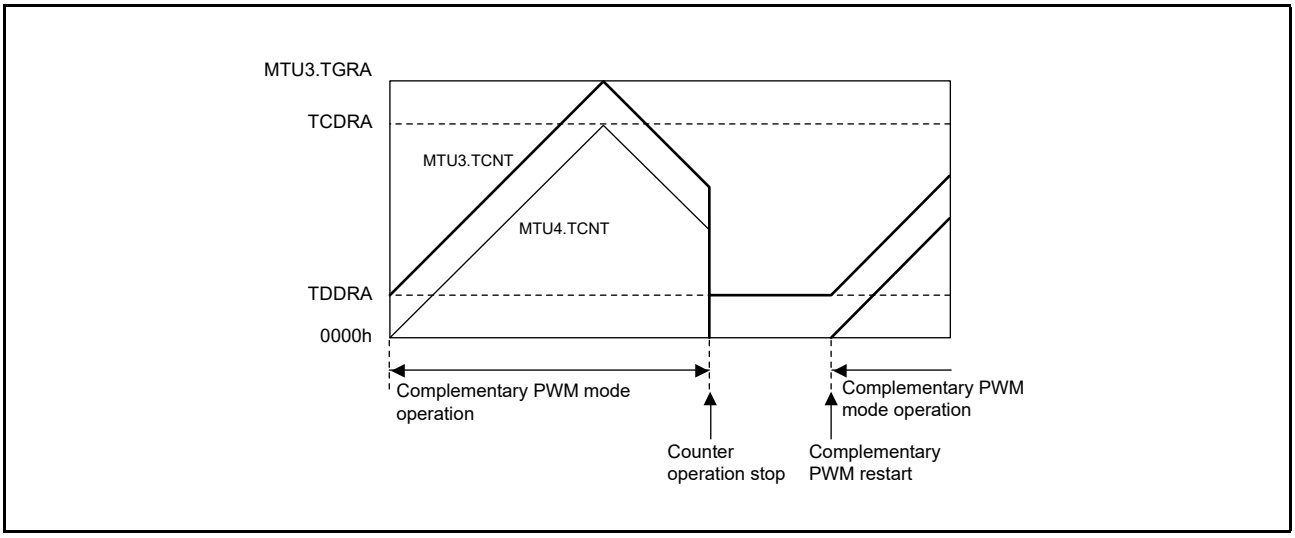


Figure 19.144 Counter Value when Stopped in Complementary PWM Mode

19.6.14 Buffer Operation Setting in Complementary PWM Mode

When modifying the PWM cycle set register (MTU3.TGRA or MTU6.TGRA), timer cycle data register (TCDRA or TCDRB), and duty set registers (MTU3.TGRB, MTU4.TGRA, and MTU4.TGRB (MTU6.TGRB, MTU7.TGRA, and MTU7.TGRB)) in complementary PWM mode, be sure to use buffer operation.
In addition, set the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the BFA bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1. Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the BFB bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.
In complementary PWM mode, buffer operation in MTU3 and MTU4 (or MTU6 and MTU7) depends on the settings in bits BFA and BFB of MTU3.TMDR1 (MTU6.TMDR1). When the BFA bit in MTU3.TMDR1 (MTU6.TMDR1) is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA), and TCBRA (TCBRB) functions as a buffer register for TCDRA (TCDRB).

19.6.15 Buffer Operation and Compare Match in Reset-Synchronized PWM Mode

When setting buffer operation in reset-synchronized PWM mode, set the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) to 0. The MTIOC4C (MTIOC7C) pin cannot output waveforms if the BFA bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.

Likewise, the MTIOC4D (MTIOC7D) pin cannot output waveforms if the BFB bit in MTU4.TMDR1 (MTU7.TMDR1) is set to 1.

In reset-synchronized PWM mode, buffer operation in MTU3 and MTU4 (or MTU 6 and MTU7) depends on the settings in the BFA and BFB bits of MTU3.TMDR1 (MTU6.TMDR1). For example, if the BFA bit in MTU3.TMDR1 (MTU6.TMDR1) is set to 1, MTU3.TGRC (MTU6.TGRC) functions as a buffer register for MTU3.TGRA (MTU6.TGRA). At the same time, MTU4.TGRC (MTU7.TGRC) functions as a buffer register for MTU4.TGRA (MTU7.TGRA).

While the MTU3.TGRC (MTU6.TGRC) and MTU3.TGRD (MTU6.TGRD) are operating as buffer registers, a TGImn interrupt (m = C, D; n = 3, 4, or 6, 7) is not generated.

Figure 19.145 shows an example of MTU3.TGR (MTU6.TGR), MTU4.TGR (MTU7.TGR), MTIOC3 (MTIOC6), and MTIOC4 (MTIOC7) operation with the BFA and BFB bits in MTU3.TMDR1 (MTU6.TMDR1) set to 1 and the BFA and BFB bits in MTU4.TMDR1 (MTU7.TMDR1) set to 0.

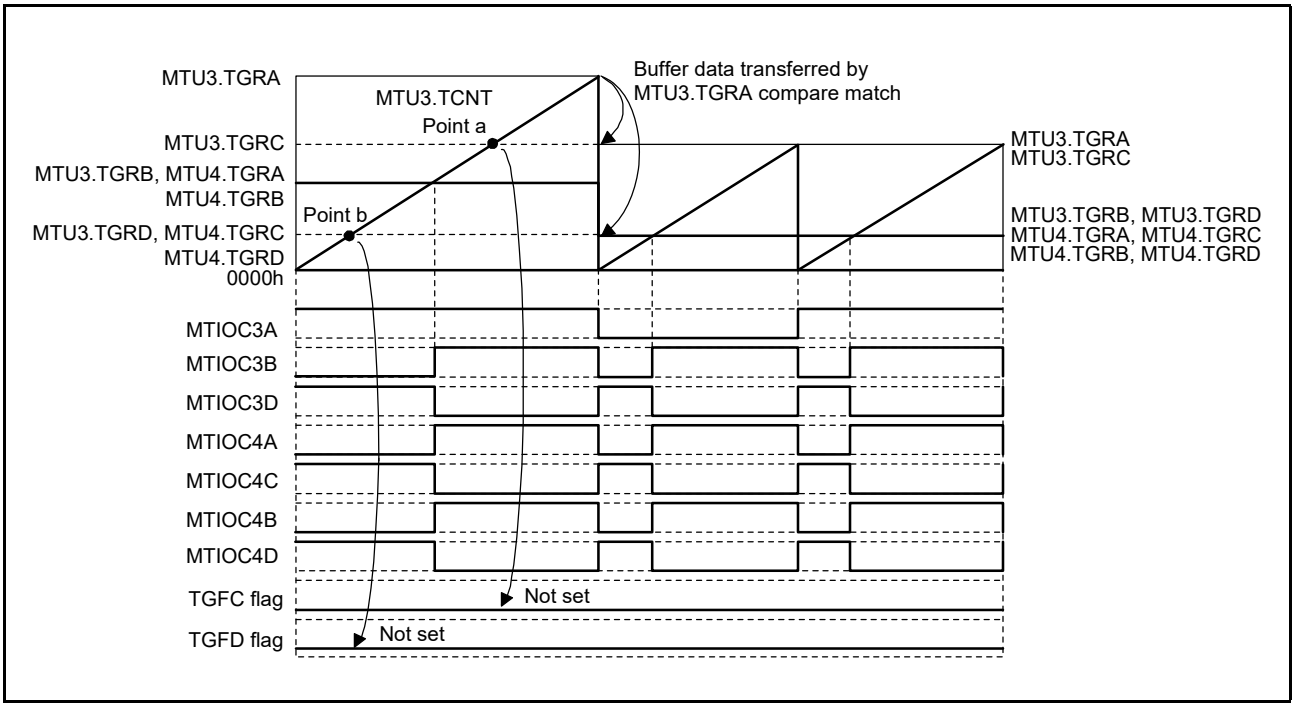


Figure 19.145 Buffer Operation and Compare Match in Reset-Synchronized PWM Mode

19.6.16 Overflow in Reset-Synchronized PWM Mode

After reset-synchronized PWM mode is selected, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) start counting when the CST3 (CST6) bit of TSTRA (TSTRB) is set to 1. In this state, the MTU4.TCNT (MTU7.TCNT) count clock source and count edge are determined by the MTU3.TCR (MTU6.TCR) setting.
In reset-synchronized PWM mode, with cycle register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match selected as the counter clearing source, MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) count up to FFFFh, then a compare match occurs with MTU3.TGRA (MTU6.TGRA), and MTU3.TCNT and MTU4.TCNT (MTU6.TCNT and MTU7.TCNT) are both cleared. In this case, a TCIVn interrupt (n = 3, 4, or 6, 7) is not generated.
Figure 19.146 shows an example of TCFV flag operation in reset-synchronized PWM mode with cycle register MTU3.TGRA (MTU6.TGRA) set to FFFFh and the MTU3.TGRA (MTU6.TGRA) compare match specified for the counter clearing source.

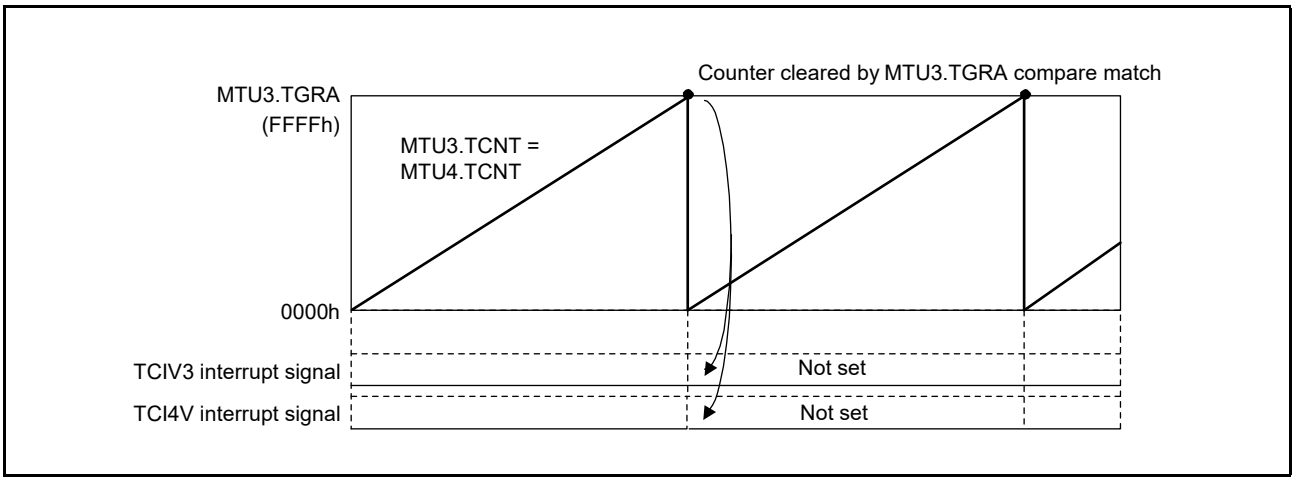


Figure 19.146 Overflow in Reset-Synchronized PWM Mode

19.6.17 Contention between Overflow/Underflow and Counter Clearing

If an overflow/underflow and counter clearing occur simultaneously, a TCIVn interrupt (n = 0 to 4, 6 to 8) nor a TCIUn interrupt (n = 1 or 2) is generated and TCNT clearing takes precedence.
Figure 19.147 shows the operation timing when a TGR compare match is specified as the clearing source and TGR is set to FFFFh.

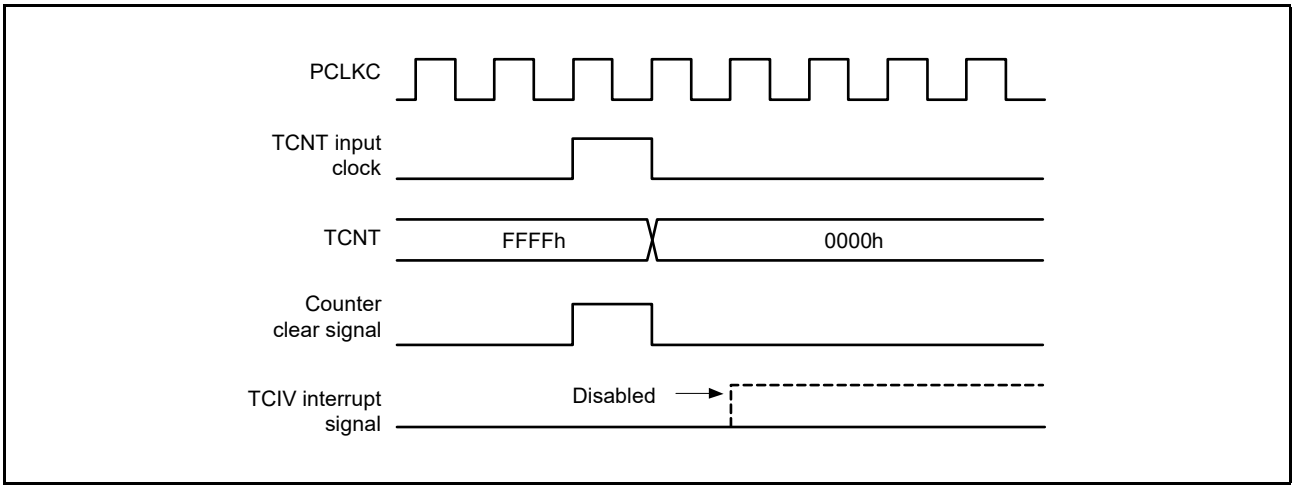


Figure 19.147 Contention between Overflow and Counter Clearing

19.6.18 Contention between TCNT Write Operation and Overflow/Underflow

If TCNT counts up or down in a TCNT write cycle and an overflow or an underflow occurs, the TCNT write operation takes precedence. A TCIVn interrupt (n = 0 to 4, 6 to 8) nor a TCIUn interrupt (n = 1 or 2) is generated.
Figure 19.148 shows the operation timing when there is contention between TCNT write operation and overflow.

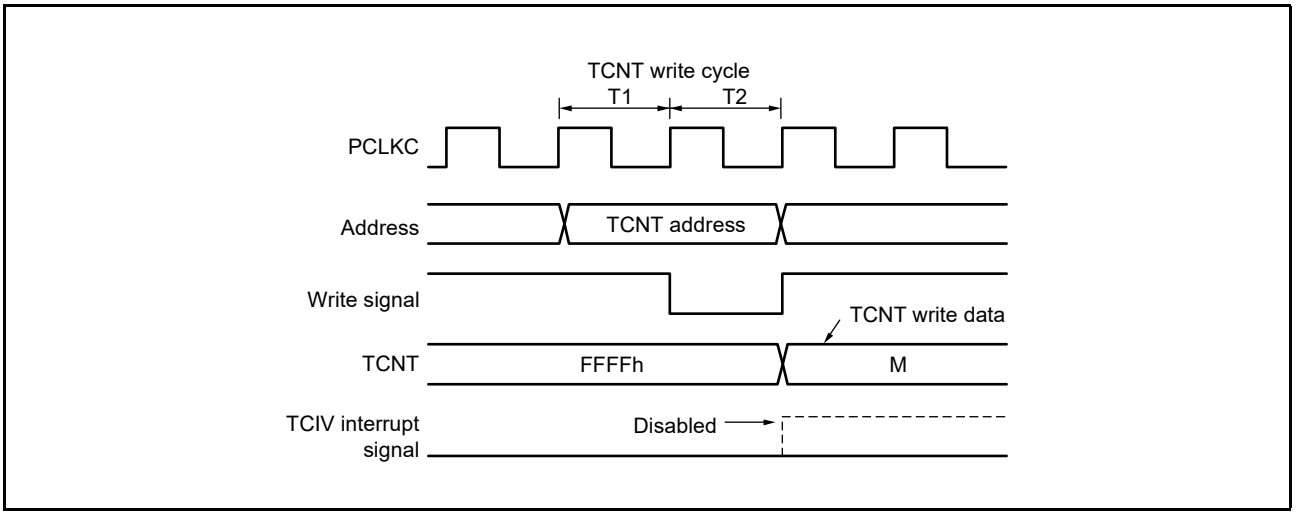


Figure 19.148 Contention between TCNT Write Operation and Overflow

19.6.19 Note on Transition from Normal Mode or PWM Mode 1 to Reset-Synchronized PWM Mode

When making a transition from normal operation or PWM mode 1 to reset-synchronized PWM mode in MTU3 and MTU4 (or MTU6 and MTU7), if the counter is stopped while the output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIOC7D) are held at a high level and then operation is started after a transition to reset-synchronized PWM mode, the initial pin output will not be correct.

When making a transition from normal mode to reset-synchronized PWM mode, write 11h to MTU3.TIORH, MTU3.TIORL, MTU4.TIORH, and MTU4.TIORL (MTU6.TIORH, MTU6.TIORL, MTU7.TIORH, and MTU7.TIORL) to initialize the output pin state to a low level, then set the registers to the initial value (00h) before making the mode transition.

When making a transition from PWM mode 1 to reset-synchronized PWM mode, switch to normal mode, initialize the output pin state to a low level, and then set the registers to the initial value (00h) before making the transition to reset-synchronized PWM mode.

19.6.20 Output Level in Complementary PWM Mode and Reset-Synchronized PWM Mode

When MTU3 and MTU4 (or MTU6 and MTU7) are in complementary PWM mode or reset-synchronized PWM mode, the PWM waveform output level is determined by the OLSP and OLSN bits in TOCR1A and TOCR1B. In complementary PWM mode or reset-synchronized PWM mode, TIOR should be set to 00h.

The output level in negative phase when the TDERA.TDER or TDERB.TDER bit is set to 0 in complementary PWM mode (the dead time is not generated) does not depend on the setting of the TOCR1A.OLSN or TOCR1B.OLSN bit. It is equivalent to the inverted level of positive phase output based on the setting of the TOCR1A.OLSP or TOCR1B.OLSP bit.

19.6.21 Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection

When timer counters 1 and 2 (MTU1.TCNT and MTU2.TCNT) operate as a 32-bit counter in cascade connection, the cascaded counter value cannot be captured successfully in some cases even if input-capture input is simultaneously done to MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B. This is because the input timing of MTIOC1A and MTIOC2A or to MTIOC1B and MTIOC2B may not be the same when external input-capture signals input into MTU1.TCNT and MTU2.TCNT are taken in synchronization with the internal clock.

For example, MTU1.TCNT (the counter for upper 16 bits) does not capture the count-up value by an overflow from MTU2.TCNT (the counter for lower 16 bits) but captures the count value before the up-counting. In this case, the values of MTU1.TCNT = FFF1h and MTU2.TCNT = 0000h should be transferred to MTU1.TGRA and MTU2.TGRA or to MTU1.TGRB and MTU2.TGRB, but the values of MTU1.TCNT = FFF0h and MTU2.TCNT = 0000h are erroneously transferred.

The MTU has a new function that allows simultaneous capture of MTU1.TCNT and MTU2.TCNT with a single input capture input as the trigger. This function allows reading of the 32-bit counter such that MTU1.TCNT and MTU2.TCNT are captured at the same time. For details, see section 19.2.11, Timer Input Capture Control Register (TICCR).

19.6.22 Interrupt-Skipping Function 2

When interrupt-skipping function 2 is in use and the difference between the values in MTU4.TADCORA and MTU4.TADCORB is small, correct counting of the number skipped may not be possible, in which case requests for A/D conversion will not be generated with the expected timing. The conditions listed below thus apply to these settings.
For MTU6 and MTU7, the same conditions apply to the settings of MTU7.TADCORA and MTU7.TADCORB.

(1) When the number skipped is zero for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least four.
- The interval of comparison for MTU4.TADCORA must be at least four cycles of PCLKC (the updated value of MTU4.TADCORA is set to the previous value plus or minus at least four).
- The interval of comparison for MTU4.TADCORB must be at least four cycles of PCLKC (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least four).

(2) When the number skipped is one or more for skipping function 2

- The difference between the values in MTU4.TADCORA and MTU4.TADCORB must be at least two.
- The interval of comparison for MTU4.TADCORB must be at least two cycles of PCLKC (the updated value of MTU4.TADCORB is set to the previous value plus or minus at least two).

19.6.23 Notes when Complementary PWM Mode Output Protection Function is not Used

The complementary PWM mode output protection function is initially enabled. If it is not used, write 00h in the POE2.POECR1 and POE2.POECR2 registers.

19.6.24 Notes Regarding Timer Counter (MTU5.TCNT) and Timer General Register (MTU5.TGR)

Do not set an MTU5.TGRj (j = U, V, W) bit to the value of the corresponding MTU5.TCNTj (j = U, V, W) plus one while counting by the MTU5.TCNTj (j = U, V, W) register is stopped. If an MTU5.TGRj (j = U, V, W) bit is set to the value of the corresponding MTU5.TCNTj (j = U, V, W) plus one while counting by the MTU5.TCNTj (j = U, V, W) is stopped, a compare-match will be generated even though counting is stopped.
In this case, if the compare match enable bit (MTU5.TIER.TGIE5j (j = U, V, W)) is set to 1 (enabling interrupts), a compare-match interrupt will also be generated. If the value of the timer compare match clear register is 1 (enabled), the timer is automatically cleared to 0000h when the compare-match is generated, regardless of whether interrupts from the MTU5.TCNTj (j = U, V, W) are enabled or disabled.

19.6.25 Points for Caution to Prevent Malfunctions in Synchronous Clearing for Complementary PWM Mode

If control of the output waveform is enabled (TWCR.WRE bit = 1) at the time of synchronous counter clearing in complementary PWM mode, satisfaction of either condition 1 or 2 below has the following effects.

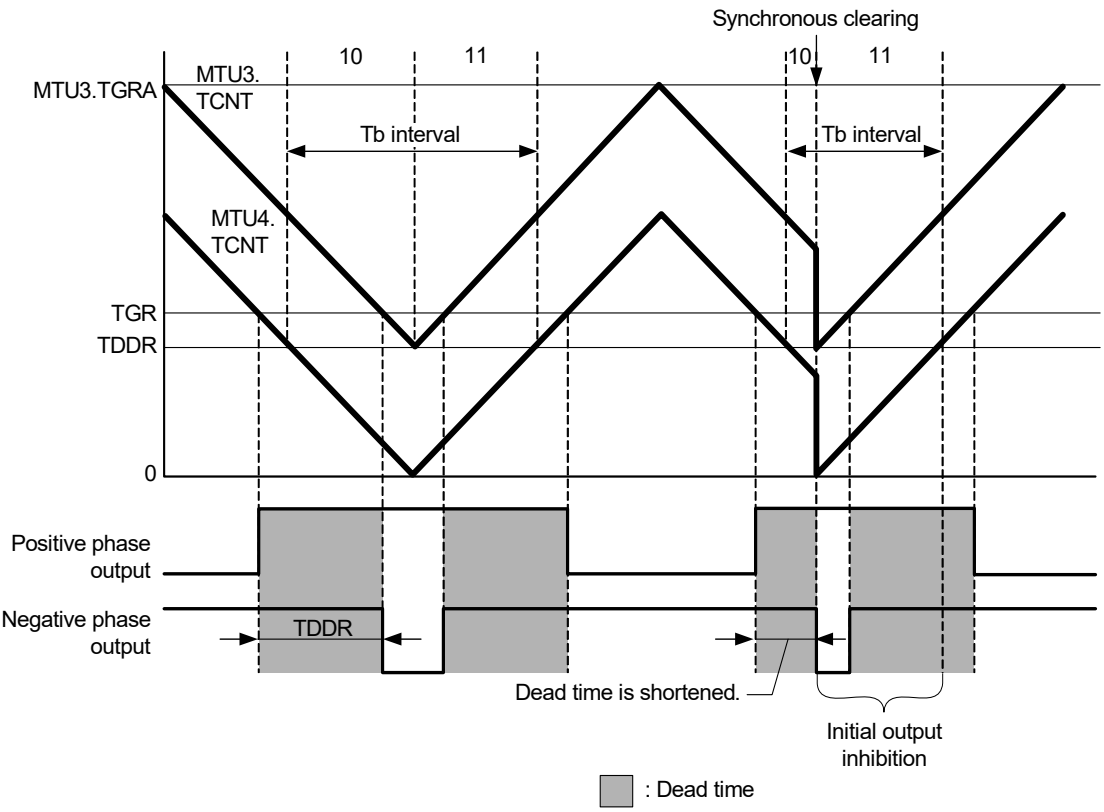
- Dead time on the PWM output pins is shortened (or disappears).
- The active level is output on the PWM negative phase output pins beyond the period for active-level output.

Condition 1: In portion (10) of the initial output inhibition period in Figure 19.149, when synchronous clearing occurs within the dead-time period for PWM output.

Condition 2: In portions (10) and (11) of the initial output inhibition period in Figure 19.150, synchronous clearing occurs when any condition from among MTU3.TGRB (MTU6.TGRB) ≤ TDDRA (TDDRB), MTU4.TGRA (MTU7.TGRA) ≤ TDDRA (TDDRB), or MTU4.TGRB (MTU7.TGRB) is satisfied.

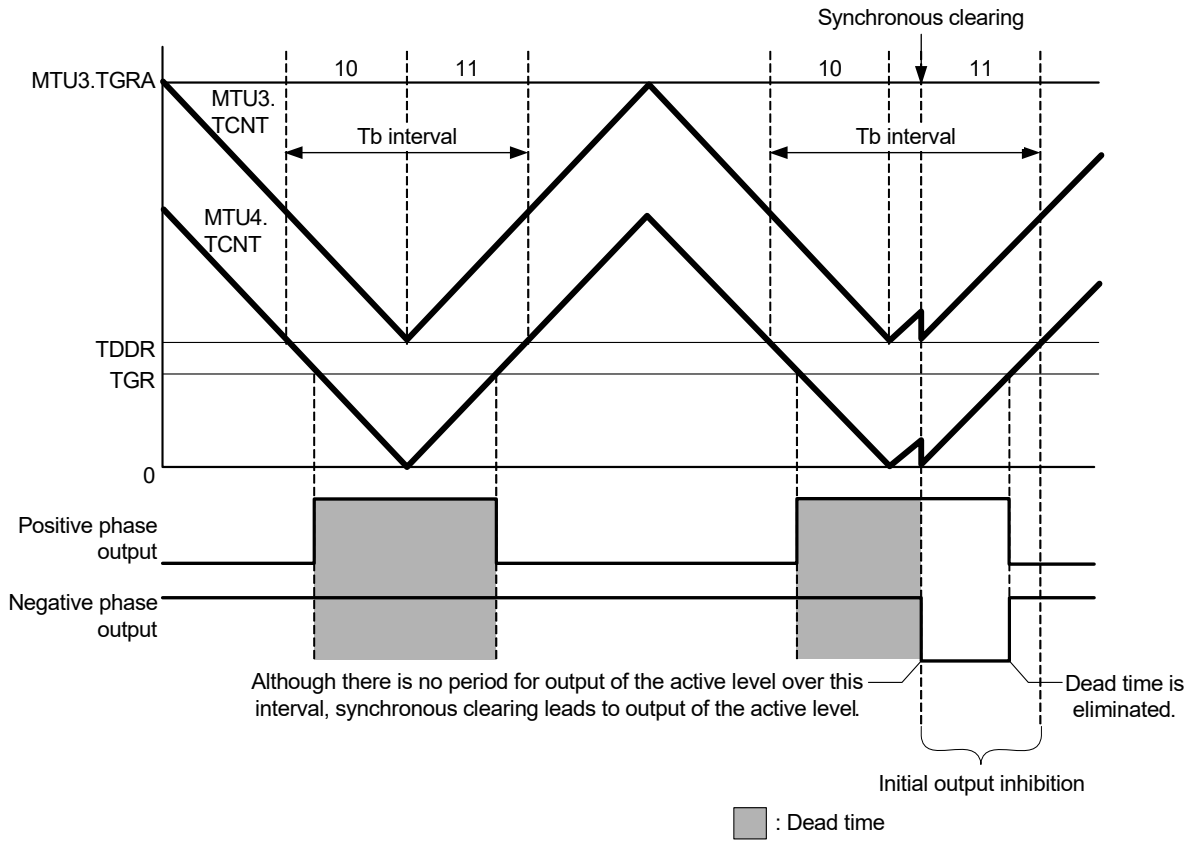
The following method avoids the above phenomena.

Ensure that synchronous clearing proceeds with the value of each of comparison registers MTU3.TGRB (MTU6.TGRB), MTU4.TGRA (MTU7.TGRA), and MTU4.TGRB (MTU7.TGRB) set to at least double the value of the TDDRA register (TDDRB register).



Note: PWM output is active low over the dead time.

Figure 19.149 Example of Synchronous Clearing (when Condition 1 Applies)



Note: PWM output is active low.

Figure 19.150 Example of Synchronous Clearing (when Condition 2 Applies)

19.6.26 Notes on Timer Mode Register Setting for ELC Event Input

When MTU is used in ELC operation, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

19.6.27 Continuous Output of Interrupt Signal in Response to a Compare Match

When the TGR register is set to 0000h, PCLK/1 clock is set as the counter clock, and compare match is set as the trigger for clearing of the counter clock, the value of the TCNT counter remains 0000h, and the interrupt signal will be output continuously (i.e. its level will be flat) rather than output over a single cycle. Consequently, interrupts will not be detected in response to second and subsequent compare matches.

Figure 19.151 shows the timing for continuous output of the interrupt signal in response to a compare match.

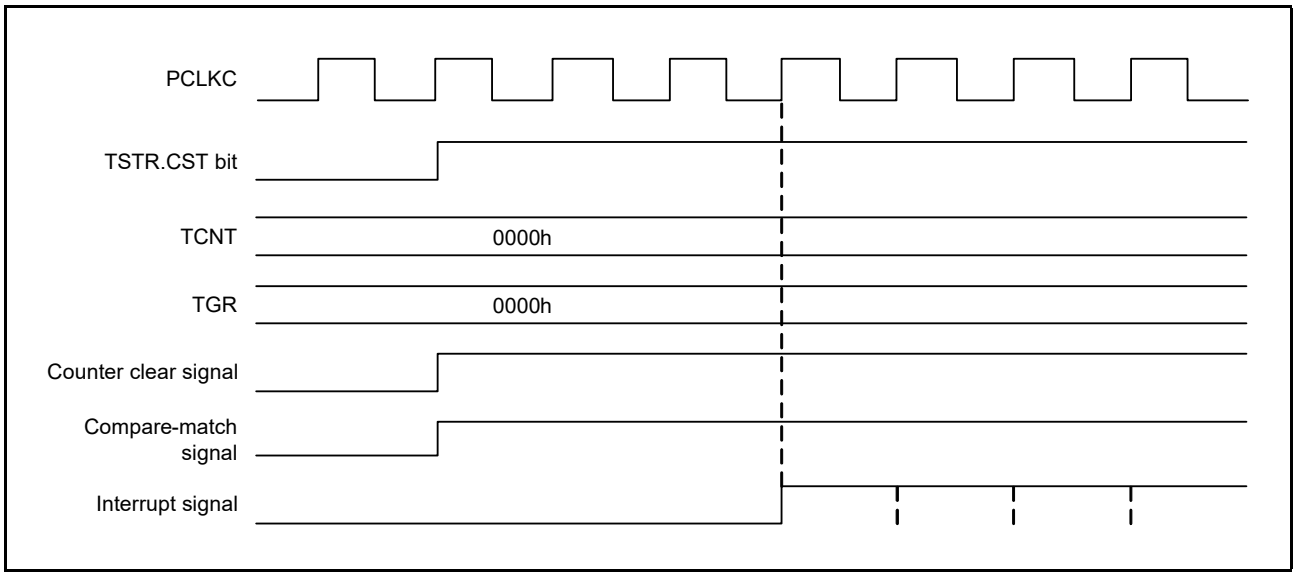


Figure 19.151 Continuous Output of Interrupt Signal in Response to a Compare Match

19.6.28 Notes on Port Settings in Complementary PWM Mode or Reset-Synchronized PWM Mode

When complementary PWM mode or reset-synchronized PWM mode is to be used, set the port pins for use as the 6-phase PWM output pins for channels 3 and 4 (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4C, MTIOC4B, and MTIOC4D) and channels 6 and 7 (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7C, MTIOC7B, and MTIO7D) in the groups in Table 19.79 and Table 19.80.
For the port settings, see section 18, Multi-Function Pin Controller (MPC).

Table 19.79 Output Pins for Channels 3 and 4

	Specified Port					
Port Group	**MTIOC3B**	**MTIOC3D**	**MTIOC4A**	**MTIOC4C**	**MTIOC4B**	**MTIOC4D**
1*1	P16	P15	P14	P13	P12	P11
2*2	PA2	PA1	PA0	P77	P76	P75
3*2	PB7	PF6	PF5	P87	P86	PD7

Table 19.80 Output Pins for Channels 6 and 7

	Specified Port					
Port Group	**MTIOC6B**	**MTIOC6D**	**MTIOC7A**	**MTIOC7C**	**MTIOC7B**	**MTIOC7D**
1*1	PS5	PS4	PS3	PS2	PS1	PS0
2*3	PA7	P70	PE7	P42	P22	PH6

Note 1. This port group is only available in 320-pin devices.
Note 2. This port group is available in both 320- and 176-pin devices.
Note 3. This port group is available in both 320- and 176-pin devices. Also, these pins are not under Hi-Z control by POE3.

19.7 MTU Output Pin Initialization

19.7.1 Operating Modes

The MTU has the following six operating modes. Waveforms can be output in any of these modes.

- Normal mode (MTU0 to MTU4 and MTU6 to MTU8)
- PWM mode 1 (MTU0 to MTU4, MTU6, and MTU7)
- PWM mode 2 (MTU0 to MTU2)
- Phase counting modes 1 to 5 (MTU1 and MTU2)
- Complementary PWM mode (MTU3, MTU4, MTU6, and MTU7)
- Reset-synchronized PWM mode (MTU3, MTU4, MTU6, and MTU7)

This section describes how to initialize the MTU output pins in each of these modes.

19.7.2 Operation in Case of Re-Setting Due to Error during Operation

If an error occurs during MTU operation, MTU output should be cut off by the system. The output can be cut off by allowing non-active level output from the pins by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports. MTU output can be disabled through TIOR settings. Complementary PWM output (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) should be specified through TOERA and TOERB settings. For PWM output pins, output can also be cut by hardware, using port output enable 3 (POE3). The pin initialization procedures for re-setting due to an error during operation and the procedures for restarting in a different mode after re-setting are described below.

The MTU has six operating modes, as stated above. There are thus 36 mode transition combinations, but some transitions are not available with certain channel and mode combinations. Available mode transition combinations are shown in Table 19.81.

Table 19.81 Mode Transition Combinations

	Normal	PWM1	PWM2	PCM	CPWM	RPWM
Normal	(1)	(2)	(3)	(4)	(5)	(6)
PWM1	(7)	(8)	(9)	(10)	(11)	(12)
PWM2	(13)	(14)	(15)	(16)	Not available	Not available
PCM	(17)	(18)	(19)	(20)	Not available	Not available
CPWM	(21)	(22)	Not available	Not available	(23) (24)	(25)
RPWM	(26)	(27)	Not available	Not available	(28)	(29)

Normal: Normal mode
PWM1: PWM mode 1
PWM2: PWM mode 2
PCM: Phase counting modes 1 to 5
CPWM: Complementary PWM mode
RPWM: Reset-synchronized PWM mode

19.7.3 Overview of Initialization Procedures and Mode Transitions in Case of Error during Operation

- When making a transition to a mode (Normal, PWM1, PWM2, or PCM) in which the pin output level is selected by the timer I/O control register (TIOR) setting, initialize the pins by means of TIOR setting.
- In PWM mode 1, waveforms are not output to the MTIOCnB and MTIOCnD (n = 3, 4, 6, or 7) pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In PWM mode 2, waveforms are not output to the cycle register pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In normal mode or PWM mode 2, if TGRC and TGRD operate as buffer registers, waveforms are not output to the corresponding pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- In PWM mode 1, if either TGRC or TGRD operates as a buffer register, waveforms are not output to the corresponding pins. If no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
- When making a transition to a mode (CPWM or RPWM) in which the pin output level is selected by the timer output control register (TOCR1A, TOCR2A, TOCR1B, or TOCR2B) setting, temporarily disable output in MTU3 and MTU4 (or MTU6 and MTU7) with the timer output master enable register (TOERA or TOERB). At this time, if no other module outputs signals through these pins, they enter high-impedance state. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports. Switch to normal mode, perform initialization with TIOR, restore TIOR to its initial value, then operate the MTU in accordance with the mode setting procedure (TOCR1A setting, TOCR2A setting, TMDR1 setting, and TOERA setting (TOCR1B setting, TOCR2B setting, TMDR1 setting, and TOERB setting)).

Note: Channel number is substituted for “n” indicated in this section, unless otherwise stated.

Pin initialization procedures are described below for the numbered combinations in Table 19.81. The active level is assumed to be low.

(1) Operation when Error Occurs in Normal Mode and Operation is Restarted in Normal Mode

Figure 19.152 shows a case in which an error occurs in normal mode and operation is restarted in normal mode after re-setting.

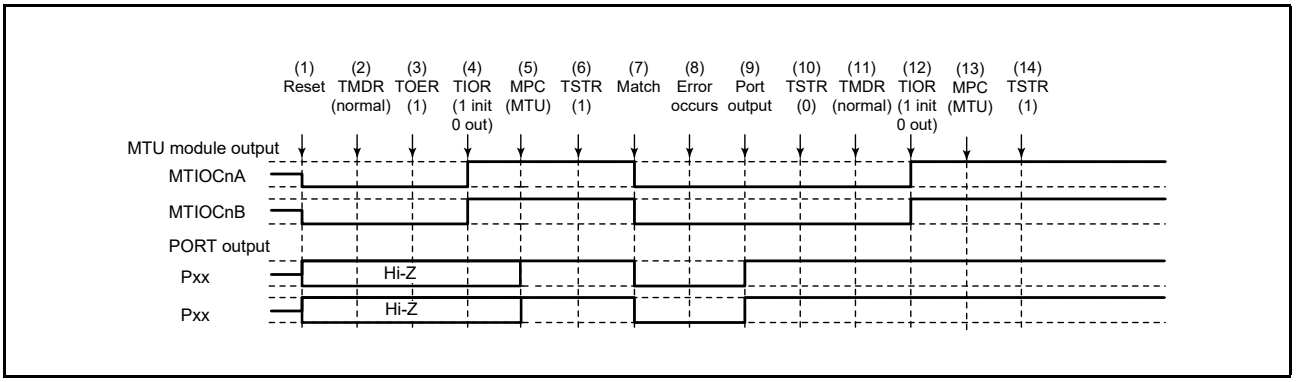


Figure 19.152 Error Occurrence in Normal Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) After a reset, the TMDR1 setting is for normal mode.
(3) For MTU3 and MTU4, enable output with TOERA before initializing the pins with TIOR.
(4) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA.
(11) This step is not necessary when restarting in normal mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(2) Operation when Error Occurs in Normal Mode and Operation is Restarted in PWM Mode 1

Figure 19.153 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 1 after re-setting.

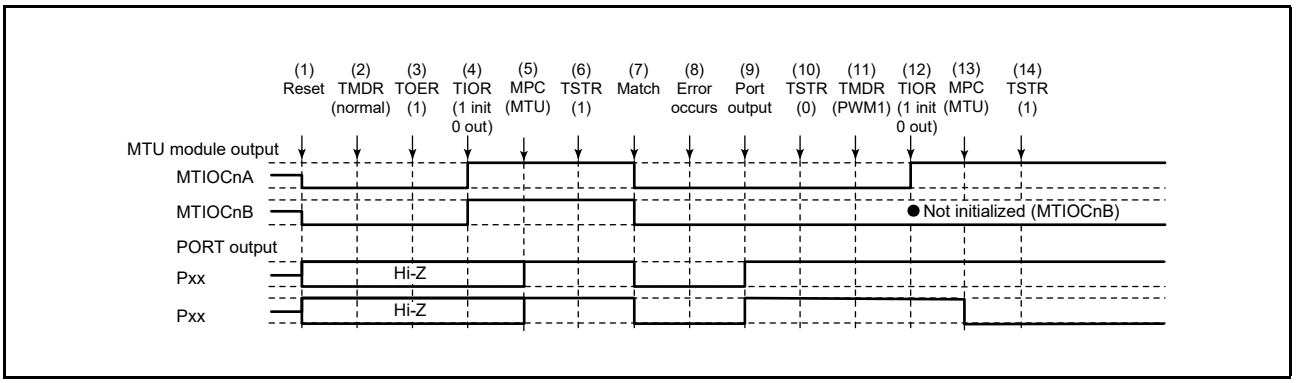


Figure 19.153 Error Occurrence in Normal Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 19.152.
(11) Set PWM mode 1.
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(3) Operation when Error Occurs in Normal Mode and Operation is Restarted in PWM mode 2

Figure 19.154 shows a case in which an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

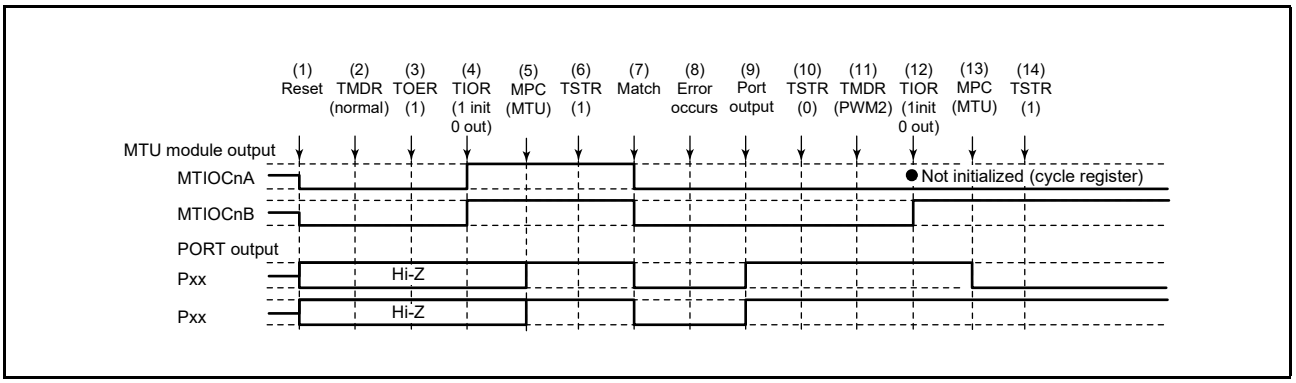


Figure 19.154 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 19.152.
(11) Set PWM mode 2.
(12) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: PWM mode 2 can only be selected for MTU0 to MTU2, and therefore TOERA setting is not necessary.

(4) Operation when Error Occurs in Normal Mode and Operation is Restarted in Phase Counting Mode

Figure 19.155 shows a case in which an error occurs in normal mode and operation is restarted in phase counting mode after re-setting.

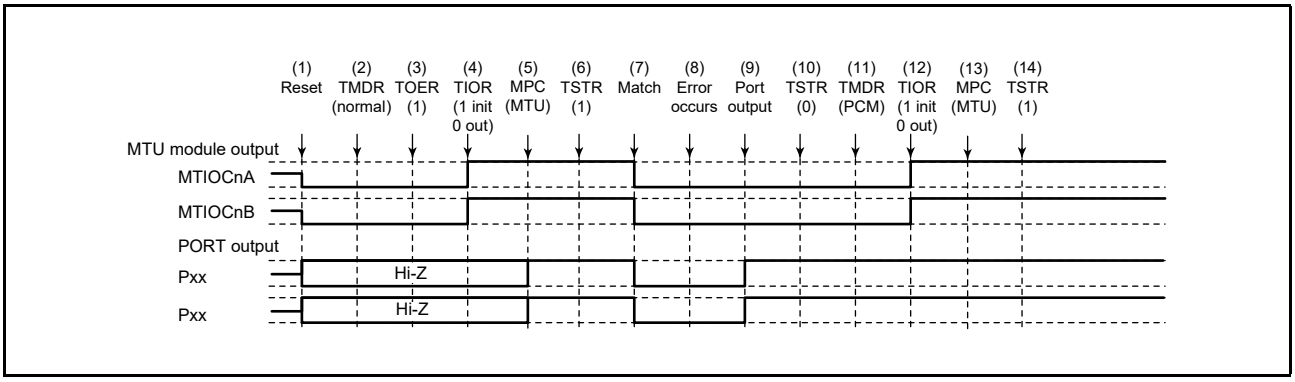


Figure 19.155 Error Occurrence in Normal Mode, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 19.152.
(11) Set the phase counting mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: The phase counting mode can only be selected for MTU1 and MTU2, and therefore TOERA setting is not necessary.

(5) Operation when Error Occurs in Normal Mode and Operation is Restarted in Complementary PWM Mode

Figure 19.156 shows a case in which an error occurs in normal mode and operation is restarted in complementary PWM mode after re-setting.

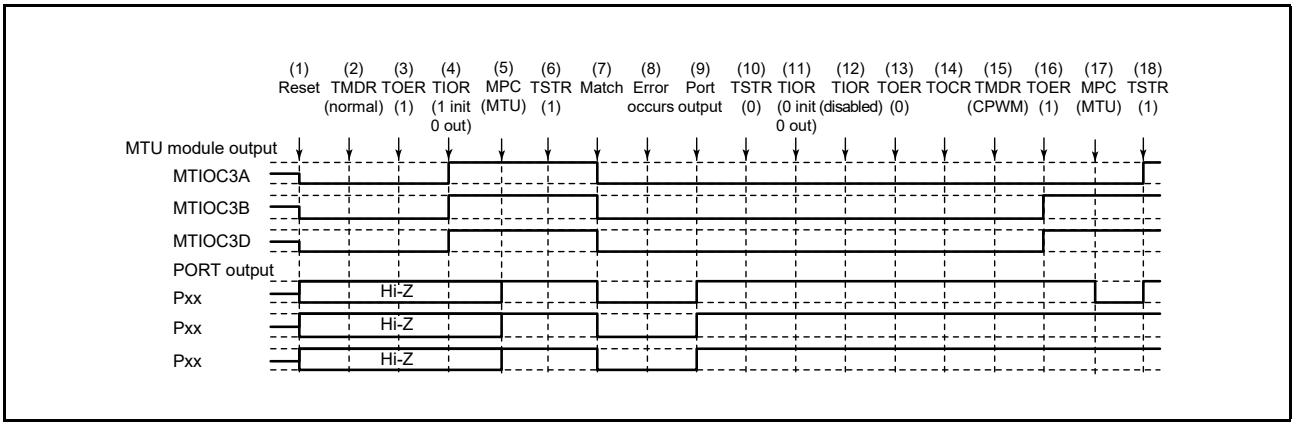


Figure 19.156 Error Occurrence in Normal Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 19.152.
(11) Initialize the normal mode waveform generation section with TIOR.
(12) Disable operation of the normal mode waveform generation section with TIOR.
(13) Disable output in MTU3 and MTU4 with TOERA.
(14) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(15) Set complementary PWM mode.
(16) Enable output in MTU3 and MTU4 with TOERA.
(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(18) Restart operation by setting TSTRA.

(6) Operation when Error Occurs in Normal Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 19.157 shows a case in which an error occurs in normal mode and operation is restarted in reset-synchronized PWM mode after re-setting.

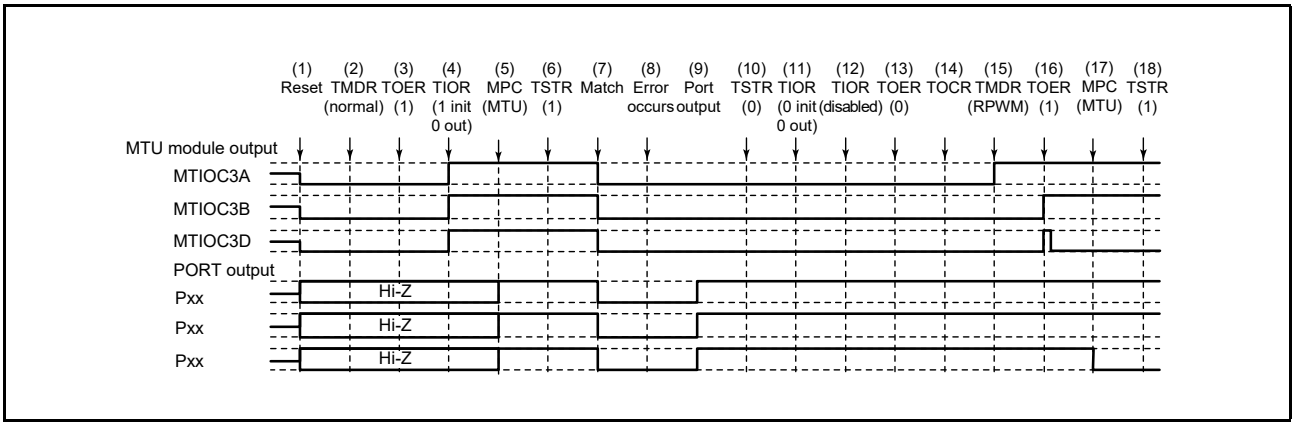


Figure 19.157 Error Occurrence in Normal Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (13) are the same as in Figure 19.152.
(14) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(15) Set reset-synchronized PWM mode.
(16) Enable output in MTU3 and MTU4 with TOERA.
(17) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(18) Restart operation by setting TSTRA.

(7) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Normal Mode

Figure 19.158 shows a case in which an error occurs in PWM mode 1 and operation is restarted in normal mode after re-setting.

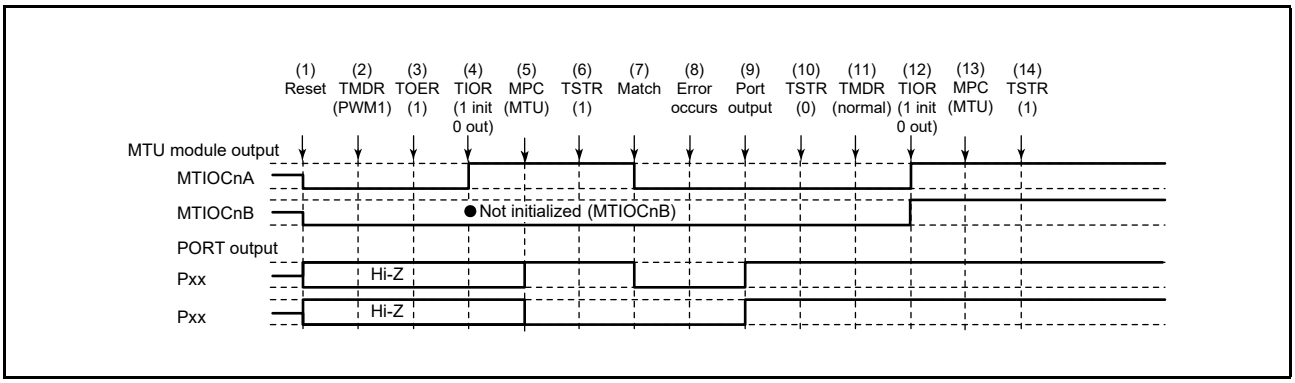


Figure 19.158 Error Occurrence in PWM Mode 1, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set PWM mode 1.
(3) For MTU3 and MTU4, enable output with TOERA before initializing the pins with TIOR.
(4) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 1, the MTIOCnB side is not initialized.)
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) Output goes low on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA.
(11) Set normal mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(8) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 1

Figure 19.159 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 1 after re-setting.

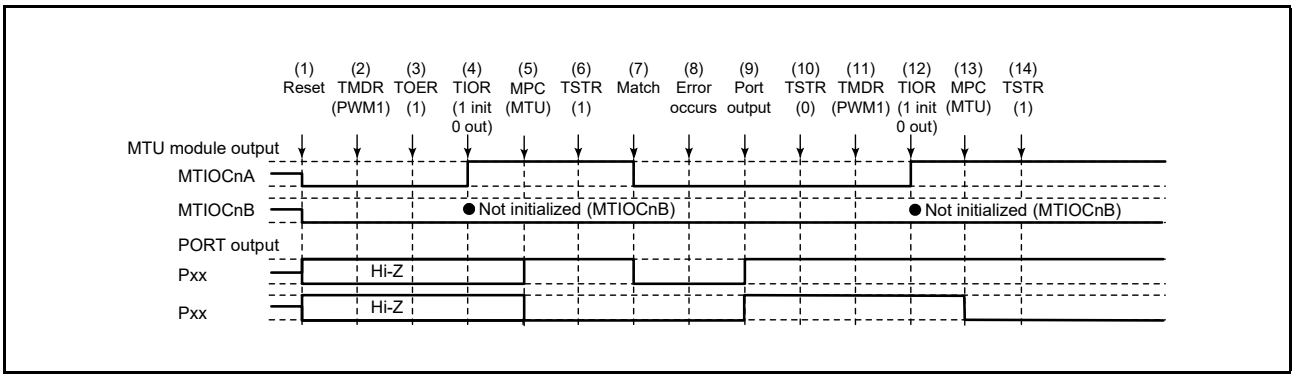


Figure 19.159 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 19.158.
(11) This step is not necessary when restarting in PWM mode 1.
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(9) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in PWM mode 2

Figure 19.160 shows a case in which an error occurs in PWM mode 1 and operation is restarted in PWM mode 2 after re-setting.

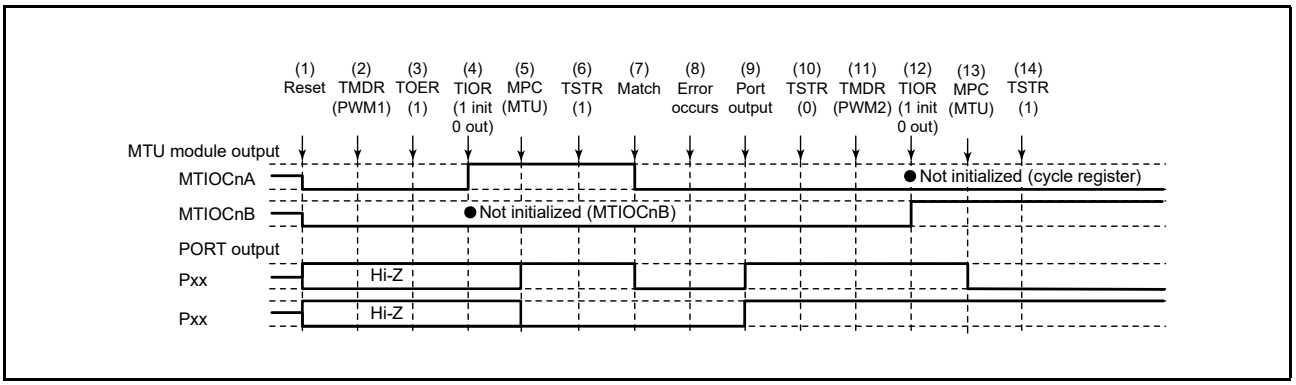


Figure 19.160 Error Occurrence in PWM Mode 1, Recovery in PWM Mode 2

(1) to (10) are the same as in Figure 19.158.
(11) Set PWM mode 2.
(12) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: PWM mode 2 can only be selected for MTU0 to MTU2, and therefore TOERA setting is not necessary.

(10) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Phase Counting Mode

Figure 19.161 shows a case in which an error occurs in PWM mode 1 and operation is restarted in phase counting mode after re-setting.

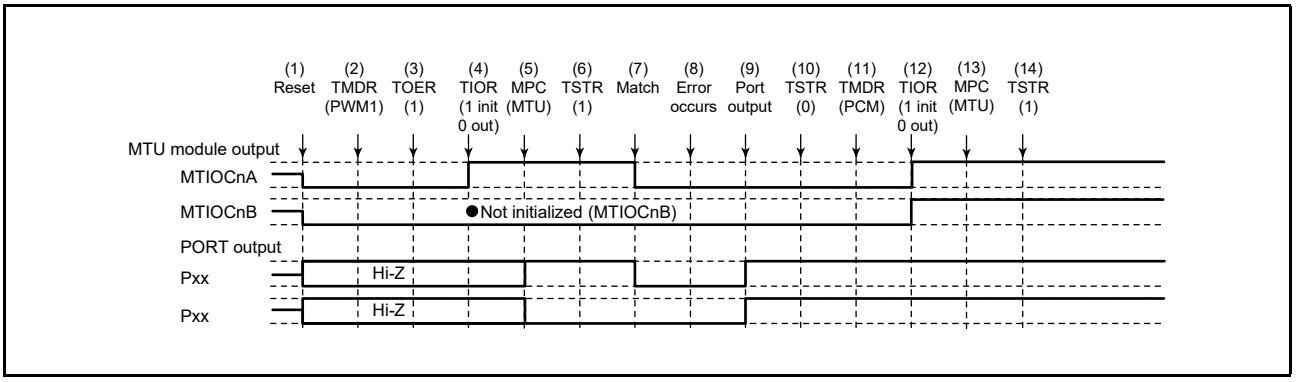


Figure 19.161 Error Occurrence in PWM Mode 1, Recovery in Phase Counting Mode

(1) to (10) are the same as in Figure 19.158.
(11) Set the phase counting mode.
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

Note: The phase counting mode can only be selected for MTU1 and MTU2, and therefore TOERA setting is not necessary.

(11) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Complementary PWM Mode

Figure 19.162 shows a case in which an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

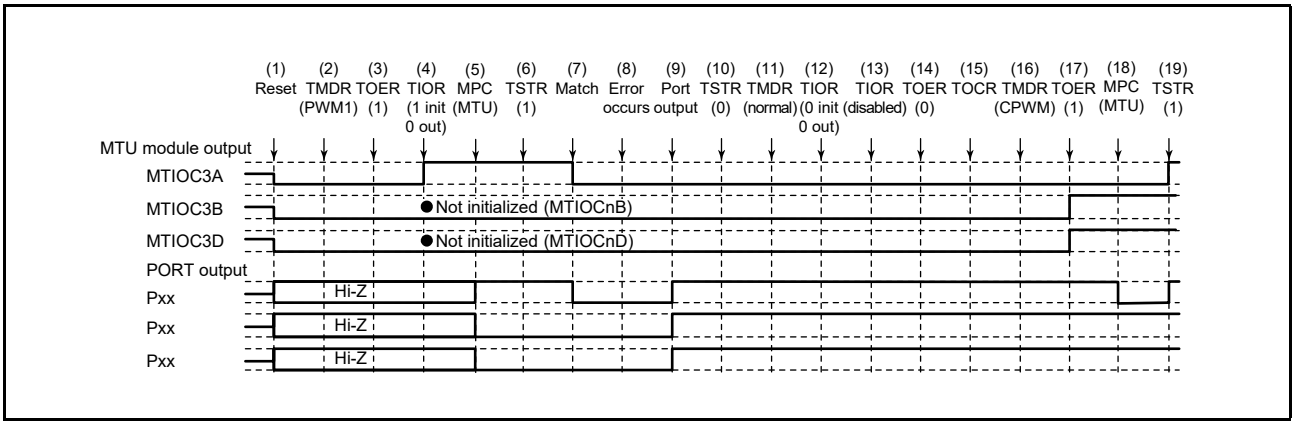


Figure 19.162 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 19.158.
(11) Set normal mode to initialize the normal mode waveform generation section.
(12) Initialize the PWM mode 1 waveform generation section with TIOR.
(13) Disable operation of the PWM mode 1 waveform generation section with TIOR
(14) Disable output in MTU3 and MTU4 with TOERA.
(15) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(16) Set complementary PWM mode.
(17) Enable output in MTU3 and MTU4 with TOERA.
(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(19) Restart operation by setting TSTRA.

(12) Operation when Error Occurs in PWM Mode 1 and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 19.163 shows a case in which an error occurs in PWM mode 1 and operation is restarted in reset-synchronized PWM mode after re-setting.

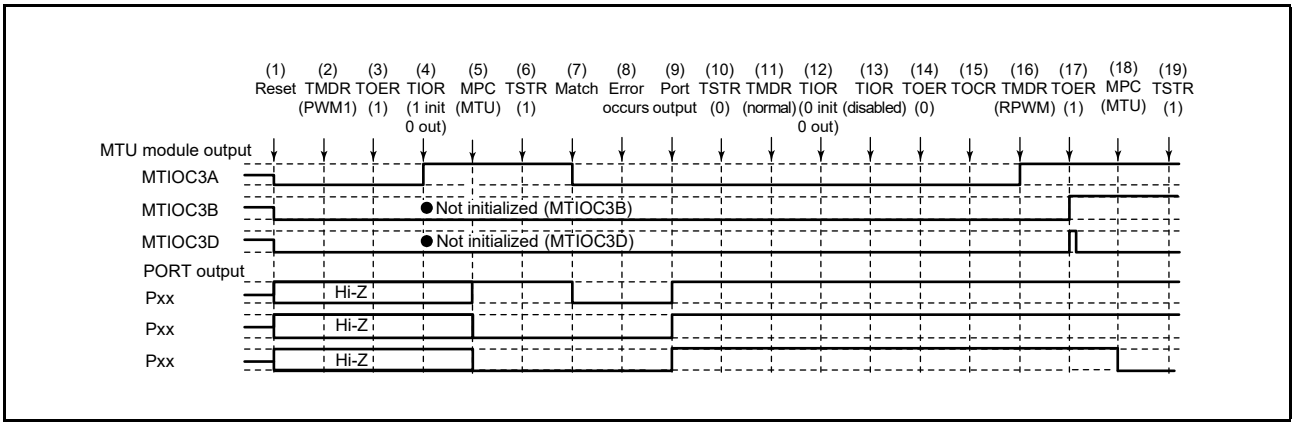


Figure 19.163 Error Occurrence in PWM Mode 1, Recovery in Reset-Synchronized PWM Mode

(1) to (14) are the same as in Figure 19.162.
(15) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(16) Set reset-synchronized PWM mode.
(17) Enable output in MTU3 and MTU4 with TOERA.
(18) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(19) Restart operation by setting TSTRA.

(13) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in Normal Mode

Figure 19.164 shows a case in which an error occurs in PWM mode 2 and operation is restarted in normal mode after re-setting.

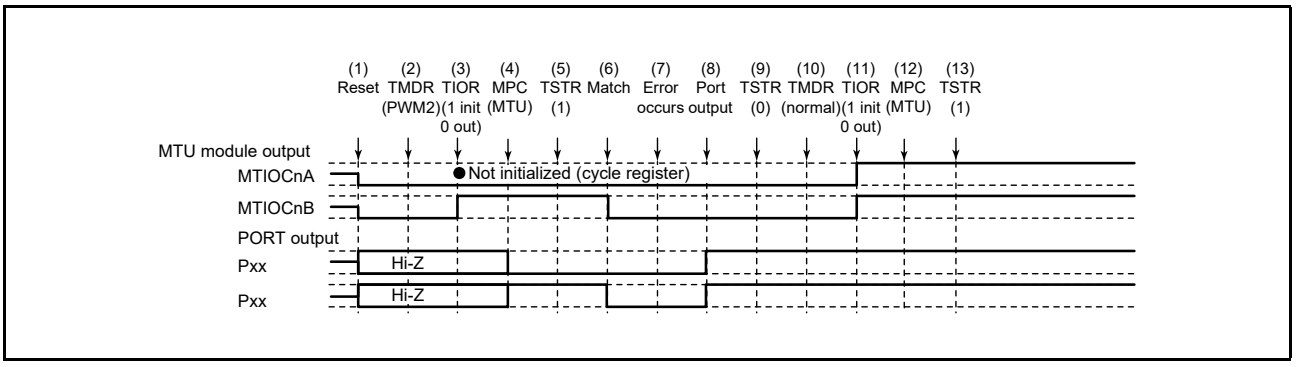


Figure 19.164 Error Occurrence in PWM Mode 2, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set PWM mode 2.
(3) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence. In PWM mode 2, the cycle register pins are not initialized. In the example, MTIOCnA is the cycle register.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting TSTRA.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting TSTRA.
(10) Set normal mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(14) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 1

Figure 19.165 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 1 after re-setting.

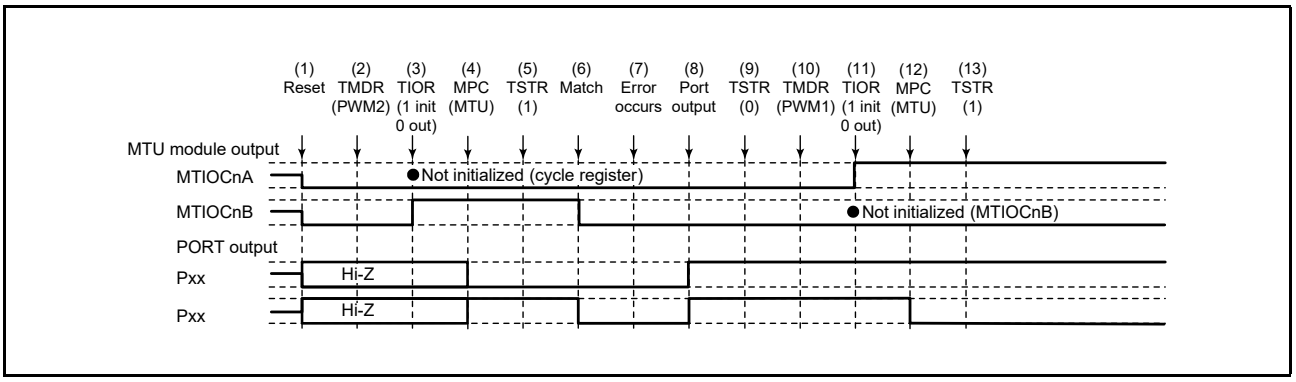


Figure 19.165 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 19.164.
(10) Set PWM mode 1.
(11) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(15) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in PWM Mode 2

Figure 19.166 shows a case in which an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

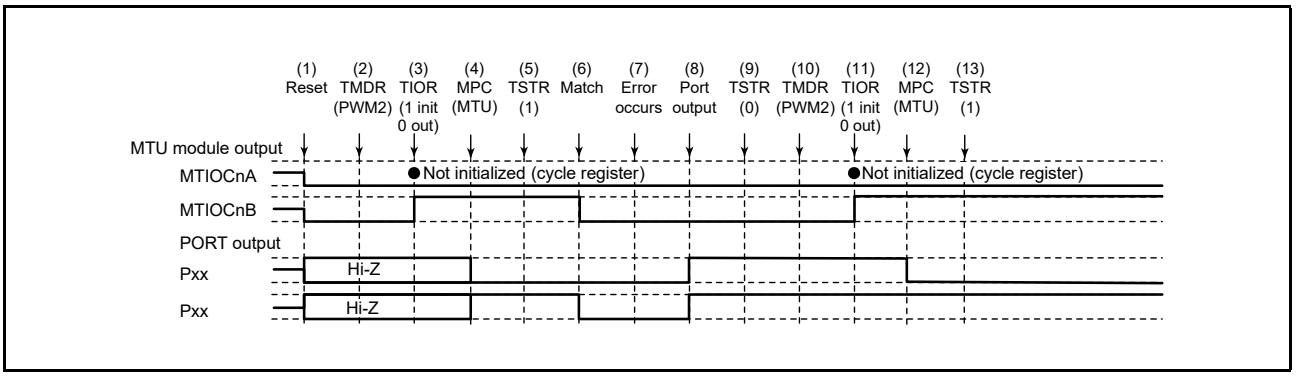


Figure 19.166 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 19.164.
(10) This step is not necessary when restarting in PWM mode 2.
(11) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(16) Operation when Error Occurs in PWM Mode 2 and Operation is Restarted in Phase Counting Mode

Figure 19.167 shows a case in which an error occurs in PWM mode 2 and operation is restarted in phase counting mode after re-setting.

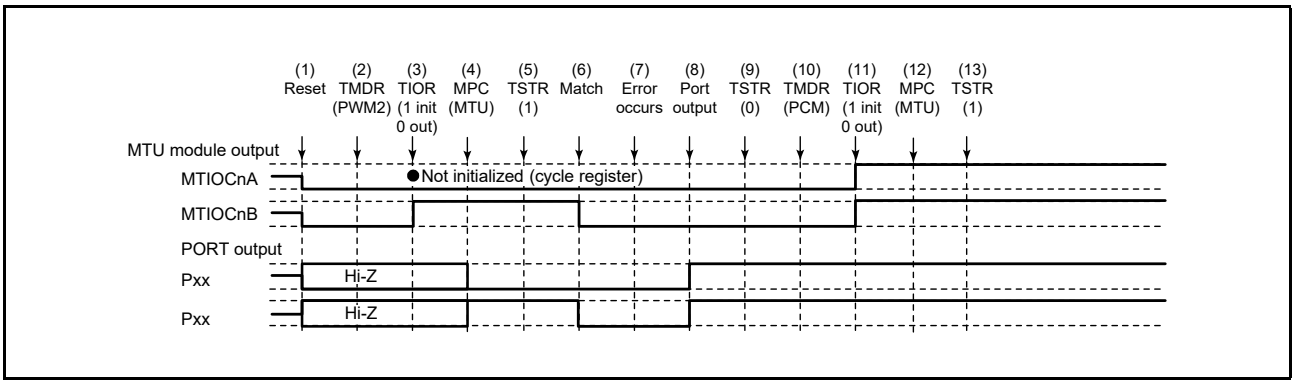


Figure 19.167 Error Occurrence in PWM Mode 2, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 19.164.
(10) Set the phase counting mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(17) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in Normal Mode

Figure 19.168 shows a case in which an error occurs in phase counting mode and operation is restarted in normal mode after re-setting.

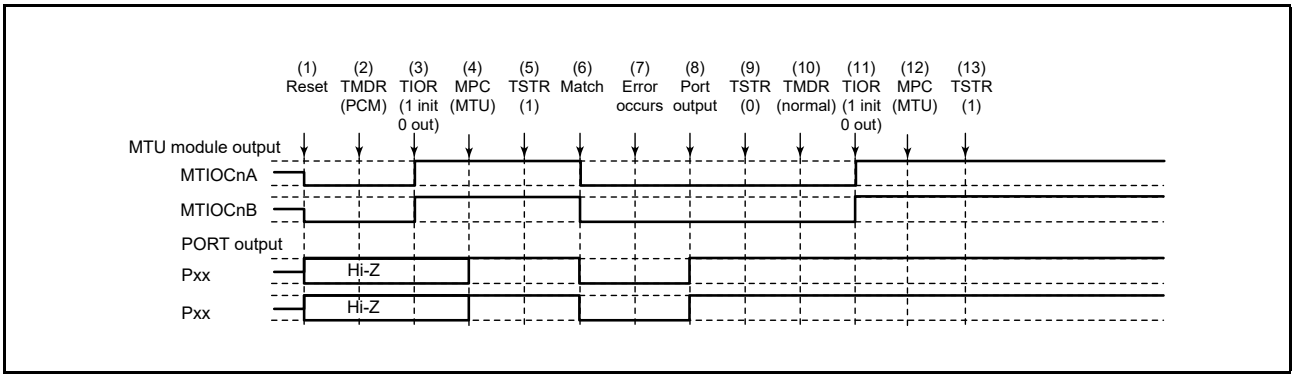


Figure 19.168 Error Occurrence in Phase Counting Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Set phase counting mode.
(3) Initialize the pins with TIOR. (In the example, the initial output is a high level, and a low level is output on compare match occurrence.)
(4) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(5) Start count operation by setting TSTRA.
(6) Output goes low on compare match occurrence.
(7) An error occurs.
(8) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(9) Stop count operation by setting TSTRA.
(10) Set normal mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(18) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 1

Figure 19.169 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 1 after re-setting.

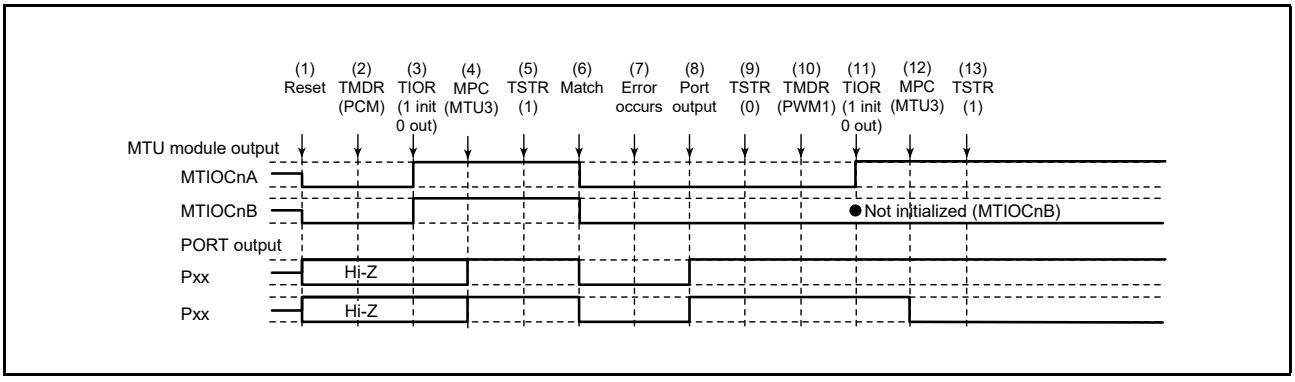


Figure 19.169 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 1

(1) to (9) are the same as in Figure 19.168.
(10) Set PWM mode 1.
(11) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(19) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in PWM Mode 2

Figure 19.170 shows a case in which an error occurs in phase counting mode and operation is restarted in PWM mode 2 after re-setting.

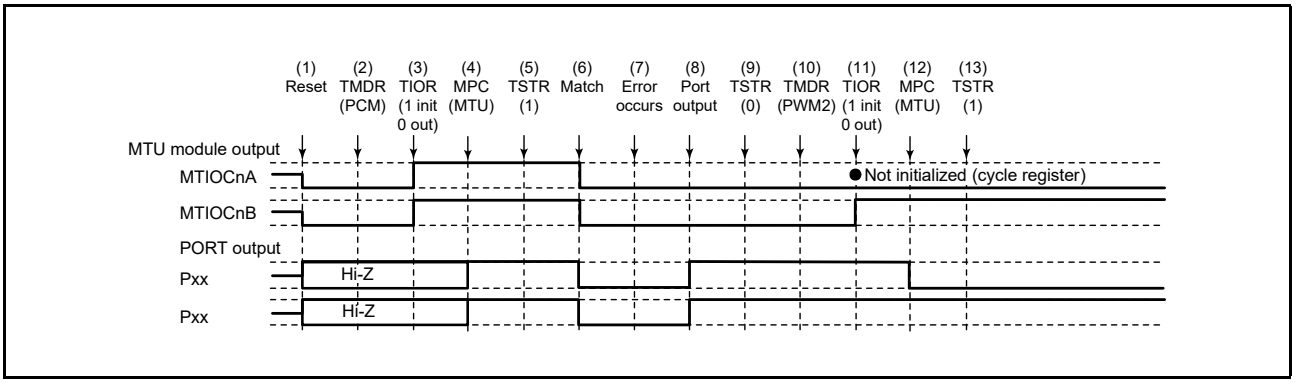


Figure 19.170 Error Occurrence in Phase Counting Mode, Recovery in PWM Mode 2

(1) to (9) are the same as in Figure 19.168.
(10) Set PWM mode 2.
(11) Initialize the pins with TIOR. (In PWM mode 2, waveforms are not output to the cycle register pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(20) Operation when Error Occurs in Phase Counting Mode and Operation is Restarted in Phase Counting Mode

Figure 19.171 shows a case in which an error occurs in phase counting mode and operation is restarted in phase counting mode after re-setting.

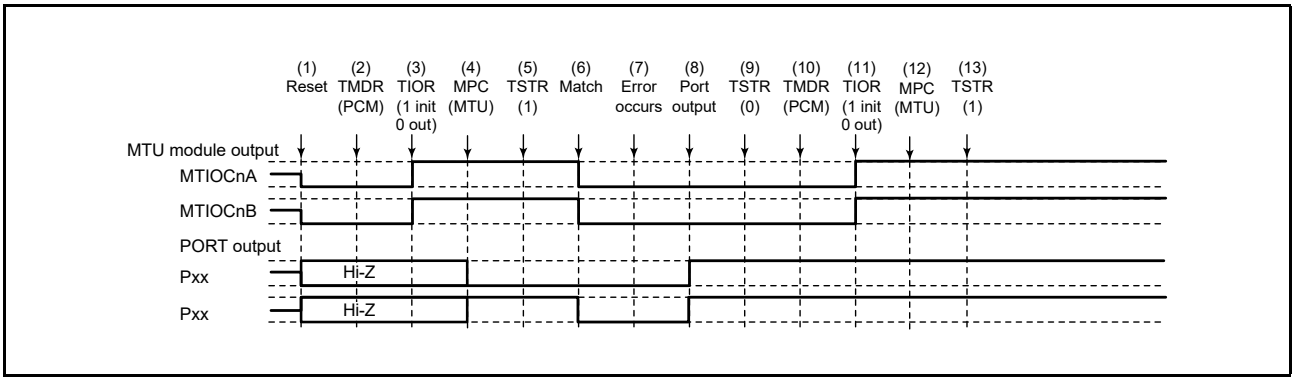


Figure 19.171 Error Occurrence in Phase Counting Mode, Recovery in Phase Counting Mode

(1) to (9) are the same as in Figure 19.168.
(10) This step is not necessary when restarting in phase counting mode.
(11) Initialize the pins with TIOR.
(12) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(13) Restart operation by setting TSTRA.

(21) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Normal Mode

Figure 19.172 shows a case in which an error occurs in complementary PWM mode and operation is restarted in normal mode after re-setting.

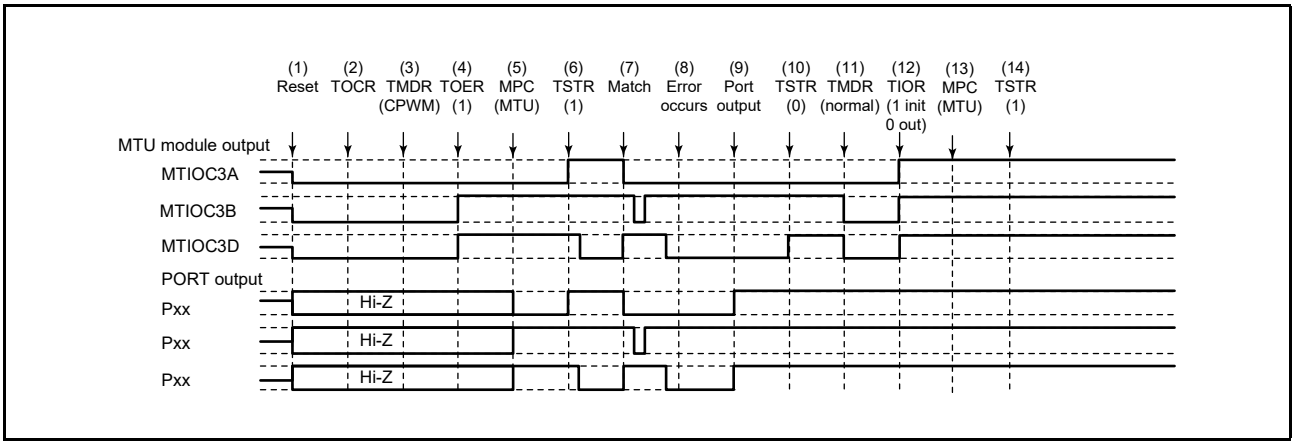


Figure 19.172 Error Occurrence in Complementary PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU3 output goes low and the ports enter high-impedance state.
(2) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(3) Set complementary PWM mode.
(4) Enable output in MTU3 and MTU4 with TOERA.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) The complementary PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA. (MTU output becomes the initial complementary PWM output value).
(11) Set normal mode (MTU output goes low).
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(22) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in PWM Mode 1

Figure 19.173 shows a case in which an error occurs in complementary PWM mode and operation is restarted in PWM mode 1 after re-setting.

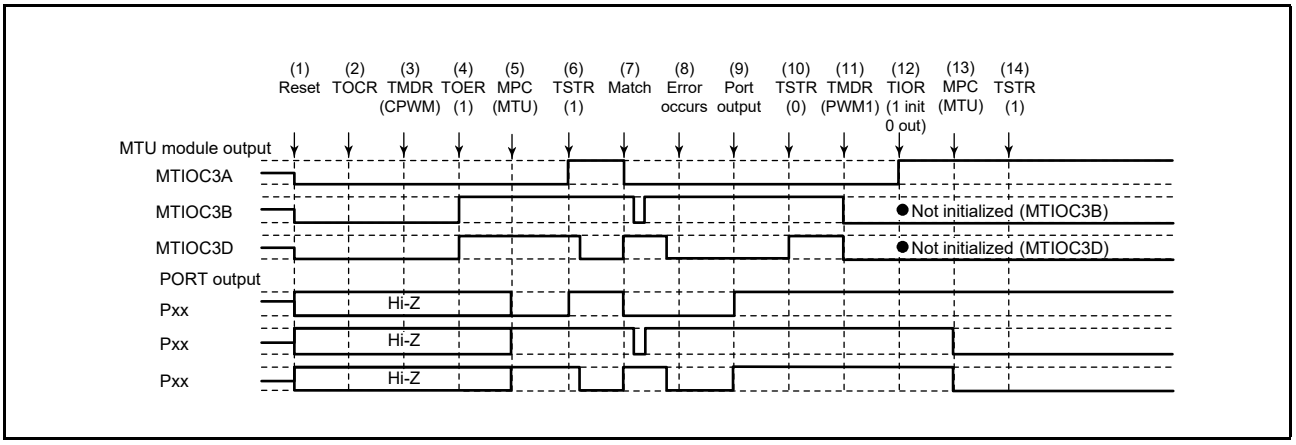


Figure 19.173 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 19.172.
(11) Set PWM mode 1 (MTU output goes low).
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(23) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 19.174 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the cycle and duty settings at the time of stopping the counter).

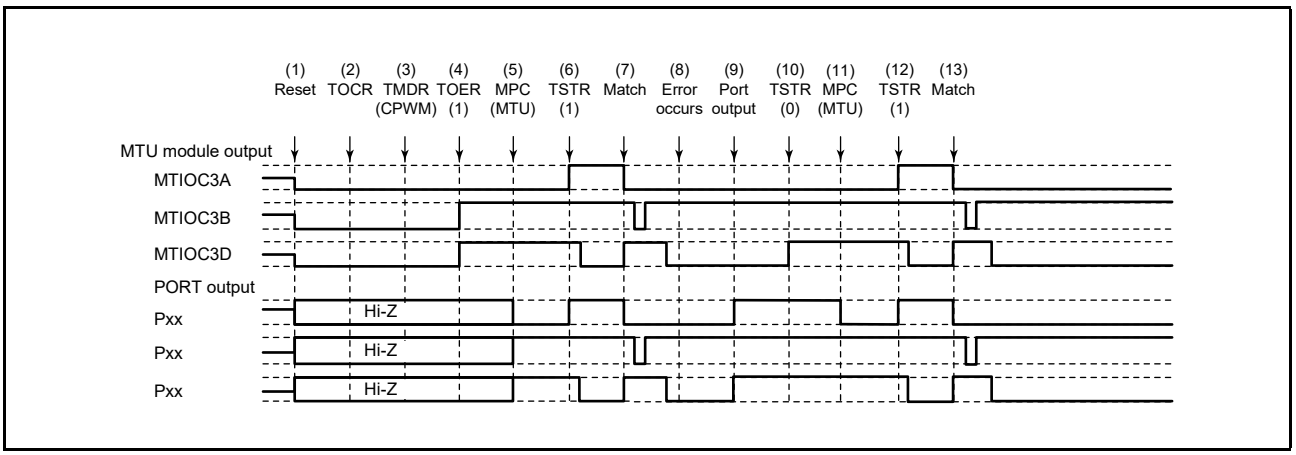


Figure 19.174 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (1)

(1) to (10) are the same as in Figure 19.172.
(11) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(12) Restart operation by setting TSTRA.
(13) The complementary PWM waveform is output on compare match occurrence.

(24) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Complementary PWM Mode with New Settings

Figure 19.175 shows a case in which an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (operation is restarted using new cycle and duty ratio settings).

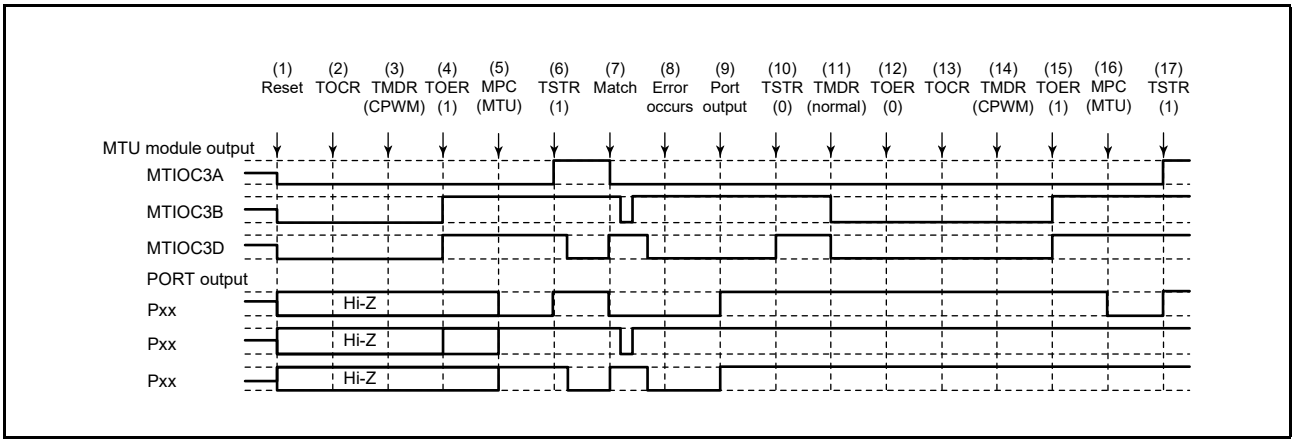


Figure 19.175 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode (2)

(1) to (10) are the same as in Figure 19.172.
(11) Set normal mode and make new settings (MTU output goes low).
(12) Disable output in MTU3 and MTU4 with TOERA.
(13) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(14) Set complementary PWM mode.
(15) Enable output in MTU3 and MTU4 with TOERA.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting TSTRA.

(25) Operation when Error Occurs in Complementary PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 19.176 shows a case in which an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

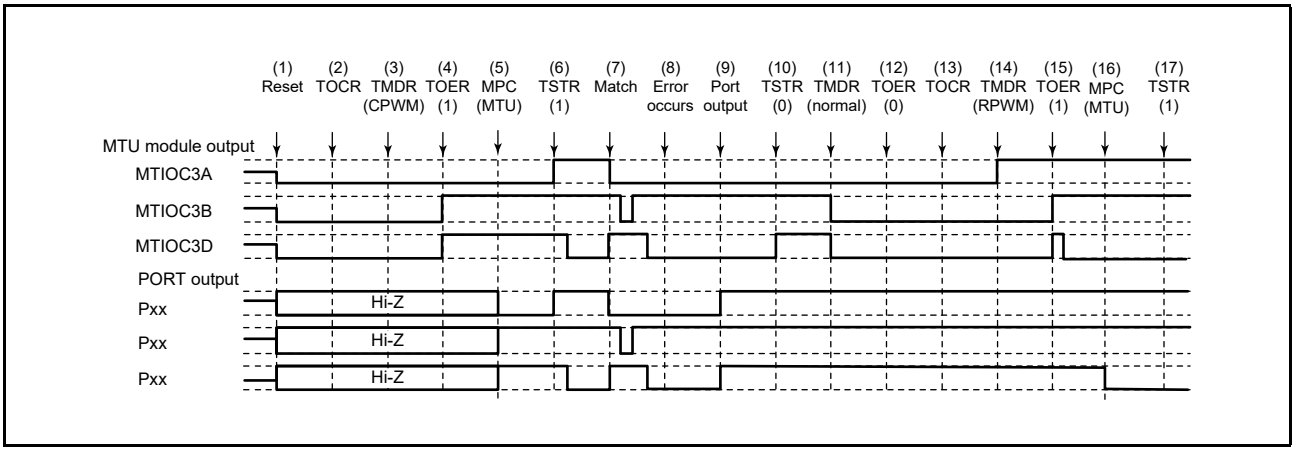


Figure 19.176 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (10) are the same as in Figure 19.172.
(11) Set normal mode (MTU output goes low).
(12) Disable output in MTU3 and MTU4 with TOERA.
(13) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(14) Set reset-synchronized PWM mode.
(15) Enable output in MTU3 and MTU4 with TOERA.
(16) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(17) Restart operation by setting TSTRA.

(26) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Normal Mode

Figure 19.177 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in normal mode after re-setting.

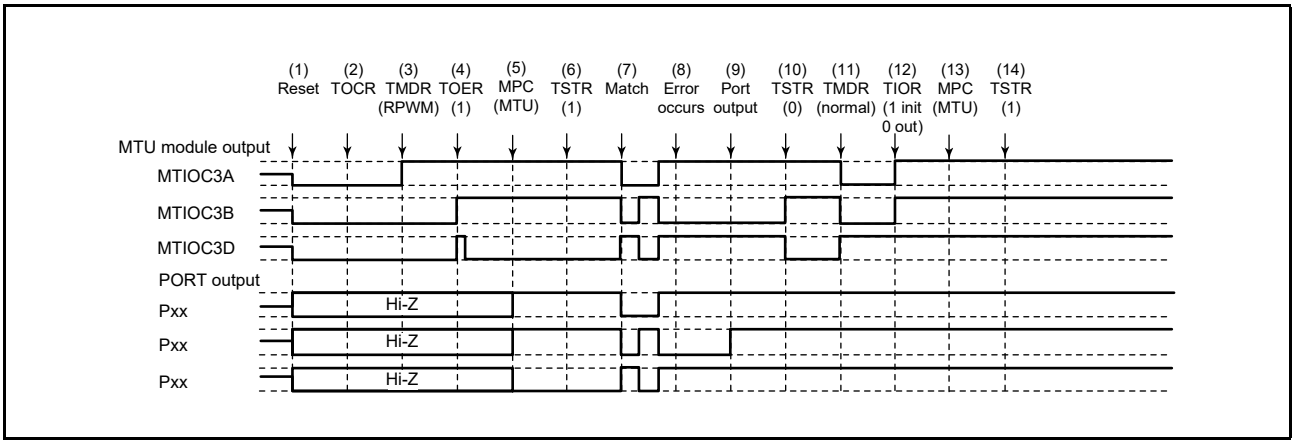


Figure 19.177 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Normal Mode

(1) After a reset, the MTU output goes low and the ports enter high-impedance state.
(2) Select the reset-synchronized PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(3) Set reset-synchronized PWM mode.
(4) Enable output in MTU3 and MTU4 with TOERA.
(5) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(6) Start count operation by setting TSTRA.
(7) The reset-synchronized PWM waveform is output on compare match occurrence.
(8) An error occurs.
(9) Allow non-active level output by setting the pins as general output ports using the port direction registers (PDR), port output data registers (PODR), and port mode registers (PMR) of the I/O ports.
(10) Stop count operation by setting TSTRA. (MTU output becomes the initial reset-synchronized PWM output value.)
(11) Set normal mode (positive-phase MTU output goes low, and negative-phase output goes high).
(12) Initialize the pins with TIOR.
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(27) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in PWM Mode 1

Figure 19.178 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

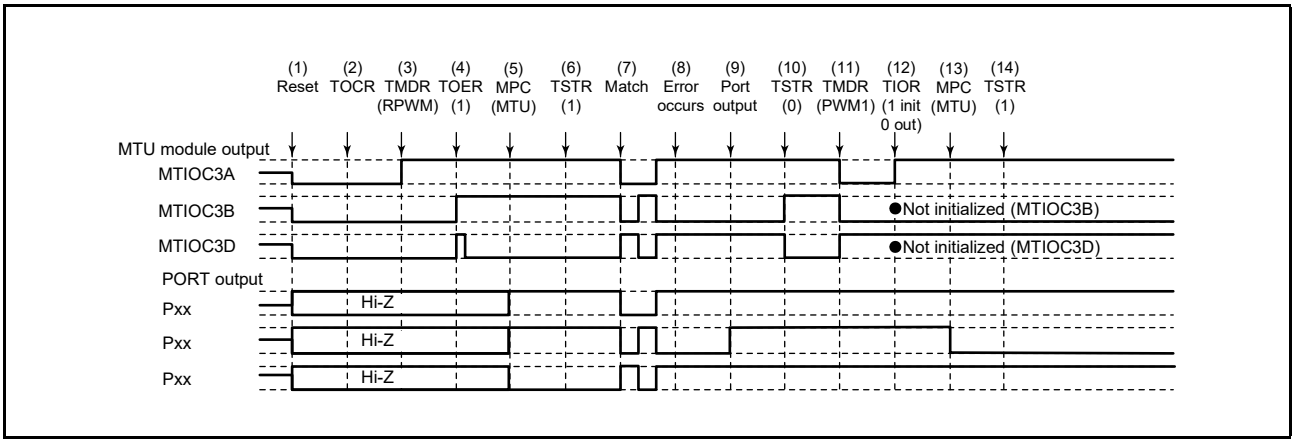


Figure 19.178 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

(1) to (10) are the same as in Figure 19.177.
(11) Set PWM mode 1 (positive-phase MTU output goes low, and negative-phase output goes high).
(12) Initialize the pins with TIOR. (In PWM mode 1, waveforms are not output to the MTIOCnB (MTIOCnD) pins. To output a specified level, make necessary settings for general output ports in the port direction registers (PDR) and port output data registers (PODR) of the I/O ports.)
(13) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(14) Restart operation by setting TSTRA.

(28) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Complementary PWM Mode

Figure 19.179 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in complementary PWM mode after re-setting.

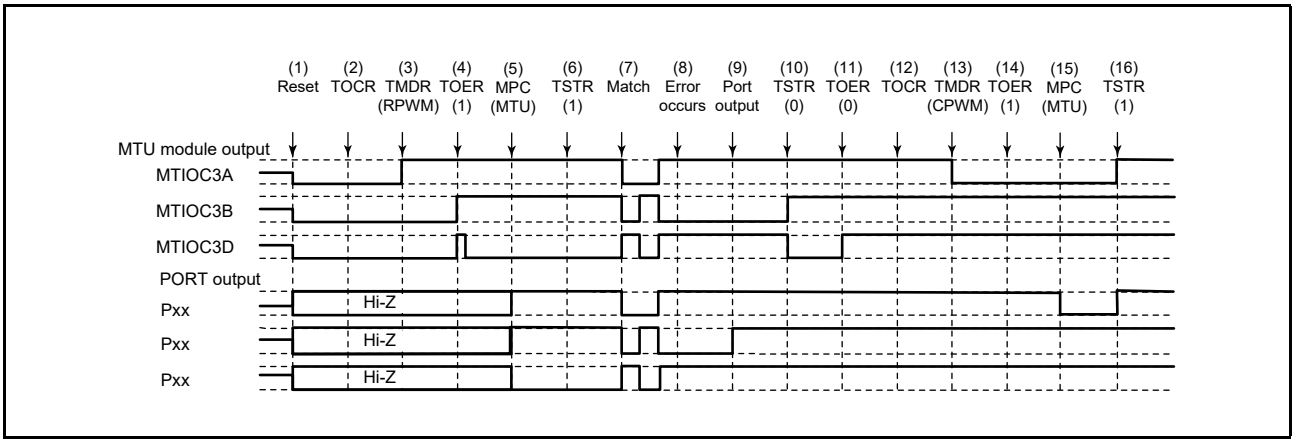


Figure 19.179 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Complementary PWM Mode

(1) to (10) are the same as in Figure 19.177.
(11) Disable output in MTU3 and MTU4 with TOERA.
(12) Select the complementary PWM output level and enable or disable cyclic output with TOCR1A and TOCR2A.
(13) Set complementary PWM mode (MTU cyclic output pin goes low).
(14) Enable output in MTU3 and MTU4 with TOERA.
(15) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(16) Restart operation by setting TSTRA.

(29) Operation when Error Occurs in Reset-Synchronized PWM Mode and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 19.180 shows a case in which an error occurs in reset-synchronized PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

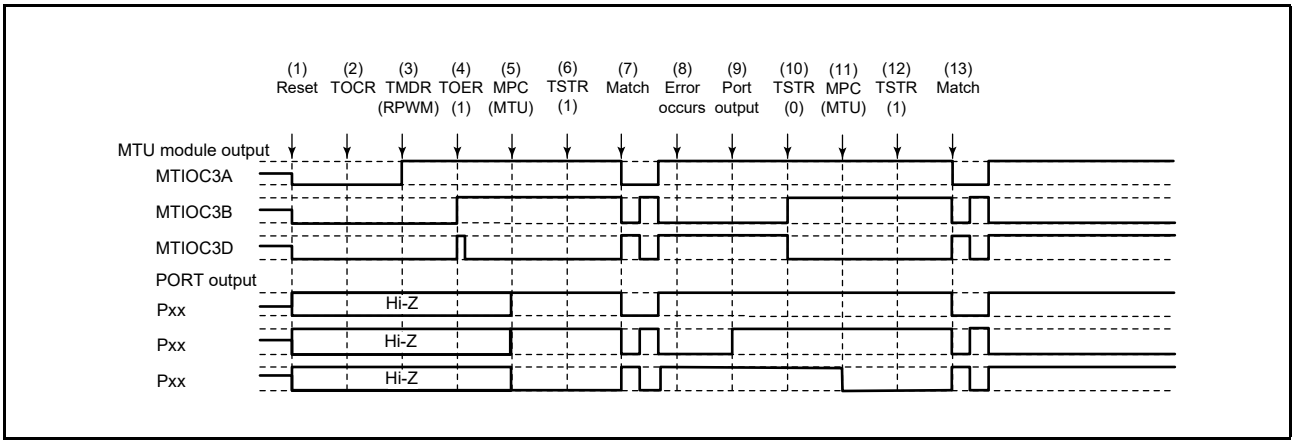


Figure 19.180 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in Reset-Synchronized PWM Mode

(1) to (10) are the same as in Figure 19.177.
(11) Set MTU output using the MPC and port mode registers (PMR) corresponding to the I/O ports.
(12) Restart operation by setting TSTRA.
(13) The reset-synchronized PWM waveform is output on compare match occurrence.

19.8 Operations Linked by the ELC

19.8.1 Event Signal Output to the ELC

The MTU is capable of operation linked with another module set in advance when its interrupt request signal is used as an event signal by the event link controller (ELC).
The MTU outputs the event signal regardless of the setting of the corresponding interrupt request enable bit.

19.8.2 MTU Operations in Response to Receiving Event Signals from the ELC

The MTU can perform the following operations in response to the event set in advance in the ELSRn register of the event link controller (ELC).

(1) Start Counting Operation

Counting by the MTU starts in response to the event when this is selected by the setting of the ELOPA or ELOPB register of the ELC. The ELOPA register handles control for MTU0 and MTU3 and the ELOPB register handles control for MTU4. When the event specified in the ELSRn register occurs, the CSTn bit in the TSTR register (timer start register) shown in Table 19.82 is set to 1, and the MTU counter starts.
However, when the specified event is generated while the CSTn bit in the TSTR register (timer start register) has already been set to 1, the event has no effect. Table 19.82 lists the TSTR register bits used for each channel.

Table 19.82 Operation of the TSTR register (timer start register) in response to the ELC

Channel No.	TSTR register (timer start register)
MTU0	TSTRA.CST0 bit
MTU3	TSTRA.CST3 bit
MTU4	TSTRA.CST4 bit

(2) Input Capture Operation

Input capture by the MTU proceeds when this is selected by the setting of the ELOPA or ELOPB register of the ELC. The ELOPA register handles control for MTU0 and MTU3 and the ELOPB register handles control for MTU4. When the event specified in the ELSRn register occurs, the TGR register (timer general register) captures the value of the TCNT register (timer counter register). When using input capture in response to an event, the corresponding bit of the TIOR register (timer I/O control register) in the MTU should be set for input capture and the CSTn bit of TSTR register (timer start register) should be set to 1 to start counting by the counter.
In this case, the TIOCnA pin (input capture pin) input has no effect.
Table 19.83 lists the timer general register and timer I/O control register used for each channel in input capture operations in response to the ELC.

Table 19.83 Timer General Register and Timer I/O Control Register Used in the Input Capture Operation

Channel No.	Timer General Register Name	Timer I/O Control Register Bit Name
MTU0	MTU0.TGRA	MTU0.TIORH.IOA[3:0] bits
MTU3	MTU3.TGRA	MTU3.TIORH.IOA[3:0] bits
MTU4	MTU4.TGRA	MTU4.TIORH.IOA[3:0] bits

(3) Clear Counting Operation

MTU counters are cleared by using the ELOPA and ELOPB registers of the ELC. The ELOPA register handles control for MTU0 and MTU3 and the ELOPB register handles control for MTU4. At this time, when the event specified in the ELSRn register occurs, the TCNT register (timer counter register) is returned to its initial value. If the corresponding CSTn bit in the TSTR register (timer start register) is set to 1, counting will continue, in other words, counting restarts. For the CSTn bits in the TSTR register (timer start register), see Table 19.83.

19.8.3 Usage Notes on MTU Operation by Event Signal Reception from ELC

The following notes on usage apply when the MTU is used in event link operation.

(1) Start Counting

If the event specified in the ELSRn register occurs during a cycle of writing to a CSTn bit in the TSTRA/TSTRB register, writing to the CSTn bit in the TSTRA/TSTRB register does not proceed because setting of the bit to 1 due to the event takes priority.

(2) Restart [Clear] Counting

If the event specified in the ELSRn register occurs during a cycle of writing to the TCNT counter, writing to the TCNT counter does not proceed because initialization of the counter's value due to the event takes priority.
In addition, for MTU3 and MTU4 in complementary PWM mode, disable the counter clearing by the ELC.

20. Port Output Enable 3 (POE3)

The port output enable 3 (POE3) register can be used to place output pins for the MTU3a and output pins for the GPT in the high-impedance state under various conditions.

20.1 Overview

Table 20.1 lists the specifications of the POE3, and Figure 20.1 shows a block diagram of the POE3.

Table 20.1 POE3 Specifications

Item	Description
Target pins to be placed in the high-impedance state	• MTU3a output pins MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) MTU3 pin (MTIOC3B, MTIOC3D) MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) MTU6 pin (MTIOC6B, MTIOC6D) MTU7 pin (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) • GPT output pins GPT0 pin (GTIOC0A, GTIOC0B) GPT1 pin (GTIOC1A, GTIOC1B) GPT2 pin (GTIOC2A, GTIOC2B) GPT3 pin (GTIOC3A, GTIOC3B)
Conditions for the high-impedance state	• Setting pins as inputs: setting the POE0#, POE4#, POE8#, or POE10# pins as inputs (falling edge or low-level sampling). • Short-circuits between output pins: A match (short circuit) between the output signal levels at the active level over one or more cycle on (the following combination of pins) **MTU complementary PWM output pins** 1 MTIOC3B and MTIOC3D 2 MTIOC4A and MTIOC4C 3 MTIOC4B and MTIOC4D 4 MTIOC6B and MTIOC6D 5 MTIOC7A and MTIOC7C 6 MTIOC7B and MTIOC7D **GPT output pins** 1 GTIOC0A and GTIOC0B 2 GTIOC1A and GTIOC1B 3 GTIOC2A and GTIOC2B • SPOER register setting being made • Detection that the clock generation circuit had stopped oscillating or the oscillation is abnormal (CLMA0/1)
Function	• Each of the POE0#, POE4#, POE8#, and POE10# input pins can be set for falling edge, PCLKD/4 × 16, PCLKD/16 × 16, or PCLKD/128 × 16 low-level sampling. • Pins for the MTU complementary PWM output, and MTU0 and GPT0 to GPT3 output pins can be placed in high-impedance state by POE0#, POE4#, POE8#, and POE10# pin falling-edge or low-level sampling. • Pins for the MTU complementary PWM output, and MTU0 and GPT0 to GPT3 output pins can be placed in high-impedance state when oscillation stoppage of the clock generation circuit or oscillation abnormality (CLMA0/1) has been detected. • Pins for the MTU complementary PWM output and GPT0 to GPT2 output pins can be placed in high-impedance state when output levels of the MTU complementary PWM output pins are compared and simultaneous active-level output continues for one cycle or more. • Pins for the MTU complementary PWM output, MTU0, and GPT0 to GPT3 output can be placed in the high-impedance state by modifying the settings of the SPOER register of POE3. • Interrupts can be generated by input-level sampling or output level comparison results.

The POE3 has input level detection circuits, pin selection circuits, output level comparison circuits, and a high-impedance request/interrupt request generating circuit as shown in Figure 20.1.

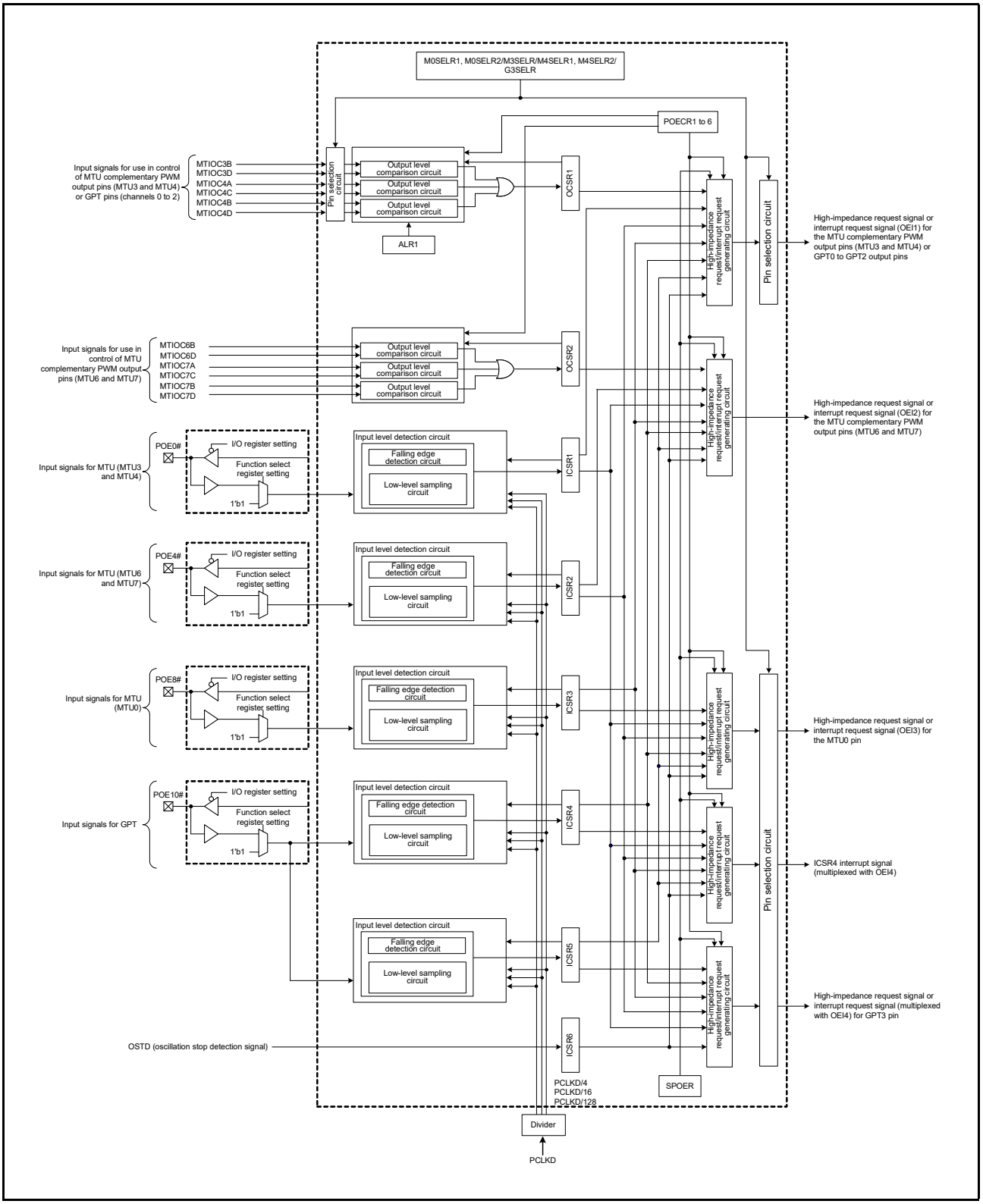


Figure 20.1 POE3 Block Diagram

Table 20.2 shows input/output pins to be used by the POE3.

Table 20.2 POE3 Input/Output Pins

Pin Name	I/O	Description
POE0#	Input	Input pin for the request signal to place the MTU3 and MTU4 pins for MTU complementary PWM output in high-impedance state. In accord with register settings, this pin is also capable of placing the MTU0, MTU6, MTU7, and GPT0 to GPT3 pins in the high-impedance state.
POE4#	Input	Input pin for the request signal to place the MTU6 and MTU7 pins for MTU complementary PWM output in high-impedance state. In accord with register settings, this pin is also capable of placing the MTU0, MTU3, MTU4, and GPT0 to GPT3 pins in the high-impedance state.
POE8#	Input	Input pin for the request signal to place the pins for MTU0 in high-impedance state. In accord with register settings, this pin is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, and GPT0 to GPT3 pins in high-impedance state.
POE10#	Input	Input pin for the request signal to place the GPT3 pins in high-impedance state. In accord with register settings, this pin is also capable of placing the MTU3 and MTU4 pins or MTU6 and MTU7 pins for MTU complementary PWM output, MTU0 pins, and GPT0 to GTP2 pins in high-impedance state.

Table 20.3 shows output level comparisons with pin combinations.

Table 20.3 Pin Combinations

Pin Combination	I/O	Description
MTIOC3B and MTIOC3D	Output	The MTU3 and MTU4 pins for MTU complementary PWM output set in the M3SELR, M4SELR1, and M4SELR2 registers are placed in high-impedance state when both pins of a pair simultaneously output the active level*1 for one or more cycles of the peripheral clock (PCLKD). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3. Note: Whether the pins selected in the M3SELR, M4SELR1, and M4SELR2 registers are MTU3a pins or GPT pins is set on the MPC. Note 1. The low level is output when the OLSP bit in TOCR1A of MTUn is 0 with the TOCS bit in TOCR1A of MTUn cleared to 0, or the high level is output when the OLSP bit is 1. Otherwise, the low level is output when the OLS3N, OLS3P, OLS2N, OLS2P, OLS1N, and OLS1P bits in TOCR2A of MTUn are 0 with the TOCS bit in TOCR1A of MTUn set to 1, or the high level is output when these bits are 1.
MTIOC4A and MTIOC4C	Output	
MTIOC4B and MTIOC4D	Output	
MTIOC6B and MTIOC6D	Output	The MTU6 and MTU7 pins for MTU complementary PWM output are placed in high-impedance state when both pins of a pair simultaneously output the active level*1 for one or more cycles of the peripheral clock (PCLKD). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3. Note 1. The low level is output when the OLSP bit in TOCR1B of MTUn is 0 with the TOCS bit in TOCR1B of MTUn cleared to 0, or the high level is output when the OLSP bit is 1. Otherwise, the low level is output when the OLS3N, OLS3P, OLS2N, OLS2P, OLS1N, and OLS1P bits in TOCR2B of MTUn are 0 with the TOCS bit in TOCR1B of MTUn set to 1, or the high level is output when these bits are 1.
MTIOC7A and MTIOC7C	Output	
MTIOC7B and MTIOC7D	Output	
GTIOC0A and GTIOC0B	Output	The GPT0 to GPT2 pins for the GPT output set in the M3SELR, M4SELR1, and M4SELR2 registers are placed in high-impedance state when all pins of a pair simultaneously output the active level (low level when the OLSG2B, OLSG2A, OLSG1B, OLSG1A, OLSG0B, and OLSG0A bits in ALR1 are 0 or high level when those bits are 1) for one or more cycles of the peripheral clock (PCLKD). Pin combinations for output comparison and high-impedance control can be selected by registers of POE3. Note: Whether the pins selected in the M3SELR, M4SELR1, and M4SELR2 registers are MTU3a pins or GPT pins is set on the MPC.
GTIOC1A and GTIOC1B	Output	
GTIOC2A and GTIOC2B	Output	

20.2 Register Descriptions

The POE3 registers are initialized by a reset.

20.2.1 Input Level Control/Status Register 1 (ICSR1)

ICSR1 selects the input modes for the POE0# pin, controls the enable/disable of interrupts, and indicates status.

Address(es): A008 0800h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE0F	—	—	—	PIE1	—	—	—	—	—	—	POE0M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE0M[1:0]	POE0 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE0# input. 0 1: Accepts a request when POE0# input has been sampled 16 times at PCLKD/4 clock pulses and all are low level. 1 0: Accepts a request when POE0# input has been sampled 16 times at PCLKD/16 clock pulses and all are low level. 1 1: Accepts a request when POE0# input has been sampled 16 times at PCLKD/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE1	Port Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE0F	POE0 Flag	0: Indicates that a high-impedance request has not been input to the POE0# pin. 1: Indicates that a high-impedance request has been input to the POE0# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

POE0M[1:0] Bits (POE0 Mode Select)

These bits select the input mode of the POE0# pin.

PIE1 Bit (Port Interrupt Enable 1)

This bit enables or disables interrupt requests when any one of the POE0F bit of the ICSR1 is set to 1.

POE0F Flag (POE0 Flag)

This flag indicates that a high-impedance request has been input to the POE0# pin.

[Setting condition]

- When the input set by POE0M[1:0] occurs at the POE0# pin

[Clearing condition]

- By writing 0 to POE0F after reading POE0F = 1

20.2.2 Input Level Control/Status Register 2 (ICSR2)

ICSR2 selects the input mode for the POE4# pin, controls the enable/disable of interrupts, and indicates status.

Address(es): A008 0804h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE4F	—	—	—	PIE2	—	—	—	—	—	—	POE4M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE4M[1:0]	POE4 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE4# input 0 1: Accepts a request when POE4# input has been sampled 16 times at PCLKD/4 clock pulses and all are low level. 1 0: Accepts a request when POE4# input has been sampled 16 times at PCLKD/16 clock pulses and all are low level. 1 1: Accepts a request when POE4# input has been sampled 16 times at PCLKD/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE2	Port Interrupt Enable 2	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE4F	POE4 Flag	0: Indicates that a high-impedance request has not been input to the POE4# pin. 1: Indicates that a high-impedance request has been input to the POE4# pin.	R/(W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

POE4M[1:0] Bits (POE4 Mode Select)

These bits select the input mode of the POE4# pin.

PIE2 Bit (Port Interrupt Enable 2)

This bit enables or disables interrupt requests when the POE4F flag in ICSR2 is set to 1.

POE4F Flag (POE4 Flag)

This flag indicates that a high-impedance request has been input to the POE4# pin.
[Setting condition]

- When the input set by POE4M[1:0] occurs at the POE4# pin

[Clearing condition]

- By writing 0 to POE4F after reading POE4F = 1

20.2.3 Input Level Control/Status Register 3 (ICSR3)

ICSR3 selects the input mode for the POE8# pin, controls the enable/disable of interrupts, and indicates status.

Address(es): A008 0808h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE8F	—	—	POE8E	PIE3	—	—	—	—	—	—	POE8M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE8M[1:0]	POE8 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE8# input 0 1: Accepts a request when POE8# input has been sampled 16 times at PCLKD/4 clock pulses and all are low level. 1 0: Accepts a request when POE8# input has been sampled 16 times at PCLKD/16 clock pulses and all are low level. 1 1: Accepts a request when POE8# input has been sampled 16 times at PCLKD/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE3	Port Interrupt Enable 3	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE8E	POE8 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE8F	POE8 Flag	0: Indicates that a high-impedance request has not been input to the POE8# pin. 1: Indicates that a high-impedance request has been input to the POE8# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

POE8M[1:0] Bits (POE8 Mode Select)

These bits select the input mode of the POE8# pin.

PIE3 Bit (Port Interrupt Enable 3)

This bit enables or disables interrupt requests when the POE8F bit in ICSR3 is set to 1.

POE8E Bit (POE8 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE8F bit is set to 1.

POE8F Flag (POE8 Flag)

This flag indicates that a high-impedance request has been input to the POE8# pin.

[Setting condition]

- When the input set by POE8M[1:0] occurs at the POE8# pin

[Clearing condition]

- By writing 0 to POE8F after reading POE8F = 1

20.2.4 Input Level Control/Status Register 4 (ICSR4)

ICSR4 selects the POE10# pin input mode, controls the enable/disable of interrupts, and indicates status.

Address(es): A008 0816h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE10F	—	—	POE10E	PIE4	—	—	—	—	—	—	POE10M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE10M[1:0]	POE10 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE10# input 0 1: Accepts a request when POE10# input has been sampled 16 times at PCLKD/4 clock pulses and all are low level. 1 0: Accepts a request when POE10# input has been sampled 16 times at PCLKD/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# input has been sampled 16 times at PCLKD/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE4	Port Interrupt Enable 4	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE10E	POE10 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE10F	POE10 Flag	0: Indicates that a high-impedance request has not been input to the POE10# pin. 1: Indicates that a high-impedance request has been input to the POE10# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

POE10M[1:0] Bits (POE10 Mode Select)

These bits select the input mode of the POE10# pin.

PIE4 Bit (Port Interrupt Enable 4)

This bit enables or disables interrupt requests when the POE10F bit is set to 1.

POE10E Bit (POE10 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE10F bit is set to 1.

POE10F Bit (POE10 Flag)

This flag indicates that a request for the high-impedance state has been input to the POE10# pin.
[Setting condition]

- When the input set by POE10M[1:0] occurs at the POE10# pin

[Clearing condition]

- By writing 0 to POE10F after reading POE10F = 1

20.2.5 Input Level Control/Status Register 5 (ICSR5)

ICSR5 selects the POE10# pin input mode, controls the enable/disable of interrupts, and indicates status.

Address(es): A008 0818h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	POE10F	—	—	POE10E	PIE5	—	—	—	—	—	—	POE10M[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: For the ICSR5 register, set the values same as those in the ICSR4 register.

Bit	Symbol	Bit Name	Description	R/W
b1, b0	POE10M[1:0]	POE10 Mode Select	b1 b0 0 0: Accepts a request on the falling edge of POE10# input 0 1: Accepts a request when POE10# input has been sampled 16 times at PCLKD/4 clock pulses and all are low level. 1 0: Accepts a request when POE10# input has been sampled 16 times at PCLKD/16 clock pulses and all are low level. 1 1: Accepts a request when POE10# input has been sampled 16 times at PCLKD/128 clock pulses and all are low level.	R/W*1
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PIE5	Port Interrupt Enable 5	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	POE10E	POE10 High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	POE10F	POE10 Flag	0: Indicates that a high-impedance request has not been input to the POE10# pin. 1: Indicates that a high-impedance request has been input to the POE10# pin.	R/(W)*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

POE10M[1:0] Bits (POE10 Mode Select)

These bits select the input mode of the POE10# pin.

PIE5 Bit (Port Interrupt Enable 5)

This bit enables or disables interrupt requests when the POE10F bit is set to 1.

POE10E Bit (POE10 High-Impedance Enable)

This bit specifies whether to place the corresponding pin in high-impedance state when the POE10F bit is set to 1.
The interrupt output is multiplexed with OEI4.

POE10F Flag (POE10 Flag)

This flag indicates that a request for the high-impedance state has been input to the POE10# pin.
[Setting condition]

- When the input set by POE10M[1:0] occurs at the POE10# pin

[Clearing condition]

- By writing 0 to POE10F after reading POE10F = 1

20.2.6 Input Level Control/Status Register 6 (ICSR6)

ICSR6 controls the high-impedance for stopped oscillation or oscillation abnormality (CLMA0/1), and indicates status.

Address(es): A008 081Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OSTSTF	—	—	OSTSTE	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	OSTSTE	OSTST High-Impedance Enable	0: Does not place the MTU complementary PWM output pins, MTU0 pins, or GPT pins in high-impedance state. 1: Places the MTU complementary PWM output pins, MTU0 pins, and GPT pins in high-impedance state.	R/W*1
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	OSTSTF	OSTST High-Impedance Flag	0: Indicates that a high-impedance request due to stopped oscillation or oscillation abnormality (CLMA0/1) has not been generated. 1: Indicates that a high-impedance request due to stopped oscillation or oscillation abnormality (CLMA0/1) has been generated.	R/W*2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

OSTSTE Bit (OSTST High-Impedance Enable)

This bit enables/disables the MTU complementary PWM output pins, MTU0 pins, and GPT0 to GPT3 pins to be placed in the high-impedance state when stopped oscillation or oscillation abnormality of the PLL (CLMA0/1) is detected.

OSTSTF Flag (OSTST High-Impedance Enable Flag)

This flag indicates that a stopped oscillation high-impedance request has been generated.
When stopped oscillation is detected, this flag is set to 1. When clearing this flag, write 0 while the detection signal for stopped oscillation or oscillation abnormality of the PLL is negated. Writing 0 to this flag while the detection signal for stopped oscillation or oscillation abnormality is asserted does not clear this flag to 0. After clearing this flag, confirm that the flag has actually been modified to 0.
[Setting condition]

- When stopped oscillation is detected

[Clearing condition]

- By writing 0 to OSTSTF after reading OSTSTF = 1

20.2.7 Output Level Control/Status Register 1 (OCSR1)

OCSR1 controls the enable/disable of output level comparison and interrupts, and indicates status.

Address(es): A008 0802h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF1	—	—	—	—	—	OCE1	OIE1	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OIE1	Output Short Interrupt Enable 1	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	OCE1	Output Short High-Impedance Enable 1	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	OSF1	Output Short Flag 1	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W) *2

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

OIE1 Bit (Output Short Interrupt Enable 1)

This bit enables or disables interrupt requests when the OSF1 bit in OCSR1 is set to 1.

OCE1 Bit (Output Short High-Impedance Enable 1)

This bit specifies whether to place the pins in high-impedance state when the OSF1 bit in OCSR1 is set to 1.

OSF1 Flag (Output Short Flag 1)

This flag indicates that any one of the three pairs of two-phase MTU3 and MTU4 pins for MTU complementary PWM output or GPT0 to GPT2 pins for the GPT output to be compared has simultaneously become an active level.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

[Clearing condition]

- By writing 0 to OSF1 after reading OSF1 = 1

20.2.8 Output Level Control/Status Register 2 (OCSR2)

OCSR2 controls the enable/disable of output level comparison and interrupts, and indicates status.

Address(es): A008 0806h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OSF2	—	—	—	—	—	OCE2	OIE2	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OIE2	Output Short Interrupt Enable 2	0: Interrupt requests disabled 1: Interrupt requests enabled	R/W
b9	OCE2	Output Short High-Impedance Enable 2	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	OSF2	Output Short Flag 2	0: Indicates that outputs have not simultaneously become an active level. 1: Indicates that outputs have simultaneously become an active level.	R/(W) *2

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.
Note 2. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

OIE2 Bit (Output Short Interrupt Enable 2)

This bit enables or disables interrupt requests when the OSF2 bit in OCSR2 is set to 1.

OCE2 Bit (Output Short High-Impedance Enable 2)

This bit specifies whether to place the pins in high-impedance state when the OSF2 bit in OCSR2 is set to 1.

OSF2 Flag (Output Short Flag 2)

This flag indicates that any one of the three pairs of two-phase MTU6 and MTU7 pins for MTU complementary PWM output to be compared has simultaneously become an active level.

[Setting condition]

- When any one of the three pairs of two-phase outputs has simultaneously become an active level

[Clearing condition]

- By writing 0 to OSF2 after reading OSF2 = 1

20.2.9 Active Level Setting Register 1 (ALR1)

ALR1 specifies the active levels of the MTU and GPT outputs selected by the MPC (multi-function pin controller), as the active levels for detection of short circuits of those outputs as reflected in OCSR1.)

Address(es): A008 081Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OLSEN	—	OLSG2B	OLSG2A	OLSG1B	OLSG1A	OLSG0B	OLSG0A
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OLSG0A	MTIOC3B/GTIOC0A Active Level Setting	0: Active low 1: Active high	R/W*1
b1	OLSG0B	MTIOC3D/GTIOC0B Active Level Setting	0: Active low 1: Active high	R/W*1
b2	OLSG1A	MTIOC4A/GTIOC1A Active Level Setting	0: Active low 1: Active high	R/W*1
b3	OLSG1B	MTIOC4C/GTIOC1B Active Level Setting	0: Active low 1: Active high	R/W*1
b4	OLSG2A	MTIOC4B/GTIOC2A Active Level Setting	0: Active low 1: Active high	R/W*1
b5	OLSG2B	MTIOC4D/GTIOC2B Active Level Setting	0: Active low 1: Active high	R/W*1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	OLSEN	Active Level Setting Enable	0: Disabled 1: Enabled	R/W*1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

OLSG0A bit (MTIOC3B/GTIOC0A Active Level Setting)

This bit sets the active level of the MTIOC3B/GTIOC0A output. Specifically, setting the OLSG0A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG0B bit (MTIOC3D/GTIOC0B Active Level Setting)

This bit sets the active level of the MTIOC3D/GTIOC0B output. Specifically, setting the OLSG0B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG1A bit (MTIOC4A/GTIOC1A Active Level Setting)

This bit sets the active level of the MTIOC4A/GTIOC1A output. Specifically, setting the OLSG1A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG1B bit (MTIOC4C/GTIOC1B Active Level Setting)

This bit sets the active level of the MTIOC4C/GTIOC1B output. Specifically, setting the OLSG1B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG2A bit (MTIOC4B/GTIOC2A Active Level Setting)

This bit sets the active level of the MTIOC4B/GTIOC2A output. Specifically, setting the OLSG2A bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSG2B bit (MTIOC4D/GTIOC2B Active Level Setting)

This bit sets the active level of the MTIOC4D/GTIOC2B output. Specifically, setting the OLSG2B bit to 0 sets the low level and to 1 sets the high level as the active level for detection of short circuits.

OLSEN bit (Active Level Setting)

This bit selects enabling or disabling of the active-level settings in the OLSGnm bits (n = 0 to 2, m = A, B). Clearing the OLSEN bit to 0 disables the OLSGnm bits, in which case the active levels of the MTU output are determined by the MTU.TOCR1A and MTU.TOCR2A registers. Setting the OLSEN bit to 1 enables the OLSGnm bits, in which case the active levels of the MTU output are as selected by the OLSGnm bits in this register.

Active levels for the GPT output can only be set when the OLSEN bit is 1. When output short-circuit detection is to be used on the GPT outputs, set the OLSEN bit to 1 and then use the OLSGnm bits to set the active levels for the GPT outputs.

20.2.10 Software Port Output Enable Register (SPOER)

SPOER controls high-impedance state of the pins.

Address(es): A008 080Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	GPT3HIZ	—	MTUCH0HIZ	MTUCH67HIZ	MTUCH34HIZ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTUCH34HIZ	MTU3, MTU4, GPT0, GPT1, or GPT2 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b1	MTUCH67HIZ	MTU6 and MTU7 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b2	MTUCH0HIZ	MTU0 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	GPT3HIZ	GPT3 Output High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

MTUCH34HIZ Bit (MTU3, MTU4, GPT0, GPT1, or GPT2 Output High-Impedance Enable)

This bit specifies whether to place the MTU complementary PWM output pins (MTIOC3B, MTIOC3D, MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D, or the GPT output pins (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, GTIOC2B)) in high-impedance state.

[Setting condition]

- By writing 1 to MTUCH34HIZ

[Clearing conditions]

- Reset
- By writing 0 to MTUCH34HIZ after reading MTUCH34HIZ = 1*1

Note 1. To write 0 to this bit, be sure to read 1 and then write 0.

MTUCH67HIZ Bit (MTU6 and MTU7 Output High-Impedance Enable)

This bit specifies whether to place the MTU complementary PWM output pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, and MTIOC7D) in high-impedance state.

[Setting condition]

- By writing 1 to MTUCH67HIZ

[Clearing conditions]

- Reset
- By writing 0 to MTUCH67HIZ after reading MTUCH67HIZ = 1*1

Note 1. To write 0 to this bit, be sure to read 1 and then write 0.

MTUCH0HIZ Bit (MTU0 Output High-Impedance Enable)

This bit specifies whether to place the MTU0 pins in high-impedance state.

[Setting condition]

- By writing 1 to MTUCH0HIZ

[Clearing conditions]

- Reset
- By writing 0 to MTUCH0HIZ after reading MTUCH0HIZ = 1*1

Note 1. To write 0 to this bit, be sure to read 1 and then write 0.

GPT3HIZ Bit (GPT3 Output High-Impedance Enable)

This bit specifies whether to place the GPT3 pins (GTIOC3A, GTIOC3B) in high-impedance state.

[Setting condition]

- By writing 1 to GPT3HIZ

[Clearing conditions]

- Reset
- By writing 0 to GPT3HIZ after reading GPT3HIZ = 1*1

Note 1. To write 0 to this bit, be sure to read 1 and then write 0.

20.2.11 Port Output Enable Control Register 1 (POECR1)

POECR1 controls high-impedance state of the MTU0 pins.

Address(es): A008 080Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MTU0DZE	MTU0CZE	MTU0BZE	MTU0AZE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MTU0AZE	MTIOC0A High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b1	MTU0BZE	MTIOC0B High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b2	MTU0CZE	MTIOC0C High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b3	MTU0DZE	MTIOC0D High-Impedance Enable	0: Does not place the pin in high-impedance state. 1: Places the pin in high-impedance state.	R/W*1
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

MTU0AZE Bit (MTIOC0A High-Impedance Enable)

This bit specifies whether to place the MTIOC0A output for the MTU0 pin in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR5, the POEmF (n = 1, 2, 4, 5; m = 0, 4, 10) flag in ICSRn, is set to 1.

MTU0BZE Bit (MTIOC0B High-Impedance Enable)

This bit specifies whether to place the MTIOC0B output for the MTU0 pin in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR5, the POEmF (n = 1, 2, 4, 5; m = 0, 4, 10) flag in ICSRn, is set to 1.

MTU0CZE Bit (MTIOC0C High-Impedance Enable)

This bit specifies whether to place the MTIOC0C output for the MTU0 pin in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR5, the POEmF (n = 1, 2, 4, 5; m = 0, 4, 10) flag in ICSRn, is set to 1.

MTU0DZE Bit (MTIOC0D High-Impedance Enable)

This bit specifies whether to place the MTIOC0D output for the MTU0 pin in high-impedance state when any of the POE8F flag in ICSR3, MTUCH0HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR5, the POEmF (n = 1, 2, 4, 5; m = 0, 4, 10) flag in ICSRn, is set to 1.

20.2.12 Port Output Enable Control Register 2 (POECR2)

POECR2 controls high-impedance state of the MTU complementary PWM output pins (MTU3, MTU4, MTU6, and MTU7 pins and the GPT pins (GPT0 to GPT2)).

Address(es): A008 080Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MTU3BDZE	MTU4ACZE	MTU4BDZE	—	—	—	—	—	MTU6BDZE	MTU7ACZE	MTU7BDZE
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	MTU7BDZE	MTIOC7B/7D High-Impedance Enable*2	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b1	MTU7ACZE	MTIOC7A/7C High-Impedance Enable*2	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b2	MTU6BDZE	MTIOC6B/6D High-Impedance Enable*2	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MTU4BDZE	MTIOC4B/4D and GTIOC2A/2B High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b9	MTU4ACZE	MTIOC4A/4C and GTIOC1A/1B High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b10	MTU3BDZE	MTIOC3B/3D and GTIOC0A/0B High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.
Note 2. Set this bit to 0 when MTU6 or MTU7 is not used.

MTU7BDZE Bit (MTIOC7B/7D High-Impedance Enable)

This bit specifies whether to place the MTIOC7B output and MTIOC7D output for the MTU3 pin in high-impedance state when any one of the OSF2 flag in OCSR2, POE4F flag in ICSR2, MTUCH67HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 1, 3 to 5; m = 0, 8, 10) flag in ICSRn, is set to 1.

MTU7ACZE Bit (MTIOC7A/7C High-Impedance Enable)

This bit specifies whether to place the MTIOC7A output and MTIOC7C output for the MTU3 pin in high-impedance state when any one of the OSF2 flag in OCSR2, POE4F flag in ICSR2, MTUCH67HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 1, 3 to 5; m = 0, 8, 10) flag in ICSRn, is set to 1.

MTU6BDZE Bit (MTIOC6B/6D High-Impedance Enable)

This bit specifies whether to place the MTIOC6B output and MTIOC6D output for the MTU3 pin in high-impedance state when any one of the OSF2 flag in OCSR2, POE4F flag in ICSR2, MTUCH67HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 1, 3 to 5; m = 0, 8, 10) flag in ICSRn, is set to 1.

MTU4BDZE Bit (MTIOC4B/4D and GTIOC2A/2B High-Impedance Enable)

This bit specifies whether to place the MTIOC4B output and MTIOC4D output for the MTU4 pin and the GTIOC2A output and GTIOC2B output for the GPT2 pin in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 2 to 5; m = 4, 8, 10) flag in ICSRn, is set to 1.

MTU4ACZE Bit (MTIOC4A/4C and GTIOC1A/1B High-Impedance Enable)

This bit specifies whether to place the MTIOC4A output and MTIOC4C output for the MTU4 pin and the GTIOC1A output and GTIOC1B output for the GPT1 pin in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 2 to 5; m = 4, 8, 10) flag in ICSRn, is set to 1.

MTU3BDZE Bit (MTIOC3B/3D and GTIOC0A/0B High-Impedance Enable)

This bit specifies whether to place the MTIOC3B output and MTIOC3D output for the MTU3 pin and the GTIOC0A output and GTIOC0B output for the GPT0 pin in high-impedance state when any one of the OSF1 flag in OCSR1, POE0F flag in ICSR1, MTUCH34HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR4, the POEmF (n = 2 to 5; m = 4, 8, 10) flag in ICSRn, is set to 1.

20.2.13 Port Output Enable Control Register 3 (POECR3)

POECR3 controls high-impedance state of the GPT pin (GPT3).

Address(es): A008 080Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	GPT3ABZE	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	GPT3ABZE	GTIOC3A/3B High-Impedance Enable	0: Does not place the pins in high-impedance state. 1: Places the pins in high-impedance state.	R/W*1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

GPT3ABZE Bit (GTIOC3A/3B High-Impedance Enable)

This bit specifies whether to place the GTIOC3A and GTIOC3B outputs for the GPT3 pin when any one of the POE10F flag in ICSR5, GPT3HIZ bit in SPOER, OSTSTF flag in ICSR6 (when the OSTSTE bit is 1), or, as additionally specified in POECR6, the POEmF (n = 1 to 4; m = 0, 4, 8, 10) flag in ICSRn, is set to 1.

20.2.14 Port Output Enable Control Register 4 (POECR4)

The POECR4 is used to extend the control conditions of the high-impedance state for the MTU3, MTU4, MTU6, and MTU7 pins for the MTU complementary PWM output.
For details about the targets and conditions of high-impedance control, see Figure 20.2.

Address(es): A008 0810h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IC5ADDMT67ZE	IC4ADDMT67ZE	IC3ADDMT67ZE	—	IC1ADDMT67ZE	—	—	—	IC5ADDMT34ZE	IC4ADDMT34ZE	IC3ADDMT34ZE	IC2ADDMT34ZE	—	—
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	IC2ADDMT34ZE	MTU3 and MTU4 High-Impedance POE4F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b3	IC3ADDMT34ZE	MTU3 and MTU4 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b4	IC4ADDMT34ZE	MTU3 and MTU4 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b5	IC5ADDMT34ZE	MTU3 and MTU4 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions. Note: Set this bit to the same value as the IC4ADDMT34ZE bit.	R/W*1
b8 to b6	—	Reserved	These bits are read as 0. The write value should be 0	R/W
b9	IC1ADDMT67ZE	MTU6 and MTU7 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	IC3ADDMT67ZE	MTU6 and MTU7 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b12	IC4ADDMT67ZE	MTU6 and MTU7 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b13	IC5ADDMT67ZE	MTU6 and MTU7 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions. Note: Set this bit to the same value as the IC4ADDMT67ZE bit.	R/W*1
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

IC2ADDMT34ZE Bit (MTU3 and MTU4 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 (POE4#) to the high-impedance control conditions for the MTU3 and MTU4 pins (MTIOC3B/MTIOC3D/MTIOC4A/MTIOC4C/MTIOC4B/MTIOC4D) or the GPT0 to GPT2 pins (GTIOC0A/GTIOC0B/GTIOC1A/GTIOC1B/GTIOC2A/GTIOC2B).

IC3ADDMT34ZE Bit (MTU3 and MTU4 High-Impedance POE8F Add)

Adds the POE8F flag in ICSR3 (POE8#) to the high-impedance control conditions for the MTU3 and MTU4 pins (MTIOC3B/MTIOC3D/MTIOC4A/MTIOC4C/MTIOC4B/MTIOC4D) or the GPT0 to GPT2 pins (GTIOC0A/GTIOC0B/GTIOC1A/GTIOC1B/GTIOC2A/GTIOC2B).

IC4ADDMT34ZE Bit (MTU3 and MTU4 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 (POE10#) to the high-impedance control conditions for the MTU3 and MTU4 pins (MTIOC3B/MTIOC3D/MTIOC4A/MTIOC4C/MTIOC4B/MTIOC4D) or the GPT0 to GPT2 pins (GTIOC0A/GTIOC0B/GTIOC1A/GTIOC1B/GTIOC2A/GTIOC2B).

IC5ADDMT34ZE Bit (MTU3 and MTU4 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR5 (POE10#) to the high-impedance control conditions for the MTU3 and MTU4 pins (MTIOC3B/MTIOC3D/MTIOC4A/MTIOC4C/MTIOC4B/MTIOC4D) or to the GPT0 to GPT2 pins (GTIOC0A/GTIOC0B/GTIOC1A/GTIOC1B/GTIOC2A/GTIOC2B).

Note: Set this bit to the same value as the IC4ADDMT34ZE bit.

IC1ADDMT67ZE Bit (MTU6 and MTU7 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 (POE0#) to the high-impedance control conditions for the MTU6, and MTU4, and GPT0 to GPT2 pins (MTIOC3B/MTIOC3D/GTIOC0A/GTIOC0B/MTIOC4A/MTIOC4C/GTIOC1A/GTIOC1B/MTIOC4B/MTIOC4D/GTIOC2A/GTIOC2B).

IC3ADDMT67ZE Bit (MTU6 and MTU7 High-Impedance POE8F Add)

Adds the POE8F flag in ICSR3 (POE8#) to the high-impedance control conditions for the MTU6, and MTU7 pins (MTIOC6B, MTIOC6D, MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D).

IC4ADDMT67ZE Bit (MTU6 and MTU7 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 (POE10#) to the high-impedance control conditions for the MTU6, and MTU7 pins (MTIOC6B/MTIOC6D/MTIOC7A/MTIOC7C/MTIOC7B/MTIOC7D).

IC5ADDMT67ZE Bit (MTU6 and MTU7 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR5 (POE10#) to the high-impedance control conditions for the MTU6, and MTU7 pins (MTIOC6B/MTIOC6D/GTIOC0A/GTIOC0B/MTIOC7A/MTIOC7C/GTIOC1A/GTIOC1B/MTIOC7B/MTIOC7D/GTIOC2A/GTIOC2B).

Note: Set this bit to the same value as the IC4ADDMT67ZE bit.

20.2.15 Port Output Enable Control Register 5 (POECR5)

The POECR5 is used to extend the control conditions of the high-impedance for the MTU0 pin.
For details about the targets and conditions of high-impedance control, see Figure 20.2.

Address(es): A008 0812h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	IC5ADDMT0ZE	IC4ADDMT0ZE	—	IC2ADDMT0ZE	IC1ADDMT0ZE	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	IC1ADDMT0ZE	MTU0 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b2	IC2ADDMT0ZE	MTU0 High-Impedance POE4F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	IC4ADDMT0ZE	MTU0 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W*1
b5	IC5ADDMT0ZE	MTU0 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions. Note: Set this bit to the same value as the IC4ADDMT0ZE bit.	R/W*1
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

IC1ADDMT0ZE Bit (MTU0 High-Impedance POE0F Add)

Adds the POE0F flag in ICSR1 (POE0#) to the high-impedance control conditions for the MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC2ADDMT0ZE Bit (MTU0 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 (POE4#) to the high-impedance control conditions for the MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC4ADDMT0ZE Bit (MTU0 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR4 (POE10#) to the high-impedance control conditions for the MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

IC5ADDMT0ZE Bit (MTU0 High-Impedance POE10F Add)

Adds the POE10F flag in ICSR5 (POE10#) to the high-impedance control conditions for the MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D).

Note: Set this bit to the same value as the IC4ADDMT0ZE bit.

20.2.16 Port Output Enable Control Register 6 (POECR6)

The POECR6 is used to extend the control conditions of the high-impedance for the GPT3 pins.
For details about the targets and conditions of high-impedance control, see Figure 20.2.

Address(es): A008 0814h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IC4ADDGPT3ZE	IC3ADDGPT3ZE	IC2ADDGPT3ZE	IC1ADDGPT3ZE	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	—	Reserved	This bit is always read as 1. The write value should be 1.	R/W
b8 to b5	—	Reserved	These bits are read as 0. The write value should be 0	R/W
b9	IC1ADDGPT3ZE	GPT3 High-Impedance POE0F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W *1
b10	IC2ADDGPT3ZE	GPT3 High-Impedance POE4F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W *1
b11	IC3ADDGPT3ZE	GPT3 High-Impedance POE8F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W *1
b12	IC4ADDGPT3ZE	GPT3 High-Impedance POE10F Add	0: Does not add the pins to the high-impedance control conditions. 1: Adds the pins to the high-impedance control conditions.	R/W *1
b13	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

IC1ADDGPT3ZE Bit (GPT3 High -Impedance POE0F Add)

Adds the POE0F flag in ICSR1 (POE0#) to the high-impedance control conditions for the GPT3 pins (GTIOC3A, GTIOC3B).

IC2ADDGPT3ZE Bit (GPT3 High-Impedance POE4F Add)

Adds the POE4F flag in ICSR2 (POE4#) to the high-impedance control conditions for the GPT3 pins (GTIOC3A, GTIOC3B).

IC3ADDGPT3ZE Bit GPT3 High -Impedance POE8F Add)

Adds the POE8F flag in ICSR3 (POE8#) to the high-impedance control conditions for the GPT3 pins (GTIOC3A, GTIOC3B).

IC4ADDGPT3ZE Bit (GPT3 High -Impedance POE10F Add)

Adds the POE10F flag in ICSR4 (POE10#) to the high-impedance control conditions for the GPT3 pins (GTIOC3A, GTIOC3B).

20.2.17 GPT3 Pin Select Register (G3SELR)

G3SELR is an 8-bit readable/writable register that selects the target pins for high-impedance control on GPT3.

Address(es): A008 0823h

	b7	b6	b5	b4	b3	b2	b1	b0
	G3BSEL[3:0]				G3ASEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	G3ASEL[3:0]	GPT3-A (GTIOC3A) Pin Select	b3 b0 0000: Controls the high-impedance state of PA6 when it is in use as the GTIOC3A pin. 0100: Controls the high-impedance state of P66 when it is in use as the GTIOC3A pin. Settings other than above are prohibited.	R/W*1
b7 to b4	G3BSEL[3:0]	GPT3-B (GTIOC3B) Pin Select	b7 b4 0000: Controls the high-impedance state of PA7 when it is in use as the GTIOC3B pin. 0100: Controls the high-impedance state of P67 when it is in use as the GTIOC3B pin. Settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

G3ASEL[3:0] Bits (GPT3-A (GTIOC3A) Pin Select)

These bits select the target GTIOC3A pin for high-impedance control.

G3BSEL[3:0] Bits (GPT3-B (GTIOC3B) Pin Select)

These bits select the target GTIOC3B pin for high-impedance control.

20.2.18 MTU0 Pin Select Register 1 (M0SELR1)

M0SELR1 is an 8-bit readable/writable register that selects the A and B pins on MTU0 as targets for high-impedance control.

Address(es): A008 0824h

	b7	b6	b5	b4	b3	b2	b1	b0
	M0BSEL[3:0]				M0ASEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	M0ASEL[3:0]	MTU0-A (MTIOC0A) Pin Select	b3 b0 0000: Controls the high-impedance state of PE6 when it is in use as the MTIOC0A pin. 0010: Controls the high-impedance state of PP4 when it is in use as the MTIOC0A pin. Settings other than above are prohibited.	R/W*1
b7 to b4	M0BSEL[3:0]	MTU0-B (MTIOC0B) Pin Select	b7 b4 0000: Controls the high-impedance state of PP3 when it is in use as the MTIOC0B pin. 0001: Controls the high-impedance state of PE4 when it is in use as the MTIOC0B pin. Settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

M0ASEL[3:0] Bits (MTU0-A (MTIOC0A) Pin Select)

These bits select the target MTIOC0A pin for high-impedance control.

M0BSEL[3:0] Bits (MTU0-B (MTIOC0B) Pin Select)

These bits select the target MTIOC0B pin for high-impedance control.

20.2.19 MTU0 Pin Select Register 2 (M0SELR2)

M0SELR2 is an 8-bit readable/writable register that selects the C and D pins on MTU0 as targets for high-impedance control.

Address(es): A008 0825h

	b7	b6	b5	b4	b3	b2	b1	b0
	M0DSEL[3:0]				M0CSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	M0CSEL[3:0]	MTU0-C (MTIOC0C) Pin Select	b3 b0 0000: Controls the high-impedance state of PE5 when it is in use as the MTIOC0C pin. 0010: Controls the high-impedance state of PP2 when it is in use as the MTIOC0C pin. Settings other than above are prohibited.	R/W*1
b7 to b4	M0DSEL[3:0]	MTU0-D (MTIOC0D) Pin Select	b7 b4 0000: Controls the high-impedance state of PE3 when it is in use as the MTIOC0D pin. 0010: Controls the high-impedance state of PP1 when it is in use as the MTIOC0D pin. Settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bit is modified once, writing this bit does not modify its value until the register is reset.

M0CSEL[3:0] Bits (MTU0-C (MTIOC0C) Pin Select)

These bits select the target MTIOC0C pin for high-impedance control.

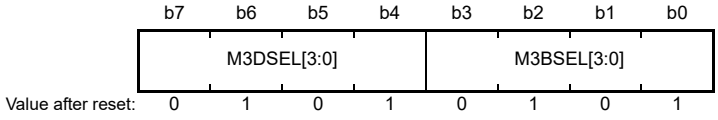
M0DSEL[3:0] Bits (MTU0-D (MTIOC0D) Pin Select)

These bits select the target MTIOC0D pin for high-impedance control.

20.2.20 MTU3 Pin Select Register (M3SELR)

M3SELR is an 8-bit readable/writable register that selects the B and D pins on MTU3 or the A and B pins on GPT channel 0 as targets for high-impedance control. MPC (multi-function pin controller) can be used to set which MTU3 or GPT pins are to be controlled.

Address(es): A008 0826h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	M3BSEL[3:0]	MTU3-B (MTIOC3B)/GPT Channel 0-A (GTIOC0A) Pin Select	b3 b0 0001: Controls the high-impedance state of P16. 0010: Controls the high-impedance state of PB7. 0011: Controls the high-impedance state of PA2. To control the high-impedance state, settings other than above are prohibited.	R/W*1
b7 to b4	M3DSEL[3:0]	MTU3-D (MTIOC3D)/GPT Channel 0-B (GTIOC0B) Pin Select	b7 b4 0001: Controls the high-impedance state of P15. 0011: Controls the high-impedance state of PF6. 0101: Controls the high-impedance state of PA1. To control the high-impedance state, settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.

M3BSEL[3:0] Bits (MTU3-B (MTIOC3B)/GPT Channel 0-A (GTIOC0A) Pin Select)

These bits select the target MTIOC3B/GTIOC0A pin for high-impedance control.

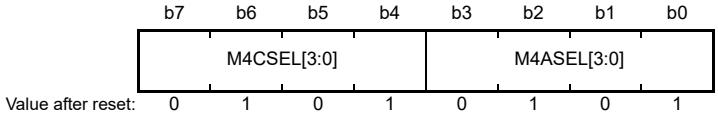
M3DSEL[3:0] Bits (MTU3-D (MTIOC3D)/GPT Channel 0-B (GTIOC0B) Pin Select)

These bits select the target MTIOC3D/GTIOC0B pin for high-impedance control.

20.2.21 MTU4 Pin Select Register 1 (M4SELR1)

M4SELR1 is an 8-bit readable/writable register that selects A and C pins on MTU4 or the A and B pins on GPT channel 1 as targets for high-impedance control. MPC (multi-function pin controller) can be used to set which MTU3 or GPT pins are to be controlled.

Address(es): A008 0827h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	M4ASEL[3:0]	MTU4-A (MTIOC4A)/GPT Channel 1-A (GTIOC1A) Pin Select	b3 b0 0001: Controls the high-impedance state of PA0. 0011: Controls the high-impedance state of PF5. 0101: Controls the high-impedance state of P14. Settings other than above are prohibited.	R/W*1
b7 to b4	M4CSEL[3:0]	MTU4-C (MTIOC4C)/GPT Channel 1-B (GTIOC1B) Pin Select	b7 b4 0001: Controls the high-impedance state of P77. 0011: Controls the high-impedance state of P87. 0101: Controls the high-impedance state of P13. Settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.

M4ASEL[3:0] Bits (MTU4-A (MTIOC4A)/GPT Channel 1-A (GTIOC1A) Pin Select)

These bits select the target MTIOC4A/GTIOC1A pin for high-impedance control.

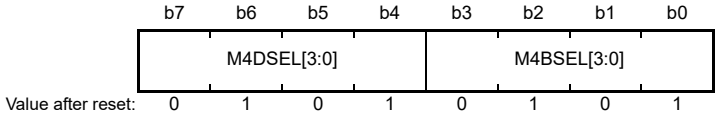
M4CSEL[3:0] Bits (MTU4-C (MTIOC4C)/GPT Channel 1-B (GTIOC1B) Pin Select)

These bits select the target MTIOC4C/GTIOC1B pin for high-impedance control.

20.2.22 MTU4 Pin Select Register 2 (M4SELR2)

M4SELR2 is an 8-bit readable/writable register that selects B and D pins on MTU4 or the A and B pins on GPT channel 2 as targets for high-impedance control. MPC (multi-function pin controller) can be used to set which MTU3 or GPT pins are to be controlled.

Address(es): A008 0828h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	M4BSEL[3:0]	MTU4-B (MTIOC4B)/GPT Channel 2-A (GTIOC2A) Pin Select	b3 b0 0000: Controls the high-impedance state of P86. 0011: Controls the high-impedance state of P76. 0101: Controls the high-impedance state of P12. Settings other than above are prohibited.	R/W*1
b7 to b4	M4DSEL[3:0]	MTU4-D (MTIOC4D)/GPT Channel 2-B (GTIOC2B) Pin Select	b7 b4 0001: Controls the high-impedance state of P75. 0011: Controls the high-impedance state of PD7. 0101: Controls the high-impedance state of P11. Settings other than above are prohibited.	R/W*1

Note 1. Can be modified only once after a reset. After the bits are modified once, writing these bits does not modify their values until the register is reset.

M4BSEL[3:0] Bits (MTU4-B (MTIOC4B)/GPT Channel 2-A (GTIOC2A) Pin Select)

These bits select the target MTIOC4B/GTIOC2A pin for high-impedance control.

M4DSEL[3:0] Bits (MTU4-D (MTIOC4D)/GPT Channel 2-B (GTIOC2B) Pin Select)

These bits select the target MTIOC4D/GTIOC2B pin for high-impedance control.

20.3 Operation

Table 20.4 shows the target pins for high-impedance control and conditions to place the pins in high-impedance state.

Table 20.4 Target Pins and Conditions for High-Impedance Control (1 / 2)

Pins	Conditions	Detailed Conditions
MTU3 or GPT0 pins (MTIOC3B and MTIOC3D, or GTIOC0A and GTIOC0B)	• Operation for detection of the POE0# input level • Operation for comparison of the output levels on the MTIOC3B and MTIOC3D or GTIOC0A and GTIOC0B pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU3BDZE• ((POE0F) +(OSF1•OCE1) +(MTUCH34HIZ) +(IC2ADDMT34ZE•POE4F) +(IC3ADDMT34ZE•POE8E•POE8F) +(IC4ADDMT34ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT34ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU4 or GPT1 pins (MTIOC4A and MTIOC4C, or GTIOC1A and GTIOC1B)	• Operation for detection of the POE0# input level • Operation for comparison of the output levels on the MTIOC4A and MTIOC4C or GTIOC1A and GTIOC1B pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU4ACZE• ((POE0F) +(OSF1•OCE1) + (MTUCH34HIZ) +(IC2ADDMT34ZE•POE4F) +(IC3ADDMT34ZE•POE8E•POE8F) +(IC4ADDMT34ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT34ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU4 or GPT2 pins (MTIOC4B and MTIOC4D, or GTIOC2A and GTIOC2B)	• Operation for detection of the POE0# input level • Operation for comparison of the output levels on the MTIOC4B and MTIOC4D or GTIOC2A and GTIOC2B pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU4BDZE• ((POE0F) +(OSF1•OCE1) +(MTUCH34HIZ) +(IC2ADDMT34ZE•POE4F) +(IC3ADDMT34ZE•POE8E•POE8F) +(IC4ADDMT34ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT34ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU6 pins (MTIOC6B and MTIOC6D)	• Operation for detection of the POE4# input level • Operation for comparison of the output levels on the MTIOC6B and MTIOC6D pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU6BDZE• ((POE4F) +(OSF2•OCE2) +(MTUCH67HIZ) +(IC1ADDMT67ZE•POE0F) +(IC3ADDMT67ZE•POE8E•POE8F) +(IC4ADDMT67ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT67ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU7 pins (MTIOC7A and MTIOC7C)	• Operation for detection of the POE4# input level • Operation for comparison of the output levels on the MTIOC7A and MTIOC7C pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU7ACZE• ((POE4F) +(OSF2•OCE2) +(MTUCH67HIZ) +(IC1ADDMT67ZE•POE0F) +(IC3ADDMT67ZE•POE8E•POE8F) +(IC4ADDMT67ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT67ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))

Table 20.4 Target Pins and Conditions for High-Impedance Control (2 / 2)

Pins	Conditions	Detailed Conditions
MTU7 pins (MTIOC7B and MTIOC7D)	• Operation for detection of the POE4# input level • Operation for comparison of the output levels on the MTIOC7B and MTIOC7D pins • SPOER setting • Additional conditions of the POECR4 • Detection of stopped oscillation or oscillation abnormality*1	MTU7BDZE• ((POE4F) +(OSF2•OCE2) +(MTUCH67HIZ) +(IC1ADDMT67ZE•POE0F) +(IC3ADDMT67ZE•POE8E•POE8F) +(IC4ADDMT67ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT67ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU0 pin (MTIOC0A)	• Operation for detection of the POE8# input level • SPOER setting • Additional conditions of the POECR5 • Detection of stopped oscillation or oscillation abnormality*1	MTU0AZE• ((POE8F•POE8E) +(MTUCH0HIZ) +(IC1ADDMT0ZE•POE0F) +(IC2ADDMT0ZE•POE4F) +(IC4ADDMT0ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT0ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU0 pin (MTIOC0B)	• Operation for detection of the POE8# input level • SPOER setting • Additional conditions of the POECR5 • Detection of stopped oscillation or oscillation abnormality*1	MTU0BZE• ((POE8F•POE8E) +(MTUCH0HIZ) +(IC1ADDMT0ZE•POE0F) +(IC2ADDMT0ZE•POE4F) +(IC4ADDMT0ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT0ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU0 pin (MTIOC0C)	• Operation for detection of the POE8# input level • SPOER setting • Additional conditions of the POECR5 • Detection of stopped oscillation or oscillation abnormality*1	MTU0CZE• ((POE8F•POE8E) +(MTUCH0HIZ) +(IC1ADDMT0ZE•POE0F) +(IC2ADDMT0ZE•POE4F) +(IC4ADDMT0ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT0ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
MTU0 pin (MTIOC0D)	• Operation for detection of the POE8# input level • SPOER setting • Additional conditions of the POECR5 • Detection of stopped oscillation or oscillation abnormality*1	MTU0DZE• ((POE8F•POE8E) +(MTUCH0HIZ) +(IC1ADDMT0ZE•POE0F) +(IC2ADDMT0ZE•POE4F) +(IC4ADDMT0ZE•ICSR4.POE10E•ICSR4.POE10F) +(IC5ADDMT0ZE•ICSR5.POE10E•ICSR5.POE10F) +(OSTSTE•OSTSTF))
GPT3 pins (GTIOC3A and GTIOC3B)	• Operation for detection of the POE10# input level • SPOER setting • Additional conditions of the POECR6 • Detection of stopped oscillation or oscillation abnormality*1	GPT3ABZE• ((ICSR5.POE10F•ICSR5.POE10E) +(GPT3HIZ) +(IC1ADDGPT3ZE•POE0F) +(IC2ADDGPT3ZE•POE4F) +(IC3ADDGPT3ZE•POE8E•POE8F) +(IC4ADDGPT3ZE•ICSR4.POE10E•ICSR4.POE10F) +(OSTSTE•OSTSTF))

Note 1. The clock monitor circuit (CLMA0, CLMA1) can detect the oscillation abnormality.

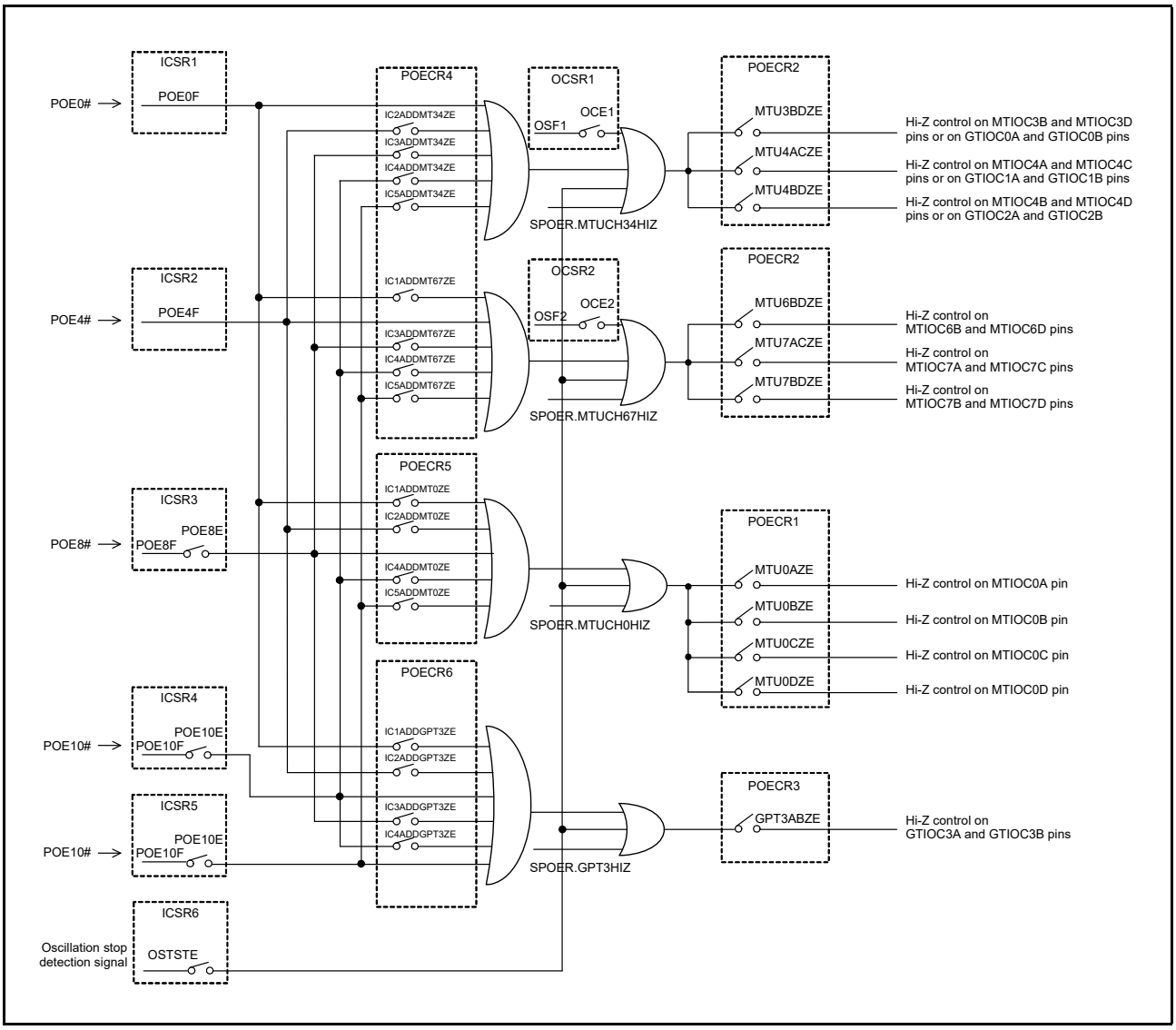


Figure 20.2 Target Pins and Conditions for High-Impedance Control

High-impedance requests to individual pins can be controlled by the settings in the POECR1 to POECR3 registers.

The following input pins can be added to high-impedance control conditions by the settings in the POECR4 to POECR6 registers: input pins other than the POE0# pin for the MTU3, MTU4, and GPT0 to GPT2 pins; input pins other than the POE4# pin for the MTU6 and MTU7 pins; input pins other than the POE8# pin for the MTU0 pins; input pins other than the POE10# pin for the GPT3 pins.

For example, setting the IC2ADDMT34ZE bit in POECR4 to 1 outputs high-impedance requests to the MTU3, MTU4, GPT0, GPT1, and GPT2 pins even when the POE4# input is detected.

High-impedance requests due to the detection of POE8# input, POE10# input, stopped oscillation, or oscillation abnormality (CLMA0/1) can be controlled by the settings in the ICSR3 to ICSR6 registers. (The ICSR1 and ICSR2 registers do not control enabling or disabling of output of high-impedance requests.)

High-impedance requests to the MTU3, MTU4, GPT0, GPT1, GPT2, MTU6, and MTU7 pins as the results of output level comparison can be controlled by the settings in the OCSR1 and OCSR2 registers.

20.3.1 MTU3/GPT Pin Selection

In RZ/T1, the pin functions for MTU and GPT are respectively assigned to multiple sets of port pins. The target pins for high-impedance control can be selected by the pin selection register in POE3 (G3SELR, M0SELR1, M0SELR2, M3SELR, M4SELR1, or M4SELR2 register). Table 20.5 shows the correspondence between MTU and GPT pins and selection registers.

Note that settings for pins to be used as MTU or GPT must be separately made in the registers of the multi-function pin controller (MPC). Take care so that there are no differences between the pins selected in the POE3 registers and the pins selected in the MPC registers. For details about MPC registers, see section 18, Multi-Function Pin Controller (MPC).

Table 20.5 Correspondence between MTU and GPT Pins

MTU/GPT Pin Functions	Corresponding Ports	Selection Registers
MTIOC0A	PP4*1 PE6	M0SELR1
MTIOC0B	PP3*1 PE4	
MTIOC0C	PP2*1 PE5	M0SELR2
MTIOC0D	PP1*1 PE3	
MTIOC3B	P16 PA2 PB7	M3SELR
MTIOC3D	P15 PA1 PF6	
MTIOC4A	P14 PA0 PF5	M4SELR1
MTIOC4C	P13 P77 P87	
MTIOC4B	P12*1 P76 P86	M4SELR2
MTIOC4D	P11*1 P75 PD7	
MTIOC6B	PA7*2 PS5*1	—
MTIOC6D	P70*2 PS4*1	
MTIOC7A	PS3*1 PE7*2	
MTIOC7C	P42*2 PS2*1	
MTIOC7B	P22*2 PS1*1	
MTIOC7D	PS0*1 PH6*2	
GTIOC0A	P16 PA2 PB7	M3SELR
GTIOC0B	P15 PA1 PF6	
GTIOC1A	P14 PA0 PF5	M4SELR1
GTIOC1B	P13 P77 P87	
GTIOC2A	P12*1 P76 P86	M4SELR2
GTIOC2B	P11*1 P75 PD7	
GTIOC3A	P66*1 PA6	G3SELR
GTIOC3B	P67*1 PA7	

Note 1. This is only selectable in 320-pin products.
Note 2. This is not a target for high-impedance control by POE3. The targets for high-impedance control are PS0 to PS5 pins.

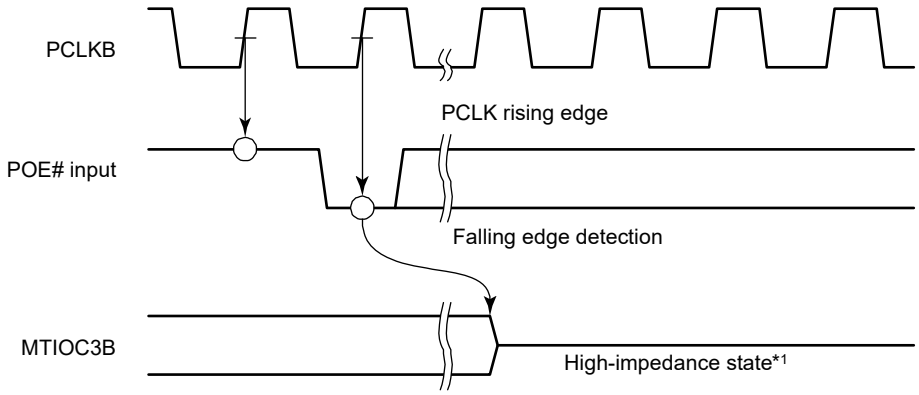
20.3.2 Input Level Detection Operation

If the input conditions set by ICSR1 to ICSR5 occur on the POE0#, POE4#, POE8#, and POE10# pins, the MTU3 and MTU4 or MTU6 and MTU7 pins for the MTU complementary PWM output, and MTU0 pins, and GPT pins are placed in high-impedance state. Note however, that these pins are still placed in the high-impedance state even when the GPT and MTU3 functions are not selected for the pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the POE0#, POE4#, POE8#, and POE10# pins, the pins for the MTU complementary PWM output, and MTU0 pins, and pin functions multiplexed with the GPT pins are placed in high-impedance state.

Figure 20.3 shows a sample timing after the level changes in input to the POE0#, POE4#, POE8#, and POE10# pins until the respective pins enter high-impedance state.

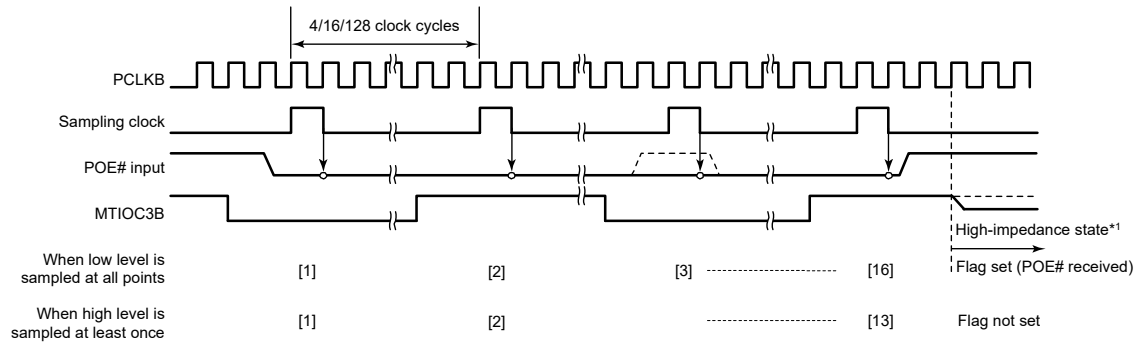


Note 1. Other pins also enter the high-impedance state at the same timing.

Figure 20.3 Falling Edge Detection

(2) Low-Level Detection

Figure 20.4 shows the low-level detection operation. Sixteen continuous low levels are sampled with the sampling clock selected by ICSR1 to ICSR5. If even one high level is detected during this interval, the low level is not accepted.
The timing when pins for the MTU complementary PWM output, and MTU0 pins and GPT pins enter the high-impedance state after the sampling clock is input is the same in both falling-edge detection and in low-level detection.



Note 1. Other pins also enter the high-impedance state at the same timing.

Figure 20.4 Low-Level Detection Operation

20.3.3 Output Level Compare Operation

Figure 20.5 shows an example of the output level compare operation for the combination of MTIOC3B and MTIOC3D. The operation is the same for the other pin combinations.

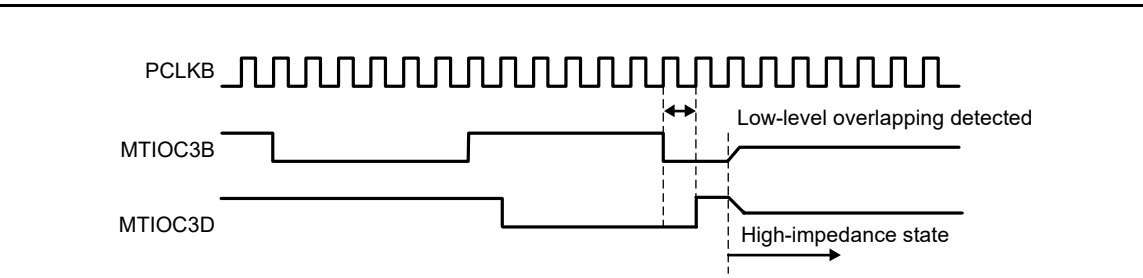


Figure 20.5 Output Level Compare Operation

20.3.4 High-Impedance Control Using Registers

The high-impedance state of the MTU pins (MTU0, MTU3, MTU4, MTU6, and MTU7) and the GPT pins can be directly controlled by using the software port output enable register (SPOER).
For instance, setting the MTUCH34HIZ bit in SPOER to 1 places the MTU3 and MTU4 pins specified by the port output enable control register 2 (POECR2) in the high-impedance state.
The high-impedance state of other pins can also be controlled by setting the appropriate bits in SPOER.

20.3.5 High-Impedance Control through Detection of Stopped Oscillation and Oscillation Abnormality

When the oscillation-stop detection circuit in the clock pulse generator detects the stopped oscillation or the clock monitor circuit (CLMA0, CLMA1) detects the oscillation abnormality, with the OSTSTE bit in ICSR6 being set, the MTU3 and MTU4 or MTU6 and MTU7 pins if specified in the port output enable control register 2 (POECR2), the MTU0 pins if specified in the port output enable control register 1 (POECR1), and the GPT pin if specified by the port enable register 3 (POECR3), can be placed in the high-impedance state.

20.3.6 Additional Functions for Controlling High-Impedance States

Settings in port enable registers 4 to 6 (POECR4 to POECR6) can add further high-impedance control conditions for the MTU complementary PWM output, MTU0, and GPT pins.
For instance, the settings listed below can be added as high-impedance control conditions for the MTU3 and MTU4 pins.

- Setting the IC2ADDMT34ZE bit in POECR4 to 1 adds the input level detection by the POE4#
- Setting the IC3ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE8#
- Setting the IC4ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE10# (ICSR4.POE10F)
- Setting the IC5ADDMT34ZE bit in POECR4 to 1 and adds the input level detection by the POE10# (ICSR5.POE10F)

The high-impedance state of other pins can also be controlled by setting the appropriate bits in the POECR4 to POECR6.

20.3.7 Release from High-Impedance State

MTU pins which have entered high-impedance state due to input-level detection can be released from the state either by returning them to their initial state with a reset, or by clearing all of the ICSR1.POE0F, ICSR2.POE4F, ICSR3.POE8F, ICSR4.POE10F, and ICSR5.POE10F flags. However, note that when low-level sampling is selected with the ICSR1.POE0M[1:0], ICSR2.POE4M[1:0], ICSR3.POE8M[1:0], ICSR4.POE10M[1:0], and ICSR5.POE10M[1:0] bits, just writing 0 to a flag is ignored (the flag is not cleared); flags can be cleared by writing 0 to it only after a high level is input to the POE0#, POE4#, POE8#, and POE10# pins and is sampled.
MTU pins which have entered high-impedance state due to output level detection can be released from the state either by returning them to their initial state with a reset, or by clearing the OCSR1.OSF1 flag or the OCSR2.OSF2 flag. When the OCSR1.OSF1 flag or the OCSR2.OSF2 flag is set to 0, the inactive level is output by setting the MTU, GRT and ALR1 registers.

20.4 POE3 Setting Procedure

Figure 20.6 shows the procedure for setting POE3. It illustrates an example of high-impedance control in response to comparison of the output levels on the GPT0 pins (GTIOC0A/GTIOC0B). In the figure, PA2 is selected as the GTIOC0A pin and PA1 is selected as the GTIOC0B pin.

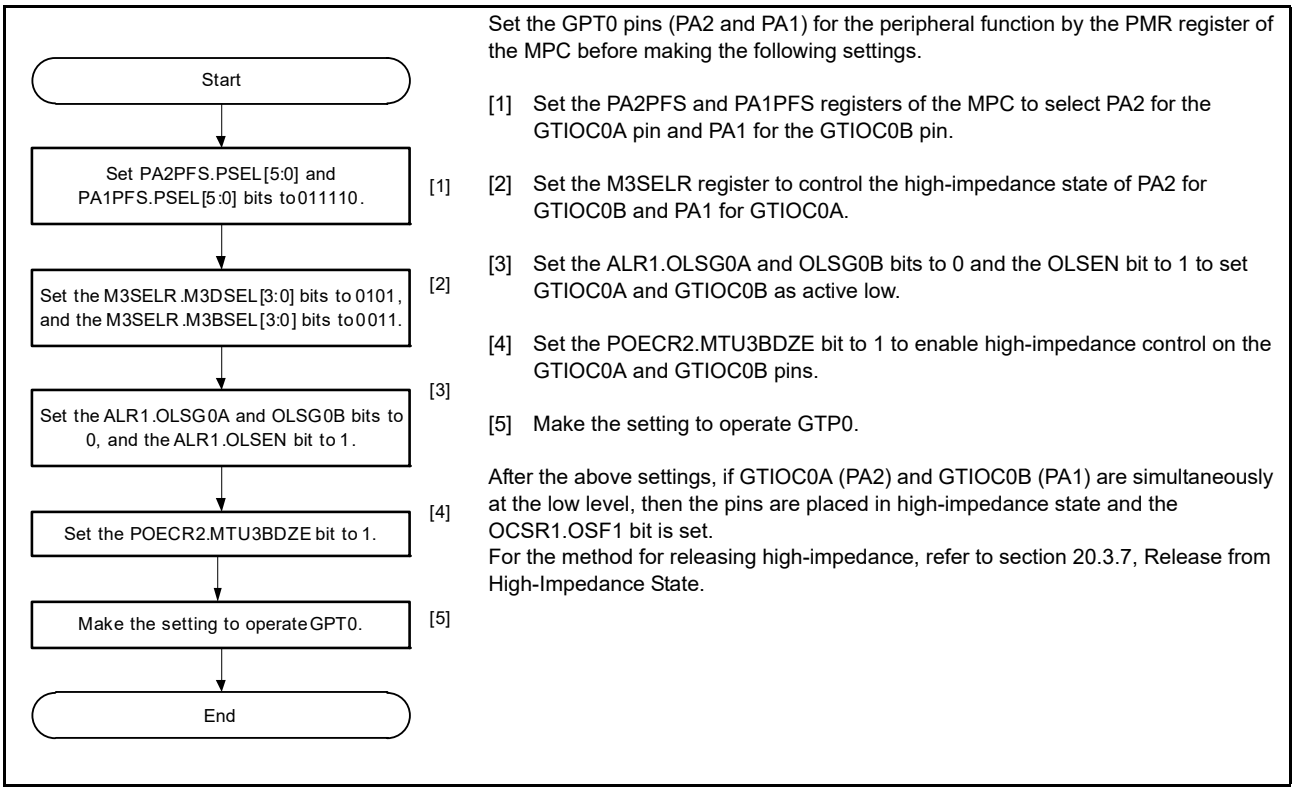


Figure 20.6 Procedure for Setting POE3

20.5 Interrupts

The POE3 issues a request to generate an interrupt when the specified condition is satisfied during input level detection or output level comparison. Table 20.6 shows the interrupt sources and their conditions.

Table 20.6 Interrupt Sources and Conditions

Name	Interrupt Source	Interrupt Flag	Condition
OEI1	Output enable interrupt 1	POE0F and OSF1	PIE1•POE0F+OIE1•OSF1
OEI2	Output enable interrupt 2	POE4F and OSF2	PIE2•POE4F+OIE2•OSF2
OEI3	Output enable interrupt 3	POE8F	PIE3•POE8F
OEI4	Output enable interrupt 4	ICSR4.POE10F and ICSR5.POE10F	PIE4•ICSR4.POE10F+PIE5•ICSR5.POE10F

20.6 Usage Notes

20.6.1 High-Impedance Control when the MTU and GPT Pins are Not Selected

If high-impedance control for a pin having a multiplexed MTU or GPT pin function on a register POECR1 to POECR3 is enabled and the high-impedance condition is satisfied, the pin is placed in the high-impedance state even if the MTU/GPT function is not selected for the pin on which it is multiplexed.
To avoid unintended high-impedance states, ensure that there are no differences between the settings for MTU and GPT pin selection in the PmnPFS registers of the MPC and for MTU and GPT pin selection in the pin selection register of the POE.

20.6.2 High-Impedance Control when MTU6 and MTU7 are Not Used

When MTU6 and MTU7 are not to be used, set the POECR2.MTU6BDZE, MTU7ACZE, and MTU7BDZE bits to 0 to disable high-impedance control.

21. General PWM Timer (GPTa)

The RZ/T1 has a general PWM timer (GPT) consisting of a four-channel 16-bit timer. The GPT can operate at up to 150 MHz.

21.1 Overview

Table 21.1 lists the specifications of the GPT, and Table 21.2 shows the functions of the GPT. Figure 21.1 shows a block diagram of the GPT.

Table 21.1 Specifications of GPT

Item	Description
Function	• 16 bits × 4 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter. • Clock sources independently selectable for each channel • Two input/output pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Synchronizable operation of the several counters • Modes of synchronized operation (synchronized, or displaced by desired times for phase shifting) • Generation of dead times in PWM operation • Through combination of three counters, generation of three-phase PWM waveforms incorporating dead times • Starting, clearing, and stopping counters in response to external or internal triggers • Internal trigger sources: software, and compare match • Starting and stopping of the counter, event capture, and count clear are possible in response to events set in the event link controller. • Noise filtering is selectable for the input capture and external trigger inputs. • The module-stop state can be set.

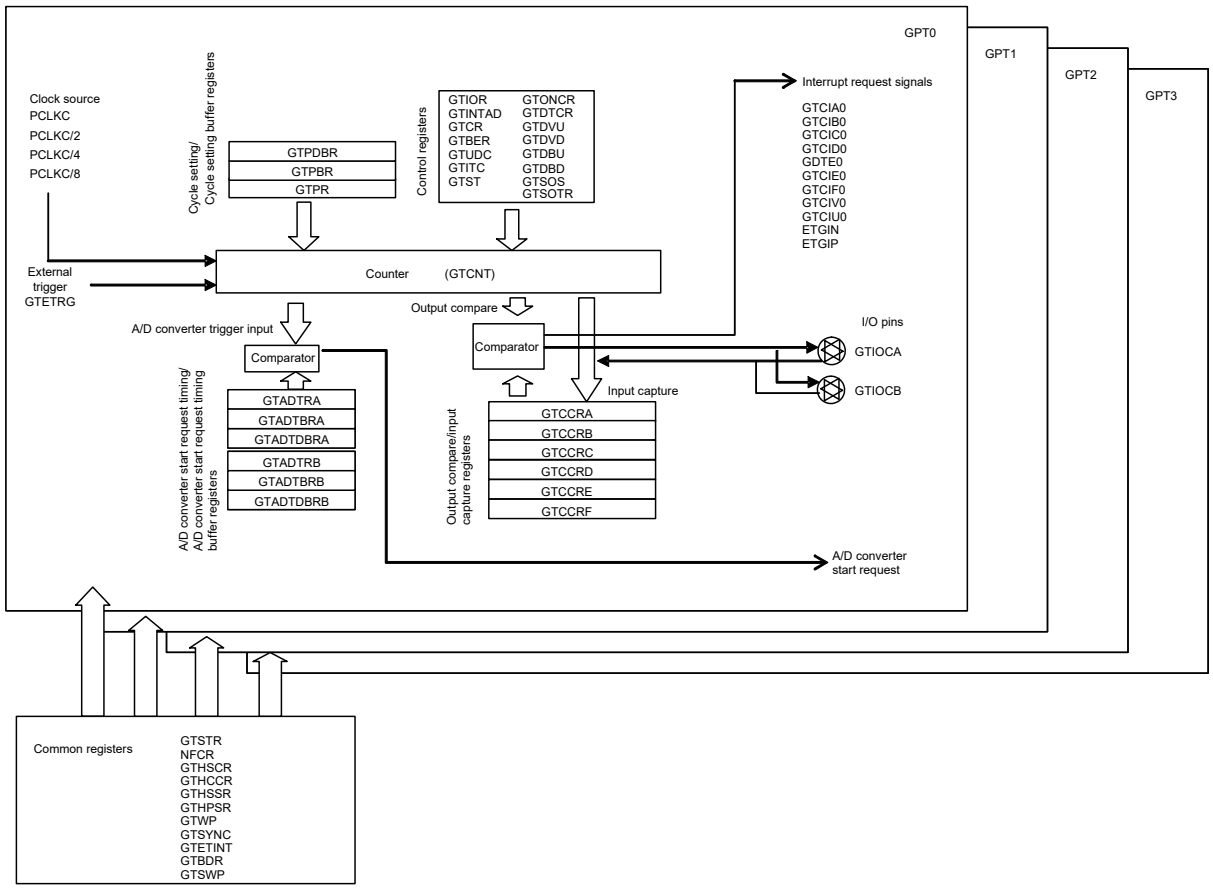
Table 21.2 Functions of GPT (1 / 2)

Item		GPT0	GPT1	GPT2	GPT3
Count clock		PCLKC PCLKC/2 PCLKC/4 PCLKC/8	PCLKC PCLKC/2 PCLKC/4 PCLKC/8	PCLKC PCLKC/2 PCLKC/4 PCLKC/8	PCLKC PCLKC/2 PCLKC/4 PCLKC/8
Output compare/input capture registers (GTCCR)		GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers		GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register		GTPR	GTPR	GTPR	GTPR
Cycle setting buffer registers		GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR	GTPBR GTPDBR
I/O pins		GTIOC0A GTIOC0B	GTIOC1A GTIOC1B	GTIOC2A GTIOC2B	GTIOC3A GTIOC3B
External trigger input pin		GTETRG			
Counter clear sources		GTPR compare match, input capture, comparator detection, GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare)			
Compare match output	Low output	√	√	√	√
	High output	√	√	√	√
	Toggle output	√	√	√	√
Input capture function		√	√	√	√
Synchronized operation		√	√	√	√
Phase shift start		√	√	√	√
Automatic addition of dead time		√	√	√	√
PWM mode		√	√	√	√
Buffer operation		√	√	√	√
One-shot operation		√	√	√	√
DMAC		All the interrupt sources			
A/D converter start trigger		Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB	Compare match of GTADTRA or GTADTRB

Table 21.2 Functions of GPT (2 / 2)

Item	GPT0	GPT1	GPT2	GPT3
Interrupt sources	Nine sources • GTCCRA compare match/input capture (GTCIA0) • GTCCRB compare match/input capture (GTCIB0) • GTCCRC compare match (GTCIC0) • GTCCRD compare match (GTCID0) • Dead time error (GDTE0) • GTCCRE compare match (GTCIE0) • GTCCRF compare match (GTCIF0) • GTCNT overflow (GTPR compare match) (GTCIV0) • GTCNT underflow (GTCIU0)	Nine sources • GTCCRA compare match/input capture (GTCIA1) • GTCCRB compare match/input capture (GTCIB1) • GTCCRC compare match (GTCIC1) • GTCCRD compare match (GTCID1) • Dead time error (GDTE1) • GTCCRE compare match (GTCIE1) • GTCCRF compare match (GTCIF1) • GTCNT overflow (GTPR compare match) (GTCIV1) • GTCNT underflow (GTCIU1)	Nine sources • GTCCRA compare match/input capture (GTCIA2) • GTCCRB compare match/input capture (GTCIB2) • GTCCRC compare match (GTCIC2) • GTCCRD compare match (GTCID2) • Dead time error (GDTE2) • GTCCRE compare match (GTCIE2) • GTCCRF compare match (GTCIF2) • GTCNT overflow (GTPR compare match) (GTCIV2) • GTCNT underflow (GTCIU2)	Nine sources • GTCCRA compare match/input capture (GTCIA3) • GTCCRB compare match/input capture (GTCIB3) • GTCCRC compare match (GTCIC3) • GTCCRD compare match (GTCID3) • Dead time error (GDTE3) • GTCCRE compare match (GTCIE3) • GTCCRF compare match (GTCIF3) • GTCNT overflow (GTPR compare match) (GTCIV3) • GTCNT underflow (GTCIU3)
Common interrupt source	External trigger			
Interrupt skipping function	Skips GTCNT overflows (GTPR compare match)(GTCIV0)/ GTCNT underflow (GTCIU0) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)(GTCIV1)/ GTCNT underflow (GTCIU1) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)(GTCIV2)/ GTCNT underflow (GTCIU2) interrupts (with interlocking function for other interrupts or A/D conversion requests).	Skips GTCNT overflows (GTPR compare match)(GTCIV3)/ GTCNT underflow (GTCIU3) interrupts (with interlocking function for other interrupts or A/D conversion requests).
Event operation according to the ELC settings	√	√	√	√
Noise filtering	√	√	√	√
Setting module-stop state	MSTPCRA.MSTPCRA9 bit			

√: Possible
—: Not possible



GTSTR:	General PWM timer software start register
NFCR:	Noise filter control register
GTHSCR:	General PWM timer hardware source start/stop control register
GTHCCR:	General PWM timer hardware source clear control register
GTHSSR:	General PWM timer hardware start source select register
GTHPSR:	General PWM timer hardware stop clear source select register
GTWP:	General PWM timer write-protection register
GTSYNC:	General PWM timer sync register
GTETINT:	General PWM timer external trigger input interrupt register
GTBDR:	General PWM timer buffer operation disable register
GTSWP:	General PWM timer start write-protection register
GTIOR:	General PWM timer I/O control register
GTINTAD:	General PWM timer interrupt output setting register
GTCR:	General PWM timer control register
GTBER:	General PWM timer buffer enable register
GTUDC:	General PWM timer count direction register
GTITC:	General PWM timer interrupt and A/D converter start request skipping setting register
GTST:	General PWM timer status register
GTCNT:	General PWM timer counter
GTCCRA:	General PWM timer compare capture register A
GTCCRB:	General PWM timer compare capture register B
GTCCRC:	General PWM timer compare capture register C
GTCCRD:	General PWM timer compare capture register D
GTCCRE:	General PWM timer compare capture register E
GTCCRF:	General PWM timer compare capture register F
GTPR:	General PWM timer cycle setting register
GTPBR:	General PWM timer cycle setting buffer register
GTPDBR:	General PWM timer cycle setting double-buffer register
GTADTRA:	A/D converter start request timing register A
GTADTBRA:	A/D converter start request timing buffer register A
GTADTDBRA:	A/D converter start request timing double-buffer register A
GTADTRB:	A/D converter start request timing register B
GTADTBRB:	A/D converter start request timing buffer register B
GTADTDBRB:	A/D converter start request timing double-buffer register B
GTONCR:	General PWM timer output negate control register
GTDTCR:	General PWM timer dead time control register
GTDVU:	General PWM timer dead time value register U
GTDVD:	General PWM timer dead time value register D
GTDBU:	General PWM timer dead time buffer register U
GTDBD:	General PWM timer dead time buffer register D
GTSOS:	General PWM timer output protection function status register
GTSOTR:	General PWM timer output protection function temporary release register

Figure 21.1 Block Diagram of GPT

Table 21.3 lists the I/O pins used in the GPT.

Table 21.3 I/O Pins of GPT

Channel	Pin Name	I/O	Function
GPT	GTETRG	Input	External trigger input pin
GPT0	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT1	GTIOC1A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT2	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3	GTIOC3A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB register input capture input/output compare output/PWM output pin

21.2 Register Descriptions

21.2.1 General PWM Timer Software Start Register (GTSTR)

GTSTR starts or stops the GPTn.GTCNT counting operation (n = 0 to 3).

Address(es): GPT.GTSTR A006 C000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CST3	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	GPT0.GTCNT Count Start	0: Count operation is stopped 1: Count operation is performed	R/W
b1	CST1	GPT1.GTCNT Count Start		R/W
b2	CST2	GPT2.GTCNT Count Start		R/W
b3	CST3	GPT3.GTCNT Count Start		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CSTn Bit (GPTn.GTCNT Count Start) (n = 0 to 3)

This bit starts or stops GPTn.GTCNT operation.

If the SWPn bit in the general PWM timer start write-protection register (GTSWP) is set to disable writing to the CSTn bit, writing to the CSTn bit is ignored.

The counter operation can also be started or stopped by GTHSCR. When count operation is started by a hardware source, this bit is automatically set to 1, and when count operation is stopped by a hardware source, this bit is automatically cleared to 0.

21.2.2 Noise Filter Control Register (NFCR)

The NFCR register controls enabling and disabling of the noise filters and selects the sampling clocks for the noise filters.

Address(es): GPT.NFCR A006 C002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCS3[1:0]		NFCS2[1:0]		NFCS1[1:0]		NFCS0[1:0]		NFB3EN	NFA3EN	NFB2EN	NFA2EN	NFB1EN	NFA1EN	NFB0EN	NFA0EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFA0EN	Noise Filter 0A Enable	0: The noise filter for the GTIOC0A pin is disabled. 1: The noise filter for the GTIOC0A pin is enabled.	R/W
b1	NFB0EN	Noise Filter 0B Enable	0: The noise filter for the GTIOC0B pin is disabled. 1: The noise filter for the GTIOC0B pin is enabled.	R/W
b2	NFA1EN	Noise Filter 1A Enable	0: The noise filter for the GTIOC1A pin is disabled. 1: The noise filter for the GTIOC1A pin is enabled.	R/W
b3	NFB1EN	Noise Filter 1B Enable	0: The noise filter for the GTIOC1B pin is disabled. 1: The noise filter for the GTIOC1B pin is enabled.	R/W
b4	NFA2EN	Noise Filter 2A Enable	0: The noise filter for the GTIOC2A pin is disabled. 1: The noise filter for the GTIOC2A pin is enabled.	R/W
b5	NFB2EN	Noise Filter 2B Enable	0: The noise filter for the GTIOC2B pin is disabled. 1: The noise filter for the GTIOC2B pin is enabled.	R/W
b6	NFA3EN	Noise Filter 3A Enable	0: The noise filter for the GTIOC3A pin is disabled. 1: The noise filter for the GTIOC3A pin is enabled.	R/W
b7	NFB3EN	Noise Filter 3B Enable	0: The noise filter for the GTIOC3B pin is disabled. 1: The noise filter for the GTIOC3B pin is enabled.	R/W
b9, b8	NFCS0[1:0]	GPT0 Noise Filter Sampling Clock Select	b9 b8 0 0: PCLKC/1 0 1: PCLKC/4 1 0: PCLKC/32 1 1: Clock source for counting (excluding ELC events)	R/W
b11, b10	NFCS1[1:0]	GPT1 Noise Filter Sampling Clock Select	b11 b10 0 0: PCLKC/1 0 1: PCLKC/4 1 0: PCLKC/32 1 1: Clock source for counting (excluding ELC events)	R/W
b13, b12	NFCS2[1:0]	GPT2 Noise Filter Sampling Clock Select	b13 b12 0 0: PCLKC/1 0 1: PCLKC/4 1 0: PCLKC/32 1 1: Clock source for counting (excluding ELC events)	R/W
b15, b14	NFCS3[1:0]	GPT3 Noise Filter Sampling Clock Select	b15 b14 0 0: PCLKC/1 0 1: PCLKC/4 1 0: PCLKC/32 1 1: Clock source for counting (excluding ELC events)	R/W

NFAnEN Bit (Noise Filter nA Enable) (n = 0 to 3)

This bit disables or enables the noise filter for input from the GTIOCnA pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register (GTIOR) or set the GTCR.MD[2:0] bits to a value other than saw-wave PWM mode (000b) before doing so.

NFBnEN Bit (Noise Filter nB Enable) (n = 0 to 3)

This bit disables or enables the noise filter for input from the GTIOCnB pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register (GTIOR) or set the GTCR.MD[2:0] bits to a value other than saw-wave PWM mode (000b) before doing so.

NFCSn Bits (Noise Filter Sampling Clock Select) (n = 0 to 3)

These bits set the sampling interval for the noise filters. When setting these bits, wait for two cycles of the selected sampling interval before setting the input-capture function.

21.2.3 General PWM Timer Hardware Source Start/Stop Control Register (GTHSCR)

GTHSCR starts or stops the GPTn.GTCNT counting operation by a hardware source (n = 0 to 3).
When starting and stopping of the GPTn.GTCNT counter by a hardware source occur simultaneously, counter start is given priority.

Address(es): GPT.GTHSCR A006 C004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CPHW3[1:0]		CPHW2[1:0]		CPHW1[1:0]		CPHW0[1:0]		CSHW3[1:0]		CSHW2[1:0]		CSHW1[1:0]		CSHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CSHW0[1:0]	GPT0.GTCNT Hardware Source Count Start	0 0: Count operation is not started by a hardware source. 0 1: Count operation is started at the rising edge of a hardware source. 1 0: Count operation is started at the falling edge of a hardware source. 1 1: Count operation is started at both rising and falling edges of a hardware source.	R/W
b3, b2	CSHW1[1:0]	GPT1.GTCNT Hardware Source Count Start		R/W
b5, b4	CSHW2[1:0]	GPT2.GTCNT Hardware Source Count Start		R/W
b7, b6	CSHW3[1:0]	GPT3.GTCNT Hardware Source Count Start		R/W
b9, b8	CPHW0[1:0]	GPT0.GTCNT Hardware Source Count Stop	0 0: Count operation is not stopped by a hardware source. 0 1: Count operation is stopped at the rising edge of a hardware source. 1 0: Count operation is stopped at the falling edge of a hardware source. 1 1: Count operation is stopped at both rising and falling edges of a hardware source.	R/W
b11, b10	CPHW1[1:0]	GPT1.GTCNT Hardware Source Count Stop		R/W
b13, b12	CPHW2[1:0]	GPT2.GTCNT Hardware Source Count Stop		R/W
b15, b14	CPHW3[1:0]	GPT3.GTCNT Hardware Source Count Stop		R/W

CSHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Start) (n = 0 to 3)

The GPTn.GTCNT counter is started by a hardware source.
When the count operation is started by a hardware source, the corresponding bit in GTSTR automatically becomes 1.
The hardware source can be selected by GTHSSR.

CPHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Stop) (n = 0 to 3)

The GPTn.GTCNT counter is stopped by a hardware source.
When the count operation is stopped by a hardware source, the corresponding bit in GTSTR automatically becomes 0.
The hardware source can be selected by GTHPSR.

21.2.4 General PWM Timer Hardware Source Clear Control Register (GTHCCR)

GTHCCR sets clearing of GPTn.GTCNT by a hardware source (n = 0 to 3).
Once the clearing of GPTn.GTCNT counter by a hardware source is set, counter clearing by the hardware source is executed whether the GPTn.GTCNT count operation is performed (GTSTR.CSTn = 1; n = 0 to 3) or stopped (GTSTR.CSTn = 0; n = 0 to 3).

Address(es): GPT.GTHCCR A006 C006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CCSW3	CCSW2	CCSW1	CCSW0	CCHW3[1:0]		CCHW2[1:0]		CCHW1[1:0]		CCHW0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCHW0[1:0]	GPT0.GTCNT Hardware Source Counter Clear	0 0: Counter is not cleared by a hardware source. 0 1: Counter is cleared at the rising edge of a hardware source. 1 0: Counter is cleared at the falling edge of a hardware source. 1 1: Counter is cleared at both rising and falling edges of a hardware source.	R/W
b3, b2	CCHW1[1:0]	GPT1.GTCNT Hardware Source Counter Clear		R/W
b5, b4	CCHW2[1:0]	GPT2.GTCNT Hardware Source Counter Clear		R/W
b7, b6	CCHW3[1:0]	GPT3.GTCNT Hardware Source Counter Clear		R/W
b8	CCSW0	GPT0.GTCNT Counter Clear	When 1 is written to this bit, the counter is cleared. This bit automatically returns to 0 after the writing of 1. These bits are read as 0.	R/W
b9	CCSW1	GPT1.GTCNT Counter Clear		R/W
b10	CCSW2	GPT2.GTCNT Counter Clear		R/W
b11	CCSW3	GPT3.GTCNT Counter Clear		R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CCHWn[1:0] Bits (GPTn.GTCNT Hardware Source Count Clear) (n = 0 to 3)

GPTn.GTCNT is cleared by a hardware source.
The hardware source can be selected by GTHPSR.
When CCHWn[1:0] is 01b, 10b, or 11b, the hardware source can be accepted repeatedly.
When CCHWn[1:0] is set to 01b, 10b, or 11b simultaneously with setting of GTHSCR.CPHWn[1:0] for the same channel to 01b, 10b, or 11b, set the GPTn.GTCR.TPCS bits to 00b in advance.

CCSWn Bit (GPTn.GTCNT Counter Clear) (n = 0 to 3)

When 1 is written to this bit, the GPTn.GTCNT counter is cleared. This bit automatically returns to 0 after the writing of 1. This bit is always read as 0.

21.2.5 General PWM Timer Hardware Start Source Select Register (GTHSSR)

GTHSSR sets the hardware source to start GPTn.GTCNT (n = 0 to 3).
To change the source, clear the GTHSCR.CSHWn[1:0] bits to 0 before changing the source.

Address(es): GPT.GTHSSR A006 C008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHSL3[3:0]				CSHSL2[3:0]				CSHSL1[3:0]				CSHSL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHSL0[3:0]	GPT0.GTCNT Hardware Counter Start Source Select	b3 b0 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To start the counter by a hardware source, settings other than above are prohibited.	R/W
b7 to b4	CSHSL1[3:0]	GPT1.GTCNT Hardware Counter Start Source Select	b7 b4 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To start the counter by a hardware source, settings other than above are prohibited.	R/W
b11 to b8	CSHSL2[3:0]	GPT2.GTCNT Hardware Counter Start Source Select	b11 b8 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To start the counter by a hardware source, settings other than above are prohibited.	R/W
b15 to b12	CSHSL3[3:0]	GPT3.GTCNT Hardware Counter Start Source Select	b15 b12 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input To start the counter by a hardware source, settings other than above are prohibited.	R/W

CSHSLn[3:0] Bits (GPTn.GTCNT Hardware Counter Start Source Select) (n = 0 to 3)

These bits select the hardware source to start GPTn.GTCNT.

Note: When 1000b is selected as the hardware source, clear b5 of the GPT3.GTIOR.GTIOA[5:0] bits and the GPT3.GTONCR.OAE bit to 0. When 1001b is selected as the hardware source, clear b5 of the GPT3.GTIOR.GTIOB[5:0] bits and the GPT3.GTONCR.OBE bit to 0.

21.2.6 General PWM Timer Hardware Stop/Clear Source Select Register (GTHPSR)

GTHPSR sets the hardware source to stop or clear GPTn.GTCNT (n = 0 to 3).
To change the source, clear the GTHSCR.CPHWn[1:0] bits and GTHCCR.CCHWn[1:0] bits to 0 before changing the source.

Address(es): GPT.GTHPSR A006 C00Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSHPL3[3:0]				CSHPL2[3:0]				CSHPL1[3:0]				CSHPL0[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CSHPL0[3:0]	GPT0.GTCNT Hardware Counter Stop/ Clear Source Select	b3 b0 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To stop or clear the counter by a hardware source, settings other than above are prohibited.	R/W
b7 to b4	CSHPL1[3:0]	GPT1.GTCNT Hardware Counter Stop/ Clear Source Select	b7 b4 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To stop or clear the counter by a hardware source, settings other than above are prohibited.	R/W
b11 to b8	CSHPL2[3:0]	GPT2.GTCNT Hardware Counter Stop/ Clear Source Select	b11 b8 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 0 1 0: GTIOC3A internal output (output compare) 1 0 1 1: GTIOC3B internal output (output compare) 1 1 0 0: GTETRG pin input To stop or clear the counter by a hardware source, settings other than above are prohibited.	R/W
b15 to b12	CSHPL3[3:0]	GPT3.GTCNT Hardware Counter Stop/ Clear Source Select	b15 b12 1 0 0 0: GTIOC3A pin input 1 0 0 1: GTIOC3B pin input 1 1 0 0: GTETRG pin input To stop or clear the counter by a hardware source, settings other than above are prohibited.	R/W

CSHPLn[3:0] Bits (GPTn.GTCNT Hardware Counter Stop/Clear Source Select) (n = 0 to 3)

These bits select the hardware source to stop or clear GPTn.GTCNT.

Note: When 1000b is selected as the stop/clear source, clear b5 of the GPT3.GTIOR.GTIOA[5:0] bits and the GPT3.GTONCR.OAE bit to 0. When 1001b is selected as the stop/clear source, clear b5 of the GPT3.GTIOR.GTIOB[5:0] bits and the GPT3.GTONCR.OBE bit to 0.

21.2.7 General PWM Timer Write-Protection Register (GTWP)

GTWP enables or disables writing to registers to prevent accidental modification.
For registers to which writing is enabled or disabled by the setting of the GPWP register, see section 21.7.1, Write-Protection for Registers.

Address(es): GPT.GTWP A006 C00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	WP3	WP2	WP1	WP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	WP0	GPT0 Register Write Disable	0: Writing to the register is enabled 1: Writing to the register is disabled	R/W
b1	WP1	GPT1 Register Write Disable		R/W
b2	WP2	GPT2 Register Write Disable		R/W
b3	WP3	GPT3 Register Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

WPn Bit (GPTn Register Write Disable) (n = 0 to 3)

This bit enables or disables writing to GPTn registers.

21.2.8 General PWM Timer Sync Register (GTSYNC)

GTSYNC sets the clearing source of the GPTn.GTCNT counter for synchronized clearing/synchronized operation. This register can be modified when count operation of GPTn.GTCNT is stopped (n = 0 to 3).

Address(es): GPT.GTSYNC A006 C00Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SYNC3[1:0]		—	—	SYNC2[1:0]		—	—	SYNC1[1:0]		—	—	SYNC0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SYNC0[1:0]	GPT0.GTCNT Counter Synchronized-Clear Source Select	b1 b0 0 0: GPT0.GTCNT is cleared by a GPT0 clearing source (synchronized clear is not performed). 0 1: GPT0.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT0.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT0.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	SYNC1[1:0]	GPT1.GTCNT Counter Synchronized-Clear Source Select	b5 b4 0 0: GPT1.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT1.GTCNT is cleared by a GPT1 clearing source (synchronized clear is not performed). 1 0: GPT1.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT1.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SYNC2[1:0]	GPT2.GTCNT Counter Synchronized-Clear Source Select	b9 b8 0 0: GPT2.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT2.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT2.GTCNT is cleared by a GPT2 clearing source (synchronized clear is not performed). 1 1: GPT2.GTCNT is synchronously cleared by a GPT3 clearing source.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	SYNC3[1:0]	GPT3.GTCNT Counter Synchronized-Clear Source Select	b13 b12 0 0: GPT3.GTCNT is synchronously cleared by a GPT0 clearing source. 0 1: GPT3.GTCNT is synchronously cleared by a GPT1 clearing source. 1 0: GPT3.GTCNT is synchronously cleared by a GPT2 clearing source. 1 1: GPT3.GTCNT is cleared by a GPT3 clearing source (synchronized clear is not performed)	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SYNCn[1:0] Bits (GPTn.GTCNT Counter Synchronized-Clear Source Select) (n = 0 to 3)

These bits select which channel's counter clearing source is used to clear GPTn.GTCNT. When setting the SYNCn[1:0] bits, first set the GPTn.GTCR.CCLR[1:0] bits to 11b (cleared by counter clearing in another channel performing synchronized clearing/synchronized operation).

21.2.9 General PWM Timer External Trigger Input Interrupt Register (GTETINT)

GTETINT enables or disables interrupts by the external trigger input pin (GTETRG).

Address(es): GPT.GTETINT A006 C010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GTETRGEN	GTENFCS[1:0]		—	—	—	—	—	—	—	—	—	—	—	ETINEN	ETIPEN
Value after reset:	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

- GTENFCS[1:0]

Bit	Symbol	Bit Name	Description	R/W
b0	ETIPEN	External Trigger Rising Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b1	ETINEN	External Trigger Falling Input Interrupt Request Enable	0: Interrupt request is disabled 1: Interrupt request is enabled	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	GTENFCS[1:0]	GTETRG Noise Filter Sampling Clock Select	b14 b13 0 0: PCLKC/1 0 1: PCLKC/2 1 0: PCLKC/4 1 1: PCLKC/32	R/W
b15	GTETRGEN	GTETRG Noise Filter Enable	0: The noise filter for the GTETRG pin is disabled. 1: The noise filter for the GTETRG pin is enabled.	R/W

ETIPEN Bit (External Trigger Rising Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the rising edge of an external trigger input.

ETINEN Bit (External Trigger Falling Input Interrupt Request Enable)

This bit enables or disables an interrupt request generated at the falling edge of an external trigger input.

GTENFCS[1:0] Bits (GTETRG Noise Filter Sampling Clock Select)

These bits set the sampling interval for the noise filters.

For the following registers and bits, wait for two cycles of the selected sampling interval after setting these bits, and then select the source of GTETRG and enable interrupt requests.

(1) Hardware start source select register GTHSSR. CSHSLn[3:0] (n = 0 to 3)
(2) Hardware stop clear source select register GTHPSR. CSHPLn [3:0] (n = 0 to 3)
(3) Output negate control register GTONCR.NFS[3:0]
(4) Interrupt request enable bits ETIPEN and ETINEN of this register

GTETRGEN Bit (GTETRG Noise Filter Enable)

This bit disables or enables the noise filter for input from the GTETRG pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, set the registers and bits as follows before doing so while interrupt requests are disabled.

(1) Hardware start source select register GTHSSR. CSHSLn[3:0] ≠ 1100b (n = 0 to 3)
(2) Hardware stop clear source select register GTHPSR. CSHPLn [3:0] ≠ 1100b (n = 0 to 3)
(3) Output negate control register GTONCR.NFS[3:0] ≠ 0111b
(4) Interrupt request enable bits ETIPEN and ETINEN of this register = 0b

21.2.10 General PWM Timer Buffer Operation Disable Register (GTBDR)

GTBDR collectively enables or disables buffer operation of each channel. Even though a bit in GTBDR is set to 0 (buffer operation is enabled), buffer operation is not performed unless buffer operation is enabled by GTBER.

Address(es): GPT.GTBDR A006 C014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BD33	BD32	BD31	BD30	BD23	BD22	BD21	BD20	BD13	BD12	BD11	BD10	BD03	BD02	BD01	BD00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BD00	GPT0.GTCCR Buffer Operation Disable	0: Buffer operation is enabled 1: Buffer operation is disabled	R/W
b1	BD01	GPT0.GTPR Buffer Operation Disable		R/W
b2	BD02	GPT0.GTADTR Buffer Operation Disable		R/W
b3	BD03	GPT0.GTDV Buffer Operation Disable		R/W
b4	BD10	GPT1.GTCCR Buffer Operation Disable		R/W
b5	BD11	GPT1.GTPR Buffer Operation Disable		R/W
b6	BD12	GPT1.GTADTR Buffer Operation Disable		R/W
b7	BD13	GPT1.GTDV Buffer Operation Disable		R/W
b8	BD20	GPT2.GTCCR Buffer Operation Disable		R/W
b9	BD21	GPT2.GTPR Buffer Operation Disable		R/W
b10	BD22	GPT2.GTADTR Buffer Operation Disable		R/W
b11	BD23	GPT2.GTDV Buffer Operation Disable		R/W
b12	BD30	GPT3.GTCCR Buffer Operation Disable		R/W
b13	BD31	GPT3.GTPR Buffer Operation Disable		R/W
b14	BD32	GPT3.GTADTR Buffer Operation Disable		R/W
b15	BD33	GPT3.GTDV Buffer Operation Disable		R/W

BDn0 Bit (GPTn.GTCCR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GPTn.GTCCRA, GPTn.GTCCRC, and GPTn.GTCCRD registers together and buffer operation using GPTn.GTCCRB, GPTn.GTCCRE, and GPTn.GTCCRF registers together.

BDn1 Bit (GPTn.GTPR Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GPTn.GTPR, GPTn.GTPBR, and GPTn.GTPDBR registers together.

BDn2 Bit (GPTn.GTADTR Counter Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using GPTn.GTADTRA, GPTn.GTADTBRA, and GPTn.GTADTDBRA registers together and buffer operation using GPTn.GTADTRB, GPTn.GTADTBRB, and GPTn.GTADTDBRB registers together.

BDn3 Bit (GPTn.GTDV Counter Buffer Operation Disable) (n = 0 to 3)

This bit disables buffer operation using the GPTn.GTDVU and GPTn.GTDBU registers together and buffer operation using GPTn.GTDVD and GPTn.GTDBD registers together.

21.2.11 General PWM Timer Start Write-Protection Register (GTSWP)

GTSWP enables or disables writing to the GTSTR register to prevent accidental modification.

Address(es): GPT.GTSWP A006 C018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SWP3	SWP2	SWP1	SWP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SWP0	GTSTR.CST0 Bit Write Disable	0: Writing to the register is enabled 1: Writing to the register is disabled	R/W
b1	SWP1	GTSTR.CST1 Bit Write Disable		R/W
b2	SWP2	GTSTR.CST2 Bit Write Disable		R/W
b3	SWP3	GTSTR.CST3 Bit Write Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWPn Bit (GTSTR.CSTn Bit Write Disable) (n = 0 to 3)

This bit enables or disables writing to the GTSTR.CSTn bit.

When this bit is set to disable writing, writing to the GTSTR.CSTn bit is ignored.

However, if the GTHSCR register is set to allow counter operation to be started or stopped by a hardware source, the status of counter operation (started or stopped by a hardware source) is written to the GTSTR.CSTn bit even if the SWPn bit is set to disable writing to GTSTR.CSTn bit.

21.2.12 General PWM Timer I/O Control Register (GTIOR)

GPTn.GTIOR sets the functions of the GTIOCnA and GTIOCnB pins (n = 0 to 3). Each channel has one GTIOCnA pin and one GTIOCnB pin. Values written to the GTIOR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTIOR A006 C100h, GPT1.GTIOR A006 C180h, GPT2.GTIOR A006 C200h, GPT3.GTIOR A006 C280h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBHLD	OBDFLT	GTIOB[5:0]						OAHLD	OADFLT	GTIOA[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	GTIOA[5:0]	GTIOCnA Pin Function Select	See Table 21.4.	R/W
b6	OADFLT	Output Value at GTIOCnA Pin Count Stop	0: The GTIOCnA pin outputs low when counting is stopped. 1: The GTIOCnA pin outputs high when counting is stopped.	R/W
b7	OAHLD	Output Retain at GTIOCnA Pin Count Start/ Stop	0: The GTIOCnA pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnA pin output level is retained at start/ stop of counting.	R/W
b13 to b8	GTIOB[5:0]	GTIOCnB Pin Function Select	See Table 21.4.	R/W
b14	OBDFLT	Output Value at GTIOCnB Pin Count Stop	0: The GTIOCnB pin outputs low when counting is stopped. 1: The GTIOCnB pin outputs high when counting is stopped.	R/W
b15	OBHLD	Output Retain at GTIOCnB Pin Count Start/ Stop	0: The GTIOCnB pin output level at start/stop of counting depends on the register setting. 1: The GTIOCnB pin output level is retained at start/ stop of counting.	R/W

Note: n = 0 to 3

GTIOA[5:0] Bits (GTIOCnA Pin Function Select)

These bits select the GTIOCnA pin function. For details, see Table 21.4.

OADFLT Bit (Output Value at GTIOCnA Pin Count Stop)

This bit sets whether the GTIOCnA pin outputs high or low when counting is stopped.

OAHLD Bit (Output Retain at GTIOCnA Pin Count Start/Stop)

This bit specifies whether the GTIOCnA pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OAHLD bit is set to 0]

- The initial output value specified by the GTIOA bit in GTIOR is output when counting starts.
- The value specified by the OADFLT bit is output when counting stops.
- If the OADFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OAHLD bit is set to 1]

- The output is retained when counting starts or stops.

GTIOB[5:0] Bits (GTIOCnB Pin Function Select)

These bits select the GTIOCnB pin function. For details, see Table 21.4.

OBDFLT Bit (Output Value at GTIOCnB Pin Count Stop)

This bit sets whether the GTIOCnB pin outputs high or low when counting is stopped.

OBHLD Bit (Output Retain at GTIOCnB Pin Count Start/Stop)

This bit specifies whether the GTIOCnB pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OBHLD bit is set to 0]

- The initial output value specified by the GTIOB bit in GTIOR is output when counting starts.
- The value specified by the OBDFLT bit is output when counting stops.
- If the OBDFLT bit is modified while counting is stopped, it is immediately reflected in the output.

[When the OBHLD bit is set to 1]

- The output is retained when counting starts or stops.

Table 21.4 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (1 / 2)

GTIOA/GTIOB[5:0] Bits						Function			
b5	b4	b3	b2	b1	b0	b5	b4	b3, b2	b1, b0
0	0	0	0	0	0	Compare match	Initial output is Low.	Output retained at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	0	0			Low output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	0	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	0	0			High output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	0	0			Toggle output at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	0	1	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match

Table 21.4 Settings of GTIOA[5:0] Bits (GTIOB[5:0] Bits) (2 / 2)

GTIOA/GTIOB[5:0] Bits						Function			
b5	b4	b3	b2	b1	b0	b5	b4	b3, b2	b1, b0
0	1	0	0	0	0	Compare match	Initial output is High.	Output retained at cycle end	Output retained at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	1	0	0			Low output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	0	1	0	1				Low output at GTPn.GTCCRA/ GTCCRB compare match
0	1	0	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	0	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	0	0			High output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	1	0	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	0	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	0	0			Toggle output at cycle end	Output retained at GTPn.GTCCRA/ GTCCRB compare match
0	1	1	1	0	1				Low output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	1	0				High output at GPTn.GTCCRA/ GTCCRB compare match
0	1	1	1	1	1				Toggle output at GPTn.GTCCRA/ GTCCRB compare match
1	x	x	x	0	0	Input capture	Don't care		Input capture at rising edge
1	x	x	x	0	1				Input capture at falling edge
1	x	x	x	1	0				Input capture at both edges
1	x	x	x	1	1				

x: Don't care

Note 1. The cycle end is an overflow (GTCNT = GTPR in up-count operation) or underflow (GTCNT = 0 in down-count operation) for saw waves, and the trough (GTCNT = 0) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3-b2 setting is given priority in saw-wave PWM mode, and the b1-b0 setting is given priority in any other mode.

Note 3. Even though a compare match is set in GTIOR, output will not be made to the pins. GTONCR needs to be set separately.

21.2.13 General PWM Timer Interrupt Output Setting Register (GTINTAD)

GTINTAD enables or disables interrupt requests and A/D converter start requests. Values written to the GTINTAD register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTINTAD A006 C102h, GPT1.GTINTAD A006 C182h, GPT2.GTINTAD A006 C202h, GPT3.GTINTAD A006 C282h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN	EINT	—	—	—	GTINTPR[1:0]		GTINTF	GTINTE	GTINTD	GTINTC	GTINTB	GTINTA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	GTINTA	GTCCRA Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b1	GTINTB	GTCCRB Compare Match/Input Capture Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b2	GTINTC	GTCCRC Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b3	GTINTD	GTCCRD Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b4	GTINTE	GTCCRE Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b5	GTINTF	GTCCRF Compare Match Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b7, b6	GTINTPR[1:0]	GTPR Compare Match Interrupt Enable	b7 b6 0 0: Interrupt request is disabled. 0 1: In saw-wave mode, interrupt requests are enabled at overflows. In triangle-wave mode, interrupt requests are enabled at crests. 1 0: In saw-wave mode, interrupt requests are enabled at under flows. In triangle-wave mode, interrupt requests are enabled at troughs. 1 1: In saw-wave mode, interrupt requests are enabled at both overflows and underflows. In triangle-wave mode, interrupt requests are enabled at both crests and troughs.	R/W
b10 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	EINT	Dead Time Error Interrupt Enable	0: Interrupt request is disabled. 1: Interrupt request is enabled.	R/W
b12	ADTRAUEN	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b13	ADTRADEN	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b14	ADTRBUEN	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W
b15	ADTRBDEN	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable	0: A/D converter start request is disabled. 1: A/D converter start request is enabled.	R/W

GTINTA Bit (GTCCRA Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRA compare match/input capture (GTCIA). Values written to the GTINTAD register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

GTINTB Bit (GTCCRB Compare Match/Input Capture Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRB compare match/input capture (GTCIB).

GTINTC Bit (GTCCRC Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRC compare match (GTCIC).

GTINTD Bit (GTCCRD Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRD compare match (GTCIC). The interrupt request is generated as a GTCIC interrupt.

GTINTE Bit (GTCCRE Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRE compare match (GTCIE).

GTINTF Bit (GTCCRF Compare Match Interrupt Enable)

This bit enables or disables interrupt requests by GTCCRF compare match (GTCIE). The interrupt request is generated as a GTCIE interrupt.

GTINTPR[1:0] Bits (GTPR Compare Match Interrupt Request Setting)

These bits enable or disable interrupt requests by a GTPR compare match (GTCNT counter overflow) and those by a GTCNT counter underflow (GTCIV/GTCIU).

EINT Bit (Dead Time Error Interrupt Enable)

This bit enables or disables interrupt requests by a dead time error (GDTE). The interrupt request is generated as a GDTE interrupt.

ADTRAUEN Bit (GTADTRA Compare Match (Up-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT up-count operation.

ADTRADEN Bit (GTADTRA Compare Match (Down-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT down-count operation.

ADTRBUEN Bit (GTADTRB Compare Match (Up-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT up-count operation.

ADTRBDEN Bit (GTADTRB Compare Match (Down-Count Operation) A/D Converter Start Request Enable)

This bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT down-count operation.

21.2.14 General PWM Timer Control Register (GTCR)

GTCR controls GTCNT. GTCR should be set while GTCNT operation is stopped. Values written to the GTCR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTCR A006 C104h, GPT1.GTCR A006 C184h, GPT2.GTCR A006 C204h, GPT3.GTCR A006 C284h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR[1:0]		—	—	TPCS[1:0]		—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MD[2:0]	Mode Select	b2 b0 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at crest) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) fixed buffer operation) Settings other than above are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	TPCS[1:0]	Timer Prescaler Select	b9 b8 0 0: PCLKC (system clock) 0 1: PCLKC/2 (system clock/2) 1 0: PCLKC/4 (system clock/4) 1 1: PCLKC/8 (system clock/8)	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	CCLR[1:0]	Counter Clear Source Select	b13 b12 0 0: None of the clearing sources is specified. 0 1: Cleared by GTCCRA input capture 1 0: Cleared by GTCCRB input capture 1 1: Cleared by counter clearing in another channel performing synchronous clearing/synchronous operation	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

MD[2:0] Bits (Mode Select)

These bits select the GPT operating mode.

TPCS[1:0] Bits (Timer Prescaler Select)

These bits select the clock for GTCNT. A clock source can be selected independently for each channel.

CCLR[1:0] Bits (Counter Clear Source Select)

These bits select the clearing source for GTCNT.

In saw-wave mode, when synchronous clearing is selected, synchronous clearing is handled equally to clearing by the counter's overflow or underflow and the pin output and buffer transfer are performed.

Even if the GTINTAD.GTINTPR[1:0] bits are set to 01b, 10b, or 11b at this time, the GTCIV interrupt is not requested.

In triangle-wave mode, when synchronous clearing is selected, only counter clearing is performed. Though the counter value becomes 0, it is not handled as a trough.

Once 01b, 10b, or 11b is selected as a counter clear source, counter clearing by the source is executed whether the GPTn.GTCNT count operation is performed (GTSTR.CSTn = 1; n = 0 to 3) or stopped (GTSTR.CSTn = 0, n = 0 to 3).

Do not set the CCLR[1:0] bits for a channel that is currently operating to 01b or 10b during synchronous clearing.

21.2.15 General PWM Timer Buffer Enable Register (GTBER)

GTBER makes settings for buffer operation.

GTBER should be set while GTCNT operation is stopped. Values written to the GTBER register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTBER A006 C106h, GPT1.GTBER A006 C186h, GPT2.GTBER A006 C206h, GPT3.GTBER A006 C286h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CCRA[1:0]	GTCCRA Buffer Operation	b1 b0 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD)	R/W
b3, b2	CCRB[1:0]	GTCCRB Buffer Operation	b3 b2 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF)	R/W
b5, b4	PR[1:0]	GTPR Buffer Operation	b5 b4 0 0: Buffer operation is not performed 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Double buffer operation (GTPDBR → GTPBR → GTPR)	R/W
b6	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9, b8	ADTTA[1:0]	GTADTRA Buffer Transfer Timing Select	• Triangle waves b9 b8 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b9 b8 0 0: No transfer Values other than 0 0: Transfer at underflow (during down-counting) or overflow (during up-counting) is performed.	R/W
b10	ADTDA	GTADTRA Double Buffer Operation	0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTDRA)	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	ADTTB[1:0]	GTADTRB Buffer Transfer Timing Select	• Triangle waves b13 b12 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • Saw waves b13 b12 0 0: No transfer Values other than 0 0: Transfer at an underflow (in down-counting) or overflow (in up-counting) is performed.	R/W
b14	ADTDB	GTADTRB Double Buffer Operation	0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTDRB)	R/W

Bit	Symbol	Bit Name	Description	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

CCRA[1:0] Bits (GTCCRA Buffer Operation)

These bits set buffer operation with GTCCRA, GTCCRC, and GTCCRD combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] Bits (GTCCRB Buffer Operation)

These bits set buffer operation with GTCCRB, GTCCRE, and GTCCRF combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] Bits (GTPR Buffer Operation)

These bits set buffer operation with GTPR, GTPBR, and GTPDBR combined.
For down-counting in saw-wave mode, set the PR[1:0] bits to 00b (buffered operation does not proceed).

CCRSWT Bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forcibly performs buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after the writing of 1. This bit is read as 0.
This bit is valid only when counting is stopped with compare match operation specified.

ADTTA[1:0] Bits (GTADTRA Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of GTADTRA, GTADTBRA, and GTADTDBRA.

ADTDA Bit (GTADTRA Double Buffer Operation)

These bits set buffer operation with GTADTRA, GTADTBRA, and GTADTDBRA combined.

ADTTB[1:0] Bits (GTADTRB Buffer Transfer Timing Select)

These bits set the transfer timing for buffer operation of GTADTRB, GTADTBRB, and GTADTDBRB.

ADTDB Bit (GTADTRB Double Buffer Operation)

These bits set buffer operation with GTADTRB, GTADTBRB, and GTADTDBRB combined.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (32-bit transfer at trough).

21.2.16 General PWM Timer Count Direction Register (GTUDC)

GTUDC sets the direction in which GTCNT counts (up-counting or down-counting).

- In saw-wave mode

When the UD value is set to 0 during up-counting, the count direction is changed at an overflow (GTCNT counter value = GTPR register value). When the UD value is set to 1 during up-counting, the count direction is changed at an underflow (GTCNT counter value = 0).
If the UD value is changed from 1 to 0 with the UDF bit being 0 and while counting is stopped, the counter starts up-count operation and the count direction is changed at an overflow (GTCNT counter value = GTPR register value).
If the UD value is changed from 0 to 1 with the UDF bit being 0 and while counting is stopped, the counter starts down-count operation and the count direction is changed at an underflow (GTCNT counter value = 0).
When the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

- In triangle-wave mode

Even if the UD value is changed during counting, the change will not be reflected in the count direction.
If the UD value is modified while the UDF bit is 0 and counting is stopped, the change will not be reflected in the count direction when counting starts. If the UDF bit is set to 1 while counting is stopped, the UD bit value at that time is reflected in the count direction when counting starts.

Address(es): GPT0.GTUDC A006 C108h, GPT1.GTUDC A006 C188h, GPT2.GTUDC A006 C208h, GPT3.GTUDC A006 C288h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT counts down. 1: GTCNT counts up.	R/W
b1	UDF	Forcible Count Direction Setting	0: Not forcibly set 1: Forcibly set	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

UD Bit (Count Direction Setting)

This bit sets the count direction (up-counting or down-counting) for GTCNT.

UDF Bit (Forcible Count Direction Setting)

This bit forcibly sets the count direction when GTCNT starts operation as the UD value.
Only 0 should be written to this bit during counter operation.
When 1 has been written to this bit while counting is stopped, this bit should be returned to 0 before counting starts.

21.2.17 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC)

GTITC sets the skipping function for GTCNT counter overflow (GTPR compare match) interrupt (GTCIV) or underflow interrupts (GTCIU) and also sets whether to link the other interrupts and A/D converter start requests with the GTCIV/GTCIU interrupt skipping function. Note that dead time error interrupts cannot be linked with the GTCIV/GTCIU interrupt skipping function.

Values written to the GTITC register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTITC A006 C10Ah, GPT1.GTITC A006 C18Ah, GPT2.GTITC A006 C20Ah, GPT3.GTITC A006 C28Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ITLA	GTCCRA Compare Match/ Input Capture Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b1	ITLB	GTCCRB Compare Match/ Input Capture Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b2	ITLC	GTCCRC Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b3	ITLD	GTCCRD Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b4	ITLE	GTCCRE Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b5	ITLF	GTCCRF Compare Match Interrupt Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b7, b6	IVTC[1:0]	GTCIV/GTCIU Interrupt Skipping Function Select	b7 b6 0 0: Skipping is not performed 0 1: Both overflow and underflow for saw waves and crest for triangle waves are counted and skipped. 1 0: Both overflow and underflow for saw waves and trough for triangle waves are counted and skipped. 1 1: Both overflow and underflow for saw waves and both crest and trough for triangle waves are counted and skipped	R/W
b10 to b8	IVTT[2:0]	GTCIV/GTCIU Interrupt Skipping Count Select	b10 b8 0 0 0: Skipping is not performed 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	ADTAL	GTADTRA A/D Converter Start Request Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADTBL	GTADTRB A/D Converter Start Request Link	0: Not linked with GTCIV/GTCIU interrupt skipping function. 1: Linked with GTCIV/GTCIU interrupt skipping function.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

ITLA Bit (GTCCRA Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRA compare match/input capture interrupt (GTCIA) with the GTCIV/GTCIU interrupt skipping function.

ITLB Bit (GTCCRB Compare Match/Input Capture Interrupt Link)

This bit specifies whether to link the GTCCRB compare match/input capture interrupt (GTCIB) with the GTCIV/GTCIU interrupt skipping function.

ITLC Bit (GTCCRC Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRC compare match interrupt (GTCIC) with the GTCIV/GTCIU interrupt skipping function.

ITLD Bit (GTCCRD Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRD compare match interrupt (GTCIC) with the GTCIV/GTCIU interrupt skipping function.

ITLE Bit (GTCCRE Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRE compare match interrupt (GTCIE) with the GTCIV/GTCIU interrupt skipping function.

ITLF Bit (GTCCRF Compare Match Interrupt Link)

This bit specifies whether to link the GTCCRF compare match interrupt (GTCIE) with the GTCIV/GTCIU interrupt skipping function.

IVTC[1:0] Bits (GTCIV/GTCIU Interrupt Skipping Function Select)

These bits set the skipping function for the GTPR compare match (GTCNT overflow) interrupt (GTCIV) or GTCNT underflow interrupt (GTCIU).

IVTT[2:0] Bits (GTCIV Interrupt Skipping Count Select)

These bits set the skipping count for the GTPR compare match (GTCNT overflow) interrupt (GTCIV) or GTCNT underflow interrupt (GTCIU).
When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL Bit (GTADTRA A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRA A/D converter start request with GTCIVn/GTCIUn interrupt skipping function. (n = 0 to 3)

ADTBL Bit (GTADTRB A/D Converter Start Request Link)

This bit specifies whether to link the GTADTRB A/D converter start request with GTCIVn/GTCIUn interrupt skipping function. (n = 0 to 3)

21.2.18 General PWM Timer Status Register (GTST)

GTST indicates the status of the GPT. Values written to the GTST register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTST A006 C10Ch, GPT1.GTST A006 C18Ch, GPT2.GTST A006 C20Ch, GPT3.GTST A006 C28Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	DTEF	ITCNT[2:0]			—	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	The read value is undefined.	R
b10 to b8	ITCNT[2:0]	GTCIV/GTCIU Interrupt Skipping Count Counter	Counter for counting the number of times a timer interrupt has been skipped.	R
b11	DTEF	Dead Time Error Flag	0: No dead time error has occurred. 1: A dead time error has occurred.	R
b14 to b12	—	Reserved	These bits are read as 0.	R
b15	TUCF	Count Direction Flag	0: The GPTn.GTCNT counter counts downward. 1: The GPTn.GTCNT counter counts upward.	R

ITCNT[2:0] Bits (GTCIV Interrupt Skipping Count Counter)

When the GTCIV/GTCIU interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter is incremented by 1 every time the GTCIV/GTCIU interrupt source is generated.

[Clearing conditions]

- The GTCIV/GTCIU interrupt skipping function is not used (GTITC.IVTT[2:0] is 000b when GTITC.IVTC[1:0] is 00b).
- The GTCIV/GTCIU interrupt skipping count matches the specified count (ITCNT[2:0] matches the skipping count specified by GTITC.IVTT[2:0]).

DTEF Flag (Dead Time Error Flag)

This flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.

This flag returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the cycle. This flag can only be read from. (Writing 0 to clear the flag is not allowed.)

When an interrupt by the DTEF flag is enabled (GTINTAD.EINT = 1), a GDTE interrupt is generated every time the DTEF flag changes from 0 to 1.

[Setting condition]

- The timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the timer cycle.

TUCF Flag (Count Direction Flag)

This flag indicates the count direction of GTCNT.

21.2.19 General PWM Timer Counter (GTCNT)

GTCNT is a 16-bit readable/writable counter. There is a total of four GTCNT counters, one counter for each channel. GTCNT can be written to only when counting is stopped; GTCNT cannot be written to during counting operation. GTCNT should always be accessed in 16-bits. Access in 8-bit units is prohibited. Values written to the GTCNT counter are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTCNT A006 C10Eh, GPT1.GTCNT A006 C18Eh, GPT2.GTCNT A006 C20Eh, GPT3.GTCNT A006 C28Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

21.2.20 General PWM Timer Compare Capture Register m (GTCCRm) (m = A to F)

GTCCRm registers are 16-bit readable/writable registers. There is a total of 24 GTCCRm registers, six registers for each channel.
GTCCRA and GTCCRB are registers used for both output compare and input capture.
GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB.
GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB). Values written to GTCCRm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTCCRA A006 C110h, GPT0.GTCCRB A006 C112h, GPT0.GTCCRC A006 C114h, GPT0.GTCCRD A006 C116h, GPT0.GTCCRE A006 C118h, GPT0.GTCCRF A006 C11Ah, GPT1.GTCCRA A006 C190h, GPT1.GTCCRB A006 C192h, GPT1.GTCCRC A006 C194h, GPT1.GTCCRD A006 C196h, GPT1.GTCCRE A006 C198h, GPT1.GTCCRF A006 C19Ah, GPT2.GTCCRA A006 C210h, GPT2.GTCCRB A006 C212h, GPT2.GTCCRC A006 C214h, GPT2.GTCCRD A006 C216h, GPT2.GTCCRE A006 C218h, GPT2.GTCCRF A006 C21Ah, GPT3.GTCCRA A006 C290h, GPT3.GTCCRB A006 C292h, GPT3.GTCCRC A006 C294h, GPT3.GTCCRD A006 C296h, GPT3.GTCCRE A006 C298h, GPT3.GTCCRF A006 C29Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.21 General PWM Timer Cycle Setting Register (GTPR)

GTPR is a 16-bit readable/writable register that sets the maximum count value of GTCNT. There is a total of four GTPR registers, one register for each channel.
For saw waves, the value of (GTPR × 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.
Values written to the GTPR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit. Do not modify the GTPR register during down-counting in saw-wave mode.

Address(es): GPT0.GTPR A006 C11Ch, GPT1.GTPR A006 C19Ch, GPT2.GTPR A006 C21Ch, GPT3.GTPR A006 C29Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.22 General PWM Timer Cycle Setting Buffer Register (GTPBR)

GTPBR is a 16-bit readable/writable register that functions as a buffer register for GTPR. There is a total of four GTPPR registers, one register for each channel. Values written to the GTPBR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTPBR A006 C11Eh, GPT1.GTPBR A006 C19Eh, GPT2.GTPBR A006 C21Eh, GPT3.GTPBR A006 C29Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.23 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR)

GTPDBR is a 16-bit readable/writable register that functions as a buffer register for GTPBR (double-buffer register for GTPR). There is a total of four GTPDBR registers, one register for each channel. Values written to the GTPDBR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTPDBR A006 C120h, GPT1.GTPDBR A006 C1A0h, GPT2.GTPDBR A006 C220h, GPT3.GTPDBR A006 C2A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.24 A/D Converter Start Request Timing Register m (GTADTRm) (m = A, B)

GTADTRm registers are 16-bit readable/writable registers that set the timing of A/D converter start request generation. When the GTADTRm value matches the GTCNT counter value, an A/D converter start request is generated. There is a total of eight GTPPRm registers, two register for each channel.

GTADTRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Values written to GTADTRm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTADTRA A006 C124h, GPT1.GTADTRA A006 C1A4h, GPT2.GTADTRA A006 C224h, GPT3.GTADTRA A006 C2A4h, GPT0.GTADTRB A006 C12Ch, GPT1.GTADTRB A006 C1ACh, GPT2.GTADTRB A006 C22Ch, GPT3.GTADTRB A006 C2ACh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.25 A/D Converter Start Request Timing Buffer Register m (GTADTBRm) (m = A, B)

GTADTBRm registers are 16-bit readable/writable registers that function as buffer registers for GTADTRm. There is a total of eight GTPPBRm registers, two register for each channel.
GTADTBRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Values written to GTADTBRm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTADTBRA A006 C126h, GPT1.GTADTBRA A006 C1A6h, GPT2.GTADTBRA A006 C226h, GPT3.GTADTBRA A006 C2A6h, GPT0.GTADTBRB A006 C12Eh, GPT1.GTADTBRB A006 C1AEh, GPT2.GTADTBRB A006 C22Eh, GPT3.GTADTBRB A006 C2AEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.26 A/D Converter Start Request Timing Double-Buffer Register m (GTADTDBRm) (m = A, B)

GTADTDBRm registers are 16-bit readable/writable registers that function as buffer registers for GTADTBRm (double-buffer registers for GTADTR). There is a total of eight GTPPDBRm registers, two register for each channel.
GTADTDBRm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Values written to GTADTDBRm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTADTDBRA A006 C128h, GPT1.GTADTDBRA A006 C1A8h, GPT2.GTADTDBRA A006 C228h, GPT3.GTADTDBRA A006 C2A8h,
GPT0.GTADTDBRB A006 C130h, GPT1.GTADTDBRB A006 C1B0h, GPT2.GTADTDBRB A006 C230h, GPT3.GTADTDBRB A006 C2B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.27 General PWM Timer Output Negate Control Register (GTONCR)

GTONCR controls negate of the GTIOCnA pin output and GTIOCnB pin output. Values written to the GTONCR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTONCR A006 C134h, GPT1.GTONCR A006 C1B4h, GPT2.GTONCR A006 C234h, GPT3.GTONCR A006 C2B4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OBE	OAE	—	SWN	—	—	—	NFV	NFS[3:0]				NVB	NVA	NEB	NEA
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NEA	GTIOCnA Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b1	NEB	GTIOCnB Pin Negate Control Enable	0: Negate is disabled 1: Negate is enabled	R/W
b2	NVA	GTIOCnA Pin Negate Value Setting	0: GTIOCnA pin is set to 0 when negate control is performed. 1: GTIOCnA pin is set to 1 when negate control is performed.	R/W
b3	NVB	GTIOCnB Pin Negate Value Setting	0: GTIOCnB pin is set to 0 when negate control is performed. 1: GTIOCnB pin is set to 1 when negate control is performed.	R/W
b7 to b4	NFS[3:0]	GTIOC Output Negate Source Select	b7 b4 0 1 1 1: GTETRG pin input 1 x x x: Software control (control through SWN bit) Settings other than above are prohibited.	R/W
b8	NFV	Negate Source Polarity Select	0: Negate control is provided when the negate source has become 0. 1: Negate control is provided when the negate source has become 1.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	SWN	Software Negate Control	When NFV bit is 0: 0: Negate control is provided. 1: Negate control is not provided. When NFV bit is 1: 0: Negate control is not provided. 1: Negate control is provided.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	OAE	GTIOCnA Pin Output Enable	0: No pin output 1: Pin output	R/W
b15	OBE	GTIOCnB Pin Output Enable	0: No pin output 1: Pin output	R/W

Note: n = 0 to 3

NEA Bit (GTIOCnA Pin Negate Control Enable)

This bit enables negate control of the GTIOCnA pin output.

NEB Bit (GTIOCnB Pin Negate Control Enable)

This bit enables negate control of the GTIOCnB pin output.

NVA Bit (GTIOCnA Pin Negate Value Setting)

This bit sets the output value of the GTIOCnA pin at negate control.

NVB Bit (GTIOCnB Pin Negate Value Setting)

This bit sets the output value of the GTIOCnB pin at negate control.

NFS[3:0] Bits (GTIOC Output Negate Source Select)

These bits select the negate source for the GTIOCnA pin output and GTIOCnB pin output.

NFV Bit (Negate Source Polarity Select)

This bit selects the negate source polarity for the GTIOCnA pin output and GTIOCnB pin output.

SWN Bit (Software Negate Control)

This bit specifies whether to provide negate control for the GTIOCnA pin output and GTIOCnB pin output.
This bit setting is valid when software control is selected as the negate source (NFS[3] bit is set to 1).

OAE Bit (GTIOCnA Pin Output Enable)

This bit selects whether to output the GTIOCnA pin output. This bit setting is valid only when compare match has been set (the GTIOR.GTIOA[5] bit is 0).

OBE Bit (GTIOCnB Pin Output Enable)

This bit selects whether to output the GTIOCnB pin output. This bit setting is valid only when compare match has been set (the GTIOR.GTIOB[13] bit is 0).

21.2.28 General PWM Timer Dead Time Control Register (GTDTCR)

GTDTCR enables automatic setting of a compare match value for negative-phase waveform with dead time. Values written to the GTDTCR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTDTCR A006 C136h, GPT1.GTDTCR A006 C1B6h, GPT2.GTDTCR A006 C236h, GPT3.GTDTCR A006 C2B6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: GTCCRB is set without using GTDVU and GTDVD. 1: GTDVU and GTDVD are used to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU Buffer Operation Enable	0: GTDVU buffer operation is disabled 1: GTDVU buffer operation is enabled	R/W
b5	TDBDE	GTDVD Buffer Operation Enable	0: GTDVD buffer operation is disabled 1: GTDVD buffer operation is enabled	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD Setting	0: GTDVU and GTDVD are set separately. 1: The value written to GTDVU is automatically set to GTDVD.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TDE Bit (Negative-Phase Waveform Setting)

This bit sets whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time that was obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD) is automatically set in GTCCRB.
The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The automatically set GTCCRB value has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB and the GPTn.GTST.DTEF flag is set to 1.

- Triangle waves
  Upper limit value: GTPR register value - 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode
  Upper limit value: GTPR register value
  Lower limit value: 0

TDBUE Bit (GTDVU Buffer Operation Enable)

This bit enables buffer operation with GTDVU and GTDBU combined.
The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.

TDBDE Bit (GTDVD Buffer Operation Enable)

This bit enables buffer operation with GTDVD and GTDBD combined.
The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.
When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

TDFER Bit (GTDVD Setting)

This bits sets whether or not the value written to GTDVU is also set to GTDVD automatically.

21.2.29 General PWM Timer Dead Time Value Register m (GTDVm) (m = U, D)

GTDVm is a 16-bit readable/writable register that sets the dead time for generating PWM waveforms with dead time.
There is a total of eight GTDVm registers, two registers for each channel: GTDVU used for up-counting and GTDVD used for down-counting.
Setting a dead time value that exceeds the cycle is prohibited. The set value can be confirmed by reading from GTCCRB.
When GTDVm is used, writing to GTCCRB is prohibited.
When this register is set to 0, waveforms without dead time are output.
GTDVm should always be accessed in 16-bit units. Access in 8-bit units is prohibited. Values written to GTDVm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTDVU A006 C138h, GPT1.GTDVU A006 C1B8h, GPT2.GTDVU A006 C238h, GPT3.GTDVU A006 C2B8h, GPT0.GTDVD A006 C13Ah, GPT1.GTDVD A006 C1BAh, GPT2.GTDVD A006 C23Ah, GPT3.GTDVD A006 C2BAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.30 General PWM Timer Dead Time Buffer Register m (GTDBm) (m = U, D)

GTDBm is a 16-bit readable/writable register that functions as a buffer register for GTDVm.
There is a total of eight GTDBm registers, two registers for each channel: GTDBU used for up-counting and GTDBD used for down-counting. Values written to GTDBm registers are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTDBU A006 C13Ch, GPT1.GTDBU A006 C1BCh, GPT2.GTDBU A006 C23Ch, GPT3.GTDBU A006 C2BCh, GPT0.GTDBD A006 C13Eh, GPT1.GTDBD A006 C1BEh, GPT2.GTDBD A006 C23Eh, GPT3.GTDBD A006 C2BEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

21.2.31 General PWM Timer Output Protection Function Status Register (GTSOS)

GTSOS is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode. Values written to the GTSOTR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTSOS A006 C140h, GPT1.GTSOS A006 C1C0h, GPT2.GTSOS A006 C240h, GPT3.GTSOS A006 C2C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SOS[1:0]	Output Protection Function Status	b1 b0 0 0: Normal operation 0 1: Protected state (GTCCRA = 0 is set during transfer at trough or crest) 1 0: Protected state (GTCCRA ≥ GTPR is set during transfer at trough) 1 1: Protected state (GTCCRA ≥ GTPR is set during transfer at crest)	R
b7 to b2	—	Reserved	These bits are read as 0 and cannot be modified.	R
b9, b8	—	Reserved	The read value is undefined. These bits cannot be modified.	R
b15 to b10	—	Reserved	These bits are read as 0 and cannot be modified.	R

SOS Bit (Output Protection Function Status)

This bit indicates the status of the output protection function in triangle-wave PWM mode. For details of the output protection function, see section 21.7.4, Output Protection Function for GTIOC Pin Output.

21.2.32 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR)

GTSOTR temporarily releases the protected state of GTIOCnB pin output when output protection has been set. The protected state can be released only for the case of GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA ≥ GTPR has occurred during transfer at trough). The protected state cannot be released for any other case. Values written to the GTSOTR register are ignored when write-protection is set to the relevant channel by the GTWP.WPn bit.

Address(es): GPT0.GTSOTR A006 C142h, GPT1.GTSOTR A006 C1C2h, GPT2.GTSOTR A006 C242h, GPT3.GTSOTR A006 C2C2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SOTR	Output Protection Function Temporary Release	0: Protected state is not released 1: Protected state is released	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SOTR Bit (Output Protection Function Temporary Release)

This bit sets whether to temporarily release the protected state of the GTIOCnB pin output in an output protected state. After the SOTR bit has been set to 1, the output protection function is canceled from the first trough. After the SOTR bit has been set to 0, output protection is resumed from the first trough.

21.3 Operation

21.3.1 Basic Operation

Each channel has a 16-bit timer which performs up-counting, down-counting, and up-/down-counting.
The cycle is controlled by compare register GTPR.
When the counter value matches the value in GTCCRA or GTCCRB, the output from the corresponding pin GTIOCnA or GTIOCnB can be changed (n = 0 to 3). GTCCRA or GTCCRB can be used as an input capture register with the GTIOCnA or GTIOCnB pin as the input.
GTCCRC and GTCCRD can function as buffer registers of GTCCRA, and GTCCRE and GTCCRF can function as buffer registers of GTCCRB.

21.3.1.1 Counter Operation

(1) Periodic Count Operation (in Up-Count Operation)

The counter in each channel starts up-count operation when the corresponding GTSTS.CSTn bit is set to 1. When the GTCNT value matches the GTPR value (overflow), the GTST.TCFPO flag is set to 1. If the GTINTAD.GTINTPR[0] bit is 1 at this time, a GTCIV interrupt is requested. After GTCNT overflows, up-count operation is resumed from 0000h.
Figure 21.2 shows an example of periodic count operation in up-count operation.

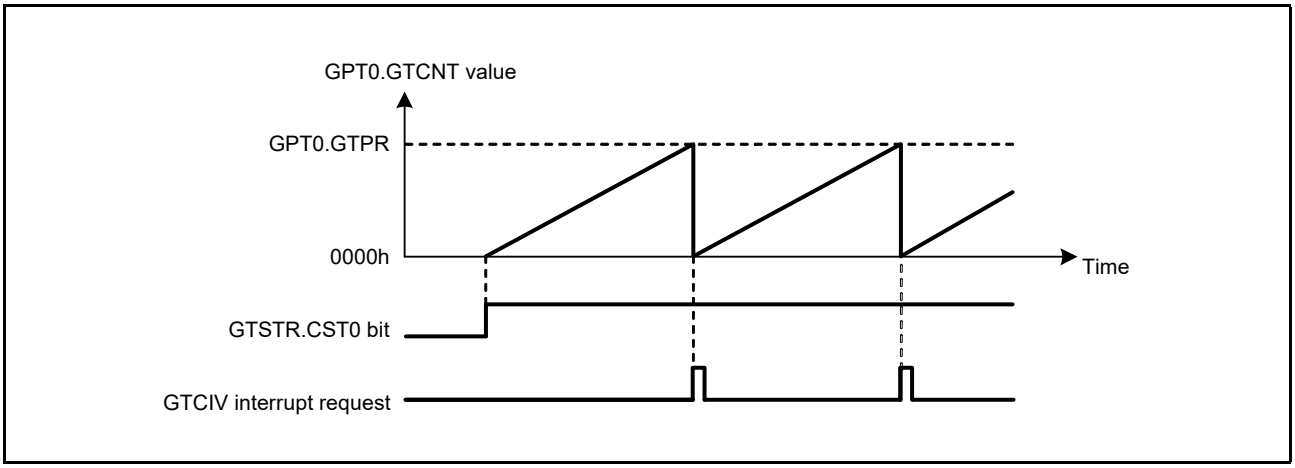


Figure 21.2 Example of Periodic Count Operation (in Up-Count Operation)

Figure 21.3 shows an example for setting periodic count operation in up-count operation.

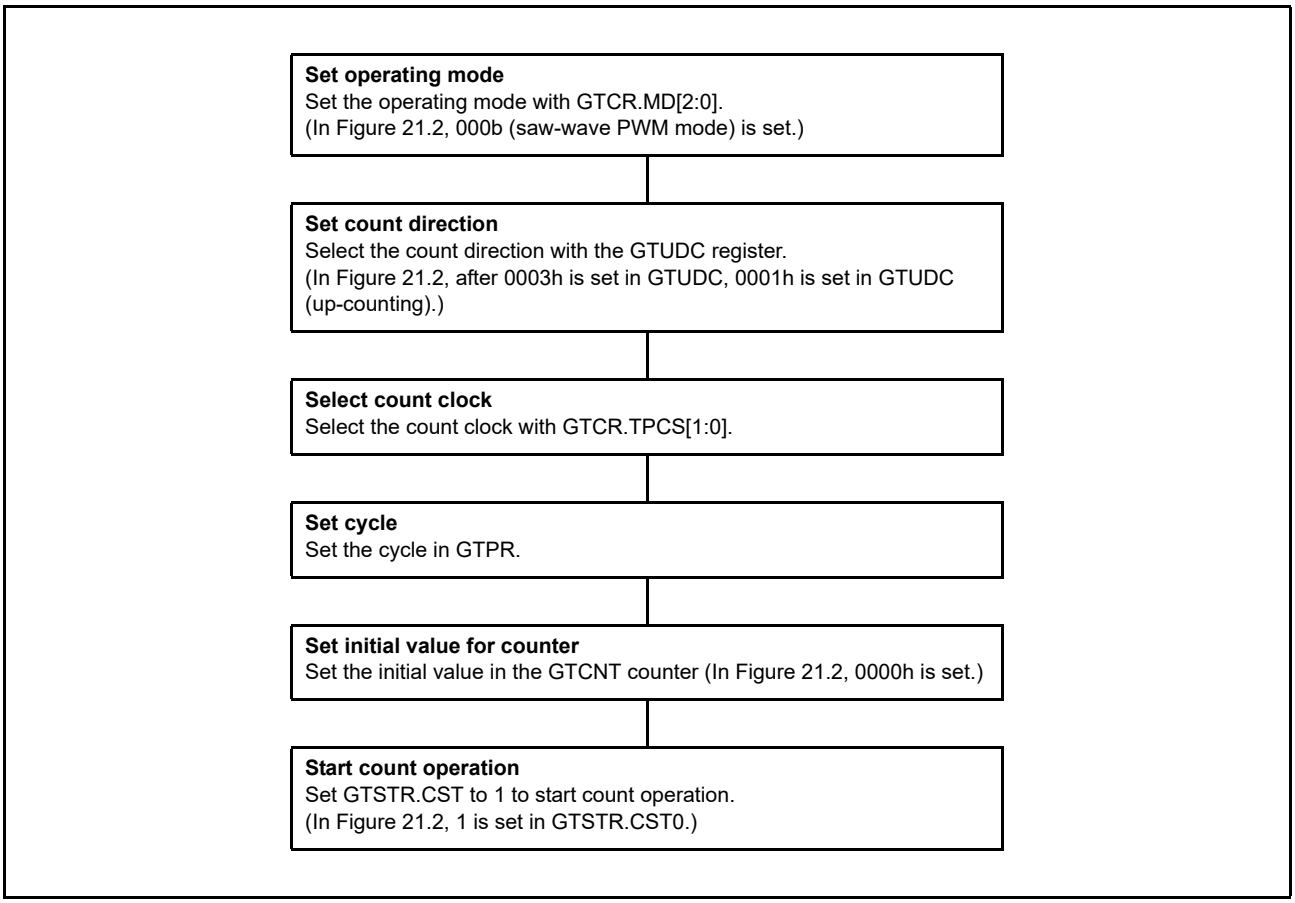


Figure 21.3 Example for Setting Periodic Count Operation (in Up-Count Operation)

(2) Periodic Count Operation (in Down-Count Operation)

The counter in each channel can perform down-count operation by setting GTUDC.
When GTCNT reaches 0 (underflow), the GTST.TCFPU flag is set to 1. If the GTINTAD.GTINTPR[1] bit is 1 at this time, a GTCIU interrupt is requested. After the GTCNT counter underflows, down-count operation is resumed from the GTPR value.
Figure 21.4 shows an example of periodic count operation in down-count operation.

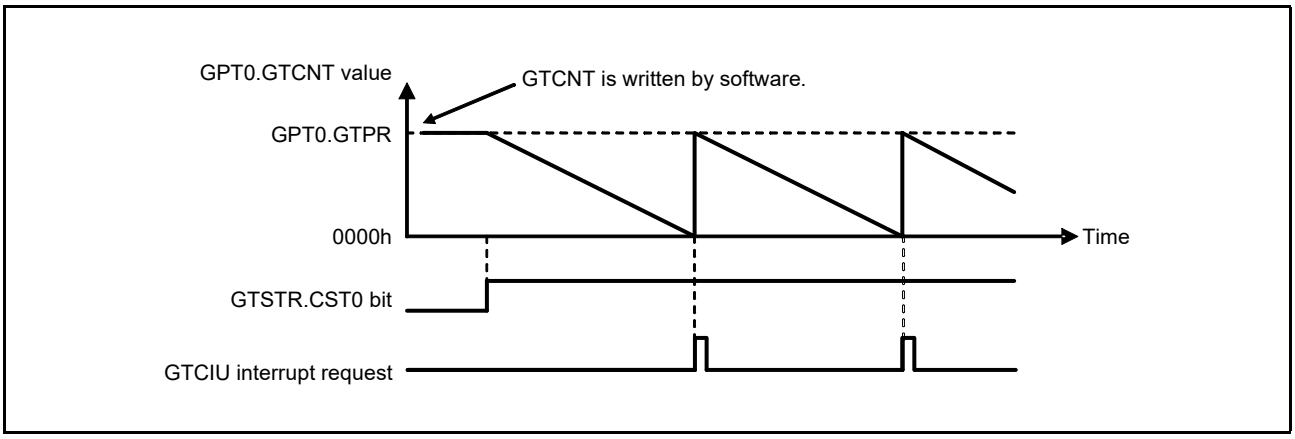


Figure 21.4 Example of Periodic Count Operation (in Down-Count Operation)

Figure 21.5 shows an example for setting periodic count operation in down-count operation.

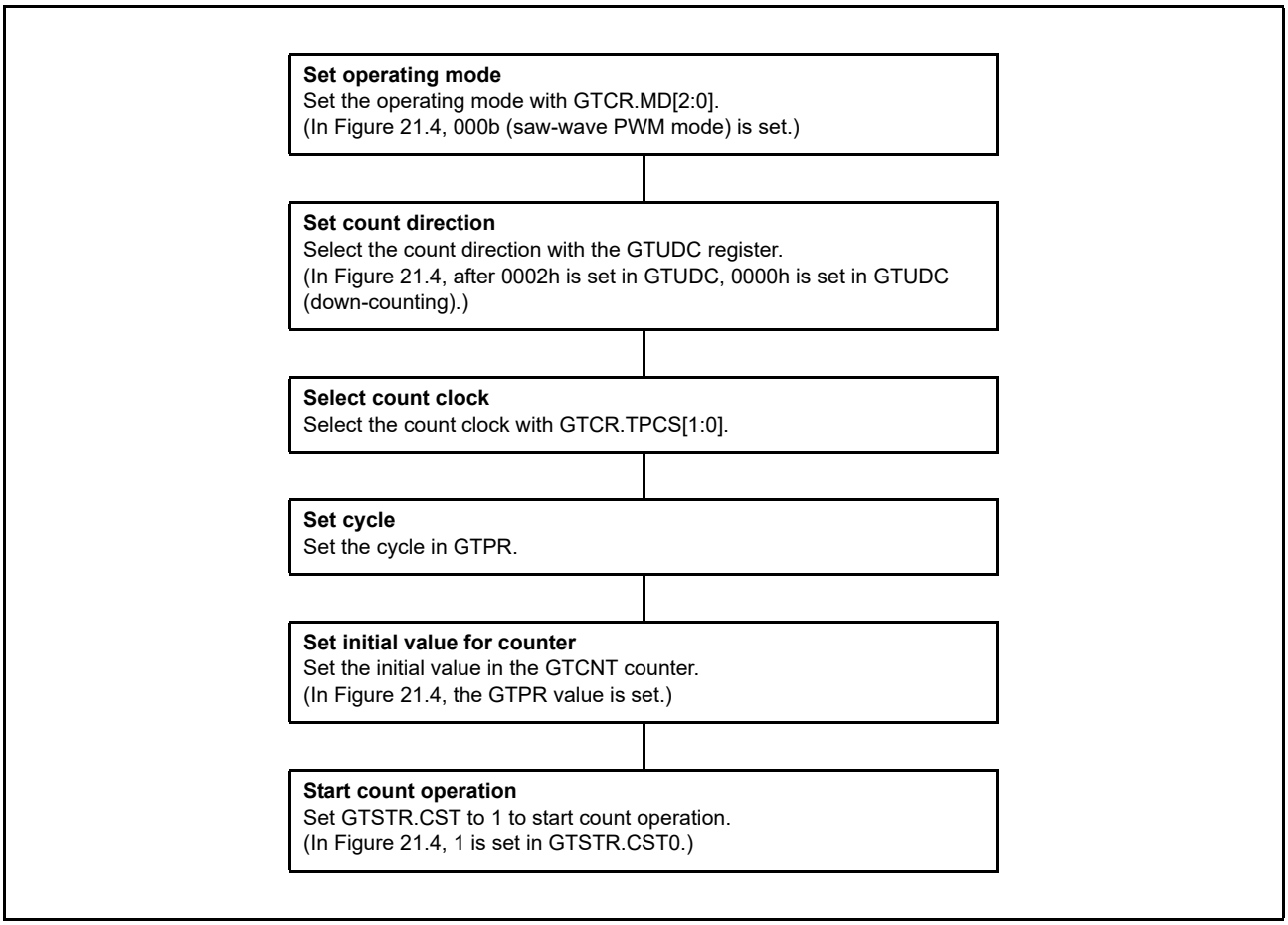


Figure 21.5 Example for Setting Periodic Count Operation (in Down-Count Operation)

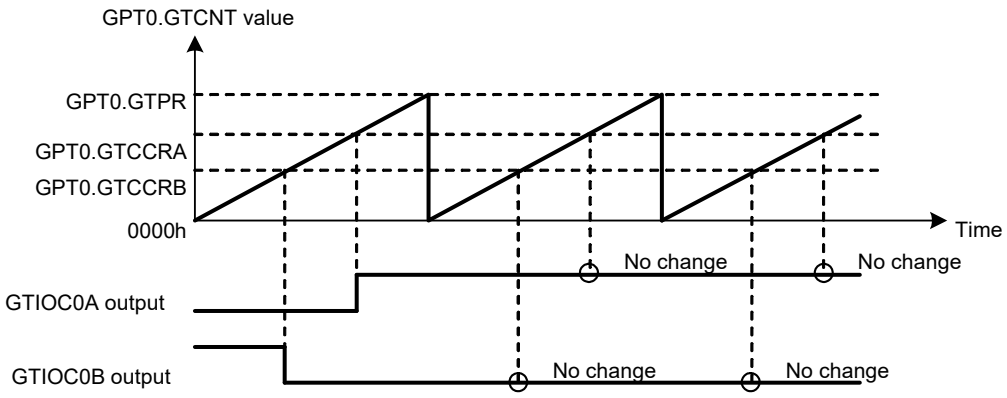
21.3.1.2 Waveform Output by Compare Match

When the GPTn.GTCNT counter value matches GTPn.GTCCRA or GTPn.GTCCRB, the GPT can output low or high or toggles output from the corresponding GTIOCnA or GTIOCnB output pin (n = 0 to 3).
In addition, the GTIOCnA or GTIOCnB pin output can be low, high, or toggled at the “cycle end” which is determined by GPTn.GTPR.
The cycle end is:

- For saw waves in up-count operation: When the GPTn.GTCNT counter value equals the GPTn.GTPR register value (overflow)
- For saw waves in down-count operation: When the GPTn.GTCNT counter value equals 0 (underflow)
- For triangle waves: When the GPTn.GTCNT counter value equals 0 (trough)

(1) Low Output and High Output

Figure 21.6 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.
In this example, up-count operation is performed in channel 0, and settings have been made so that high is output from the GTIOC0A pin by a GPT0.GTCCRA compare match, and low is output from the GTIOC0B pin by a GPT0n.GTCCRB compare match. The pin level does not change when the specified level and pin level match.



[Setting examples]
GPT0.GTIOR.GTIOA[5:0]: Initial output of 0, 1 output at compare match, output retained at cycle end
GPT0.GTIOR.GTIOB[5:0]: Initial output of 1, 0 output at compare match, output retained at cycle end

Figure 21.6 Example of Low Output and High Output Operation

Figure 21.7 shows an example for setting low output and high output operation.

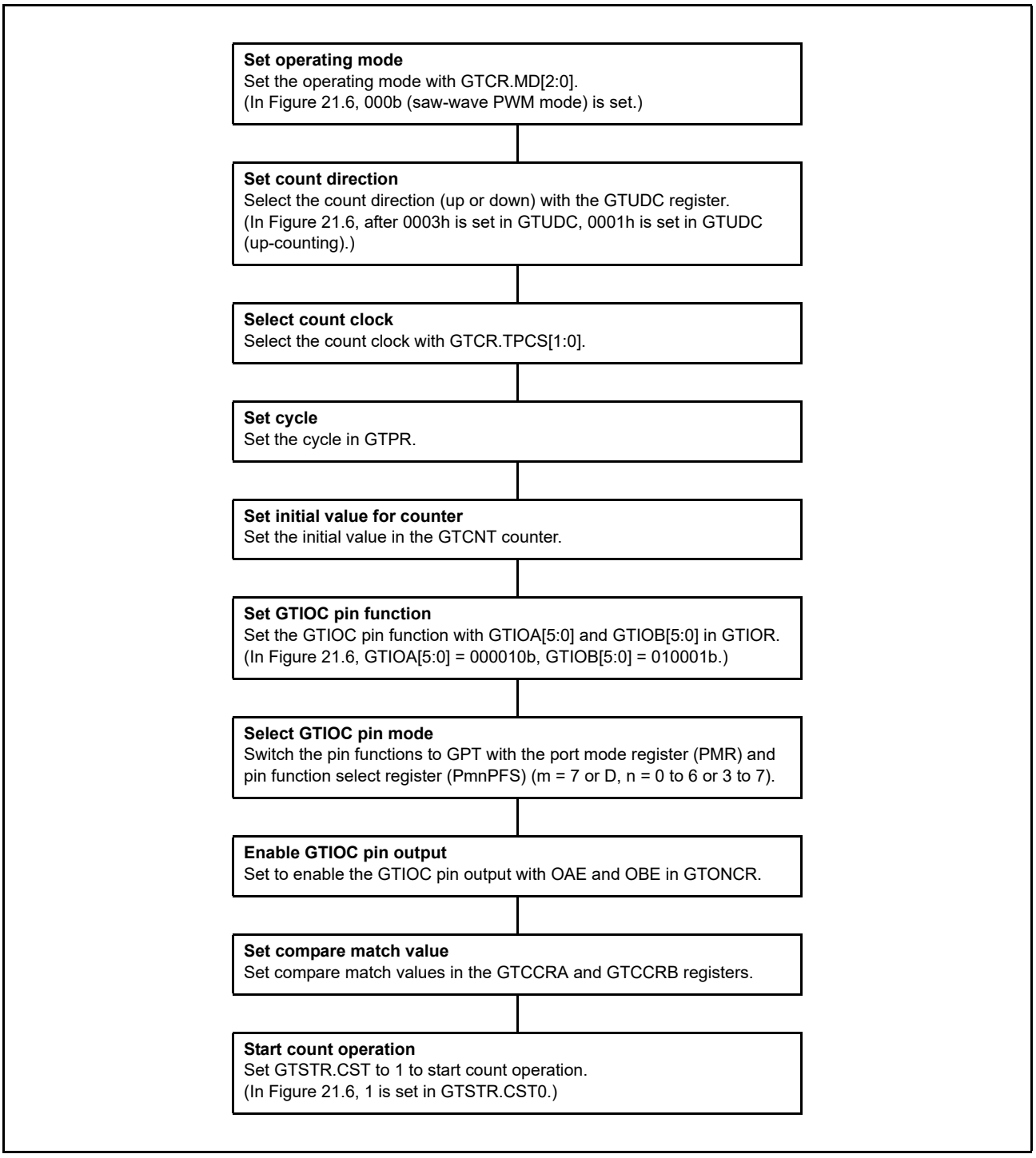
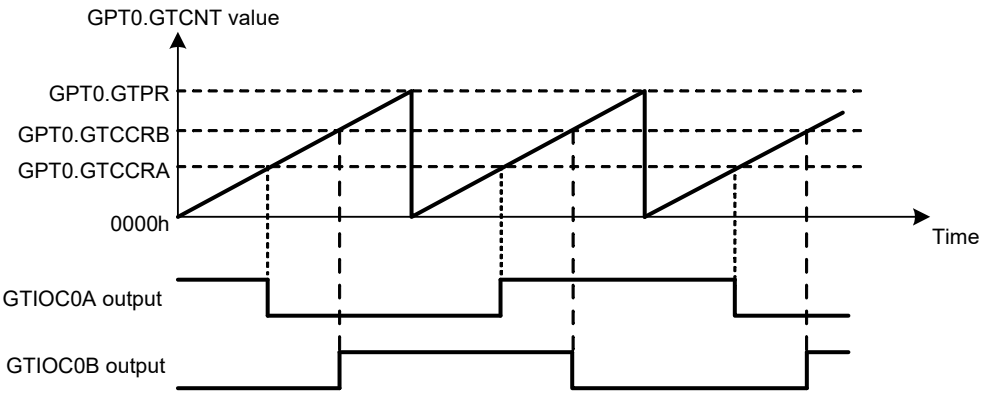


Figure 21.7 Example for Setting Low Output and High Output Operation

(2) Toggled Output

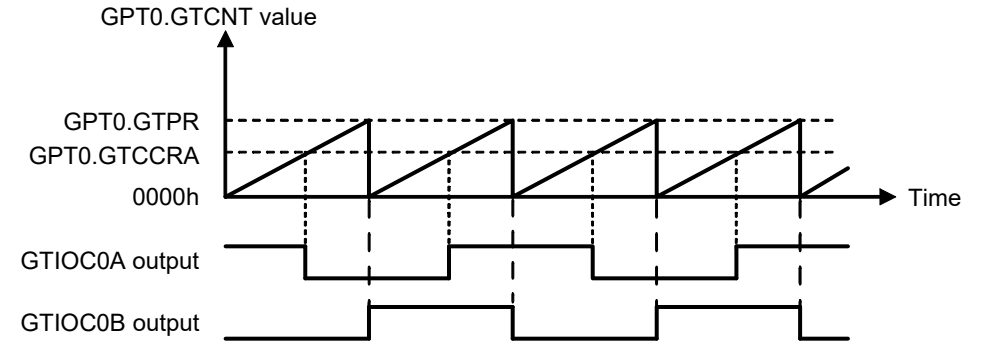
Figure 21.8 and Figure 21.9 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 21.8, up-count operation is performed in channel 0, and settings have been made so that the GTIOC0A pin output by a GPT0.GTCCRA compare match and GTIOC0B pin output by a GPT0n.GTCCRB compare match are toggled.

In Figure 21.9, up-count operation is performed in channel 0, and settings have been made so that the GTIOC0A output is toggled by a compare match of GPT0.GTCCRA and the GTIOC0B output is toggled at the cycle end.



[Setting examples]
GPT0.GTIOR.GTIOA[5:0]: Initial output of 1, toggle output at compare match, output retained at cycle end
GPT0.GTIOR.GTIOB[5:0]: Initial output of 0, toggle output at compare match, output retained at cycle end

Figure 21.8 Example of Toggled Output Operation (1)



[Setting examples]
GPT0.GTIOR.GTIOA[5:0]: Initial output of 1, toggle output at compare match, output retained at cycle end
GPT0.GTIOR.GTIOB[5:0]: Initial output of 0, output retained at compare match, toggle output at cycle end

Figure 21.9 Example of Toggled Output Operation (2)

Figure 21.10 shows an example for setting toggled output operation.

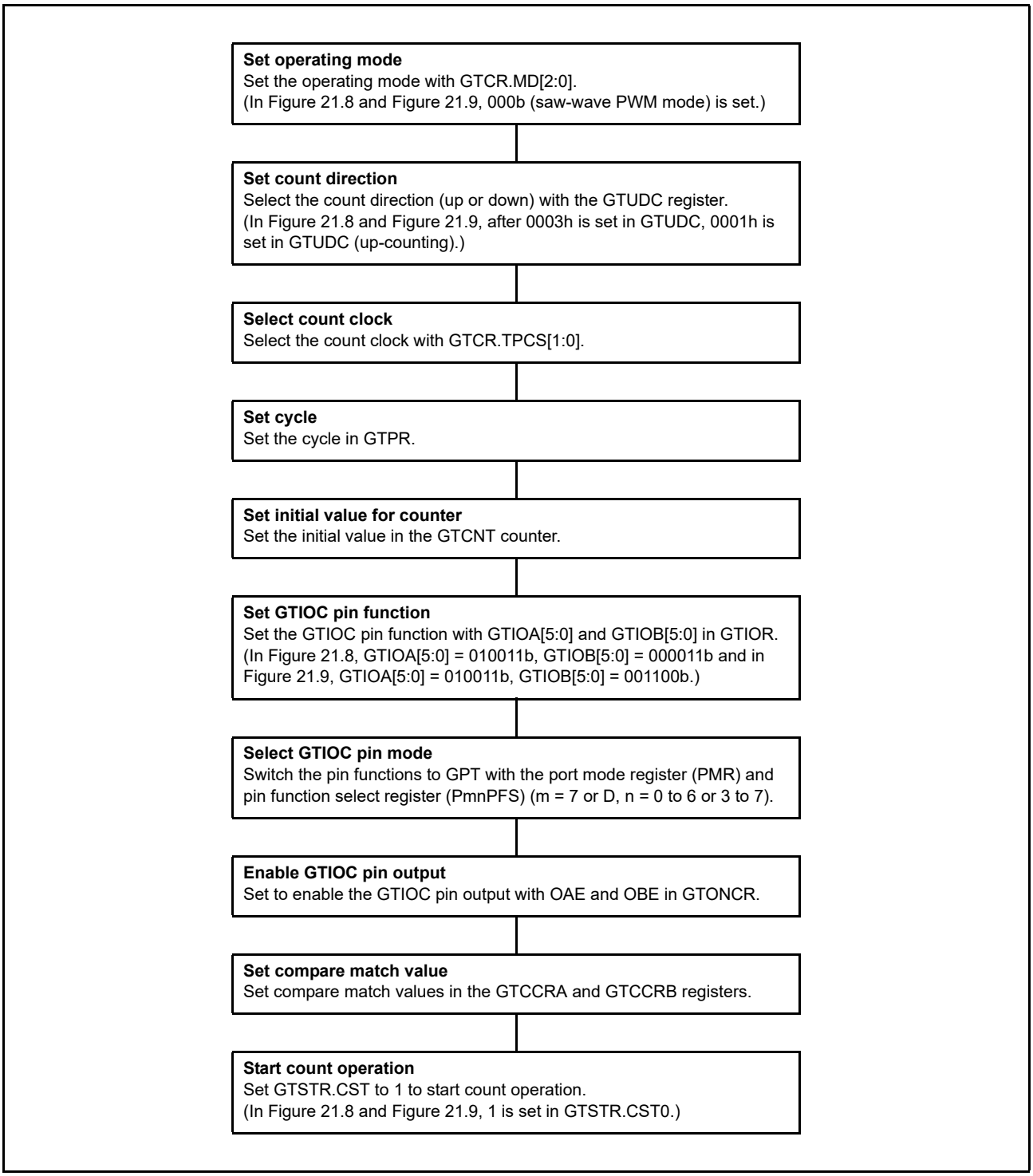


Figure 21.10 Example for Setting Toggled Output Operation

21.3.1.3 Input Capture Function

The GPTn.GTCNT counter value can be transferred to either GPTn.GTCCRA or GPTn.GTCCRB on detection of the input edge of the GTIOCnA input pin or GTIOCnB input pin, respectively (n = 0 to 3). The rising edge, falling edge, or both edges can be selected as the detection edge.

Figure 21.11 shows an example of the input capture function. In this example, up-count operation is performed on channel 0, and settings have been made so that an input capture is performed at both edges of the GTIOC0A input pin and at the rising edge of the GTIOC0B input pin.

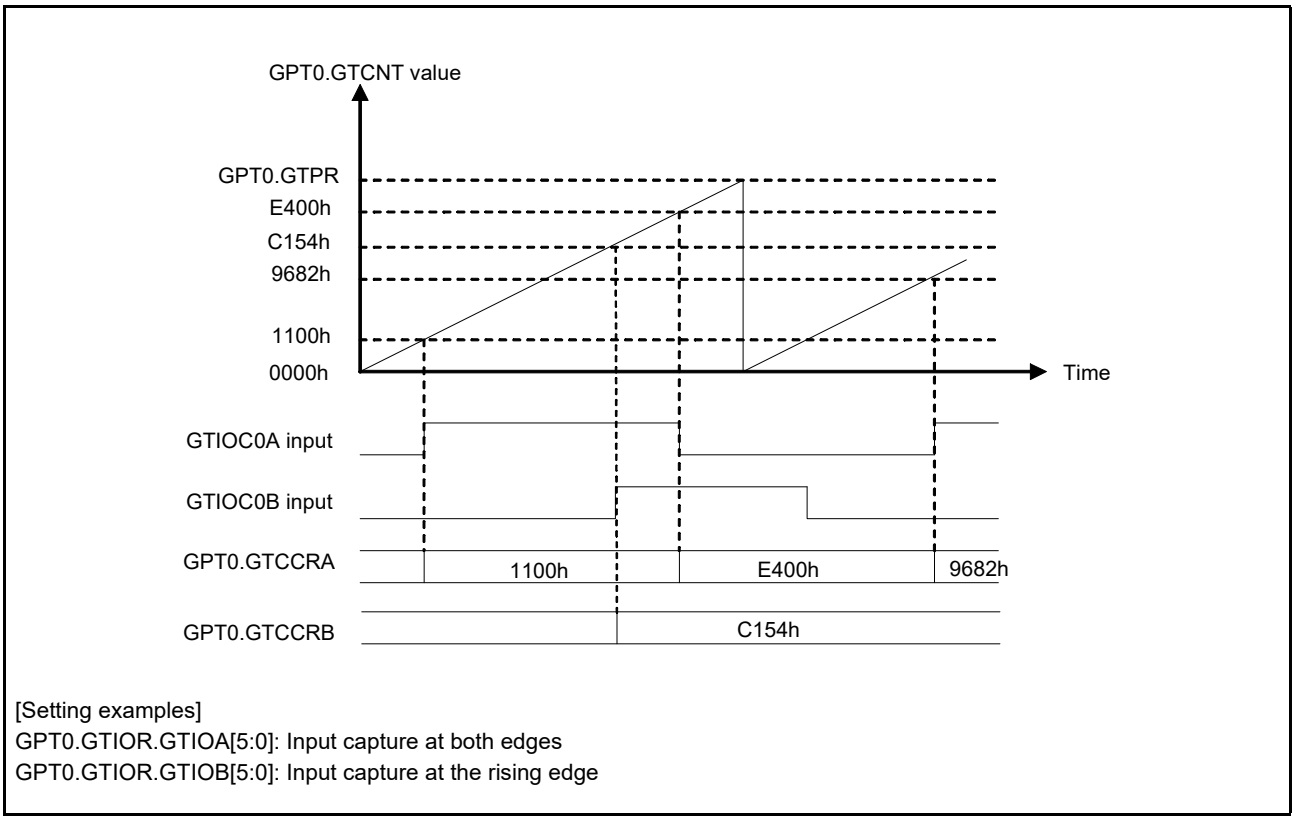


Figure 21.11 Example of Input Capture Operation

Figure 21.12 shows an example for setting input capture operation.

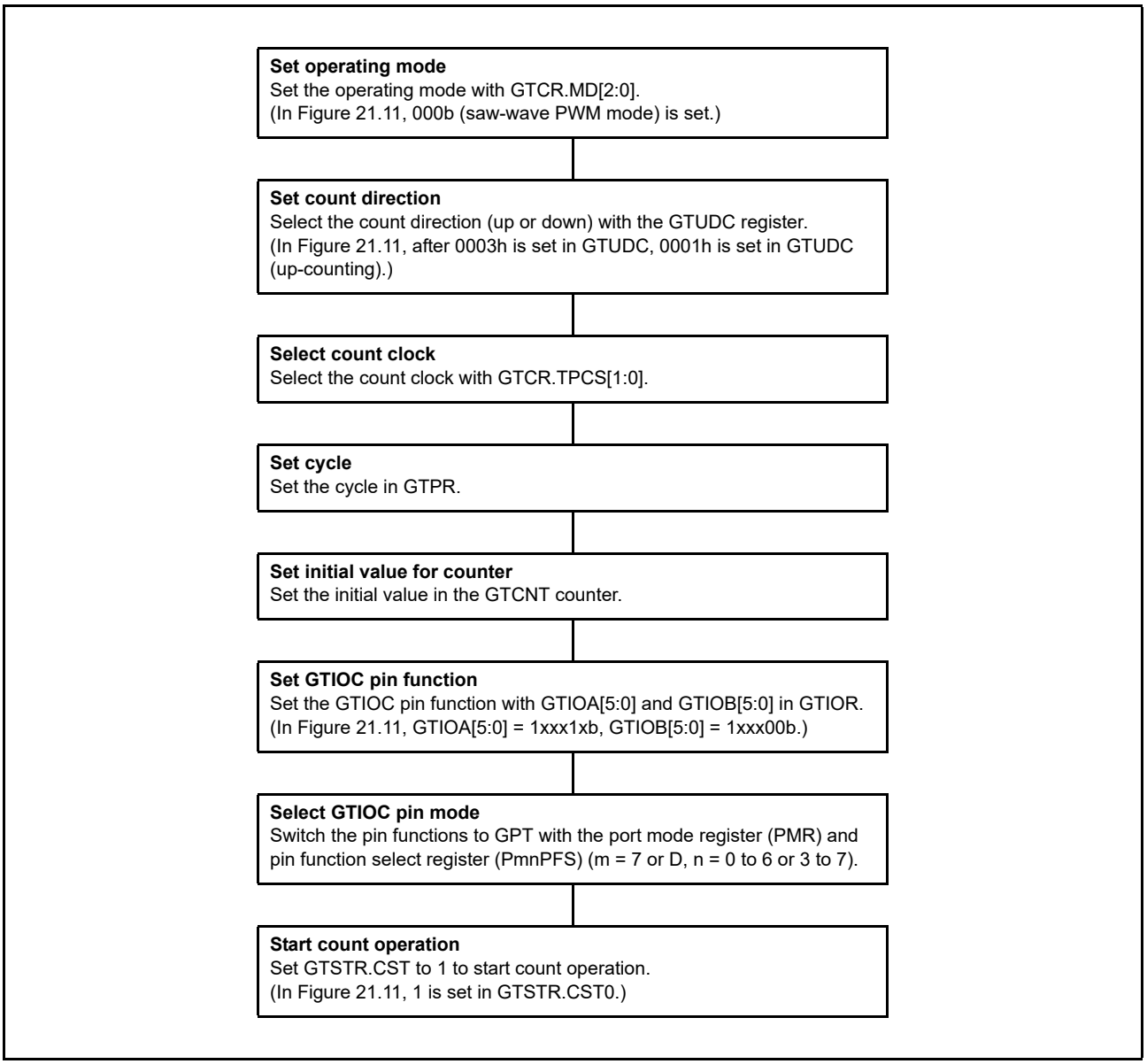


Figure 21.12 Example for Setting Input Capture Operation

21.3.2 Buffer Operation

The following buffer operation can be set with GTBER.

- Buffer operation with GTCCRA, GTCCRC, and GTCCRD used together
- Buffer operation with GTCCRB, GTCCRE, and GTCCRF used together
- Buffer operation with GTPR, GTPBR, and GTPDBR used together
- Buffer operation with GTADTRA, GTADTBRA, and GTADTDBRA used together
- Buffer operation with GTADTRB, GTADTBRB, and GTADTDBRB used together

The following buffer operation can be set with GTDTCR.

- Buffer operation with GTDVU and GTDBU used together
- Buffer operation with GTDVU and GTDBD used together

21.3.2.1 GTPR Register Buffer Operation

GTPBR can function as a buffer register for GTPR, and GTPCBR can function as a buffer register for GTPBR (double-buffer register for GTPR).
The buffer transfer is performed at an overflow (during up-count operation) or an underflow (during down-count operation) in saw-wave mode, and at a trough in triangle-wave mode.
To set GTPR to function as double buffer, set GTBER.PR[1:0] to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.
When the direction of counting is down in saw-wave mode, the setting to select buffered operation is prohibited. Transfer from the buffer proceeds on overflow and clearing of the counter in saw-wave mode, and at troughs in triangle-wave mode.
Figure 21.13 and Figure 21.14 show examples of GTPR buffer operation and Figure 21.15 shows an example for setting GTPR buffer operation.

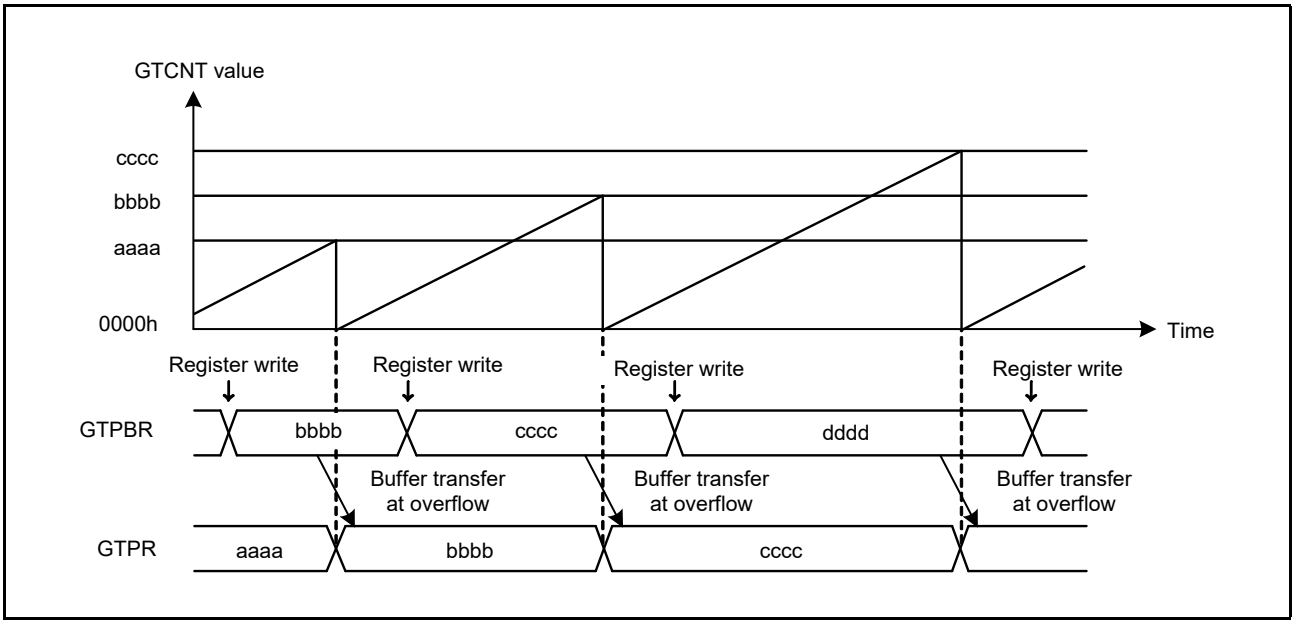


Figure 21.13 Example of GTPR Buffer Operation (Saw Waves in Up-Count Operation)

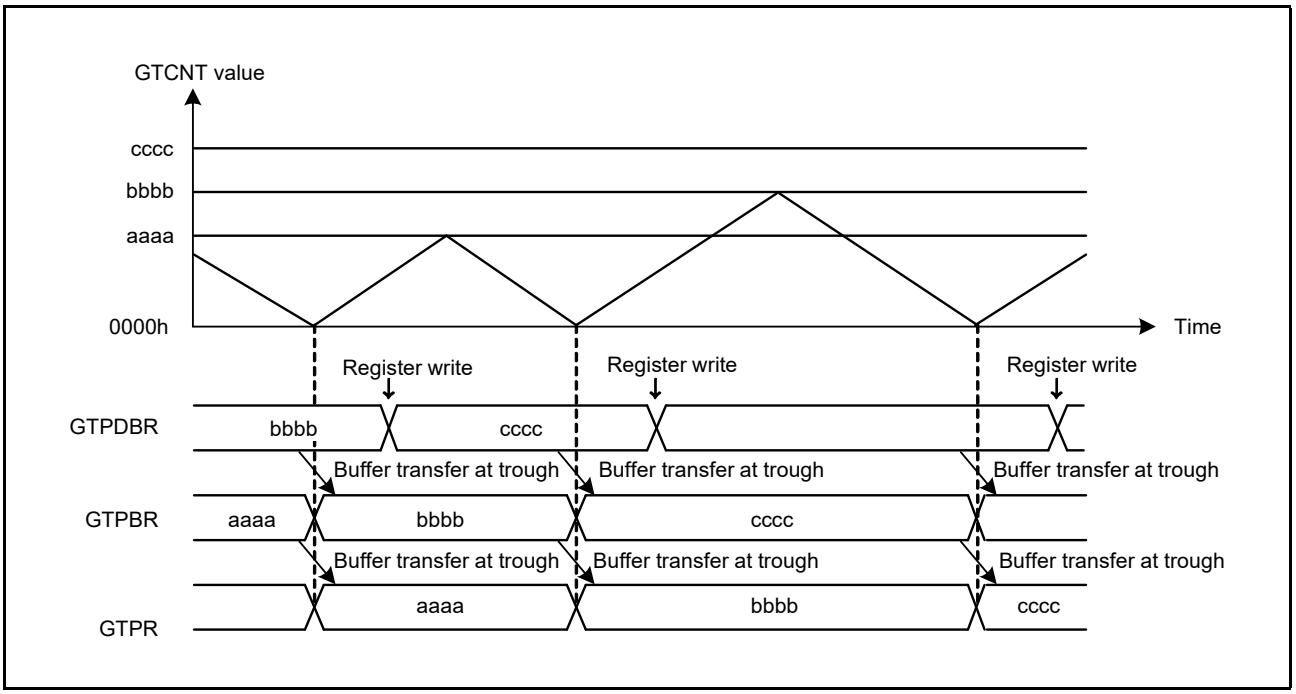


Figure 21.14 Example of GTPR Double Buffer Operation (Triangle Waves)

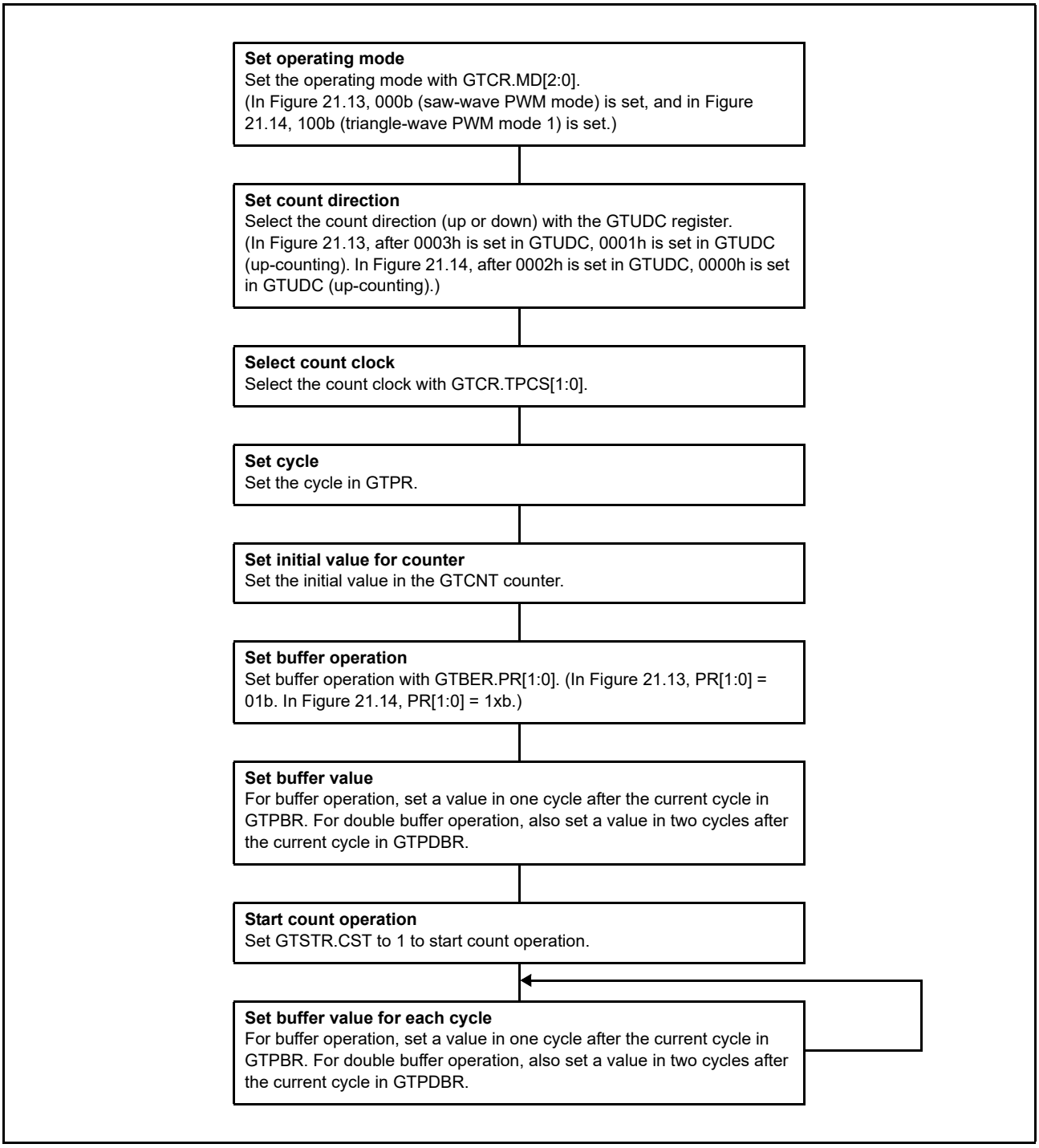


Figure 21.15 Example for Setting GTPR Buffer Operation

21.3.2.2 Buffer Operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).
To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single buffer operation, set 01b. Not to function as buffer, set 00b.

(1) When GTCCRA or GTCCRB Functions as Output Compare Register

Buffer transfer is performed at an overflow (during up-count operation) or an underflow (during down-count operation) in saw-wave mode, and at a trough in triangle-wave mode.
Figure 21.16 to Figure 21.18 show examples of GTCCRA and GTCCRB buffer operation and Figure 21.19 shows an example for setting GTCCRA and GTCCRB buffer operation.

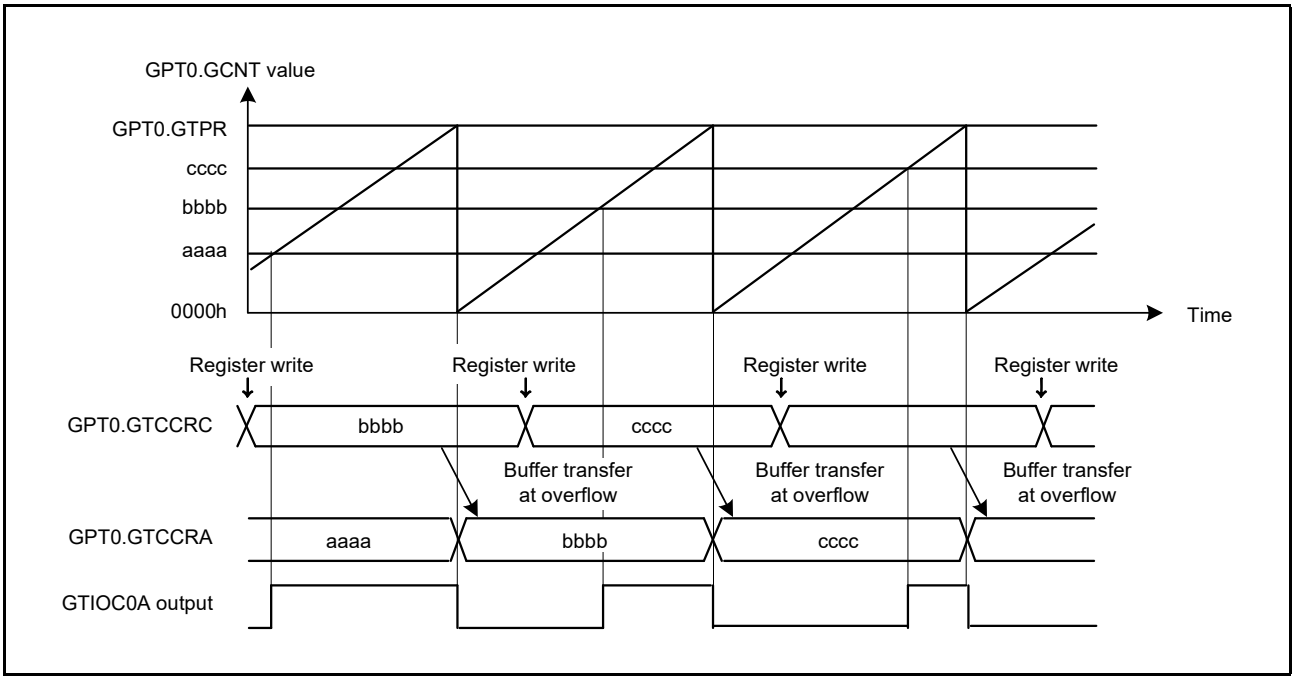


Figure 21.16 Example of GTCCRA and GTCCRB Buffer Operation (Output Compare, Saw Waves in Up-Count Operation, High Output at GTCCRA Compare Match, Low Output at Cycle End)

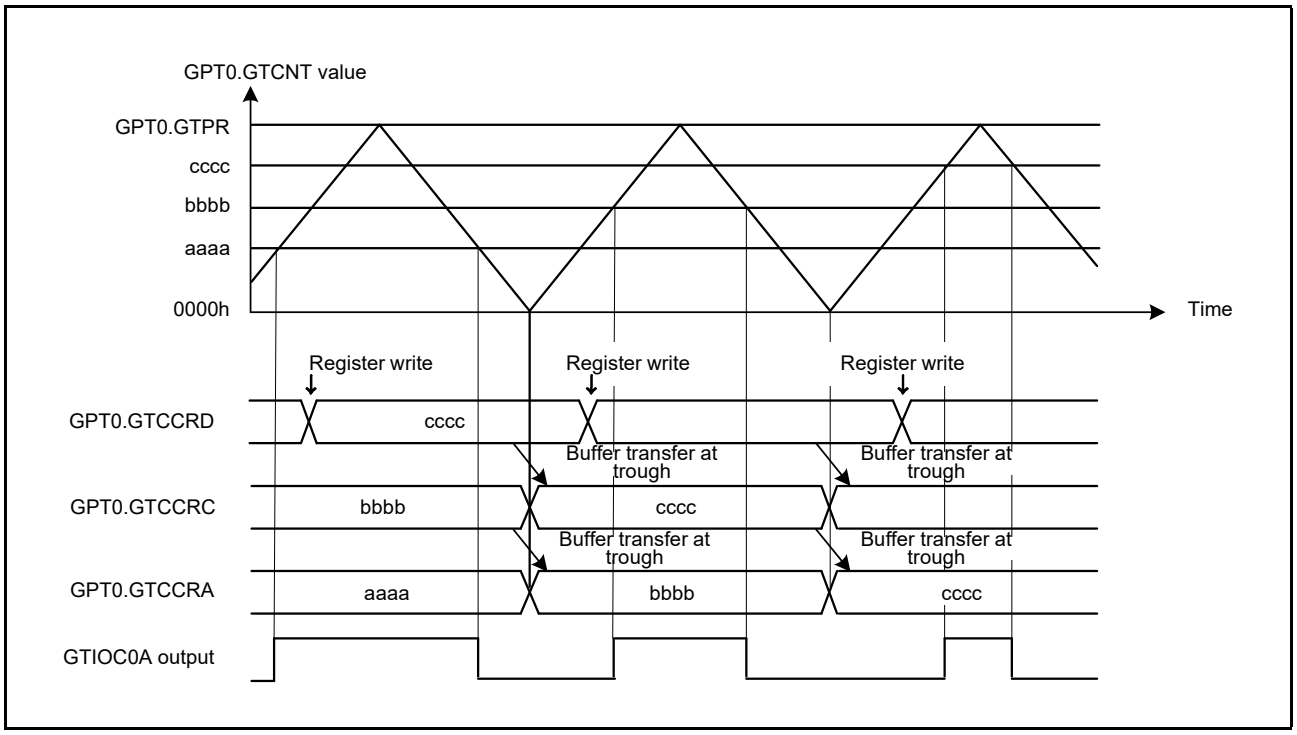


Figure 21.17 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Trough, Toggle Output at GTCCRA Compare Match, Output Retained at Cycle End)

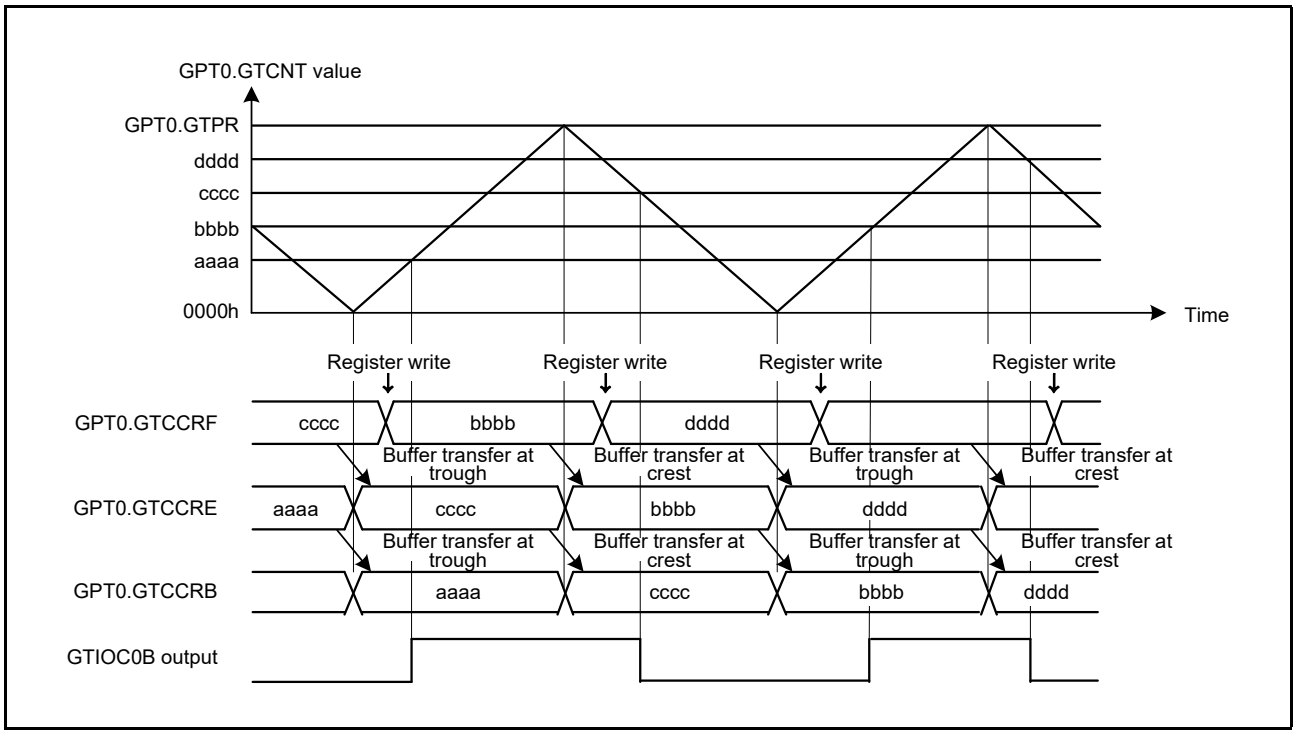


Figure 21.18 Example of GTCCRA and GTCCRB Double Buffer Operation (Output Compare, Triangle Waves, Buffer Operation at Both Troughs and Crests, Toggle Output at GTCCRB Compare Match, Output Retained at Cycle End)

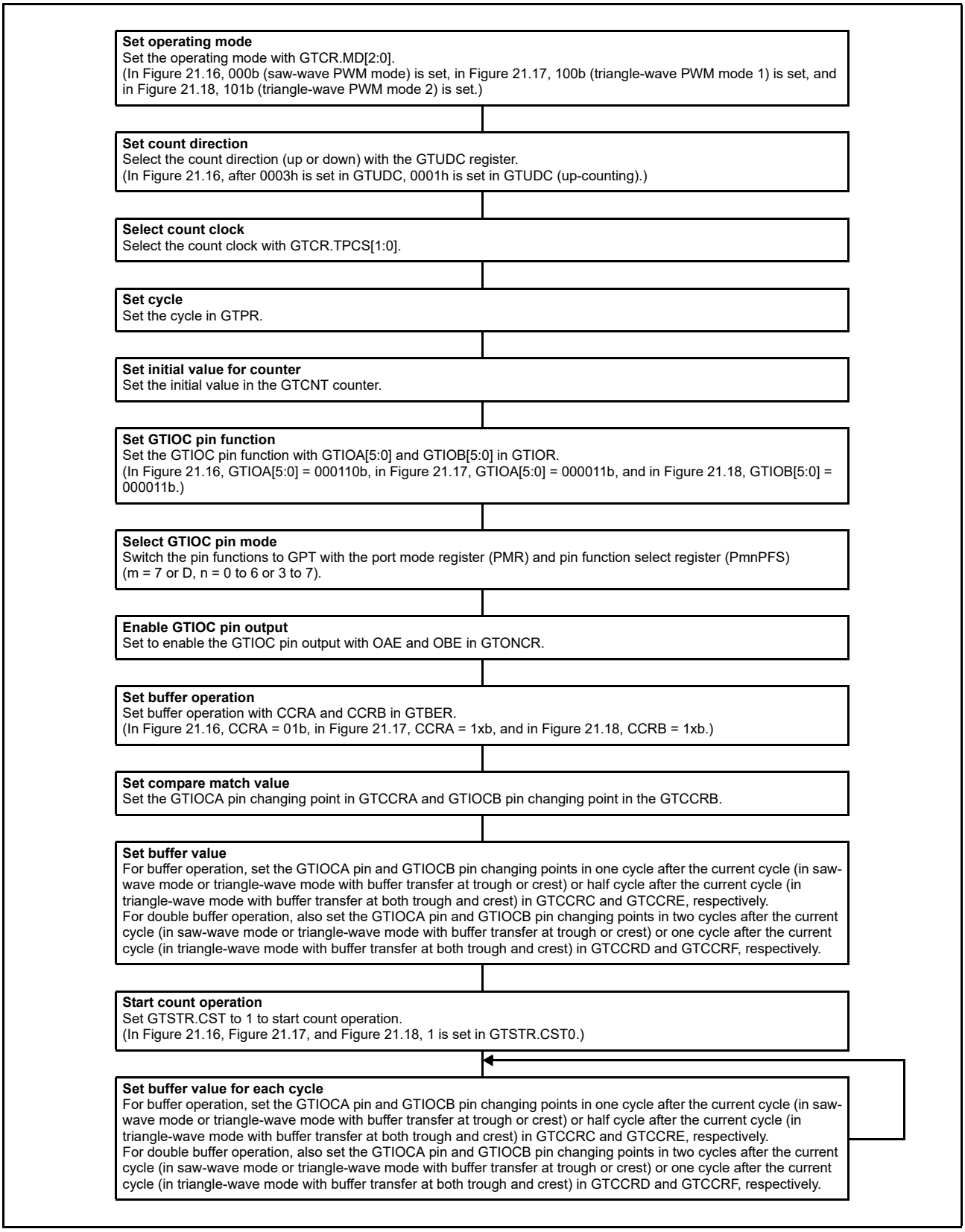


Figure 21.19 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Output Compare)

(2) When GTCCRA or GTCCRB Functions as Input Capture Register

Buffer transfer is performed at a point when an input capture is generated. When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to buffer registers.

Figure 21.20 and Figure 21.21 show examples of GTCCRA and GTCCRB buffer operation and Figure 21.22 shows an example for setting GTCCRB buffer operation.

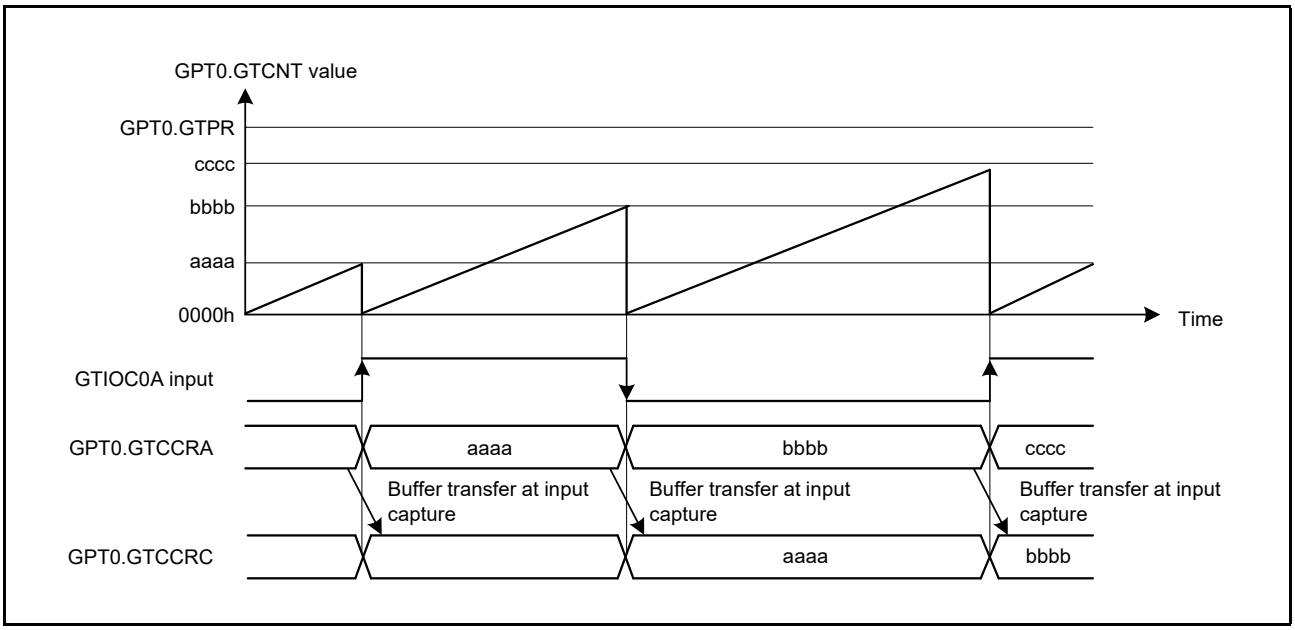


Figure 21.20 Example of GTCCRA and GTCCRB Buffer Operation (Input Capture at Both Edges of GTIOC0A Input, Saw Waves in Up-Count Operation, GTCNT Counter Cleared at GTCCRA Input Capture)

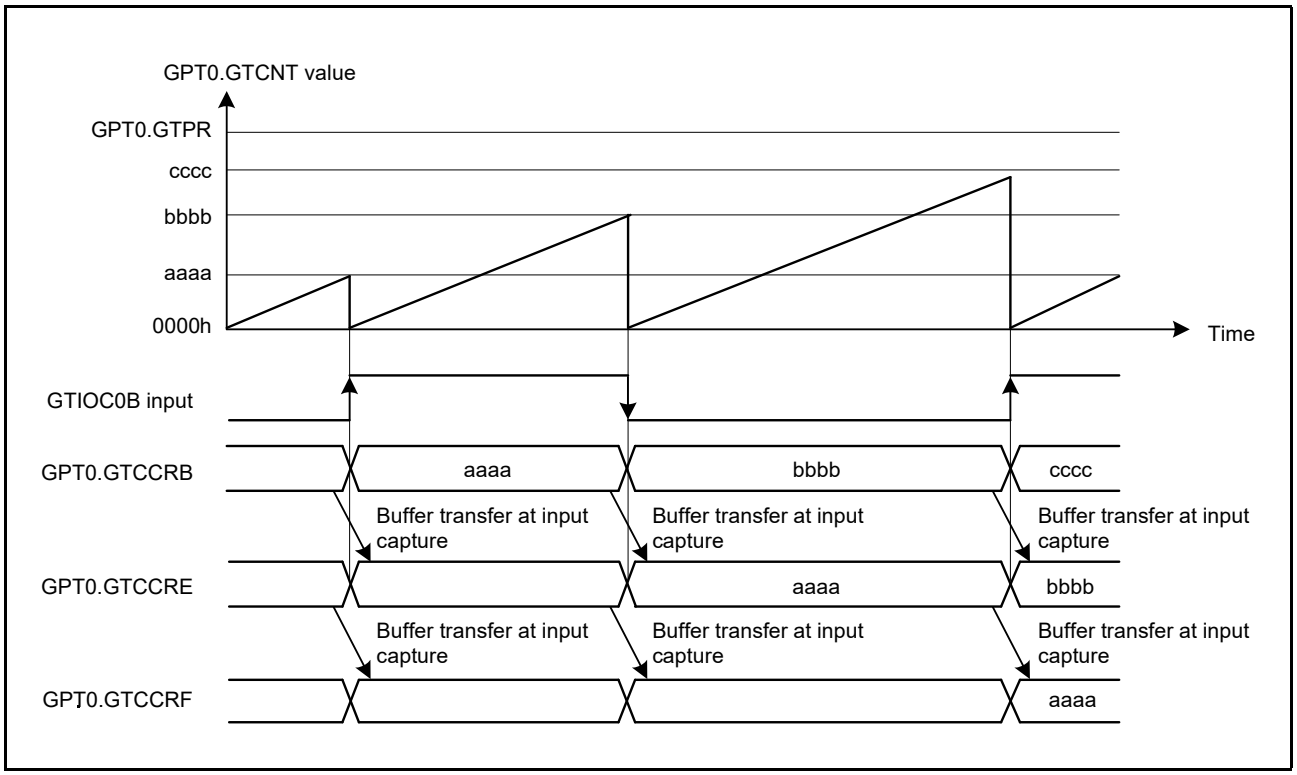


Figure 21.21 Example of GTCCRA and GTCCRB Double Buffer Operation (Input Capture at Both Edges of GTIOC0B Input, Saw Waves in Up-Count Operation, GTCNT Counter Cleared at GTCCRB Input Capture)

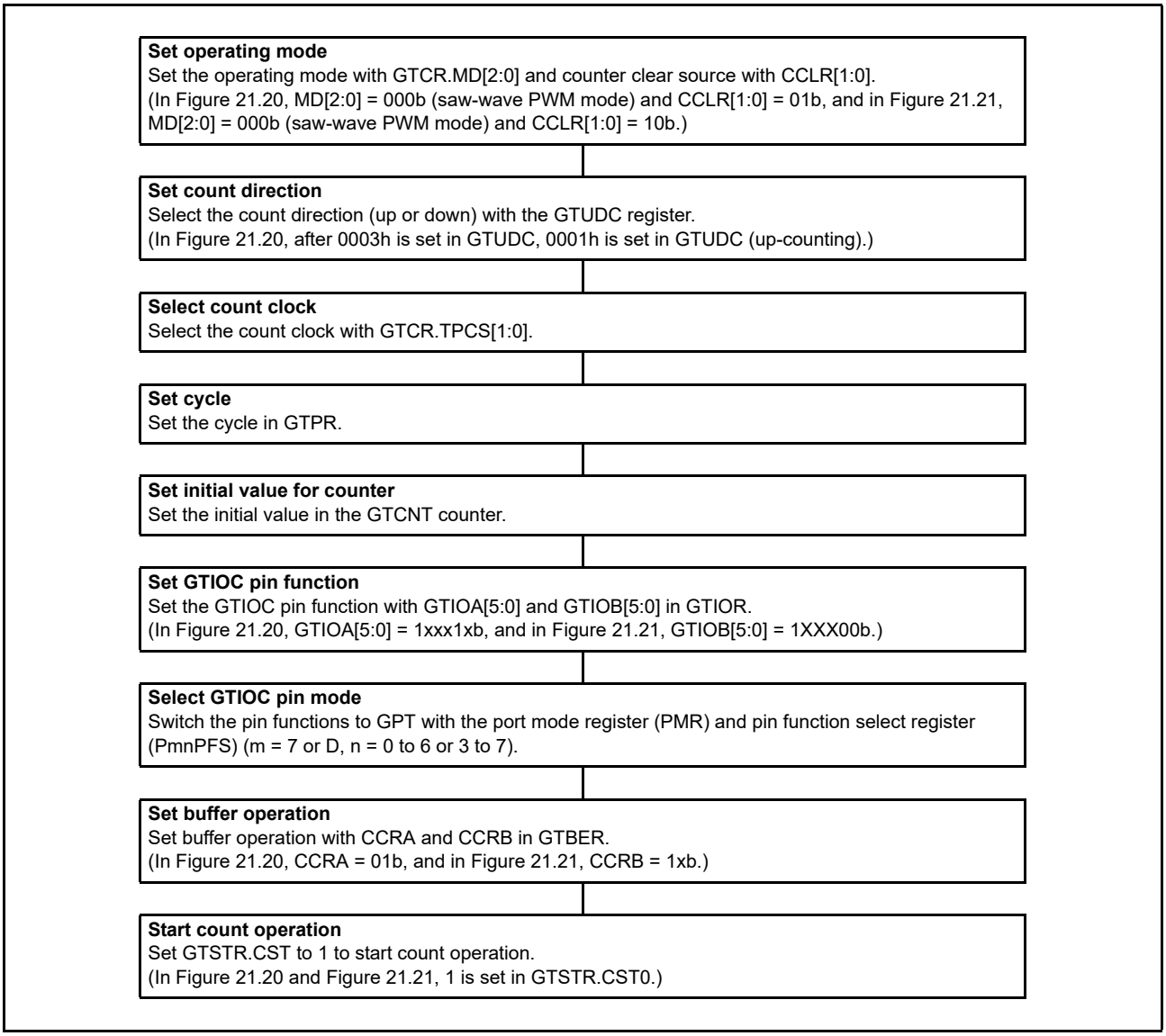


Figure 21.22 Example for Setting GTCCRA and GTCCRB Buffer Operation (for Input Capture)

21.3.2.3 Buffer Operation for GTADTRA and GTADTRB

GTADTBRA can function as the GTADTRA buffer register and GTADTDBRA can function as the GTADTBRA buffer register (double-buffer register for GTADTRA). Similarly, GTADTBRB can function as the GTADTRB buffer register and GTADTDBRB can function as the GTADTBRB buffer register (double-buffer register for GTADTRB).
To set GTADTRA or GTADTRB to function as a double buffer, set GTBER.ADTDA or GTBER.ADTDB to 1. For single buffer operation, set 0. Not to function as buffer, set GTBER.ADTTA[1:0] or GTBER.ADTTB[1:0] to 00b.
The buffer transfer timing can be set with the GTBER.ADTTA[1:0] bits. For saw waves, overflows (during up-count operation) or underflows (during down-count operation) can be selected. For triangle waves, crests are selected when GTBER.ADTTA[1:0] = 01b, troughs are selected when GTBER.ADTTA[1:0] = 10b, and both crests and troughs are selected when GTBER.ADTTA[1:0] = 11b.
Figure 21.23 to Figure 21.25 show examples of GTADTRA and GTADTRB buffer operation and Figure 21.26 shows an example for setting GTDTRA and GTADTRB buffer operation.

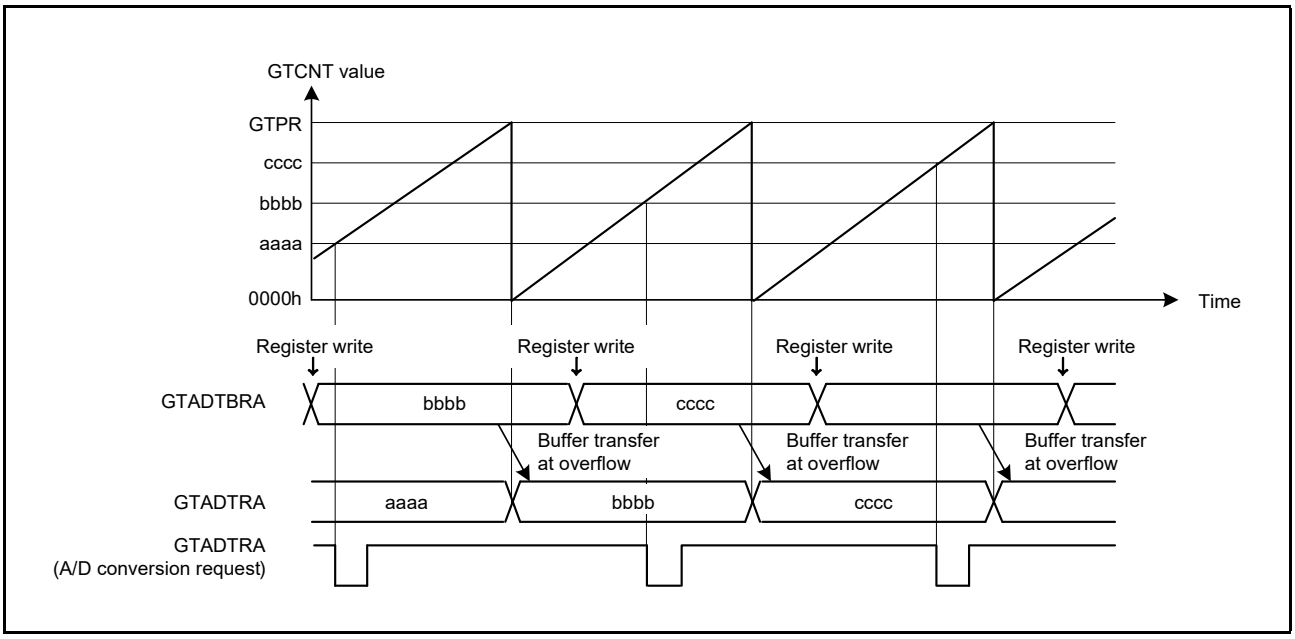


Figure 21.23 Example of GTADTRA and GTADTRB Buffer Operation (Saw Waves in Up-Count Operation, A/D Converter Start Request Generated by Up-Counting)

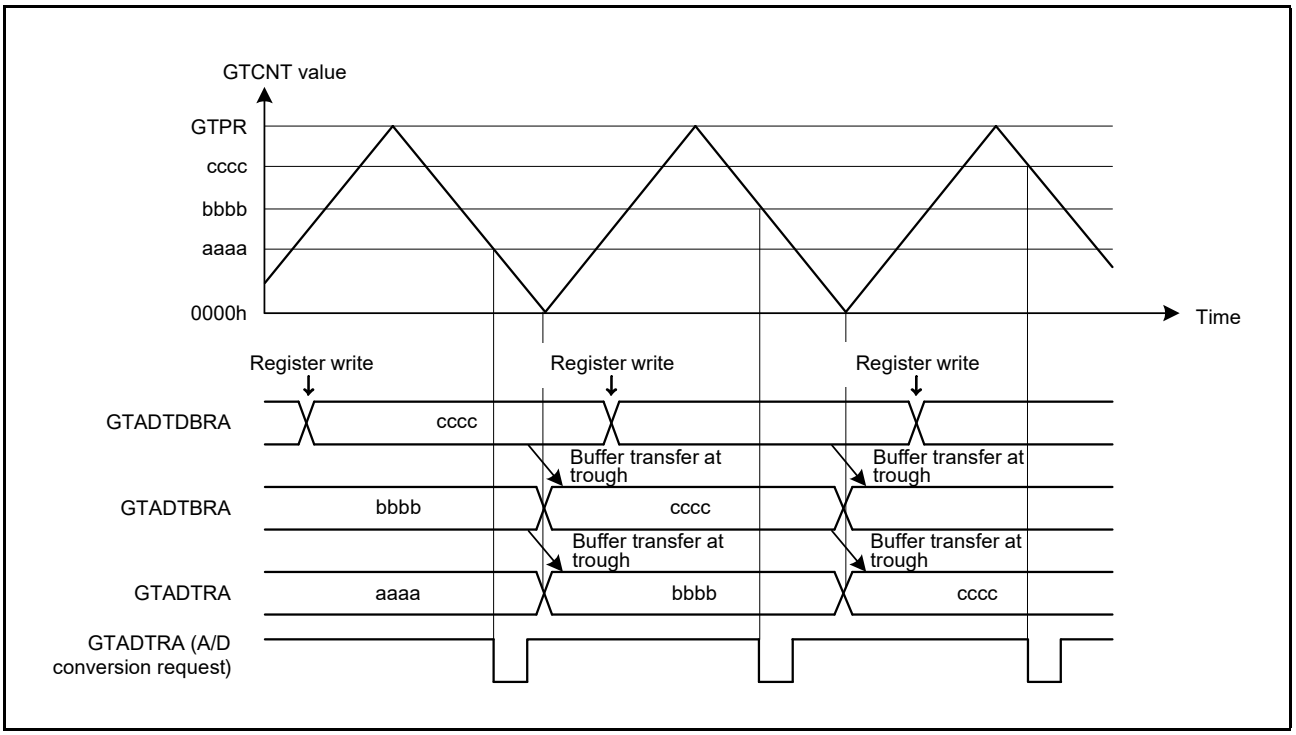


Figure 21.24 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Troughs, A/D Converter Start Request Generated by Down-Counting)

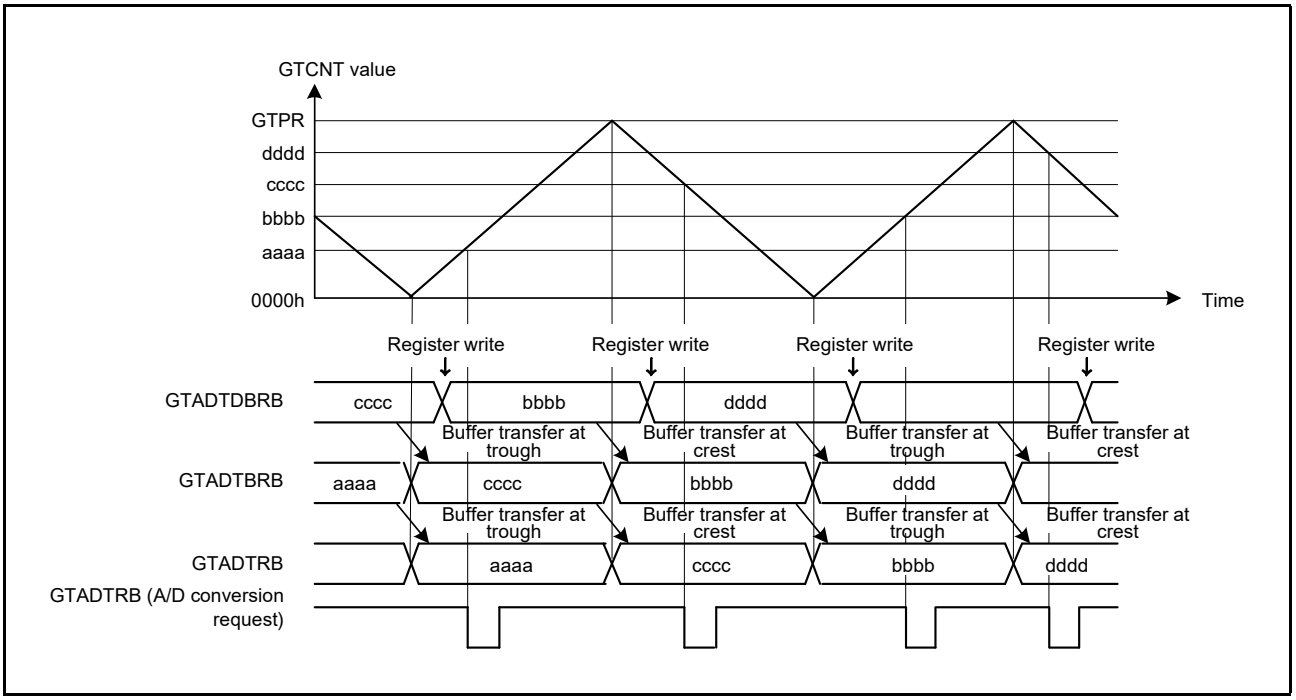


Figure 21.25 Example of GTADTRA and GTADTRB Double Buffer Operation (Triangle Waves, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Request Generated by Both Up- and Down-Counting)

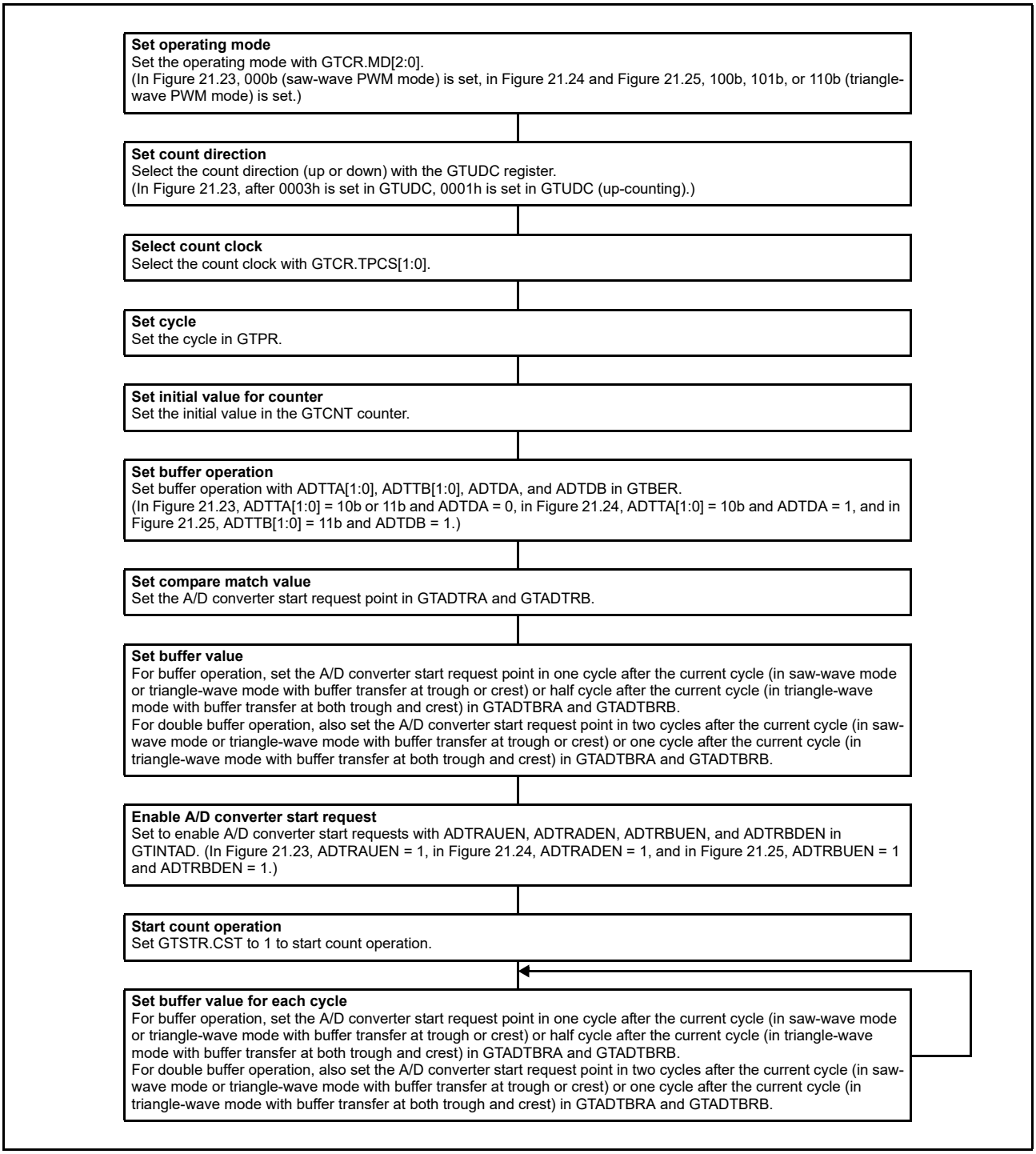


Figure 21.26 Example for Setting GTADTRA and GTADTRB Buffer Operation

21.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCnA pin or GTIOCnB pin by a compare match between the GPTn.CTCNT counter and GPTn.GTCCRA or GPTn.GTCCRB (n = 0 to 3). An operating mode can be set independently for each channel, and synchronized operation on channels is also possible.
By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

(1) Saw-Wave PWM Mode (GTCR.MD = 000b)

In saw-wave PWM mode, GPTn.GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n = 0 to 3). The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting
Figure 21.27 shows an example of saw-wave PWM mode operation, and Figure 21.28 shows an example for setting saw-wave PWM mode.

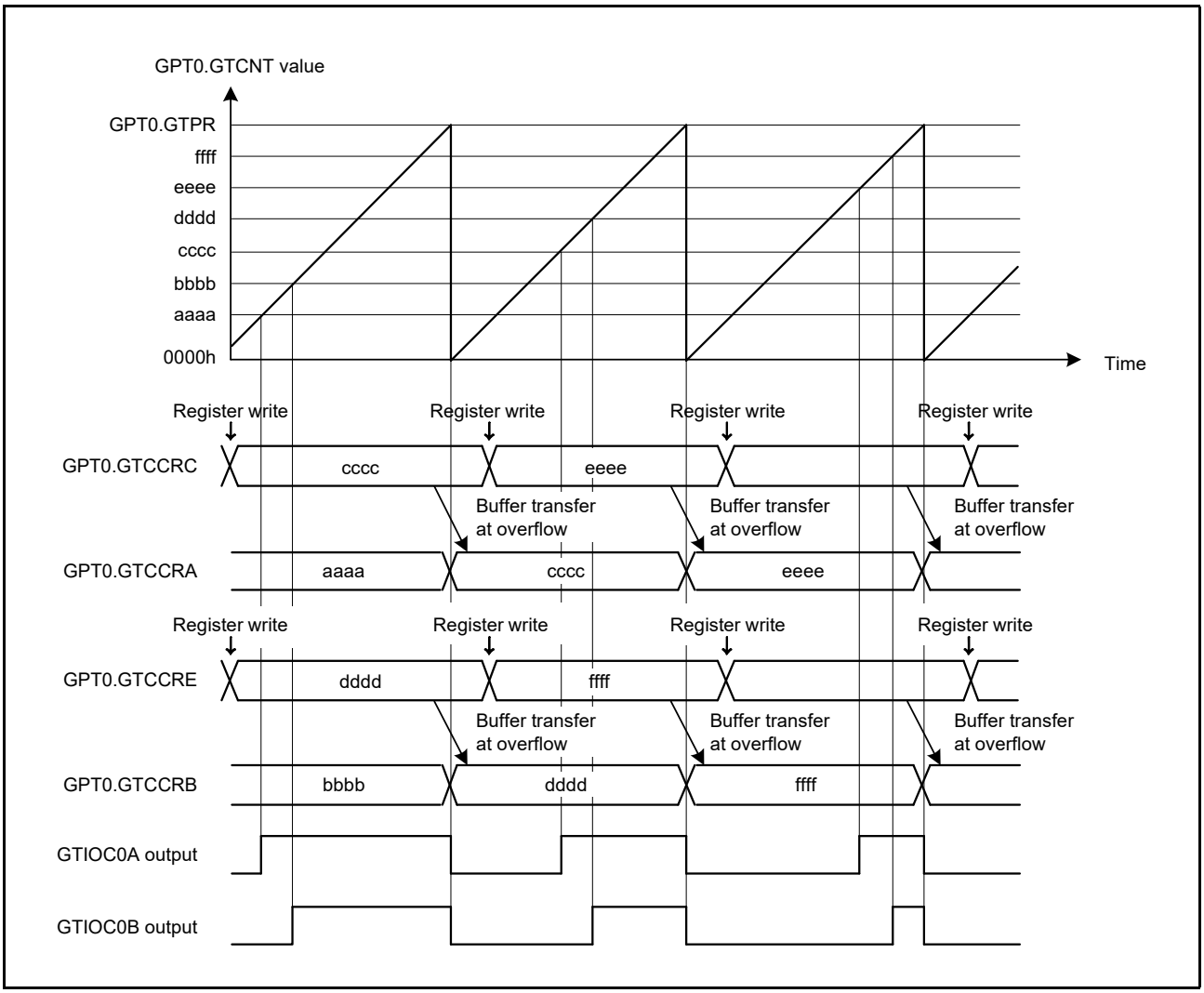


Figure 21.27 Example of Saw-Wave PWM Mode Operation (Up-Count Operation, Buffer Operation, High Output at GTCCRA/GTCCRB Compare Match, Low Output at Cycle End)

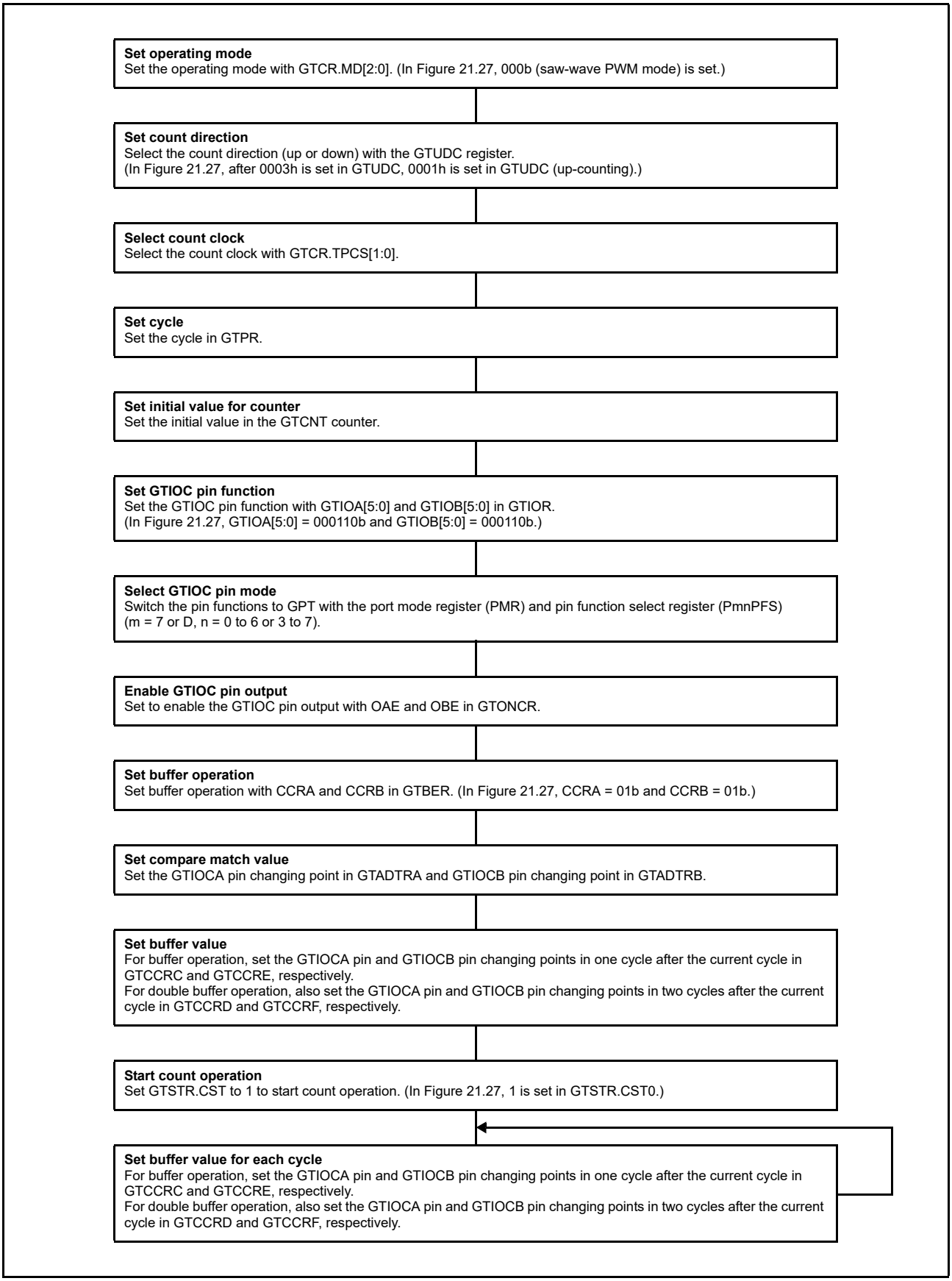


Figure 21.28 Example for Setting Saw-Wave PWM Mode

(2) Saw-Wave One-Shot Pulse Mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of GPTn.GTCCRA or GPTn.GTCCRB with buffer operation fixed (n = 0 to 3).

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from GTCCRC to GTCCRA, from GTCCRE to GTCCRB, from GTCCRD to temporary register A, and from GTCCRF to temporary register B at the cycle end, and from temporary register A to GTCCRA at a GTCCRA compare match and from temporary register B to GTCCRB at a GTCCRB compare match. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting.

By setting GTDTCR, GTCVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.29 shows an example of saw-wave one-shot pulse mode operation, and Figure 21.30 shows an example for setting saw-wave one-shot pulse mode.

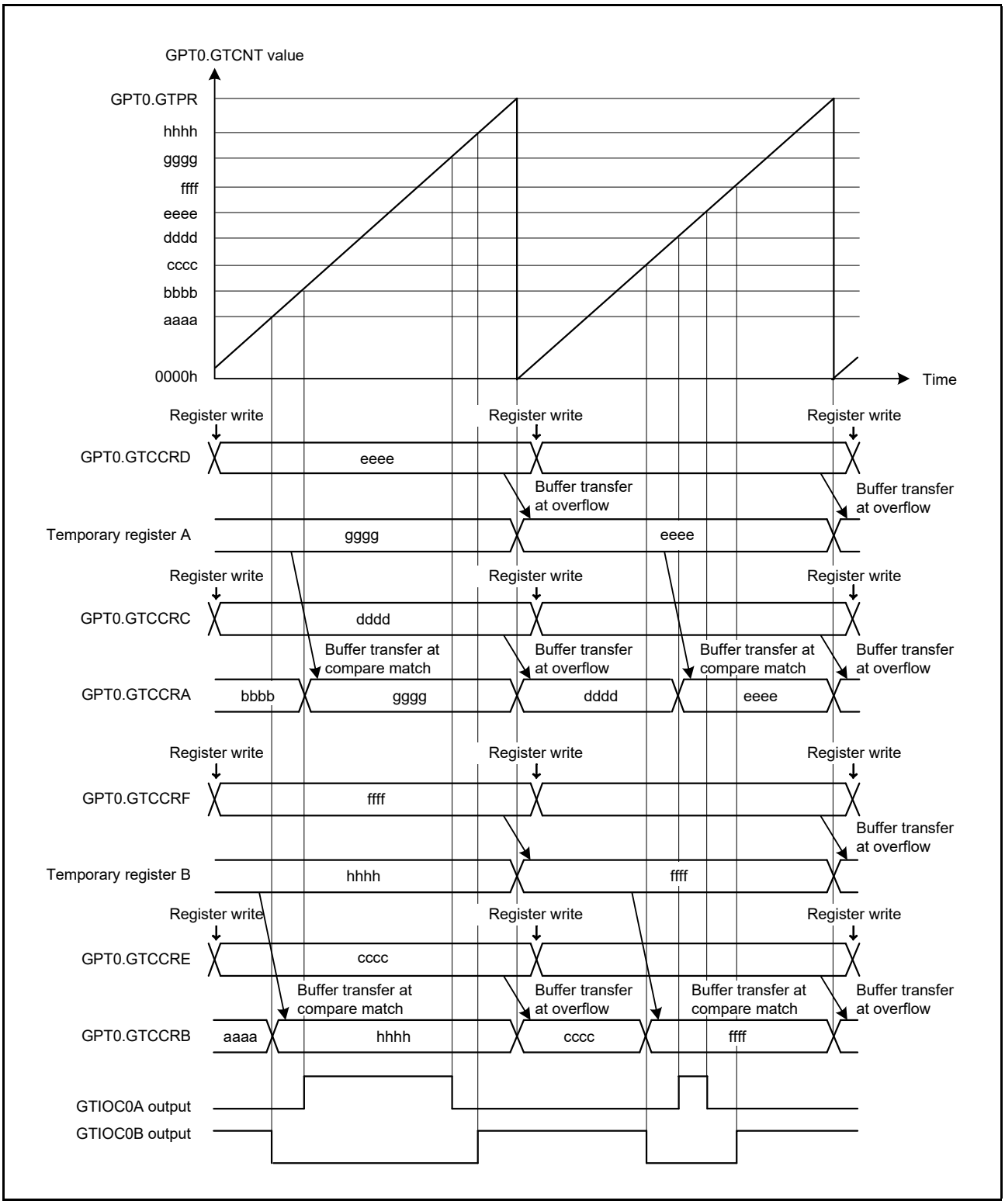


Figure 21.29 Example of Saw-Wave One-Shot Pulse Mode Operation (Up-Count Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

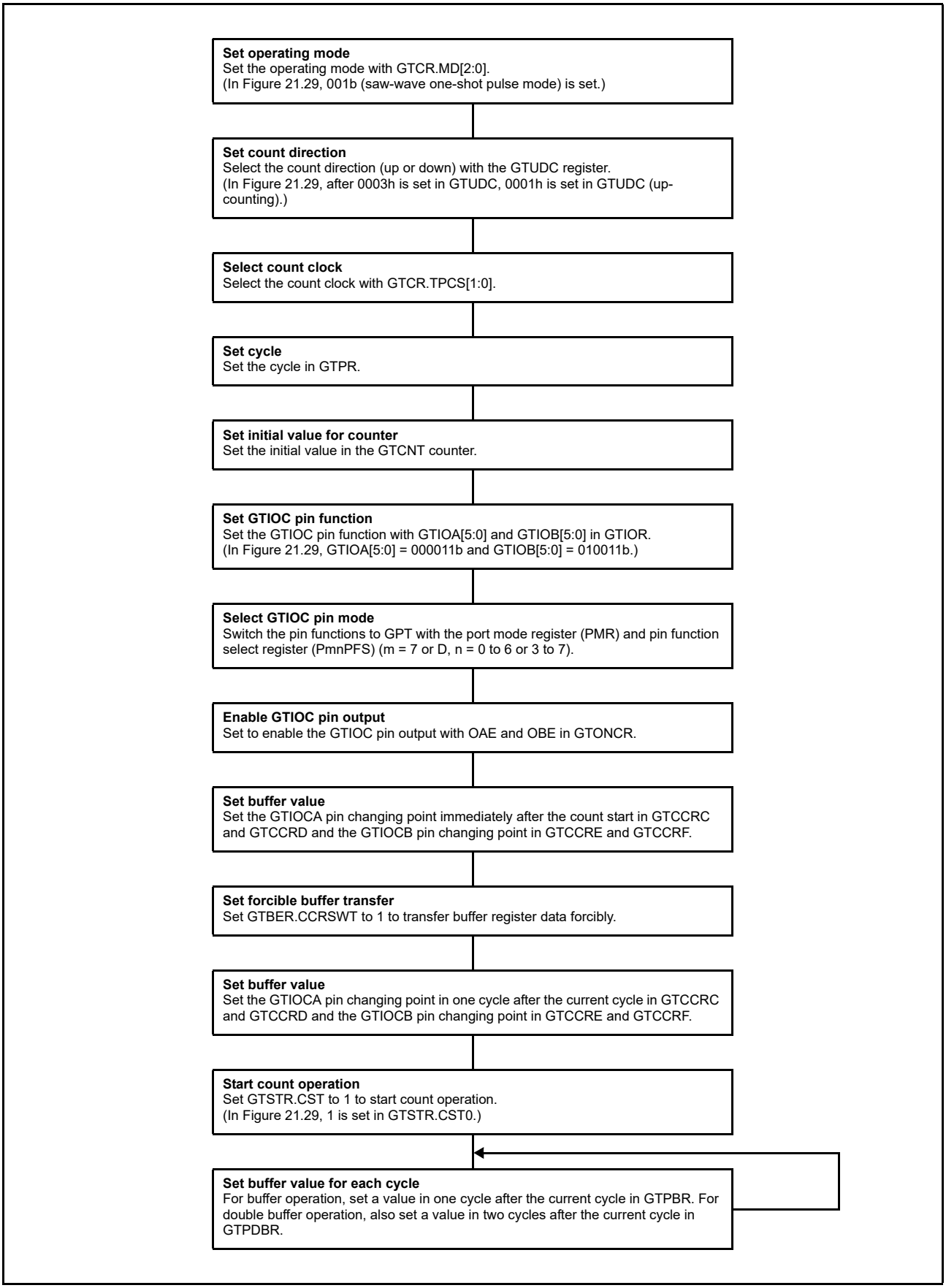


Figure 21.30 Example for Setting Saw-Wave One-Shot Pulse Mode

(3) Triangle-Wave PWM Mode 1 (16-Bit Transfer at Trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n = 0 to 3). Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTCVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.31 shows an example of triangle-wave PWM mode 1 operation, and Figure 21.32 shows an example for setting triangle-wave PWM mode 1.

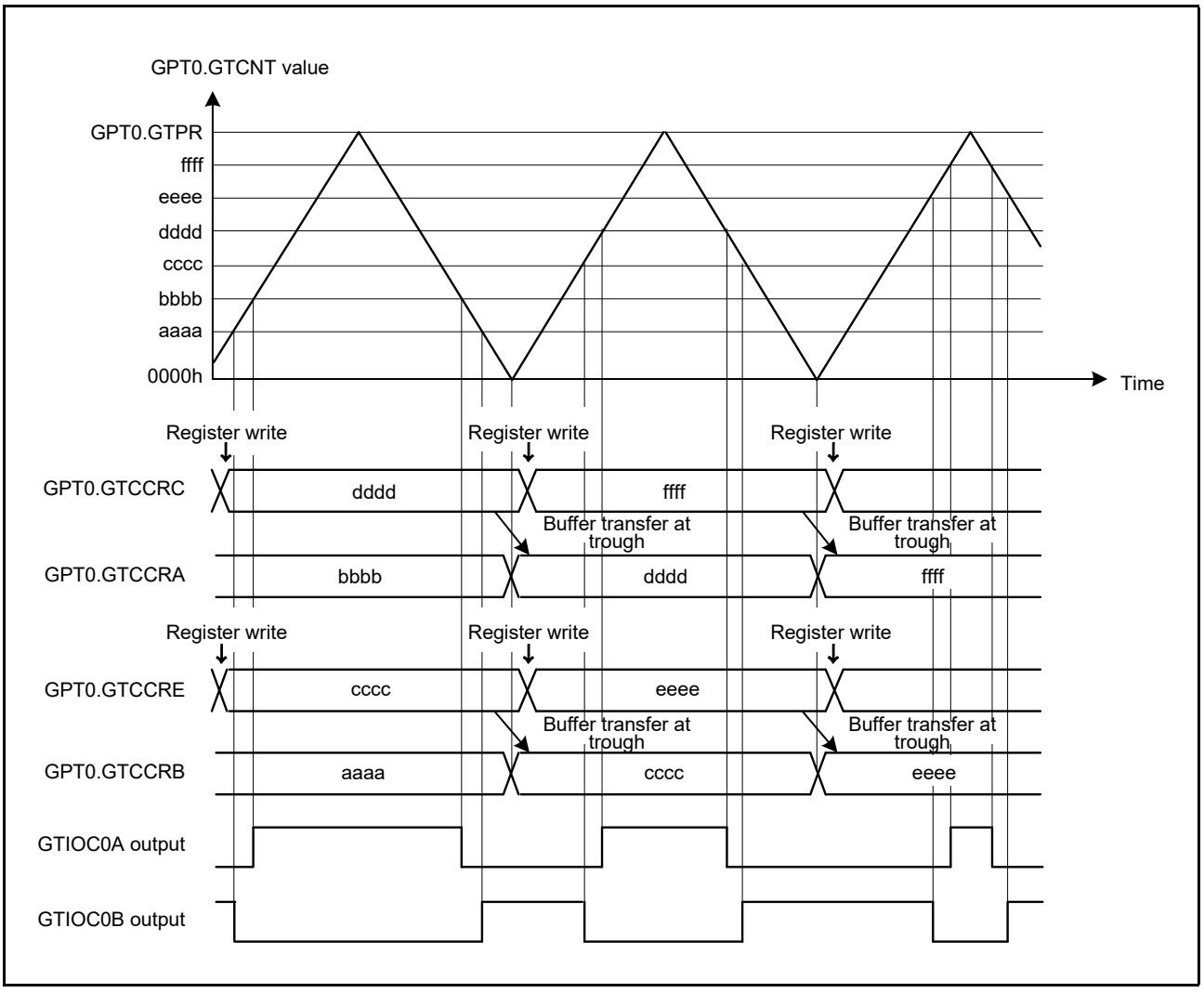


Figure 21.31 Example of Triangle-Wave PWM Mode 1 Operation (Buffer Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

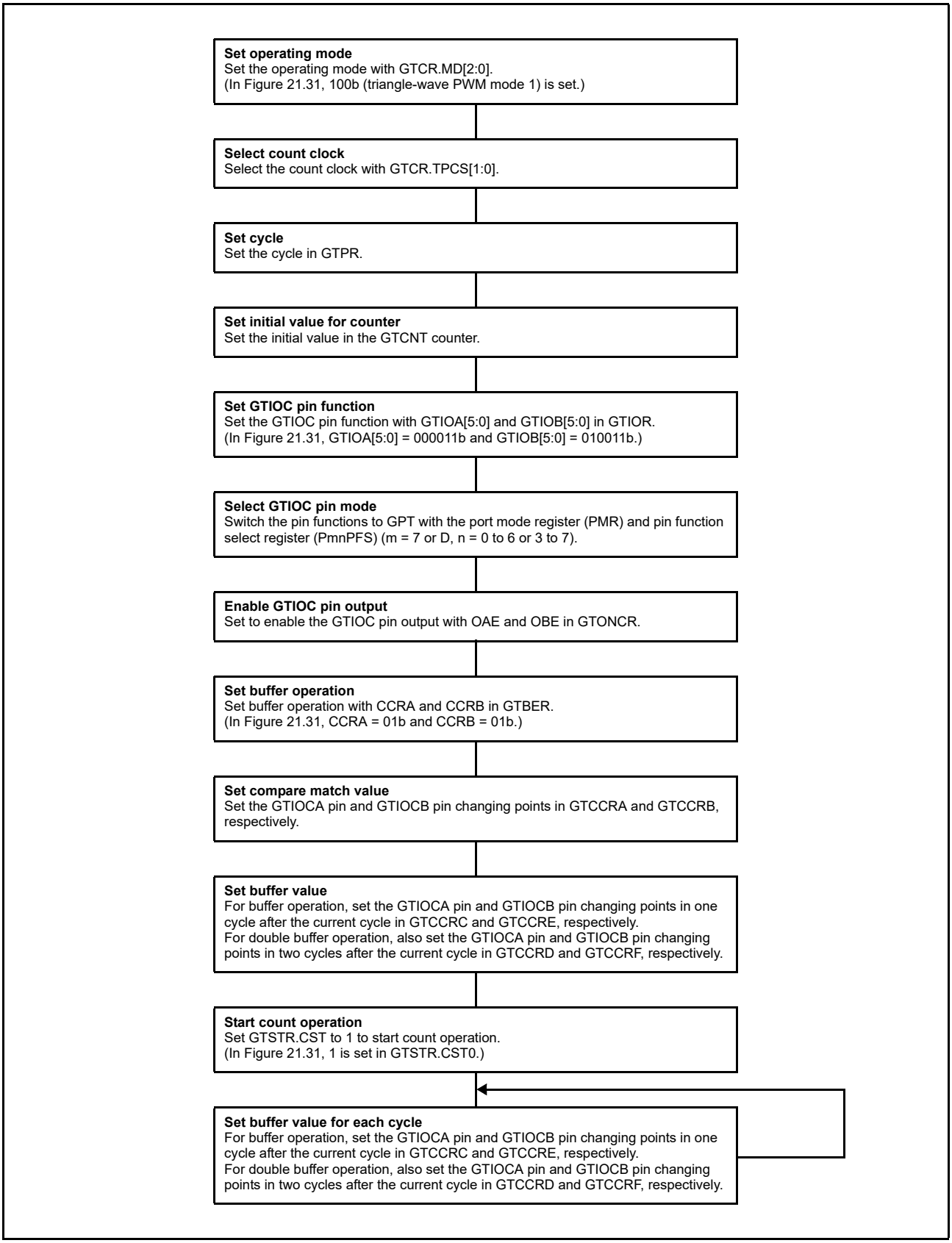


Figure 21.32 Example for Setting Triangle-Wave PWM Mode 1

(4) Triangle-Wave PWM Mode 2 (16-Bit Transfer at Crest and Trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCnA or GTIOCnB pin when a GPTn.GTCCRA or GPTn.GTCCRB compare match occurs (n = 0 to 3). The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.
By setting GTDTCR, GTCVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.
Figure 21.33 shows an example of triangle-wave PWM mode 2 operation, and Figure 21.34 shows an example for setting triangle-wave PWM mode 2.

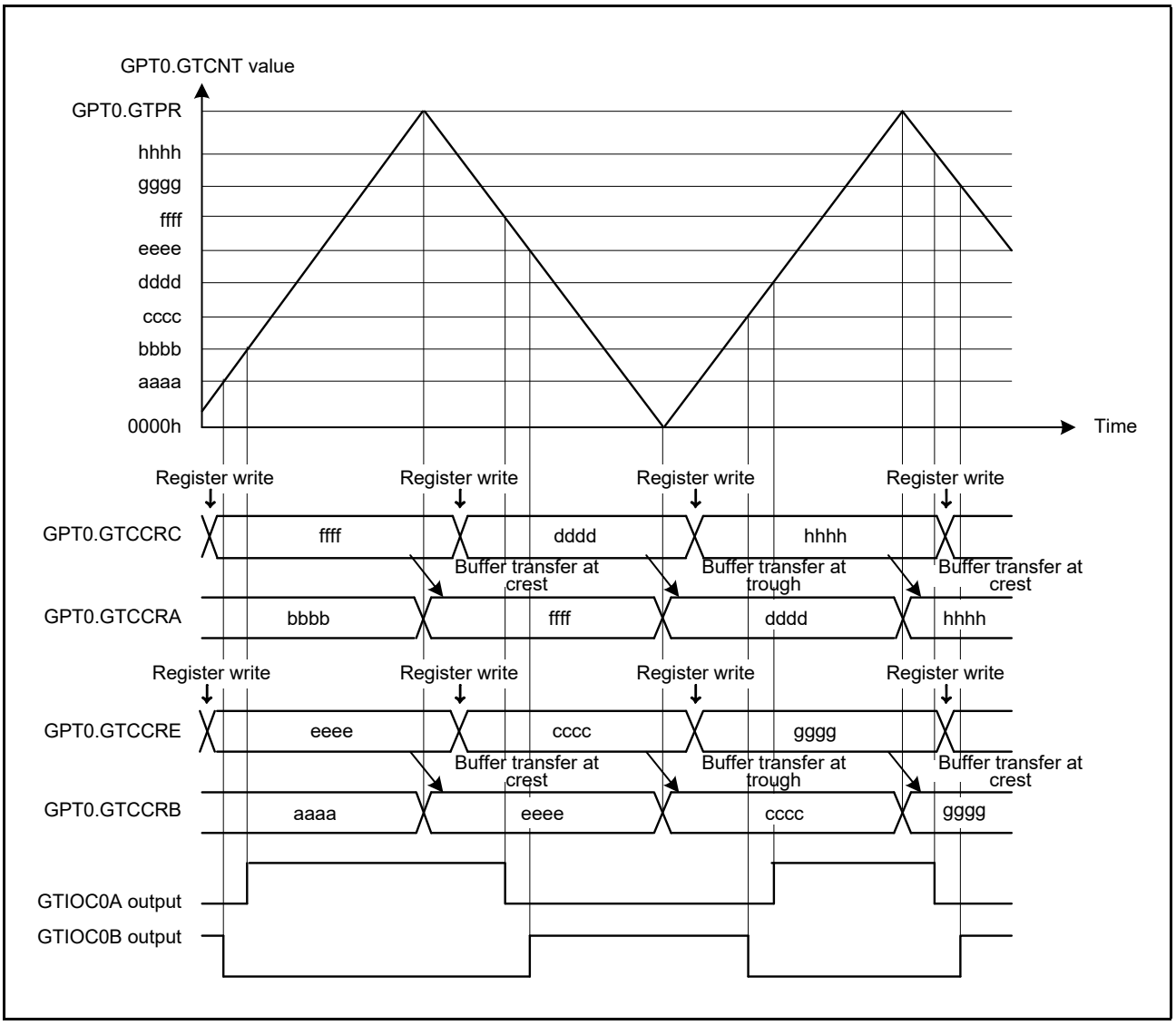


Figure 21.33 Example of Triangle-Wave PWM Mode 2 Operation (Buffer Operation, Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

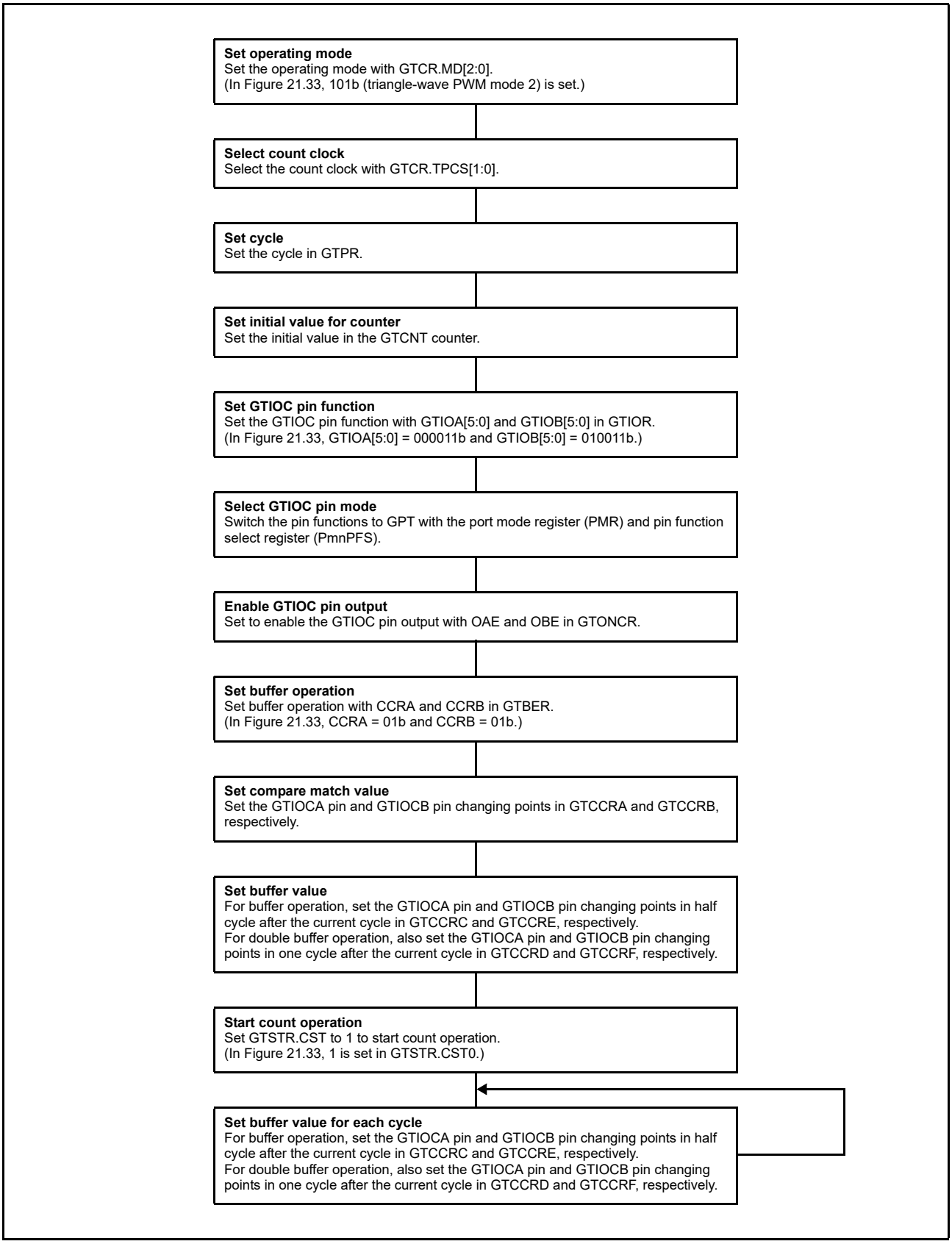


Figure 21.34 Example for Setting Triangle-Wave PWM Mode 2

(5) Triangle-Wave PWM Mode 3 (32-Bit Transfer at Trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GPTn.GTPR, the GPTn.GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCnA or GTIOCnB pin at a compare match of GPTn.GTCCRA or GPTn.GTCCRB with buffer operation fixed (n = 0 to 3). Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from GTCCRC to GTCCRA, from GTCCRE to GTCCRB, from GTCCRD to temporary register A, and from GTCCRF to temporary register B at the trough, and from temporary register A to GTCCRA and from temporary register B to GTCCRB at the crest. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

By setting GTDTCR, GTCVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 21.35 shows an example of triangle-wave PWM mode 3 operation, and Figure 21.36 shows an example for setting triangle-wave PWM mode 3.

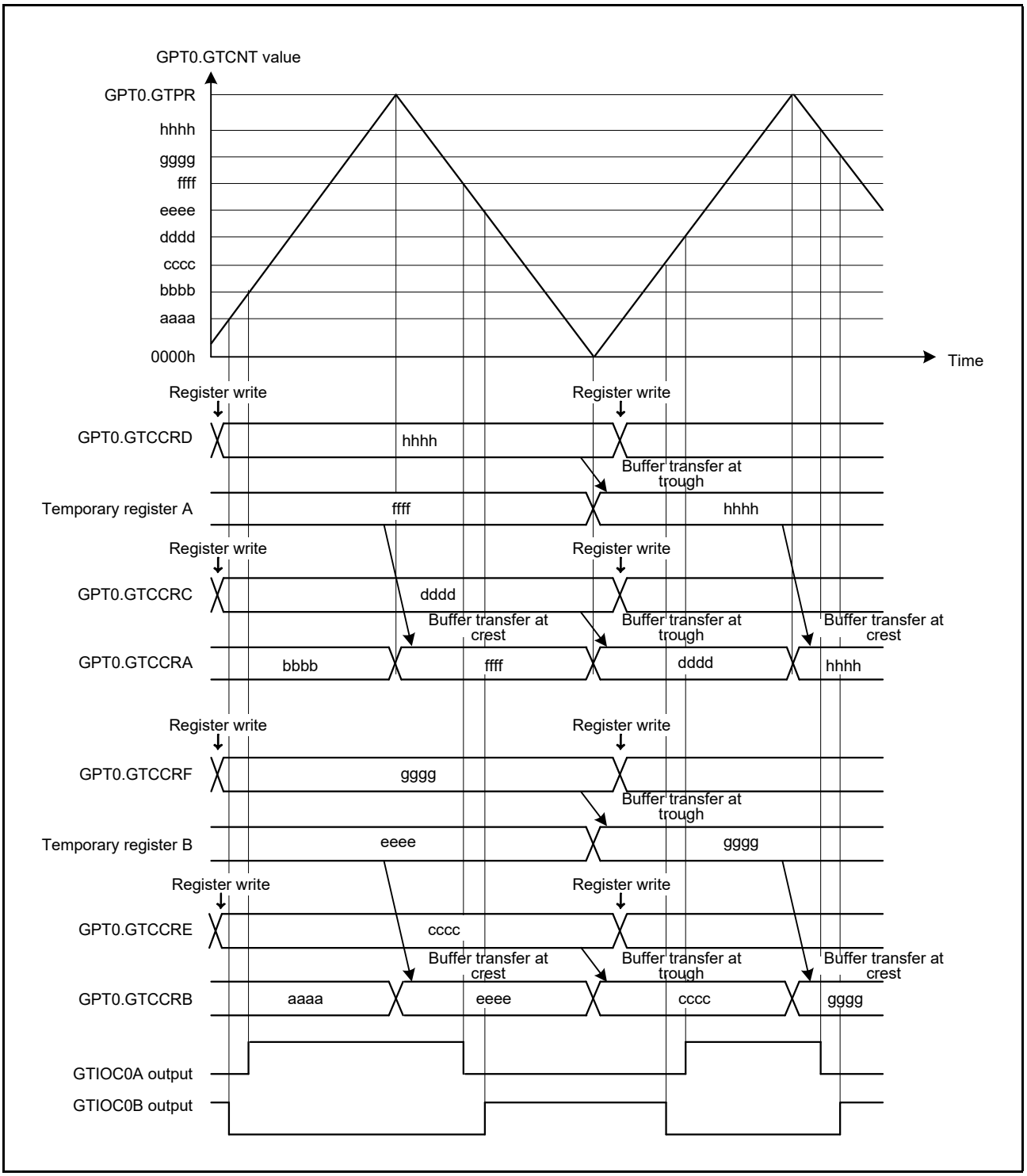


Figure 21.35 Example of Triangle-Wave PWM Mode 3 Operation (Low Output from GTIOC0A and High Output from GTIOC0B at Count Start, Toggle Output at GTCCRA/GTCCRB Compare Match, Output Retained at Cycle End)

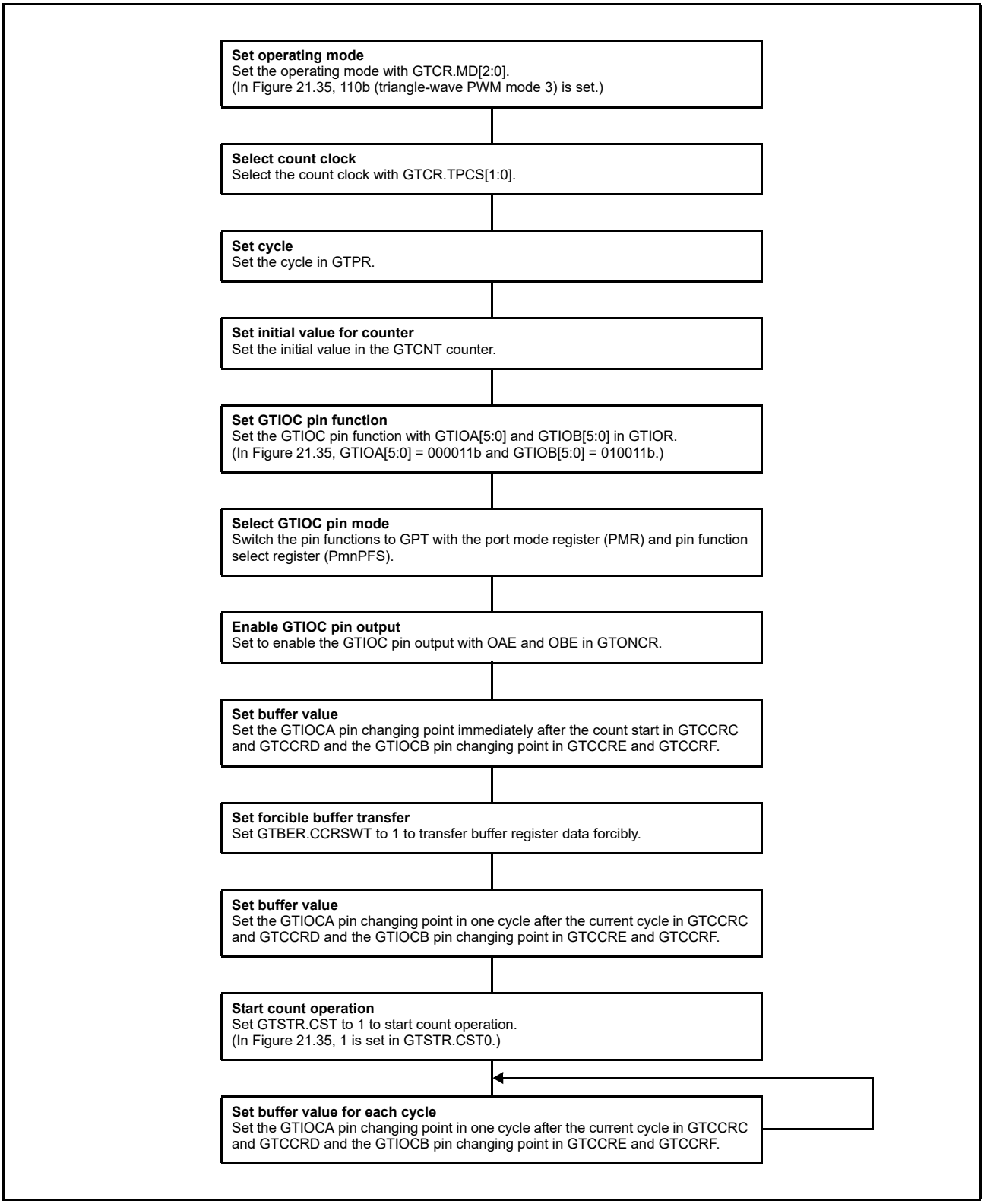


Figure 21.36 Example for Setting Triangle-Wave PWM Mode 3

21.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB.

The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes. Dead time can be separately set for the first half and second half of a waveform. Dead time for the changing point in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at the cycle end (at a GTCNT overflow (during up-count operation) or an underflow (during down-count operation) for saw waves and at the trough for triangle waves).

Writing to GTCCRB is prohibited when the automatic dead time setting function is used. Dead time setting beyond the cycle is also prohibited. Values for automatic dead time setting can be read from GTCCRB.

Figure 21.37 to Figure 21.39 show examples of automatic dead time setting function operation. Figure 21.40 and Figure 21.41 show the setting examples.

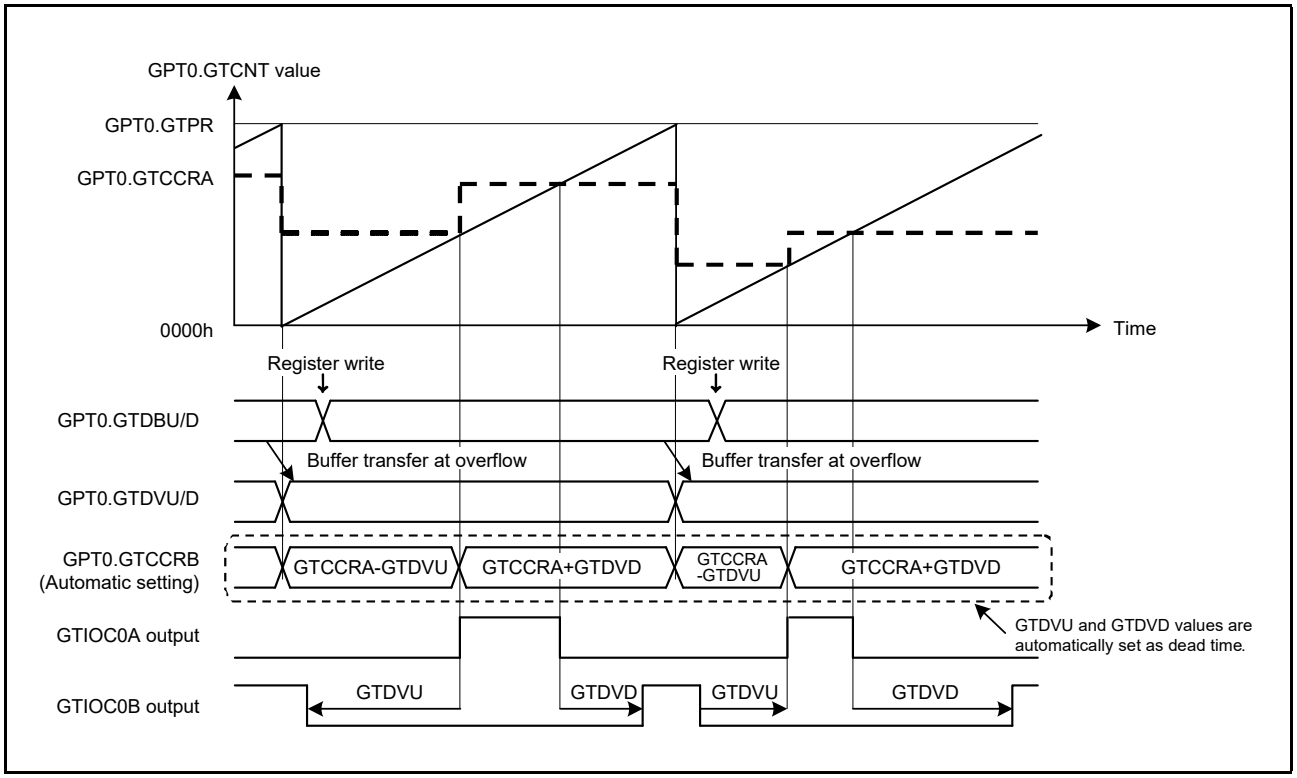


Figure 21.37 Example of Automatic Dead Time Setting Function Operation (Saw-Wave One-Shot Pulse Mode, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

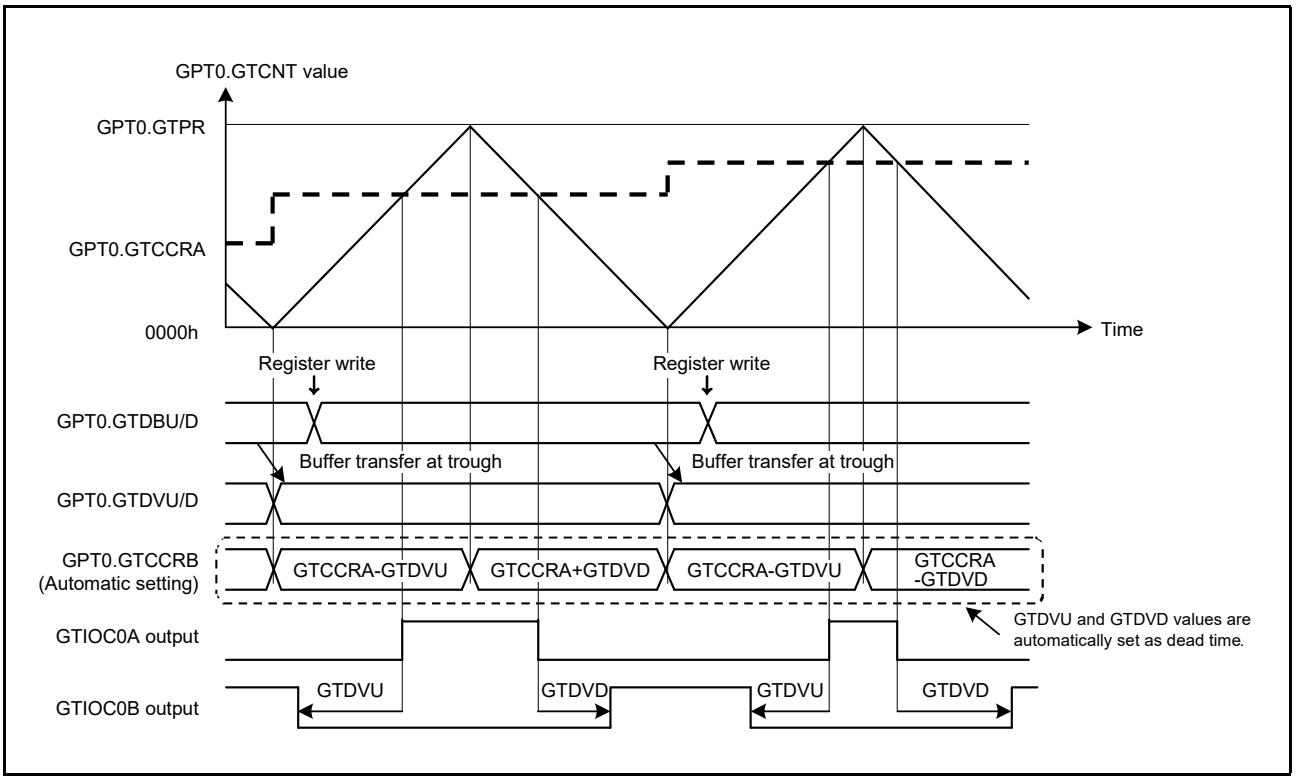


Figure 21.38 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 1, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

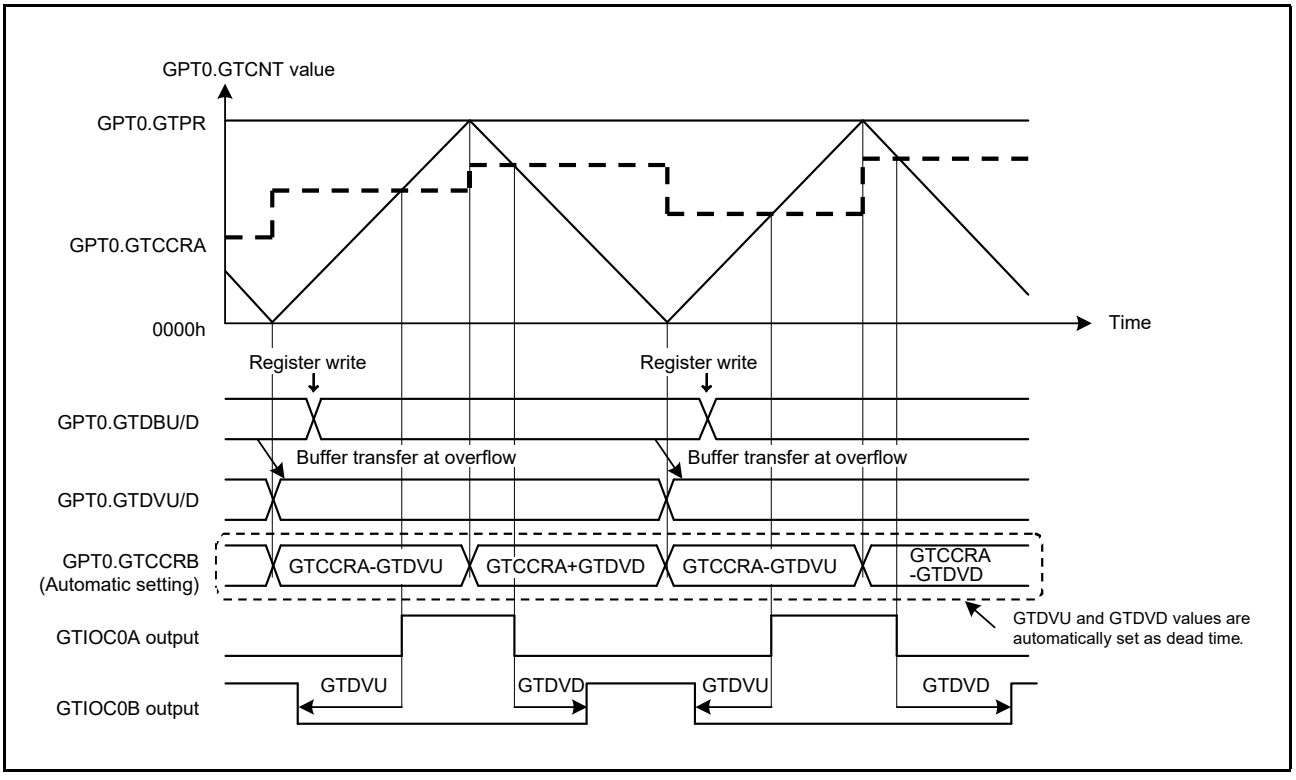


Figure 21.39 Example of Automatic Compare-Match Value Setting Function with Dead Time (Triangle-Wave PWM Mode 2 or 3, GTDVU and GTDVD Set to Buffer Operation, Active Level: High)

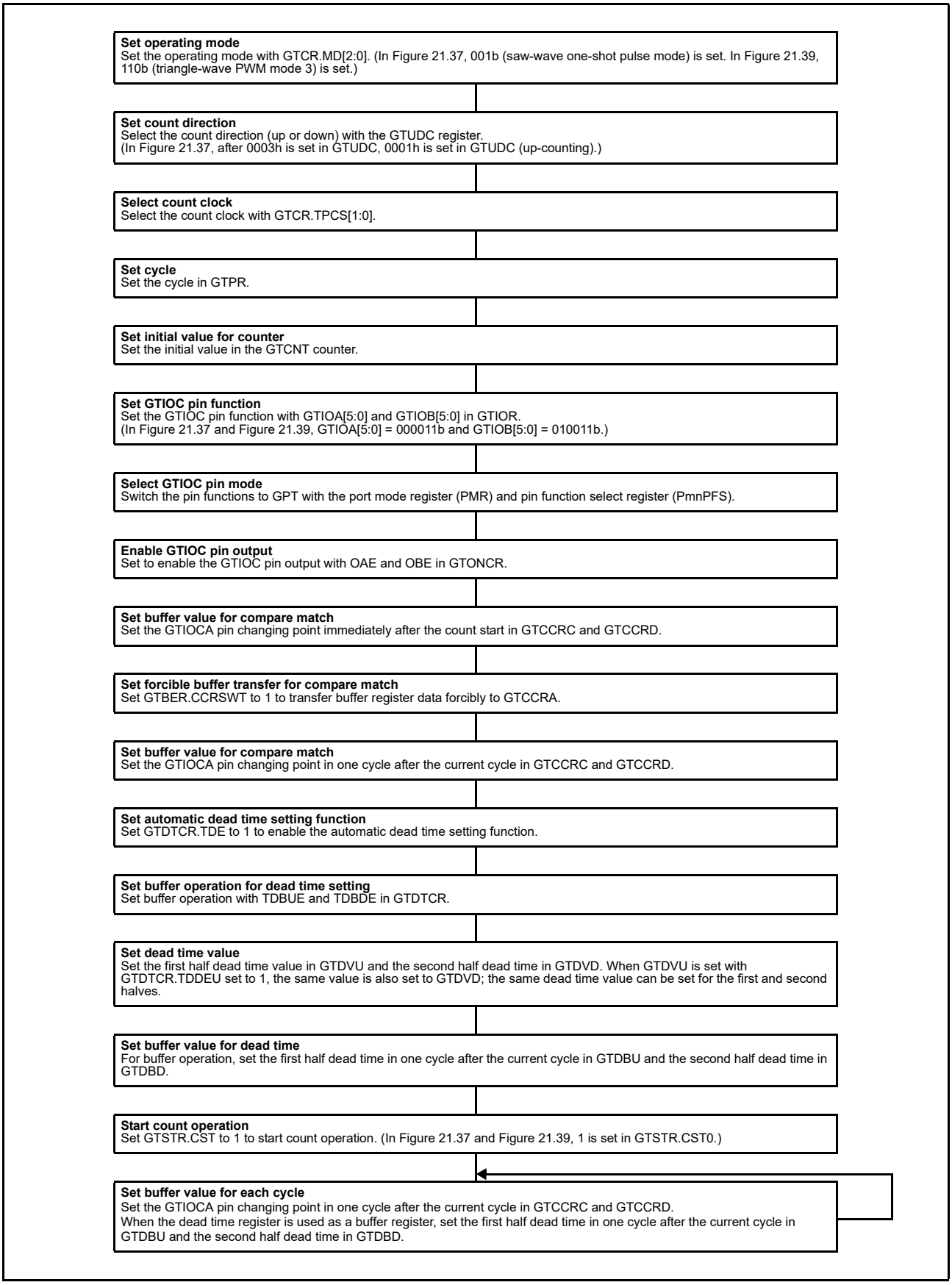


Figure 21.40 Example for Setting Automatic Dead Time Setting Function (Saw-Wave One-Shot Pulse Mode, Triangle-Wave PWM Mode 3)

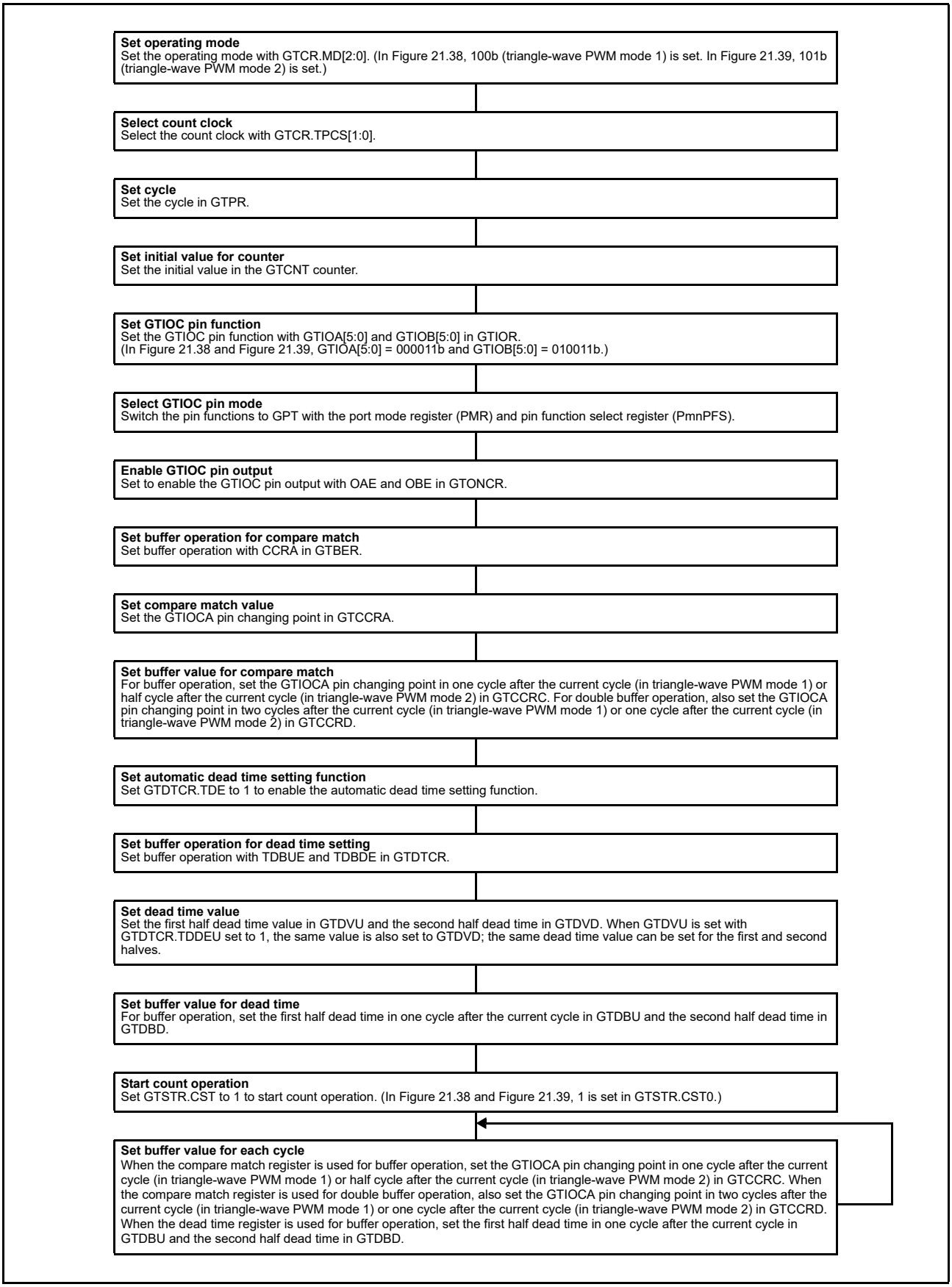


Figure 21.41 Example for Setting Automatic Dead Time Setting Function (Triangle-Wave PWM Mode 1 or 2)

21.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDC.
In saw-wave mode, if the UD bit in GTUDC is modified during count operation, the count direction is changed at an overflow (when modified during up-count operation) or an underflow (when modified during down-count operation). If the UD bit is modified while count operation is stopped and the UDF bit is 0, the UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
In triangle-wave mode, the count direction is not changed even though the UD bit in GTUDC is modified during count operation. Similarly, even though the UD bit is modified while count operation is stopped and UDF bit is 0, the UD bit value is not reflected to the count operation. If the UDF bit is set to 1 while count operation is stopped, the UD bit value at that time is reflected at the start of counting.
If the count direction is changed during saw-wave count operation, the GTPR value after the start of up-counting is reflected to the count cycle during up-count operation and the GTPR value before the start of down-counting is reflected during down-count operation.

Figure 21.42 shows an example of count direction changing function operation.

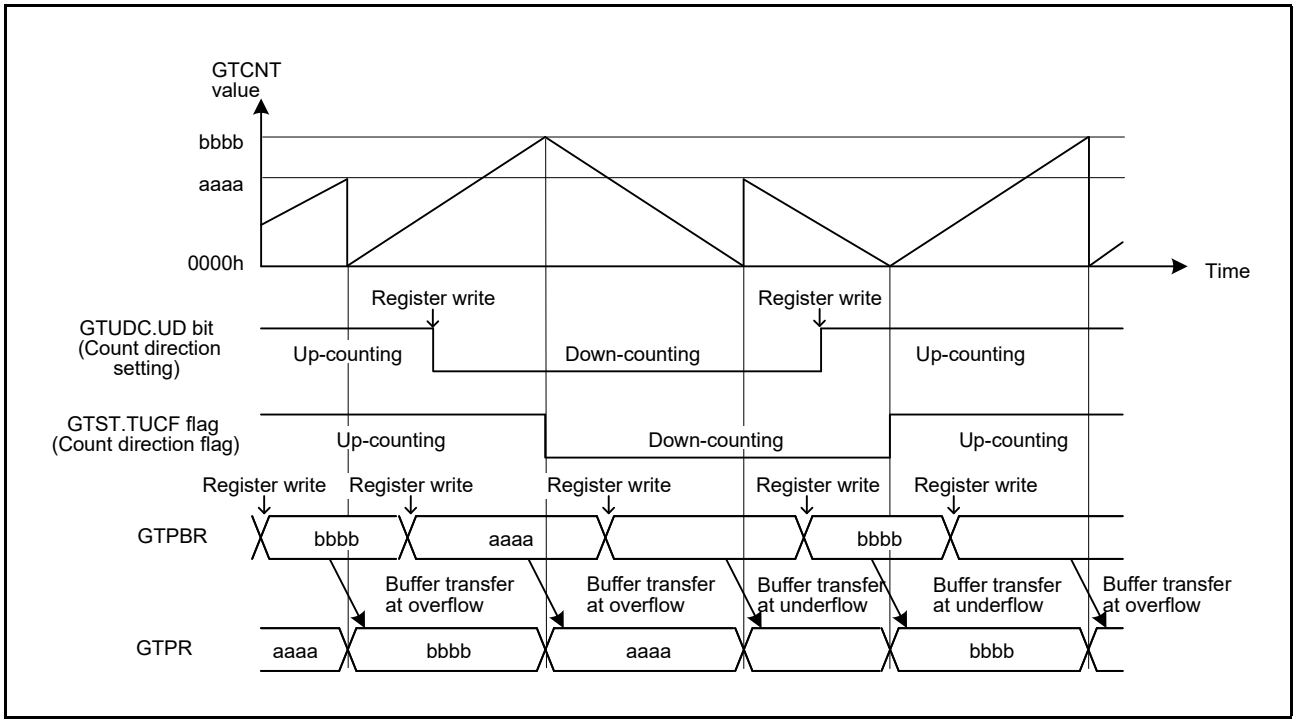


Figure 21.42 Example of Count Direction Changing Function Operation (during Buffer Operation)

21.3.6 Hardware Start/Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by following hardware sources: GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare).
The counter can also be cleared by the GTCCRA or GTCCRB input capture.

21.3.6.1 Hardware Start Operation

The GTCNT counter can be started by a hardware source. Select a hardware source to start counting using GTHSSR.CSHSL, set the changing edge for the hardware source with GTHSCR.CSHW, and then enable to start counting.
Figure 21.43 shows an example of count start operation by a hardware source. Figure 21.44 shows the setting example.

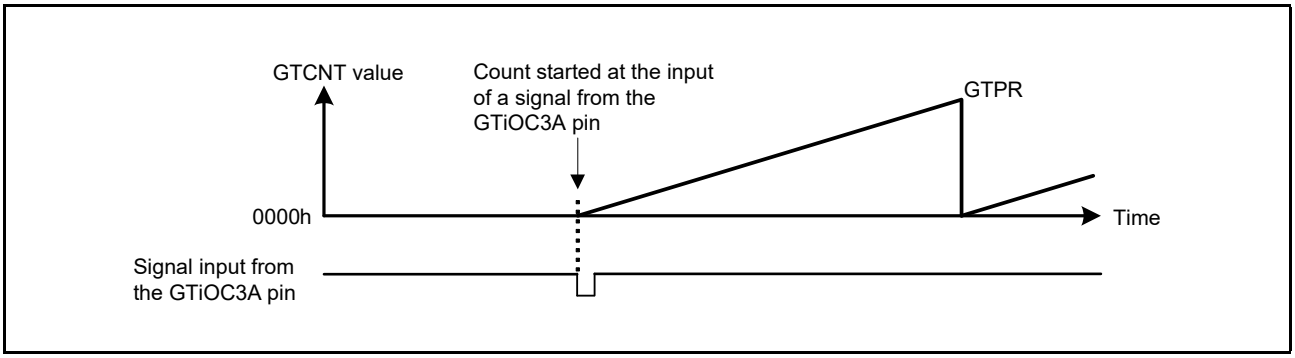


Figure 21.43 Example of Count Start Operation by Hardware Source (Started at Input of Signal from the GTiOC3A Pin)

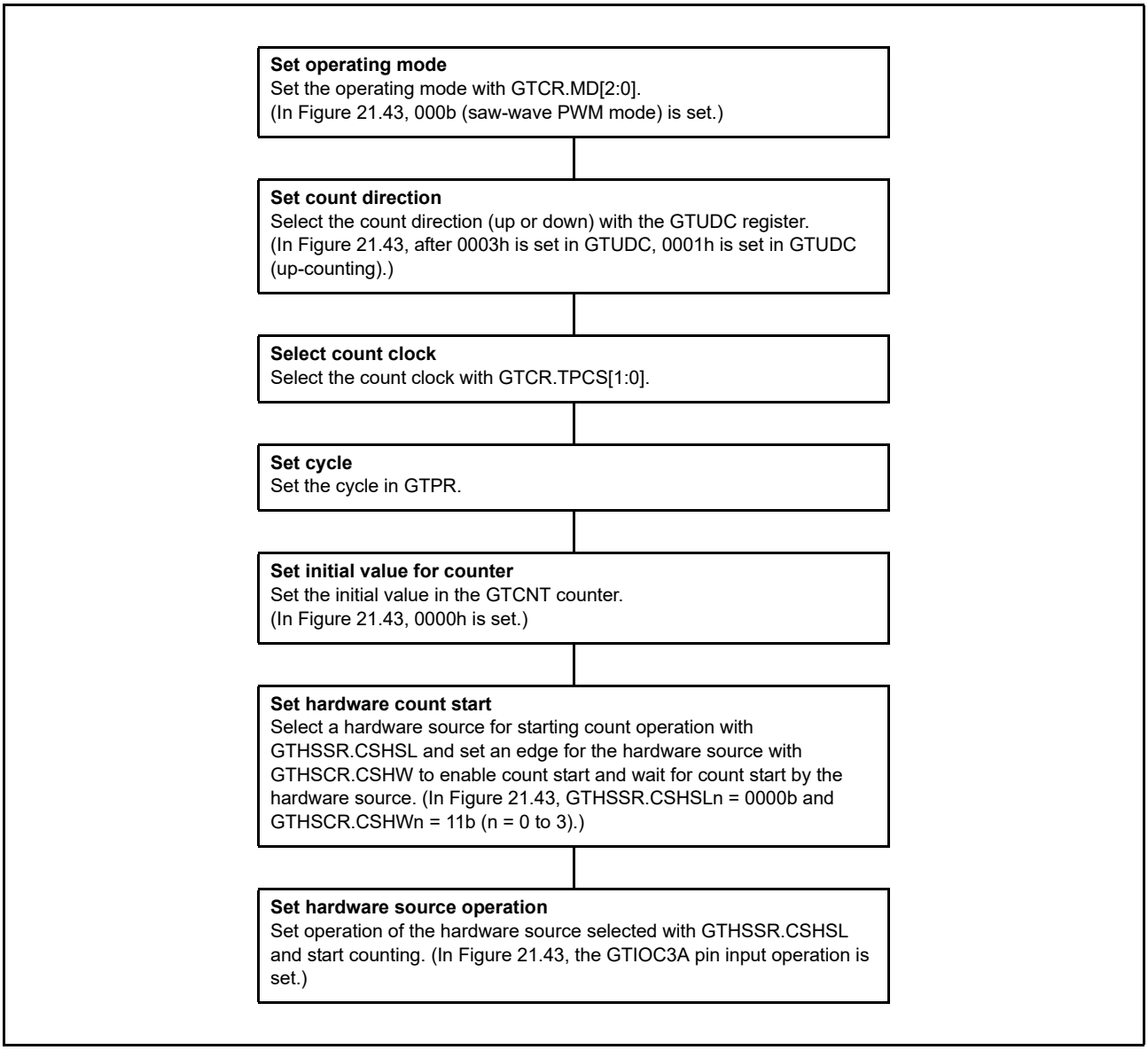


Figure 21.44 Example for Setting Count Start Operation by Hardware Source

21.3.6.2 Hardware Stop Operation

The GTCNT counter can be stopped by a hardware source. Select a hardware source to stop counting using GTHPSR.CSHPL, set the changing edge for the hardware source with GTHSCR.CPHW, and then enable to stop counting.

Figure 21.45 shows an example of count stop operation by a hardware source. Figure 21.46 shows the setting example. In this example, the count operation is stopped at both edges of the GTIOC3A internal output (output compare) and is restarted at both edges of the GTIOC3B internal output (output compare).

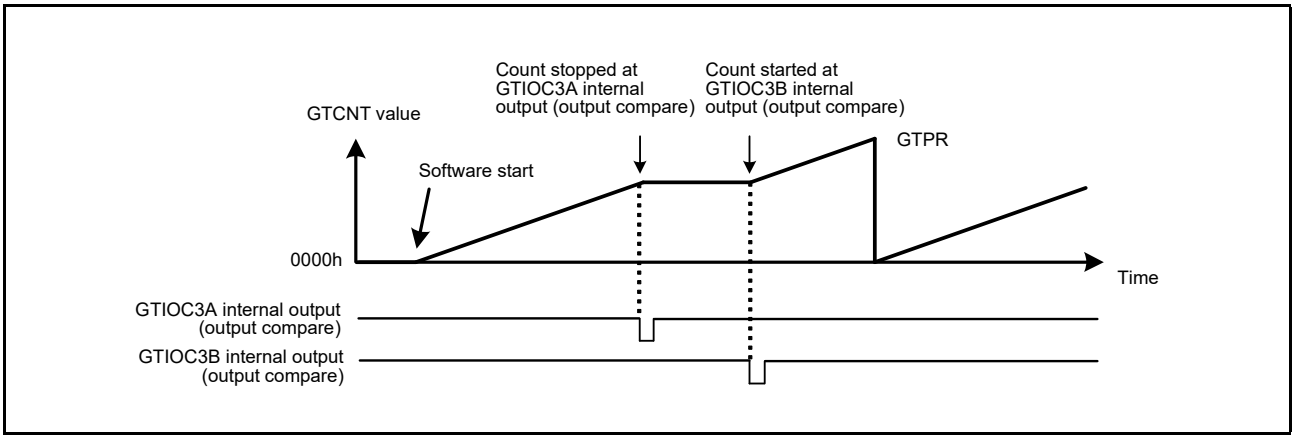


Figure 21.45 Example of Count Stop Operation by Hardware Source (Started by Software, Stopped at GTIOC3A Internal Output (Output Compare), Restarted at GTIOC3B Internal Output (Output Compare))

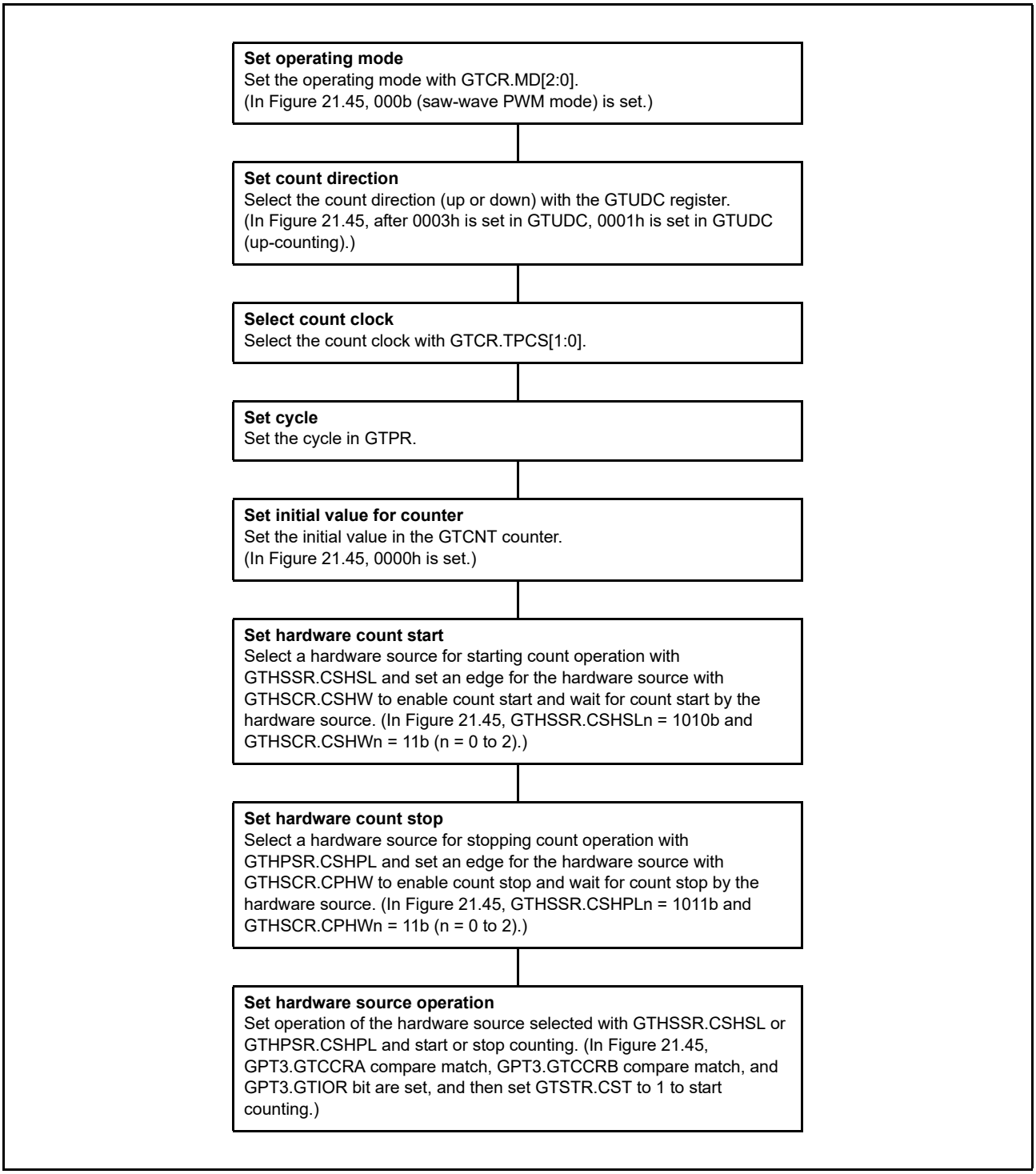


Figure 21.46 Example for Setting Count Stop Operation by Hardware Source

Figure 21.47 shows an example of count start/stop operation by a hardware source. Figure 21.48 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRG.

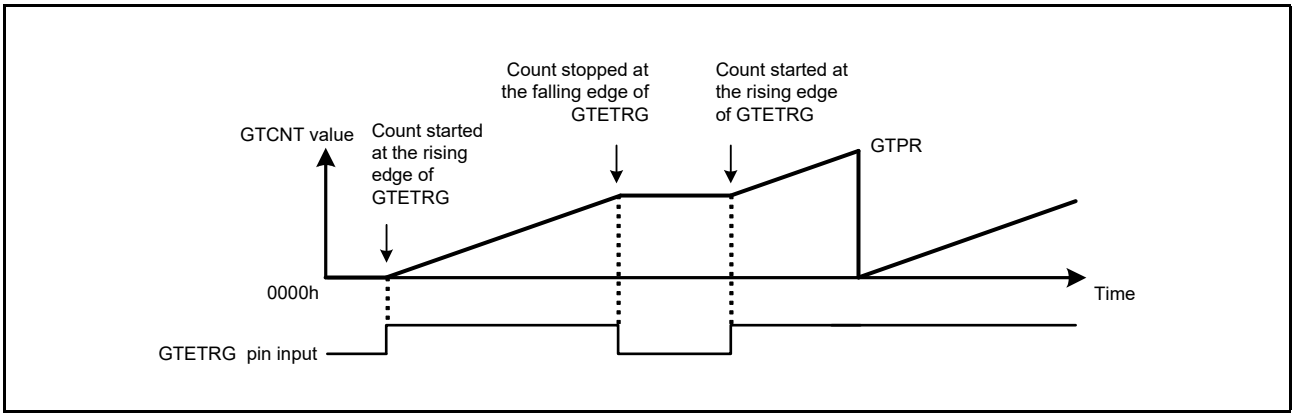


Figure 21.47 Example of Count Start/Stop Operation by Hardware Source (Started at Rising Edge of GTETRG Pin Input, Stopped at Falling Edge of GTETRG Pin Input)

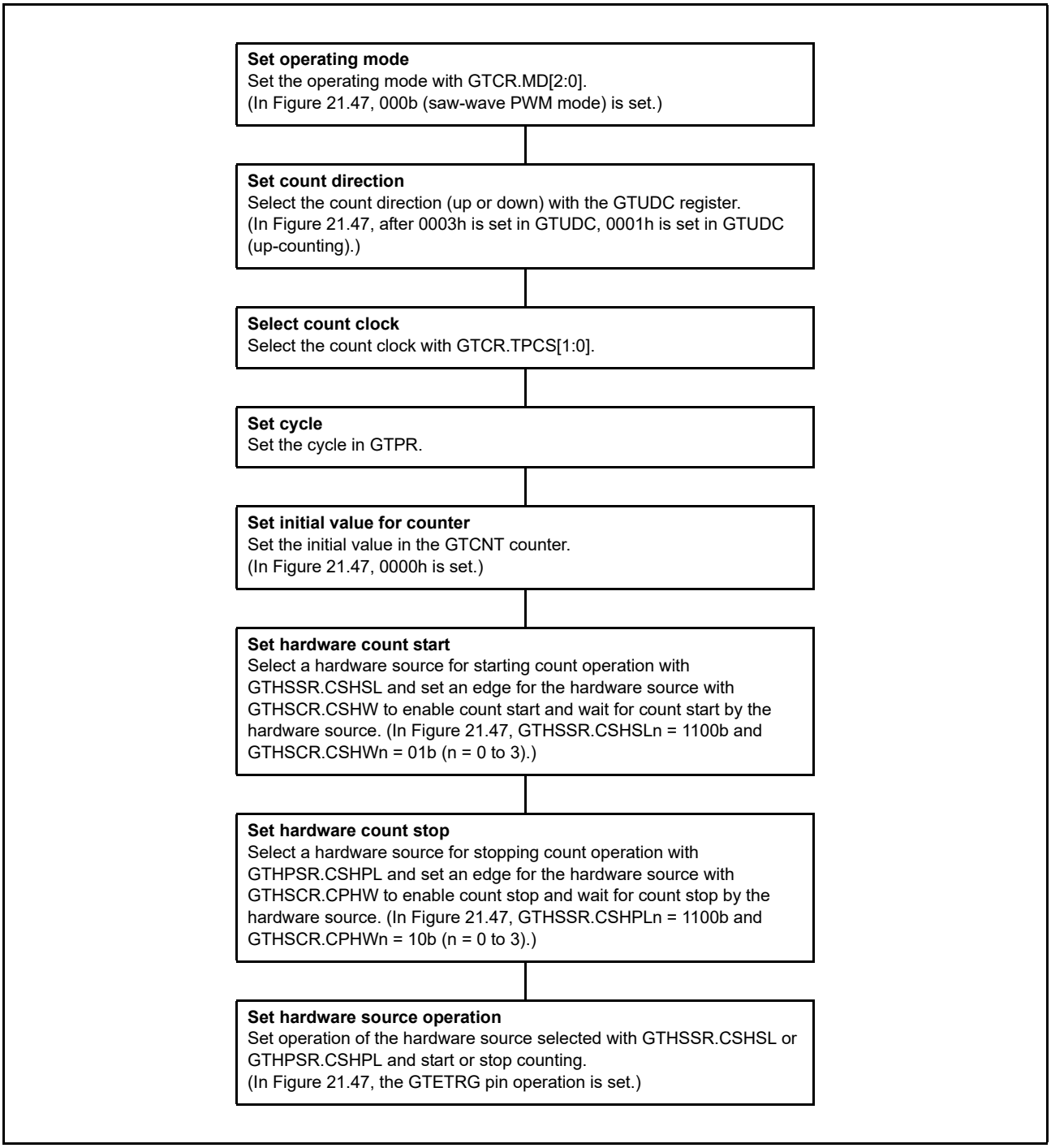


Figure 21.48 Example for Setting Count Start/Stop Operation by Hardware Source

21.3.6.3 Hardware Clear Operation

The GTCNT counter can be cleared by a hardware source. Select a hardware source to clear the counter using GTHPSR.CSHPL, set the changing edge for the hardware source with GTHCCR.CCHW, and then enable to clear the counter.

The counter can also be cleared by a GTCCRA or GTCCRB input capture by setting GTCR.CCLR[1:0].

Note that the GTCIV/GTCIU interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 21.49 and Figure 21.50 show examples of counter clearing operation by a hardware source. Figure 21.51 shows the setting example. In this example, the counter is started at both edges of the GTIOC3A pin, and the counter is stopped/cleared at both edges of the GTOC3B pin input.

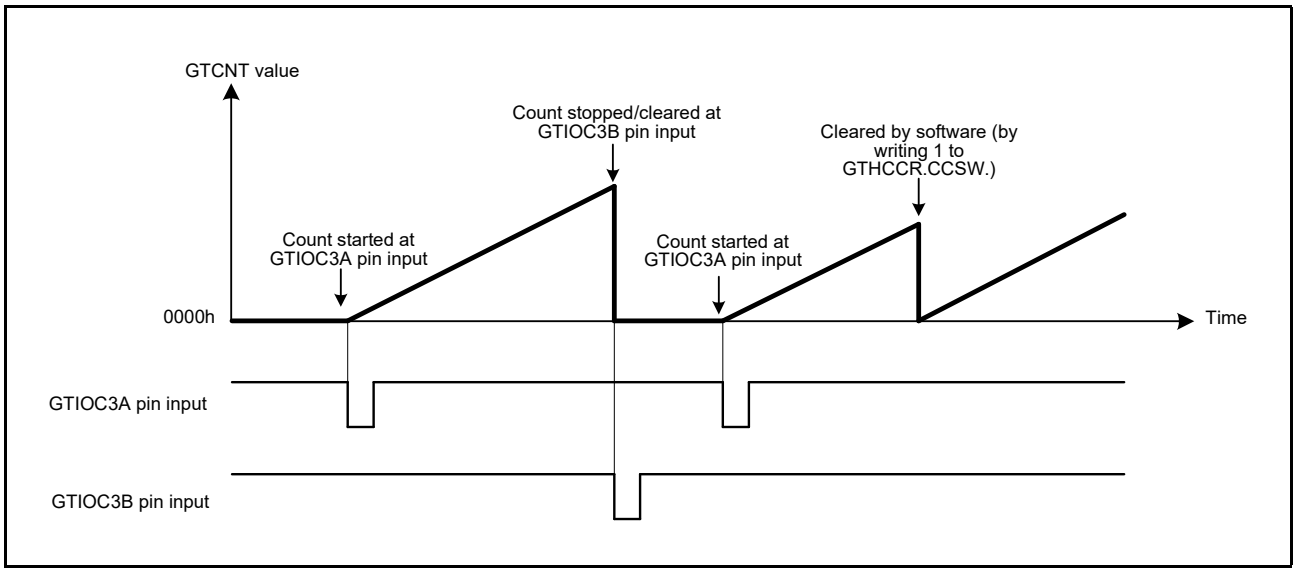


Figure 21.49 Examples of Count Clearing Operation by Hardware Source (Saw-Wave Up-Counting, Started at GTIOC3A Pin Input, Stopped/Cleared at GTIOC3B Pin Input)

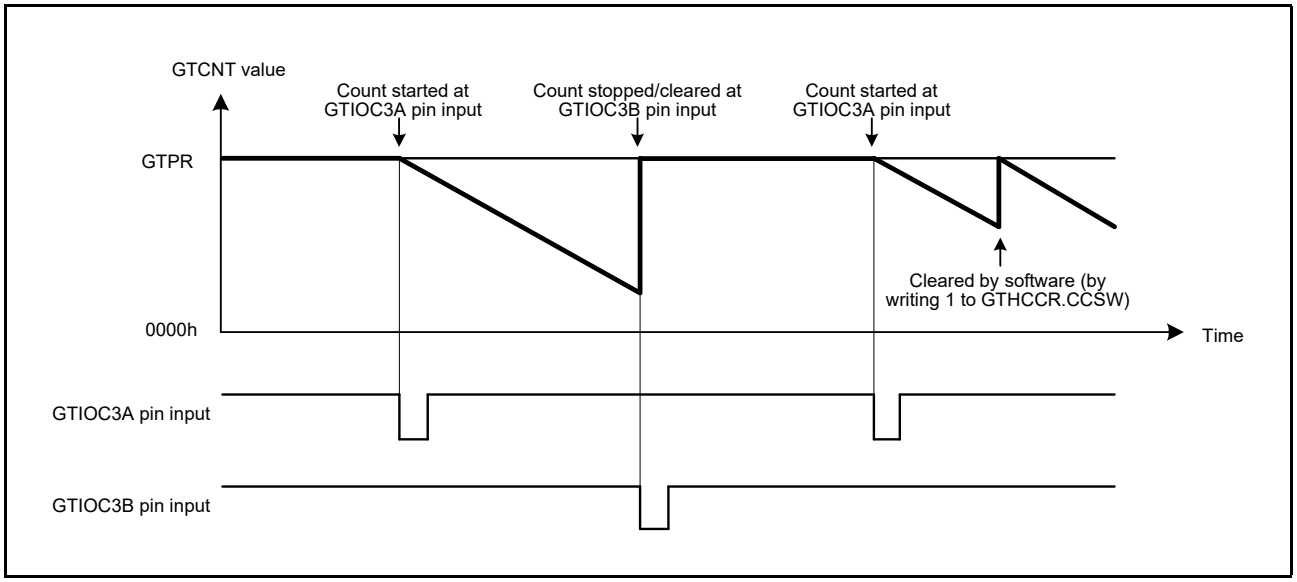


Figure 21.50 Examples of Count Clearing Operation by Hardware Source (Saw-Wave Down-Counting, Started at GTIOC3A Pin Input, Stopped/Cleared at GTIOC3B Pin Input)

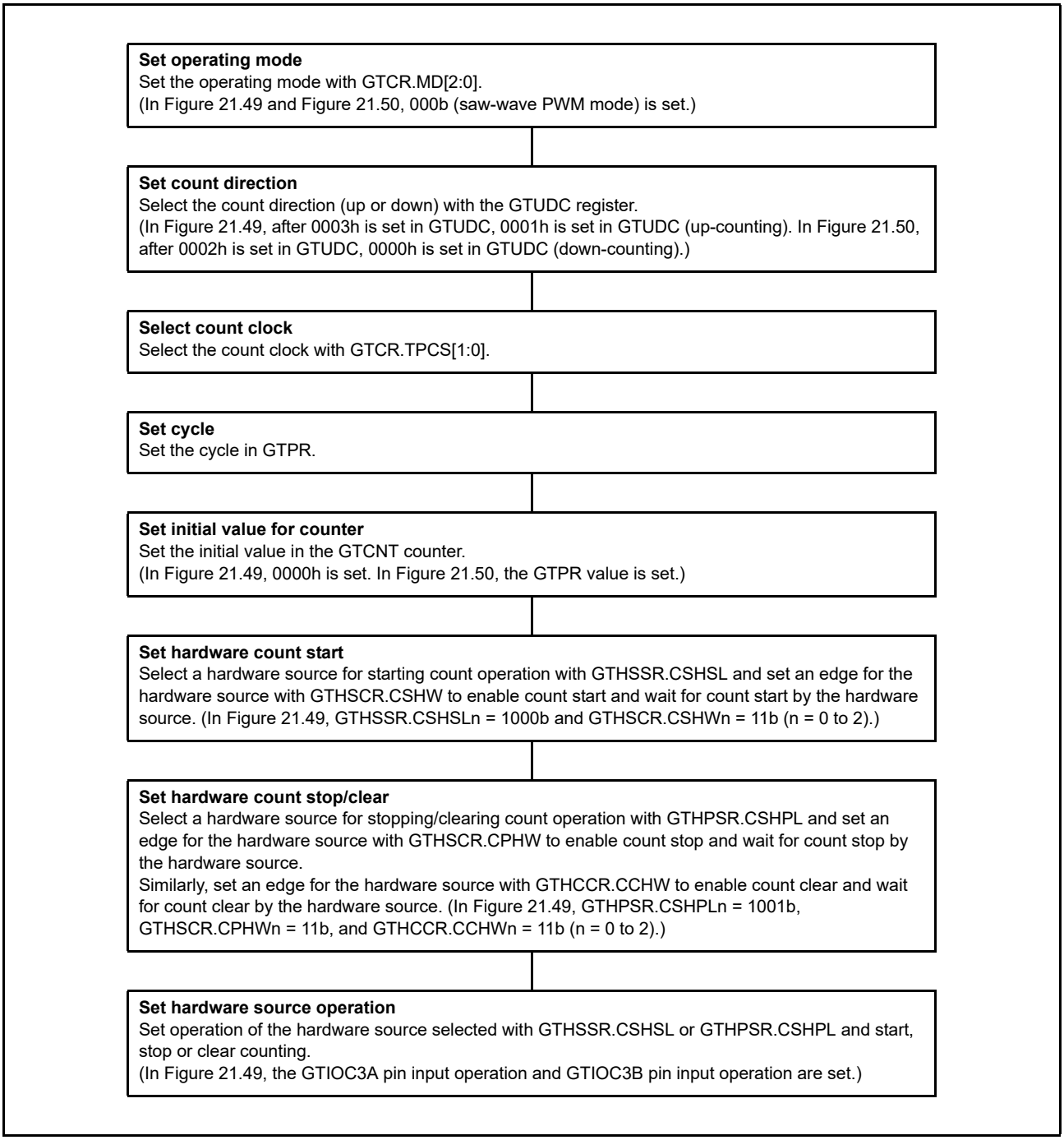


Figure 21.51 Example for Setting Count Clearing Operation by Hardware Source

The GTCIV/GTCIU interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 21.52 shows the relationship between the counter clearing by a hardware source and the GTCIV interrupt.

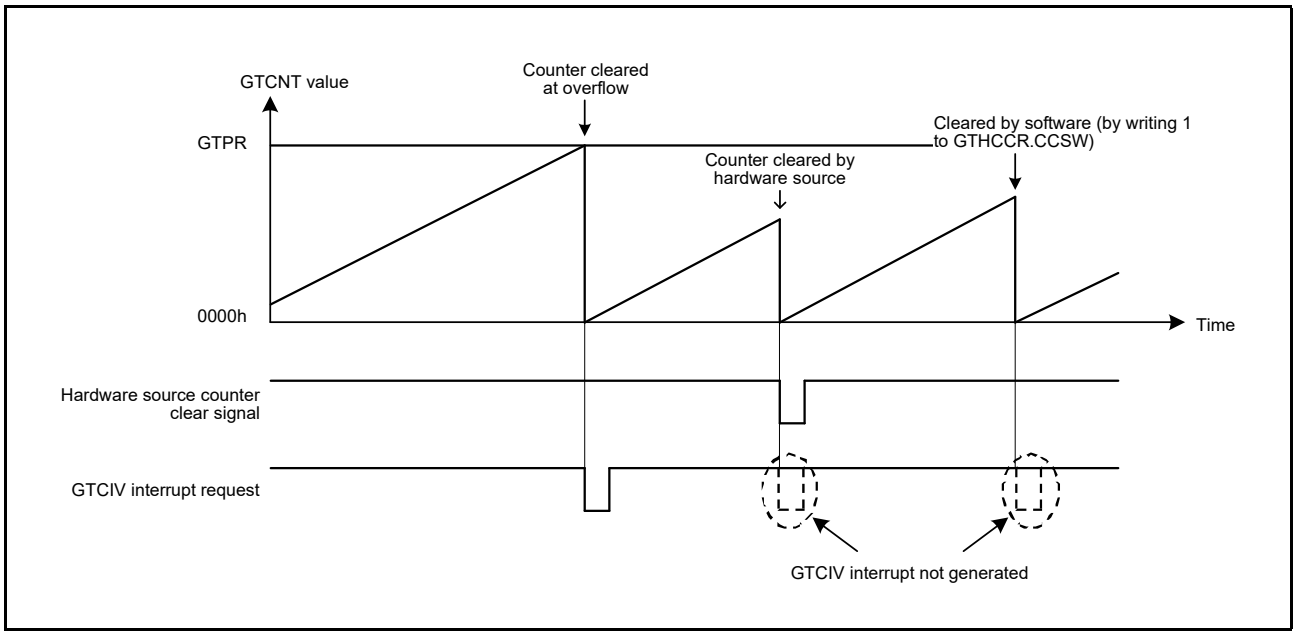


Figure 21.52 Relationship between Counter Clearing by Hardware Source and GTCIV Interrupt

21.3.7 Synchronized Operation

Synchronized operation on channels (synchronized clear operation, synchronized start operation) can be performed.

21.3.7.1 Synchronized Clear Operation

Synchronized clearing on channels can be controlled. Select which channels to be synchronously cleared by setting GTCR.CCLR[1:0] of the pertinent channels to 11b and which channel clearing source to be used for synchronized clearing by setting GTSYNC.SYNCn[1:0] (n = 0 to 3).

Figure 21.53 shows an example of synchronized clear operation, and Figure 21.55 shows the setting example. In this example, GPT1.GTCNT and GPT2.GTCNT are synchronously cleared by the GPT0.GTCNT clearing source (overflow).

Synchronized clearing of channels by a clear source does not cause synchronized clearing of another channel by the same clear source. (Synchronized clearing is not transmitted.)

Figure 21.54 shows an operation example in which two channels are synchronously cleared by the clear source of one of the channels and another channel is synchronously cleared by the clear source of the other one of the two channels.

Figure 21.55 shows the setting example. In this example, GPT1.GTCNT is synchronously cleared by GPT0.GTCNT clearing source (overflow), and GPT2.GTCNT is synchronously cleared by GPT1.GTCNT clearing source (overflow).

Although GPT1.GTCNT is synchronously cleared by the GPT0.GTCNT clearing source (overflow), GPT2.GTCNT is not synchronously cleared when GPT1.GTCNT is cleared by the GPT0.GTCNT clearing source.

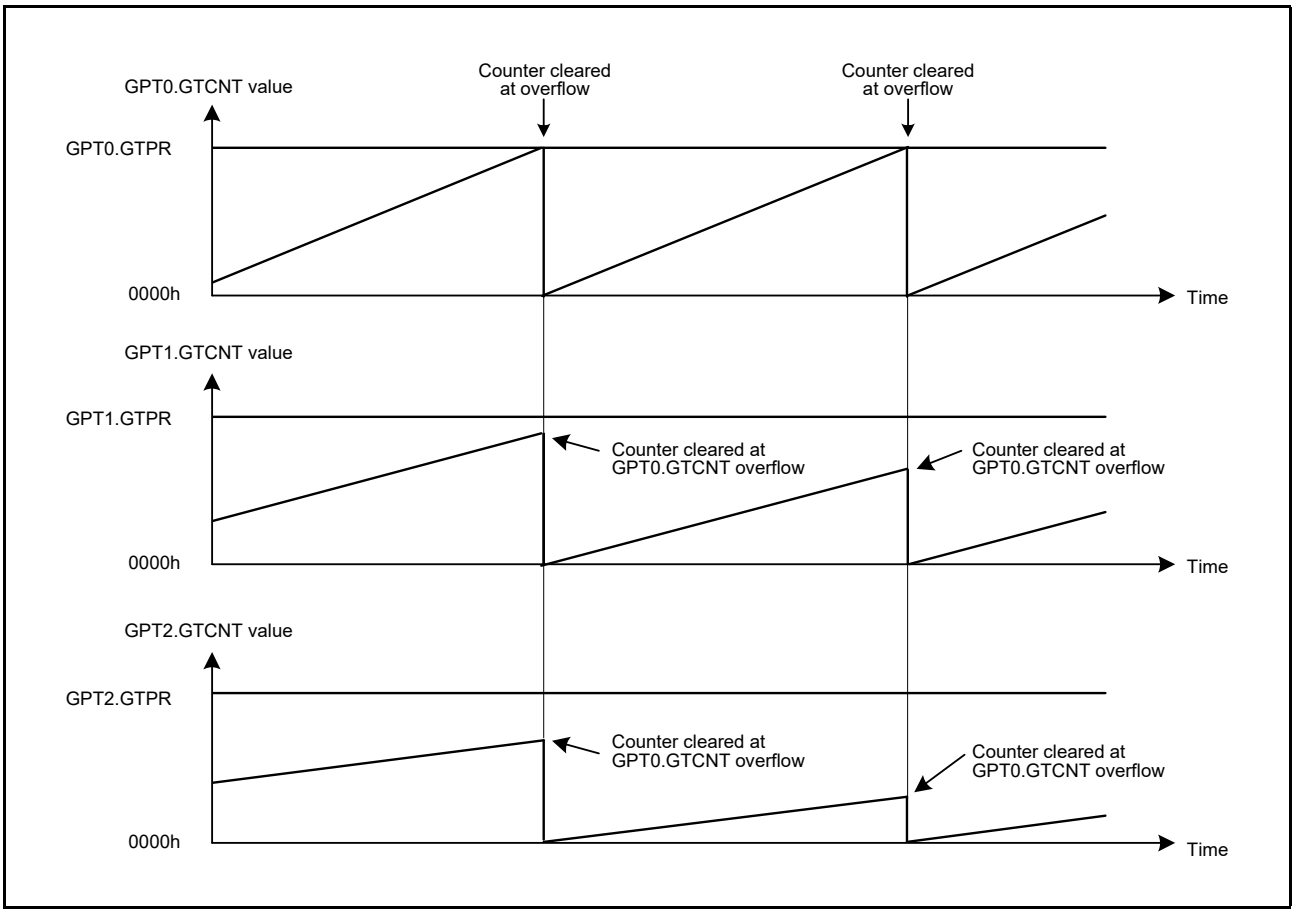


Figure 21.53 Example of Synchronized Clear Operation (GPT1.GTCNT and GPT2.GTCNT are Synchronously Cleared by GPT0.GTCNT Clearing Source)

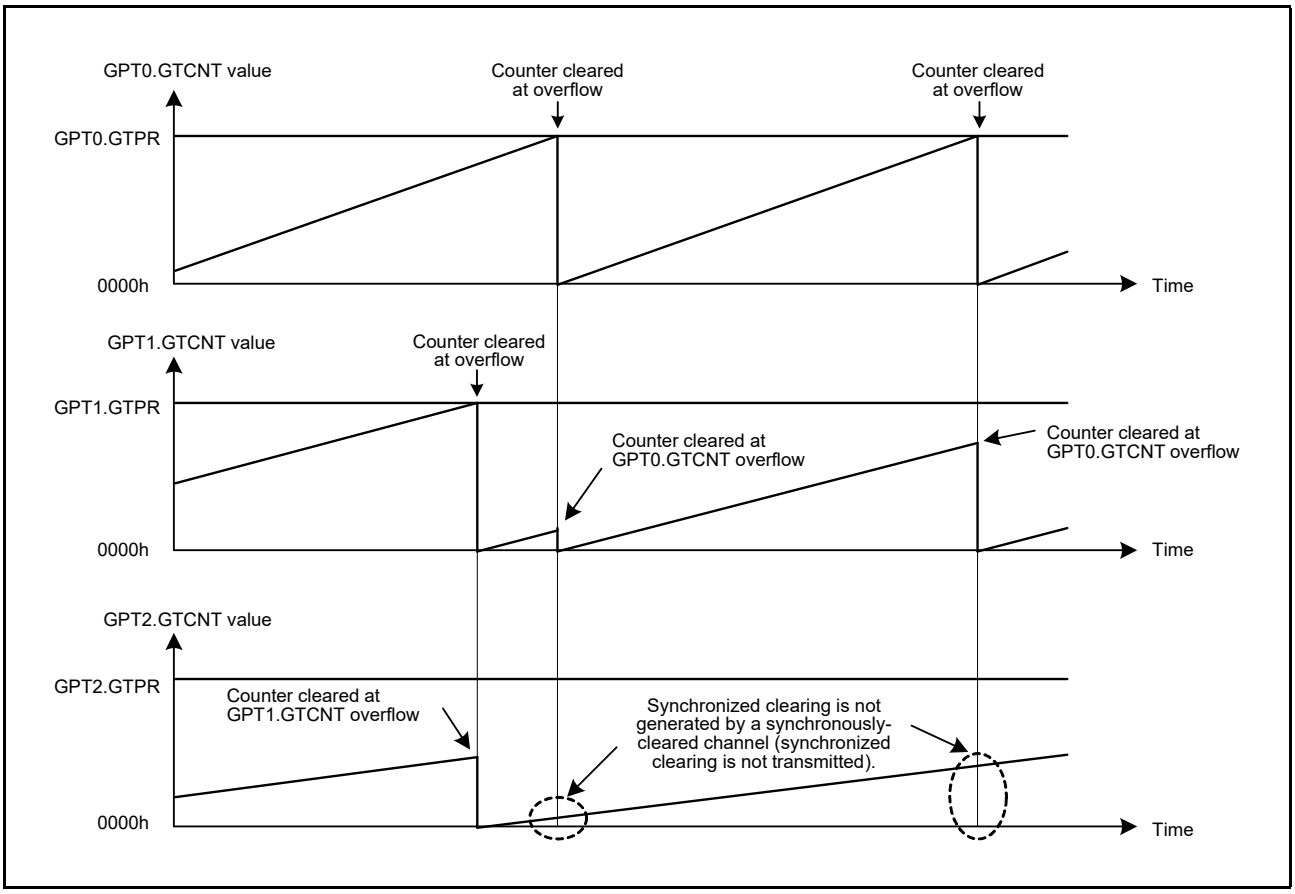


Figure 21.54 Example of Synchronized Clear Operation (GPT1.GTCNT is Synchronously Cleared by GPT0.GTCNT Clearing Source and GPT2.GTCNT is Synchronously Cleared by GPT1.GTCNT Clearing Source)

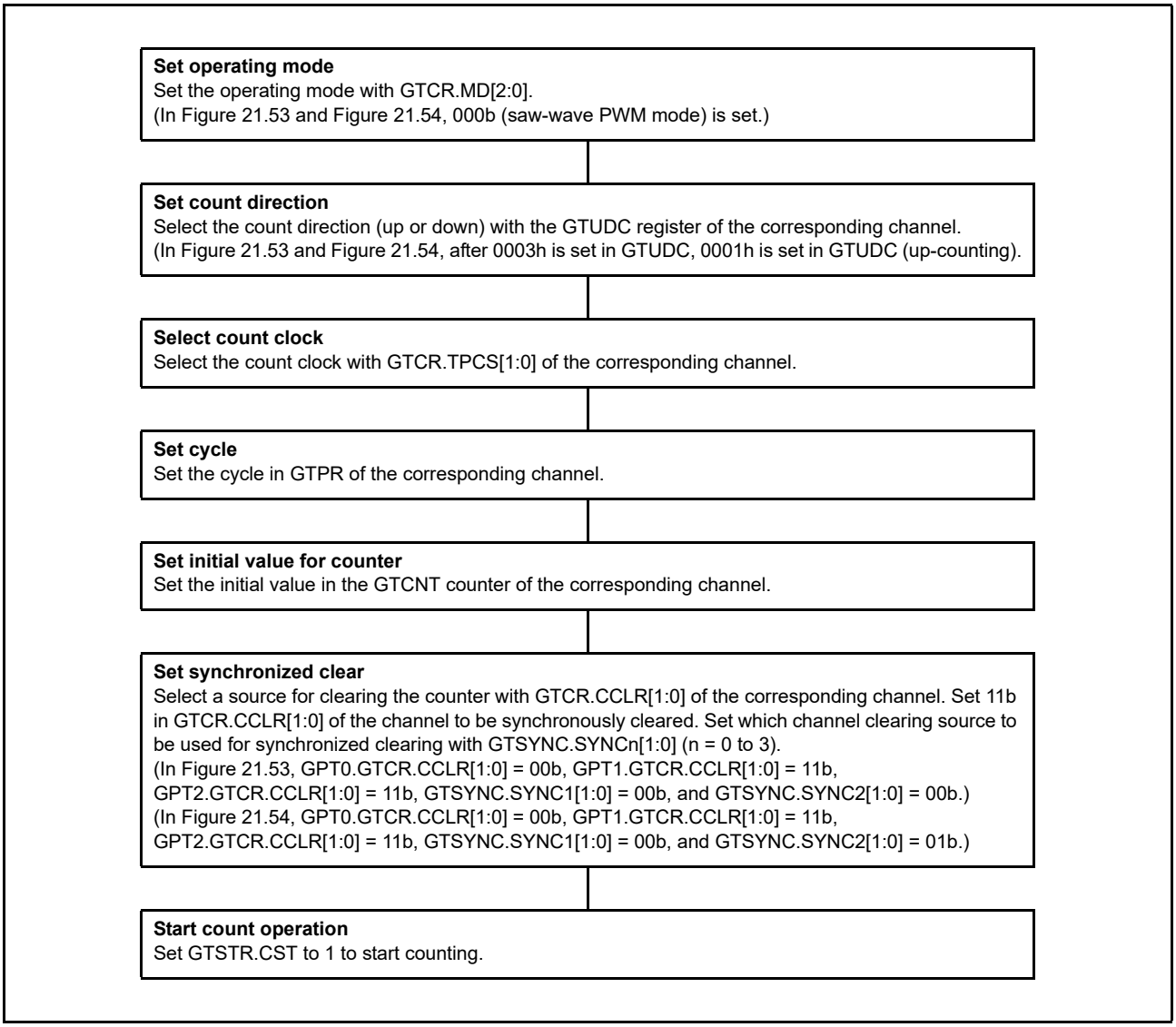


Figure 21.55 Example for Setting Synchronized Clear Operation

21.3.7.2 Synchronized Start Operation

(1) Simultaneous Start by Software

Count operation can be started simultaneously on channels by simultaneously setting the GTSTR.CST bits which correspond to the channels to be started simultaneously to 1 (n = 0 to 3).

Figure 21.56 shows an example of simultaneous start by software.

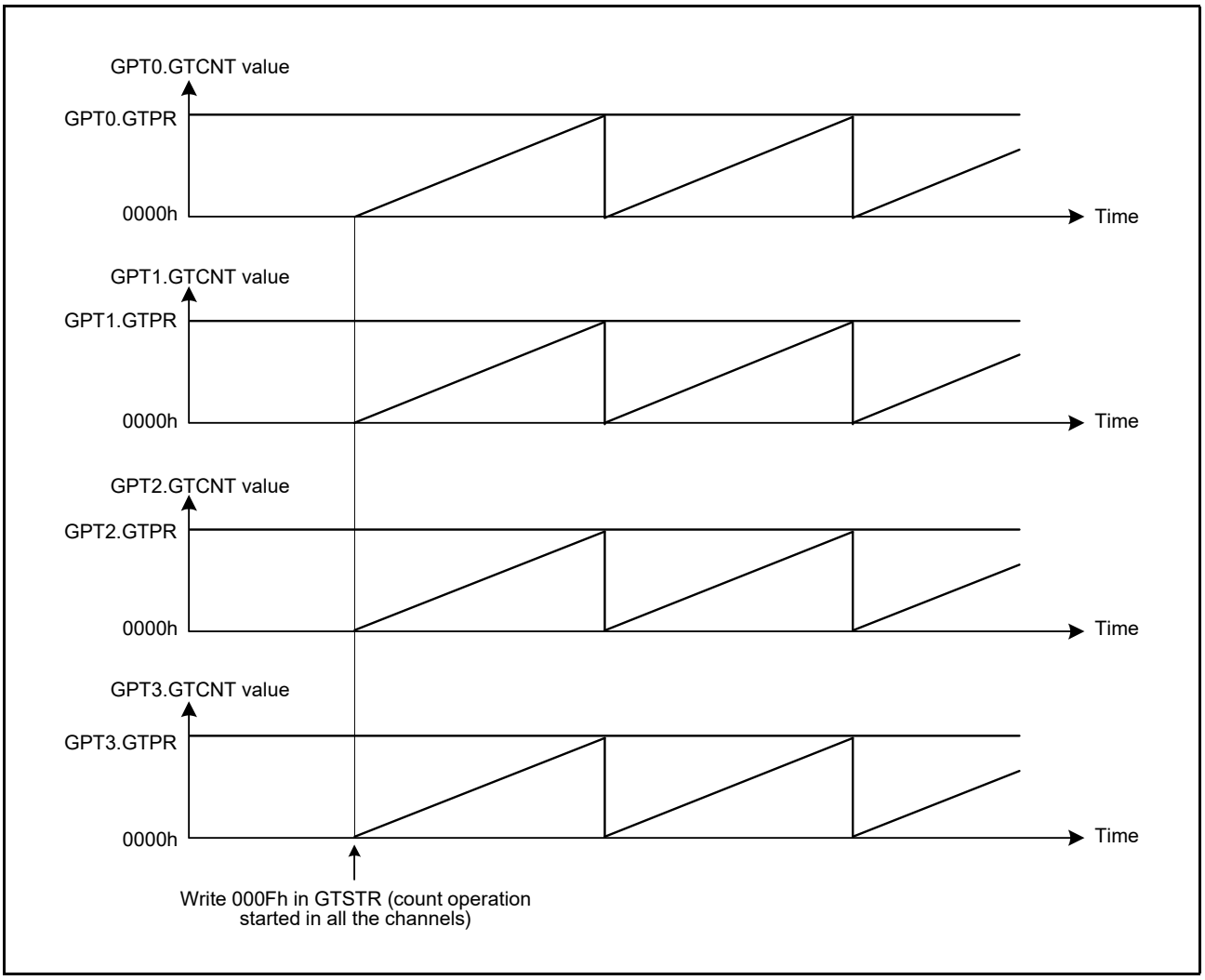


Figure 21.56 Example of Simultaneous Start by Software (with Same Count Cycle (GTPR Value))

(2) Phase Start by Software

Count start with a phase difference is possible by setting the initial value in GCNT before counting starts and then simultaneously setting the CST bits in GTSTR which correspond to the channels to be started simultaneously to 1 (n = 0 to 3).

Figure 21.57 shows an example of phase start operation by software.

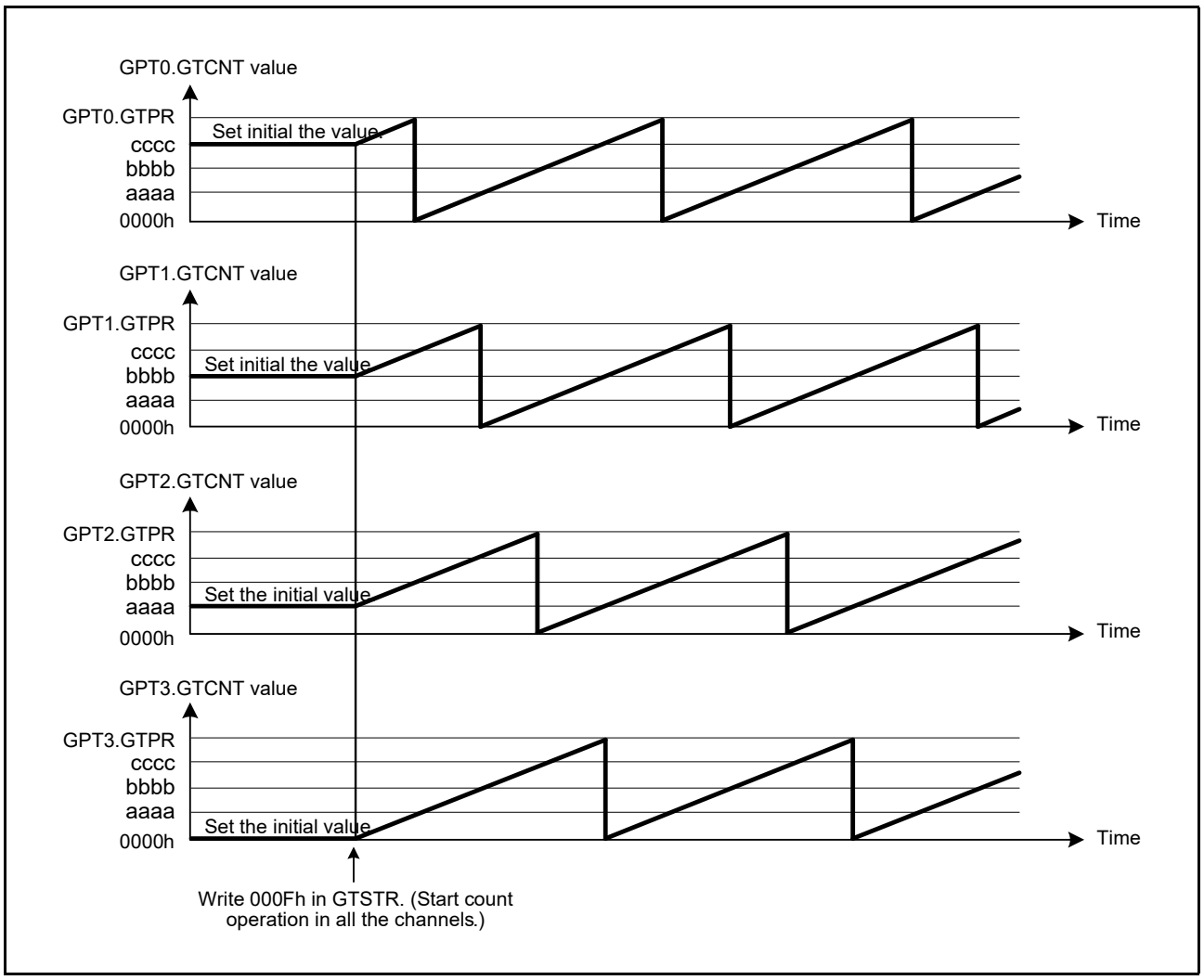


Figure 21.57 Example of Software Phase Start (with Same Count Cycle (GTPR Value))

(3) Simultaneous Start by Hardware Source

Count operation can be started simultaneously on channels by following hardware sources: GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare).
Figure 21.58 shows an example of simultaneous start operation by a hardware source and Figure 21.59 shows the setting example. In this example, count operation is started in all the channels by the input of a signal from the GTiOC3A pin.

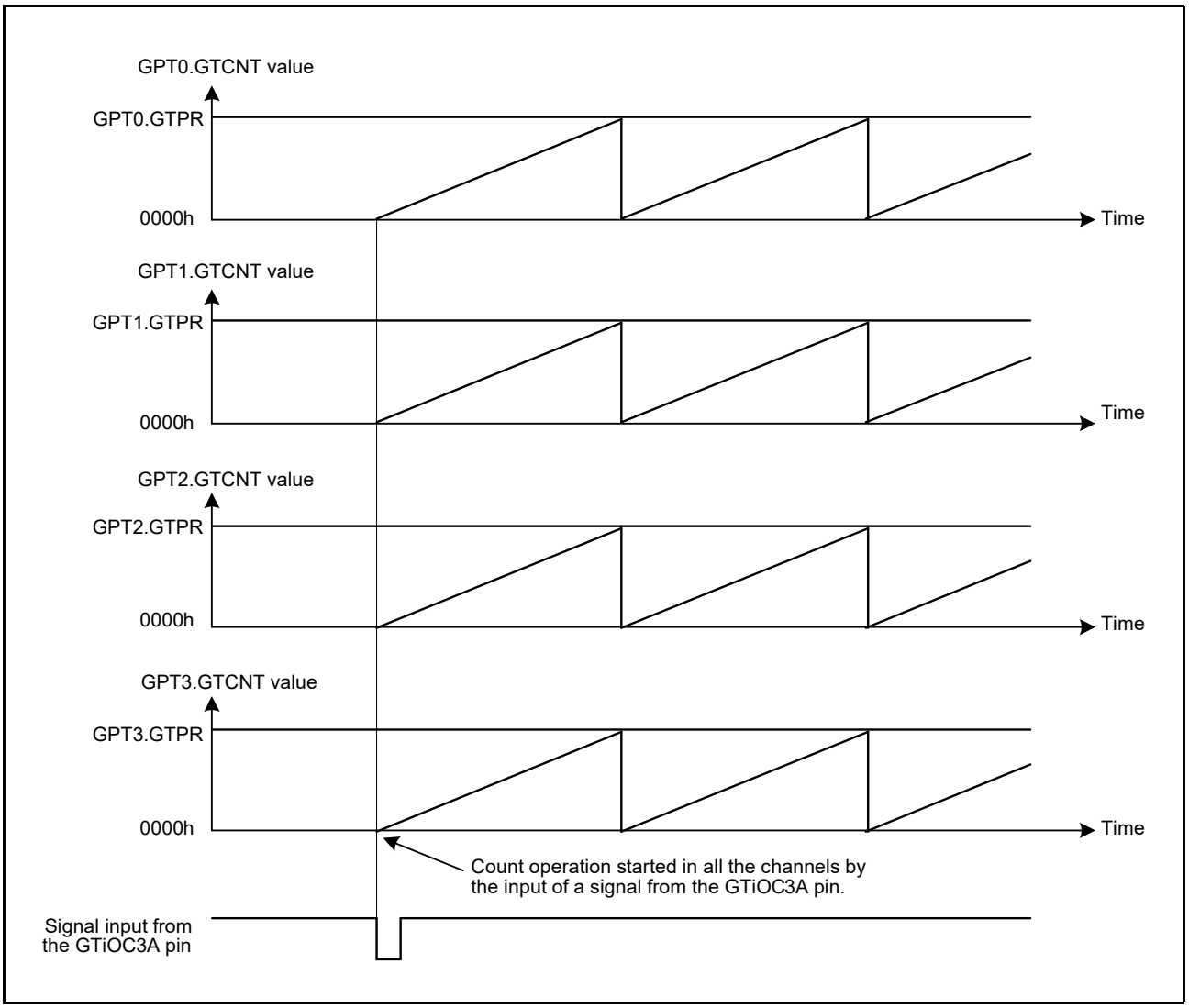


Figure 21.58 Example of Simultaneous Start Operation by Hardware Source (with Same Count Cycle (GTPR Value))

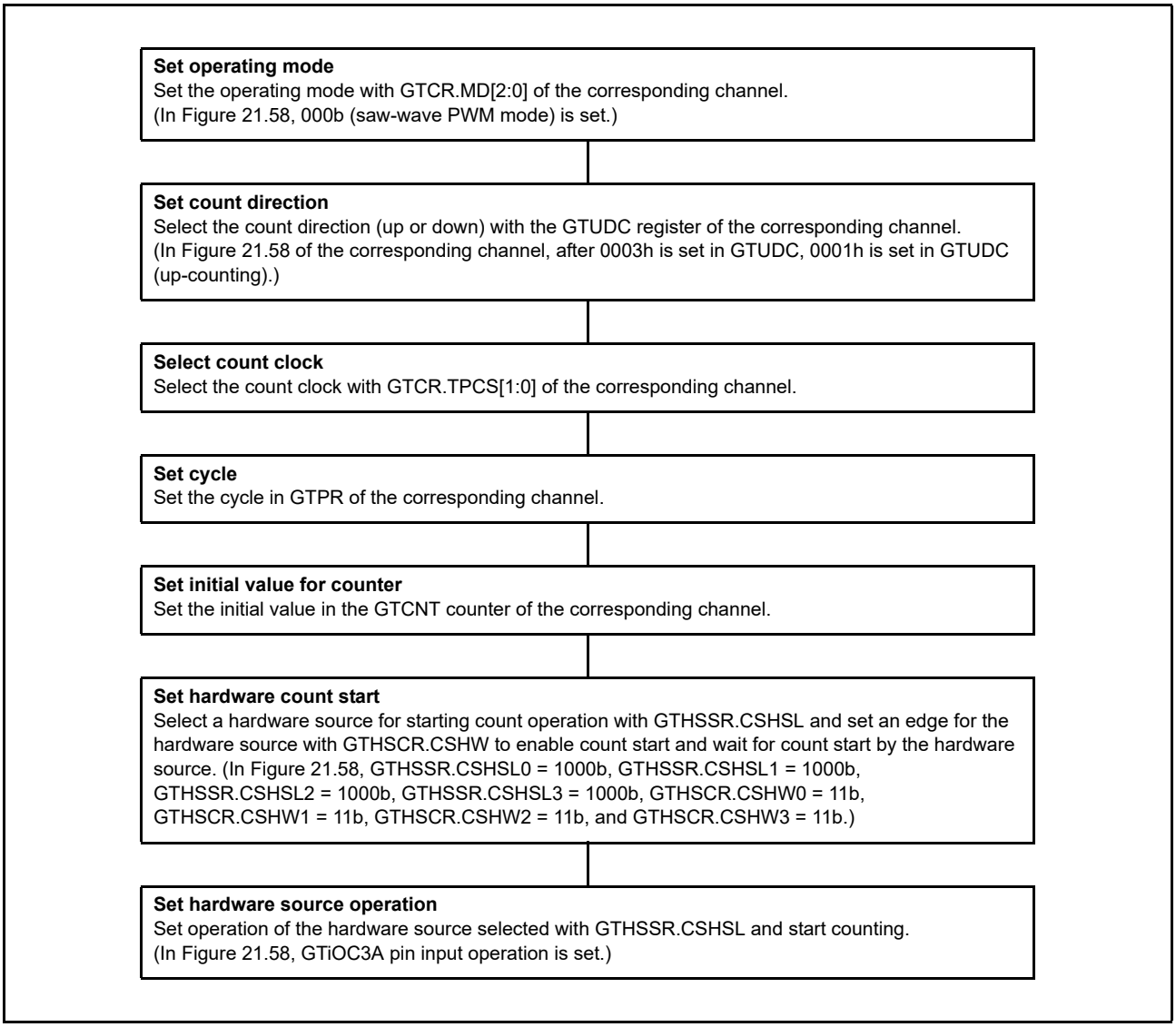


Figure 21.59 Example for Setting Simultaneous Start by Hardware Source

(4) Phase Start by Hardware Source

Count start with a phase difference is possible by following hardware sources: GTETRG pin input, GTIOC3A/GTIOC3B pin input, and GTIOC3A/GTIOC3B internal output (output compare).

Figure 21.60 shows an example of phase start operation by a hardware source and Figure 21.61 shows the setting example. In this example, GPT3.GTCNT and GPT0.GTCNT simultaneously start counting and GPT1.GTCNT and GPT2.GTCNT start counting by the GTIOC3A and GTIOC3B internal outputs (output compare).

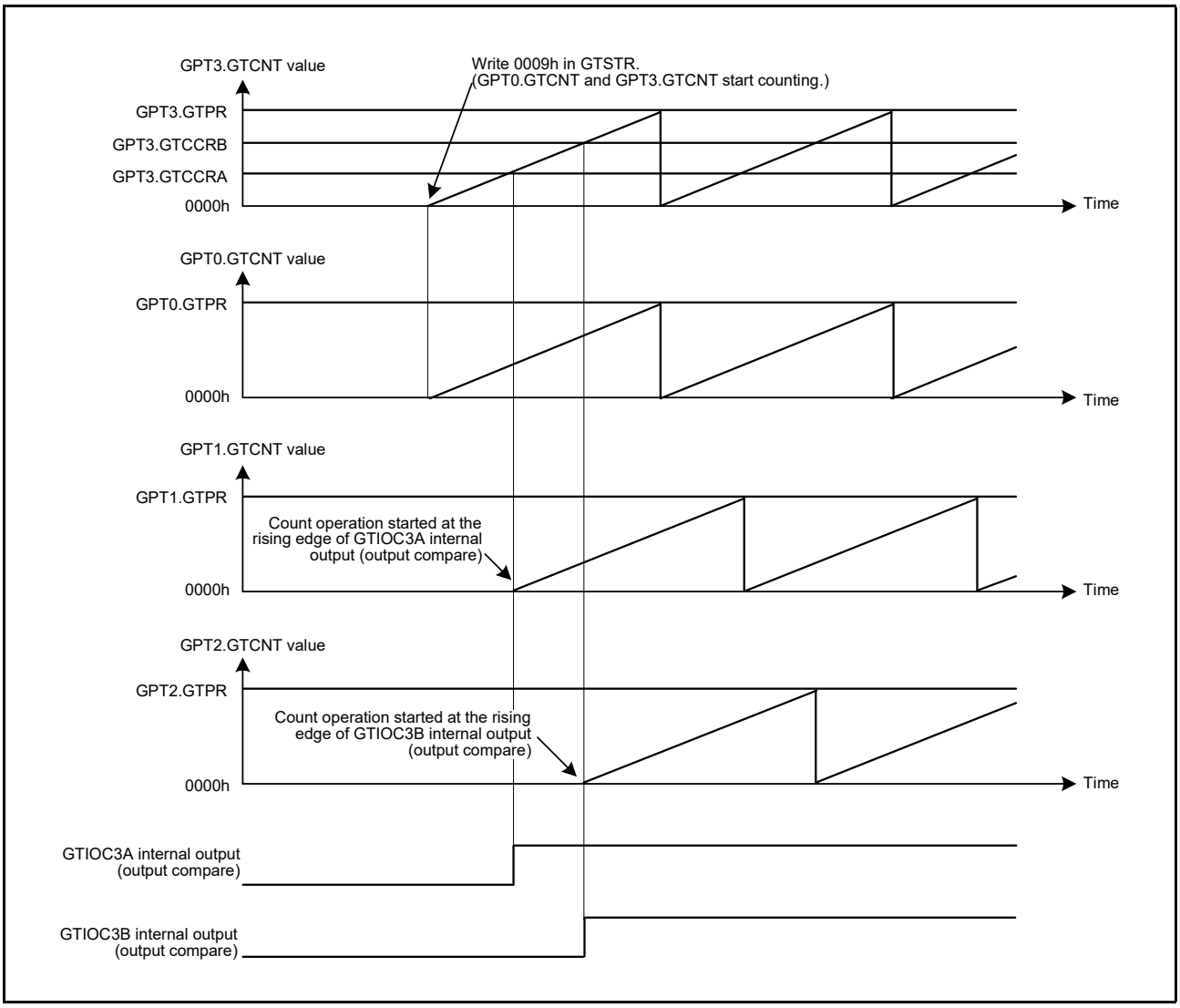


Figure 21.60 Example of Phase Start Operation by Hardware Source (with Same Count Cycle (GTPR Value))

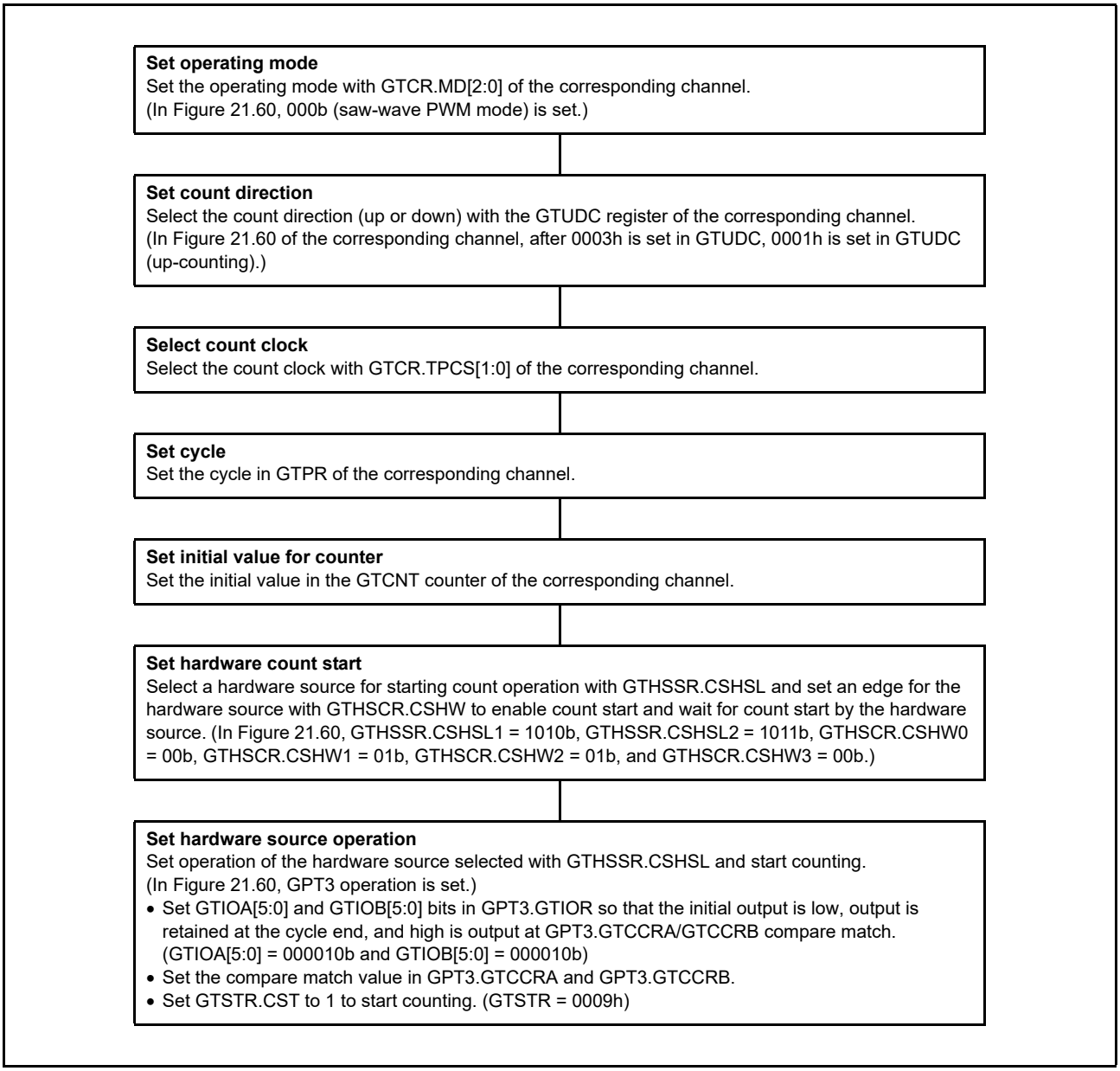


Figure 21.61 Example for Setting Phase Start by Hardware Source

21.3.8 PWM Output Operation Examples

(1) Synchronized PWM Output

The GPT can output eight phases of linked PWM waveforms for a maximum of four channels by synchronizing operation of the channels.

Figure 21.62 shows an example in which all the channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it will output low as the initial value, high at a GTCCRB compare match, and low at the cycle end (n = 0 to 3).

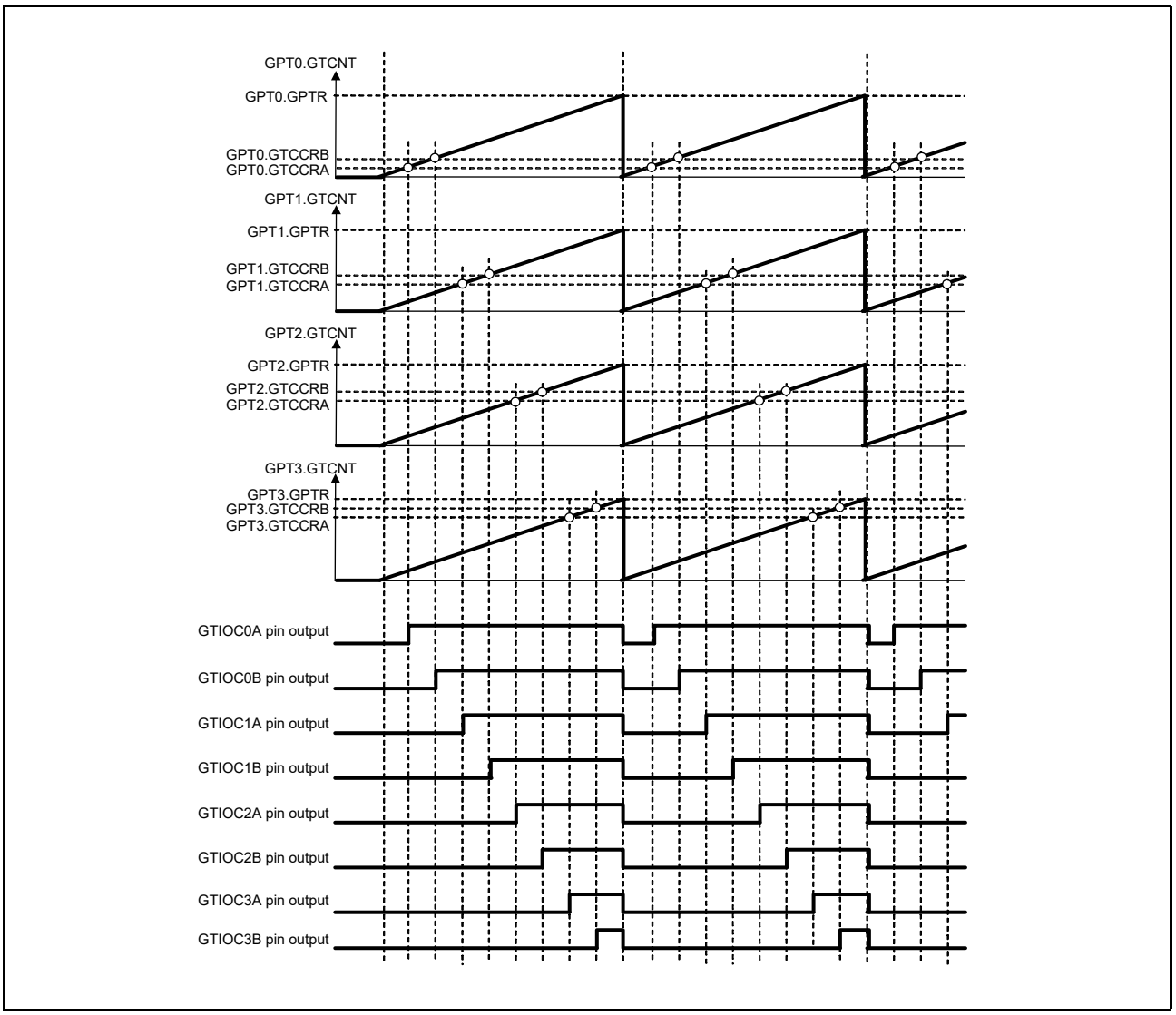


Figure 21.62 Example of Synchronized PWM Output

(2) Three-Phase Saw-Wave Complementary PWM Output

Figure 21.63 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCnB is set so that it will output high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

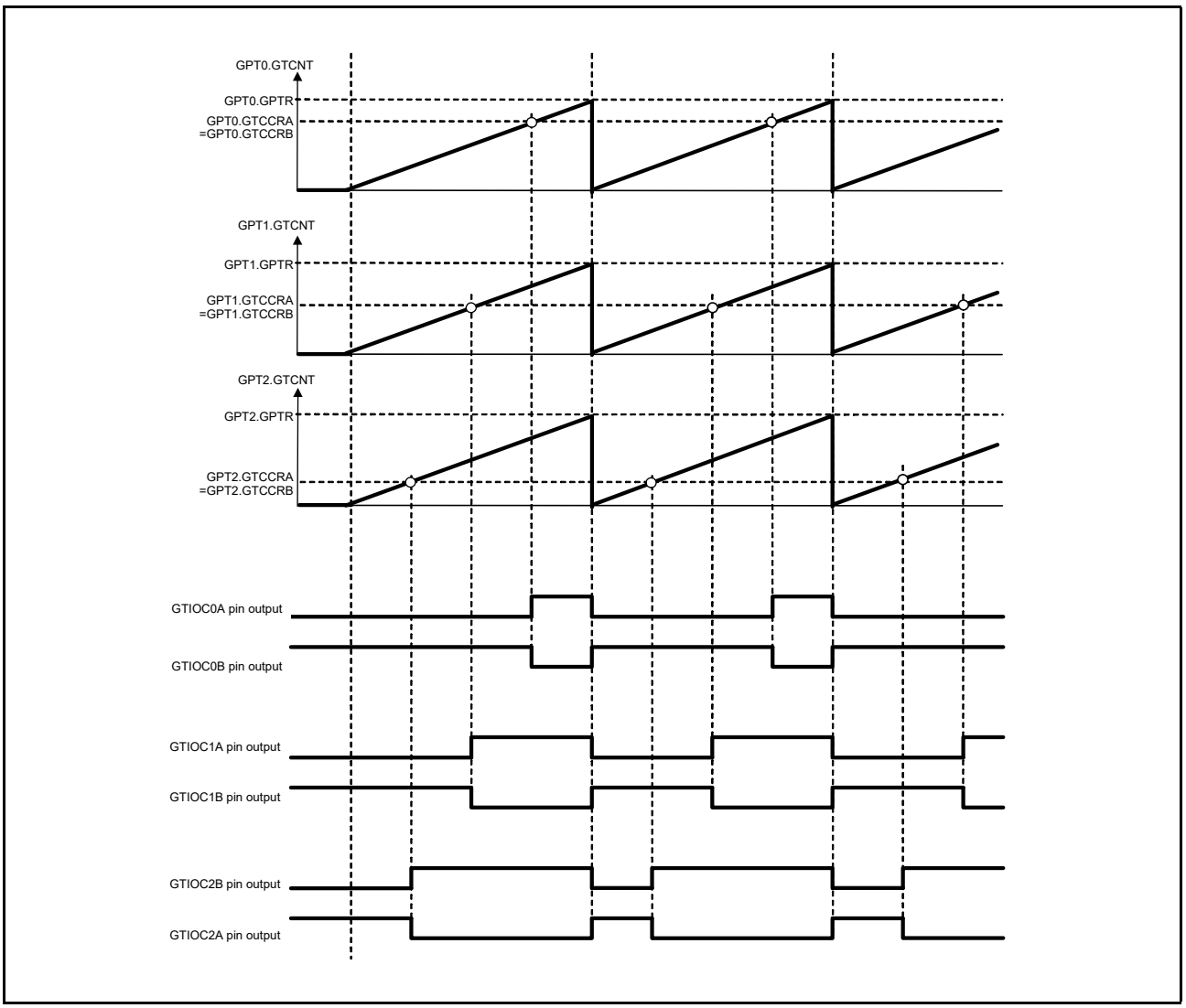


Figure 21.63 Example of Three-Phase Saw-Wave Complementary PWM Output

(3) Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 21.64 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

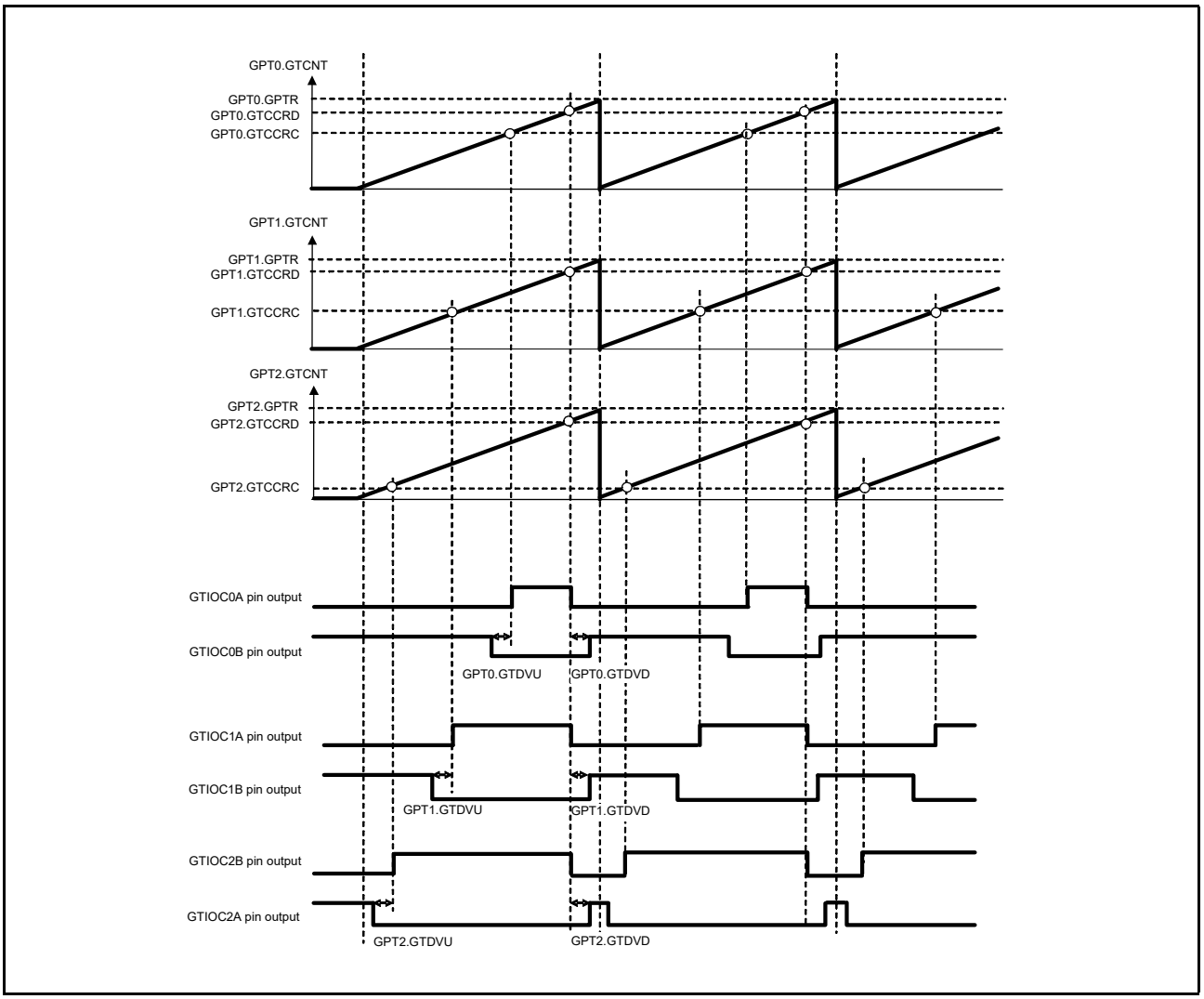


Figure 21.64 Example of Three-Phase Saw-Wave Complementary PWM Output with Automatic Dead Time Setting

(4) Three-Phase Triangle-Wave Complementary PWM Output

Figure 21.65 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

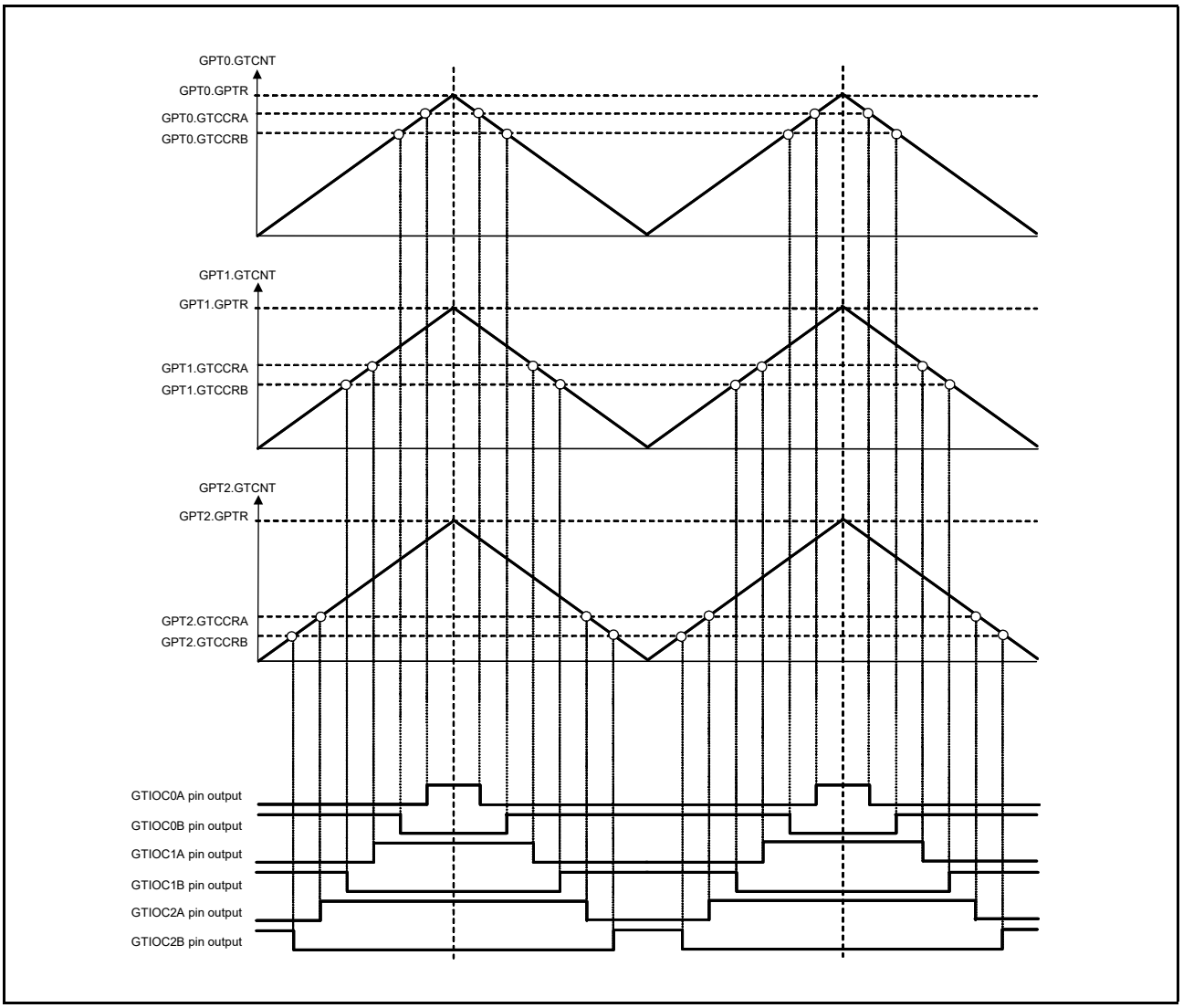


Figure 21.65 Example of Three-Phase Triangle-Wave Complementary PWM Output

(5) Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 21.66 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

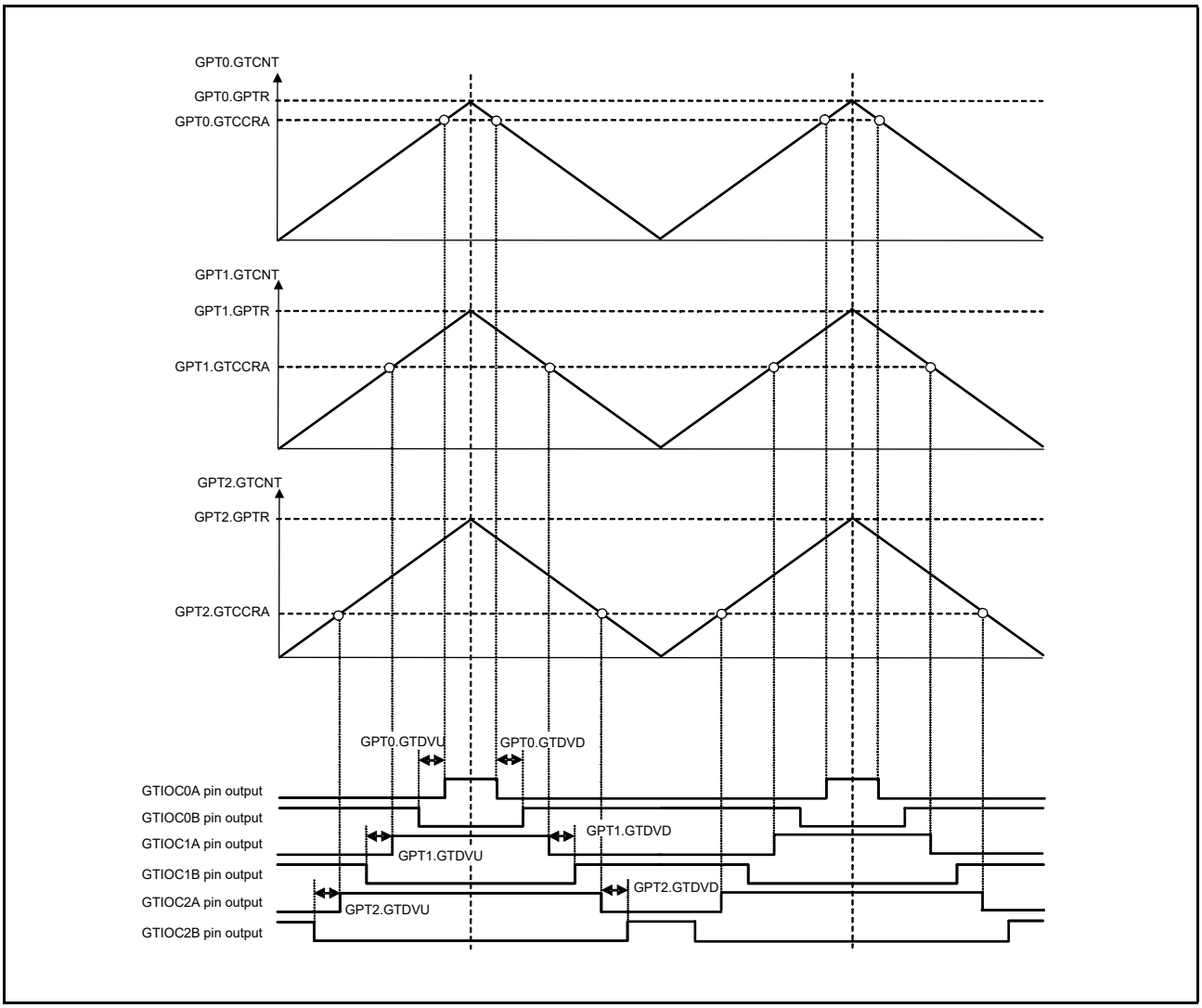


Figure 21.66 Example of Three-Phase Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

(6) Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

Figure 21.67 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and three-phase complementary PWM waveforms are output. The GTIOCnA is set so that it will output low as the initial value, toggle the output at a GTCCRA compare match, and retain the output at the cycle end. The GTIOCnB is set so that it will output high as the initial value, toggle the output at a GTCCRB compare match, and retain the output at the cycle end.

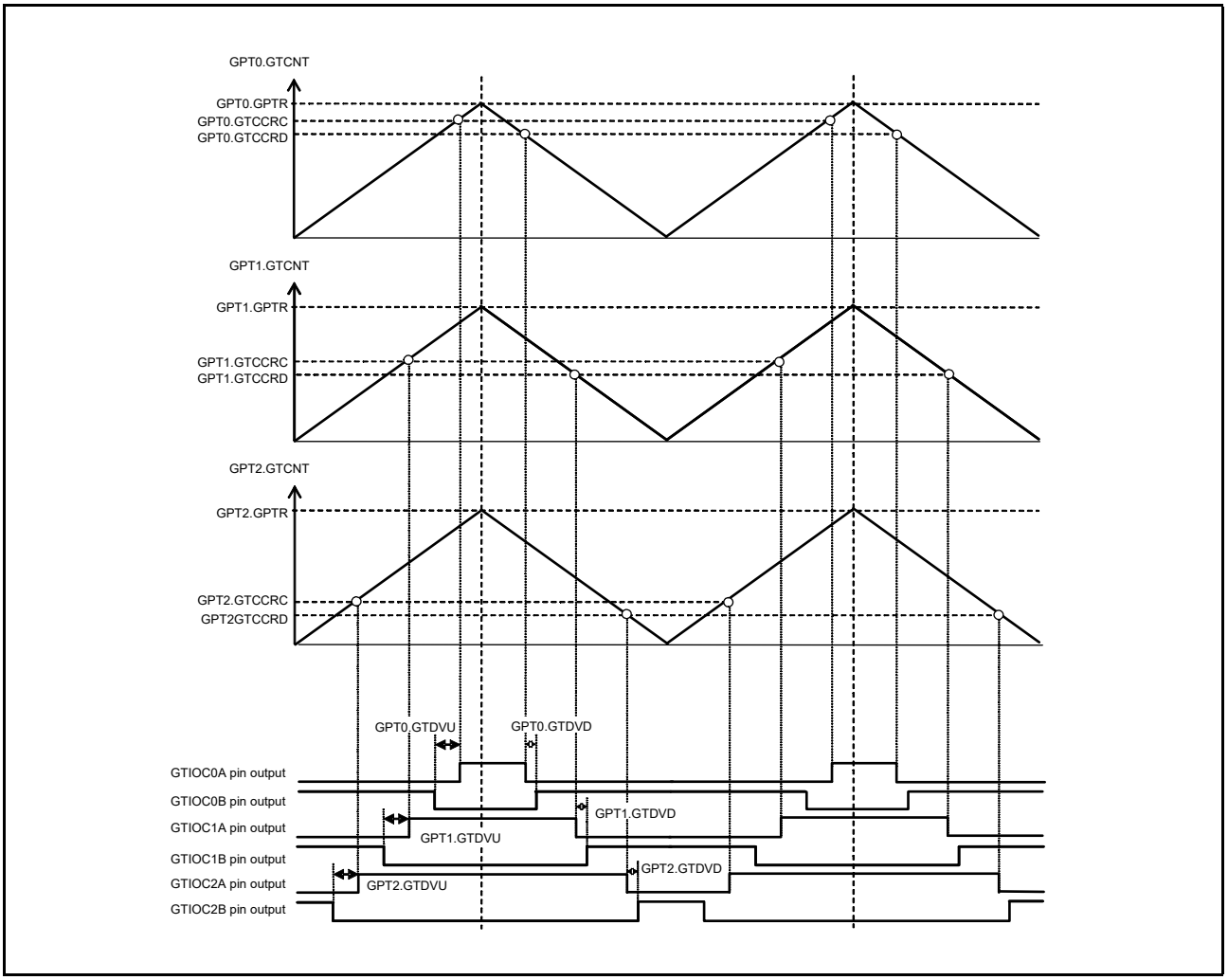


Figure 21.67 Example of Three-Phase Asymmetric Triangle-Wave Complementary PWM Output with Automatic Dead Time Setting

21.3.9 Noise Filter Function

Each pin for use in input capture and external trigger input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses of which length is less than three sampling cycles. The noise filter functionality includes enabling and disabling of the noise filter for each pin and setting of the sampling clock for each channel.

Figure 21.68 shows the timing of noise filtering.

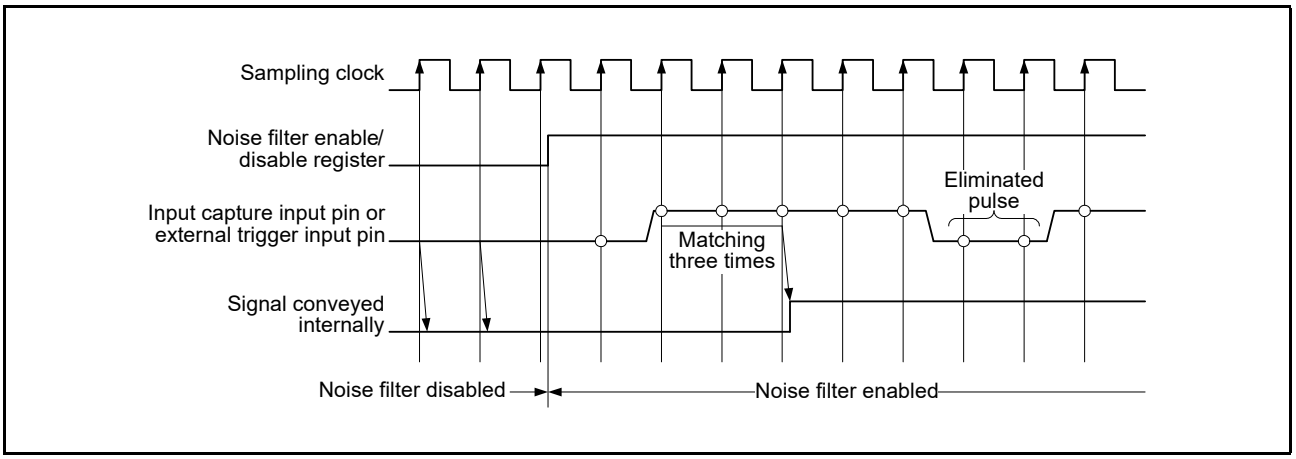


Figure 21.68 Timing of Noise Filtering

If noise filtering is enabled, input capture operation or external trigger operation is performed on the edges of noise-filtered signal after a delay of (minimum sampling interval × 2 + PCLKC) due to noise filtering for the input capture input or external trigger operation.

21.4 Interrupt Sources

21.4.1 Interrupt Sources and Priorities

Table 21.5 lists the GPTa interrupt sources.
Each interrupt source has a control bit for the respective dedicated interrupt request generation and enables or disables the generation of interrupt request independently.
The priority of channels can be changed by the interrupt controller settings. For details, see section 12, Interrupt Controller (ICUA).

Table 21.5 GPT Interrupt Sources (1 / 2)

Channel	Name	Interrupt Source	DMAC Activation
Common	ETGIN	External trigger falling input	Possible
	ETGIP	External trigger rising input	Possible
0	GTCIA0	GPT0.GTCCRA input capture/compare match	Possible
	GTCIB0	GPT0.GTCCRB input capture/compare match	Possible
	GTCIC0	GPT0.GTCCRC compare match	Possible
	GTCID0	GPT0.GTCCRD compare match	Possible
	GDTE0	Dead time error	Possible
	GTCIE0	GPT0.GTCCRE compare match	Possible
	GTCIF0	GPT0.GTCCRF compare match	Possible
	GTCIV0	GPT0.GTCNT overflow (GPT0.GTPR compare match)	Possible
	GTCIU0	GPT0.GTCNT underflow	Possible
1	GTCIA1	GPT1.GTCCRA input capture/compare match	Possible
	GTCIB1	GPT1.GTCCRB input capture/compare match	Possible
	GTCIC1	GPT1.GTCCRC compare match	Possible
	GTCID1	GPT1.GTCCRD compare match	Possible
	GDTE1	Dead time error	Possible
	GTCIE1	GPT1.GTCCRE compare match	Possible
	GTCIF	GPT1.GTCCRF compare match	Possible
	GTCIV1	GPT1.GTCNT overflow (GPT1.GTPR compare match)	Possible
	GTCIU1	GPT1.GTCNT underflow	Possible
2	GTCIA2	GPT2.GTCCRA input capture/compare match	Possible
	GTCIB2	GPT2.GTCCRB input capture/compare match	Possible
	GTCIC2	GPT2.GTCCRC compare match	Possible
	GTCID2	GPT2.GTCCRD compare match	Possible
	GDTE2	Dead time error	Possible
	GTCIE2	GPT2.GTCCRE compare match	Possible
	GTCIF2	GPT2.GTCCRF compare match	Possible
	GTCIV2	GPT2.GTCNT overflow (GPT2.GTPR compare match)	Possible
	GTCIU2	GPT2.GTCNT underflow	Possible

Table 21.5 GPT Interrupt Sources (2 / 2)

Channel	Name	Interrupt Source	DMAC Activation
3	GTCIA3	GPT3.GTCCRA input capture/compare match	Possible
	GTCIB3	GPT3.GTCCRB input capture/compare match	Possible
	GTCIC3	GPT3.GTCCRC compare match	Possible
	GTCID3	GPT3.GTCCRD compare match	Possible
	GDTE3	Dead time error	Possible
	GTCIE3	GPT3.GTCCRE compare match	Possible
	GTCIF3	GPT3.GTCCRF compare match	Possible
	GTCIV3	GPT3.GTCNT overflow (GPT3.GTPR compare match)	Possible
	GTCIU3	GPT3.GTCNT underflow	Possible

Note: This table shows the initial state immediately after a reset. The relative channel priorities can be changed by the interrupt controller.

(1) GTCIAn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTA) in the GTINTAD register is 1, an interrupt request is generated under the following conditions.

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register.
- When the GTCCRA register functions as an input capture register, the input-capture signal has caused transfer of the GTCNT counter value to the GTCCRA register.

(2) GTCIBn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTB) in the GTINTAD register is 1, an interrupt request is generated under the following conditions.

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register.
- When the GTCCRB register functions as an input capture register, the input-capture signal has caused transfer of the GTCNT counter value to the GTCCRB register.

(3) GTCICn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTC) in the GTINTAD register is 1, an interrupt request is generated under the following condition.

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register)

(4) GTCIDn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTD) in the GTINTAD register is 1, an interrupt request is generated under the following condition.

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register)

(5) GTCIEn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTE) in the GTINTAD register is 1, an interrupt request is generated under the following condition.

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register)

(6) GTCIFn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTF) in the GTINTAD register is 1, an interrupt request is generated under the following condition.

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register.

A compare match is not performed and thus interrupt is not requested under the following conditions.

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register)

(7) GTCIVn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTPR[0]) in the GTINTAD register is 1, an interrupt request is generated under the following conditions.

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value matches with the GTPR register during up-counting).
- In triangle-wave mode, interrupt requests are enabled at crests (GTCNT = GTPR).

(8) GTCIUn interrupt (n = 0 to 3)

When the interrupt enable bit (GTINTPR[1]) in the GTINTAD register is 1, an interrupt request is generated under the following conditions.

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value reaches 0 during down-counting).
- In triangle-wave mode, interrupt requests are enabled at troughs (GTCNT = 0).

(9) ETGIP interrupt

When the interrupt enable bit (ETIPEN) in the GTETINT register is 1, an interrupt request is generated under the following condition.

- When the rising edge of an external trigger input is detected

(10) ETGIN interrupt

When the interrupt enable bit (ETINEN) in the GTETINT register is 1, an interrupt request is generated under the following condition.

- When the falling edge of an external trigger input is detected

(11) GDTEn interrupt (n = 0 to 3)

When automatic dead time setting has been made, the GTST.DTEF flag becomes 1 when the timer output toggle point with dead time added exceeds the timer cycle. If GTINTAD.EINT is 1 at this time, a dead time error interrupt request (GDTE) is generated.
In addition, when the timer output toggle point with dead time added is back within the timer cycle, the GTST.DTEF flag changes from 1 to 0.

21.4.2 DMAC Activation

The DMAC can be activated by the interrupt in each channel. For details, see section 12, Interrupt Controller (ICUA) and section 15, DMA Controller (DMACAa).

21.4.3 Interrupt and A/D Conversion Request Skipping Function

By setting the GTITC register, the GTCNT counter overflows (GTPR compare matches) (GTCIV) or underflow interrupts (GTCIU) can be skipped. Other interrupts and A/D converter start request signals can be skipped in coordination with the GTCIV/GTCIU skipping function. However, the dead time error interrupts cannot be linked with the GTCIV/GTCIU skipping function.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GTCIV/GTCIU interrupt requests cannot be generated at troughs only or at crests only depending on the skipping counter start timing. Therefore, in order to count both troughs and crests and generate the GTCIV/GTCIU interrupts at troughs only or crests only in triangle-wave mode, the number of times of skipping should be even.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GTCIV interrupt requests cannot be generated at overflows only or at underflows only. Therefore, in order to count both overflows and underflows with the count direction changed and generate the GTCIV/GTCIU interrupts at overflows only or underflows only in saw wave mode, the skipping state should be carefully checked before using.

When changing the skipping count, be sure to release the skipping count setting (GTITC.IVTC[1:0] = 00b).

Figure 21.69 to Figure 21.74 show examples of skipping function operation.

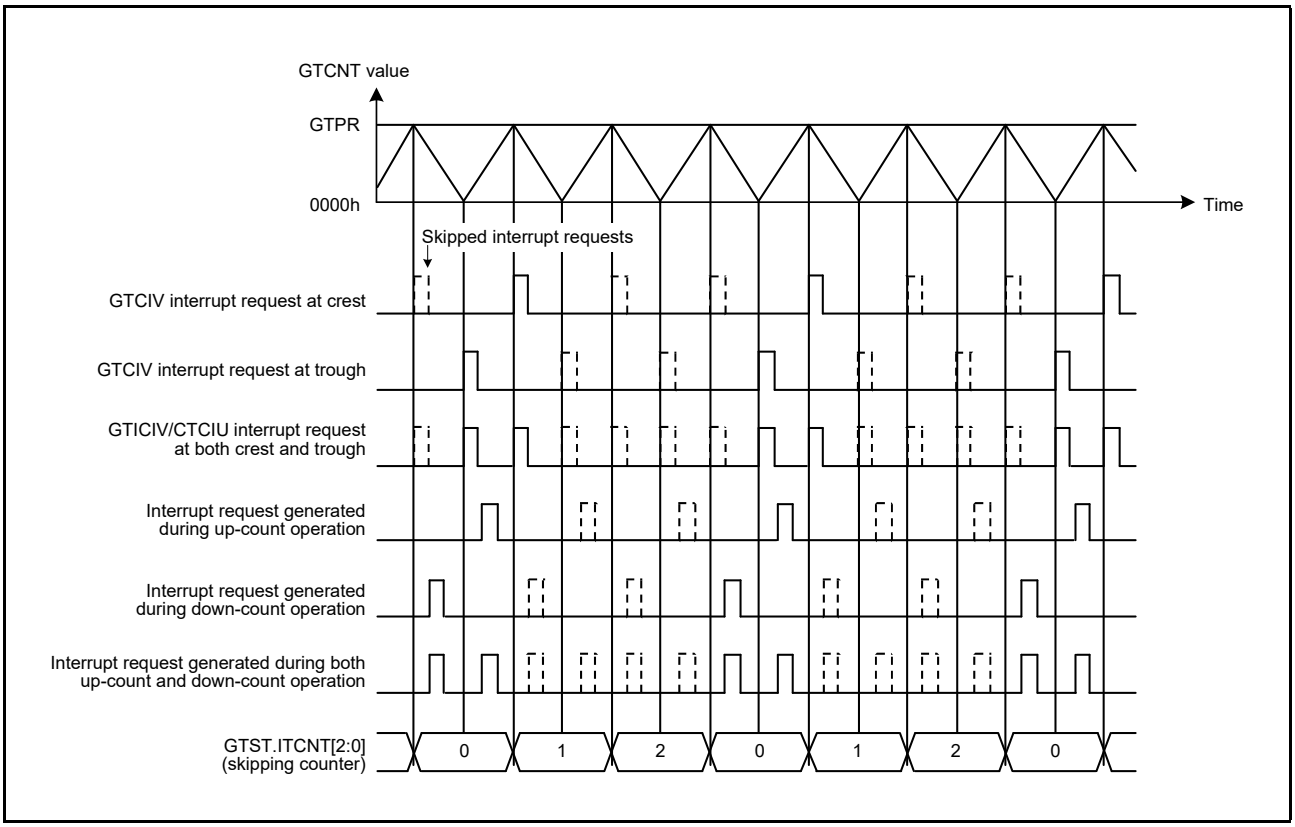


Figure 21.69 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Crests, Skipping Count: 2)

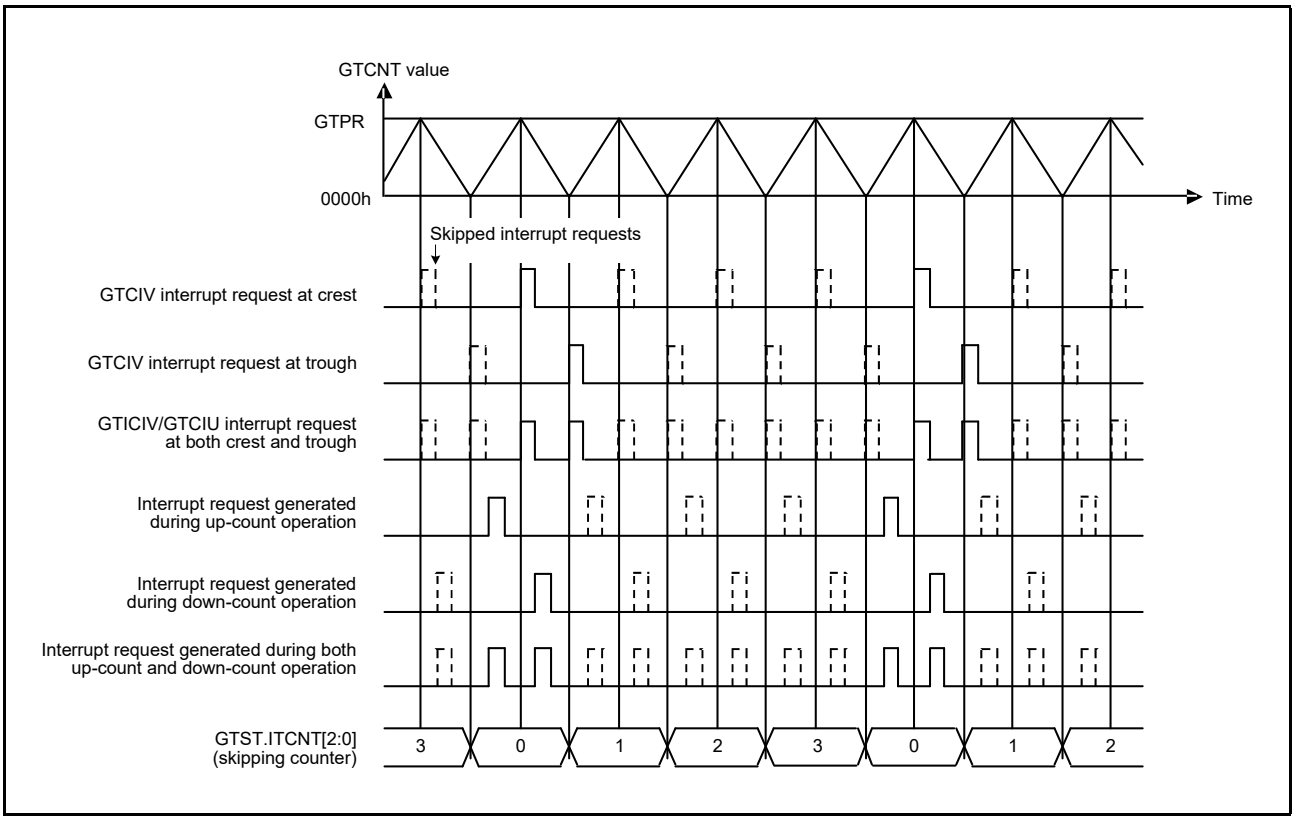


Figure 21.70 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Troughs, Skipping Count: 3)

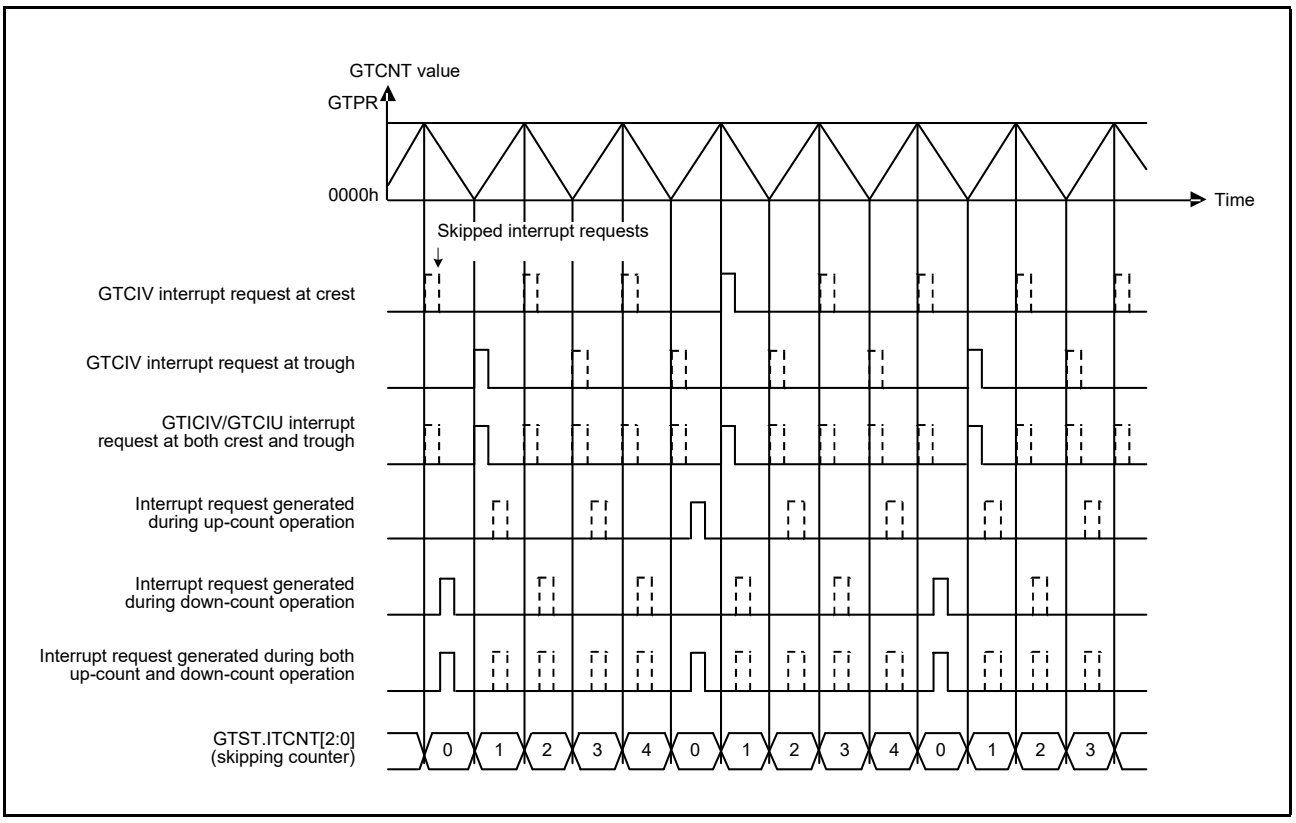


Figure 21.71 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 4)

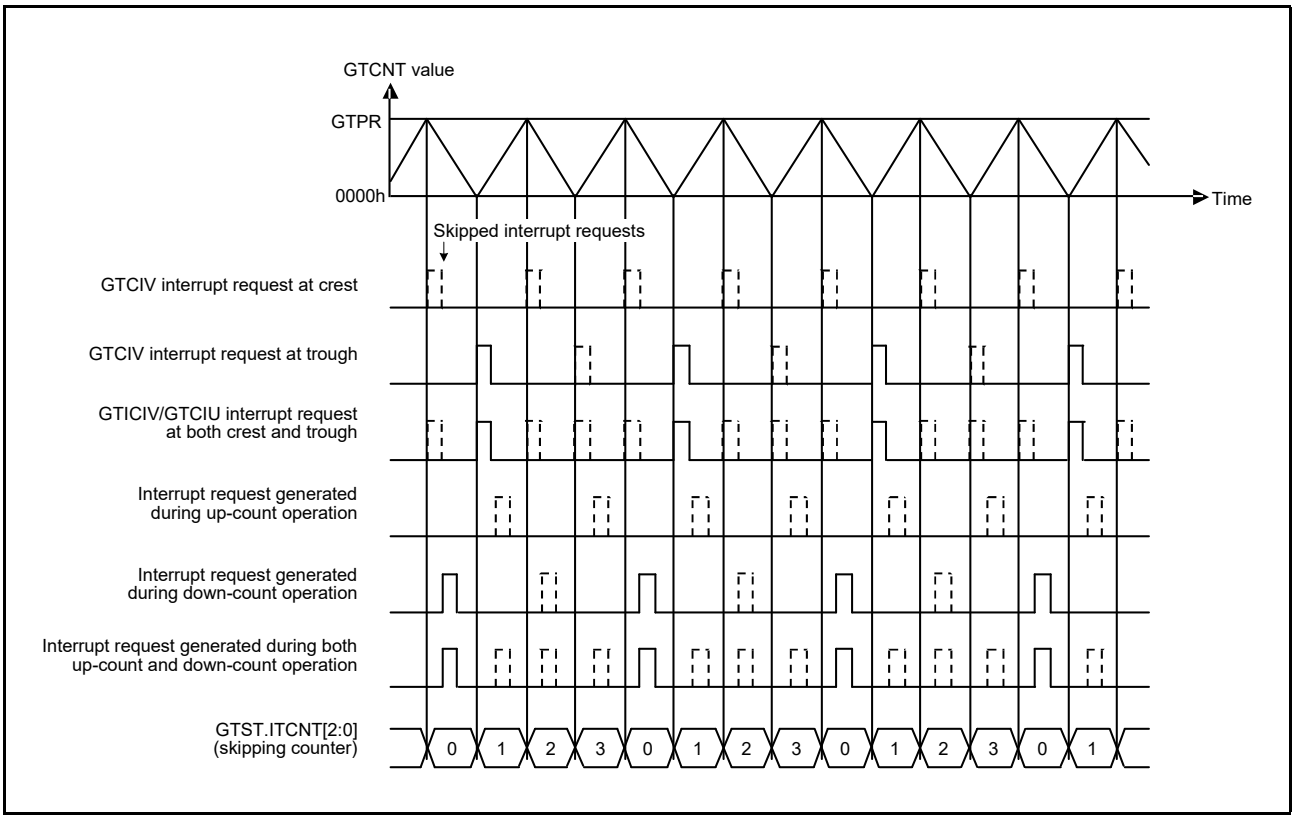


Figure 21.72 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Up-Counting)

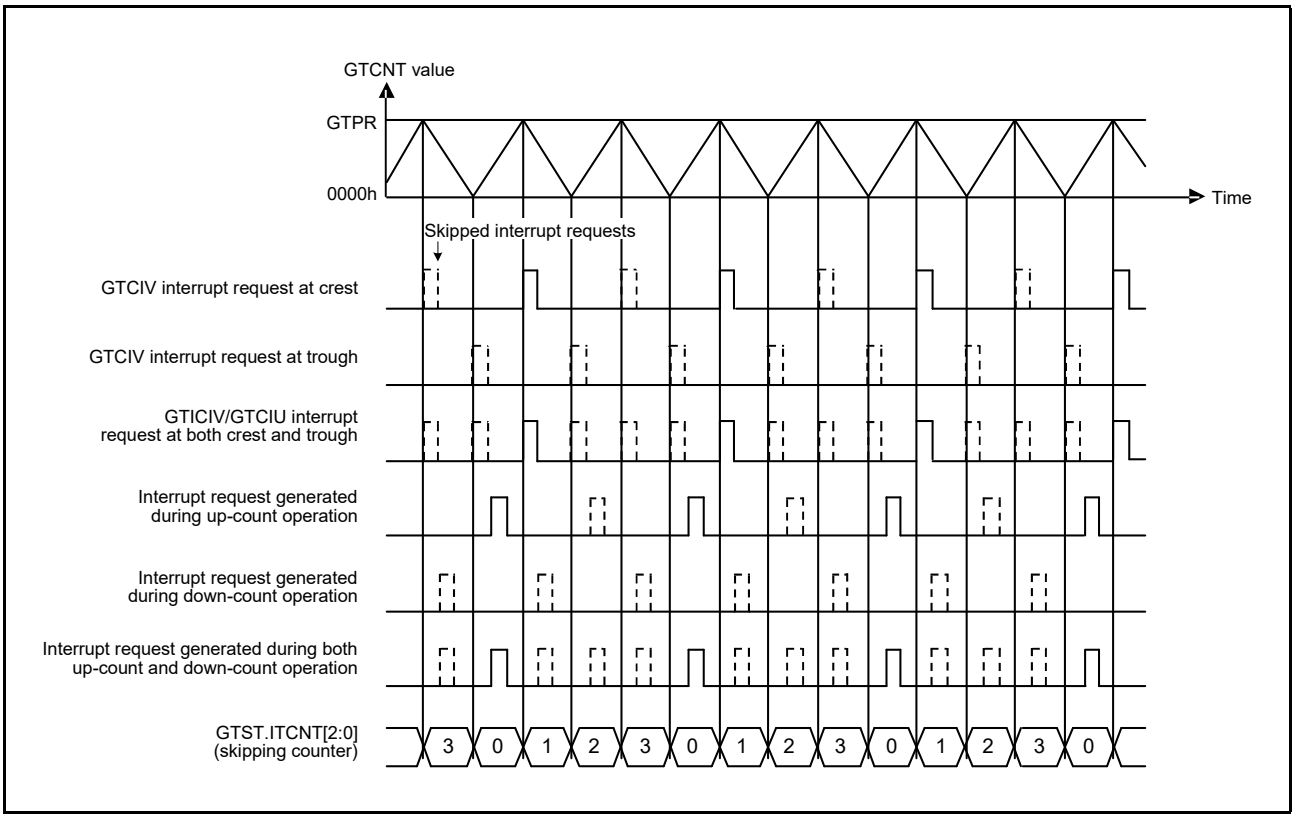


Figure 21.73 Example of Interrupt Skipping Function Operation (Triangle Waves, Counting and Skipping Both Troughs and Crests, Skipping Count: 3, Skipping Started at Down-Counting)

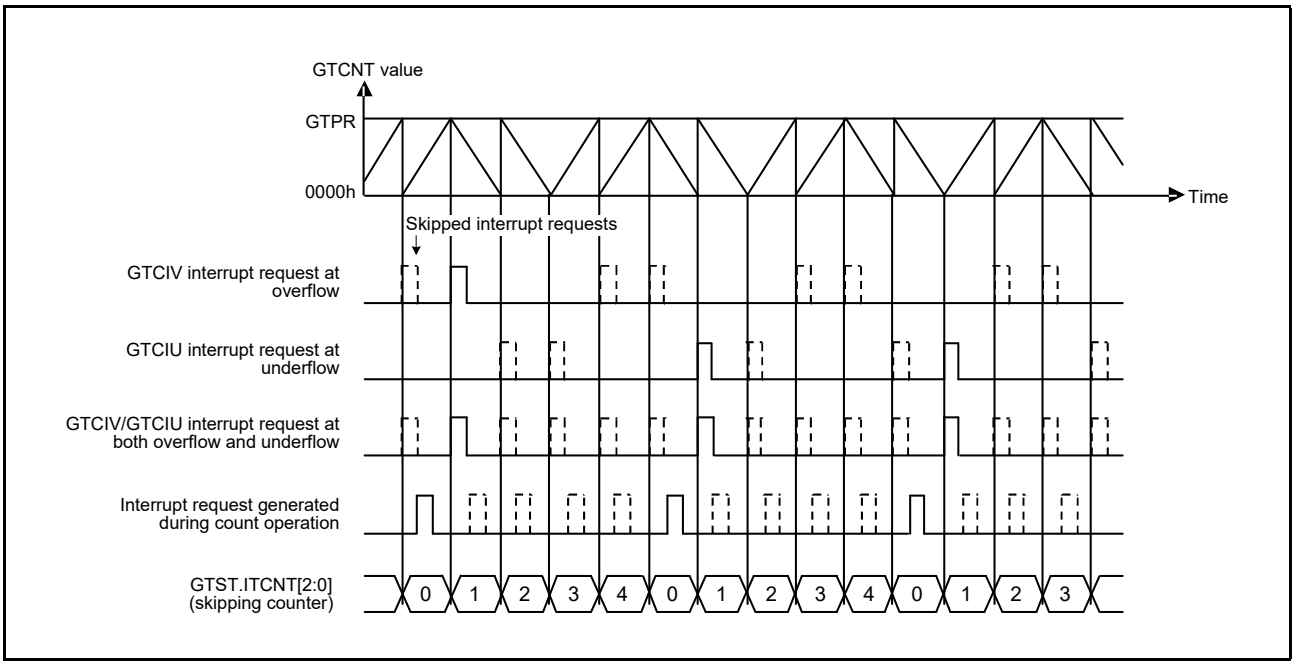


Figure 21.74 Example of Interrupt Skipping Function Operation (Saw Waves, Operation with Count Direction Changed, Counting and Skipping Both Overflows and Underflows, Skipping Count: 4)

21.5 A/D Converter Start Request

An A/D converter start request can be issued at a compare match between the GTCNT counter and GTADTRA or GTADTRB, and up-counting only, down-counting only, or both up-counting and down-counting can be specified. GTADTRA and GTADTRB each has two buffer registers. Buffer operation with GTADTRA used together with GTADTBRA and GTADTDBRA, and buffer operation with GTADTRB used together with GTADTBRB and GTADTDBRB can be performed.

Figure 21.75 shows an example of A/D converter start request operation, and Figure 21.76 shows an example for setting A/D converter start request operation.

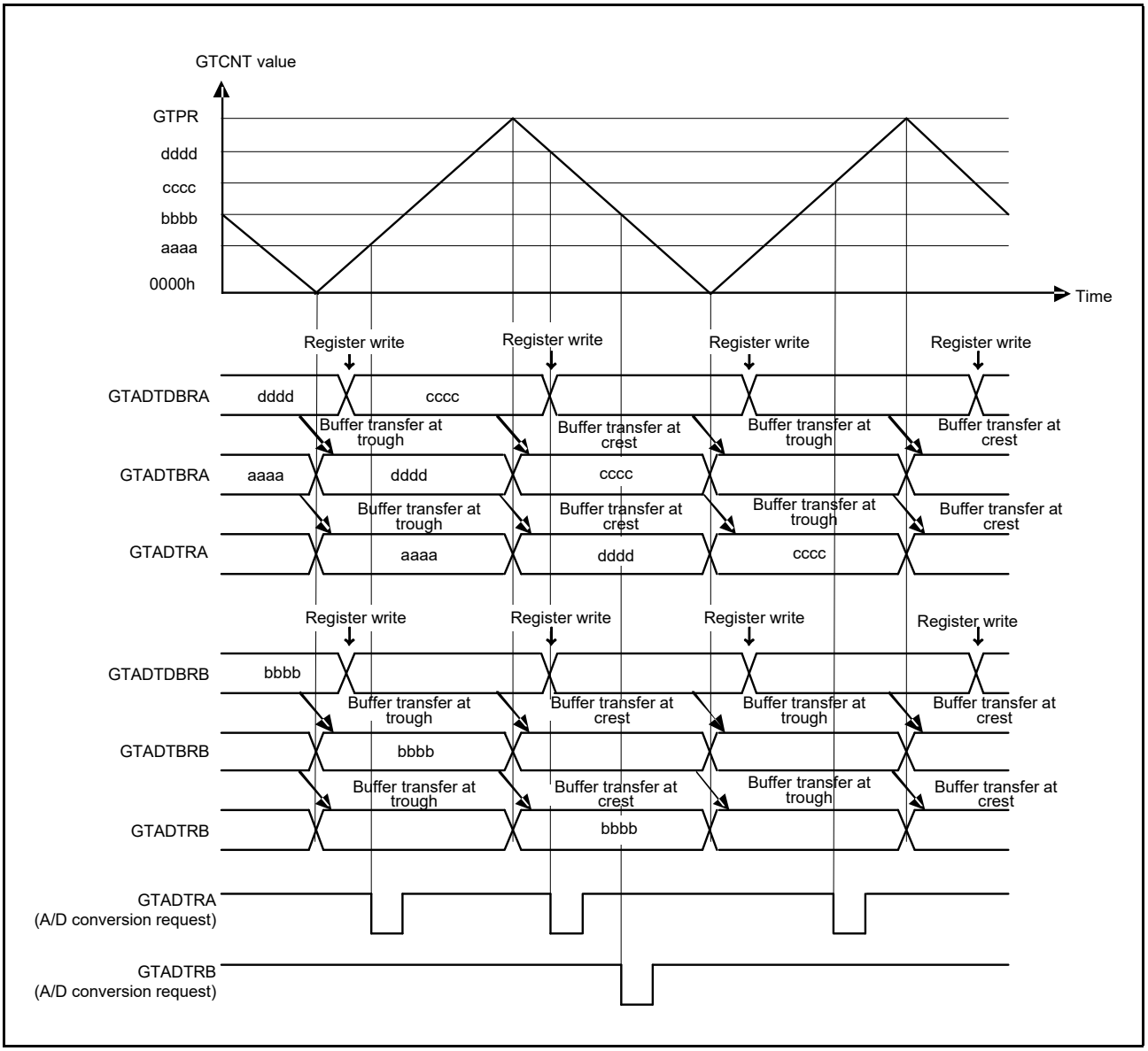


Figure 21.75 Example of A/D Converter Start Request Timing Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests, A/D Converter Start Requested by GTADTRA0 at Both Up-Counting and Down-Counting, A/D Converter Start Requested by GTADTRB0 at Down-Counting)

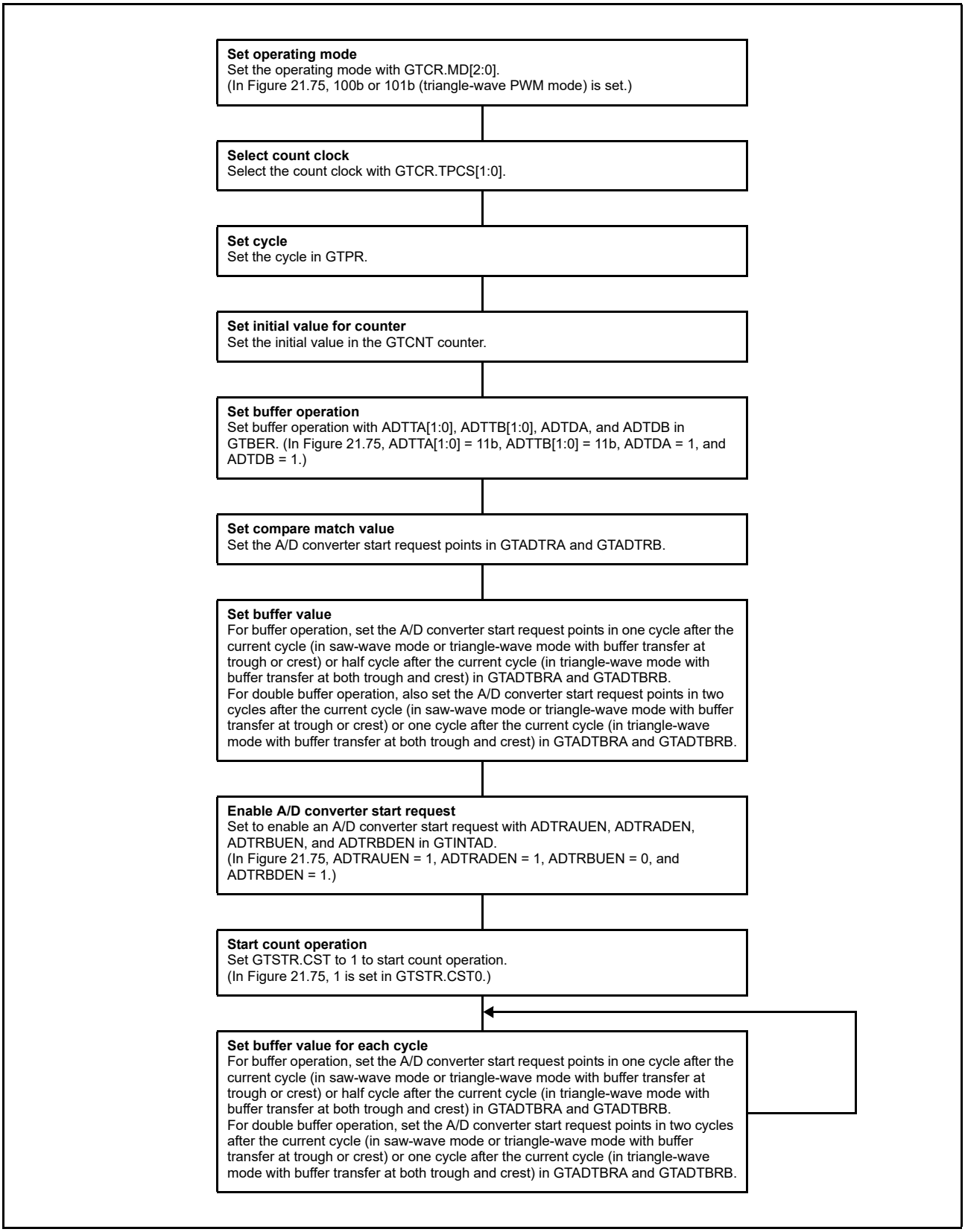


Figure 21.76 Example for Setting A/D Converter Start Request Timing Operation

21.6 Operations Linked by the ELC

21.6.1 Event Signal Output to the ELC

GPT is capable of operation linked with another module set in advance when its interrupt request signal is used as an event signal by the event link controller (ELC).
GPT outputs the event signal regardless of the setting of the corresponding interrupt request enable bit.
For details, see section 16, Event Link Controller (ELC).

21.6.2 GPT Operations in Response to Receiving Event Signals from the ELC

The GPT can perform the following operations in response to the event set in advance in the ELSRn register of the event link controller (ELC).

(1) Start Counting

Counting by the GPT starts in response to the event when this is selected by the setting of the ELOPI or ELOPJ register of the ELC. The ELOPI register handles control for GPT0 to 2 and the ELOPJ register handles control for GPT2 and 3.
When the start event specified in the ELSRn register occurs, the CSTn bit in the GTSTR register (timer start register) shown in Table 21.6 is set to 1, and the GPT counter starts.
However, when the specified count start event is generated while the CSTn bit in the GTSTR register (timer start register) has already been set to 1, the event has no effect. Table 21.6 lists the GTSTR register bits used for each channel.

Table 21.6 Operation of the GTSTR register (timer start register) in response to the ELC

Channel No.	GTSTR Register (Timer Start Register)
Channel 0	GTSTR.CST0 bit
Channel 1	GTSTR.CST1 bit
Channel 2	GTSTR.CST2 bit
Channel 3	GTSTR.CST3 bit

(2) Input Capture Operation

Input capture by the GPT proceeds when this is selected by the setting of the ELOPI or ELOPJ register of the ELC. The ELOPI register handles control for GPT0 and 1 and the ELOPJ register handles control for GPT2 and 3. When the event specified in the ELSRn register occurs, the GTCCR register (general PWM timer compare capture register) captures the value of the GTCNT register (general PWM timer counter). When using input capture in response to an event, the corresponding bit of the GTIOR register (general PWM timer I/O control register) in the GPT should be set for input capture and the CSTn bit of GTSTR register (timer start register) should be set to 1 to start counting by the counter.
In this case, the GTIOCnA pin (input capture pin) input has no effect.
Table 21.7 lists the GTCCR and GTIOR registers used for each channel in input capture operation in response to the ELC.

Table 21.7 Registers Used in the Input Capture Operation by ELC

Channel No.	Timer General Register Name	Timer I/O Control Register
Channel 0	GPT0.GTCCRA bit	GPT0.GTIOR.GTIOA[5:0] bit
Channel 1	GPT1.GTCCRA bit	GPT1.GTIOR.GTIOA[5:0] bit
Channel 2	GPT2.GTCCRA bit	GPT2.GTIOR.GTIOA[5:0] bit
Channel 3	GPT3.GTCCRA bit	GPT3.GTIOR.GTIOA[5:0] bit

(3) Clear Counting

Counting by GPTa is cleared when this is selected by the setting of the ELOPI or ELOPJ register of the ELC. The ELOPI register handles control for GPT0 and 1 and the ELOPJ register handles control for GPT2 and 3. When the event specified in the ELSRn register occurs while count clearing is set by the associated bit, the GTCNT counter (timer counter) is returned to its initial value. If the corresponding CSTn bit in the GTSTR register (timer start register) is set to 1 (count operation is performed), counting continues, i.e. counting is restarted. For the CSTn bits in the GTSTR register, see Table 21.6.

(4) Stop Counting

Counting by GPTa stops when this is selected by the setting of the ELOPI or ELOPJ register of the ELC. The ELOPI register handles control for GPT0 and 1 and the ELOPJ register handles control for GPT2 and 3. When the event specified in the ELSRn register occurs, the corresponding CSTn bit in the GTSTR register (timer start register) shown in Table 21.6 is cleared to 0 and the GPTa counter stops.
If an event occurs while the CSTn bit in the GTSTR register (timer start register) is 0, the event is ignored.

21.6.3 Usage Notes on GPT Operation by Event Signal Reception from ELC

The following notes on usage apply when the GPT is used in event link operation.

(1) Start Counting

If the event specified in the ELSRn register occurs during a cycle of writing to a CSTn bit in the GTSTR counter (timer start), writing to the CSTn bit in the GTSTR register takes priority.

(2) Stop Counting

If the event specified in the ELSRn register occurs during a cycle of writing to the GTCNT register (timer counter register), writing to the GTCNT register takes priority.

21.6.4 Noise Filtering

Each input pin for use in input capture and external trigger is equipped with a noise filter. The noise filter functionality includes enabling and disabling of the noise filter for each pin.
The sampling clock of the noise filter can be set for each channel and even clock signals with frequencies differing from that of the counter source setting (except in cases where the counter source itself is selected) can be set. Figure 21.77 shows the timing of noise filtering.

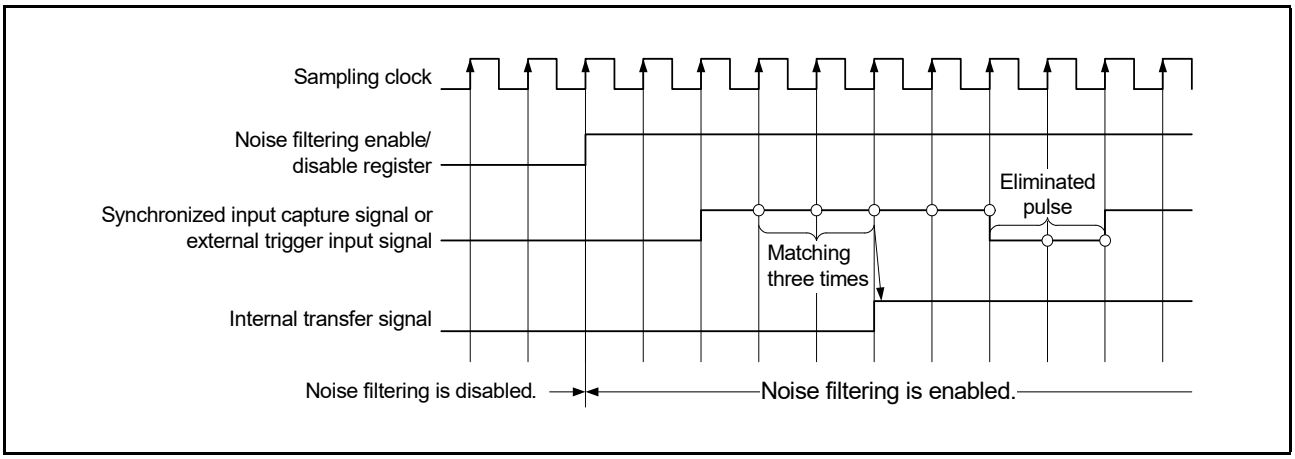


Figure 21.77 Timing of Noise Filtering

Table 21.8 lists the types of noise that can be removed when noise filtering is enabled. When the level of the synchronized input capture signal or external trigger input signal changes and then remains at the new level for at least three cycles of the sampling clock, the new level is conveyed by the filter. It is not conveyed if it only stays at the new level for two cycles of the sampling clock.

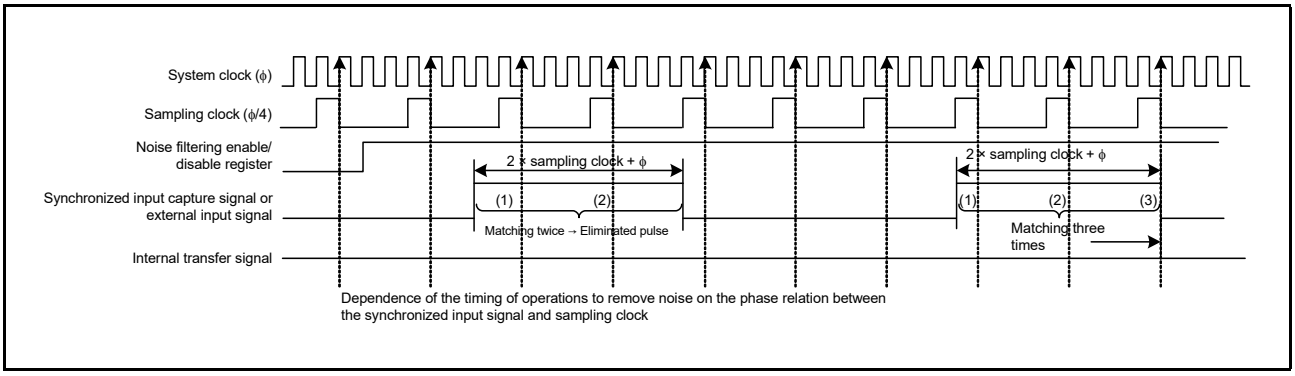


Figure 21.78 Dependence of the Timing of Operations to Remove Noise on the Phase Relation between the Synchronized Input Signal and Sampling Clock

Table 21.8 Relationship between Noise and Sampling Clock

Synchronized Input Capture Signal or External Trigger Input Signal	Number of Times Samples Match	Removed or Not Removed
At least as long as three cycles of the sampling clock	At least three times	Not removed
From two cycles of the sampling clock to three cycles of the sampling clock (but not exactly twice or three times the cycle)	Three times or twice (both are possible since this depends on the phase relation between the synchronized signal and the sampling clock)	The signal is not eliminated after matching three times The signal is eliminated after matching twice
Shorter than or lasting for only two cycles of the sampling clock	Twice, once, or not at all	Removed

21.7 Protection Function

21.7.1 Write-Protection for Registers

In order to prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WPn (n = 0 to 3).
The write-protection can be set for the following registers:

Table 21.9 List of Write-Protected Registers

Register Symbol	Register Name
GTIOR	General PWM timer I/O control register
GTINTAD	General PWM timer interrupt output register
GTCR	General PWM timer control register
GTBER	General PWM timer buffer enable register
GTUDC	General PWM timer count direction register
GTITC	General PWM timer interrupt and A/D converter start request skipping setting register
GTST	General PWM timer status register
GTCNT	General PWM timer counter
GTCCRA to GTCCRF	General PWM timer compare capture registers A to F
GTPR	General PWM timer period cycle setting register
GTPBR	General PWM timer cycle setting buffer register
GTPDBR	General PWM timer cycle setting double-buffer register
GTADTRA, GTADTRB	A/D converter start request timing registers A and B
GTADTBRA, GTADTBRB	A/D converter start request timing buffer registers A and B
GTADTDBRA, GTADTDBRB	A/D converter start request timing double-buffer registers A and B
GTONCR	General PWM timer output negate control register
GTDTCR	General PWM timer dead time control register
GTDVU, GTDVD	General PWM timer dead time value registers U and D
GTDBU, GTDBD	General PWM timer dead time buffer registers U and D
GTSOS	General PWM timer output protection function status register
GTSOTR	General PWM timer output protection function temporary release register

21.7.2 Disabling of Buffer Operation

If the timing of buffer register write is too late for the buffer transfer timing, buffer operation can be suspended with the GTBDR setting. Specifically, buffer transfer can be temporarily disabled, even though a buffer transfer condition is generated during buffer register write, by setting the corresponding GTBDR bit to 1 (buffer operation disabled) before buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all the buffer registers.

Figure 21.79 shows an example of operation for disabling buffer operation

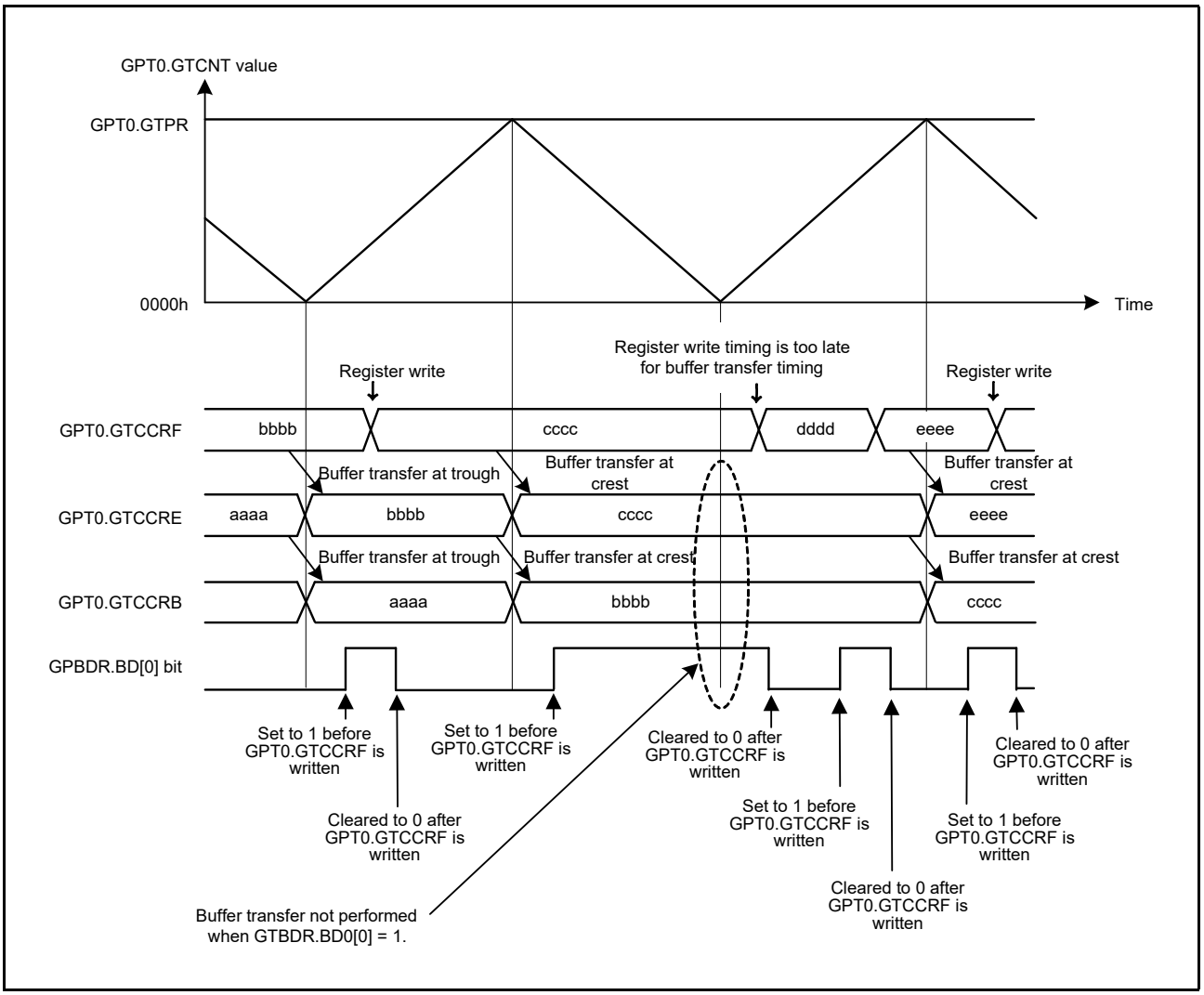


Figure 21.79 Example of Operation for Disabling Buffer Operation (Triangle Waves, Double Buffer Operation, Buffer Transfer at Both Troughs and Crests)

21.7.3 GTIOC Pin Output Negate Control

For protection from system failure, the negate control (deactivating the output level) is provided for GTIOC pin output with the GTONCR setting. There are three negate control sources: GTETRG pin input, and writing to GTONCR.SWN. Figure 21.80 shows an example of the GTIOC pin output negate control operation.

Note that once the negate control is performed, the negate control will not be released in the same cycle if the negate condition is no longer satisfied. The negate control is released in the next cycle.

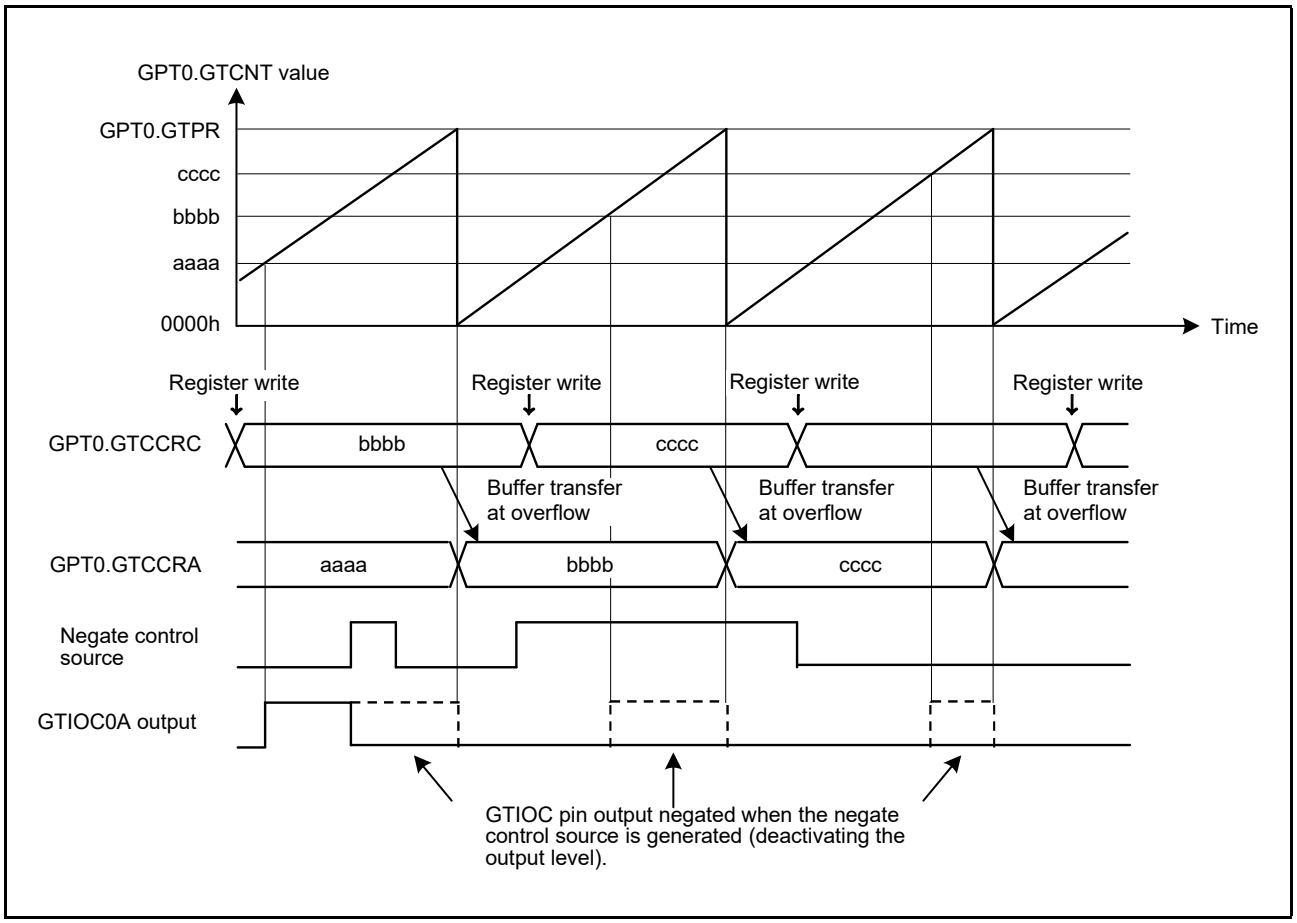


Figure 21.80 Example of GTIOC Pin Output Negate Control Operation (Saw-Wave Up-Counting, Buffer Operation, Active Level: 1, High Output at GTCCRA Compare Match, Low Output at Cycle End)

21.7.4 Output Protection Function for GTIOC Pin Output

In preparation for incorrect GTCCRA settings (settings outside the range of 0 < GTCCRA < GTPR), the output protection function for the GTIOC pin output (disabling function) is activated when the automatic dead time setting (GTDTCR.TDE = 1) is made in triangle-wave mode.

The status of the output protection function can be read from GTSOS.SOS[1:0].

Figure 21.81 shows the output protection function state transition.

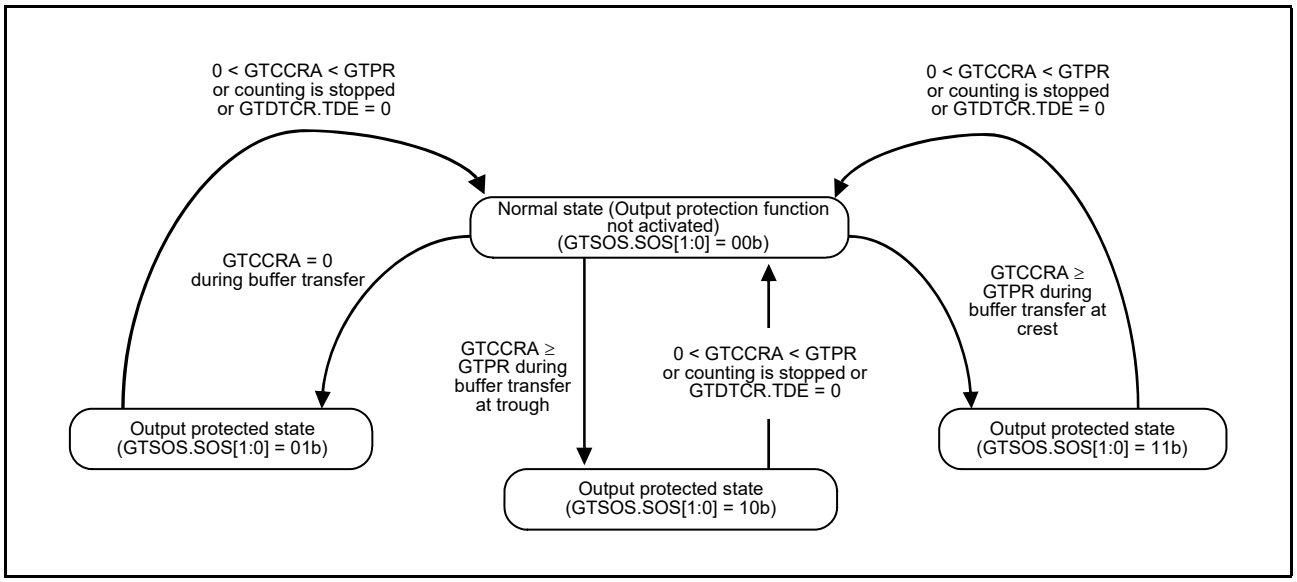
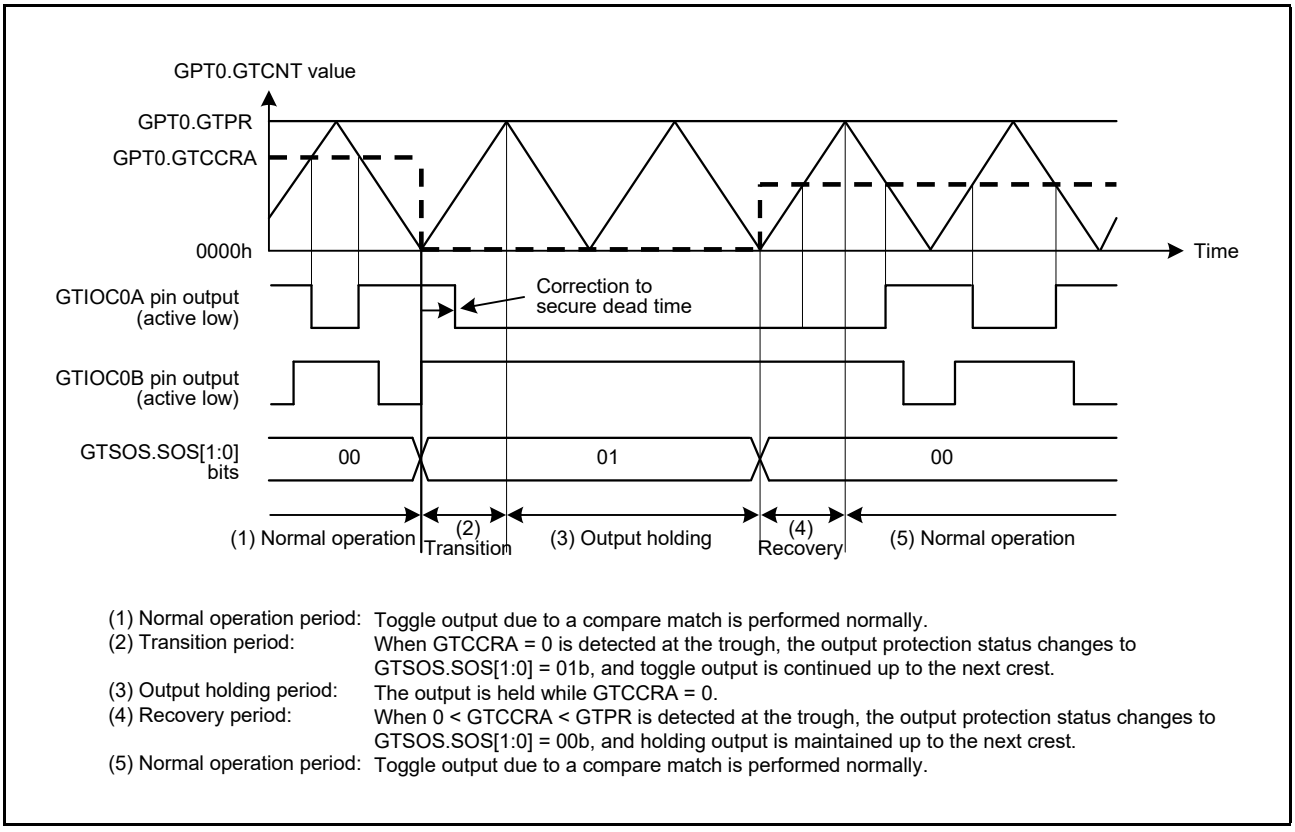


Figure 21.81 Output Protection Function

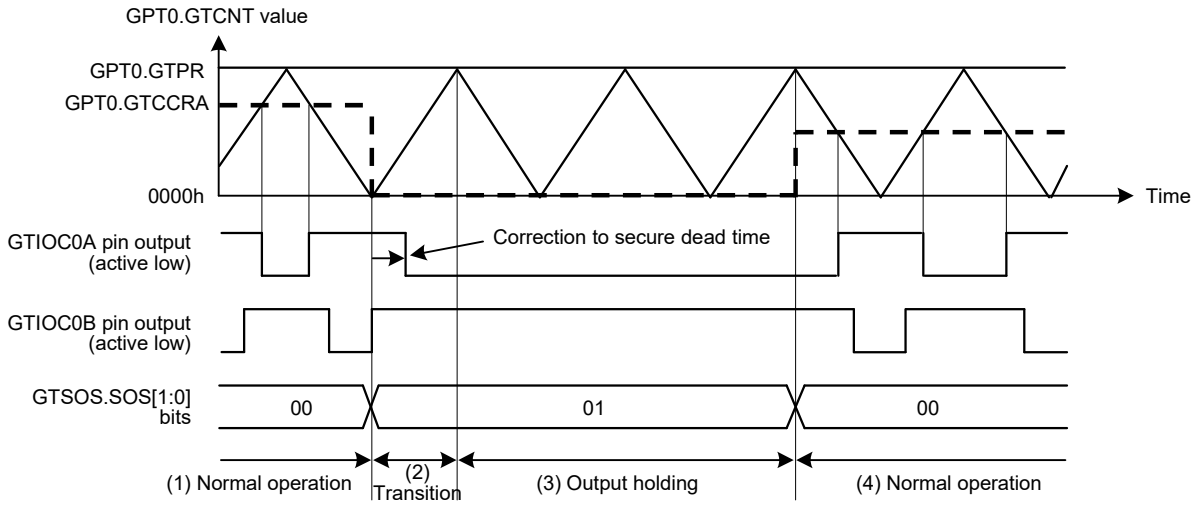
(1) Output Protection Function When GTCCRA is Set to 0 during Buffer Transfer

Figure 21.82 and Figure 21.83 show examples of output protection function operation when GTCCRA is set to 0 during buffer transfer at troughs, and Figure 21.84 and Figure 21.85 show examples when GTCCRA is set to 0 during buffer transfer at crests.



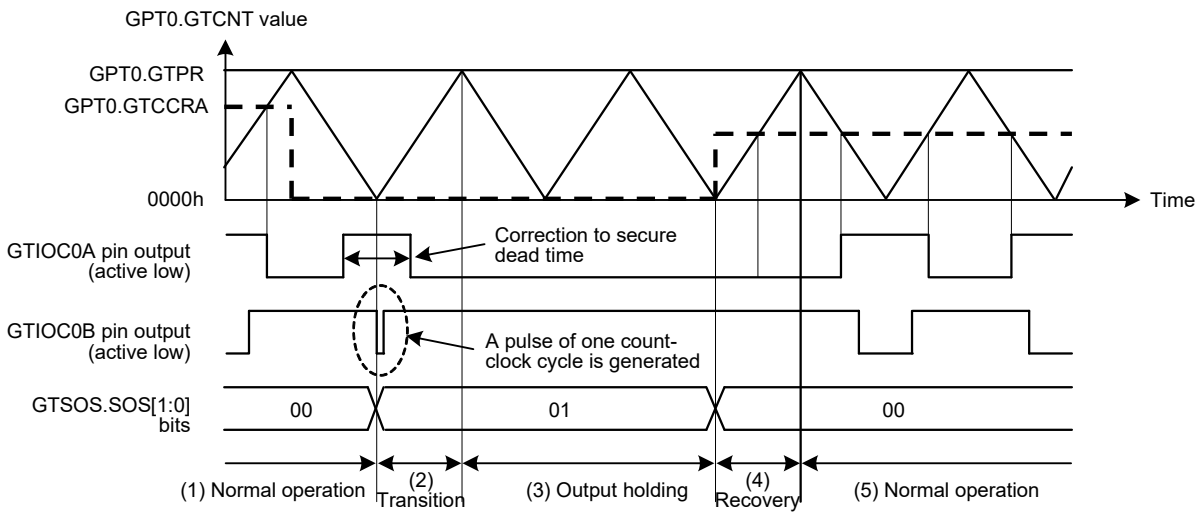
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Recovery period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 21.82 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Normal operation period: When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and toggle output due to a compare match is performed normally.

Figure 21.83 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA = 0 is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA = 0.
(4) Recovery period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 21.84 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

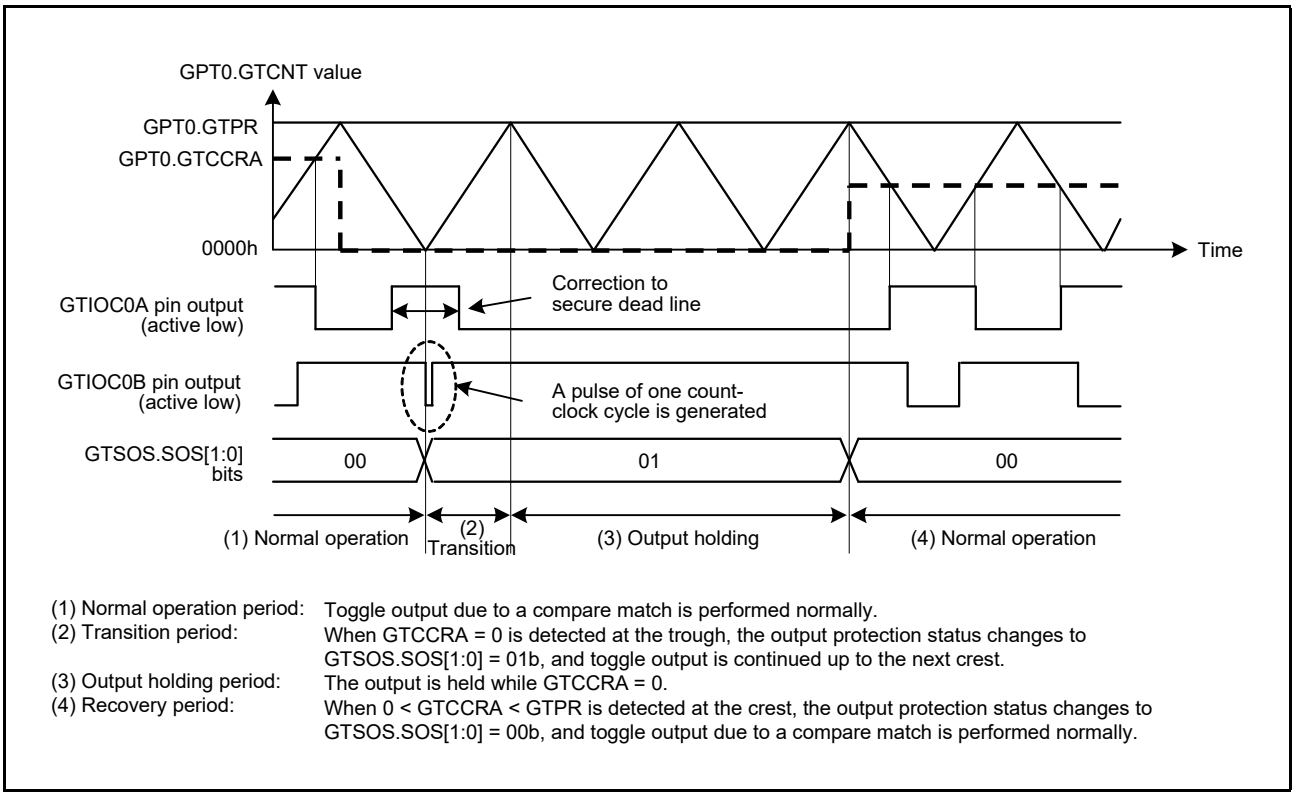


Figure 21.85 Example of Output Protection Function Operation When GTCCRA is Set to 0 during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

(2) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs

Figure 21.86 and Figure 21.87 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.

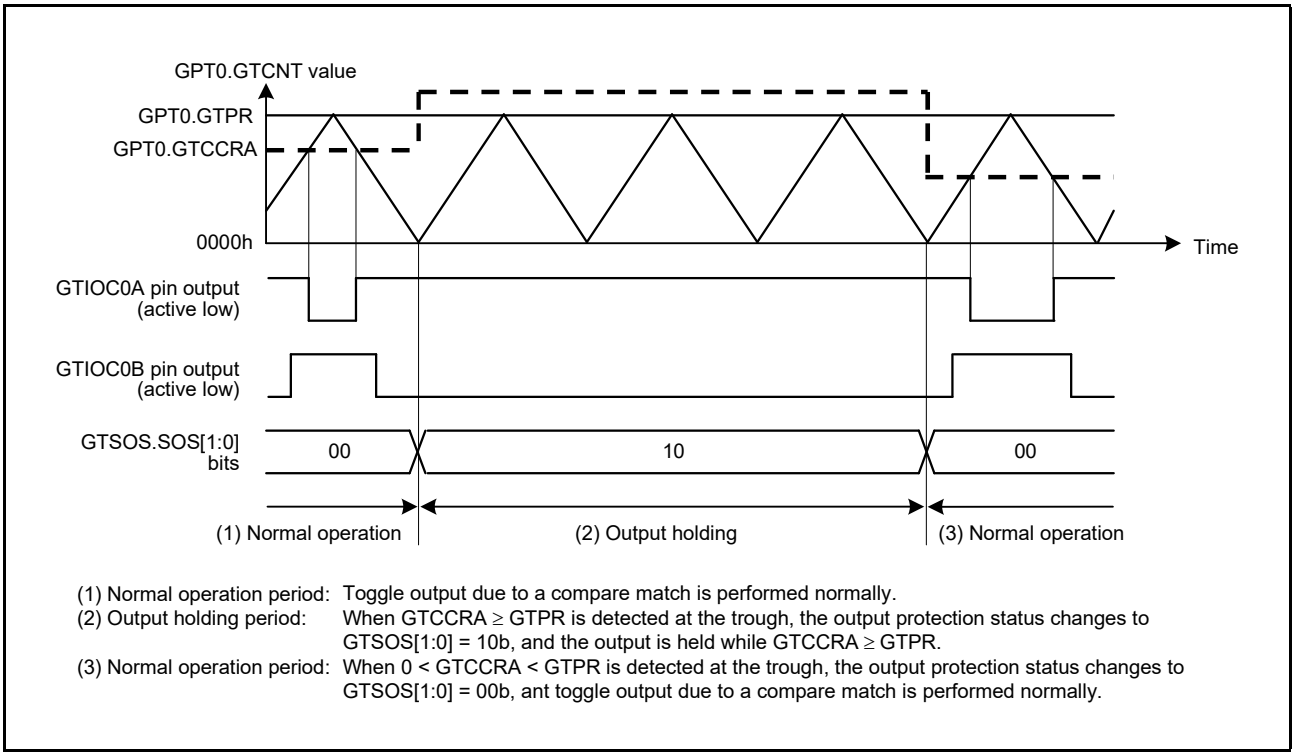
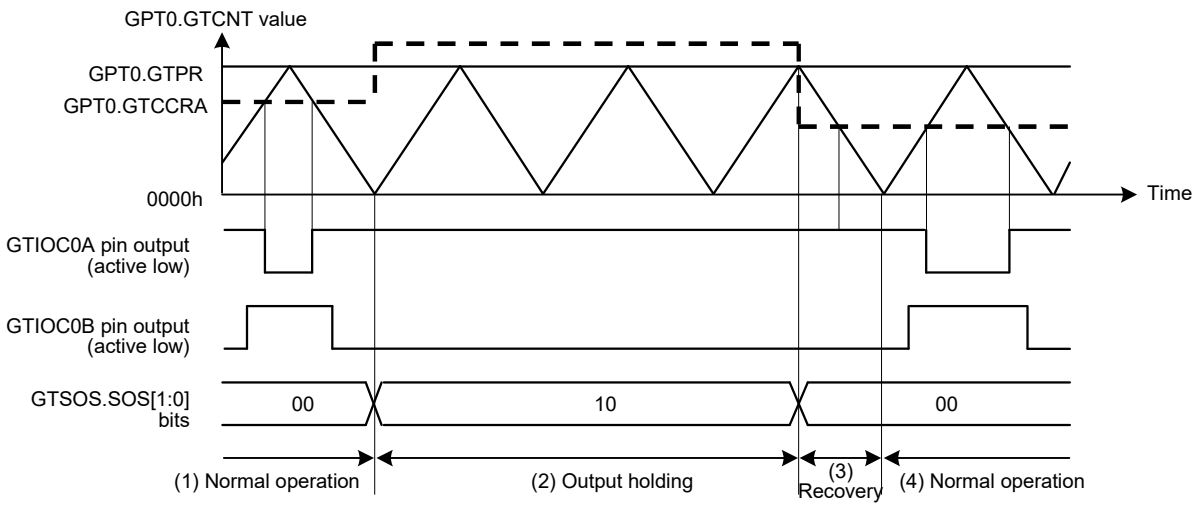


Figure 21.86 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

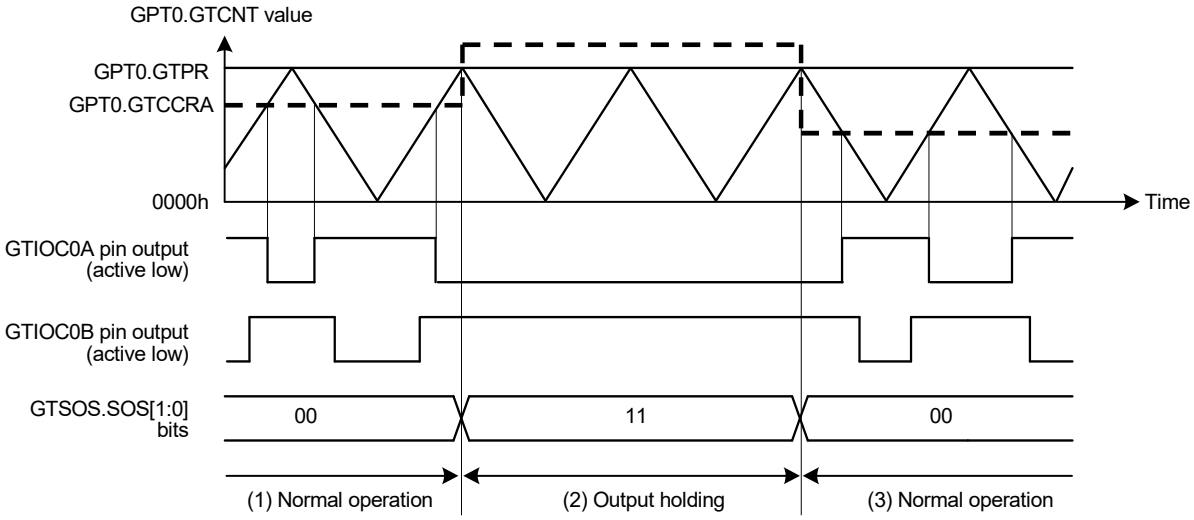


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected at the trough, the output protection status changes to GTSOS[1:0] = 10b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected at the crest, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 21.87 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Troughs (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)

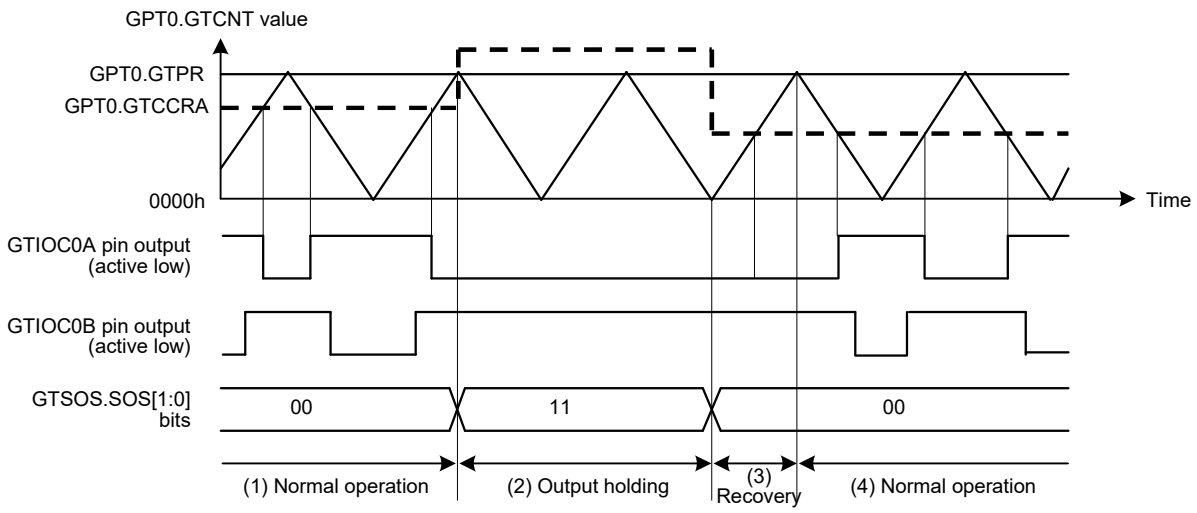
(3) Output Protection Function When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests

Figure 21.88 and Figure 21.89 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected at the crest, the output protection status changes to GTSOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 21.88 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Crests, Active Level: Low)



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR Is detected at the crest, the output protection status changes to GTSOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected at the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 21.89 Example of Output Protection Function Operation When GTCCRA ≥ GTPR is Set during Buffer Transfer at Crests (Restored to 0 < GTCCRA < GTPR during Buffer Transfer at Troughs, Active Level: Low)

(4) Restricted Specification of Output Protection Function

The GTCCRA value must be set within the range of (0 < GTCCRA < GTPR) at count start.
If an incorrect value is set in GTCCRA during count operation, (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs. However, the function does not operate correctly if counting starts with an incorrect value set in GTCCRA.
Even when the value set in the GTCCRA register may be greater than or equal to the GTPR register setting, set the values of the GTCCRA, GTDVU, GTDVD, and GTPR registers to satisfy the conditions below.

- During buffer transfer at crests, GTCCRA < GTPR + GTDVD – 1.
- If the condition GTCCRA = GTPR may apply during buffer transfer in troughs, GTDVU < GTPR – 1.

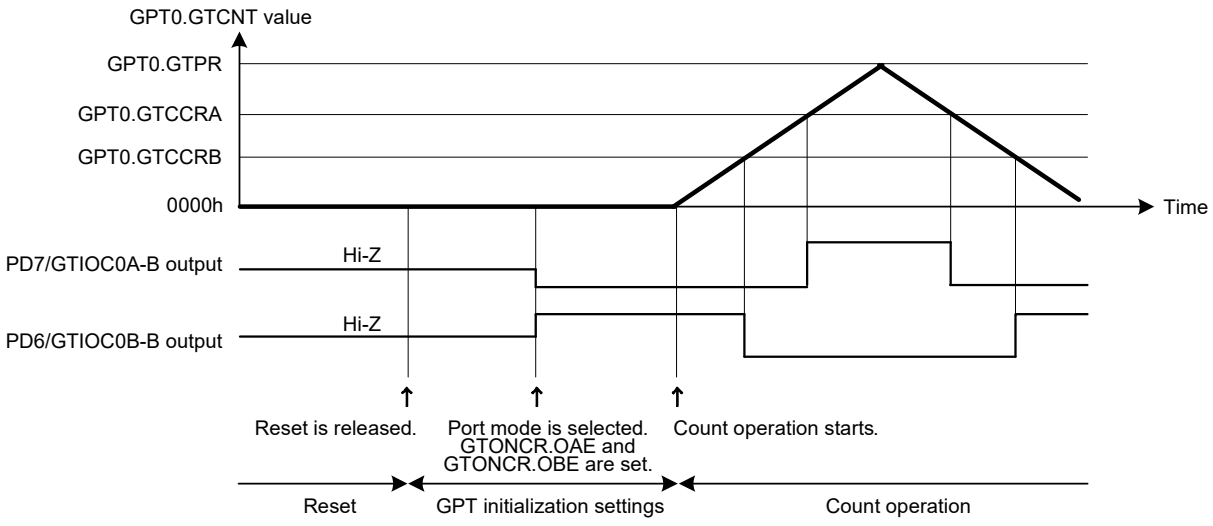
21.7.5 High-Impedance Control of GTIOC Pin Output by POE Function

For protection from system failure, the high-impedance state of the GTIOC pin output can be controlled by the port output enable (POE) function.
For details, see section 20, Port Output Enable 3 (POE3).

21.8 Initialization Method of Output Pins

21.8.1 Pin Settings after Reset

The GPT registers are initialized at a reset. Start counting after selecting the port mode (PMR and PmnPFS), setting GTIOR and the OAE and OBE bits in GTONCR and setting pins to function as GPT output.



[Setting examples]
GTIOR.GTIOA[5:0]: Initial output of low, output retained at cycle end, toggle output at compare match
GTIOR.GTIOB[5:0]: Initial output of high, output retained at cycle end, toggle output at compare match

Figure 21.90 Example of Pin Settings after Reset

21.8.2 Pin Initialization Due to Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization.

(1) Set OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop.
(2) Set OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values at OADFLT and OBDFLT in GTIOR, and output the arbitrary values at count stop.
(3) Similar to the MTU3, set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PMR registers of the I/O port in advance. Set the OAE and OBE bits in GTONCR to 0 and the control bit in PMR that corresponds to the pin to 0 to allow the arbitrary values to be output from the pin set as a general output port when an error occurs.
(4) Drive the output to a high impedance state using the POE function of the port output enable 3 (POE3).

When automatic dead time setting has been made, clear the GTDTCR.TDE bit to 0 once after counting is stopped.

When counting is stopped, only the values of registers that are changed by a GPT external source will change. If counting is resumed, operation will carry on from where it was stopped.
If counting was stopped, registers should be initialized before counting is started.

21.9 Usage Notes

21.9.1 Module Stop Function Setting

Operation of the GPT can be disabled or enabled by the module stop control register. The initial setting is for operation of the GPT to be halted. Register access is enabled by clearing module stop state. For details, see section 9, Low-Power Consumption Function.

21.9.2 Settings of GTCCRn during Compare Match Operation (n = A, B, C, D, E, F)

(1) When automatic dead time setting has been made in triangle-wave PWM mode

GTCCRA should be set within the range of GTDVU < GTCCRA, GTDVD < GTCCRA, and GTCCRA < GTPR.
When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated.
Be sure to set 0 < GTCCRA < GTPR at count start. Otherwise, the output protection function is not be activated correctly.
In addition, satisfy all the conditions below.

- During buffer transfer at crests, GTCCRA < GTPR + GTDVD – 1.
- If the condition GTCCRA = GTPR may apply during buffer transfer in troughs, GTDVU < GTPR – 1.

For details, refer to section 21.7.4, Output Protection Function for GTIOC Pin Output.

(2) When automatic dead time setting has not been made in triangle-wave PWM mode

GTCCRA should be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. In the case of GTCCRA > GTPR, no compare match occurs.
Similarly, GTCCRB should be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRA ≥ GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. In the case of GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting has been made in saw-wave one-shot pulse mode

GTCCRC and GTCCRD should be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

- In up-count operation: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-count operation: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVD

Similarly, GTCCRE and GTCCRF should be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

- In up-count operation: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR - GTDVD
- In down-count operation: GTCCRE > GTCCRF, GTCCRE < GTPR – GTDVU, GTCCRF > GTDVD

(4) When automatic dead time setting has not been made in saw-wave one-shot pulse mode

GTCCRC and GTCCRD should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-count operation: 0 < GTCCRC < GTCCRD < GTPR
- In down-count operation: GTPR > GTCCRC > GTCCRD > 0

Similarly, GTCCRE and GTCCRF should be set to satisfy the following restrictions. If the restrictions are not satisfied, two compare matches do not occur and pulse output cannot be performed.

- In up-count operation: 0 < GTCCRE < GTCCRF < GTPR
- In down-count operation: GTPR > GTCCRE > GTCCRF > 0

(5) In saw-wave PWM mode

GTCCRA should be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.
Similarly, GTCCRB should be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

21.9.3 Stopping the Timer in the Safe Way

When the timer stopping by the GTSTR writing and the GPT compare match interrupt conflict, an interrupt may be generated after the GTSTR writing.
Therefore, stop the timer in the following order. Then, a compare match interrupt is not generated after the timer has been stopped, and the timer can be stopped in the safe way.
(1) Disable the interrupt request by the interrupt request enable registers (IER15 to IER18) of the ICU.
(2) Disable the interrupt request by the interrupt output setting register (GTINTAD) of the GPT.
(3) Clear the CSTn bit in GTSTR to 0.

21.9.4 Priority Order of Events for the Counter

(1) While the counter is stopped, writing to the counter is given priority over clearing.
(2) If automatic setting of the CST bit and automatic resetting of the CST bit due to writing by the CPU are in contention, the priority order is as follows:
CPU writing > Automatic setting of the CST bit > Automatic resetting of the CST bit
- Automatic setting of the CST bit
  - Hardware start by the source set by the GTHSCR and GTHSSR registers
  - Start of counting by the ECL
- Automatic resetting of the CST bit
  - Hardware stop by the source set by the GTHSCR and GTHSSR registers
  - Stop of counting by the ECL

21.9.5 Notes on Port Settings in PWM Output Operating Mode

For the 6-phase PWM output using channels 0 to 2 (GTIOC0A, GTIOC0B, GTIOC1A, GTIOC1B, GTIOC2A, and GTIOC2B), set the port pins for use as the 6-phase PWM output pins in the groups in Table 21.10.
For the port settings, see section 18, Multi-Function Pin Controller (MPC).

Table 21.10 Output Pins for Channels 0 to 2

	Specified Port					
Port Group	**GTIOC0A**	**GTIOC0B**	**GTIOC1A**	**GTIOC1B**	**GTIOC2A**	**GTIOC2B**
1*1	P16	P15	P14	P13	P12	P11
2*2	PA2	PA1	PA0	P77	P76	P75
3*2	PB7	PF6	PF5	P87	P86	PD7

Note 1. This port group is only available in 320-pin devices.
Note 2. This port group is available in both 320- and 176-pin devices.

22. 16-Bit Timer Pulse Unit (TPUa)

This LSI has two on-chip 16-bit timer pulse units (TPU) (unit 0 and unit 1) comprising six-channel 16-bit timers, and a total of 12 channels (TPU0 to TPU11).

22.1 Overview

Specifications of the TPU are listed in Table 22.1. Functions of the TPU (unit 0) are listed in Table 22.2, and functions of the TPU (unit 1) are listed in Table 22.3.
A block diagram of TPU (unit 0) is shown in Figure 22.1, and a block diagram of TPU (unit 1) is shown in Figure 22.2.

Table 22.1 Specifications of TPU

Item	Description
Pulse input/output	Maximum 16 × 2 units
Count clock	Seven or eight types are provided for each channel.
Settable operations	• Waveform output at compare match • Input capture function (noise filters can be set) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match and input capture • Synchronous input/output for registers by counter synchronous operation • Maximum of 15-phase × 2 units of PWM output by combination with synchronous operation • Cascaded operation • Internal PWM feedback input select
Channels 0 and 3 (unit 0), and channels 6 and 9 (unit 1)	Buffer operation can be set.
Channels 1, 2, 4, and 5 (unit 0), and channels 7, 8, 10, and 11 (unit 1)	Phase counting mode can be set for individual channels
Interrupt source	26 sources × 2 units
Buffer operation	Automatic transfer of register data
Generation of trigger (unit 0)	Programmable pulse generator (PPG) output trigger can be generated.
Generation of trigger	Conversion start trigger for the A/D converter can be generated.
Event linking (output) (unit 0)	Six types of event signal can be output to the ELC. • Compare match A (TPU0 to TPU3) • Compare match B (TPU0 to TPU3) • Compare match C (TPU0, TPU3) • Compare match D (TPU0, TPU3) • Overflow (TPU0 to TPU3) • Underflow (TPU1, TPU2)
Event linking (input) (unit 0)	Any of the three operations in response to event reception is possible. • Starting counts (TPU0 to TPU3) • Clearing counts (TPU0 to TPU3) • Input capture operation (TPU0 to TPU3)
Low-power consumption function	Module-stop state can be set for each unit.

Note: One unit for 176-pin devices (only unit 0 is provided)

Table 22.2 TPU (Unit 0) Functions (1 / 2)

Item		TPU0	TPU1	TPU2	TPU3	TPU4	TPU5
Count clock*1		PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 TCLKA TCLKB TCLKC TCLKD	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 TCLKA TCLKB	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/1024 TCLKA TCLKB TCLKC	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024 PCLKD/4096 TCLKA	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/1024 TCLKA TCLKC	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 TCLKA TCLKC TCLKD
Timer general registers		TGRA TGRB TGRC*2 TGRD*2	TGRA TGRB	TGRA TGRB	TGRA TGRB TGRC*2 TGRD*2	TGRA TGRB	TGRA TGRB
I/O pins		TIOCA0 TIOCB0 TIOCC0 TIOCD0	TIOCA1 TIOCB1	TIOCA2 TIOCB2	TIOCA3 TIOCB3 TIOCC3 TIOCD3	TIOCA4 TIOCB4	TIOCA5 TIOCB5
Counter clear function		TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture
Compare match output	Low output	Possible	Possible	Possible	Possible	Possible	Possible
	High output	Possible	Possible	Possible	Possible	Possible	Possible
	Toggle output	Possible	Possible	Possible	Possible	Possible	Possible
Input capture function		Possible	Possible	Possible	Possible	Possible	Possible
Synchronous operation		Possible	Possible	Possible	Possible	Possible	Possible
PWM mode		Possible	Possible	Possible	Possible	Possible	Possible
Phase counting mode		Not possible	Possible	Possible	Not possible	Possible	Possible
Buffer operation		Possible	Not possible	Not possible	Possible	Not possible	Not possible
DMAC activation		TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture
A/D conversion start trigger		TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	Not possible
PPG trigger		TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	TGRA/TGRB compare match or input capture	Not possible	Not possible
Interrupt sources		5 sources • Compare match or input capture 0A • Compare match or input capture 0B • Compare match or input capture 0C • Compare match or input capture 0D • Overflow	4 sources • Compare match or input capture 1A • Compare match or input capture 1B • Overflow • Underflow	4 sources • Compare match or input capture 2A • Compare match or input capture 2B • Overflow • Underflow	5 sources • Compare match or input capture 3A • Compare match or input capture 3B • Compare match or input capture 3C • Compare match or input capture 3D • Overflow	4 sources • Compare match or input capture 4A • Compare match or input capture 4B • Overflow • Underflow	4 sources • Compare match or input capture 5A • Compare match or input capture 5B • Overflow • Underflow
Event linking (output)		5 sources • Compare match 0A • Compare match 0B • Compare match 0C • Compare match 0D • Overflow	4 sources • Compare match 1A • Compare match 1B • Overflow • Underflow	4 sources • Compare match 2A • Compare match 2B • Overflow • Underflow	5 sources • Compare match 3A • Compare match 3B • Compare match 3C • Compare match 3D • Overflow	Not possible	Not possible

Table 22.2 TPU (Unit 0) Functions (2 / 2)

Item	TPU0	TPU1	TPU2	TPU3	TPU4	TPU5
Event linking (input)	• Starting counts • Clearing counts • Input capture operation (data is captured in TGRA)	• Starting counts • Clearing counts • Input capture operation (data is captured in TGRA)	• Starting counts • Clearing counts • Input capture operation (data is captured in TGRA)	• Starting counts • Clearing counts • Input capture operation (data is captured in TGRA)	Not possible	Not possible
Module-stop setting*3	MSTPCRA.MSTPCRA8 bit					

Note 1. The external count clocks not listed in this table are available in phase counting mode. For details, see section 22.3.6, Phase Counting Mode.
Note 2. TGRC and TGRD can be set as a buffer register.
Note 3. For details, see section 9, Low-Power Consumption Function.

Table 22.3 TPU (Unit 1) Functions (1 / 2)

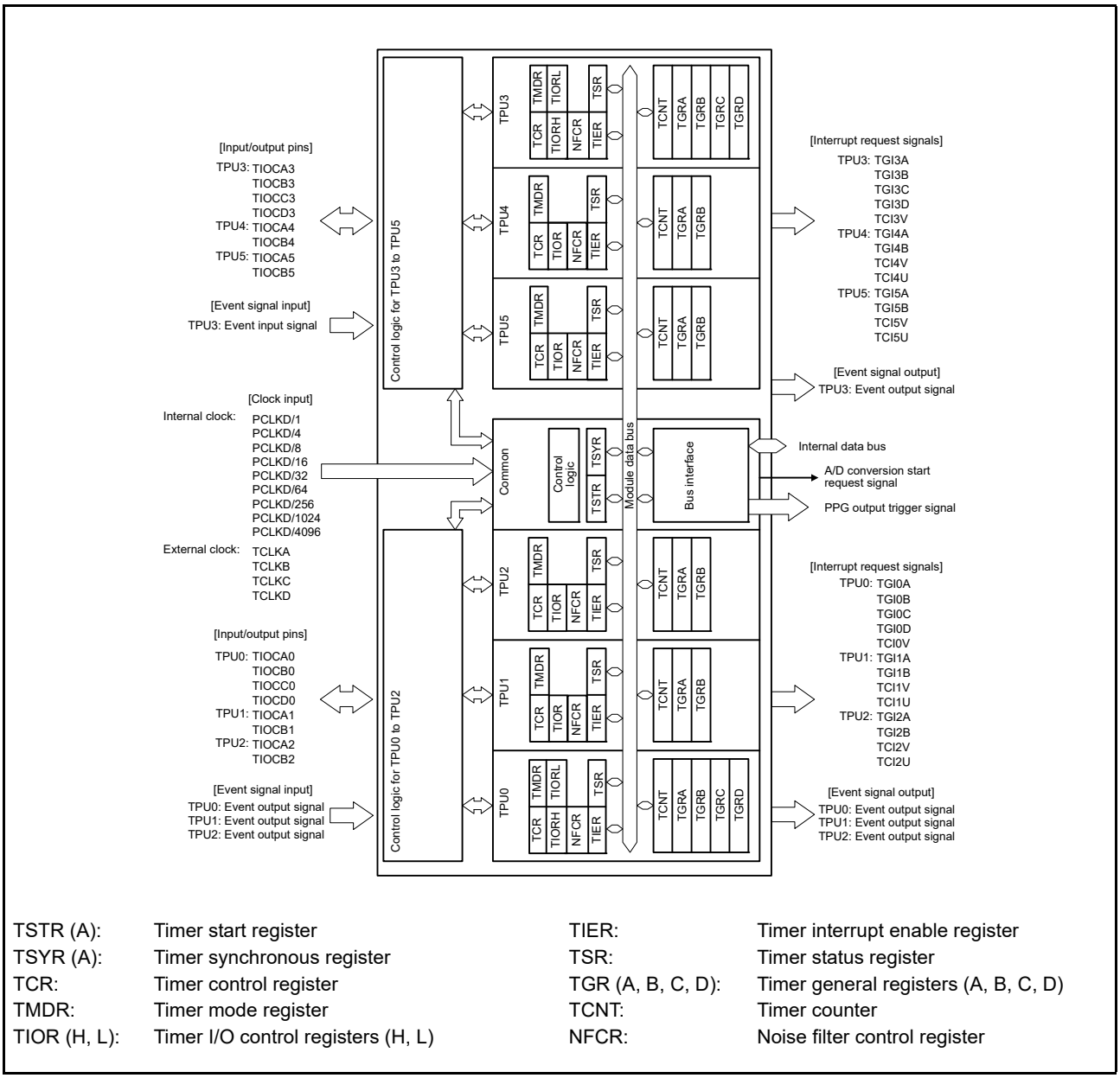
Item		TPU6	TPU7	TPU8	TPU9	TPU10	TPU11
Count clock*1		PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 TCLKE TCLKF TCLKG TCLKH	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 TCLKE TCLKF	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/1024 TCLKE TCLKF TCLKG	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024 PCLKD/4096 TCLKE	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/1024 TCLKE TCLKG	PCLKD/1 PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 TCLKE TCLKG TCLKH
Timer general registers		TGRA TGRB TGRC*2 TGRD*2	TGRA TGRB	TGRA TGRB	TGRA TGRB TGRC*2 TGRD*2	TGRA TGRB	TGRA TGRB
I/O pins		TIOCA6 TIOCB6 TIOCC6 TIOCD6	TIOCA7 TIOCB7	TIOCA8 TIOCB8	TIOCA9 TIOCB9 TIOCC9 TIOCD9	TIOCA10 TIOCB10	TIOCA11 TIOCB11
Counter clear function		TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture	TGRy compare match or input capture
Compare match output	Low output	Possible	Possible	Possible	Possible	Possible	Possible
	High output	Possible	Possible	Possible	Possible	Possible	Possible
	Toggle output	Possible	Possible	Possible	Possible	Possible	Possible
Input capture function		Possible	Possible	Possible	Possible	Possible	Possible
Synchronous operation		Possible	Possible	Possible	Possible	Possible	Possible
PWM mode		Possible	Possible	Possible	Possible	Possible	Possible
Phase counting mode		Not possible	Possible	Possible	Not possible	Possible	Possible
Buffer operation		Possible	Not possible	Not possible	Possible	Not possible	Not possible
DMAC activation		Not possible	Not possible	Not possible	Not possible	Not possible	Not possible
A/D conversion start trigger		TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	TGRA compare match or input capture	Not possible
PPG trigger		Not possible	Not possible	Not possible	Not possible	Not possible	Not possible

Table 22.3 TPU (Unit 1) Functions (2 / 2)

Item	TPU6	TPU7	TPU8	TPU9	TPU10	TPU11
Interrupt sources	5 sources • Compare match or input capture 6A • Compare match or input capture 6B • Compare match or input capture 6C • Compare match or input capture 6D • Overflow	4 sources • Compare match or input capture 7A • Compare match or input capture 7B • Overflow • Underflow	4 sources • Compare match or input capture 8A • Compare match or input capture 8B • Overflow • Underflow	5 sources • Compare match or input capture 9A • Compare match or input capture 9B • Compare match or input capture 9C • Compare match or input capture 9D • Overflow	4 sources • Compare match or input capture 10A • Compare match or input capture 10B • Overflow • Underflow	4 sources • Compare match or input capture 11A • Compare match or input capture 11B • Overflow • Underflow
Event linking (output)	Not possible	Not possible	Not possible	Not possible	Not possible	Not possible
Event linking (input)	Not possible	Not possible	Not possible	Not possible	Not possible	Not possible
Module-stop setting	MSTPCRA.MSTPCRA7 bit					

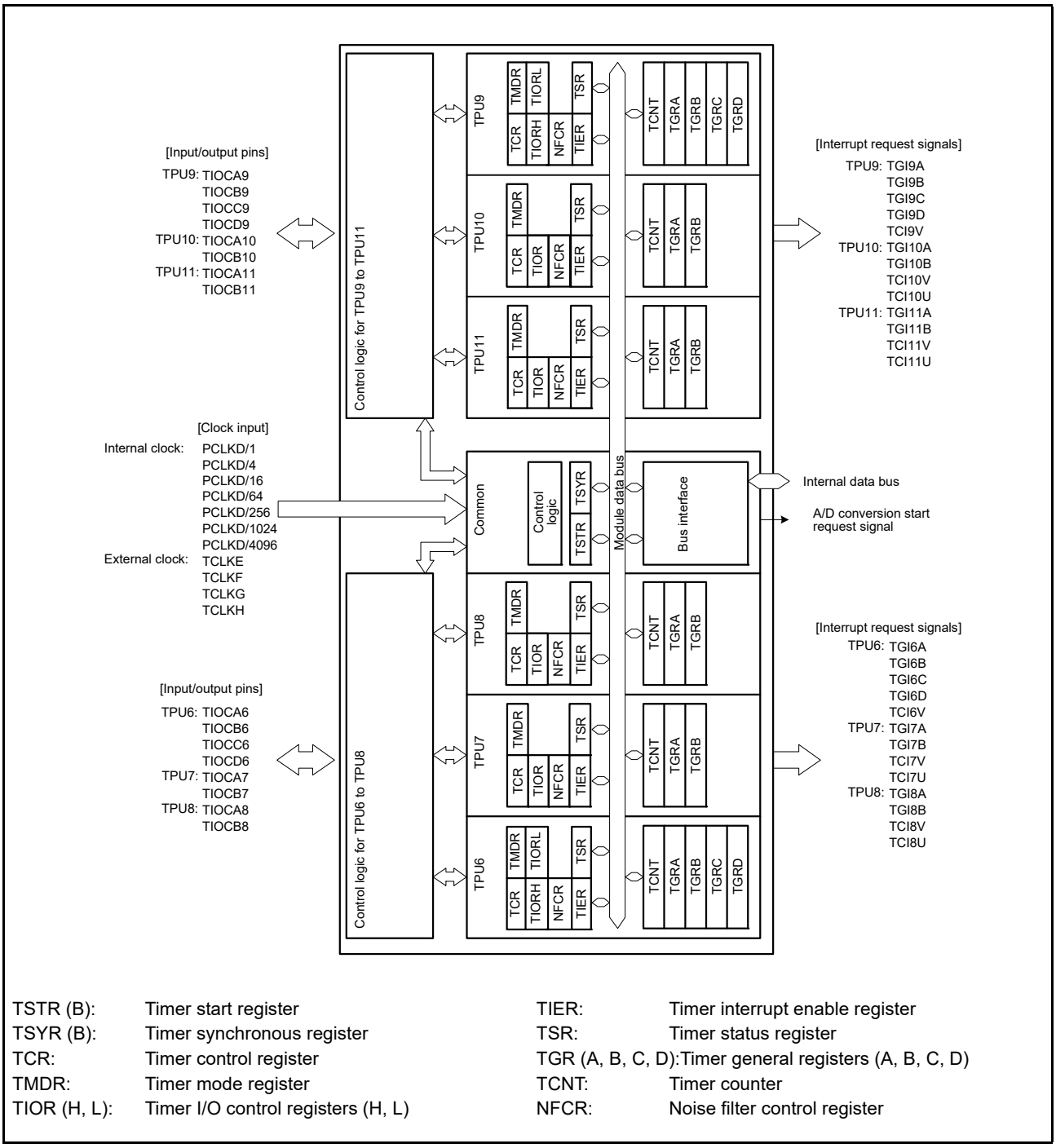
Note 1. The external count clocks not listed in this table are available in phase counting mode. For details, see section 22.3.6, Phase Counting Mode.

Note 2. The TGRC and TGRD registers can be set as a buffer register.



TSTR (A):	Timer start register	TIER:	Timer interrupt enable register
TSYR (A):	Timer synchronous register	TSR:	Timer status register
TCR:	Timer control register	TGR (A, B, C, D):	Timer general registers (A, B, C, D)
TMDR:	Timer mode register	TCNT:	Timer counter
TIOR (H, L):	Timer I/O control registers (H, L)	NFCR:	Noise filter control register

Figure 22.1 Block Diagram of TPU (Unit 0)



TSTR (B):	Timer start register	TIER:	Timer interrupt enable register
TSYR (B):	Timer synchronous register	TSR:	Timer status register
TCR:	Timer control register	TGR (A, B, C, D):	Timer general registers (A, B, C, D)
TMDR:	Timer mode register	TCNT:	Timer counter
TIOR (H, L):	Timer I/O control registers (H, L)	NFCR:	Noise filter control register

Figure 22.2 Block Diagram of TPU (Unit 1)

Table 22.4 lists the input/output pins of the TPU.

Table 22.4 Pin Configuration of TPU

Unit	Channel	Pin Name	I/O	Description
Unit 0	Common	TCLKA	Input	External clock A input pin (TPU1 and TPU5 phase counting mode A phase input)
		TCLKB	Input	External clock B input pin (TPU1 and TPU5 phase counting mode B phase input)
		TCLKC	Input	External clock C input pin (TPU2 and TPU4 phase counting mode A phase input)
		TCLKD	Input	External clock D input pin (TPU2 and TPU4 phase counting mode B phase input)
	TPU0	TIOCA0	I/O	TPU0.TGRA input capture input/output compare output/PWM output pin
		TIOCB0	I/O	TPU0.TGRB input capture input/output compare output/PWM output pin
		TIOCC0	I/O	TPU0.TGRC input capture input/output compare output/PWM output pin
		TIOCD0	I/O	TPU0.TGRD input capture input/output compare output/PWM output pin
	TPU1	TIOCA1	I/O	TPU1.TGRA input capture input/output compare output/PWM output pin
		TIOCB1	I/O	TPU1.TGRB input capture input/output compare output/PWM output pin
	TPU2	TIOCA2	I/O	TPU2.TGRA input capture input/output compare output/PWM output pin
		TIOCB2	I/O	TPU2.TGRB input capture input/output compare output/PWM output pin
	TPU3	TIOCA3	I/O	TPU3.TGRA input capture input/output compare output/PWM output pin
		TIOCB3	I/O	TPU3.TGRB input capture input/output compare output/PWM output pin
		TIOCC3	I/O	TPU3.TGRC input capture input/output compare output/PWM output pin
		TIOCD3	I/O	TPU3.TGRD input capture input/output compare output/PWM output pin
	TPU4	TIOCA4	I/O	TPU4.TGRA input capture input/output compare output/PWM output pin
		TIOCB4	I/O	TPU4.TGRB input capture input/output compare output/PWM output pin
	TPU5	TIOCA5	I/O	TPU5.TGRA input capture input/output compare output/PWM output pin
		TIOCB5	I/O	TPU5.TGRB input capture input/output compare output/PWM output pin
Unit 1	Common	TCLKE	Input	External clock A input pin (TPU7 and TPU11 phase counting mode A phase input)
		TCLKF	Input	External clock B input pin (TPU7 and TPU11 phase counting mode B phase input)
		TCLKG	Input	External clock C input pin (TPU8 and TPU10 phase counting mode A phase input)
		TCLKH	Input	External clock D input pin (TPU8 and TPU10 phase counting mode B phase input)
	TPU6	TIOCA6	I/O	TPU6.TGRA input capture input/output compare output/PWM output pin
		TIOCB6	I/O	TPU6.TGRB input capture input/output compare output/PWM output pin
		TIOCC6	I/O	TPU6.TGRC input capture input/output compare output/PWM output pin
		TIOCD6	I/O	TPU6.TGRD input capture input/output compare output/PWM output pin
	TPU7	TIOCA7	I/O	TPU7.TGRA input capture input/output compare output/PWM output pin
		TIOCB7	I/O	TPU7.TGRB input capture input/output compare output/PWM output pin
	TPU8	TIOCA8	I/O	TPU8.TGRA input capture input/output compare output/PWM output pin
		TIOCB8	I/O	TPU8.TGRB input capture input/output compare output/PWM output pin
	TPU9	TIOCA9	I/O	TPU9.TGRA input capture input/output compare output/PWM output pin
		TIOCB9	I/O	TPU9.TGRB input capture input/output compare output/PWM output pin
		TIOCC9	I/O	TPU9.TGRC input capture input/output compare output/PWM output pin
		TIOCD9	I/O	TPU9.TGRD input capture input/output compare output/PWM output pin
	TPU10	TIOCA10	I/O	TPU10.TGRA input capture input/output compare output/PWM output pin
		TIOCB10	I/O	TPU10.TGRB input capture input/output compare output/PWM output pin
	TPU11	TIOCA11	I/O	TPU11.TGRA input capture input/output compare output/PWM output pin
		TIOCB11	I/O	TPU11.TGRB input capture input/output compare output/PWM output pin

22.2 Register Descriptions

22.2.1 Timer Control Register (TCR)

TPU has 12 TCR registers in total (one register per channel).
TCR controls the TCNT counter for each channel. TCR settings should be made while TCNT counter operation is stopped.

Address(es): TPU0.TCR A008 0110h, TPU1.TCR A008 0120h, TPU2.TCR A008 0130h, TPU3.TCR A008 0140h, TPU4.TCR A008 0150h, TPU5.TCR A008 0160h, TPU6.TCR A008 0190h, TPU7.TCR A008 01A0h, TPU8.TCR A008 01B0h, TPU9.TCR A008 01C0h, TPU10.TCR A008 01D0h, TPU11.TCR A008 01E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	TPSC[2:0]	Timer Prescaler Select	See Table 22.5 to Table 22.10.	R/W
b4, b3	CKEG[1:0]	Input Clock Edge Select	See Table 22.11.	R/W
b7 to b5	CCLR[2:0]*1	Counter Clear Source Select	See Table 22.12 and Table 22.13.	R/W

Note 1. Bit 7 in TPU1.TCR, TPU2.TCR, TPU4.TCR, and TPU5.TCR (unit 0) and in TPU7.TCR, TPU8.TCR, TPU10.TCR, and TPU11.TCR (unit 1) is reserved. These bits are read as 0. The write value should be 0.

TPSC[2:0] Bits (Timer Prescaler Select)

These bits select the TCNT counter clock. The clock source can be selected independently for each channel.
To select the external clock as the clock source, set the bit in the port direction register (PDR) for the corresponding pin to 0 (input port), and set the bit in the port mode register (PMR) to 1 (uses the pin as an I/O port for peripheral functions). For details, see section 17, I/O Ports.

CKEG[1:0] Bits (Input Clock Edge Select)

These bits select the input clock edge.
When the internal clock is counted using both edges, the input clock period is halved (e.g. Both edges of PCLKD/4 = PCLKD/2 rising edge).
Internal clock edge selection is valid when the input clock is PCLKD/4 or slower. This setting is ignored if the input clock is PCLKD/1, or when overflow/underflow of another channel is selected.

CCLR[2:0] Bits (Counter Clear Source Select)

These bits select the clear source of the TCNT counter.

Table 22.5 Bits TPSC[2:0] (TPU0, TPU6)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU0 (unit 0) TPU6 (unit 1)	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU0: Counts on TCLKA pin input • TPU6: Counts on TCLKE pin input
	1	0	1	External clock • TPU0: Counts on TCLKB pin input • TPU6: Counts on TCLKF pin input
	1	1	0	External clock • TPU0: Counts on TCLKC pin input • TPU6: Counts on TCLKG pin input
	1	1	1	External clock • TPU0: Counts on TCLKD pin input • TPU6: Counts on TCLKH pin input

Table 22.6 Bits TPSC[2:0] (TPU1, TPU7)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU1 (unit 0) TPU7 (unit 1)	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU1: Counts on TCLKA pin input • TPU7: Counts on TCLKE pin input
	1	0	1	External clock • TPU1: Counts on TCLKB pin input • TPU7: Counts on TCLKF pin input
	1	1	0	Internal clock: Counts on PCLKD/256
	1	1	1	• TPU1: Counts on TPU2.TCNT counter overflow/underflow • TPU7: Counts on TPU8.TCNT counter overflow/underflow

Note: This setting is invalid when TPU1 or TPU7 is in phase counting mode.

Table 22.7 Bits TPSC[2:0] (TPU2, TPU8)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU2 TPU8	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU2: Counts on TCLKA pin input • TPU8: Counts on TCLKE pin input
	1	0	1	External clock • TPU2: Counts on TCLKB pin input • TPU8: Counts on TCLKF pin input
	1	1	0	External clock • TPU2: Counts on TCLKC pin input • TPU8: Counts on TCLKG pin input
	1	1	1	Internal clock: Counts on PCLKD/1024

Note: This setting is invalid when TPU2 or TPU8 is in phase counting mode.

Table 22.8 Bits TPSC[2:0] (TPU3, TPU9)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU3 TPU9	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU3: Counts on TCLKA pin input • TPU9: Counts on TCLKE pin input
	1	0	1	Internal clock: Counts on PCLKD/1024
	1	1	0	Internal clock: Counts on PCLKD/256
	1	1	1	Internal clock: Counts on PCLKD/4096

Table 22.9 Bits TPSC[2:0] (TPU4, TPU10)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU4 TPU10	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU4: Counts on TCLKA pin input • TPU10: Counts on TCLKE pin input
	1	0	1	External clock • TPU4: Counts on TCLKC pin input • TPU10: Counts on TCLKG pin input
	1	1	0	Internal clock: Counts on PCLKD/1024
	1	1	1	• TPU4: Counts on TPU5.TCNT counter overflow/underflow • TPU10: Counts on TPU11.TCNT counter overflow/underflow

Note: This setting is invalid when TPU4 or TPU10 is in phase counting mode.

Table 22.10 Bits TPSC[2:0] (TPU5, TPU11)

Channel	Bits TPSC[2:0] b2	b1	b0	Description
TPU5 TPU11	0	0	0	Internal clock: Counts on PCLKD/1
	0	0	1	Internal clock: Counts on PCLKD/4
	0	1	0	Internal clock: Counts on PCLKD/16
	0	1	1	Internal clock: Counts on PCLKD/64
	1	0	0	External clock • TPU5: Counts on TCLKA pin input • TPU11: Counts on TCLKE pin input
	1	0	1	External clock • TPU5: Counts on TCLKC pin input • TPU11: Counts on TCLKG pin input
	1	1	0	Internal clock: Counts on PCLKD/256
	1	1	1	External clock • TPU5: Counts on TCLKD pin input • TPU11: Counts on TCLKH pin input

Note: This setting is invalid when TPU5 or TPU11 is in phase counting mode.

Table 22.11 Bits CKEG[1:0]

Bits CKEG[1:0]		Input Clock	
b4	**b3**	**Internal Clock**	**External clock**
0	0	Counted at falling edge	Counted at rising edge
0	1	Counted at rising edge	Counted at falling edge
1	0	Counted at both edges	Counted at both edges
1	1	Counted at both edges	Counted at both edges

Table 22.12 Bits CCLR[2:0] (TPU0, TPU3, TPU6, TPU9)

	Bits CCLR[2:0]			
Channel	**b7**	**b6**	**b5**	**Description**
(Unit 0) TPU0, TPU3 (Unit 1) TPU6, TPU9	0	0	0	TCNT counter clearing disabled
	0	0	1	TCNT counter cleared by TGRA compare match/input capture
	0	1	0	TCNT counter cleared by TGRB compare match/input capture
	0	1	1	TCNT counter cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*2
	1	0	0	TCNT counter clearing disabled
	1	0	1	TCNT counter cleared by TGRC compare match/input capture*1
	1	1	0	TCNT counter cleared by TGRD compare match/input capture*1
	1	1	1	TCNT counter cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*2

Note 1. When TGRC or TGRD is used as a buffer register, TCNT counter is not cleared because the buffer register setting has priority, and compare match/input capture does not occur.
Note 2. Synchronous operation is selected by setting the TSYRA.SYNCj bit (j = 0, 3) in unit 0 or the TSYRB.SYNCj bit (j = 0, 3) in unit 1 to 1.

Table 22.13 Bits CCLR[2:0] (TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, TPU11)

	Bits CCLR[2:0]*1			
Channel	**b7**	**b6**	**b5**	**Description**
(Unit 0) TPU1, TPU2, TPU4, TPU5 (Unit 1) TPU7, TPU8, TPU10, TPU11	0	0	0	TCNT counter clearing disabled
	0	0	1	TCNT counter cleared by TGRA compare match/input capture
	0	1	0	TCNT counter cleared by TGRB compare match/input capture
	0	1	1	TCNT counter cleared by counter clearing for another channel performing synchronous clearing/synchronous operation*2
	1	0	0	Setting prohibited
	1	0	1	Setting prohibited
	1	1	0	Setting prohibited
	1	1	1	Setting prohibited

Note 1. Bit 7 in TPU1.TCR, TPU2.TCR, TPU4.TCR, and TPU5.TCR (unit 0) and in TPU7.TCR, TPU8TCR, TPU10.TCR, TPU11.TCR (unit 1) is reserved. These bits are read as 0. The write value should be 0.
Note 2. Synchronous operation is selected by setting the TSYRA.SYNCj bit (j = 1, 2, 4, 5) in unit 0 or the TSYRB.SYNCj bit (j = 1, 2, 4, 5) in unit 1 to 1.

22.2.2 Timer Mode Register (TMDR)

TMDR sets the operating mode of each channel.
TPU has 12 TMDR registers in total (one register per channel). TMDR settings should be made while TCNT counter operation is stopped.

Address(es): TPU0.TMDR A008 0111h, TPU1.TMDR A008 0121h, TPU2.TMDR A008 0131h, TPU3.TMDR A008 0141h, TPU4.TMDR A008 0151h, TPU5.TMDR A008 0161h, TPU6.TMDR A008 0191h, TPU7.TMDR A008 01A1h, TPU8.TMDR A008 01B1h, TPU9.TMDR A008 01C1h, TPU10.TMDR A008 01D1h, TPU11.TMDR A008 01E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICSELD	ICSELB	BFB	BFA	MD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	MD[3:0]	Mode Select	b3*1 b0 0 0 0 0: Normal operation 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1*2 0 1 0 1: Phase counting mode 2*2 0 1 1 0: Phase counting mode 3*2 0 1 1 1: Phase counting mode 4*2 Settings other than above are prohibited.	R/W
b4	BFA*3	Buffer Operation A	0: TPUm.TGRA operates normally 1: TPUm.TGRA and TPUm.TGRC used together for buffer operation (m = 0, 3, 6, 9)	R/W
b5	BFB*4	Buffer Operation B	0: TGRB operates normally 1: TGRB and TGRD used together for buffer operation (m = 0, 3, 6, 9)	R/W
b6	ICSELB	TGRB Input Capture Input Select	0: Input capture input source is TIOCBn pin 1: Input capture input source is TIOCAn pin (n = 0 to 11)	R/W
b7	ICSELD*4	TGRD Input Capture Input Select	0: Input capture input source is TIOCDn pin 1: Input capture input source is TIOCCn pin (n = 0, 3, 6, 9)	R/W

Note 1. Bit 3 is reserved. This bit is read as 0. The write value should be 0.
Note 2. Phase counting mode cannot be set for TPU0, TPU3, TPU6, and TPU9. A 0 should be written to bit 2 for them.
Note 3. Bit 4 of TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11 that do not have TGRC is reserved. This bit is read as 0. The write value should be 0.
Note 4. Bits 5 and 7 of TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11 that do not have TGRD are reserved. These bits are read as 0. The write value should be 0.

MD[3:0] Bits (Mode Select)

Specifies the operating mode of the timer.

BFA Bit (Buffer Operation A)

Specifies whether TPUm.TGRA is to normally operate, or TPUm.TGRA and TPUm.TGRC are to be used together for buffer operation (m = 0, 3, 6, 9).
When TGRC is used as a buffer register, TGRC input capture/output compare is not generated.

BFB Bit (Buffer Operation B)

Specifies whether TPUm.TGRB is to normally operate, or TPUm.TGRB and TPUm.TGRD are to be used together for buffer operation (m = 0, 3, 6, 9).
When TGRD is used as a buffer register, TGRD input capture/output compare is not generated.

ICSELB Bit (TGRB Input Capture Input Select)

Selects the input capture input for TPUm.TGRB (m = 0 to 11). This function allows measurement of high-level width and period of the input pulse on a TIOCAn input pin.

ICSELD Bit (TGRD Input Capture Input Select)

Selects the input capture input for TPUm.TGRD (m = 0, 3, 6, 9).
This function allows measurement of high-level width and period of the input pulse on a TIOCCn input pin.

22.2.3 Timer I/O Control Register (TIORH, TIORL, TIOR)

TPU has four TIORH registers (one for TPU0, TPU3, TPU6, and TPU9), four TIORL registers (one for TPU0, TPU3, TPU6, and TPU9), and eight TIOR registers (one for TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11) Thus, the TPU has 16 timer I/O control registers in total.
TIORH, TIORL, and TIOR control registers TGRA, TGRB, TGRC, and TGRD.
Note that TIORH, TIORL, and TIOR are affected by the TMDR setting.
For details, see Table 22.14 to Table 22.21.
The initial output specified by TIORH, TIORL, and TIOR is valid when the counter is stopped (the TPUA.TSTRA.CSTj bit in unit 0 or the TPUA.TSTRB.CSTj bit in unit 1 is cleared to 0 (j = 0 to 5)). In PWM mode 2, the output at the time when the TCNT counter is cleared to 0 is specified as the initial output.
When buffer operation has been selected for register TGRC or TGRD, the settings of the corresponding set of IOC[3:0] or IOD[3:0] bits becomes ineffective, and the TGRC or TGRD register simply operates as a buffer.
To specify the input capture pin in TIORH, TIORL, or TIOR, set the bit in the port direction register (PDR) for the corresponding pin to 0 (input port), and set the bit in the port mode register (PMR) to 1 (uses the pin as an I/O port for peripheral functions). For details, see section 17, I/O Ports.

- TPU0.TIORH, TPU1.TIOR, TPU2.TIOR, TPU3.TIORH, TPU4.TIOR, TPU5.TIOR, TPU6.TIORH, TPU7.TIOR, TPU8.TIOR, TPU9.TIORH, TPU10.TIOR, TPU11.TIOR

Address(es): TPU0.TIORH A008 0112h, TPU1.TIOR A008 0122h, TPU2.TIOR A008 0132h, TPU3.TIORH A008 0142h, TPU4.TIOR A008 0152h, TPU5.TIOR A008 0162h, TPU6.TIORH A008 0192h, TPU7.TIOR A008 01A2h, TPU8.TIOR A008 01B2h, TPU9.TIORH A008 01C2h, TPU10.TIOR A008 01D2h, TPU11.TIOR A008 01E2h

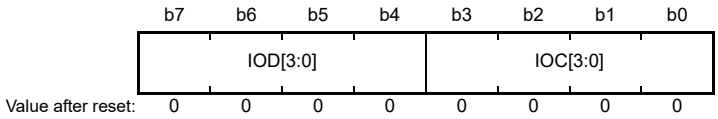
	b7	b6	b5	b4	b3	b2	b1	b0
	IOB[3:0]				IOA[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOA[3:0]	TGRA Control	See Table 22.14 to Table 22.19.*1	R/W
b7 to b4	IOB[3:0]	TGRB Control	See Table 22.14 to Table 22.19.*1	R/W

Note 1. If the IOn[3:0] (n = A, B) bits are changed to an “output prohibited” setting (0000b or 0100b) while the output of 0, output of 1, or toggling of the output in response to compare matches is in progress, the output becomes high impedance.

- TPU0.TIORL, TPU3.TIORL, TPU6.TIORL, TPU9.TIORL

Address(es): TPU0.TIORL A008 0113h, TPU3.TIORL A008 0143h, TPU6.TIORL A008 0193h, TPU9.TIORL A008 01C3h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	IOC[3:0]	TGRC Control	See Table 22.20 and Table 22.21.*1	R/W
b7 to b4	IOD[3:0]	TGRD Control	See Table 22.20 and Table 22.21.*1	R/W

Note 1. If the IOn[3:0] (n = C, D) bits are changed to an “output prohibited” setting (0000b or 0100b) while the output of 0, output of 1, or toggling of the output in response to compare matches is in progress, the output becomes high impedance.

IOA[3:0] Bits (TGRA Control)

Select the function of TPUm.TGRA (m = 0 to 11).

IOB[3:0] Bits (TGRB Control)

Select the function of TPUm.TGRB (m = 0 to 11).

IOC[3:0] Bits (TGRC Control)

Select the function of TPUm.TGRC (m = 0, 3, 6, 9).

IOD[3:0] Bits (TGRD Control)

Select the function of TPUm.TGRD (m = 0, 3, 6, 9).

Table 22.14 TPU0.TIORH, TPU6.TIORH

Bits IOA[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRA (m = 0, 6) Function	TIOCAn Pin (n = 0, 6) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCAn pin; input capture at both edges
1	1	x	x		• TPU0 Capture input source is TPU1 count clock Input capture at TPU1.TCNT count-up/count-down*1 • TPU6 Capture input source is TPU7 count clock Input capture at TPU7.TCNT count-up/count-down*1

Bits IOB[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRB (m = 0, 6) Function	TIOCBn Pin (n = 0, 6) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*2; input capture at rising edge
1	0	0	1		Capture input source is TIOCBn or TIOCAn pin*2; input capture at falling edge
1	0	1	x		Capture input source is TIOCBn or TIOCAn pin*2; input capture at both edges
1	1	x	x		• TPU0 Capture input source is TPU1 count clock Input capture at TPU1.TCNT count-up/count-down*1 • TPU6 Capture input source is TPU7 count clock Input capture at TPU7.TCNT count-up/count-down*1

x: Don't care

Note 1. When the TPUm.TCR.TPSC[2:0] bits are set to 000b and PCLKD/1 is used as the TPUm.TCNT count clock, this setting is invalid and input capture is not generated (m = 1, 7).

Note 2. Selected by the TPUm.TMDR.ICSELB bit (m = 0, 6).

Table 22.15 TPU1.TIOR, TPU7.TIOR

Bits IOA[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRA (m = 1, 7) Function	TIOCAn Pin (n = 1, 7) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCAn pin; input capture at both edges
1	1	x	x		• TPU1 Capture input source is TPU0.TGRA compare match/input capture Input capture at generation of TPU0.TGRA compare match/input capture • TPU7 Capture input source is TPU6.TGRA compare match/input capture Input capture at generation of TPU6.TGRA compare match/input capture

Bits IOB[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRB (m = 1, 7) Function	TIOCBn Pin (n = 1, 7) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*1; input capture at rising edge
1	0	0	1		Capture input source is TIOCBn or TIOCAn pin*1; input capture at falling edge
1	0	1	x		Capture input source is TIOCBn or TIOCAn pin*1; input capture at both edges
1	1	x	x		• TPU1 Capture input source is TPU0.TGRC compare match/input capture Input capture at generation of TPU0.TGRC compare match/input capture • TPU7 Capture input source is TPU6.TGRC compare match/input capture Input capture at generation of TPU6.TGRC compare match/input capture

x: Don't care

Note 1. Selected by the TPUm.TMDR.ICSELB bit (m = 1, 7).

Table 22.16 TPU2.TIOR, TPU8.TIOR

Bits IOA[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRA (m = 2, 8) Function	TIOCAn Pin (n = 2, 8) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	x	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	x	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	x	1	x		Capture input source is TIOCAn pin; input capture at both edges

Bits IOB[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRB (m = 2, 8) Function	TIOCBn Pin (n = 2, 8) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	x	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*1; input capture at rising edge
1	x	0	1		Capture input source is TIOCBn or TIOCAn pin*1; input capture at falling edge
1	x	1	x		Capture input source is TIOCBn or TIOCAn pin*1; input capture at both edges

x: Don’t care

Note 1. Selected by the TPUm.TMDR.ICSELB bit (m = 2, 8).

Table 22.17 TPU3.TIORH, TPU9.TIORH

Bits IOA[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRA (m = 3, 9) Function	TIOCAn Pin (n = 3, 9) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCAn pin; input capture at both edges
1	1	x	x		• TPU3 Capture input source is TPU4 count clock Input capture at TPU4.TCNT count-up/count-down*1 • TPU9 Capture input source is TPU10 count clock Input capture at TPU10.TCNT count-up/count-down*1

Bits IOB[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRB (m = 3, 9) Function	TIOCBn Pin (n = 3, 9) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*2; input capture at rising edge
1	0	0	1		Capture input source is TIOCBn or TIOCAn pin*2; input capture at falling edge
1	0	1	x		Capture input source is TIOCBn or TIOCAn pin*2; input capture at both edges
1	1	x	x		• TPU3 Capture input source is TPU4 count clock Input capture at TPU4.TCNT count-up/count-down*1 • TPU9 Capture input source is TPU10 count clock Input capture at TPU10.TCNT count-up/count-down*1

x: Don't care

Note 1. When the TPUm.TCR.TPSC[2:0] bits are set to 000b and PCLKD/1 is used as the TPUm.TCNT count clock, this setting is invalid and input capture is not generated (m = 4, 10).

Note 2. Selected by the TPUm.TMDR.ICSELB bit (m = 3, 9).

Table 22.18 TPU4.TIOR, TPU10.TIOR

Bits IOA[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRA (m = 4, 10) Function	TIOCAn Pin (n = 4, 10) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCAn pin; input capture at both edges
1	1	x	x		• TPU4 Capture input source is TPU3.TGRA compare match/input capture Input capture at generation of TPU3.TGRA compare match/input capture • TPU10 Capture input source is TPU9.TGRA compare match/input capture Input capture at generation of TPU9.TGRA compare match/input capture

Bits IOB[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRB (m = 4, 10) Function	TIOCBn Pin (n = 4, 10) Function and Related Issue
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*1; input capture at rising edge
1	0	0	1		Capture input source is TIOCBn or TIOCAn pin*1; input capture at falling edge
1	0	1	x		Capture input source is TIOCBn or TIOCAn pin*1; input capture at both edges
1	1	x	x		• TPU4 Capture input source is TPU3.TGRC compare match/input capture Input capture at generation of TPU3.TGRC compare match/input capture • TPU10 Capture input source is TPU9.TGRC compare match/input capture Input capture at generation of TPU9.TGRC compare match/input capture

x: Don't care

Note 1. Selected by the TPUm.TMDR.ICSELB bit (m = 4, 10).

Table 22.19 TPU5.TIOR, TPU11.TIOR

Bits IOA[3:0]				Description	
b3	**b2**	**b1**	**b0**	**TPUm.TGRA (m = 5, 11) Function**	**TIOCAn Pin (n = 5, 11) Function and Related Issue**
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	x	0	0	Input capture register	Capture input source is TIOCAn pin; input capture at rising edge
1	x	0	1		Capture input source is TIOCAn pin; input capture at falling edge
1	x	1	x		Capture input source is TIOCAn pin; input capture at both edges

Bits IOB[3:0]				Description	
b7	**b6**	**b5**	**b4**	**TPUm.TGRB (m = 5, 11) Function**	**TIOCBn Pin (n = 5, 11) Function and Related Issue**
0	0	0	0	Output compare register	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	x	0	0	Input capture register	Capture input source is TIOCBn or TIOCAn pin*1; input capture at rising edge
1	x	0	1		Capture input source is TIOCBn or TIOCAn pin*1; input capture at falling edge
1	x	1	x		Capture input source is TIOCBn or TIOCAn pin*1; input capture at both edges

x: Don’t care

Note 1. Selected by the ITPUm.TMDR.ICSELB bit (m = 5, 11).

Table 22.20 TPU0.TIORL, TPU6.TIORL

Bits IOC[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRC (m = 0, 6) Function	TIOCCn Pin (n = 0, 6) Function and Related Issue
0	0	0	0	Output compare register*1	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register*1	Capture input source is TIOCCn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCCn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCCn pin; input capture at both edges
1	1	x	x		• TPU0 Capture input source is TPU1 count clock Input capture at TPU1.TCNT count-up/count-down*3 • TPU6 Capture input source is TPU7 count clock Input capture at TPU7.TCNT count-up/count-down*3

Bits IOD[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRD (m = 0, 6) Function	TIOCDn Pin (n = 0, 6) Function and Related Issue
0	0	0	0	Output compare register*2	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register*2	Capture input source is TIOCDn or TIOCCn pin*4; input capture at rising edge
1	0	0	1		Capture input source is TIOCDn or TIOCCn pin*4; input capture at falling edge
1	0	1	x		Capture input source is TIOCDn or TIOCCn pin*4; input capture at both edges
1	1	x	x		• TPU0 Capture input source is TPU1 count clock Input capture at TPU1.TCNT count-up/count-down*3 • TPU6 Capture input source is TPU7 count clock Input capture at TPU7.TCNT count-up/count-down*3

x: Don't care

Note 1. When the TPUm.TMDR.BFA bit is set to 1 (TPUm.TGRA and TPUm.TGRC are used for buffer operation) and TPUm.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated (m = 0, 6).

Note 2. When the TPUm.TMDR.BFB bit is set to 1 (TPUm.TGRB and TPUm.TGRD are used for buffer operation) and TPUm.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated (m = 0, 6).

Note 3. When the TPUm.TCR.TPSC[2:0] bits are set to 000b and PCLKD/1 is used as the TPUm.TCNT count clock, this setting is invalid and input capture is not generated. (m = 1, 7)

Note 4. Selected by the TPUm.TMDR.ICSELD bit (m = 0, 6).

Table 22.21 TPU3.TIORL, TPU9.TIORL

Bits IOC[3:0]				Description	
b3	b2	b1	b0	TPUm.TGRC (m = 3, 9) Function	TIOCCn Pin (n = 3, 9) Function and Related Issue
0	0	0	0	Output compare register*1	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register*1	Capture input source is TIOCCn pin; input capture at rising edge
1	0	0	1		Capture input source is TIOCCn pin; input capture at falling edge
1	0	1	x		Capture input source is TIOCCn pin; input capture at both edges
1	1	x	x		• TPU3 Capture input source is TPU4 count clock Input capture at TPU4.TCNT count-up/count-down*3 • TPU9 Capture input source is TPU10 count clock Input capture at TPU10.TCNT count-up/count-down*3

Bits IOD[3:0]				Description	
b7	b6	b5	b4	TPUm.TGRD (m = 3, 9) Function	TIOCDn Pin (n = 3, 9) Function and Related Issue
0	0	0	0	Output compare register*2	Output disabled
0	0	0	1		Initial output is low output; low output at compare match
0	0	1	0		Initial output is low output; high output at compare match
0	0	1	1		Initial output is low output; toggle output at compare match
0	1	0	0		Output disabled
0	1	0	1		Initial output is high output; low output at compare match
0	1	1	0		Initial output is high output; high output at compare match
0	1	1	1		Initial output is high output; toggle output at compare match
1	0	0	0	Input capture register*2	Capture input source is TIOCDn or TIOCCn pin*4; input capture at rising edge
1	0	0	1		Capture input source is TIOCDn or TIOCCn pin*4; input capture at falling edge
1	0	1	x		Capture input source is TIOCDn or TIOCCn pin*4; input capture at both edges
1	1	X	x		• TPU3 Capture input source is TPU4 count clock Input capture at TPU4.TCNT count-up/count-down*3 • TPU9 Capture input source is TPU10 count clock Input capture at TPU10.TCNT count-up/count-down*3

x: Don't care

Note 1. When the TPUm.TMDR.BFA bit is set to 1 (TPUm.TGRA and TPUm.TGRC are used for buffer operation) and TPUm.TGRC is used as a buffer register, this setting is invalid and input capture/output compare is not generated (m = 3, 9).

Note 2. When the TPUm.TMDR.BFB bit is set to 1 (TPUm.TGRB and TPUm.TGRD are used for buffer operation) and TPUm.TGRD is used as a buffer register, this setting is invalid and input capture/output compare is not generated (m = 3, 9).

Note 3. When the TPUm.TCR.TPSC[2:0] bits are set to 000b and PCLKD/1 is used as the TPUm.TCNT count clock, this setting is invalid and input capture is not generated (m = 4, 10).

Note 4. Selected by the TPUm.TMDR.ICSELD bit (m = 3, 9).

22.2.4 Timer Interrupt Enable Register (TIER)

TPU has 12 TIER registers in total (one register per channel).

TPUAm.TIER controls enabling or disabling of interrupt requests to individual channels (m = 0 to 11).

Address(es): TPU0.TIER A008 0114h, TPU1.TIER A008 0124h, TPU2.TIER A008 0134h, TPU3.TIER A008 0144h, TPU4.TIER A008 0154h, TPU5.TIER A008 0164h, TPU6.TIER A008 0194h, TPU7.TIER A008 01A4h, TPU8.TIER A008 01B4h, TPU9.TIER A008 01C4h, TPU10.TIER A008 01D4h, TPU11.TIER A008 01E4h

	b7	b6	b5	b4	b3	b2	b1	b0
	TTGE	—	TCIEU	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGIEA	TGRA Interrupt Enable	0: Interrupt requests (TGImA) disabled 1: Interrupt requests (TGImA) enabled (m = 0 to 11)	R/W
b1	TGIEB	TGRB Interrupt Enable	0: Interrupt requests (TGImB) disabled 1: Interrupt requests (TGImB) enabled (m = 0 to 11)	R/W
b2	TGIEC*1	TGRC Interrupt Enable	0: Interrupt requests (TGImC) disabled 1: Interrupt requests (TGImC) enabled (m = 0, 3, 6, 9)	R/W
b3	TGIED*1	TGRD Interrupt Enable	0: Interrupt requests (TGImD) disabled 1: Interrupt requests (TGImD) enabled (m = 0, 3, 6, 9)	R/W
b4	TCIEV	Overflow Interrupt Enable	0: Interrupt requests (TCImV) disabled 1: Interrupt requests (TCImV) enabled (m = 0 to 11)	R/W
b5	TCIEU*2	Underflow Interrupt Enable	0: Interrupt requests (TCImU) disabled 1: Interrupt requests (TCImU) enabled (m = 1, 2, 4, 5, 7, 8, 10, 11)	R/W
b6	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b7	TTGE*3	A/D Conversion Start Request Enable	0: A/D conversion start request generation disabled 1: A/D conversion start request generation enabled	R/W

Note 1. Bits 3 and 2 in TPU1.TIER, TPU2.TIER, TPU4.TIER, and TPU5.TIER of unit 0 and in TPU7.TIER, TPU8.TIER, TPU10.TIER, and TPU11.TIER of unit 1 are reserved. These bits are read as 0. The write value should be 0.

Note 2. Bit 5 in TPU0.TIER and TPU3.TIER of unit 0 and in TPU6.TIER and TPU9.TIER of unit 1 is reserved. This bit is read as 0. The write value should be 0.

Note 3. Bit 7 in TPU5.TIER of unit 0 and TPU11.TIER of unit 1 is reserved. This bit is read as 0. The write value should be 0.

TGIEA Bit (TGRA Interrupt Enable)

This bit enables or disables interrupt TGImA (m = 0 to 11).

TGIEB Bit (TGRB Interrupt Enable)

This bit enables or disables interrupt TGImB (m = 0 to 11).

TGIEC Bit (TGRC Interrupt Enable)

This bit enables or disables interrupt TGImC (m = 0, 3, 6, 9).

TGIED Bit (TGRD Interrupt Enable)

This bit enables or disables interrupt TGImD (m = 0, 3, 6, 9).

TCIEV Bit (Overflow Interrupt Enable)

This bit enables or disables interrupt TCImV (m = 0 to 11).

TCIEU Bit (Underflow Interrupt Enable)

This bit enables or disables interrupt TCImU (m = 1, 2, 4, 5, 7, 8, 10, 11).

TTGE Bit (A/D Conversion Start Request Enable)

Enables/disables generation of A/D conversion start requests by TPUm.TGRA (m = 0 to 4, 6 to 10) input capture/ compare match.

22.2.5 Timer Status Register (TSR)

TPU has 12 TSR registers in total (one register per channel).

TPUm.TSR indicates the status of individual channels, and the count direction of TPUm.TCNT counter (m = 0 to 11).

Address(es): TPU0.TSR A008 0115h, TPU1.TSR A008 0125h, TPU2.TSR A008 0135h, TPU3.TSR A008 0145h, TPU4.TSR A008 0155h, TPU5.TSR A008 0165h, TPU6.TSR A008 0195h, TPU7.TSR A008 01A5h, TPU8.TSR A008 01B5h, TPU9.TSR A008 01C5h, TPU10.TSR A008 01D5h, TPU11.TSR A008 01E5h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCFD	—	TCFU	TCFV	TGFD	TGFC	TGFB	TGFA
Value after reset:	1	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TGFA	Input Capture/Output Compare Flag A	0: Input capture to TPUm.TGRA or compare match with TPUm.TGRA has not occurred. 1: Input capture to TPUm.TGRA or compare match with TPUm.TGRA has occurred. (m = 0 to 11)	R/W*2
b1	TGFB	Input Capture/Output Compare Flag B	0: Input capture to TPUm.TGRB or compare match with TPUm.TGRB has not occurred. 1: Input capture to TPUm.TGRB or compare match with TPUm.TGRB has occurred. (m = 0 to 11)	R/W*2
b2	TGFC*4	Input Capture/Output Compare Flag C	0: Input capture to TPUm.TGRC or compare match with TPUm.TGRC has not occurred. 1: Input capture to TPUm.TGRC or compare match with TPUm.TGRC has occurred. (m = 0, 3, 6, 9)	R/W*2
b3	TGFD*4	Input Capture/Output Compare Flag D	0: Input capture to TPUm.TGRD or compare match with TPUm.TGRD has not occurred. 1: Input capture to TPUm.TGRD or compare match with TPUm.TGRD has occurred. (m = 0, 3, 6, 9)	R/W*2
b4	TCFV	Overflow Flag	0: TPUm.TCNT has not overflowed. 1: TPUm.TCNT has overflowed. (m = 0 to 11)	R/W*2
b5	TCFU*3	Underflow Flag	0: TPUm.TCNT has not underflowed. 1: TPUm.TCNT has underflowed. (m = 1, 2, 4, 5, 7, 8, 10, 11)	R/W*2
b6	—	Reserved	This bit is read as 1.	R
b7	TCFD*1	Counting Direction Flag	0: TPUm.TCNT counter counts down. 1: TPUm.TCNT counter counts up. (m = 1, 2, 4, 5, 7, 8, 10, 11)	R

Note 1. Bit 7 in TPU0.TSR and TPU3.TSR of unit 0 and in TPU6.TSR and TPU9.TSR of unit 1 is reserved. The bit is read as 1. The write value should be 1.

Note 2. Only writing 0 to this bit is possible; this clears the flag.

Note 3. Bit 5 in TPU0.TSR and TPU3.TSR of unit 0 and in TPU6.TSR and TPU9.TSR of unit 1 is reserved. The bit is read as 0. The write value should be 0.

Note 4. Bits 2 and 3 in TPU1.TSR, TPU2.TSR, TPU4.TSR, and TPU5.TSR of unit 0 and in TPU7.TSR, TPU8.TSR, TPU10.TSR, and TPU11.TSR of unit 1 are reserved. The bits are read as 0. The write value should be 0.

TGFA Flag (Input Capture/Output Compare Flag A)

This status flag indicates that input capture to TPUm.TGRA or compare match with TPUm.TGRA (m = 0 to 11) has occurred.

[Setting conditions]

- When TPUm.TGRA holds the value for comparison in output-compare operations, TPUm.TCNT matches TPUm.TGRA.
- When TPUm.TGRA is serving as an input-capture register, the input-capture signal has caused transfer of the value in TPUm.TCNT to TPUm.TGRA.

[Clearing condition]

- Writing 0 to TGFA after reading its value as 1.

TGFB Flag (Input Capture/Output Compare Flag B)

This status flag indicates that input capture to TPUm.TGRB or compare match with TPUm.TGRB (m = 0 to 11) has occurred.

[Setting conditions]

- When TPUm.TGRB holds the value for comparison in output-compare operations, TPUm.TCNT matches TPUm.TGRB.
- When TPUm.TGRB is serving as an input-capture register, the input-capture signal has caused transfer of the value in TPUm.TCNT to TPUm.TGRB.

[Clearing condition]

- Writing 0 to TGFB after reading its value as 1.

TGFC Flag (Input Capture/Output Compare Flag C)

This status flag indicates that input capture to TPUm.TGRC or compare match with TPUm.TGRC (m = 0, 3, 6, 9) has occurred.

[Setting conditions]

- When TPUm.TGRC holds the value for comparison in output-compare operations, TPUm.TCNT matches TPUm.TGRC.
- When TPUm.TGRC is serving as an input-capture register, the input-capture signal has caused transfer of the value in TPUm.TCNT to TPUm.TGRC.

[Clearing condition]

- Writing 0 to TGFC after reading its value as 1.

TGFD Flag (Input Capture/Output Compare Flag D)

This status flag indicates that input capture to TPUm.TGRD or compare match with TPUm.TGRD (m = 0, 3, 6, 9) has occurred.

[Setting conditions]

- When TPUm.TGRD holds the value for comparison in output-compare operations, TPUm.TCNT matches TPUm.TGRD.
- When TPUm.TGRD is serving as an input-capture register, the input-capture signal has caused transfer of the value in TPUm.TCNT to TPUm.TGRD.

[Clearing condition]

- Writing 0 to TGFD after reading its value as 1.

TCFV Flag (Overflow Flag)

This status flag indicates an overflow of TPUm.TCNT (m = 0 to 11).

[Setting condition]

- Overflow of the value in TPUm.TCNT (TPUm.TCNT counted from FFFFh to 0000h).

[Clearing condition]

- Writing 0 to TCFV after reading its value as 1.

TCFU Flag (Underflow Flag)

This status flag indicates an underflow of TPUm.TCNT (m = 1, 2, 4, 5, 7, 8, 10, 11).

[Setting condition]

- Underflow of the value in TPUm.TCNT (TPUm.TCNT counted from 0000h to FFFFh).

[Clearing condition]

- Writing 0 to TCFU after reading its value as 1.

22.2.6 Timer Counter (TCNT)

TPUm.TCNT is a 16-bit counter that counts the internal clock or external events (m = 0 to 11).
This counter can be read/written in 16-bit units.
This counter is initialized to 0000h by a reset.

Address(es): TPU0.TCNT A008 0116h, TPU1.TCNT A008 0126h, TPU2.TCNT A008 0136h, TPU3.TCNT A008 0146h, TPU4.TCNT A008 0156h, TPU5.TCNT A008 0166h, TPU6.TCNT A008 0196h, TPU7.TCNT A008 01A6h, TPU8.TCNT A008 01B6h, TPU9.TCNT A008 01C6h, TPU10.TCNT A008 01D6h, TPU11.TCNT A008 01E6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

22.2.7 Timer General Register A (TGRA)
Timer General Register B (TGRB)
Timer General Register C (TGRC)
Timer General Register D (TGRD)

TPU has 32 TGR registers in total, four each for TPU0, TPU3, TPU6, and TPU9 and two each for TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11.
TPUm.TGRA (m = 0 to 11), TPUm.TGRB (m = 0 to 11), TPUm.TGRC (m = 0, 3, 6, 9), and TPUm.TGRD (m = 0, 3, 6, 9) are 16-bit registers with a dual function as output compare and input capture registers.
These registers can be read/written in 16-bit units.
TPUm.TGRC and TPUm.TGRD can also be specified for operation as buffer registers. Register combinations during buffer operations are TPUm.TGRA-TPUm.TGRC and TPUm.TGRB-TPUm.TGRD.

Address(es): TPU0.TGRA A008 0118h, TPU0.TGRB A008 011Ah, TPU0.TGRC A008 011Ch, TPU0.TGRD A008 011Eh, TPU1.TGRA A008 0128h, TPU1.TGRB A008 012Ah, TPU2.TGRA A008 0138h, TPU2.TGRB A008 013Ah, TPU3.TGRA A008 0148h, TPU3.TGRB A008 014Ah, TPU3.TGRC A008 014Ch, TPU3.TGRD A008 014Eh, TPU4.TGRA A008 0158h, TPU4.TGRB A008 015Ah, TPU5.TGRA A008 0168h, TPU5.TGRB A008 016Ah, TPU6.TGRA A008 0198h, TPU6.TGRB A008 019Ah, TPU6.TGRC A008 019Ch, TPU6.TGRD A008 019Eh, TPU7.TGRA A008 01A8h, TPU7.TGRB A008 01AAh, TPU8.TGRA A008 01B8h, TPU8.TGRB A008 01BAh, TPU9.TGRA A008 01C8h, TPU9.TGRB A008 01CAh, TPU9.TGRC A008 01CCh, TPU9.TGRD A008 01CEh, TPU10.TGRA A008 01D8h, TPU10.TGRB A008 01DAh, TPU11.TGRA A008 01E8h, TPU11.TGRB A008 01EAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

22.2.8 Timer Start Register (TSTRA, TSTRB)

TSTRA starts or stops count operation for TCNT counter of TPU0 to TPU5.
TSTRB starts or stops count operation for TCNT counter of TPU6 to TPU11.
Before setting the operating mode in TPUm.TMDR or setting the TPUm.TCNT count clock in TPUm.TCR, stop the TPUm.TCNT counter.

Address(es): TPUA.TSTRA A008 0100h, TPUA.TSTRB A008 0180h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CST5	CST4	CST3	CST2	CST1	CST0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CST0	Counter Start 0	0: TCNT count operation is stopped 1: TCNT performs count operation	R/W
b1	CST1	Counter Start 1		R/W
b2	CST2	Counter Start 2		R/W
b3	CST3	Counter Start 3		R/W
b4	CST4	Counter Start 4		R/W
b5	CST5	Counter Start 5		R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CSTn Bits (Counter Start) (n = 0 to 5)

These bits start or stop the TCNT counter.
When the CSTn bit is cleared to 0 with CSTn = 1 and the corresponding TIOCyn pin (y = A to D, n = 0 to 5) specified for output, the counter stops but the output compare output level of the corresponding TIOCyn pin is retained.
If TIORH, TIORL, or TIOR is written to when the CSTn bit is 0, the pin output level will be changed to the set initial output value.

22.2.9 Timer Synchronous Register (TSYRA, TSYRB)

TSYRA selects independent operation or synchronous operation for the TCNT counters of TPU0 to TPU5.
TSYRB selects independent operation or synchronous operation for the TCNT counters of TPU6 to TPU11.

Address(es): TPUA.TSYRA A008 0101h, TPUA.TSYRB A008 0181h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SYNC5	SYNC4	SYNC3	SYNC2	SYNC1	SYNC0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SYNC0	Timer Synchronization 0	0: TCNT operates independently (TCNT presetting/clearing is unrelated to other channels) 1: TCNT performs synchronous operation*1 (TCNT synchronous presetting/synchronous clearing is possible)	R/W
b1	SYNC1	Timer Synchronization 1		R/W
b2	SYNC2	Timer Synchronization 2		R/W
b3	SYNC3	Timer Synchronization 3		R/W
b4	SYNC4	Timer Synchronization 4		R/W
b5	SYNC5	Timer Synchronization 5		R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To set synchronous operation, the SYNCn bit (n = 0 to 5) for at least two channels must be set to 1. To set synchronous clearing, the TCNT clearing source must also be set by the TCR.CCLR[2:0] bits in addition to the SYNCn bit.

SYNCn Bits (Timer Synchronization) (n = 0 to 5)

These bits select whether the TCNT operation is independent of or synchronized with TCNT of other channels.
When synchronous operation is selected, synchronous presetting of multiple TCNT counters and synchronous clearing through counter clearing on another channel are possible.

22.2.10 Noise Filter Control Register (NFCR)

TPU has 12 noise filter control registers in total (one register per channel).
TPUm.NFCR controls noise filtering of input capture signal on each channel. Only set the TPUm.NFCR register while the TPUm.TCNT counter is stopped (m = 0 to 11).

Address(es): TPU0.NFCR A008 0108h, TPU1.NFCR A008 0109h, TPU2.NFCR A008 010Ah, TPU3.NFCR A008 010Bh, TPU4.NFCR A008 010Ch, TPU5.NFCR A008 010Dh, TPU6.NFCR A008 0188h, TPU7.NFCR A008 0189h, TPU8.NFCR A008 018Ah, TPU9.NFCR A008 018Bh, TPU10.NFCR A008 018Ch, TPU11.NFCR A008 018Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	NFCS[1:0]		NFDEN	NFCEN	NFBEN	NFAEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NFAEN	Noise Filter Enable A	0: The noise filter for TIOCAm is disabled. 1: The noise filter for TIOCAm is enabled. (m = 0 to 11)	R/W
b1	NFBEN	Noise Filter Enable B	0: The noise filter for TIOCBm is disabled. 1: The noise filter for TIOCBm is enabled. (m = 0 to 11)	R/W
b2	NFCEN*1	Noise Filter Enable C	0: The noise filter for TIOCCm is disabled. 1: The noise filter for TIOCCm is enabled. (m = 0, 3, 6, 9)	R/W
b3	NFDEN*1	Noise Filter Enable D	0: The noise filter for TIOCDm is disabled. 1: The noise filter for TIOCDm is enabled. (m = 0, 3, 6, 9)	R/W
b5, b4	NFCS[1:0]	Noise Filter Clock Select	00: PCLKD/1 01: PCLKD/8 10: PCLKD/32 11: Clock source that drives counting	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Bits 2 and 3 in TPU1.NFCR, TPU2.NFCR, TPU4.NFCR, and TPU5.NFCR of unit 0 and bits 2 and 3 in TPU7.NFCR, TPU8.NFCR, TPU10.NFCR, TPU11.NFCR of unit 1 are reserved. The bits are read as 0. Writing to these bits is not possible.

NFAEN Bit (Noise Filter Enable A)

This bit disables or enables the noise filter for the TIOCAm pin (m = 0 to 11).
Since unexpected edges may be internally generated when the value of NFAEN is changed, select the output compare function in the timer I/O control register before changing the NFAEN value.

NFBEN Bit (Noise Filter Enable B)

This bit disables or enables the noise filter for the TIOCBm pin (m = 0 to 11).
Since unexpected edges may be internally generated when the value of NFBEN is changed, select the output compare function in the timer I/O control register before changing the NFBEN value.

NFCEN Bit (Noise Filter Enable C)

This bit disables or enables the noise filter for the TIOCCm pin (m = 0, 3, 6, 9).
Since unexpected edges may be internally generated when the value of NFCEN is changed, select the output compare function in the timer I/O control register before changing the NFCEN value.

NFDEN Bit (Noise Filter Enable D)

This bit disables or enables the noise filter for the TIOCDm pin (m = 0, 3, 6, 9).
Since unexpected edges may be internally generated when the value of NFDEN is changed, select the output compare function in the timer I/O control register before changing the NFDEN value.

NFCS[1:0] Bits (Noise Filter Clock Select)

These bits select the sampling clock for the noise filter.
When the count source is selected with NFCS[1:0] bits set to 11b, the clock that can be used as sampling clock are the internal clocks other than PCLKD/1 specified with the TPSC[2:0] bits and the external clock. To select the PCLKD/1 as both the counter clock and the sampling clock, set the NFCS[1:0] bits to 00b.
The input-capture signal is sampled on rising edges of the selected clock signal. If the sampled levels match three times in a row, the given level is passed through as the input-capture signal. If the levels do not match, the existing value is retained.
After setting the NFCS[1:0] bits, wait for two selected sampling periods before setting the input capture function.

22.2.11 PWM Feedback Select Register (PWMFBSLR)

PWMFBSLR controls internal PWM feedback input for the TPU.
This function can capture any of the PWM output signals generated with MTU3a and GPTa as an input capture input through the inside of this LSI, and measure the cycle and duty cycle of the PWM waveform.

Address(es): TPUSL.PWMFBSLR A008 0200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FBSL1[2:0]			—	TPU1 EN	—	—	—	FBSL0[2:0]			—	TPU0 EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TPU0EN	TPU (Unit 0) Internal PWM Feedback Enable*1	0: Disable (Normal TIOCAn and TIOCBn pins (n = 0 to 5) are used for TPU input capture.) 1: Enable (Internal PWM feedback input can be selected.)	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4 to b2	FBSL0[2:0]	Internal PWM Feedback Input Source Select 0	100: PWM output signals of MTU3 and MTU4 (Inside the LSI) 101: PWM output signals of MTU6 and MTU7 (Inside the LSI) 110: PWM output signals of GPT0 to GPT2 (Inside the LSI) Do not set any values other than above.	R/W
b7 to b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	TPU1EN	TPU (Unit 1) Internal PWM Feedback Enable	0: Disable (TIOCAn and TIOCBn pins (n = 6 to 11) are used for TPU input capture.) 1: Enable (Internal PWM feedback input can be selected.)	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12 to b10	FBSL1[2:0]	PWM Feedback Input Source Select 1	100: PWM output signals of MTU3 and MTU4 (Inside the LSI) 101: PWM output signals of MTU6 and MTU7 (Inside the LSI) 110: PWM output signals of GPT0 to GPT2 (Inside the LSI) Do not set any values other than above	R/W
b31 to b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Be sure to enable selection of the PWM feedback input source to be used with the FBSL0[2:0] and FBSL1[2:0] bits before setting the TPUnEN bit to enable internal PWM feedback input. The setting value of FBSL0[2:0] and FBSL1[2:0] after reset is 000h (Setting prohibited). Settings of the TPUnEN bit, and FBSL0[2:0] and FBSL1[2:0] can be performed at the same time.

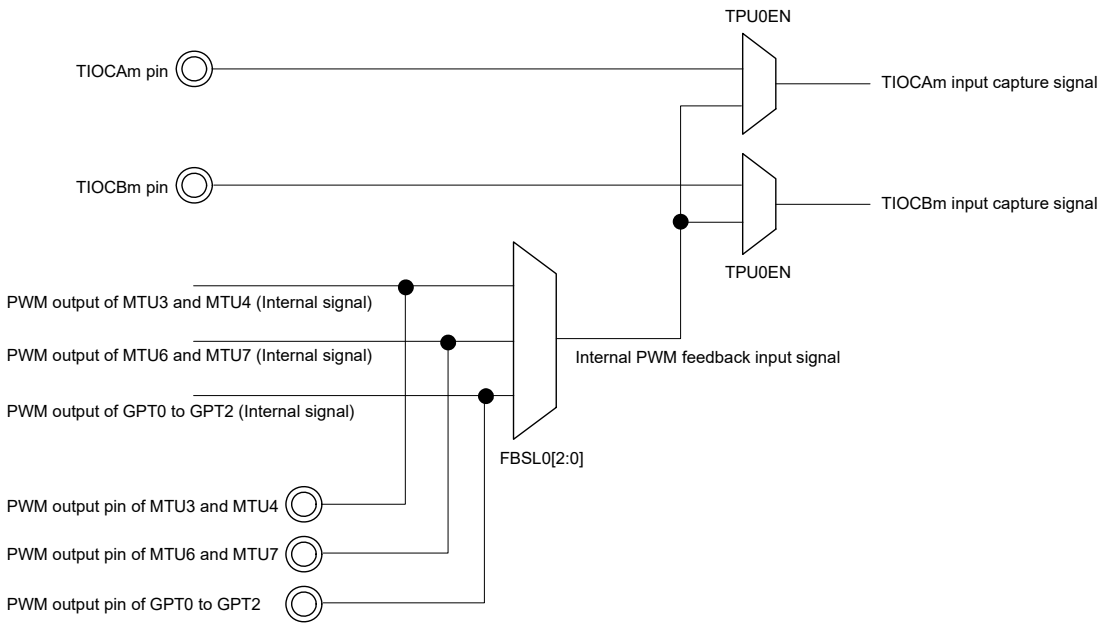
TPUnEN (TPU Unit n Internal PWM Feedback Enable) (n = 0, 1)

This bit enables TPU internal PWM feedback input.
If this function is enabled (= 1b), the PWM signal selected by the FBSLn bit is input as the TPU input capture signal through inside of the LSI. In this case, input signals on the TIOCAm and TIOCBm pins are not captured as input capture signals (m = 0 to 5 when n = 0; m = 6 to 11 when n = 1).
If this function is disabled (= 0b), input signals on the TIOCAm and TIOCBm pins are input as input capture signals.
To use normal input capture function, set this function disabled (= 0b).
When using this bit, set TGRA and TGRB of each TPU channel for input capture.
Setting of this bit should be made while TPU operation is stopped.

FBSLn (Internal PWM Feedback Input Source Select n) (n = 0, 1)

These bits select (from MTU3, MTU4, MTU6, MTU7, GPT 0, GPT1, and GPT2) the input source of internal PWM feedback that is input to TPU.
If the TPUnEN bit is “disable” (= 0b), the setting value in the FBSLn bits is invalid.
To use these bits, set TGRA and TGRB of each TPU channel for input capture. Setting of these bits should be made while TPU operation is stopped.

Figure 22.3 shows the PWM feedback setting and TPU input capture configuration. Table 22.22 describes the correspondence between the TPU input capture signals and individual I/O pins when PWM feedback is placed.



m = 0 to 5
Note: For details about the relationship between the PWMFBSLR.FBSLn[0:2] setting and the PWM output pins of MTU3a and GPTa, see Table 22.22.

Figure 22.3 PWM Feedback Setting and TPU Input Capture Configuration (Example of Unit 0)

Table 22.22 Correspondence Between the PWM Feedback Settings and TPU Input Capture Input Pins (n = 0, 1)

	Internal PWM Feedback Input Disabled (TPUnEN bit = 0)	Internal PWM Feedback Input Enabled (TPUnEN bit = 1)		
TPU Input Capture Signal	TPU Input Capture Pin	PWM Output Pin of MTU3 and MTU4 (FBSLn[2:0] = 100b)	PWM Output Pin of MTU6 and MTU7 (FBSLn[2:0] = 101b)	PWM Output Pin of GPT0 to GPT2 (FBSLn[2:0] = 110b)
TIOCA0	TIOCA0	MTIOC3B	MTIOC6B	GTIOC0A
TIOCB0	TIOCB0	MTIOC3B	MTIOC6B	GTIOC0A
TIOCA1	TIOCA1	MTIOC3D	MTIOC6D	GTIOC0B
TIOCB1	TIOCB1	MTIOC3D	MTIOC6D	GTIOC0B
TIOCA2	TIOCA2	MTIOC4A	MTIOC7A	GTIOC1A
TIOCB2	TIOCB2	MTIOC4A	MTIOC7A	GTIOC1A
TIOCA3	TIOCA3	MTIOC4C	MTIOC7C	GTIOC1B
TIOCB3	TIOCB3	MTIOC4C	MTIOC7C	GTIOC1B
TIOCA4	TIOCA4	MTIOC4B	MTIOC7B	GTIOC2A
TIOCB4	TIOCB4	MTIOC4B	MTIOC7B	GTIOC2A
TIOCA5	TIOCA5	MTIOC4D	MTIOC7D	GTIOC2B
TIOCB5	TIOCB5	MTIOC4D	MTIOC7D	GTIOC2B

22.3 Operation

22.3.1 Basic Functions

Each channel has a TPUm.TCNT counter and a TPUm.TGRy register (y = A to D).
TCNT is a 16-bit up-counter, which can function as a free-running counter, periodic counter, or event counter.
TGRy can be used as an input capture register or output compare register.

(1) Counter Operation

When the TSTRA.CSTj bit of unit 0 and the TSTRB.CSTj bit (j = 0 to 5) of unit 1 are set to 1, the TCNT counter for the corresponding channel starts counting.

(a) Example of count operation setting procedure

Figure 22.4 shows an example of the count operation setting procedure.

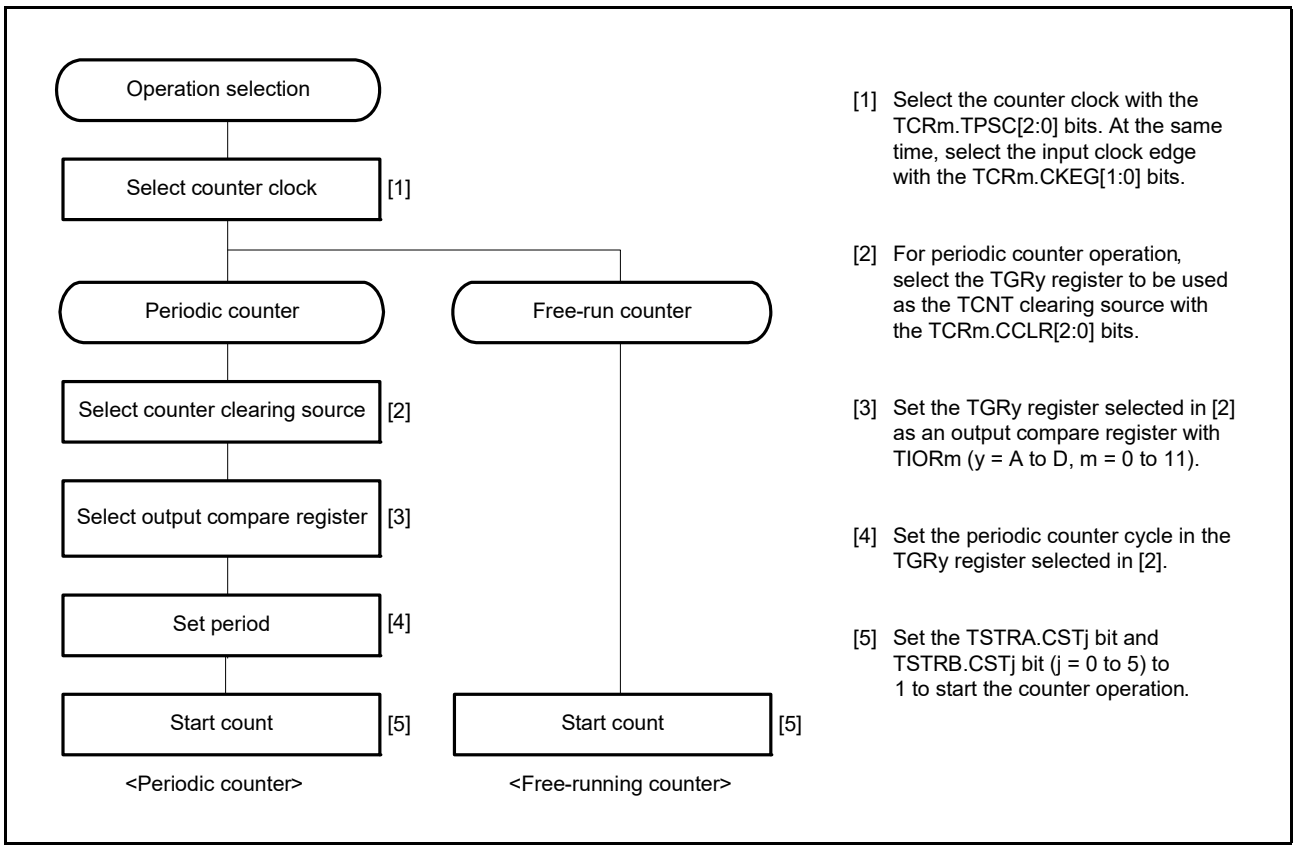


Figure 22.4 Example of Counter Operation Setting Procedure

(b) Free-running count operation and periodic count operation

Immediately after a reset, the TPUm.TCNT counters are all set as free-running counters. When the relevant bit in TSTRA of unit 0 or in TSTRB of unit 1 is set to 1, the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (changes from FFFFh to 0000h), the TPU requests an overflow interrupt (TCImV). After an overflow, TCNT restarts counting up from 0000h (m = 0 to 11).
Figure 22.5 shows free-running counter operation.

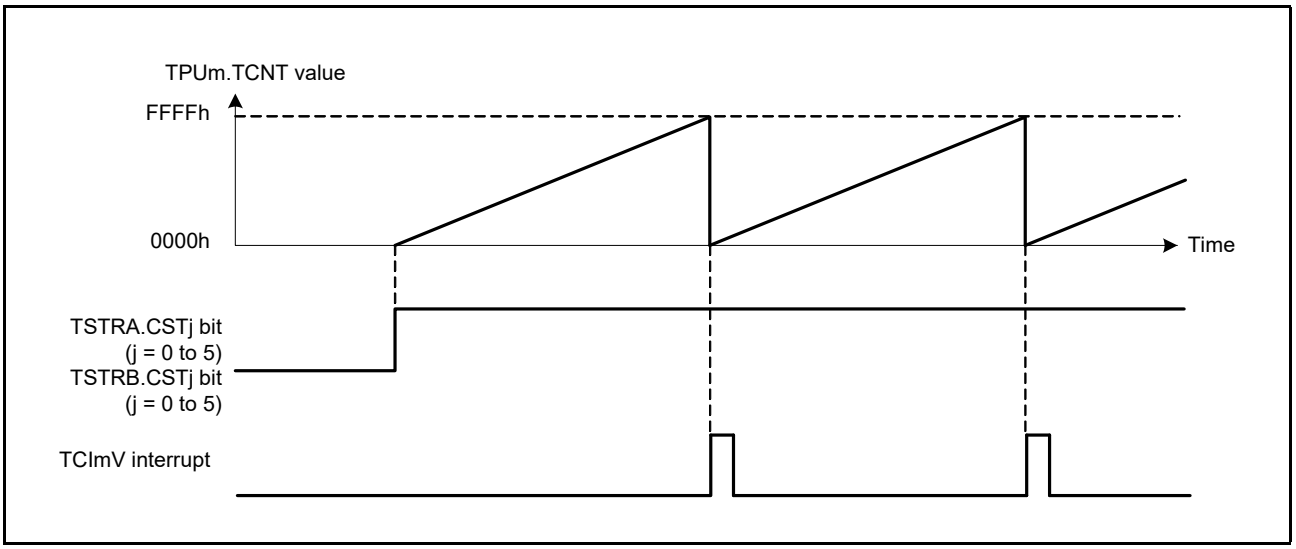


Figure 22.5 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TPUm.TGRy register for setting the period is set as an output compare register, and counter clearing by compare match is selected by the TPUm.TCR.CCLR[2:0] bits. After the settings have been made, TCNT starts count-up operation as a periodic counter when the corresponding bit in TSTRA and TSTRB is set to 1. When the count value matches the TGRy value, TCNT is cleared to 0000h.
At this time, the TPU requests an interrupt (TGImy). After a compare match, TCNT restarts counting up from 0000h (m = 0 to 11).
Figure 22.6 shows periodic counter operation.

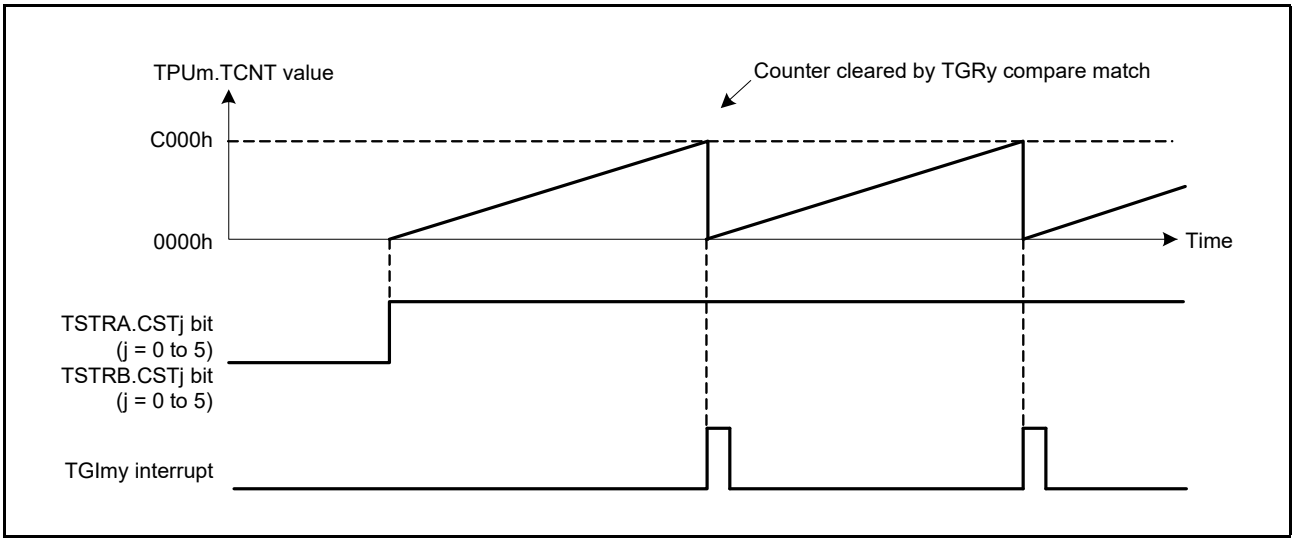


Figure 22.6 Periodic Counter Operation

(2) Waveform Output by Compare Match

The TPU can perform low, high, or toggle output from the corresponding output pin using a compare match.

(a) Example of setting procedure for waveform output by compare match

Figure 22.7 shows an example of the setting procedure for waveform output by a compare match.

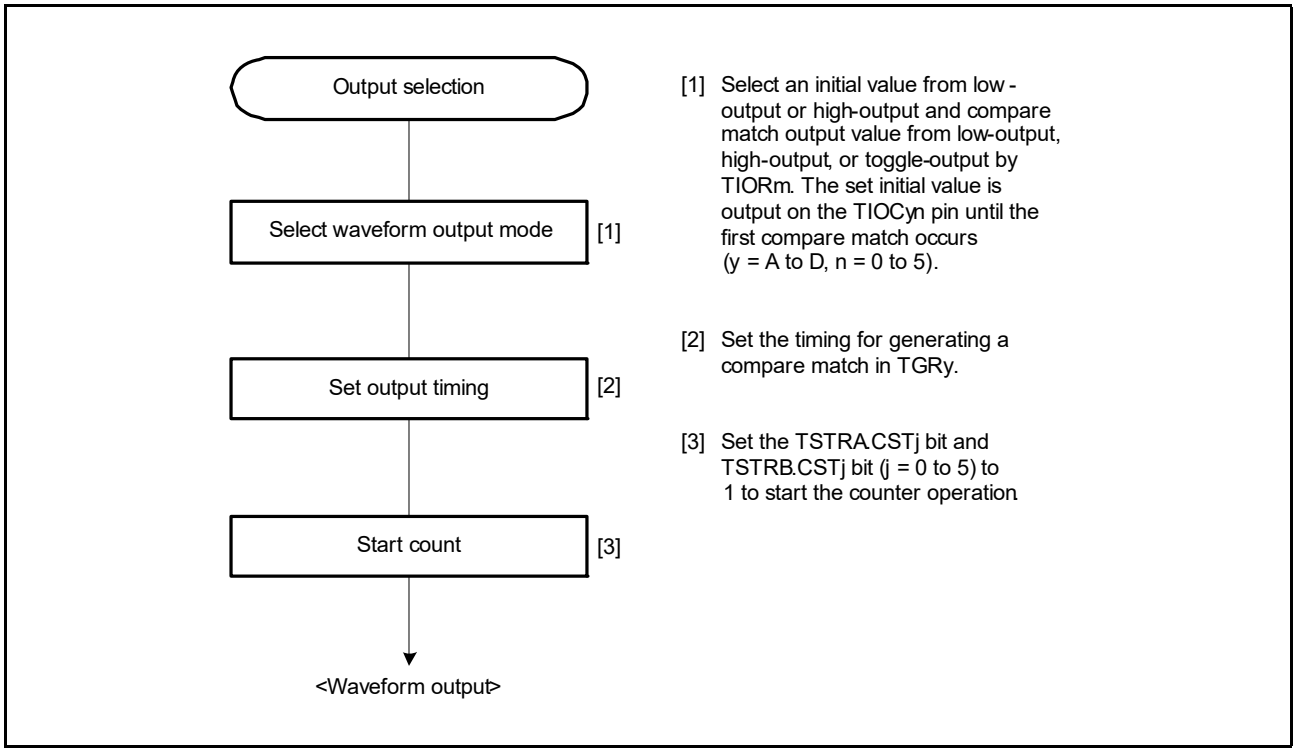


Figure 22.7 Example of Setting Procedure for Waveform Output by Compare Match

(b) Examples of waveform output operation

Figure 22.8 shows an example of low output/high output.

In this example, TPUm.TCNT (m = 0 to 11) has been set as a free-running counter, and settings have been made so that high is output by compare match A and low is output by compare match B. When the set level and the pin level match, the pin level does not change.

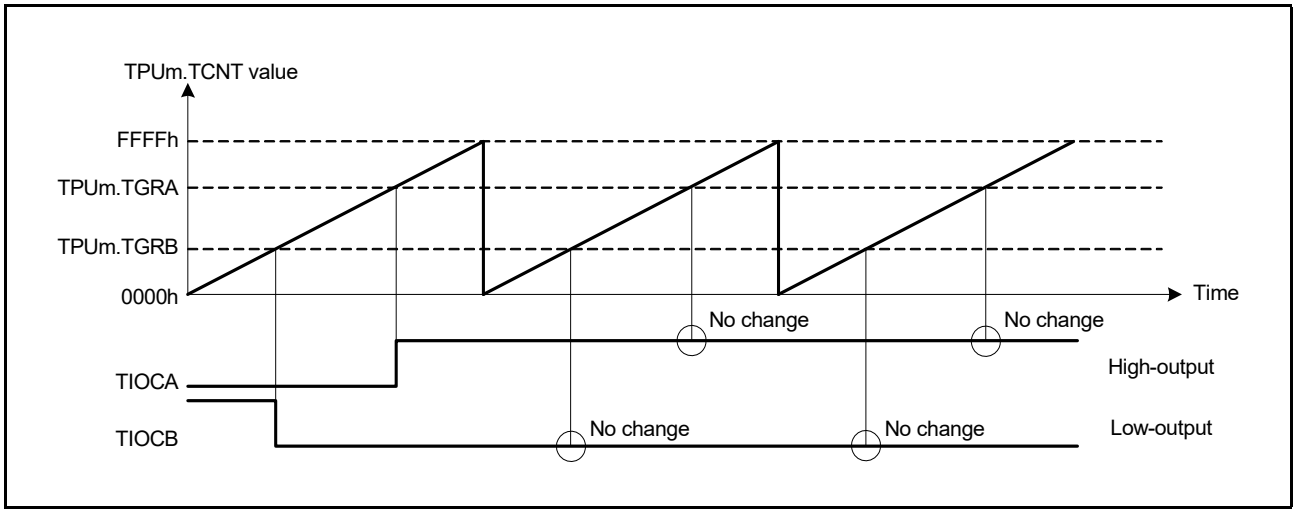


Figure 22.8 Example of Low-Output/High-Output Operation

Figure 22.9 shows an example of toggle output.
In this example, TPUm.TCNT (m = 0 to 11) has been set as a periodic counter (with counter clearing performed by compare match B), and settings have been made so that output is toggled by both compare match A and compare match B.

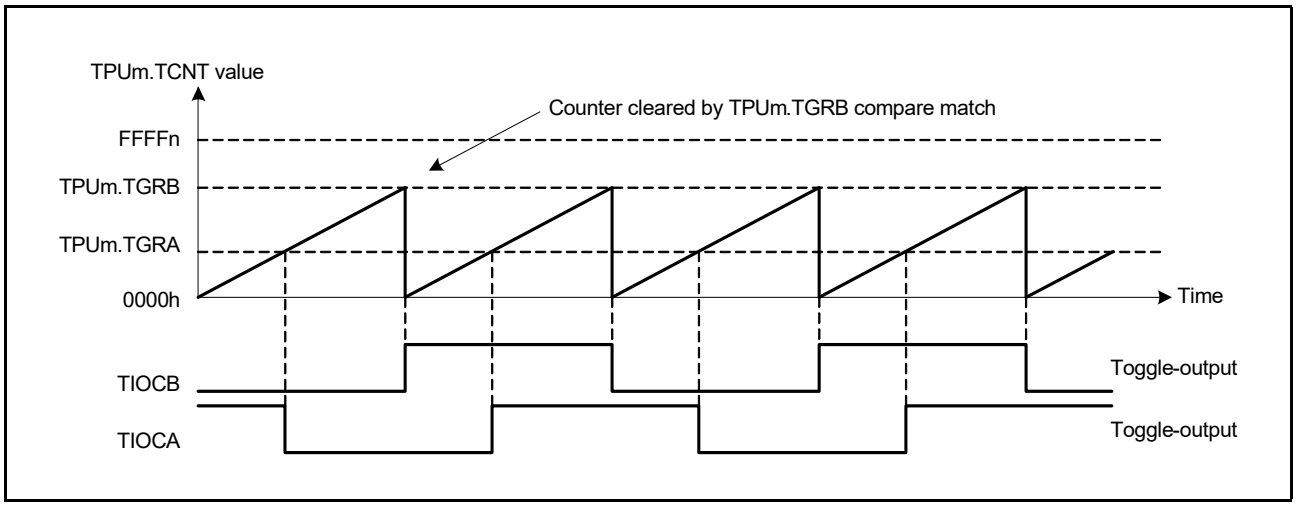


Figure 22.9 Example of Toggle Output Operation

(3) Input Capture Function

The TCNT value can be transferred to TGRy on detection of the TIOCyn pin (n = 0 to 11 when y = A, B; n = 0, 3, 6, 9 when y = C, D) input edge.

The rising edge, the falling edge, or both edges can be selected as the detection edge. It is also possible to specify the counter input clock or compare match signal of TPU0, TPU1, TPU3, and TPU4 in unit 0 and of TPU6, TPU7, TPU9, and TPU10 in unit 1 as the input capture source. Noise filtering can be applied to the input capture input.

Note: Even if the counter is halted, an input capture is generated, and flag and interrupt signals are generated.

Note: When another channel's counter input clock is used as the input capture input for TPU0, TPU3, TPU6, and TPU9, PCLKD/1 should not be selected as the counter input clock used for input capture input. Input capture will not be generated if PCLKD/1 is selected.

(a) Example of setting procedure for input capture operation

Figure 22.10 shows an example of the setting procedure for input capture operation.

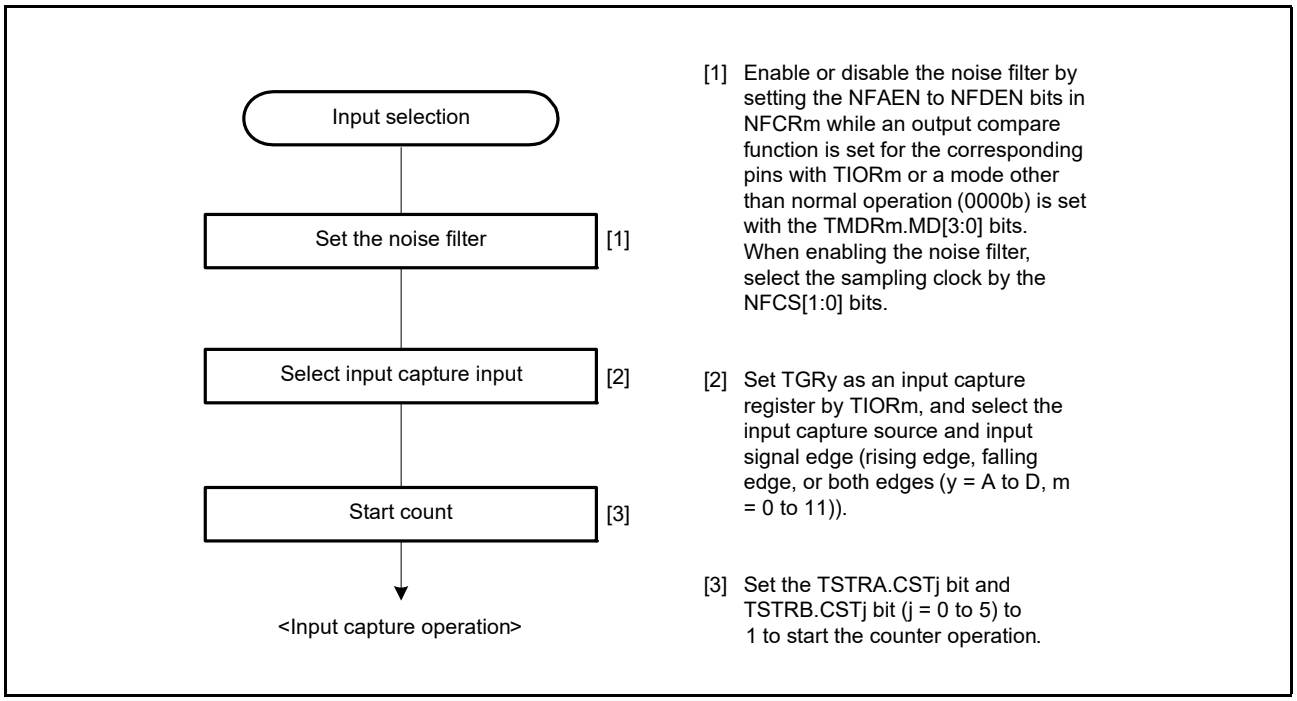


Figure 22.10 Example of Setting Procedure for Input Capture Operation

(b) Example of input capture operation

Figure 22.11 shows an example of input capture operation when the noise filter is stopped.
In this example, both rising and falling edges have been selected as the TIOCAm pin input capture input edge, the falling edge has been selected as the TIOCBm pin input capture input edge, and counter clearing by TGRB input capture has been set for TCNT (m = 0 to 11).

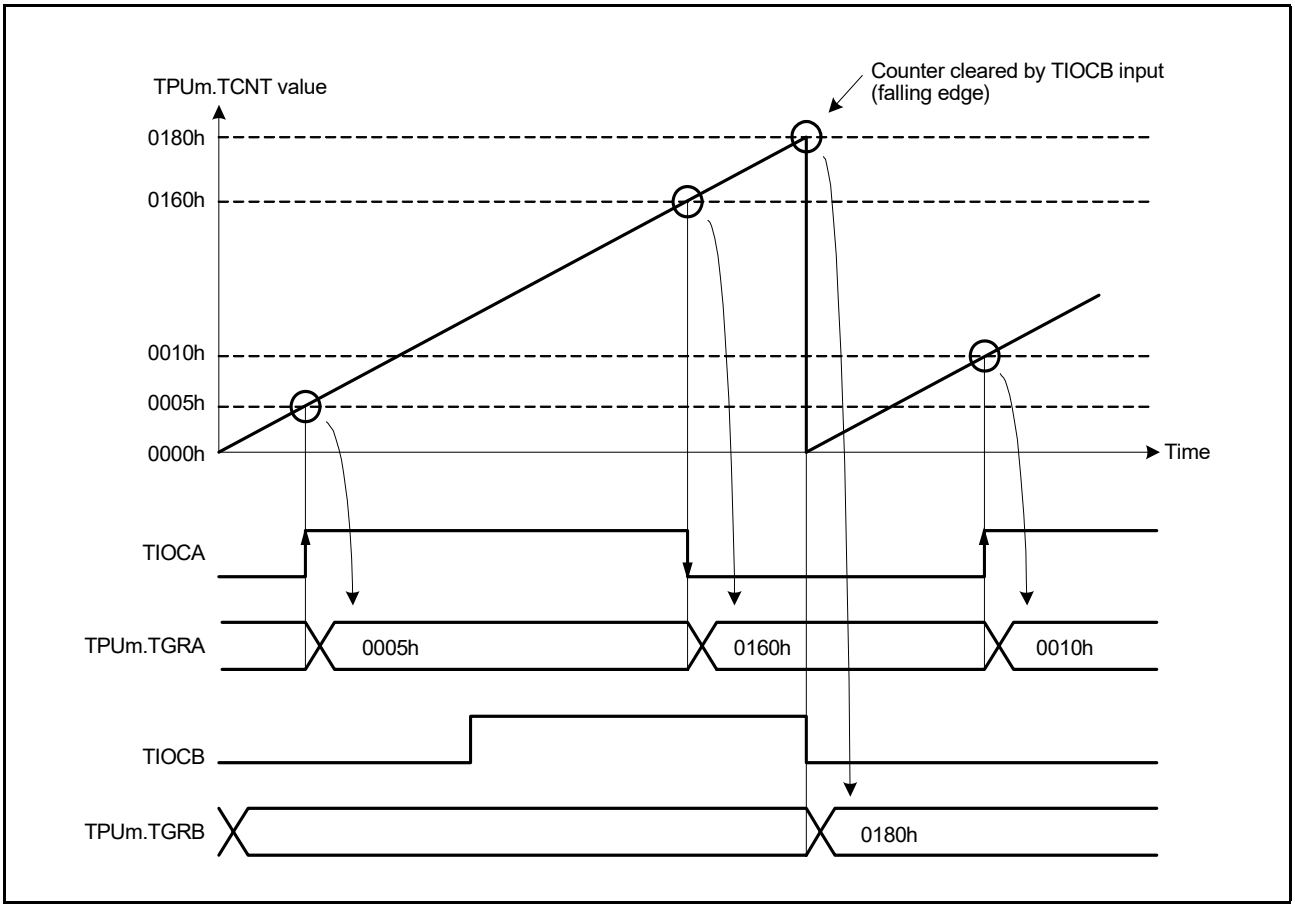


Figure 22.11 Example of Input Capture Operation (with Noise Filter Stopped)

When noise filtering is enabled, see Figure 22.32.

22.3.2 Synchronous Operation

In synchronous operation, the values in multiple TCNT counters in a unit can be rewritten simultaneously (synchronous presetting). Also, multiple TCNT counters can be cleared simultaneously (synchronous clearing) by making the appropriate setting in TCR.
Synchronous operation enables TGRy to be incremented with respect to a single time base.
All channels of TPU0 to TPU5 in unit 0 or of TPU6 to TPU11 in unit 1 can be set for synchronous operation.

(1) Example of Synchronous Operation Setting Procedure

Figure 22.12 shows an example of the synchronous operation setting procedure.

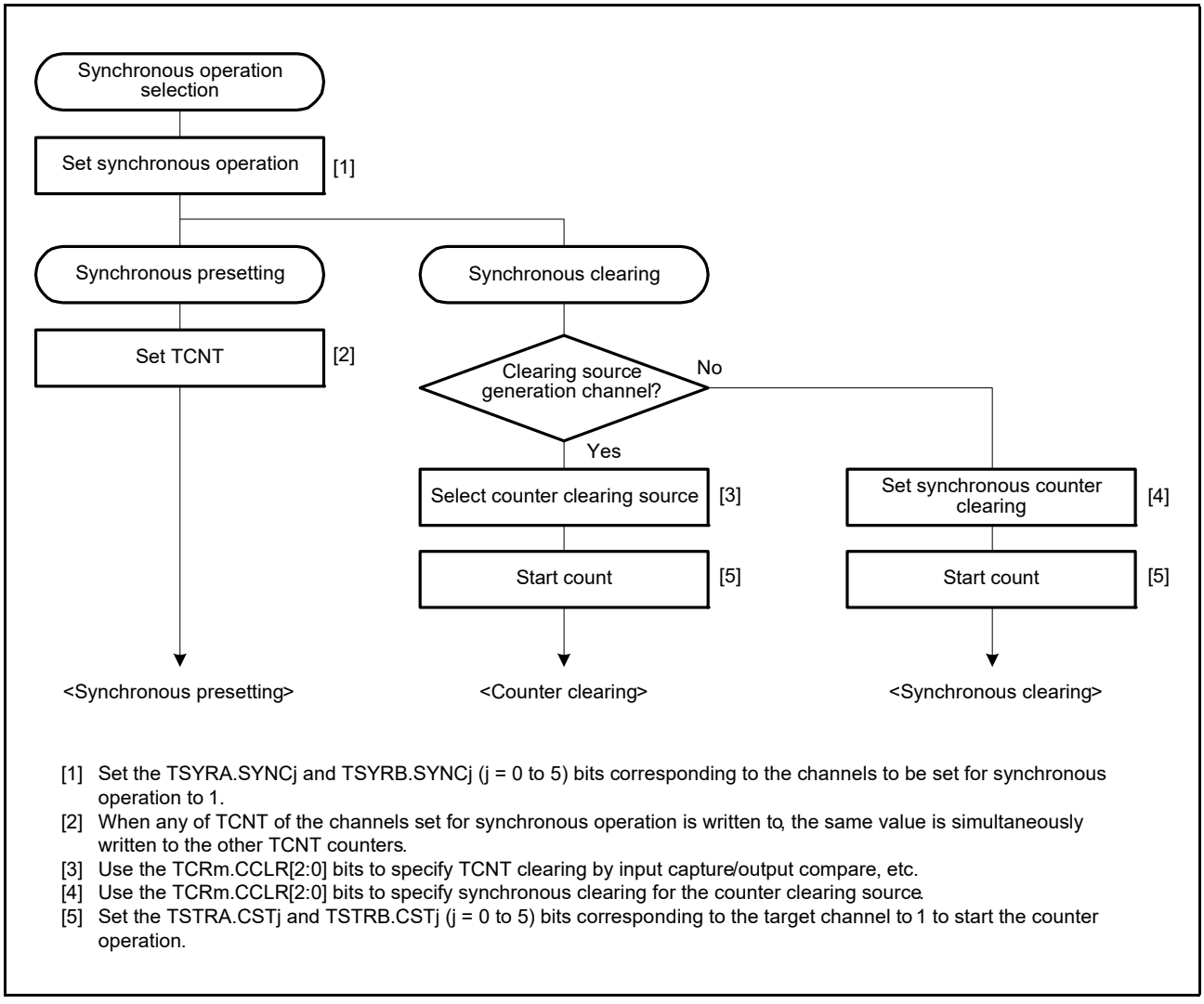


Figure 22.12 Example of Synchronous Operation Setting Procedure

(2) Example of Synchronous Operation

Figure 22.13 shows an example of synchronous operation.
In this example, synchronous operation and PWM mode 1 have been set for TPU0 to TPU2, TPU0.TGRB compare match has been set as the TPU0 counter clearing source, and synchronous clearing has been set for the TPU1 and TPU2 counter clearing source.
Three-phase PWM waveforms are output from pins TIOCA0, TIOCA1, and TIOCA2. At this time, synchronous presetting and synchronous clearing by TPU0.TGRB compare match are performed for TCNT of TPU0 to TPU2, and the data set in TPU0.TGRB is used as the PWM cycle.
For details on PWM modes, see section 22.3.5, PWM Modes.

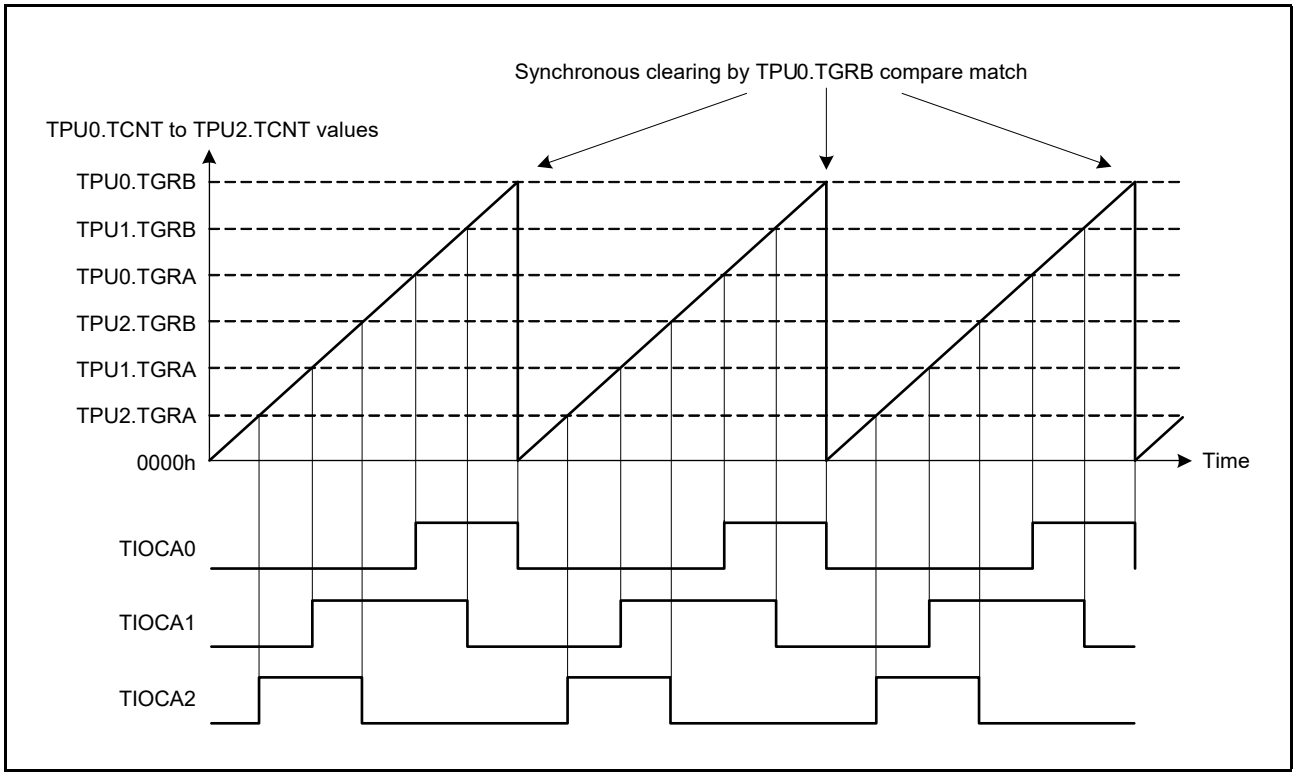


Figure 22.13 Example of Synchronous Operation

22.3.3 Buffer Operation

Buffer operation, provided for TPU0, TPU3, TPU6, and TPU9, enables TPUm.TGRC and TPUm.TGRD to be used as buffer registers.

Buffer operation differs depending on whether TPUm.TGRy has been set as an input capture register or a compare match register.

Table 22.23 lists the register combinations used in buffer operation.

Table 22.23 Register Combinations in Buffer Operation

Unit	Channel	Timer General Register	Buffer Register
0	TPU0	TPU0.TGRA	TPU0.TGRC
		TPU0.TGRB	TPU0.TGRD
	TPU3	TPU3.TGRA	TPU3.TGRC
		TPU3.TGRB	TPU3.TGRD
1	TPU6	TPU6.TGRA	TPU6.TGRC
		TPU6.TGRB	TPU6.TGRD
	TPU9	TPU9.TGRA	TPU9.TGRC
		TPU9.TGRB	TPU9.TGRD

- When TPUm.TGRy is an output compare register

When a compare match occurs, the value in the buffer register for the corresponding channel is transferred to the timer general register.

This operation is shown in Figure 22.14.

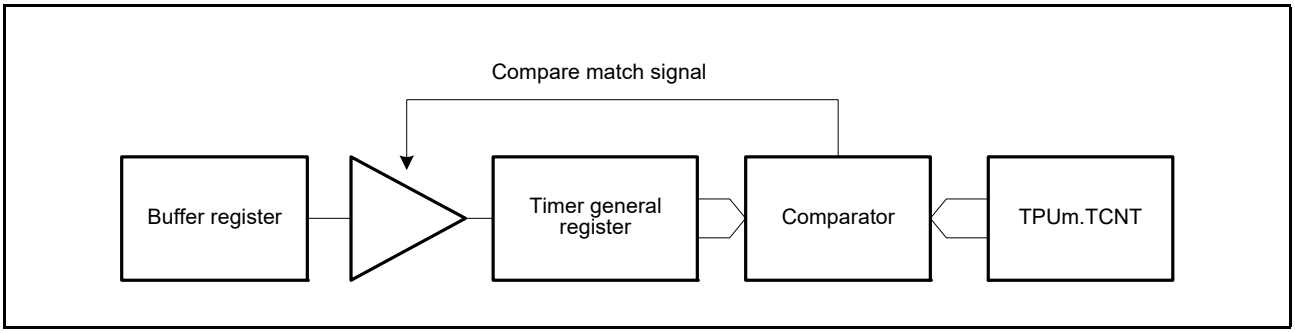


Figure 22.14 Compare Match Buffer Operation

- When TPUm.TGRy is an input capture register

When input capture occurs, the value in TPUm.TCNT is transferred to TGRy and the value previously held in TGRy is simultaneously transferred to the buffer register.

This operation is shown in Figure 22.15.

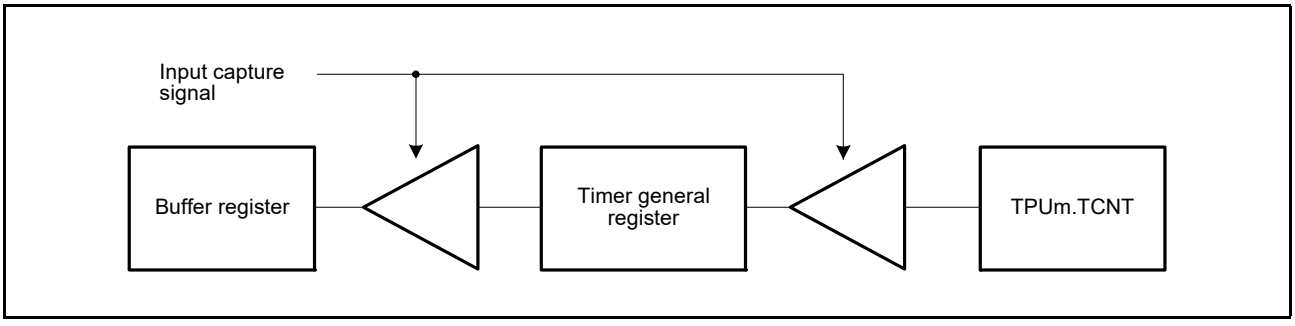


Figure 22.15 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 22.16 shows an example of the buffer operation setting procedure.

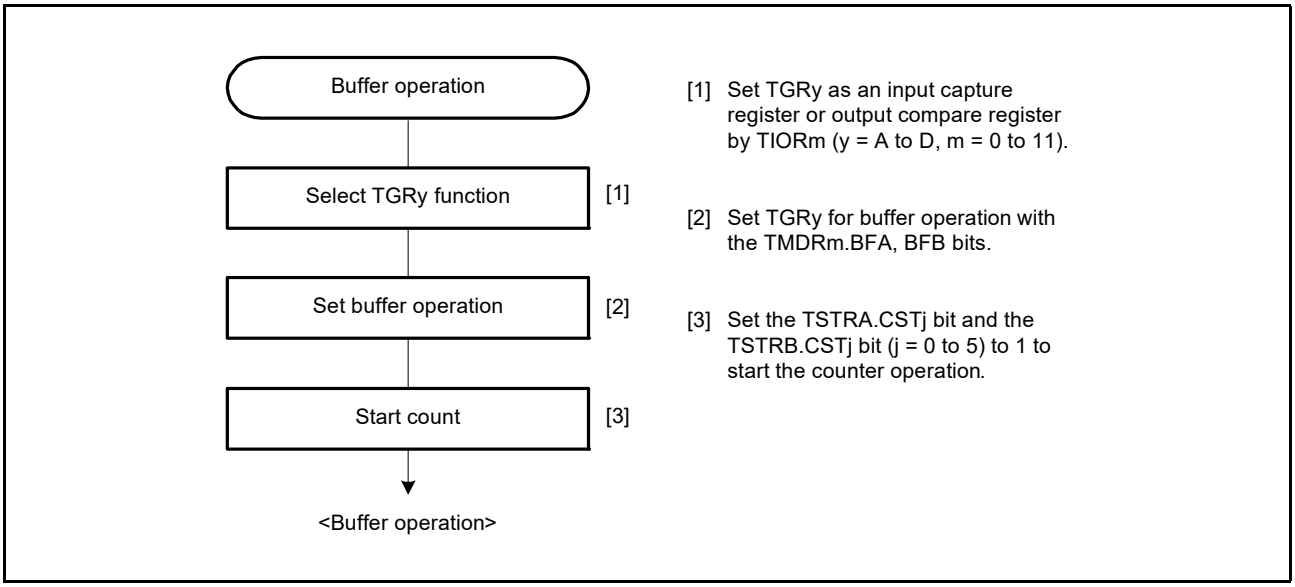


Figure 22.16 Example of Buffer Operation Setting Procedure

(2) Examples of Buffer Operation

(a) When TPUm.TGRy is an output compare register

Figure 22.17 shows an operation example in which PWM mode 1 has been set for TPU0, and buffer operation has been set for TPU0.TGRA and TPU0.TGRC. The settings used in this example are TPU0.TCNT clearing by compare match B, high output at compare match A, and low output at compare match B.
As buffer operation has been set, when compare match A occurs, the output changes and the TPU0.TGRC value is simultaneously transferred to TPU0.TGRA. This operation is repeated each time compare match A occurs.
For details on PWM modes, see section 22.3.5, PWM Modes.

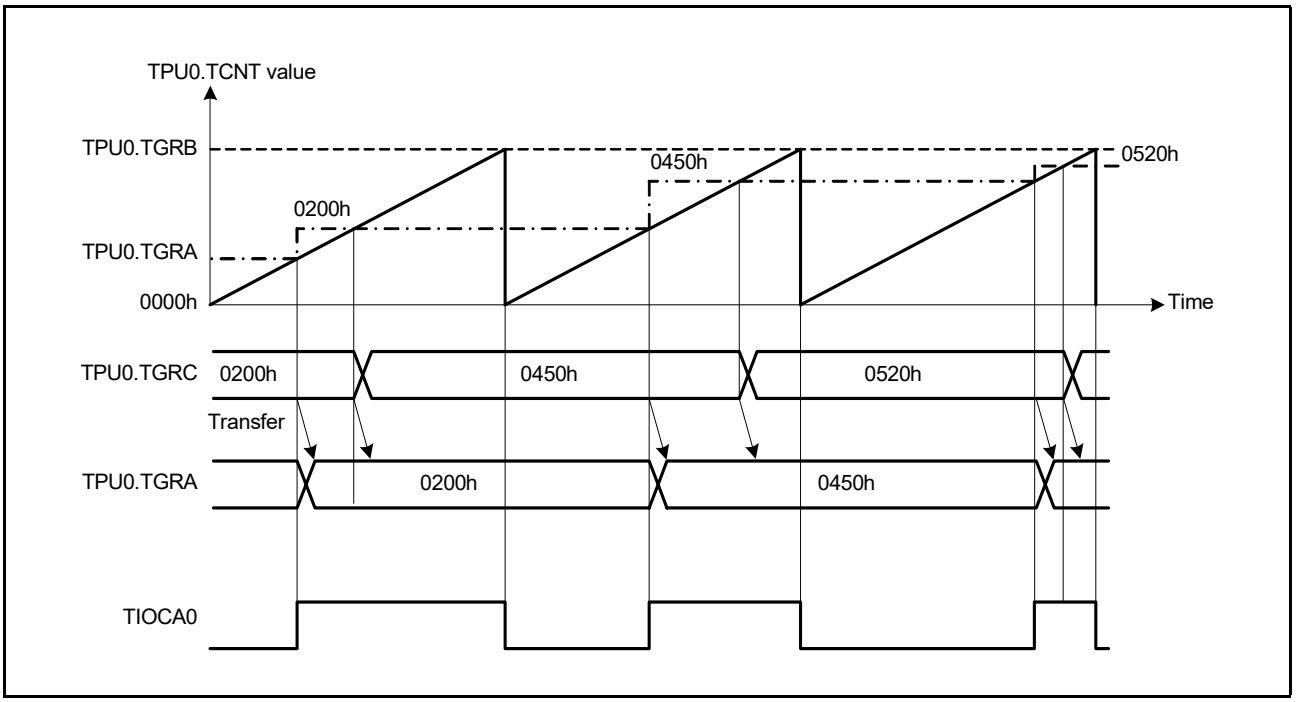


Figure 22.17 Example of Buffer Operation (1)

(b) When TPUm.TGRy is an input capture register

Figure 22.18 shows an operation example in which TPUm.TGRA has been set as an input capture register, and buffer operation has been set for TGRA and TPUm.TGRC.
Counter clearing by TGRA input capture has been set for TPUm.TCNT, and both rising and falling edges have been selected as the TIOCAn pin input capture input edge.
As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC (m = 0 to 11).

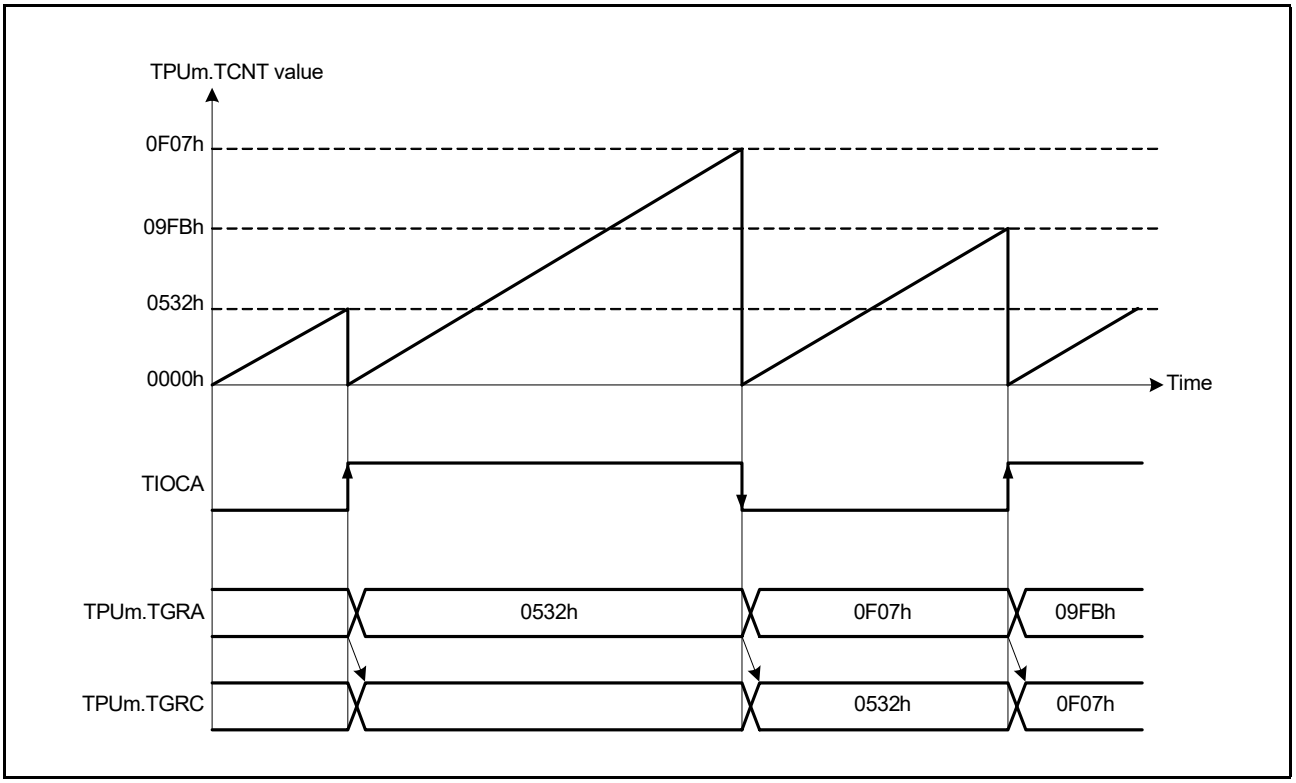


Figure 22.18 Example of Buffer Operation (2)

22.3.4 Cascaded Operation

In cascaded operation, two 16-bit counters for different channels are used together as a 32-bit counter.

In unit 0, this function works by counting the TPUm (m = 1, 4) counter clock at overflow/underflow of TPUn.TCNT (n = 2, 5) as set by the TPUm.TCR.TPSC[2:0] bits (m = 1, 4).

Underflow occurs only when the lower 16-bit TPUn.TCNT is in phase counting mode.

Table 22.24 lists the register combinations used in cascaded operation.

Note 1. When phase counting mode is set for TPU1 or TPU4, the counter clock setting is invalid and the counter operates independently in phase counting mode (this also applies to TPU7 and TPU10).

Note 2. For input capture operation with a cascade connection, be sure to see section 22.9.16, Input Capture Operation in Cascaded Operation.

Note 3. For operation in 32-bit phase counting mode, set the lower-order 16 bits of TPUn to phase counting mode and the higher-order 16 bits of TPUm to normal operating mode.

Table 22.24 Cascaded Combinations

Unit	Combination	Upper 16 Bits	Lower 16 Bits
0	TPU1 and TPU2	TPU1.TCNT	TPU2.TCNT
	TPU4 and TPU5	TPU4.TCNT	TPU5.TCNT
1	TPU7 and TPU8	TPU7.TCNT	TPU8.TCNT
	TPU10 and TPU11	TPU10.TCNT	TPU11.TCNT

(1) Example of Cascaded Operation Setting Procedure

Figure 22.19 shows an example of the setting procedure for cascaded operation.

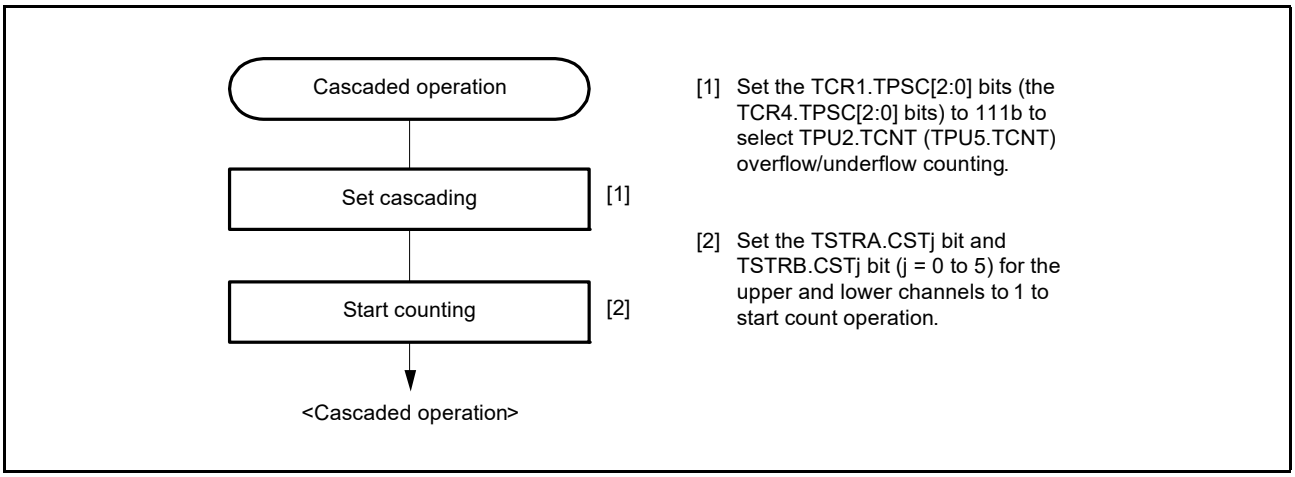


Figure 22.19 Cascaded Operation Setting Procedure

(2) Examples of Cascaded Operation

Figure 22.20 shows the operation when counting upon TPU2.TCNT overflow/underflow has been set for TPU1.TCNT, TPU1.TGRA and TPU2.TGRA have been set as input capture registers, and the rising edge of the TIOCA1 and TIOCA2 pins has been selected.

When a rising edge is simultaneously input to the TIOCA1 and TIOCA2 pins, the 16 higher-order bits and the 16 lower-order bits of the 32-bit value are transferred to the TPU1.TGRA and TPU2.TGRA registers, respectively.

However, even if the rising edge is input to the TIOCA1 and TIOCA2 pins simultaneously, the 16 higher- and 16 lower-order bits may not be captured simultaneously due to delays within the LSI chip, so a value may vary from that at the time. If this is the case, discard the captured value by following the procedure described in section 22.9.16, Input Capture Operation in Cascaded Operation.

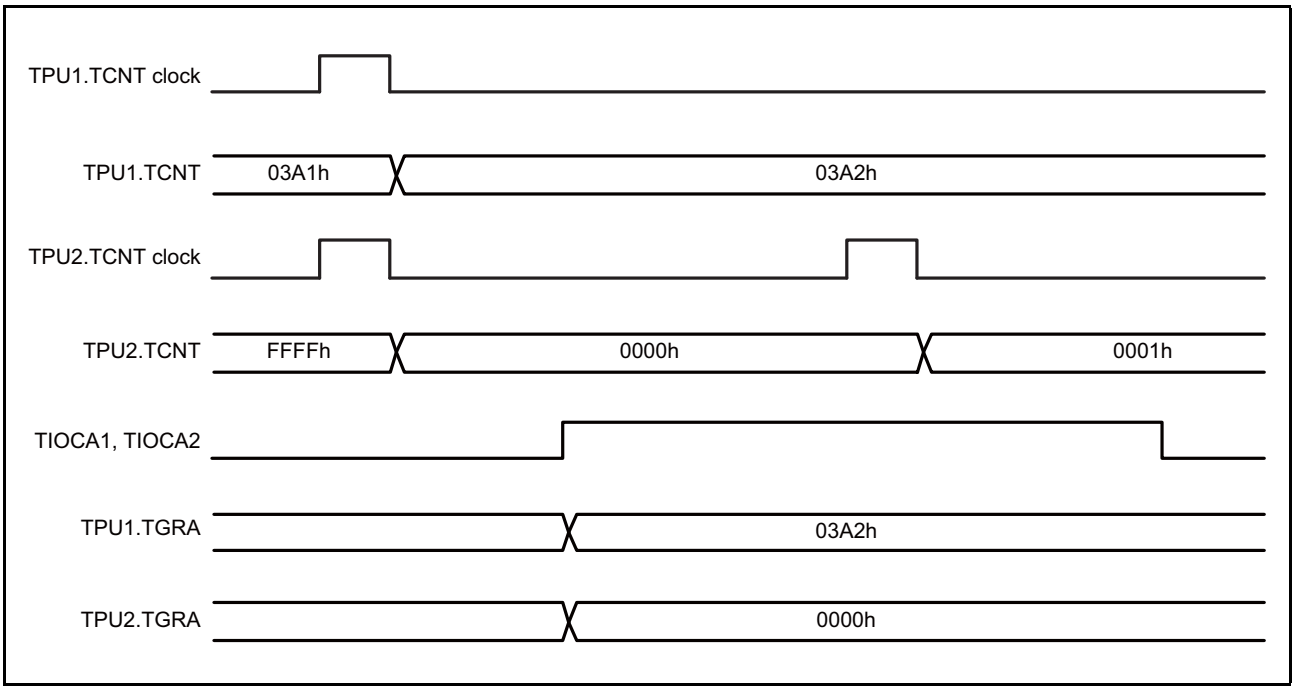


Figure 22.20 Example of Cascaded Operation (1)

Figure 22.21 shows the operation when counting upon TPU2.TCNT overflow/underflow has been set for TPU1.TCNT, and phase counting mode has been specified for TPU2.

TPU1.TCNT is incremented by TPU2.TCNT overflow and decremented by TPU2.TCNT underflow.

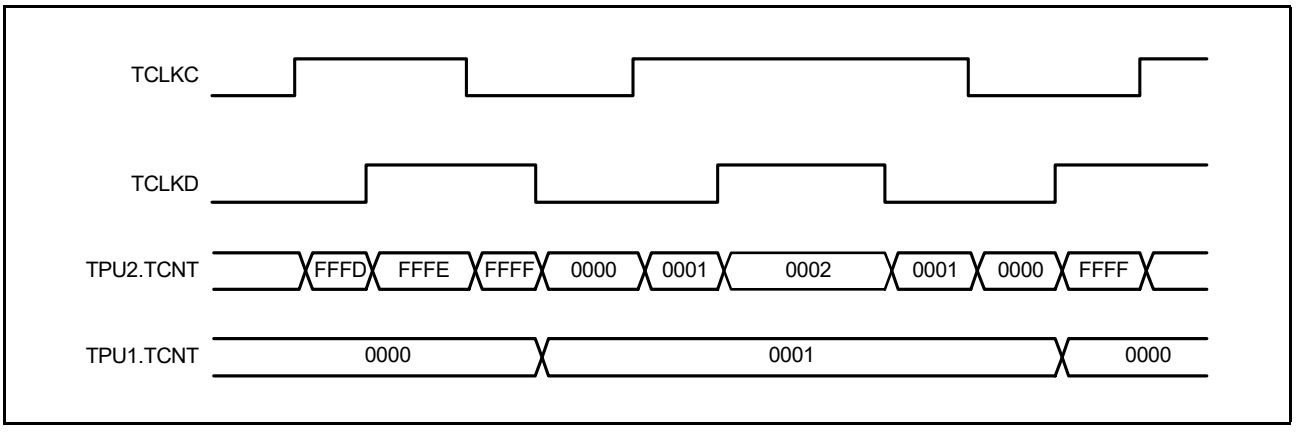


Figure 22.21 Example of Cascaded Operation (2)

22.3.5 PWM Modes

In PWM mode, PWM waveforms are output from the output pins. low-, high-, or toggle-output can be selected as the output level in response to compare match of each TGRy.
Settings of TGRy registers can output a PWM waveform in the range of 0% to 100% duty cycle.
Specifying TGRy compare match as the counter clearing source enables the cycle to be set in that register. All channels can be set for PWM mode independently. Synchronous operation is also possible.
There are two PWM modes, as described below.

1. PWM mode 1
   PWM waveform is generated from the TIOCAn and TIOCCn pins by pairing TPUm.TGRA with TPUm.TGRB and TPUm.TGRC with TPUm.TGRD. The levels specified by the TPUm.TIOR(H).IOA[3:0] bits and TPUm.TIORL.IOC[3:0] bits are output from the TIOCAn and TIOCCn pins at compare matches A and C, respectively. The levels specified by theTPUm.TIOR(H).IOB[3:0] bits and TPUm.TIORL.IOD[3:0] bits are output from the TIOCAn and TIOCCn pins at compare matches B and D, respectively. The initial output value of the TIOCAn or TIOCCn pin is the value set in the TIOR.IOA or TIORL.IOC bit. If the set values of paired TGRy registers are identical, the output value does not change even when a compare match occurs.
   In PWM mode 1, up to eight phases of PWM waveforms can be output.
2. PWM mode 2
   PWM waveform is generated by using one TPUm.TGRy as the cycle register and the others as duty cycle registers. The level specified in TPUm.TIORH, TPUm.TIORL, or TPUm.TIOR is output at compare matches. Upon counter clearing by a cycle register compare match, the output value of each pin is the initial value set in TIORH, TIORL, or TIOR. If the set values of the cycle register and duty cycle register are identical, the output value does not change even when a compare match occurs.
   In PWM mode 2, up to 15 phases (× 2 units) of PWM waveforms can be output when using synchronous operation in combination.

(m = 0 to 11 when y = A, B; m = 0, 3, 6, 9 when y = C, D)

The correspondence between PWM output pins and registers is listed in Table 22.25.

Table 22.25 PWM Output Registers and Output Pins

		Output Pin	
Channel	**Register**	**PWM Mode 1**	**PWM Mode 2**
TPU0	TPU0.TGRA	TIOCA0	TIOCA0
	TPU0.TGRB		TIOCB0
	TPU0.TGRC	TIOCC0	TIOCC0
	TPU0.TGRD		TIOCD0
TPU1	TPU1.TGRA	TIOCA1	TIOCA1
	TPU1.TGRB		TIOCB1
TPU2	TPU2.TGRA	TIOCA2	TIOCA2
	TPU2.TGRB		TIOCB2
TPU3	TPU3.TGRA	TIOCA3	TIOCA3
	TPU3.TGRB		TIOCB3
	TPU3.TGRC	TIOCC3	TIOCC3
	TPU3.TGRD		TIOCD3
TPU4	TPU4.TGRA	TIOCA4	TIOCA4
	TPU4.TGRB		TIOCB4
TPU5	TPU5.TGRA	TIOCA5	TIOCA5
	TPU5.TGRB		TIOCB5
TPU6	TPU6.TGRA	TIOCA6	TIOCA6
	TPU6.TGRB		TIOCB6
	TPU6.TGRC	TIOCC6	TIOCC6
	TPU6.TGRD		TIOCD6
TPU7	TPU7.TGRA	TIOCA7	TIOCA7
	TPU7.TGRB		TIOCB7
TPU8	TPU8.TGRA	TIOCA8	TIOCA8
	TPU8.TGRB		TIOCB8
TPU9	TPU9.TGRA	TIOCA9	TIOCA9
	TPU9.TGRB		TIOCB9
	TPU9.TGRC	TIOCC9	TIOCC9
	TPU9.TGRD		TIOCD9
TPU10	TPU10.TGRA	TIOCA10	TIOCA10
	TPU10.TGRB		TIOCB10
TPU11	TPU11.TGRA	TIOCA11	TIOCA11
	TPU11.TGRB		TIOCB11

Note: In PWM mode 2, PWM waveform output is not possible for the TPUm.TGRy register in which the cycle is set.

(1) Example of PWM Mode Setting Procedure

Figure 22.22 shows an example of the PWM mode setting procedure.

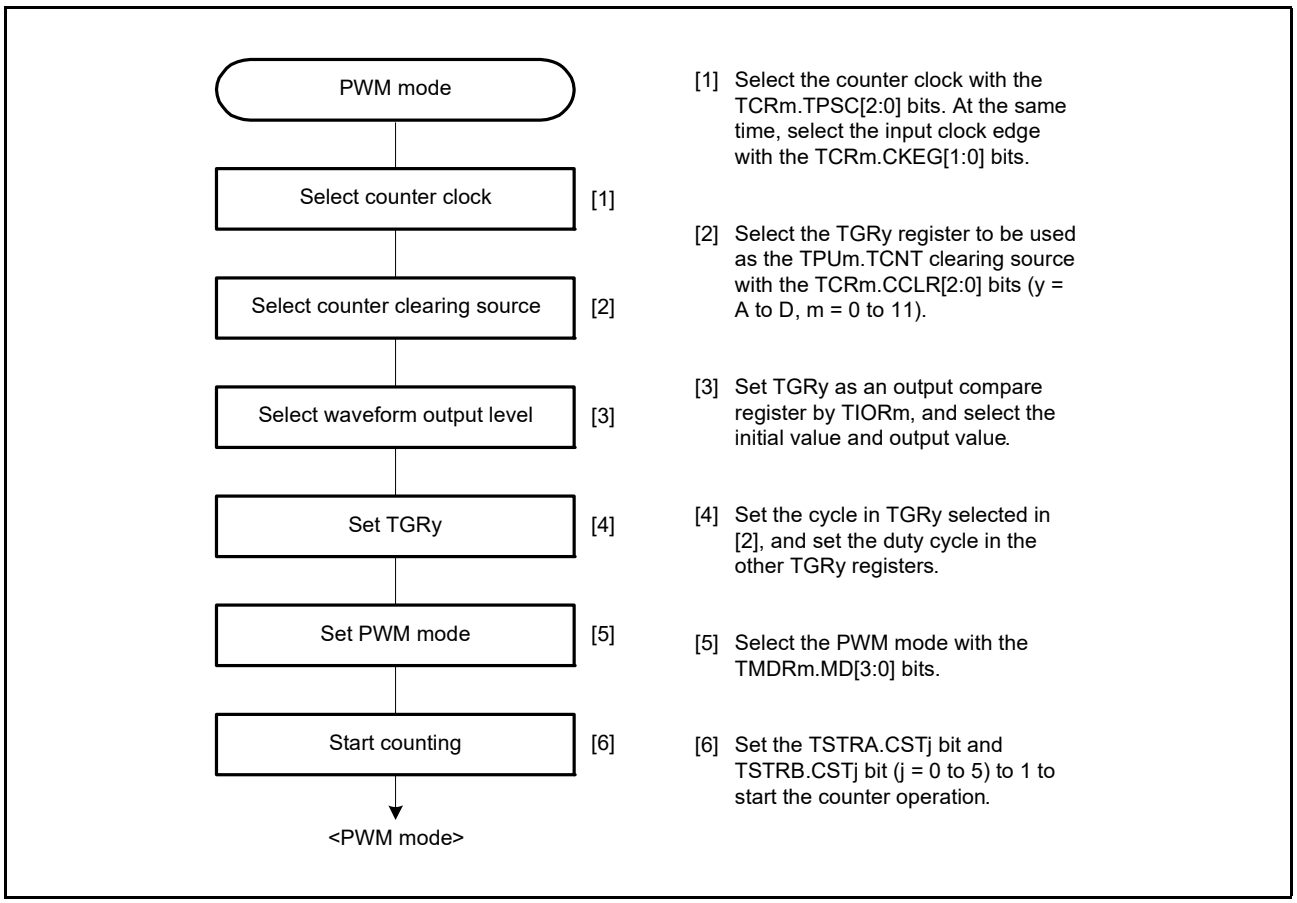


Figure 22.22 Example of PWM Mode Setting Procedure

(2) Examples of PWM Mode Operation

Figure 22.23 shows an example of PWM mode 1 operation.

In this example, TPUm.TGRA compare match is set as the TPUm.TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TPUm.TGRB output value (m = 0 to 11).

In this case, the value set in TGRA is used as the cycle, and the value set in TGRB is used as the duty cycle.

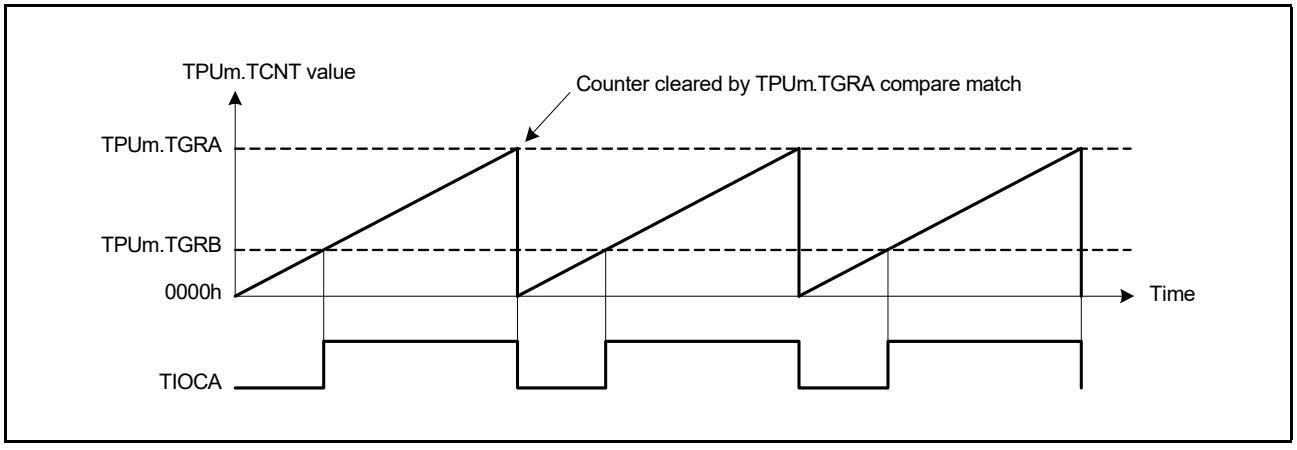


Figure 22.23 Example of PWM Mode Operation (1)

Figure 22.24 shows an example of PWM mode 2 operation.
In this example, synchronous operation is specified for TPU0 and TPU1, TPU1.TGRB compare match is set as TPUm.TCNT (m = 0, 1) clearing source, and 0 is set for the initial output value and 1 for the output value of the other TGRy registers (TPU0.TGRA to TPU0.TGRD and TPU1.TGRA), to output a 5-phase PWM waveform.
In this case, the value set in TPU1.TGRB is used as the cycle, and the values set in the other TGRy registers are used as the duty cycle.

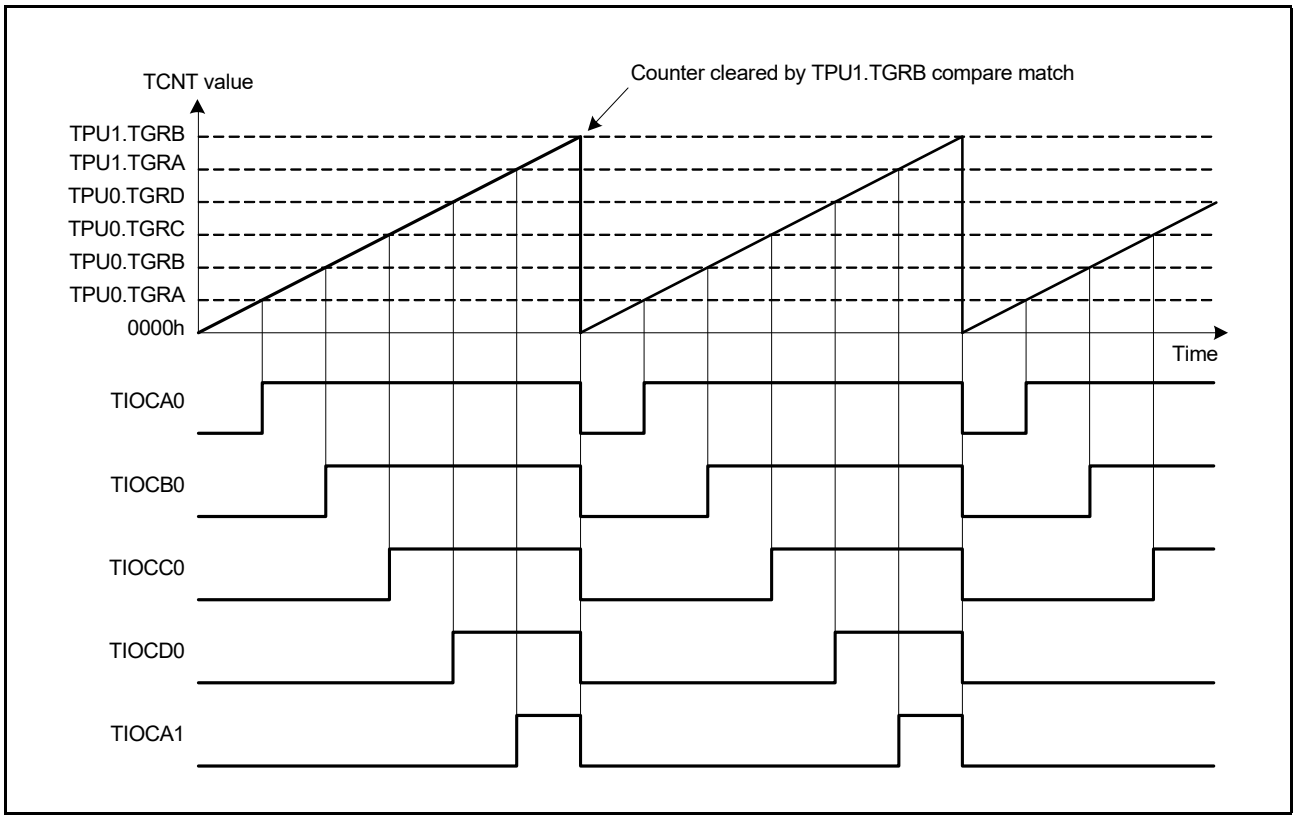


Figure 22.24 Example of PWM Mode Operation (2)

Figure 22.25 shows examples of PWM waveform output with 0% duty cycle and 100% duty cycle in PWM mode.

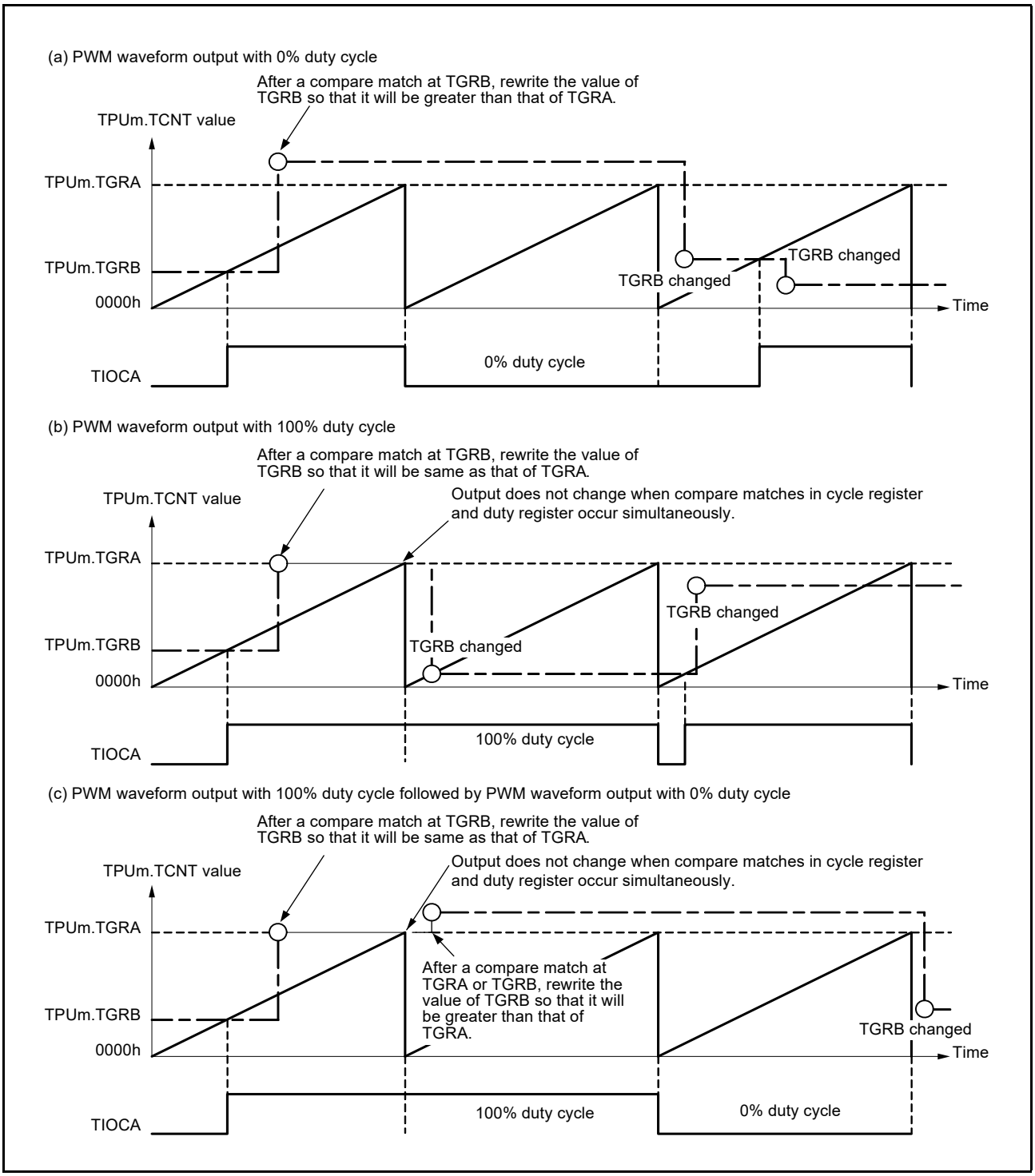


Figure 22.25 Example of PWM Mode Operation (3)

22.3.6 Phase Counting Mode

In phase counting mode, the phase difference between two external clock inputs is detected by the settings for channels 1, 2, 4, and 5 in unit 0 and for channels 7, 8, 10, and 11 in unit 1, and TPUm.TCNT is incremented/decremented accordingly (m = 1, 2, 4, 5, 7, 8, 10, 11).

When phase counting mode is set, an external clock is selected as the counter input clock and TCNT operates as an up-/down-counter regardless of the setting of the TPUm.TCR.TPSC[2:0] and CKEG[1:0] bits. However, the lower 2 bits of the TPUm.TCR.CCLR[2:0] bits and the functions of TPUm.TIORH, TPUm.TIORL, TPUm.TIOR, TPUm.TIER, and TPUm.TGRy are valid, and therefore input capture/compare match and interrupt functions are available.

This can be used for two-phase encoder pulse input.

When an overflow occurs while TCNT is counting up, a TCIV interrupt request is generated; when an underflow occurs while TCNT is counting down, a TCIU interrupt request is generated. The TPUm.TSR.TCFD flag is the count direction flag. Reading the TCFD flag provides an indication of whether TCNT is counting up or down.

Table 22.26 lists the correspondence between external clock pins and channels.

Table 22.26 Clock Input Pins in Phase Counting Mode

		External Clock Pins	
Unit	**Channel**	**A-Phase**	**B-Phase**
0	When TPU1 or TPU5 is set to phase counting mode	TCLKA	TCLKB
	When TPU2 or TPU4 is set to phase counting mode	TCLKC	TCLKD
1	When TPU7 or TPU11 is set to phase counting mode	TCLKE	TCLKF
	When TPU8 or TPU10 is set to phase counting mode	TCLKG	TCLKH

(1) Example of Phase Counting Mode Setting Procedure

Figure 22.26 shows an example of the phase counting mode setting procedure.

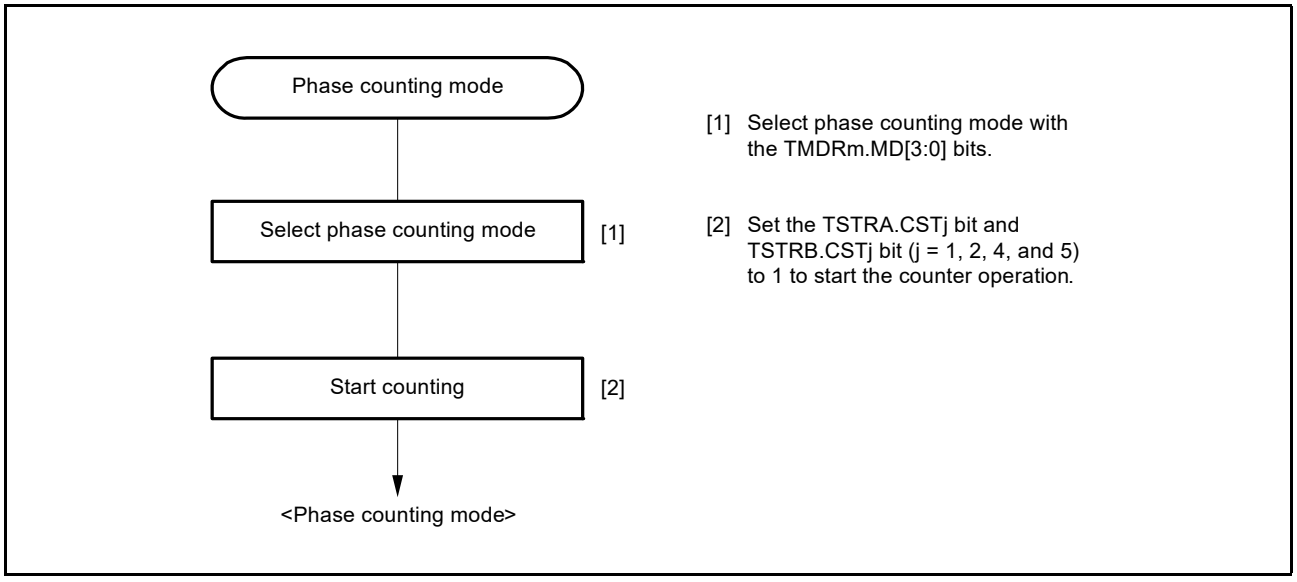


Figure 22.26 Example of Phase Counting Mode Setting Procedure

(2) Examples of Phase Counting Mode Operation

In phase counting mode, TPUm.TCNT (m = 1, 2, 4, 5, 7, 8, 10, 11) counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

(a) Phase counting mode 1

Figure 22.27 shows an example of phase counting mode 1 operation for unit 0, and Table 22.27 lists the TPUm.TCNT up-/down-count conditions (m = 1, 2, 4, 5).

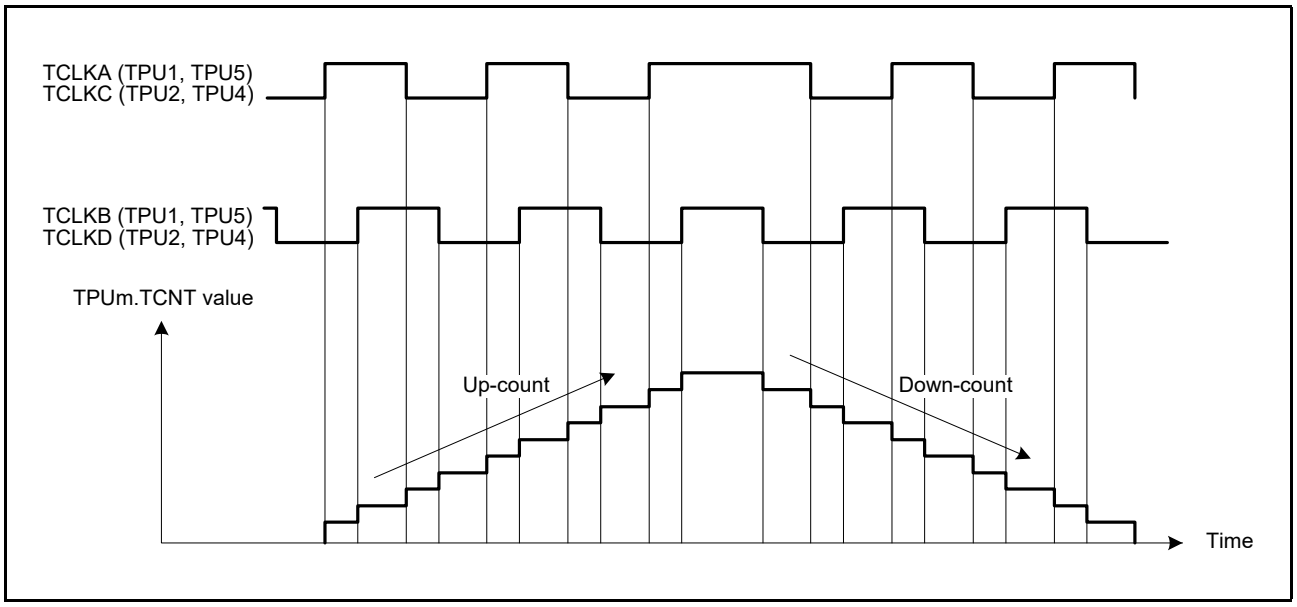


Figure 22.27 Example of Phase Counting Mode 1 Operation

Table 22.27 Up-/Down-Count Conditions in Phase Counting Mode 1

TCLKA (TPU1, TPU5) TCLKC (TPU2, TPU4)	TCLKB (TPU1, TPU5) TCLKD (TPU2, TPU4)	Operation
High	↑	Up-count
Low	↓	
↑	Low	
↓	High	
High	↓	Down-count
Low	↑	
↑	High	
↓	Low	

↑ : Rising edge

↓ : Falling edge

(b) Phase counting mode 2

Figure 22.28 shows an example of phase counting mode 2 operation for unit 0, and Table 22.28 lists the TPUm.TCNT up-/down-count conditions (m = 1, 2, 4, 5).

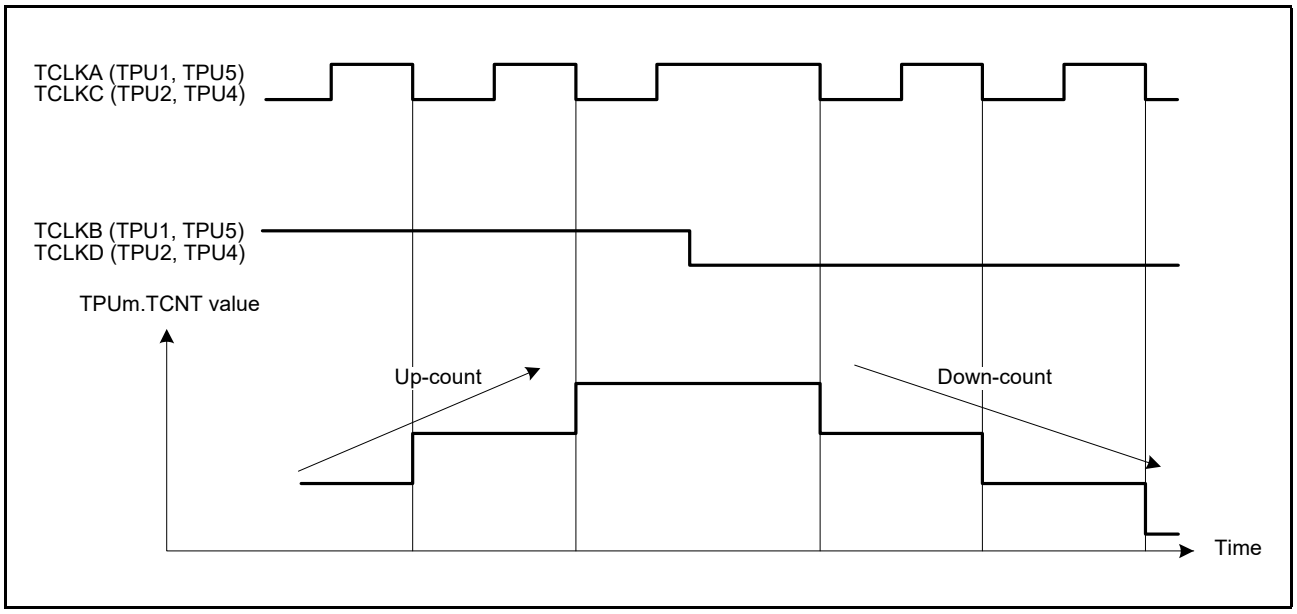


Figure 22.28 Example of Phase Counting Mode 2 Operation

Table 22.28 Up-/Down-Count Conditions in Phase Counting Mode 2

TCLKA (TPU1, TPU5) TCLKC (TPU2, TPU4)	TCLKB (TPU1, TPU5) TCLKD (TPU2, TPU4)	Operation
High	↑	Don't care
Low	↓	Don't care
↑	Low	Don't care
↓	High	Up-count
High	↓	Don't care
Low	↑	Don't care
↑	High	Don't care
↓	Low	Down-count

↑ : Rising edge

↓ : Falling edge

(c) Phase counting mode 3

Figure 22.29 shows an example of phase counting mode 3 operation for unit 0, and Table 22.29 lists the TPUm.TCNT up-/down-count conditions (m = 1, 2, 4, 5).

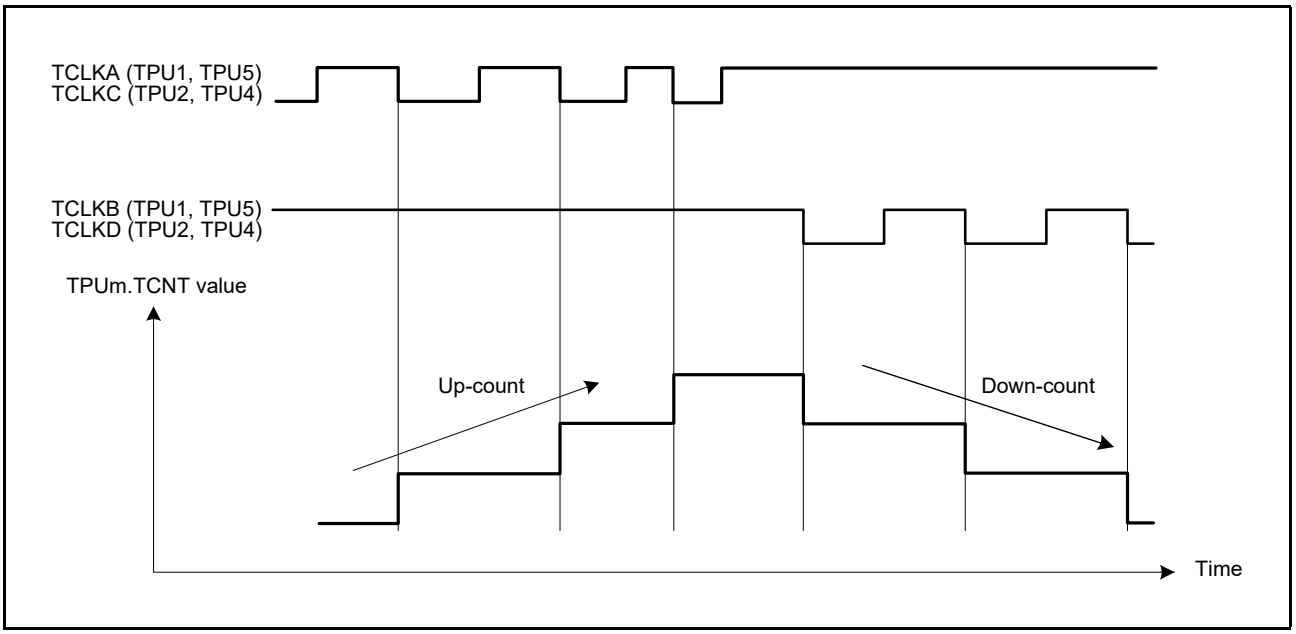


Figure 22.29 Example of Phase Counting Mode 3 Operation

Table 22.29 Up-/Down-Count Conditions in Phase Counting Mode 3

TCLKA (TPU1, TPU5) TCLKC (TPU2, TPU4)	TCLKB (TPU1, TPU5) TCLKD (TPU2, TPU4)	Operation
High	↑	Don't care
Low	↓	Don't care
↑	Low	Don't care
↓	High	Up-count
High	↓	Down-count
Low	↑	Don't care
↑	High	Don't care
↓	Low	Don't care

↑ : Rising edge

↓ : Falling edge

(d) Phase counting mode 4

Figure 22.30 shows an example of phase counting mode 4 operation for unit 0, and Table 22.30 lists the TPUm.TCNT up-/down-count conditions (m = 1, 2, 4, 5).

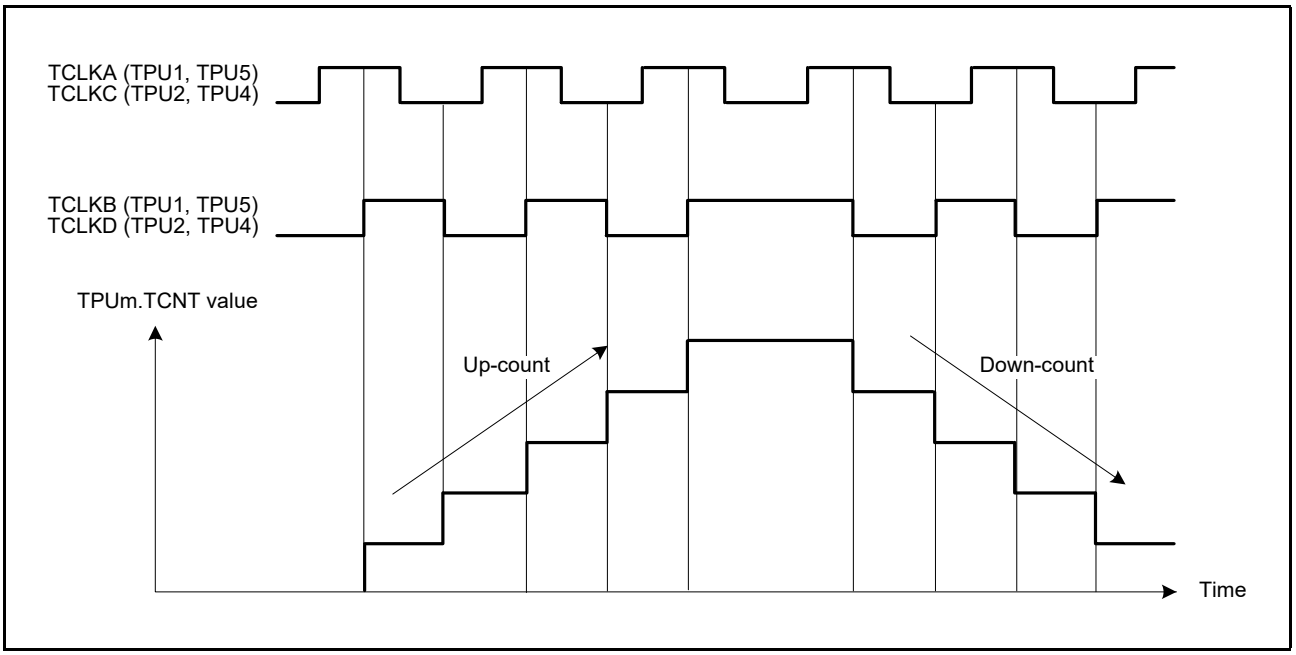


Figure 22.30 Example of Phase Counting Mode 4 Operation

Table 22.30 Up-/Down-Count Conditions in Phase Counting Mode 4

TCLKA (TPU1, TPU5) TCLKC (TPU2, TPU4)	TCLKB (TPU1, TPU5) TCLKD (TPU2, TPU4)	Operation
High	↑	Up-count
Low	↓	
↑	Low	Don't care
↓	High	
High	↓	Down-count
Low	↑	
↑	High	Don't care
↓	Low	

↑ : Rising edge

↓ : Falling edge

22.3.6.1 Phase Counting Mode Application Example

Figure 22.31 shows an example in which phase counting mode is set for TPU1, and TPU1 is coupled with TPU0 to input servo motor 2-phase encoder pulses in order to detect the position or speed.
In this example, TPU1 is set to phase counting mode 1, and the encoder pulse A-phase and B-phase are input to the TCLKA and TCLKB pins.
TPU0 operates with TPU0.TCNT counter clearing by TPU0.TGR compare match; TPU0.TGRA and TPU0.TGRC are used for the compare match function and are set with the speed control cycle and position control cycle. TPU0.TGRB is used for input capture, with TPU0.TGRB and TPU0.TGRD operating in buffer mode. The TPU1 counter input clock is specified as the source to drive input capture in TPU0.TGRB. The TPU0 counter values are input to and captured by TPU0.TGRB in response to counting up or down by the TPU1.TCNT counter (with the previously captured value being transferred to TPU0.TGRD), allowing measurement of edge occurrence (pulse width measurement).
TPU1.TGRA and TPU1.TGRB for TPU1 are specified for input capture, TPU0.TGRA and TPU0.TGRC compare matches are selected as the input capture source, and the up-/down-counter values for the control cycles are stored.
This procedure enables accurate position/speed detection to be achieved.

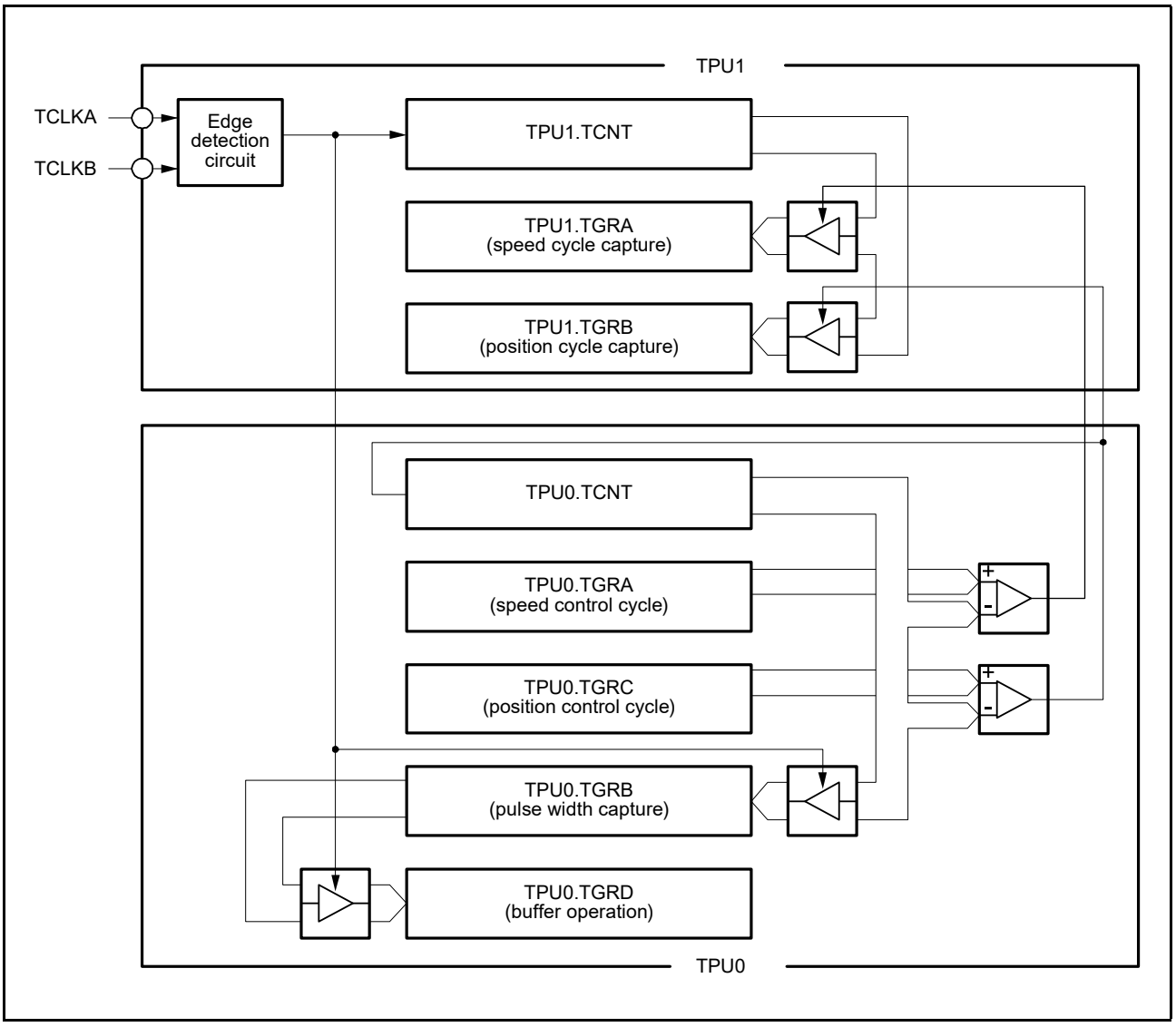


Figure 22.31 Phase Counting Mode Application Example

22.3.7 Noise Filters

Each pin for use in input capture by TPU is equipped with a noise filter. The noise filter samples input signals at the frequency of the sampling clock and pulses with levels that only match once or twice are removed.
The noise filter functionality includes enabling and disabling of the noise filter for each pin and setting of the sampling clock for each channel.
Figure 22.32 is a timing chart for the noise filter.

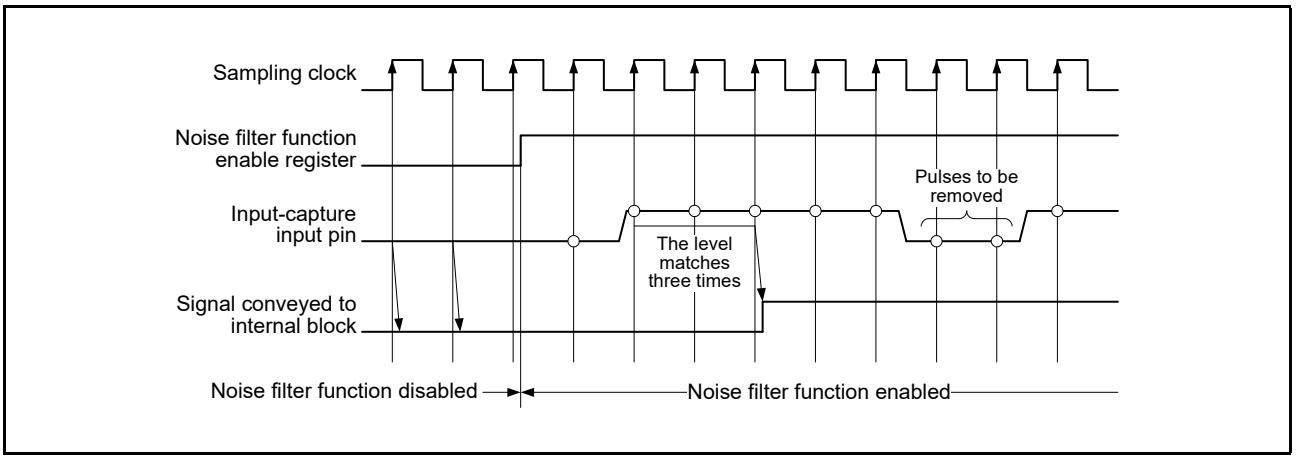


Figure 22.32 Timing Chart for the Noise Filter

If noise filtering is set, input capture operation is performed on the edges of noise-filtered signal after a minimum delay of (sampling interval × 2 + PCLKD) due to noise filtering for the input capture input.

22.3.8 Internal PWM Feedback Input Select

The internal PWM feedback input select function uses pin out signals of MTU3a and GPTa selected with PWMFBSLR.FBSLn (n = 0, 1) as the TPU input capture input through the inside of this LSI.
As an example usage, assume that pin out signals of MTU3a and GPTa that are set as the PWM output are selected as the internal PWM feedback input, and the duty cycle and cycle of the PWM waveform are measured with the input captured value.
Section 22.3.8.1 and section 22.3.8.2 describe example settings of PWM waveform measurement with the internal PWM feedback input select function. section 22.3.8.3 and section 22.3.8.4 describe example settings for measurement of the external PWM waveform input to the TIOCAm and TIOCBm pins with the normal input capture function.

22.3.8.1 Example Setting of PWM 1-Axis Measurement (TPU (Unit 0) is Set as the Internal PWM Feedback Input)

MTU3 and MTU4 are selected as the sources of PWM internal feedback input to a TPU (unit 0), and PWM waveforms can be measured through the internal circuits of the LSI chip.
In this example, TPU0 starts operation in synchronization with the carrier cycles of MTU3 or MTU4, while the latter are used for 6-phase PWM output.
An example of settings so that PWM waveforms are measured from the counter values input and captured at the times of the detection of edges in the PWM outputs is given below.
For details about the module connection in this setting, see Figure 22.33.

Prerequisite: In the PWM timer (MTU3, MTU4) used as the internal PWM feedback input source, one cycle is defined as trough-to-trough. PWM is operating with active-low setting.

(1) Stop the count operation of all channels of the TPU (unit 0). Set TGRA and TGRB of each channel for output compare (input capture disable).
(2) Set the digital noise filter for each input capture pin of the TPU (unit 0).
(3) Set the count clock, clear conditions, and operating mode for each channel of the TPU (unit 0).
Count clock: PCLKD/1
Clear conditions: Counter clear at the timing of TGRA input capture
Operating mode: Normal mode
(4) Clear the counter value of all channels of the TPU (unit 0) to 0000h.
(5) Set TGRA and TGRB for each channel of TPU (unit 0) for input capture operation.
TGRA: Rising edge detection (Falling edge detection for a reverse phase channel)
TGRB: Falling edge detection (Rising edge detection for a reverse phase channel)
(6) Set the PWMFBSLR register as follows:
TPU0EN bit: 1b (Internal PWM feedback enable)
FBSL0 bit: 100b (PWM output signals of MTU3 and MTU4)
(7) Enable interrupts by the TGRA input capture of each channel of TPU (unit 0).
(8) Counting on each channel of the TPU (unit 0) is started, triggered by the timing of the trough of the carrier of MTU3 and MTU4.
(9) An interrupt is generated due to input capture at the rising edge of PWM. The active period can be calculated with the count values at the falling edge and at the rising edge.

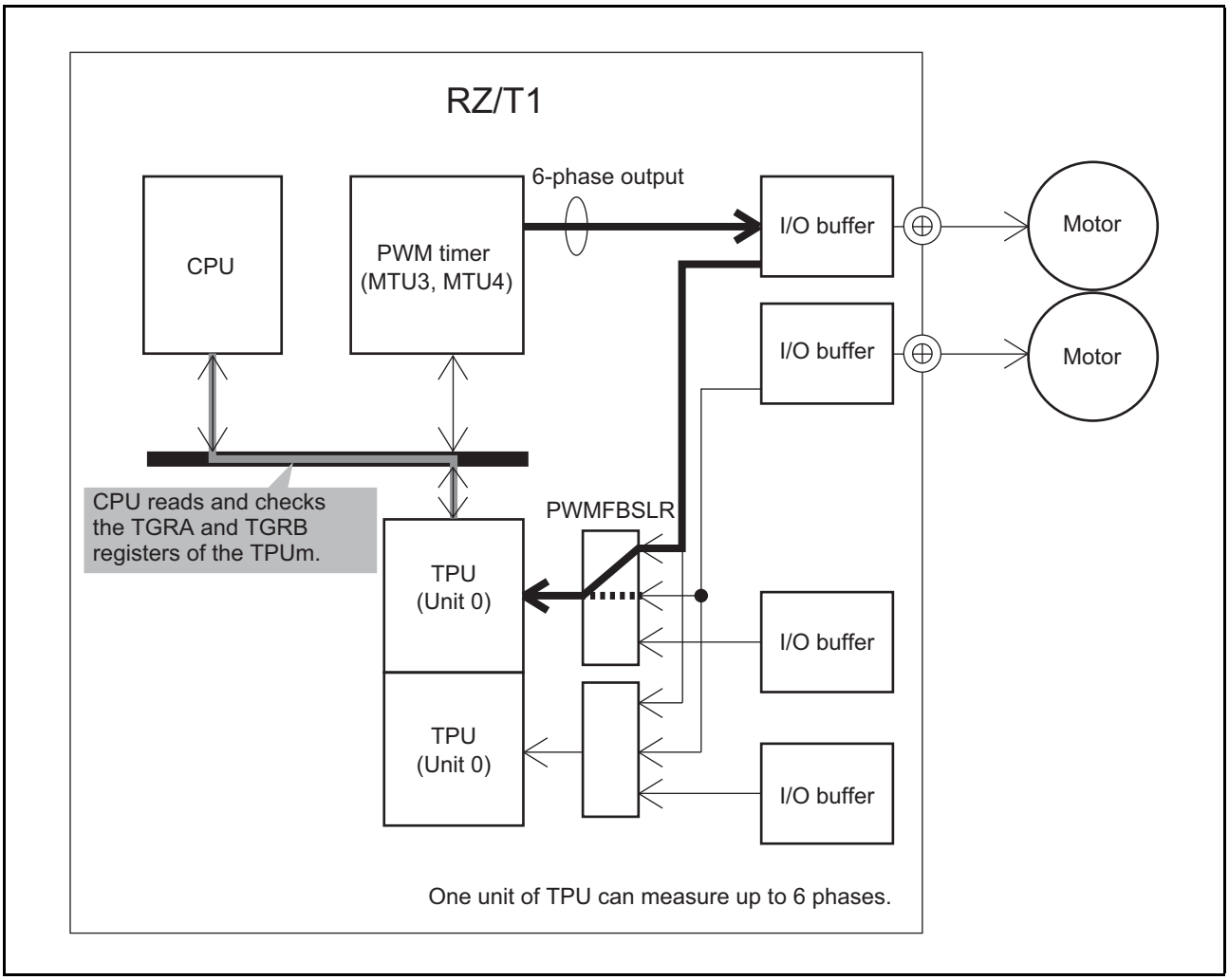


Figure 22.33 Connection Diagram of Example Setting for PWM 1-Axis Measurement

22.3.8.2 Example Setting of PWM 2-Axes Measurement (TPU (Unit 0) is Set as the Internal PWM Feedback Input)

MTU3 and MTU4, and MTU6 and MTU7, are selected by switching between them as the sources of PWM internal feedback input to a TPU (unit 0), and PWM waveforms from two axes can be measured through the internal circuits of the LSI chip.
In this example, TPU0 starts operating in synchronization with the carrier cycles of MTU3 and MTU4 or MTU6 and MTU7, while either pair is used for 6-phase PWM output.
An example of settings so that the PWM waveforms are obtained from the counter values input and captured at the times of the detection of edges in the PWM outputs is given below.
For details about connection of this module, TPU, and PWM timer, see Figure 22.34.

Prerequisite: In the PWM timer (MTU3 and MTU4, and MTU6 and MTU7) used as the internal PWM feedback input source, one cycle is defined as trough-to-trough. PWW is operating with active-low setting.

(1) Stop the count operation of all channels of the TPU (unit 0). Set TGRA and TGRB of each channel for output compare (input capture disable).
(2) Set the digital noise filter for each input capture pin of the TPU (unit 0).
(3) Set the count clock, clear conditions, and operating mode for each channel of the TPU (unit 0).
Count clock: PCLKD/1
Clear conditions: Counter clear at the timing of TGRA input capture
Operating mode: Normal mode
(4) Clear the counter value of all channels of the TPU (unit 0) to 0000h.
(5) Set TGRA and TGRB for each channel of the TPU (unit 0) for input capture operation.
TGRA: Rising edge detection (Falling edge detection for a reverse phase channel)
TGRB: Falling edge detection (Rising edge detection for a reverse phase channel)
(6) Set the PWMFBSLR register as follows:
TPU0EN bit: 1b (Internal PWM feedback enable)
FBSL0 bit: 100b (PWM output signals of MTU3 and MTU4)
(7) Enable interrupts by the TGRA input capture for each channel of the TPU (unit 0).
(8) Counting on each channel of the TPU (unit 0) is started, triggered by the timing of the trough of the carrier of MTU3 and MTU4.
(9) An interrupt is generated due to input capture at the rising edge of PWM for each phase. The active period can be calculated with the count values at the falling edge and at the rising edge.
(10) Calculate the cycle and duty cycle of the PWM feedback, stop count operation for all channels of the TPU (unit 0), and set TGRA and TGRB for output compare (input capture disable).
Disable interrupts due to TGRA input capture.
(11) Clear the counter value of all channels of the TPU (unit 0) to 0000h.
(12) Set TGRA and TGRB on each channel of the TPU (unit 0) for input capture operation.
TGRA: Rising edge detection (Falling edge detection for a reverse phase channel)
TGRB: Falling edge detection (Rising edge detection for a reverse phase channel)
(13) Set the PWMFBSLR register as follows:
TPU0EN bit: 1b (Internal feedback enable)
FBSL0 bit: 101b (PWM output signals of MTU6 and MTU7)
(14) Enable interrupts by the TGRA input capture on each channel of the TPU (unit 0).
(15) Counting on each channel of the TPU (unit 0) is started, triggered by the timing of the trough of the carrier of MTU6 and MTU7.
(16) An interrupt is generated due to interrupt capture at the rising edge of PWM for each phase.
The active period can be calculated with the count value at the falling edge and at the rising edge.
(17) After calculating the cycle and duty cycle, switch the input source, as necessary, according to the above procedure.

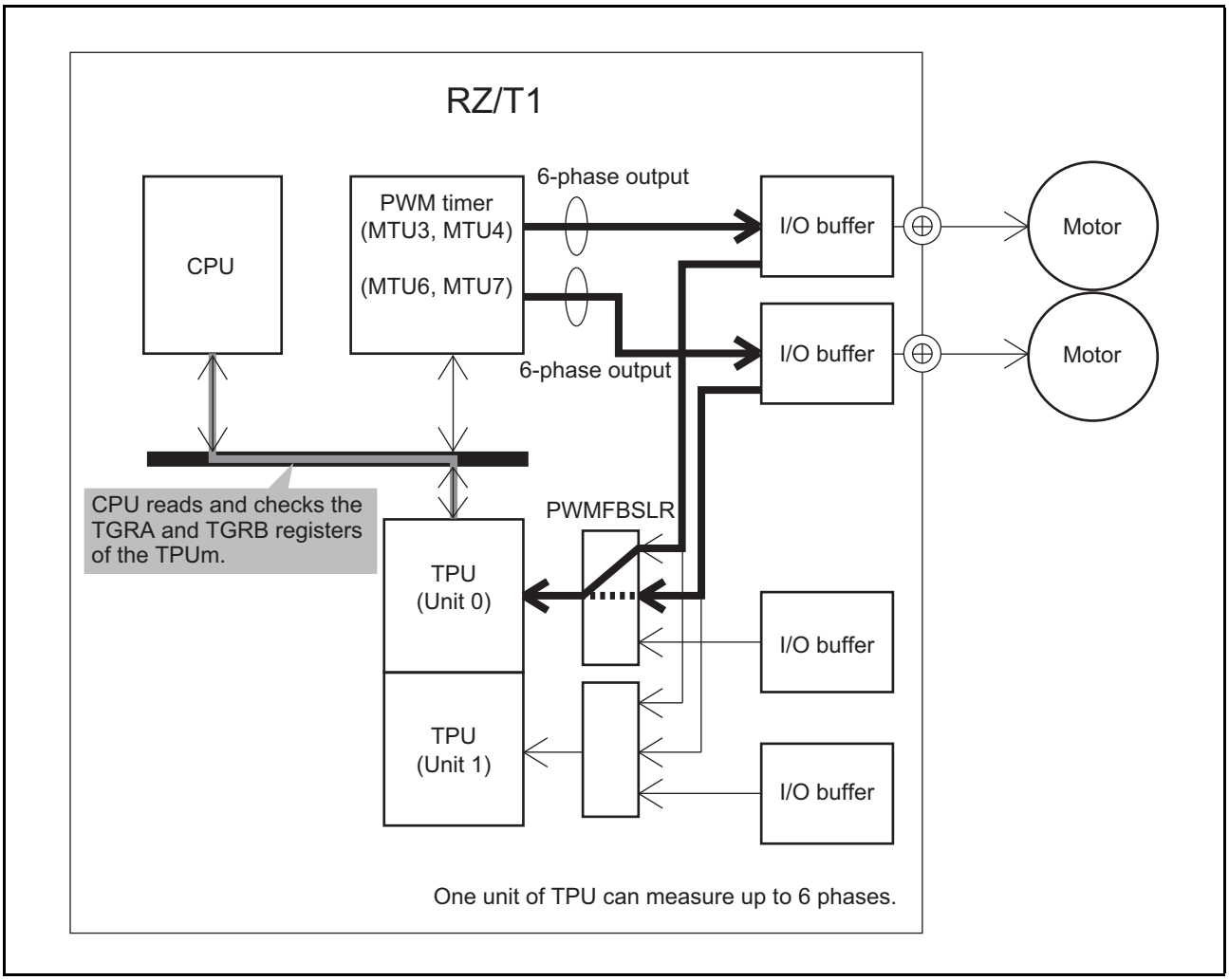


Figure 22.34 Connection Diagram of Example Setting for PWM 2-Axes Measurement

22.3.8.3 Example Setting of PWM 1-Axis Measurement (TPU (Unit 0) Is Set as the Input Capture Function)

Even when the internal PWM feedback input select function is not used (PWMFBSLR.TPUnEN bit = 0), the PWM signals externally input from the TIOCAm and TIOCBm pins can be measured (m = 0 to 5 when n = 0; m = 6 to 11 when n = 1) with the normal input capture function.
In the example below, MTU3 and MTU4 are used to output PWM waveforms. These are treated as PWM signals for external input to the LSI chip. The input signals are captured on either the TIOCAm or TIOCBm pins (m = 0 to 5) and used in the measurement of the PWM waveforms.
For details about the module connection in this setting, see Figure 22.35.

Prerequisite: MTU3a or GPTa to be used is operating as the PWM timer, where one cycle of the carrier is defined as trough-to-trough, and PWM is set to active low. This PWM output signal is externally connected to this LSI with the TIOCAm and TIOCBm pins, and the signal can be input from these pins.

(1) Stop the count operation of all channels of the TPU (unit 0). Set TGRA and TGRB on each channel for output compare (input capture disable).
(2) Set the digital noise filter for each input capture pin of the TPU (unit 0).
(3) Set the count clock, clear conditions, and operating mode for each channel of the TPU (unit 0).
Count clock: PCLKD
Clear conditions: Counter clear at the timing of TGRA input capture
Operating mode: Normal mode
(4) Clear the counter value of all channels of the TPU (unit 0) to 0000h.
(5) Set TGRA and TGRB for each channel of TPU (unit 0) for input capture operation.
TGRA: Rising edge detection (Falling edge detection for a reverse phase channel)
TGRB: Falling edge detection (Rising edge detection for a reverse phase channel)
(6) Set the PWMFBSLR register as follows:
TPU0EN bit: 1b (Internal PWM feedback disable)
FBSL0 bit: Invalid
(7) Enable interrupts by the TGRA input capture on each channel of TPU (unit 0).
(8) Counting on each channel of the TPU (unit 0) is started, triggered by the timing of the trough of the carrier that is input from outside of this LSI via the TIOCmA and TIOCmB pins (m = 0 to 5).
(9) An interrupt is generated due to input capture at the rising edge of PWM for each phase. The active period can be calculated with the count values at the falling edge and at the rising edge.

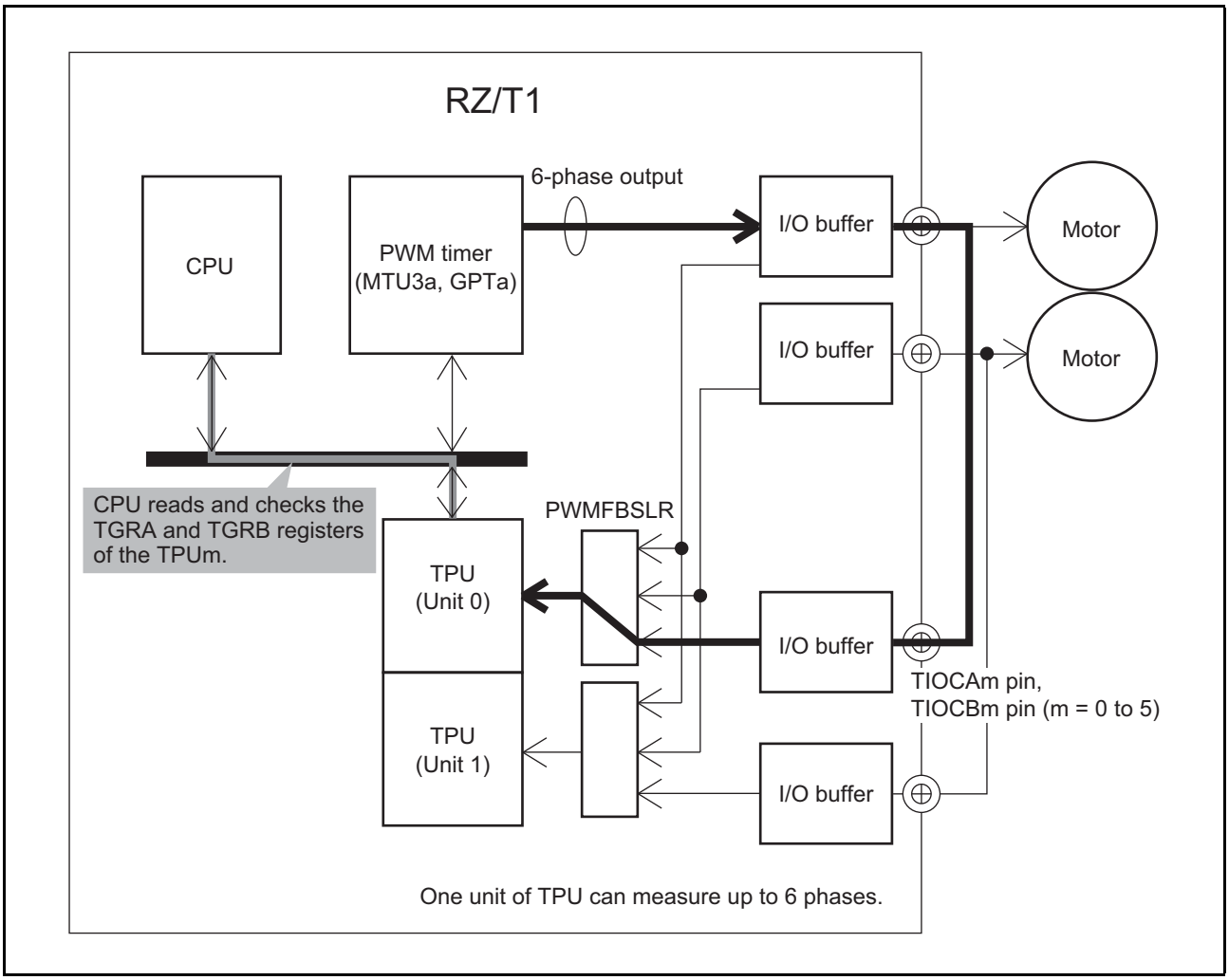


Figure 22.35 Connection Diagram of Example Setting for PWM 1-Axis Measurement

22.3.8.4 Example Setting of PWM 2-Axes Measurement (TPU (Unit 0, Unit 1) Is Set as the Input Capture Function)

Even when the internal PWM feedback input select function is not used (PWMFBSLR.TPUnEN bit = 0), the PWM signals externally input from the TIOCAm and TIOCBm pins can be measured with the normal input capture function (m = 0 to 5 when n = 0; m = 6 to 11 when n = 1).
In the example below, MTU3 and MTU4, and MTU6 and MTU7 are used to output PWM waveforms. These are treated as PWM signals on two axes to be externally input to the LSI. The input signals are captured on either the TIOCAm or TIOCBm pins (m = 0 to 11) or a TPU (unit 0 or unit 1) and used in measurement of the PWM waveforms.
For details about the module connection in this setting, see Figure 22.36.

Prerequisite: MTU3a to be used is operating as the PWM timer, where one cycle of the carrier is defined as trough-to-trough, and PWM is set to active low. This PWM output signal is externally connected to this LSI with the TIOCAm and TIOCBm pins, and the signal can be input from these pins.

(1) Stop the count operation of all channels of the TPU (unit 0) and TPU (unit 1). Set TGRA and TGRB on each channel for output compare (input capture disable).
(2) Set the digital noise filter for each input capture pin of the TPU (unit 0) and TPU (unit 0)
(3) Set the count clock, clear conditions, and operating mode for each channel of the TPU (unit 0) and TPU (unit 1).
- Unit 0/1
Count clock: PCLKD/1
Clear conditions: Counter clear at the timing of TGRA input capture
Operating mode: Normal mode
(4) Clear the counter value of all channels of the TPU (unit 0) and TPU (unit 1) to 0000h.
(5) Set TGRA and TGRB for each channel of the TPU (unit 0) for input capture operation.
- Unit 0/1
TGRA: Rising edge detection (Falling edge detection for a reverse phase channel)
TGRB: Falling edge detection (Rising edge detection for a reverse phase channel)
(6) Set the PWMFBSLR register as follows:
- Unit 0
TPU0EN bit: 0b (Internal feedback disable)
FBSL0 but: Unused
- Unit 1
TPU1EN bit: 0b (Internal feedback disable)
FBSL1 bit: Unused
(7) Enable interrupts by the TGRA input capture on each channel of the TPU (unit 0).
(8) Counting on each channel of the TPU (unit 0) is started, triggered by the timing of the trough of the carrier for the PWM timer, which input the PWM signal from the outside via the pins of the TPU (unit 0).*1
(9) Counting on each channel of the TPU (unit 1) is started, triggered by the timing of the trough of the carrier for the PWM timer, which input the PWM signal from the outside via the pins of the TPU (unit 1).*1
(10) An interrupt is generated due to interrupt capture at the rising edge of PWM for each phase.
The active period can be calculated with the count values at the falling edge and at the rising edge.

Note 1. The orders of step (8) and step (9) can be reversed.

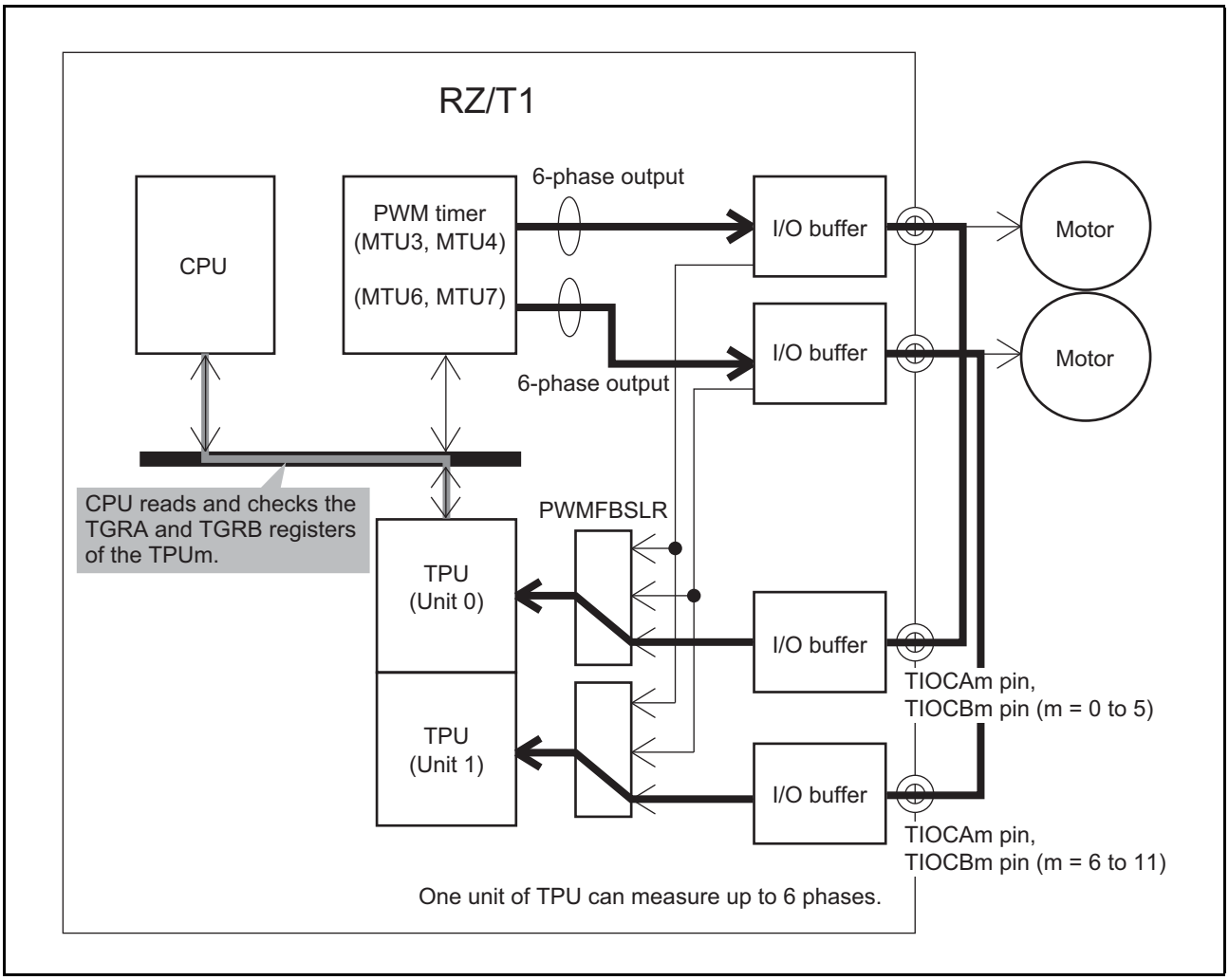


Figure 22.36 Connection Diagram of Example Setting for PWM 2-Axes Measurement

22.4 Interrupt Sources

There are three kinds of TPU interrupt sources: TPUm.TGRy input capture/compare match, TPUm.TCNT overflow, and TPUm.TCNT underflow.

Relative channel priority levels can be changed by the interrupt controller, but the priority within a channel is fixed. For details, see section 12, Interrupt Controller (ICUA).

Table 22.31 lists the TPU interrupt sources.

Table 22.31 TPU Interrupt Sources (1 / 2)

Unit	Channel	Name	Interrupt Source	DMAC Activation
0	TPU0	TGI0A	TPU0.TGRA input capture/compare match	Possible
		TGI0B	TPU0.TGRB input capture/compare match	Possible
		TGI0C	TPU0.TGRC input capture/compare match	Not possible
		TGI0D	TPU0.TGRD input capture/compare match	Not possible
		TCI0V	TPU0.TCNT overflow	Not possible
	TPU1	TGI1A	TPU1.TGRA input capture/compare match	Possible
		TGI1B	TPU1.TGRB input capture/compare match	Possible
		TCI1V	TPU1.TCNT overflow	Not possible
		TCI1U	TPU1.TCNT underflow	Not possible
	TPU2	TGI2A	TPU2.TGRA input capture/compare match	Possible
		TGI2B	TPU2.TGRB input capture/compare match	Possible
		TCI2V	TPU2.TCNT overflow	Not possible
		TCI2U	TPU2.TCNT underflow	Not possible
	TPU3	TGI3A	TPU3.TGRA input capture/compare match	Possible
		TGI3B	TPU3.TGRB input capture/compare match	Possible
		TGI3C	TPU3.TGRC input capture/compare match	Not possible
		TGI3D	TPU3.TGRD input capture/compare match	Not possible
		TCI3V	TPU3.TCNT overflow	Not possible
	TPU4	TGI4A	TPU4.TGRA input capture/compare match	Possible
		TGI4B	TPU4.TGRB input capture/compare match	Possible
		TCI4V	TPU4.TCNT overflow	Not possible
		TCI4U	TPU4.TCNT underflow	Not possible
	TPU5	TGI5A	TPU5.TGRA input capture/compare match	Possible
		TGI5B	TPU5.TGRB input capture/compare match	Possible
		TCI5V	TPU5.TCNT overflow	Not possible
		TCI5U	TPU5.TCNT underflow	Not possible

Table 22.31 TPU Interrupt Sources (2 / 2)

Unit	Channel	Name	Interrupt Source	DMAC Activation
1	TPU6	TGI6A	TPU6.TGRA input capture/compare match	Not possible
		TGI6B	TPU6.TGRB input capture/compare match	Not possible
		TGI6C	TPU6.TGRC input capture/compare match	Not possible
		TGI6D	TPU6.TGRD input capture/compare match	Not possible
		TCI6V	TPU6.TCNT overflow	Not possible
	TPU7	TGI7A	TPU7.TGRA input capture/compare match	Not possible
		TGI7B	TPU7.TGRB input capture/compare match	Not possible
		TCI7V	TPU7.TCNT overflow	Not possible
		TCI7U	TPU7.TCNT underflow	Not possible
	TPU8	TGI8A	TPU8.TGRA input capture/compare match	Not possible
		TGI8B	TPU8.TGRB input capture/compare match	Not possible
		TCI8V	TPU8.TCNT overflow	Not possible
		TCI8U	TPU8.TCNT underflow	Not possible
	TPU9	TGI9A	TPU9.TGRA input capture/compare match	Not possible
		TGI9B	TPU9.TGRB input capture/compare match	Not possible
		TGI9C	TPU9.TGRC input capture/compare match	Not possible
		TGI9D	TPU9.TGRD input capture/compare match	Not possible
		TCI9V	TPU9.TCNT overflow	Not possible
	TPU10	TGI10A	TPU10.TGRA input capture/compare match	Not possible
		TGI10B	TPU10.TGRB input capture/compare match	Not possible
		TCI10V	TPU10.TCNT overflow	Not possible
		TCI10U	TPU10.TCNT underflow	Not possible
	TPU11	TGI11A	TPU11.TGRA input capture/compare match	Not possible
		TGI11B	TPU11.TGRB input capture/compare match	Not possible
		TCI11V	TPU11.TCNT overflow	Not possible
		TCI11U	TPU11.TCNT underflow	Not possible

Note: This table lists the initial state immediately after a reset. The relative channel priority levels can be changed by the interrupt controller.

(1) Input Capture/Compare Match Interrupt

A TGImy interrupt (m = 0 to 11) is requested when the TPUm.TIER.TGIEy bit (y = A, B, C, D) is set to 1 by the occurrence of a TPUm.TGRy input capture/compare match on a channel. The TPU has 32 input capture/compare match interrupts, four each for TPU0, TPU3, TPU6, and TPU9, and two each for TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11.

(2) Overflow Interrupt

A TCImV interrupt (m = 0 to 11) is requested when the TPUm.TIER.TCIEV bit is set to 1 by the occurrence of a TPUm.TCNT overflow on a channel. The TPU has 12 overflow interrupts, one for each channel.

(3) Underflow Interrupt

A TCImU interrupt (m = 0 to 11) is requested when the TPUm.TIER.TCIEU bit is set to 1 by the occurrence of a TPUm.TCNT underflow on a channel. The TPU has total of eight underflow interrupts, one each for TPU1, TPU2, TPU4, TPU5, TPU7, TPU8, TPU10, and TPU11.

22.5 DMAC Activation

Input capture/compare match interrupts from the TPUm.TGRA and TPUm.TGRB registers can activate the corresponding DMACs. For details, see section 15, DMA Controller (DMACAa).
As the sources for activating DMACs, the TPU can use two input capture/compare match interrupts from the TPUm.TGRA and TPUm.TGRB registers (m = 0 to 5) per channel of unit 0, twelve interrupts in total. Unit 1 does not have sources for activating DMACs.

22.6 A/D Converter Activation

The TPU can activate the A/D converter by the TPUm.TGRA input capture/compare match for each channel (m = 0 to 4, 6 to 10).
When the TPUm.TIER.TTGE bit is set to 1, the TPU requests the A/D converter to start A/D conversion by the occurrence of a TPUm.TGRA input capture/compare match on a particular channel (m = 0 to 4, 6 to 10).
For the corresponding unit of A/D converter, see section 43, 12-Bit A/D Converter (S12ADCa).

22.7 PPG Trigger

Input capture to or compare match with TGRA and TGRB in TPU0 to TPU3 of unit 0 can be made to act as a PPG1 waveform trigger. Unit 1 does not generate a PPG trigger. For details, see section 23, Programmable Pulse Generator (PPG).

22.8 Operation Timing

22.8.1 Input/Output Timing

(1) TPUm.TCNT Count Timing

Figure 22.37 shows TPUm.TCNT count timing in internal clock operation, and Figure 22.38 shows TCNT count timing in external clock operation (m = 0 to 11).

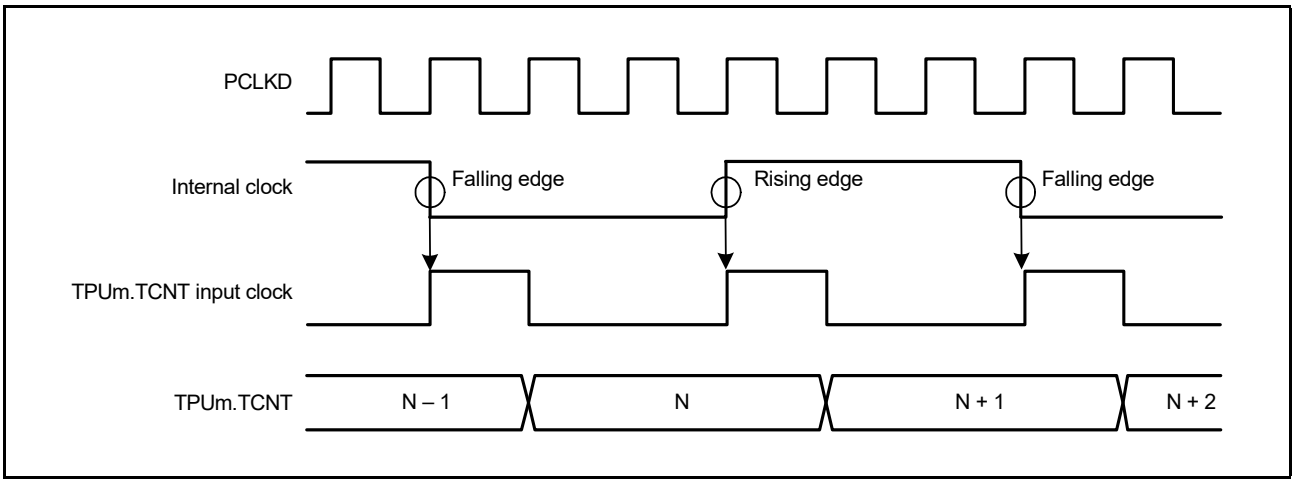


Figure 22.37 Count Timing in Internal Clock Operation

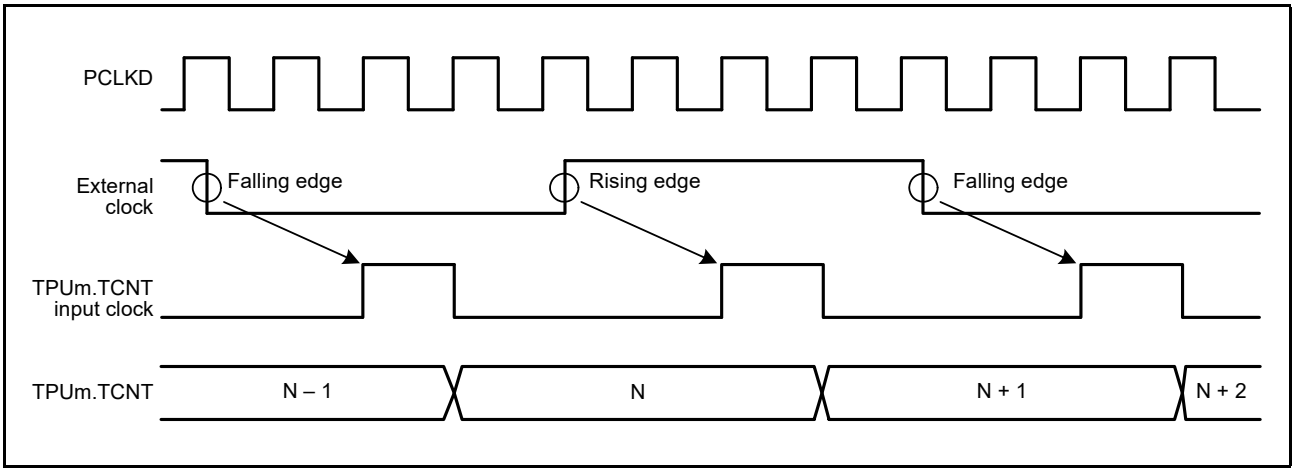


Figure 22.38 Count Timing in External Clock Operation

(2) Output Compare Output Timing

A compare match signal is generated in the final state in which TPUm.TCNT and TPUm.TGRy match (the point at which the count value matched by TCNT is updated). When a compare match signal is generated, the output value set in TPUm.TIORH, TPUm.TIORL, or TPUm.TIOR is output to the output compare output pin TIOCyn (y = A to D when n = 0, 3, 6, 9; y = A, B when n = 1, 2, 4, 5, 7, 8, 10, 11). After a match between TCNT and TGRy, the compare match signal is not generated until the TCNT input clock is generated.

Figure 22.39 shows output compare output timing.

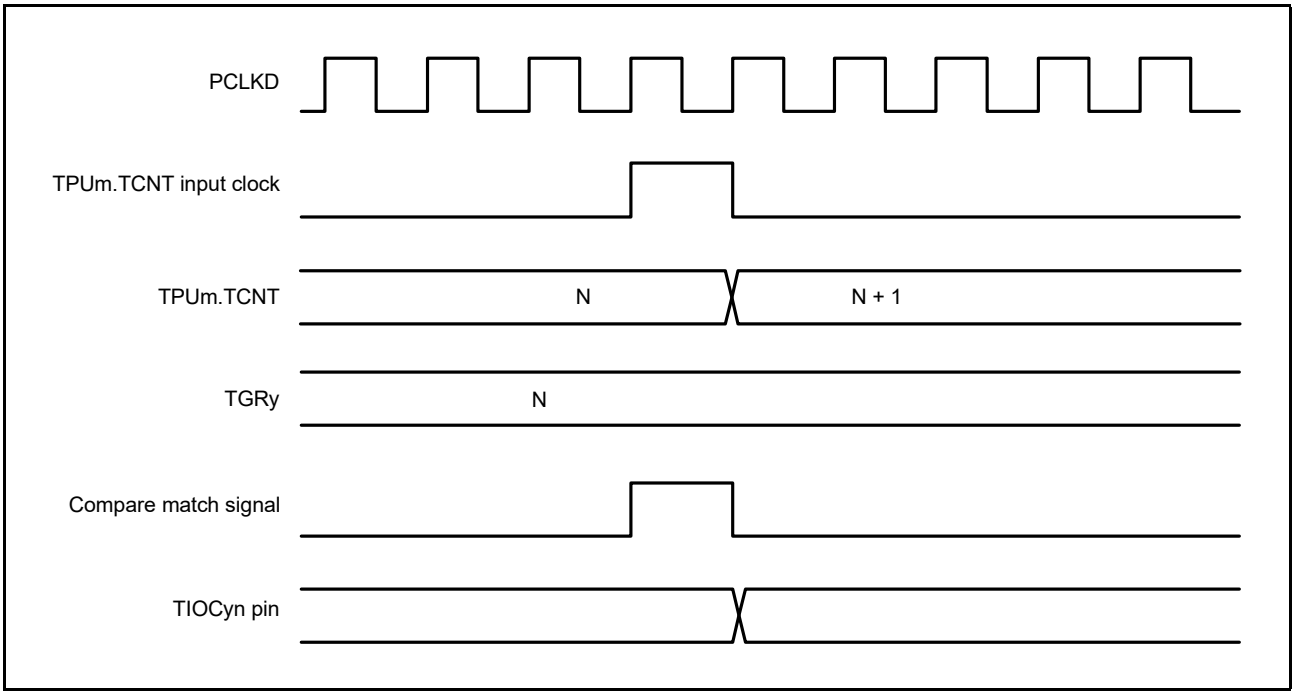


Figure 22.39 Output Compare Output Timing

(3) Input Capture Signal Timing

Figure 22.40 shows input capture signal timing.

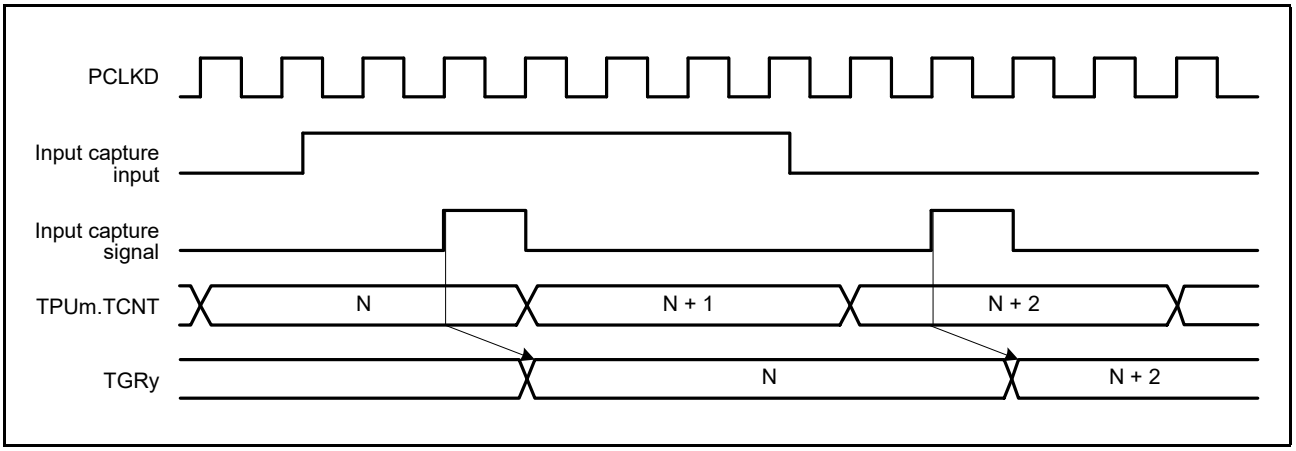


Figure 22.40 Input Capture Signal Timing

(4) Timing for Counter Clearing by Compare Match/Input Capture

Figure 22.41 shows the timing when counter clearing by compare match occurrence is specified, and Figure 22.42 shows the timing when counter clearing by input capture occurrence is specified.

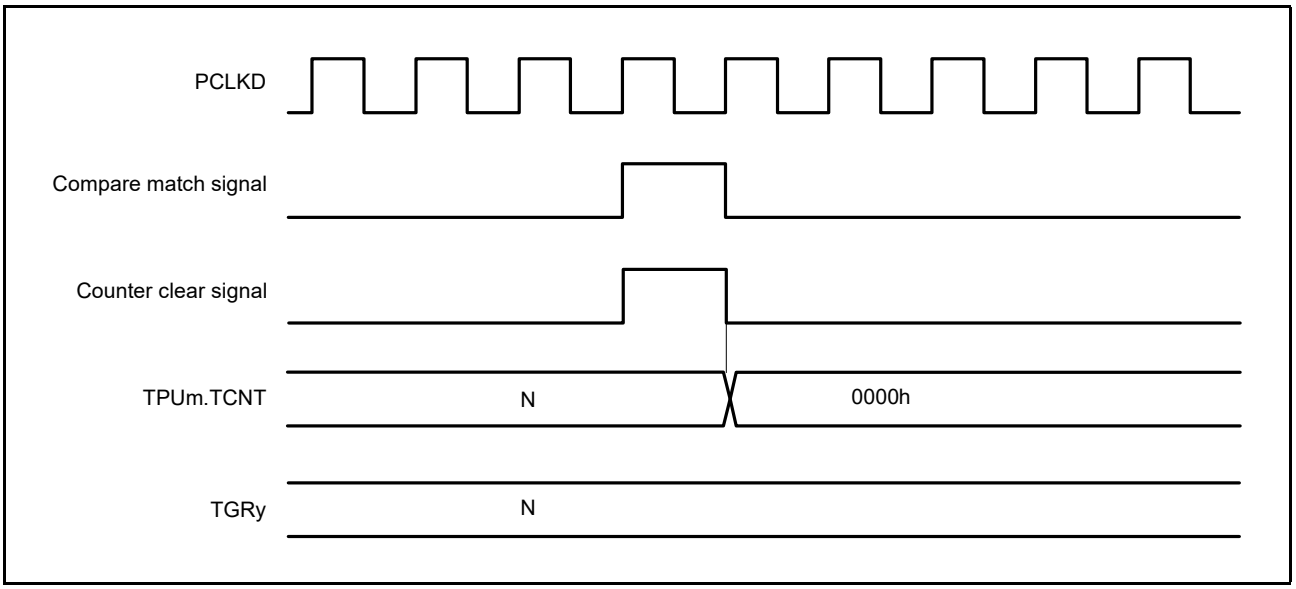


Figure 22.41 Counter Clear Timing (Compare Match)

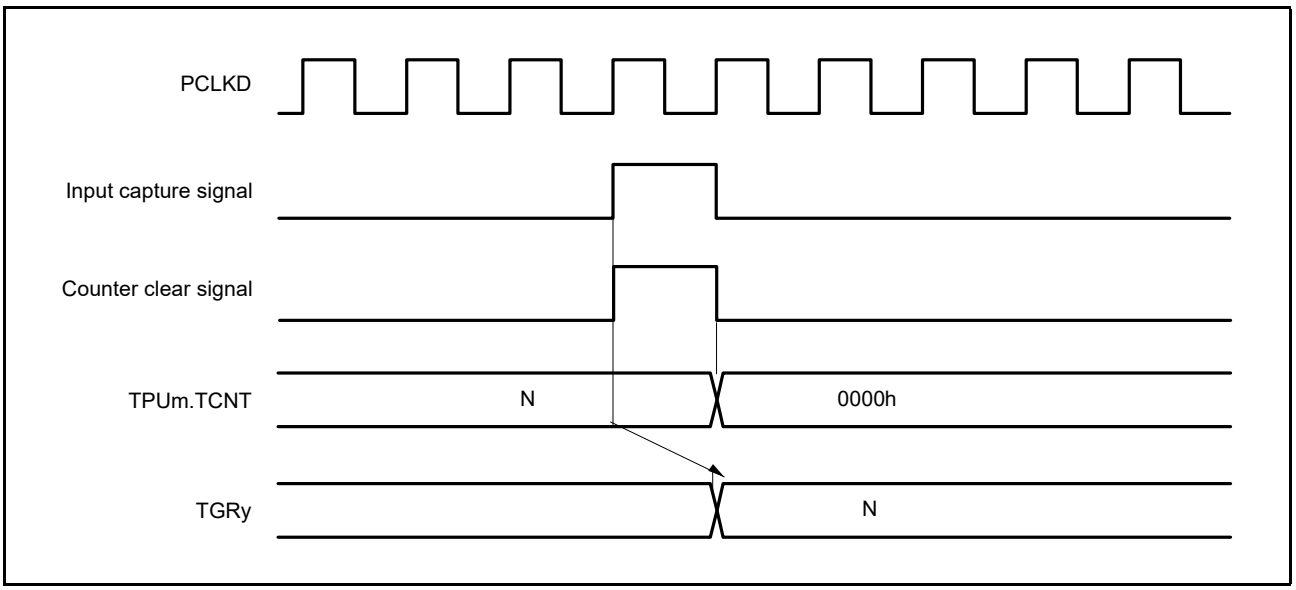


Figure 22.42 Counter Clear Timing (Input Capture)

(5) Buffer Operation Timing

Figure 22.43 and Figure 22.44 show the timings in buffer operation.

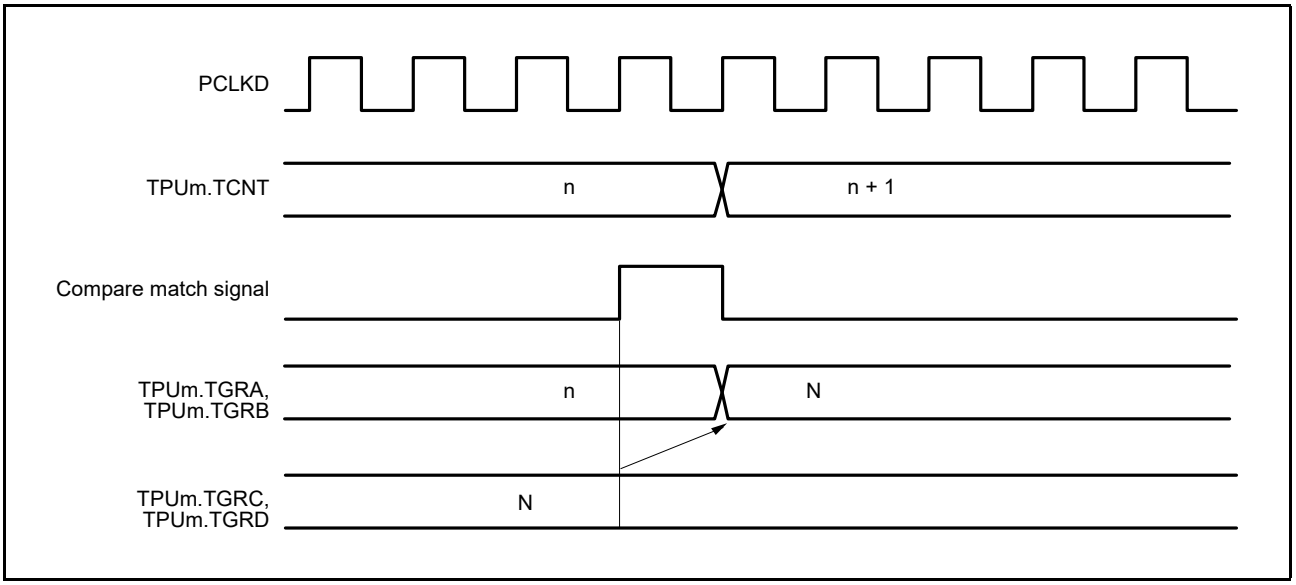


Figure 22.43 Buffer Operation Timing (Compare Match)

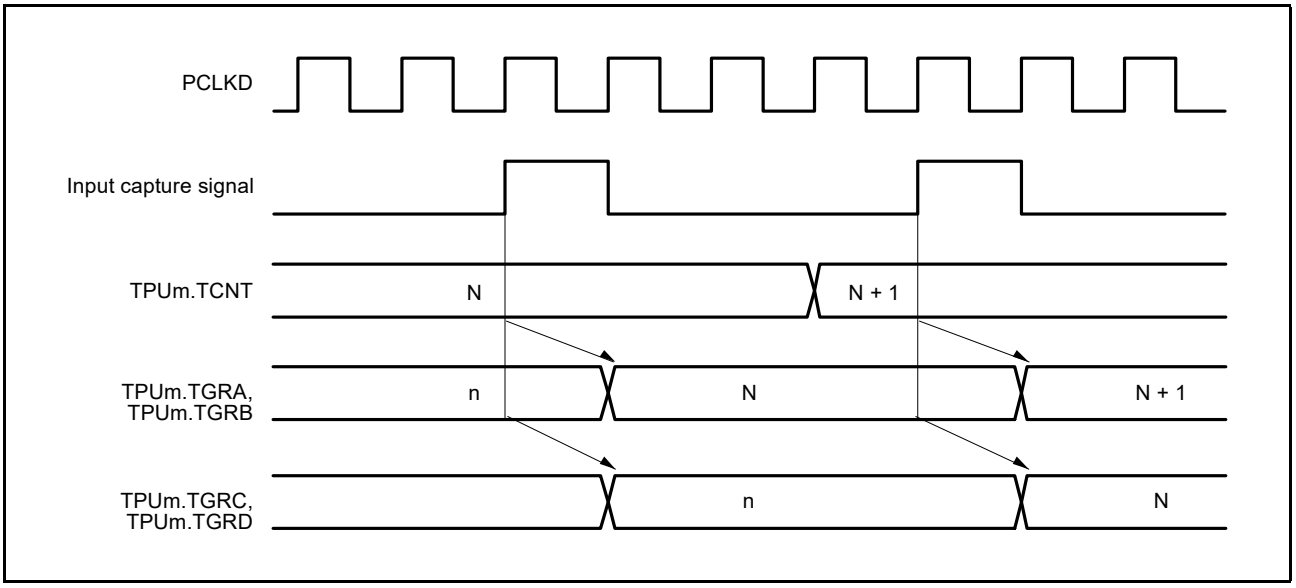


Figure 22.44 Buffer Operation Timing (Input Capture)

22.8.2 Interrupt Signal Timing

(1) Timing of Interrupt Signal Setting on Compare Match

Figure 22.45 shows the timing for setting the TGImy interrupt signal by compare match occurrence (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).

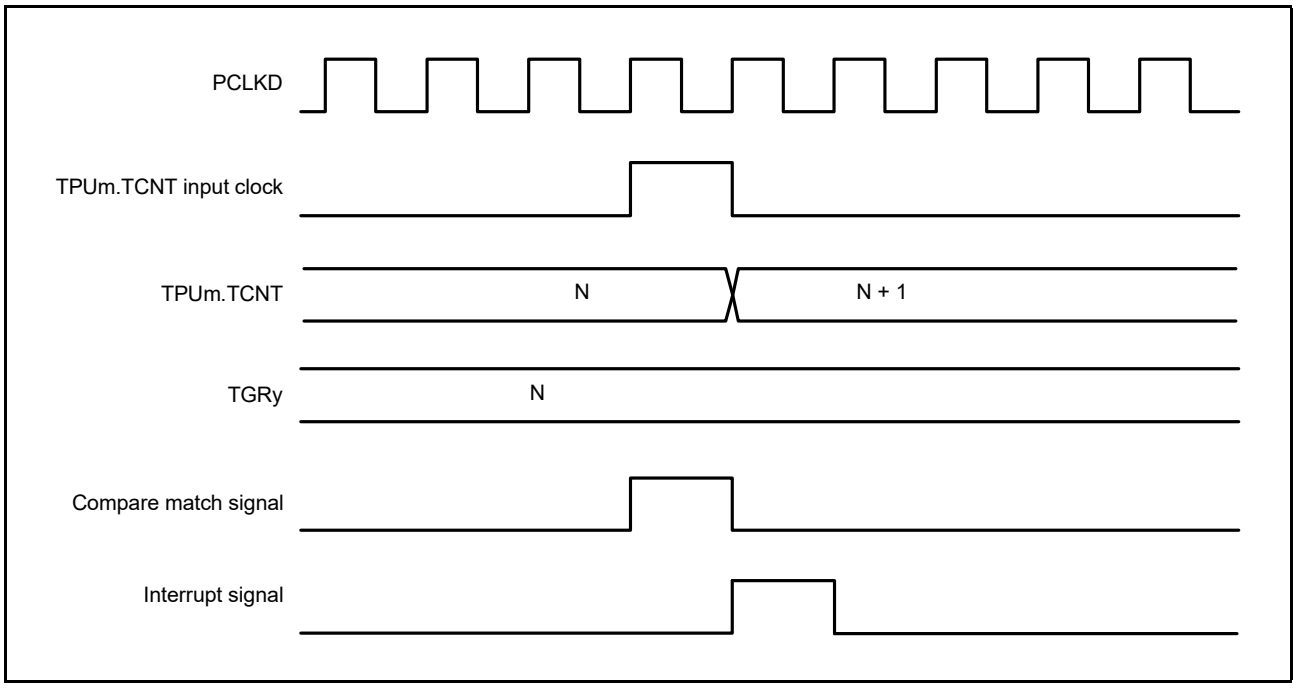


Figure 22.45 TGImy Interrupt Timing (Compare Match)

(2) Timing of Interrupt Signal Setting on Input Capture

Figure 22.46 shows the timing for setting the TGImy interrupt signal by input capture occurrence (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).

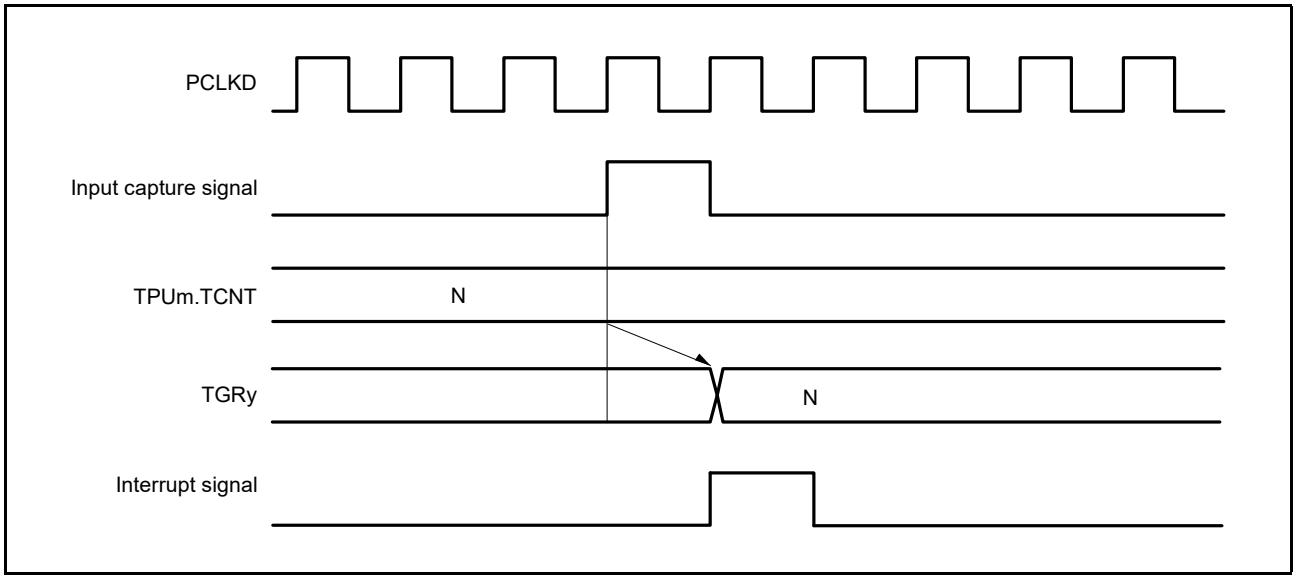


Figure 22.46 TGImy Interrupt Timing (Input Capture)

(3) Timing of TCImV/TCImU Interrupt Signal Setting

Figure 22.47 shows the timing for generating the TCImV interrupt signal by overflow occurrence (m = 0 to 11).
Figure 22.48 shows the timing for generating the TCInU interrupt signal by underflow occurrence (n = 1, 2, 4, 5, 7, 8, 10, 11).

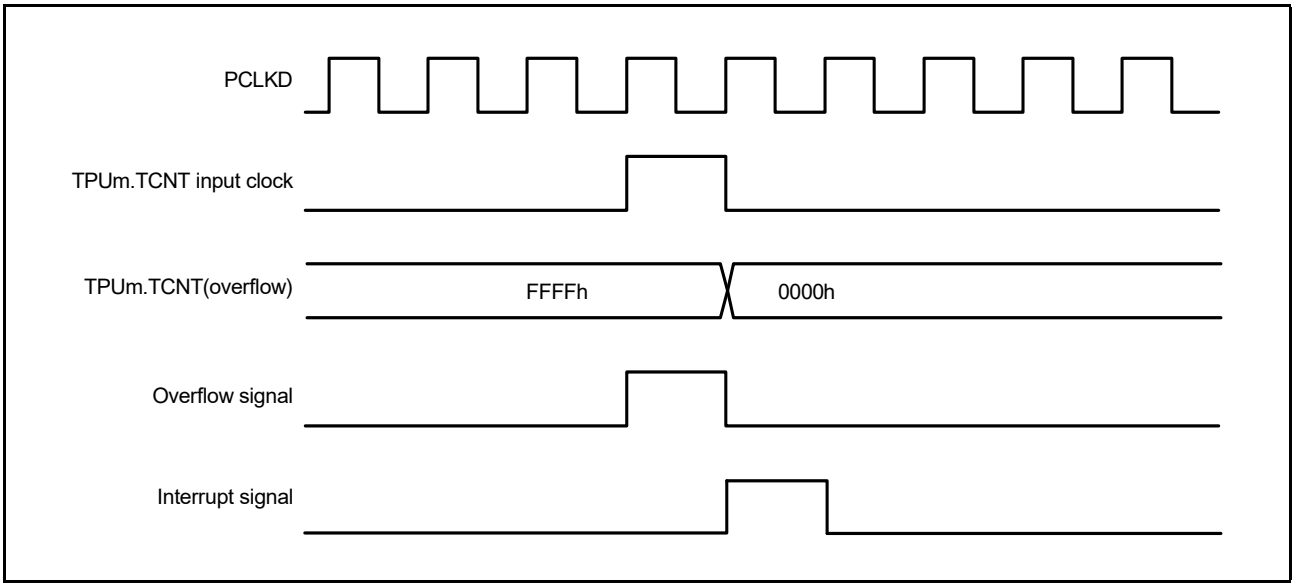


Figure 22.47 TCImV Interrupt Setting Timing

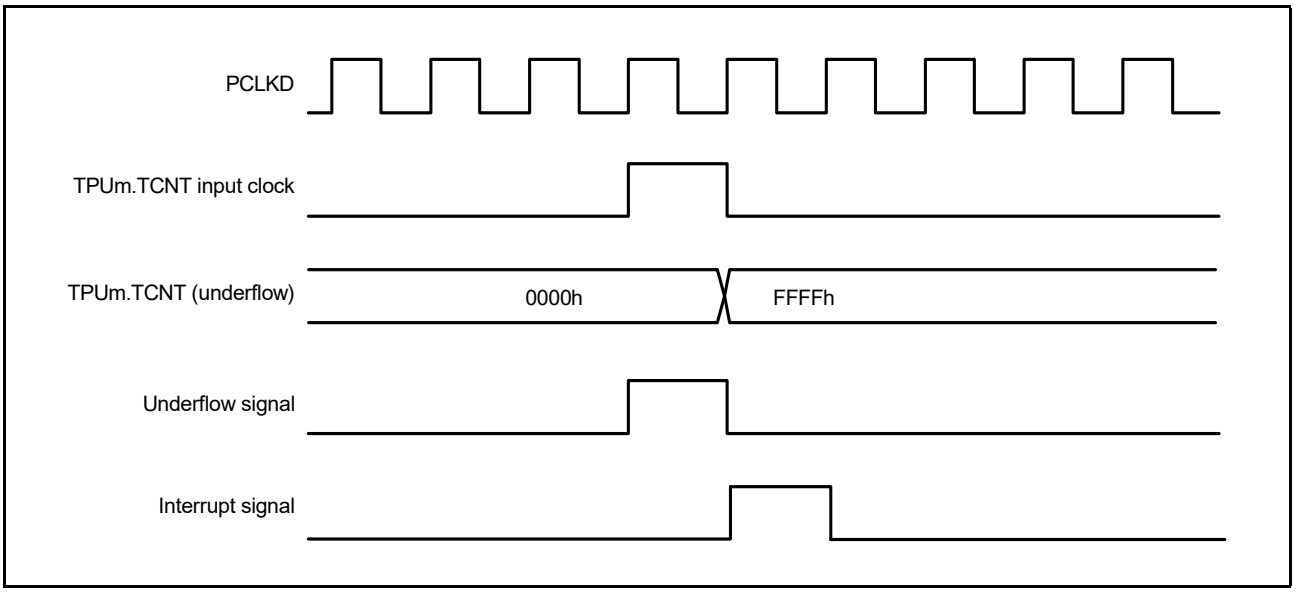


Figure 22.48 TCImU Interrupt Setting Timing

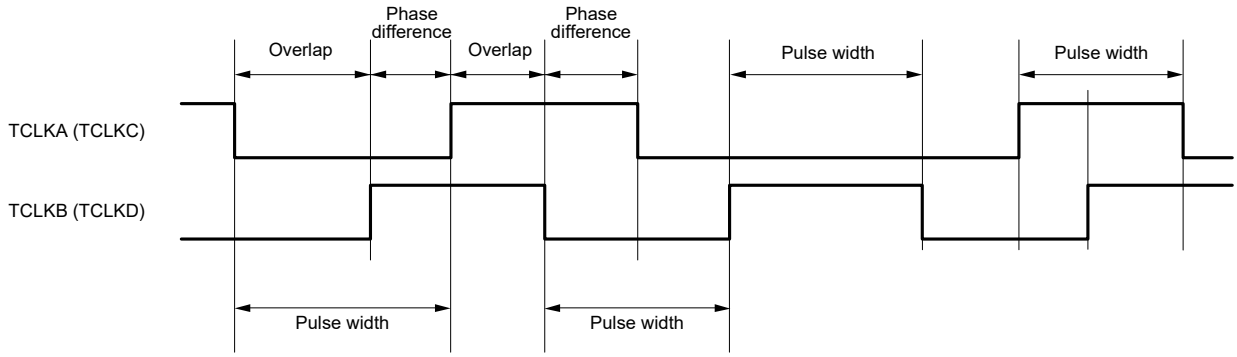
22.9 Usage Notes

22.9.1 Module-Stop Function Setting

Operation of the TPU can be disabled or enabled using the module-stop control register. The TPU does not operate with the initial setting. Register access is enabled by clearing module-stop state. For details, see section 9, Low-Power Consumption Function.

22.9.2 Input Clock Restrictions

The input clock pulse width must be at least 1.5 cycles of PCLKD in the case of single-edge detection, and at least 2.5 cycles of PCLKD in the case of both-edge detection. The TPU will not operate properly with a narrower pulse width. In phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 cycles of PCLKD, and the pulse width must be at least 2.5 cycles of PCLKD. Figure 22.49 shows the input clock conditions in phase counting mode.



Note: Phase difference or overlap: At least 1.5 cycles of PCLKD
Pulse width : At least 2.5 cycles of PCLKD

Figure 22.49 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

22.9.3 Caution on Cycle Setting

When counter clearing by compare match is set, TPUm.TCNT is cleared in the final state in which it matches the TGRy value (the point at which the count value matched by TCNT is updated). Consequently, the actual counter frequency is given by the following formula (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).

$$f = \frac{f_{TCNT_CLK}}{(N+1)}$$

f : Counter frequency
f_{TCNT_CLK} : Counter clock frequency
N : TGRy set value

22.9.4 Conflict between TPUm.TCNT Write and Clear Operations

If the counter clearing signal is generated in a TPUm.TCNT write cycle, TPUm.TCNT clearing takes precedence and the TPUm.TCNT write is not performed (m = 0 to 11). Figure 22.50 shows the timing in this case.

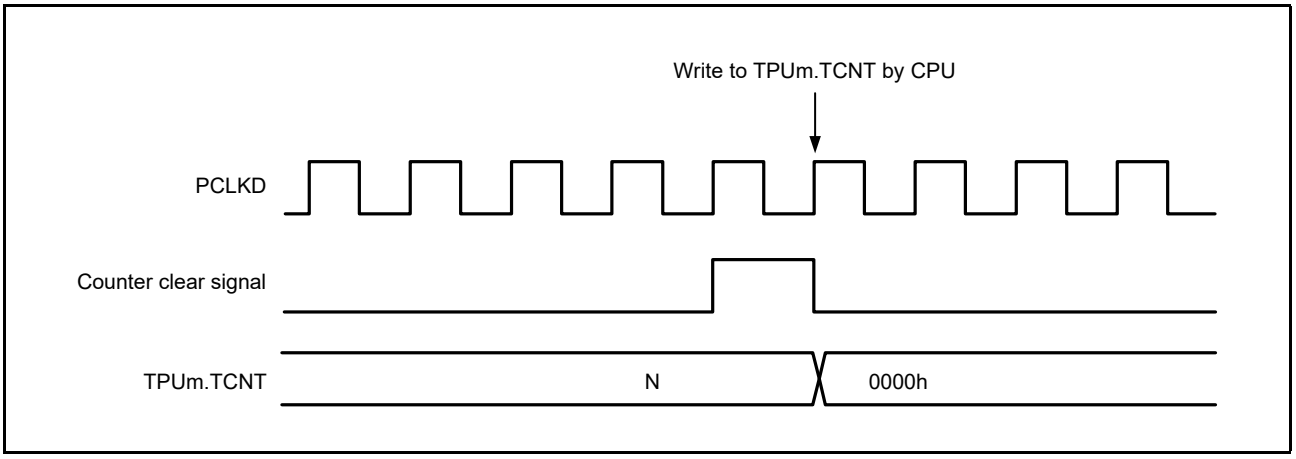


Figure 22.50 Conflict between TPUm.TCNT Write and Clear Operations

22.9.5 Conflict between TPUm.TCNT Write and Increment Operations

If incrementing occurs in a TPUm.TCNT write cycle, the TPUm.TCNT write takes precedence and TPUm.TCNT is not incremented (m = 0 to 11). Figure 22.51 shows the timing in this case.

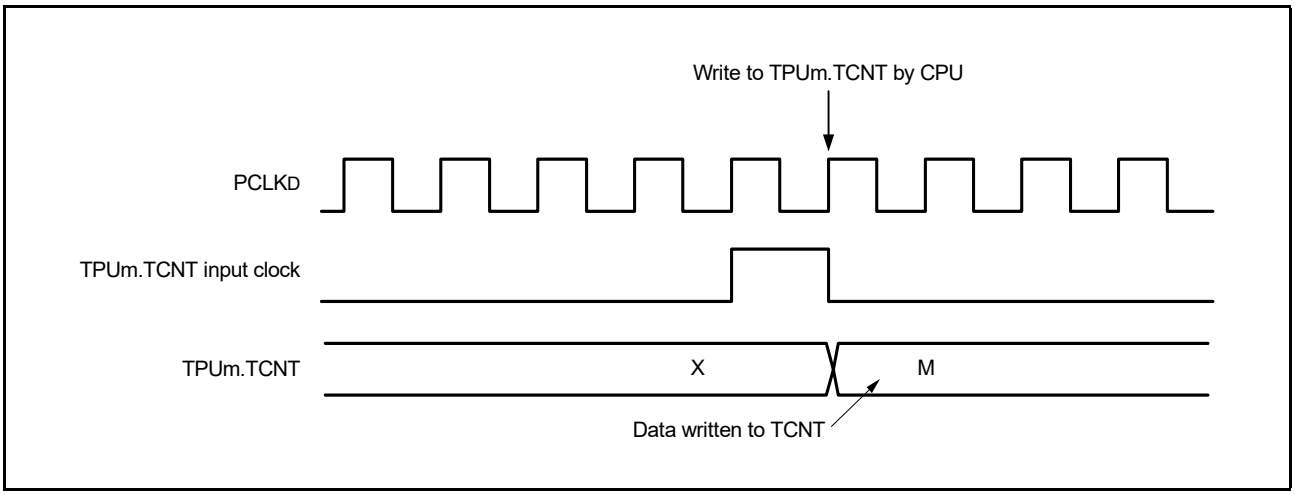


Figure 22.51 Conflict between TPUm.TCNT Write and Increment Operations

22.9.6 Conflict between TPUm.TGRy Write and Compare Match

If a compare match occurs in a TGRy write cycle, the TGRy write takes precedence and the compare match signal is disabled. A compare match also does not occur when the same value as before is written (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).
Figure 22.52 shows the timing in this case.

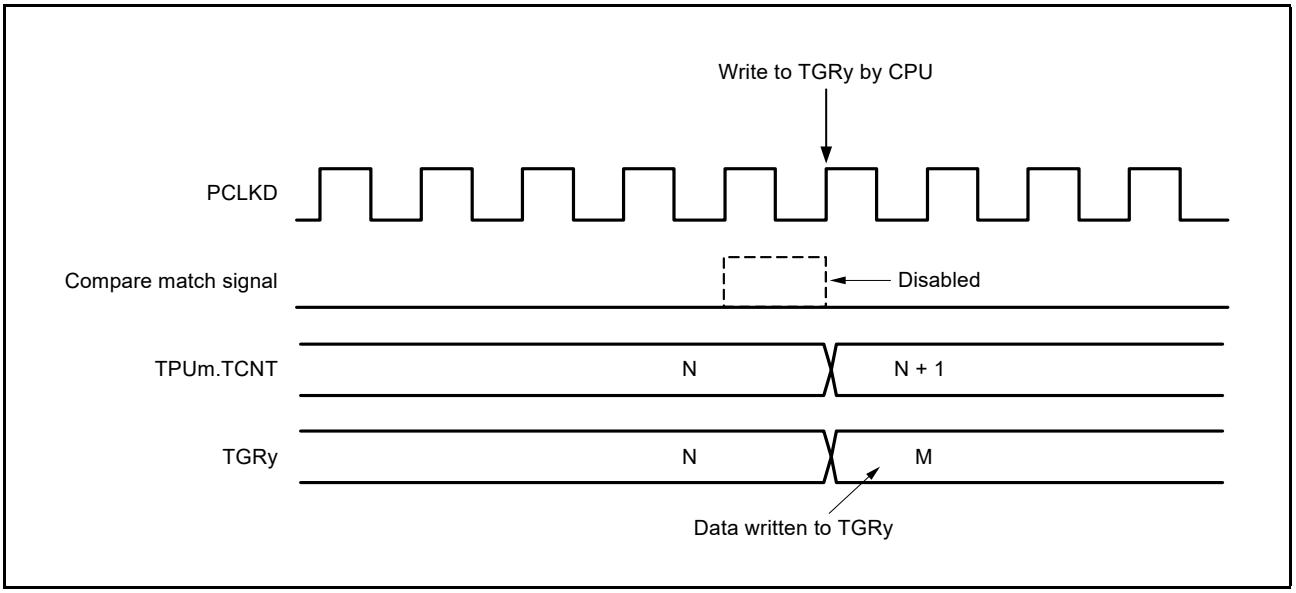


Figure 22.52 Conflict between TGRy Write and Compare Match

22.9.7 Conflict between Buffer Register Write and Compare Match

If a compare match occurs in a TGRy write cycle, the data transferred to TGRy by the buffer operation will be the data before writing (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).
Figure 22.53 shows the timing in this case.

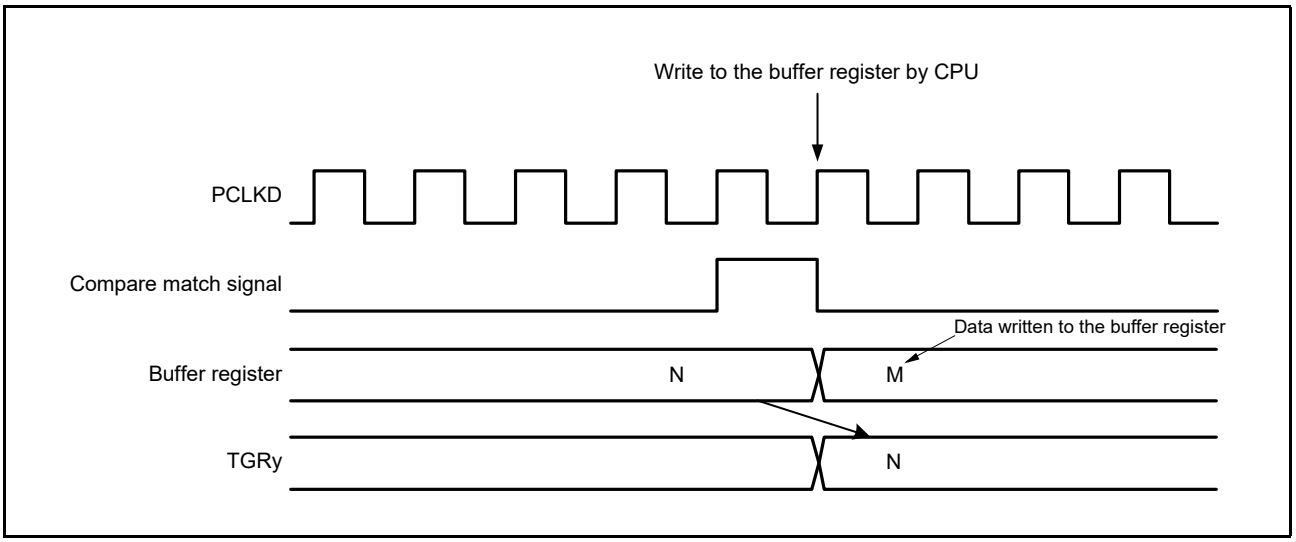


Figure 22.53 Conflict between Buffer Register Write and Compare Match

22.9.8 Conflict between TPUm.TGRy Read and Input Capture

If the input capture signal is generated in a TGRy read cycle, the data that is read will be the data before input capture transfer (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).
Figure 22.54 shows the timing in this case.

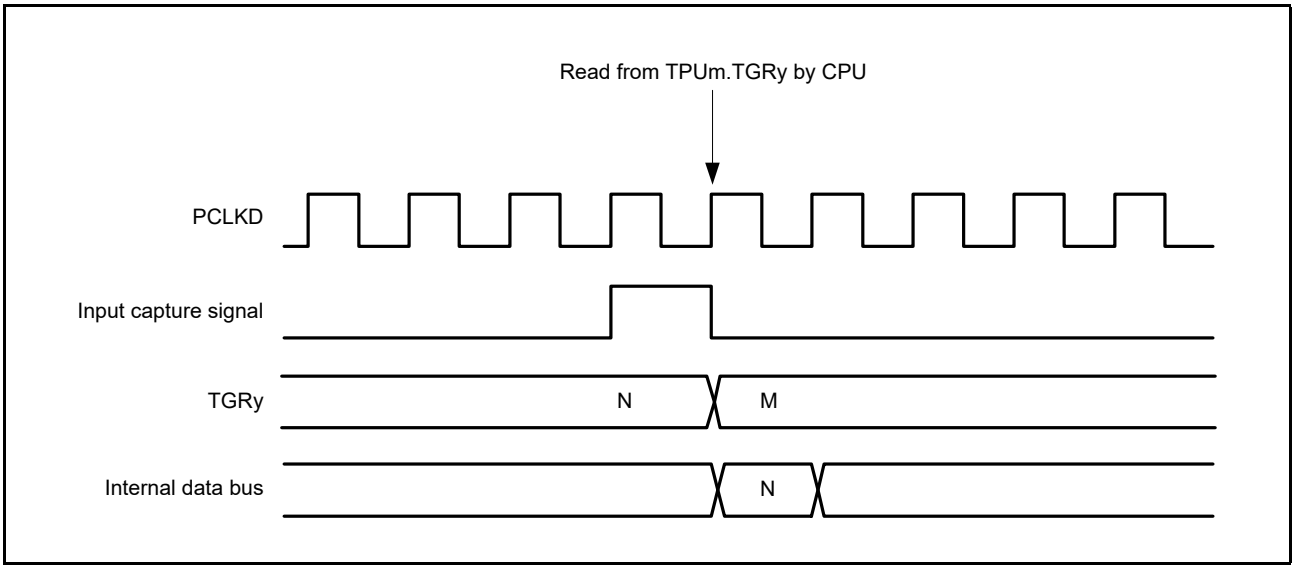


Figure 22.54 Conflict between Reading from the TPUm.TGRy Register and Input Capture

22.9.9 Conflict between TPUm.TGRy Write and Input Capture

If the input capture signal is generated in a TGRy write cycle, the input capture operation takes precedence and the write to TGRy is not performed (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11). Figure 22.55 shows the timing in this case.

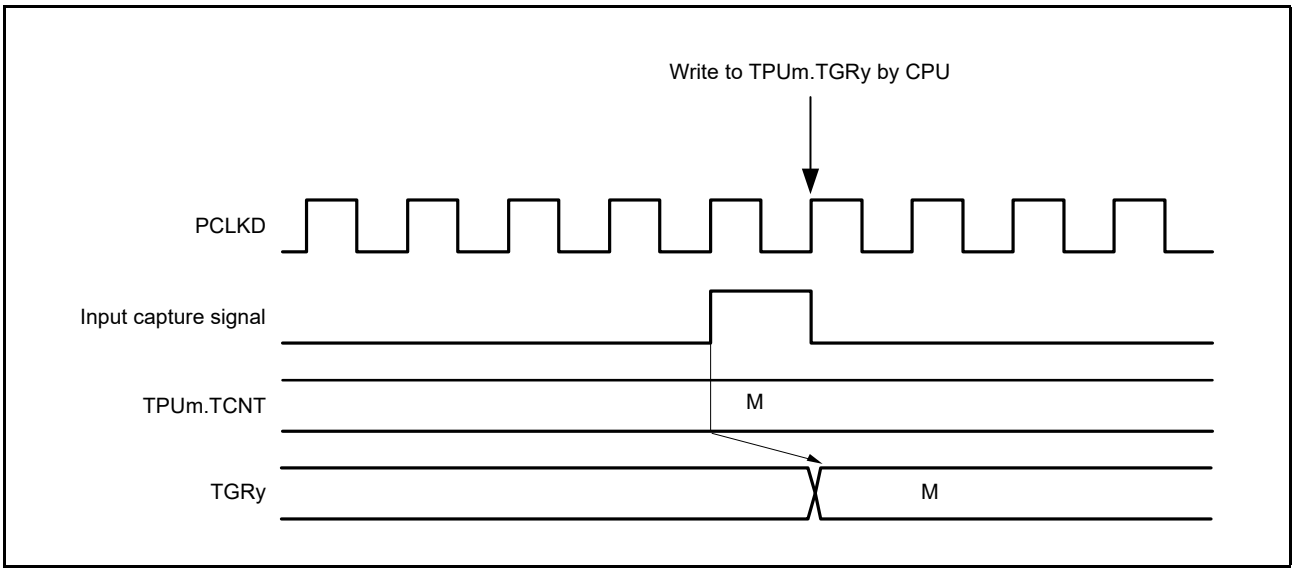


Figure 22.55 Conflict between Writing to the TPUm.TGRy Register and Input Capture

22.9.10 Conflict between Buffer Register Write and Input Capture

If the input capture signal is generated in a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11). Figure 22.56 shows the timing in this case.

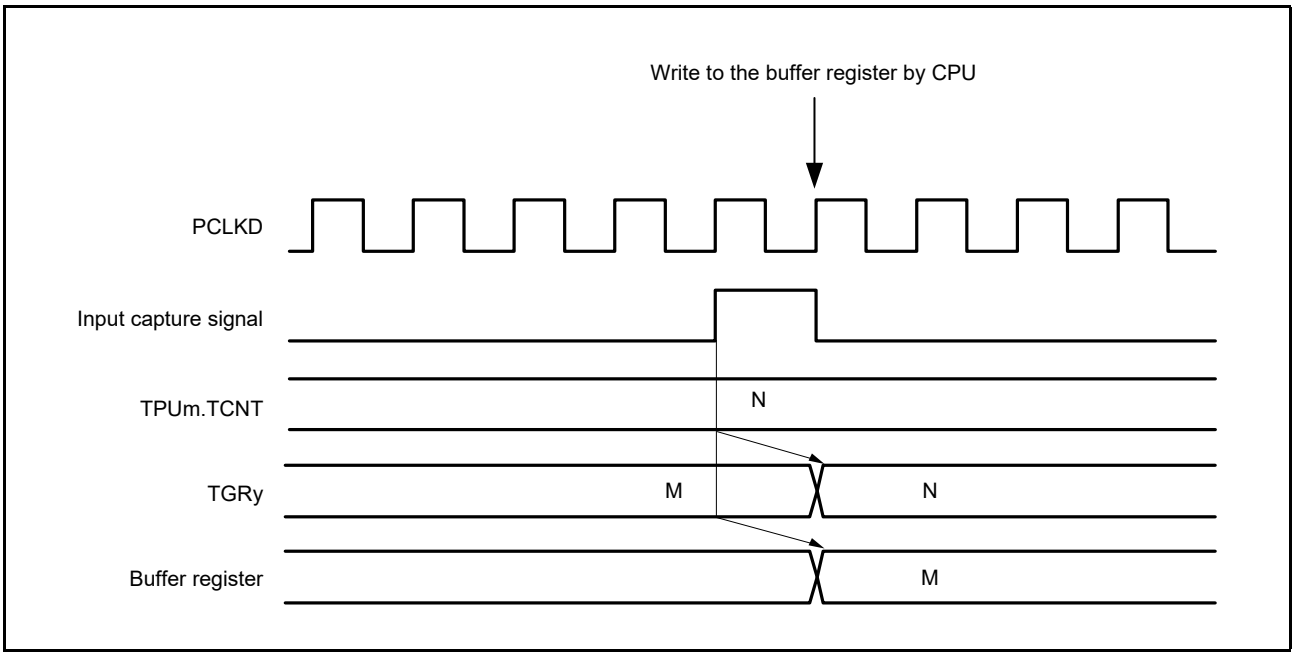


Figure 22.56 Conflict between Buffer Register Write and Input Capture

22.9.11 Conflict between Overflow/Underflow and Counter Clearing

If overflow/underflow and counter clearing*1 occur simultaneously, TPUm.TCNT counter is cleared and an overflow interrupt (TCImV)/underflow interrupt (TCInU) is generated (m = 0 to 11, n = 1, 2, 4, 5, 7, 8, 10, 11).
Figure 22.57 shows the operation timing when a TPUm.TGRy compare match is specified as the clearing source and FFFFh is set in TGRy (y = A to D when m = 0, 3, 6, 9; y = A, B when m = 1, 2, 4, 5, 7, 8, 10, 11).

Note 1. There are four counter clearing sources:
- Compare match
- Input capture
- Synchronous clearing
- Counter clear operation by an event signal

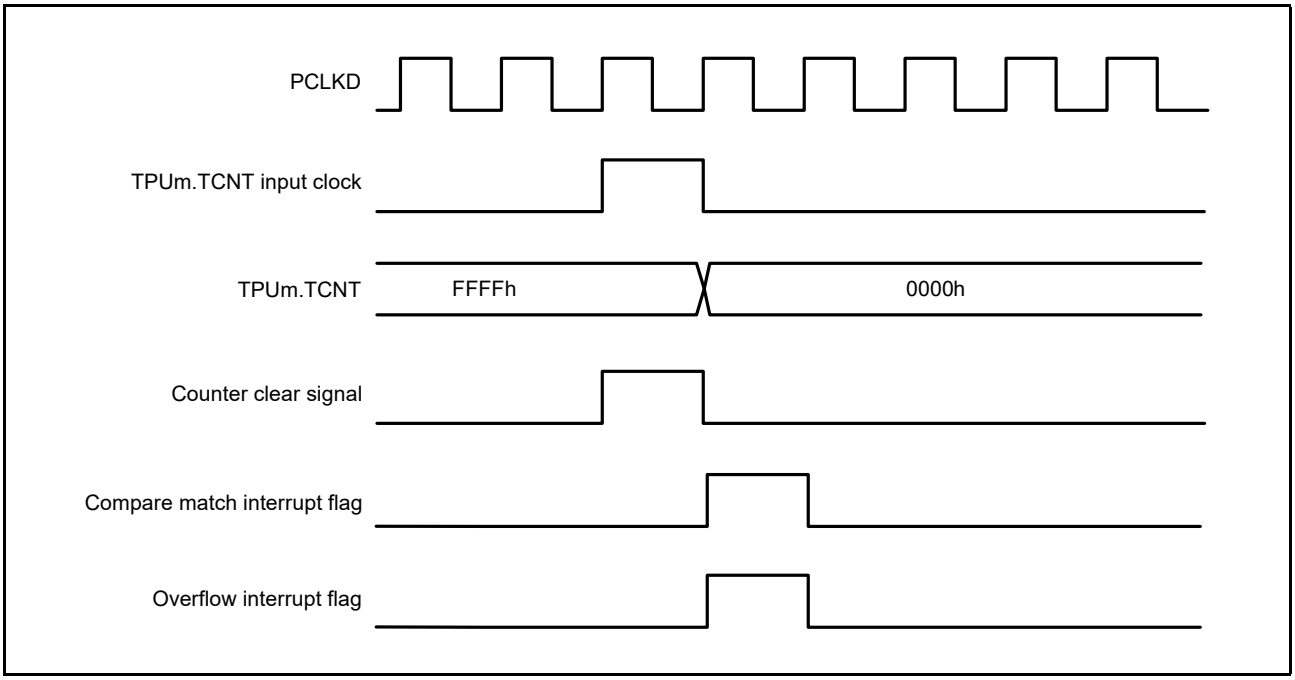


Figure 22.57 Conflict between Overflow and Counter Clearing

22.9.12 Conflict between TPUm.TCNT Write and Overflow/Underflow

If an overflow/underflow occurs due to increment/decrement in a TPUm.TCNT write cycle, the TPUm.TCNT write takes precedence.

Figure 22.58 shows the operation timing when there is conflict between TPUm.TCNT write and overflow (m = 0 to 11).

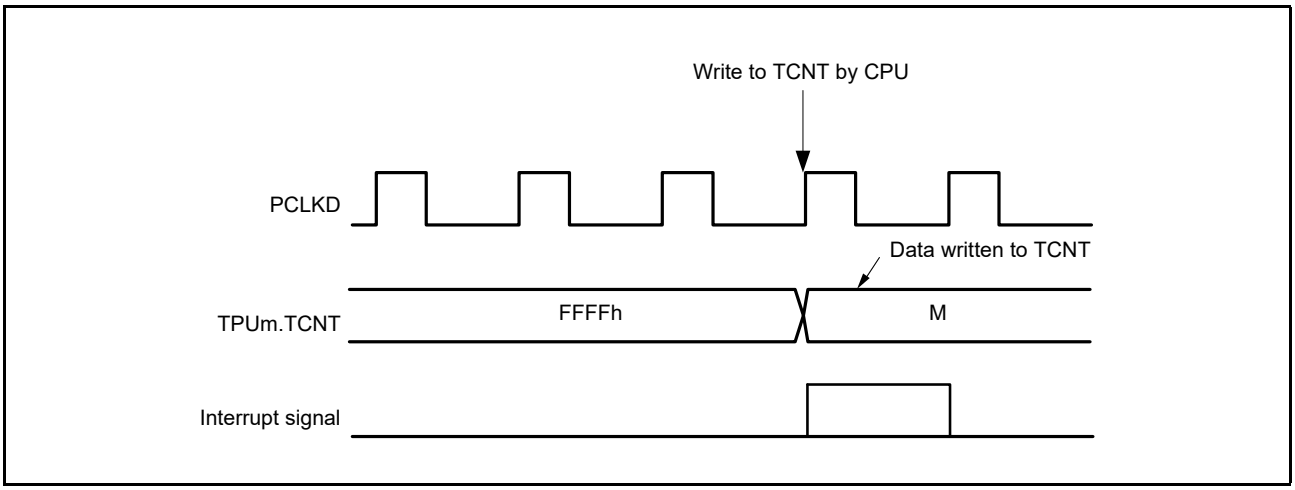


Figure 22.58 Conflict between TCNT Write and Overflow

22.9.13 Continuous Output of Interrupt Signal in Response to Compare Match

When TGRy is set to 0000h, PCLKD/1 is set as the counter clock, and compare match is set as the trigger for clearing of the counter clock, the value of the counter (TCNT) counter remains 0000h, and the interrupt signal will be output continuously (i.e. its level will be flat) rather than output over a single cycle. Consequently, interrupts will not be detected in response to second and subsequent compare matches. (y = A to D)

Figure 22.59 shows the timing for continuous output of the interrupt signal in response to a compare match.

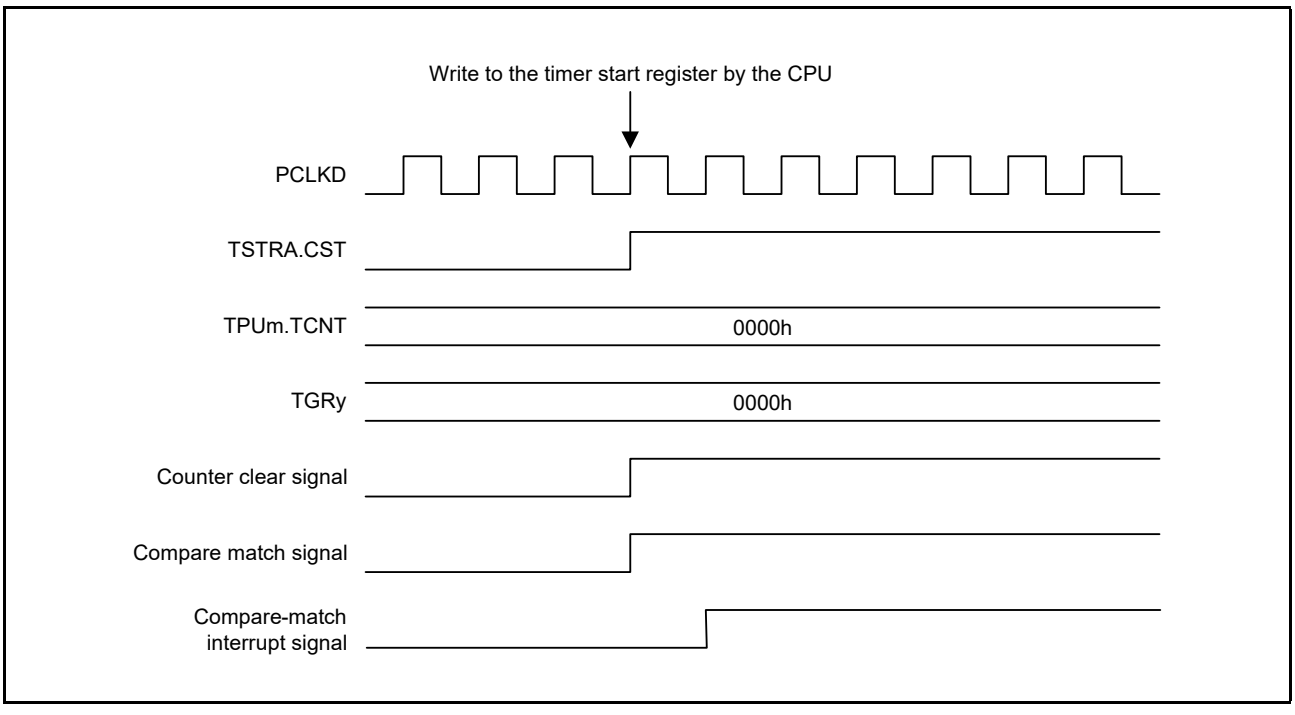


Figure 22.59 Continuous Output of the Interrupt Signal in Response to a Compare Match

22.9.14 Continuous Output of Interrupt Signal in Response to Input Capture

When input-capture signal is set on both edges and when the pulse width of the input-capture input equals to one PCLKD cycle detected by internal sampling, input capture is generated continuously on the rising and falling edges. Therefore, the interrupt signal will be output continuously (i.e. its level will be flat) rather than output over a single cycle. Consequently, interrupts will not be detected in response to second and subsequent input capture.
Figure 22.60 shows the timing for continuous output of the interrupt signal in response to input capture.

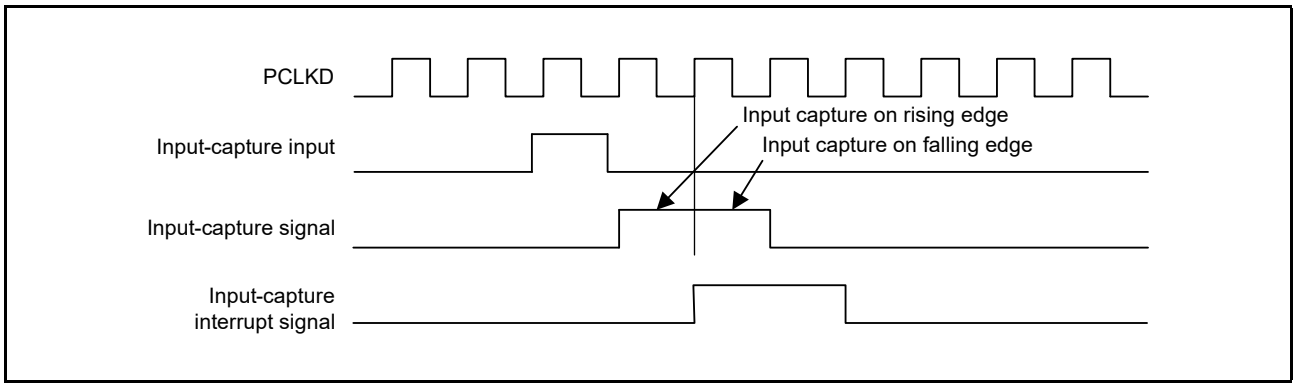


Figure 22.60 Continuous Output of the Interrupt Signal in Response to Input Capture

22.9.15 Continuous Output of Interrupt Signal in Response to Underflow

If two external clock signals' same direction edges to be phase counted are generated within two PCLKD cycles in phase counting mode 1, with TGRy being 0000h, and compare match set as the counter clear source, the TPUm.TCNT counter remains 0000h, and a compare-match interrupt signal and an underflow interrupt signal are output continuously to form a flat signal level (y = A to D, m = 1, 2, 4, 5, 7, 8, 10, 11). Consequently, interrupts will not be detected in response to second and subsequent compare match and underflow.

Figure 22.61 shows the timing for continuous output of the interrupt signal in response to underflow.

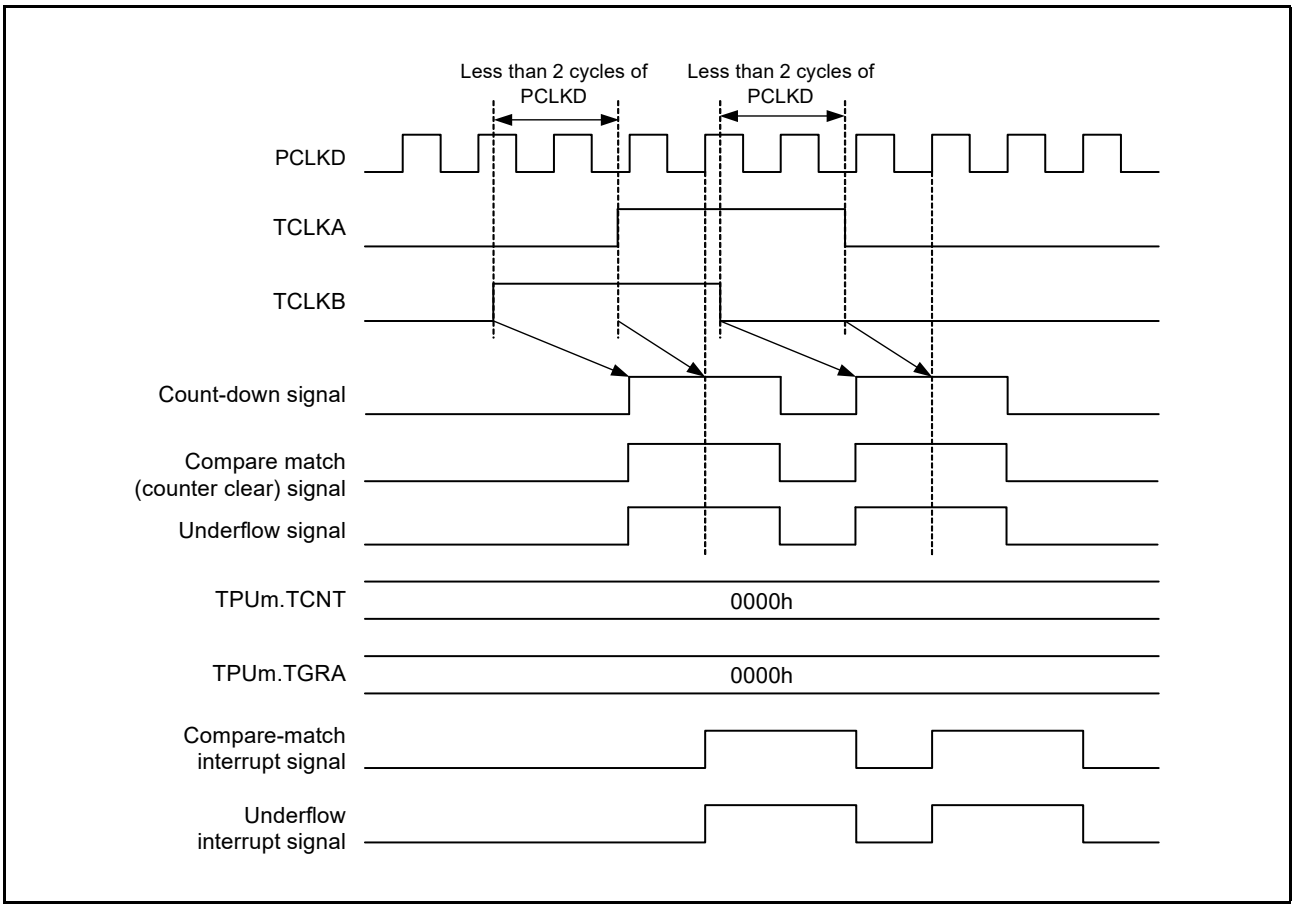


Figure 22.61 Continuous Output of the Interrupt Signal in Response to Underflow

22.9.16 Input Capture Operation in Cascaded Operation

When two 16-bit counters are cascade-connected, with the counter for the 16 higher-order bits (TPUm.TCNT; m = 1, 4, 7, 10) and the counter for the 16 lower-order bits TPUn.TCNT (n = 2, 5, 8, 11) being used together to form a 32-bit counter, if a rising edge is input to the TIOCAm and TIOCAn pins simultaneously, the value of the 16 higher-order bits is transferred to the TPUm.TGRA register and that of the 16 lower-order bits is transferred to the TPUn.TGRA register. However, even when a rising edge is input to the TIOCA1 and TIOCA2 pins simultaneously, the timing for capturing the 16 higher- and 16 lower-order bits may differ by one clock cycle due to the difference between the delays until they are latched within the LSI chip.

If such a difference coincides with an overflow of the lower-order 16-bit counter so that the value of the 32- bit counter is changing from 0000 FFFFh or 0001 0000h, while the actual value of the counter at the time of capture is 0000 FFFFh or 0001 0000h, the actual captured value may be 0000 0000h or 0001 FFFFh.

Accordingly, with input capture while the counters are in use as a 32-bit counter, if the value of the lower-order 16-bit counter when the values may deviate in the way described is 0000h or FFFFh, take care to handle processing for invalidation, for example, discarding the captured value.

Alternatively, use MTU3a, which has functionality for simultaneous input capture by two 16-bit timers cascaded to form a 32-bit timer in response to a single input trigger. For details, see section 19.6.21, Simultaneous Input Capture in MTU1.TCNT and MTU2.TCNT in Cascade Connection.

22.10 Link Operation (Unit 0 Only)

22.10.1 Transmitting an Event Signal to ELC

The TPU (unit 0) uses the ELC (event link controller) to perform link operation to the previously specified module using the interrupt request signal as the event signal.
The event signal can be output regardless of the setting of the interrupt request enable bits (TGIEA, TGIEB, TGIEC, or TGIED, and TCIEV, or TCIEU) of the corresponding TIER0 register.
Table 22.32 lists the event signals that can be transmitted through the respective channels.

Table 22.32 Ability of Interrupt Sources to Serve as Event Signals for Transmission to the ELC

Channel No.	Compare match A	Compare match B	Compare match C	Compare match D	Overflow	Underflow
Channel 0	√	√	√	√	√	—*1
Channel 1	√	√	—*2	—*2	√	√
Channel 2	√	√	—*2	—*2	√	√
Channel 3	√	√	√	√	√	—*1

√: Possible
—: Not possible
Note 1. Channels 0 and 3 do not have these interrupt request signals since they will never underflow.
Note 2. Channels 1 and 2 do not have these interrupt request signals since they do not have TGRC and TGRD registers.

22.10.2 Receiving an Event Signal from ELC

The TPU (unit 0) can perform any of the following three operations using the event link setting register of the ELC (event link controller).

(1) Start Counting

When an event signal is received while the TPU count start operation is selected by the ELOPF register of the ELC, the CSTn bit in TSTRA (the timer start register) is set to 1 and counting starts.
However, if this event is generated for the channels when the CSTn bit is set to 1, the event is ignored.
Table 22.33 lists the CSTn bits in TSTR used for each channel.
Figure 22.62 shows the timing of the count start operation.

For details on the setting procedure to start counting, see section 22.3.1, (1) Counter Operation.

Table 22.33 Correspondence between Channels and CSTn Bits in TSTRA

Channel No.	CSTn Bits in TSTRA
Channel 0	CST0
Channel 1	CST1
Channel 2	CST2
Channel 3	CST3

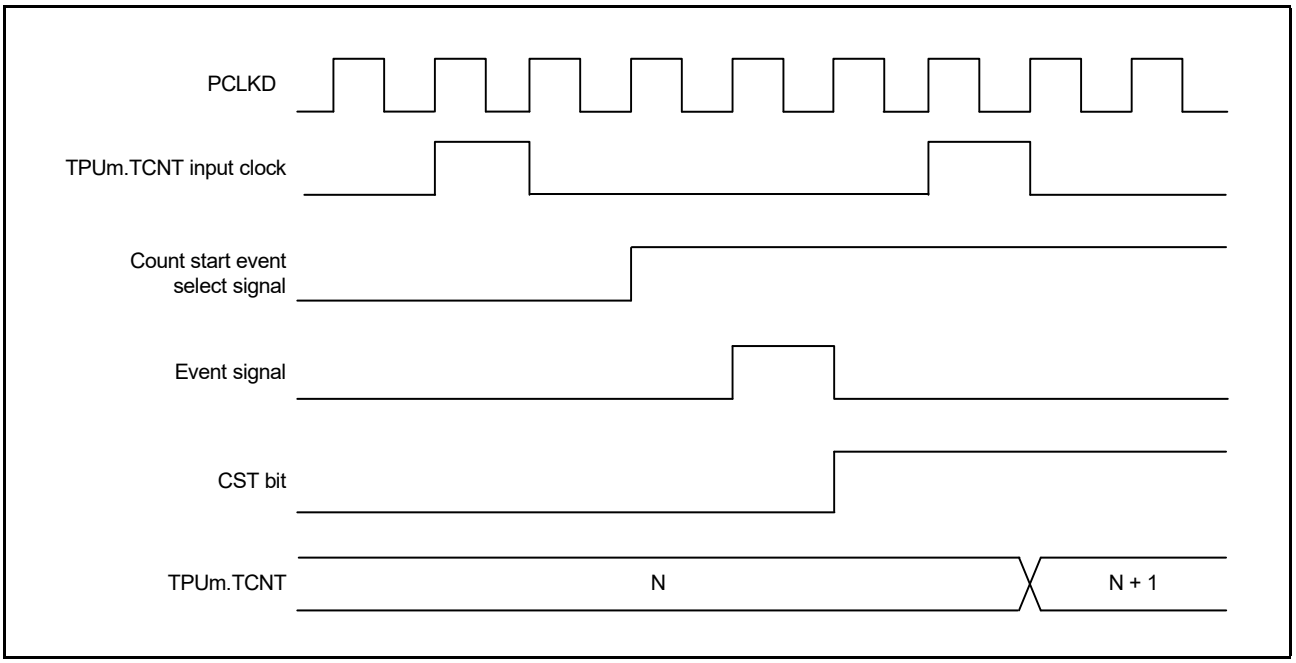


Figure 22.62 Start Counting on Reception of the Event Signal

(2) Clear Counting

Counter clearing operation of a TPU is selected by the ELOPF register of the ELC. When the event specified in the corresponding ELSRn register is generated, the timer counter (TCNT) is returned to its initial value (0000h). Counting continues, however, if the setting of the CSTn bit of the timer start register (TSTRA) is 1 at this time, so counting can be automatically restarted in this way.

Table 22.33 lists the CSTn bits in TSTR used for each channel.

Figure 22.63 shows the timing of the count restart operation.

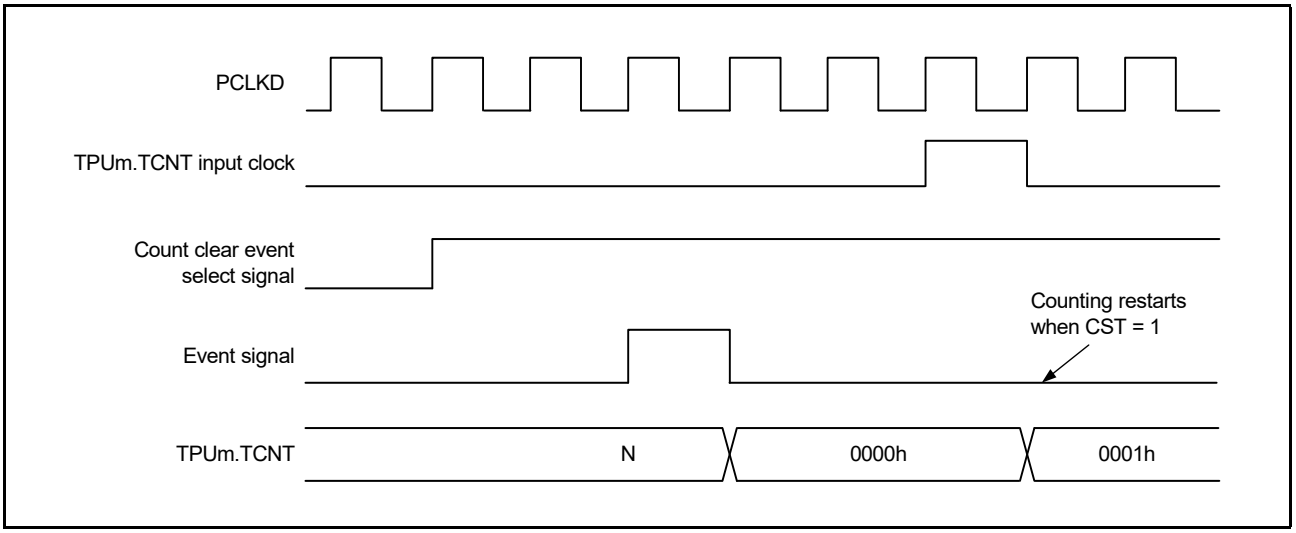


Figure 22.63 Restart Counting on Reception of the Event Signal

(3) Input Capture Operation

When an event signal is received while the TPU input capture operation is selected by the ELOPF register of the ELC, the value of TCNT (the timer counter) of the corresponding channel is captured in TGRA (timer general register A).
When using input capture due to the event link, set the IOA bit in TIOR (the timer I/O control register) to specify input capture, and then set the CSTn bit in TSTRA (the timer start register) to 1 to start counting.
Table 22.34 lists TGRA and TIOR register bits used for each channel. For the CSTn bits in TSTRA used for each channel, see Table 22.33.
Figure 22.64 shows the timing of input capture operation.
When input capture operation due to the event link is selected, the setting of TIOR and the corresponding input capture (the linkage of the TIOCAm pin (input capture pin) input with the specific operation of other channels) are not effective (n = 0 to 11).

For details on the setting procedure for input capture, see section 22.3.1, (3) Input Capture Function.

Table 22.34 TGR and TIOR Used for Input Capture by ELC

Channel No.	Capture Destination Registers	Bits in TIOR
Channel 0	TGRA (channel 0)	IOA[3:0] bits (TIORH0)
Channel 1	TGRA (channel 1)	IOA[3:0] bits (TIOR1)
Channel 2	TGRA (channel 2)	IOA[3:0] bits (TIOR2)
Channel 3	TGRA (channel 3)	IOA[3:0] bits (TIORH3)

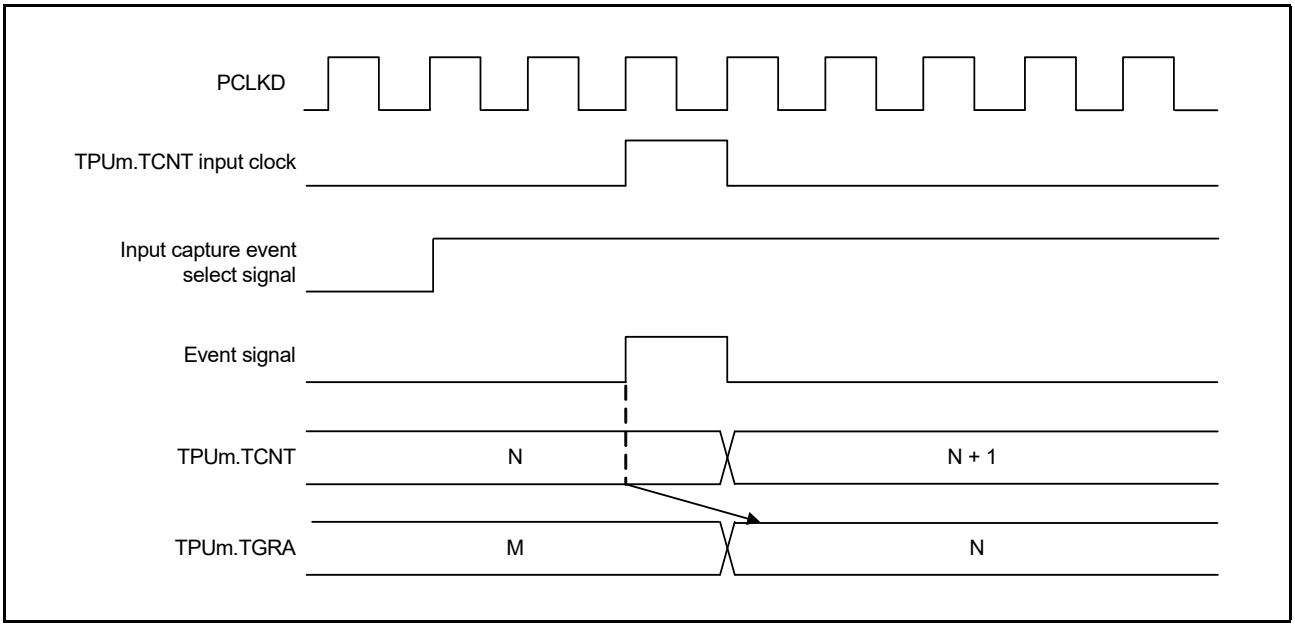


Figure 22.64 Input Capture on Reception of the Event Signal

22.10.3 Usage Notes on Operation on Reception of the Event Link Signal

The followings are the notes on using the TPU (unit 0) for event link operations.

(1) Start Counting

When writing to the CSTn bit in TSTRA (the timer start register) and a counting start are in contention, writing to the CSTn bit does not proceed since setting of the CSTn bit to 1 in response to the event takes priority.
Figure 22.65 shows the timing in this case.
Furthermore, even when a counting start due to the event link is selected, CPU writing to the CSTn bit proceeds if the event signal is at a low level.

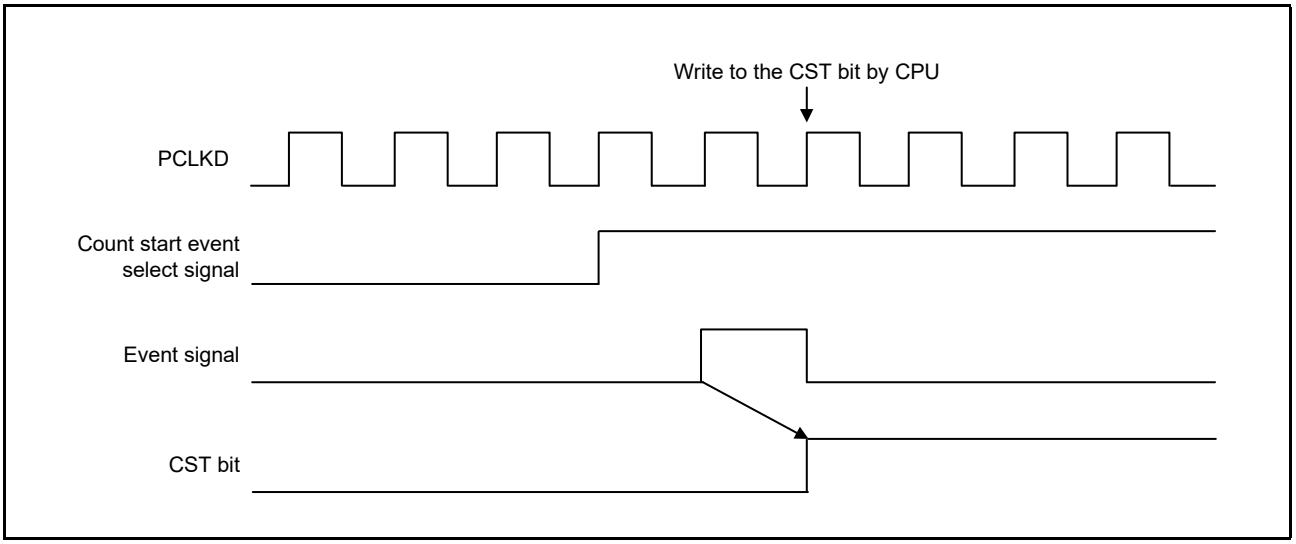


Figure 22.65 Conflict between Writing to the CSTn Bit and Counting Start

(2) Clear Counting

When a TCNT (a timer counter) write cycle and a counting clear are in contention, writing to TCNT does not proceed since the counter value initialization in response to the counting clear takes priority.
Figure 22.66 shows the timing in this case.
Furthermore, even when a counting clear due to the event link is selected, CPU writing to TCNT proceeds if the event signal is at a low level.

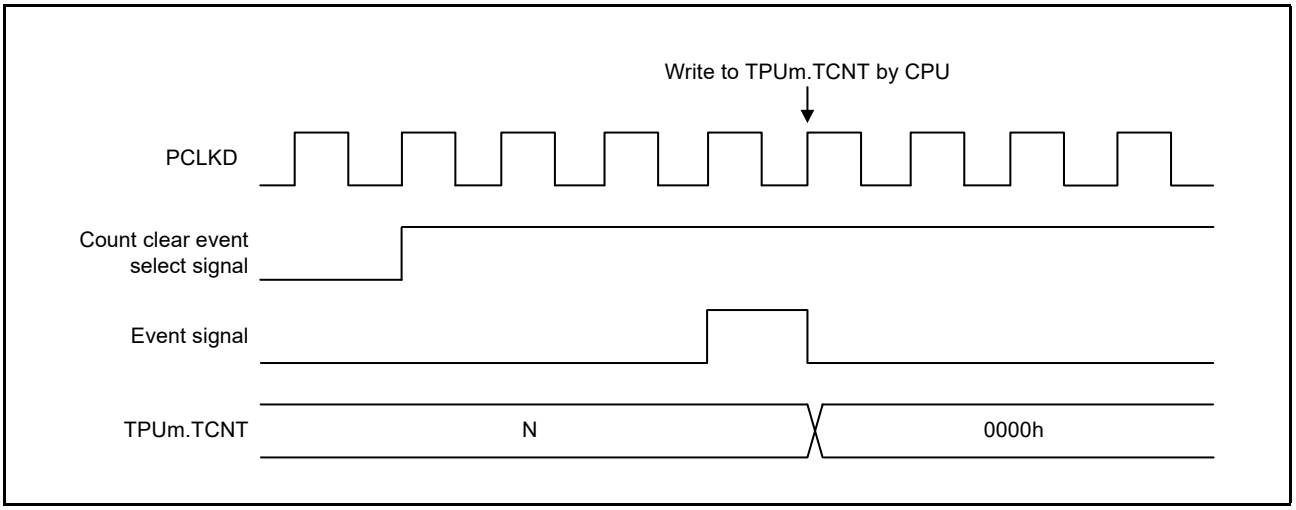


Figure 22.66 Conflict between TCNT Write Cycle and Counting Clear

(3) Input Capture Operation

If a TGRy (the timer general register) read/write cycle and input capture operation are in contention, operation proceeds as follows (y = A to D).

(a) Conflict between TGRy Read Cycle and Input Capture

The internal data bus reads the data before input capture transfer.
Figure 22.67 shows the timing in this case.

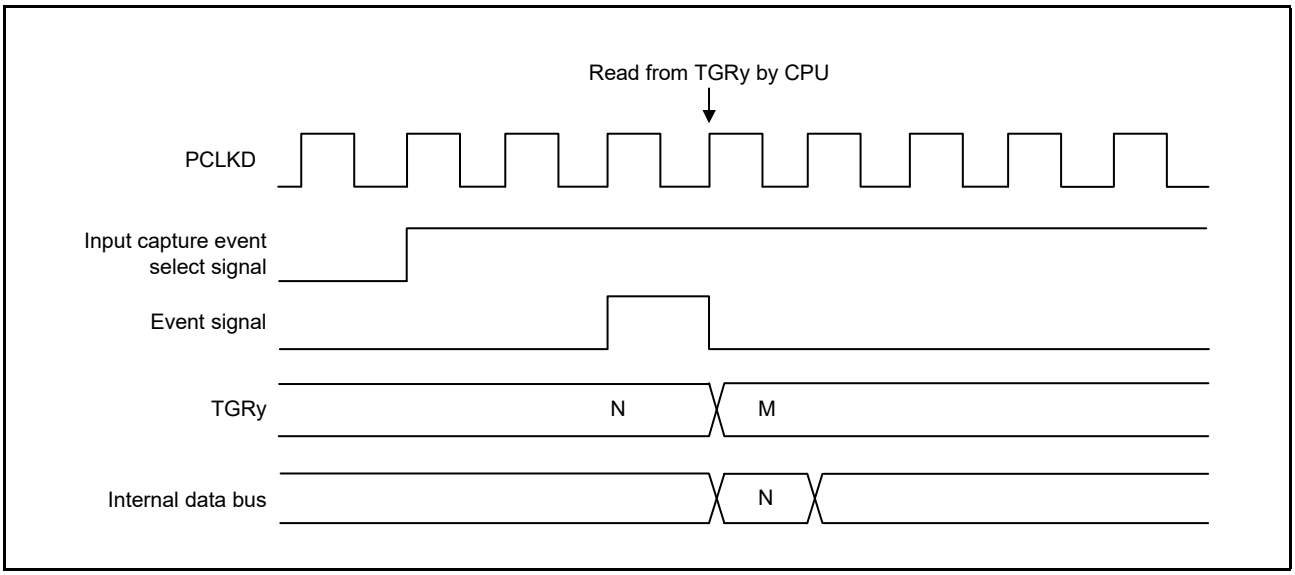


Figure 22.67 Conflict between TGRy Read Cycle and Input Capture Operation

(b) Conflict between TGRy Write Cycle and Input Capture

Writing to TGRy does not proceed since input capture takes priority.
Figure 22.68 shows the timing in this case.
Furthermore, even when input capture operation due to the event link is selected, CPU writing to TGRy proceeds if the event signal is at a low level.

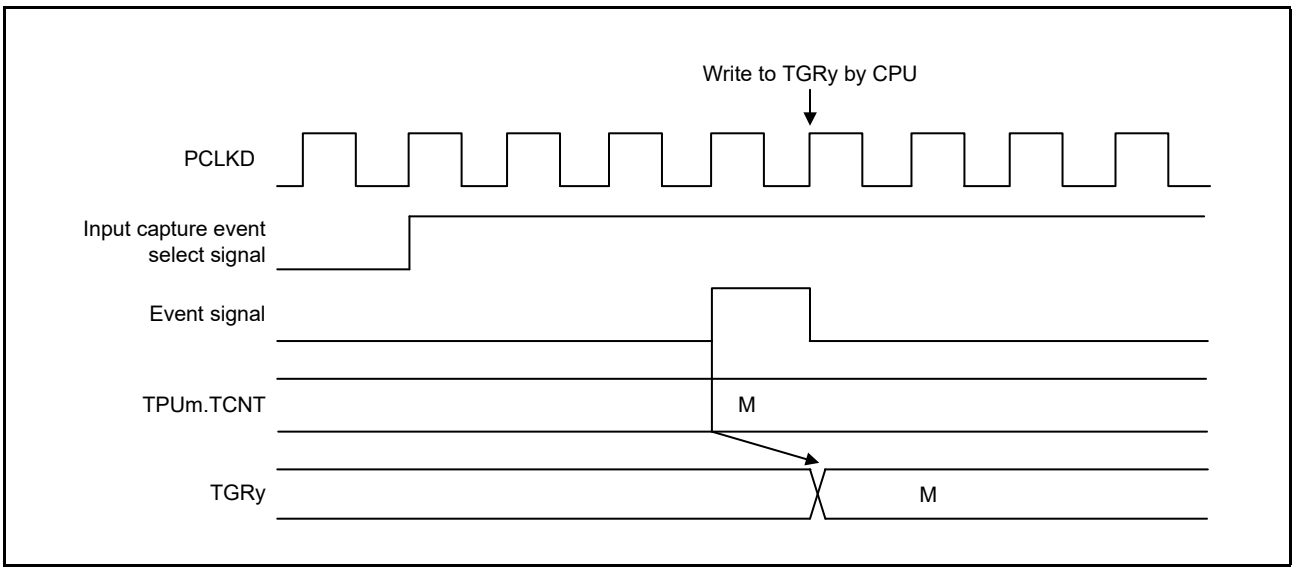


Figure 22.68 Conflict between TGRy Write Cycle and Input Capture Operation

22.10.4 Notes on Transmitting the Event Link Signal

The followings are the notes on transmitting the event link signal.

(1) Transmitting the Compare Match Event Signal

When the TGRy register is set to 0000h, PCLKD/1 is set as the counter clock (TCRn.TPSC[2:0] = 000b), and compare match is set as the trigger for clearing of the counter clock , the value of the TCNT remains 0000h, and the event output signal will be output continuously (i.e. its level will be flat) rather than output over a single cycle (y = A to D).
Figure 22.69 shows the timing for continuous output of the event output signal in response to a compare match.

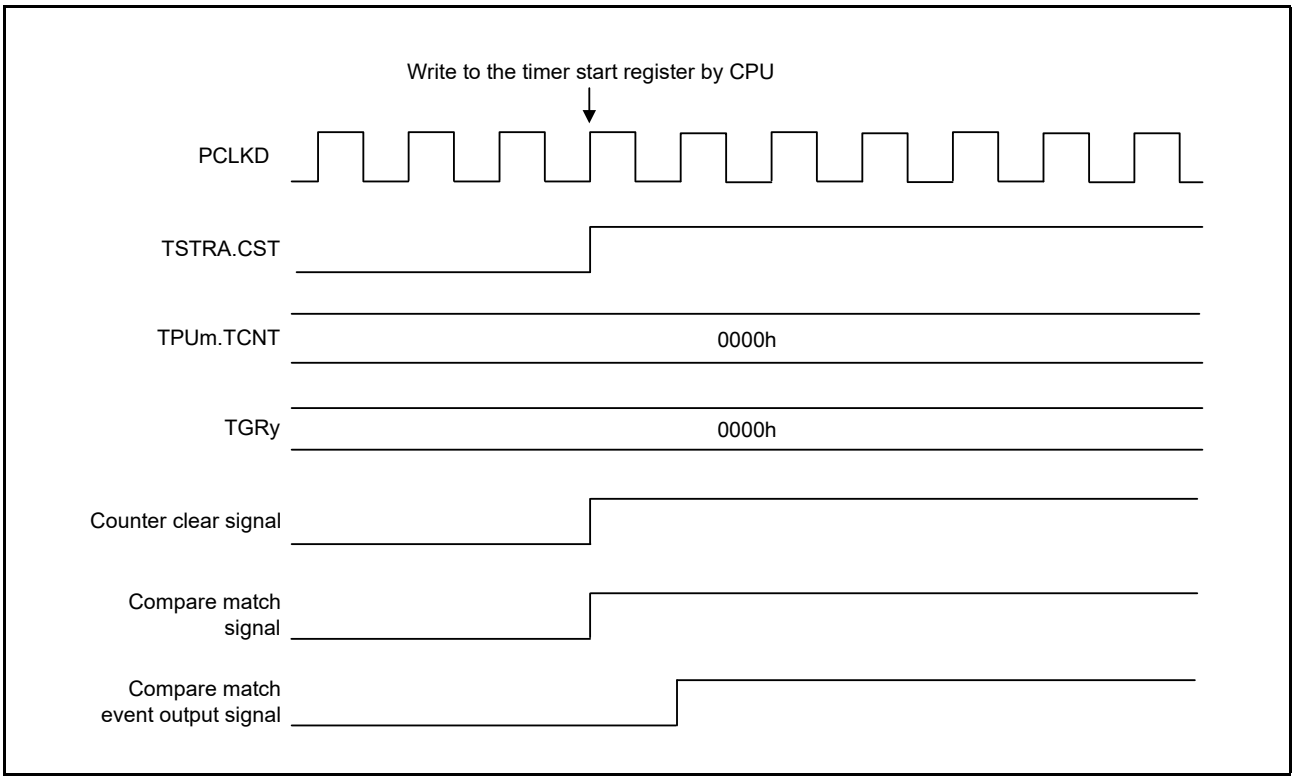


Figure 22.69 Continuous Output of the Compare Match Event Output Signal

(2) Transmitting the Underflow Event Signal

If two external clock signals' same direction edges to be phase counted are generated within two PCLKD cycles in phase counting mode 1, with TGRy being 0000h, and compare match set as the counter clear source, the TCNT counter remains 0000h, and a compare-match event signal and an underflow event signal are output continuously to form a flat signal level (y = A to D).

Figure 22.70 shows the timing for continuous output of the event output signal in response to underflow.

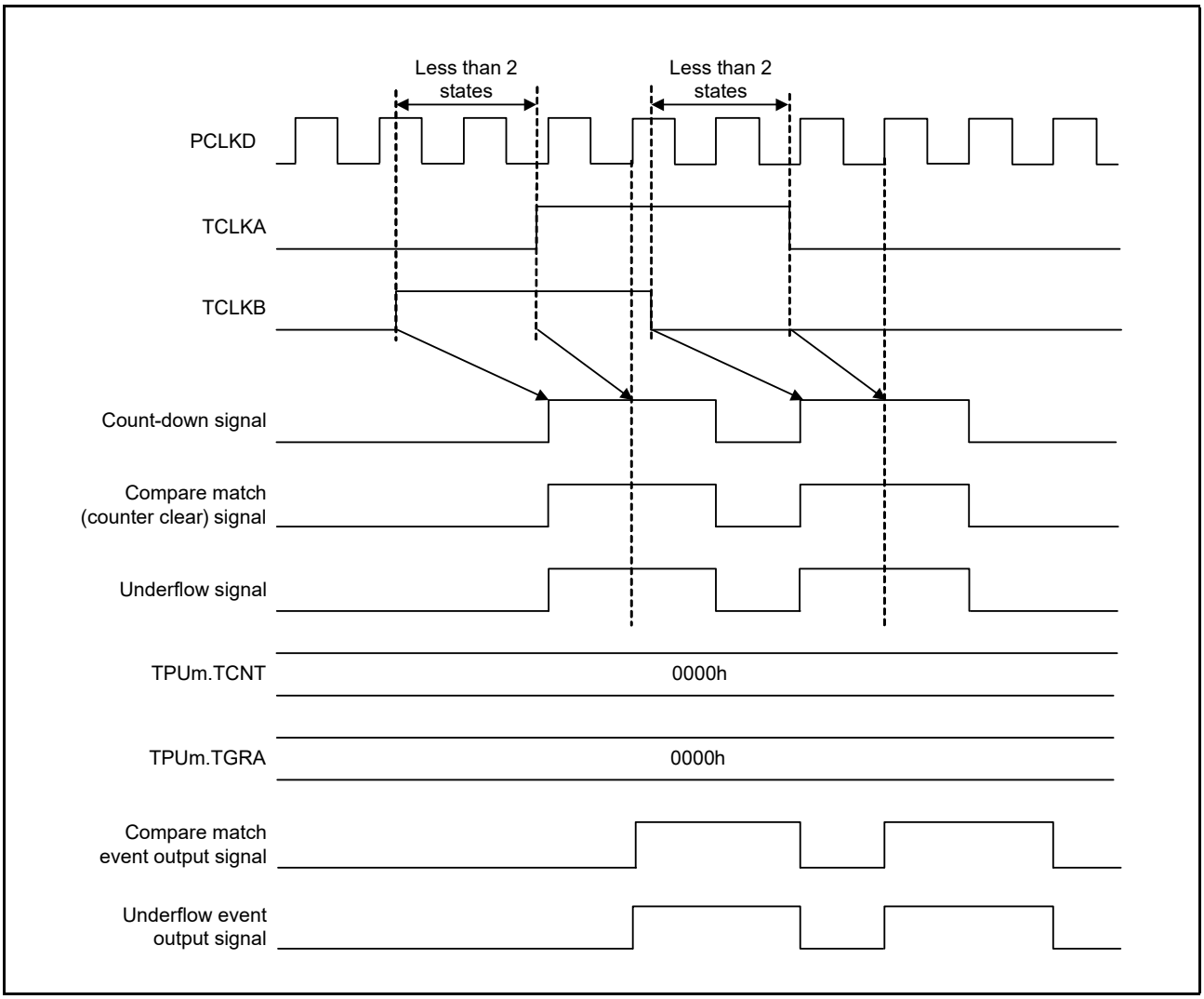


Figure 22.70 Continuous Output of the Underflow Event Output Signal

23. Programmable Pulse Generator (PPG)

The programmable pulse generator (PPG) generates pulse outputs by using the 16-bit timer pulse unit (TPUa) and the multi-function timer pulse unit 3 (MTU3a) as a time base.
The pulse outputs from the PPGs are divided into 4-bit groups, and one PPG unit has four groups (16 bits) of pulse output pins.
Individual pulse output groups can operate all simultaneously and independently.
This LSI has two internal PPG units (PPG0 and PPG1).

23.1 Overview

Table 23.1 lists the specifications of the PPG and Table 23.2 lists PPG functions.
Figure 23.1 shows a block diagram of the PPG.

Table 23.1 Specifications of PPG

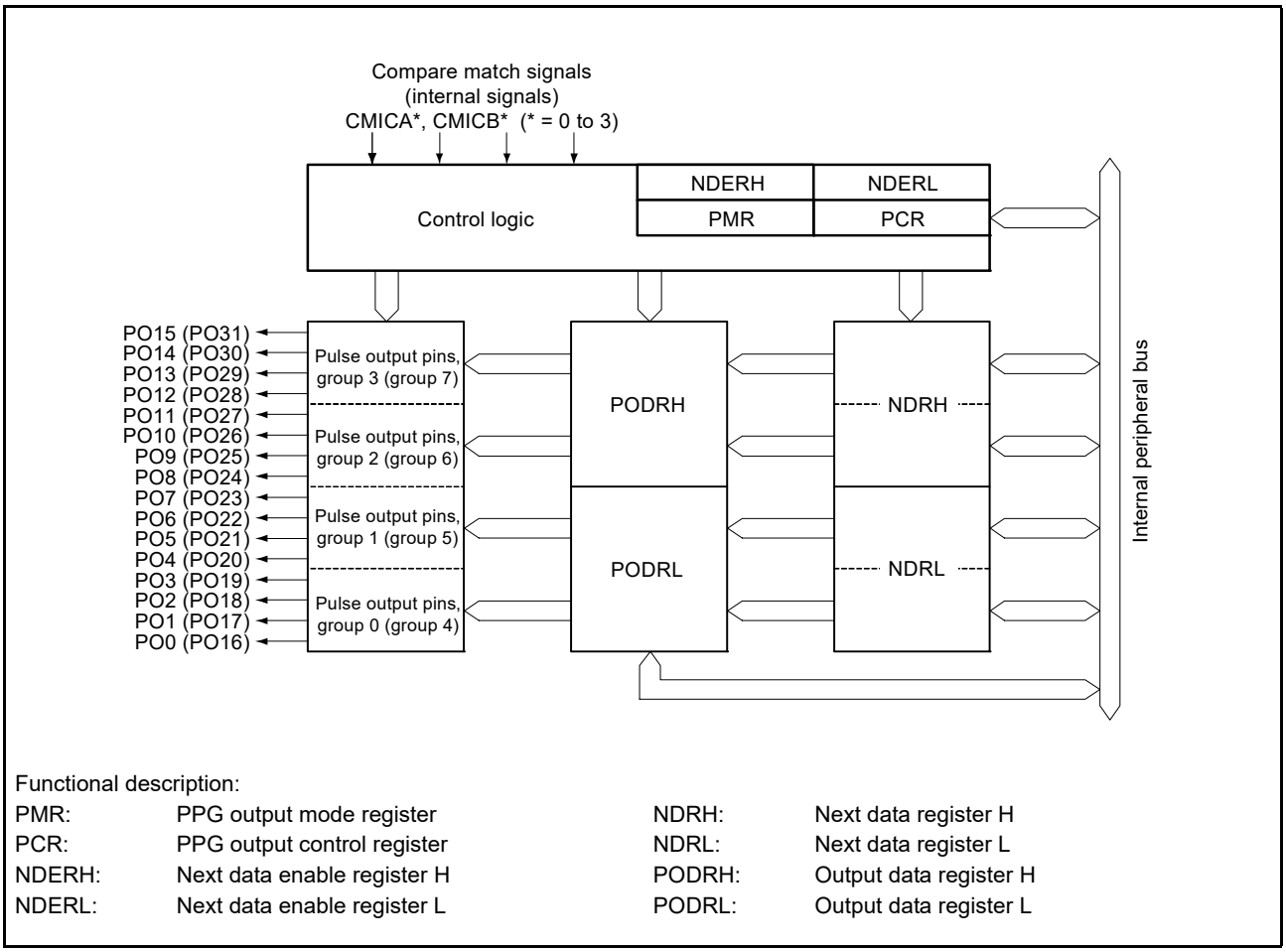
Item	Specifications
Number of output bits	Up to 32 bits (Two units are used. Up to 16 bits per unit.)*1
Pulse output	• Two units, each capable of output through four pin groups • Output trigger signals are selectable. • Non-overlapping operation is possible. • Inverted output is selectable.
Output data transfer	Can operate together with the DMAC (when TPUa (unit 0) and MTU3a interrupts are in use)
Power consumption reducing function	Module-stop state can be set for each unit.

Note 1. One unit for 176-pin devices (only unit 0 is provided)

Table 23.2 Functions of the PPG

Item			PPG0	PPG1
PPG output trigger	MTU3a channels 0 to 3 (MTU0 to MTU3)	Compare match	√	√
		Input capture	√	√
	TPUa (unit 0) channels 0 to 3 (TPU0 to TPU3)	Compare match	—	√
		Input capture	—	√
Non-overlapping operation			√	√
Output data transfer	DMAC		√	√
Selecting inverted output			√	√
Setting the module-stop state*1			The MSTPCRA6 bit in MSTPCRA	The MSTPCRA5 bit in MSTPCRA

Legend:
√: Possible
—: Not possible
Note 1. For details, see section 9, Low-Power Consumption Function.



Functional description:

PMR:	PPG output mode register	NDRH:	Next data register H
PCR:	PPG output control register	NDRL:	Next data register L
NDERH:	Next data enable register H	PODRH:	Output data register H
NDERL:	Next data enable register L	PODRL:	Output data register L

Figure 23.1 Block Diagram of PPG

Table 23.3 lists the pin configuration of the PPG.

Table 23.3 Pin Configuration of the PPG

Unit	Pin Name	I/O	Function
PPG0	PO0	Output	Group 0 pulse output
	PO1	Output	
	PO2	Output	
	PO3	Output	
	PO4	Output	Group 1 pulse output
	PO5	Output	
	PO6	Output	
	PO7	Output	
	PO8	Output	Group 2 pulse output
	PO9	Output	
	PO10	Output	
	PO11	Output	
	PO12	Output	Group 3 pulse output
	PO13	Output	
	PO14	Output	
	PO15	Output	
PPG1	PO16	Output	Group 4 pulse output
	PO17	Output	
	PO18	Output	
	PO19	Output	
	PO20	Output	Group 5 pulse output
	PO21	Output	
	PO22	Output	
	PO23	Output	
	PO24	Output	Group 6 pulse output
	PO25	Output	
	PO26	Output	
	PO27	Output	
	PO28	Output	Group 7 pulse output
	PO29	Output	
	PO30	Output	
	PO31	Output	

23.2 Register Descriptions

23.2.1 PPG Trigger Select Register (PTRSLR)

The PTRSLR register selects the trigger input for PPG (unit 1) from the multi-function timer pulse unit 3 (MTU3a) or from unit 0 of the 16-bit timer pulse unit (TPUa).

Address(es): PPG1: A008 0520h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PTRSL
Value after reset:	0	0	0	0	0	0	0	1

- PTRSLR

Bit	Symbol	Bit Name	Description	R/W
b0	PTRSL	PPG Trigger Select	Selects the output trigger channels for PPG1 from the set of MTU0 to MTU3, or from the set of TPU0 to TPU3. 0: Selects the set of MTU0 to MTU3 as the trigger channels for PPG1. 1: Selects the set of TPU0 to TPU3 as the trigger channels for PPG1.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

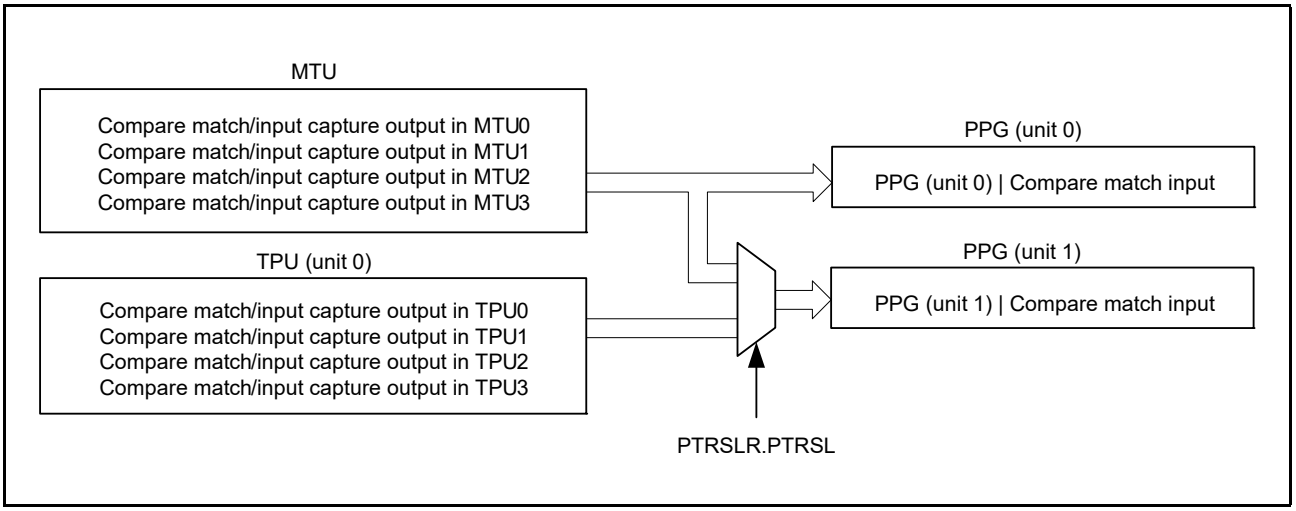


Figure 23.2 Block Diagram of PPG Trigger Selection

23.2.2 Next Data Enable Registers H (NDERH) Next Data Enable Registers L (NDERL)

The NDERH and NDERL registers select the pins (PO15 to PO8) and pins (PO7 to PO0), respectively, for outputs of pulse on a bit-by-bit basis. By setting the bits corresponding to individual pins so that data transfer is enabled, pulse output is enabled for the pins.

Address(es): PPG0: A008 0508h
PPG1: A008 0518h

	b7	b6	b5	b4	b3	b2	b1	b0
NDERH	NDER 15	NDER 14	NDER 13	NDER 12	NDER 11	NDER 10	NDER9	NDER8
Value after reset:	0	0	0	0	0	0	0	0

Address(es): PPG0: A008 0509h, PPG1: A008 0519h

	b7	b6	b5	b4	b3	b2	b1	b0
NDERL	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0
Value after reset:	0	0	0	0	0	0	0	0

- NDERH

Bit	Symbol	Bit Name	Description	R/W
b0	NDER8	Next Data Transfer Enable	0: Data transfer is disabled. 1: Data transfer is enabled.	R/W
b1	NDER9	Next Data Transfer Enable		R/W
b2	NDER 10	Next Data Transfer Enable		R/W
b3	NDER 11	Next Data Transfer Enable		R/W
b4	NDER 12	Next Data Transfer Enable		R/W
b5	NDER 13	Next Data Transfer Enable		R/W
b6	NDER 14	Next Data Transfer Enable		R/W
b7	NDER 15	Next Data Transfer Enable		R/W

NDER8 to NDER15 Bits (Next Data Transfer Enable)

When these bits are set to 1, if the trigger selected in PCR occurs, data is transferred from the corresponding bit in NDRH to the bit in PODRH. When these bits are set to 0, the data is not transferred from NDRH to PODRH.

- NDERL

Bit	Symbol	Bit Name	Description	R/W
b0	NDER0	Next Data Transfer Enable	0: Data transfer is disabled. 1: Data transfer is enabled.	R/W
b1	NDER1	Next Data Transfer Enable		R/W
b2	NDER2	Next Data Transfer Enable		R/W
b3	NDER3	Next Data Transfer Enable		R/W
b4	NDER4	Next Data Transfer Enable		R/W
b5	NDER5	Next Data Transfer Enable		R/W
b6	NDER6	Next Data Transfer Enable		R/W
b7	NDER7	Next Data Transfer Enable		R/W

NDER0 to NDER7 Bits (Next Data Transfer Enable)

When these bits are set to 1, if the trigger selected in PCR occurs, data is transferred from the corresponding bit in NDRL to the bit in PODRL. When these bits are set to 0, the data is not transferred from NDRL to PODRL.

23.2.3 Output Data Registers H (PODRH) Output Data Registers L (PODRL)

The PODRH and PODRL registers store the values output from the pins for pulse output (PO15 to PO8, PO7 to PO0). When an output trigger is generated, the values of bits for which data transfer is enabled in the NDERH register are transferred from the NDRH register to the corresponding bits in the PODRH register. In the same way, the values of bits for which data transfer is enabled in the NDERL register are transferred from the NDRL register to the corresponding bits in the PODRL register.

Address(es): PPG0: A008 050Ah
PPG1: A008 051Ah

	b7	b6	b5	b4	b3	b2	b1	b0
PODRH	POD15	POD14	POD13	POD12	POD11	POD10	POD9	POD8
Value after reset:	0	0	0	0	0	0	0	0

Address(es): PPG0: A008 050Bh
PPG1: A008 051Bh

	b7	b6	b5	b4	b3	b2	b1	b0
PODRL	POD7	POD6	POD5	POD4	POD3	POD2	POD1	POD0
Value after reset:	0	0	0	0	0	0	0	0

- PODRH

Bit	Symbol	Bit Name	Description	R/W
b0	POD8	Output Data Register	0: The low level is output on the POi pin. 1: The high level is output on the POi pin. (i = 15 to 8)	R/W
b1	POD9	Output Data Register		R/W
b2	POD10	Output Data Register		R/W
b3	POD11	Output Data Register		R/W
b4	POD12	Output Data Register		R/W
b5	POD13	Output Data Register		R/W
b6	POD14	Output Data Register		R/W
b7	POD15	Output Data Register		R/W

POD8 to POD15 Bit (Output Data Register)

When an output trigger is generated during PPG operation, the values of bits for which data transfer is enabled in the NDERH register are transferred from the NDRH register to the corresponding bits in this register. Writing from the CPU to this register is impossible while NDERH is set to 1. The initial output level for the pulse signal can be set when the value in the NDERH register is 0.

- PODRL

Bit	Symbol	Bit Name	Description	R/W
b0	POD0	Output Data Register	0: The low level is output on the POi pin. 1: The high level is output on the POi pin. (i = 7 to 0)	R/W
b1	POD1	Output Data Register		R/W
b2	POD2	Output Data Register		R/W
b3	POD3	Output Data Register		R/W
b4	POD4	Output Data Register		R/W
b5	POD5	Output Data Register		R/W
b6	POD6	Output Data Register		R/W
b7	POD7	Output Data Register		R/W

POD0 to POD7 Bit (Output Data Register)

When an output trigger is generated during PPG operation, the values of bits for which data transfer is enabled in the NDERL register are transferred from the NDRL register to the corresponding bits in this register. Writing from the CPU to this register is impossible while the NDERL register is set to 1. The initial output level for the pulse signal can be set when the value in the NDERL register is 0.

23.2.4 Next Data Registers H (NDRH) Next Data Registers L (NDRL)

The NDRH and NDRL registers store the next data to be output from the pins for pulse output (PO15 to PO8, PO7 to PO0).

Address(es): PPG0: NDRH A008 050Ch, NDRH2 A008 050Eh
PPG1: NDRH A008 051Ch, NDRH2 A008 051Eh

	b7	b6	b5	b4	b3	b2	b1	b0
NDRH	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8
Value after reset:	0	0	0	0	0	0	0	0

Address(es): PPG0: NDRL A008 050Dh, NDRL2 A008 050Fh
PPG1: NDRL A008 051Dh, NDRL2 A008 051Fh

	b7	b6	b5	b4	b3	b2	b1	b0
NDRL	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0
Value after reset:	0	0	0	0	0	0	0	0

- NDRH

The NDRH address differs depending on whether the same output trigger signal is set or different output trigger signals are set for pulse output groups in the PCR register.

(1) When pulse output groups 2 and 3 have the same output trigger signal
If pulse output groups 2 and 3 have the same output trigger signal, all eight bits in the NDRH register are mapped to the same address*1 and can be accessed at one time.

- PPG0: NDRH A008 050Ch (groups 2 and 3 are mapped)
- PPG1: NDRH A008 051Ch (groups 6 and 7 are mapped)

Bit	Symbol	Bit Name	Description	R/W
b0	NDR8	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRH.	R/W
b1	NDR9	Next Data Register		R/W
b2	NDR10	Next Data Register		R/W
b3	NDR11	Next Data Register		R/W
b4	NDR12	Next Data Register		R/W
b5	NDR13	Next Data Register		R/W
b6	NDR14	Next Data Register		R/W
b7	NDR15	Next Data Register		R/W

Note 1. The address (PPG0: NDRH2 A008 050Eh, PPG1: NDRH2 A008 051Eh) to which NDRH address has not been assigned is read as FFh. Writing to this address is ignored.

(2) When pulse output groups 2 and 3 have different output trigger signals

If pulse output groups 2 and 3 have different output trigger signals, upper 4 bits and lower 4 bits are mapped to the different addresses.

- PPG0: NDRH A008 050Ch (group 3 is mapped)
- PPG1: NDRH A008 051Ch (group 7 is mapped)

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b4	NDR12	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRH.	R/W
b5	NDR13	Next Data Register		R/W
b6	NDR14	Next Data Register		R/W
b7	NDR15	Next Data Register		R/W

- PPG0: NDRH2 A008 050Eh (group 2 is mapped)
- PPG1: NDRH2 A008 051Eh (group 6 is mapped)

Bit	Symbol	Bit Name	Description	R/W
b0	NDR8	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRH.	R/W
b1	NDR9	Next Data Register		R/W
b2	NDR10	Next Data Register		R/W
b3	NDR11	Next Data Register		R/W
b7 to b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

- NDRL

The NDRL address differs depending on whether the same output trigger signal is set or different output trigger signals are set for pulse output groups in the PCR register.

(1) When pulse output groups 0 and 1 have the same output trigger signal

If pulse output groups 0 and 1 have the same output trigger signal, all eight bits in the NDRL register are mapped to the same address*1 and can be accessed at one time.

- PPG0: NDRL A008 050Dh (groups 0 and 1 are mapped)
- PPG1: NDRL A008 051Dh (groups 4 and 5 are mapped)

Bit	Symbol	Bit Name	Description	R/W
b0	NDR0	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRL.	R/W
b1	NDR1	Next Data Register		R/W
b2	NDR2	Next Data Register		R/W
b3	NDR3	Next Data Register		R/W
b4	NDR4	Next Data Register		R/W
b5	NDR5	Next Data Register		R/W
b6	NDR6	Next Data Register		R/W
b7	NDR7	Next Data Register		R/W

Note 1. The address (PPG0: NDRL2 A008 050Fh: PPG1: NDRL2 A008 051Fh) to which NDRL address has not been assigned is read as FFh. Writing to this address is ignored.

(2) When pulse output groups 0 and 1 have different output trigger signals

If pulse output groups 0 and 1 have different output trigger signals, upper 4 bits and lower 4 bits are mapped to the different addresses.

- PPG0: NDRL A008 050Dh (group 1 is mapped)
- PPG1: NDRL A008 051Dh (group 5 is mapped)

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b4	NDR4	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRL.	R/W
b5	NDR5	Next Data Register		R/W
b6	NDR6	Next Data Register		R/W
b7	NDR7	Next Data Register		R/W

- PPG0: NDRL2 A008 050Fh (group 0 is mapped)
- PPG1: NDRL2 A008 051Fh (group 4 is mapped)

Bit	Symbol	Bit Name	Description	R/W
b0	NDR0	Next Data Register	The output trigger signal specified by PCR transfers the values in this register to the corresponding bits in PODRL.	R/W
b1	NDR1	Next Data Register		R/W
b2	NDR2	Next Data Register		R/W
b3	NDR3	Next Data Register		R/W
b7 to b4	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

23.2.5 PPG Output Control Register (PCR)

The PCR register selects the timers for use in pulse output trigger signals and associated channels on a group-by-group basis.

Types of compare match signals for the individual timers in use differ according to the output mode set in the PMR register. For details, see section 23.2.6, PPG Output Mode Register (PMR).

Address(es): PPG0: A008 0506h
PPG1: A008 0516h

	b7	b6	b5	b4	b3	b2	b1	b0
	G3CMS[1:0]		G2CMS[1:0]		G1CMS[1:0]		G0CMS[1:0]	
Value after reset:	1	1	1	1	1	1	1	1

- PPG0.PCR

Bit	Symbol	Bit Name	Description	R/W
b1, b0	G0CMS[1:0]	Group 0 Compare Match Select	b1 b0 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3	R/W
b3, b2	G1CMS[1:0]	Group 1 Compare Match Select	b3 b2 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3	R/W
b5, b4	G2CMS[1:0]	Group 2 Compare Match Select	b5 b4 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3	R/W
b7, b6	G3CMS[1:0]	Group 3 Compare Match Select	b7 b6 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3	R/W

- PPG1.PCR

Bit	Symbol	Bit Name	Description	R/W
b1, b0	G0CMS[1:0]	Group 4 Compare Match Select	• When the PTRSL bit in PPG1.PTRSLR is set to 0. b1 b0 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1. b1 b0 0 0: Compare match in TPU0 0 1: Compare match in TPU1 1 0: Compare match in TPU2 1 1: Compare match in TPU3	R/W
b3, b2	G1CMS[1:0]	Group 5 Compare Match Select	• When the PTRSL bit in PPG1.PTRSLR is set to 0. b3 b2 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1. b3 b2 0 0: Compare match in TPU0 0 1: Compare match in TPU1 1 0: Compare match in TPU2 1 1: Compare match in TPU3	R/W
b5, b4	G2CMS[1:0]	Group 6 Compare Match Select	• When the PTRSL bit in PPG1.PTRSLR is set to 0. b5 b4 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1. b5 b4 0 0: Compare match in TPU0 0 1: Compare match in TPU1 1 0: Compare match in TPU2 1 1: Compare match in TPU3	R/W
b7, b6	G3CMS[1:0]	Group 7 Compare Match Select	• When the PTRSL bit in PPG1.PTRSLR is set to 0. b7 b6 0 0: Compare match in MTU0 0 1: Compare match in MTU1 1 0: Compare match in MTU2 1 1: Compare match in MTU3 • When the PTRSL bit in PPG1.PTRSLR is set to 1. b7 b6 0 0: Compare match in TPU0 0 1: Compare match in TPU1 1 0: Compare match in TPU2 1 1: Compare match in TPU3	R/W

23.2.6 PPG Output Mode Register (PMR)

The PMR register selects the pulse output mode and whether to invert the output or not of the PPG on a group-by-group basis.

While inverted output is selected, a low-level pulse is output to the corresponding pins when the values in PODRH and PODRL are 1, and a high-level pulse is output to the corresponding pins when the values in PODRH and PODRL are 0. In addition, when non-overlapping operation is selected, the programmable pulse generator (PPG) updates its output values on compare match A or B in MTU3a or TPUa that functions as an output trigger.

For details, see section 23.3.4, Non-Overlapping Pulse Output.

Address(es): PPG0: A008 0507h
PPG1: A008 0517h

	b7	b6	b5	b4	b3	b2	b1	b0
	G3INV	G2INV	G1INV	G0INV	G3NOV	G2NOV	G1NOV	G0NOV
Value after reset:	1	1	1	1	0	0	0	0

- PPG0.PMR

Bit	Symbol	Bit Name	Description	R/W
b0	G0NOV	Group 0 Non-Overlap	0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3)	R/W
b1	G1NOV	Group 1 Non-Overlap	0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3)	R/W
b2	G2NOV	Group 2 Non-Overlap	0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3)	R/W
b3	G3NOV	Group 3 Non-Overlap	0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3)	R/W
b4	G0INV	Group 0 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b5	G1INV	Group 1 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b6	G2INV	Group 2 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b7	G3INV	Group 3 Output Polarity Change	0: Inverted output 1: Direct output	R/W

- PPG1.PMR

Bit	Symbol	Bit Name	Description	R/W
b0	G0NOV	Group 4 Non-Overlap	• When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) • When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)	R/W
b1	G1NOV	Group 5 Non-Overlap	• When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) • When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)	R/W
b2	G2NOV	Group 6 Non-Overlap	• When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) • When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)	R/W

Bit	Symbol	Bit Name	Description	R/W
b3	G3NOV	Group 7 Non-Overlap	• When the PPG1.PTRSLR.PTRSL bit is 0 0: Normal operation (Output values updated on compare match A in the selected MTUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected MTUn) (n = 0 to 3) • When the PPG1.PTRSLR.PTRSL bit is 1 0: Normal operation (Output values updated on compare match A in the selected TPUn) (n = 0 to 3) 1: Non-overlapping operation (Output values updated on compare match A or B in the selected TPUn) (n = 0 to 3)	R/W
b4	G0INV	Group 4 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b5	G1INV	Group 5 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b6	G2INV	Group 6 Output Polarity Change	0: Inverted output 1: Direct output	R/W
b7	G3INV	Group 7 Output Polarity Change	0: Inverted output 1: Direct output	R/W

23.3 Operation

Figure 23.3 shows a schematic diagram of the programmable pulse generator (PPG).
Pulse output for individual pins is enabled when the bits corresponding to individual pulse output pins in NDERH and NDERL are set to 1 (data transfer is enabled).
An initial output value is determined by the initial settings (in PODRH and PODRL) corresponding to individual pulse output pins. When the compare match event specified as the output trigger signal by PCR occurs, the output values are updated by transfer of the values in NDRH and NDRL to PODRH and PODRL, respectively.
Consecutive output of up to 16 bits of data per unit is possible by writing new output data to NDRH and NDRL before the next compare match.

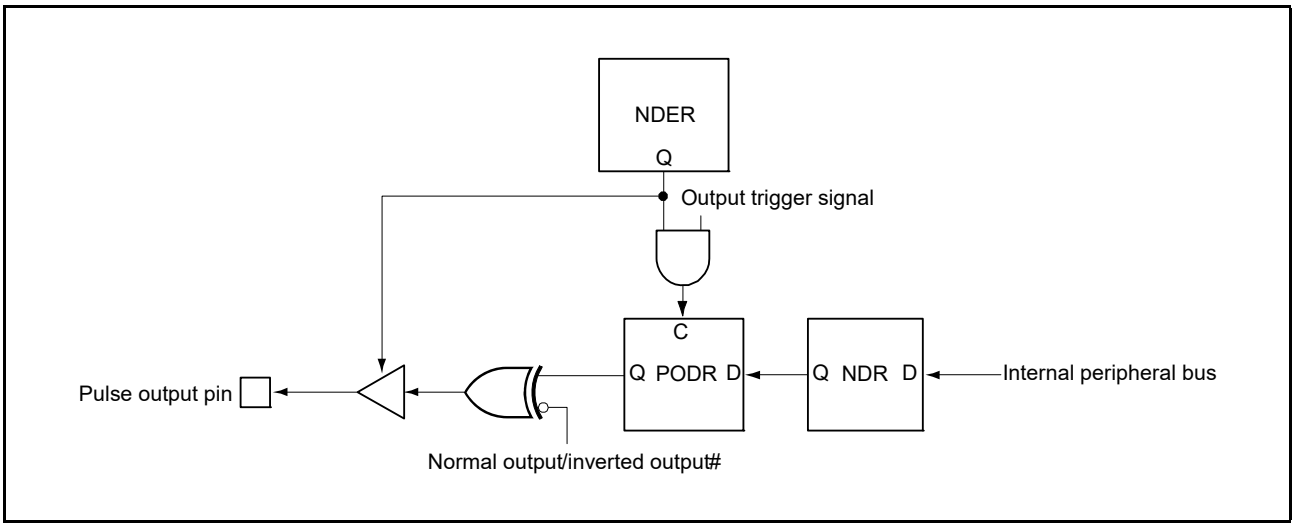


Figure 23.3 Schematic Diagram of PPG

23.3.1 Output Timing

When the selected compare match event occurs while pulse output is enabled, the contents in NDRH and NDRL are transferred to PODRH and PODRL, respectively, and then the values are output on the pulse output pins.
Figure 23.4 shows the timing of the above operation. In this case, the timing when compare match A triggers normal output from groups 2 and 3 is shown.

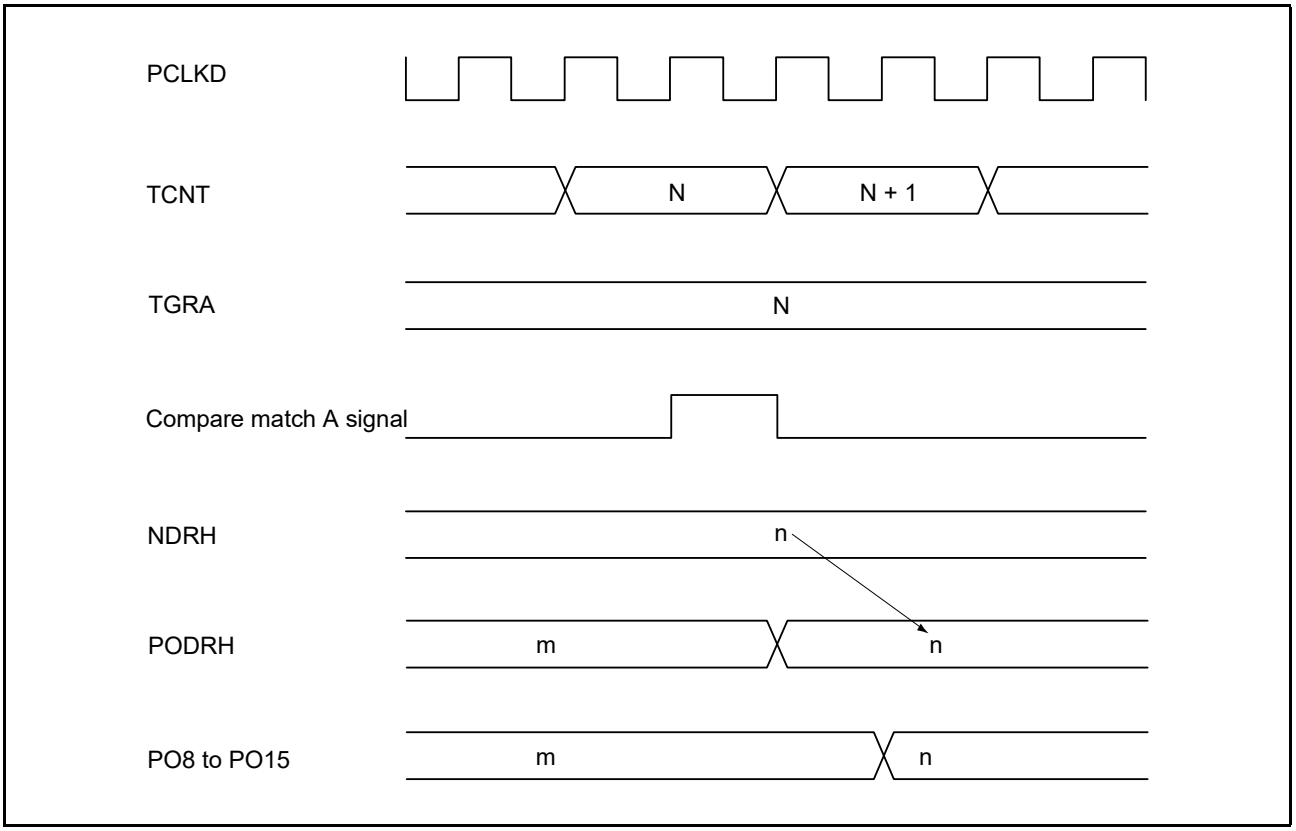


Figure 23.4 Timing of Transfer and Output of the Values in NDR (Example)

23.3.2 Sample Setup Procedure for Normal Pulse Output

Figure 23.5 shows a sample procedure for setting normal pulse output.

(1) PPG Setting

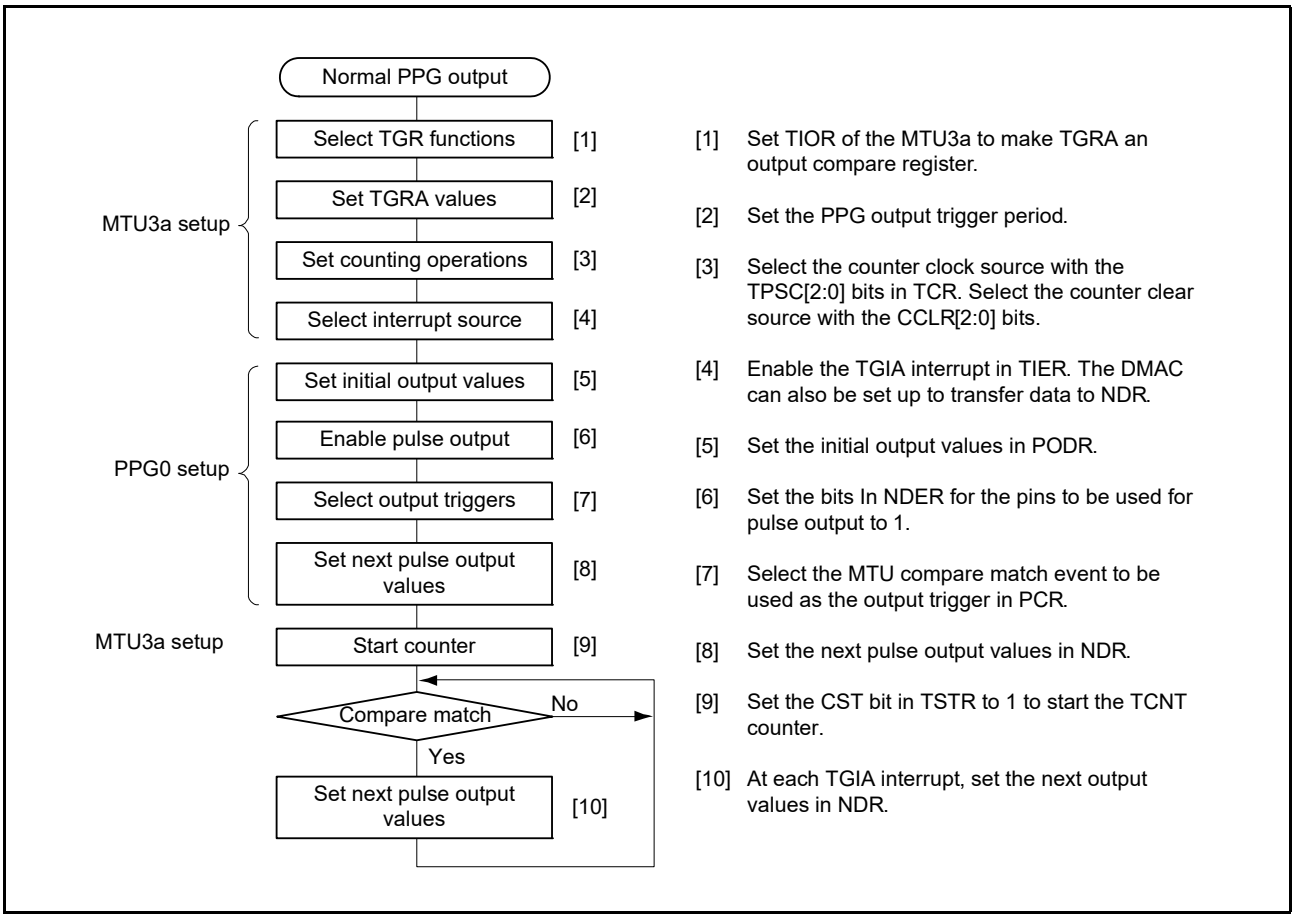


Figure 23.5 Sample Setup Procedure for Normal Pulse Output (PPG Setting)

23.3.3 Example of Normal Pulse Output (Example of Five-Phase Pulse Output)

Figure 23.6 shows an example in which five-phase pulse is output on PPG0 (PO11 to PO15) with MTU1 as the trigger for output.

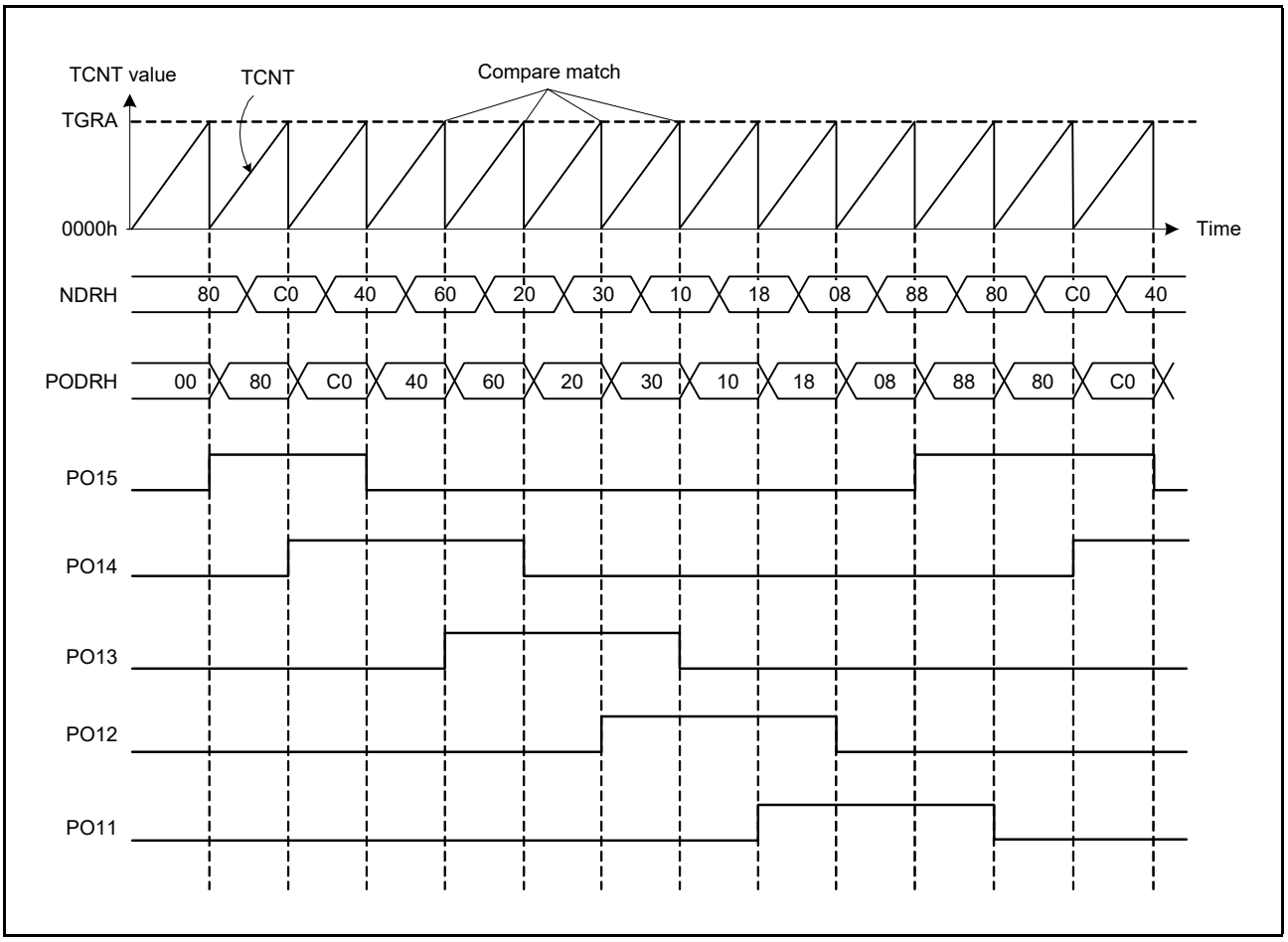


Figure 23.6 Example of Normal Pulse Output (Example of Five-Phase Pulse Output)

1. Set the MTU1.TGRA register to serve as an output compare register for trigger output. Specify the number of counting cycles in the TGRA register and select the counter clearing source as a compare match A by the MTU1.TCR.CCLR bit. Also, set the MTU1.TIER.TGIEA bit to 1 and enable the compare match/input capture A (TGIA1) interrupt request.
2. Write F8h to PPG0.NDERH and select the output triggers for the G3CMS[1:0] and G2CMS[1:0] bits in PPG0.PCR as that specified in step 1, compare match at MTU1. Then, write 80h to PPG0.NDRH as the value for output.
3. The timer counter in the MTU1 starts. When compare match A occurs, the values in PPG0.NDRH are transferred to PPG0.PODRH and output. The TGIA1 interrupt handling routine writes the next output data C0h to NDRH.
4. Five-phase pulse output (one or two phases active at a time) can be obtained subsequently by writing 40h, 60h, 20h, 30h, 10h, 18h, 08h, 88h... at successive TGIA1 interrupts.
   If the DMAC is set for activation by the TGIA1 interrupt, pulse output can be obtained without imposing a load on the CPU.

23.3.4 Non-Overlapping Pulse Output

During non-overlapping operation, data transfer from PPGn.NDRH and PPGn.NDRL to PPGn.PODRH and PPGn.PODRL is performed as follows (n = 0, 1).

- On compare match A, the contents in NDRH and NDRL are always transferred to PODRH and PODRL.
- On compare match B, data transfer proceeds for bits in NDRH and NDRL that have the value 0. It does not proceed for bits having the value 1.

Therefore, compare match B before compare match A allows 0-valued data to be transferred in advance of 1-valued data. In this case, write the next data to NDRH and NDRL from within the TGIAm (m = 0 to 3) interrupt handling routine of MTU3a, and after compare match B occurs, do not change the values in NDRH and NDRL during the interval from compare match B to compare match A (the non-overlap margin).
Figure 23.7 shows the non-overlapping pulse output operation.

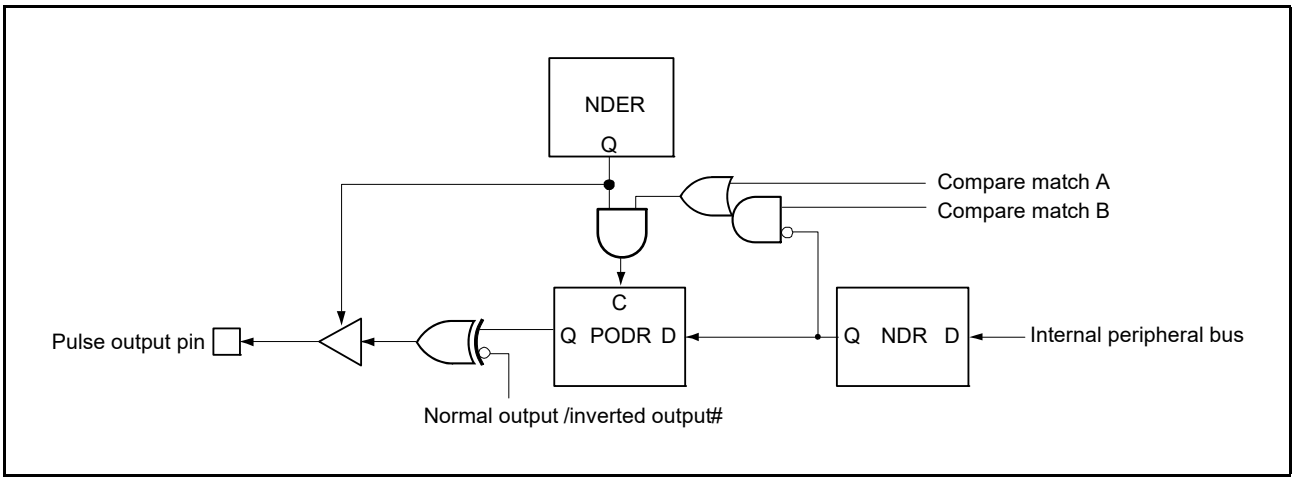


Figure 23.7 Non-Overlapping Pulse Output

Using a TGIAm interrupt to activate transfer by the DMAC can also write the next data to NDRH and NDRL. In any case, the next data must be written before the next compare match B occurs.
Figure 23.8 shows the timing of the above procedure.

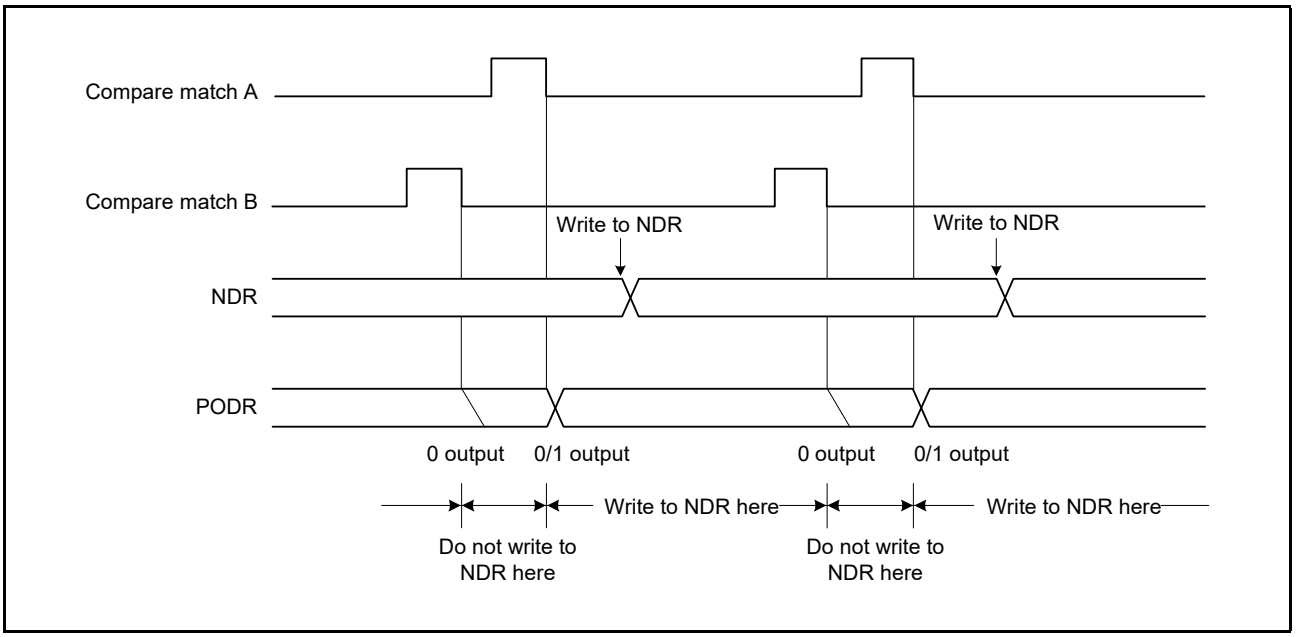


Figure 23.8 Non-Overlapping Operation and Write Timing to PPGn.NDRH and PPGn.NDRL

23.3.5 Sample Setup Procedure for Non-Overlapping Pulse Output

Figure 23.9 shows a sample procedure for setting up non-overlapping pulse output.

(1) PPG Setting

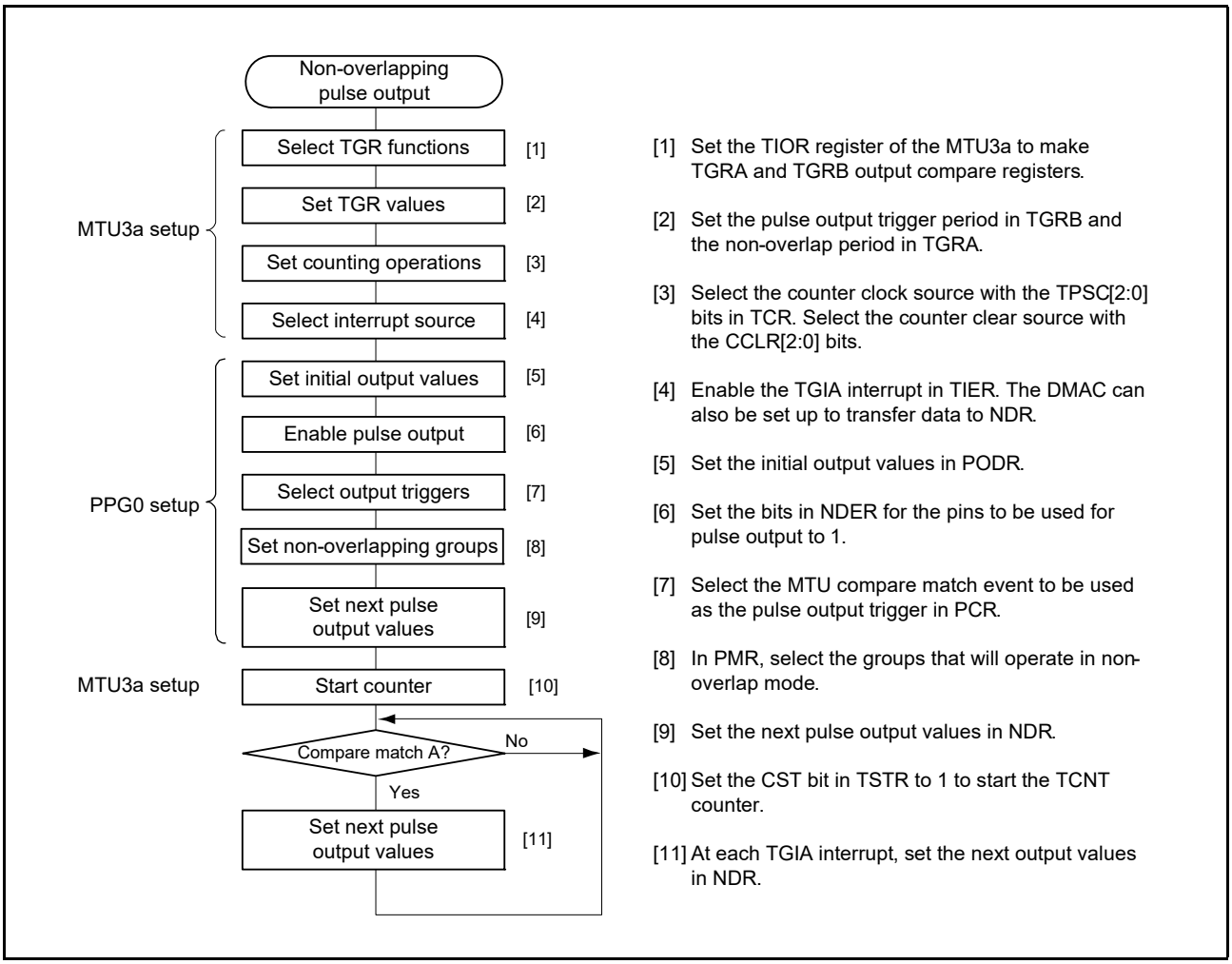


Figure 23.9 Sample Setup Procedure for Non-Overlapping Pulse Output (PPG Setting)

23.3.6 Example of Non-Overlapping Pulse Output (Example of Four-Phase Complementary Non-Overlapping Output)

Figure 23.10 shows an example in which four-phase complementary non-overlapping pulse is output on PPG0 (PO8 to PO15) with MTU1 as the trigger for output.

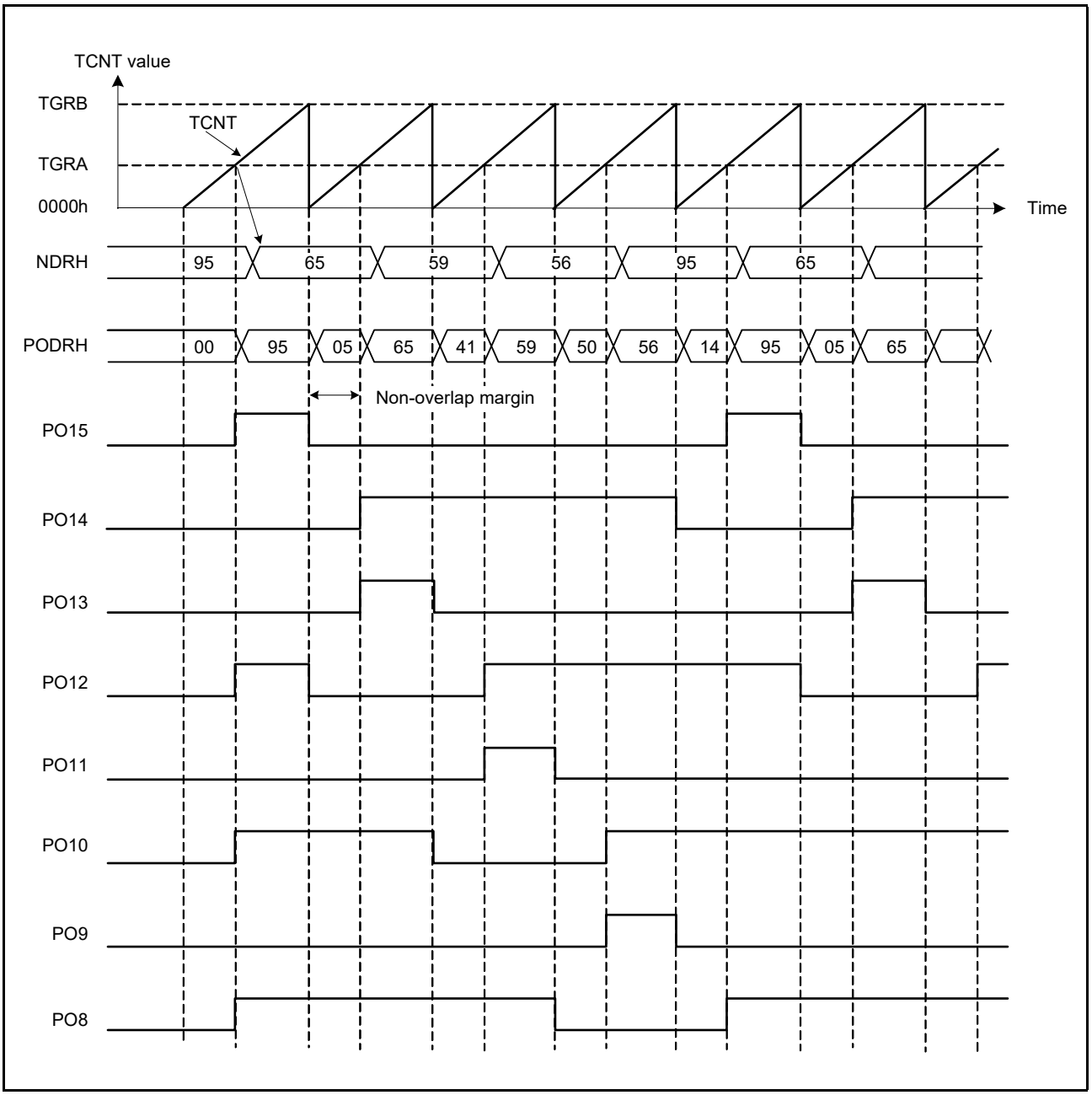


Figure 23.10 Example of Non-Overlapping Pulse Output (Four-Phase Complementary Non-Overlapping Output)

1. Set output compare registers of the TGRA and TGRB of MTU1 so that the corresponding compare match signals are the output triggers. Set the trigger period in TGRB and the non-overlap margin in TGRA, and specify MTU1.TCR.CCLR to set the counter to be cleared by compare match B. Set MTU1.TIER.TGIEA to 1 to enable the compare match/input capture A (TGIA1) interrupt.
2. Write FFh in PPG0.NDERH, and set the G3CMS[1:0] and G2CMS[1:0] bits in PPG0.PCR to select the respective compare matches in the MTU1 selected in the previous step to be the output triggers.
   Set the G3NOV and G2NOV bits in PPG0.PMR to 1 to select non-overlapping outputs. Write output data 95h in PPG0.NDRH.
3. The timer counter in MTU1 starts. When a compare match with MTU1.TGRB occurs, outputs change from high to low. When a compare match with MTU1.TGRA occurs, outputs change from low to high (the change from low to high is delayed by the value set in TGRA).
   The TGIA1 interrupt handling routine writes the next output data 65h in PPG0.NDRH.
4. Four-phase complementary non-overlapping pulse output can be obtained subsequently by writing 59h, 56h, 95h... at successive TGIA1 interrupts.
   If the DMAC is set for activation by the TGIA1 interrupt, pulse output can be obtained without imposing a load on the CPU.

23.3.7 Inverted Pulse Output

When the G3INV, G2INV, G1INV, and G0INV bits in the PMR register are cleared to 0, the values that are the inverse of the respective values in PODRH and PODRL can be output.

Figure 23.11 shows the outputs when the G3INV and G2INV bits are cleared to 0 in addition to the settings in Figure 23.10.

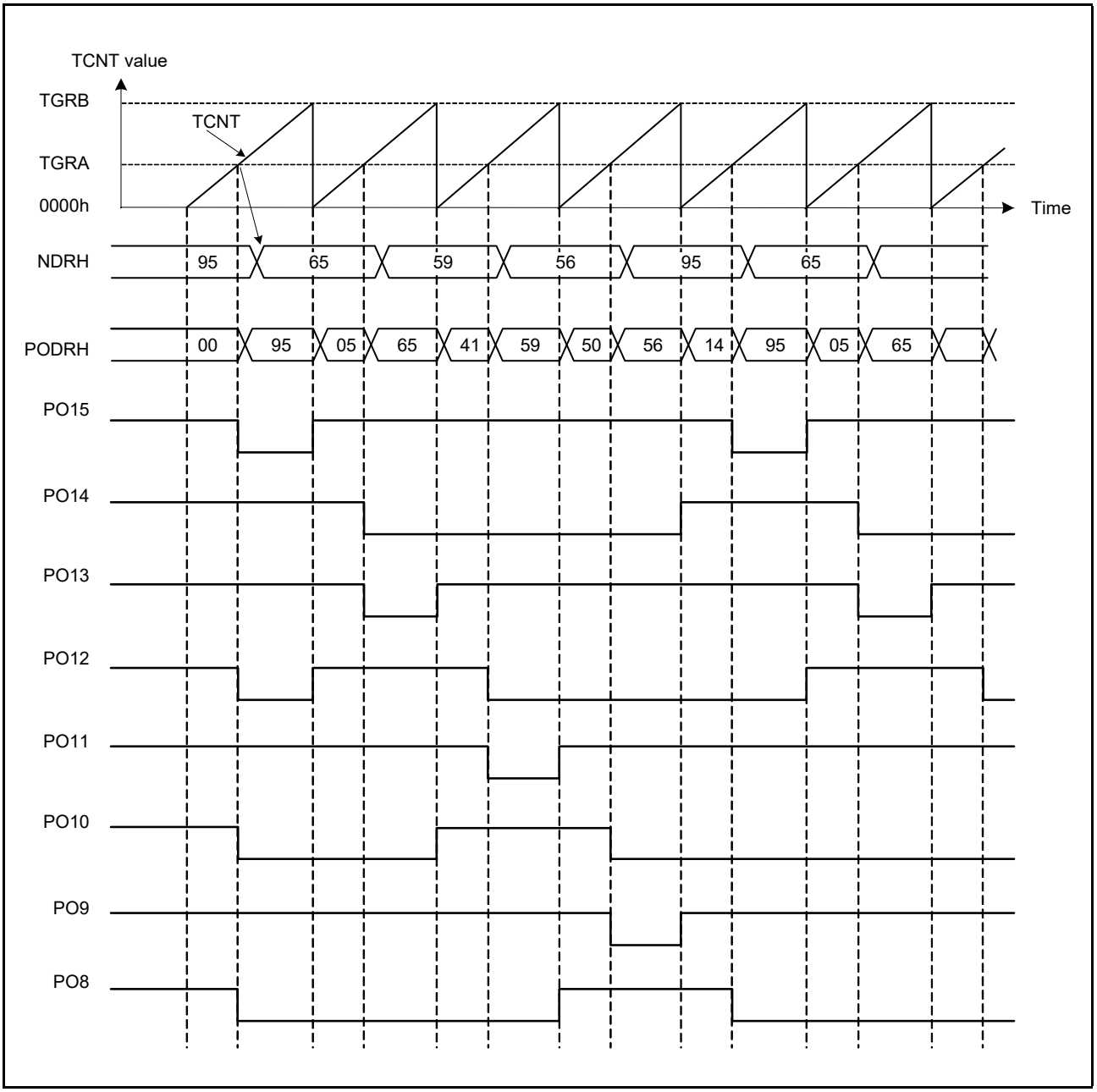


Figure 23.11 Inverted Pulse Output (Example)

23.3.8 Pulse Output Triggered by Input Capture

Pulse output from the PPG1 can be triggered by MTU3a or TPUa input capture as well as by compare match. When TGRA in the timer selected by PCR functions as an input capture register, pulse output is triggered by the input capture signal.

Figure 23.12 shows the timing of pulse output triggered by input capture.

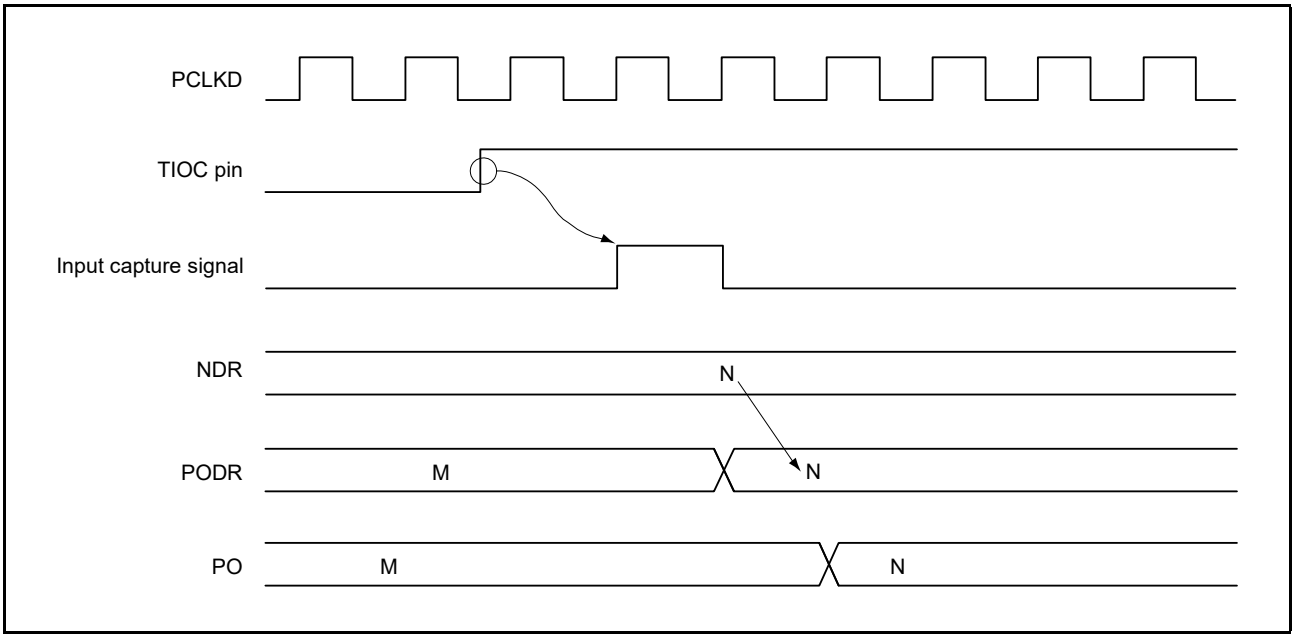


Figure 23.12 Timing of Pulse Output Triggered by Input Capture (Example)

23.4 Usage Note

23.4.1 Module-Stop Function Setting

Operation of the PPG can be disabled or enabled by the module stop control register. The initial setting is for operation of the PPG to be stopped. Register access is enabled by clearing module-stop state. For details, see section 9, Low-Power Consumption Function.

24. Compare Match Timer (CMT)

The compare match timer (CMT) consists of a two-channel 16-bit timer, and can generate interrupts at set intervals by using its 16-bit counter.

24.1 Overview

Table 24.1 lists the specifications for the CMT.
Figure 24.1 shows a block diagram of the CMT.

Table 24.1 CMT Specifications

Item	Description
Number of internal channels	Two channels × three units
Timer counter (per channel)	16-bit up counter (Counted according to the count enable signal output by the prescaler.) Returned to 0000h after compare match.
Prescaler (per channel)	9-bit counter (Linked with enabling/disabling of timer counter operation.) • Outputs four types of count enable signals. The type can be selected from PCLKD/8, PCLKD/32, PCLKD/128, and PCLKD/512.
Event link function (only channel 1 of unit 0)	One of the following three operations is possible depending on the received event: • Count start • Event count • Count clear This function can issue a compare match event.
Reset	Asynchronous reset

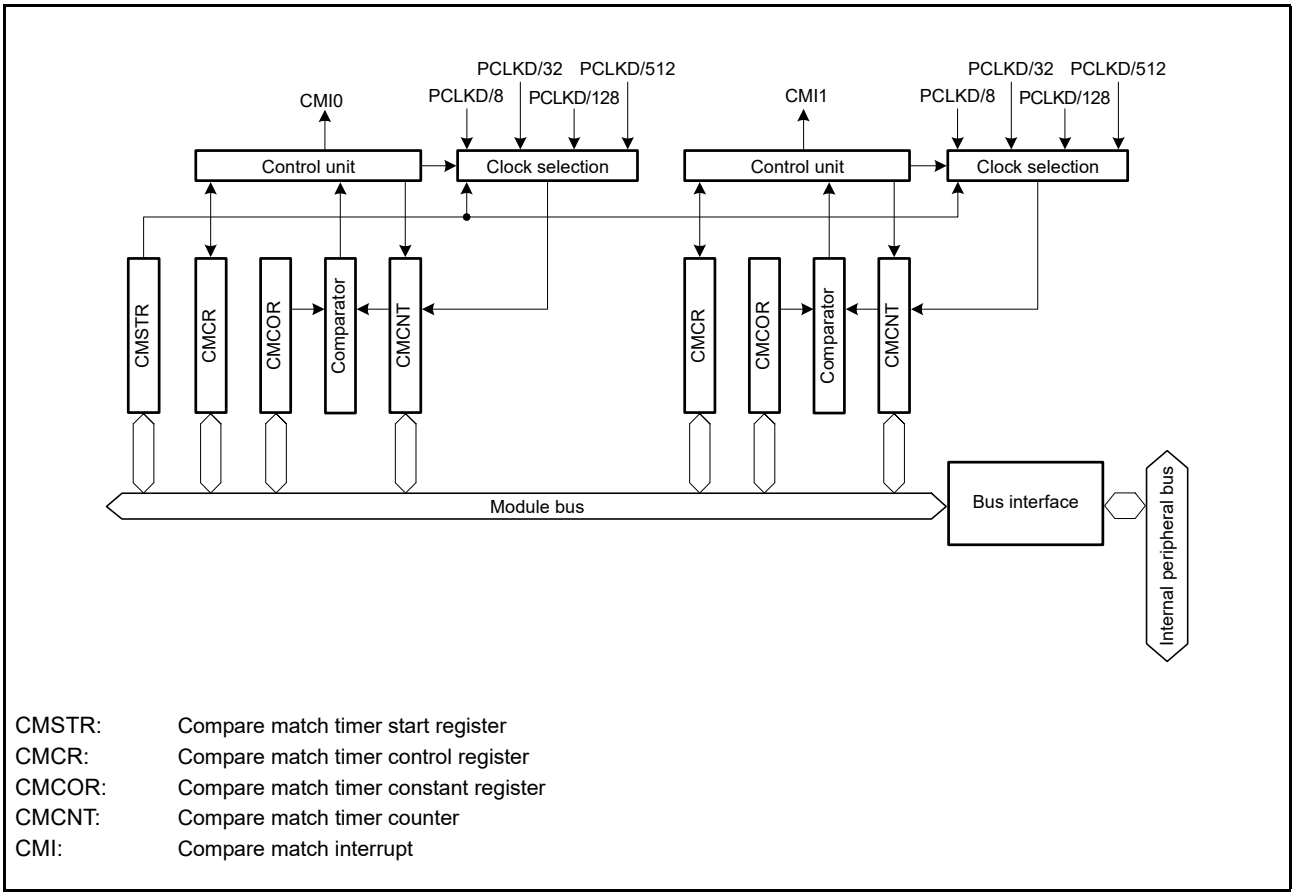


Figure 24.1 Block Diagram of CMT (Units 0 to 2)

24.2 Register Descriptions

24.2.1 Compare Match Timer Start Register 0 (CMSTR0)

The CMSTR0 register sets starting or stopping of the CMT0.CMCNT and CMT1.CMCNT counters of unit 0.

Address(es): A008 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR1	STR0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR0	Count Start 0	This bit selects starting or stopping of the CMT0.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT0.CMCNT counter is stopped. 1: The CMT0.CMCNT counter is started.	R/W
b1	STR1	Count Start 1	This bit selects starting or stopping of the CMT1.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT1.CMCNT counter is stopped. 1: The CMT1.CMCNT counter is started.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.2 Compare Match Timer Start Register 1 (CMSTR1)

The CMSTR1 register sets starting or stopping of the CMT2.CMCNT and CMT3.CMCNT counters of unit 1.

Address(es): A008 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR3	STR2
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR2	Counter Start 2	This bit selects starting or stopping of the CMT2.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT2.CMCNT counter is stopped. 1: The CMT2.CMCNT counter is started.	R/W
b1	STR3	Counter Start 3	This bit selects starting or stopping of the CMT3.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT3.CMCNT counter is stopped. 1: The CMT3.CMCNT counter is started.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.3 Compare Match Timer Start Register 2 (CMSTR2)

The CMSTR2 register sets starting or stopping of the CMT4.CMCNT and CMT5.CMCNT counters of unit 2.

Address(es): A008 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR5	STR4
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR4	Counter Start 4	This bit selects starting or stopping of the CMT4.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT4.CMCNT counter is stopped. 1: The CMT4.CMCNT counter is started.	R/W
b1	STR5	Counter Start 5	This bit selects starting or stopping of the CMT5.CMCNT counter operation. The corresponding prescaler starts or stops according to the setting of this bit. 0: The CMT5.CMCNT counter is stopped. 1: The CMT5.CMCNT counter is started.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.4 Compare Match Timer Control Register (CMCR)

The CMCRn register specifies a clock used for count-up operation.

Address(es): CMT0: A008 0002h, CMT1: A008 0008h, CMT2: A008 0022h, CMT3: A008 0028h, CMT4: A008 0042h, CMT5: A008 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CMIE	—	—	—	—	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	These bits select a clock to be input to the CMTn.CMCNT counter from the internal clocks obtained by dividing the frequency of the low-speed peripheral module clock (PCLKD). Setting the CMSTRm.STRn bit to 1 starts count-up operation of the corresponding CMCNT counter by using the clock selected in the CKS[1:0] bits (m = 0 to 2, n = 0 to 5). b1 b0 0 0: PCLKD/8 0 1: PCLKD/32 1 0: PCLKD/128 1 1: PCLKD/512	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CMIE	Compare Match Interrupt Enable	This bit selects whether to enable or disable generation of a compare match interrupt (CMIn) when the values in the CMCNT counter and in the CMCOR register match (n = 0 to 5). 0: Compare match interrupt (CMIn) disabled 1: Compare match interrupt (CMIn) enabled	R/W
b7	—	Reserved	When read, the value returned is undefined. The write value should be 0.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

24.2.5 Compare Match Timer Counter (CMCNT)

The CMCNT counter (the main unit of the compare match timer) is a readable/writable up-counter.
When an internal clock is selected by the CMCR.CKS[1:0] bits and the CMSTRm.STRn (m = 0 to 2, n = 0 to 5) bit is set to 1, the CMCNT counter starts counting up using the selected clock.
When the value in the CMCNT counter and the value in the CMCOR register match, the CMCNT counter is cleared to 0000h. At the same time, a compare match interrupt (CMIn) is generated (n = 0 to 5).

Address(es): CMT0: A008 0004h, CMT1: A008 000Ah, CMT2: A008 0024h, CMT3: A008 002Ah, CMT4: A008 0044h, CMT5: A008 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24.2.6 Compare Match Timer Constant Register (CMCOR)

The CMCOR register is a readable/writable register to set a cycle for compare match with the CMCNT counter.
The cycle for compare matches is as follows.

Compare-match cycle = (setting of the CMCOR register + 1) × counter-clock cycle*1

Note 1. This is a clock cycle set by the CMCR.CKS[1:0] bits.

Address(es): CMT0: A008 0006h, CMT1: A008 000Ch, CMT2: A008 0026h, CMT3: A008 002Ch, CMT4: A008 0046h, CMT5: A008 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

24.3 Operation

24.3.1 Periodic Count Operation

When an internal clock is selected by the CMCRn.CKS[1:0] bits and the CMSTRm.STRn (m = 0 to 2, n = 0 to 5) bit is set to 1, the CMCNT counter starts counting up using the selected clock.
When the value in the CMCNT counter and the value in the CMCOR register match, the CMCNT counter is cleared to 0000h, and then a compare match interrupt (CMIn) is generated. The CMCNT counter then starts counting up again from 0000h. Figure 24.2 shows the operation of the CMCNT counter.

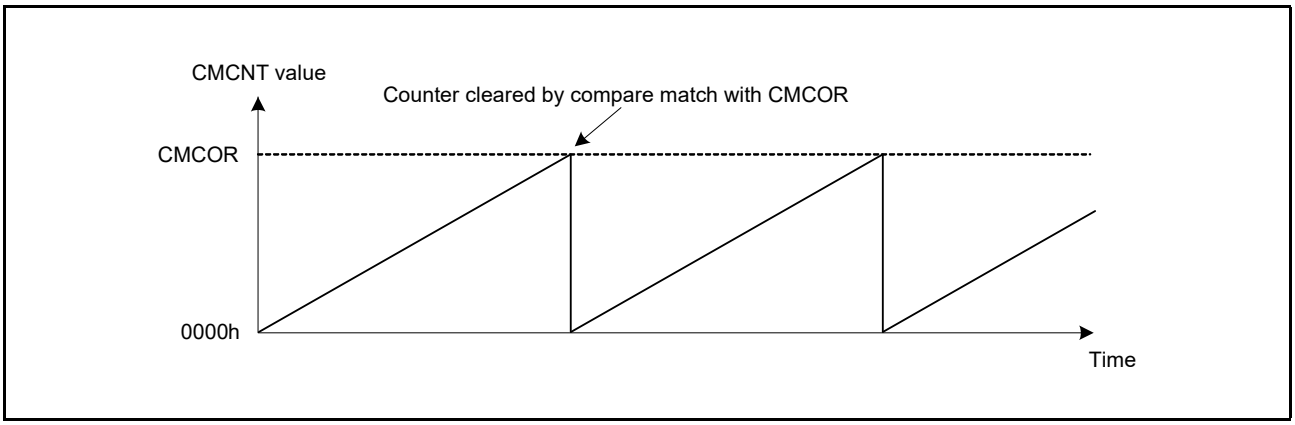


Figure 24.2 Counter Operation

24.3.2 CMCNT Count Timing

As the count clock, one of four internal clocks (PCLKD/8, PCLKD/32, PCLKD/128, and PCLKD/512) obtained by dividing the low-speed peripheral module clock (PCLKD) can be selected with the CMCR.CKS[1:0] bits. Figure 24.3 shows the timing of the CMCNT counter.

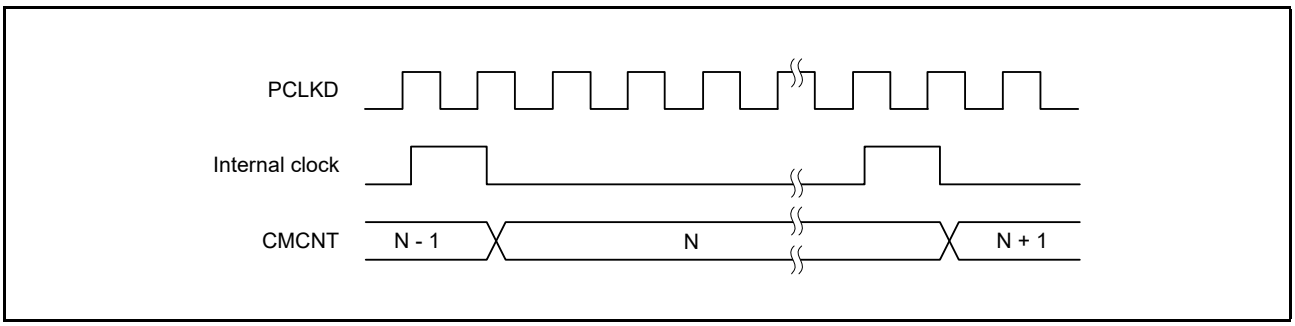


Figure 24.3 CMCNT Count Timing

24.4 Interrupts

24.4.1 Interrupt Sources

The CMT has channels and each of them to which a different vector address is allocated has a compare match interrupt (CMIn). The priority of channels can be changed by the interrupt controller settings.

Table 24.2 CMT Interrupt Sources

Name	Interrupt Sources
CMI0	Compare match between the CMT0.CMCNT counter and CMT0.CMCOR register
CMI1	Compare match between the CMT1.CMCNT counter and CMT1.CMCOR register
CMI2	Compare match between the CMT2.CMCNT counter and CMT2.CMCOR register
CMI3	Compare match between the CMT3.CMCNT counter and CMT3.CMCOR register
CMI4	Compare match between the CMT4.CMCNT counter and CMT4.CMCOR register
CMI5	Compare match between the CMT5.CMCNT counter and CMT5.CMCOR register

24.4.2 Timing of Compare Match Interrupt Generation

When the CMCNT counter and the CMCOR register match, a compare match interrupt (CMIn) is generated.
A compare match signal is generated at the last state in which the values match (the timing when the CMCNT counter updates the matched count value). That is, after a match between the CMCOR register and the CMCNT counter, the compare match signal is not generated until the CMCNT counter input clock is generated (n = 0 to 5).
Figure 24.4 shows the timing of a compare match interrupt.

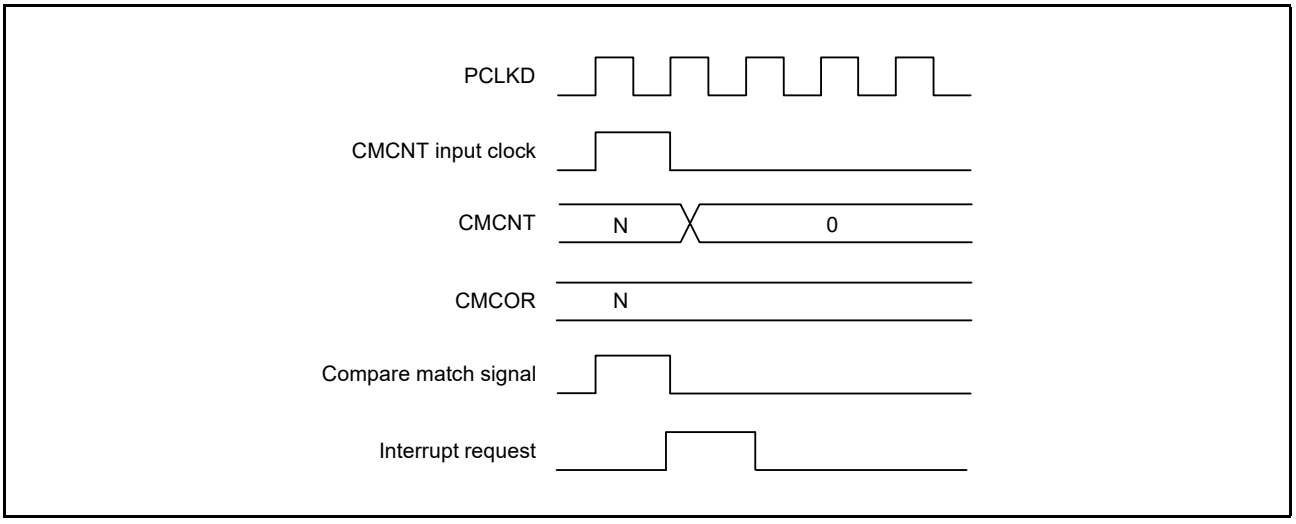


Figure 24.4 Timing a Compare Match Interrupt is Set

24.5 Event Link Operations

24.5.1 Event Issuance to ELC

The CMT issues an interrupt request when compare match occurs. Then, the CMT can use the event link controller (ELC) to perform link operation to a preset module using the interrupt request signal as the event signal.
The event signal can be output regardless of the setting of the corresponding interrupt request enable bit (CMT1.CMCR.CMIE).

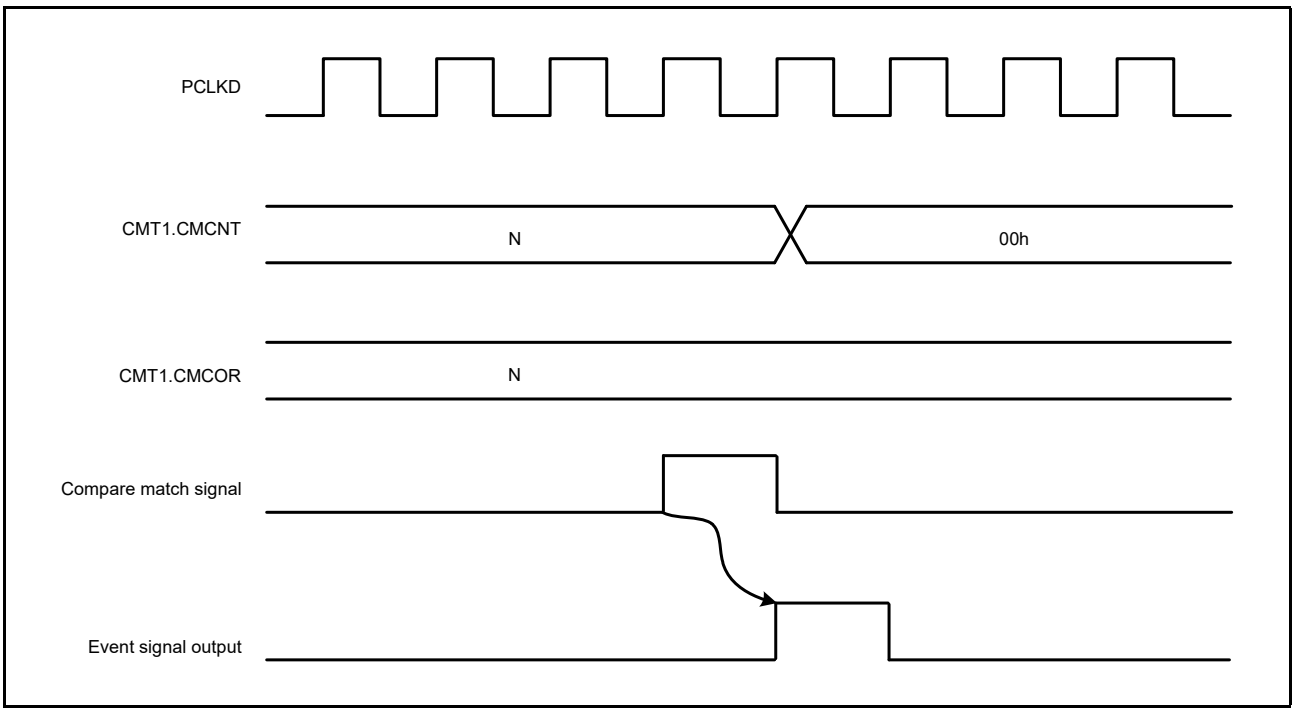


Figure 24.5 Timing of Event Issuance

24.5.2 CMT Operation When Receiving an Event from ELC

The CMT can perform either of the following three operations upon the event preset in the event link controller (ELC).

(1) Count Start

When the CMT count start operation is selected in the ELC and an event is received, the STR1 bit in the corresponding CMSTR0 (compare match timer start register 0) is set to 1, starting the count operation.
However, if the specified event occurs while the CMSTR0.STR1 bit is 1, the event is invalid.

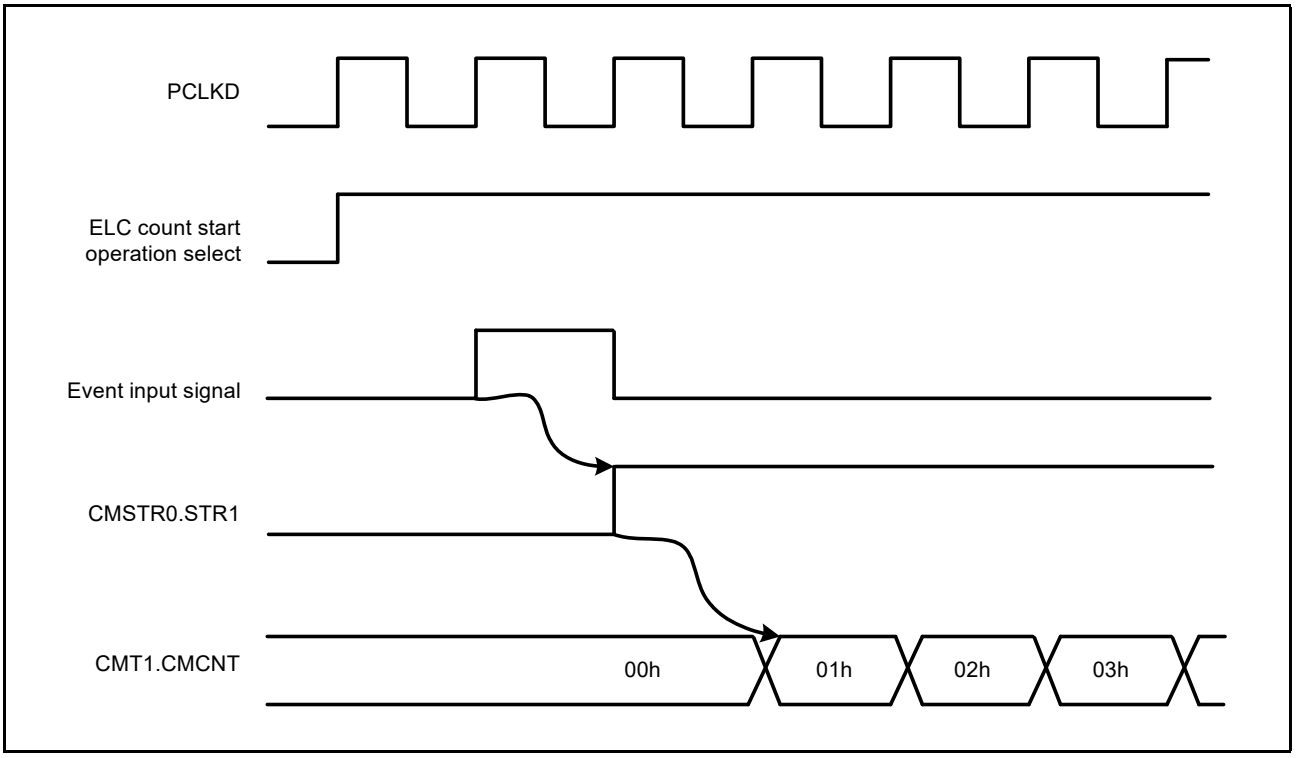


Figure 24.6 Count Start Operation at Reception of an Event

(2) Event Count

When the CMT event count operation is selected in the ELC and an event is received, the CMT1.CMCNT (compare match timer counter) is incremented, regardless of the setting of the CKS[1:0] bits in CMT1.CMCR (compare match timer control register). The STR1 bit in the CMSTR0 (compare match timer start register) must be set to 1 before receiving an event.

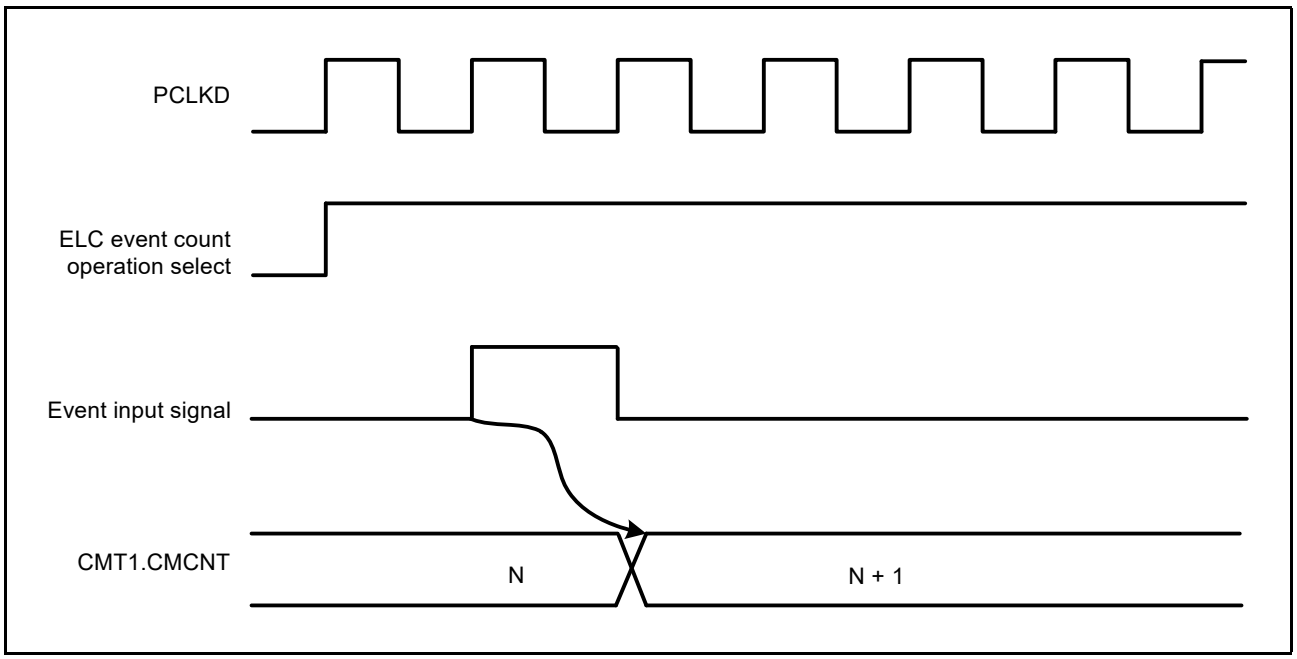


Figure 24.7 Event Count Operation at Reception of an Event

(3) Count Clear

When the CMT count clear operation is selected in the ELC and an event is received, the compare match timer counter (CMT1.CMCNT) is returned to its initial value. Counting continues, however, if the setting of the STR1 bit of compare match timer start register 0 (CMSTR0) is 1 at this time, so counting can be automatically restarted in this way.

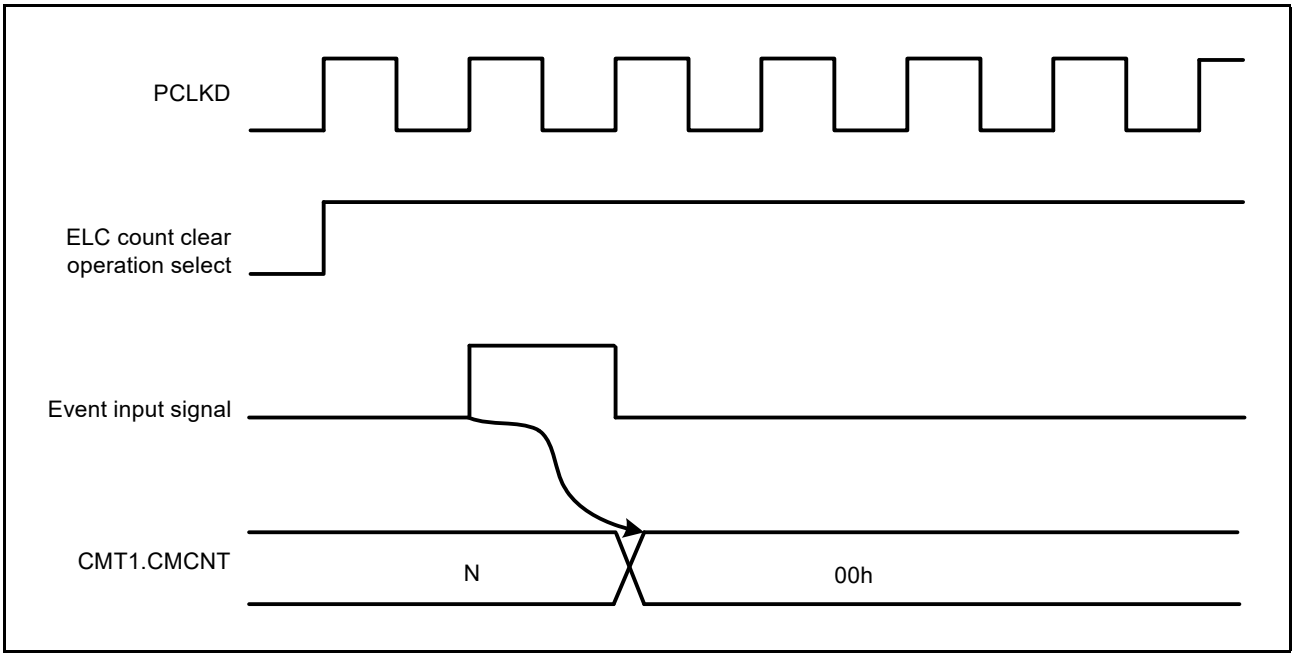


Figure 24.8 Count Clear Operation at Reception of an Event

24.5.3 Notes on CMT Event Link Operation

Note the following when using the CMT with event link operation.

(1) Count Start

When an event occurs during the write access to the STR1 bit in the CMSTR0 (compare match timer start register 0), that write access is not performed, and setting 1 according to the event occurrence takes priority.

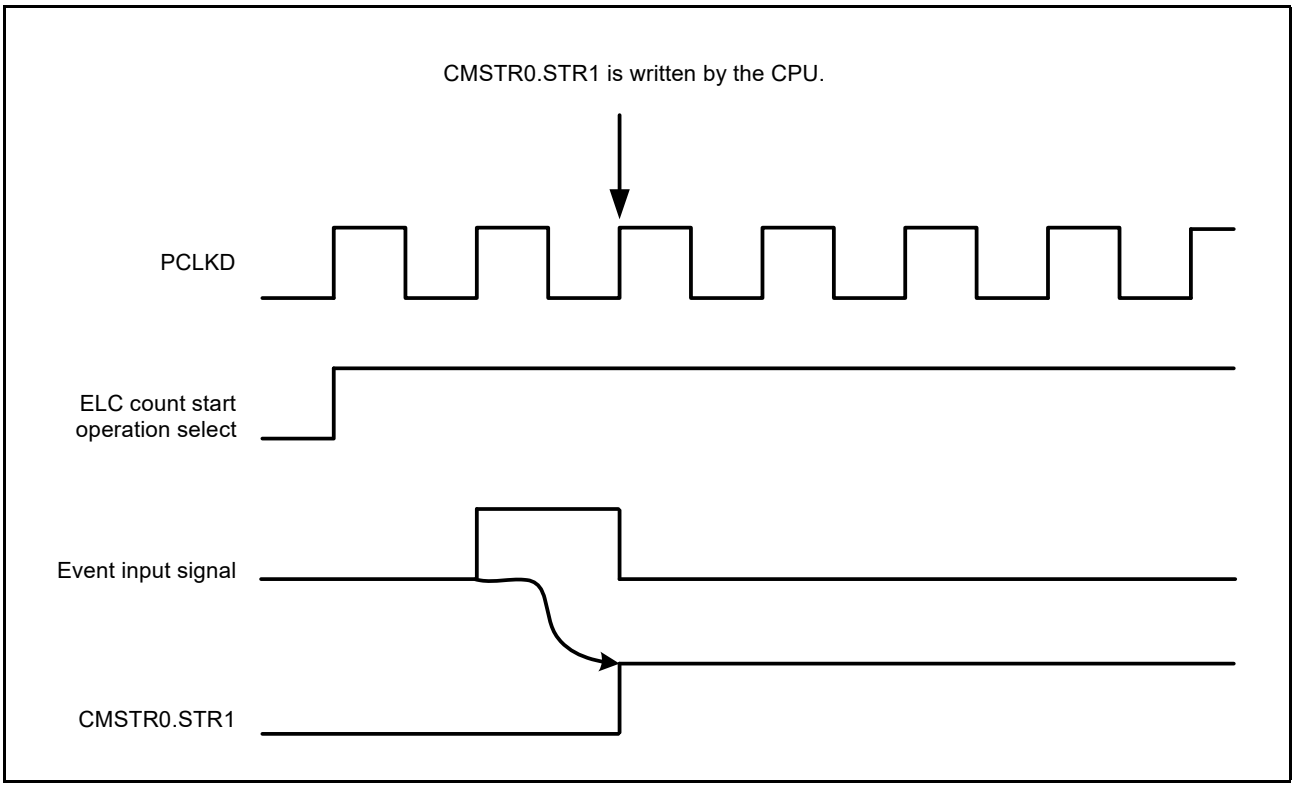


Figure 24.9 Conflict between Event Reception and Register Access at Count Start Operation

(2) Event Count

When an event occurs during the write access to the CMT1.CMCNT (compare match timer counter), that write access is not performed, and event count operation according to the event occurrence takes priority.

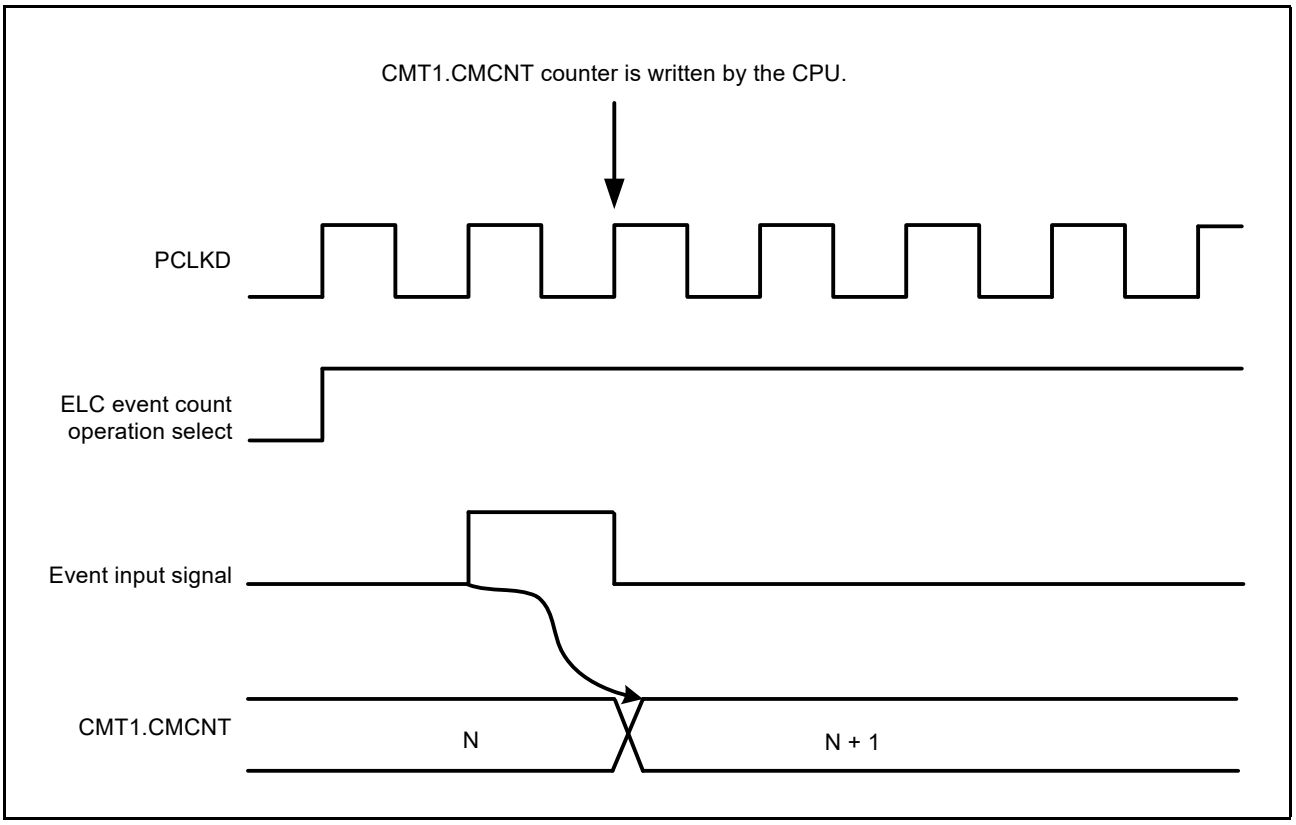


Figure 24.10 Conflict between Event Reception and Register Access at Event Count Operation

(3) Count Clear

When an event occurs during the write access to the CMT1.CMCNT (compare match timer counter), that write access is not performed, and count value initialization according to the event occurrence takes priority.

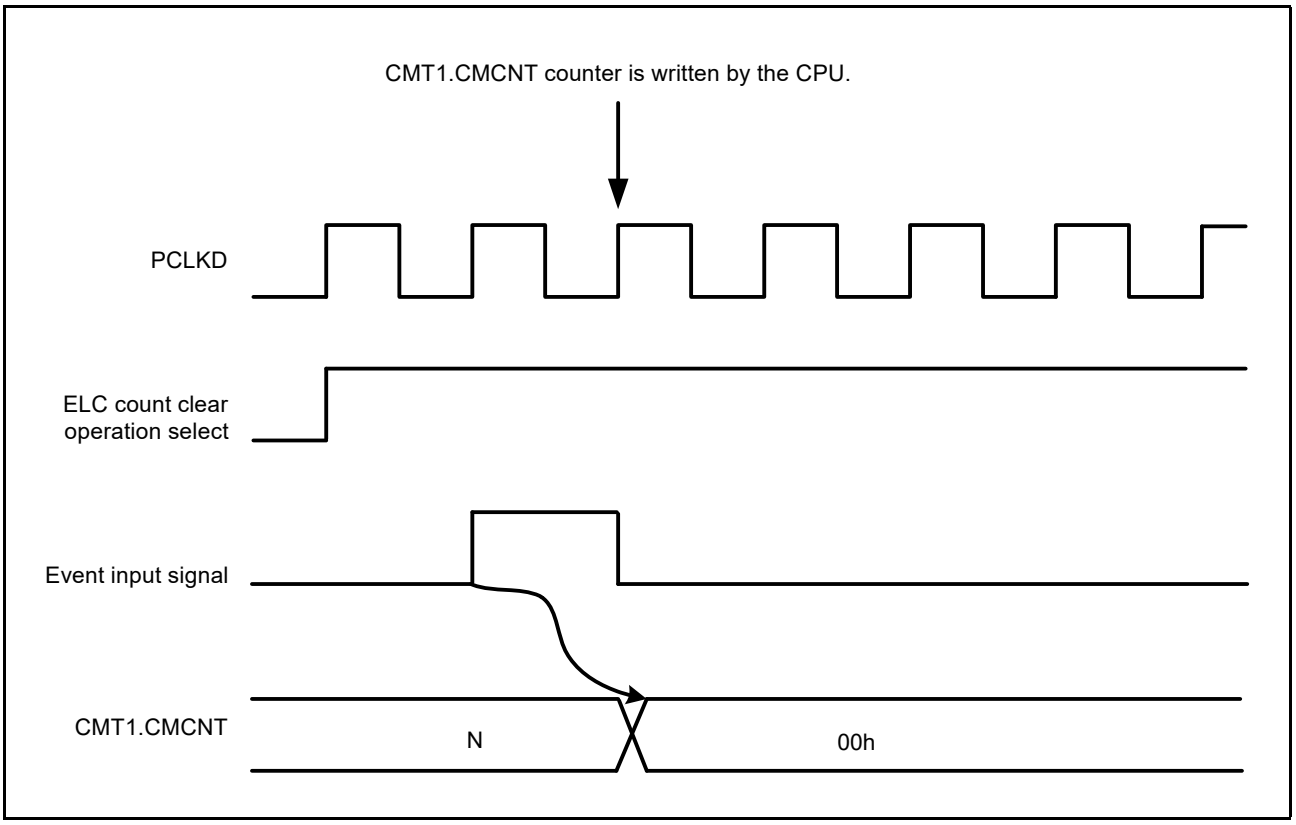


Figure 24.11 Conflict between Event Reception and Register Access at Count Clear Operation

24.6 Usage Notes

24.6.1 Setting the Module Stop Function

The CMT can be enabled or disabled using the module stop control register. After a reset, the CMT is in the module-stop state. The registers can be accessed by canceling the module-stop state. For details, see section 9, Low-Power Consumption Function.

24.6.2 Conflict between Write and Compare-Match Processes of CMCNT

When the compare match signal is generated while writing to the CMCNT counter, clearing the CMCNT counter is given priority over writing to it. In this case, the CMCNT counter is not written to. Figure 24.12 shows the timing to clear the CMCNT counter.

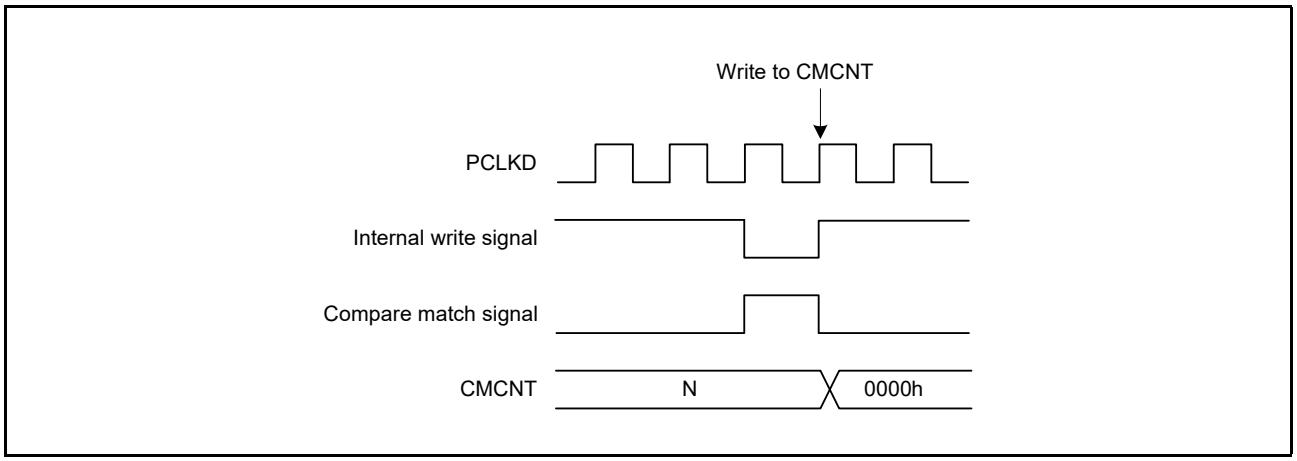


Figure 24.12 Conflict between Write and Compare Match Processes of CMCNT

24.6.3 Conflict between Write and Count-Up Processes of CMCNT

If count-up occurs during the write access to the CMCNT counter, that writing has priority over the count-up. Figure 24.13 shows the timing to write the CMCNT counter.

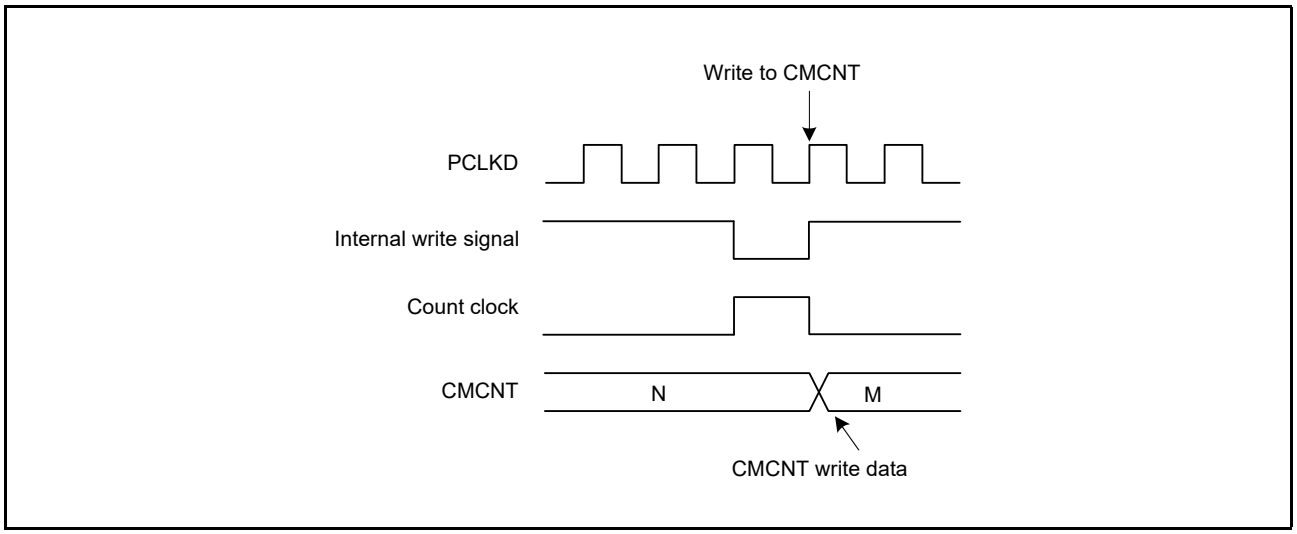


Figure 24.13 Conflict between Write and Count-Up Processes of CMCNT

Table 24.3 Summary of Conflicted Operations among Event Link Operation, Register Access, and Counter Status

Event Link Operation	Register Access	CMCNT Status	Operation to be Performed
Count start	Writing to CMSTR0.STR1	Stopped	Count start
		Compare match	Count start
		Count up	Count start
Event count	Writing to CMCNT	—	Event count
	Writing to CMCOR	Compare match	Compare match
Count clear	Writing to CMCNT	Other than compare match	Count clear
	Writing to CMCNT	Compare match	Compare match
	(No register access)	Compare match	Compare match
(No event)	Writing to CMCNT	Compare match	Compare match
		Count up	Writing to CMCNT
	Writing to CMCOR	Compare match	Compare match

25. Compare Match Timer W (CMTW)

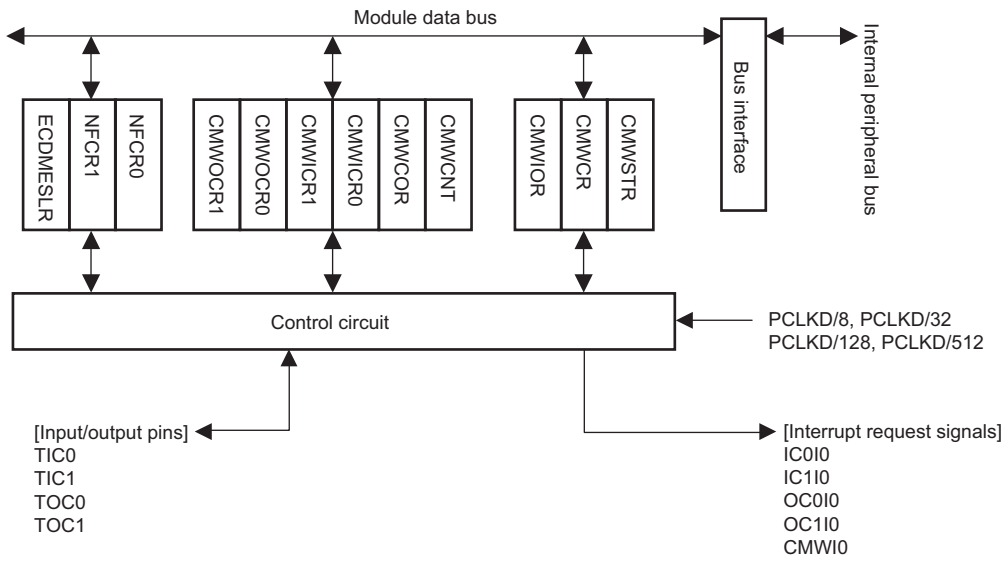
This LSI includes two units with one channel of 32-bit compare match timer W (CMTW).
CMTW has a 32-bit counter and can generate interrupts each time a set period elapses.

25.1 Overview

Table 25.1 shows the specifications of the CMTW. Figure 25.1 shows a block diagram of the CMTW.

Table 25.1 Specifications of CMTW

Item	Function
Number of channel	One channel × two units
Timer counter	16-bit/32-bit selectable up-counter Counting starts after the output of a counting enable signal from the prescaler. The counter returns to 0000 0000h after a compare match.
Prescaler	9-bit counter (operates to enable and disable the timer counter) Outputs four signals to enable counting. Selectable either of PCLKD/8, PCLKD/32, PCLKD/128, and PCLKD/512
Input capture	Up to two input capture input signals available.
Output compare	Up to two output compare output signals available.
Compare match	One compare match available.
Interrupt	• Compare match interrupt • Input capture 0 and 1 interrupts • Output compare 0 and 1 interrupts
Event link	One of the following three operations is enabled after an event signal is received: • Counting start • Event counting • Counting clear Also, the following event signal can be issued: • Compare match event
Low-power consumption function	The module-stop state can be set for each unit.



CMWSTR: Timer start register
CMWCR: Timer control register
CMWIOR: Timer I/O control register
CMWCNT: Timer counter
CMWCOR: Compare match constant register
CMWICR0: Input capture register 0
CMWICR1: Input capture register 1
CMWOCR0: Output compare register 0
CMWOCR1: Output compare register 1
NFCR0: Digital noise filter control register 0
NFCR1: Digital noise filter control register 1
ECDMESLR: ECM dynamic mode error output select register

Figure 25.1 Block Diagram of CMTW (Unit 0)

Table 25.2 shows the CMTW pin configuration.

Table 25.2 Input/Output Pins of CMTW

Unit	Pin Name	I/O	Description
CMTW0	TIC0	Input	Input capture input 0
	TIC1	Input	Input capture input 1
	TOC0	Output	Output compare output 0
	TOC1	Output	Output compare output 1
CMTW1	TIC2	Input	Input capture input 2
	TIC3	Input	Input capture input 3
	TOC2	Output	Output compare output 2
	TOC3	Output	Output compare output 3

25.2 Register Descriptions

25.2.1 Timer Start Register (CMWSTR)

The CMWSTR register is used to start or stop the CMWCNT counter.

Address(es): CMTW0.CMWSTR A008 0300h, CMTW1.CMWSTR A008 0380h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STR	Counter Start	0: The CMWCNT counter stops counting. (The value immediately before a stop of counting is retained and counting is stopped.) 1: The CMWCNT counter starts counting.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

STR Bit (Counter Start)

Specifies whether the timer counter operates or is stopped. The relevant prescaler operates or is stopped according to the settings of STR bit.

25.2.2 Timer Control Register (CMWCR)

The CMWCR register selects the counter clearing source and the counter input clock, and enables or disables interrupts. The CMWCR register should be set while the timer counter (CMWCNT) operation is stopped.

Address(es): CMTW0.CMWCR A008 0304h, CMTW1.CMWCR A008 0384h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CCLR[2:0]			—	—	—	CMS	—	OC1IE	OC0IE	IC1IE	IC0IE	CMWIE	—	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKD/8 0 1: PCLKD/32 1 0: PCLKD/128 1 1: PCLKD/512	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	CMWIE	Compare Match Interrupt Enable	0: Disables a compare match interrupt request (CMWI). 1: Enables a compare match interrupt request (CMWI).	R/W
b4	IC0IE	Input Capture 0 Interrupt Enable	0: Disables an interrupt request by the input capture 0 bit (IC0I). 1: Enables an interrupt request by the input capture 0 bit (IC0I).	R/W
b5	IC1IE	Input Capture 1 Interrupt Enable	0: Disables an interrupt request by the input capture 1 bit (IC1I). 1: Enables an interrupt request by the input capture 1 bit (IC1I).	R/W
b6	OC0IE	Output Compare 0 Interrupt Enable	0: Disables an interrupt request by the output compare 0 bit (OC0I). 1: Enables an interrupt request by the output compare 0 bit (OC0I).	R/W
b7	OC1IE	Output Compare 1 Interrupt Enable	0: Disables an interrupt request by the output compare 1 bit (OC1I). 1: Enables an interrupt request by the output compare 1 bit (OC1I).	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9	CMS	Timer Counter Size	0: 32 bits 1: 16 bits	R/W
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b13	CCLR[2:0]	Counter Clear	b15 b13 0 0 0: The CMWCNT counter is cleared by CMWCOR register compare match. 0 0 1: The CMWCNT counter is not cleared. 0 1 0: The CMWCNT counter is not cleared. 0 1 1: The CMWCNT counter is not cleared. 1 0 0: The CMWCNT counter is cleared by CMWICR0 register input capture. 1 0 1: The CMWCNT counter is cleared by CMWICR1 register input capture. 1 1 0: The CMWCNT counter is cleared by CMWOCR0 register compare match. 1 1 1: The CMWCNT counter is cleared by CMWOCR1 register compare match.	R/W

CKS[1:0] Bits (Clock Select)

Select the clock to be input to the CMWCNT counter among four internal clocks obtained by dividing the peripheral clock (PCLKD). When the CMWSTR.STR bit is set to 1, the CMWCNT counter starts counting up based on the clock selected with the CMWCNT.CKS[1:0] bits.

CMWIE Bit (Compare Match Interrupt Enable)

Enables or disables compare match interrupt (CMWI) request generation when the CMWCNT counter and CMWCOR register values match.

IC0IE Bit (Input Capture 0 Interrupt Enable)

Enables or disables input capture interrupt 0 (IC0I) request generation when input capture is generated in the CMWICR0 register.

IC1IE Bit (Input Capture 1 Interrupt Enable)

Enables or disables input capture interrupt 1 (IC1I) request generation when input capture is generated in the CMWICR1 register.

OC0IE Bit (Output Compare 0 Interrupt Enable)

Enables or disables compare match interrupt 0 (OC0I) request generation when the CMWCNT counter and CMWOCR0 register values match.

OC1IE Bit (Output Compare 1 Interrupt Enable)

Enables or disables compare match interrupt 1 (OC1I) request generation when the CMWCNT counter and CMWOCR1 register values match.

CMS Bit (Timer Counter Size)

Selects either 16 or 32 bits as the size of the timer counter (CMWCNT). The size selected with the CMS bit is valid in the compare match constant register (CMWCOR), input capture registers (CMWICR0 and CMWICR1), and output compare registers (CMWOCR0 and CMWOCR1).

CCLR[2:0] Bits (Counter Clear)

Selects the CMWCNT counter clearing source.

25.2.3 Timer I/O Control Register (CMWIOR)

The CMWIOR register controls the CMWCOR, CMWICR0, CMWICR1, CMWOCR0, and CMWOCR1 registers. CMWIOR should be set while the timer counter (CMWCNT) operation is stopped.

Address(es): CMTW0.CMWIOR A008 0308h, CMTW1.CMWIOR A008 0388h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMWE	—	OC1E	OC0E	OC1[1:0]		OC0[1:0]		—	—	IC1E	IC0E	IC1[1:0]		IC0[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	IC0[1:0]	Input Compare Control 0	b1 b0 0 0: Input capture at the rising edge on the TIC0 pin. 0 1: Input capture at the falling edge on the TIC0 pin. 1 0: Input capture at both edges on the TIC0 pin. 1 1: Setting prohibited	R/W
b3, b2	IC1[1:0]	Input Capture Control 1	b3 b2 0 0: Input capture at the rising edge on the TIC1 pin. 0 1: Input capture at the falling edge on the TIC1 pin. 1 0: Input capture at both edges on the TIC1 pin. 1 1: Setting prohibited	R/W
b4	IC0E	Input Capture Enable 0	0: Disables the input capture operation of the CMWICR0 register. 1: Enables the input capture operation of the CMWICR0 register.	R/W
b5	IC1E	Input Capture Enable 1	0: Disables the input capture operation of the CMWICR1 register. 1: Enables the input capture operation of the CMWICR1 register.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	OC0[1:0]	Output Compare Control 0	b9 b8 0 0: Retains the output value.*1 0 1: Initially outputs 0 and toggles the output value upon compare match. 1 0: Initially outputs 1 and toggles the output value upon compare match. 1 1: Setting prohibited	R/W
b11, b10	OC1[1:0]	Output Compare Control 1	b11 b10 0 0: Retains the output value.*1 0 1: Initially outputs 0 and toggles the output value upon compare match. 1 0: Initially outputs 1 and toggles the output value upon compare match. 1 1: Setting prohibited	R/W
b12	OC0E	Compare Match Enable 0	0: Disables the compare match operation using the CMWOCR0 register. 1: Enables the compare match operation using the CMWOCR0 register.	R/W
b13	OC1E	Compare Match Enable 1	0: Disables the compare match operation using the CMWOCR1 register. 1: Enables the compare match operation using the CMWOCR1 register.	R/W
b14	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15	CMWE	Compare Match Enable	0: Disables the compare match operation using the CMWCOR register. 1: Enables the compare match operation using the CMWCOR register.	R/W

Note 1. After reset, 0 is output until the CMWIOR register is set.

IC0[1:0] Bits (Input Compare Control 0)

Selects the input capture operation of the CMWICR0 register.

IC1[1:0] Bits (Input Capture Control 1)

Selects the input capture operation of the CMWICR1 register.

IC0E Bit (Input Capture Enable 0)

Enables or disables the input capture operation of the CMWICR0 register.

IC1E Bit (Input Capture Enable 1)

Enables or disables the input capture operation of the CMWICR1 register.

OC0[1:0] Bits (Output Compare Control 0)

Sets the output compare operation using the CMWOCR0 register.

OC1[1:0] Bits (Output Compare Control 1)

Sets the output compare operation using the CMWOCR1 register.

OC0E Bit (Compare Match Enable 0)

Enables or disables the compare match operation using the CMWOCR0 register.

OC1E Bit (Compare Match Enable 1)

Enables or disables the compare match operation using the CMWOCR1 register.

CMWE Bit (Compare Match Enable)

Enables or disables the compare match operation using the CMWCOR register.

25.2.4 Timer Counter (CMWCNT)

The CMWCNT counter is used as a readable/writable up-counter.

Before starting counter operation, the timer control register (CMWCR) should be set. When the 16-bit counter size is selected with the CMS bit in the timer control register (CMWCR), bits 15 to 0 in the CMWCNT counter are valid. Since access to this register is in 32-bit units, when writing, write 32-bit values to it with 0000h in the higher-order bits. If a value other than 0000h is set in the higher-order bits, a value greater than 0000 FFFFh may be read when this register is read.

When the STR bit is set to 1, the CMWCNT counter starts counting. When the STR bit is set to 0, the CMWCNT counter retains the value immediately before a stop of counting and stops counting.

Address(es): CMTW0.CMWCNT A008 0310h, CMTW1.CMWCNT A008 0390h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.5 Compare Match Constant Register (CMWCOR)

The CMWCOR register is a readable/writable register that specifies the time up to a compare match between the timer counter (CMWCNT) value and CMWCOR value. When the 16-bit counter size is selected with the CMS bit in the timer control register (CMWCR), bits 15 to 0 in this register are valid. Since access to this register is in 32-bit units, when writing, write 32-bit values to it with 0000h in the higher-order bits.
The cycle for compare matches is as follows.

Compare-match cycle = (setting of the CMWCOR register + 1) × counter-clock cycle*1

Note 1. This is a clock cycle set by the CMWCR.CKS[1:0] bits.

Address(es): CMTW0.CMWCOR A008 0314h, CMTW1.CMWCOR A008 0394h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

25.2.6 Input Capture Registers 0 and 1 (CMWICR0 and CMWICR1)

The CMWICR0 and CMWICR1 registers are read-only registers in which the CMWCNT counter value is stored when an input capture is generated.
When the 16-bit counter size is selected with the CMS bit in the timer control register (CMWCR), bits 15 to 0 in these registers are valid. Writing to these registers is invalid.

Address(es): CMTW0.CMWICR0 A008 0318h, CMTW0.CMWICR1 A008 031Ch,
CMTW1.CMWICR0 A008 0398h, CMTW1.CMWICR1 A008 039Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

25.2.7 Output Compare Registers 0 and 1 (CMWOCR0 and CMWOCR1)

The CMWOCR0 and CMWOCR1 registers are readable/writable registers that set the value to be compared when an output compare is generated.

When the 16-bit counter size is selected with the CMS bit in the timer control register (CMWCR), bits 15 to 0 of these registers become valid. Since access to this register is in 32-bit units, when writing, write 32-bit values to it with 0000h in the higher-order bits.

Address(es): CMTW0.CMWOCR0 A008 0320h, CMTW0.CMWOCR1 A008 0324h, CMTW1.CMWOCR0 A008 03A0h, CMTW1.CMWOCR1 A008 03A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

25.2.8 Digital Noise Filter Control Register 0 (NFCR0)

The NFCR0 register controls digital noise filters for input capture signals (TICn, n = 0, 1) of CMTW0.
The NFCR0 register should be set while the CMTW0.CMWCNT counter operation is stopped.

Address(es): CMTW.NFCR0 A008 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	NFCS0[1:0]		NF1EN	NF0EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NF0EN	Digital Noise Filter Enable 0	0: The digital noise filter for the TIC0 pin is disabled. 1: The digital noise filter for the TIC0 pin is enabled.	R/W
b1	NF1EN	Digital Noise Filter Enable 1	0: The digital noise filter for the TIC1 pin is disabled. 1: The digital noise filter for the TIC1 pin is enabled.	R/W
b3, b2	NFCS0 [1:0]	Digital Noise Filter Clock Select 0	b3 b2 0 0: PCLKD/1 0 1: PCLKD/8 1 0: PCLKD/32 1 1: PCLKD/64	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NF0EN Bit (Digital Noise Filter Enable 0)

This bit enables or disables the noise filter for the TIC0 pin. Before changing the value of this bit, select the output compare function for the relevant pin in the timer I/O control register. Changing the value of the bit when the output compare function is not selected may lead to the internal generation of an unexpected edge.

NF1EN Bit (Digital Noise Filter Enable 1)

This bit enables or disables the noise filter for the TIC1 pin. Before changing the value of this bit, select the output compare function for the relevant pin in the timer I/O control register. Changing the value of the bit while the output compare function is not selected may lead to the internal generation of an unexpected edge.

NFCS0[1:0] Bits (Digital Noise Filter Clock Select 0)

These bits select the sampling clock for the digital noise filter of CMTW0.
The input-capture signal is sampled on rising edges of the selected clock signal. If the sampled levels match three times in a row, the given level is regarded as the input-capture signal. If the levels do not match, the existing value is retained.
After setting these bits, wait for two selected sampling periods before selecting the input capture function.

25.2.9 Digital Noise Filter Control Register 1 (NFCR1)

The NFCR1 register controls digital noise filters for input capture signals (TICn, n = 2, 3) of CMTW1.
The NFCR1 register should be set while the CMTW1.CMWCNT counter operation is stopped.

Address(es): CMTW.NFCR1 A008 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	NFCS1[1:0]		NF3EN	NF2EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	NF2EN	Digital Noise Filter Enable 2	0: The digital noise filter for the TIC2 pin is disabled. 1: The digital noise filter for the TIC2 pin is enabled.	R/W
b1	NF3EN	Digital Noise Filter Enable 3	0: The digital noise filter for the TIC3 pin is disabled. 1: The digital noise filter for the TIC3 pin is enabled.	R/W
b3, b2	NFCS1 [1:0]	Digital Noise Filter Clock Select 1	b3 b2 0 0: PCLKD/1 0 1: PCLKD/8 1 0: PCLKD/32 1 1: PCLKD/64	R/W
b31 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NF2EN Bit (Digital Noise Filter Enable 2)

This bit enables or disables the noise filter for the TIC2 pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register before doing so.

NF3EN Bit (Digital Noise Filter Enable 3)

This bit enables or disables the noise filter for the TIC3 pin. Since changing the value of the bit may lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the timer I/O control register before doing so.

NFCS1[1:0] Bits (Digital Noise Filter Clock Select 1)

These bits select the sampling clock for the digital noise filter of CMTW1.
The input-capture signal is sampled on rising edges of the selected clock signal. If the sampled levels match three times in a row, the given level is regarded as the input-capture signal. If the levels do not match, the existing value is retained.
After setting these bits, wait for two selected sampling periods before selecting the input capture function.

25.2.10 ECM Dynamic Mode Error Output Select Register (ECDMESLR)

The ECDMESLR register is used to select the error output signal in error control module (ECM) dynamic mode.

Address(es): CMTW.ECDMESLR A008 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMERSL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	DMERSL [2:0]	ECM Dynamic Mode Error Output Select	b2 b1 b0 0 0 0: Fixed to 0 (an output compare signal not used) 0 0 1: CMTW0.CMWCOR0 output compare signal 0 1 0: CMTW0.CMWCOR1 output compare signal 0 1 1: CMTW1.CMWCOR0 output compare signal 1 0 0: CMTW1.CMWCOR1 output compare signal Settings other than above are prohibited.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMERSL[2:0] Bit (ECM Dynamic Mode Error Output Select)

These bits are used to select the error output signal in ECM dynamic mode from among the CMTW output compare signals.

For details of ECM dynamic mode, see section 42, Error Control Module (ECM).

25.3 Operation

When the CMWCR register is set and then the STR bit in CMWSTR is set to 1, the CMTW starts counter operation. Setting the CMWSTR.STR bit to 0 enables the CMWCNT counter to retain the value immediately before a stop of counting and stop counting. Setting CMWIOR register enables using the compare match function, input capture input function, and output compare output function.

25.3.1 Period Counting Operation

When the internal clock is selected by using the CMWCNT.CKS[1:0] bits and the CMWSTR.STR bit is set to 1, the CMWCNT counter starts counting up cycles of the selected clock. When the CCLR[2:0] bits in CMWCR are set so that CMWCNT should be cleared by a specific counter clearing source and the counter clearing source is generated, the CMWCNT counter is cleared to 0000 0000h and continues incrementing. When the CCLR[2:0] bits are set so that CMWCNT should not be cleared by any specific counter clearing source, the CMWCNT counter is cleared to 0000 0000h only when an overflow is generated (FFFF FFFFh → 0000 0000h (when the counter size is 32 bits) or 0000 FFFFh → 0000 0000h (when the counter size is 16 bits)) and continues incrementing.

25.3.2 Compare Match Function

When the values of the CMWCNT counter and CMWCOR register match, a compare match interrupt (CMWI) is generated. The CMWCNT counter operates as follows according to the setting of CMWCR.CCLR[1:0].

1. When CMWCR.CCLR[2:0] = 000b
   When the values of the CMWCNT counter and CMWCOR register match, the CMWCNT counter is cleared to 0000 0000h. The CMWCNT counter then restarts counting up from 0000 0000h.
2. When CMWCR.CCLR[2:0] ≠ 000b
   Even when the values of the CMWCNT counter and CMWCOR register match, the CMWCNT counter is not cleared to 0000 0000h but continues counting up until the clearing condition set in CMWCR.CCLR[1:0] is satisfied or the value of the counter reaches FFFF FFFFh (when the size of the counter is 32 bits) or ****FFFFh (when the size of the counter is 16 bits).
   The CMWCNT counter is then cleared to 0000 0000h and restarts counting up from 0000 0000h.

Figure 25.2 shows an example of procedure for setting compare match operation.

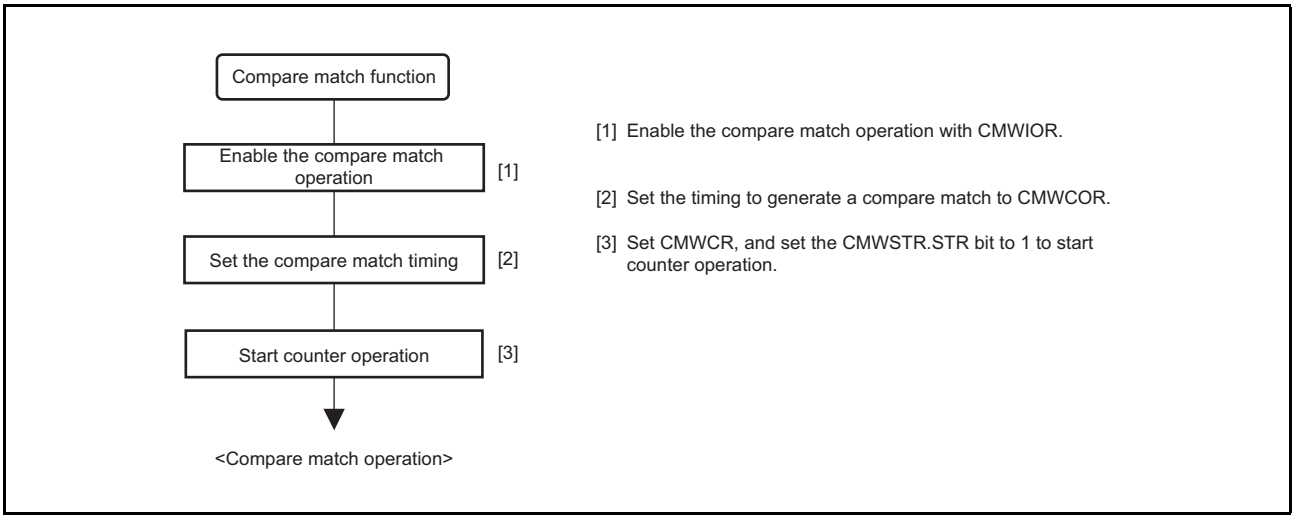


Figure 25.2 Procedure for Setting Compare Match Operation

Figure 25.3 shows an example when compare match with CMWCOR is set as a counter clearing source.

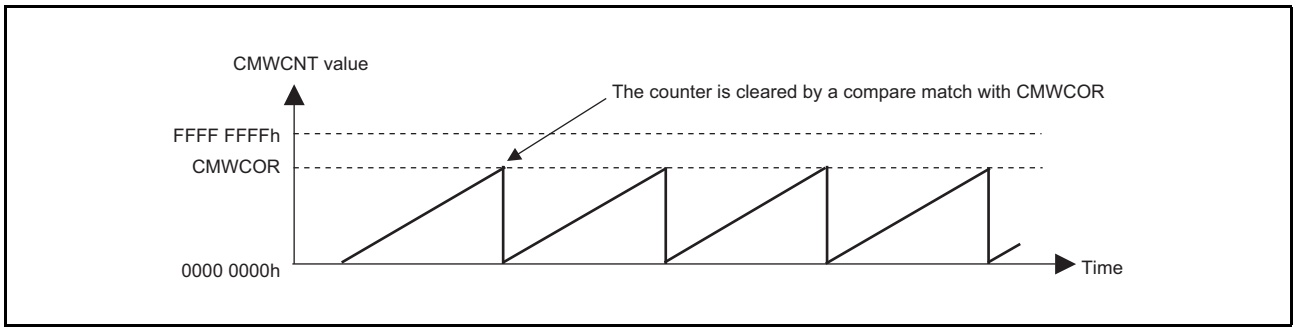


Figure 25.3 Example of Compare Match Operation

Figure 25.4 shows an example when CMWCOR is set to FFFF FFFFh and an overflow is detected.

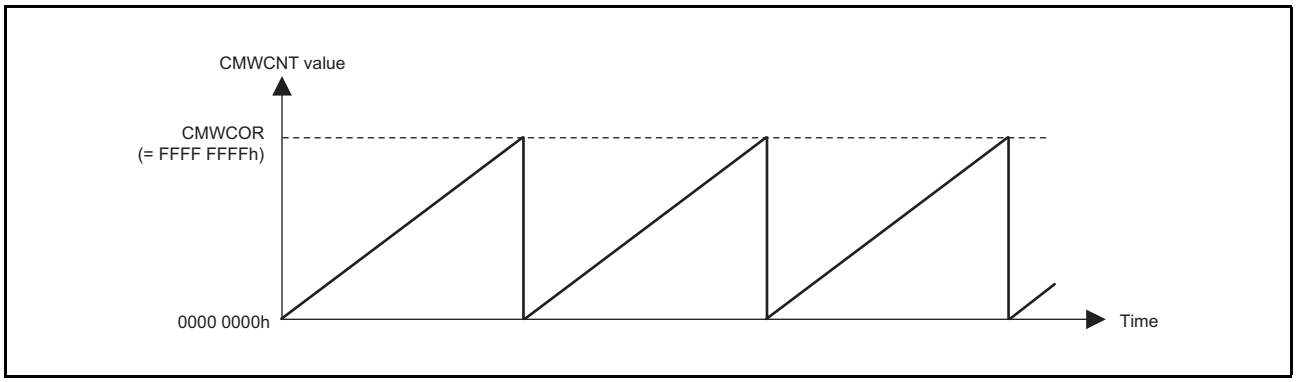


Figure 25.4 Example of Compare Match Operation (Overflow Detected)

25.3.3 Output Compare Function

Using the output compare function, toggle output from the relevant output pins can be provided. When the CMWCNT counter value matches either of the values of CMWOCR0 or CMWOCR1 register, the output compare interrupt (OC0I or OC1I) is generated. The CMWCNT counter operates as follows according to the setting of CMWCR.CCLR[2:0].

1. When CMWCR.CCLR[2:0] = 110b
   When the values of the CMWCNT counter and CMWOCR0 register match, the CMWCNT counter is cleared to 0000 0000h. The CMWCNT counter then restarts counting up from 0000 0000h.
2. When CMWCR.CCLR[2:0] = 111b
   When the values of the CMWCNT counter and CMWOCR1 register match, the CMWCNT counter is cleared to 0000 0000h. The CMWCNT counter then restarts counting up from 0000 0000h.
3. When CMWCR.CCLR[2:0] ≠ 110b or 111b
   Even when the values of the CMWCNT counter and CMWOCR0 or CMWOCR1 register match, the CMWCNT counter is not cleared to 0000 0000h but continues counting up until the clearing condition set in CMWCR.CCLR[2:0] is satisfied or the value of the counter reaches FFFF FFFFh (when the size of the counter is 32 bits) or ****FFFFh (when the size of the counter is 16 bits). The CMWCNT counter is then cleared to 0000 0000h and restarts counting up from 0000 0000h.

Figure 25.5 shows an example of procedure for setting output compare operation.

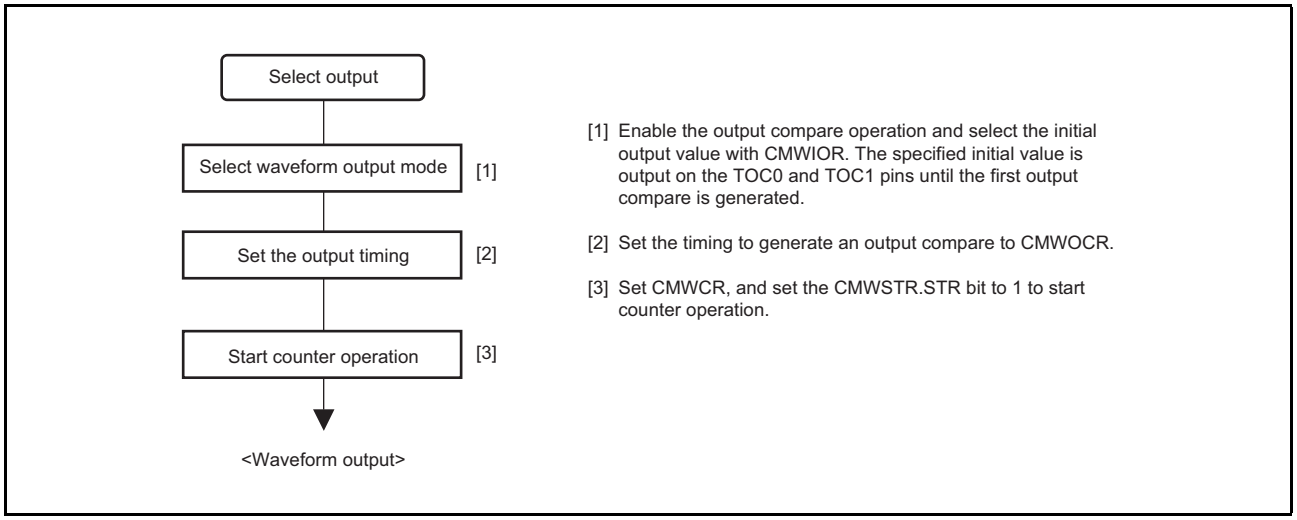


Figure 25.5 Procedure for Setting Output Compare Operation

Figure 25.6 shows an example when the counter is cleared upon compare match with CMWOCR1 register and toggle outputs are provided from the TOC0 and TOC1 pins.

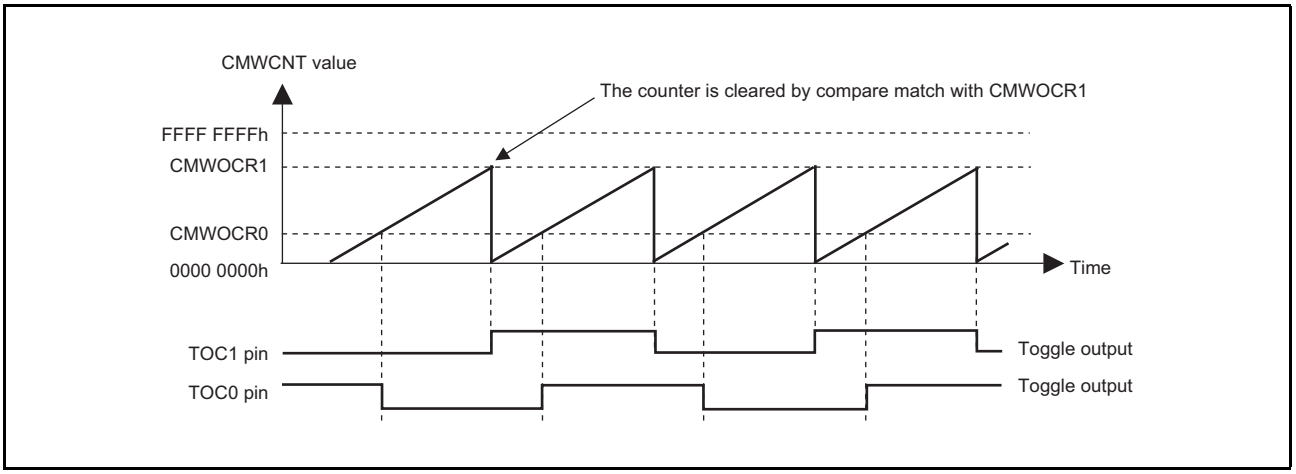


Figure 25.6 Example of Output Compare Operation

25.3.4 Input Capture Function

Through detecting the edge on the TIC0 and TIC1 pin input, the CMWCNT counter value can be transferred to CMWICR0 and CMWICR1 registers, respectively. The edges to be detected can be selected from among the rising edge alone, falling edge alone, and both the rising and falling edges. When the CMWCNT counter value is transferred to CMWICR0 or CMWICR1 register using the input capture function, an input compare interrupt (IC0I or IC1I) is generated. The CMWCNT counter operates as follows according to the setting of CMWCR.CCLR[2:0].

1. When CMWCR.CCLR[2:0] = 100b
   When the CMWCNT counter value is transferred to CMWICR0 using the input capture operation, the CMWCNT counter is cleared to 0000 0000h.
   The CMWCNT counter then restarts counting up from 0000 0000h.
2. When CMWCR.CCLR[2:0] = 101b
   When the CMWCNT counter value is transferred to CMWICR1 using the input capture operation, the CMWCNT counter is cleared to 0000 0000h.
   The CMWCNT counter then restarts counting up from 0000 0000h.
3. When CMWCR.CCLR[2:0] ≠ 100b or 101b
   Even when the CMWCNT counter value is transferred to CMWICR0 or CMWICR1 using the input capture operation, the CMWCNT counter is not cleared to 0000 0000h but continues counting up until the clearing condition set in CMWCR.CCLR[2:0] is satisfied or the value of the counter reaches FFFF FFFFh (when the size of the counter is 32 bits) or ****FFFFh (when the size of the counter is 16 bits). The CMWCNT counter is then cleared to 0000 0000h and restarts counting up from 0000 0000h.

Figure 25.7 shows an example of procedure for setting input capture operation.

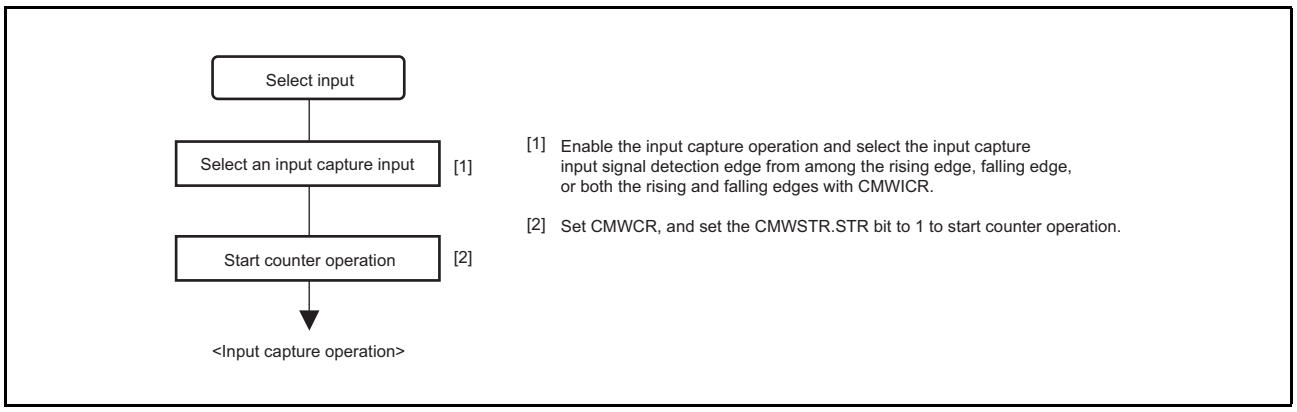


Figure 25.7 Procedure for Setting Input Capture Operation

Figure 25.8 shows an example in which both the rising and falling edges are selected for the TIC0 pin input capture input edge and the falling edge for the TIC1 pin, and the CMWCNT counter is cleared by a CMWICR1 register input capture.

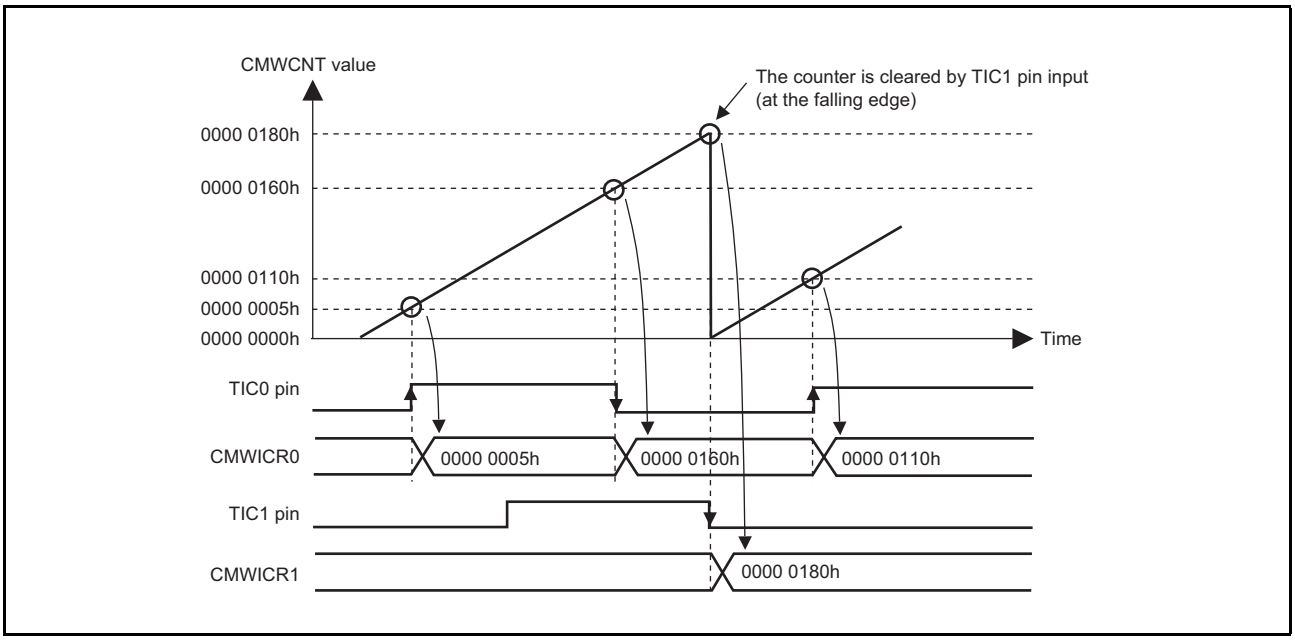


Figure 25.8 Example of Input Capture Operation

25.3.5 Counter Size

With the CMTW, either 16 or 32 bits can be selected as the counter size by using the CMWSTR.CMS bit. When the counter is used as a 32-bit counter, set the CMWCOR, CMWOCR0, or CMWOCR1 register to the desired values in 32-bit units. In reading, all 32 bits of CMWICR0 and CMWICR1 are valid. When the counter is used as a 16-bit counter, a 32-bit value should be set to the CMWCOR register with 0000h in the higher-order bits. Similarly, a 32-bit value should be set to CMWOCR0 and CMWOCR1 registers with 0000h in the higher-order bits.
A 32-bit value with 0000h in the higher-order bits is read from CMWICR0 and CMWICR1 registers.

25.3.6 Count Timing based on CMWCNT

One of four clocks (PCLKD/8, PCLKD/32, PCLKD/128, and PCLKD/512) obtained by dividing the peripheral clock (PCLKD) can be selected with the CMWCR.CKS[1:0] bits. Figure 25.9 shows the timing.

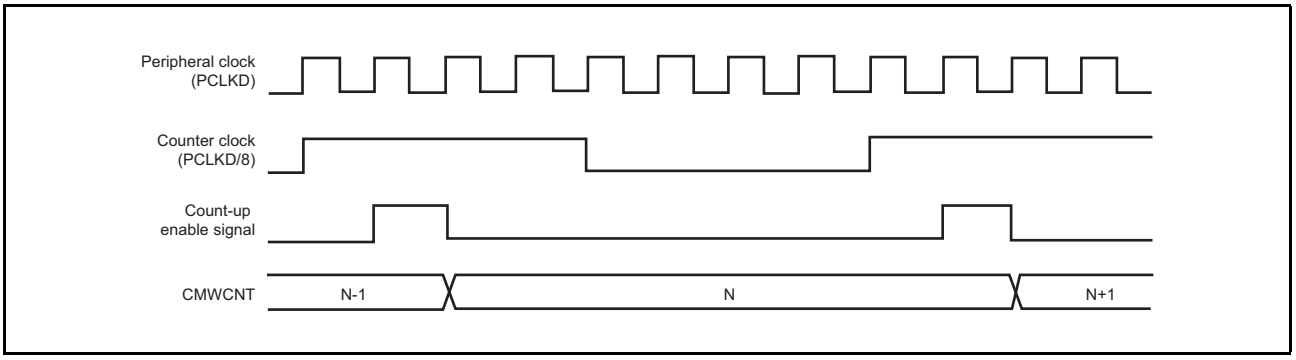


Figure 25.9 Count Timing (PCLKD/8)

25.3.7 Output Compare Output Timing

A compare match signal is generated in the last state in which the CMWOCR register and CMWCNT counter values match (the CMWCNT counter value is updated immediately after the state). That is, the compare match signal is not generated if the CMWCNT counter clock is not input after a match between the CMWOCR register and CMWCNT counter values. When a compare match signal is generated, the output compare output pin (TOC) changes in accord with the setting of the OC0 or OC1 bit in the CMWIOR register. Figure 25.10 shows output compare output timing.

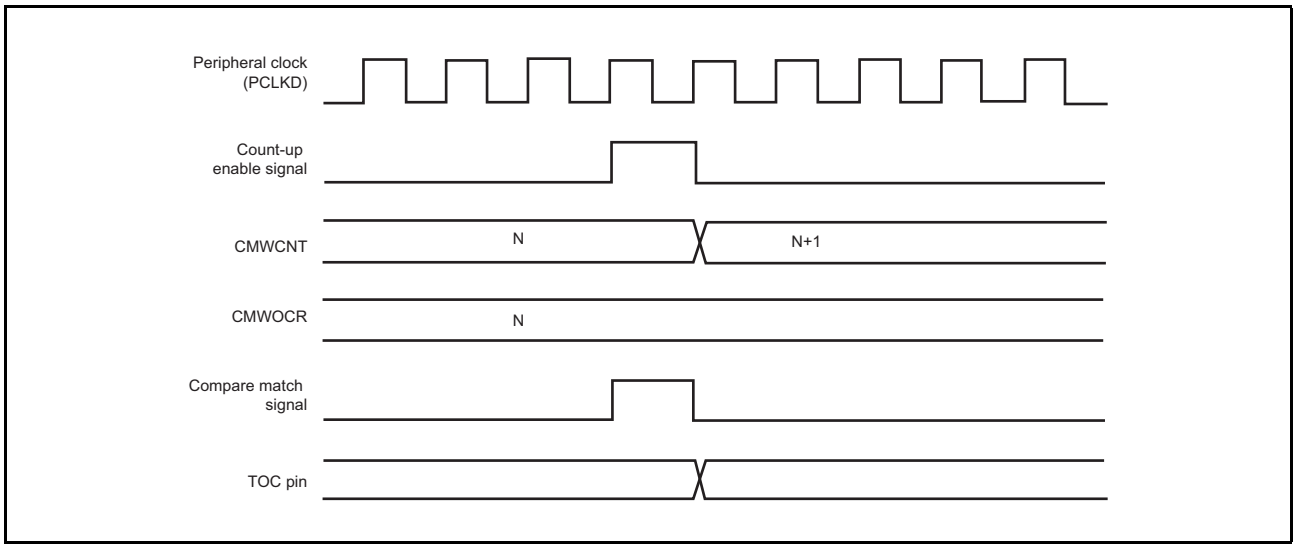


Figure 25.10 Output Compare Output Timing

25.3.8 Input Capture Signal Timing

Figure 25.11 shows the input capture timing.

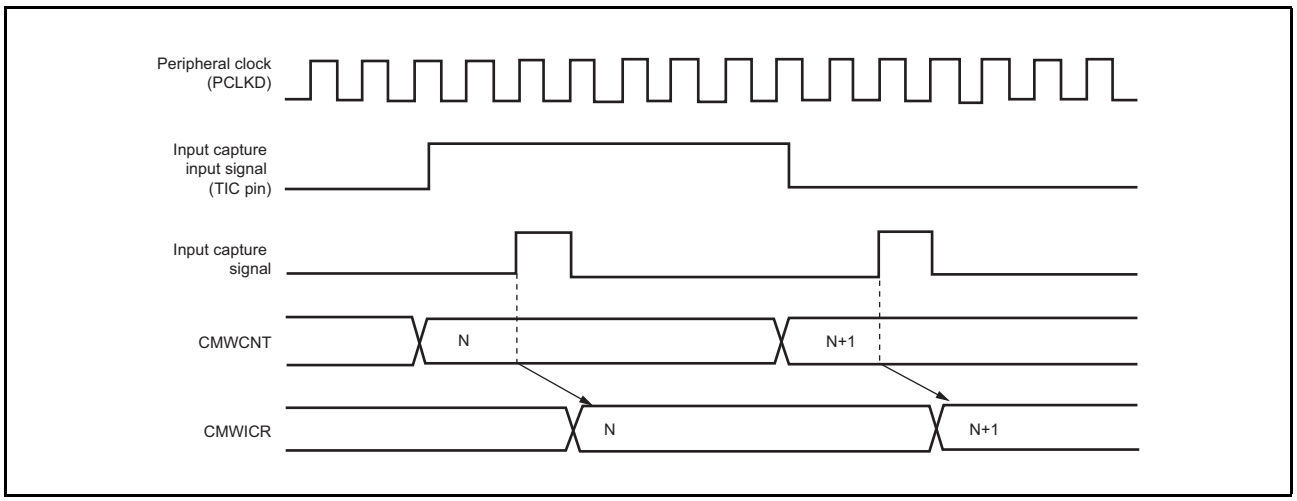


Figure 25.11 Input Capture Input Signal Timing

25.3.9 Digital Noise Filtering

The noise filter samples CMTW input-capture signals at the frequency of the sampling clock and the pulses with levels that only match once or twice are removed.
The digital noise filtering functionality includes enabling and disabling of the noise filtering for each pin. Figure 25.12 shows the timing of digital noise filtering.

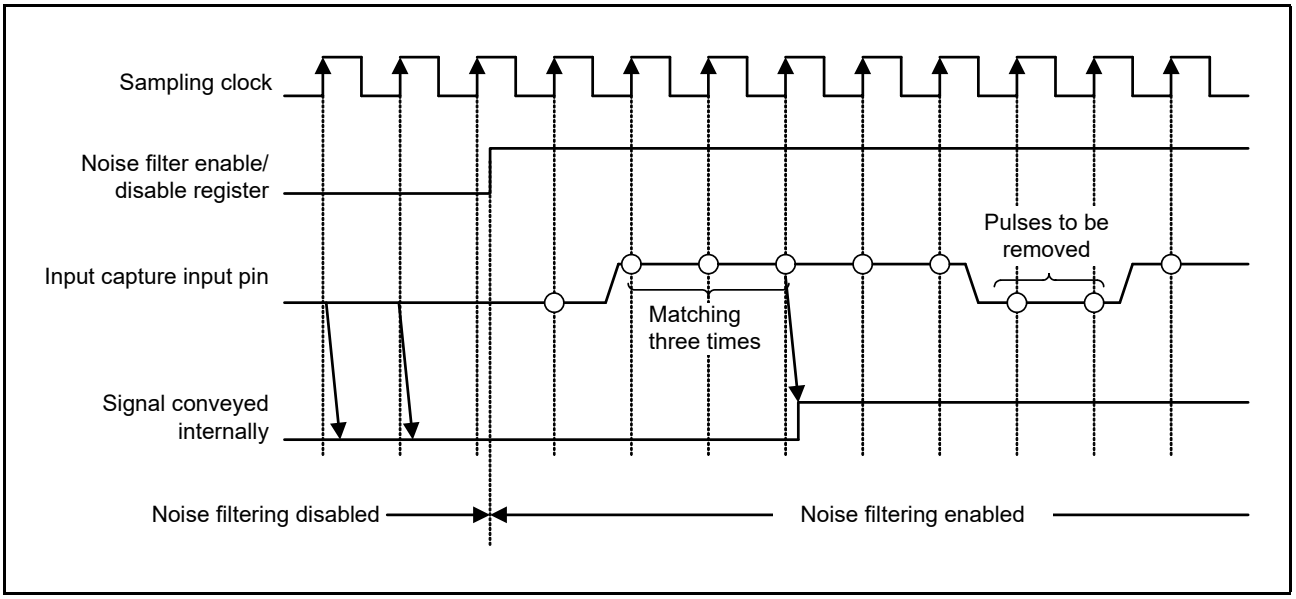


Figure 25.12 Timing of Digital Noise Filtering

If digital noise filtering is enabled, input capture proceeds on edges of the noise filtered signal after a delay of (minimum sampling interval × 2 + PCLKD) due to noise filtering of the input capture input.

25.3.10 ECM Dynamic Mode Error Output Selection

This LSI, uses an output compare signal of CMTW as an error output signal in ECM dynamic mode. That is, one of the CMTW output compare signals is selected as the error output in ECM dynamic mode.
When an actual output compare signal of CMTW is to be output to the ECM, set up the output comparison for the CMTW channels to be used in this way before setting the ECDMESLR register.
For the procedure for setting up output comparison, see section 25.3.3, Output Compare Function.
For details of ECM dynamic mode, see section 42, Error Control Module (ECM).

25.4 Interrupts

25.4.1 CMTW Interrupt Sources and DMAC Transfer Requests

The CMTW has five interrupt sources: two input capture interrupt requests (IC0In and IC1In), two output compare interrupt requests (OC0In and OC1In), and a compare match interrupt request (CMWIn) (n = 0, 1).
Table 25.3 shows the interrupt sources and priority. The interrupt sources can be enabled or disabled using the IC0IE, IC1IE, OC0IE, OC1IE, and CMWIE bits in CMWCR and are separately issued to the interrupt controller.

Table 25.3 CMTW Interrupt Sources

Interrupt Source	Interrupt	Interrupt Enable Bit	DMAC Activation	Priority
CMWIn	Interrupt caused by compare match	CMWIE	Possible	High
IC0In	Interrupt caused by input capture 0	IC0IE	Possible	
IC1In	Interrupt caused by input capture 1	IC1IE	Possible	
OC0In	Interrupt caused by output compare 0	OC0IE	Possible	
OC1In	Interrupt caused by output compare 1	OC1IE	Possible	Low

25.4.2 Timing of Compare Match Interrupt Generation

When the values of the CMWCNT counter and CMWCOR register match, a compare match interrupt (CMWI) is generated. The compare match signal is generated at the end of the cycle where the values matched (i.e. when the CMWCNT counter is updated from the matching counter value). The compare match signal, therefore, is not generated until a further cycle of the input clock (PCLKD/8, PCLKD/32, PCLKD/128, or PCLKD/512) for the CMWCNT counter arrives after the values of the CMWCNT counter and CMWCOR register have matched. Figure 25.13 shows the timing of compare match interrupt generation.

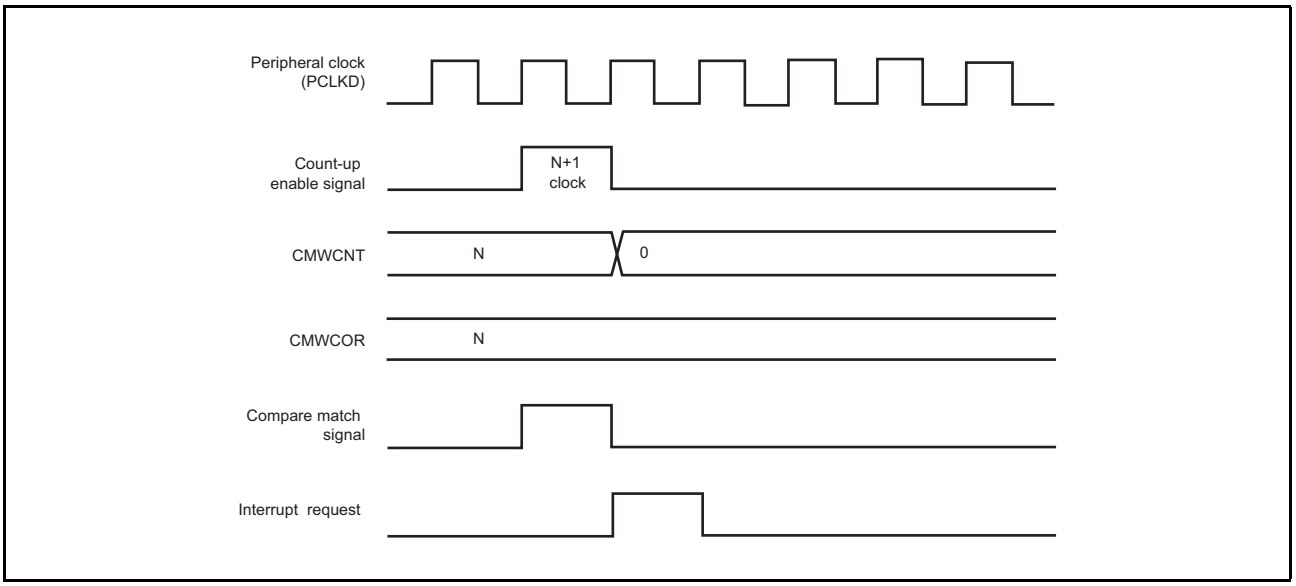


Figure 25.13 Timing of Compare Match Interrupt Generation

25.4.3 Timing of Output Compare Interrupt Generation

Figure 25.14 shows the timing of output compare interrupt generation.

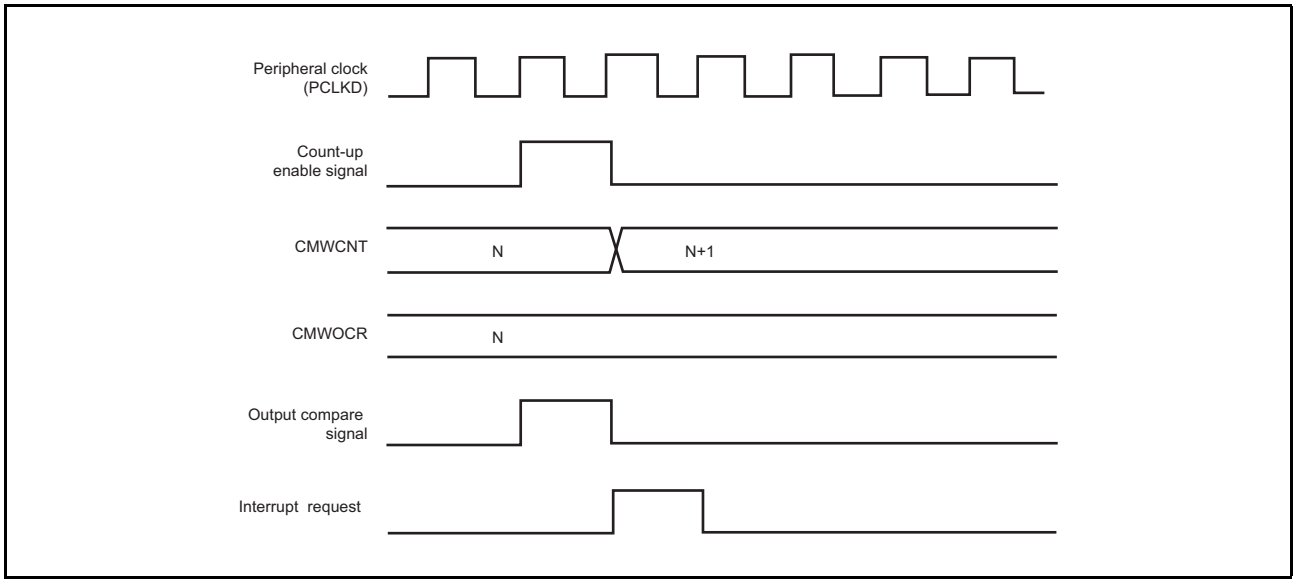


Figure 25.14 Timing of Output Compare Interrupt Generation

25.4.4 Timing of Input Capture Interrupt Generation

Figure 25.15 shows the timing of input capture interrupt generation.

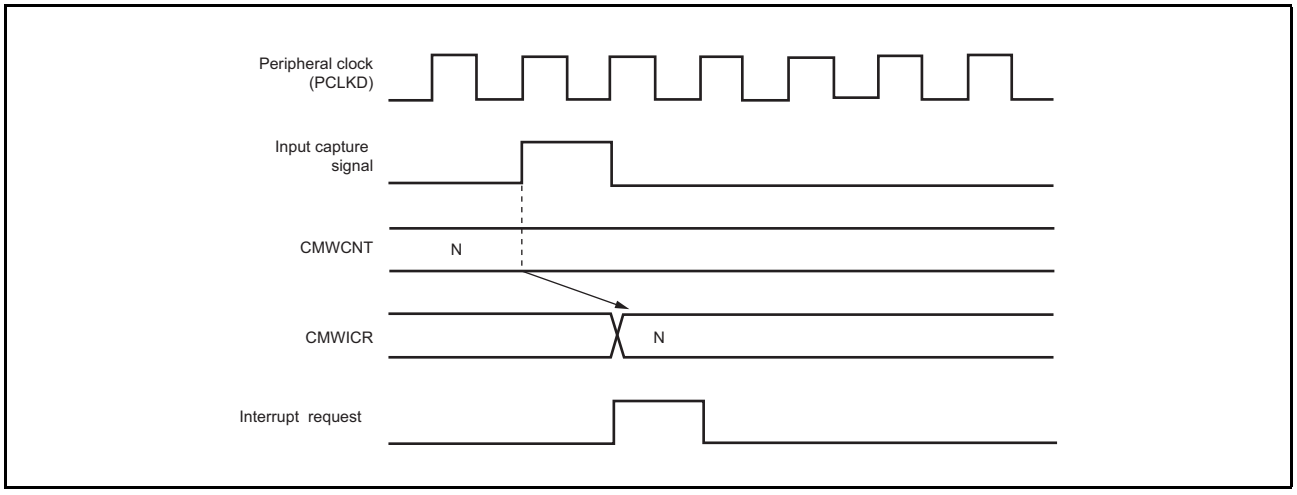


Figure 25.15 Timing of Input Capture Interrupt Generation

25.5 Event Link Operation

25.5.1 Issuing Events to the ELC

The CMTW can issue event signals to the event link controller (ELC) in response to the following events.

Compare Match Event

In response to a compare match, the CMTW simultaneously issues an interrupt request and a compare match event signal to the ELC. The event signal is issued regardless of the settings of the corresponding interrupt request enable bit (CMWCR.CMWIE bit).

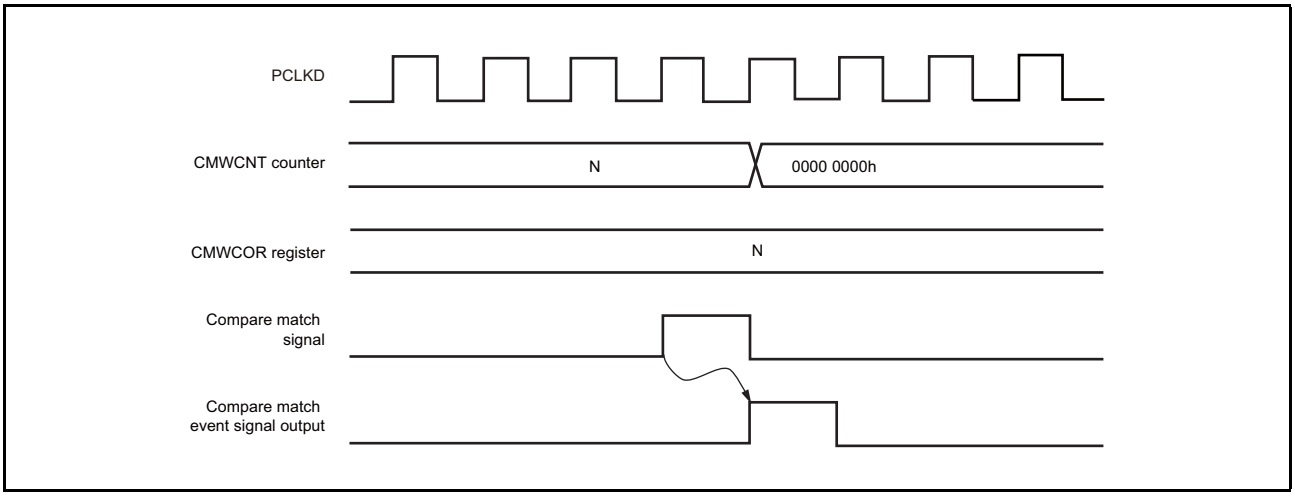


Figure 25.16 Timing of Issuing a Compare Match Event Signal

25.5.2 Actions on Acceptance of Event Signals from ELC

CMTW can respond with any of the following three actions when the action is set in the event link controller (ELC) and CMTW accepts the event signal.

(1) Start Counting

When an event signal is received while starting to count is the selected action, the STR bit in CMWSTR (the timer start register) is set to 1 and counting starts.

However, the event signal is ignored if it is accepted when the CMWSTR.STR bit has already been set to 1.

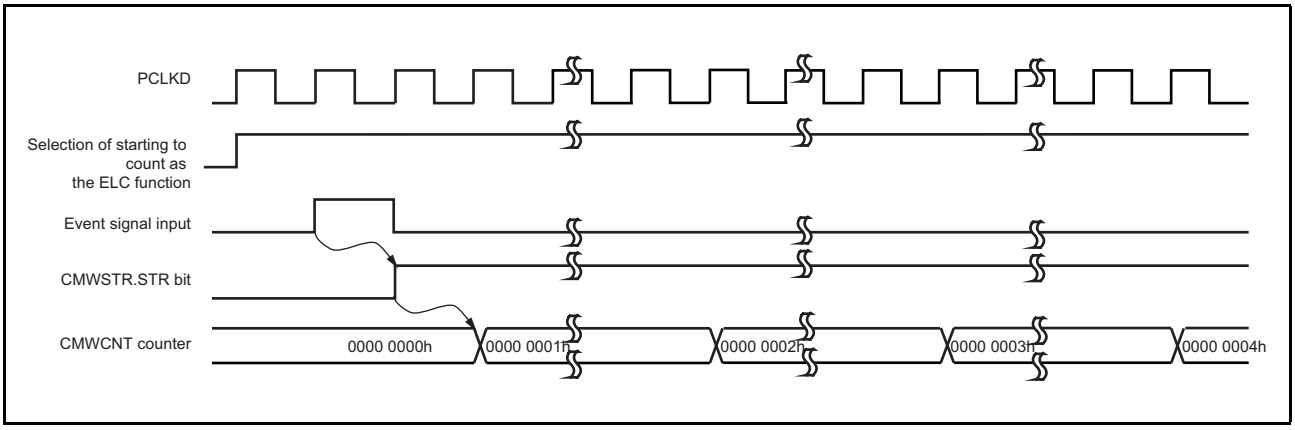


Figure 25.17 Starting to Count on Acceptance of the Event Signal

(2) Event Counting

When an event signal is received while counting events is the selected action, CMWCNT (the timer counter) is incremented. In this case, however, the STR bit in CMWSTR (the timer start register) must be set to 1 before the event signal is received.

In event counting, the setting of the CKS[1:0] bit in CMWCR (the timer control register) is not effective.

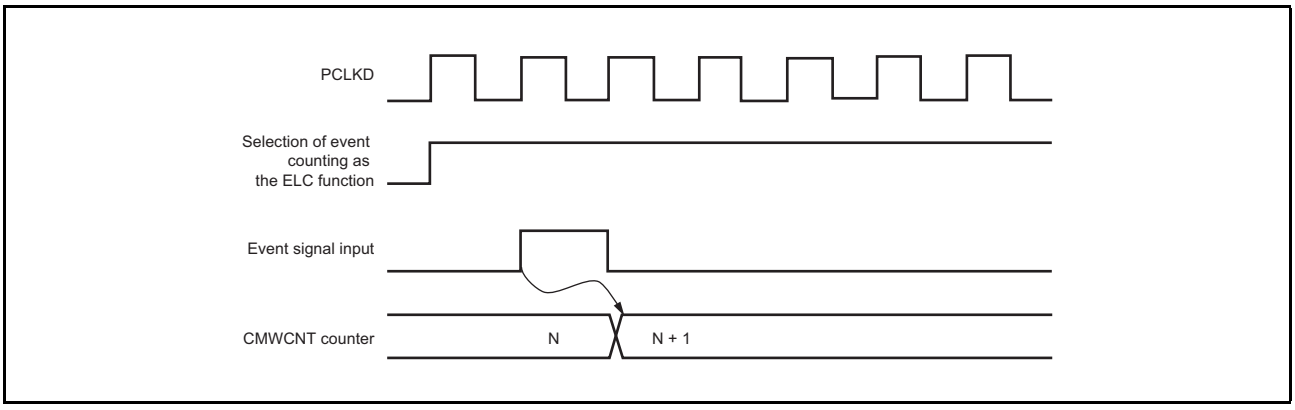


Figure 25.18 Counting an Event on Acceptance of the Event Signal

(3) Clear a Counter

Clearing of the CMTW counter is selected in the ELOPH register of the ELC. When the event specified in the corresponding ELSRn register is generated, the timer counter (CMWCNT) is returned to its initial value (0000h). Counting continues, however, if the setting of the STR bit of the timer start register (CMWSTR) is 1 at this time, so counting can be automatically restarted in this way. A timing chart of restarting the counter is shown in Figure 25.19

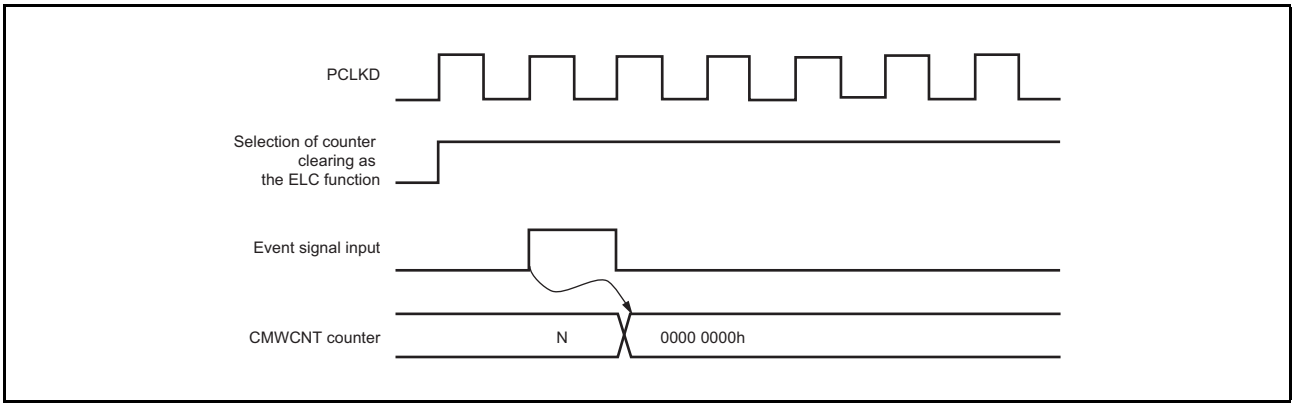


Figure 25.19 Restarting Counting on Acceptance of the Event Signal

25.6 Usage Notes

25.6.1 Module-Stop Function

The CMTW operation can be enabled or disabled by using the module-stop control register (MSTPCRA). In the initial setting, the CMTW is in the module-stop state. Register access is enabled by releasing the CMTW from the module-stop state. For details, refer to section 9, Low-Power Consumption Function.

25.6.2 Contention between CMWCNT Counter Writing and Compare Match

If the compare match signal is generated during CPU writing to the CMWCNT counter, the compare match request is output but the counter is not cleared since the CPU writing to the counter is given priority.
Figure 25.20 shows the timing of contention between CMWCNT counter writing and compare match.

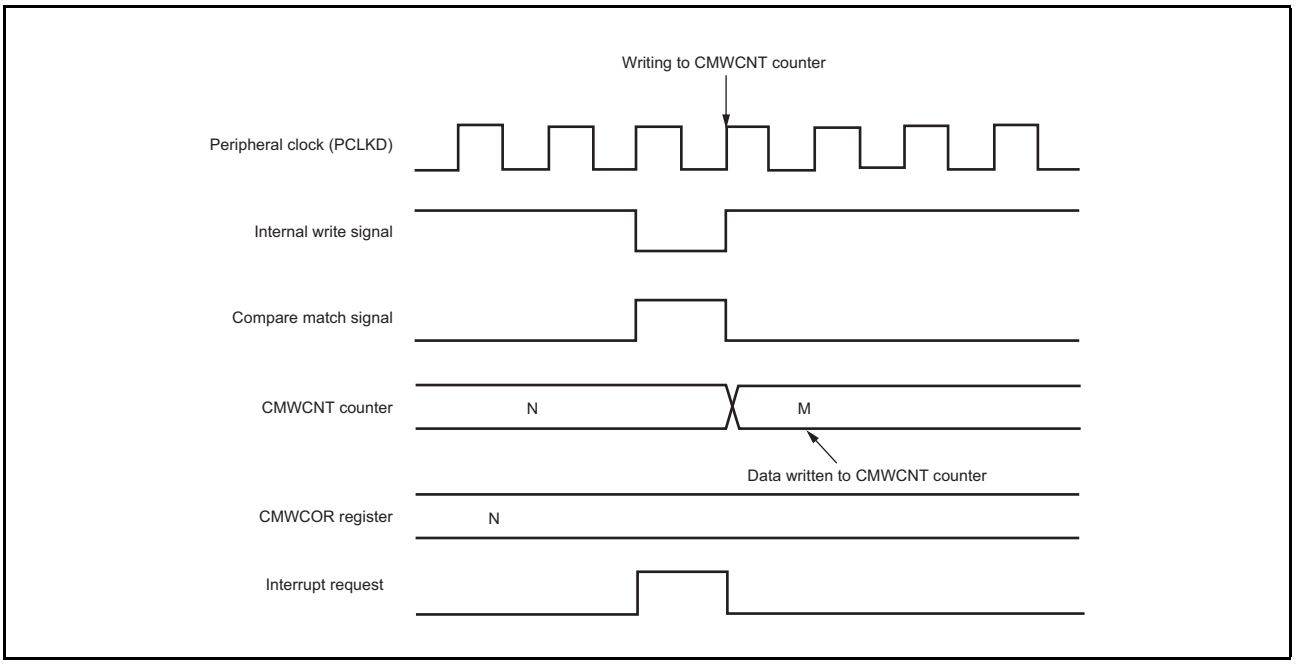


Figure 25.20 Contention between CMWCNT Counter Writing and Compare Match

25.6.3 Contention between CMWCNT Counter Writing and Incrementing or Clearing

In case of contention between incrementation or clearing of the CMWCNT counter and CPU writing to the counter, the counter is not actually incremented or cleared since the CPU writing to the CMWCNT counter is given priority.
Figure 25.21 shows the timing in the case of contention between writing to the CMWCNT counter and incrementation or clearing.

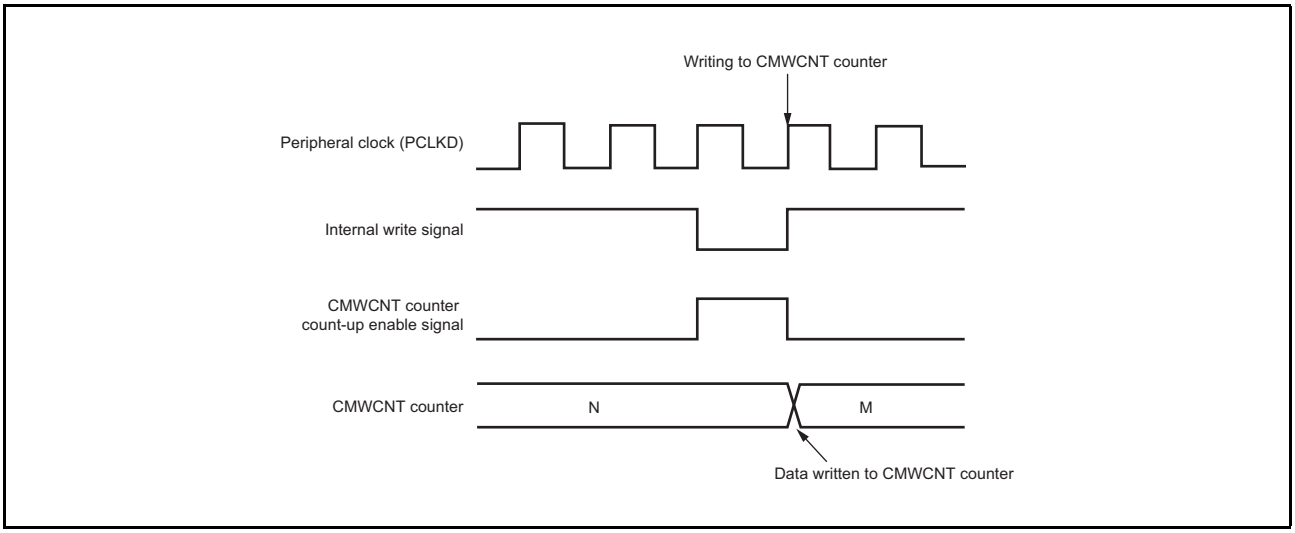


Figure 25.21 Contention between CMWCNT Counter Writing and Incrementing

25.6.4 Contention between CMWCOR Register Writing and Compare Match

If the compare match is generated during CPU writing to the CMWCOR register, the CPU writing to the CMWCOR register proceeds and also the compare match signal is output.
Figure 25.22 shows the timing of contention between CMWCOR register writing and compare match.

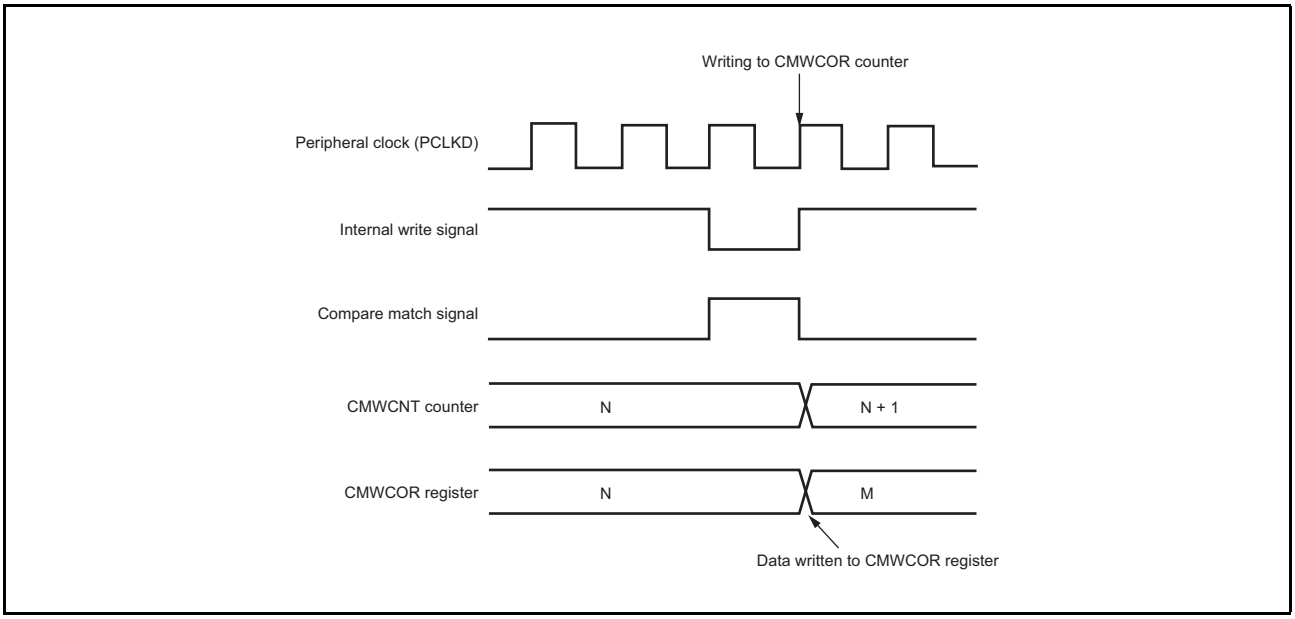


Figure 25.22 Contention between CMWCOR Register Writing and Compare Match

25.6.5 Contention between CMWOCR Register Writing and Compare Match

If the compare match is generated during CPU writing to the CMWOCR register, the CPU writing to the CMWOCR register proceeds and also the compare match signal is output.
Figure 25.23 shows the timing of contention between CMWOCR register writing and compare match.

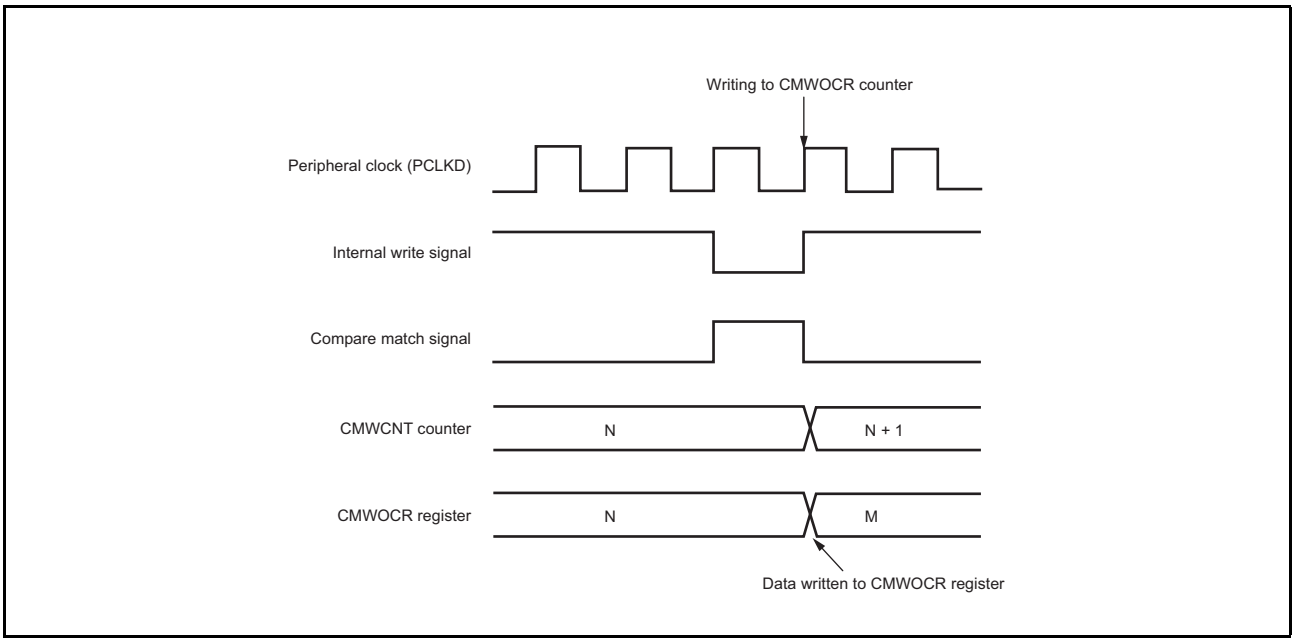


Figure 25.23 Contention between CMWOCR Register Writing and Compare Match

25.6.6 Contention between CMWCNT Counter Reading and Incrementing or Clearing

If the CMWCNT counter incrementing or clearing process occurs at the same time that the data of the CMWCNT counter is read, the value having been in the CMWCNT counter before incremented or cleared is read.
Figure 25.24 shows the timing of contention between the CMWCNT counter reading and incrementing.

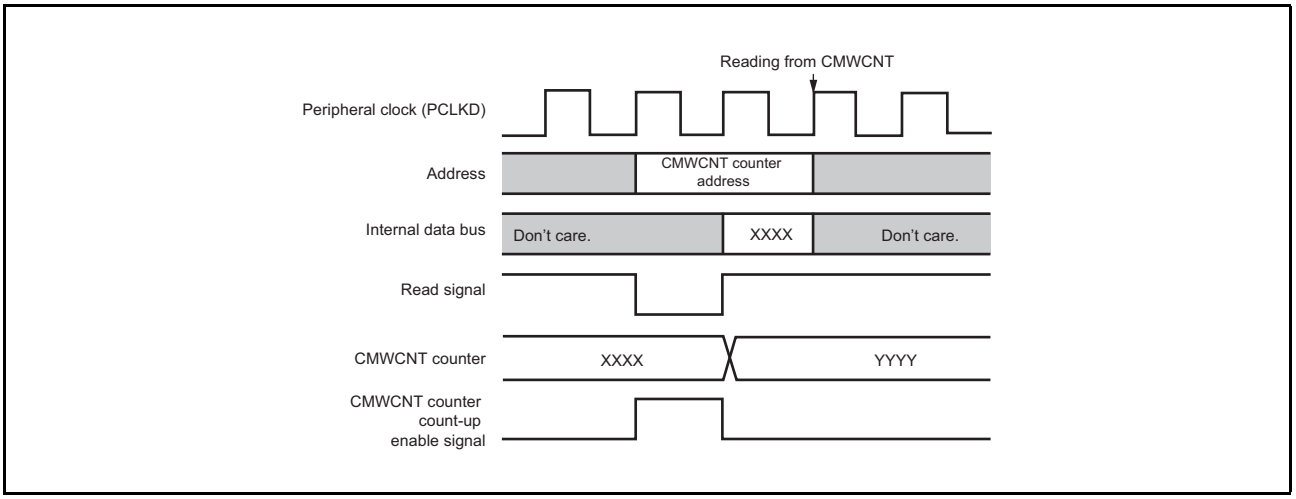


Figure 25.24 Contention between CMWCNT Counter Reading and Incrementing (When the Data Reading and Incrementing Process Occur Simultaneously)

25.6.7 Contention between CMWICR Register Reading and Input Capture

If the input capture signal is generated at the same time that the data of CMWICR register is read, the value having been in CMWICR register before updated by input capture transfer is read.

Figure 25.25 shows the timing of contention between CMWICR register reading and input capture.

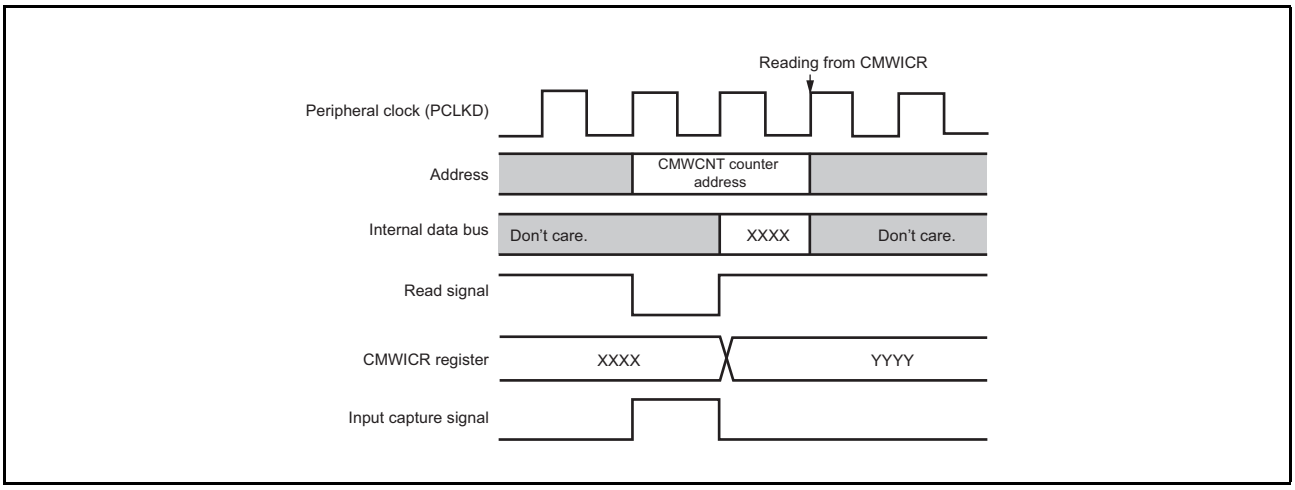


Figure 25.25 Contention between CMWICR Register Reading and Input Capture (When the Input Capture Signal and Read Signal are Generated Simultaneously)

25.6.8 Contention between Event Link Operation and Register Access

The followings are the notes on using CMTW for event link operations.
Table 25.4 summarizes contention between operations due to the event link, access to registers, and changes to the counter's state.

(1) Start Counting

When writing to the STR bit in the CMWSTR register and acceptance of the event signal are in contention, the CPU writing to the STR bit is ignored since setting of the STR bit to 1 in response to the event is given priority.

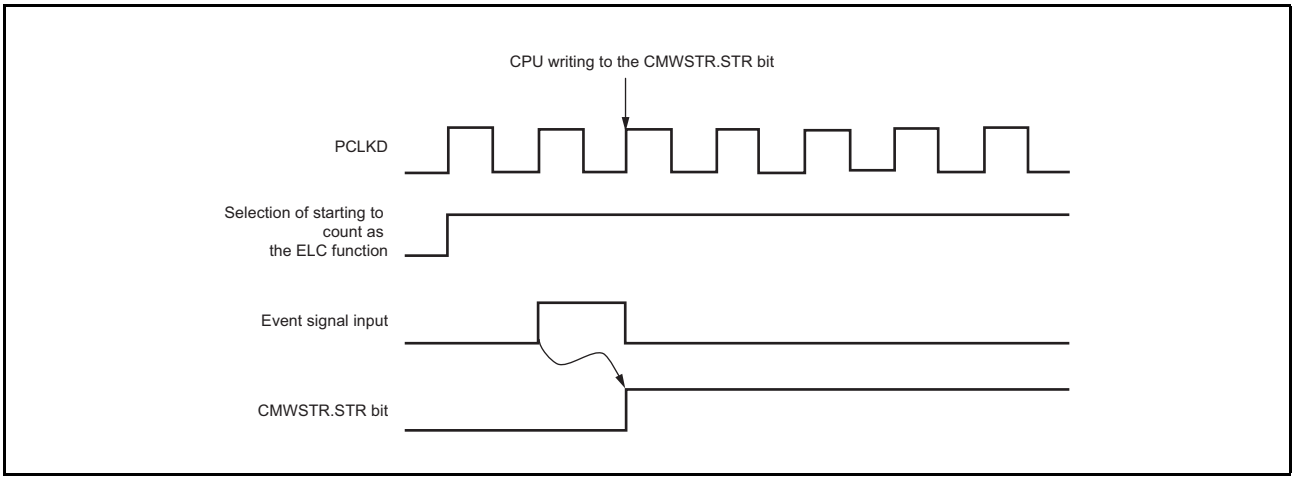


Figure 25.26 Contention between Event Acceptance and Register Access in Counting Start Operation

(2) Event Counting

When writing to CMWCNT (the timer counter) and acceptance of the event signal are in contention, the CPU writing to the CMWCNT counter is ignored since the counting operation in response to the event is given priority.

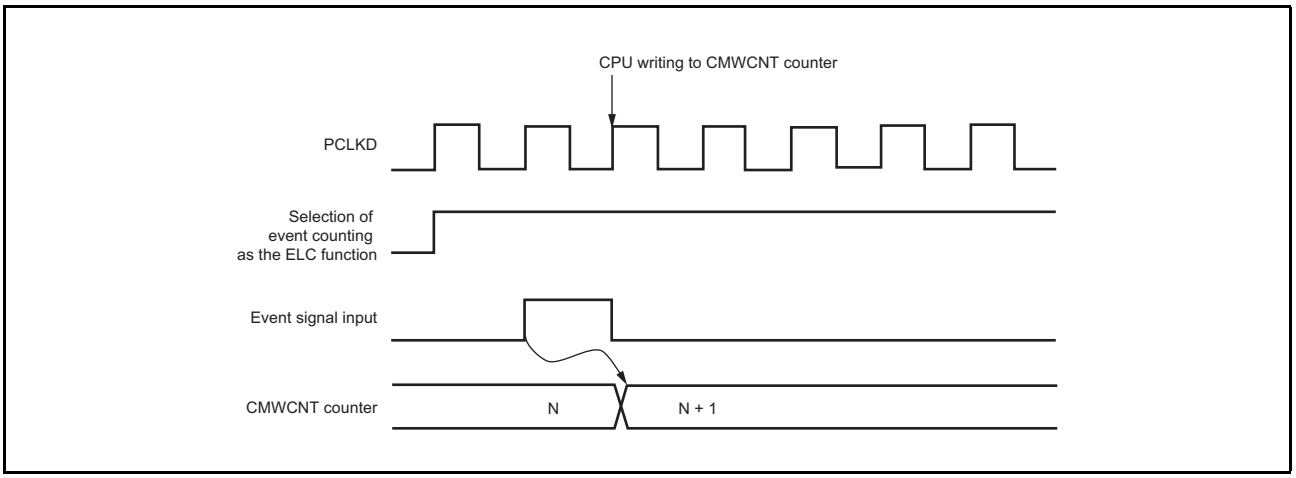


Figure 25.27 Contention between Event Acceptance and Register Access in Event Counting Operation

(3) Clear a Counter

When writing to CMWCNT (the timer counter) and acceptance of the event signal are in contention, the CPU writing to the CMWCNT counter is ignored since the counter value initialization in response to the event occurrence is given priority.

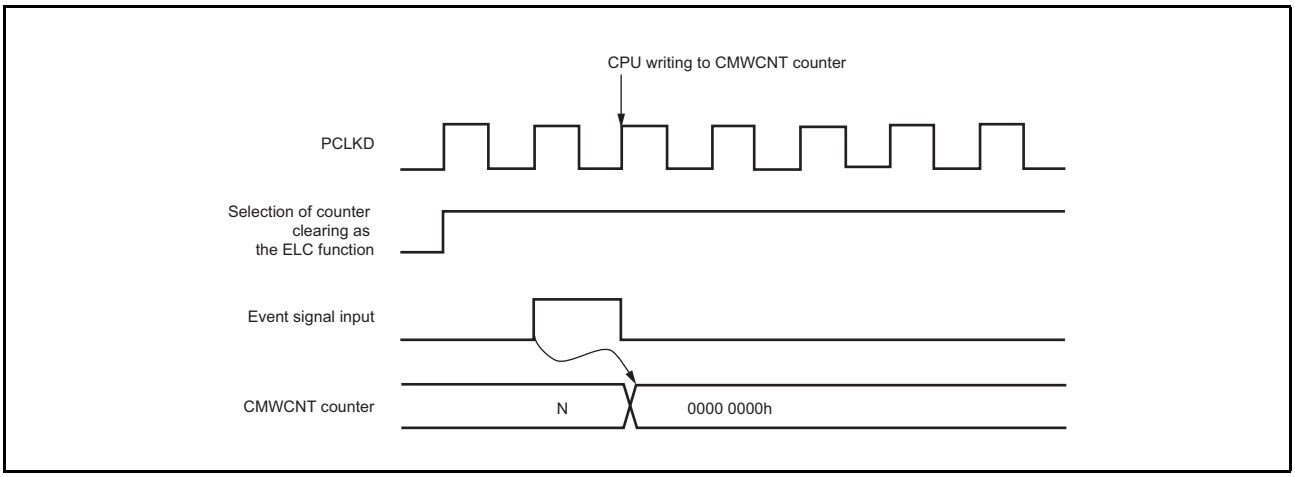


Figure 25.28 Contention between Event Acceptance and Register Access in Counting Clear Operation

Table 25.4 Summary of Contention between Operations Due to the Event Link, Access to Registers, and Changes to the Counter's State

Event Link Operation	Register Access	CMWCNT State	CMWICR0/1 State	Operation to be Performed
Counting start	Writing to CMWSTR.STR	Stopped state	—	Counting start
		Operating	—	Counting start
		Compare match	—	Counting start (CMWSTR.STR retains 1) and compare match
		Counting up	—	Counting start (CMWSTR.STR retains 1) and counting up
Event counting	Writing to CMWCNT	—	—	Event counting
	Writing to CMWCOR	Compare match	—	Compare match
Counting clear	Writing to CMWCNT	Other than compare match	—	Counting clear
	Writing to CMWCNT	Compare match	—	Compare match and counter clear
	(No access to registers)	Compare match	—	Compare match and counter clear
(No events)	Writing to CMWCNT	Compare match	—	Output of compare match interrupt request / Writing to CMWCNT
		Counting up	—	Writing to CMWCNT
	Writing to CMWCOR	Compare match	—	Compare match
	Writing to CMWOCR0	Output compare 0	—	Output compare 0
	Writing to CMWOCR1	Output compare 1	—	Output compare 1
	Reading from CMWCNT	Counting up	—	Counting up and reading of the previous value
	Reading from CMWICR0	—	Input capture 0	Input capture 0 and reading of the value before transfer
	Reading from CMWICR1	—	Input capture 1	Input capture 1 and reading of the value before transfer

26. Watchdog Timer (WDTA)

The watchdog timer (WDT) contains a 14-bit down-counter. If the counter underflows, an error notification to the error control module (ECM) is generated. The count value of the down-counter can be refreshed to the value after reset to enable counting to start again. Counter refreshing can be preformed during a period (the refresh-permitted period) you specify. If you perform refresh (register writing) outside of the permitted period, an error notification is generated and sent to the ECM. This enables detection of runaway of the program, taking the refresh interval into consideration. If underflow occurs or if refresh is performed outside of the refresh-permitted period, the WDT stops counting. Counting restarts after refresh is performed. (For details on refresh operation, see section 26.3.3, Refresh Operation.)
For details on the error control module (ECM), see section 42, Error Control Module (ECM).

26.1 Overview

WDT starts counting when refresh (register writing) is performed after reset is released.
Before starting the count, it is necessary to set the clock division ratio, the window start/end positions, and the timeout period in the WDT control register (WDTCR).
Table 26.1 lists the specifications of the WDT and Figure 26.1 shows a block diagram of the WDT.

Table 26.1 WDT Specifications

Item	Specifications
Number of internal channels	One channel (two channels for products incorporating an R-IN engine)
Count source	Peripheral clock (PCLKE)
Clock division ratio	Divide by 4, 64, 128, 512, 2048, or 8192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	Refresh (writing 00h and then FFh to the WDTRR register)
Conditions for stopping the counter	• Reset (the down-counter and other registers return to the values after reset) • A counter underflows or a refresh error occurs
Window function	Window start and end positions can be specified (refresh-permitted period)
Sources of sending an error notification to ECM	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.
WDT register control	• Selection of clock division ratio after refresh operation (WDTCR.CKS[3:0] bits) • Selection of timeout period of the watchdog timer (WDTCR.TOPS[1:0] bits) • Selection of window start position of the watchdog timer (WDTCR.RPSS[1:0] bits) • Selection of window end position of the watchdog timer (WDTCR.RPES[1:0] bits)

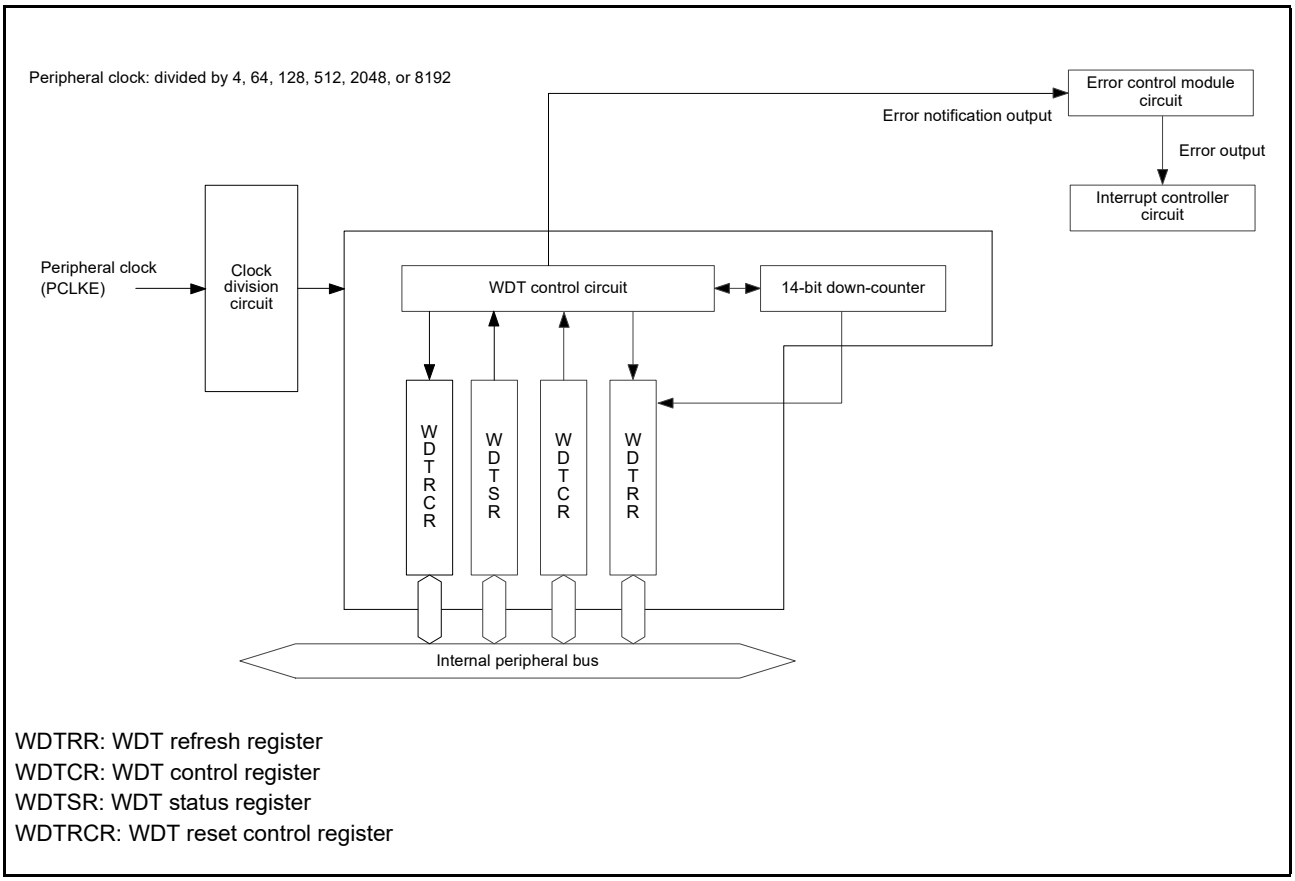


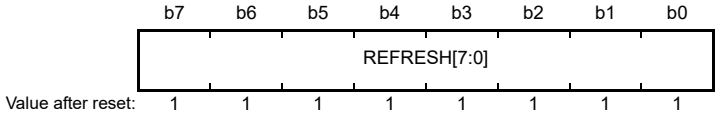
Figure 26.1 WDT Block Diagram

26.2 Register Descriptions

26.2.1 WDT Refresh Register (WDTRR)

The WDTRR register refreshes the down-counter of the WDT. To refresh the down-counter of the WDT, write 00h and then FFh (refresh operation) to the WDTRR register in the refresh-permitted period. After being refreshed, the down-counter starts counting down from the value specified with the WDTCR.TOPS[1:0] bits.
When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is always FFh.
For details on the refresh operation, see section 26.3.3, Refresh Operation.

Address(es): WDT0.WDTRR A008 0600h, WDT1.WDTRR A008 0620h



Note: For a reset by the WDT1, the values after a reset are the same as those on release from software reset 2. For details, see section 6, Reset.

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	REFRESH [7:0]	Refresh Register	The down-counter is refreshed by writing 00h and then writing FFh to this register.	R/W

26.2.2 WDT Control Register (WDTCR)

The WDTCR register allows you to select a timeout period before the down-counter underflows, a clock division ratio, and a window start/end position for refreshing. There are some restrictions on writing to this register. For details, see section 26.3.2, Control over Writing to the WDTCR and WDTRCR Registers.

Address(es): WDT0.WDTCR A008 0602h, WDT1.WDTCR A008 0622h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Note: For a reset by the WDT1, the values after a reset are the same as those on release from software reset 2. For details, see section 6, Reset.

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Selection	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh) Values within parentheses are down-count start values.	R/W
b3, b2	—	Reserved	These bits are read as 0 and cannot be modified.	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Selection	b7 b4 0 0 0 1: PCLKE/4 0 1 0 0: PCLKE/64 1 1 1 1: PCLKE/128 0 1 1 0: PCLKE/512 0 1 1 1: PCLKE/2048 1 0 0 0: PCLKE/8192 Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Selection	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified)	R/W
b11, b10	—	Reserved	These bits are read as 0 and cannot be modified.	R/W
b13, b12	RPSS[1:0]	Window Start Position Selection	These bits allow selection of a window start position of the down-counter from among 100%, 75%, 50%, and 25% of the counting period (assuming that the count start position as 100% and underflow occurrence as 0%). The period from the window start position to the window end position is the refresh-permitted period, and any other periods are the refresh-prohibited periods. Figure 26.2 shows the relation between the settings of the RPSS[1:0] and RPES[1:0] bits and the refresh-permitted and refresh-prohibited periods. b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified)	R/W
b15, b14	—	Reserved	These bits are read as 0 and cannot be modified.	R/W

TOPS[1:0] Bits (Timeout Period Selection)

These bits allow you to select a timeout period (period before the down-counter underflows) from among 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified by the CKS[3:0] bits as one cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (the number of peripheral clock (PCLKE) cycles) before the counter underflows.

Table 26.2 lists relations between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKE cycles.

CKS[3:0] Bits (Clock Division Ratio Selection)

These bits allow you to select a division ratio from among the peripheral clocks (PCLKE) divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, a counting period between 4,096 and 134,217,728 cycles of the peripheral clock (PCLKE) can be selected for the WDT.

RPES[1:0] Bits (Window End Position Selection)

These bits allow selection of a window end position from among 75%, 50%, 25%, and 0% of the counting period. The selected window end position should be a value smaller than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is valid.

The counter values of the window start and end positions specified by the RPES[1:0] and RPSS[1:0] bit settings vary according to the TOPS[1:0] bit setting.

Table 26.3 lists the counter values of the window start and end positions corresponding to the TOPS[1:0] bit setting.

RPSS[1:0] Bits (Window Start Position Selection)

These bits allow selection of a window start position of the down-counter from among 100%, 75%, 50%, and 25% of the counting period (assuming that the count start position as 100% and underflow occurrence as 0%). The period from the window start position to the window end position is the refresh-permitted period, and any other periods are the refresh-prohibited periods.

Figure 26.2 shows the relation between the settings of the RPSS[1:0] and RPES[1:0] bits and the refresh-permitted and refresh-prohibited periods.

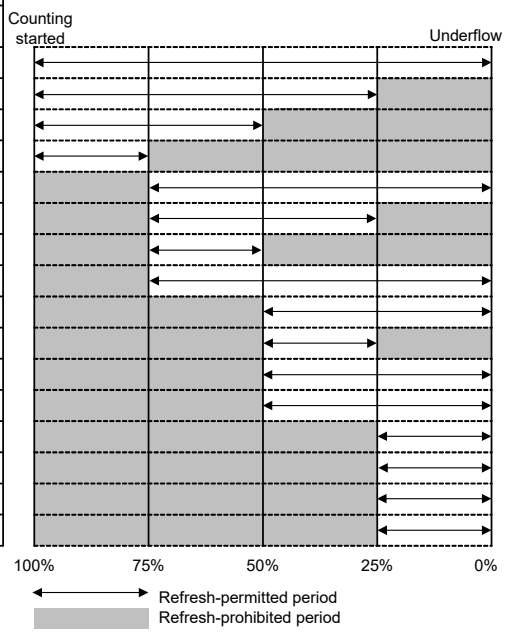
Table 26.2 Timeout Period Settings

CKS[3:0] Bits				TOPS[1:0] Bits				
b7	b6	b5	b4	b1	b0	Clock Division Ratio	Timeout Period (Number of Cycles)	No. of Peripheral Clock (PCLKE) Cycles @Count clock = PCLKE
0	0	0	1	0	0	Count clock/4	1024	4096
				0	1		4096	16384
				1	0		8192	32768
				1	1		16384	65536
0	1	0	0	0	0	Count clock/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	Count clock/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	1	0	0	0	Count clock/512	1024	524288
				0	1		4096	2097152
				1	0		8192	4194304
				1	1		16384	8388608
0	1	1	1	0	0	Count clock/2048	1024	2097152
				0	1		4096	8388608
				1	0		8192	16777216
				1	1		16384	33554432
1	0	0	0	0	0	Count clock/8192	1024	8388608
				0	1		4096	33554432
				1	0		8192	67108864
				1	1		16384	134217728

Table 26.3 Relationship between Timeout Period and Window Start/End Counter Values

TOPS[1:0] Bits		Timeout Period		Window Start/End Counter Value			
b1	b0	Cycles	Counter Value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 26.2 RPSS[1:0] and RPES[1:0] Bit Settings and the Refresh-Permitted and Refresh-Prohibited Periods

26.2.3 WDT Status Register (WDTSR)

The WDTSR register shows the counter value of the down-counter and whether an underflow or refresh error has occurred.

Address(es): WDT0.WDTSR A008 0604h, WDT1.WDTSR A008 0624h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: For a reset by the WDT1, the values after a reset are the same as those on release from software reset 2. For details, see section 6, Reset.

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred	R/(W)
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred	R/(W)

CNTVAL[13:0] Bits (Down-Counter Value)

Read these bits to confirm the value of the down-counter, but note that the read value may differ from the actual count by a value of one count.

UNDFF Flag (Underflow Flag)

Read this bit to confirm whether an underflow has occurred in the down-counter.
The value 1 indicates that the down-counter has underflowed. The value 0 indicates that the down-counter has not underflowed.
Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

REFEF Flag (Refresh Error Flag)

Read this bit to confirm whether a refresh error (performing a refresh operation during a refresh-prohibited period) has occurred.
The value 1 indicates that a refresh error has occurred. The value 0 indicates that no refresh error has occurred.
Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

26.2.4 WDT Reset Control Register (WDTRCR)

The WDTRCR register controls whether to send an error notification to the error control module (ECM) when underflow occurs in the down-counter of WDT.

There are some restrictions on writing to this register. For details, see section 26.3.2, Control over Writing to the WDTCR and WDTRCR Registers.

Address(es): WDT0.WDTRCR A008 0606h, WDT1.WDTRCR A008 0626h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Note: For a reset by the WDT1, the values after a reset are the same as those on release from software reset 2. For details, see section 6, Reset.

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0 and cannot be modified.	R/W
b7	RSTIRQS	Reset Interrupt Request Selection	0: Error notification to ECM is permitted 1: Error notification to ECM is not performed	R/W

RSTIRQS Bit (Reset Interrupt Request Selection)

This bit specifies whether an error notification should be sent to the error control module (ECM) when an underflow or refresh error occurs in the down-counter.

26.3 Operation

26.3.1 Count Operation in Start Mode

Counting starts by a refresh operation of the WDT refresh register (WDTRR) when the WDT control register (WDTCR) and WDT reset control register (WDTRCR) are set.

26.3.1.1 Register Setting

After the reset state is released, set the clock division ratio, window start and end positions, and timeout period in the WDTCR register, and also set the error notification to the error control module (ECM) in the WDTRCR register. Then, the value specified by the WDTCR.TOPS[1:0] bits is set in the down-counter by a refresh operation to start counting down.
Thereafter, the value in the counter is re-set at each refresh operation and count-down continues if the program runs normally and the counter is refreshed in the refresh-permitted period. The WDT does not output an error notification to ECM as long as the count-down continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter is refreshed outside of the refresh-permitted period, the WDT outputs an error notification to the ECM.

Figure 26.3 shows an example of operation under the following conditions.

- Reset interrupt request bit (RSTIRQS): 0b (Error notification to ECM is permitted.)
- Window start position selection bits (RPSS[1:0]): 10b (75%)
- Window end position selection bits (RPES[1:0]): 10b (25%)

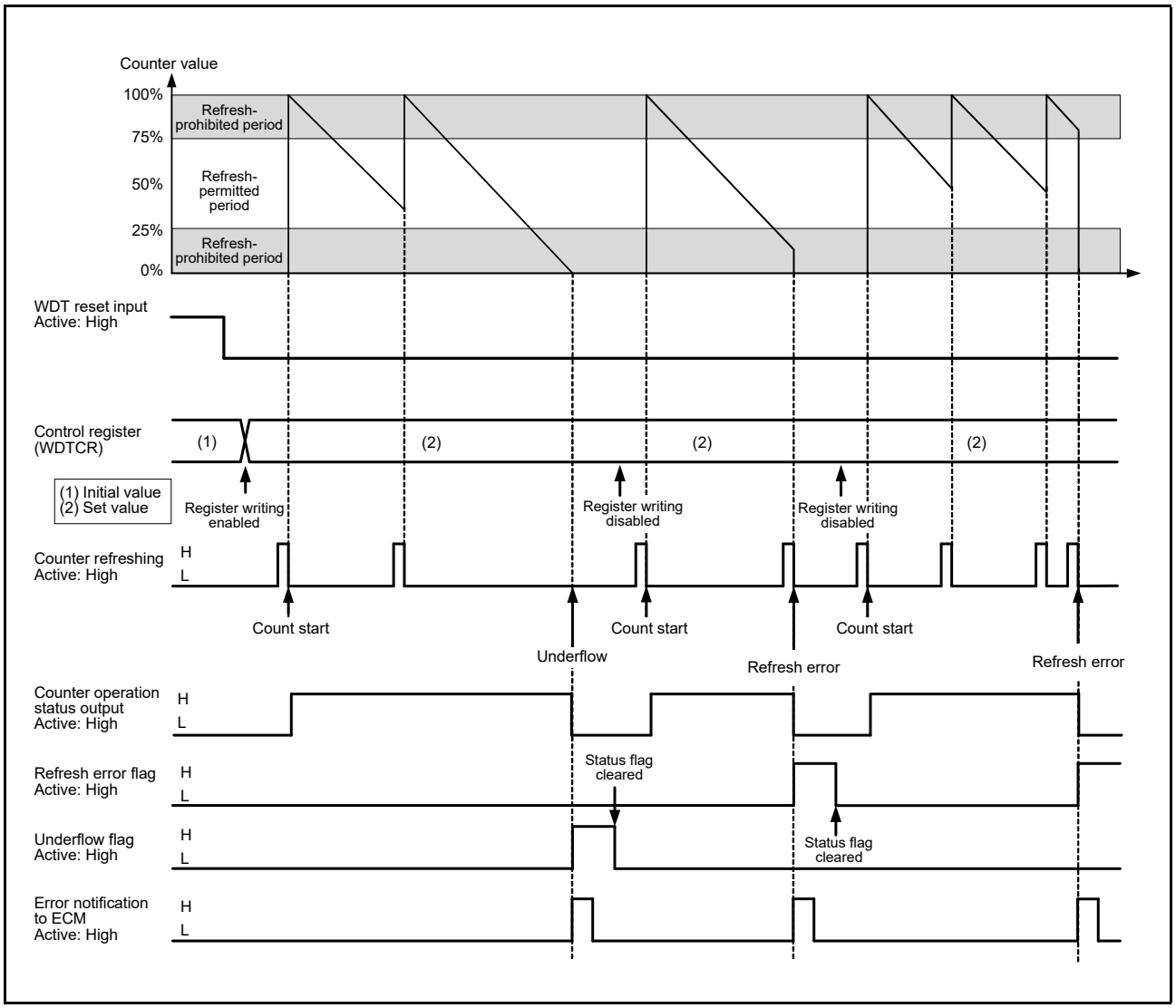


Figure 26.3 Operation Example in Register Start Mode

26.3.2 Control over Writing to the WDTCR and WDTRCR Registers

Writing to the WDT control register (WDTCR) is possible only once between the release from the reset state and the first refresh operation.

After a refresh operation (counting starts) or writing to the WDTCR register, the protection signal in the WDT becomes 1 and WDTCR is protected from subsequent attempts of writing.

Writing to the WDT reset control register (WDTRCR) is also controlled similarly.

This protection is released by the reset source for the WDT. Any other reset sources cannot release the protection.

Figure 26.4 shows control waveforms produced in response to writing to the WDTCR.

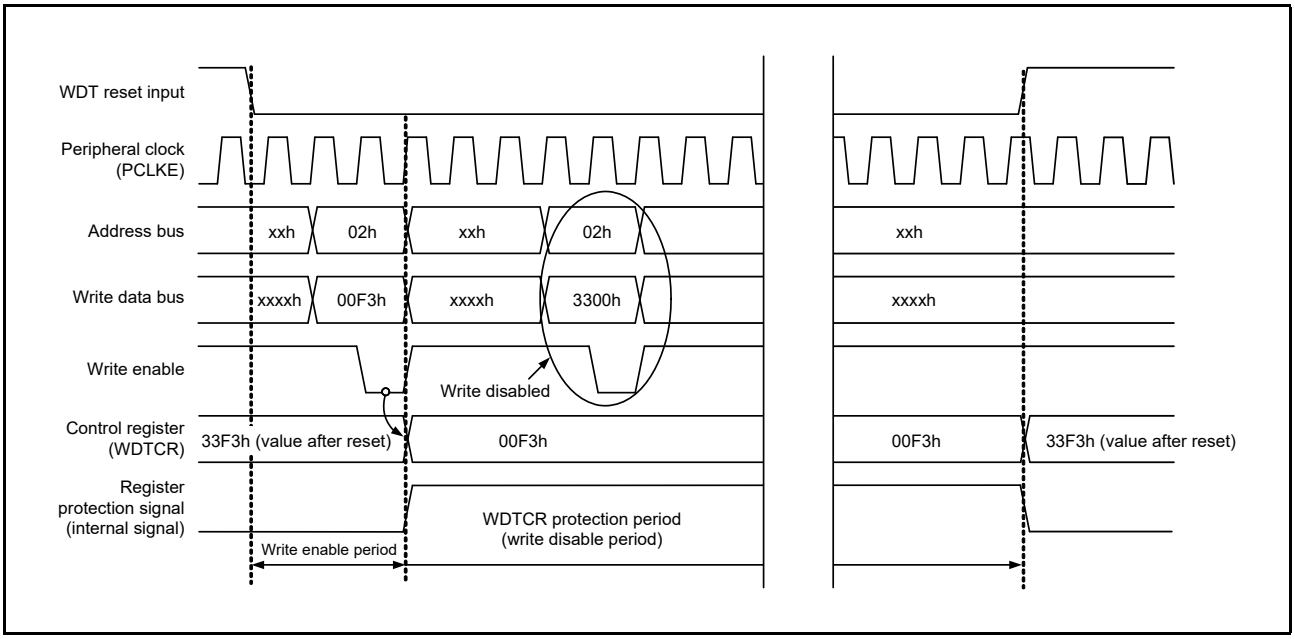


Figure 26.4 Control Waveforms Produced in Response to Writing to the WDTCR Register

26.3.3 Refresh Operation

To refresh the down-counter and to start the down-counter operation (count start due to refreshing), write the values 00h and then FFh to the WDT refresh register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. To perform refreshing after such invalid writing, write 00h and then FFh again to the WDTRR register.
If 00h is written twice in succession, writing FFh after the second 00h refreshes the down-counter because the 00h→FFh condition is satisfied. The writing sequence of 00h (n-1th)→00h (nth)→FFh also satisfies the refreshing condition and thus refreshes the down-counter.
Even if a register other than WDTRR is accessed or WDTRR is read between writing 00h and writing FFh to WDTRR, correct refreshing will be done.

[Sample sequences of writing that are valid for refreshing the counter]

- 00h→FFh
- 00h (n–1-th time)→00h (nth time)→FFh
- 00h→access to another register or read from WDTRR→FFh

[Sample sequences of writing that are not valid for refreshing the counter]

- 23h (a value other than 00h)→FFh
- 00h→54h (a value other than FFh)
- 00h→AAh (values other than 00h and FFh)→FFh

If FFh is written to the WDTRR register during the refresh-permitted period after 00h is written outside of the period, write operation is acknowledged and down-counter is refreshed. (Whether writing is made within the refresh-permitted period is determined by when FFh is written.)

After FFh is written to the WDT refresh register (WDTRR), refreshing the down-counter requires up to four counting cycles. (The number of peripheral clock (PCLKE) cycles in a single counting cycle differs depending on the setting of the clock division ratio selection bits (WDTCR.CKS[3:0]).) Therefore, writing FFh to the WDTRR register should be completed within four count-cycles before the refresh-permitted period end position or before the down-counter underflows. Confirm the down-counter value with the down-counter value bits (WDTSR.CNTVAL[13:0]).

[Sample of refresh operation timing]

- When the window start position is 1FFFh, if 00h is written to the WDTRR register before 1FFFh (for example, 2002h), the down-counter can be refreshed by writing FFh to the WDTRR register after the value of WDTSR.CNTVAL[13:0] becomes 1FFFh.
- When the window end position is 1FFFh, if the value of WDTSR.CNTVAL[13:0] is 2003h (four counts before 1FFFh) or more immediately after 00h and FFh are written to the WDTRR register, the down-counter will be refreshed.
- If the refresh-permitted period ranges down to 0000h, refreshing is possible until just before underflow. In this case, if the value of WDTSR.CNTVAL[13:0] is 0003h (four counts before underflow) or more immediately after 00h and FFh are written to the WDTRR register, underflow does not occur and the down-counter is refreshed.

Figure 26.5 shows the WDT refresh-operation waveforms when the clock division ratio = PCLKE/64.

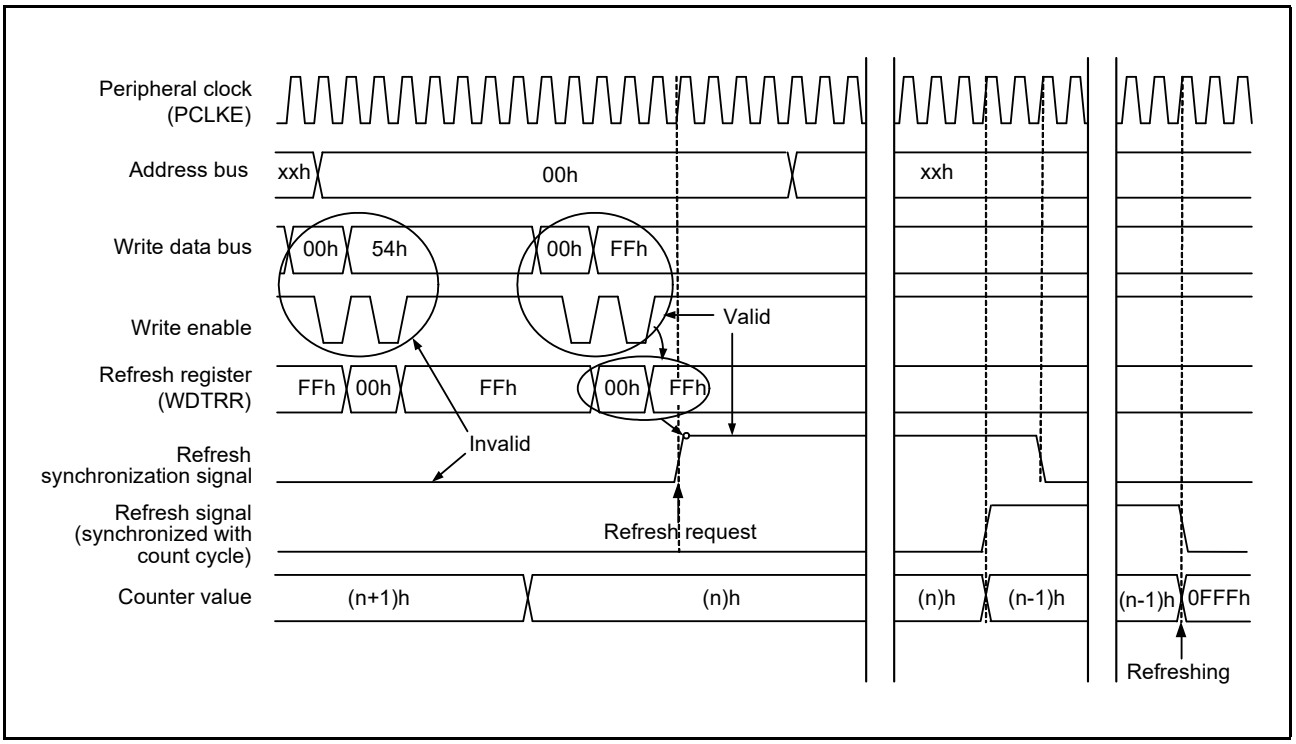


Figure 26.5 WDT Refresh Operation Waveforms (WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b)

26.3.4 Status Flag

The refresh error flag (WDTSR.REFEF) and the underflow flag (WDTSR.UNDFF) retain the error causes after error notifications were output to the error control module (ECM) of WDT.
Occurrence state of error notifications to ECM can be confirmed by reading the WDTSR.REFEF flag or the WDTSR.UNDFF flag after reset is released or upon occurrence of an error notification to ECM.
To clear these flags, write 0. Writing 1 is ignored.
If these flags are not cleared, it will give no effect to the operation. Upon occurrence of the next error notification to ECM, the previous error notification is automatically cleared and a new notification to ECM is written.

26.3.5 Error Notification to the Error Control Module (ECM)

When the reset interrupt selection bit (WDTRCR.RSTIRQS) is set to 0, underflow or refresh error of the down-counter causes an error notification to ECM to be generated during one count cycle.

26.3.6 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT status register. Thus, the counter value can be checked through the WDTSR.CNTVAL[13:0] bits.

Reading requires up to four peripheral clock (PCLKE) cycles. Therefore, the read value may differ from the actual down-counter value by one count.

Figure 26.6 shows the processing for reading the WDT down-counter value when the clock division ratio = PCLKE/64.

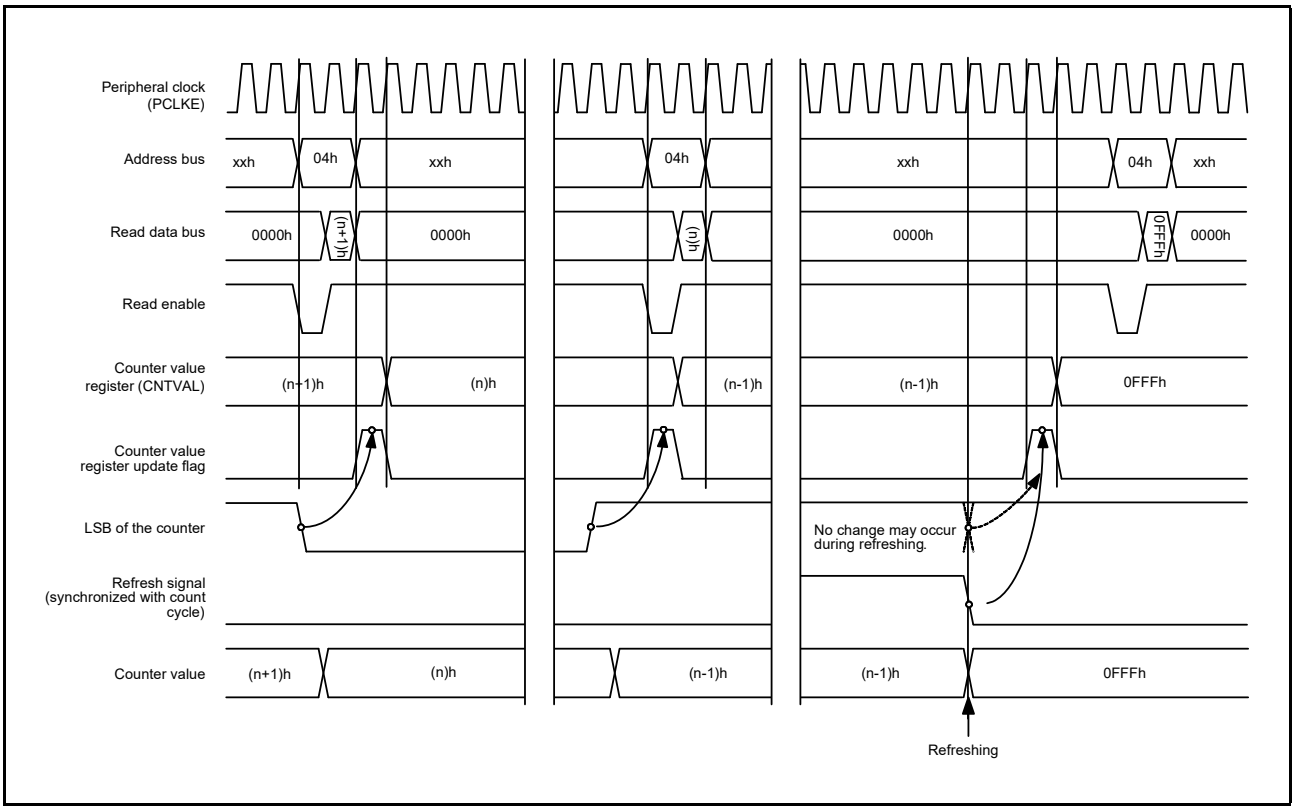


Figure 26.6 Processing for Reading WDT Down-Counter Value (WDTCR.CKS[3:0] = 0100b, WDTCR.TOPS[1:0] = 01b)

26.4 Low-Power Consumption Control

26.4.1 Watchdog Timer Operations in Low-Power Consumption Mode Transition

Clock supply can be controlled during transition to the standby mode of Cortex-R4 or the sleep mode of Cortex-M3 while the down-counter of WDT is operating.

Table 26.4 lists the WDT operations during transition to the low-power consumption mode.

Table 26.4 WDT Operations during Transition to Low-Power Consumption Mode <in Low-Power Consumption Mode Transition>

Low-Power Consumption Mode	WDT0 Clock Supply	WDT1 Clock Supply	WDT0 Operation	WDT1 Operation
Cortex-R4 standby	√	√	√	√
Cortex-M3 sleep	√	√	√	√

√: Operating

27. Independent Watchdog Timer (IWDTa)

The independent watchdog timer (IWDT) contains a 14-bit down-counter. If the counter underflows, an error notification to the error control module (ECM) is generated. The count value of the down-counter can be refreshed to the value after reset to enable counting to start again. Counter refreshing can be preformed during a period (the refresh-permitted period) you specify. If you perform refresh (register writing) outside of the permitted period, an error notification is generated and sent to the ECM. This enables detection of runaway of the program, taking the refresh interval into consideration. If underflow occurs or if refresh is performed outside of the refresh-permitted period, the IWDT stops counting. Counting restarts after refresh is performed. (For details on refresh operation, see section 27.3.3, Refresh Operation.)
For details on the error control module (ECM), see section 42, Error Control Module (ECM).

27.1 Overview

The IWDT starts counting when refresh (register writing) is performed after reset is released.
Before starting the count, it is necessary to set the clock division ratio, the window start/end positions, and the timeout period in the IWDT control register (IWDTCR).
Table 27.1 lists the specifications of the IWDT.

Table 27.1 IWDT Specifications

Item	Description
Count source	IWDT clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
IWDT clock (IWDTCLK) oscillation enable	IWDT clock oscillation starts by a refresh operation.
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	Counting starts by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to the values after reset) • A counter underflows or a refresh error is generated
Window function	Window start and end positions can be specified (refresh-permitted period)
Sources for the output of error notification to ECM	• When the down-counter underflows • When refreshing is done outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by reading the IWDTSR register.
IWDT register control	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits)

For operation to continue even if the peripheral clock (PCLKB) stops unexpectedly, counting by the IWDT is driven by two clock signals, the peripheral clock (PCLKB) and the IWDT clock (IWDTCLK). The peripheral clock (PCLKB) provides the timing for the bus interface and registers, and the IWDT clock (IWDTCLK) provides the timing for the 14-bit down-counter and control circuits.
Signals between the peripheral clock (PCLKB) operation blocks and the IWDT clock (IWDTCLK) operation blocks are connected via a synchronization circuit.

Figure 27.1 is a block diagram of the IWDT.

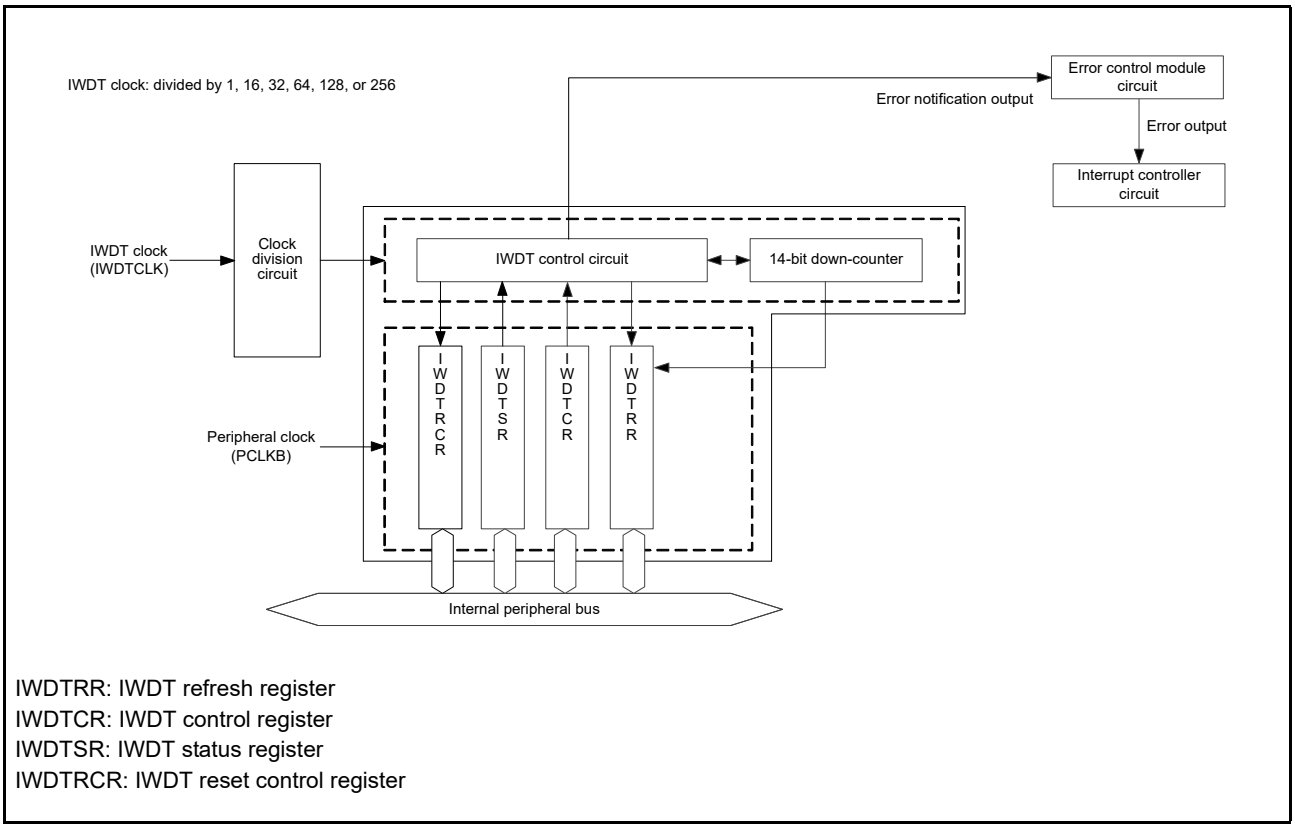


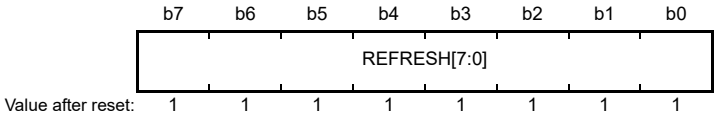
Figure 27.1 IWDT Block Diagram

27.2 Register Descriptions

27.2.1 IWDT Refresh Register (IWDTRR)

The IWDTRR register refreshes the down-counter of the IWDT.
To refresh the down-counter of the IWDT, write 00h and then FFh (refresh operation) to the IWDTRR register in the refresh-permitted period. After being refreshed, the down-counter starts counting down from the value specified with the IWDTCR.TOPS[1:0] bits.
When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is always FFh. For details on the refresh operation, see section 27.3.3, Refresh Operation.

Address(es): A008 0700h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	REFRESH [7:0]	Refresh Register	The down-counter is refreshed by writing 00h and then writing FFh to this register.	R/W

27.2.2 IWDT Control Register (IWDTCR)

The IWDTCR register allows you to select a timeout period before the down-counter underflows, a clock division ratio, and a window start/end position for refreshing.

There are some restrictions on writing to this register. For details, see section 27.3.2, Control Over Writing to the IWDTCR and IWDTRCR Registers.

Address(es): A008 0702h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Selection	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh) Values within parentheses are down-count start values.	R/W
b3, b2	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Selection	b7 b4 0 0 0 0: IWDTCLK 0 0 1 0: IWDTCLK/16 0 0 1 1: IWDTCLK/32 0 1 0 0: IWDTCLK/64 1 1 1 1: IWDTCLK/128 0 1 0 1: IWDTCLK/256 Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Selection	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (window end position is not specified.)	R/W
b11, b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W
b13, b12	RPSS[1:0]	Window Start Position Selection	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (window start position is not specified.)	R/W
b15, b14	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W

TOPS[1:0] Bits (Timeout Period Selection)

These bits allow you to select a timeout period (a period before the down-counter underflows) from among 1024, 4096, 8192, and 16384 cycles, taking the divided clock specified by the CKS[3:0] bits as one cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the time (the number of IWDT clock (IWDTCLK) cycles) before the counter underflows.

Table 27.2 lists relations between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of IWDT clock (IWDTCLK) cycles.

CKS[3:0] Bits (Clock Division Ratio Selection)

These bits allow you to select the IWDT clock (IWDTCLK) division ratio from among division by 1, 16, 32, 64, 128, and 256. Combined with the TOPS[1:0] bit setting, a counting period between 1024 and 4194304 cycles of the IWDT clock (IWDTCLK) can be selected for the IWDT. The down-counter value may not be read correctly depending on the relation between the lowest peripheral clock (PCLKB) frequency and the highest IWDT clock (IWDTCLK) frequency.

RPES[1:0] Bits (Window End Position Selection)

These bits allow selection of a window end position from among 75%, 50%, 25%, and 0% of the counting period. The selected window end position should be a value smaller than the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is valid.

The counter values of the window start and end positions specified by the RPES[1:0] and RPSS[1:0] bit settings vary according to the TOPS[1:0] bit setting.

Table 27.3 lists the counter values of the window start and end positions corresponding to the TOPS[1:0] bit setting.

RPSS[1:0] Bits (Window Start Position Selection)

These bits allow selection of a window start position of the down-counter from among 100%, 75%, 50%, and 25% of the counting period (assuming that the count start position as 100% and underflow occurrence as 0%). The period from the window start position to the window end position is the refresh-permitted period, and any other periods are the refresh-prohibited periods.

Figure 27.2 shows the relation between the settings of the RPSS[1:0] and RPES[1:0] bits and the refresh-permitted and refresh-prohibited periods.

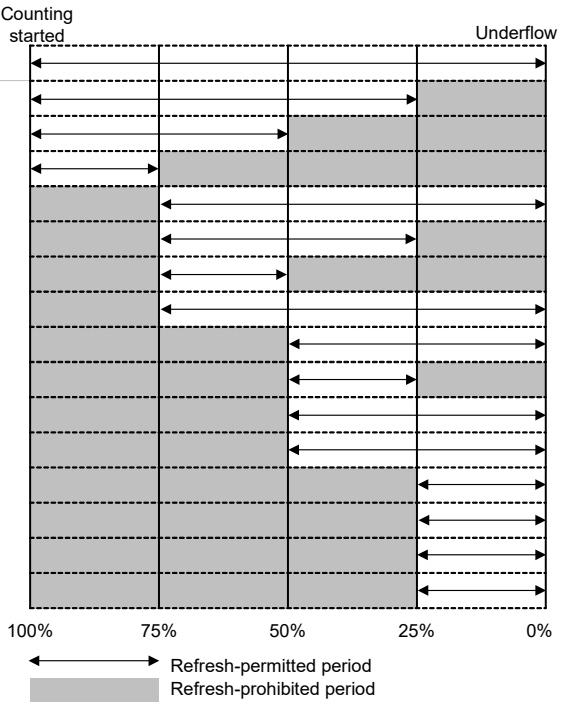
Table 27.2 Settings and Timeout Periods

CKS[3:0] Bits				TOPS[1:0] Bits		Clock Division Ratio	Timeout Period (Number of Cycles)	No. of IWDT Clock (IWDTCLK) Cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	1024	1024
				0	1		4096	4096
				1	0		8192	8192
				1	1		16384	16384
0	0	1	0	0	0	IWDTCLK/16	1024	16384
				0	1		4096	65536
				1	0		8192	131072
				1	1		16384	262144
0	0	1	1	0	0	IWDTCLK/32	1024	32768
				0	1		4096	131072
				1	0		8192	262144
				1	1		16384	524288
0	1	0	0	0	0	IWDTCLK/64	1024	65536
				0	1		4096	262144
				1	0		8192	524288
				1	1		16384	1048576
1	1	1	1	0	0	IWDTCLK/128	1024	131072
				0	1		4096	524288
				1	0		8192	1048576
				1	1		16384	2097152
0	1	0	1	0	0	IWDTCLK/256	1024	262144
				0	1		4096	1048576
				1	0		8192	2097152
				1	1		16384	4194304

Table 27.3 Relationship between Timeout Period and Window Start and End Counter Values

TOPS[1:0] Bits		Timeout Period		Window Start and End Counter Value			
b1	b0	Cycles	Counter Value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

RPSS[1:0] Bits		RPES[1:0] Bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75



Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 27.2 RPSS[1:0] and RPES[1:0] Bit Settings and the Refresh-Permitted Period

27.2.3 IWDT Status Register (IWDTSR)

The IWDTSR register shows the counter value of the down-counter and whether an underflow or refresh error has occurred.

Address(es): A008 0704h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred	R/(W)
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred	R/(W)

CNTVAL[13:0] Bits (Counter Value)

Read these bits to confirm the value of the down-counter, but note that the read value may differ from the actual count by a value of one count.

UNDFF Flag (Underflow Flag)

Read this bit to confirm whether an underflow has occurred in the down-counter.

The value 1 indicates that the down-counter has underflowed. The value 0 indicates that the down-counter has not underflowed.

Write 0 to the UNDFF flag to set the value to 0. Writing 1 has no effect.

REFEF Flag (Refresh Error Flag)

Read this bit to confirm whether a refresh error (performing a refresh operation during a refresh-prohibited period) has occurred.

The value 1 indicates that a refresh error has occurred. The value 0 indicates that no refresh error has occurred.

Write 0 to the REFEF flag to set the value to 0. Writing 1 has no effect.

27.2.4 IWDT Reset Control Register (IWDTRCR)

The IWDTRCR register controls whether to send an error notification to the error control module (ECM) when underflow occurs in the down-counter of IWDT.

There are some restrictions on writing to this register. For details, see section 27.3.2, Control Over Writing to the IWDTCR and IWDTRCR Registers.

Address(es): A008 0706h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R/W
b7	RSTIRQS	Reset Interrupt Request Selection	0: Error notification to ECM is permitted. 1: Error notification to ECM is not performed.	R/W

RSTIRQS Bit (Reset Interrupt Request Selection)

This bit specifies whether an error notification should be sent to the error control module (ECM) when an underflow or refresh error occurs in the down-counter.

27.3 Operation

27.3.1 Count Operation in Start Mode

Counting starts by a refresh operation of the IWDT refresh register (IWDTRR) if the IWDT control register (IWDTCR) and IWDT reset control register (IWDTRCR) are set.

27.3.1.1 Register Setting

After the reset state is released, set the clock division ratio, window start and end positions, and timeout period in the IWDTCR register, and also set whether to send an error notification to the error control module (ECM) in the IWDTRCR register. Then, the value specified by the timeout period selection bits (IWDTCR.TOPS[1:0]) is set in the down-counter by a refresh operation to start counting down.
Thereafter, the value in the counter is re-set at each refresh operation and count-down continues if the program runs normally and the counter is refreshed in the refresh-permitted period. The IWDT does not output an error notification to ECM as long as the count-down continues.
However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter is refreshed outside of the refresh-permitted period, the IWDT outputs an error notification to the ECM.

Figure 27.3 shows an example of operation under the following conditions.

- Reset interrupt request bit (IWDTCR.RSTIRQS): 0b (Error notification to ECM is permitted.)
- Window start position selection bits (IWDTCR.RPSS[1:0]): 10b (75%)
- Window end position selection bits (IWDTCR.RPES[1:0]): 10b (25%)

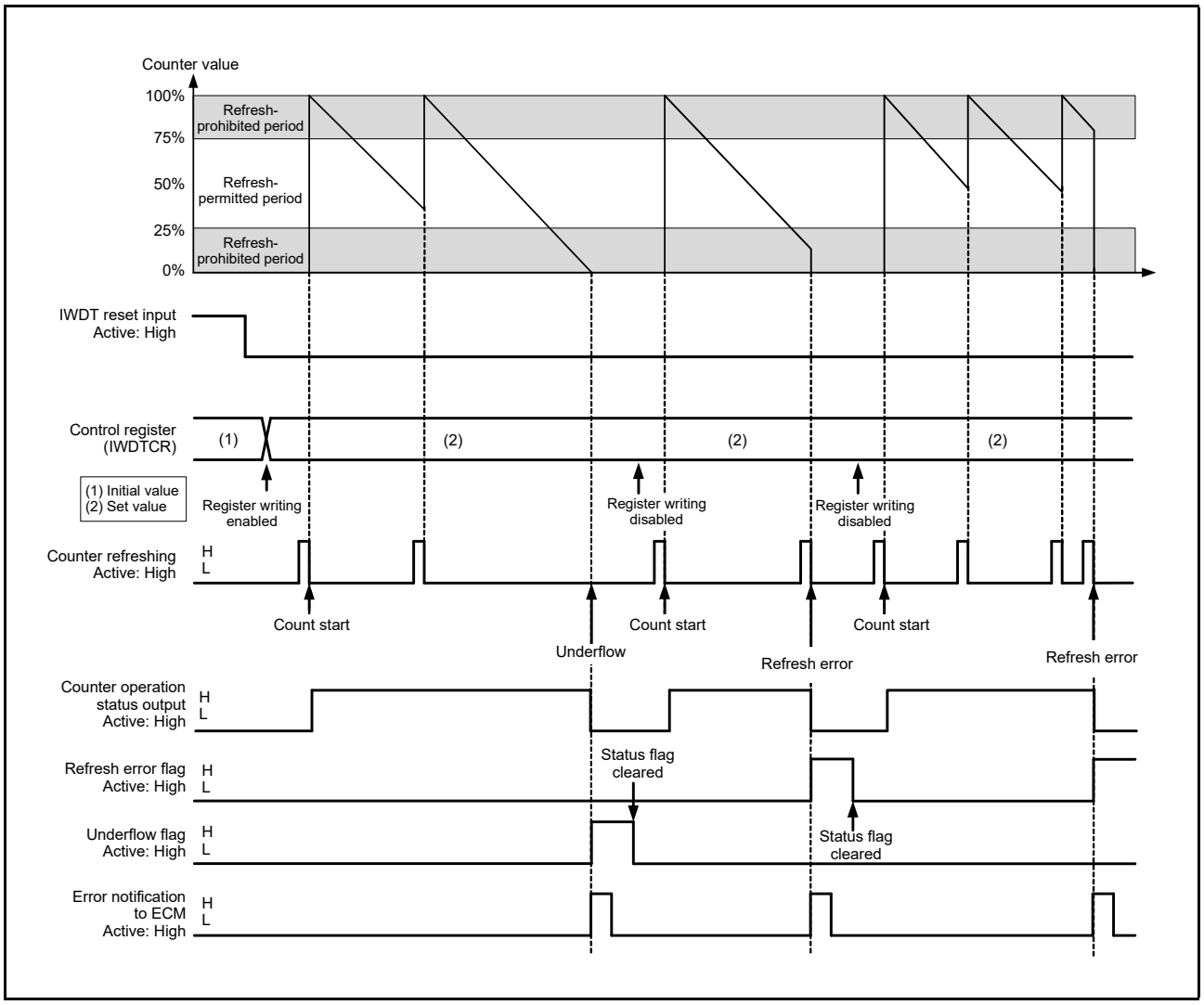


Figure 27.3 Operation Example in Register Start Mode

27.3.2 Control Over Writing to the IWDTCR and IWDTRCR Registers

Writing to the IWDT control register (IWDTCR) is possible only once between the release from the reset state and the first refresh operation.

After a refresh operation (counting starts) or writing to the IWDTCR register, the protection signal in the IWDT becomes 1 to protect IWDTCR from subsequent attempts of writing.

Writing to the IWDT reset control register (IWDTRCR) is also controlled similarly.

This protection is released by the reset source for the IWDT. With other reset sources, the protection is not released.

Figure 27.4 shows control waveforms produced in response to writing to the IWDTCR register.

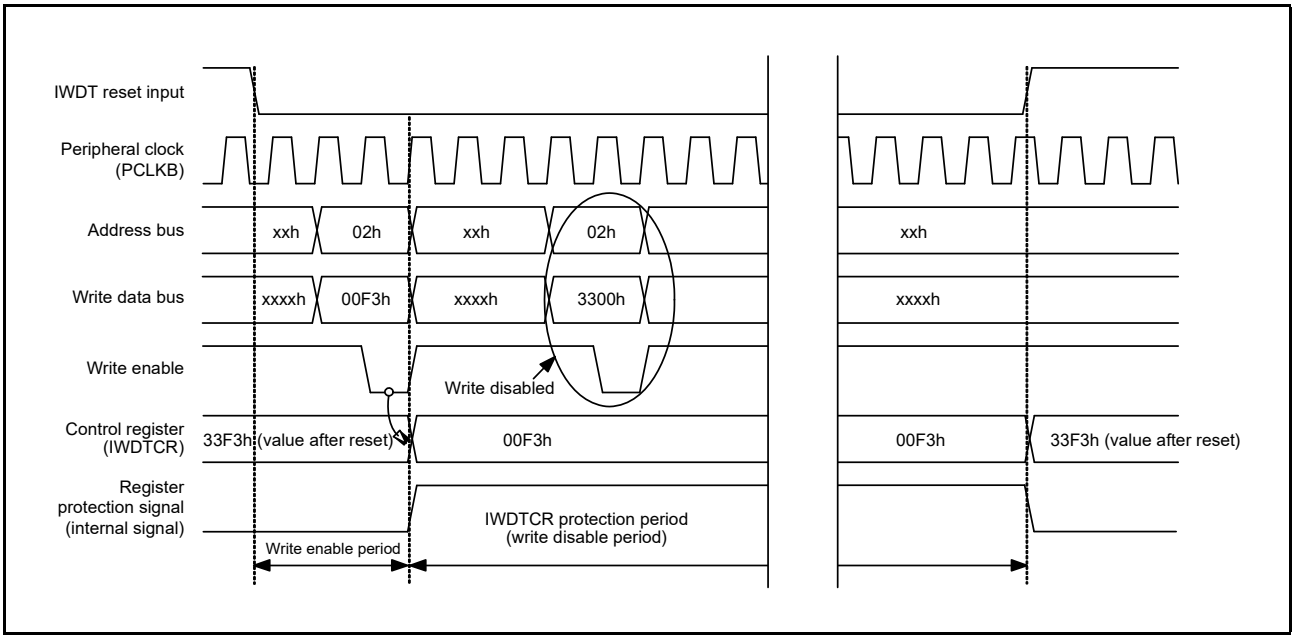


Figure 27.4 Control Waveforms Produced in Response to Writing to the IWDTCR Register

27.3.3 Refresh Operation

To refresh the counter and to start the counter operation (counting is started by refreshing), write the values 00h and then FFh to the IWDT refresh register (IWDTRR). If a value other than FFh is written after 00h, the counter is not refreshed. To perform refreshing after such invalid writing, write 00h and FFh again to the IWDT refresh register (IWDTRR).
When writing is done in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied; writing 00h (n–1-th time) → 00h (nth time) → FFh is valid and correct refreshing will be done. Moreover, even if a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR, correct refreshing will be done.

[Sample sequences of writing that are valid for refreshing the counter]

- 00h → FFh
- 00h (n–1-th time) → 00h (nth time) → FFh
- 00h → access to another register or read from IWDTRR → FFh

[Sample sequences of writing that are not valid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (values other than 00h and FFh) → FFh

Even when 00h is written to IWDTRR outside the refresh-permitted period, if FFh is written to IWDTRR in the refresh-permitted period, the writing sequence is valid and refreshing will be done. (Whether writing is made within the refresh-permitted period is determined by when FFh is written.)
After FFh is written to the IWDTRR register, refreshing the counter requires up to four cycles of the signal for counting (the clock division ratio selection bits (IWDTCR.CKS[3:0]) determine how many cycles of the IWDT clock (IWDTCLK) make up one cycle for counting). Therefore, writing FFh to the IWDTRR should be completed four-count cycles before the end position of the refresh-permitted period or a counter underflow. The value of the down-counter can be checked by the down-counter bits (IWDTSR.CNTVAL[13:0]).

[Sample refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to IWDTRR before 1FFFh is reached (2002h, for example), refreshing is done if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits has reached 1FFFh.
- When the window end position is set to 1FFFh, refreshing is done if 2003h (four-count cycles before 1FFFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR.
- When the refresh-permitted period continues until count 0000h, refreshing can be done immediately before an underflow. In this case, if 0003h (four-count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after writing 00h → FFh to IWDTRR, no underflow occurs and refreshing is done.

Figure 27.5 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and clock division ratio = IWDTCLK. Figure 27.6 shows the IWDT refresh-operation waveforms when PCLKB < IWDTCLK and clock division ratio = IWDTCLK/16.

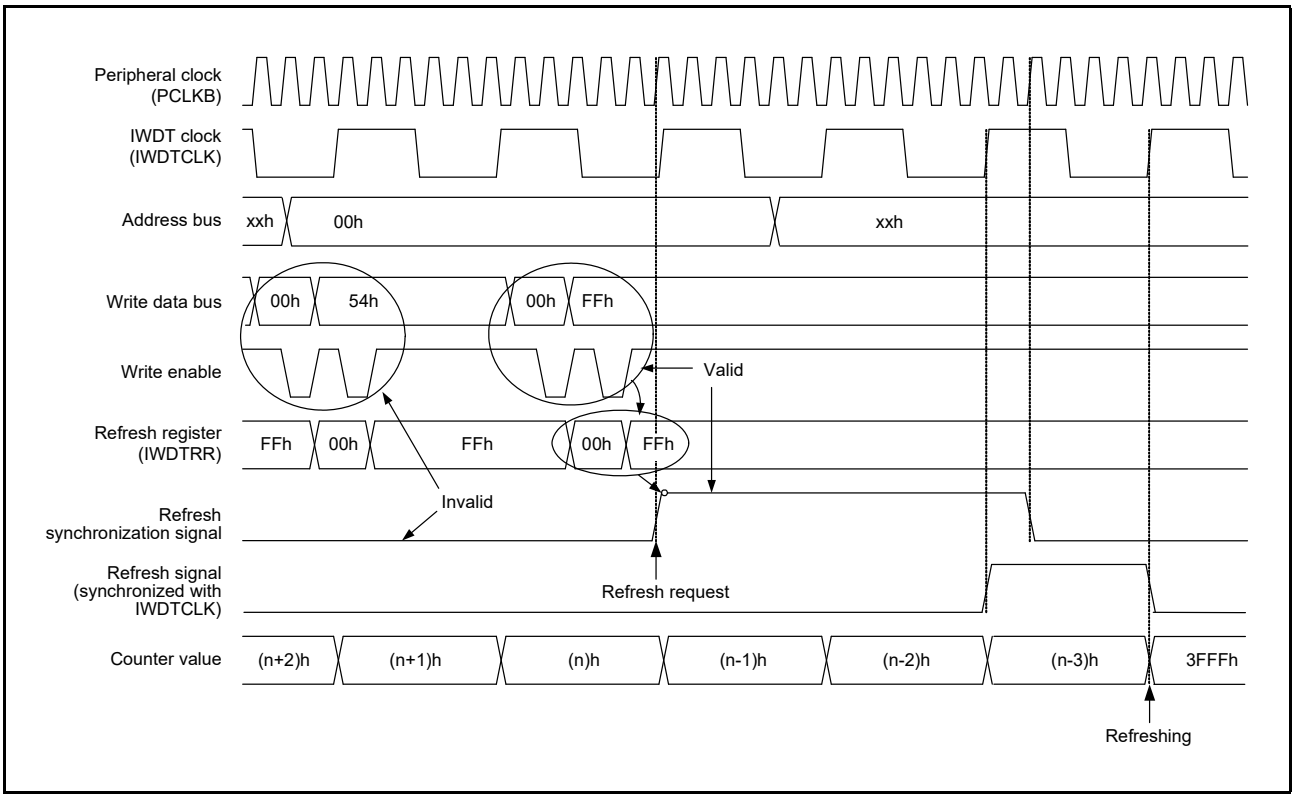


Figure 27.5 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

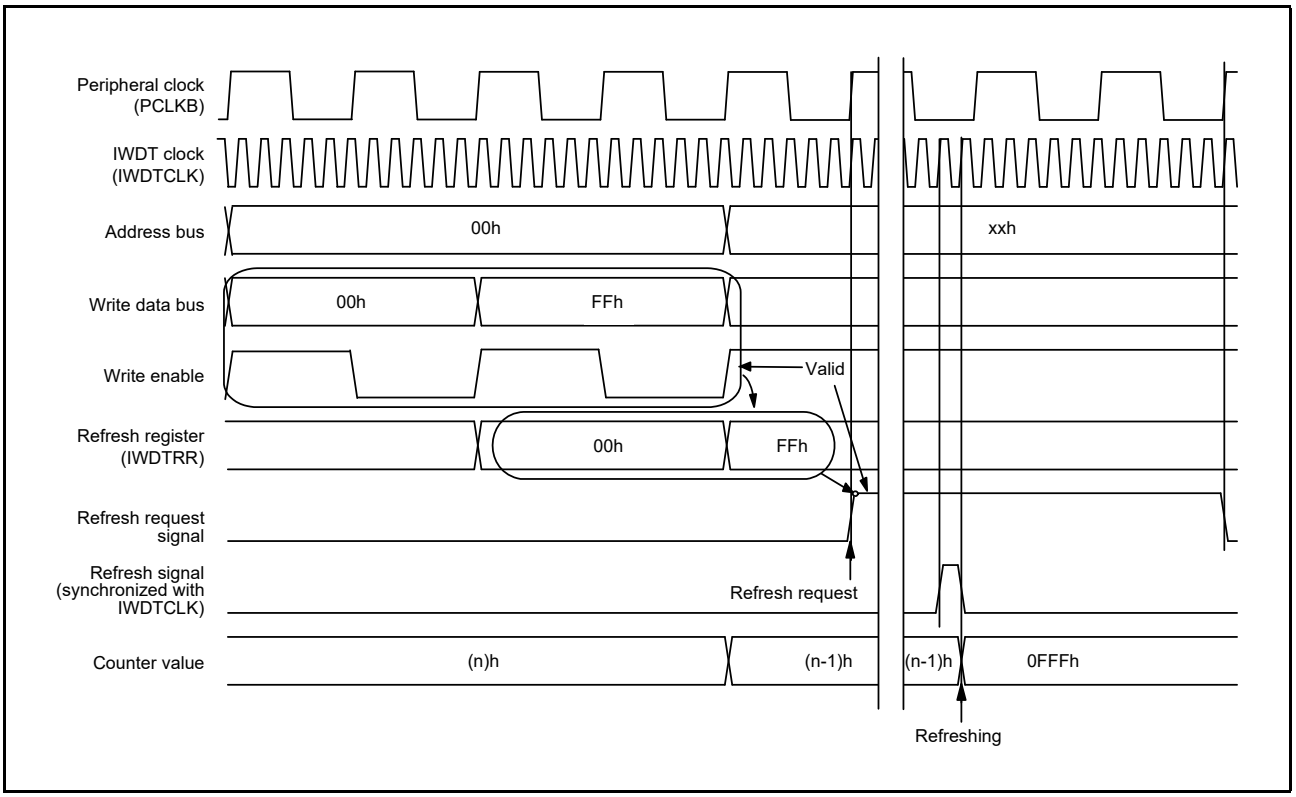


Figure 27.6 IWDT Refresh Operation Waveforms (IWDTCR.CKS[3:0] = 0010b, IWDTCR.TOPS[1:0] = 01b)

27.3.4 Status Flags

The refresh error flag (IWDTSR.REFEF) and the underflow flag (IWDTSR.UNDFF) retain the error causes when error notifications are output to the error control module (ECM) of IWDT.
Occurrence state of error notifications to ECM can be confirmed by reading the IWDTSR.REFEF flag or the IWDTSR.UNDFF flag after reset is released or upon occurrence of an error notification to ECM.
To clear these flags to 0, write 0. Writing 1 is ignored.
If these flags are not cleared, it will give no effect to the operation. Upon occurrence of the next error notification to ECM, the previous error notification is automatically cleared and a new notification to ECM is written.

27.3.5 Error Notification to the Error Control Module (ECM)

When the reset interrupt selection bit (IWDTRCR.RSTIRQS) is set to 0, underflow or refresh error of the down-counter causes an error notification to ECM to be generated during one count cycle.

27.3.6 Reading the Down-Counter Value

As the counter in the IWDT operates with the IWDT clock (IWDTCLK), the IWDT cannot read the counter value directly. Therefore, the IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT status register. Thus, the counter value can be checked indirectly through the IWDTSR.CNTVAL[13:0] bits.

Reading the counter value requires multiple PCLKB clock cycles (up to four clock cycles), and the read counter value may differ from the actual counter value by a value of one count.

Figure 27.7 shows the processing for reading the IWDT down-counter value.

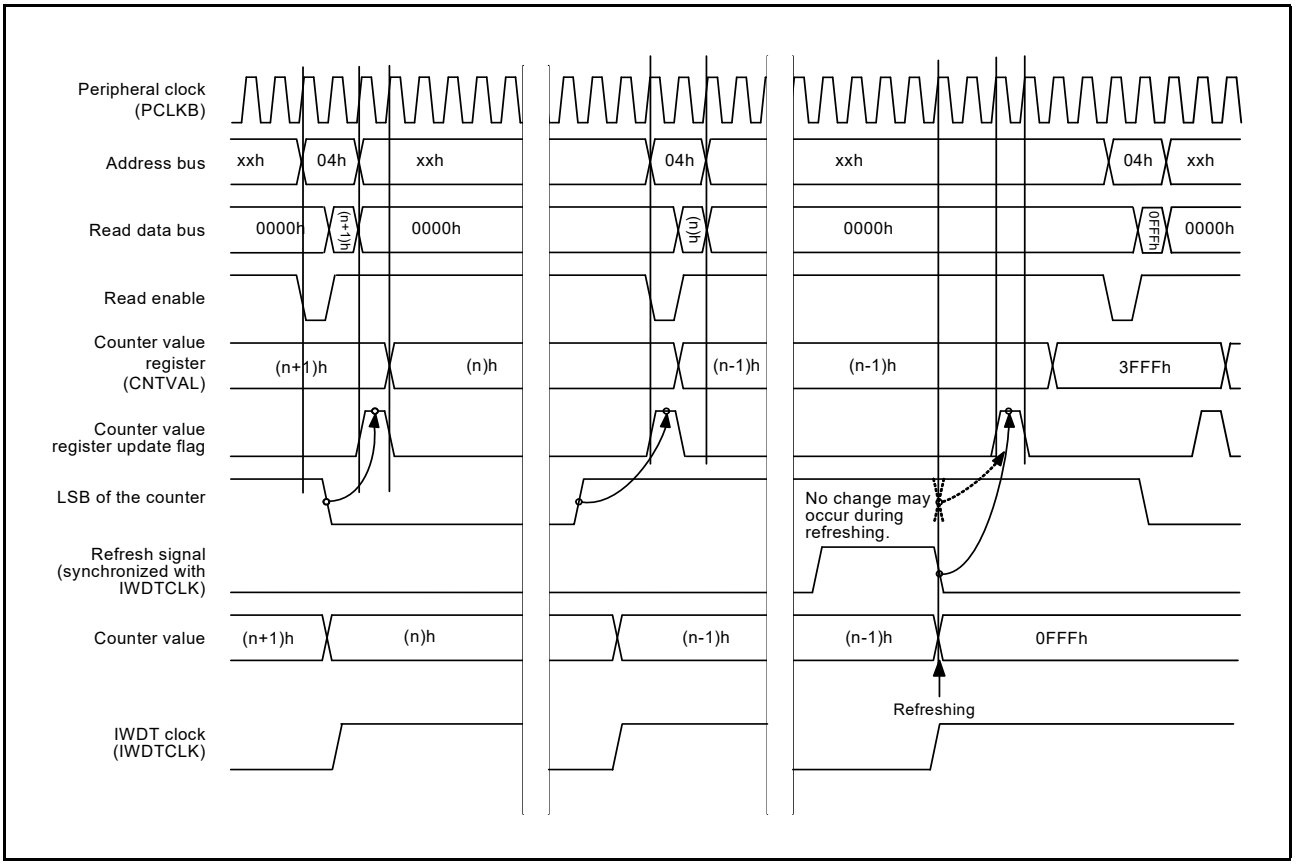


Figure 27.7 Processing for Reading IWDT Counter Value (IWDTCR.CKS[3:0] = 0000b, IWDTCR.TOPS[1:0] = 11b)

27.4 Low-Power Consumption Control

27.4.1 Watchdog Timer Operations in Low-Power Consumption Mode Transition

Clock supply to the IWDT can be controlled during transition to the standby mode of Cortex-R4 or the sleep mode of Cortex-M3 while the down-counter of IWDT is operating.

Table 27.4 lists the IWDT operations during transition to the low-power consumption mode.

Table 27.4 IWDT Operations during Transition to Low-Power Consumption Mode <in Low-Power Consumption Mode Transition>

Low-Power Consumption Mode	IWDT Clock Supply	IWDT Operation
Cortex-R4 standby	√	√
Cortex-M3 sleep	√	√

√: Operating

28. Ethernet MAC (ETHERC)

This LSI has Ethernet MAC (ETHERC) with an accelerator.

28.1 Overview

Table 28.1 describes the Ethernet MAC (ETHERC) functions.

Table 28.1 ETHERC Specifications

Item	Specifications
Functions	• 1 port*1 • IEEE802.3 is supported • 10BASE and 100BASE are supported • Full duplex and half duplex are supported • Automatic pause packet transmission function • Auto broadcast suspension function by the pause packet reception • MII/RMII interface is supported
Interrupt sources	Seven sources: • Ethernet MII management access completion interrupt • Ethernet pause packet transmission completion interrupt • Ethernet transmission completion interrupt • RX FIFO overflow interrupt • TX FIFO underflow interrupt • TX FIFO error interrupt • Ethernet reception frame error interrupt

Note 1. Use of two ports is possible with the Ethernet switch function. For details, see section 28.2.1.4, MAC Select Register (MACSEL).

Note: 1 Gbps mode is not supported because the supported interfaces are only MII and RMII. However, when connecting to an Ethernet switch, use 1 Gbps mode because GMII is used for connection.

Figure 28.1 and Figure 28.2 are block diagrams of the ETHERC. Modules, registers, and other items indicated in gray are described in section 29, Ethernet Switch and section 30, EtherCAT Slave Controller (optional).

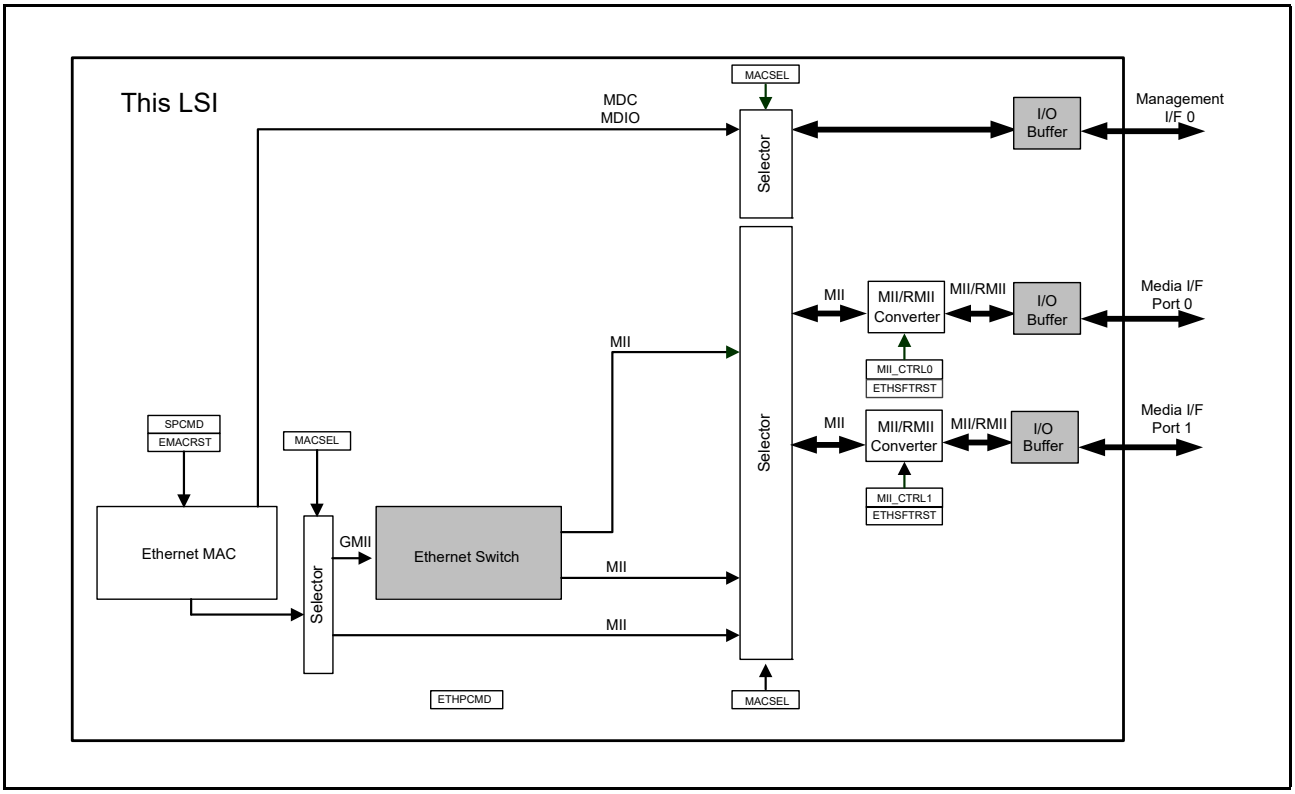


Figure 28.1 Block Diagram of the ETHERC

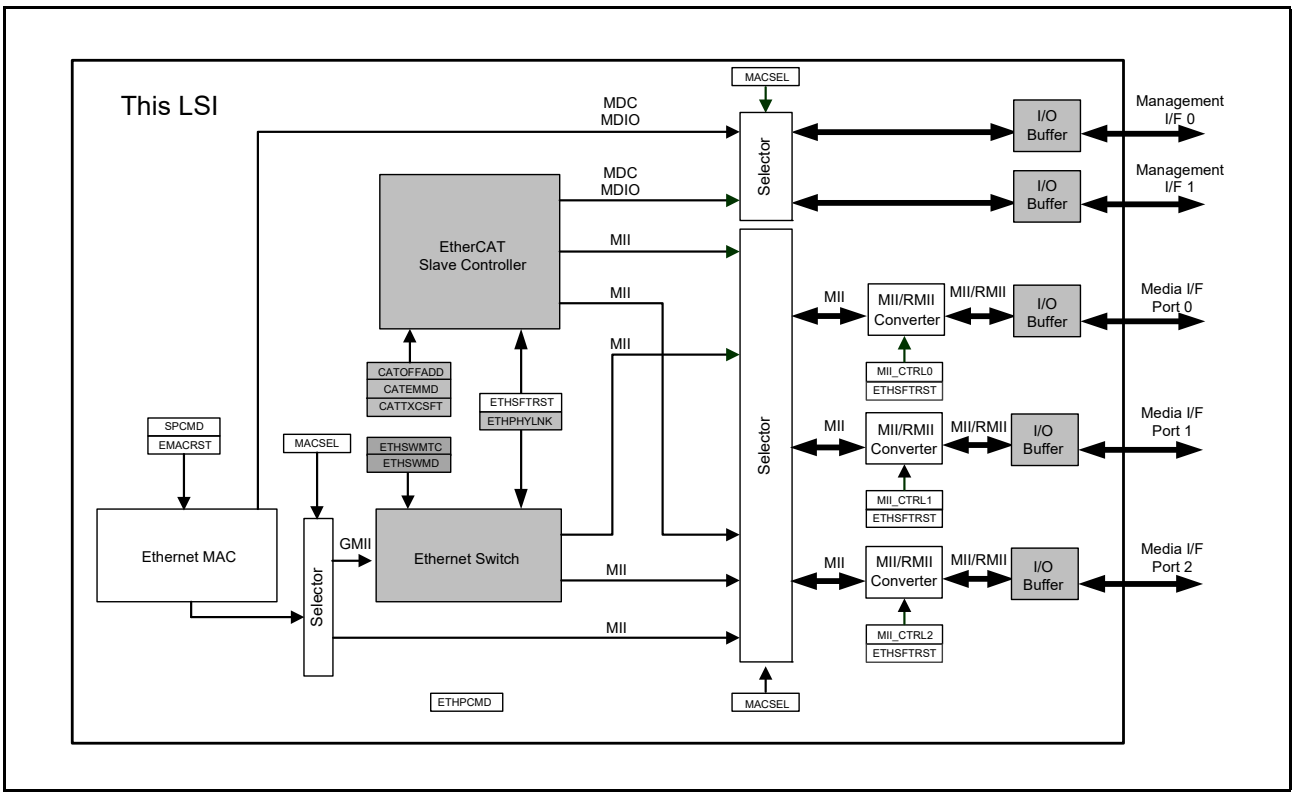


Figure 28.2 Block Diagram of the ETHERC (for products incorporating an EtherCAT (optional))

Table 28.2 lists the input/output pins of the ETHERC.

Table 28.2 Input/Output Pins of the ETHERC

Pin Name	I/O	Description
ETH0_TXC, ETH1_TXC, ETH2_TXC	Input	10M/100M transmission clock (2.5 MHz/25 MHz) input pin
ETH0_TXEN, ETH1_TXEN, ETH2_TXEN	Output	Transmission enable signal output pin
ETH0_TXER, ETH1_TXER, ETH2_TXER	Output	Transmission error signal output pin
ETH0_TXD0 to ETH0_TXD3, ETH1_TXD0 to ETH1_TXD3, ETH2_TXD0 to ETH2_TXD3	Output	Transmission data signal output pin
ETH0_RXC, ETH1_RXC, ETH2_RXC	Input	Reception clock input pin
ETH0_RXDV, ETH1_RXDV, ETH2_RXDV	Input	Received data enable signal input pin
ETH0_RXER, ETH1_RXER, ETH2_RXER	Input	Received data error signal input pin
ETH0_RXD0 to ETH0_RXD3, ETH1_RXD0 to ETH1_RXD3 ETH2_RXD0 to ETH2_RXD3	Input	Received data signal input pin
ETH0_CRS, ETH1_CRS, ETH2_CRS	Input	Carrier sense signal input pin
ETH0_COL, ETH1_COL, ETH2_COL	Input	Collision detection signal input pin
ETH_MDC, MII2_MDC	Output	Management interface clock output pin
ETH_MDIO, MII2_MDIO	I/O	Management data signal input/output pin
PHYLINK0, PHYLINK1	Input	PHY Link signal input pin
ETHSWSECOUT	Output	Ethernet switch SYNCOUT signal output pin
PHYRESETOUT#, PHYRESETOUT2#	Output	Output the PHY RESET signal (PHYRESETOUT#: for Ether0 and Ether1, PHYRESETOUT2#: for Ether2)

Table 28.3 and Table 28.4 list the names of the I/O pin functions for each of the modules.

Table 28.3 I/O Pin Functions for ETHERC (in MII Mode)

Media I/F	Port 0	Port 1	Port 2
10M/100M transmission clock input	ETH0_TXC	ETH1_TXC	ETH2_TXC
Transmission enable output	ETH0_TXEN	ETH1_TXEN	ETH2_TXEN
Transmission error output	ETH0_TXER	ETH1_TXER	ETH2_TXER
Transmission data output	ETH0_TXD0 to 3	ETH1_TXD0 to 3	ETH2_TXD0 to 3
Reception clock input	ETH0_RXC	ETH1_RXC	ETH2_RXC
Received data enable input	ETH0_RXDV	ETH1_RXDV	ETH2_RXDV
Received data error input	ETH0_RXER	ETH1_RXER	ETH2_RXER
Received data input	ETH0_RXD0 to 3	ETH1_RXD0 to 3	ETH2_RXD0 to 3
Carrier sense input	ETH0_CRS	ETH1_CRS	ETH2_CRS
Collision detection input	ETH0_COL	ETH1_COL	ETH2_COL

Management I/F	Port 0	Port 1	Port 2
Management interface clock output	ETH_MDC		MII2_MDC
Management data input/output	ETH_MDIO		MII2_MDIO

Others	Port 0	Port 1	Port 2
PHY Link input	PHYLINK0	PHYLINK1	—
Ethernet switch SYNCOUT output	ETHSWSECOUT		—
PHY reset output	PHYRESETOUT#		PHYRESTOUT2#
External clock output for Ethernet PHY*1	CLKOUT25M0	CLKOUT25M1	CLKOUT25M2

Note 1. The clock frequency is 25 MHz in MII mode.

Table 28.4 I/O Pin Functions for ETHERC (in RMII Mode)

Media I/F	Port 0	Port 1	Port 2
Transmission enable output	ETH0_TXEN	ETH1_TXEN	ETH2_TXEN
Transmission data output	ETH0_TXD0, 1	ETH1_TXD0, 1	ETH2_TXD0, 1
Carrier sense/received data enable input	ETH0_RXDV	ETH1_RXDV	ETH2_RXDV
Received data error input	ETH0_RXER	ETH1_RXER	ETH2_RXER
Received data input	ETH0_RXD0, 1	ETH1_RXD0, 1	ETH2_RXD0, 1

Management I/F	Port 0	Port 1	Port 2
Management interface clock output	ETH_MDC		MII2_MDC
Management data input/output	ETH_MDIO		MII2_MDIO

Others	Port 0	Port 1	Port 2
PHY Link input	PHYLINK0	PHYLINK1	—
Ethernet switch SYNCOUT output	ETHSWSECOUT		—
PHY reset output	PHYRESETOUT#		PHYRESTOUT2#
External clock output for Ethernet PHY*1	CLKOUT25M0	CLKOUT25M1	CLKOUT25M2

Note 1. The clock frequency is 50 MHz in RMII mode.

28.2 Register Descriptions

28.2.1 Ethernet interface selection registers

28.2.1.1 System Protect Command Register (SPCMD)

The SPCMD register is used to control writing to write-protected registers.
For details, see section 28.3.6, Protect Command Register.
The SPCMD register allows read/write access in 32-bit units.

Address(es): ETHERC.SPCMD A00F 2100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PROTREL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PROTREL	Protection Unlock Enable	Permits write access to a write-protected register. Writing is allowed in a specific instruction sequence only. 1: Enables write access. 0: Disables write access (write-protected).	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: After data is written to the write-protected register, be sure to clear the SPCMD.PROTREL bit (to 0) to enable protection again.

28.2.1.2 Ethernet MAC Reset Register (EMACRST)

The EMACRST register is used to control the reset status of ETHERC by software. After reset is released, the EMACRST bit is initialized to 0. This means that ETHERC is still in the reset state. After Ethernet MAC selection or PHY mode setting has been completed, use this register to release the reset state.
To reset ETHERC during operation, after 0s are written to this register, use software to read the EMACRST bit. Then, after confirming that the bit is set to 0, write 1 to release the reset state.
This register is write-protected by the system protect command register (SPCMD). To write to this register, use the SPCMD register to release write protection. For products with a built-in R-IN engine, this register also resets the HW-RTOS.

Address(es): ETHERC.EMACRST A00F 2110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EMAC RST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EMACRST	Ethernet MAC Reset Control	Controls the reset state of Ethernet MAC. 1: Reset-released state 0: Reset state (initial value)	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

28.2.1.3 Ethernet System Protect Command Register (ETSPCMD)

The ETSPCMD register is used to control writing to write-protected registers.
For details, see section 28.3.6, Protect Command Register.
The ETSPCMD register allows read/write access in 32-bit units.

Address(es): ETHERC.ETSPCMD A00B F000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PROTREL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PROTREL	Protection Unlock Enable	Permits write access to a write-protected register. Writing is allowed in a specific instruction sequence only. 1: Enables write access. 0: Disables write access (write-protected).	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: After data is written to the write-protected register, be sure to clear the ETSPCMD.PROTREL bit (to 0) to enable protection again.

28.2.1.4 MAC Select Register (MACSEL)

The MACSEL register is used to select the function of the Ethernet interface.
Before changing the settings of this register, use the EMACRST register to place Ethernet MAC in the reset state. After changing the register settings, be sure to reset PHY, and then specify the MAC settings. This register allows read/written access in 32-bit units. For the configuration of the MAC function, see Figure 28.1, Figure 28.2, Table 28.5, and Table 28.6.
This register is write-protected by the Ethernet system protect command register (ETSPCMD). To write to this register, use the ETSPCMD register to release write protection.

Address(es): ETHERC.MACSEL A00B F004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MAC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	MAC[2:0]	Ethernet MAC Mode Select	Selects the function of the Media/Management interface of the MAC to be used. For details, see Table 28.5 and Table 28.6.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 28.5 MAC Function Selection Method for products incorporating EtherCAT (an Optional Function)

MAC[2:0]	Media I/F Port 0	Media I/F Port 1	Media I/F Port 2	Management I/F 0	Management I/F 1
000	Ethernet Switch Port 0	Ethernet Switch Port 1	Not used	EthernetMAC	Not used
001	EtherCAT Slave Port 0	EtherCAT Slave Port 1	EthernetMAC (if the switch function is not used)	EtherCAT	EthernetMAC
011	Not used	Ethernet MAC (If the switch function is not used)	Not used	EthernetMAC	Not used
101	EtherCAT Slave Port 0	EtherCAT Slave Port 1	Ethernet Switch Port 0	EtherCAT	EthernetMAC
Other than above	Setting prohibited				

Table 28.6 MAC Function Selection Method

MAC[2:0]	Media I/F Port 0	Media I/F Port 1	Management I/F 0
000	Ethernet Switch Port 0	Ethernet Switch Port 1	EthernetMAC
011	Not used	EthernetMAC (if the switch function is not used)	EthernetMAC
Other than above	Setting prohibited		

28.2.1.5 MII Control Register (MII_CTRLn) (n = 0 to 2)

The MII_CTRLn register is used to control the MII/RMII converter. This register allows read/written access in 32-bit units.

Address(es): ETHERC.MII_CTRL0 A00B F008h, ETHERC.MII_CTRL1 A00B F00Ch, ETHERC.MII_CTRL2 A00B F010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	RMII_CRS_MODE	—	FULLD	—	—	—	MODE[4:0]				
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MODE[4:0]	MII Converter Mode Select	Sets the mode of the MII converter. b4 b0 x_0000: MII mode 1_0100: RMII mode (10 Mbps)*1 1_0101: RMII mode (100 Mbps)*1 Others: Setting prohibited	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	FULLD	Duplex Mode Setting	Specifies the Duplex Mode settings. 0: Half duplex 1: Full duplex (initial value)	R/W
b9	—	Reserved	When used in RMII mode, be sure to set this bit to 1.	R/W
b10	RMII_CRS_MODE	CRS Determination Condition Select	Sets the condition for determining the carrier sense (CRS) signal. This bit takes effect in RMII mode only. CRS determination condition 0: CRS | TXEN 1: CRS | RXDV | TXEN (initial value)	R/W
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For use in RMII mode, be sure to set b9 to 1.

28.2.1.6 Ethernet Peripheral Reset Register (ETHSFTRST)

The ETHSFTRST register is used to control the reset states of the RMII converter, EtherCAT*1, Ethernet switch, and other Ethernet peripheral circuits by software.

After reset is released, all bits are initialized to 0. Therefore, all Ethernet peripheral circuits, including the RMII converter, EtherCAT*1, and Ethernet switch, are placed in the reset state. After Ethernet MAC selection or PHY mode setting has been completed, use this register to release the reset state of each circuit.

To reset Ethernet peripheral circuits during operation, after 0s are written to this register, use software to read the target bits. Then, after confirming that the bits are set to 0, write 1 to release the reset state.

This register is write-protected by the Ethernet system protect command register (ETSPCMD). To write to this register, use the ETSPCMD register to release write protection.

Note 1. Optional

Address(es): ETHERC.ETHSFTRST A00B F118h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	MIICRST	PHYRST2*1	PHYRST	SWRST	CATRST*1
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note 1. These bits are only for products incorporating an EtherCAT (optional).

Bit	Symbol	Bit Name	Description	R/W
b0	CATRST*1	EtherCAT Reset Control (only for products incorporating an EtherCAT (optional))	Resets EtherCAT. 1: Reset-released state 0: Reset state (initial value)	R/W
b1	SWRST	Ethernet Switch Reset Control	Resets the Ethernet switch. 1: Reset-released state 0: Reset state (initial value)	R/W
b2	PHYRST	PHYRESETOUT# Pin Reset Control	Resets the PHYRESETOUT# output pin. For products with EtherCAT (an optional function), the RESETOUT signals are output from EtherCAT with their functions being logically ORed. 1: Reset-released state 0: Reset state (initial value)	R/W
b3	PHYRST2*1	PHYRESETOUT2# Pin Reset Control (only for products incorporating an EtherCAT (optional))	Resets the PHYRESETOUT2# output pin. 1: Reset-released state 0: Reset state (initial value)	R/W
b4	MIICRST	RMII Converter Reset Control	Resets the RMII converter. 1: Reset-released state 0: Reset state (initial value)	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is reserved for products other than those incorporating an EtherCAT (optional). It is read as 0. The write value should always be 0.

28.2.2 Ethernet MAC Control Register

28.2.2.1 MIIM Register (GMAC_MIIM)

The GMAC_MIIM register is used to control register access to each Ethernet PHY. For access to this register, clear the MSTPCRB18 bit in the MSTPCRB register to release the Ethernet MAC from the module-stop state, and then follow the procedure below.

For write access:

1. Start of a write operation: Set the RWDV bit to 1; set the PHYADDR[4:0] bits to the PHY address; set the REGADDR[4:0] bits to the PHY register address; set the DATA[15:0] bits to the write data.
2. Wait for the operation to finish: Wait until 1 is read from the RWDV bit.
3. Wait for the operation to finish: The write operation finishes when 1 is read from the RWDV bit.

For read access:

1. Start of a read operation: Set the RWDV bit to 0; set the PHYADDR[4:0] bits to the PHY address; set the REGADDR[4:0] bits to the PHY register address.
2. Wait for the operation to finish: Wait until 1 is read from the RWDV bit.
3. Wait for the operation to finish: When 1 is read from the RWDV bit and valid data is read from the DATA[15:0] bits, the read operation finishes.

Note: The setting of the GMAC_MIIM register is only effective when the Ethernet MAC or Ethernet switch port is selected by the MAC select register (MACSEL). In other cases, writing to this register has no effect and the value read is undefined.

Address(es): ETHERC.GMAC_MIIM A00F 00A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	RWDV	PHYADDR[4:0]					REGADDR[4:0]				
Value after reset:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	DATA[15:0]	Data	Indicates write data or read data.	R/W
b20 to b16	REGADDR [4:0]	PHY Register Address	Specifies the register address of the PHY to be accessed. Because this is a write-only bit, the value read from the bit is undefined.	W
b25 to b21	PHYADDR [4:0]	PHY Address	Specifies the address of the PHY to be accessed. Because this is a write-only bit, the value read from the bit is undefined.	W
b26	RWDV	Read/Write Operation	Reading or writing starts when the values shown below are written to this bit. Set the other effective bits in this register at the same time as the setting of this bit. 1: Starts a write operation. 0: Starts a read operation.	W
			After a read/write operation has started, the status of the operation can be checked by reading the value of this bit.*1 1: Operation is completed. 0: Waiting for the operation to start.	R

Bit	Symbol	Bit Name	Description	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. After reset is released, the RWDV bit is set to 1. However, the values held by the DATA[15:0] bits at this time are not valid. To use the RWDV bit to check the status correctly, make sure that the value is read from the bit after the operation has started.

28.2.2.2 TX ID Register (GMAC_TXID)

The GMAC_TXID register is used to indicate the ID of the transmission frame for the GMAC_TXRESULT register. To check the transmission frame result ID, be sure to read this register before reading the GMAC_TXRESULT register. If the GMAC_TXRESULT register is read first, the transmission frame result is updated. Therefore, the updated transmission frame ID is read from the GMAC_TXID register.

Address(es): ETHERC.GMAC_TXID A00F 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TXID[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TXID[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TXID[31:0]	Transmission Frame ID	Indicates the ID of the transmission frame for the TX RESULT register.	R

28.2.2.3 TX RESULT Register (GMAC_TXRESULT)

The GMAC_TXRESULT register is used to indicate the transmission frame result.
The flags in this register are only valid when the TRBMODE[1:0] bits in the GMAC_TXMODE register are 00 or 01.
The results for the transmission of a frame are held in the transmission result buffer at the same time as the Ethernet transmission complete interrupt (ETHIT) is generated. The transmission result buffer can hold the information for four frames. The results of transmission for a next frame are acquired from the transmission result buffer by reading this register. The GMAC_TXFIFO.TRBFR[2:0] bits indicate the number of frames for which the transmission result buffer currently holds information.
When transmission proceeds while the buffer already holds information for four frames, the transmission is illicit, so a TX-FIFO error interrupt (ETHTFIE) is generated. Read the frame transmission information appropriately so that errors are not generated while this register is valid.

Address(es): ETHERC.GMAC_TXRESULT A00F 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TCMP	TABT	TFAIL	SCOLLIS	MCOLLIS	CSERR	OVERFW	UNDERFW	LCOLLIS	RETRYN[3:0]				FIFOUFLOW
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FIFOUFLOW	FIFO Underflow Status	An FIFO underflow occurred during transmission.	R
b4 to b1	RETRYN[3:0]	Retry Count Status	Retry count	R
b5	LCOLLIS	Late Collision Detection Status	Late Collision was detected.	R
b6	UNDERFW	Frame Length Underflow Status	A frame shorter than the minimum frame length was written to the transmit FIFO.	R
b7	OVERFW	Frame Length Overflow Status	A frame longer than 1,518 octets was written to the transmit FIFO.	R
b8	CSERR	Carrier Sense Error Status	Disappearance of the carrier has been detected.	R
b9	MCOLLIS	Multi-Collision Detection Status	Multiple collisions were experienced.	R
b10	SCOLLIS	Single-Collision Detection Status	1 collision was experienced.	R
b11	TFAIL	Transmission Fail Status	Transmission failed because an Excessive Collision error occurred (16 consecutive failures in re-transmission).	R
b12	TABT	Transmission Abort Status	Transmission abort occurred.	R
b13	TCMP	Transmission Completion Status	Transmission finished.	R
b31 to b14	—	Reserved	These bits are read as 0.	R

28.2.2.4 MODE Register (GMAC_MODE)

The GMAC_MODE register is used to control the operating mode of ETHERC.

Address(es): ETHERC.GMAC_MODE A00F 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ETHMODE	DUPMODE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b29 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30	DUPMODE	Duplex Mode	1: ETHERC operates in Full Duplex mode. Use this mode when ETHERC connects to an Ethernet switch. 0: ETHERC operates in Half Duplex mode.	R/W
b31	ETHMODE	Ethernet Mode	1: ETHERC operates in Giga bit Ethernet mode. Use this mode when ETHERC connects to an Ethernet switch. 0: ETHERC operates in 10/100 Ethernet mode. Use this mode when ETHERC does not connect to an Ethernet switch.	R/W

28.2.2.5 RX MODE Register (GMAC_RXMODE)

The GMAC_RXMODE register is used to control frame reception. One word in the reception FIFO buffer is 64 bits and the buffer has a capacity of 4 Kbytes.

Address(es): ETHERC.GMAC_RXMODE A00F 0024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	AFILLTEREN	MFILLTEREN	SFRXFIFO	RAMASKEN	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REMPTH[1:0]		RFULLTH[1:0]		RRTTH[2:0]			—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b8 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b9	RRTTH[2:0]	RX FIFO Read Trigger Threshold	The RRT bit in the GMAC_RXFIFO register is set to 1 when the SFRXFIFO bit is 0 and the number of words in the FIFO is greater than or equal to the value corresponding to the setting as shown below. b11 b10 b9 0 0 0: 4 words 0 0 1: 8 words 0 1 0: 16 words 0 1 1: 32 words 1 0 0: 64 words 1 0 1: 128 words 1 1 0: 256 words 1 1 1: 512 words	R/W
b13, b12	RFULLTH[1:0]	Receive Almost Full Threshold	The RFULL bit in the GMAC_RXFIFO register is set to 1 when the number of empty words in the FIFO buffer is less than or equal to the value corresponding to the setting as shown below. b13 b12 0 0: 4 words 0 1: 8 words 1 0: 16 words 1 1: 32 words	R/W
b15, b14	REMPTH[1:0]	Receive Almost Empty Threshold	The REMP bit in the GMAC_RXFIFO register is set to 1 when the number of words in the FIFO is less than or equal to or the value corresponding to the setting as shown below. b15 b14 0 0: 4 words 0 1: 8 words 1 0: 16 words 1 1: 32 words	R/W
b27 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	RAMASKEN	RX Address Mask Enable	1: Enables the function that can be set by the BITMSK[7:0] bits of the GMAC_ADRnB register (comparative mask function for Destination Address[7:0]). (n = 0 to 15) 0: Disables the above function.	R/W

Bit	Symbol	Bit Name	Description	R/W
b29	SFRXFIFO	Store & Forward For RX FIFO	1: Store & Forward mode The reception DMA controller starts to operate after data up to the end of the frame are written to the RX FIFO buffer. 0: Cut-through mode The reception DMA controller starts to operate when the number of words set in the RRTTH[2:0] bits is written to the RX FIFO buffer.	R/W
b30	MFILLTEREN	Multicast Filtering Enable	1: Discards multicast address frames that are not registered in MAC address registers (GMAC_ADRnA and GMAC_ADRnB). (n = 0 to 15) 0: Includes all multicast address frames.	R/W
b31	AFILLTEREN	Address Filtering Enable	1: Enables address filtering.*1 0: Includes all address frames.	R/W

Note 1. Even if address filtering is enabled, MAC control frames (pause packets, etc.) are always received whether or not the addresses are registered in the MAC address register. A MAC control frame is a frame having the destination address 01-80-C2-00-00-01.

28.2.2.6 TX MODE Register (GMAC_TXMODE)

The GMAC_TXMODE register is used to control frame transmission. One word in the transmission FIFO buffer is 64 bits and the buffer has a capacity of 4 Kbytes.

Address(es): ETHERC.GMAC_TXMODE A00F 0028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RTRANSDEN	LPTXEN	SF	SPTXEN	RTRANSLC	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TEMPTH[2:0]			TFULLTH[1:0]		—	TRBMODE[1:0]		—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7, b6	TRBMODE[1:0]	Transmission Result Buffer Mode	Controls how to write the transmission result to the GMAC_TX RESULT register. b7 b6 0 0: The result is always written. 0 1: The result is written only when an error occurred. 1 0: The result is never written. Others: Setting prohibited	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10, b9	TFULLTH[1:0]	Transmit Almost Full Threshold	The TFULL bit in the GMAC_TXFIFO register is set to 1 when the number of empty words in the TX FIFO buffer is less than or equal to the value corresponding to the setting as shown below. b10 b9 0 0: 4 words 0 1: 8 words 1 0: 16 words 1 1: 32 words	R/W
b13 to b11	TEMPTH[2:0]	Transmit Almost Empty Threshold	The TEMP bit in the GMAC_TXFIFO register is set to 1 when the number of data words in the TX FIFO buffer is less than or equal to the value corresponding to the setting as shown below. b13 b12 b11 0 0 0: 4 words 0 0 1: 8 words 0 1 0: 16 words 0 1 1: 32 words 1 0 0: 64 words 1 0 1: 128 words 1 1 0: 256 words 1 1 1: 512 words	R/W
b26 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27	RTRANSLC	Retransmission at Late Collision	1: Performs retransmission if a Late Collision occurs. 0: Aborts processing if a Late Collision occurs.	R/W
b28	SPTXEN	Short Packet TX Enable	1: Permits transmission of frames that are shorter than the length prescribed by IEEE802.3. 0: Prohibits transmission of frames that are shorter than the length prescribed by IEEE802.3.	R/W
b29	SF	Store & Forward	1: Starts transmission after the data up to the end of the frame is written to TX FIFO. Use this setting to use TCP/IP Accelerator. 0: Setting prohibited	R/W

Bit	Symbol	Bit Name	Description	R/W
b30	LPTXEN	Long Packet TX Enable	1: Permits transmission of frames that are longer than the length prescribed by IEEE802.3.*1 0: Prohibits transmission of frames that are longer than the length prescribed by IEEE802.3.	R/W
b31	RTRANSDEN	No Retransmission	1: Does not perform retransmission when a collision occurs. 0: Performs retransmission as prescribed when a collision occurs.	R/W

Note 1. When the management tag insertion function of the Ethernet switch is enabled (the SWTAGEN bit in the ETHSWMTC register = 1), the size of the frame may exceed the maximum frame size of 1518 bytes. Therefore, the LPTXEN bit must be set to 1 in this case.
Note that the maximum frame size before insertion of the management tag should still be within 1518. For details, see section 28.4.7, Frame with Size Exceeding 1518 Bytes.

28.2.2.7 RESET Register (GMAC_RESET)

The GMAC_RESET register is a trigger register that is used to reset the ETHERC module by software.
The module is reset by setting all bits to 1. All bits will automatically be initialized to 0 afterward.
The time required for the completion of a reset depends on the MAC operating mode as shown below.

- Operation at 1 Gbps (125 MHz): 60 ns
- Operation at 100 Mbps (25 MHz): 200 ns
- Operation at 10 Mbps (2.5 MHz): 2000 ns

Address(es): ETHERC.GMAC_RESET A00F 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ALLRST	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TXRST	—	RXRST	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	RXRST	RX Reset Trigger	Resets the RX MAC, RX FIFO, and RX DMA modules. 0: Performs nothing. 1: Resets the modules.	R/W
b14	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15	TXRST	TX Reset Trigger	Resets the TX MAC, TX FIFO, and TX DMA modules. 0: Performs nothing. 1: Resets the modules.	R/W
b30 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	ALLRST	ALL Reset Trigger	Resets all Ethernet MAC modules. 0: Performs nothing. 1: Resets the modules.	R/W

28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5)

The GMAC_PAUSEn register is used to specify the pause packet to be sent.

Address(es): ETHERC.GMAC_PAUSE1 A00F 0080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPDATA1[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PPDATA1[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PPDATA1 [31:0]	Pause Packet Data 1	Specifies 4th to 1st bytes of the pause packet to be sent. Data is sent in LSB-first order.	R/W

Address(es): ETHERC.GMAC_PAUSE2 A00F 0084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPDATA2[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PPDATA2[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PPDATA2 [31:0]	Pause Packet Data 2	Specifies the 8th to 5th bytes of the pause packet to be sent. Data is sent in LSB-first order.	R/W

Address(es): ETHERC.GMAC_PAUSE3 A00F 0088h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPDATA3[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PPDATA3[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PPDATA3 [31:0]	Pause Packet Data 3	Specifies the 12th to 9th bytes of the pause packet to be sent. Data is sent in LSB-first order.	R/W

Address(es): ETHERC.GMAC_PAUSE4 A00F 008Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPDATA4[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PPDATA4[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PPDATA4 [31:0]	Pause Packet Data 4	Specifies the 16th to 13th bytes of the pause packet to be sent. Data is sent in LSB-first order.	R/W

Address(es): ETHERC.GMAC_PAUSE5 A00F 0090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPDATA5[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PPDATA5[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	PPDATA5 [31:0]	Pause Packet Data 5	Specifies the 20th to 17th bytes of the pause packet to be sent. Data is sent in LSB-first order.	R/W

28.2.2.9 RX FLOW CONTROL Register (GMAC_FLWCTL)

The setting of the GMAC_FLWCTL register determines whether or not transmission is suspended after a pause packet is received.

When a pause packet is received while suspension is enabled, transmission is suspended for the time specified by the pause packet.

Address(es): ETHERC.GMAC_FLWCTL A00F 0098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPRXEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	PPRXEN	Pause Packet Reception Function Enable	1: Enables the pause packet reception function. 0: Disables the pause packet reception function.	R/W

28.2.2.10 PAUSE Packet Register (GMAC_PAUSPKT)

The GMAC_PAUSPKT register is used to control pause packet transmission.

Writing 1 to the PPR bit causes transmission of the data set in the PAUSE packet data register (GMAC_PAUSEn). The bit is cleared to 0 when the transmission is completed.

Address(es): ETHERC.GMAC_PAUSPKT A00F 009Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

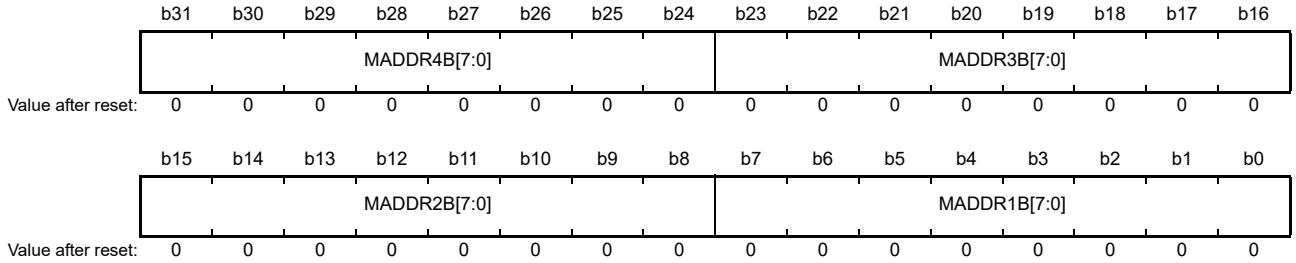
Bit	Symbol	Bit Name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	PPR	Pause Packet Transmission Trigger	Controls pause packet transmission. 0: Performs nothing. 1: Starts pause packet transmission.	R/W

28.2.2.11 MAC Address Registers (GMAC_ADRnA and GMAC_ADRnB) (n = 0 to 15)

The GMAC_ADRnA and GMAC_ADRnB registers are used to set MAC addresses.
A maximum of 16 addresses can be registered. Multiple addresses can be filtered by using the BITMSK[7:0] bits of the GMAC_ADRnB register.

- GMAC_ADRnA

Address(es): ETHERC.GMAC_ADR0A A00F 0100h, ETHERC.GMAC_ADR1A A00F 0108h, ETHERC.GMAC_ADR2A A00F 0110h, ETHERC.GMAC_ADR3A A00F 0118h, ETHERC.GMAC_ADR4A A00F 0120h, ETHERC.GMAC_ADR5A A00F 0128h, ETHERC.GMAC_ADR6A A00F 0130h, ETHERC.GMAC_ADR7A A00F 0138h, ETHERC.GMAC_ADR8A A00F 0140h, ETHERC.GMAC_ADR9A A00F 0148h, ETHERC.GMAC_ADR10A A00F 0150h, ETHERC.GMAC_ADR11A A00F 0158h, ETHERC.GMAC_ADR12A A00F 0160h, ETHERC.GMAC_ADR13A A00F 0168h, ETHERC.GMAC_ADR14A A00F 0170h, ETHERC.GMAC_ADR15A A00F 0178h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MADDR1B [7:0]	MAC Address Byte 1	Indicates the first byte of the MAC address to be included.	R/W
b15 to b8	MADDR2B [7:0]	MAC Address Byte 2	Indicates the 2nd byte from the beginning of the MAC address to be included.	R/W
b23 to b16	MADDR3B [7:0]	MAC Address Byte 3	Indicates the 3rd byte from the beginning of the MAC address to be included.	R/W
b31 to b24	MADDR4B [7:0]	MAC Address Byte 4	Indicates the 4th byte from the beginning of the MAC address to be included.	R/W

- GMAC_ADRnB

Address(es): ETHERC.GMAC_ADR0B A00F 0104h, ETHERC.GMAC_ADR1B A00F 010Ch, ETHERC.GMAC_ADR2B A00F 0114h, ETHERC.GMAC_ADR3B A00F 011ch, ETHERC.GMAC_ADR4B A00F 0124h, ETHERC.GMAC_ADR5B A00F 012Ch, ETHERC.GMAC_ADR6B A00F 0134h, ETHERC.GMAC_ADR7B A00F 013Ch, ETHERC.GMAC_ADR8B A00F 0144h, ETHERC.GMAC_ADR9B A00F 014Ch, ETHERC.GMAC_ADR10B A00F 0154h, ETHERC.GMAC_ADR11B A00F 015Ch, ETHERC.GMAC_ADR12B A00F 0164h, ETHERC.GMAC_ADR13B A00F 016Ch, ETHERC.GMAC_ADR14B A00F 0174h, ETHERC.GMAC_ADR15B A00F 017Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BITMSK[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MADDR6B[7:0]								MADDR5B[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MADDR5B [7:0]	MAC Address Byte 5	Indicates the 5th byte from the beginning of the MAC address to be included.	R/W
b15 to b8	MADDR6B [7:0]	MAC Address Byte 6	Indicates the 6th byte from the beginning of the MAC address to be included.	R/W
b23 to b16	BITMSK[7:0]	Bit Mask Specification	Places comparative masks on a bit basis for Destination Address[7:0]. Bits [23:16] correspond to Destination Address[7:0]. Bits that are set to 0 are not subject to comparison. For example, if the bits BITMSK[2:0] of the mask register are set to 0, Destination Address[2:0] are not subject to comparison. That is, the frame is included if only the Destination Address [47:3] bits match.	R/W
b31 to b24	—	Reserved	When read, the value returned is undefined. The write value should be 0.	R/W

28.2.2.12 RX FIFO Status Register (GMAC_RXFIFO)

The GMAC_RXFIFO register is a status register that indicates the status of the receive FIFO.

Address(es): ETHERC.GMAC_RXFIFO A00F 0200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RFULL	REMP	RRT	RSW[11:0]												—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b16 to b0	—	Reserved	These bits are read as 0.	R
b28 to b17	RSW[11:0]	Stored Words in RX FIFO	Indicates the number of data words in RX FIFO.	R
b29	RRT	RX FIFO Read Trigger	This bit is set to 1 when the number of words in the RX FIFO buffer is greater than or equal to the threshold for RX FIFO reading. (RX FIFO Read Threshold is set by using the GMAC_RX MODE register.)	R
b30	REMP	RX FIFO Almost Empty	This bit is set to 1 when the number of words in RX FIFO is equal to or less than Receive Almost Empty Threshold. (Receive Almost Empty Threshold is set by using the GMAC_RX MODE register.)	R
b31	RFULL	RX FIFO Almost Full	This bit is set to 1 when the number of words in RX FIFO is equal to or more than Receive Almost Full Threshold. (Receive Almost Full Threshold is set by using the GMAC_RX MODE register.)	R

28.2.2.13 TX FIFO Status Register (GMAC_TXFIFO)

The GMAC_TXFIFO register is a status register that indicates the status of the transmit FIFO.

Address(es): ETHERC.GMAC_TXFIFO A00F 0204h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TFULL	TEMP	TSTATUS[2:0]			TRBFR[2:0]			—	—	—	—	—	—	—	—
Value after reset:	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b23 to b0	—	Reserved	These bits are read as 0.	R
b26 to b24	TRBFR[2:0]		Indicates the number of frames existing in the transmission result buffer.	R
b29 to b27	TSTATUS [2:0]	TX FIFO Status	Indicates the status of TX FIFO. The meanings of bit settings are as follows: b2 b1 b0 1 0 0: ACC NEW FR: TX FIFO can accept new frames. 1 0 1: WRITE ENABLE: TX FIFO can continue to accept frame data. 1 1 0: CMPLT: Inclusion of one frame was completed. 1 1 1: FULL: TX FIFO is in FIFO Full status. 0 x x: STOP: TX FIFO is inactive (or being initialized).	R
b30	TEMP	TX FIFO Almost Empty	This bit is set to 1 when the number of data words in TX FIFO is equal to or less than the threshold value set by the TEMPTH[2:0] bits of the GMAC_TXMODE register.	R
b31	TFULL	TX FIFO Almost Full	This bit is set to 1 when the number of empty words in the TX FIFO buffer is less than or equal to the threshold set by the TFULLTH[1:0] bits in the GMAC_TXMODE register.	R

28.2.2.14 TCPIPACC Register (GMAC_ACC)

The GMAC_ACC register is used to control operation of the TCP/IP accelerator.

Address(es): ETHERC.GMAC_ACC A00F 0208h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RTCPIPACC	TTCPIPEN	RTCPIPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	RTCPIPEN	RX TCPIP Accelerator Enable	1: RX TCPIP Enable Enables the RX TCPIP accelerator. 0: RX TCPIP Disable Disables the RX TCPIP accelerator. Padding is not inserted in the MAC headers.	R/W
b1	TTCPIPEN	TX TCPIP Accelerator Enable	1: TX TCPIP Enable Enables the TX TCPIP accelerator. 0: TX TCPIP Disable Disables the TX TCPIP accelerator. The padding in the MAC header is also disabled.	R/W
b2	RTCPIPACC	RX TCPIP Checksum Disable	1: RX TCPIPACC Off Disables checksum support for the RX TCPIP accelerator. Padding in the MAC header is inserted. 0: Checksum support for the RX TCPIP accelerator continues to be enabled (initial value).	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

28.2.2.15 RX MAC ENABLE Register (GMAC_RXMAC_ENA)

The GMAC_RXMAC_ENA register is used to control operation of the receive MAC.

Address(es): ETHERC.GMAC_RXMAC_ENA A00F 0220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMACEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RMACEN	RX MAC ENABLE	1: Enables reception (initial value). 0: Disables reception.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

28.2.2.16 LPI Mode Control Register (GMAC_LPI_MODE)

The GMAC_LPI_MODE register is used to control LPI (Low Power Idle) mode. When the LPMEN bit is 1, if transmission is not requested for a time longer than that specified by the LPRDEF bits in the GMAC_LPI_TIMING register, an LPI request is automatically issued to other party in the link. A transmission request being issued in LPI mode leads to exit from the LPI mode. After that, frames are transmitted after the time specified by the LPWTIME bit in the GMAC_LPI_TIMING register has elapsed.

Do not use this register to set LPI mode if ETHERC is connected via an Ethernet switch.

Address(es): ETHERC.GMAC_LPI_MODE A00F 0224h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LPMEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	LPMEN	Low Power Idle Mode	1: ETHERC operates in LPI mode. 0: ETHERC does not operate in LPI mode.	R/W

28.2.2.17 LPI CLIENT Timing Control Register (GMAC_LPI_TIMING)

The GMAC_LPI_TIMING register is used to control the signal timing in LPI mode.
Note that this register is not used if ETHERC is connected via an Ethernet switch.

Address(es): ETHERC.GMAC_LPI_TIMING A00F 0228h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LPRDEF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LPWTIME[15:0]															
Value after reset:	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	LPWTIME [15:0]	Low Power Idle Wake Time	Sets the time before frames can be sent to a link after the IDLE signal is sent to the link when LPI is terminated for the link partner. In Gigabit mode, a value can be set in 8 nanoseconds. In 100 Mbps mode, a value can be set in 40 nanoseconds.	R/W
b31 to b16	LPRDEF [15:0]	Low Power Idle Request Deferral	Sets the delay time before an LPI request is sent to the link partner. In Gigabit mode, a value can be set in 8 nanoseconds. In 100 Mbps mode, a value can be set in 40 nanoseconds.	R/W

28.2.2.18 Reception Buffer Information Register (BUFID)

The BUFID register is a status register that indicates the information on the reception buffer (such as whether or not it contains received data, the address of the buffer, and the number of words it holds). On completion of transfer by the reception MACDMA, up to 64 items of reception buffer information are written to this register. Storage of the data in the reception buffer information register leads to the generation of an Ethernet MACDMA reception complete interrupt (ETHDMAIR). This interrupt remains active until the NOEMP bit is cleared to 0 after no received data remains to be read from the buffers.

This register indicates the information of the next received data every time it is read. 0 is read from this register if there are no received data.

Address(es): ETHERC.BUFID A00F 1100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NOEMP	—	—	VALID	WORD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ADDR[15:0]	Reception Buffer Address Data	Reception buffer address (bits 26 to 11)	R
b27 to b16	WORD[11:0]	Receive Data Word Count	Number of words in receive data (including receive MAC information)	R
b28	VALID	Receive Data Validity	1: The receive data is valid. 0: The receive data is invalid.	R
b30, b29	—	Reserved	These bits are read as 0. The write value should be 0.	R
b31	NOEMP	Reception Buffer Data Storing Status	1: There are data in the reception buffer. 0: There are no data in the reception buffer.	R

ADDR[15:0]

The ADDR bits cannot indicate an address in the 32-bit address space. Therefore, to access a memory-mapped buffer, use an offset of 0800 0000h, where the buffer RAM starts from.

To calculate the reception buffer Address(es):

1. Obtain the value of the ADDR bits.
2. Shift the value to the left by 11 bits.
3. Add an offset of 0800 0000h.

WORD[11:0]

The number of words indicated by the WORD bits includes the number of words in the receive frame information. Therefore, the start address of the receive frame information is calculated as follows.

To calculate the start address of the receive frame information:

1. Obtain the value of the Word bits.
2. Shift the value to the right by 16 bits.
3. Add the number of words shifted in step 2 to the reception buffer address as an offset.
4. Negatively offset the value by 2 words (the size of the receive frame information).

28.2.3 Hardware Function Call Register

The hardware function call register is used to obtain a buffer. This register is also used to start transmission or reception. After argument registers (R4 to R7) are configured, a hardware function is executed by writing a command to the command register (SYSC). For details on how to configure the hardware function call register, see section 28.3.1, Hardware Functions.

Note: Registers related to hardware functions are also used to control the hardware OS accelerator.

28.2.3.1 Hardware Function System Call Register (SYSC)

When a command is written to the SYSC register, the corresponding function is executed.

Address(es): ETHERC.SYSC A00E F000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSC[15:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SYSC[15:0]	System Command Specification	Specifies the hardware function to be used. One of the following functions can be specified:	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SYSC[15:0]	Functions
5000h	Acquires a long buffer.
5006h	Acquires a short buffer.
5001h	Release the whole area of the buffer.
5002h	Release the part of the buffer.
5101h	Enables DMA for the reception MAC.
5102h	Disables DMA for the reception MAC.
510Bh	Controls reception MACDMAC interrupts.
510Dh	Obtains the error source in reception MACDMAC.
5100h	Starts transfer of reception MACDMAC.
510Ch	Obtains the error source in transmission MACDMAC.
5211h	Starts DMA transfer between the buffer RAM and data RAM.
5212h	Starts replacing data in the buffer RAM or data RAM.
Other than above	Setting prohibited

28.2.3.2 Hardware Function Argument Register (Rn) (n = 4 to 7)

The Rn register is used to write an argument to be passed to a hardware function. The argument register to be used differs depending on the hardware function. For details, see section 28.3, Operation.

- R4

Address(es): ETHERC.R4 A00E F004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	R4B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	R4B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R4B[31:0]	R4 Argument Specification	Specifies the argument to be passed to the hardware function.	R/W

- R5

Address(es): ETHERC.R5 A00E F008h

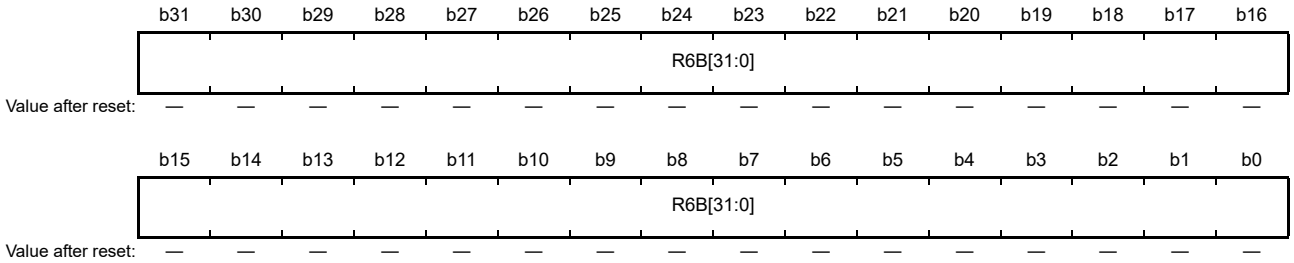
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	R5B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	R5B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R5B[31:0]	R5 Argument Specification	Specifies the argument to be passed to the hardware function.	R/W

- R6

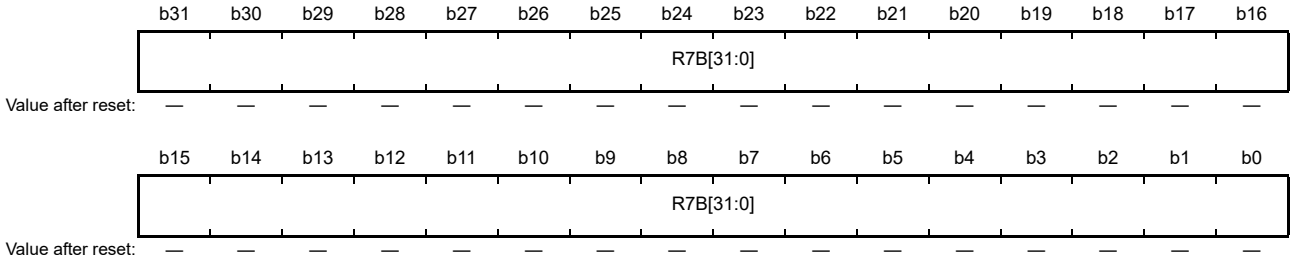
Address(es): ETHERC.R6 A00E F00Ch



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R6B[31:0]	R6 Argument Specification	Specifies the argument to be passed to the hardware function.	R/W

- R7

Address(es): ETHERC.R7 A00E F010h

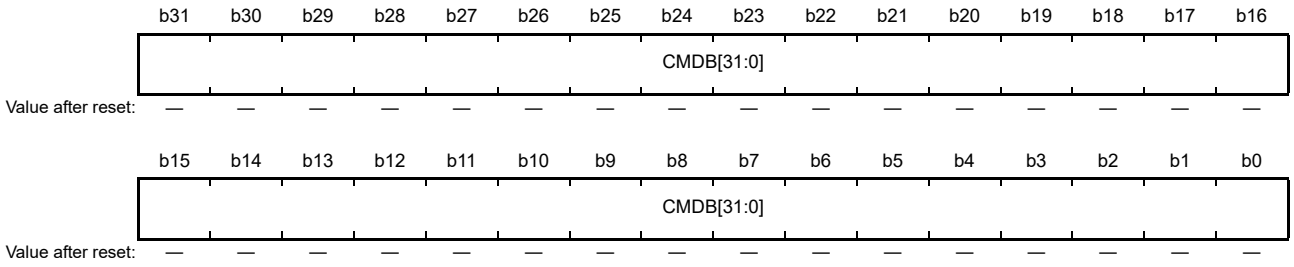


Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R7B[31:0]	R7 Argument Specification	Specifies the argument to be passed to the hardware function.	R/W

28.2.3.3 Hardware Function Command Register(CMD)

This register is for setting commands for hardware functions.

Address(es): A00E F014h



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CMDB[31:0]	Command Setting	These bits set the commands for hardware functions.	R/W

28.2.3.4 Hardware Function Return Value Register (R0, R1)

R0 and R1 are the read-and-clear registers that are used to store the value returned from a hardware function. The returned value depends on the hardware function. For details, see section 28.3, Operation.

- R0

Address(es): ETHERC.R0 A00E F020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	R0B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	R0B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R0B[31:0]	R0 Return Value Storage	Specifies the argument to be passed to the hardware function. These bits are read as 0 due to read-and-clear function.	R/W

- R1

Address(es): ETHERC.R1 A00E F024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	R1B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	R1B[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	R1B[31:0]	R1 Return Value Storage	Specifies the argument to be passed to the hardware function. R0 and R1 are the read-and-clear registers that	R/W

28.2.3.5 Hardware Function Type Register (C0TYPE)

This register is for setting type of hardware function.

Address(es): A00E 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	C0TYPEB[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	C0TYPEB[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	C0TYPEB[31:0]	HW Function Type Setting	These bits set the type of hardware function.	R/W

28.2.3.6 Hardware Function State Register (C0STAT)

This register is for setting the states of hardware function.

Address(es): A00E 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	C0STATB[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	C0STATB[31:0]															
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	C0STATB[31:0]	HW Function State Setting	These bits set the states of hardware function.	R/W

28.3 Operation

28.3.1 Hardware Functions

A hardware function (HWF) is defined as a function for reducing the load on the CPU, such as a DMAC or Ethernet communications accelerator.
A hardware function consists of a combination of hardware modules which are divided by function, and an overall function is defined for the set of individual hardware modules.
The following three functions are defined as hardware functions.

- Buffer allocator
- MAC DMA controller
- Buffer RAM DMA controller

Figure 28.3 is a schematic block diagram of these hardware functions in context. Solid lines in the figure indicate the flow of data, while broken lines indicate a command interface with the hardware function.

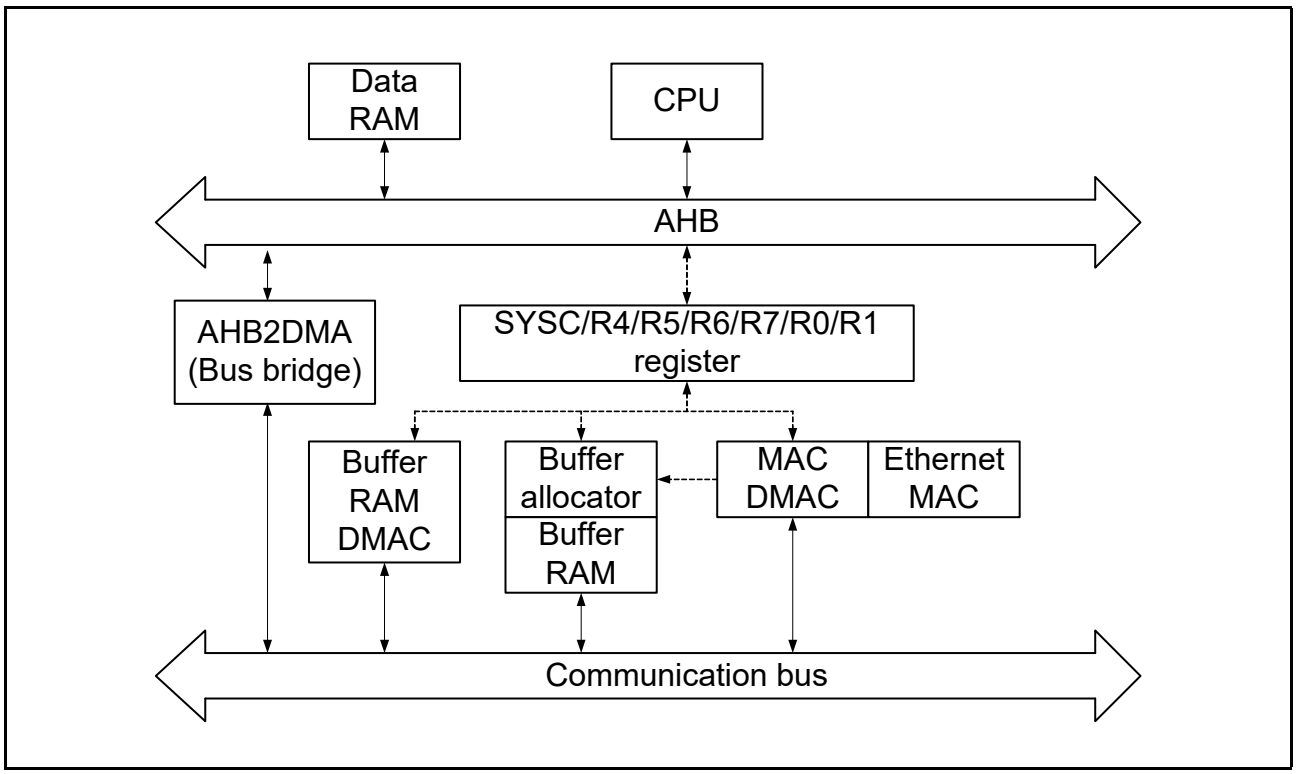


Figure 28.3 Schematic Block Diagram of the Hardware Functions

Note: For products incorporating an R-IN Engine, calling the hardware function while the hardware real-time OS is prohibited from dispatching does not successfully execute the call. Be sure to call the hardware function while dispatching is allowed. Also, the operations of the hardware real-time OS are not synchronized with the operations of the Ethernet MAC controlled by the Cortex-R4, which means, whether to allow dispatching or not is not properly controlled by the core. Therefore, do not use the hardware real-time OS while controlling the Ethernet MAC by the Cortex-R4.

28.3.1.1 Initial Settings

First, use the MSTPCRB18 bit of the module stop control register B (MSTPCRB) to release the module from the module-stop state and use the Ethernet MAC reset register (EMACRST) to release the entire Ethernet MAC module from the reset state. Also, use the Ethernet peripheral reset register (ETHSFTRST) to release the peripheral devices from the reset states. It does not matter which of EMACRST and ETHSFTRST to be set first.
After that, execute the commands listed below to set up the hardware functions.

Procedure for setting up the hardware functions
<1> Set 0000 0003h in the C0TYPE register.
<2> Set 0000 0003h in the C0STAT register.
<3> Set 0000 8004h in the CMD register.
Confirm that the bit 31 of the hardware function return value register R0 is set. Also, dummy-read the hardware function return value register R1 to clear it.
<4> Wait until 8000 0000h is read from the R0 register.
<5> Set 8000 0000h in the GMAC_RESET register to initialize the Ethernet MAC.

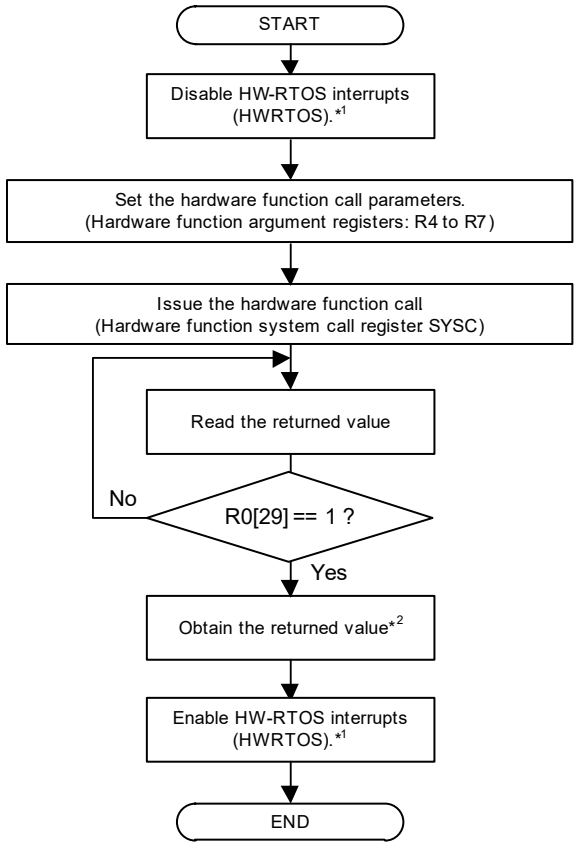
Note: When using the hardware OS accelerator function, the above settings are not required since it is controlled by setting up the OS accelerator function (only for the products incorporating and R-IN engine).

After the completion of setup, make initial settings in the registers below.

- MAC address register (→ Section 28.2.2.11)
- TX MODE register (→ Section 28.2.2.6)
- RX MODE register (→ Section 28.2.2.5)

28.3.1.2 Flow of Processing for Issuing the Hardware Function Call

If you are using a hardware function, follow the flowchart below to issue the hardware function call.



Note 1. This processing is only required when the hardware real-time OS is in use.
Note 2. The hardware function recognizes that the result registers were read by reading the R0 and R1 registers. Be sure to read R1 even in the system call which does not use R1 for storing the returned value.

Figure 28.4 Flow of Processing for Issuing the Hardware Function Call

28.3.1.3 Buffer Allocator

(1) Functional Overview

The buffer allocator is a module for controlling the buffer RAM.
The buffer RAM is a communications buffer to improve throughput in Ethernet transfer. Although the buffer RAM has 128 Kbytes, an area of 128 Mbytes is used as the logical space for the dynamic securing and releasing of memory space by the buffer allocator.
To use the buffer RAM, secure the required area (hereafter “buffer”) beforehand, and then issue the hardware function calls provided for the buffer allocator. When writing to an area which has not been secured, access by the CPU or MAC DMA controller generates an interrupt, whereas access to such area by the buffer RAM DMA controller generates an interrupt or returns an exception to the return value register R0 depending on the type of hardware function call.
To reuse a buffer after having secured it, the buffer must be released after it has been used.

The outline of the functions is as follows:

- A long buffer of up to 2048 bytes and short buffer of up to 512 bytes are available.
- When securing a buffer, the size is specified in bytes.
- When releasing a buffer, the size can be specified for the whole area or as the location of a byte (the part of the buffer from that address is released).

The segments which constitute a buffer are of 128 bytes each. The buffer allocator controls each of these 128-byte segments, and connect these segments in response to hardware function calls to provide these as buffers. Addresses are seen as continuous across contiguous segments.

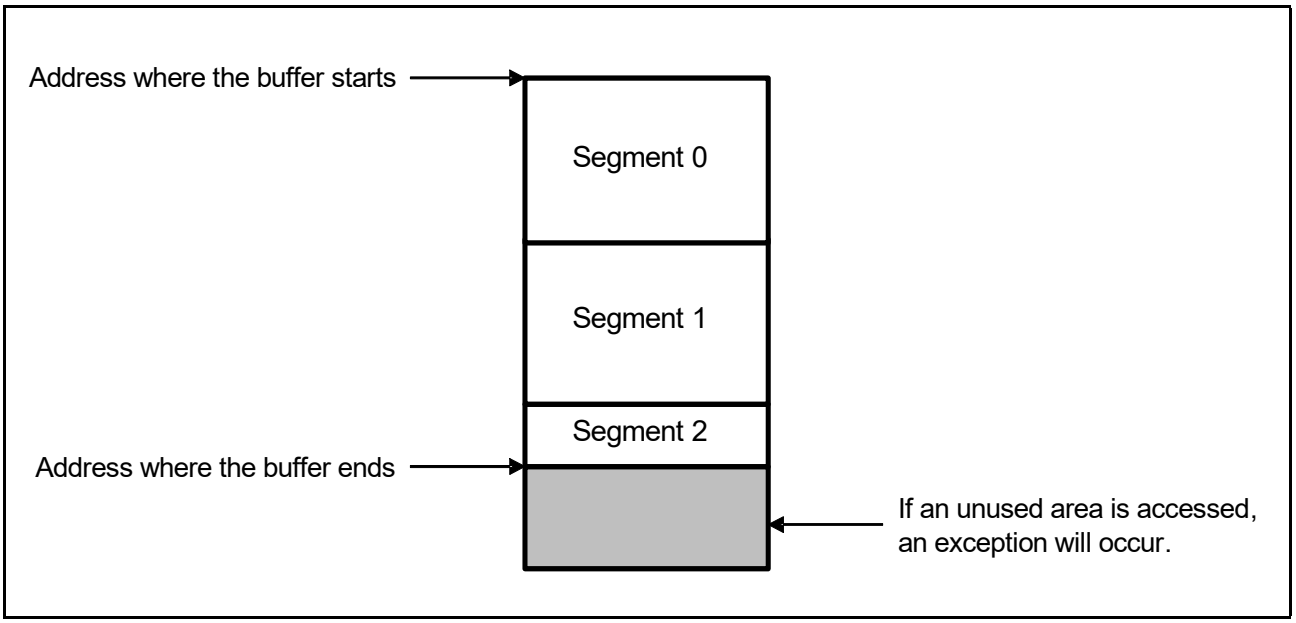


Figure 28.5 Method of Controlling a Buffer

(2) Buffer Control Operation

In this section, short and long buffers are collectively referred to as “buffers”. A short buffer has up to four segments and a long buffer has up to 16 segments.

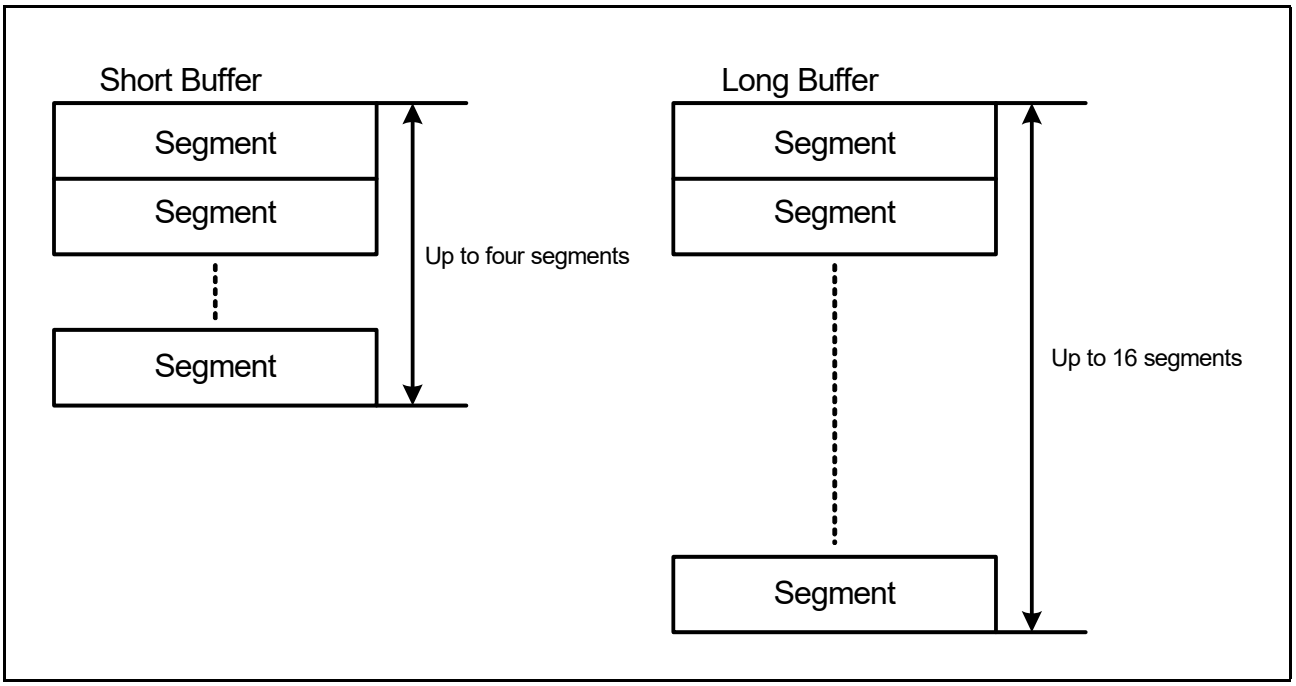


Figure 28.6 Buffer Structure

(a) Acquisition of buffers (HWFNC_ShortBuffer_Get, HWFNC_LongBuffer_Get)

Buffers can be acquired by issuing an HWFNC_ShortBuffer_Get or HWFNC_LongBuffer_Get hardware function call. The size of the buffer is specified in bytes when calling these hardware functions. The number of bytes does not have to reach a segment boundary (128 bytes). The value returned is the address where the buffer starts.
The maximum numbers of short and long buffers that can be acquired are as listed in Table 28.7. Even if fewer short and long buffers are acquired than the maximum, acquisition will fail if the total size of buffers of both sizes exceeds the maximum size imposed by the 128 Kbytes of buffer RAM.

Table 28.7 Number of Buffers that can be Acquired

Buffer Type	Maximum Number of Buffers that can be Acquired	Remarks
Short buffer	128	Up to 512 segments (= 64 Kbytes)
Long buffer	64	Up to 1024 segments (= 128 Kbytes)

The address structure of buffers is shown below. When a buffer is acquired, the function returns the address range from 0C00 0000h to 0FFF FFFFh and 0800 0000h to 0BFF FFFFh for a long buffer and short buffer, respectively.

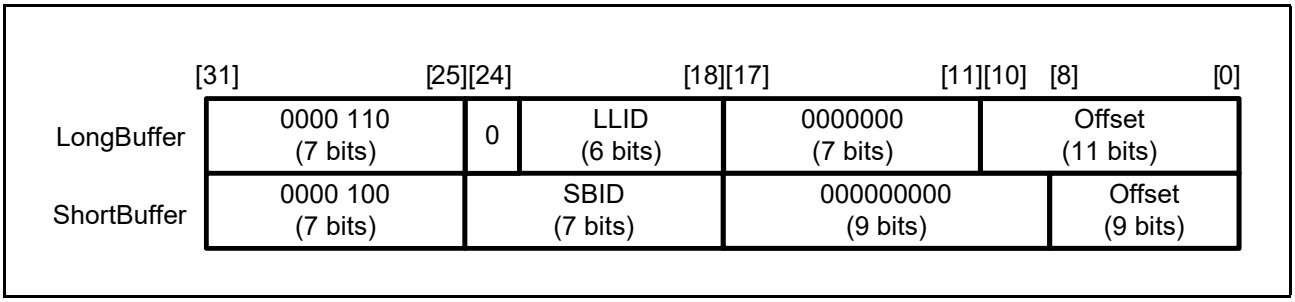


Figure 28.7 Address Structure of Buffers

If a short buffer is acquired, bits [24:18] are given an SBID (short buffer ID), which is used as an identifier for the buffer. The buffer area is allocated with the offset field as 0 to indicate the address where the buffer starts.
If a long buffer is acquired, bits [23:18] are given an LLID (linked long buffer ID), which is used as an identifier for the buffer. The buffer area is allocated with the offset field as 0 to indicate the address where the buffer starts.

(b) Releasing whole area of a buffer (HWFNC_Buffer_Release)

The whole area of an acquired buffer can be released by calling the HWFNC_Buffer_Release hardware function. When calling the hardware function, specify the address where the acquired buffer to be released starts.

(c) Releasing part of a buffer (HWFNC_Buffer_Return)

By calling the HWFNC_Buffer_Return hardware function, desired bytes can be released, starting from the location of a byte within the acquired buffer. This is provided for efficiency in using the space; for example, when a frame is received, another resource can use the area obtained by releasing the area following the end of the received frame data. When executing this system call, the addresses where the buffer and the space to be released start must be given as arguments.

(d) Testing memory and initializing buffers

Since it is not allocated at the time of a reset, buffer RAM is neither writable nor readable in that situation. Accordingly, to test the memory, execute the HWFUNC LongBuffer_Get system call, etc., to secure the full capacity of the buffer RAM and make that memory available for access. This enables subsequent checking of the memory and initializing its contents.

(e) List of Hardware Function Calls

The hardware function calls are listed below and on the following pages.
If an argument of a hardware function call is not correct, the code indicating an invalid system call is returned to the return value register, R0.

Table 28.8 HWFNC_LongBuffer_Get

Name	HWFNC_LongBuffer_Get	
Function	Acquires a long buffer for use in the transmission and reception of frames. A buffer can be acquired with any size in bytes between 1 and 2048. Long buffers are mainly used to hold the data sections of frames. The address where the acquired buffer starts is returned in R1 as the value returned.	
Command register		
SYSC[15:0]	5000h	
Argument registers		
R4	[15:0] Buffer Length	Required buffer length. Unit: bytes. 1 to 2048
	[23:16]	These bits are reserved. Always set these bits to 0.
	[31:24]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0] First logical address of the buffer	[31:27] 00001b [26:24] 100b [23:18] LLID [17: 0] 0

Note: For the products incorporating an R-IN Engine, issuing of this command while the hardware real-time OS is prohibited from dispatching does not successfully excecute the hardware function call. In this case, bits 15:0 of the return value register R0 indicates FFE7h.

Table 28.9 HWFNC_ShortBuffer_Get

Name	HWFNC_ShortBuffer_Get	
Function	Acquires a short buffer for use in the transmission and reception of frames. A buffer can be acquired with any size in bytes between 1 and 512. Short buffers are mainly used to hold the header sections of frames, the data sections of ICMP and MAC management frames, etc. The address where the acquired buffer starts is returned in R1 as the value returned.	
Command register		
SYSC[15:0]	5006h	
Argument registers		
R4	[15:0] Buffer Length	Required buffer length. Unit: bytes. 1 to 512
	[31:16]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	0xb: Success 10b: Invalid system call 11b: The buffer is insufficient
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0] First logical address of the buffer	[31:27] 00001b [26:25] 00b [24:18] SBID [17: 0] 0

Table 28.10 HWFNC_Buffer_Release

Name	HWFNC_Buffer_Release	
Function	Releases an acquired long or short buffer.	
Command register		
SYSC[15:0]	5001h	
Argument registers		
R4	[31:0] First logical address of the buffer	First logical address of the buffer to be released The value is returned in R1 following a call of HWFNC_LongBuffer_Get or HWFNC_ShortBuffer_Get.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	0xb: Success 10b: Invalid system call 11b: A buffer is not definable at the given address.
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

Table 28.11 HWFNC_Buffer_Return

Name	HWFNC_Buffer_Return	
Function	Releases some of the latter half of an acquired short or long buffer. Specifying the location where the address range to be released starts leads to the release of the part of the buffer beginning at that address. The address can be set at byte boundaries. This HWF is for the efficient use of buffer resources, for example when a received frame is short.	
Command register		
SYSC[15:0]	5002h	
Argument registers		
R4	[31:0] First logical address of the buffer	First logical address of the buffer to be released The value is returned in R1 following a call of HWFNC_LongBuffer_Get or HWFNC_ShortBuffer_Get.
R5	[31:0] First logical address of the part for release	First address of the part for release (the part of the buffer at addresses beginning from this address is released)
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[2:0] Result	00xb: Success 010b: Invalid system call 011b: A buffer has not been defined at the address specified by R4. 100b: The buffer at the address specified by R5 has already been released.
	[28:3]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

28.3.1.4 MAC DMA Controller

(1) Functional Overview

The MAC DMA controller is used to transfer data between the buffer RAM and Ethernet MAC. In transmission, the DMAC transfers data to be transmitted from the buffer RAM to the Ethernet MAC; in reception, the DMAC transfers data received by the Ethernet MAC to the buffer RAM. This allows improved throughput for communications.
Figure 28.8 is a block diagram of the MACDMAC in context and the respective interrupt signals.

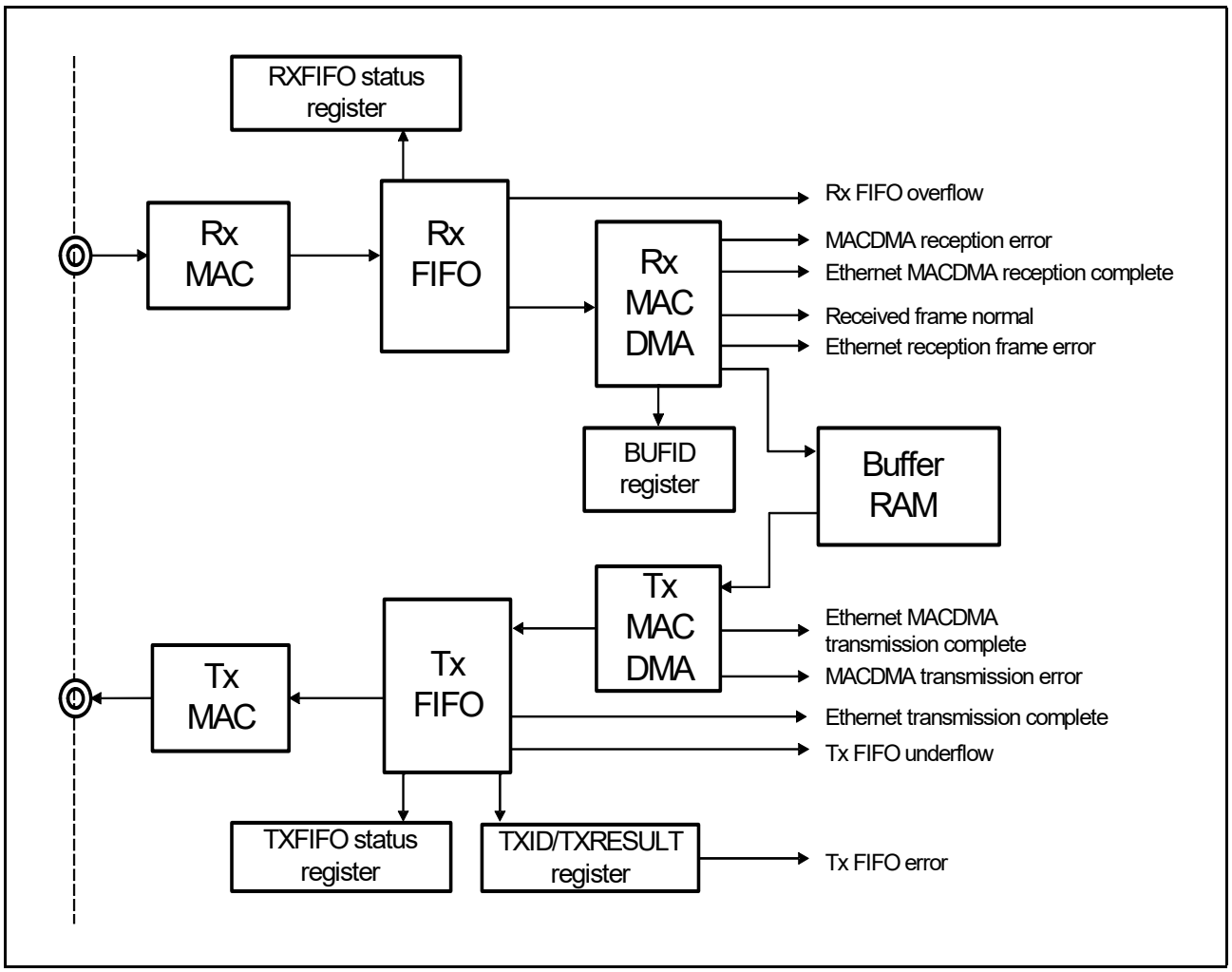


Figure 28.8 Block Diagram of the MACDMAC in context and Interrupt Signals

(2) DMA for the reception MAC

Figure 28.9 shows an outline of processing by the reception MACDMAC. A hardware function call (HWFNC_MACDMA_RX_Enable) must be issued to enable operation of the reception MACDMAC. The reception MACDMAC remains active until HWFNC_MACDMAC_RX_Disable is issued.
While active, the reception MACDMAC constantly monitors the state of the MAC Rx FIFO. When the FIFO holds a received frame, the reception MACDMAC sends a request for the acquisition of a long (2048-byte) buffer to the buffer allocator. Once the long buffer has been acquired, the reception MACDMAC reads data from the MAC Rx FIFO and writes the data sequentially from the start of the acquired long buffer.
After the completion of the full transfer of one frame, the reception MACDMAC writes the number of received words (one word: 32 bits) and the first logical address of the buffer to the BUFID register as information on reception. The information written to the BUFID is described in section 28.2.2.18, Reception Buffer Information Register (BUFID). The BUFID can be read by the CPU and is capable of holding up to 64 pieces of information.

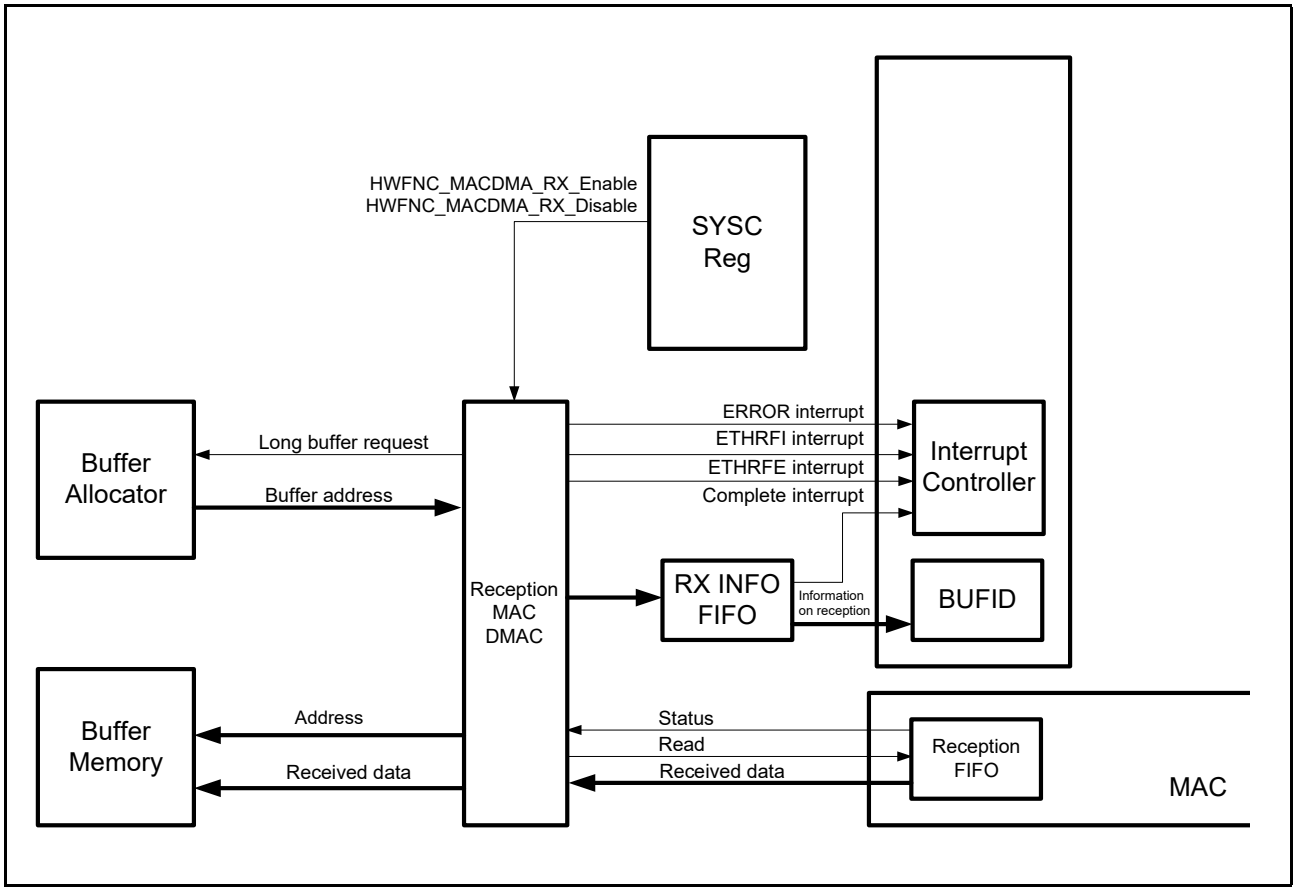


Figure 28.9 Outline of Processing by the Reception MACDMAC

(a) Description of the individual functions of the MAC DMA controller

1-1) Partial release of buffer space

The reception MACDMAC automatically releases an unused area that has no received data in the last buffer to have been acquired (buffer return function call). However, if the unused area is no larger than 128 bytes (one segment), buffer return does not proceed. Buffer return is a function call to release part of the secured buffer area and differs from the buffer release function call that releases the whole area of a secured buffer.

1-2) Full release of the buffer

If the following conditions are satisfied, the reception MACDMAC automatically releases the acquired buffer (calls the buffer release function).

(1) The result of executing the function call for the buffer acquisition request was failure (the buffer has no unused area).
(2) The result of analyzing the information on the received frame is that the received frame is made invalid by HWFNC_MACDMA_RX_Control.
(3) HWFNC_MACDMA_RX_Disable is executed under the following condition:
- The number of received words is not greater than 4092 words

In the above cases 1) and 2), all received frames are discarded and the buffer is released. In case 3), the received frames are not discarded (data resides in the MAC Rx FIFO) but only the release of the buffer is executed, after which the reception MACDMAC is immediately disabled. In any of cases 1), 2), and 3), the result of reception is not written to the BUFID.

1-3) Generation of an error interrupt

An error interrupt is issued in response to detection of the reception MACDMAC having failed to continue operation for reception for some reason or data not having been received correctly. The source of an error interrupt can be checked by executing the hardware function call HWFNC_MACDMA_RX_Errstat.
For details, see (c) List of hardware function calls.

1-4) Generation of reception completed interrupts

If the BUFID has information on the reception of one or more frames, the reception completed interrupt goes to its active level. The reception completed interrupt remains active as long as the BUFID register is not empty; that is, it has information on the reception of one or more frames.
The reception completed interrupt is de-asserted when the BUFID is read and becomes empty.

1-5) Judging whether a received frame is valid or invalid

Judgment of whether a received frame is valid or invalid leads to a received frame normal interrupt (ETHRFI) or Ethernet reception frame error interrupt (ETHRFE) being issued. Each interrupt has more than one source and the generation of interrupts is enabled for all sources in the initial state.

A specified source can be disabled by executing HWFNC_MACDMA_RX_Control. The frame corresponding to the factor that caused disabling is discarded by the whole-buffer release function.

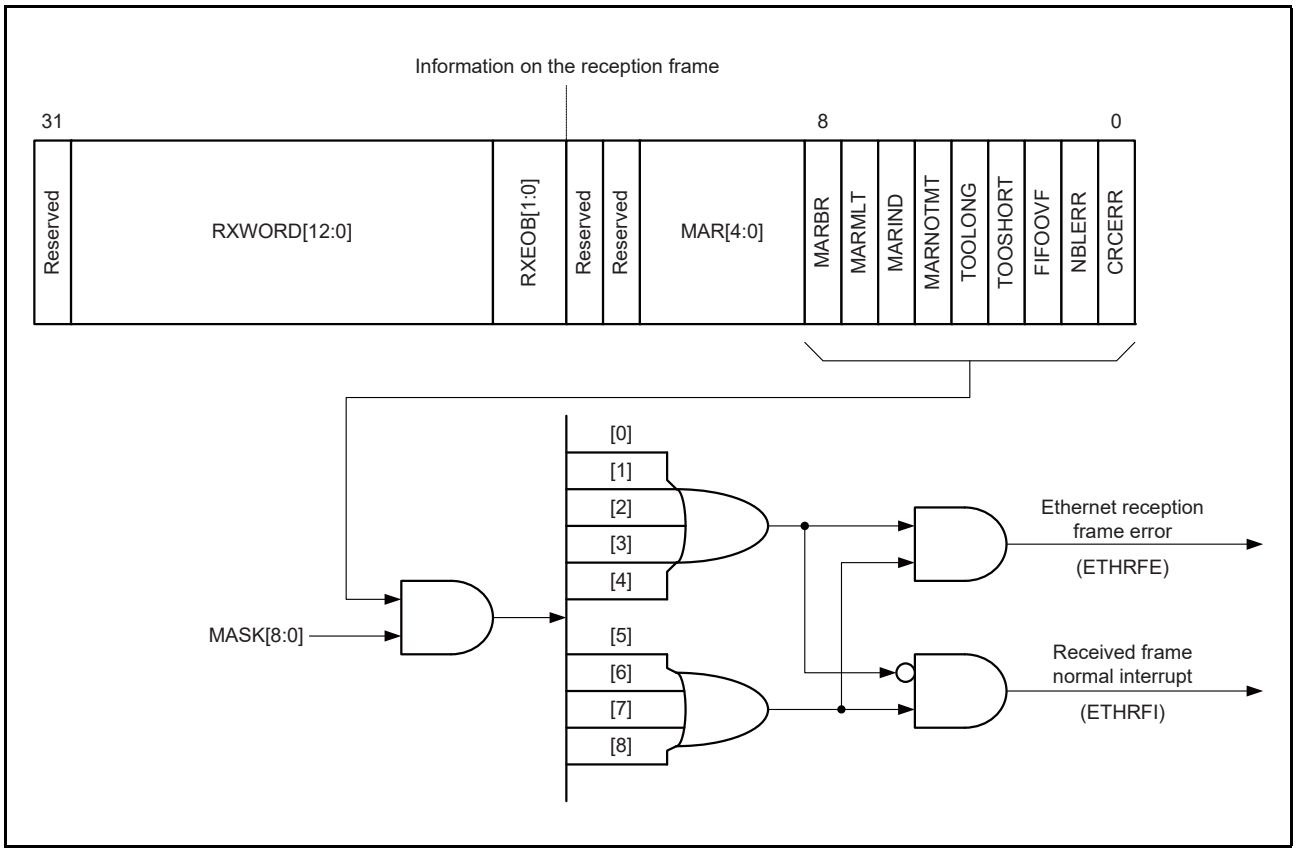


Figure 28.10 Conceptual Diagram of Judging Whether a Received Frame is Valid or Invalid

(b) Usage

2-1) Procedure for reading and releasing buffers

A buffer which has received data must always be released after use. An example of the procedure is given below.

[Example of reading and releasing a buffer]

(1) Read the BUFID register.
(2) Shift the bits [27:16] read from BUFID 16 bits to the right to obtain the number of received words.
(3) The bits [15:0] read from the BUFID are bits [26:11] of the address where the acquired buffer starts.
The individual bits of the address where the acquired buffer starts are configured as follows.
[31:27]: 00001b
[26:18]: Equivalent to bits [15:7] in the BUFID
[17:11]: Equivalent to bits [6:0] in the BUFID
[10:0]: Always 0
(4) After using the buffer, specify the start address as an argument and issue the buffer release function call to release the buffer.

2-2) Procedure for processing in response to an error interrupt

An example of the recommended procedure for processing in response to an error interrupt is given below. The value of R0[7:0] obtained by the HWFNC_MACDMA_RX_ERRSTAT function call is hereafter called bits [7:0] of the result of reading the error state.

(1) Bit [3] of the result of reading the error state = 1 (a function call to forcibly end MACDMA Rx has been executed)
(a) If bit [0] of the result of reading the error state = 1, proceed to step 3).
(b) If bits [2:0] of the result of reading the error state have the value 4 or 0, the interrupt source is the forced termination of reception while it was in progress and this does not represent a problem. Since the received frames are all discarded and the information is not written to the BUFID, nothing is done, so simply return to normal processing. The reception MAC FIFO may still have frame data that was received, but in such cases, the hardware automatically discards that data before the next round of reception starts.

(2) Bit [2] of the result of reading the error state = 1 (the size of the frame is at least 4096 words)
(a) If bit [0] of the result of reading the error state = 1, proceed to step 3).
(b) Received data are all stored. The start address is obtained by reading the BUFID.
(c) Buffers that are no longer required are released according to the method given as [Example 2] in 2-1) Procedure for reading and releasing buffers.
(d) Returns to normal processing.

(3) Bit [0] of the result of reading the error state = 1 (the remaining capacity of the buffer is insufficient)
(a) If bit [2] of the result of reading the error state = 1 (the size of the received frame is at least 4096 words) is satisfied at the same time, the buffer capacity is considered temporarily insufficient, so nothing is done.
(b) If the remaining capacity of the buffer is considered insufficient, the buffer is released to provide space.
(c) Return to normal processing. Note that received frames may have been lost during this period.

(c) List of hardware function calls

The table below lists the hardware function calls.
If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.
If an error occurs while the hardware function call is running, an interrupt is generated.

Table 28.12 HWFNC_MACDMA_RX_Enable

Name	HWFNC_MACDMA_RX_Enable	
Function	Enables DMA for the reception MAC, that is, the transfer of data to the buffer memory from the MAC. As long as the reception DMAC is enabled, transfer starts automatically whenever the FIFO buffer within the MAC collects received frames. Since the DMAC executes Get Buffer at this time, the buffer memory is automatically acquired.	
Command register		
SYSC[15:0]	5101h	
Argument registers		
R4	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[0] Result	0: Success 1: Invalid system call*1
	[28:1]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

Note 1. If this hardware function is called while it is not disabled (this function call is already being executed) or this hardware function is called while a buffer return or release operation is in progress after reception has been suspended, the result is an invalid system call.

Note: The number of bytes to be transferred at a time is from 4 to 2048 bytes. Exceeding this range leads to the generation of an exception.

Table 28.13 HWFNC_MACDMA_RX_Disable

Name	HWFNC_MACDMA_RX_Disable		
Function	Disables DMA for the reception MAC. When forced reset is enabled, the data being received are discarded and information on reception is not stored in the BUFID register. At this time, the buffer is automatically released. When forced reset is disabled, the buffer is not automatically released.		
Command register			
SYSC[15:0]	5102h		
Argument registers			
R4	[0] Forced reset		0: This function is disabled while reception is in progress. 1: If the reception DMAC is enabled, it is disabled even if reception is in progress (the reception DMAC is forcibly reset). Nothing is done if the reception DMAC is already disabled.
	[31:1]		Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]		Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]		Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]		Note: These bits are not used in this function call. The setting will be ignored.
Return value registers			
R0	[1:0] Result	When R4[0] = 0	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended) 10b: The function cannot be disabled since reception is in progress. 11b: The function has already been disabled.
		When R4[0] = 1	00b: Success 01b: Invalid system call (the buffer is in use or reception is suspended)
	[28:2]		These bits are reserved. The value is always 0.
	[29] Complete		0: Hardware function call not completed 1: Hardware function call completed
	[31:30]		These bits are reserved. The value is always 0.
R1	[31:0]		These bits are reserved. The value is always 0.

Table 28.14 HWFNC_MACDMA_RX_Control

Name	HWFNC_MACDMA_RX_Control	
Function	Controls enabling or disabling of the interrupt source corresponding to bits [8:0] of the received frame information.	
Command register		
SYSC[15:0]	510Bh	
Argument registers		
R4	[8:0] Interrupt source	Controls enabling or disabling of the interrupt source corresponding to each bit.*1 0: Interrupts disabled 1: Interrupts enabled (initial value)
	[31:9]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[0] Result	0: Success 1: Invalid system call
	[28:1]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

Note 1. For details on the interrupt sources, see Figure 28.10, Conceptual Diagram of Judging Whether a Received Frame is Valid or Invalid.

Table 28.15 HWFNC_MACDMA_RX_Errstat

Name	HWFNC_MACDMA_RX_Errstat	
Function	Obtains error interrupt sources for the reception MACDMAC.	
Command register		
SYSC[15:0]	510Dh	
Argument registers		
R4	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[3:0] Result	[0]: Buffer Get fails [1]: Always 0 [2]: Received data has exceeded 4096 words (16 Kbytes). [3]: HWFNC_MACDMA_Rx_Disable is issued when forced reset is enabled.
	[28:4]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

(3) DMA for the transmission MAC

(a) Usage

The transmission MACDMAC uses descriptors. The descriptors are located in the buffer memory. That is, the software must acquire a buffer for the descriptor by issuing using a hardware function call before DMA can be set up. This buffer can be long or short. One buffer can hold multiple descriptors.

A transmission descriptor is shown in detail in Figure 28.11, Transmission Descriptor. Note that a descriptor must start on a 64-bit boundary. If it is not on a 64-bit boundary, the result of trying to use it is in an invalid system call and the error value is stored in the return value register R0.
A descriptor is formed in a succession of a 32-bit address and a 32-bit transfer byte count. Address FFFF FFFFh indicates the end of a descriptor. The address field of a descriptor indicates the transmission start address, and the byte count indicates the number of bytes to be transmitted from that address. The DMAC reads the first pair of address and byte count in a descriptor, and then writes the specified data to transmission MAC FIFO. After that, the DMAC reads the next pair of address and byte count, and then writes the specified data to the transmission MAC FIFO. The DMAC continues this processing until it reads the end of the descriptor (FFFF FFFFh).
Source start addresses in the descriptor can be specified in units of bytes. The size of data to be transmitted can be specified in units of bytes. If the data writing point in the transmission FIFO is not at a word boundary, the DMAC automatically inserts padding.
The transmission MACDMAC starts when a function call HWFNC_MACDMA_TX_Start is issued. When this function call is issued, the start address of the transmit descriptor must be specified in the argument register R4.
Note that if the address field is not FFFF FFFFh and 0 is specified in the descriptor byte count field, the DMAC ignores the address field and does not perform transmission. In this case, DMA reads the next descriptor.
If the value of an address field is incorrect (for example, the address is outside the buffer area) or the number of transfer bytes is incorrect (for example, continued access causes a buffer area overflow), a MACDMA transmission error interrupt occurs.

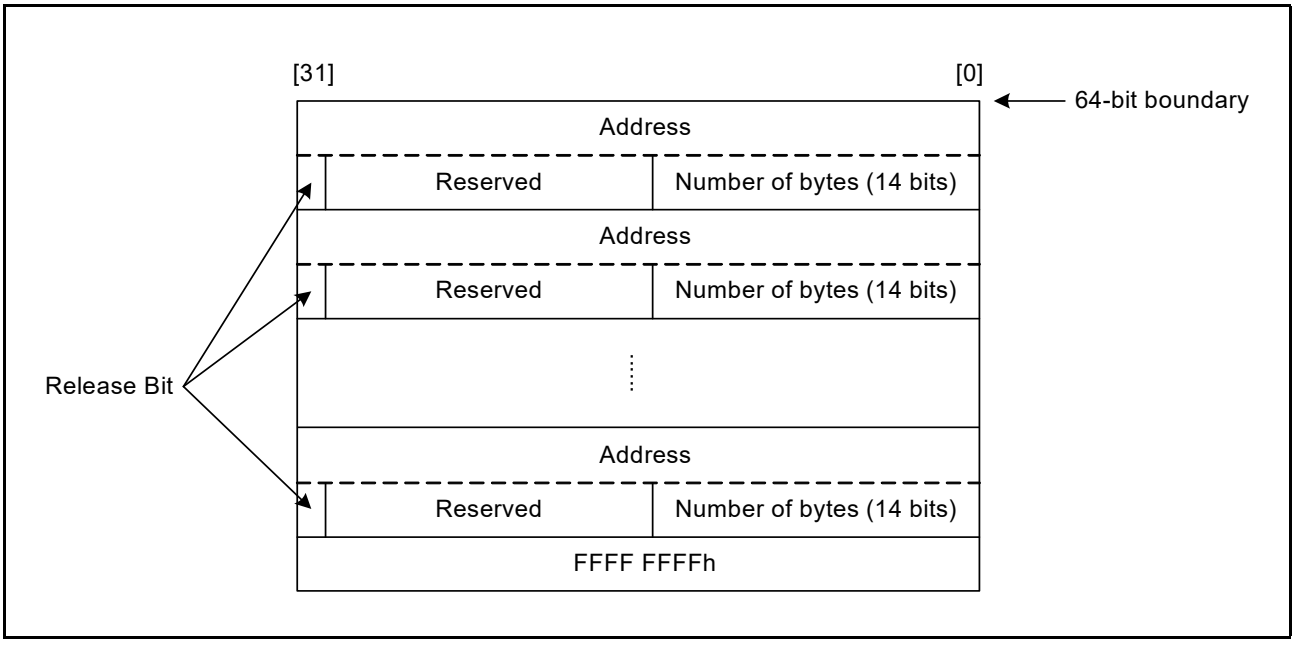


Figure 28.11 Transmission Descriptor

(b) Automatic release of the buffer

If the release bit of the transmission descriptor is 0, no buffer is released. If the release bit is 1, the transmission MACDMAC uses a buffer release function call to automatically release a buffer from the buffer area whose start address is indicated by the relevant descriptor after completion of transmission.

(c) Example of operation

Figure 28.12 shows an example of operation for transmission by combining multiple buffers for use by the transmission MACDMAC.

Two independent buffers of buffer 1 and buffer 2 are combined for transmission by the transmission MACDMA by allocating transmission descriptors at the consecutive 64-bit boundary addresses. The area labelled “Unused” means that the data end before the end of the segment (that is, it does not end at the 128-byte boundary). In transfer, the address where the data in a buffer start need not necessarily be the start of the buffer.

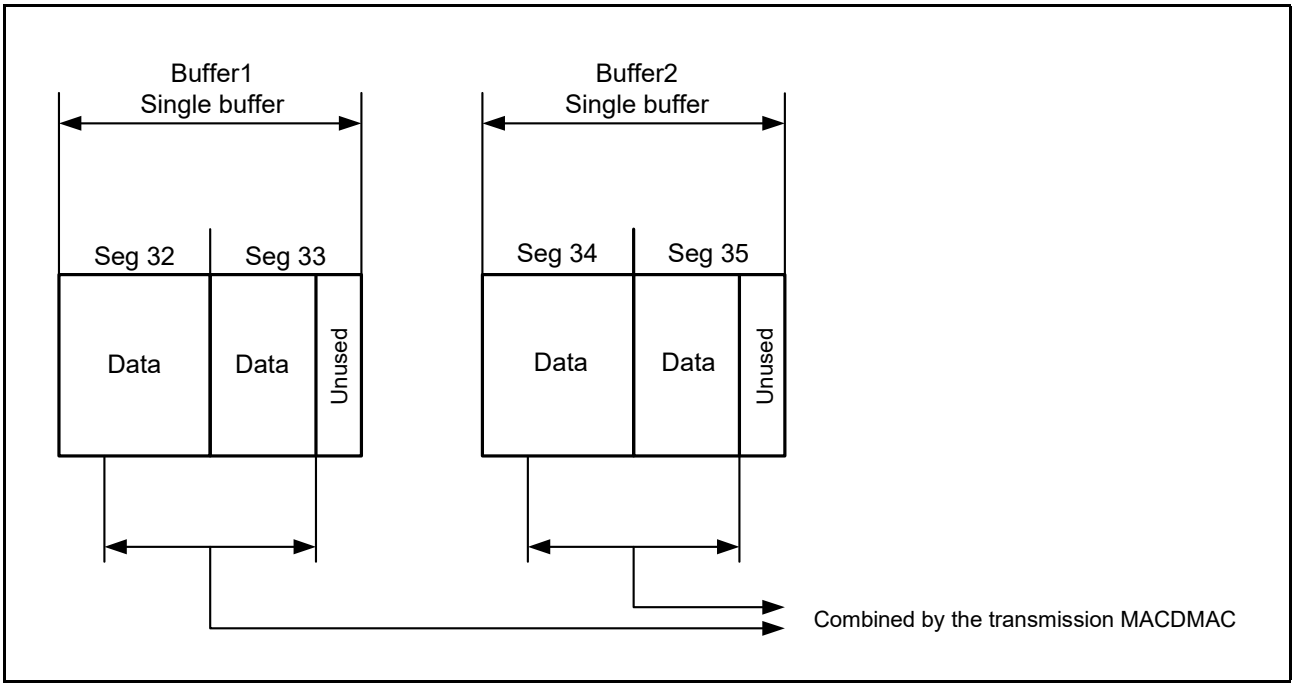


Figure 28.12 Example of Transmission as One Frame by Combining Multiple Buffers

(d) List of hardware function calls

The table below lists the hardware function calls.
If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.
If an error occurs while the hardware function call is running, an interrupt is generated.

Table 28.16 HWFNC_MACDMA_TX_Start

Name	HWFNC_MACDMA_TX_Start	
Function	Transfers data from the buffer memory to the Ethernet MAC. The address where the transmission descriptor starts is set in R4. When transfer ends, an interrupt is generated. The number of bytes to be transferred at a time is from 1 to 2048 bytes.	
Command register		
SYSC[15:0]	5100h	
Argument registers		
R4	[31:0] Address of the descriptor	Address of the transmission descriptor
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[6:0]	These bits are reserved. Always set these bits to 0.
	[31:7]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[0] Result	0: Success 1: Invalid system call
	[28:1]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

Table 28.17 HWFNC_MACDMA_TX_Errstat

Name	HWFNC_MACDMA_TX_Errstat	
Function	Obtains error interrupt sources for the transmission MACDMAC	
Command register		
SYSC[15:0]	510Ch	
Argument registers		
R4	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R5	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R6	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	[0]: 0: Success 1: Memory access violation • Access to a buffer that is not acquired • The number of bytes for transfer is invalid. • The address where the descriptor starts is not on a 64-bit boundary. [1]: 0: Success 1: Memory access timeout • The address where the transmission descriptor starts turns to be an end value (FFFF FFFFh). • Releasing the buffer with automatic buffer release failed.
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0]	These bits are reserved. The value is always 0.

28.3.1.5 Buffer RAM DMA Controller

(1) Functional Overview

The buffer RAM DMA controller transfers data between the buffer RAM and data RAM. It is used to transfer data for transmission by the MAC DMAC to the buffer and to transfer data received by the MAC DMAC to the data RAM.

(2) DMA transfer

Control of the buffer RAM DMA controller for each form of transfer is described below.

(a) Transfer between the buffer RAM and the data RAM

Calling the HWFNC_Direct_Memory_Transfer hardware function starts transfer between the buffer RAM and data RAM.
After the command has been issued, check that issuing the hardware function call has been completed by reading bit 29 in the R0 register. The DMA transfer has been completed at this point.

(b) Replacing data in the buffer RAM or data RAM

By executing the hardware function HWFNC_Direct_Memory_Replace, an area in the buffer RAM or data RAM can be overwritten by a desired 32-bit data pattern.
The start and end of the area to be written must be on 128-bit boundaries so the amount of data written must be a multiple of 128 bits.
After the command has been issued, check that issuing the hardware function call has been completed by reading bit 29 in the R0 register. The writing of the data pattern has been completed at this point.

(c) List of hardware function calls

The table below lists the hardware function calls.
If an argument of a hardware function call is invalid, an invalid system call error code is returned in the return value register, R0.
Access to an access-prohibited area (an area other than the buffer RAM, etc.) while the hardware function call is running leads to the return of an exception code in the return value register R0.

Table 28.18 HWFNC_Direct_Memory_Transfer

Name	HWFNC_Direct_Memory_Transfer	
Function	Transfers data from the data RAM to the buffer RAM or from the buffer RAM to the data RAM.	
Command register		
SYSC[15:0]	5211h	
Argument registers		
R4	[31:0] Address where the source area for transfer starts	Specifies the address where the source area for transfer starts.
R5	[31:0] Address where the destination area for transfer starts	Specifies the address where the destination area for transfer starts.
R6	[31:0] Number of bytes for transfer	Specifies the number of bytes for transfer.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	00b: Success 01b: Invalid system call (transfer from the buffer RAM to the buffer RAM has been specified) 10b: An exception has occurred
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0] Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

Table 28.19 HWFNC_Direct_Memory_Replace

Name	HWFNC_Direct_Memory_Replace	
Function	Replaces the specified memory area in the data RAM or buffer RAM with a defined data pattern. The number of words to be written must be at least four (a word is 32 bits).	
Command register		
SYSC[15:0]	5212h	
Argument registers		
R4	[31:0] Pattern	Specifies the data pattern for writing.
R5	[31:0] Start address	Specifies the address where the destination area for writing starts.
R6	[31:0] Number of words	Specifies the number of words to be written.
R7	[31:0]	Note: These bits are not used in this function call. The setting will be ignored.
Return value registers		
R0	[1:0] Result	00b: Success 01b: Invalid system call The set address was specified in byte units or the setting for the number of words to be transferred is three or fewer. 10b: An exception has occurred.
	[28:2]	These bits are reserved. The value is always 0.
	[29] Complete	0: Hardware function call not completed 1: Hardware function call completed
	[31:30]	These bits are reserved. The value is always 0.
R1	[31:0] Address where the exception occurred	When an exception has occurred, this is the address where it occurred. In other cases, all 0s.

28.3.2 Interrupts

The interrupts that the Ethernet MAC generates are described below.

Table 28.20 Interrupts related to Operations for Transmission

Interrupt Name	Symbol	Conditions for Asserting and De-asserting Interrupts
TX FIFO underflow	ETHTFIU	This interrupt is generated when the transmission size specified in the descriptor and transmission frame control information differ. At this time, transmission does not proceed. Modify the settings of the descriptor or the transmission frame information for retransmission. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
TX FIFO error interrupt	ETHTFIE	This interrupt is generated when information is further updated while the GMAC_TXID/GMAC_TXRESULT register is holding the maximum number of items of information (four). Take care, since the oldest of the retained information will have been overwritten when this error occurs. Reading the GMAC_TXID/GMAC_TXRESULT register repeatedly until the value of the GMAC_TXFIFO.TRBFR bit becomes 0 leads to clearing of the retained information and restoring normal operation.
MACDMA transmission error interrupt	ETHDTIE	This interrupt is generated when an error occurs while the transmission MAC DMA is operating. There are several error sources and HWFNC_MACDMA_TX_Errstat is used to obtain the error source. Modify the settings of the transmission descriptor for retransmission. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
Ethernet MACDMA transmission complete	ETHDMAIT	This interrupt is generated when DMA transfer from the buffer RAM to the transmission MAC FIFO is completed. At this time, DMA transfer has been completed but operations for communications by the MAC are not. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
Ethernet transmission complete interrupt	ETHIT	This interrupt occurs when operations for communications by the transmission MAC are completed. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.

Table 28.21 Interrupts related to Operations for Reception

Interrupt Name	Symbol	Conditions for Asserting and De-asserting Interrupts
Ethernet MACDMA reception complete	ETHDMAIR	This interrupt is generated when operations by the reception MACDMAC end normally. It remains active until the BUFID register becomes empty of information on reception. The interrupt source is de-asserted when the BUFID is read and becomes empty.
MACDMA reception error interrupt	ETHDRIE	This interrupt indicates that an error has occurred while the reception MACDMAC was operating. There is more than one source for this error, and the precise source is obtained by issuing HWFNC_MACDMA_RX_Errstat. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
Received frame normal interrupt	ETHRFI	This interrupt is generated when operations by the reception MACDMAC end normally and the received frame is normal. The interrupt source can be specified by referring to information on the received frame. It remains active until the BUFID register becomes empty of information on reception. The interrupt source is de-asserted when the BUFID is read and becomes empty.
Ethernet reception frame error	ETHRFE	This interrupt is generated when operations by the reception MACDMAC end normally and the received frame has an error. The interrupt source can be specified by referring to information on the received frame. It remains active until the BUFID register becomes empty of information on reception. The interrupt source is de-asserted when the BUFID is read and becomes empty.
RX FIFO overflow	ETHRFIV	This interrupt is generated when data are received while the buffer does not have enough space, so the Rx FIFO overflows. When this error occurs, received data may already have been discarded. Restore the system to the state where reception is possible by releasing the buffer, etc. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.

Table 28.22 Interrupts related to Other Operations

Interrupt Name	Symbol	Conditions for Asserting and De-asserting Interrupts
Ethernet MII management access complete interrupt	ETHMMAI	This interrupt is generated when reading from or writing to the MII management bus is completed. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
Ethernet pause packet transmission complete	ETHPPIT	This interrupt is generated when the transmission of a pause packet is completed. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
LPI start notification interrupt from MII	ETHLPIST	This interrupt is generated when a link partner notifies the Ethernet MAC of an LPI request. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.
LPI end notification interrupt from MII	ETHLPIEND	This interrupt is generated when a link partner de-asserts an LPI request. Since this interrupt is generated as a pulse, de-asserting the interrupt source is not required.

28.3.3 Ethernet Frame Transmission Function

This section describes transmission of Ethernet frames. For Ethernet MAC, Ethernet frames are transmitted in the following sequence:

1. Initial setup is performed. (Section 28.3.1.1)
2. A send buffer is obtained. (Section 28.3.3.1)
3. Transmission frame control information is created. (Section 28.3.3.2(1))
4. Ethernet frame data is created. (Section 28.3.3.2(2))
5. Transmit descriptors are created. (Section 28.3.3.3)
6. A DMA wake-up command is executed. (Section 28.3.3.4)
7. DMA transfer is performed according to transmit descriptors.
8. Ethernet transmission is started by MAC according to the transmission frame control information included in the transmit data.
9. A transmission completion interrupt occurs.
10. Post-transmission processing, including the status check, is performed. (Section 28.3.3.5)
11. The send buffer is released. (Optional)

The above steps are described in the following sections.

28.3.3.1 Obtaining a transmission buffer

Set hardware function call registers as shown below to obtain a transmission buffer.

Register	Setting Value
SYSC	5000h
R4	Size of the memory block to be secured (1 to 2048 bytes).
R5	0 (Unused)
R6	0 (Unused)
R7	0 (Unused)

The hardware function returns a value as follows:

Register	Setting Value
R0	0xb and R0[29] = 1: Success 10b: Invalid system call 11b: The buffer is insufficient
R1	Start address of the allocated memory block

28.3.3.2 Creating transmit data

Figure 28.13 shows the format of transmit data. The start address of this frame is specified by using transmit descriptors.
For Ethernet MAC, the size and other items for controlling transmit frames are specified by prefixing 64-bit transmission frame control information to the ordinary Ethernet frame data.

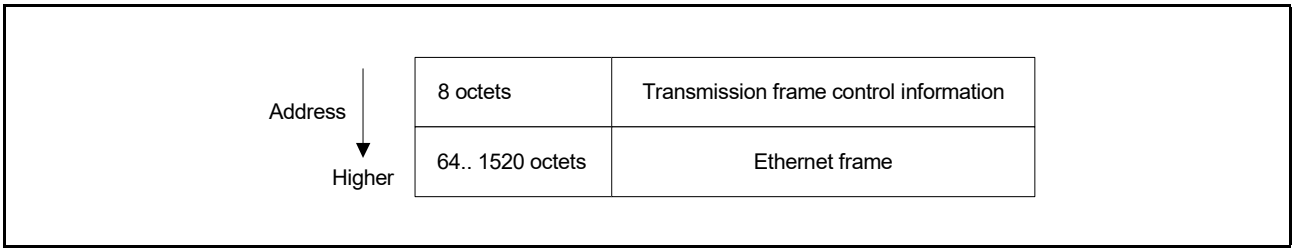


Figure 28.13 Format of Transmit Data

Note: Make sure that the transmission data is in this format.

(1) Transmission frame control information

The fields of the transmission frame control information are described below.

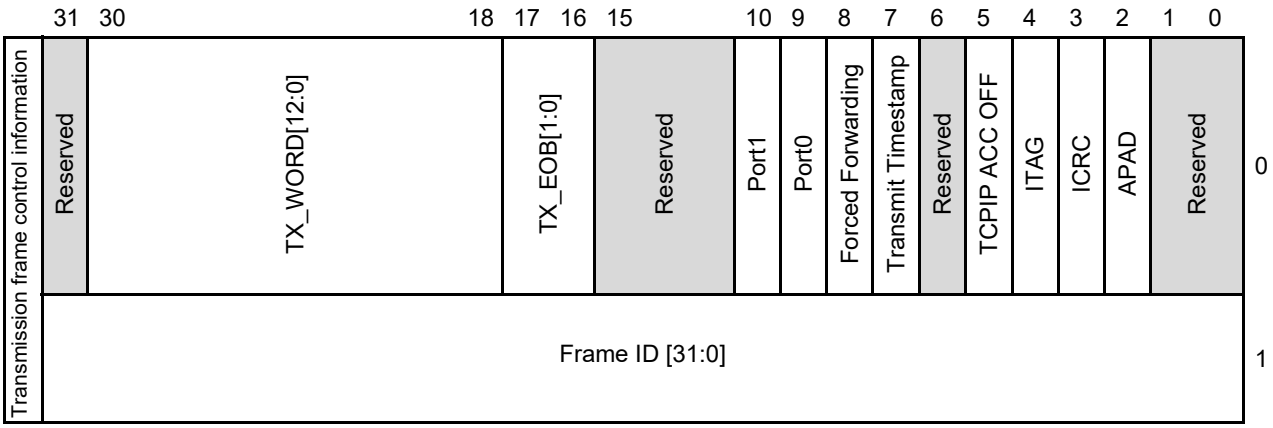


Figure 28.14 Transmission Frame Control Information

Note: Any value is allowed for the Reserved bit.

Item	Explanation
TX_WORD[12:0]	Specifies the number of words in the Ethernet frame to be transmitted (a word is 32 bits). The number of valid bytes in the last word is specified by using TX_EOB[1:0].
TX_EOB[1:0]	Indicates the extent of valid octets in the last 1 word of this frame. 00: 1 byte is valid. 01: 2 bytes are valid. 10: 3 bytes are valid. 11: 4 bytes are valid.
Port 1*1	The Forced Forwarding function of the Ethernet switch is permitted for Port 1.
Port 0*1	The Forced Forwarding function of the Ethernet switch is permitted for Port 0.
Forced Forwarding*1	The Forced Forwarding function of the Ethernet switch is enabled. If this function is enabled, frames are output from the specified port regardless of the filter settings of the switch.
Transmit Timestamp*1	The timestamp function for transmit frames is enabled when an Ethernet switch is used.
TCPIP ACC OFF*2	1: Disables the TCPIP accelerator. 0: Enables the TCPIP accelerator.
ITAG	Indicates that this frame includes a VLAN TAG.
ICRC	The CRC has already been attached to the frame. When the setting of this bit is 1, APAD is invalid.
APAD	APAD selects the automatic inclusion of padding if the frame length is less than 64 octets.
Frame ID[31:0]	Specifies a frame identifier.

Note 1. This item is valid only when insertion of the management tag is permitted for the Ethernet switch management TAG control register (ETHSWMTC). If no management tag is inserted, this field is invalid. For details on the Ethernet switch, see section 29, Ethernet Switch.

Note 2. Disable the TCPIP accelerator when a frame of either of the following types is to be transmitted.
- An IPv6 frame which does not include a UDP or TCP packet.
- An IEEE802.3 + IEEE802.2 (LLC) frame

If TX_LENGH[14:0] (15 bits) consists of TX_WORD[12:0] and TX_EOB[1:0], TX_LENGH[14:0] can be calculated from the Ethernet frame transmission size (in bytes) by using the following expression:
TCPIPACC Pad Size is 2 when the transmission TCPIP accelerator is enabled (GMAC_ACC.TTCPIPEN = 1), and 0 when disabled.

TX_LENGH [14:0] = (TX Frame Size – TCPIPACC Pad Size + 3) (bytes)

(2) Ethernet frame

The fields (data format) of Ethernet frames for transmission are listed in the table below.

Item	Explanation
Destination MAC Address	MAC address of the transmission destination
Source MAC Address	MAC address of the transmission source
Type/Length	Ethernet type or length
VLAN Tag	Tag protocol identifier: Used when VLAN tag is included.
VLAN Info	Tag control information: Used when VLAN tag is included.
Frame Payload	Payload

(a) When the transmission TCPIP accelerator is enabled

When the transmission TCPIP accelerator is enabled (GMAC_ACC.TTCPIPEN = 1), two bytes of padding must be inserted between the type/length field and the payload.

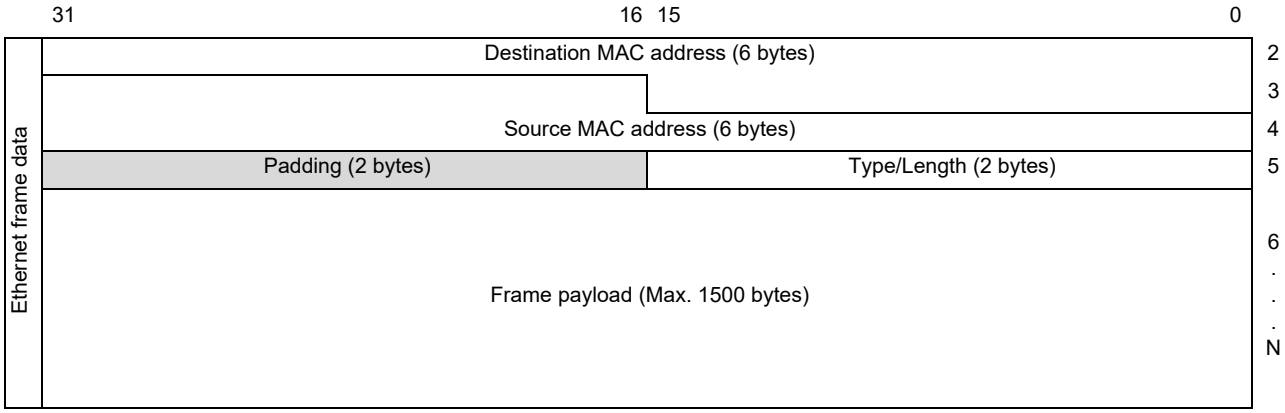


Figure 28.15 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag not Included)

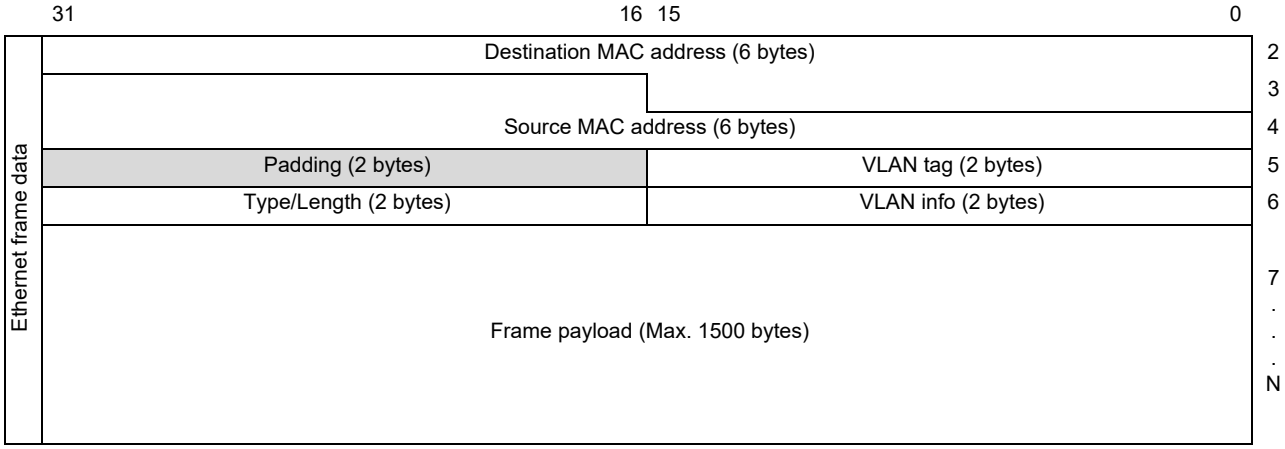


Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag Included)

Note: The padding field (2 bytes) can have any value. The padding (two bytes) is not included in the size to be specified for the Ethernet frame (TX_WORD[12:0] and TX_EOB[1:0]).

(b) When the transmission TCPIP accelerator is disabled

The following shows the Ethernet frame when the transmission TCPIP accelerator is disabled (GMAC_ACC.TTCPIPEN = 0).

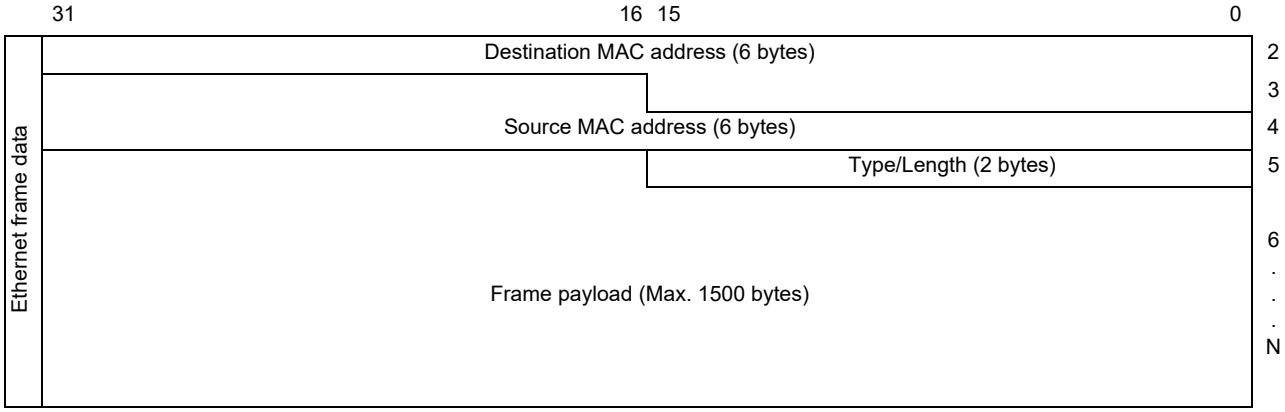


Figure 28.17 Format for Transmission Data (TCPIP Accelerator Disabled, VLAN Tag not Included)

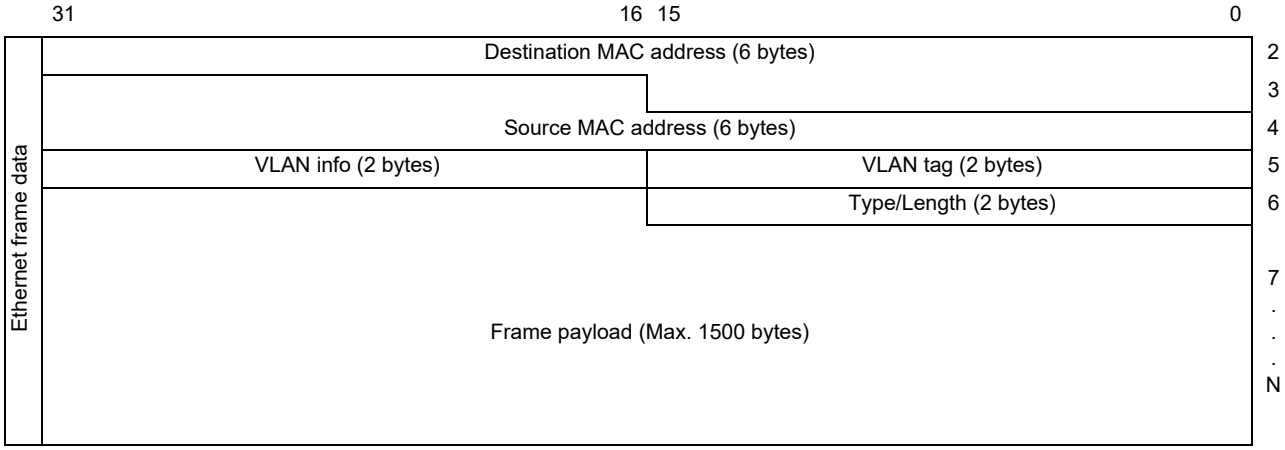


Figure 28.18 Format for Transmission Data (TCPIP Accelerator Disabled, VLAN Tag Included)

28.3.3.3 Creating transmit descriptors

A descriptor for use with the DMA controller for the TX MAC needs to be created. Activating the TX DMAC after creating a descriptor starts transmission. For details on the transmit descriptor, see Section 28.3.1.4 (3) DMA for the transmission MAC.

28.3.3.4 Starting transmission

When hardware function call registers are set as shown below, the transmission DMAC is started. DMA then starts transmission.

Register	Setting Value
SYSC	5100h
R4	Transmit descriptor address
R5	0 (Unused)
R6	0 (Unused)
R7	Set 0.

The hardware function returns a value as follows:

Register	Setting Value
R0	0: Success 1: Error (invalid call)
R1	Fixed to 0

28.3.3.5 Completing transmission

An Ethernet MACDMA transmission completed interrupt is generated on completion of the DMA transfer. An Ethernet transmission completed interrupt is generated on completion of transmission from the MAC.
If the transmission buffer that has already been secured is reused for the next transmission, you do not need to obtain another transmission buffer.

28.3.4 Ethernet Frame Reception Function

This section describes reception of Ethernet frames. For Ethernet MAC, Ethernet frames are received in the following sequence:

1. Initial setup is performed. (Section 28.3.4.1)
2. The reception MAC is enabled. (Section 28.3.4.2)
3. The reception DMAC is started. (Section 28.3.4.3)
4. Frames are received and a buffer is obtained. (Section 28.3.4.4)
5. A reception completion interrupt occurs.
6. Reception buffer information is obtained. (Section 28.3.4.5)
7. Frame status is checked. (Section 28.3.4.6(1))
8. Ethernet frame data is obtained. (Section 28.3.4.6(2))
9. The reception buffer is released.

28.3.4.1 Initial setup

MAC is reset and each register is set up in the same way as in initial setup for the Ethernet frame transmission function.

28.3.4.2 Enabling the reception MAC

Set the reception enable register (GMAC_RXMAC_ENA) to 1 to enable the reception MAC.

28.3.4.3 Starting the reception DMAC

Set hardware function call registers as shown below to start the receive DMA controller.

Register	Setting Value
SYSC	5101h
R4	0 (Unused)
R5	0 (Unused)
R6	0 (Unused)
R7	Set 0.

The hardware function returns a value as follows:

Register	Setting Value
R0	0: Success 1: Error (invalid call)
R1	Fixed to 0

28.3.4.4 Receiving frames and obtaining a buffer

When frame reception occurs, the reception buffer is automatically obtained by hardware.

28.3.4.5 Obtaining reception buffer information

After completion of reception is detected by a reception completion interrupt or another means, the reception buffer information register (BUFID) is read to obtain address and size of the buffer that stores receive data.
After the address information is obtained, the buffer that stores data is referenced to obtain the received frame information and Ethernet frame data. For the format of received data, see the format of received data in the next section.

28.3.4.6 Format of received data

In the reception of frames by the Ethernet MAC, 64 bits of received frame information will be appended after the frame data. This information indicates the state of reception: size of the Ethernet frame, errors, and so on.
Since the received frame information starts on a 64-bit boundary, the amount of padding following the Ethernet frame will vary with the frame size.

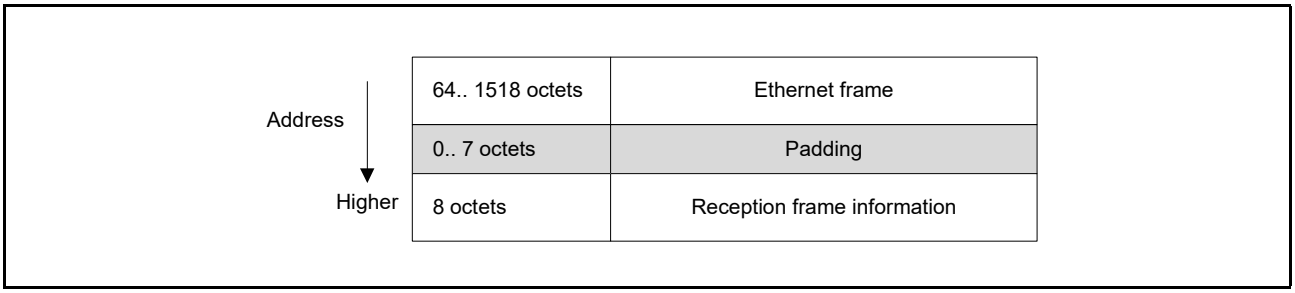


Figure 28.19 Format of Received Data

(1) Received frame information

The fields of the received frame information are described below.

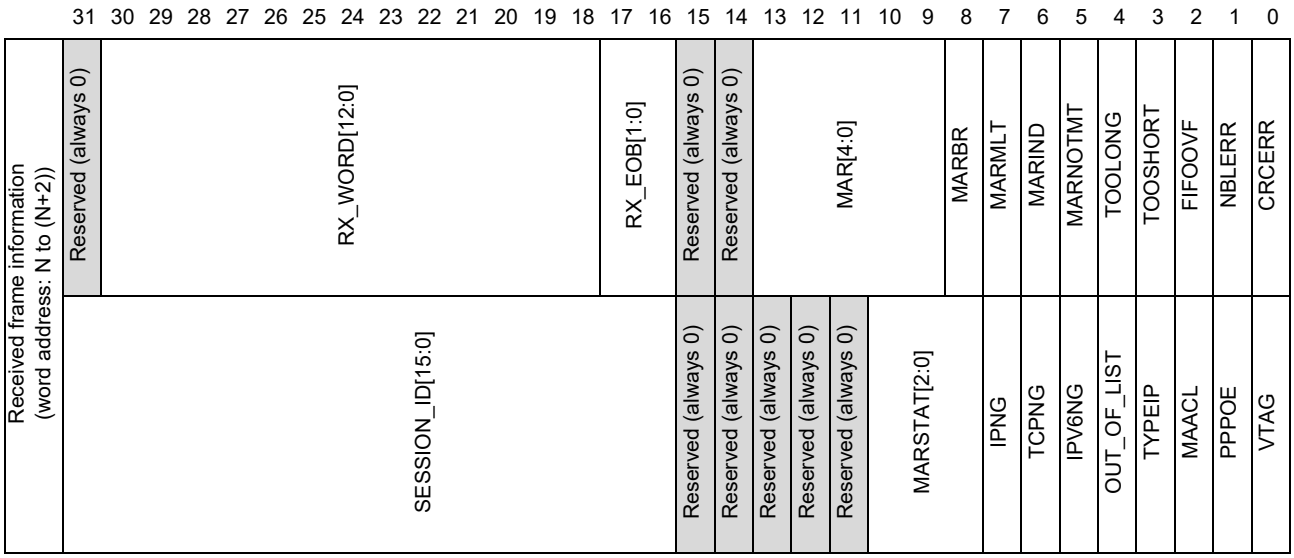


Figure 28.20 Received Frame Information

Item	Explanation
SESSION_ID[15:0]	If this field is set to ‘1’, it indicates Session ID of PPPoE Session Stage.
MARSTAT[2:0]	MARSTAT[2]: If this field is set to ‘1’, it indicates Broadcast Address. MARSTAT[1]: If this field is set to ‘1’, it indicates Multicast Address. MARSTAT[0]: If this field is set to ‘1’, it indicates Individual Address.
IPNG*2	If this field is set to ‘1’, it indicates that the checksum of the IPv4 header conflicts with the calculation result of the TCPIP accelerator.
TCPNG*2	If this field is set to ‘1’, it indicates that the checksum of the TCP or UDP header conflicts with the calculation result of the TCPIP accelerator.
IPV6NG*2	If this field is set to ‘1’, it indicates that the IPv6 extended header is one from among routing, Hop-by-Hop, or Destination Opt, and that the value of the header length field is incorrect.
OUT_OF_LIST*2	If this field is set to ‘1’, it indicates that a protocol number not listed below was detected in the IPv6 extended header. 06h: TCP header 11h: UDP header 00h: Hop-by-Hop 3Ch: Destination Opt 2Ch: Fragment 2Bh: Routing 3Bh: No next header 32h: ESP header 33h: AH header
TYPEIP*2	If this field is set to ‘1’, it indicates that an IP packet was received.
MAACL*2	If this field is set to ‘1’, it indicates that an 802.3 (LLC/SNAP) packet was received.
PPPOE*2	If this field is set to ‘1’, it indicates that a PPPoE packet was received.
VTAG*2	If this field is set to ‘1’, it indicates that the packet included a VLAN tag.
RX_WORD[12:0]	Number of Ethernet Frame words*1
RX_EOB[1:0]	Indicates the number of valid bytes in the last word of this frame.*1 00: 1 byte is valid. 01: 2 bytes are valid. 10: 3 bytes are valid. 11: 4 bytes are valid.
MAR[4:0]	MAR[4:1]: Unused (always 0) MAR[0]: Indicates that the Pause Packet destination address was received.

Item	Explanation
MARBR	If this field is set to ‘1’, it indicates that the receive frame is a Broadcast address.
MARMLT	If this field is set to ‘1’, it indicates that the receive frame is a Multicast address.
MARIND	If this field is set to ‘1’, it indicates that the receive frame is a packet from an address registered in the MAC address register.
MARNOTMT	If the receive frame is not an address for this station, this field is set to ‘1’.
TOOLONG	If this field is set to ‘1’, it indicates that the receive frame is longer than the maximum frame length (1518 octets).
TOOSHORT	If this field is set to ‘1’, it indicates that the receive frame is shorter than the minimum frame length (64 octets). This MAC never receives a packet in which TOOSHORT is ‘1’ because the TOOSHORT packet is automatically discarded.
FIFOOVF	If this field is set to ‘1’, it indicates that the FIFO buffer has overflowed during reception. When this occurs, the data of a received frame may be missing.
NBLERR	If this field is set to ‘1’, it indicates that the words in the receive frame have an error such as an encoding error.
CRCERR	If this field is set to ‘1’, it indicates that the receive frame has a CRC error.

Note 1. FCS (4 bytes) in the Ethernet frame and the padding (2 bytes) of the MAC header inserted by the reception TCPIP accelerator are also included in the number of received bytes.
Note 2. The values of these fields are ineffective if the TCPIP accelerator is disabled.

If RX_WORD[12:0] and RX_EOB[1:0] are combined into RX_LENGTH [14:0] (by using RX_WORD[12:0] as the upper bits and RX_EOB[1:0] as the lower bits), the number of bytes in the received frame can be calculated by using the following expression:

(Number of receive bytes in the Ethernet frame*1) = RX_LENGTH [14:0] - 3

Examples are as follows:

- When the size of receive data is 1 byte: RX_WORD = 1h, RX_EOB = 0h: 4 - 3 = 1 (byte)
- When the size of receive data is 8 bytes: RX_WORD = 2h, RX_EOB = 3h: 11 - 3 = 8 (bytes)
- When the size of receive data is 5 bytes: RX_WORD = 2h, RX_EOB = 0h: 8 - 3 = 5 (bytes)
- When the size of receive data is 9 bytes: RX_WORD = 3h, RX_EOB =0h: 12 - 3 = 9 (bytes)

Note 1. FCS (4 bytes) in the Ethernet frame and the padding (2 bytes) of the MAC header inserted by Ethernet MAC are also included in the number of receive bytes.

(2) Ethernet frame

The data format of received Ethernet frames is shown below.
For details on the Ethernet switch, see section 29, Ethernet Switch.

Item	Explanation
Destination MAC Address	MAC address of the transmission destination. If insertion of management tags is permitted by the Ethernet switch management TAG control register (ETHSWMTC), management TAG information is stored.
Source MAC Address	MAC address of the transmission source
Type/Length	Ethernet type or length
VLAN Tag	Tag protocol identifier: Used when a VLAN tag is included.
VLAN Info	Tag control information: Used when a VLAN tag is included.
Frame Payload	Payload
FCS	Frame check sequence: When the reception TCPIP accelerator is enabled and a received packet includes TCP/UDP, the FCS field is overwritten by the checksum value of TCP/UDP. This checksum value can be used for calculating the total checksum value of fragmented TCP/UDP packets.

(a) If insertion of management tags is permitted

If insertion of management tags is permitted by the Ethernet switch management TAG control register (ETHSWMTC), the Destination MAC Address [47:0] field is used as follows:

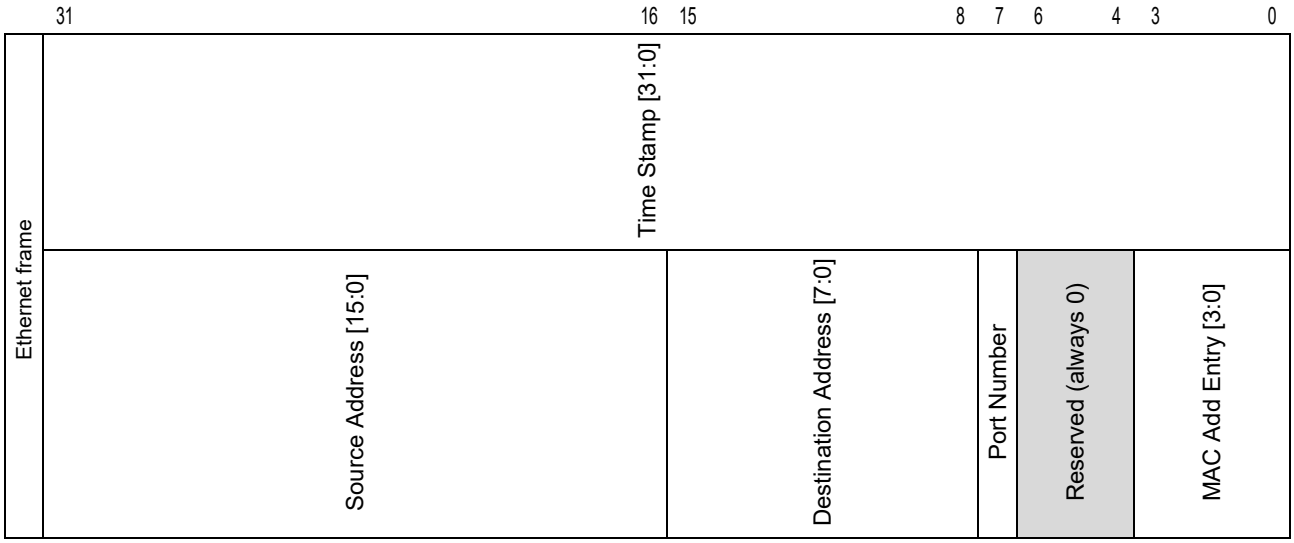


Figure 28.21 Destination MAC Address Field when Insertion of Management Tags is Permitted

Item	Explanation
Time Stamp [31:0]	Timestamp of the time at which the receive frame passed the port
MAC Add Entry [3:0]	Index number of the MAC address setting register (GMAC_ADRnA and GMAC_ADRnB) that matches the received frame Example: When the value is 5 The frame destination address corresponds to the setting of GMAC_ADR5A and GMAC_ADR5B.
Port Number	Port for which the receive timestamp was added
Destination MAC Address	MAC address of the transmission destination
Source MAC Address	MAC address of the transmission source

Note: When the AFILLTEREN bit in the GMAC_RXMODE register is 1, the value of the MAC Add Entry field is disabled and the destination MAC address is thus not stored.

(b) When the reception TCPIP accelerator is enabled and TCP/UDP packet data is not included

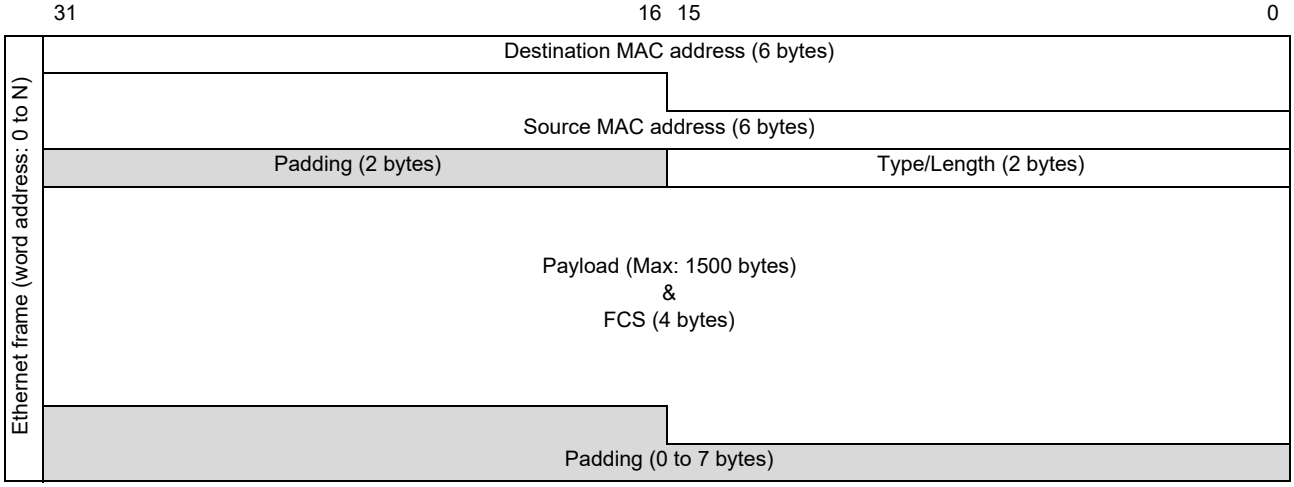


Figure 28.22 Received Ethernet Frame (TCPIPACC Enabled, VLAN Tag not Included, TCP/UDP not Included)

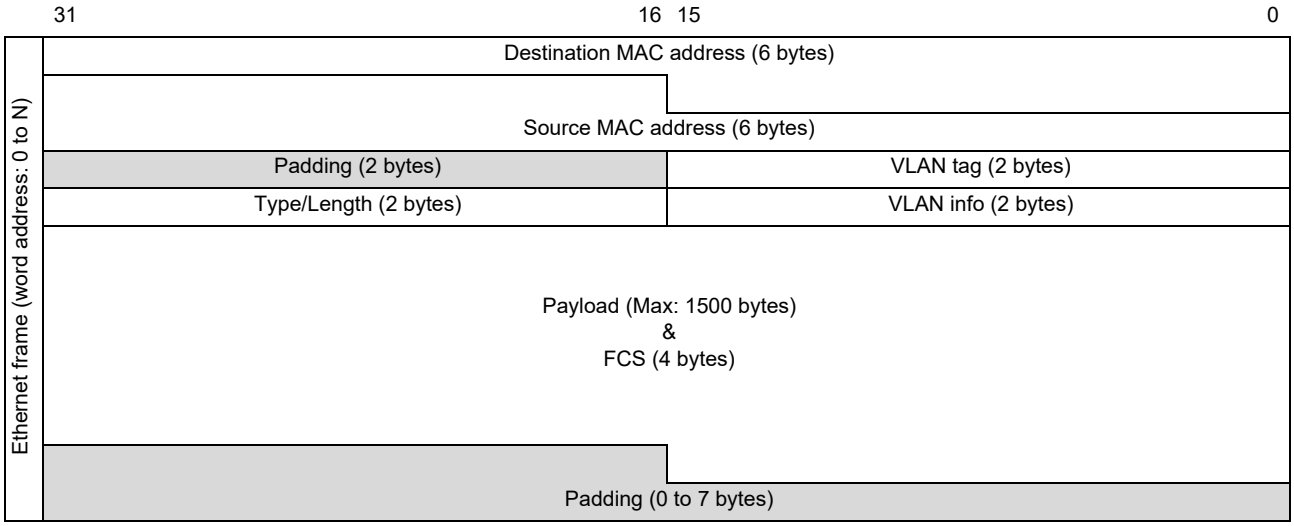


Figure 28.23 Received Ethernet Frame (TCPIPACC Enabled, VLAN Tag Included, TCP/UDP not Included)

(c) When the reception TCPIP accelerator is enabled and TCP/UDP packet data is included

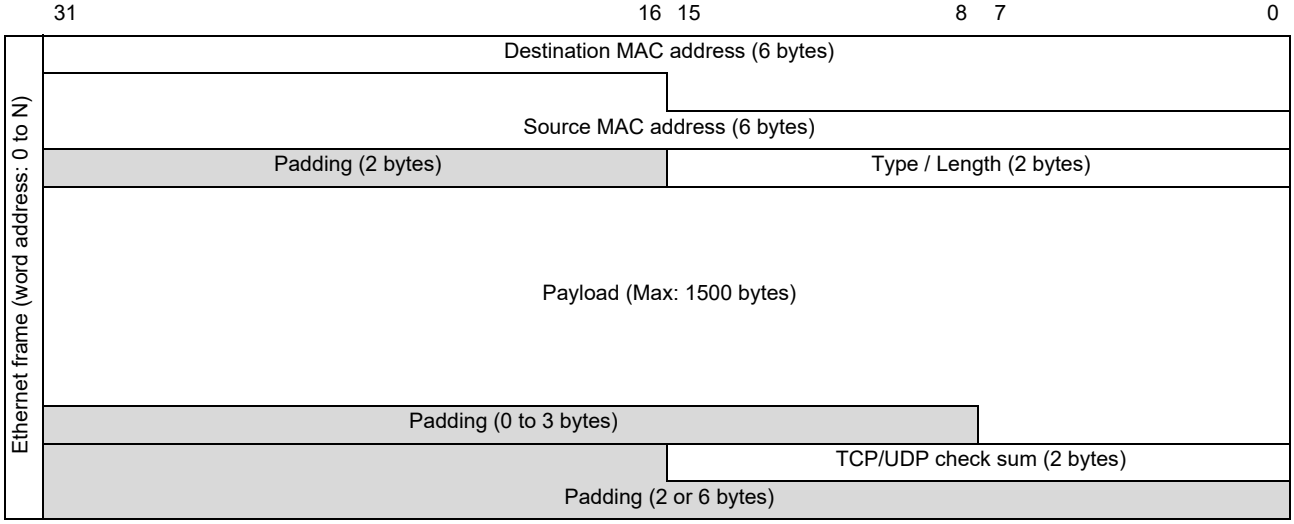


Figure 28.24 Received Ethernet Frame (TCPIPACC Enabled, VLAN Tag not Included, TCP/UDP Included)

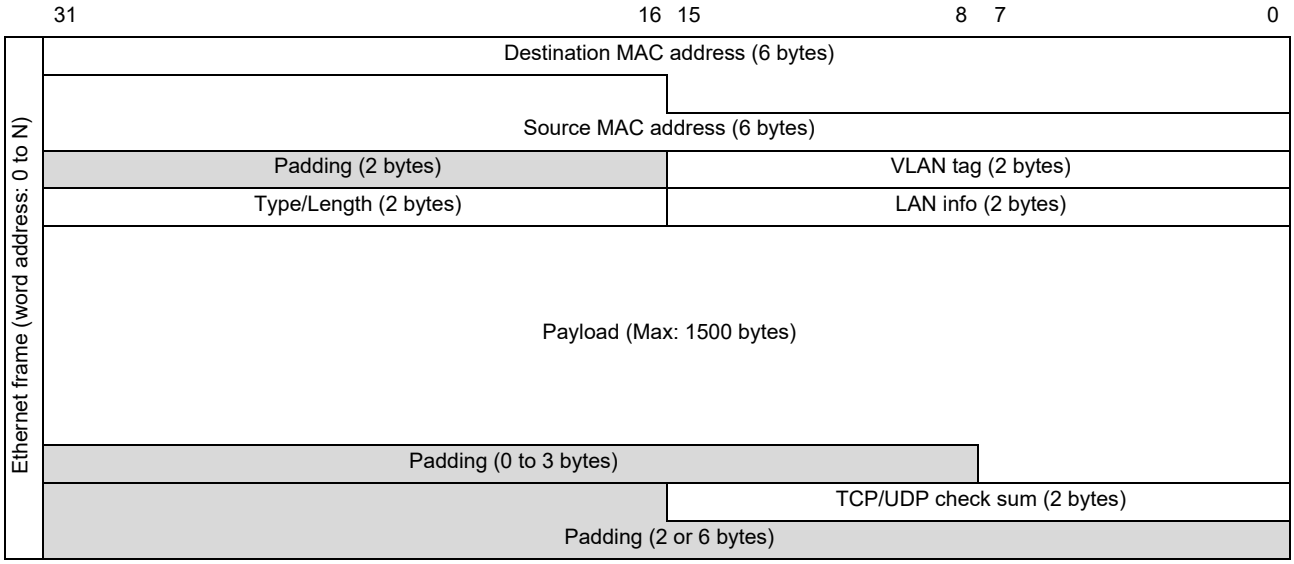


Figure 28.25 Received Ethernet Frame (TCPIPACC Enabled, VLAN Tag Included, TCP/UDP Included)

(d) When the reception TCPIP accelerator is disabled

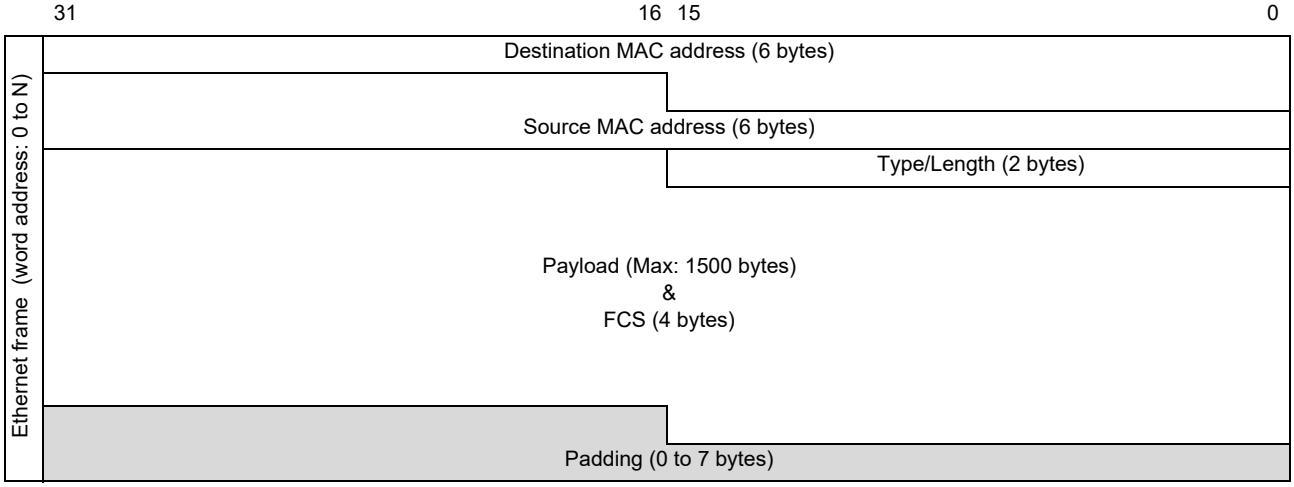


Figure 28.26 Received Ethernet Frame (TCPIPACC Disabled, VLAN Tag not Included)

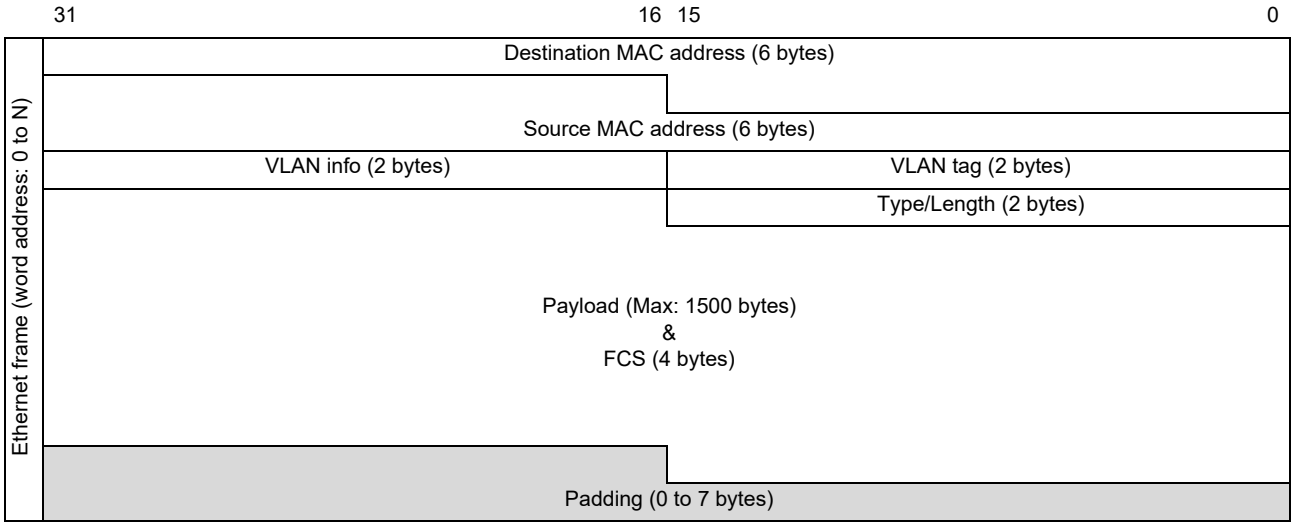


Figure 28.27 Received Ethernet Frame (TCPIPACC Disabled, VLAN Tag Included)

28.3.5 TCPIP Accelerator

With the TCPIP accelerator enabled, checksum calculations during transmission and reception can be executed by hardware. Frames for the following three protocols are checked by calculating the checksum.

- IPv4 header checksum
- TCP checksum
- UDP checksum

Usage of the TCPIP accelerator for transmission and reception is described below and on the next page.

28.3.5.1 Transmission with Use of the TCPIP Accelerator

Setting the TTCPIPEN bit in the GMAC_ACC register to 1 enables the TCPIP accelerator for transmission. When a packet for any from among IPv4, TCP/IP, or UDP/IP is transmitted in this state, hardware calculates the checksum and the checksum field for the given protocol is automatically overwritten and then transmitted. At this time, two bytes of padding for the TCPIP accelerator are required in the MAC header.
In addition, setting 1 in the TCPIP ACC OFF field of the transmission frame control information disables the transmission TCPIP accelerator for the packets.
For fragmented packets, hardware does not calculate the TCP and UDP checksums, so software should calculate the checksums.
When the TTCPIPEN bit in the GMAC_ACC register is 0, the transmission TCPIP accelerator is disabled.

Table 28.23 GMAC_ACC Register Settings and Transmission TCPIP Accelerator Operation

GMAC_ACC.TTCPIPEN	TCPIP ACC OFF Transmission Frame Control Information TCPIP ACC OFF	Calculation of Checksum (in Transmission)	Padding for TCPIPACC (in Transmission)
0	0	Disabled	Not required
0	1	Disabled	Not required
1	0	Enabled	Required
1	1	Disabled	Required

Note 1. If the result of calculating the UDP checksum of a packet for transmission is 0000h, write FFFFh to the checksum field.
Note 2. If the value of the header length field in an IPv4 header does not match the actual length of the header, transmission may not be completed and recovering normal operation may not be possible. Be sure to set the correct value.

28.3.5.2 Reception with Use of the TCPIP Accelerator

Setting the RTCPIPEN bit in the GMAC_ACC register enables the TCPIP accelerator for reception. When a packet for any from among IPv4, TCP/IP, or UDP/IP is received in this state, hardware calculates the checksum. If the result of calculation does not match the value of the packet's checksum field, error information is stored in the IPNG and TCPNG fields of the information on the received frame.

When TCPIPACC is enabled, two bytes of padding for the TCPIP accelerator are inserted in the MAC headers of received frames.

When the reception TCPIP accelerator is enabled and a received packet includes TCP/UDP, the FCS field is overwritten by the checksum value of TCP/UDP. This checksum value can be used for calculating the total checksum value of fragmented TCP/UDP packets. In the case of fragmented data, however, the pseudo-header does not include the checksum value, so software must be used to calculate the checksum value for the pseudo-header.

When any field from among IPNG, IPV6NG, or OUT_OF_LIST of the information on a received frame is 1, hardware does not calculate the TCP or UDP checksum for that frame.

Moreover, when the IPv6 extended header indicates any from among the fragment, ESP, and AH protocols, the TCP or UDP checksum is not calculated.

When the RTCPIPACC bit in the GMAC_ACC register is 1, the checksum is not calculated, but padding is inserted for the TCPIP accelerator.

When the RTCPIPEN bit in the GMAC_ACC register is 0, the reception TCPIP accelerator is disabled. In this case, padding for the accelerator is not assigned.

Table 28.24 GMAC_ACC Register Settings and Reception TCPIP Accelerator Operation

GMAC_ACC.RTCPIPEN	GAMC_ACC.RTCPIPACC	Calculation of Checksum (in Reception)	Padding for TCPIPACC (in Reception)	Overwriting of FCS Field with Calculated Checksum Value
0	0	Disabled	No	Not done
0	1	Disabled	No	Not done
1	0	Enabled	Yes	Done
1	1	Disabled	Yes	Not done

Note: If the checksum field of the UDP header of the received packet is 0000h, checksum comparison does not proceed. TCPNG becomes 0.

28.3.6 Protect Command Register

If a program runs out of control, the application might stop unexpectedly. To prevent such a problem, protect command registers are used to protect registers from write operations that might significantly affect the system. ETHERC has the following protect command registers:

- System protect command register (SPCMD)
- Ethernet system protect command register (ETSPCMD)

A write operation for a protected register can be performed only when the register is unlocked by setting the protection unlock enable bit of the SPCMD or ETSPCMD protect command register to ON (1).

To set a protect command register (to 1), only write operations performed in the following specific sequence are accepted. There is no special sequence for clearing the register (to 0) or reading it.

(1) Write 0000 00A5h to the protect command register as a specific value.
(2) Write 0000 00001h to the protect command register as an expected value.
(3) Write 0000 FFFEh to the protect command register as a reversal value.
(4) Write 0000 0001h to the protect command register as an expected value.

Note 1. In steps (2) and (3), no write operation is performed for the target register.
Note 2. After a write operation for the target register is completed, make sure that you clear the protect unlock enable bit (to 0) to enable protection.

The state transition is shown in the following diagram:

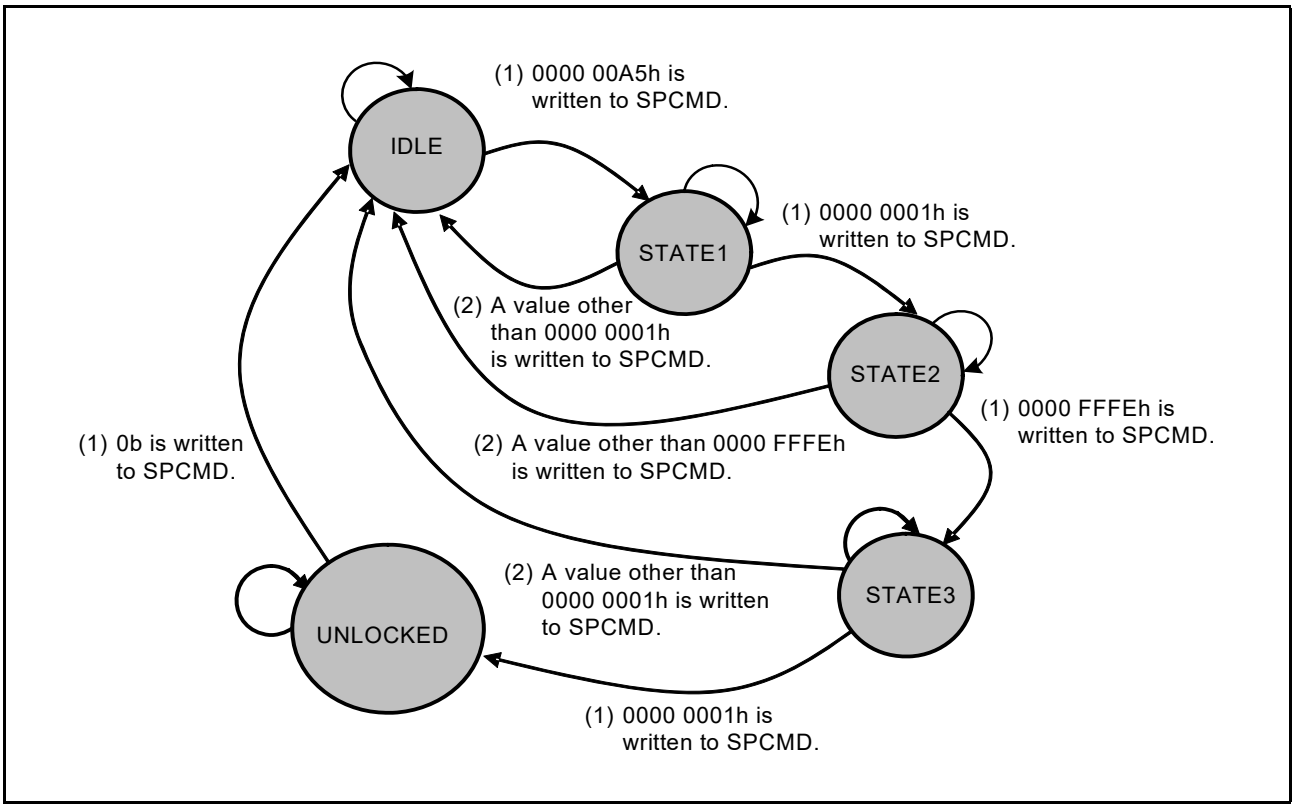


Figure 28.28 State Transition Diagram for a Protect Command Register (Example for the SPCMD Register)

28.4 Notes

The following sections describe points that must be noted.

28.4.1 Padding added to the MAC header in the transmit frame

In the gigabit Ethernet MAC, to enable the handling of data by the TCPIP accelerator, two bytes of padding are added to the 14-byte MAC headers to configure frames for transmission.
However, this padding is not actually sent. Therefore, note that it is not included in the data sizes of frames for transmission.
For details, see section 28.3.5.1, Transmission with Use of the TCPIP Accelerator.

28.4.2 Misjudgment of the Result of Checksum Calculation by Hardware in Reception

If the value of the checksum field in an IPv4 or TCP header included in the received packet is 0000h or FFFFh, the IPNG and TCPNG fields of the information on the received frame may be 1 even if the packet is actually normal (e.g., when the result of calculation by hardware is 0000h but the value of the checksum field in the header is FFFFh). Therefore, when both of the following conditions are satisfied, use software to check the checksum.

- IPNG or TCPNG is 1
- The value of the checksum field in the header is 0000h or FFFFh

28.4.3 Setting of the Module Stop Function

In the initial state, Ethernet-related functions are not activated. To use these functions, set the MSTPCRB.MSTPCRB16 to MSTPCRB.MSTPCRB19 bits to disable the module stop function. Note that after the module stop function is disabled, it must not be re-enabled. When the re-enabled module stop function is disabled again, correct operation cannot be guaranteed. It is possible to re-disable the module stop function after it is placed in the initial state (inactive state) by reset.

28.4.4 Misjudgment of the Result of Checksum Calculation in Reception

(1) Applicable to Ethernet II and IEEE802.3 + IEEE802.2 (LLC+SNAP) frames

If a frame which satisfies any of the following conditions has been received, the IPNG or TCPNG field of the information in the received frame may be 1 even if the packet is actually normal. Therefore, when this condition is satisfied, use software to check the checksum.

- The value of the checksum field in an IPv4 or TCP header is 0000h or FFFFh.
- The frame is not an IPv6 or FCS frame, its length is 60 or more bytes, the TCP or UDP payload is one byte, and the subsequent value is non-0.
- The calculated checksum value for a pseudo-header to be used in checksum calculation for IPv6, TCP, or UDP takes up 21 or more bits.

(2) Applicable to IEEE802.3 + IEEE802.2 (LLC) frames

If an IEEE802.3 + IEEE802.2 (LLC) frame with no SNAP extension is received, the value of the TYPEIP and IPNG fields may become 1. If this condition is met, use software to check whether the frame has a SNAP extension and handle it as a normal frame if it has no SNAP extension.

28.4.5 Incorrect Information on Received Frames when the Reception FIFO Overflows

If the reception FIFO buffer overflows while the reception TCPIP accelerator is enabled, information that is incorrect in the ways described below may be stored as information on the received frame.

- Error information on a previously received frame that caused the reception FIFO buffer to overflow is stored as information on a frame received as a normal frame.
- The received frame that caused the reception FIFO buffer to overflow is recognized as a normal frame and an incorrect value is stored as information on the received frame.

As a workaround for this, take action (1) or (2) below.

(1) Disable the inclusion of padding insertion in MAC headers by the reception TCP/IP accelerator. Specifically, clear bit 0 in the GMAC_ACC register.

(2) If the reception FIFO buffer overflows, discard all remaining frames in the reception FIFO buffer and in buffer RAM.
Specifically, take the following measures when the reception FIFO buffer overflows.
1. Stop the reception MAC.
2. Discard all remaining frames in the reception FIFO.
3. Discard all remaining frames in the buffer RAM.
4. Restart the reception MAC.
5. Discard frames in which the setting of the VALID bit of BUFID is 1 at least once. This measure is taken to discard residual frames by receiving a normal frame once, because, in the case of frames that cause overflows, FIFO Empty may be read from the register even while frames remain in the FIFO buffer.

Figure 28.29 to Figure 28.32 are example flowcharts to handle processing to accomplish the items in point (2).

- The following apply when the HW-RTOS is in use in a product with an R-IN Engine
  Figure 28.29: Example Task for Processing to Handle Overflows of the Reception FIFO Buffer
  Figure 28.30: Example Task to Handle Reception Processing

√ Prepare the overflow processing task so that it has higher priority than the reception processing task.
√ Make the setting to start task processing by the HWISR for overflow error interrupts.
√ Wait for the completion of the HWISR for reception interrupts before discarding the last frame.

- The following apply when the HW-RTOS may be unused with products that have no R-IN Engine or with products that have an R-IN Engine.
  Figure 28.31: Example of Processing for Reception FIFO Overflow Interrupts
  Figure 28.32: Example of Processing for Reception

√ Discard the last frame in reception processing. Discard valid data once if the return-from-overflow processing flag has been set.
√ Disable overflow interrupts during the period from reading of BUFID to checking of the return-from-overflow processing flag.

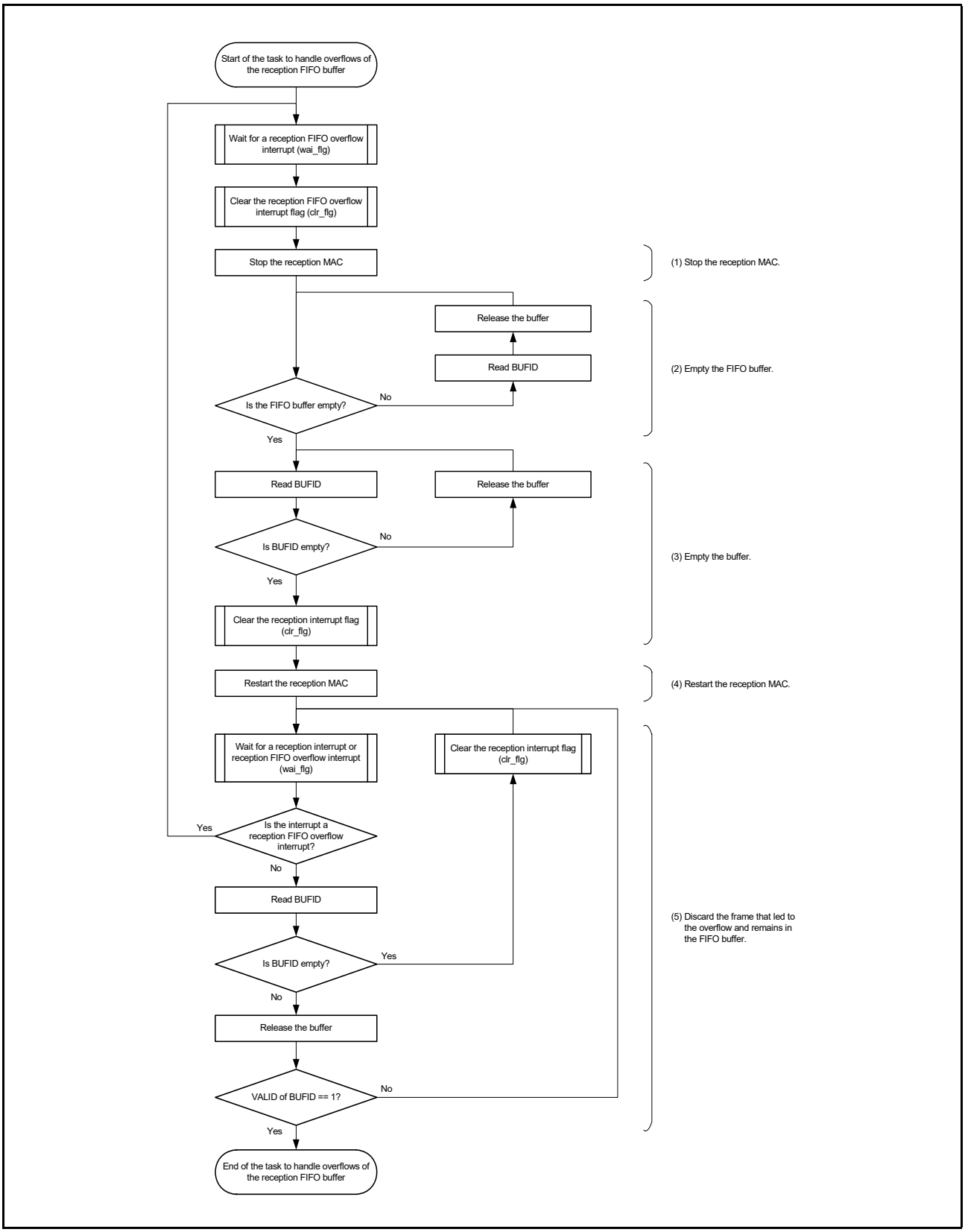


Figure 28.29 Example Task to Handle Overflows of the Reception FIFO Buffer (when the HW-RTOS is in Use)

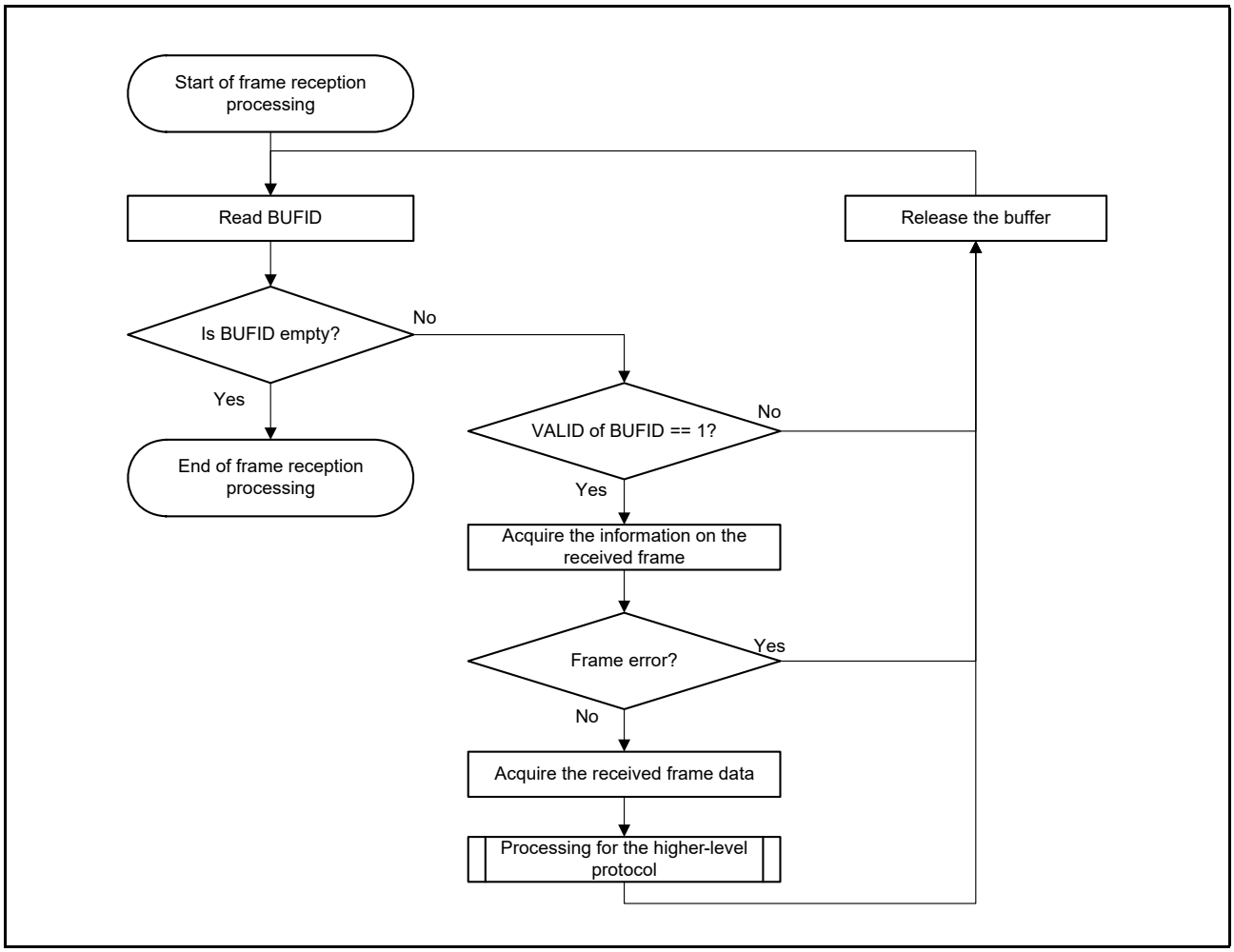
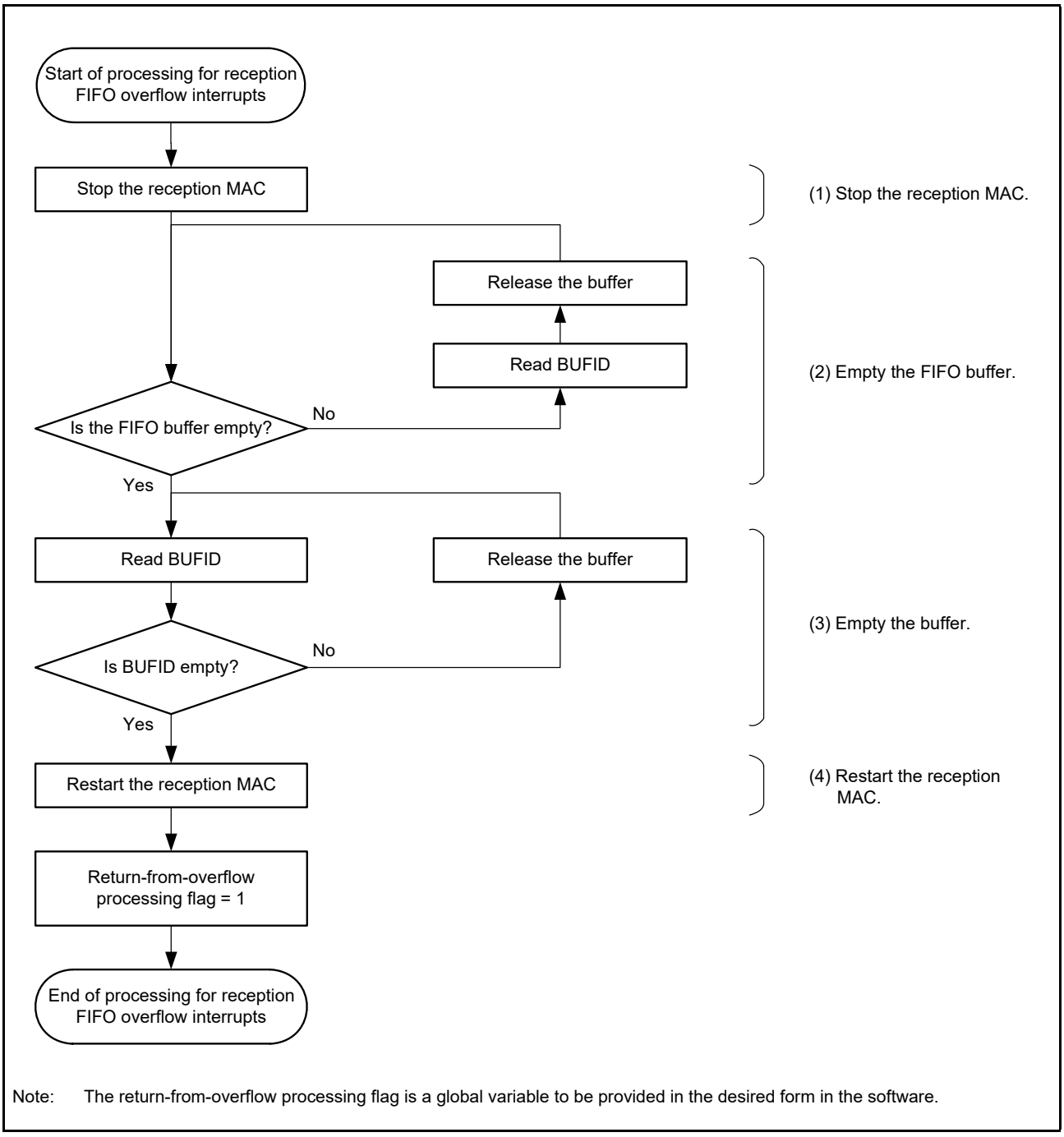
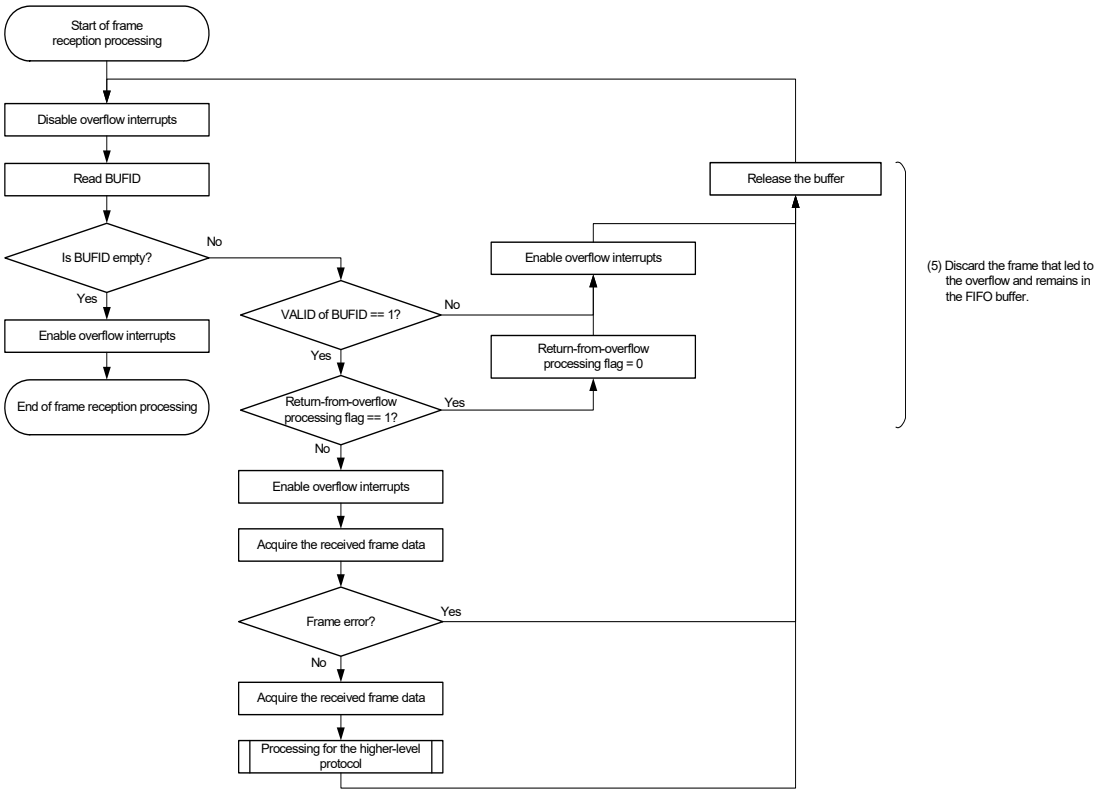


Figure 28.30 Example Task to Handle Reception Processing (when the HW-RTOS is in Use)



Note: The return-from-overflow processing flag is a global variable to be provided in the desired form in the software.

Figure 28.31 Example of Processing for Reception FIFO Overflow Interrupts (when the HW-RTOS is Not in Use)



Note: The return-from-overflow processing flag is a global variable to be provided in the desired form in the software.

Figure 28.32 Example of Processing for Reception (when the HW-RTOS is Not in Use)

28.4.6 Incorrect Information on Received Frames with Size, Inclusive of Padding, Exceeding 64 Bytes

If a frame which satisfies all conditions listed below is received while the reception TCPIP accelerator is enabled, the number of received words (RX_WORD[12:0]) indicated as information on the received frame may be greater or lower by one word (one word here meaning 4 bytes) than the actual number. In cases where it is lower by one word, the information may indicate an amount of data corresponding to the loss of the IP packet. However, this does not necessarily mean that the received IP packet was actually lost.

- The size of the frame including the frame check sequence (FSC) exceeds 64 bytes.
- The frame contains a TCP/IP or UDP/IP packet.
- The frame includes padding (a trailer) between the IP packet and the FCS.

As a workaround for this, take action (1) or (2) below.

(1) Disable the reception TCP/IP accelerator or turn its support for checksum calculation off.
Specifically, clear bit 0 or set bit 2 in the GMAC_ACC register.

(2) To prevent the loss of data, add one word to the number of received words in the case of IP packets and pass the packets to the higher-levels of the stack for processing. In the higher-levels, acquire the payload in the form of the IP packet based on the total length of the IP header and discard subsequent data. Figure 28.33 is an example flowchart of processing for reception.

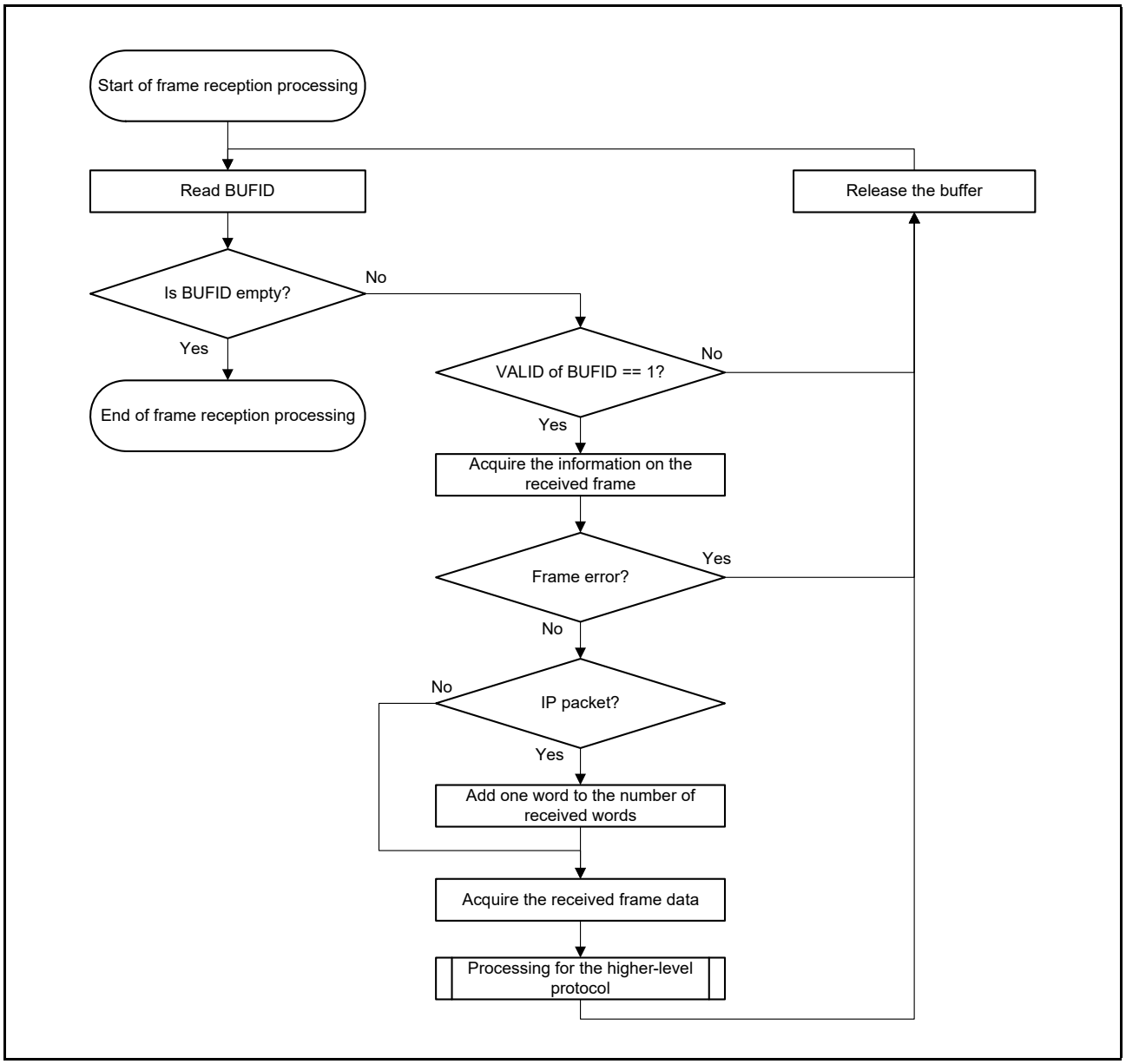


Figure 28.33 Example of Processing for Reception

28.4.7 Frame with Size Exceeding 1518 Bytes

This product does not support transfer of frames (jumbo frames) whose size exceeds 1518 bytes.

28.4.8 Use of Hardware Real-Time OS

For products incorporating an R-IN engine, when a hardware function call is executed while dispatching by the hardware real-time OS (HW-RTOS) is disabled, the call will not be executed successfully. To avoid this, be sure to execute hardware function calls while dispatching by the HW-RTOS is enabled. When the Cortex-R4 has control of the Ethernet MAC, however, it is not synchronized with the HW-RTOS, so the correct enabling and disabling of dispatching is not possible. Therefore, do not use the HW-RTOS while the Cortex-R4 is controlling the Ethernet MAC.

29. Ethernet Switch

This LSI has the Ethernet switch function.

29.1 Overview

With the Ethernet switch function, the LSI enables to build the network topology such as line and ring type without external switching hub.
Use of the Ethernet switch and mode setting are controlled by the related registers.
The specifications of the Ethernet switch are summarized in Table 29.1.

Table 29.1 Ethernet Switch Specifications

Item	Description
Function	• 2-port PHY interfaces • IEEE802.3 • 10BASE, 100BASE • Full and half duplex • Hardware switching, lookup, and filtering • QoS with frame prioritization • Priority control based on VLAN Priority (IEEE802.1Q), which enables priority reassignment • Classification and priority assignment based on IPv4 DiffServ Code Point Field, IPv6 Class of Service • Queue with four priority levels • Multicasting and broadcasting • VLAN frame • IEEE1588 timer module • Cut-through and hub features • Device level ring (DLR)

Figure 29.1 and Figure 29.2 are block diagrams of the Ethernet interface.
Gray modules and registers are described in section 28, Ethernet MAC (ETHERC), and section 30, EtherCAT Slave Controller (optional). See the related sections regarding the other registers and modules which are needed to operate the Ethernet switch.

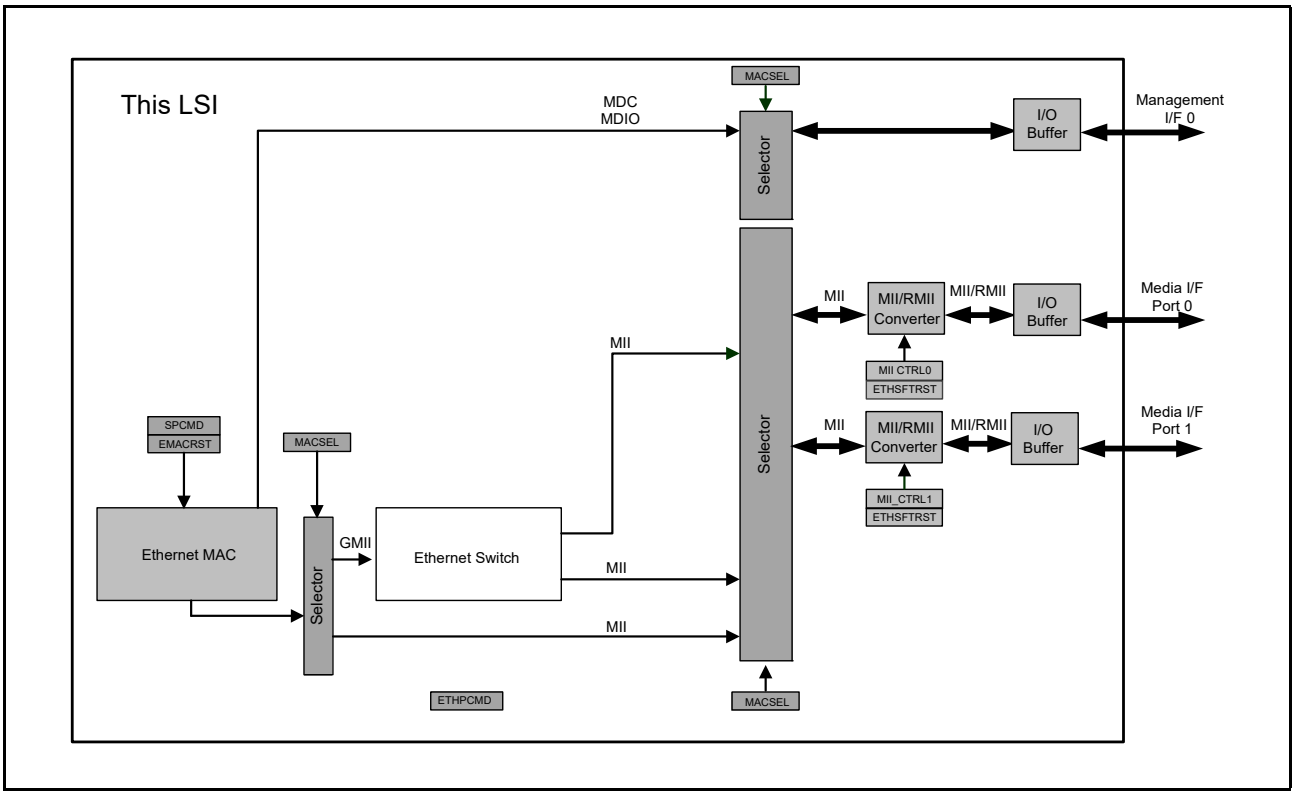


Figure 29.1 Block Diagram of the Ethernet Interface

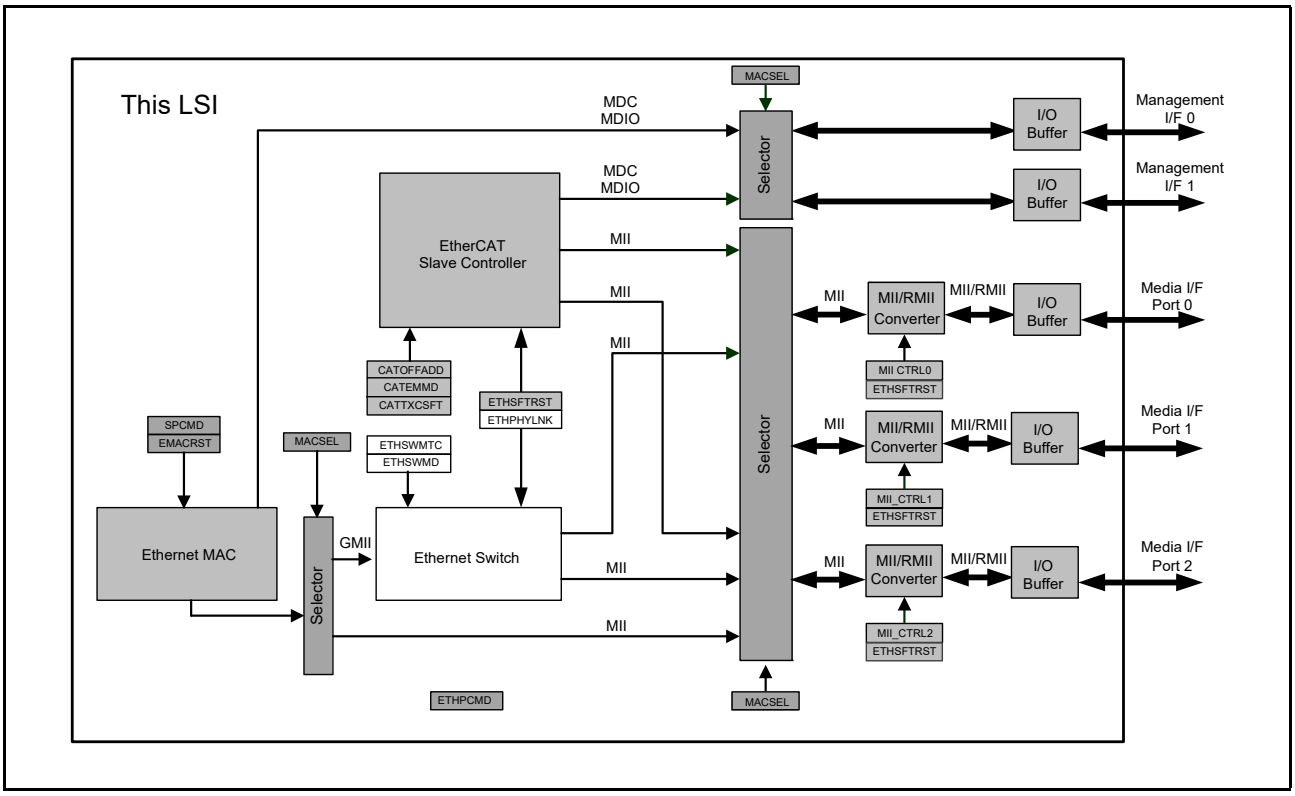


Figure 29.2 Block Diagram of the Ethernet Interface (for products incorporating an EtherCAT (optional))

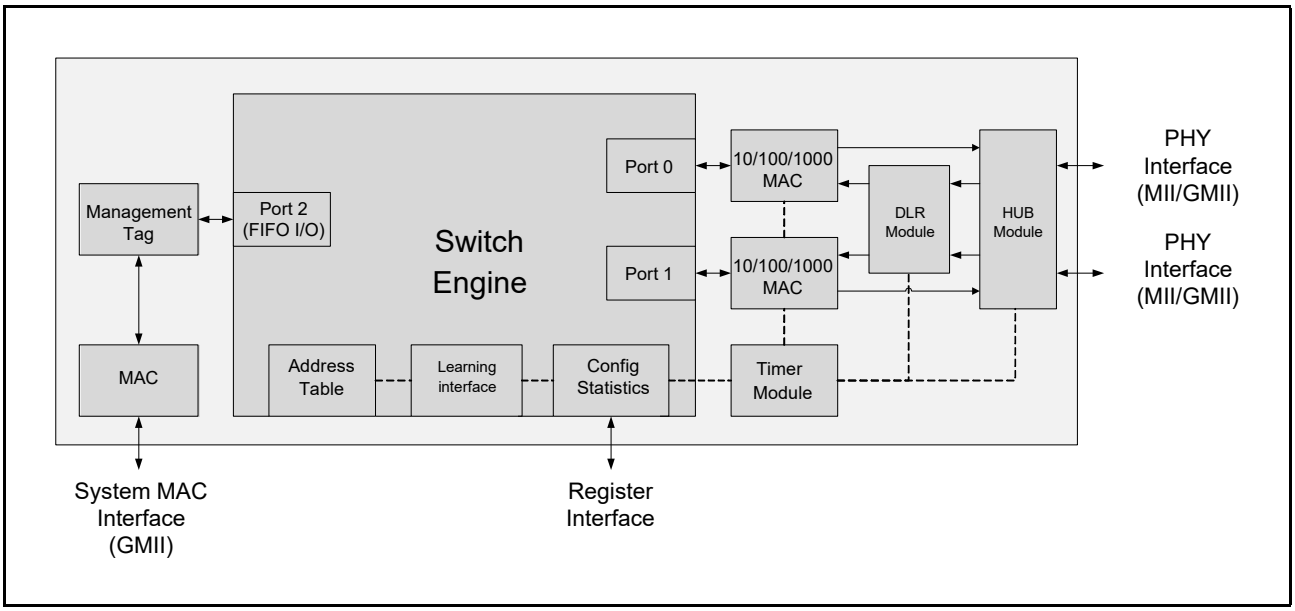


Figure 29.3 Ethernet Switch Overview

29.2 Register Description

29.2.1 Operating Mode Setting Registers

29.2.1.1 Ethernet PHY LINK Mode Register (ETHPHYLNK)

This register is used to specify the active level of the LINK signal of the Ethernet interface.

Note: This register is write-protected and can only be written after being protection-unlocked by using a special instruction sequence initiated through the Ethernet system protection command register (ETSPCMD) (For ETSPCMD, see section 28, Ethernet MAC (ETHERC)). For how to unlock protection, see section 28.2.1.3, Ethernet System Protect Command Register (ETSPCMD). No special instruction sequence is required for reading this register.

Address ETHERSW.ETHPHYLNK A00B F014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CATLINK1*1	CATLINK0*1	SWLINK1	SWLINK0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Note 1. These bits are only for products incorporating an EtherCAT (optional).

Bit	Symbol	Bit Name	Description	R/W
b0	SWLINK0	PHYLINK0 Pin Active Level Switching in Use with Ethernet Switch	Specify the active level of the PHYLINK0 signal using the Ethernet switch interface. 0: Active-High PHYLINK signal (value after reset). 1: Active-Low PHYLINK signal.	R/W
b1	SWLINK1	PHYLINK1 Pin Active Level Switching in Use with Ethernet Switch	Specify the active level of the PHYLINK1 signal using the Ethernet switch interface. 0: Active-High PHYLINK signal (value after reset). 1: Active-Low PHYLINK signal.	R/W
b2	CATLINK0*1	PHYLINK0 Pin Active Level Switching in Use with EtherCAT	Specify the active level of the PHYLINK0 signal using the EtherCAT interface. 0: Active-High PHYLINK signal. 1: Active-Low PHYLINK signal (value after reset).	R/W
b3	CATLINK1*1	LINK1 Pin Active Level Switching in Use with EtherCAT	Specify the active level of the PHYLINK1 signal using EtherCAT interface. 0: Active-High PHYLINK signal. 1: Active-Low PHYLINK signal (value after reset).	R/W
b31 to b4	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note 1. These bits are only for products incorporating an EtherCAT (optional). For other products, these bits are reserved. They are read as 0. The write value should always be 0.

29.2.1.2 Ethernet Switch Management TAG Control Register (ETHSWMTC)

This register is used to specify management tag information when Ethernet switching is used.

Note: This register is write-protected and can only be written after being protection-unlocked by using a special instruction sequence initiated by using the Ethernet system protection command register (ETSPCMD) (For ETSPCMD, see section 28, Ethernet MAC (ETHERC)). For how to unlock protection, see section 28.2.1.3, Ethernet System Protect Command Register (ETSPCMD). No special instruction sequence is required for reading this register.

Address(es): ETHERSW.ETHSWMTC A00B F110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SWTAGEN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SWTAGTYP[15:0]															
Value after reset:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SWTAGTYP [15:0]	Ethernet Type Specifying	Specify the Ethernet type (the field name defined in the Ethernet frame) to be set to a management tag. The initial value is E001h.	R/W
b30 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b31	SWTAGEN	Management Tag Insert Enable	Inserts management tags into frames 0: Disabled 1: Enabled	R/W

29.2.1.3 Ethernet Switch Operating Mode Setting Register (ETHSWMD)

This register is used to specify the operating mode when Ethernet switching is used.

Address(es): ETHERSW.ETHSWMD A00B F114h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	P1HDMODE	—	P0HDMODE	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b1	P0HDMODE	Port 0 Transfer Mode Setting	Specifies the transfer mode of port 0. 0: Full-duplex mode 1: Half-duplex mode	R/W
b2	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b3	P1HDMODE	Port 1 Transfer Mode Setting	Specifies the transfer mode of port 1. 0: Full-duplex mode 1: Half-duplex mode	R/W
b31 to b4	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.1.4 Ethernet Switch 10-Mbps/Half-Duplex Mode Setting Register (ETHSW10HDEN)

This register is used to mask inputs on the ETHn_RXDV pins (Read Data Valid) by using the Ethernet switching function.
In transfer of 10-Mbps/half-duplex data, the data are looped back from TX (transmission data) to RX (reception data) by using some Ethernet PHYs. If these PHYs are used with the Ethernet switching function of this device for loop-back operation between two ports, the data are repeatedly transferred between the ports without involving Ethernet.
If the Ethernet PHY you are using is applied to the case described above, make sure to set the bits of this register to 1 (to enable masking).

Address(es): A00F 201Ch
For accesses from the Cortex-M3:
Address 400F 201Ch (products incorporating an R-IN Engine)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SW10HDEN1	SW10HDEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SW10HDEN0	Mask RXDV for Ethernet Switch Port 0	0: Masking is disabled 1: Masking is enabled	R/W
b1	SW10HDEN1	Mask RXDV for Ethernet Switch Port 1	0: Masking is disabled 1: Masking is enabled	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

29.2.2 Switch Configuration Registers

29.2.2.1 Port Enable Register (PORT_ENA)

This register is used to enable or disable each port of the Ethernet switch. A disabled port does not transmit frames, but can still receive frames.

Address(es): ETHERSW.PORT_ENA A00C 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2ENA	P1ENA	P0ENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	P0ENA	Port 0 Enable Setting	Enables or disables port 0 0: Disabled 1: Enabled	R/W
b1	P1ENA	Port 1Enable Setting	Enables or disables port 1 0: Disabled 1: Enabled	R/W
b2	P2ENA	Internal Interface Enable Setting	Enables or disables the internal interface port (port 2) 0: Disabled 1: Enabled	R/W
b31 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.2 Unicast Default Mask Register (UCAST_DEFAULT_MASK)

This register is used to mask unicast frames of each port of the Ethernet switch. When the destination address is unicast and not found in the address table, the frame is transferred to the ports where the mask is enabled.

Address(es): ETHERSW.UCAST_DEFAULT_MASK A00C 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2UCASTDM	P1UCASTDM	P0UCASTDM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	P0UCASTDM	Port 0 Unicast Default Mask Setting	Selects the default unicast mask of port 0 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 0 even if the addresses of the frames are not found in the address table.	R/W
b1	P1UCASTDM	Port 1 Unicast Default Mask Setting	Selects the default unicast mask of port 1 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 1 even if the addresses of the frames are not found in the address table.	R/W
b2	P2UCASTDM	Internal Interface Unicast Default Mask Setting	Selects the default unicast mask of the internal interface (port 2). The internal interface does not generally need to receive unnecessary unicast traffic, so in most of cases, a mask setting is not required. Either of the following is required when a mask is not set: statically setting its own unicast address in the table of the switch or letting the interface learn dynamically based on the results of previous transfers. 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 2 even if the addresses of the frames are not found in the address table.	R/W
b31 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.3 Broadcast Default Mask Register (BCAST_DEFAULT_MASK)

This register is used to mask broadcast frames of each port of the Ethernet switch. When the destination address is broadcast, the frame is transferred to the ports given in this mask.

Address(es): ETHERSW.BCAST_DEFAULT_MASK A00C 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2BCA STDM	P1BCA STDM	P0BCA STDM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	P0BCASTDM	Port 0 Default Broadcast Mask Setting	Selects the default broadcast mask of port 0 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 0 if the destination addresses of the frames are broadcast addresses.	R/W
b1	P1BCASTDM	Port 1 Default Broadcast Mask Setting	Selects the default broadcast mask of port 1 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 1 if the destination addresses of the frames are broadcast addresses.	R/W
b2	P2BCASTDM	Internal Interface Default Broadcast Mask Setting	Selects the default broadcast mask of the internal interface port (port 2) 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 2 if the destination addresses of the frames are broadcast addresses.	R/W
b31 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.4 Multicast Default Mask Register (MCAST_DEFAULT_MASK)

This register is used to mask multicast frames of each ports of the Ethernet switch. When the destination address is multicast, the frame is transferred to the ports given in this mask.

Address(es): ETHERSW.MCAST_DEFAULT_MASK A00C 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2MCA STDM	P1MCA STDM	P0MCA STDM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	P0MCASTDM	Port 0 Default Multicast Mask Setting	Select the default multicast mask of port 0. 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 0 if the destination addresses of the frames are multicast addresses.	R/W
b1	P1MCASTDM	Port 1 Default Multicast Mask Setting	Select the default multicast mask of port 1. 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 1 if the destination addresses of the frames are multicast addresses.	R/W
b2	P2MCASTDM	Internal Interface Default Multicast Mask Setting	Select the default multicast mask of the internal interface port (port 2). 0: Invalid 1: Valid When masking is enabled, frames are transferred to port 2 if the destination addresses of the frames are multicast addresses.	R/W
b31 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.5 Input Learning Blocking Register (INPUT_LEARN_BLOCK)

This register is used to set address learning function and frame blocking function of each port of the Ethernet switch. When learning is disabled for a port (bit = 1), only bridge protocol data units (BPDU) are targeted for learning, all other frames are ignored. When blocking is enabled for a port (bit = 1), only bridge protocol data unit frames will be received, while other frames will be discarded on the port and not be transferred to other ports.

Address(es): ETHERSW.INPUT_LEARN_BLOCK A00C 001Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2LEARNDIS	P1LEARNDIS	P0LEARNDIS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2BLOCKEN	P1BLOCKEN	P0BLOCKEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	P0BLOCKEN	Port 0 Input Port Blocking Setting	Sets the blocking function of port 0 0: Invalid 1: Valid	R/W
b1	P1BLOCKEN	Port 1 Input Port Blocking Setting	Sets the blocking function of port 1 0: Invalid 1: Valid	R/W
b2	P2BLOCKEN	Internal Interface Input Port Blocking Setting	Sets the blocking function of the internal interface port (port 2) 0: Invalid 1: Valid	R/W
b15 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b16	P0LEARNDIS	Port 0 Address Learning Setting	Sets the address learning of port 0 0: Valid 1: Invalid	R/W
b17	P1LEARNDIS	Port 1 Address Learning Setting	Sets the address learning of port 1 0: Valid 1: Invalid	R/W
b18	P2LEARNDIS	Internal Interface Address Learning Setting	Sets the address learning of the internal interface port (port 2) 0: Valid 1: Invalid	R/W
b31 to b19	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.6 Management Configuration Register (MGMT_CONFIG)

This register is used to configure the bridge management port of the Ethernet switch and to enable the management port that receives bridge protocol frames. It is necessary to set the internal interface port (port 2) in the management port.

Address(es): ETHERSW.MGMT_CONFIG A00C 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	P1PORTMASK	P0PORTMASK
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRIORITY			—	—	—	—	—	DISCARD	ENABLE	MSGTRANS	—	—	—	PORT	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PORT	Management Port Setting	Set the port that should act as a management port. These bits must always be set to 10b since it is necessary to set the internal interface port (port 2) in the management port.	R/W
b4 to b2	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b5	MSGTRANS	Message Transfer Status	This bit is set to 1 when a message is transmitted from the management port to any output port. Write 0 to this bit for a reset.	R/W
b6	ENABLE	Setting of Transfer to Management Port	Sets transfer of the BPDU frame to the management port. 0: Bridge protocol frames are forwarded as any other frame, or discarded if the DISCARD bit is set to 1. 1: All bridge protocol frames are forwarded exclusively	R/W
b7	DISCARD	BPDU Frame Discard Setting	Sets BPDU Frame Discard BPDU frames are always discarded when setting this bit to 1. Always set this bit to 0 if the ENABLE bit is set to 1. 0: Disabled 1: Enabled	R/W
b12 to b8	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b15 to b13	PRIORITY	Management Frame Priority Setting	Set priority of the management frames to be transmitted. Used to transmit a management frame faster than a normal frame. The priority in the output queue can be set to a higher priority level.	R/W
b16	P0PORTMASK*1	Port 0 Management Frame Transfer Mask Setting	Sets mask for transferring management frames from the management port to port 0. Setting this bit to 1 forcibly transfers only BPDU frames to port 0. Any other frames have no effect. 0: Invalid 1: Valid	R/W
b17	P1PORTMASK*1	Port 1 Management Frame Transfer Mask Setting	Sets mask for transferring of management frames from the management port to port 1. Setting this bit to 1 forcibly transfers only BPDU frames to port 0. Any other frames have no effect. 0: Invalid 1: Valid	R/W
b31 to b18	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note 1. The herein specified PORTMASK takes precedence over the forced forwarding per each frame by management tag when a BPDU frame is forwarded. Hence it should be set to 0 when tag controlled forced forwarding is used.

29.2.2.7 Mode Configuration Register (MODE_CONFIG)

This register is used to reset the statistics counter in the Ethernet switch.

Address(es): ETHERSW.MODE_CONFIG A00C 0024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	STATS RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b30 to b0	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b31	STATSRESET	Statistics Counter Reset	Resets the statistics counter in the Ethernet switch (A00C 0300h to A00C 0324h). Writing 1 to this bit resets the counter. Afterwards, this bit is cleared to 0.	R/W

29.2.2.8 VLAN Tag ID Register (VLAN_TAG_ID)

This register is used to set a VLAN tag ID to identify a VLAN tagged frame. In valid IEEE802.1Q, a VLAN tag ID is defined as 8100h. The value should not be changed since the value after reset of the register is 8100h.

Address(es): ETHERSW.VLAN_TAG_ID A00C 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VLANTAGID															
Value after reset:	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	VLANTAGID	ID Identification Setting	Identify a VLAN tag ID. In valid IEEE802.1Q, VLAN tag ID is defined as 8100h.The value should not be changed from the value after reset.	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.9 Output Queue Management Status Register (OQMGR_STATUS)

This register is used to indicate the status of output queue of the Ethernet switch.
Writing a given value to the register clears latched bits (bit 1 and bit 3).

Address(es): ETHERSW.OQMGR_STATUS A00C 0080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CELLAVILABLE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DEQUEGRANT	—	—	MEMFULL_LT	MEMFULL	NOCELL	BUSYINIT
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	BUSYINIT	Memory Initialization Status	When set to 1, the memory controller in the Ethernet switch indicates the initialization status. This bit is set to 0 when it is asserted after a reset and the initialization of the memory controller is complete. The switch must not be enabled before the initialization of the memory controller has been completed.	R/W
b1	NOCELL	Memory Cell Remaining Status	This bit is set to 1 when no cell remains in the output queue. This bit is always set to 1 after a reset. When initialization is complete, (the BUSYINIT bit is 0), write a given value to the register to clear this bit. When this bit is set to 1 during operation, this is a fatal error. As long as the hardware is in normal operation, this bit is never set to 1. If happens, for any reasons, reset this bit and set a larger value to the output queue minimum memory register (QMGR_MINCELLS).	R/W
b2	MEMFULL	Memory Full Status	Indicates whether or not the memory is currently full. This bit is set to 1 when the number of available memory is less than the minimum memory size specified in QMGR_MINCELLS. This is not an error, unlike the NOCELL, the memory controller operates normally. To avoid an overflow of the memory, the switch stops the operation of the input port.	R/W
b3	MEMFULL_LT	MEMFULL Result	Indicates the latched value of the MEMFULL result. Even when MEMFULL is cleared 0 from 1, the MEMFULL_LT bit retains 1. The bit is cleared when any value is written to the register.	R/W
b5, b4	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b6	DEQUEGRANT	De-queue Status Indication	Indicates whether or not any input is de-queued. This bit is set to 1 generally, but set to 0 once the memory is full.	R/W
b15 to b7	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b31 to b16	CELLAVILABLE	Memory Cell Number Indication	Indicates the number of currently available cells in real-time.	R/W

29.2.2.10 Output Queue Minimum Memory Register (QMGR_MINCELLS)

This register is used to set the minimum ensure value of memory for output queue for the Ethernet switch and must be set with a margin to avoid memory underflow.

Address(es): ETHERSW.QMGR_MINCELLS A00C 0084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	MINCELLS				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	MINCELLS	Available Cell Threshold Setting	Set the threshold of available cells of the output queue memory. The switch stops input port operation and discards received frames when available cells becomes less than this value. The value should be chosen to give enough margin of at least 1 full-sized frame. A memory underflow due to a too low threshold is a fatal error and requires a reset. 1 cell consists of 256 bytes and the value after reset is 9 (2.3 Kbytes).	R/W
b31 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.11 Output Queue Minimum Memory Statistics Register (QMGR_ST_MINCELLS)

This register is used to indicate the minimum number of free cells in the memory for output queue of the Ethernet switch.

Address(es): ETHERSW.QMGR_ST_MINCELLS A00C 0088h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	STMINCELLS				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	STMINCELLS	Minimum Free Cell Indication	Indicate the lowest number of free cells reached in the memory during operation after this register is cleared. Writing a given value resets the register value to 0.	R/W
b31 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.12 Output Queue Congestion Status Register (QMGR_CGS_STAT)

This register is used to indicate the congestion status (concentration of access, etc.) of each port of the Ethernet switch.

Address(es): ETHERSW.QMGR_CGS_STAT A00C 008Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2CGS	P1CGS	P0CGS
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	P0CGS	Port 0 Congestion Status Indication	Congestion status of the queues of port 0 0: Vacancy 1: Congested	R
b1	P1CGS	Port 1 Congestion Status Indication	Congestion status of the queues of port 1 0: Vacancy 1: Congested	R
b2	P2CGS	Internal Interface Port Congestion Status Indication	Congestion status of the queues of the internal interface port (port 2) 0: Vacancy 1: Congested	R
b31 to b3	—	Reserved	When read, an undefined value is read.	R

29.2.2.13 Internal Queue Interface Status Register (QMGR_IFACE_STAT)

This register is used to indicate the RX and TX FIFO status of each port of the Ethernet switch and to indicate the result of internal interface handshaking.

Address(es): ETHERSW.QMGR_IFACE_STAT A00C 0090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2RXFIFOAV	P1RXFIFOAV	P0RXFIFOAV
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	P2TXFIFOST	P1TXFIFOST	P0TXFIFOST
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1	1

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	P0TXFIFOST	Port 0 TX FIFO Status	Indicates whether or not TX FIFO of port 0 is READY 0: Not READY 1: READY	R
b1	P1TXFIFOST	Port 1 TX FIFO Status	Indicates whether or not TX FIFO of port 1 is READY 0: Not READY 1: READY	R
b2	P2TXFIFOST	Internal Interface TX FIFOStatus	Indicates whether or not TX FIFO of the internal interface port (port 2) is READY 0: Not READY 1: READY	R
b15 to b3	—	Reserved	When read, an undefined value is read.	R
b16	P0RXFIFOAV	Port 0 RX FIFO Status	Indicates whether RX FIFO data of port 0 is available 0: Not available 1: Available	R
b17	P1RXFIFOAV	Port 1RX FIFO Status	Indicates whether RX FIFO data of port 1 is available 0: Not available 1: Available	R
b18	P2RXFIFOAV	Internal Interface RX FIFO Status	Indicates whether RX FIFO data of the internal interface port (port 2) is available 0: Not available 1: Available	R
b31 to b19	—	Reserved	When read, an undefined value is read.	R

29.2.2.14 Queue Weight Register (QMGR_WEIGHTS)

This register is used to define weights (priority levels) for the corresponding queues for all ports of the Ethernet switch. Each port has 4 queues and a weight can be set for each queue. The weight settings are common to all ports.
Setting the weights of all queues to 0 implements a strict priority scheme. In this case, queue 3 is the highest priority queue.
If you do not wish to use strict priority, set respective weights of 1, 2, 4, and 8 to queues 0, 1, 2, and 3.

Address(es): ETHERSW.QMGR_WEIGHTS A00C 0094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	QUEUE3					—	—	—	QUEUE2				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	QUEUE1					—	—	—	QUEUE0				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	QUEUE0	Queue0 Weight Setting	Set the weight of queue 0. The valid range is from 0 to 12 (although 5 bits are writable per queue).	R/W
b7 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b12 to b8	QUEUE1	Queue1 Weight Setting	Set the weight of queue 1. The valid range is from 0 to 12 (although 5 bits are writable per queue).	R/W
b15 to b13	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b20 to b16	QUEUE2	Queue2 Weight Setting	Set the weight of queue 2. The valid range is from 0 to 12 (although 5 bits are writable per queue).	R/W
b23 to b21	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b28 to b24	QUEUE3	Queue3 Weight Setting	Set the weight of queue 3. The valid range is from 0 to 12 (although 5 bits are writable per queue).	R/W
b31 to b29	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.2.15 VLAN Priority Register n (VLAN_PRIORITYn) (n = 0 to 2)

These registers are used to set priority of the VLAN tag of the input frames.
The Ethernet switch has an 8-entry programmable priority lookup table for each port. The priority included in the 3 high-order bits of the of the first octet of the VLAN tag is used as an index of the lookup table and can be remapped.
Note: The range of values that can be set is 0 to 3 respectively for each priority. Always write 0 to the third bit.

Address(es): ETHERSW.VLAN_PRIORITY0 A00C 0100h, ETHERSW.VLAN_PRIORITY1 A00C 0104h, ETHERSW.VLAN_PRIORITY2 A00C 0108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	PRIORITY7			PRIORITY6			PRIORITY5	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRIORITY5	PRIORITY4			PRIORITY3			PRIORITY2			PRIORITY1			PRIORITY0		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	PRIORITY0	Priority 0 Setting	Priority for priority 0 of VLAN tag of input frames	R/W
b5 to b3	PRIORITY1	Priority 1 Setting	Priority for priority 1 of VLAN tag of input frames	R/W
b8 to b6	PRIORITY2	Priority 2 Setting	Priority for priority 2 of VLAN tag of input frames	R/W
b11 to b9	PRIORITY3	Priority 3 Setting	Priority for priority 3 of VLAN tag of input frames	R/W
b14 to b12	PRIORITY4	Priority 4 Setting	Priority for priority 4 of VLAN tag of input frames	R/W
b17 to b15	PRIORITY5	Priority 5 Setting	Priority for priority 5 of VLAN tag of input frames	R/W
b20 to b18	PRIORITY6	Priority 6 Setting	Priority for priority 6 of VLAN tag of input frames	R/W
b23 to b21	PRIORITY7	Priority 7 Setting	Priority for priority 7 of VLAN tag of input frames	R/W
b31 to b24	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0 to 2
n = 0: port 0, n = 1: port 1, n = 2: internal interface port (port 2)

29.2.2.16 IP Priority Register n (IP_PRIORITYn) (n = 0 to 2)

Each port of the Ethernet switch has class of services (COS) tables for IPv4 and IPv6. In the COS table entries for IPv4, the frame's 6-bit DiffServ field is provided as an index to the lookup table and a 2-bit priority can be set. In the COS table entries for IPv6, the frame's 8-bit COS field is provided as an index to the lookup table and a 2-bit priority can be set. This register is used to make and refer to COS table settings by writing to the COS table or making the settings for reference to a priority level.

Address(es): ETHERSW.IP_PRIORITY0 A00C 0140h, ETHERSW.IP_PRIORITY1 A00C 0144h, ETHERSW.IP_PRIORITY2 A00C 0148h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	READ	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PRIORITY		IPV6SELECT	ADDRESS							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ADDRESS	COS Table Address Specifying	Specify an address for the index of the COS table. The IPv4 priority table is 6 bits (64 entries) and the IPv6 table is 8 bits (256 entries).	R/W
b8	IPV6SELECT	IPv6 COS Table Selection	Indicates the selection of the IPv6 COS table. 0: The IPv4 table is accessed. The valid range of the ADDRESS bits is from 0 to 63. 1: The IPv6 table is accessed. The valid range of the ADDRESS bits is from 0 to 255.	R/W
b10, b9	PRIORITY	COS Table Priority	When writing, set the priority information to be written to the COS table. When read, the priority information written to the COS table can be read. The address index of the COS table to be read is the address of the last write operation.	R/W
b30 to b11	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b31	READ	COS Table Operation Switching	Switches write or read operation to the COS table. Write operation to the register: 0: Write the priority information to the COS table. 1: Does not write the priority information to the COS table. (unchanged) Read operation from the register: The priority information of the address of the last write operation is read from the table. Follow the procedure below to read the priority information from the COS table. • Perform writing (specification of the address to be read) while this bit being 1 and the IPV6SELECT and ADDRESS bits are set to the desired values. • Execute read operation.	R/W

n = 0 to 2
n = 0: port 0, n = 1: port 1, n = 2: internal interface port (port 2)

29.2.2.17 PRIORITY Configuration Register n (PRIORITY_CFGn) (n = 0 to 2)

This register is used to set each port how received frames are assigned according to the priority of the queues in the switch by using which priority in the frames.
When several types of the priority fields are enabled, priority reassignment is executed according to higher priority (IP priority (DiffServ/COS), VLAN priority, and default priority).

Address(es): ETHERSW.PRIORITY_CFG0 A00C 0180h, ETHERSW.PRIORITY_CFG1 A00C 0184h, ETHERSW.PRIORITY_CFG2 A00C 0188h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DEFAULTPRI			—	—	IPEN	VLANEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	VLANEN	VLAN Priority Enable	Enables VLAN priority for a frame received on port n. 0: VLAN priority is not used. The priority field of the VLAN tag of a frame is ignored. 1: Priority in the switch is determined by using the priority field of the VLAN tag of a frame according to the VLAN_PRIORITYn setting for the port on which the frame was received.	R/W
b1	IPEN	IP Priority Enable	Enables IP priority for a frame received on port n. 0: IP priority is not used and IP DiffServ/COS fields of the frame are ignored. 1: Priority in the switch is determined by using the IP DiffServ/COS field according to the IP_PRIORITYn setting for the port on which the frame was received.	R/W
b3, b2	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b6 to b4	DEFAULTPRI	Default Priority Enable Setting	Set the default priority of a frame received on port n. When neither of the priorities is used, this priority is applied. The valid range is from 0 to 3 and always write 0 to the 3rd bit.	R/W
b31 to b7	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0 to 2
n = 0: port 0, n = 1: port 1, n = 2: internal interface port (port 2)

29.2.2.18 HUB Control Register (HUB_CONTROL)

This register is used to set the hub operation. High speed cut through will be possible by enabling the hub function.

Address(es): ETHERSW.HUB_CONTROL A00C 01C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	HUBIPG				BROCAFILEN	DIR1TO0EN	DIR0TO1EN	HUBEN
Value after reset:	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	HUBEN	Hub Enable	Enables or disables the hub. 0: Disabled 1: Enabled Note: When set to 0 and the HUB_FLT_MACnhi.FORCEFOW bit is disabled, the hub is reset. Note: Disabling the hub does not disable the forced forwarding that can be enabled within each individual HUB_FLT_MACnhi register.	R/W
b1	DIR0TO1EN	Port 0 Hub Forwarding Enable	Enables or disables a transfer from port 0 to port 1 by the hub. When enabled, all traffic received on port 0 is transferred to port 1 through the hub when the hub is active. 0: Disabled 1: Enabled	R/W
b2	DIR1TO0EN	Port 1 Hub Forwarding Enable	Enables or disables a transfer from port 1 to port 0 by the hub. When enabled, all traffic received from port 1 is transferred to port 0 through the hub when the hub is active. 0: Disabled 1: Enabled	R/W
b3	BROCAFILEN	Broadcast Filter Enable	Enables or disables broadcast filter. If set, the hub will not transfer any broadcast frames (should be set normally). 0: Disabled 1: Enabled	R/W
b7 to b4	HUBIPG	IPG Size Setting	Set the size of the Inter-Packet-Gap (number of octets) to be inserted between frames when the hub transmits frames consecutively. The gap value to be inserted must be given - 2. The default Ethernet IPG is 12 octets, resulting in a value of 10 set in this register. The valid value range is from 6 to 13. Note: The hub must be disabled if either of the ports operates in half-duplex mode.	R/W
b31 to b8	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note: DIR1TO0EN and DIR0TO1EN can be enabled at the same time. Simultaneous transfers of both directions is possible.

29.2.2.19 HUB Frame Count Register (HUB_STATS)

This register is used to indicate the number of frames transferred through the hub from one port to another. The counter of the channel is cleared when transfer is disabled (bit DIR1TO0EN or DIR0TO1EN of register HUB_CONTROL is set to 0).

Address(es): ETHERSW.HUB_STATS A00C 01C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NUM1TO0															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NUM0TO1															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	NUM0TO1	Port 0 Transfer Frame Number Indication	Number of frames transferred through the hub from port 0 to port 1 (the HUB_CONTROL.DIR0TO1EN bit is 1).	R
b31 to b16	NUM1TO0	Port 1 Transfer Frame Number Indication	Number of frames forwarded through the hub from port 1 to port 0 (the HUB_CONTROL.DIR1TO0EN bit is 1).	R

29.2.2.20 MAC Address Low Register For Hub Input Filter (HUB_FLT_MACnlo) (n = 0 to 6)

This register is used to set MAC addresses to be filtered in the hub. The first 4 octets of the MAC address are set to the HUB_FLT_MACnlo register and the remaining 2 octets are set to the HUB_FLT_MACnhi register. Up to 7 MAC addresses can be set. When any of the set MAC addresses matches with the destination address of the incoming frame, the frame is not transferred through the hub. MAC addresses of the unused register should be set to 0.

Address(es): ETHERSW.HUB_FLT_MAC0lo A00C 01C8h, ETHERSW.HUB_FLT_MAC1lo A00C 01D0h, ETHERSW.HUB_FLT_MAC2lo A00C 01D8h, ETHERSW.HUB_FLT_MAC3lo A00C 01E0h, ETHERSW.HUB_FLT_MAC4lo A00C 01E8h, ETHERSW.HUB_FLT_MAC5lo A00C 01F0h, ETHERSW.HUB_FLT_MAC6lo A00C 01F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MACADD4n								MACADD3n							
Value after reset:	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD2n								MACADD1n							
Value after reset:	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1

Note 1. n = 0 to 5: The value after reset is 0000 0000h.
n = 6: The value after reset is 006C 2101h. The destination address of the beacon frame is set for the value after reset. The beacon frame destination address must be held in the register when the DLR function is used.

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD1n	MAC Address n First Byte Setting	Set the 1st byte of MAC address n	R/W
b15 to b8	MACADD2n	MAC Address n Second Byte Setting	Set the 2nd byte of MAC address n	R/W
b23 to b16	MACADD3n	MAC Address n Third Byte Setting	Set the 3rd byte of MAC address n	R/W
b31 to b24	MACADD4n	MAC Address n Fourth Byte Setting	Set the 4th byte of MAC address n	R/W

n = 0 to 6

29.2.2.21 MAC Address High Register For Hub Input Filter (HUB_FLT_MACnhi) (n = 0 to 6)

This register is used to set MAC addresses to be filtered in the hub. The first 4 octets of the MAC address are set to the HUB_FLT_MACnlo register and the remaining 2 octets are set to the HUB_FLT_MACnhi register. Up to 7 MAC addresses can be set. When any of the MAC addresses set matches with the destination address of the incoming frame, the frame is not transferred through the hub. MAC addresses of unused registers should be set to 0 and the MASKCOMP bit should be set to 0xFF.

Address(es): ETHERSW.HUB_FLT_MAC0hi A00C 01CCh, ETHERSW.HUB_FLT_MAC1hi A00C 01D4h, ETHERSW.HUB_FLT_MAC2hi A00C 01DCh, ETHERSW.HUB_FLT_MAC3hi A00C 01E4h, ETHERSW.HUB_FLT_MAC4hi A00C 01ECh, ETHERSW.HUB_FLT_MAC5hi A00C 01F4h, ETHERSW.HUB_FLT_MAC6hi A00C 01FCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b2b. 1	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	FORCE FOW	MASKCOMP							
Value after reset:	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD6n								MACADD5n							
Value after reset:	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1	*1

Note 1. n = 0 to 5: The value after reset is 0000 0000h.
n = 6: The value after reset is 01FF 0100h. The destination address of the beacon frame and enabling of forced forwarding are set for the value after reset. The beacon frame destination address must be held in the register when the DLR function is used.

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD5n	MAC Address n Fifth Byte Setting	Set the 5th byte of MAC address n	R/W
b15 to b8	MACADD6n	MAC Address n Sixth Byte Setting	Set the 6th byte of MAC address n Bits of this field that correspond to bits of MASKCOMP for which the setting is 0 must also be set to 0.	R/W
b23 to b16	MASKCOMP	MAC Address Last Byte Mask Setting	The last byte of the MAC address (6th byte) can be masked and filtered in bit units. Of these 8 bits, only the bits set to 1 are compared in the case of filtering. The bits set to 0 are not compared. The logical AND of the last byte of received MAC addresses and these bits is taken and the result is compared with the value of the MACADD6n bits. Thus, the setting of MACADD6n bits corresponding to zero-valued bits of the mask setting should be 0.	R/W
b24	FORCEFOW	Forced Forward Setting	Enables or disables forced forwarding. 0: Disabled 1: Enabled When enabled, a frame whose MAC address matches is not filtered, and transferred through the hub. This frame is not transferred to the switch. The switch does not receive the frame because the frame is forcibly forwarded before being handled in the MAC in the switch. The DLR module will still be able to receive the frame. Forced forwarding is enabled even when the hub function is disabled (the HUB_CONTROL.HUBEN bit is set to 0).	R/W
b31 to b25	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0 to 6

29.2.2.22 Switch Statistics Registers

This LSI stores statistics of the frame to be processed by the Ethernet switch in the following registers.
All registers are 32-bit, read only and the value after reset is 0000 0000h.

Address	Symbol	Description
A00C 0300h	TOTAL_BYT_FRM	Total number of incoming frames processed and not discarded in bytes. (Sum of bytes of frames counted in TOTAL_FRM)
A00C 0304h	TOTAL_BYT_DISC	Total number of incoming frames processed but discarded in the switch in bytes. (Sum of bytes of frames counted in TOTAL_DISC)
A00C 0308h	TOTAL_FRM	Total number of incoming frames processed and not discarded.
A00C 030Ch	TOTAL_DISC	Total number of incoming frames processed but discarded in the switch.
A00C 0310h + 0008h*n	ODISCn	Port n outgoing frames discarded due to output queue congestion.
A00C 0314h + 0008h*n	IDISC_BLOCKEDn	Port n incoming frames discarded (after learning) as port is configured in blocking mode.

n = 0 to 2
n = 0: port 0, n = 1: port 1, n = 2: internal interface port (port 2)

29.2.3 Learning Interface Registers

Source addresses that the switch has learned and port information can be obtained through the learning interface to build a look-up table. The information can be obtained through two registers, but register LRN_REC_A must be read first, followed by a read to register LRN_REC_B.
After accessing register LRN_REC_B, the next learning entry, if available, is presented in registers LRN_REC_A and LRN_REC_B by FIFO.

29.2.3.1 Learning Record A Register (LRN_REC_A)

Address(es): ETHERSW.LRN_REC_A A00C 0500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SRCADD4								SRCADD3							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRCADD2								SRCADD1							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SRCADD1	Source MAC Address First Octet Indication	Indicate the 1st octet of source MAC address.	R
b15 to b8	SRCADD2	Source MAC Address Second Octet Indication	Indicate the 2nd octet of source MAC address.	R
b23 to b16	SRCADD3	Source MAC Address Third Octet Indication	Indicate the 3rd octet of source MAC address.	R
b31 to b24	SRCADD4	Source MAC Address Fourth Octet Indication	Indicate the 4th octet of source MAC address.	R

29.2.3.2 Learning Record B Register (LRN_REC_B)

Address(es): ETHERSW.LRN_REC_B A00C 0504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	PORT				HASH							
Value after reset:	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRCADD6								SRCADD5							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SRCADD5	Source MAC Address Fifth Octet Indication	Indicate the 5th octet of the source MAC address.	R
b15 to b8	SRCADD6	Source MAC Address Sixth Octet Indication	Indicate the 6th octet of the source MAC address.	R
b23 to b16	HASH	Source MAC Address Hash Code Indication	Indicate hash code for the source MAC address.	R
b27 to b24	PORT	Port Number Indication	Indicate port number.	R
b31 to b28	—	Reserved	When read, an undefined value is read.	R

29.2.3.3 Learning Data Status Register (LRN_STATUS)

This register is used to indicate whether the learning data in register LRN_REC_A and register LRN_REC_B are valid.

Address(es): ETHERSW.LRN_STATUS A00C 0508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LERNAVAL
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	LERNAVAL	Learning Data Status	Indicates learning data status. 0: Invalid 1: Valid	R
b31 to b1	—	Reserved	When read, an undefined value is read.	R

29.2.3.4 Address Table (ADR_TABLE)

The address table consists of blocks of 256 entries and each block contains 8 records which include 64-bit information. The 64-bit length record includes 48-bit MAC addresses and information necessary for transfer information as well as priority or time stamp information. The start address of such an 8-entry block is defined by the hash code derived from the MAC address. For the details, see section 29.3.1.4, Layer 2 Look Up Engine, section (3), Address Table, and section 29.4.3, Address Table Setting.

29.2.4 MAC Port Registers

These registers are related to the MACs of port 0 and port 1 that share most of the registers (COMMAND_CONFIGn and registers except for statistics register). Read and write operation are possible with access to the address configured by each port. The shared registers are indicated as “shared” in the names.

29.2.4.1 Command Configure Register n (COMMAND_CONFIGn) (n = 0, 1)

This register is used to configure and reset the MAC.

Address(es): ETHERSW.COMMAND_CONFIG0 A00C 8008h, ETHERSW.COMMAND_CONFIG1 A00C A008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CNTRESET	—	—	—	—	RXERRDISC	—	NOLGTHCHK	CNTRLREMEN	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SWRESET	—	—	—	—	—	—	—	—	—	—	—	RXENA	TXENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TXENA	Transmission Enable	Enables or disables a MAC transmit path. 0: Disabled 1: Enabled This bit is cleared to 0 by a software reset.	R/W
b1	RXENA	Reception Enable	Enables or disables a MAC receive path. 0: Disabled 1: Enabled This bit is cleared to 0 by a software reset.	R/W
b3, b2	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b4	—	Reserved	The read value is undefined. When writing, write 1.	R/W
b12 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b13	SWRESET	Software Reset	Self-clearing software reset command. When written with 1, transmission and reception by MAC are disabled and the reception buffer is cleared. After software reset sequence is complete, this bit is automatically cleared to 0. Note: The bit is cleared to 0 only when the clock on the line of both MACs are supplied. When the clock on the line is not supplied, clear this bit by writing 0.	R/W
b22 to b14	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b23	CNTRLREMEN	Control Frame Enable	Enables or disables MAC control frames. 0: MAC Control frames with any Opcode other than 0001h are discarded. 1: MAC Control frames with any Opcode other than 0001h are received and transferred to other port.	R/W
b24	NOLGTHCHK	Payload Length Check Setting	Enables or disables payload length checking. 0: Enabled (debug) 1: Disabled Note: Always write 1 for this LSI.	R/W
b25	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b26	RXERRDISC	Reception Error Frame Discard Setting	Enables or disables receive error frame discard 0: Error frames are transferred to other port when RX_ER is asserted. (debug) 1: Any frame received with an error is discarded in the Core and not transferred to other port. Note: Always write 1 for this LSI.	R/W
b30 to b27	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b31	CNTRESET	Counter Reset	Self-clearing counter reset command When written with 1, the statistic counters are all set to 0. Afterwards, the bit is automatically cleared to 0. Note: This register is not shared between MAC0 and MAC1. However, this bit is an exception. Writing 1 to the bit through the MAC0 or MAC1 register will clear both MAC statistics.	R/W

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.4.2 Maximum Frame Length Register n (FRM_LENGTHn) (Shared) (n = 0, 1)

This register is used to set maximum frame length and to check frame length in the MAC reception circuit. The value after reset is set to 1522 allowing frames with a single VLAN tag. The value can be set to around 1536 to be more flexible for the tag. The allowed maximum is 1700.

Address(es): ETHERSW.FRM_LENGTH0 A00C 8014h, ETHERSW.FRM_LENGTH1 A00C A014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	FRMLEN													
Value after reset:	0	0	0	0	0	1	0	1	1	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	FRMLEN	Maximum Frame Length Setting	Set maximum frame length.	R/W
b31 to b14	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.4.3 FIFO Buffer Threshold Register n (Shared) (n = 0, 1)

This register is used to configure the threshold of the FIFO buffer of the MAC and to manage overflow and underflow. It is not necessary to change from the value after reset basically.

Address	Symbol	Initial Value	R/W	Description
A00C 801Ch + 2000h*n	RX_SECTION_EMPTYn	0000 0000h	R	Threshold to indicate that the reception buffer is almost full. Reaching this is typically used as a trigger for transmitting a pause frame. Generation does not proceed when the setting is 0. The value cannot be changed from 0 in this LSI.
A00C 8020h + 2000h*n	RX_SECTION_FULLn	0000 0000h	RW	Threshold to indicate whether there are enough entries for a read from the reception buffer When set to 0, it enters to “Store and Forward”. Always set 0 in this LSI.
A00C 8024h + 2000h*n	TX_SECTION_EMPTYn	0000 0048h	RW	Threshold to indicate that the transmit FIFO is almost full.
A00C 8028h + 2000h*n	TX_SECTION_FULLn	0000 0014h	RW	Threshold to indicate whether there are enough entries for a read from the transmit FIFO.
A00C 802Ch + 2000h*n	RX_ALMOST_EMPTYn	0000 0008h	R	Threshold for unread entries before the reception buffer becomes empty. This is used to avoid any underflow of the FIFO. The value cannot be changed in this LSI.
A00C 8030h + 2000h*n	RX_ALMOST_FULLn	0000 0005h	R	Threshold for unread entries before the reception buffer becomes empty. This is used to avoid an overflow of the FIFO. The value cannot be changed in this LSI.
A00C 8034h + 2000h*n	TX_ALMOST_EMPTYn	0000 0004h	R	Threshold for unread entries before the transmit FIFO becomes empty. This is used to avoid an underflow of the FIFO. The value cannot be changed in this LSI.
A00C 8038h + 2000h*n	TX_ALMOST_FULLn	0000 0010h	R	Threshold for unread entries before the transmit FIFO becomes empty. This is used to avoid an overflow of the FIFO. The value cannot be changed in this LSI.

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.4.4 MAC Status Register n (MAC_STATUSn) (Shared) (n = 0, 1)

This register is used to indicate communication settings of the MAC.

Address(es): ETHERSW.MAC_STATUS0 A00C 8058h, ETHERSW.MAC_STATUS1 A00C A058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	HDPP1	—	SPEED P1	—	HDPP0	—	SPEED P0	—	—	—	—	—	—	—	—
Value after reset:	x	0	x	0	x	0	x	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	When read, an undefined value is read.	R
b8	SPEEDP0	MAC port 0 Link Speed Setting	Sets the link speed of the MAC port 0. 0: 10/100 Mbps 1: 1 Gbps	R
b9	—	Reserved	When read, an undefined value is read.	R
b10	HDPP0	MAC port 0 Duplex Setting	Sets duplex of the MAC port 0 0: Full duplex 1: Half duplex	R
b11	—	Reserved	When read, an undefined value is read.	R
b12	SPEEDP1	MAC port 1 Link Speed Setting	Sets the link speed of the MAC port 1. 0: 10/100 Mbps 1: 1 Gbps	R
b13	—	Reserved	When read, an undefined value is read.	R
b14	HDPP1	MAC port 1 Duplex Setting	Sets duplex of the MAC port 1 0: Full duplex 1: Half duplex	R
b31 to b15	—	Reserved	When read, an undefined value is read.	R

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.4.5 Transmit IPG Length Register n (TX_IPG_LENGTHn) (Shared) (n = 0, 1)

This register is used to set the Inter-Packet Gap (IPG) during transmission.

Address(es): ETHERSW.TX_IPG_LENGTH0 A00C 805Ch, ETHERSW.TX_IPG_LENGTH1 A00C A05Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	TXIPGLEN				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	TXIPGLEN	Inter-Packet Gap Setting	Sets Inter-Packet Gap (IPG) (byte-times) during transmission. The valid range is from 8 to 27. If a value outside of the range is programmed, the IPG is set to 12.	R/W
b31 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.4.6 MAC RX/TX Statistic Counters

This LSI stores statistics of the frame processed by the Ethernet switch in the register for each port.
The registers listed below are all 32-bit, read only and the value after reset is 0000 0000h.

(1) MAC RX Statistic Counters

Address	Symbol	Description
A00C 8100h + 2000h*n	etherStatsOctets_n	Total octets of the frames received on port n (including both normal and abnormal frames)
A00C 8104h + 2000h*n	OctetsOK_n	Total octets of the frames received on port n (normal frames only). A substitute of ifInOctets of the MIB counter.
A00C 8108h + 2000h*n	aAlignmentErrors_n	Number of frames received on port n when SDF is not detected even if RX_DV of the frame is deasserted
A00C 810Ch + 2000h*n	aPAUSEMACCtrlFrames_n	Number of normal pause frames received on port n
A00C 8110h + 2000h*n	FramesOK_n	Number of normal frames received on port n
A00C 8114h + 2000h*n	CRCErrors_n	Number of frames with abnormal CRC but normal length received on port n
A00C 8118h + 2000h*n	VLANOK_n	Number of normal frames with VLAN tag received on port n
A00C 811Ch + 2000h*n	ifInErrors_n	Number of frames received on port n with any of receive errors. • FIFO overflow errors • CRC errors • Payload length errors • Jabber and oversized errors • PHY errors (RX_ER asserted)
A00C 8120h + 2000h*n	ifInUcastPkts_n	Number of normal unicast frames received on port n
A00C 8124h + 2000h*n	ifInMulticastPkts_n	Number of normal multicast frames received on port n
A00C 8128h + 2000h*n	ifInBroadcastPkts_n	Number of normal broadcast frames received on port n
A00C 812Ch + 2000h*n	etherStatsDropEvents_n	Number of frames failed to receive on port n due to not enough space in FIFO
A00C 8130h + 2000h*n	etherStatsPkts_n	Total frames received on port n (normal and abnormal)
A00C 8134h + 2000h*n	etherStatsUndersizePkts_n	Number of frames with length of 64 bytes or less and normal CRC (excluding frames with length of 24 bytes or less)
A00C 8138h + 2000h*n	etherStatsPkts64Octets_n	Number of frames with length of 64 bytes received on port n
A00C 813Ch + 2000h*n	etherStatsPkts65to127Octets_n	Number of frames with length from 65 to 127 bytes received on port n
A00C 8140h + 2000h*n	etherStatsPkts128to255Octets_n	Number of frames with length from 128 to 255 bytes received on port n
A00C 8144h + 2000h*n	etherStatsPkts256to511Octets_n	Number of frames with length from 256 to 511 bytes received on port n
A00C 8148h + 2000h*n	etherStatsPkts512to1023Octets_n	Number of frames with length from 512 to 1023 bytes received on port n
A00C 814Ch + 2000h*n	etherStatsPkts1024to1518Octets_n	Number of frames with length from 1024 to 1518 bytes received on port n
A00C 8150h + 2000h*n	etherStatsPkts1519toMax_n	Number of frames with length from 1519 bytes to the value of the maximum frame length register (FRM_LENTGHn) received on port n
A00C 8154h + 2000h*n	etherStatsOversizePkts_n	Number of frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) and with normal CRC received on port n

Address	Symbol	Description
A00C 8158h + 2000h*n	etherStatsJabbers_n	Number of frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) and with abnormal CRC received on port n
A00C 815Ch + 2000h*n	etherStatsFragments_n	Number of frames with length of 64 bytes or less and abnormal CRC received on port n (excluding frames with length of 24 bytes or less) DLR beacon frames are also counted.
A00C 8160h + 2000h*n	aMACControlFramesReceived_n	Number of normal frames with type 0x8808 received on port n
A00C 8164h + 2000h*n	aFrameTooLong_n	Total frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) in received on port n (normal and abnormal)
A00C 816Ch + 2000h*n	StackedVLANOK_n	Number of normal frames with the stacked VLAN tag received on port n

n = 0, 1
n = 0: port 0, n = 1: port 1

(2) MAC TX Statistic Counters

Address	Symbol	Description
A00C 8180h + 2000h*n	TXetherStatsOctets_n	Total octets of the frames transmitted on port n (including both normal and abnormal frames)
A00C 8184h + 2000h*n	TxOctetsOK_n	Total octets of the frames transmitted on port n (normal frames only)
A00C 818Ch + 2000h*n	TXaPAUSEMACCtrlFrames_n	Number of formal pause frames transmitted on port n
A00C 8190h + 2000h*n	TxFramesOK_n	Number of formal frames transmitted on port n
A00C 8194h + 2000h*n	TxCRCErrors_n	Number of frames with abnormal CRC but normal length transmitted on port n
A00C 8198h + 2000h*n	TxVLANOK_n	Number of formal frames with the VLAN tag transmitted on port n
A00C 819Ch + 2000h*n	ifOutErrors_n	Number of frames transmitted on port n with any of receive errors. • TX_ER • Frame length errors
A00C 81A0h + 2000h*n	ifUcastPkts_n	Number of normal unicast frames transmitted on port n
A00C 81A4h + 2000h*n	ifMulticastPkts_n	Number of normal multicast frames transmitted on port n
A00C 81A8h + 2000h*n	ifBroadcastPkts_n	Number of normal broadcast frames transmitted on port n
A00C 81ACh + 2000h*n	TXetherStatsDropEvents_n	Number of undersized frames transmitted on port n. Caused either by FIFO full or collisions during half- duplex communications.
A00C 81B0h + 2000h*n	TXetherStatsPkts_n	Total frames transmitted on port n (normal and abnormal)
A00C 81B4h + 2000h*n	TXetherStatsUndersizePkts_n	Number of frames with length of 64 bytes or less and normal CRC (rarely occurs)
A00C 81B8h + 2000h*n	TXetherStatsPkts64Octets_n	Number of frames with length of 64 bytes transmitted on port n
A00C 81BCh + 2000h*n	TXetherStatsPkts65to127Octets_n	Number of frames with length from 65 to 127 bytes transmitted on port n
A00C 81C0h + 2000h*n	TXetherStatsPkts128to255Octets_n	Number of frames with length from 128 to 255 bytes transmitted on port n
A00C 81C4h + 2000h*n	TXetherStatsPkts256to511Octets_n	Number of frames with length from 256 to 511 bytes transmitted on port n
A00C 81C8h + 2000h*n	TXetherStatsPkts512to1023Octets_n	Number of frames with length from 512 to 1023 bytes transmitted on port n

Address	Symbol	Description
A00C 81CCh + 2000h*n	TXetherStatsPkts1024to1518Octets_n	Number of frames with length from 1024 to 1518 bytes transmitted on port n
A00C 81D0h + 2000h*n	TXetherStatsPkts1519toMax_n	Number of frames with length from 1519 bytes to the value of maximum frame length register (FRM_LENTGHn)
A00C 81D4h + 2000h*n	TXetherStatsOversizePkts_n	Frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) and with normal CRC transmitted on port n
A00C 81D8h + 2000h*n	TXetherStatsJabbers_n	Frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) and with abnormal CRC transmitted on port n
A00C 81DCh + 2000h*n	TXetherStatsFragments_n	Frames with length 64 bytes or less transmitted on port n and marked erroneous
A00C 81E0h + 2000h*n	aMACControlFrames_n	Normal frames with type 0x8808 transmitted on port n
A00C 81E4h + 2000h*n	TXaFrameTooLong_n	Total frames with length exceeding the value of the maximum frame length register (FRM_LENTGHn) received on port n (normal and abnormal)
A00C 81ECh + 2000h*n	aMultipleCollisions_n	Number of frames successfully transmitted after multiple collisions occurred on port n Relevant only for half-duplex communications
A00C 81F0h + 2000h*n	aSingleCollisions_n	Number of frames successfully transmitted after one collision occurred on port n Relevant only for half-duplex communications
A00C 81F4h + 2000h*n	aLateCollisions_n	Number of frames sent in error due to late collisions on port n Relevant only for half-duplex communications
A00C 81F8h + 2000h*n	aExcessCollisions_n	Number of frames discarded due to excessive collisions (16 unsuccessful transmissions) on port n Relevant only for half-duplex communications

n = 0, 1
n = 0: port 0, n = 1: port 1

29.2.5 Timer Module Registers

The Ethernet switch incorporates a programmable timer module that is used for all timestamping functions. The timer module registers are used to indicate the settings and status.

29.2.5.1 Timer Module Configuration Register (TSM_CONFIG)

This register is used to control interrupt generation due to any event occurred during use of the timer functions.

Address(es): ETHERSW.TSM_CONFIG A00C C004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IRQTXENAP1	IRQTXENAP0	—	—	—	—	—	—	—	IRQTEST	IRQTIMOVER	IRQEVTPERD	IRQEVTOFF	IRQENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IRQENA	Timer Interrupt setting	Enables or disables an timer interrupt. No interrupt is generated unless this bit is set to 1 even when other bits are set to 1. 0: Disabled 1: Enabled	R/W
b1	IRQEVTOFF	Offset Correction Complete Interrupt Setting	Controls interrupt generation when timer offset correction is complete. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b2	IRQEVTPERD	ns Timer Interrupt Setting	Controls interrupt generation when ns timer reaches 1 second. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b3	IRQTIMOVER	Overflow Interrupt Setting	Controls interrupt generation when timer overflows. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b4	IRQTEST	Interrupt Setting for Test	Controls interrupt generation for software testing. 0: Normal operation 1: Interrupt is generated at the same timing of a write operation.	R/W
b11 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b12	IRQTXENAP0	Port 0 Transmit Timestamp Capture Interrupt Setting	Enables or disables transmit timestamp capture interrupt of port 0 0: Disabled 1: Enabled (interrupt is generated) When set, an interrupt is generated when the port's transmit timestamp register has stored a new timestamp.	R/W
b13	IRQTXENAP1	Port 1 Transmit Timestamp Capture Interrupt Setting	Enables or disables an interrupt due to transmit timestamp capture of port 1 0: Disabled 1: Enabled (interrupt is generated) When set, an interrupt is generated when the port's transmit timestamp register has stored a new timestamp.	R/W
b31 to b14	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.5.2 Interrupt Status/ACK Register (TSM_IRQ_STAT_ACK)

This register is used to check status of the interrupt by timer.
Reading the register can check the interrupt status/acknowledge. Interrupt generation is indicated by 1 while no interrupt generation by 0.
Writing 1 to the register clears the interrupt as well as the bit value.

Address(es): ETHERSW.TSM_IRQ_STAT_ACK A00C C008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IRQTXP1	IRQTXP0	—	—	—	—	—	—	—	IRQTEST	IRQTIMOVER	IRQEVTPERD	IRQEVTOFF	IRQENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IRQENA	Timer Interrupt Status	Indicates interrupt generation.	R/W
b1	IRQEVTOFF	Offset Addition Interrupt Status	Indicates interrupt generation due to timer offset addition	R/W
b2	IRQEVTPERD	ns Timer Interrupt Status	Indicates interrupt generation when ns timer reaches 1 second.	R/W
b3	IRQTIMOVER	Overflow Interrupt Status	Indicates overflow interrupt generation.	R/W
b4	IRQTEST	Interrupt Status for Test	Indicates interrupt generation for software testing.	R/W
b11 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b12	IRQTXP0	Port 0 Transmit Timestamp Capture Interrupt Status	Indicates interrupt generation of transmit timestamp capture of port 0	R/W
b13	IRQTXP1	Port 1 Transmit Timestamp Capture Interrupt Status	Indicates interrupt generation of transmit timestamp capture of port 1	R/W
b31 to b14	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.5.3 Port Timestamp Control/Status Register (PORTn_CTRL) (n = 0, 1)

This register is used to indicate the storage method of the timestamp acquired on port n to the register and status of the stored timestamp.

Address(es): ETHERSW.PORT0_CTRL A00C C020h, ETHERSW.PORT1_CTRL A00C C028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TSKEEP	TSOVR	TSVALID
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSVALID	Timestamp Status	Indicates the status of stored timestamp. 0: Timestamp is invalid. 1: Timestamp is valid. Writing to the register (with any value) clears the bit.	R/W
b1	TSOVR	Timestamp Overwrite Status	Indicates that a newer timestamp has overwritten the last stored timestamp. 0: Timestamp is not overwritten. 1: Timestamp is overwritten. This bit is set to 1 when a valid timestamp is stored (TSVALID = 1) and another timestamp is received before the software read the value. Writing to the register (with any value) clears the bit. When the configuration bit TSKEEP is set, if a new timestamp is received while TSVALID is 1, this bit indicates that timestamp(s) are ignored.	R/W
b2	TSKEEP	Timestamp Operation Setting	Sets timestamp to be stored in the timestamp register upon reception of a new timestamp. 0: The stored timestamp is overwritten with the new one. 1: The last timestamp is retained. When set, the stored timestamp is retained and a new timestamp is ignored until software has processed the timestamp and the TSVALID bit becomes 0.	R/W
b31 to b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.5.4 Port Timestamp Register (PORTn_TIME) (n = 0, 1)

This register is used to store time stamps obtained on port n.

Address(es): ETHERSW.PORT0_TIME A00C C024h, ETHERSW.PORT1_TIME A00C C02Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSREG															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSREG															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TSREG	Timestamp Store	Timestamp acquired on port n	R

n = 0, 1
n = 0: MAC port 0, n = 1: MAC port 1

29.2.5.5 Timer Control Register (ATIME_CTRL)

This register is used to set timer interrupt events and control timer.

Address(es): ETHERSW.ATIME_CTRL A00C C120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PLUS1	CAPTR	—	RST	—	—	—	EVTPERIRST	EVTPERIENA	—	EVTOFFENA	—	TMENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMENA	Timer Operation Control	0: Timer stops at the current value. 1: Timer starts counting.	R/W
b1	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b2	EVTOFFENA	Offset Correction Event Setting	Enables or disables an offset correction event. 0: Offset correction is not executed. 1: Offset correction is executed. When offset correction is complete, and if interrupt generation is set through the TSM_CONFIG register, an offset correction-event interrupt is generated and this bit is cleared to 0. For another offset correction, setting the bit to 1 is required. Note: The timer offset value should be set in advance.	R/W
b3	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b4	EVTPERIENA	Periodical Event Setting	Enables or disables periodical event in 1-second units. 0: No periodical event is generated. 1: A periodical event in 1-second units is generated. When interrupt generation is set through the TSM_CONFIG register, a periodical event due to switch interrupt is also generated. Note: The timer periodical value should be set in advance.	R/W
b5	EVTPERIRST	Periodical Event Timer Reset Setting	Sets a reset of the periodical event timer. 0: Timer counts up till wraparound. 1: Timer is reset to 0 when the count value of the timer reaches 1 second.	R/W
b8 to b6	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b9	RST	Timer Reset	Writing 1 resets the timer. This has no effect on the counter enable. When written with 1 while the counter is enabled, timer is reset to 0 and starts counting from the point.	R/W
b10	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b11	CAPTR	Timer Value Capture	Writing 1 captures the current timer value. When capture is complete, the bit is cleared, and time can be read from the ATIME and ATIME_SEC registers.	R/W
b12	PLUS1	Timer Counter Increment Setting	Writing 1 increments the timer counter by 1. When increment is complete, the bit is cleared.	R/W
b31 to b13	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note 1. Bits 12, 11, and 9 are for command and can be used to activate the corresponding events directly. It is not necessary to retain any value of other bits set in the register when the command bit is set (i.e. read-modify-write is not required). The bits are read as 0 after the command has completed. If any of the command bits are non-zero, other bits are ignored.

Note 2. The value of timer can not be captured accurately while the timer is stopped. The captured value is invalid.

29.2.5.6 Timer Nanoseconds Register (ATIME)

This register is used to indicate the value of the nanosecond(ns)-timer and set time of the ns timer.

Address(es): ETHERSW.ATIME A00C C124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMR	ns Timer Setting	Indicate setting value and read value of the timer. When writing to the register: set time to the timer. When read from the register: return the last captured value. To read the current value, a capture command of the ATIME_CTRL register (CAPTR bit) must be issued in advance. The value represents in nanoseconds (ns).	R/W

Note: The seconds value must be programmed into the ATIME_SEC register prior to writing into this register.

29.2.5.7 Timer Offset Correction Register (ATIME_OFFSET)

This register is used to set the value to be used to perform offset corrections. The offset can be corrected in two different methods and different setting values must be set for each method.
Write operation to the register starts offset correction. Thus, the value must be set to the ATIME_OFFS_CORR register in advance to select the correction method.

Address(es): ETHERSW.ATIME_OFFSET A00C C128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	OFFSET															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OFFSET															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	OFFSET	Offset Correction Value Setting	Set values for performing offset corrections. • When register ATIME_OFFS_CORR is 0: Write the value to be offset. The value represents in nanoseconds. The written value is immediately added to the current timer value when this register is written. When a negative value is written, the value is subtracted. • When register ATIME_OFFS_CORR is not 0: Write the value that defines how many offset corrections will be performed. When written, correction starts. The value is not immediately added to the current timer value When offset correction is performed, the value of the register is decremented by 1. Offset correction and decrementation are repeated until it reaches 0. When it has reached 0, no more offset corrections is performed and the register then is reset to 0. The interval of the offset is specified by the ATIME_OFFS_CORR register while the offset value is specified by the ATIME_INC register.	R/W

29.2.5.8 Generate Timer Periodic Event Register (ATIME_EVT_PERIOD)

This register is used to set the periodical value for generating periodic events. The nanoseconds timer has reached this time, the periodical event occurs and the nanoseconds timer restarts. The value represents in nanoseconds (ns). The value after reset is 10^9 nanoseconds, representing 1 second.

Address(es): ETHERSW.ATIME_EVT_PERIOD A00C C12Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TIMPEREVET															
Value after reset:	0	0	1	1	1	0	1	1	1	0	0	1	1	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TIMPEREVET															
Value after reset:	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TIMPEREVET	Event Periodical Setting	Period of an periodical event. It is necessary to set 3B9A CA00h (1 sec).	R/W

Note: Cycle events is fixed to 1 second and can not be changed. Otherwise, the timer will not operate normally.

29.2.5.9 Timer Drift Correction Register (ATIME_CORR)

This register is used to set correction period to be applied for drift correction by using clock cycle count. The amount of correction is defined in the ATIME_INC register.

Address(es): ETHERSW.ATIME_CORR A00C C130h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	DRIFCORVAL														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DRIFCORVAL															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b30 to b0	DRIFCORVAL	Drift Correction Period Setting	Period for drift correction. Set the value by using clock cycles (100 MHz (10 ns)). For example, a drift correction with 1 msec intervals, set 10^5 (0001 86A0h) (set a desirable value for correction interval according to the actual application).	R/W
b31	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note: The correction value is the reciprocal of the ppm deviation between the master and slave oscillators. This value is given in clock cycles, not in nanoseconds.

29.2.5.10 Timer Increment Register (ATIME_INC)

This register is used to set the correction amount to be used for offset or drift correction.

Address(es): ETHERSW.ATIME_INC A00C C134h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	OFFSCORRINC						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CORRINC							—	CLKPERD						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	CLKPERD	Clock Cycle Setting	Clock cycle of the timestamping clock in nanoseconds. Always set 10 ns (001010b). The clock 100 MHz and no other value cannot be set. The timer will increment by this amount with every clock cycle.	R/W
b7	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b14 to b8	CORRINC	Clock Cycle Correction Amount Setting	Set correction amount for clock cycle for drift corrections. This value will be added for each correction cycle specified in register ATIME_CORR. Setting a value smaller than in the CLKPERD bit will slow down the timer. Setting a value larger than in the CLKPERD bit will speed up the timer.	R/W
b15	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b22 to b16	OFFSCORRINC	Offset Correction Amount Setting	Set correction amount for offset correction. This value will be added for each clock cycle specified in register ATIME_OFFS_CORR.	R/W
b31 to b23	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.5.11 Timer Second Register (ATIME_SEC)

This register is used to indicate the seconds timer value. The time of the seconds timer can be set and the captured time can be obtained. The seconds-timer is incremented when the nanoseconds timer has reached 10^9 nanoseconds.

Address(es): ETHERSW.ATIME_SEC A00C C138h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SECTIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECTIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SECTIM	Seconds Timer Setting	Indicate the setting value and read value of the seconds time. When writing to the register: set time to the timer. The register is not updated when written and the value is retained in the local register. Afterwards, the ATIME register is written, the value in the local register is acquired to the register. When read from the register: return the last captured value. To read the current value, the capture command of register ATIME_CTRL (CAPTR bit) must be issued in advance. The unit of the value is in seconds.	R/W

29.2.5.12 Timer Offset Correction Count Register (ATIME_OFFS_CORR)

This register is used to set the interval for offset correction.
It is used in combination with the ATIME_OFFSET register to distribute the time change over a longer time due to additional offsets. It avoids jumps in time and minimizes jitter during offset corrections.

Address(es): ETHERSW.ATIME_OFFS_CORR A00C C13Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	OFFCOR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OFFCOR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	OFFCOR	Offset Correction Interval Setting	Specify the interval of offset correction. The interval will be set with cycle count of a 100 MHz clock.	R/W

29.2.5.13 Timer Output Enable Register (SWTMEN)

This register is used to enable time synchronous timer pulse output (SYNCOUT signal).
This register can be read and written in 32-bit units.
Note: Always enable output after setting the timer output control registers below:
SWTMSTSEC, SWTMSTNS, SWTMPSEC, SWTMPNS, and SWTMWTH.

Address(es): ETHERSW.SWTMEN A00B F200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	OUTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	OUTEN	SYNCOUT Signal Output Setting	Enables output of the SYNCOUT signal. 0: Disabled 1: Enabled	R/W
b31 to b1	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.5.14 Timer Start Second Register (SWTMSTSEC)

This register is used to set start time of SYNCOUT output in seconds.

Address(es): ETHERSW.SWTMSTSEC A00B F204h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMSTSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMSTSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMSTSEC	SYNCOUT Signal Output Start Time Setting	Set the start time of SYNCOUT output in seconds.	R/W

29.2.5.15 Timer Start Nanosecond Register (SWTMSTNS)

This register is used to set start time of SYNCOUT output in nanoseconds.

Address(es): ETHERSW.SWTMSTNS A00B F208h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMSTNS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMSTNS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMSTNS	SYNCOUT Signal Output Start Time Setting	Set the start time of SYNCOUT output in nanoseconds.	R/W

29.2.5.16 Timer Period Second Register (SWTMPSEC)

This register is used to set the period of SYNCOUT output in seconds.

Address(es): ETHERSW.SWTMPSEC A00B F20Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMPSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMPSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMPSEC	SYNCOUT Signal Output Period Setting	Set the period of SYNCOUT output in seconds.	R/W

29.2.5.17 Timer Period Nanosecond Register (SWTMPNS)

This register is used to set the period of SYNCOUT output in nanoseconds. Set the value which is to define the cycle when used as a divisor of the value for one second specified in the ATIME_EVT_PERIOD register.

Note 1. Set this register before enabling SYNCOUT signal output.

Note 2. The value must be greater than or equal to 30 ns.

Address(es): ETHERSW.SWTMPNS A00B F210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMPNS															
Value after reset:	0	0	1	1	1	0	1	1	1	0	0	1	1	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMPNS															
Value after reset:	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMPNS	SYNCOUT Signal Output Period Setting	Set the period of SYNCOUT output in nanoseconds. The value must be a multiple of 10 ns.	R/W

29.2.5.18 Timer Pulse Width Register (SWTMWTH)

This register is used to set the pulse width of SYNCOUT output in nanoseconds. When the SYNCOUT signal is used as an interrupt signal, do not change the value after reset. When the signal is used as an external signal, appropriate width must be specified.

Note 1. Always set this register before enabling SYNCOUT signal output.

Address(es): ETHERSW.SWTMWTH A00B F214h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMWTH															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMWTH	SYNCOUT Signal Output Width Setting	Set the pulse width of SYNCOUT output in nanoseconds. The value must be a multiple of 10 ns. The SYNCOUT signal is fixed to 0 in case this register is set to 0h.	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.5.19 Timer Latch Second Register (SWTMLATSEC)

This register is used to latch the IEEE1588 timer value in seconds when the SYNCOUT signal rises. The value is updated whenever the SYNCOUT signal rises.

Address(es): ETHERSW.SWTMLATSEC A00B F22Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMLATSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMLATSEC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMLATSEC	SEC Count Value Latching	Latch the time of rising of SYNCOUT in seconds.	R

29.2.5.20 Timer Latch Nanosecond Register (SWTMLATNS)

This register is used to latch the IEEE1588 timer value in nanoseconds when the SYNCOUT signal rises. The value is updated whenever the SYNCOUT signal rises.

Address(es): ETHERSW.SWTMLATNS A00B F230h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMLATNS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMLATNS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	TMLATNS	ns Count Value Latching	Latch the time of rising of SYNCOUT in nanoseconds.	R

29.2.6 DLR Module Registers

29.2.6.1 DLR Control Register (DLR_CONTROL)

This register is used to set the DLR.

Address(es): ETHERSW.DLR_CONTROL A00C E000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CYCMCLK								—	—	—	BECTIMOUT	—	—	—	DLRENA
Value after reset:	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DLRENA	DLR Setting	Enables or disables the DLR. 0: Disabled 1: Enabled	R/W
b3 to b1	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b4	BECTIMOUT	Beacon Frame Handling	Ignores the beacon frames with invalid timeout timer value. When timeout timer value not within the range of 200 microseconds to 500 milliseconds, the beacon frames will be ignored and parameters will not locally stored. Invalid timeout timer value will always be stored within register INV_TMOUT irrespective of the value of this bit. Ignored frames will be transferred through the hub normally. 0: Not ignored 1: Ignored	R/W
b7 to b5	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b15 to b8	CYCMCLK	Clock Count Setting	Set the number of cycles required for 1 microsecond. The DLR module of this LSI operates at 75 MHz, thus this register must be set to 4Bh. The value after reset needs to be changed.	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.6.2 DLR Status Register (DLR_STATUS)

This register is used to indicate the state of the DLR link node.

Address(es): ETHERSW.DLR_STATUS A00C E004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NETTOPGY								—	—	—	—	—	—	LINSTAP1	LINSTAP0
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	0*1	0*1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CURRSTA								—	—	—	—	—	—	BEAREV1	BEAREV0
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	0	0

x: Undefined

Note 1. When released from the reset state, the latched values of the pin levels of the PHYLINK0 and PHYLINK1 pins are read.

Bit	Symbol	Bit Name	Description	R/W
b0	BEAREV0	Port 0 Beacon Frame Reception Status	Indicates that beacon frames are received from the active supervisor on port 0. 0: No beacon frame received 1: Beacon frame received	R
b1	BEAREV1	Port 1 Beacon Frame Reception Status	Indicates that beacon frames are received from the active supervisor on port 1 0: No beacon frame received 1: Beacon frame received	R
b7 to b2	—	Reserved	When read, an undefined value is read.	R
b15 to b8	CURRSTA	Local Node Status	Indicate current state of local node 0h: IDLE_STATE 1h: NORMAL_STATE 2h: FAULT_STATE Others: Unused	R
b16	LINSTAP0	Port 0 Link Status Indication	Indicates the link status of port 0. 0: Port 0 link is down 1: Port 0 link is up	R
b17	LINSTAP1	Port 1 Link Status Indication	Indicates the link status of port 1. 0: Port 1 link is down 1: Port 1 link is up	R
b23 to b18	—	Reserved	When read, an undefined value is read.	R
b31 to b24	NETTOPGY	Network Topology Indication	Indicate current network topology 0h: Linear topology: when local node is in IDLE state 1h: Ring topology: when local node is not in IDLE state Others: Unused	R

29.2.6.3 DLR Ethernet Type Register (DLR_ETH_TYP)

This register is used to set the Ethernet type for detecting the DLR frame. This value is compared with type field of a received frame to detect DLR frame.

Address(es): ETHERSW.DLR_ETH_TYP A00C E008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ETHTYPDLR															
Value after reset:	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ETHTYPDLR	Ethernet Type Setting	Specify the Ethernet type for DLR frame detection.	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.6.4 DLR Interrupt Control Register (DLR_IRQ_CTRL)

This register is used to control interrupt generation due to the DLR.

Address(es): ETHERSW.DLR_IRQ_CTRL A00C E00Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ATOMICAND	ATOMICOR	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQFRMDSP1	IRQFRMDSP0	IRQBECENA1	IRQBECENA0	IRQINVTMREN	IRQIPADDREN	IRQSUPIGENA	IRQLINKENA1	IRQLINKENA0	IRQSUPENA	IRQBECTOUT1	IRQBECTOUT0	IRQSTOPP1	IRQSTOPP0	IRQFLUENA	IRQCHNGENA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IRQCHNGENA	State Change Interrupt Control	Controls interrupt generation when state change occurs for the local beacon-based DLR ring node. 0: No interrupt is generated. 1: Interrupt is generated. Note: For the interrupt service routine, the beacon frame parameters must be re-read first to clear the bit.	R/W
b1	IRQFLUENA	Learning Table Interrupt Control	Controls interrupt generation when local MAC addresses must be erased from the learning table 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b2	IRQSTOPP0	Port 0 Neighbor Check Timeout Interrupt Control	Controls interrupt generation when neighbor check timeout timer interrupt to port 0 needs to be stopped. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b3	IRQSTOPP1	Port 1 Neighbor Check Timeout Interrupt Control	Controls interrupt generation when neighbor check timeout timer interrupt to port 1 needs to be stopped. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b4	IRQBECTOUT0	Port 0 Beacon Timeout Interrupt Control	Controls interrupt generation when the timeout time for the beacon timeout timer on port 0 has elapsed. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b5	IRQBECTOUT1	Port 1 Beacon Timeout Interrupt Control	Controls interrupt generation when the timeout time for the beacon timeout timer on port 1 has elapsed. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b6	IRQSUPENA	Ring Supervisor Change Interrupt Control	Controls interrupt generation when the ring supervisor changes 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b7	IRQLINKENA0	Port 0 Link Change Interrupt Control	Controls interrupt generation when the link of port 0 changes 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b8	IRQLINKENA1	Port 1 Link Change Interrupt Control	Controls interrupt generation when the link of port 1 changes 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b9	IRQSUPIGENA	Beacon Frame Detection Interrupt Control	Controls interrupt generation when a beacon frame is detected from a ring supervisor with lower priority than that of the current ring supervisor or with a lower MAC address value in case the priority level is the same. 0: No interrupt is generated. 1: Interrupt is generated.	R/W

Bit	Symbol	Bit Name	Description	R/W
b10	IRQIPADDREN	IP Address Change Interrupt Control	Controls interrupt generation when the IP address in a beacon frame output from a ring supervisor changes 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b11	IRQINVTMREN	Beacon Timeout Timer Interrupt Control	Controls interrupt generation when a frame in which beacon timeout timer value is outside of the specified range is detected. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b12	IRQBECENA0	Port 0 Beacon Frame Detection Interrupt Control	Controls interrupt generation when a beacon frame is detected on port 0. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b13	IRQBECENA1	Port 1 Beacon Frame Detection Interrupt Control	Controls interrupt generation when a beacon frame is detected on port 1. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b14	IRQFRMDSP0	Port 0 Frame Discard Interrupt Control	Controls interrupt generation when a frame is discarded due to source address match with the local address on port 0. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b15	IRQFRMDSP1	Port 1 Frame Discard Interrupt Control	Controls interrupt generation when a frame is discarded due to source address match with the local address on port 1. 0: No interrupt is generated. 1: Interrupt is generated.	R/W
b29 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W
b30	ATOMICOR	Register Write OR Operation Setting	When writing to the register, the logical OR of the values for the bits corresponding to enable bits of this register and the value of this bit is taken and the result is written to the register. 0: Normal write operation 1: All bits are set to 1	R/W
b31	ATOMICAND	Register Write AND Operation Setting	When writing to the register, the logical AND of the values for the bits corresponding to enable bits of this register and the value of this bit is taken the result is written to the register. 0: All bits are cleared to 0. 1: Normal write operation	R/W

29.2.6.5 DLR Interrupt Status/ACK Register (DLR_IRQ_STAT_ACK)

This register is used to indicate the status of DLR interrupts.
The status can be checked by reading the register: 1 indicates that an event has occurred whereas 0 indicates that no event has occurred.
Writing 1 to the register clears the interrupt and the bit value.

Address(es): ETHERSW.DLR_IRQ_STAT_ACK A00C E010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FRMDISP1	FRMDISP0	BECFRAP1	BECFRAP0	INVTMR	IPCHANEVET	SUPIGNBEC	LINKSTAP1	LINKSTAP0	SUPRCHAG	BECTMRP1	BECTMRP0	STOPNBCHK1	STOPNBCHK0	FLUEVENT	STACHANGE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	STACHANGE	DLR Ring Node Status	Indicates that the state of local beacon-based DLR node has changed.	R/W
b1	FLUEVENT	Local MAC Address Event	Indicates that local MAC addresses need to be erased from the learning table.	R/W
b2	STOPNBCHK0	Port 0 Neighbor Check Timeout Timer Event	Indicates that the neighbor check timeout timer needs to be stopped on port 0.	R/W
b3	STOPNBCHK1	Port 1 Neighbor Check Timeout Timer Event	Indicates that the neighbor check timeout timer needs to be stopped on port 1.	R/W
b4	BECTMRP0	Port 0 Beacon Timeout Timer Status	Indicates that the timeout time for the beacon timeout timer on port 0 has elapsed.	R/W
b5	BECTMRP1	Port 1 Beacon Timeout Timer Status	Indicates that the timeout time for the beacon timeout timer on port 1 has elapsed.	R/W
b6	SUPRCHAG	Ring Supervisor Change Status	Indicates that when the ring supervisor has been changed.	R/W
b7	LINKSTAP0	Port 0 Link State Status	Indicates that the state of link has changed on port 0.	R/W
b8	LINKSTAP1	Port 1 Link State Status	Indicates that the state of link has changed on port 1.	R/W
b9	SUPIGNBEC	Beacon Frame Detection Indication	Indicates that a beacon frame has been detected from a supervisor with lower priority or with lower value of the MAC address in case the priority level is the same.	R/W
b10	IPCHANEVET	IP Address Change Indication	Indicates that the IP address in the beacon frame output from the ring supervisor has been changed.	R/W
b11	INVTMR	Beacon Timeout Timer Status	Indicates that the beacon timeout timer has detected a frame with a value outside of the specified range.	R/W
b12	BECFRAP0	Port 0 Beacon Frame Status	Indicates that the beacon frame has been detected on port 0.	R/W
b13	BECFRAP1	Port 1 Beacon Frame Status	Indicates that the beacon frame has been detected on port 1.	R/W
b14	FRMDISP0	Port 0 Frame Status	Indicates that a frame has been discarded due to source address match with the local address on port 0.	R/W
b15	FRMDISP1	Port 1 Frame Status	Indicates that a frame has been discarded due to source address match with the local address on port 1.	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

Note: When any event described above happens, the corresponding bit is latched to 1, regardless of the DLR_IRQ_CONTROL register setting.

29.2.6.6 DLR Local MAC Address Low Register (LOC_MAClo)

This register is used to specify the local MAC address to be used in loop filter. The first 4 octets of the local MAC address and the remaining 2 octets are set to the LOC_MAClo register and LOC_MAChi register respectively.

Address(es): ETHERSW.LOC_MAClo A00C E014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MACADD4								MACADD3							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD2								MACADD1							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD1	Local MAC Address First Byte Setting	Specify the 1st byte of local MAC address	R/W
b15 to b8	MACADD2	Local MAC Address Second Byte Setting	Specify the 2nd byte of local MAC address	R/W
b23 to b16	MACADD3	Local MAC Address Third Byte Setting	Specify the 3rd byte of local MAC address	R/W
b31 to b24	MACADD4	Local MAC Address Fourth Byte Setting	Specify the 4th byte of local MAC address	R/W

29.2.6.7 DLR Local Mac Address High Register (LOC_MAChi)

This register is used to specify the local MAC address to be used in the loop filter. The first 4 octets of the local MAC address and the remaining 2 octets are set to LOC_MAClo register and LOC_MAChi register respectively.

Address(es): ETHERSW.LOC_MAChi A00C E018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD6								MACADD5							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD5	Local MAC Address Fifth Byte Setting	Specify the 5th byte of local MAC address	R/W
b15 to b8	MACADD6	Local MAC Address Sixth Byte Setting	Specify the 6th byte of local MAC address	R/W
b31 to b16	—	Reserved	The read value is undefined. When writing, write 0.	R/W

29.2.6.8 DLR Supervisor MAC Address Low Register (SUPR_MAClo)

This register is used to indicate the first 4 octets of the active ring supervisor's MAC address extracted from the destination address field of the beacon frame.

Address(es): ETHERSW.SUPR_MAClo A00C E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MACADD4								MACADD3							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD2								MACADD1							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD1	Active Ring Supervisor MAC Address First Byte Setting	Indicate the 1st byte of active ring supervisor's MAC address	R
b15 to b8	MACADD2	Active Ring Supervisor MAC Address Second Byte Setting	Indicate the 2nd byte of active ring supervisor's MAC address	R
b23 to b16	MACADD3	Active Ring Supervisor MAC Address Third Byte Setting	Indicate the 3rd byte of active ring supervisor's MAC address	R
b31 to b24	MACADD4	Active Ring Supervisor MAC Address Fourth Byte Setting	Indicate the 4th byte of active ring supervisor's MAC address	R

29.2.6.9 DLR Supervisor MAC Address High Register (SUPR_MAChi)

This register is used to indicate the remaining 2 octets of the active ring supervisor's MAC address extracted from the destination address field of the beacon frame as well as priority order of the supervisor.

Address(es): ETHERSW.SUPR_MAChi A00C E024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SUPRPRE							
Value after reset:	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MACADD6								MACADD5							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	MACADD5	Active Ring Supervisor MAC Address Fifth Byte Setting	Indicate the 5th byte of active ring supervisor's MAC address	R
b15 to b8	MACADD6	Active Ring Supervisor MAC Address Sixth Byte Setting	Indicate the 6th byte of active ring supervisor's MAC address	R
b23 to b16	SUPRPRE	Ring Supervisor Priority Order Value Indication	Indicate priority of the ring supervisor.	R
b31 to b24	—	Reserved	When read, an undefined value is read.	R

29.2.6.10 DLR Ring Status/VLAN Register (STATE_VLAN)

This register is used to indicate the ring state of the DLR and VLAN ID that are extracted from the ring state field and VLAN control information field of the beacon frame.

Address(es): ETHERSW.STATE_VLAN A00C E028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	VLANCI															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VLANVALID	RINGSTATE							
Value after reset:	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RINGSTATE	DLR Ring Status	Indicate DLR ring state extracted from the ring state field of the beacon frame. 1h: RING_NORMAL_STATE 2h: RING_FAULT_STATE Others: Unused	R
b8	VLANVALID	VLAN Status	Indicates that VLAN is enabled. When asserted, the VLANCI contains valid VLAN ID. 0: Invalid 1: Valid	R
b15 to b9	—	Reserved	When read, an undefined value is read.	R
b31 to b16	VLANCI	VLAN Tag Control Field Indication	Indicate the 802.1Q VLAN tag control field extracted from the VLAN information field of the beacon frame. VLAN ID of the DLR is included.	R

29.2.6.11 DLR Beacon Timeout Register (BEC_TMOUT)

This register is used to indicate the beacon timeout timer value extracted from the beacon timeout field of the beacon frame.

Address(es): ETHERSW.BEC_TMOUT A00C E02Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BECTMOUT															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BECTMOUT															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	BECTMOUT	Beacon Timeout Timer Indication	Indicate beacon timeout timer value in microseconds (µs). Invalid timeout timer values will be not written to this register when bit 4 of register DLR_CONTROL (BECTIMOUT bit) is set to 1. State transition will not be considered. Normal expected value is in the range between 200 microseconds and 500 milliseconds. Typical value is 1960 microseconds.	R

29.2.6.12 DLR Beacon Interval Register (BEC_INTRVL)

This register is used to indicate the beacon frame interval extracted from the beacon interval field of the beacon frame.

Address(es): ETHERSW.BEC_INTRVL A00C E030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BECINTVAL															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BECINTVAL															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	BECINTVAL	Beacon Frame Interval Indication	Indicate beacon frame interval in microseconds (µ sec). Expected value is in the range between 100 microseconds and 100 milliseconds. Typical value is 400 microseconds.	R

29.2.6.13 DLR Supervisor IP Address Register (SUPR_IPADR)

This register is used to indicate the ring supervisor's IP address extracted from the source IP address field of the beacon frame.

Address(es): ETHERSW.SUPR_IPADR A00C E034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SPVIP															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SPVIP															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SPVIP	Ring Supervisor IP Address Indication	Indicate the ring supervisor's IP address A value of 0h is received when the supervisor has no IP address.	R

29.2.6.14 DLR Sub Type/Protocol Version Register (ETH_STYP_VER)

This register is used to indicate DLR message information extracted from the corresponding field in the beacon frame.

Address(es): ETHERSW.ETH_STYP_VER A00C E038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SOURP							
Value after reset:	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DLRRINGVER								DLRRINGTPY							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	DLRRINGTPY	Ring Sub Type Indication	Indicate ring sub type of the DLR message. The value is expected to be 02h.	R
b15 to b8	DLRRINGVER	Ring Protocol Version Indication	Indicate ring protocol version of the DLR message. The value is expected to be 01h.	R
b23 to b16	SOURP	Transmit Source Port Indicator	Indicate transmit source port of the DLR message. The value is expected to be 00h.	R
b31 to b24	—	Reserved	When read, an undefined value is read.	R

29.2.6.15 DLR Beacon Timeout Timer Register (INV_TMOUT)

This register is used to indicate a timeout timer value outside of the specified range. When an invalid beacon frame with a timeout timer value outside of the range is received, such timeout value is extracted from the beacon frame and stored in the register.

Address(es): ETHERSW.INV_TMOUT A00C E03Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	INVBECTMOUT															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	INVBECTMOUT															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	INVBECTMOUT	Timeout Timer Value Indication	Indicate a beacon timeout timer value of the frame with invalid timeout timer value outside of the specified range in microseconds (μ sec). The target is outside of the valid range between 200 microseconds and 500 milliseconds. This register will be always overwritten whenever a new frame with an invalid value is received. The value contained in the register is valid when bit 11 of register IRQ_STAT_ACK is asserted to 1.	R

29.2.6.16 DLR Sequence ID Register (SEQ_ID)

This register is used to indicate the sequence ID of the beacon frame extracted from the sequence ID field of the beacon frame.

Address(es): ETHERSW.SEQ_ID A00C E040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SEQID															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SEQID															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	SEQID	Sequence ID Indication	Indicate the sequence ID of the last beacon frame received on port 0 or port 1. When a frame is ignored due to an invalid timeout timer value, the sequence ID of the ignored frame is not stored.	R

29.2.6.17 DLR MAC Statistics Counters

This LSI stores statistics of the beacon frame to be processed by the DLR module in the following registers.
All registers are 32-bit, read only and the initial value is 0000 0000h.

Address	Symbol	Description
A00C E060h + 0010h*n	RX_STATn	Number of beacon frames received on port n: The counter will increment with the beacon frames which match the destination address, Ether type, DLR frame type and CRC, and will not with type mismatch. The counter is cleared if the DLR module is disabled.
A00C E064h + 0010h*n	RX_ERR_STATn	Number of beacon frames received with CRC error on port n: The counter will increment with the beacon frames which match the destination address, Ether type, DLR frame type but with CRC error. The counter is cleared if the DLR module is disabled.
A00C E068h + 0010h*n	TX_STATn	Number of beacon frames forwarded through the hub from port n to port m: The counter is cleared if the DLR module is disabled.

n = 0, 1

n = 0: MAC port 0, n = 1: MAC port 1

m = 1 when n = 0, m = 0 when n = 1

29.3 Functional Description

29.3.1 Switching Engine

29.3.1.1 Overview

The Ethernet switch incorporates the following main functions:

- Input frame parsing and priority extraction
- Output port(s) judgment
- Frame queuing
- Output queue scheduling

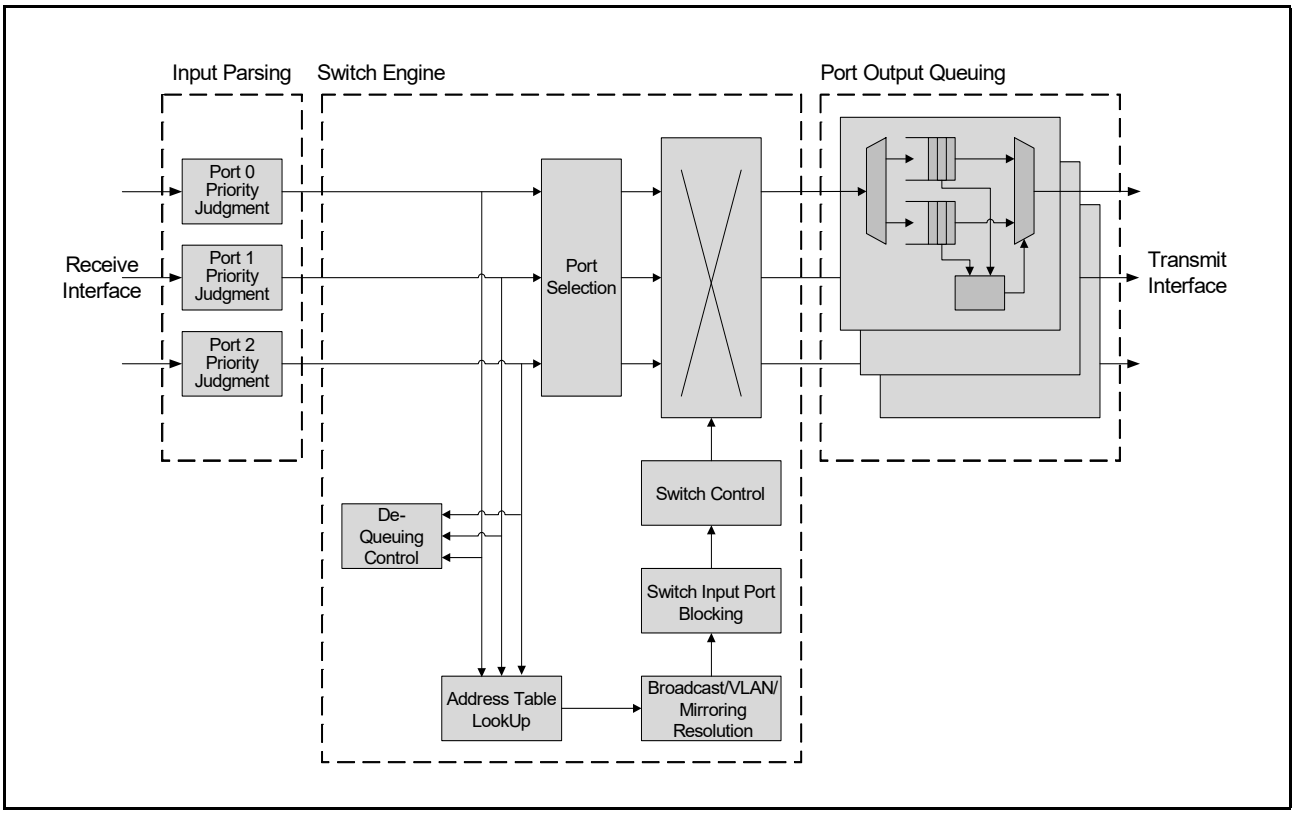


Figure 29.4 Switching Engine Overview

29.3.1.2 Frame Classification and Priority Processing

(1) Overview

When a frame is received on an input port, several pieces of information are extracted from the frame as the Ethernet MAC address, VLAN tag, and IP Headers to determine the frame type and classify the types.
The frame is classified with up to 8 different priorities (for VLAN) which can be remapped into any output priority. The frame is stored in the corresponding queue on the output port. If a frame is classified to a higher priority than available output queues of a port, it is stored into the queue with the highest priority.

(2) VLAN Priority Look-Up

On each port, an 8 entry programmable priority table is implemented. The registers VLAN_PRIORITYn contain the priority mapping for port n (n = 0 to 2). The function uses the 3-bit VLAN priority and maps it to the final priority.
The index in the mapping table consists of 3 bits (bit 7 to 5) of the first octet of the VLAN tag data with bit 5 as the LSB and bit 7 as the MSB.
Mapped value has 4 priorities. A value of 0 is interpreted as the lowest priority. A value of 3 is interpreted as the highest priority.

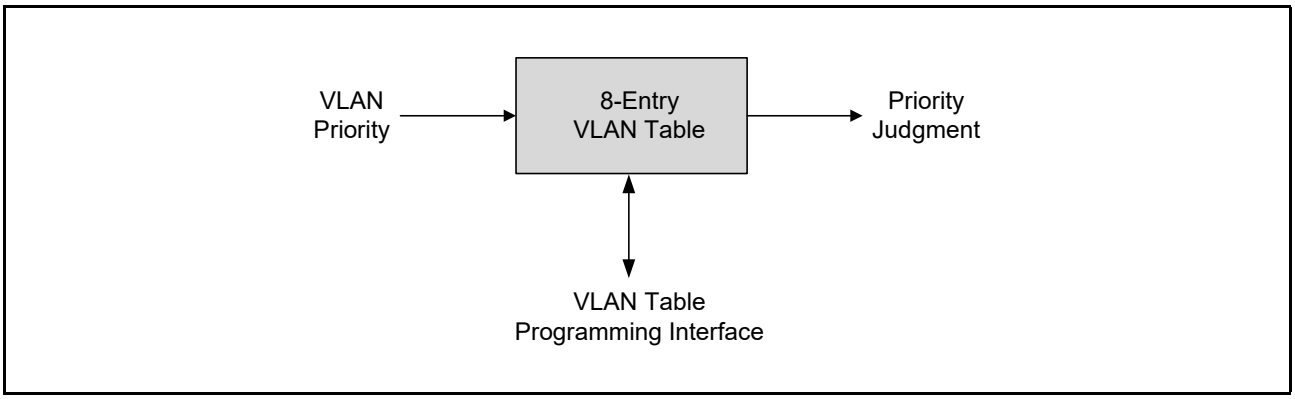


Figure 29.5 VLAN Priority Table Overview

(3) IPv4 and IPv6 Priority Look Up

The switch can classify priorities of both IPv4 and IPv6 frames: A 64-entry table is implemented per port to classify the IPv4 frames and a 256-entry table is implemented per port to classify IPv6 frames. The look-up table is set through the IP_PRIORITYn register.
On the IPv4 COS table entry, the 6-bit DiffServ field is provided as input and the table returns the 2-bit priority information.
On the IPv6 COS table entry, the 8-bit Class of Service field is provided as input and the table returns the 2-bit priority information.

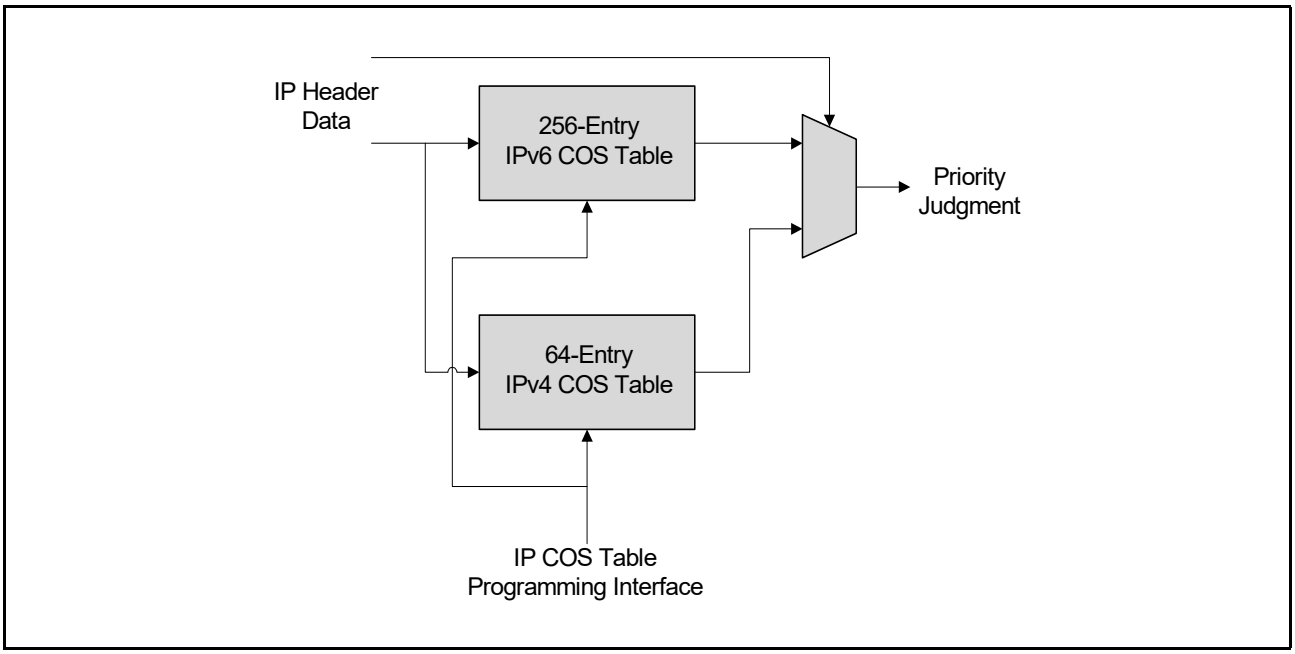


Figure 29.6 IP COS Tables Overview

(4) Priority Judgment

Priority can be judged on each port independently by programming registers PRIORITY_CFGn to enable or disable priority classification based on VLAN, IP, or MAC address.
The priority is judged according to the rules below depending on enabled classification method and fields found in the frame:

(1) When priority judgment by IP classification is enabled and an the IP header is found, priority is mapped by register IP_PRIORITYn.
(2) If not (1) above, when priority judgment by VLAN_PRIORITY is enabled and a VLAN tag is found, priority is mapped by register VLAN_PRIORITYn.
(3) If neither of (1) or (2) above, the default priority specified in register PRIORITY_CFG is used.

29.3.1.3 Input Port Selection

The port selection circuit constantly checks all input ports by polling for available data. If any data is available, a port is selected and frame data is read from the port. After one frame has been read, another port is selected, even if further data is available on the current port.
This means for the application on a port FIFO input interface (e.g MAC), that it is not allowed to perform consecutive frame transfers to the switch. Instead the application must wait for a new selection after one frame has been transferred.

29.3.1.4 Layer 2 Look Up Engine

(1) Overview

A hash code is calculated by using the frame destination MAC address. It is used as an entry (address) to a table, which contains MAC addresses, destination port number, and validity information for each hash value.
As one hash code value can represent multiple MAC address, the memory implements for each pointer, up to eight MAC address entries (8-entry block), which are searched linearly.

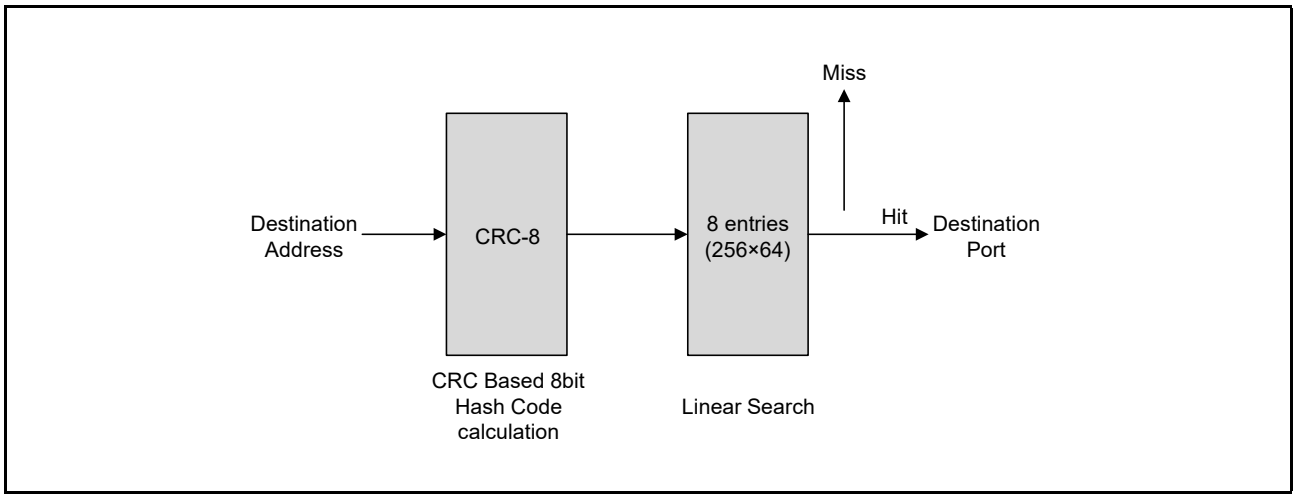


Figure 29.7 Port Look-Up Overview

(2) Hash Code

A MAC address table with up to 2048 entries is used in calculating 8-bit hash values from the least significant 24 bits (or all 48 bits) of the MAC addresses. The hash codes are calculated by using a CRC-8 polynomial: $x^8 + x^2 + x + 1$ (07h)
The 8-bit CRC is used also for all smaller address tables down to 256 entries. In this case, every hash value directly points to one entry in the memory and the 8-entry blocks overlap.
Note: The address table size of this LSI is 256 entries.

(3) Address Table

The address table is divided into blocks. Each block contains 8 records, which contain 64-bit of information each. Each record contains the 48-bit MAC address and provides the necessary forwarding information as well as priority or time stamp information. The start address of such an 8-entry block is defined by the hash value calculated from the MAC address. Two types of records are defined.

- Dynamic Record: The dynamic entry provides the MAC address together with a 10-bit timestamp and destination port number. These entries are created by the learning function based on received frames and this enables forwarding of frames to specific ports. Dynamic entries are deleted by aging function if not updated.
- Static Multiport/Priority Record: static entries can be written in the address table and include priority information as well as multiple destination port numbers (port bit mask). The MAC address can be unicast or multicast. These records can be used to e.g. specify the ports to participate in a specific multicast domain or to assign a MAC address-based priority to a frame. The aging and learning functions ignore static records.

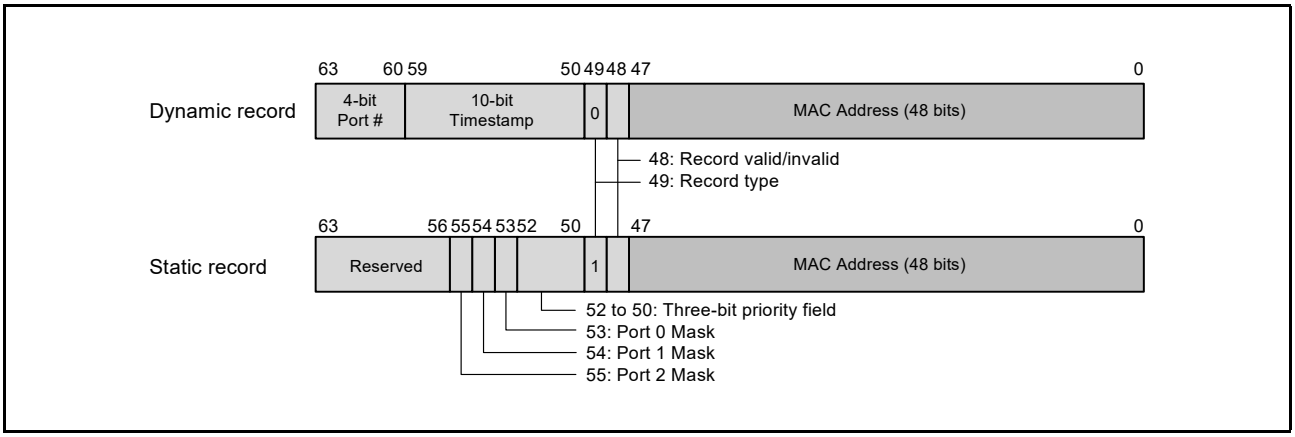


Figure 29.8 Record Types of Address Table

Bit 49 of the record indicates the type of records in the table.
The value 0 indicates that the entry is dynamic, so the higher-order bits of the record will consist of a 10-bit timestamp and 4-bit port number.
The value 1 indicates that the entry is static and has a 3-bit priority field and 3-bit port bit masks. Of the port bit masks, bits 53, 54, and 55 of the record correspond to ports 0, 1, and 2 (the internal port). The frame will be forwarded to each of the ports for which the value of the bit mask is 1. However, a frame is never forwarded to the source port even if the value of its port bit mask is 1.

29.3.1.5 Learning Interface

The learning interface provides to software the information required to build the look-up tables. The interface implements a FIFO buffer that stores multiple entries.

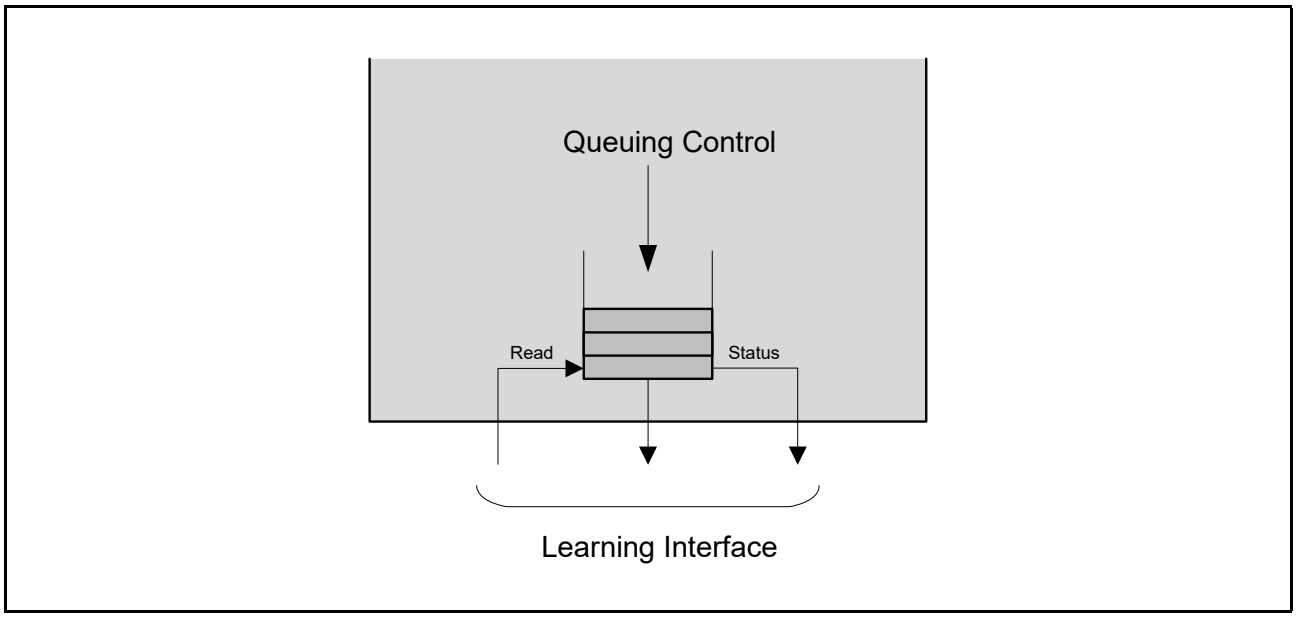


Figure 29.9 Learning Interface Overview

For each frame received by the switch, two 32-bit records (records A and B) are written in the FIFO, record A is written first, then record B.
Records A and B include the MAC address of frame transmit source, 8-bit hash code calculated based on the address, and port number of the transmission source. For the MAC address, the 1st octet is in bits 7:0 of the record A, and 6th octet is in bits 15:8 of the record B.

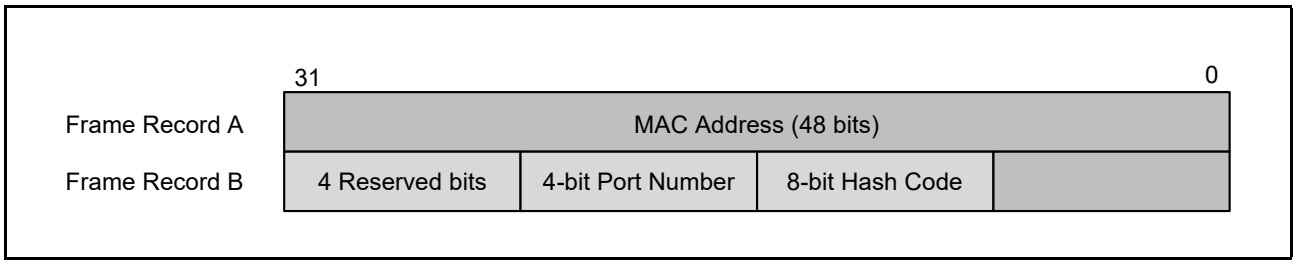


Figure 29.10 Format of Records

Software can read the records through registers LRN_REC_A and LRN_REC_B.

29.3.1.6 Frame Forwarding Tasks

(1) Overview

When a frame is processed, its 48-bit source and destination MAC addresses are extracted. The address table is searched for the destination MAC address. The following rules apply in the order from top to bottom:

(1) If the destination address is found, the frame is forwarded to the port(s) given by the address table entry.
(2) When (1) is not satisfied, but if the destination address is a unicast frame, the frame is forwarded to all ports identified by register UCAST_DEFAULT_MASK.
(3) When (1) is not satisfied, but if the destination address is a broadcast frame, the frame is forwarded to all ports identified by register BCAST_DEFAULT_MASK.
(4) When (1) is not satisfied, but if the destination address is a multicast frame, the frame is forwarded to all ports identified by register MCAST_DEFAULT_MASK.
(5) When (1) to (4) are not satisfied, the frame is forwarded to all ports identified by register BCAST_DEFAULT_MASK.

Note that the address table can hold static entries, and multicast addresses can be registered to static entries. Therefore, specific multicast addresses can be forwarded by using static entries without setting register MCAST_DEFAULT_MASK.

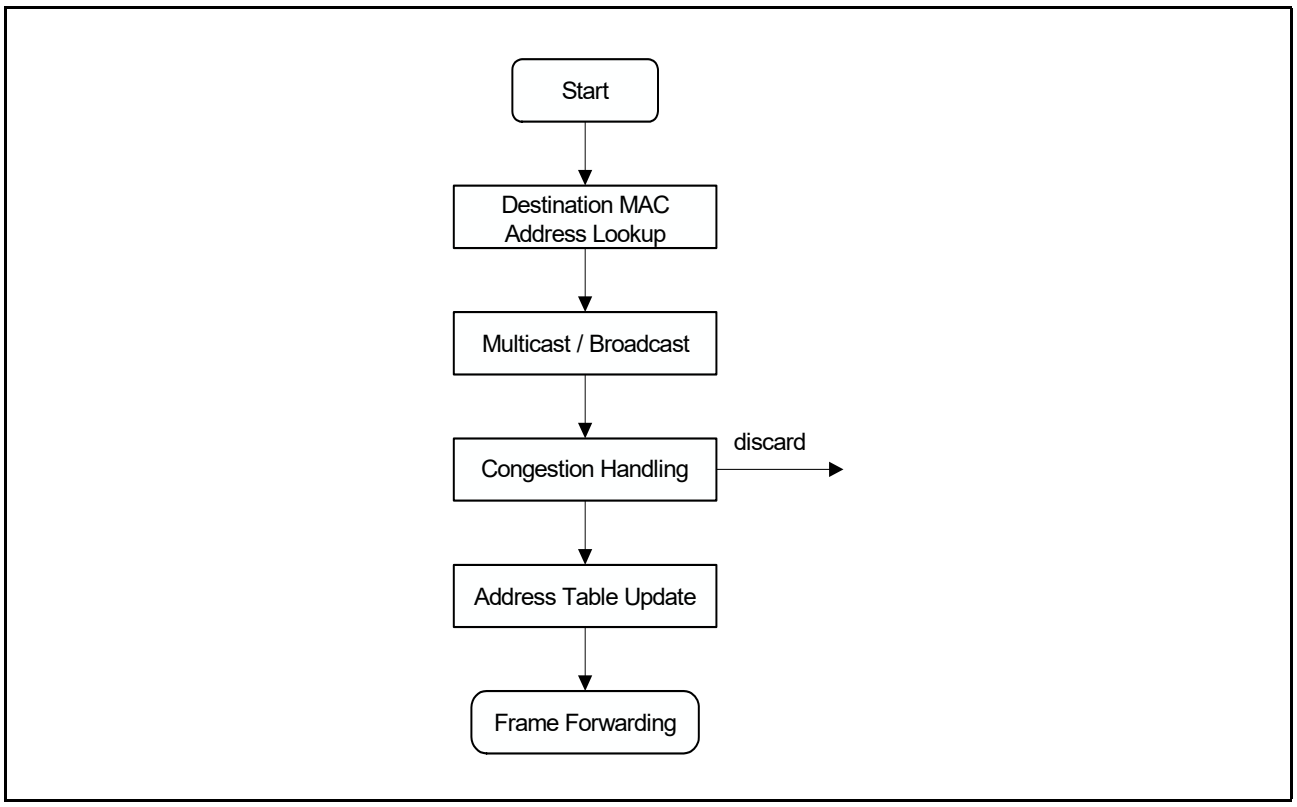


Figure 29.11 Frame Forwarding Tasks Overview

(2) Congestion Handling

(a) Overview

The congestion handling function is used whenever an output port is not available and data needs to be sent to the port. “Available” is defined as a state if the port is enabled through the PORT_ENA register and the corresponding output queue has enough room to store a full sized frame. In congestion handling, the frame should be processed further or discarded according to the following rules:

(b) Single Destination (one input to one output)

If the output port is enabled and can accept a frame, the frame will be forwarded normally. In any other case, the frame will be discarded.

(c) Multiple Destinations (Flooding)

After broadcast, multicast, or flooding handling, a frame needs to be forwarded to multiple output ports.

- Output disabled:
  All disabled ports are removed from the list of outputs.
- Output congested:
  If any of the output ports cannot accept a frame (as indicated by the output queue management for the port) due to output congestion, the port is removed from the list of outputs.

After the removal of the output list, if no available output port is left in the list, if the frame is read from the input and discarded. The port's corresponding discard counter (ODISCn) is incremented.

(3) Bridge Protocol Frame Handling

To implement bridge control protocols like the spanning tree protocol, the following control functions are performed by protocol frame handling function:

(a) Input Port Blocking

Input port blocking function is used to avoid forwarding of frames after address learning. Enabling or disabling of the function can be set through the INPUT_LEARN_BLOCK register. If a frame is received on a port which should block and the frame is not a bridge protocol frame, the frame will be targeted for discard and will not be forwarded to any output port.

(b) Input Port Learning Disabling

To reduce processing load of software, a port can be configured for exclusion from learning (see the INPUT_LEARN_BLOCK register). When learning is disabled on a port, no source address is extracted for incoming frames. BPDU frames, as exception, the source addresses are always extracted and forwarded to the learning interface.

(c) Management Port (Internal Port) Forwarding

When bit 6 of the MGMT_CONFIG register is enabled, the bridge protocol frames are always forwarded to the management port (internal port), independent of any address lookup or other handling functions.
The bridge protocol frames are identified by its destination address of the following:

- 01-80-c2-00-00-00 to 01-80-c2-00-00-0F (Spanning Tree, IEEE 802.1d)
- 01-80-c2-00-00-10 (Bridge Management Address, 802.1d)
- 01-80-c2-00-00-20 to 01-80-c2-00-00-2F (Generic Attribute Registration Protocol, 802.1d)

(d) Management Frame Forwarding

If the management port (internal port) transmits frames, they are forwarded according to the port mask settings of bits 17 and 16 configured in register MGMT_CONFIG. A handshaking mechanism is implemented (bit 5 in register MGMT_CONFIG) that can be used to change the port mask configuration on a frame-by-frame basis for management frames.

(4) Forced Forwarding

The switch has the capability to disable the forwarding method specified by the forwarding processing and to forward a frame to a specific port forcibly. This is typically used for management frames that use multicast addresses but still need to be forwarded only to specific output ports.
Depending on the switch application, two methods exist:

- When a BPDU is forwarded, the mask defined in the MGMT_CONFIG register can be used. The application needs to set the register prior to transferring the BPDU frame to the switch. Afterwards, bit 5 that notifies completion of the transfer is set, the port mask can be cleared.
- Forced forwarding can be set per frame by using the management tag which can be used between the internal port and the Ethernet switch. This is the preferred method as it does not need any handshaking with the MGMT_CONFIG register.

A difference between two methods above is target frames for forced forwarding: the former is only for BPDU frames and the latter is for all frames.

Note: For forced forwarding by the management tag, bits 17 and 16 in MGMT_CONFIG must always be set to 0. Otherwise, the setting of the management tag will be overwritten due to precedence of the setting of MGMT_CONFIG.

29.3.1.7 Output Frame Queuing

(1) Overview

The memory controller implements a shared memory architecture to store frames of arbitrary size for multiple output ports.
Each output port can have multiple (up to 4) priority queues. The memory controller offers a single write input port (write port) and multiple output ports with the capability to perform virtual frame duplication on the output ports (multiple read ports).
A single large memory is partitioned in small cells to efficiently share the available memory for small and large frames without leaving large unused space when storing small frames.

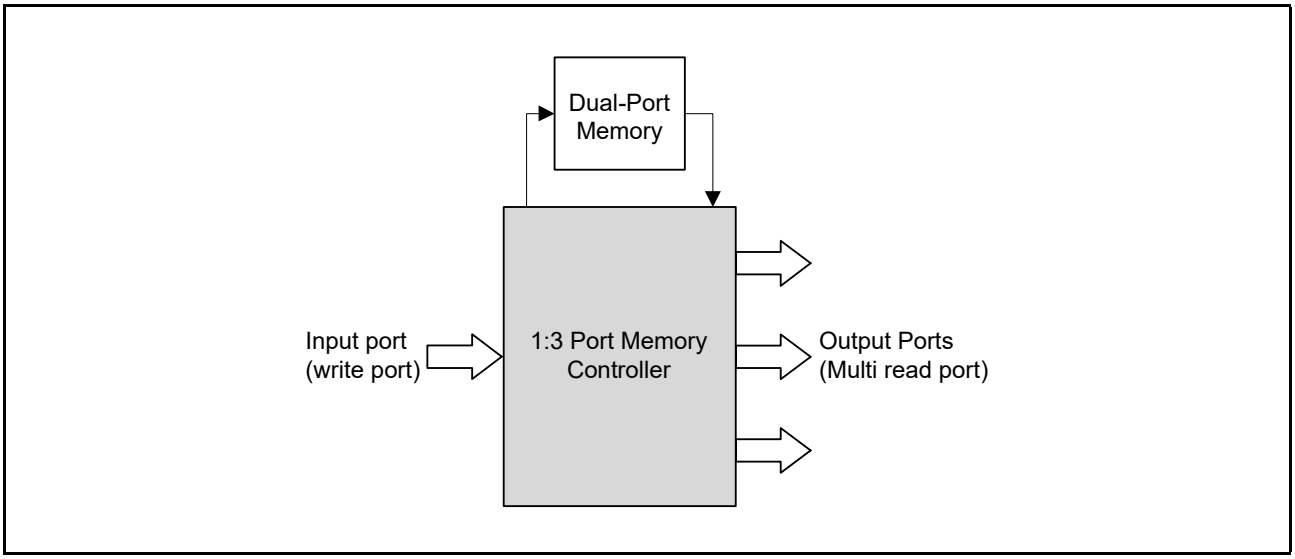


Figure 29.12 Overview of Output Port Memory Controller

(2) Functions

- Memory controller with single write port and multiple read ports
- Shared memory (8 Kbytes) partitioned in 256-byte cells
- Simultaneous write to multiple destinations during writing to memory from input port (virtual frame duplication)
- Multiple read ports using time-division multiplexing for simultaneous output serving to multiple output ports
- Multiple queues (4 stages) per output port
- Function to use congestion information for protection of backpressure and overflow
- Memory status statistics

(3) Implementation

The memory manager implements a shared 8-Kbyte storage for all queues on output ports 0 and 1 only. Port 2 (internal port) has a single FIFO queue, which operates independently of the shared memory. Therefore, even if the local port is congested due to slow processing by software, the forwarding between ports 0 and 1 is not affected.

29.3.2 Hub Module for Cut-Through

The Ethernet switch incorporates hub module for cut-through. This module enables high-speed frame transfer without using the switch engine between port 0 and port 1.
The hub module operates between the MAC and PHY at the MII level. The hub can operate on packets coming from both port 0 and port 1, or only one port. When the hub is enabled for only one port, in one direction cut-through can occur while store and forward is implemented in the other direction. The direction and enabling/disabling of the hub module can be controlled by software.
When the hub module is enabled, all frames received are immediately forwarded to the opposite port before the frame has been received (cut-through transfer). The filters in the module can be configured to avoid cut-through forwarding for specific management frames that must always be routed through the switch with the normal store and forward behavior.

29.3.2.1 Operation of Normal Switch Mode

In normal switching mode, the MAC is directly connected to the Ethernet PHY and data are transmitted and received in the switch. The switch engine is responsible for forwarding all frames between the individual ports.

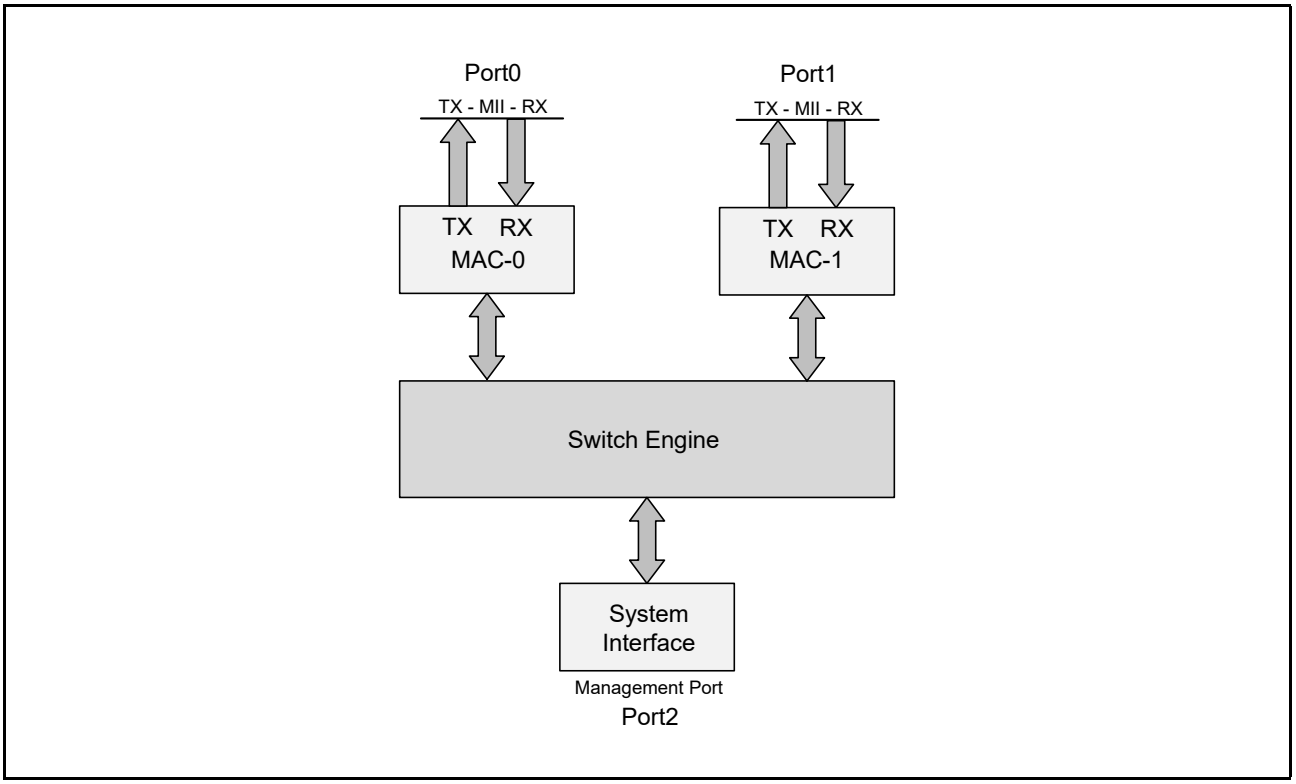


Figure 29.13 Normal Operation of Switch Mode

29.3.2.2 Hub Mode from Port 0 to Port 1

When hub mode is active in the direction from port 0 to port 1, the datapathes are changed at the PHY interface level as follows:

- The port 0 receive interface is connected to both the switch and the hub receive sides. The hub will transmit received frames to the port 1 transmit interface. A filtering mechanism is implemented to avoid frame duplication.
- The switch can transmit frames to port 0 normally and will continue to receive all traffic from port 0.
- The switch will receive frames from port 1 normally.
- For transmission to port 1 by the switch, it is necessary to avoid frame duplication as it must be ensured that it does not repeat frames that were already forwarded or are queued for transmission through the hub. The address filter table is used for this purpose.
- IEEE 1588 frames must never pass through the hub to ensure proper operation of the protocol (correction field updates).

When the hub mode is active in the direction from port 0 to port 1, the datapathes are changed at the PHY interface level as follows:
Even when hub mode is enabled, the frame received is transmitted to the switch and its transfer method of the frame will be determined in the switch. However, in case forwarding takes place to the same port as the port to which the hub already transmitted, the frame is discarded. Data transfer to the internal port (port 2) can occur. A FIFO is used for arbitration of frames transmitted from both the switch and the hub.

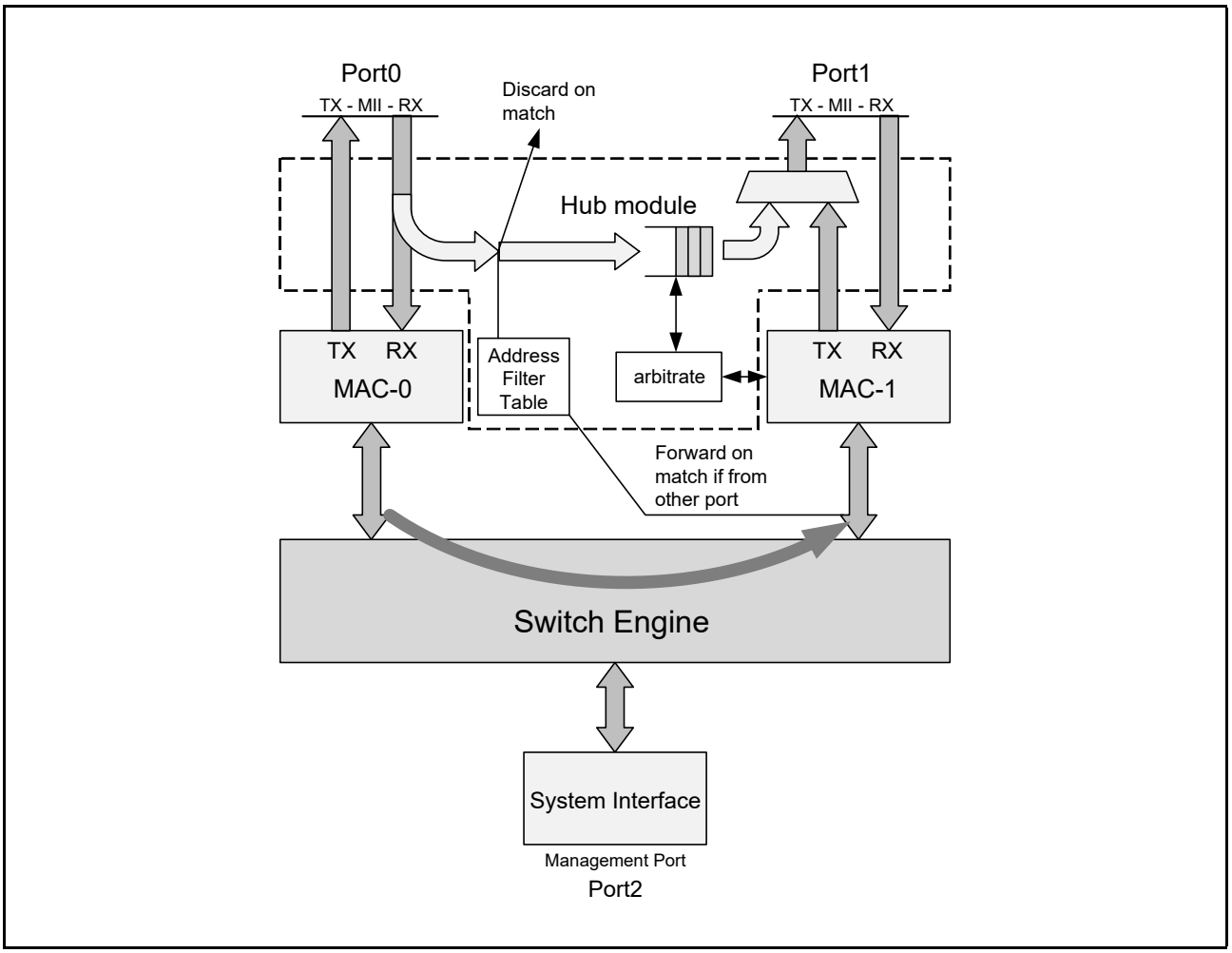


Figure 29.14 Hub Mode from Port 0 to Port 1

29.3.2.3 Hub Mode from Port 1 to Port 0

When the hub mode is enabled in the direction from port 1 to port 0, the datapathes are changed at the PHY interface level to receive from port 1 and transmit to port 0 directly. Now the transmission from both the switch and the hub to port 0 is arbitrated. The operation is the same as that of the hub mode in the direction from port 0 to port 1.
Note that both directions can be enabled separately and also both can be enabled at the same time.

29.3.2.4 Hub Receive Filtering

When the hub mode is enabled, the hub receive interface must not forward the following frames through the hub:

- Frames having a unicast MAC destination address matching the local system's unicast MAC address
- IEEE 1588 frames
- Any local management frames (e.g. MAC pause frames) that should not be transmitted through a switch

The hub receive filter operates on MAC destination addresses. Up to 7 addresses can be registered for filtering with the ability to use a mask on the last byte to cover address ranges and to perform forced forwarding instead of filtering (see sections of the HUB_FLT_MACnlo and HUB_FLT_MACnhi registers).
Forwarding operation of the hub and switch differs due to the setting of the filter.

Table 29.2 Operations of the Hub and Switch by Filter Settings

Forced Forwarding		**Disabled**		**Enabled*1**	
Address Match/Mismatch		**Match**	**Mismatch**	**Match**	**Mismatch**
Hub function enabled	Hub	Not forward	Cut-through	Cut-through	Filter behavior of invalid forced forwarding
	Switch	Store and forward*2	Not forward	—*3	
Hub function disabled	Hub	Not forward	Not forward	Cut-through	
	Switch	Store and forward*2	Store and forward*2	—*3	

Note 1. Use of the DLR for beacon frames is assumed.
Note 2. Forwarding frames between the PHY ports. May not be forwarded, depending on the settings of the address table and the default mask.
Note 3. Frames will be discarded before they enter the switch.

- When frame forced forwarding is disabled

When the destination address of a received frame matches with the one registered in the filter, the hub does not forward the frame to other port. When transfer between port 0 and port 1 in the switch occurs, the hub forwards the frame to the other port.
When the destination address of a received frame does not match with the one registered in the filter, the hub forwards the frame to the other port. On the other hand, the switch does not forward the frame to other port. This prevents any frame duplication.

- When frame forced forwarding is enabled

When the destination address of a received frame matches with the one registered in the filter and even when the hub mode is disabled, the hub always forwards the frame to other port. Generally, forced forwarding is applied to the beacon frames. When DLR mode is enabled, the DLR module can process the beacon frame, but the frame is discarded before acquiring by the switch. This prevents any frame duplication.

The management port (port 2) is not affected by any frame filtering and will always receive frames from both MAC ports.
The system must set up the filter address to contain the local system unicast MAC address as well as any destination (multicast) addresses of the IEEE 1588 frames and of the frames that should not be forwarded through the hub with forced forwarding bit disabled. The following tables give typical examples of relevant addresses. For the details, see relevant specifications.

Table 29.3 PTPv2 Multicast Domains for Layer 2

Name	MAC Address Mapping
Normal messages	01-1b-19-00-00-00
Peer delay messages	01-80-c2-00-00-0e

Table 29.4 PTP Multicast Domains for UDP/IP

Name	IP Address	MAC Address Mapping
Default PTP domain	224.0.1.129	01-00-5e-00-01-81
Alternate PTP domain1	224.0.1.130	01-00-5e-00-01-82
Alternate PTP domain2	224.0.1.131	01-00-5e-00-01-83
Alternate PTP domain3	224.0.1.132	01-00-5e-00-01-84

Table 29.5 Management Frame Domains

Name	IP Address	MAC Address Mapping Mapping
Generic Switch Management	224.0.0.0	01-00-5e-00-00-00
IGMP	224.0.0.1	01-00-5e-00-00-01

Table 29.6 Switch Management Frame Domains

Name	MAC Address Mapping
Spanning Tree, IEEE 802.1d	01-80-c2-00-00-00 to 01-80-c2-00-00-0F
Bridge Management Address, 802.1d	01-80-c2-00-00-10
GARP	01-80-c2-00-00-20 to 01-80-c2-00-00-2F
MAC Layer Control Frames (Pause)	01-80-c2-00-00-01

Table 29.7 DLR Multicast Domains

Name	MAC Address Mapping
Beacon Frame	01-21-6C-00-00-01
Neighbor Check Request, Neighbor Check Response, Sign ON	01-21-6C-00-00-02
Announce, Locate Fault	01-21-6C-00-00-03

Based on the above, filter initialization for the hub module should cover at least the addresses listed in Table 29.8.
The address and mask values are programmed using the HUB_FLT_MACnlo and HUB_FLT_MACnhi registers. Note that the first byte of the MAC address must be set in bits 7 to 0 of the HUB_FLT_MACnlo register. The logical AND of values of the mask and the last byte of the address of the received frame is taken and the result is compared with the specified address.
The forced forwarding bit should be set to 1 only when the frame should always be forwarded through the hub. Note that forced forwarding operates regardless of the hub setting (enabling or disabling). That is, when the hub module is disabled, the forced forwarding can still be used for cut-through forwarding of only specific frames.
Broadcast frames should not be forwarded through the hub without any clear request by application. Broadcast addresses are needed to be input to the filter table. Filtering can be enabled through the control bit in the HUB_CONTROL.

Table 29.8 Typical HUB MAC Filter Setup

MAC Address	Mask	Forced Forwarding	Notes
01-80-c2-00-00-00	C0h	0	Filters all frames in range 01-80-c2-00-00-{00..3F} The register settings for MAClo and MAChi would be: HUB_FLT_MACnlo = 00C2 8001h HUB_FLT_MACnhi = 00C0 0000h
01-1b-19-00-00-00	FFh	0	Filters only this address (PTPv2)
01-00-5e-00-01-80	F8h	0	Filters 01-00-5e-00-01-{80..87}(224.0.1.{128..135})
01-00-5e-00-00-00	FCh	0	Filters 01-00-5e-00-00-{00..03} (224.0.0.{0..3})
<Local node unicast address>	FFh	0	Must be entered to avoid unnecessary forwarding of frames that are directed to the local node only.
01-21-6C-00-00-01	FFh	1	Must be forced-forwarded through the hub. The register settings for MAC6lo/ MAC6hi would be: HUB_FLT_MAC6lo = 006C 2101h HUB_FLT_MAC6hi = 01FF 0100h

29.3.2.5 Hub Module Forced Forwarding

Forced forwarding bit (bit 24 in HUB_FLT_MACnhi) can be set for each filter entry. The bit changes the filter function not to frame filtering, but to frame forced forwarding. When an address match occurs and forced forwarding bit is set for the address entry, a frame is forwarded through the hub (cut-through). On the other hand, a frame to be forwarded to the MAC or switch will be discarded before the MAC or switch receives. The forced forwarding takes place always, independent of the hub's enable control (bit 0 of HUB_CONTROL).
Due to the discard behavior in this mode of operation, a forced-forwarded frame is not processed by the switch. Hence no address learning can take place on such frames. It also cannot be forwarded to the local application through port 2. This is different from the normal hub operation, where all frames are still passed up to the switch normally and then discarded by the switch only at the line port to avoid duplication to the line.
As described in the next section, the DLR module will receive forced forwarded frames normally. This is because the module is located before the MAC or switch and is not affected by the discard. Thus, generally, the forced forwarding is expected to be used for DLR beacon frames. DLR module processing of the beacon frames enables to reduce load for application.

29.3.2.6 Loop Filtering

The hub module includes a loop filter that is capable of discarding frames with defined source addresses arriving at the receiving ports to prevent frames from the given addresses passing through the hub or switch. This is typically required within applications that are connected to the ring.
Frames transmitted from the local node may be received again after they passed through the ring, so once the loop filter has discarded a frame, it is completely removed from the network and never processed again by the hub or switch.
The MAC address local node for processing by the loop filter can be set in the LOC_MAClo and LOC_MAChi registers of the DLR module.

29.3.3 DLR Module

The Device Level Ring (DLR) module offers beacon frame processing on receive path of both port 0 and port 1 of the switch core.
The DLR module is inserted between the hub module and switch module. Beacon frames on receive paths are detected and discarded by the DLR module before entering the switch from both external ports. All the beacon frame parameters are interpreted and stored locally for software access.
Any ring status change for beacon based node implementation is notified to the CPU through the interrupt. This enables to read the received beacon frame parameters at any time. Statistics counters are implemented for the count of beacon frames received and transmitted.

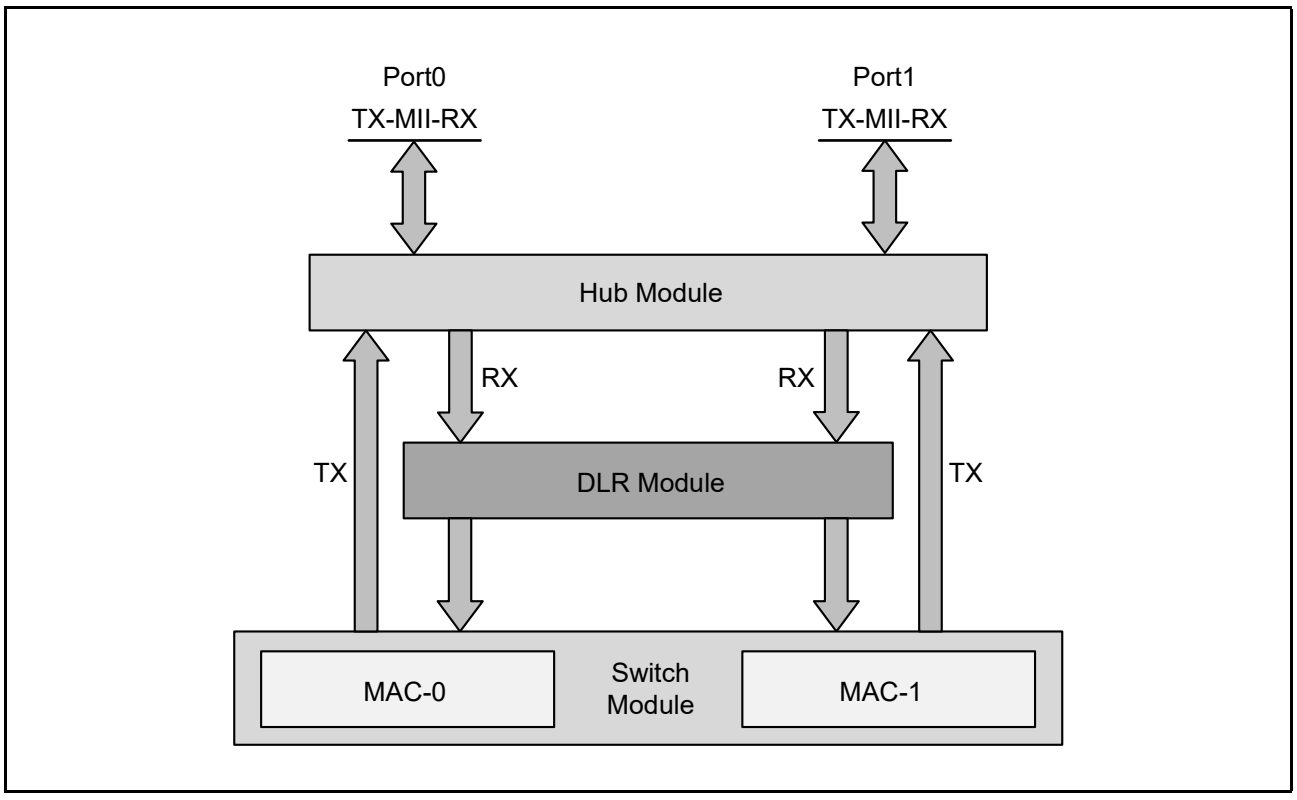
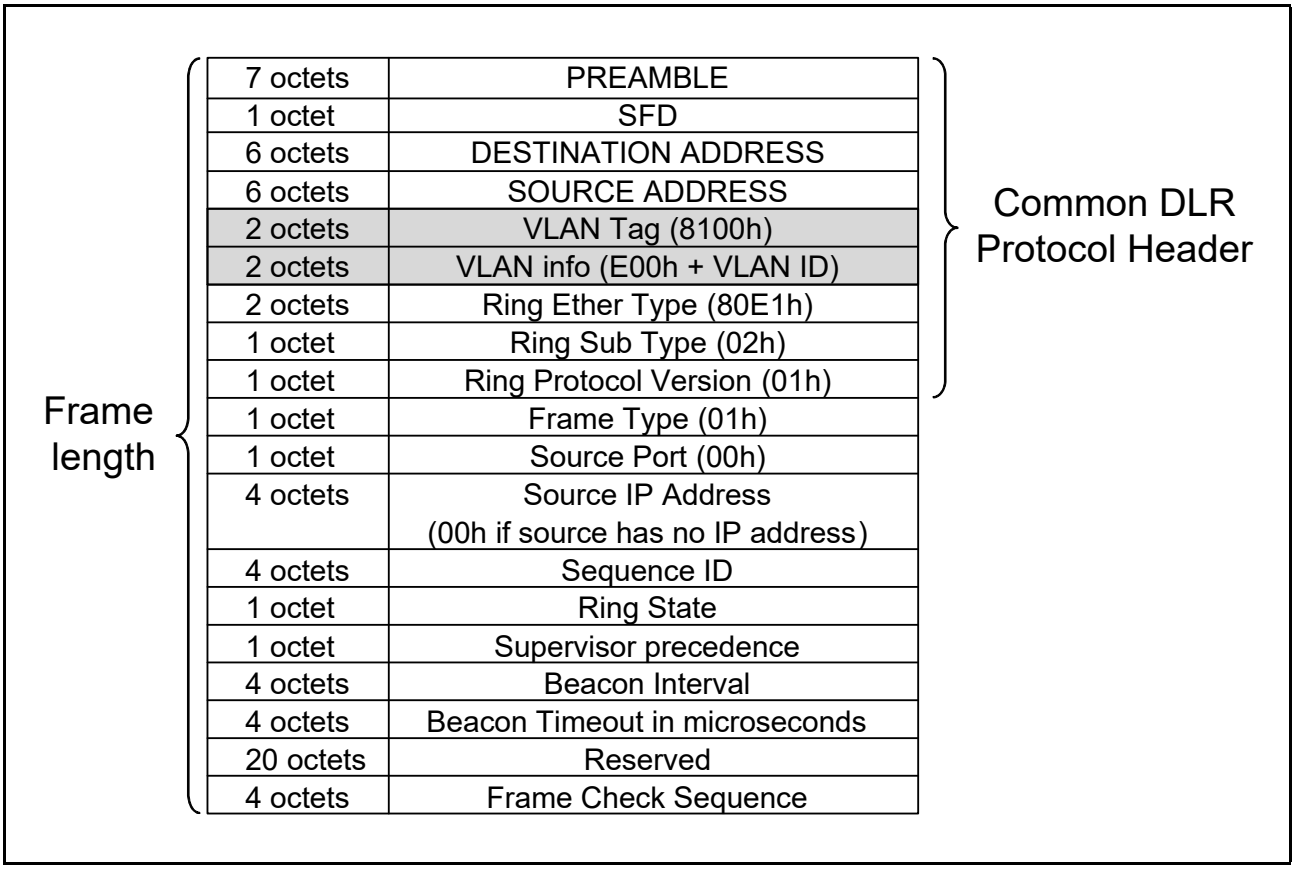


Figure 29.15 Connection Image of Hub Module and DLR Module

29.3.3.1 Beacon Frame Format

Within a DLR Network, the active ring supervisor transmits a beacon frame through both of its Ethernet ports in the beacon interval (400 microseconds by default). DLR frames use the frame format of 802.1Q. Frames are transmitted with highest priority (7). A beacon frame is the DLR frame with length of 64 bytes, excluding the preamble and the SFD. A beacon frame consists of the following fields:



7 octets	PREAMBLE
1 octet	SFD
6 octets	DESTINATION ADDRESS
6 octets	SOURCE ADDRESS
2 octets	VLAN Tag (8100h)
2 octets	VLAN info (E00h + VLAN ID)
2 octets	Ring Ether Type (80E1h)
1 octet	Ring Sub Type (02h)
1 octet	Ring Protocol Version (01h)
1 octet	Frame Type (01h)
1 octet	Source Port (00h)
4 octets	Source IP Address (00h if source has no IP address)
4 octets	Sequence ID
1 octet	Ring State
1 octet	Supervisor precedence
4 octets	Beacon Interval
4 octets	Beacon Timeout in microseconds
20 octets	Reserved
4 octets	Frame Check Sequence

Figure 29.16 Beacon Frame Format

Beacon frames are processed and parameters are stored in the local registers for the software access. Table 29.9 lists the fields of beacon frames and the names of the relevant registers which hold the values for the ring node.

Table 29.9 Beacon Frame Field Definitions

Term	Description	Register Name
Destination Address	The destination MAC address for the beacon frame is a fixed multicast address of 01-21-6C-00-00-01. This is an exclusive MAC address used only for beacon frames. Cut-through forwarding can be used based on this address match.	—
Source Address	Source MAC address of the supervisor. 48-bit address is stored in two separate registers.	SUPR_MAClo/ SUPR_MAChi
VLAN TAG	DLR messages contain 2 octets VLAN tag (8100h) after the source MAC address according to 802.1Q.	—
VLAN information	16-bit information field contains the priority field and the VLAN_ID. VLAN ID is configured at the ring supervisor and received by the ring nodes. The default value for the VLAN ID is 0 when there is no VLAN ID available. The default VLAN ID does not need to be changed unless a commercial switch is being used within the ring.	Bits 31 to 16 of STATE_VLAN When bit 8 is set to 1, the value is valid.
Ring Ether Type	Ether type for DLR frames is 80E1h	—
Ring Sub Type	Ring Sub type value is always 02h for the DLR messages	Bits 7 to 0 in ETH_STYP_VER
Ring Protocol Version	Protocol version for the DLR messages	Bits 15 to 8 of ETH_STYP_VER
Frame Type	Frame Type value for the beacon frame is always 01h	—
Source Port	Source port value is always 0h for the beacon frame	Bits 23 to 16 of ETH_STYP_VER
Source IP address	IP address of the supervisor. The default value for the IP address is 0 when there is no IP address available.	SUPR_IPADR
Sequence ID	Sequence identification number of the frame	SEQ_ID
Ring State	State of the ring network transmitted by the ring supervisor.	Bits 7 to 0 of STATE_VLAN
Supervisor priority	The ring supervisor priority value contains the priority value assigned to the ring supervisor. When multiple supervisors are enabled, the priority value enables the user to select a single supervisor with the highest priority. The ring supervisor’s priority value can be any value within the range from 0 to 255, with numerically higher values indicating higher priority.	Bits 23 to 16 of SUPR_MAChi
Beacon Interval	Interval in microseconds at which the ring supervisor sends beacon frames. The valid value is in the range between to minimum 100 microseconds and maximum 100 milliseconds. The typical value is 400 microseconds.	BEC_INTRVL
Beacon Timeout	Amount of time in microseconds, nodes shall wait before timing out reception of beacon frames and taking appropriate action. The valid value is in the range between minimum 200 microseconds and maximum 500 milliseconds. The typical value is 1960 microseconds.	BEC_TMOUT
Frame Check Sequence	CRC value for the frame	—

29.3.3.2 Functional Description of Ring Node

Beacon frames are detected and interpreted by the ring module, so that the CPU is not burdened with processing the beacon frames for ring node implementation. Any ring status change for beacon-based node structure is notified to the CPU through the interrupt.
It is also possible to read the received beacon frame parameters at any time. Statistics counters are also implemented to view the number of beacon frames received and transmitted.

(1) Initial Settings

The following are the steps to configure the DLR module:

- Set the 4 low-order bytes of the beacon destination address (006C 2101h) for register HUB_FLT_MAC6lo which is also the value after reset.
- Set the 2 high-order bytes of the beacon destination address and enable forced forwarding (01FF 0100h) for register HUB_FLT_MAC6hi which is also the value after reset. The mask bit is FFh.
- Set the 4 low-order bytes of the MAC address of the local device to the DLR module register LOC_MAClo which is used by the loop filter.
- Set the 2 high-order bytes of the MAC address of the local device to the DLR module register LOC_MAChi which is used by the loop filter.
- Set the DLR Ethernet frame type value of 80E1h to register DLR_ETH_ TYP which is also the value after reset.
- Enable the DLR module through the control register DLR_CONTROL. Number of cycles required to count 1 microsecond should also be set by this register. The DLR module of this LSI is 75 MHz, hence resister DLR_CONTROL needs to be set to 4Bh, which needs to be changed from the value after reset.
- Any interrupt source can be enabled or disabled through register DLR_IRQ_CTRL as required by the software.

(2) Start Up

Upon start up, the ring node will be in IDLE_STATE and presumes the network is in linear topology mode. The current state of the local ring node and other status bits are stored within the status register for software access.
An invalid timer value should be ignored by setting bit 4 of the DLR_CONTROL register. The beacon frame with invalid timeout timer value is received, the frame is ignored. On the other hand, an invalid timer value is stored in the INV_TMOUT register irrespective of the setting of bit 4 of DLR_CONTROL. An interrupt will also be generated by enabling through bit 11 of DLR_IRQ_CTRL.
Upon receiving a beacon frame through either port, the ring node shall transition to FAULT_STATE, which presumes the network is in ring topology mode. An interrupt will be generated by enabling bit 1 of DLR_IRQ_CTRL and this interrupt generation notifies the CPU of a need for flushing the MAC address learning table as well as a change in the state. All ring supervisor parameters will be saved within the register for software access. The following parameters will be saved only during transition from IDLE_STATE to FAULT_STATE:

- Supervisor's MAC address and will be stored in registers SUPR_MAClo and SUPR_MAChi.
- Supervisor's priority value will be stored in register SUPR_MAChi.
- VLAN ID will be stored in register STATE_VLAN.
- Beacon timeout timer value will be stored in register BEC_TMOUT.

The supervisor IP address is accepted to change at any time. A new IP address will always replace the old one and interrupt will be generated indicating a change in the IP address if enabled through bit 10 of register DLR_IRQ_CTRL.
If a beacon frame received from a different supervisor with a higher priority value or higher numeric value for MAC address even with the same priority level, new beacon frame parameters will replace all the old values. An interrupt will be generated indicating change of supervisor if enabled through bit 6 of register DLR_IRQ_CTRL. The ring node will stay in FAULT_STATE.
If a beacon frame received from a different supervisor with a lower priority value or lower numeric value for MAC address with same priority value, the beacon frame will be ignored. An interrupt will be generated indicating an ignored beacon frame if enabled through bit 9 of register DLR_IRQ_CTRL. The ring node will stay in FAULT_STATE.
The ring supervisor is not expected to change parameters within the beacon frame. If parameters need to be changed, the supervisor stops transmitting the beacon frame for at least two beacon timeout periods before transmitting beacon frames with new parameters.
If the local node state changes back to IDLE_STATE due to the elapse of the beacon timeout timer on both ports, it will generate an interrupt if enabled through bits 4 and 5 of register DLR_IRQ_CTRL. Current interrupt status is available for software access showing beacon timeout has occurred on both ports, need to erase the MAC address learning table and to change the state of register DLR_IRQ_STAT_ACK.
Upon receiving beacon frames through both ports and after receiving a beacon frame from the active ring supervisor with ring state field set to RING_STATE_NORMAL on either one of its ports, the local node shall transition to NORMAL_STATE. Interrupt status bits will show the change in the state, need to erase the unicast MAC address learning table and to stop neighbor check timeout timer when enabled within the software.

Note: Neighbor check time out timer (100 milliseconds) for neighbor check process should be implemented by the software. Software can use bits 3 and 2 of register DLR_IRQ_STAT_ACK to stop the timer.

(3) Fault Detection

Any of the following events shall cause the ring node to transition from NORMAL_STATE to other states:

- Receipt of a beacon frame with a state parameter set to RING_FAULT_STATE:
  Bit 0 of register DLR_IRQ_STAT_ACK is set indicating a change in the node state.
  An interrupt is generated when interrupt generation is enabled.
- Receipt of a beacon frame with a different MAC address or higher priority than the current active ring supervisor:
  In addition to state change, bit 6 of register DLR_IRQ_STAT_ACK is set indicating a change in the supervisor.
- A case that both ports failed to receive a beacon frame for a period specified by the beacon timeout value:
  The node state transitions to IDLE_STATE. In addition to the state change, bits 5 and 4 of register DLR_IRQ_STAT_ACK are set indicating timeout of the beacon timeout timer on the both ports.
- A case that one of the ports failed to receive beacon frame for a period specified by the beacon timeout period:
  The node state transitions to FAULT_STATE. In addition to the state change, bit 5 or 4 of register DLR_IRQ_STAT_ACK is set indicating timeout of the beacon timeout timer on the port.

(4) Error Handling

The DLR node is able to handle several error conditions:

- CRC errors detected in beacon frames:
  When a CRC error is detected in a beacon frame, the beacon frame in not processed in the DLR node and discarded before entering the switch. The parameters of the beacon frame with an error are not stored in the register. On the other hand, even with a beacon frame with an error Beacon frames with CRC errors are forwarded through the hub module since the hub does not check for CRC. Beacon frames with CRC error are counted by the statistics counter RX_ERR_STAT0 and RX_ERR_STAT1.
- Beacon frame timeout timer value in the invalid range:
  The valid range for the beacon frame time out timer value is between 200 microseconds to 500 milliseconds. When a beacon frame from the supervisor has an invalid value of the beacon timeout and if bit 4 of register DLR_CONTROL is set, the frame will be ignored and discarded before entering the switch. Regardless of this setting, beacon frames with an invalid timeout timer value are always detected and the invalid timeout value is stored within register INV_TMOUT. An interrupt is also generated if bit 11 of register DLR_IRQ_CTRL is set.

This document describes the DLR module incorporated in this LSI. For details of the DLR, see the relevant ODVA specifications.

29.3.4 IEEE 1588 Timer and Control Module

29.3.4.1 Overview

The timer and control module (TSM) implements an adjustable timer for IEEE 1588 implementations allowing synchronizing the local time of the timer to a remote master clock (through some protocol specific application software such as PTP).
In addition, the module provides the time base for all frame timestamping performed at the MAC/PHY interfaces of all external ports. The timestamps enable use of time synchronization protocols (e.g. IEEE 1588 Precision-Time-Protocol, PTP) to synchronize distributed clocks in the network to a common master clock.

29.3.4.2 IEEE 1588 Message Formats

(1) Transport Encapsulation

The Precision-Time-Protocol (PTP) datagrams are encapsulated in Ethernet frames using the UDP/IP transport mechanism, or, in addition to UDP/IP, with PTPv2, directly described in Ethernet frames (Layer 2). Typically multicast addresses are used to allow efficient distribution of the synchronization messages.

- UDP/IP

The 1588 messages (v1 and v2) can be transmitted using UDP/IP multicast messages. The following IP multicast groups in Table 29.10 are defined for PTP. The table also shows their respective MAC layer multicast address mapping according to RFC 1112.

Table 29.10 UDP/IP Multicast Domains

Name	IP Address	MAC Address Mapping
Default PTP domain	224.0.1.129	01-00-5e-00-01-81
Alternate PTP domain1	224.0.1.130	01-00-5e-00-01-82
Alternate PTP domain2	224.0.1.131	01-00-5e-00-01-83
Alternate PTP domain3	224.0.1.132	01-00-5e-00-01-84

Table 29.11 UDP Port Numbers

Message Type	UDP Port	Note
Event	319	Used for SYNC and DELAY_REQUEST messages.
General	320	Any messages other than the above (e.g. follow-up, delay-response)

- Native Ethernet (Layer 2)

In addition to the usage of UDP/IP frames, IEEE 1588v2 defines a native Ethernet frame format that uses EtherType = 88F7h. The payload of the Ethernet frame directly contains the PTP datagram, starting with the PTPv2 header.
Besides, version 2 adds a peer delay mechanism to allow delay measurements between individual point-to-point links along a path over multiple nodes. The following multicast domains are additionally defined in PTPv2.

Table 29.12 PTPv2 Multicast Domains

Name	MAC Address
Normal messages	01-1b-19-00-00-00
Peer delay messages	01-80-c2-00-00-0e

(2) PTP Header

All PTP frames contain a common header, which is used to determine the protocol version as well as the type of message, which defines the further content of the message. All multi-octet fields are transmitted in big-endian order. The version field's last 4 bits are at the same position for both PTPv1 and PTPv2 headers, allowing a correct identification by inspecting the first 2 bytes of the message.

Note: For details on the meaning of the PTP frame contents, see the IEEE 1588 specification. The following sections only describe some of the relevant information that may be useful to help the reader to understand some of the terms used in the documentation. PTPv1 refers to the version 1 of the IEEE 1588 standard specification. PTPv2 refers to version 2 of the standard.

- PTPv1 Header

Table 29.13 Common PTPv1 Message Header

Bits									
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Octets**	**Offset**
versionPTP = 0x0001								2	0
versionNetwork								2	2
subdomain								16	4
messageType								1	20
sourceCommunicationTechnology								1	21
sourceUuid								6	22
sourcePortId								2	28
sequenceId								2	30
control								1	32
0x00								1	33
flags								2	34
reserved								4	36

The type of message is encoded in the messageType and control fields as follows:

Table 29.14 PTPv1 Message Type Identification

messageType	Control	Message Name	Message
0x01	0	SYNC	Event message
0x01	1	DELAY_REQ	Event message
0x02	2	FOLLOW_UP	General message
0x02	3	DELAY_RESP	General message
0x02	4	MANAGEMENT	General message
Others	Others		Reserved

- PTPv2 Header

Table 29.15 Common PTPv2 Message Header

Bits								Octets	Offset
7	6	5	4	3	2	1	0		
ransportSpecific				messageId				1	0
reserved				versionPTP = 0x2				1	1
messageLength								2	2
domainNumber								1	4
reserved								1	5
flags								2	6
correctionField								8	8
reserved								4	16
sourcePortIdentity								10	20
sequenceId								2	30
control								1	32
logMeanMessageInterval								1	33

The type of message is encoded in the messageId field as shown in Table 29.16.

Table 29.16 PTPv2 Message Type Identification

messageId	Message Name	Message
0x0	SYNC	Event message
0x1	DELAY_REQ	Event message
0x2	PATH_DELAY_REQ	Event message
0x3	PATH_DELAY_RESP	Event message
0x4 to 0x7		Reserved
0x8	FOLLOW_UP	General message
0x9	DELAY_RESP	General message
0xa	PATH_DELAY_FOLLOW_UP	General message
0xb	ANNOUNCE	General message
0xc	SIGNALING	General message
0xd	MANAGEMENT	General message

The PTPv2 flags field contains further details on the type of message, especially if one-step or two-step implementations are used. The flags field consists of two octets with the following meanings for the bits. Reserved bits are set to 0.

Table 29.17 PTPv2 Message Flags Field Definitions

Octet Offset	Bit	Name	Description
6 (first)	0	ALTERNATE_MASTER	See IEEE 1588 Clause 17.4
	1	TWO_STEP	0: One-step clock 1: Two-step clock
	2	UNICAST	0: Multicast Address 1: Unicast Address
	3, 4	Reserved	
	5	Profile specific	
	6	Profile specific	
	7	Reserved	

Note: See the IEEE 1588 specification for details on frame formats and these fields.

29.3.4.3 Adjustable Timer Module

(1) Overview

The adjustable timer module (TSM) implements the Free Running Counter (FRC), the timer, which is used to generate the timestamps for received and transmitted frames. The FRC operates with the clock (100 MHz), whose time resolution is 10 ns.

Through a dedicated correction circuit, the timer can be adjusted allowing synchronization to a remote master and provide a synchronized timing reference to the local system. The timer consist of a nanosecond-timer and second-timer. When the nanosecond-timer reaches 10^9, an interrupt is generated.

It is possible to generate the synchronous pulse signal which is arbitrary period based on the current time of the FRC. Time reference can be provided to the external system of this LSI.

(2) Adjustable Timer Implementation

The adjustable timer consists of a programmable counter/accumulator and two correction counters. The periods of the counters and its increment rate are freely configurable allowing very fine tuning of the timer.

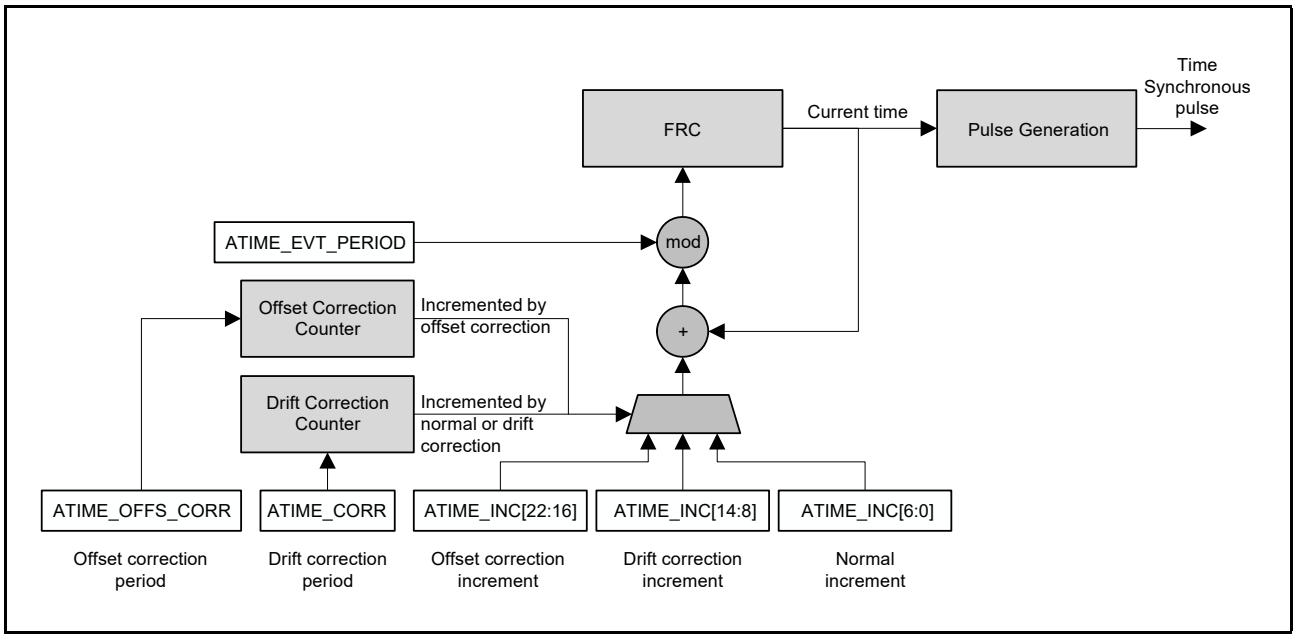


Figure 29.17 Adjustable Timer Structure

(3) Normal Timer Operation

The Free Running Counter (timer) continues to produce the current time. A constant value is added to the current time per clock cycle as programmed in bits 6 to 0 of the ATIME_INC register. To obtain accurate time, the ATIME_INC bits 6 to 0 always need to be set to 001010b, which represents in 10 ns.

The period, configured in register ATIME_EVT_PERIOD, defines the modulo and is used when the counter has to wrap around. The period must always be set to 10^9. By this setting, all timestamps can be used in nanoseconds.

(4) Drift Correction

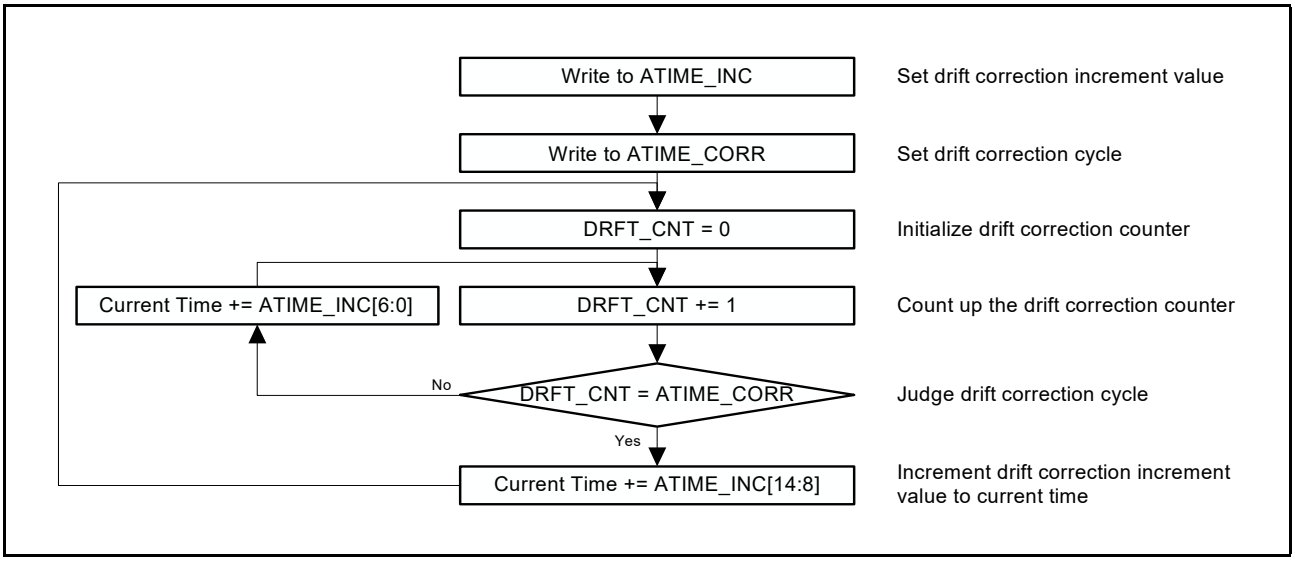


Figure 29.18 Drift Correction

The drift correction counter operates fully independently of the FRC (timer) and increments by 1 with each clock cycle. When it reaches the value configured in ATIME_CORR, it restarts and instructs the timer once to increment by the correction value, instead of the normal value. The normal and correction increments are configured in register ATIME_INC. To speed up the timer, the correction increment would be larger than the normal increment value. To slow down the timer, the correction increment would be smaller than the normal increment value. Note that the correction counter only defines the distance of the corrective actions, not the amount. This allows very fine corrections (low jitter) happening in the range of 1 ns independently from the clock frequency.

(5) Offset Correction

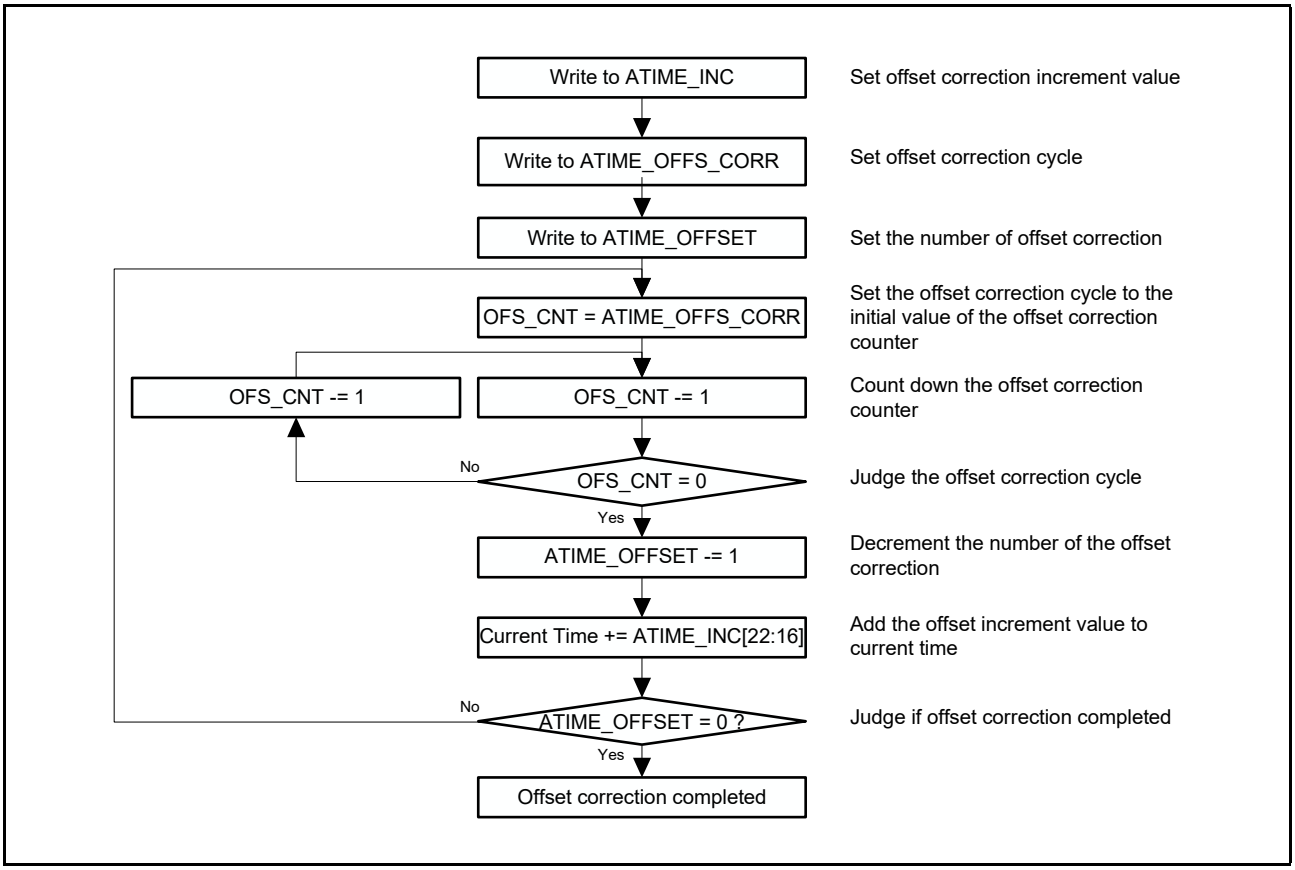


Figure 29.19 Offset Correction (When ATIME_OFFS_CORR is not 0)

The offset correction counter operates fully independently of the FRC (timer) and decrements by 1 with each clock cycle, when a value is loaded. It can be loaded with a value by writing register ATIME_OFFS_CORR. The timer does not start until an offset correction has been written into ATIME_OFFSET (i.e. the ATIME_OFFS_CORR must be written before writing the ATIME_OFFSET value).

When a value is written into ATIME_OFFSET, the offset correction counter is loaded with ATIME_OFFS_CORR and starts counting. When it reaches 0, it decrements the ATIME_OFFSET value and applies the offset correction increment as defined in bits [22:16] of ATIME_INC to the time counter. If the ATIME_OFFSET value is not 0 after it was decremented, the counter is reloaded with ATIME_OFFS_CORR value and the cycle repeats. This will repeat until the value in ATIME_OFFSET has reached 0, after which no more corrections will be performed.

With this correction, it is possible to shift the timer to another time without causing an immediate jump in time. When the offset correction has completed, the ATIME_OFFSET register will read out 0 and the offset event interrupt can be triggered as needed.

Instead of distributing the offset correction over time using the offset correction timer, it is possible to immediately change the current time by the offset amount. This leads to a jump of the timer to the time *current-time + offset*. Setting ATIME_OFFS_CORR to 0 and then writing the offset into ATIME_OFFSET achieves this. A positive or negative value can be written to adjust the timer accordingly.

(6) Pulse Signal Generation

This LSI chip is capable of generating desired periodic pulse signals (SYNCOUT signals) based on the current time values output by the timer.

Table 29.18 Parameter List of Pulse Signal Generation

Parameter	Registers	Description
Pulse generation enable	SWTMEN	Enables or disables to output pulse signal
Pulse output start time	SWTMSTSEC SWTMSTNS	Set the start time of the output signal in seconds and nanoseconds. After set the start time and set 1 to the SWTMEN register in order to enable to output the pulse signal, the pulse output starts when current time is over the start time set. If pulse output is enabled after the set start time, no pulse is output.
Pulse period	SWTMPSEC SWTMPNS	Set the pulse period of the output signal in seconds and nanoseconds. The value set in the SWTMPNS register must produce an integer when used as a divisor for the value for one second which is set in the ATIME_EVT_PERIOD register and be a multiple of 10 ns. The value must be set before pulse output is enabled.
Pulse width	SWTMWTH	Set the pulse high level width in nanoseconds. The value must be a multiple of 10 ns. If the pulse width set in the SWTMWTH register is greater than pulse period, output is fixed to high level. If the pulse width is set to 0, no pulse is generated and output is fixed to low level. The value must be set before pulse output is enabled.
Pulse rising time latch	SWTMLATSEC SWTMLATNS	The pulse output rising time is latched into the registers. The value is updated whenever pulse output rises.

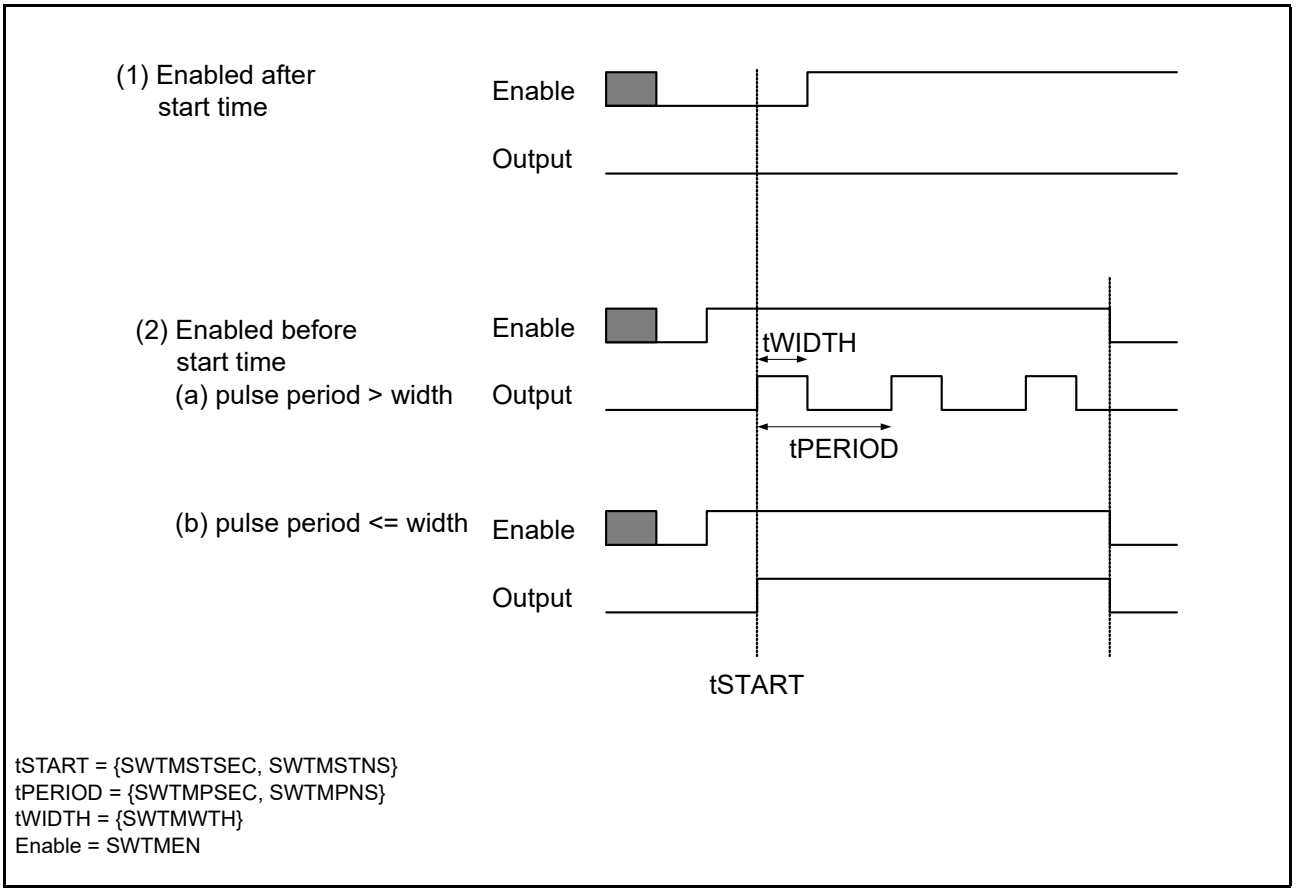


Figure 29.20 Timing Chart of Pulse Signal Generation Function

29.3.4.4 Timestamp Processing

(1) Receive Timestamp Processing

When port 0 or port 1 receives a frame, the timestamp, based on the current time from the timer, is captured when the start of frame delimiter (SFD) is detected at the PHY interface. The timestamp is forwarded together with the frame to the switch module and can be accessed by the internal port (management port) to implement e.g. the Precision-Time-Protocol (PTP). The timestamp information is encapsulated in the dedicated tag in the frames.

(2) Transmit Timestamp Processing

When a frame is transmitted from port 0 or port 1 to the PHY, the timestamp is also captured. The outgoing timestamp can be stored in the port specific timestamp register (PORTn_TIME) for each port. The internal port adds special control information to each frame to limit frames for outgoing timestamp capture, as timestamps must only be captured for dedicated event frames, not for all frames.

29.3.4.5 Transparent Clock Support

(1) General

The hardware implements the necessary functions to implement so-called transparent clocks (TC) for the end-to-end variant.

(2) Implementation of Correction Field Update

The correction field within outgoing Layer 2 PTP frames (i.e. frames with type 0x88F7) can be updated automatically. PTP messages within UDP/IP frames are not automatically updated.
The module that updates the correction field only processes event messages. To detect event messages, frames with the message type field found within the PTP header (type < 4) are extracted. This means that follow-up frames which are not event frames are not processed. Therefore, any correction field detected in the corresponding SYNC frame will be updated automatically. This allows supporting correction field update by one-step as well as two-step master and slave nodes.
For an end-to-end implementation, the correction field of SYNC and DELAY_REQ messages is updated only with the transient time (output time - input time).
Correction field updates occur only on frames that are exchanged between port 0 and port 1. Any frame transmitted from and to the internal port will not be modified.

29.3.5 Frame Tag Dedicated to Management Port (Internal Port)

Information related to frames such as control and timestamp information needs to be delivered between the Ethernet switch and internal Ethernet MAC. Such information can be added to frames as a management tag. The frames with the tag can be transmitted between the Ethernet switch and internal Ethernet MAC. The frames with the tag are used only for transfers between the Ethernet switch and internal Ethernet MAC and once accepted on the receiving side, the information in the tag is acquired. Then the tag is removed.

29.3.5.1 Format of Management Tag

The information of control and timestamp is added into a frame right after the frame source address field as a frame type tag (programmable with a given value). If the tag is added to the position before any other tag (VLAN tag), if exists. The tag includes the following information:

- ControlTag: Identifier that indicates the additional control data is present within the frame. Defined by the ETHSWMTC register and its size is 2 octets.
- ControlData: Control information of the frame. The size is 2 octets.
- ControlData2: Specifies timestamp information on reception and transmit port on transmission. The size is 4 octets.

The original frame follows the ControlData2. For example, any VLAN tags will be found after ControlData2.

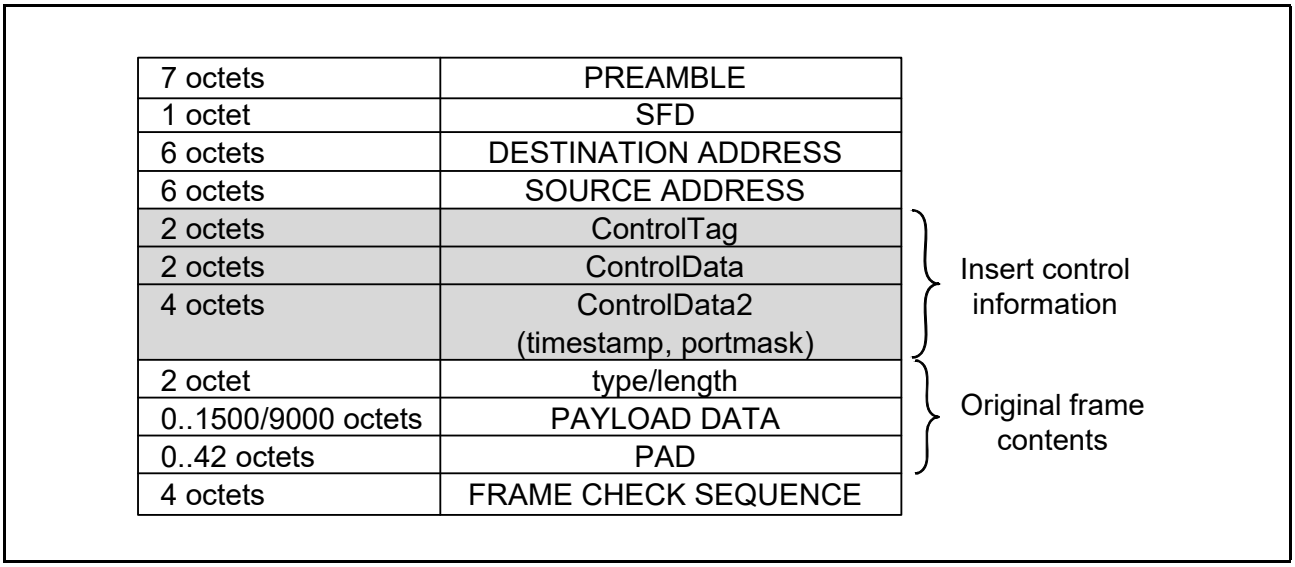


Figure 29.21 Format of Frame with Management Tag in Internal Port

Once a tag is added to a frame, the CRC is recalculated and a new CRC replaces the original CRC received with the frame.
The first octet of ControlData is the more significant byte (bits 15:8) and the 2nd octet of ControlData is the less significant byte (7:0). The first octet of ControlData2 is the more significant byte (bits 31:24) and the 4th octet of ControlData2 is the less significant byte (7:0).

29.3.5.2 Transmit Processing (from Switch to Internal Ethernet MAC)

When the switch forwards a frame to the internal Ethernet MAC, the following information is added into all frames when the tag function has been enabled through bit 31 in register ETHSWMTC.

Table 29.19 Management Frame Tag (During Transfer from Switch to Internal Ethernet MAC)

Field	Bit	Description
ControlData	0	Indicates the number of the external port from which the frame was received. 0: Port 0 1: Port 1
	15 to 1	Reserved
ControlData2	31 to 0	Indicate received timestamp of the frame. The 32-bit nanoseconds value when the SFD of the frame was detected on the port from which the frame was received.

29.3.5.3 Receive Processing (from Internal Ethernet MAC to Switch)

When the internal Ethernet MAC forwards a frame to the switch, the internal Ethernet MAC adds the following information to all frames when the tag function has been enabled through bit 31 in register ETHSWMTC. Once the switch receives the frame with a management tag, it removes the tag from the frame after acquiring the tag contents.

Table 29.20 Management Frame Tag (During Transfer from Switch to Internal Ethernet MAC)

Field	Bit	Description
ControlData	0	Specifies forced forwarding. 0: Forced forwarding is disabled: The frame is forwarded normally. 1: Forced forwarding is enabled: The frame is forwarded to all ports defined in bits 1 and 0 in ControlData2.
	1, 2	Reserved
	3	Marks frame for outgoing timestamping. When set, the frame transmit timestamp will be latched into the corresponding port's transmit timestamp register PORTn_TIME, when the frame is transmitted.
	15 to 4	Reserved
ControlData2	1, 0	Set a destination port mask. Relevant only if ControlData forced forwarding bit (bit 0) is set. Specify the port to which the frames are transferred. Simultaneous forced forwarding to multiple ports is possible. Bit 0 is for port 0 and bit 1 is for port 1. The bits can set: 0: Frame is not forwarded forcibly to the port. 1: Frame is forwarded forcibly to the port.
	31 to 2	Reserved

29.3.5.4 Setting Management Tag Function

The tag insertion or removal function is enabled with register ETHSWMTC. When enabled, a tag inserted automatically to all frames transferred from the switch to the internal Ethernet MAC as well as those transmitted from the internal Ethernet MAC to the switch. When the switch finds any tag, it acquires the tag information and removes the tag for normal transmit processing.

Note: The tag identifier must be configured to a value (e.g. value after reset: E001h) which is not used in the network. For handling management tags in the internal Ethernet MAC, see section 28, Ethernet MAC (ETHERC).

29.4 Overview of Control Software

29.4.1 Overview

The Ethernet switch is the hardware to forward frames between ports. During the forwarding processing, MAC destination address is searched and frames that requires special specific forwarding such as BPDU are filtered. Software needs to initialize the switch and executes tasks to operate the switch.
The software that operates the IEEE1588 timestamp and the DLR is necessary, when they are used. In addition, the higher protocol such as spanning tree needs to be implemented as required.
This section describes the most basic procedures required for switch initialization and learning table management to operate the switch.

29.4.2 Switch Initialization

Initialization of the Ethernet switch includes the following steps.

- Make settings in the MSTPCRB register for release from the module-stop state and reset the Ethernet switch.
- Clear the address table.
- Configure the management (internal) port
- Enable switch ports.
- Enable the MACs on ports.
- Configure the hub module.
- Configure the timer module.
- Configure the DLR module.

Table 29.21 shows examples of initial settings of the address table. Table 29.22 shows examples of initial settings at least required for switch operation. As to the timer module, correction is not performed, the DLR module is also in disable state. For these, set appropriate values in higher-level protocols such as PTP and DLR.

Table 29.21 Examples of Initial Settings of Address Table

Address	Register	Setting Example	Description
A00C 4000h to A00C 47FCh (4-byte units)	ADR_TABLE	0000 0000h	Initializes all entries to 0 in the address table.
A00C 4000h + Hash value of Unicast MAC address×8h	ADR_TABLE	0403 0201h	Sets a unicast address as a static entry. The setting example is when the MAC address is 01-02-03-04-05-06. Only mask port 2 with priority 0. Setting is not required when set dynamically.
Address above +4h	ADR_TABLE	0083 0605h	

Table 29.22 Examples of Initial Settings of Switch Engine

Address	Register	Setting Example	Description
A00B F110h	ETHSWMTC	0000 E001h	Does not use a management tag. Set the register to 8000 E001h when use it. Release the protection using the system protect command register when writing to this register.
A00B F114h	ETHSWMD	0000 0000h	Sets the mode of 10/100 Mbps full-duplex. Release the protection using the system protect command register when writing to this register.
A00B F118h	ETHSFTRST	0000 0006h	Releases the Ethernet switch module and the PHYRESET# pin from the reset state. When writing to this register, protection must be unlocked by using the protect command register.
A00C 000Ch	UCAST_DEFAULT_MASK	0000 0007h	Set the forwarding mask for unknown unicast traffic. When an unknown unicast is received on any port, it is forwarded to all ports set by this mask. When the address table has been initialized, it may be removed from the management (internal) port from the list, which will prevent any unnecessary transfer of unknown unicast the local system. However, this requires the local system's unicast address is set in the address table (i.e. either set during initialization statically, or change the mask setting after at least one frame was sent from the local system and dynamically activate the learning function).
A00C 0014h	BCAST_DEFAULT_MASK	0000 0007h	Specifies all ports to which a broadcast frame will be forwarded.
A00C 0018h	MCAST_DEFAULT_MASK	0000 0007h	Specifies all ports to which a multicast frame will be forwarded, if the address is not found in the address table.
A00C 0020h	MGMT_CONFIG	000 0042h	Enables reception of BPDU frames (bit 6 = 1) and forward the frames to the management port (port 2). If management frames should be discarded, bit 7 should be set.
A00C 0100h A00C 0104h A00C 0108h	VLAN_PRIORITY0 VLAN_PRIORITY1 VLAN_PRIORITY2	006D B688h	Map VLAN priority into the 4 queues available for each port. In this setting, priorities 0 to 3 into queues 0 to 3 and priorities 4 to 7 all into queue 3.
A00C 0180h A00C 0184h A00C 0188h	PRIORITY_CFG0 PRIORITY_CFG1 PRIORITY_CFG2	000 0001h	Enable mapping of the output queue by VLAN priority classification for each port and set default port priority to 0.
A00C 0080h	OQMGR_STATUS	0000 0000h	Enables the output queue. Since bit 1 is set to 1 during the initialization of the memory cell, if bit1 becomes 0, the register should be cleared to 0.
A00C 0088h	QMGR_ST_MINCELLS	0000 0000h	Clears the minimum information of memory free state.
A00C 0094h	QMGR_WEIGHTS	0804 0201h	Sets the weight on the output queue.
A00C 0008h	PORT_ENA	0000 0007h	Enables all ports of the switch.

Table 29.23 Examples of Initial Settings of MAC

Address	Register	Setting Example	Description
A00C 801Ch A00C A01Ch	RX_SECTION_EMPTY0 RX_SECTION_EMPTY1	0000 0000h	The value cannot be changed.
A00C 8020h A00C A020h	RX_SECTION_FULL0 RX_SECTION_FULL1	0000 0000h	The value cannot be changed.
A00C 8024h A00C A024h	TX_SECTION_EMPTY0 TX_SECTION_EMPTY1	0000 0048h	128-stage FIFO has been included in MAC. If an entry to the transmit FIFO exceeds the threshold, the transfer of data from internal to the transmit FIFO stops. It is the threshold to prevent TX overflow. Set the value to 65 or higher.
A00C 8028h A00C A028h	TX_SECTION_FULL0 TX_SECTION_FULL1	0000 0014h	Set the number of entries required for the transmit FIFO to start transmission. Set the value to 17 or higher.
A00C 802Ch A00C A02Ch	RX_ALMOST_EMPTY0 RX_ALMOST_EMPTY1	0000 0008h	The value cannot be changed.
A00C 8030h A00C A030h	RX_ALMOST_FULL0 RX_ALMOST_FULL1	0000 0005h	The value cannot be changed.
A00C 8034h A00C A034h	TX_ALMOST_EMPTY0 TX_ALMOST_EMPTY1	0000 0004h	The value cannot be changed.
A00C 8038h A00C A038h	TX_ALMOST_FULL0 TX_ALMOST_FULL1	0000 0010h	The value cannot be changed.
A00C 8014h A00C A014h	FRM_LENGTH0 FRM_LENGTH1	0000 05F2h	Set the maximum allowable value of the received frame size. For example, set 1522 to respond to a frame with 1 VLAN tag. Also can be set to around 1536 with a margin.
A00C 8008h A00C A008h	COMMAND_CONFIG0 COMMAND_CONFIG1	0580 0013h	Enable the transmission and reception of MAC.

Table 29.24 Examples of Initial Settings of Hub

Address	Register	Setting Example	Description
A00C 01C8h	HUB_FLT_MAC0lo	00C2 8001h	A setting example of the switch management frame such as spanning tree. Filters MAC addresses in 01-80-c2-00-00-{00.3F}.
A00C 01CCh	HUB_FLT_MAC0hi	00C0 0000h	
A00C 01D0h	HUB_FLT_MAC1lo	0019 1B01h	A setting example of normal message of PTPv2. Filters MAC addresses in 01-1b-19-00-00-00.
A00C 01D4h	HUB_FLT_MAC1hi	00FF 0000h	
A00C 01D8h	HUB_FLT_MAC2lo	005E 0001h	A setting example of UDP/IP of PTP. Filters MAC addresses in 01-00-5e-00- 01-{80..87}.
A00C 01DCh	HUB_FLT_MAC2hi	00F8 8001h	
A00C 01E0h	HUB_FLT_MAC3lo	005E 0001h	A setting example of management frame. Filters MAC addresses in 01-00-5e-00- 00-{00..03}.
A00C 01E4h	HUB_FLT_MAC3hi	00FC 0000h	
A00C 01E8h	HUB_FLT_MAC4lo	0403 0201h	Set unicast address. A setting example is for 01-02-03-04-05-06.
A00C 01ECh	HUB_FLT_MAC4hi	00FF 0605h	
A00C 01F0h	HUB_FLT_MAC5lo	0000 0000h	A setting example when not in use.
A00C 01F4h	HUB_FLT_MAC5hi	00FF 0000h	
A00C 01F8h	HUB_FLT_MAC6lo	006C 2101h	A setting example of the beacon frame of the DLR. Frames of the MAC address (01-21-6C-00- 00-01) are forced forwarded.
A00C 01FCh	HUB_FLT_MAC6hi	01FF 0100h	
A00C 01C0h	HUB_CONTROL	0000 00AFh	Enables the hub. Set it to 0000 00A0h when not using the hub.

Table 29.25 Examples of Initial Settings of Timer Module

Address	Register	Setting Example	Description
A00C C004h	TSM_CONFIG	0000 300Bh	Enables one second arrival interrupt (bit 2) of the nanosecond-timer and interrupt generation except for test interrupt (bit 4).
A00C C008h	TSM_IRQ_STAT_ACK	0000 301Fh	Clears all interrupts.
A00C C138h	ATIM_SEC	0000 0000h	Initializes the timer. Should be set before ATIME.
A00C C124h	ATIME	0000 0000h	Initializes the timer.
A00C C12Ch	ATIME_EVT_PERIOD	3B9A CA00h	Sets to 1 second.
A00C C134h	ATIME_INC	0000 0808h	Sets the clock period. Correction is not applied.
A00C C130h	ATIME_CORR	0000 0000h	Drift correction is not applied.
A00C C120h	ATIME_CTRL	0000 00A1h	Starts the timer. Correction is not applied.
A00C C020h A00C C028h	PORT0_CTRL PORT1_CTRL	0000 0000h	Clear the timestamp control and status registers.

Table 29.26 Examples of Initial Settings of DLR Module

Address	Register	Setting Example	Description
A00C E000h	DLR_CONTROL	0000 6400h	Sets the clock period of the timeout timer. Disables the DLR function.
A00C E008h	DLR_ETH_TYP	0000 80E1h	Sets EtherType of DLR frame.
A00C E00Ch	DLR_IRQ_CTRL	0000 0000h	Does not generate DLR interrupt.
A00C E010h	DLR_IRQ_STAT_ACK	0000 FFFFh	Clears all interrupt.
A00C E014h	LOC_MAClo	0403 0201h	Set unicast address. A setting example is for 01-02-03-04-05-06.
A00C E018h	LOC_MAChi	0000 0605h	

29.4.3 Address Table Setting

29.4.3.1 Definition of Block Entry of Address Table

When the hardware receives frames, it searches the address table to find the destination port(s) the frame should be forwarded to. Software is not involved in the forwarding process and all frame processing is performed in hardware. Software, however, takes care of the address table initialization and management. This software task does not require a high priority. However, during operations, a low priority software task is required to continually check for learning data and add MAC addresses to the table or delete old entries when they are out of use for a longer time.
The hardware operates on hash values for an immediate search for the address table. A hash value is used directly as starting address to the address table to search for entries. The next 8 entries starting address are targeted for a linear search to find the MAC address. This is a system called “block entry”.
When the address table is small, the individual per-hash blocks of 8 entries do overlap. The hardware however does not distinguish and will always search all 8 entries starting with the first entry that is pointed to by the hash value. This allows efficient storage in a smaller table without the need to reduce the per hash entries available in a block.
Figure 29.22 shows the principle of the address table layout. The software designer needs to understand this when writing the learning and aging functions.

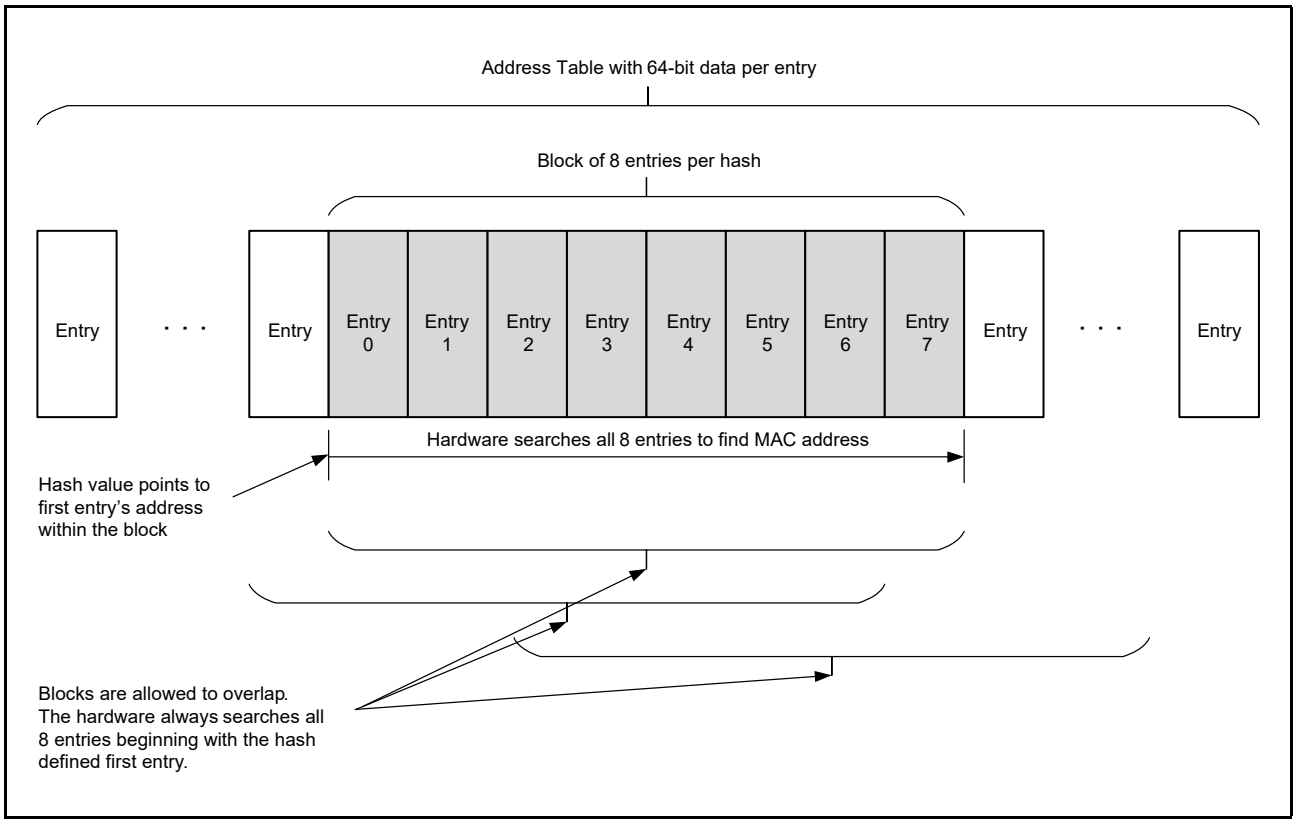


Figure 29.22 Entries of Address Table and Definition of Hash Block

29.4.3.2 Address Learning

The address table is used by the switch forwarding hardware to understand at which destination ports the frame must be transmitted. The hardware automatically looks into the table when it receives frames to determine its destinations. The software is responsible for keeping the table current and inserting the forwarding information that is then used by the hardware.

The software learning function is a low priority background task, which continuously keeps inspecting the learning data (retrieving source address and port number of received frames) and updates the address table whenever a new address is found.

Learning includes the following steps:

- Read data from the learning interface (through registers LRN_REC_A and LRN_REC_B): The data records include a hash value, which is used as the start address where the entries in the address table should be found.
- From the hash-generated start address, search through the 8 entries and update the aging time if the entry is already in the table (or update the port number to implement migration).
- If the entry is not found in any of the 8 entries in the address table, the entry is a new entry that must be added. Adding a new entry is either done into an unused position of the 8 entries, or overwriting a current entry (e.g. random, or the oldest).

Figure 29.23 shows the individual steps in learning and how an address table control function should be implemented. Implement the address learning task with reference to this flowchart.

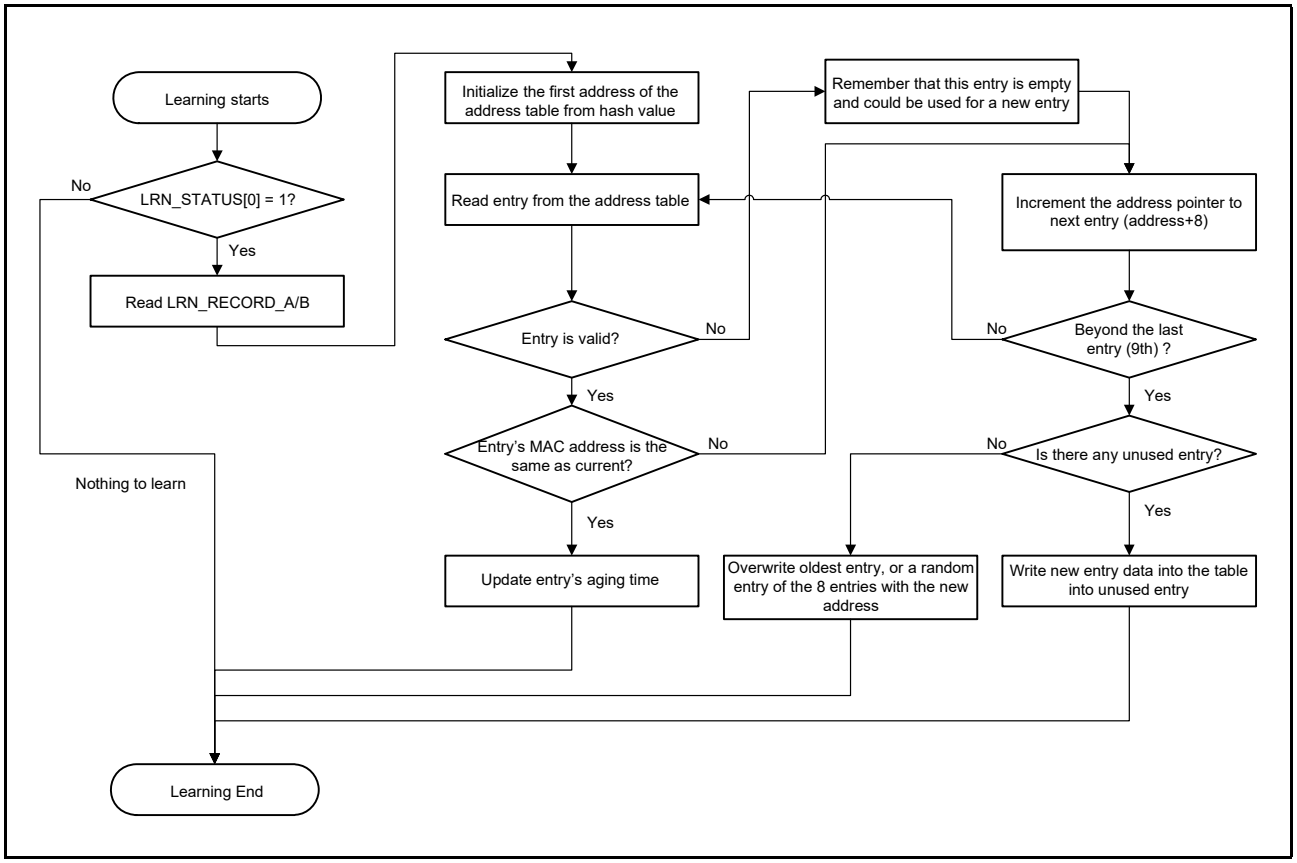


Figure 29.23 Address Learning Flow

29.4.4 Setting of Module Stop Function

Ethernet switch functions are stopped at the initial state. To use any of these functions, set the MSTPCRB.MSTPCRB14 bit and release the module stop function. Note that setting the module stop function again after releasing the function is prohibited. Operations after the second release of the function is not guaranteed. It is possible to release the module stop function after returning to the initial state (stop state) by a reset.

30. EtherCAT Slave Controller (optional)

30.1 Overview

The EtherCAT slave controller (ESC) uses an EtherCAT Slave Controller IP Core made by Beckhoff Automation GmbH, Germany.
The ESC handles EtherCAT communications as an interface between the EtherCAT field bus and slave applications.

Table 30.1 Specification of the EtherCAT Slave Controller

Item	Description
Number of ports	2
FMMU	8
SyncManager	8
Process data RAM [Kbyte]	8
Distributed clocks	64 bits
EBus	No
Process data interfaces (PDI)	
Digital I/O	No
SPI slave	No
Host MPU interface	On-chip bus

Figure 30.1 is a block diagram of the EtherCAT slave controller.
This section describes the function of the registers and modules in white. The registers and modules in gray are described in section 28, Ethernet MAC (ETHERC) and section 29, Ethernet Switch. Refer to the related sections regarding the registers and modules which are needed to operate the EtherCAT slave controller.

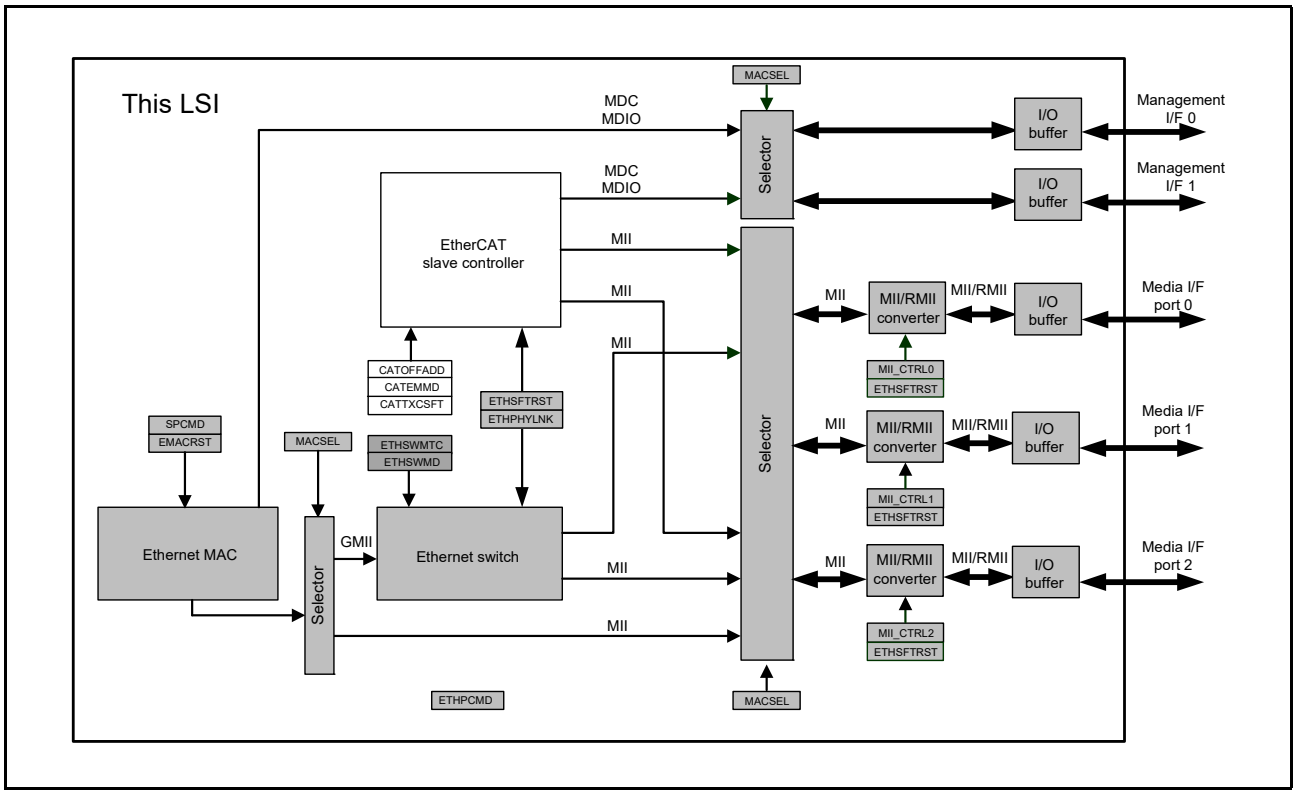


Figure 30.1 Block Diagram of the EtherCAT Slave Controller

Table 30.2 lists the input/output pins of the EtherCAT controller.

Table 30.2 Input/Output Pins of the EtherCAT Slave Controller (excluding PHY MII pins)

Pin Name	I/O	Function	Active
CATLEDRUN	O	EtherCAT RUN LED signal output port	High
CATIRQ	O	EtherCAT IRQ signal output port	High
CATLEDSTER	O	EtherCAT Dual-color State LED signal output port	High
CATLEDERR	O	EtherCAT Error LED signal output port	High
CATLINKACT0	O	EtherCAT link / Activity LED signal output port (port 0)	High
CATLINKACT1	O	EtherCAT link / Activity LED signal output port (port 1)	High
CATSYNC0	O	EtherCAT SYNC0 signal output port	High
CATSYNC1	O	EtherCAT SYNC1 signal output port	High
CATLATCH0	I	EtherCAT LATCH0 signal input port	High
CATLATCH1	I	EtherCAT LATCH1 signal input port	High
CATI2CCLK	O	EtherCAT EEPROM I2C clock output port	—
CATI2CDATA	I/O	EtherCAT EEPROM I2C data signal I/O port	—

30.2 Functional Overview

Typical functions of the EtherCAT slave controller and supported functions by this LSI are shown below. Regarding the detailed specification of EtherCAT and ESC, refer to the documentation (ETG.1000 EtherCAT Specification, etc.) provided by EtherCAT Technology Group (ETG) and the EtherCAT Slave Controller IP Core (v2.04) data sheet provided by Beckhoff Automation.

Table 30.3 Typical Functions of EtherCAT Slave Controller and Supported Functions by this LSI (1 / 3)

Features	Functions	Support
EtherCAT protocol	Handling the following frames: • Ethernet frames with Ether type 88A4h • EtherCAT frames encapsulated in UDP/IP • EtherCAT frames with VLAN Tag • Normal Ethernet frames	√
Addressing modes	Device addressing • Auto increment address • Configured station address • Broadcast address	√
	Logical addressing	√
Working counter	Counting the number of read/write from/to the device	√
EtherCAT command type	Processing the command that master requests slaves to address each addressing mode	√
Loop control	Loop control and loop state in ESC	√
Shadow buffer	Shadow buffers function when register is read/written	√
Circulating frames	Processing of circulating frames during the failure	√
Link detection	Link MII signal (PHY link signal) (monitoring the PHY register via the management interface)	√
	MI Link detection and configuration	—
	Enhanced link detection (monitoring the state of transfer by MII RX error monitor)	√
FIFO size reduction	RX FIFO size reduction because of reduction of propagation delay	√
Ethernet physical layer	MII	√
	EBUS	—
	Back-to-Back MII connection	√
	MII management interface	√
	Read/write of the PHY register via MII management interface	√
	PHY address offset	√
	Manual TX clock shift compensation	√
	Automatic TX clock shift compensation	√
FMMU	Mapping between logical address and physical address	√
SyncManager	Buffer mode	√
	Mailbox mode	√
	Interrupt and latch event generation when a buffer was completely and successfully written or read.	√
	Repeating mailbox communication	√
	SyncManager deactivation by the PDI	√

Table 30.3 Typical Functions of EtherCAT Slave Controller and Supported Functions by this LSI (2 / 3)

Features	Functions	Support
Distributed clocks	Clock Synchronization considering propagation delay and drift compensation	√
	Generation of synchronous output signals (SYNC0 and 1 signals) • Cyclic mode • Single shot mode • Cyclic acknowledge mode • Single shot acknowledge mode	√
	Precise time stamping of input events (LATCH0 and 1 signals) • Single event mode • Continuous mode • SyncManager event mode (for debugging)	√
	Generation of synchronous interrupts	√
	Synchronous digital output updates / Synchronous digital input sampling	—
	Exclusive control for the SYNC and LATCH signals of the ECAT and PDI	√
	System time control by the PDI	—
	Communication Timing • Free run • Synchronized to output event • Synchronized to SYNC signal	√
EtherCAT state machine	Control of state machine / Indication of the status and error code	√
	Device emulation	—
SII EEPROM	SII EEPROM commands	√
	SII EEPROM error indication	√
	SII EEPROM access interface	√
	EEPROM size selection	√
	EEPROM emulation	—
Interrupt	AL event request (PDI interrupt)	√
	ECAT event request (ECAT interrupt)	√
Watchdog	Process data watchdog	√
	PDI watchdog	√
Error counters	Port error counters	√
	Forwarded RX error counter	√
	ECAT processing unit error counter	√
	PDI error counter	√
	Lost link counter	√
	Watchdog counter process data	√
	Watchdog counter PDI	√
LED signals	RUN LED signal	√
	ERR LED signal	√
	STATE LED and STATE_RUN LED signals	√
	LINK/ACT LED signals	√
	Port error LED signal	—
	RUN/ERR LED override	√

Table 30.3 Typical Functions of EtherCAT Slave Controller and Supported Functions by this LSI (3 / 3)

Features	Functions	Support
Process data interface (PDI)	Digital I/O	—
	SPI slave	—
	8-bit/16-bit synchronous/asynchronous microcontroller interface	—
	On-chip bus	√
	General purpose I/O	—
Write protection	Write protection for the register area (0000h to 0FFFh)	√
	Write protection for the whole area including the user RAM and process data RAM (0000h to 2FFFh)	√
ESC reset	ESC reset from the master or PDI	√

30.3 Description of Registers

30.3.1 EtherCAT PHY Offset Address Setting Register (CATOFFADD)

This register sets the offset address of the Ethernet PHY in case of using the EtherCAT.

This register can be read/written in 32-bit units.

Note: This register can only be written when protection is unlocked by the specific sequence using the Ethernet system protect command register (ETSPCMD). For the ETSPCMD register, see section 28, Ethernet MAC (ETHERC). For the protection unlock procedure, see section 28.2.1.3, Ethernet System Protect Command Register (ETSPCMD). The special sequence is not necessary in case of reading the value of this register.

Address(es): A00B F100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	OADD4	OADD3	OADD2	OADD1	OADD0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	OADD4 to OADD0	PHY Offset Address Setting	Set the offset address of PHY of using the EtherCAT.	R/W
b31 to b5	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R/W

30.3.2 EtherCAT Operation Mode Setting Register (CATEMMD)

This register sets the EEPROM memory size in case of using the EtherCAT.

This register can be read/written in 32-bit units.

Note: This register can only be written when protection is unlocked by the specific sequence using the Ethernet system protect command register (ETSPCMD). For the protection unlock procedure, see section 28.2.1.3, Ethernet System Protect Command Register (ETSPCMD). The special sequence is not necessary in case of reading the value of this register.

Address(es): A00B F104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EEPROMSIZE
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	EEPROMSIZE	EEPROM Memory Size Specification	Sets the size of the EEPROM memory of the EtherCAT. 0: 16 Kbits or less 1: 32 Kbits to 4 Mbits	R/W
b31 to b1	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R/W

30.3.3 EtherCAT TXC Shift Setting Register (CATTXCSFT)

This register controls the delay time of TXC. This register can be read/written in 32-bit units.

Note: This register can only be written when protection is unlocked by the specific sequence using the Ethernet system protect command register (ETSPCMD). For the protection unlock procedure, see section 28.2.1.3, Ethernet System Protect Command Register (ETSPCMD). The special sequence is not necessary in case of reading the value of this register.

Address(es): A00B F10Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	TXSFT11	TXSFT10	TXSFT01	TXSFT00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b1 to b0	TXSFT01, TXSFT00	ETH0_TXC Delay Time Setting	Set the delay time for ETH0_TXC of the EtherCAT. 00: 0 ns 01: 10 ns 10: 20 ns 11: 30 ns	R/W
b3 to b2	TXSFT11, TXSFT10	ETH1_TXC Delay Time Setting	Set the delay time for ETH1_TXC of the EtherCAT. 00: 0 ns 01: 10 ns 10: 20 ns 11: 30 ns	R/W
b31 to b4	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R/W

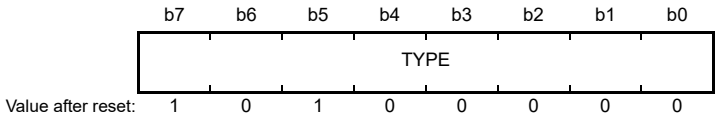
30.4 ESC Information Register

In the tables, ECAT indicates access by the EtherCAT master controller and PDI indicates access by the local CPU.

30.4.1 Type Register (TYPE)

This register indicates the type of the EtherCAT slave controller.

Address(es): A00D 0000h

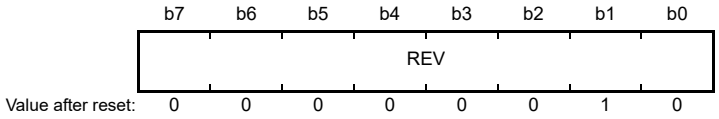


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	TYPE	Slave Controller Type Indication	Type of the EtherCAT slave controller	R	R

30.4.2 Revision Register (REVISION)

This register indicates the revision of the EtherCAT slave controller.

Address(es): A00D 0001h

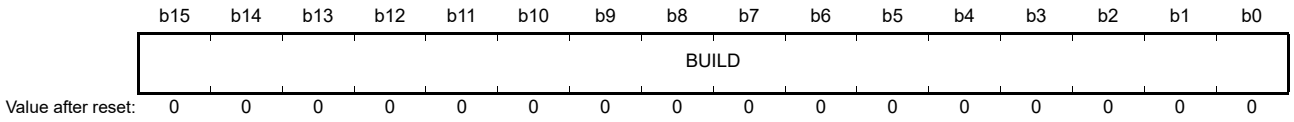


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	REV	Slave Controller Type Indication	Revision of the EtherCAT slave controller	R	R

30.4.3 Build Register (BUILD)

This register indicates the build number of the EtherCAT slave controller.

Address(es): A00D 0002h

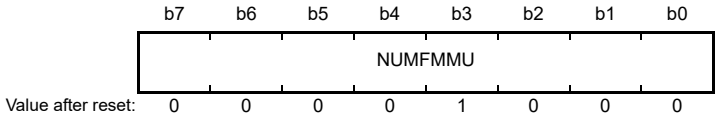


Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	BUILD	Slave Controller Build Number Indication	Build number of the EtherCAT slave controller	R	R

30.4.4 FMMU Supported Register (FMMU_NUM)

This register indicates the number of FMMU channels supported in the EtherCAT slave controller.

Address(es): A00D 0004h

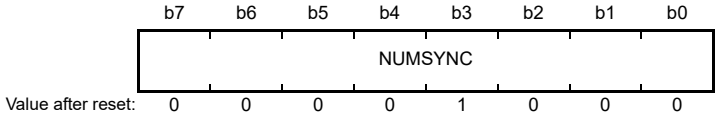


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	NUMFMMU	FMMU Channel Number Indication	Number of FMMU channels supported in the EtherCAT slave controller.	R	R

30.4.5 SyncManager Supported Register (SYNC_MANAGER)

This register indicates the number of SyncManager channels supported in the EtherCAT slave controller.

Address(es): A00D 0005h

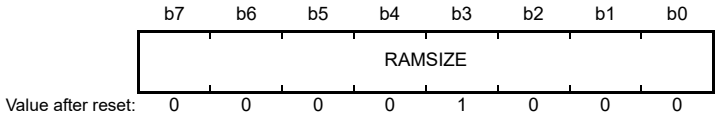


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	NUMSYNC	SyncManager Channel Number Indication	Number of SyncManager channels supported in the EtherCAT slave controller	R	R

30.4.6 RAM Size Register (RAM_SIZE)

This register indicates the process data RAM size supported in the EtherCAT slave controller in Kbyte.

Address(es): A00D 0006h



Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	RAMSIZE	Process Data RAM Size Indication	Process data RAM size supported in the EtherCAT slave controller (unit: Kbyte)	R	R

30.4.7 Port Descriptor Register (PORT_DESC)

This register indicates the port configuration.

Address(es): A00D 0007h

	b7	b6	b5	b4	b3	b2	b1	b0
	P3		P2		P1		P0	
Value after reset:	0	0	0	0	1	1	1	1

Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	P0	Port 0 Configuration	Port 0 configuration: Fixed to the setting for MII connection (11) in this LSI. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII	R	R
b3, b2	P1	Port 1 Configuration	Port 1 configuration: Fixed to the setting for MII connection (11) in this LSI. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII	R	R
b5, b4	P2	Port 2 Configuration	Port 2 configuration: This LSI does not implement port 2. Fixed to (00). 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII	R	R
b7, b6	P3	Port 3 Configuration	Port 3 configuration: This LSI does not implement port 3. Fixed to (00). 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII	R	R

30.4.8 ESC Features Supported Register (FEATURE)

This register indicates the features supported in the EtherCAT slave controller.

Address(es): A00D 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	FSCONFIG	RWSUPP	LRW	DCSYNC	FCS	LINKDECMII	—	—	DCWID	DC	—	FMMU
Value after reset:	x	x	x	x	0	0	0	1	1	1	x	x	1	1	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	FMMU	FMMU Operation Specification	FMMU operation 0: Bit oriented 1: Byte oriented	R	R
b1	—	Reserved	When read, the value returned is undefined.	R	R
b2	DC	Distributed Clock Specification	Distributed clocks 0: Not available 1: Available	R	R
b3	DCWID	Distributed Clock Width Specification	Distributed clocks (width) 0: 32 bits 1: 64 bits	R	R
b5, b4	—	Reserved	When read, the value returned is undefined.	R	R
b6	LINKDECMII	Enhanced Link Detection Specification	Enhanced link detection in MII 0: Not available 1: Available	R	R
b7	FCS	FCS Error Specification	Separate handling of FCS errors 0: Not supported 1: Supported. Frames with wrong FCS and additional nibble will be counted separately in forwarded RX error counter.	R	R
b8	DCSYNC	DC SYNC Specification	Enhanced DC SYNC activation 0: Not available 1: Available	R	R
b9	LRW	LRW Command Support Specification	EtherCAT LRW command support 0: Supported 1: Not supported	R	R
b10	RWSUPP	Command Support Specification	EtherCAT read/write command support (BRW, APRW, FPRW) 0: Supported 1: Not supported	R	R
b11	FSCONFIG	FMMU/SyncManager Specification	Fixed FMMU/SyncManager configuration 0: Variable configuration 1: Fixed configuration	R	R
b15 to b12	—	Reserved	When read, the value returned is undefined.	R	R

30.5 Station Address Registers

30.5.1 Configured Station Address Register (STATION_ADR)

This register indicates the address used for node addressing.

Address(es): A00D 0010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NODADDR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	NODADDR	Node Addressing Address Indication	Address used for node addressing (FPxx commands)	R	R/W

30.5.2 Configured Station Alias Register (STATION_ALIAS)

This register indicates the alias address used for node addressing (FPxx commands).

Address(es): A00D 0012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NODALIADDR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	NODALIADDR	Alias Address Indication	Alias address used for node addressing (FPxx commands). The use of this alias is activated by setting bit 8 of the extended ESC DL control register (ESC_EX_DL_CONTROL at 0102h) to 1.	R/W	R

Note: The initial value, 0, is retained until the EEPROM is loaded. After that, the value becomes the value at address 0004h in the EEPROM. This value is only taken over from the EEPROM the first time the EEPROM is loaded after a power-on or reset.

30.6 Write Protection Registers

30.6.1 Write Register Enable Register (WR_REG_ENABLE)

This register is used to unlock the write protection temporarily while registers are write-protected.

Address(es): A00D 0020h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ENABLE
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ENABLE	Register Write Protection Unlock	When registers are currently being protected against writing (bit 0 is 1 in the write register protection register, WR_REG_PROTECT, at 0021h) and freely writing to registers of the given node is to be permitted, the operation to do so by writing to this register has to proceed in the same Ethernet frame and preceding the other desired writing to registers. Write protection will be reactivated once the frame period elapses (unless the value in the write register protection register is changed).	R	R/W
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.6.2 Write Register Protection Register (WR_REG_PROTECT)

This register is used to protect registers against writing. The registers in the area A00D 0000h to A00D 0FFFh are write-protected (except for the WR_REG_ENABLE register (0020h) and ESC_WR_ENABLE register (0030h)).

Address(es): A00D 0021h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PROTECT
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	PROTECT	Register Write Protection Specification	Protection of registers against writing 0: Protection disabled 1: Protection enabled	R	R/W
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.6.3 ESC Write Enable Register (ESC_WR_ENABLE)

This register is used to unlock the write protection temporarily while registers and memories are write-protected by ESC write protection.

Address(es): A00D 0030h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ENABLE
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ENABLE	Register/Memory Write Protection Unlock	When registers are currently being protected against writing by ESC write protection (bit 0 is 1 in the ESC write protection register, ESC_WR_PROTECT, at 0031h) and freely writing to registers of the given node is to be permitted, the operation to do so by writing to this register has to proceed in the same Ethernet frame and preceding the other desired writing to registers. Write protection will be reactivated once the frame period elapses (unless the value in the ESC write protection register is changed).	R	R/W
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.6.4 ESC Write Protection Register (ESC_WR_PROTECT)

This register is used to protect registers against writing. Registers and memories in the area A00D 0000h to A00D 2FFFh including the process data RAM are write-protected (except for the WR_REG_ENABLE register (0020h) and ESC_WR_ENABLE register (0030h)).

Address(es): A00D 0031h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PROTECT
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	PROTECT	Register/Memory Write Protection Specification	Protection of registers and process memories against writing 0: Protection disabled 1: Protection enabled	R	R/W
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.7 Data Link Layer Registers

30.7.1 ESC Reset ECAT Register (ESC_RESET_ECAT)

This register is used to reset the EtherCAT slave controller from the ECAT (master) by software.

When written: ESC_RESET_ECAT_W

Address(es): A00D 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	RESET_ECAT							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	RESET_ECAT	Software Reset Setting	A reset is enabled after writing 52h (“R”), 45h (“E”) and 53h (“S”) consecutively to this register.	R	R/W

When read: ESC_RESET_ECAT_R

Address(es): A00D 0040h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RESET_ECAT	
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	RESET_ECAT	Reset Progress Status	Progress of the reset procedure 01: After writing 52h 10: After writing 45h (if 52h was written before) 00: Others	R	R/W
b7 to b2	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R	R/W

30.7.2 ESC Reset PDI Register (ESC_RESET_PDI)

This register is used to reset the EtherCAT slave controller from the PDI (slave) by software.

When written: ESC_RESET_PDI_W

Address(es): A00D 0041h

	b7	b6	b5	b4	b3	b2	b1	b0
	RESET_PDI							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	RESET_PDI	Software Reset Setting	A reset is enabled after writing 52h (“R”), 45h (“E”) and 53h (“S”) consecutively to this register.	R/W	R

When read: ESC_RESET_PDI_R

Address(es): A00D 0041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RESET_PDI	
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	RESET_PDI	Reset Progress Status	Progress of the reset procedure 01: After writing 52h 10: After writing 45h (if 52h was written before) 00: Others	R/W	R
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R

30.7.3 ESC DL Control Register (ESC_DL_CONTROL)

This register is used to control loop in the EtherCAT slave controller and configure the RX FIFO size and station alias.

Address(es): A00D 0100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	STAALIAS	—	—	—	—	—	RXFIFO		
Value after reset:	x	x	x	x	x	x	x	0	x	x	x	x	x	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LP3		LP2		LP1		LP0		—	—	—	—	—	—	TEMPUSE	FWDRULE
Value after reset:	1	1	0	0	0	0	0	0	x	x	x	x	x	x	0	1

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	FWDRULE	Forwarding Rule Specification	Forwarding rule 0: EtherCAT frames are processed. Non-EtherCAT frames are forwarded without processing. 1: EtherCAT frames are processed. Non-EtherCAT frames are destroyed. The source MAC address is changed for every frame (SOURCE_MAC[1] is set to 1 (locally administered address)) regardless of the forwarding rule.	R	R/W
b1	TEMPUSE	Temporary Use of Bits 15 to 8	Temporary use of bits 15 to 8 settings 0: Permanent use 1: Use for about 1 second, then revert to previous settings	R	R/W
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R
b9, b8	LP0	Loop Port 0 Configuration	Loop port 0 configuration 00: Auto 01: Auto close 10: Open 11: Closed	R	R/W
b11, b10	LP1	Loop Port 1 Configuration	Loop port 1 configuration 00: Auto 01: Auto close 10: Open 11: Closed	R	R/W
b13, b12	LP2	Loop Port 2 Configuration	Loop port 2 configuration (port 2 is not available on this LSI.) 00: Auto 01: Auto close 10: Open 11: Closed	R	R/W
b15, b14	LP3	Loop Port 3 Configuration	Loop port 3 configuration (port 3 is not available on this LSI.) 00: Auto 01: Auto close 10: Open 11: Closed	R	R/W
b18 to b16	RXFIFO	RX FIFO Size Specification	Set the RX FIFO size. The transfer time can be reduced by reducing the FIFO size. 0 to 3: Shortened by 40 ns 4 to 6: No change 7: Default	R	R/W
b23 to b19	—	Reserved	When read, the value returned is undefined.	R	R

Bit	Symbol	Bit Name	Description	PDI	ECAT
b24	STAALIAS	Station Alias Status Specification	Station alias 0: Ignore station alias 1: Alias can be used for all configured address command types (FPRD, FPWR, ...).	R	R/W
b31 to b25	—	Reserved	When read, the value returned is undefined.	R	R

Note: Changes to loop configurations are delayed until any current reception or transmission of a frame through the port is completed.
Note: Reducing the size of the Rx FIFO depends on all masters and slaves connected to the same network as the EtherCAT having very precise clock sources. An Rx FIFO size of 7 (default) is sufficient if the precision of all clocks is 100 ppm or better and Rx FIFO sizes of 0 to 3 are possible if the precision is 25 ppm or better.

30.7.4 Physical Read/Write Offset Register (PHYSICAL_RW_OFFSET)

This register is used to set the offset between read address and write address in the R/W commands.

Address(es): A00D 0108h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RWOFFSET															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	RWOFFSET	Offset between Read and Write Addresses	Offset of R/W commands (FPRW, APRW) between read address and write address. That is, in the case of reading, RD_ADR = ADR (the given address is read) In the case of writing, WR_ADR = ADR + R/W offset (writing is to the address obtained by adding the offset set in this register to the given address)	R	R/W

30.7.5 ESC DL Status Register (ESC_DL_STATUS)

This register indicates the state of the EtherCAT slave controller.

Address(es): A00D 0110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COMP3	LP3	COMP2	LP2	COMP1	LP1	COMP0	LP0	PHYP3	PHYP2	PHYP1	PHYP0	—	ENHLINKD	PDIWDST	PDIOPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	x	1	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	PDIOPE	PDI/EEPROM Load State Indication	PDI operation/EEPROM load state 0: EEPROM not loaded, the PDI not operational (process data RAM is not accessible) 1: EEPROM loaded correctly, the PDI operational (process data RAM is accessible)	R	R (ack)
b1	PDIWDST	Watchdog Status	PDI watchdog timer status 0: Timeout of the watchdog timer 1: Watchdog timer reloaded	R	R (ack)
b2	ENHLINKD	Enhanced Link Detection Indication	Enhanced link detection 0: Deactivated for all ports 1: Activated for at least one port Note: This bit is set to the value of bit 9 at address 0000h in the EEPROM the first time the EEPROM is loaded after power is initially supplied or after a reset.	R	R (ack)
b3	—	Reserved	When read, the value returned is undefined.	R	R (ack)
b4	PHYP0	Port 0 Link State Indication	Physical link on port 0 0: No link 1: Link detected	R	R (ack)
b5	PHYP1	Port 1 Link State Indication	Physical link on port 1 0: No link 1: Link detected	R	R (ack)
b6	PHYP2	Port 2 Link State Indication	Physical link on port 2 (port 2 is not available on this LSI.) 0: No link 1: Link detected	R	R (ack)
b7	PHYP3	Port 3 Link State Indication	Physical link on port 3 (port 3 is not available on this LSI.) 0: No link 1: Link detected	R	R (ack)
b8	LP0	Loop Port 0 State Indication	Loop port 0 0: Open 1: Closed	R	R (ack)
b9	COMP0	Port 0 Communication State Indication	Communication on port 0 0: No stable communication 1: Communication established	R	R (ack)
b10	LP1	Loop Port 1 State Indication	Loop port 1 0: Open 1: Closed	R	R (ack)
b11	COMP1	Port 1 Communication State Indication	Communication on port 1 0: No stable communication 1: Communication established	R	R (ack)
b12	LP2	Loop Port 2 State Indication	Loop port 2 (port 2 is not available on this LSI.) 0: Open 1: Closed	R	R (ack)
b13	COMP2	Port 2 Communication State Indication	Communication on port 2 (port 2 is not available on this LSI.) 0: No stable communication 1: Communication established	R	R (ack)

Bit	Symbol	Bit Name	Description	PDI	ECAT
b14	LP3	Loop Port 3 State Indication	Loop port 3 (port 3 is not available on this LSI.) 0: Open 1: Closed	R	R (ack)
b15	COMP3	Port 3 Communication State Indication	Communication on port 3 (port 3 is not available on this LSI.) 0: No stable communication 1: Communication established	R	R (ack)

Note: Reading this register from the ECAT clears bit 2 of the ECAT event request register (ECAT_EVENT_REQ at 0210h).

30.8 Application Layer Registers

30.8.1 AL Control Register (AL_CONTROL)

This register is used to change the state transition of the device state machine and to acknowledge error indication.

Address(es): A00D 0120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	DEVICEID	ERRINDACK	INISTATE			
Value after reset:	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	1

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b3 to b0	INISTATE	State Machine State Change Specification	Change the state transition of the device state machine. 1: Initial state request 3: Bootstrap state request 2: Pre-operational state request 4: Safe-operational state request 8: Operational state request	R (clear)	R/(W)
b4	ERRINDACK	Error Indication Acknowledge	Error indication acknowledge (response) 0: Error Indication in AL status register is not acknowledged. 1: Error Indication in AL status register is acknowledged.	R (clear)	R/(W)
b5	DEVICEID	Device ID Request	Device ID request 0: No request is present. 1: A request is present.	R (clear)	R/(W)
b15 to b6	—	Reserved	When read, the value returned is undefined.	R (clear)	R/(W)

Note: The PDI has to read the AL control register after the ECAT has written it. Otherwise the ECAT cannot write again to the AL control register. Reading the AL control register from the PDI clears bit 0 of the AL event request register (AL_EVENT_REQ at 0220h).

30.8.2 AL Status Register (AL_STATUS)

This register indicates the state of slave application.

Address(es): A00D 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	DEVICEID	ERR	ACTSTATE			
Value after reset:	x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	1

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b3 to b0	ACTSTATE	State Machine State Indication	Actual state of the device state machine 1: Initial state 3: Request bootstrap state 2: Pre-operational state 4: Safe-operational state 8: Operational state	R/(W)	R (ack)
b4	ERR	Error State Indication	Error indicator 0: The device is in the state as requested or flag was cleared by command. 1: The device has not entered the requested state or the state was changed as a result of local action.	R/(W)	R (ack)
b5	DEVICEID	Device ID Load State Indication	Device ID load state 0: Loading the device ID failed. 1: The device ID was loaded.	R/(W)	R (ack)
b15 to b6	—	Reserved	When read, the value returned is undefined.	R/(W)	R (ack)

Note: Reading this register from the ECAT clears bit 3 of the ECAT event request register (ECAT_EVENT_REQ at 0210h).

30.8.3 AL Status Code Register (AL_STATUS_CODE)

This register indicates an error code from slave application.

Address(es): A00D 0134h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	STATUSCODE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	STATUSCODE	Error Code Indication	AL status code	R/W	R

30.8.4 RUN LED Override Register (RUN_LED_OVERRIDE)

This register is used to override control of the RUN LED pin.

Address(es): A00D 0138h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OVERRIDEEN	LEDCODE			
Value after reset:	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W	PDI	ECAT
b3 to b0	LEDCODE	LED Code Indication	LED code 0h: Off 1h - Ch: Flash 1x - 12x Dh: Blinking Eh: Flickering Fh: On	(FSM state) (1-Init) (4-SafeOp 1x) (2-PreOp) (3-Bootstrap) (8-Op) Note: Bits 3 to 0 of the AL status register (AL_STATUS)	R/W	R/W
b4	OVERRIDEEN	Override Setting	Override enable 0: Override disabled 1: Override enabled		R/W	R/W
b7 to b5	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.		R/W	R/W

Note: Changing the value of the AL status register to an appropriate value will clear bit 4 (override enable).
Normally RUN LED is controlled by the AL status register (AL_STATUS at 0130h) automatically. It is not necessary to override RUN LED in order to indicate the state of a general state machine.
For example, this register can be used to run special lighting patterns that indicate the positions of specific slaves.

30.8.5 ERR LED Override Register (ERR_LED_OVERRIDE)

This register is used to override control of the error LED pin.

Address(es): A00D 0139h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OVERRIDEEN	LEDCODE			
Value after reset:	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b3 to b0	LEDCODE	LED Code Indication	LED code 0h: Off 1h to Ch: Flash 1x to 12x Dh: Blinking Eh: Flickering Fh: On	R/W	R/W
b4	OVERRIDEEN	Override Setting	Override enable 0: Override disabled 1: Override enabled	R/W	R/W
b7 to b5	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R/W	R/W

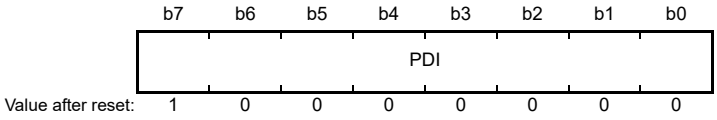
Note: Bit 4 (override enable) will be cleared if a new error occurs.
The ESC automatically controls an error LED under the conditions below. Regarding other errors, the error LED should be controlled by application using this register.
- SII EEPROM load error
- PDI watchdog timeout

30.9 PDI Registers

30.9.1 PDI Control Register (PDI_CONTROL)

This register indicates the type of PDI.

Address(es): A00D 0140h



Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	PDI	PDI Type Indication	Process data interface. In this chip, the below value is indicated. 80h: On-chip bus	R	R

30.9.2 ESC Configuration Register (ESC_CONFIG)

This register indicates configuration of the EtherCAT slave controller.

Address(es): A00D 0141h

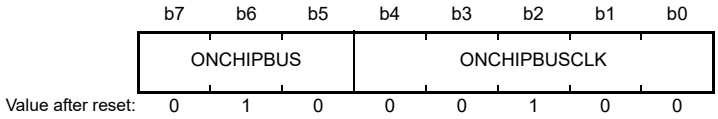
	b7	b6	b5	b4	b3	b2	b1	b0
	ENLP3	ENLP2	ENLP1	ENLP0	DCLATCH	DCSYNC	ENLALLP	DEVEMU
Value after reset:	0	0	0	0	1	1	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	DEVEMU	Device Emulation Setting	Device emulation (control of AL status) 0: The AL status register has to be set by the PDI. 1: The AL status register will be set to a value written to the AL control register.	R	R
b1	ENLALLP	All Ports Enhanced Link Detection Setting	Sets enhanced link detection for all ports. 0: Disabled (if bits 15 to 12 of address 0 in the EEPROM = 0) 1: Enabled at all ports	R	R
b2	DCSYNC	SYNC Output Unit State Indication	Sets the SYNC output unit for distributed clocks (fixed to 1 in this LSI). 0: Disabled (power saving) 1: Enabled	R	R
b3	DCLATCH	Latch Input Unit Setting	Sets the latch input unit for distributed clocks (fixed to 1 in this LSI). 0: Disabled (power saving) 1: Enabled	R	R
b4	ENLP0	Port 0 Enhanced Link Detection Setting	Sets enhanced link detection for port 0. 0: Disabled (if bit 9 of address 0 in the EEPROM = 0) 1: Enabled	R	R
b5	ENLP1	Port 1 Enhanced Link Detection Setting	Sets enhanced link detection for port 1. 0: Disabled (if bit 9 of address 0 in the EEPROM = 0) 1: Enabled	R	R
b6	ENLP2	Port 2 Enhanced Link Detection Setting	Sets enhanced link detection for port 2 (port 2 is not available on this LSI). 0: Disabled (if bit 9 of address 0 in the EEPROM = 0) 1: Enabled	R	R
b7	ENLP3	Port 3 Enhanced Link Detection Setting	Sets enhanced link detection for port 3 (port 3 is not available on this LSI). 0: Disabled (if bit 9 of address 0 in the EEPROM = 0) 1: Enabled	R	R

30.9.3 PDI Configuration Register (PDI_CONFIG)

This register indicates configuration of the PDI.

Address(es): A00D 0150h

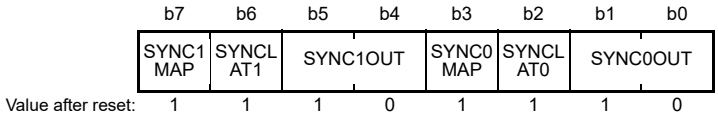


Bit	Symbol	Bit Name	Description	PDI	ECAT
b4 to b0	ONCHIPBUSCLK	On-Chip Bus Clock Indication	Indicate the frequency of the on-chip bus clock. In this chip, the value is always 4 (corresponding to 100 MHz).	R	R
b7 to b5	ONCHIPBUS	On-Chip Bus Type Indication	Indicate the type of on-chip bus. In this chip, the value is always 010.	R	R

30.9.4 SYNC/LATCH PDI Configuration Register (SYNC_LATCH_CONFIG)

This register indicates the configuration of SYNC output and LATCH input.

Address(es): A00D 0151h



Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	SYNC0OUT	SYNC0 Polarity Indication	Indicate the SYNC0 output driver/polarity. In this chip, the value is always 10 (push-pull active high).	R	R
b2	SYNCLAT0	SYNC0/LATCH0 Indication	Indicates the SYNC0/LATCH0 configuration. In this chip, the value is always 1*1. 0: LATCH0 input 1: SYNC0 output	R	R
b3	SYNC0MAP	SYNC0 State Mapping Indication	Indicates enabling or disabling of mapping of the SYNC0 state to bit 2 of the AL event request register (AL_EVENT_REQ at 0220h). This is always enabled in this chip, so the value indicated is always 1 (enabled). 0: Disabled 1: Enabled	R	R
b5, b4	SYNC1OUT	SYNC1 Polarity Indication	Indicate the SYNC1 output driver/polarity. In this chip, the value is always 10 (push-pull active high).	R	R
b6	SYNCLAT1	SYNC1/LATCH1 Indication	Indicates the SYNC1/LATCH1 configuration. In this chip, the value is always 1*1. 0: LATCH1 input 1: SYNC1 output	R	R
b7	SYNC1MAP	SYNC1 State Mapping Indication	Indicates enabling or disabling of mapping of the SYNC1 state to bit 3 of the AL event request register (AL_EVENT_REQ at 0220h). This is always enabled in this chip, so the value indicated is always 1 (enabled). 0: Disabled 1: Enabled	R	R

Note 1. Latch input is available though the value indicates SYNC output. Use the MPC function in order to switch SYNC output to LATCH input and vice versa.

30.9.5 Extended PDI Configuration Register (EXT_PDI_CONFIG)

This register indicates configuration of the PDI.

Address(es): A00D 0152h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DATABUSWID	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	DATABUSWID	PDI Data Bus Width Indication	Indicate the data bus width of the PDI. In this chip, the value is always 0 (4 bytes). 00: 4 bytes 01: 1 byte 10: 2 bytes 11: Reserved	R	R
b15 to b2	—	Reserved	When read, the value returned is undefined.	R	R

30.10 Interrupt Registers

30.10.1 ECAT Event Mask Register (ECAT_EVENT_MASK)

The ECAT event request (ECAT interrupt) is used to transmit the slave event to the EtherCAT master. This register is used to set mask to each event of the ECAT event request register (ECAT_EVENT_REQ at 0210h). The logical AND of each effective bit in the ECAT event request register and the corresponding bit of this register is taken and the result produces the interrupt signal.

Address(es): A00D 0200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECATEVMASK															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	ECATEVMASK	Event Request Mask Setting	0: The corresponding bit of the ECAT event request register (ECAT_EVENT_REQ at 0210h) is not mapped. 1: The corresponding bit of the ECAT event request register is mapped.	R	R/W

30.10.2 AL Event Mask Register (AL_EVENT_MASK)

The AL event request (PDI interrupt) is used to transmit the ESC interrupt to the slave application. This register is used to set mask to each event of the AL event request register (AL_EVENT_REQ at 0220h). The logical AND of each effective bit in the AL event request register and the corresponding bit of this register is taken and the result produces the interrupt signal.

Address(es): A00D 0204h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ALEVMASK															
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ALEVMASK															
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	ALEVMASK	Event Request Mask Setting	0: The corresponding bit of the AL event request register (AL_EVENT_REQ at 0220h) is not mapped. 1: The corresponding bit of the AL event request register is mapped.	R/W	R

30.10.3 ECAT Event Request Register (ECAT_EVENT_REQ)

This register indicates the source of ECAT event requests (ECAT interrupts).

Address(es): A00D 0210h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SMSTA7	SMSTA6	SMSTA5	SMSTA4	SMSTA3	SMSTA2	SMSTA1	SMSTA0	ALSTA	DLSTA	—	DCLATCH
Value after reset:	x	x	x	x	0	0	0	0	0	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	DCLATCH	DC Latch Event State Indication	DC latch event 0: No change on DC latch Inputs 1: At least one change on DC latch Inputs This bit is cleared by reading DC latch event times from the ECAT for ECAT controlled latch units, so the latch 0 and 1 status registers (DC_LATCH_STAT0 and DC_LATCH_STAT1 at 09AEh and 09AFh) indicate no event.	R	R
b1	—	Reserved	When read, the value returned is undefined.	R	R
b2	DLSTA	DL Status Event State Indication	DL status event 0: No change in DL status 1: DL status change This bit is cleared by reading out the DL status register (ESC_DL_STATUS at 0110h or 0111h) from the ECAT.	R	R
b3	ALSTA	AL Status Event State Indication	AL status event 0: No change in AL status 1: AL status change This bit is cleared by reading out the AL status register (AL_STATUS at 0130h or 0131h) from the ECAT.	R	R
b4	SMSTA0	SyncManager 0 Status Indication	Mirror value of SyncManager 0 status 0: No Sync channel 0 event 1: Sync channel 0 event pending	R	R
b5	SMSTA1	SyncManager 1 Status Indication	Mirror value of SyncManager 1 status 0: No Sync channel 1 event 1: Sync channel 1 event pending	R	R
b6	SMSTA2	SyncManager 2 Status Indication	Mirror value of SyncManager 2 status 0: No Sync channel 2 event 1: Sync channel 2 event pending	R	R
b7	SMSTA3	SyncManager 3 Status Indication	Mirror value of SyncManager 3 status 0: No Sync channel 3 event 1: Sync channel 3 event pending	R	R
b8	SMSTA4	SyncManager 4 Status Indication	Mirror value of SyncManager 4 status 0: No Sync channel 4 event 1: Sync channel 4 event pending	R	R
b9	SMSTA5	SyncManager 5 Status Indication	Mirror value of SyncManager 5 status 0: No Sync channel 5 event 1: Sync channel 5 event pending	R	R
b10	SMSTA6	SyncManager 6 Status Indication	Mirror value of SyncManager 6 status 0: No Sync channel 6 event 1: Sync channel 6 event pending	R	R
b11	SMSTA7	SyncManager 7 Status Indication	Mirror value of SyncManager 7 status 0: No Sync channel 7 event 1: Sync channel 7 event pending	R	R
b15 to b12	—	Reserved	When read, the value returned is undefined.	R	R

30.10.4 AL Event Request Register (AL_EVENT_REQ)

This register indicates the source of AL event requests (PDI interrupts).

Address(es): A00D 0220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SMINT 7	SMINT 6	SMINT 5	SMINT 4	SMINT 3	SMINT 2	SMINT 1	SMINT 0	—	WDPD	—	SYNCA CT	DCSYN C1STA	DCSYN C0STA	DCLAT CH	ALCTR L
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ALCTRL	AL Control Event State Indication	AL control event 0: No change in the AL control register 1: The AL control register has been written. This bit is cleared by reading the AL control register (AL_CONTROL at 0120h or 0121h) from the PDI.	R	R
b1	DCLATCH	DC Latch Event State Indication	DC latch event 0: No change on DC latch Inputs 1: At least one change on DC latch inputs This bit is cleared by reading DC latch event times from the PDI for PDI controlled latch units, so the latch 0 and 1 status registers (DC_LATCH_STAT0 and DC_LATCH_STAT1 at 09AEh and 09AFh) indicate no event.	R	R
b2	DCSYNC0STA	DC SYNC0 State Indication	State of DC SYNC0 This bit is cleared by reading the SYNC0 status register (DC_SYNC0_STAT at 098Eh) from the PDI.	R	R
b3	DCSYNC1STA	DC SYNC1 State Indication	State of DC SYNC1 This bit is cleared by reading the SYNC1 status register (DC_SYNC1_STAT at 098Fh) from the PDI.	R	R
b4	SYNCACT	SyncManager Activation Indication	Change of the SyncManager activation register (SMm.ACT at 0806h + 8h*m) 0: No change in any SyncManager 1: At least one SyncManager changed This bit is cleared by reading SyncManager activation registers from the PDI.	R	R
b5	—	Reserved	When read, the value returned is undefined.	R	R
b6	WDPD	Watchdog Process Data Indication	Watchdog process data 0: Valid 1: Timeout This bit is cleared by reading the watchdog status process data register (WDS_DATA at 0440h) from the PDI.	R	R
b7	—	Reserved	When read, the value returned is undefined.	R	R
b8	SMINT0	SyncManager 0 Interrupt Status	SyncManager 0 interrupt (bit 0 or 1 of the SyncManager status register (0805h)) 0: No SyncManager 0 interrupt 1: SyncManager 0 interrupt pending	R	R
b9	SMINT1	SyncManager 1 Interrupt Status	SyncManager 1 interrupt (bit 0 or 1 of the SyncManager status register (080Dh)) 0: No SyncManager 1 interrupt 1: SyncManager 1 interrupt pending	R	R
b10	SMINT2	SyncManager 2 Interrupt Status	SyncManager 2 interrupt (bit 0 or 1 of the SyncManager status register (0815h)) 0: No SyncManager 2 interrupt 1: SyncManager 2 interrupt pending	R	R

Bit	Symbol	Bit Name	Description	PDI	ECAT
b11	SMINT3	SyncManager 3 Interrupt Status	SyncManager 3 interrupt (bit 0 or 1 of the SyncManager status register (081Dh)) 0: No SyncManager 3 interrupt 1: SyncManager 3 interrupt pending	R	R
b12	SMINT4	SyncManager 4 Interrupt Status	SyncManager 4 interrupt (bit 0 or 1 of the SyncManager status register (0825h)) 0: No SyncManager 4 interrupt 1: SyncManager 4 interrupt pending	R	R
b13	SMINT5	SyncManager 5 Interrupt Status	SyncManager 5 interrupt (bit 0 or 1 of the SyncManager status register (082Dh)) 0: No SyncManager 5 interrupt 1: SyncManager 5 interrupt pending	R	R
b14	SMINT6	SyncManager 6 Interrupt Status	SyncManager 6 interrupt (bit 0 or 1 of the SyncManager status register (0835h)) 0: No SyncManager 6 interrupt 1: SyncManager 6 interrupt pending	R	R
b15	SMINT7	SyncManager 7 Interrupt Status	SyncManager 7 interrupt (bit 0 or 1 of the SyncManager status register (083Dh)) 0: No SyncManager 7 interrupt 1: SyncManager 7 interrupt pending	R	R
b31 to b16	—	Reserved	When read, the value returned is undefined.	R	R

30.11 Error Counter Registers

30.11.1 Rx Error Counter n Register (RX_ERR_COUNTn)

This register counts RX frame errors.

Address(es): A00D 0300h + 0002h*n

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RXERRCNT								INVFRMCNT							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	INVFRMCNT	Invalid Frame Counter Value Indication	Counter value of invalid frames for port n Counting is stopped when FFh is reached. These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written.	R	R/W (clr)
b15 to b8	RXERRCNT	RX Frame Error Counter Value Indication	Counter value of RX errors for port n Counting is stopped when FFh is reached. The number of RX errors of MII interface is counted. These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written.	R	R/W (clr)

n = 0, 1
n = 0 for port 0; n = 1 for port 1

30.11.2 Forwarded Rx Error Counter n Register (FWD_RX_ERR_COUNTn)

This register counts forwarded RX frame errors.

Address(es): A00D 0308h + 0001h*n

	b7	b6	b5	b4	b3	b2	b1	b0
	FWDERRCNT							
Value after reset:	0	0	0	0	0	0	0	0

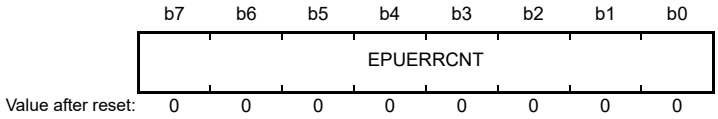
Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	FWDERRCNT	Forwarded Error Counter Value Indication	Counter value of forwarded RX error frames for port n Counting is stopped when FFh is reached. These bits are cleared if one of the RX error counters (RX_ERR_COUNTn, FWD_RX_ERR_COUNTn) is written.	R	R/W (clr)

n = 0, 1
n = 0 for port 0; n = 1 for port 1

30.11.3 ECAT Processing Unit Error Counter Register (ECAT_PROC_ERR_COUNT)

This register counts frame errors passing the ECAT processing unit.

Address(es): A00D 030Ch

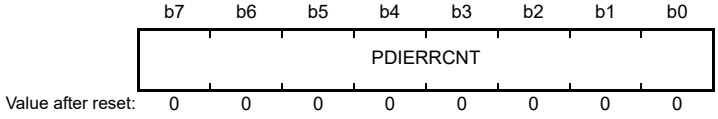


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	EPUERRCNT	Processing Unit Error Counter Value Indication	ECAT processing unit error counter value Counting is stopped when FFh is reached. This register counts errors of frames passing the processing unit. Writing to this register clears it.	R	R/W (clr)

30.11.4 PDI Error Counter Register (PDI_ERR_COUNT)

This register counts PDI access errors.

Address(es): A00D 030Dh

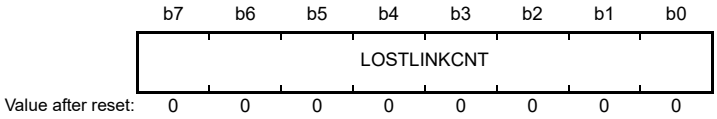


Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	PDIERRCNT	PDI Error Counter Value Indication	PDI error counter value Counting is stopped when FFh is reached. Counting starts when an interface error occurs due to access to the PDI. Writing to this register clears it.	R	R/W (clr)

30.11.5 Lost Link Counter n Register (LOST_LINK_COUNTn)

This register counts lost links at port n.

Address(es): A00D 0310h + 0001h*n



Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	LOSTLINKCNT	Lost Link Counter Value Indication	Lost link counter value for port n Counting is stopped when FFh is reached. Counting starts only when port loop is Auto or Auto-Close. Only lost links at open ports are counted. Writing to one of the lost link counter registers clears it.	R	R/W (clr)

n = 0, 1

n = 0 for port 0; n = 1 for port 1

30.12 Watchdog Registers

30.12.1 Watchdog Divider Register (WD_DIVIDE)

This register is used to set the ratio for dividing 25 MHz to obtain the basic period for incrementing the watchdog timer.

Address(es): A00D 0400h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WDDIV															
Value after reset:	0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	WDDIV	Watchdog Clock Frequency Divisor Setting	Set the frequency divisor of the clock to drive counting by the watchdog timer in units of ticks at 25 MHz. The clock that drives counting by the watchdog timer is obtained by dividing 25 MHz by the value in this register plus two. The default value is 2498, which corresponds to a period of 100 µs.	R	R/W

30.12.2 Watchdog Time PDI Register (WDT_PDI)

This register is used to set the time until the PDI watchdog timer overflows.

Address(es): A00D 0410h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WDTIMPDI															
Value after reset:	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	WDTIMPDI	Watchdog Overflow Time Setting	Set the time until the PDI watchdog timer overflows as a number of times the watchdog is incremented. With the default values for these bits and the setting of the watchdog divider, the time for a single incrementation is 100 µs, so the watchdog timer overflows when 100 µs x 1000 = 100 ms elapse. Setting these bits to 0 disables the watchdog timer. Access to the PDI restarts the watchdog timer.	R	R/W

30.12.3 Watchdog Time Process Data Register (WDT_DATA)

This register is used to set the time until the process data watchdog timer overflows.

Address(es): A00D 0420h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WDTIMPD															
Value after reset:	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	WDTIMPD	Watchdog Overflow Time Setting	Set the time until the process data watchdog timer overflows as a number of times the watchdog is incremented. With the default values for these bits and the setting of the watchdog divider, the time for a single incrementation is 100 µs, so the watchdog timer overflows when 100 µs x 1000 = 100 ms elapse. There is one Watchdog for all SyncManagers. Setting these bits to 0 disables the watchdog timer. Access to the watchdog trigger enable bit of SyncManager restarts the watchdog timer.	R	R/W

30.12.4 Watchdog Status Process Data Register (WDS_DATA)

This register indicates the state of the process data watchdog timer.

Address(es): A00D 0440h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WDSTAPD
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	WDSTAPD	Watchdog State Indication	Indicates the state of the process data watchdog timer triggered by SyncManagers. 0: The timeout period of the process data watchdog timer elapses. 1: The process data watchdog timer is active or disabled Reading this register clears bit 6 of the AL event request register (AL_EVENT_REQ at 0220h).	R (ack)	R
b15 to b1	—	Reserved	When read, the value returned is undefined.	R (ack)	R

30.12.5 Watchdog Counter Process Data Register (WDC_DATA)

This register indicates the timeout counter value of the process data watchdog timer.

Address(es): A00D 0442h

	b7	b6	b5	b4	b3	b2	b1	b0
	WDCNTPD							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	WDCNTPD	Watchdog Counter Value Indication	Counter value of the process data watchdog timer Counting stops when FFh is reached. Counting starts on a timeout of the process data watchdog timer. Writing to one of the watchdog counter registers (WDC_DATA, WDC_PDI at 0442h and 0443h) clears the counter.	R	R/W (clr)

30.12.6 Watchdog Counter PDI Register (WDC_PDI)

This register indicates the timeout counter value of the PDI watchdog timer.

Address(es): A00D 0443h

	b7	b6	b5	b4	b3	b2	b1	b0
	WDCNTPDI							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b7 to b0	WDCNTPDI	Watchdog Counter Value Indication	Counter value of the PDI watchdog timer Counting stops when FFh is reached. Counting starts on a timeout of the PDI watchdog timer. Writing to one of the watchdog counter registers (WDC_DATA, WDC_PDI at 0442h and 0443h) clears the counter.	R	R/W (clr)

30.13 SII EEPROM Interface Registers

The EtherCAT controls the SII EEPROM interface if bit 0 is 0 in the EEPROM configuration register (EEP_CONF at 0500h) and in the EEPROM PDI access state register (EEP_PDI_ACCESS at 0501h). Otherwise, the PDI controls the EEPROM interface.

30.13.1 EEPROM Configuration Register (EEP_CONF)

This register is used to configure EEPROM access.

Address(es): A00D 0500h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FORCE ECAT	CTRLP DI
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	CTRLPDI	PDI EEPROM Control	Specifies whether EEPROM control is offered to the PDI. 0: The PDI has no EEPROM control. 1: The PDI has EEPROM control.	R	R/W
b1	FORCEECAT	EEPROM Access Right Change	Forcibly changes the right of access to the EEPROM by the ECAT. 0: No change 1: Reset bit 0 of the EEPROM PDI access state register (EEP_PDI_ACCESS at 0501h) to 0. That is, prohibit access to the EEPROM by the PDI.	R	R/W
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R

30.13.2 EEPROM PDI Access State Register (EEP_STATE)

This register is used to set the right of access to the EEPROM by the PDI.

Address(es): A00D 0501h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PDIAC CESS
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	PDIACCESS	EEPROM Access Right Setting	Sets the right of access to the EEPROM. 0: Prohibits the PDI from access to the EEPROM. 1: The PDI has access to the EEPROM. Write access from the PDI is only possible when bit 0 is 1 and bit 1 is 0 in the EEPROM configuration register (EEP_CONF at 0500h).	R/(W)	R
b7 to b1	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R/(W)	R

30.13.3 EEPROM Control/Status Register (EEP_CONT_STAT)

This register is used to control access to the EEPROM and indicate the status.

Address(es): A00D 0502h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BUSY	WRENERR	ACKCMDERR	LOADSTA	CKSUMERR	COMMAND			PROMSIZE	READBYTE	—	—	—	—	—	ECATWREN
Value after reset:	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ECATWREN	Write Enable	ECAT write enable*2 0: Write requests are disabled. 1: Write requests are enabled. This bit is always 1 if the PDI has EEPROM control.	R	R/(W)
b5 to b1	—	Reserved	When read, the value returned is undefined.	R	R
b6	READBYTE	EEPROM Read Byte Indication	Indicates supported EEPROM read bytes. 0: 4 bytes 1: 8 bytes	R	R
b7	PROMSIZE	EEPROM Algorithm Indication	Indicates the selected EEPROM algorithm. 0: 1 address byte (1-Kbit to 16-Kbit EEPROMs) 1: 2 address bytes (32-Kbit to 4-Mbit EEPROMs)	R	R
b10 to b8	COMMAND	Command Setting/ Indication	Command*2 Write: Initiates the commands below. Read: Indicates the currently executed command. Commands: 000: No command/EEPROM idle (clear error bits) 001: Read 010: Write 100: Reload Others: Reserved/invalid commands (must not be issued)	R/(W)	R/(W)
b11	CKSUMERR	Checksum Error Indication	Indicates checksum error in the ESC configuration area. 0: No error in the checksum 1: Error in the checksum	R	R
b12	LOADSTA	EEPROM Loading Status Indication	Indicates EEPROM loading status. 0: EEPROM has been loaded and device information has no problem. 1: EEPROM has not been loaded and device information is not available (EEPROM loading in progress or finished with a failure).	R	R
b13	ACKCMDERR	Acknowledge/Command Error Indication	Indicates error acknowledge/command *1 0: No error 1: Missing EEPROM acknowledge or invalid command	R	R
b14	WRENERR	Write Enable Error Indication	Indicates error write enable*1. 0: No error 1: Write command without write enable	R	R
b15	BUSY	EEPROM Interface State Indication	Indicates a busy state of the EEPROM interface. 0: The EEPROM Interface is idle. 1: The EEPROM Interface is busy.	R	R

Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 = 1).

Note 1. Error bits are cleared by writing “000” (or any valid command) to command bits b10 to b8.

Note 2. ECAT write enable bit 0 is self-cleared at the SOF of the next frame. Command bits b10 to b8 are also self-cleared after the command is executed (EEPROM busy ends).
Writing “000” to command bits b10 to b8 will also clear the error bits b14 and b13. Command bits b10 to b8 are ignored if the acknowledge/command error bit b13 is 1.

30.13.4 EEPROM Address Register (EEP_ADR)

This register is used to set the EEPROM address to be accessed.

Address(es): A00D 0504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ADDRESS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDRESS															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	ADDRESS	EEPROM Address Setting	EEPROM address 0: First word (= 16 bits) 1: Second word : Actually used EEPROM address bits: [9:0]: EEPROM size of up to 16 Kbits [17:0]: EEPROM size of 32 Kbits to 4 Mbits	R/(W)	R/(W)

Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 is 1 in the EEPROM control/status register, EEP_CONT_STAT, at 0502h).

30.13.5 EEPROM Data Register (EEP_DATA)

This register is used to set write data to the EEPROM or indicates read data from the EEPROM. It can be written in 1-word units and read in 2-word units.

Address(es): A00D 0508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	HIDATA															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LODATA															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	LODATA	EEPROM Write Data Setting	Data to be written to the EEPROM or data read from the EEPROM (lower 2 bytes)	R/(W)	R/(W)
b31 to b16	HIDATA	EEPROM Read Data Indication	Data read from the EEPROM (upper 2 bytes)	R	R

Write access depends on the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if the EEPROM interface is busy (bit 15 is 1 in the EEPROM control/status register, EEP_CONT_STAT, at 0502h).

30.14 MII Management Interface Registers

30.14.1 MII Management Control/Status Register (MII_CONT_STAT)

This register is used to control the MII management interface and to indicate the status.

Address(es): A00D 0510h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BUSY	CMDERR	READERR	—	—	—	COMMAND		PHYOFFSET					MILINK	PDICTRL	WREN
Value after reset:	0	0	0	x	x	x	0	0	0	0	0	0	0	0	1	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	WREN	Write Enable	Write enable 0: Disabled 1: Enabled This bit is always 1 if the PDI controls the MII management interface.	R	R/(W)
b1	PDICTRL	PDI Control Indication	Indicates whether the MII management interface can be controlled by the PDI. 0: Only ECAT control 1: PDI control possible The interface is controlled by the MII management ECAT access state register (MII_ECAT_ACS_STAT at 0516h) and the MII management PDI access state register (MII_PDI_ACS_STAT at 0517h).	R	R
b2	MILINK	Link Detection Availability Indication	MI link detection 0: Not available 1: Available	R	R
b7 to b3	PHYOFFSET	PHY Address Offset Indication	Indicate the PHY address offset.	R	R
b9, b8	COMMAND	Command	Command Write: Initiates the commands below. Read: Indicates the currently executed command. Commands: 00: No command/MI idle (clear error bits) 01: Read 10: Write Others: Reserved/invalid commands (must not be issued)	R/(W)	R/(W)
b12 to b10	—	Reserved	When read, the value returned is undefined.	R	R
b13	READERR	Read Error Indication	Indicates whether a read error occurred. 0: No read error 1: Read error occurred (PHY or register not available) This bit is cleared by writing to this register.	R/(W)	R/(W)
b14	CMDERR	Command Error Indication	Indicates whether a command error occurred. 0: Last command was successful 1: Invalid command or write command without write enable This bit is cleared by executing a valid command or writing “00” to command bits 9 and 8.	R	R
b15	BUSY	MII Management State Indication	Indicates that the MII management interface is busy. 0: MII management interface is idle. 1: MII management interface is busy.	R	R

Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (b15 in this register = 1).

Note: Write enable bit (b0) is self-cleared at the SOF of the next frame. Command bits (b9 and b8) are also self-cleared after the command is executed (busy ends).
Writing “00” to command bits will also clear the error bits (b14 and b13). Command bits are cleared after the command is executed.

30.14.2 PHY Address Register (PHY_ADR)

This register is used to set the PHY address.

Address(es): A00D 0512h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PHYADDR				
Value after reset:	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b4 to b0	PHYADDR	PHY Address Setting	PHY address	R/(W)	R/(W)
b7 to b5	—	Reserved	When read, the value returned is undefined.	R	R

Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 is 1 in the MII management control/status register, MII_CONT_STAT, at 0510h).

30.14.3 PHY Register Address Register (PHY_REG_ADR)

This register is used to set the PHY register address.

Address(es): A00D 0513h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PHYREGADDR				
Value after reset:	x	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b4 to b0	PHYREGADDR	PHY Address Setting	Address of PHY register	R/(W)	R/(W)
b7 to b5	—	Reserved	When read, the value returned is undefined.	R	R

Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 is 1 in the MII management control/status register, MII_CONT_STAT, at 0510h).

30.14.4 PHY Data Register (PHY_DATA)

This register is used to set data to write to PHY registers or to indicate data read from PHY registers.

Address(es): A00D 0514h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PHYREGDATA															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	PHYREGDATA	PHY Register Data Indication/Setting	PHY register read/write data	R/(W)	R/(W)

Write access depends on the assignment of the management interface (ECAT/PDI). Write access is generally blocked if the management interface is busy (bit 15 is 1 in the MII management control/status register, MII_CONT_STAT, at 0510h).

30.14.5 MII Management ECAT Access State Register (MII_ECAT_ACS_STAT)

This register is used to set the right of access to the MII management interface.

Address(es): A00D 0516h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ACSMII
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ACSMII	MII Management Interface Access Right Setting	Right of access to the MII management interface 0: Enables access to the MII management interface by the PDI. 1: Exclusive access to the MII management interface by the ECAT	R	R/(W)
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

Write access is only possible when bit 0 is 1 in the MII management PDI access state register (MII_PDI_ACS_STAT at 0517h).

30.14.6 MII Management PDI Access State Register (MII_PDI_ACS_STAT)

This register is used to set the right of access to the MII management interface.

Address(es): A00D 0517h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FORPDI	ACSMII
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ACSMII	MII Management Interface Access Right Change	Right of access to the MII management interface 0: Access to the MII management interface by the PDI 1: Access to the MII management interface by the ECAT	R/(W)	R
b1	FORPDI	PDI Access State Change	Forced change of access by the PDI (forced change of bit 0) 0: The value of bit 0 of this register is not changed. 1: The value of bit 0 of this register is reset to 0 (the right of access is changed to the ECAT)	R	R/W
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R

Write access to bit 0 from the PDI is only possible if the following two conditions are satisfied.
- Bit 0 is 0 in the MII management ECAT access state register (MII_ECAT_ACS_STAT at 0516h).
- Bit 1 is 0 in the MII management PDI access state register (MII_PDI_ACS_STAT at 0517h).

30.15 FMMU Registers

30.15.1 FMMU Logical Start Address m Register (FMMUm_L_START_ADR)

This register is used to set the logical start address within the EtherCAT address space for FMMU.

Address(es): A00D 0600h : FMMU0_L_START_ADR
A00D 0610h : FMMU1_L_START_ADR
A00D 0620h : FMMU2_L_START_ADR
A00D 0630h : FMMU3_L_START_ADR
A00D 0640h : FMMU4_L_START_ADR
A00D 0650h : FMMU5_L_START_ADR
A00D 0660h : FMMU6_L_START_ADR
A00D 0670h : FMMU7_L_START_ADR

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LSTAADR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LSTAADR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	LSTAADR	Logical Start Address Setting	Set the start of the logical address within the EtherCAT address space.	R	R/W

m = 0 to 7

30.15.2 FMMU Length m Register (FMMUm_LEN)

This register is used to set the length for FMMU area in byte units.

Address(es): A00D 0604h : FMMU0_LEN
A00D 0614h : FMMU1_LEN
A00D 0624h : FMMU2_LEN
A00D 0634h : FMMU3_LEN
A00D 0644h : FMMU4_LEN
A00D 0654h : FMMU5_LEN
A00D 0664h : FMMU6_LEN
A00D 0674h : FMMU7_LEN

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FMMULEN															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	FMMULEN	Area Size Specification	Set the area size in byte units. Address at the end of the logical address range set by the FMMU minus the address at the start of the logical address range set by the FMMU plus one	R	R/W

m = 0 to 7

30.15.3 FMMU Logical Start Bit m Register (FMMUm_L_START_BIT)

This register is used to set the start bits of the logical start address for FMMU.

Address(es): A00D 0606h : FMMU0_L_START_BIT
A00D 0616h : FMMU1_L_START_BIT
A00D 0626h : FMMU2_L_START_BIT
A00D 0636h : FMMU3_L_START_BIT
A00D 0646h : FMMU4_L_START_BIT
A00D 0656h : FMMU5_L_START_BIT
A00D 0666h : FMMU6_L_START_BIT
A00D 0676h : FMMU7_L_START_BIT

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LSTABIT		
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b2 to b0	LSTABIT	Start Bit Setting	Set the start bits of the logical start address for FMMU.	R	R/W
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.15.4 FMMU Logical Stop Bit m Register (FMMUm_L_STOP_BIT)

This register is used to set the last bits of the logical end address for FMMU.

Address(es): A00D 0607h : FMMU0_L_STOP_BIT
A00D 0617h : FMMU1_L_STOP_BIT
A00D 0627h : FMMU2_L_STOP_BIT
A00D 0637h : FMMU3_L_STOP_BIT
A00D 0647h : FMMU4_L_STOP_BIT
A00D 0657h : FMMU5_L_STOP_BIT
A00D 0667h : FMMU6_L_STOP_BIT
A00D 0677h : FMMU7_L_STOP_BIT

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LSTPBIT		
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b2 to b0	LSTPBIT	Last Bit Setting	Set the last bits of the logical end address for FMMU.	R	R/W
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.15.5 FMMU Physical Start Address m Register (FMMUm_P_START_ADR)

This register is used to set the physical start address of the ESC to which the logical start address will be mapped by the FMMU.

Address(es): A00D 0608h : FMMU0_P_START_ADR
A00D 0618h : FMMU1_P_START_ADR
A00D 0628h : FMMU2_P_START_ADR
A00D 0638h : FMMU3_P_START_ADR
A00D 0648h : FMMU4_P_START_ADR
A00D 0658h : FMMU5_P_START_ADR
A00D 0668h : FMMU6_P_START_ADR
A00D 0678h : FMMU7_P_START_ADR

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PHYSTAADR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	PHYSTAADR	Physical Start Address Setting	Set the physical start address to which the logical start address will be mapped. The address is set as an offset from the base address (A00D 0000h).	R	R/W

m = 0 to 7

30.15.6 FMMU Physical Start Bit m Register (FMMUm_P_START_BIT)

This register is used to set the start bits of the physical start address of the ESC to which the start bits of the logical start address will be mapped by the FMMU.

Address(es): A00D 060Ah : FMMU0_P_START_BIT
A00D 061Ah : FMMU1_P_START_BIT
A00D 062Ah : FMMU2_P_START_BIT
A00D 063Ah : FMMU3_P_START_BIT
A00D 064Ah : FMMU4_P_START_BIT
A00D 065Ah : FMMU5_P_START_BIT
A00D 066Ah : FMMU6_P_START_BIT
A00D 067Ah : FMMU7_P_START_BIT

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PHYSTABIT		
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b2 to b0	PHYSTABIT	Physical Start Bit Setting	Set the start bits of the physical start address to which the start bits of the logical start address will be mapped.	R	R/W
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.15.7 FMMU Type m Register (FMMUm_TYPE)

This register is used to set the type of FMMU access.

Address(es): A00D 060Bh : FMMU0_TYPE
A00D 061Bh : FMMU1_TYPE
A00D 062Bh : FMMU2_TYPE
A00D 063Bh : FMMU3_TYPE
A00D 064Bh : FMMU4_TYPE
A00D 065Bh : FMMU5_TYPE
A00D 066Bh : FMMU6_TYPE
A00D 067Bh : FMMU7_TYPE

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	WRITE	READ
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	READ	Read Access Mapping Setting	Sets the mapping for read access. 0: Disabled 1: Enabled	R	R/W
b1	WRITE	Write Access Mapping Setting	Sets the mapping for write access. 0: Disabled 1: Enabled	R	R/W
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.15.8 FMMU Activate m Register (FMMUm_ACT)

This register is used to enable or disable FMMU.

Address(es): A00D 060Ch : FMMU0_ACT
A00D 061Ch : FMMU1_ACT
A00D 062Ch : FMMU2_ACT
A00D 063Ch : FMMU3_ACT
A00D 064Ch : FMMU4_ACT
A00D 065Ch : FMMU5_ACT
A00D 066Ch : FMMU6_ACT
A00D 067Ch : FMMU7_ACT

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ACTIVATE
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	ACTIVATE	FMMU Enable/Disable	Enables or disables FMMU. 0: Disabled 1: Enabled	R	R/W
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.16 SyncManager Registers

30.16.1 SyncManager Physical Start Address m Register (SMm_P_START_ADR)

This register is used to set the physical start address for the area assigned to SyncManager.

Address(es): A00D 0800h : SM0_P_START_ADR
A00D 0808h : SM1_P_START_ADR
A00D 0810h : SM2_P_START_ADR
A00D 0818h : SM3_P_START_ADR
A00D 0820h : SM4_P_START_ADR
A00D 0828h : SM5_P_START_ADR
A00D 0830h : SM6_P_START_ADR
A00D 0838h : SM7_P_START_ADR

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SMSTAADDR															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	SMSTAADDR	Physical Start Address Setting	Specify the physical start address for the area assigned to SyncManager.	R	R/(W)

m = 0 to 7
This register can only be written when SyncManager is disabled (bit 0 is 0 in the SyncManager activate m register (SMm.ACT at 0806h+8h*m).

30.16.2 SyncManager Length m Register (SMm_LEN)

This register is used to set the size of the area assigned to SyncManager.

Address(es): A00D 0802h : SM0_LEN
A00D 080Ah : SM1_LEN
A00D 0812h : SM2_LEN
A00D 081Ah : SM3_LEN
A00D 0822h : SM4_LEN
A00D 082Ah : SM5_LEN
A00D 0832h : SM6_LEN
A00D 083Ah : SM7_LEN

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SMLEN															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	SMLEN	Area Size Setting	Set the number of bytes assigned to SyncManager. Set a value greater than 1. Otherwise, SyncManager is not activated.	R	R/(W)

m = 0 to 7
This register can only be written when SyncManager is disabled (bit 0 is 0 in the SyncManager activate m register (SMm.ACT at 0806h+8h*m).

30.16.3 SyncManager Control m Register (SMm_CONTROL)

This register is used to set operation of SyncManager.

Address(es): A00D 0804h : SM0_CONTROL
A00D 080Ch : SM1_CONTROL
A00D 0814h : SM2_CONTROL
A00D 081Ch : SM3_CONTROL
A00D 0824h : SM4_CONTROL
A00D 082Ch : SM5_CONTROL
A00D 0834h : SM6_CONTROL
A00D 083Ch : SM7_CONTROL

	b7	b6	b5	b4	b3	b2	b1	b0
	—	WDTRGEN	IRQPDI	IRQECAT	DIR		OPEMODE	
Value after reset:	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b1, b0	OPEMODE	Operating Mode Setting	Operating mode 00: Buffer mode (3 buffer mode) 10: Mailbox mode (single buffer mode) Others: Reserved	R	R/(W)
b3, b2	DIR	Transfer Direction Setting	Transfer direction 00: Read (ECAT: read access; PDI: write access) 01: Write (ECAT: write access; PDI: read access) Others: Reserved	R	R/(W)
b4	IRQECAT	ECAT Event Interrupt Setting	Enables or disables interrupts (ECAT interrupts) by the ECAT event request register (ECAT_EVENT_REQ at 0210h). 0: Disabled 1: Enabled	R	R/(W)
b5	IRQPDI	AL Event Interrupt Setting	Enables or disables interrupts (PDI interrupts) by the AL event request register (AL_EVENT_REQ at 0220h). 0: Disabled 1: Enabled	R	R/(W)
b6	WDTRGEN	Watchdog Trigger Setting	Enables or disables watchdog trigger. 0: Disabled 1: Enabled	R	R/(W)
b7	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

This register can only be written when SyncManager is disabled (bit 0 is 0 in the SyncManager activate m register (SMm.ACT at 0806h+8h*m).

30.16.4 SyncManager Status m Register (SMm_STATUS)

This register indicates the state of SyncManager.

Address(es): A00D 0805h : SM0_STATUS
A00D 080Dh : SM1_STATUS
A00D 0815h : SM2_STATUS
A00D 081Dh : SM3_STATUS
A00D 0825h : SM4_STATUS
A00D 082Dh : SM5_STATUS
A00D 0835h : SM6_STATUS
A00D 083Dh : SM7_STATUS

	b7	b6	b5	b4	b3	b2	b1	b0
	WRBUF	RDBUF	BUFFERED		MAILBOX	—	INTRD	INTWR
Value after reset:	0	0	1	1	0	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	INTWR	Write Complete Interrupt State Indication	Indicates write complete interrupt. 1: Indicates that the first byte of the buffer was read (interrupt cleared) 0: Indicates that the buffer was successfully written.	R	R
b1	INTRD	Read Complete Interrupt State Indication	Indicates read complete interrupt. 1: Indicates that the first byte of the buffer was written (interrupt cleared) 0: Indicates that the buffer was successfully read.	R	R
b2	—	Reserved	When read, the value returned is undefined.	R	R
b3	MAILBOX	Mailbox Status Indication	Indicates the mailbox status in mailbox mode. 0: Mailbox empty 1: Mailbox full This bit is not used in buffer mode.	R	R
b5, b4	BUFFERED	Buffer Status Indication	Indicates the buffer status in buffer mode (last written buffer). 00: 1st buffer 01: 2nd buffer 10: 3rd buffer 11: No buffer written This bit is not used in mailbox mode.	R	R
b6	RDBUF	Read State Indication	Indicates that the buffer is being read.	R	R
b7	WRBUF	Write State Indication	Indicates that the buffer is being written.	R	R

m = 0 to 7

30.16.5 SyncManager Activate m Register (SMm_ACT)

This register is used to set operation of SyncManager.

Address(es): A00D 0806h : SM0_ACT
A00D 080Eh : SM1_ACT
A00D 0816h : SM2_ACT
A00D 081Eh : SM3_ACT
A00D 0826h : SM4_ACT
A00D 082Eh : SM5_ACT
A00D 0836h : SM6_ACT
A00D 083Eh : SM7_ACT

	b7	b6	b5	b4	b3	b2	b1	b0
	LATCH PDI	LATCH ECAT	—	—	—	—	REPEA TREQ	SMEN
Value after reset:	0	0	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SMEN	SyncManager Enable/ Disable	Enables or disables SyncManager. 0: Disabled. Memory is accessed without SyncManager control. 1: Enabled. SyncManager is active and controls memory area set in configuration.	R (ack)	R/W
b1	REPEATREQ	Repeat Request	Repeat request Toggling of the repeat request signal means that retrying the mailbox is required (primarily used in conjunction with reading of the ECAT mailbox).	R (ack)	R/W
b5 to b2	—	Reserved	When read, the value returned is undefined.	R (ack)	R
b6	LATCHECAT	ECAT Latch Event Specification	ECAT latch event 0: No 1: Generates latch events if the EtherCAT master switches the buffers.	R (ack)	R/W
b7	LATCHPDI	PDI Latch Event Specification	PDI latch event 0: No 1: Generates latch events if the PDI switches the buffers or accesses the buffer start address.	R (ack)	R/W

m = 0 to 7
Reading this register from the PDI in all SyncManagers which have changed activation clears bit 4 of the AL event request register (AL_EVENT_REQ at 0220h).

30.16.6 SyncManager PDI Control m Register (SMm_PDI_CONT)

This register is used to set operation of SyncManager from the PDI.

Address(es): A00D 0807h : SM0_PDI_CONT
A00D 080Fh : SM1_PDI_CONT
A00D 0817h : SM2_PDI_CONT
A00D 081Fh : SM3_PDI_CONT
A00D 0827h : SM4_PDI_CONT
A00D 082Fh : SM5_PDI_CONT
A00D 0837h : SM6_PDI_CONT
A00D 083Fh : SM7_PDI_CONT

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	REPEATACK	DEACTIVE
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	DEACTIVE	SyncManager Operation Indication/Setting	Deactivates SyncManager. Read: 0: Normal operation. SyncManager is activated. 1: SyncManager is deactivated and reset. SyncManager locks access to memory area. Write: 0: Activates SyncManager. 1: Deactivates SyncManager. Note: Writing 1 is delayed until the end of a frame which is currently processed.	R/W	R
b1	REPEATACK	Repeat Acknowledge	Repeat Acknowledge If this bit is set to the same value as set by bit 0 (repeat request) of the SyncManager activate register (SMm.ACT at 0806h+8h*m), the PDI acknowledges the execution of a previous set repeat request.	R/W	R
b7 to b2	—	Reserved	When read, the value returned is undefined.	R	R

m = 0 to 7

30.17 Distributed Clock Registers

30.17.1 DC Receive Time Registers

30.17.1.1 Receive Time Port 0 Register (DC_RCV_TIME_PORT0)

Writing to this register latches the received time of frames at all ports and reading this register indicates the received time of a frame latched at port 0.

Address(es): A00D 0900h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RCVTIME0															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVTIME0															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	RCVTIME0	Receive Time Indication/ Latch	Write: A write access to this register with the BWR, APWR (any address) or FPWR (configured address) command latches the local time when each port starts to receive a frame (first start bit of preamble). Read: Indicate the local time at the beginning of reception of the last frame containing a write access to this register. Note: The time stamps cannot be read in the same frame in which this register was written.	R	R/W

30.17.1.2 Receive Time Port 1 Register (DC_RCV_TIME_PORT1)

This register indicates the received time of the frame latched at port 1.

Address(es): A00D 0904h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RCVTIME1															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVTIME1															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	RCVTIME1	Receive Time Indication	Indicate the local time when port 1 starts to receive a frame (first start bit of preamble) containing the BWR, APWR or FPWR command to the receive time port 0 register (DC_RCV_TIME_PORT0 at 0900h).	R	R

30.17.2 DC Time Loop Control Unit Registers

30.17.2.1 System Time Register (DC_SYS_TIME)

This register indicates the local copy of the system time.

Address(es): A00D 0910h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIME	System Time Indication	Access from the ECAT Read: Indicate the local copy of the system time when the frame passed the reference clock (i.e., including a system time delay). The time latched at the start of frame (SOF) is indicated. Write: A written value is compared with the local copy of the system time. The result is input to the time control loop unit.	R	R/W
			Access from the PDI Read: Indicate the local copy of the system time. The time latched when the first byte of this register was read is indicated.	R	R

30.17.2.2 Receive Time ECAT Processing Unit Register (DC_RCV_TIME_UNIT)

This register indicates the received time of a frame latched at EtherCAT processing unit.

Address(es): A00D 0918h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	RCVTIMEEPU															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	RCVTIMEEPU															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RCVTIMEEPU															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVTIMEEPU															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

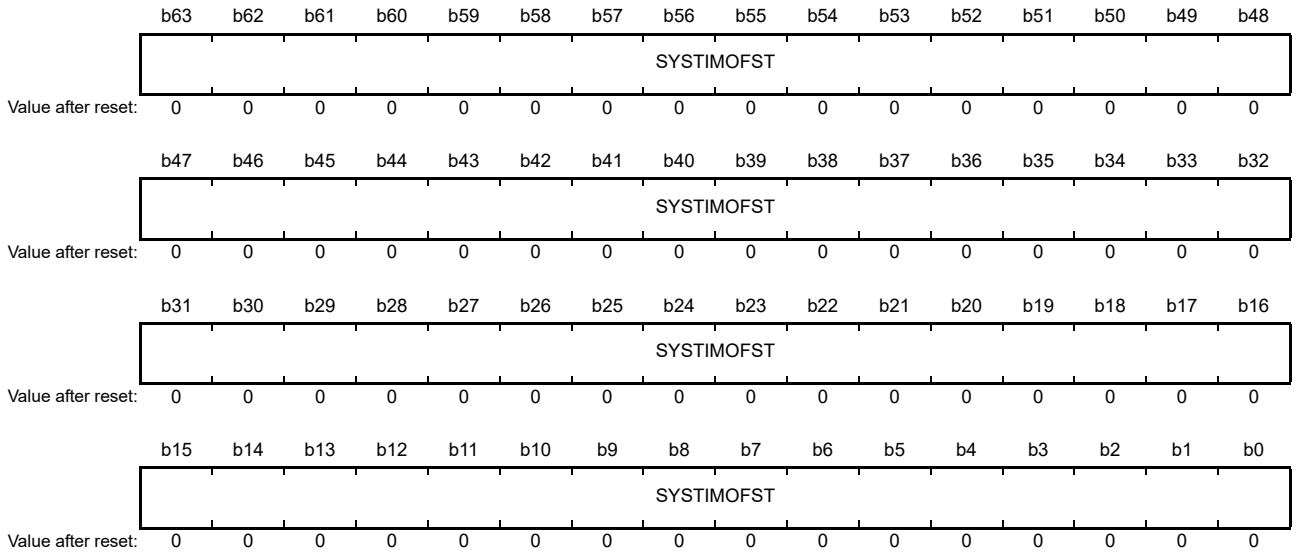
Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	RCVTIMEEPU	Receive Time Indication	This register indicates the local time at the beginning of reception by the EtherCAT processing unit of a frame (i.e. the first start bit of the preamble), including write access to the receive time port 0 register (DC_RCV_TIME_PORT0 at 0900h).	R	R

If port 0 is open, the value in this register reflects the same time as the value in the receive time port 0 register (DC_RCV_TIME_PORT0 at 0900h), but as 64 bits.

30.17.2.3 System Time Offset Register (DC_SYS_TIME_OFFSET)

This register is used to indicate a difference (offset) between the local time and system time.

Address(es): A00D 0920h

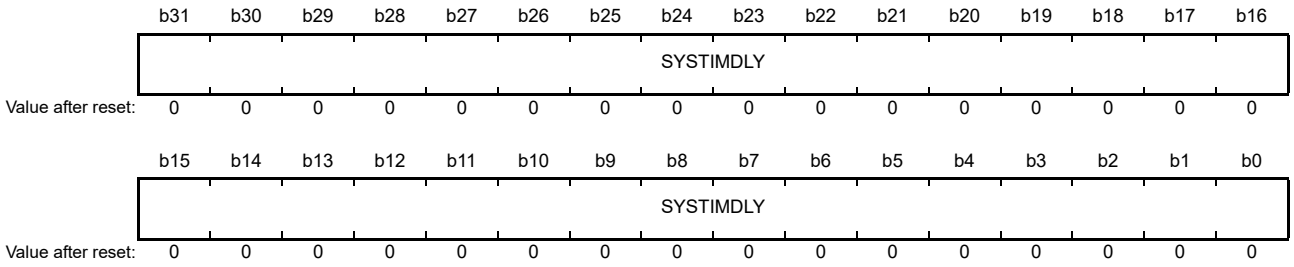


Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIMOFST	System Time and Local Time Difference Indication	Indicate a difference between the local time and system time. This offset is added to the local time to obtain the local system time.	R	R/W

30.17.2.4 System Time Delay Register (DC_SYS_TIME_DELAY)

This register indicates a propagation delay between the reference clock and slave (ESC).

Address(es): A00D 0928h

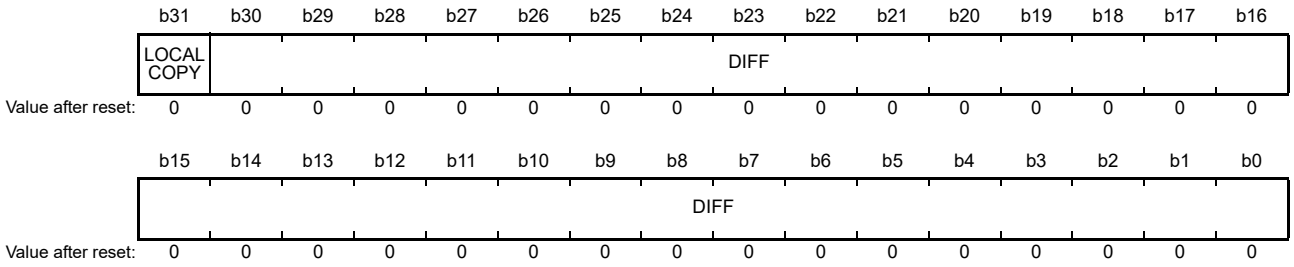


Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	SYSTIMDLY	Propagation Delay Indication	Indicate a delay between the reference clock and the ESC.	R	R/W

30.17.2.5 System Time Difference Register (DC_SYS_TIME_DIFF)

This register indicates a mean difference between the local copy of the system time and received system time.

Address(es): A00D 092Ch



Bit	Symbol	Bit Name	Description	PDI	ECAT
b30 to b0	DIFF	System Time Mean Difference Indication	Indicates a mean difference between the local copy of the system time and received system time.	R	R
b31	LOCALCOPY	System Time Greater/Less Indication	Indicates whether the local copy of the system time is greater than or equal to, or is less than, the latest received copy of the system time. 0: Local copy of the system time greater than or equal to the received system time 1: Local copy of the system time less than the received system time	R	R

30.17.2.6 Speed Counter Start Register (DC_SPEED_COUNT_START)

This register is used to set the bandwidth for drift correction of the local copy of the system time.

Address(es): A00D 0930h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPDCNTSTRT														
Value after reset:	x	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b14 to b0	SPDCNTSTRT	Drift Correction Bandwidth Setting	Indicate the bandwidth for adjustment of the local copy of the system time (larger values → smaller bandwidth and smoother adjustment). A write access resets the system time difference register (DC_SYS_TIME_DIFF at 092Ch) and the speed counter difference register (DC_SPEED_COUNT_DIFF at 0932h). Valid range: 0080h to 3FFFh	R	R/W
b15	—	Reserved	When read, the value returned is undefined. When writing to this bit, write 0.	R	R/W

30.17.2.7 Speed Counter Difference Register (DC_SPEED_COUNT_DIFF)

This register indicates the deviation between the local clock period and reference clock's clock period.

Address(es): A00D 0932h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SPDCNTDIFF															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	SPDCNTDIFF	Clock Period Deviation Indication	Indicate the deviation between the local clock period and reference clock's clock period (represented by two's complements). Range: ± (speed counter start value - 7Fh)	R	R

30.17.2.8 System Time Difference Filter Depth Register (DC_SYS_TIME_DIFF_FIL_DEPTH)

This register is used to set the filter depth for averaging the received system time deviation.

Address(es): A00D 0934h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SYSTIMDEP			
Value after reset:	x	x	x	x	0	1	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b3 to b0	SYSTIMDEP	Filter Depth Setting	Set the filter depth for averaging the received system time deviation. A write access resets the system time difference register (DC_SYS_TIME_DIFF at 092Ch).	R	R/W
b7 to b4	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R	R/W

30.17.2.9 Speed Counter Filter Depth Register (DC_SPEED_COUNT_FIL_DEPTH)

This register is used to set the filter depth for averaging the clock period deviation.

Address(es): A00D 0935h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CLKPERDEP			
Value after reset:	x	x	x	x	1	1	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b3 to b0	CLKPERDEP	Filter Depth Setting	Set the filter depth for averaging the clock period deviation. A write access resets the internal speed counter filter.	R	R/W
b7 to b4	—	Reserved	When read, the value returned is undefined. When writing to these bits, write 0.	R	R/W

30.17.3 Cyclic Unit Control Registers

30.17.3.1 Cyclic Unit Control Register (DC_CYC_CONT)

This register sets whether to control SYNC and latch units by the ECAT or PDI.

Address(es): A00D 0980h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	LATCH1	LATCH0	—	—	—	SYNCOUT
Value after reset:	x	x	0	0	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SYNCOUT	SYNC Output Unit Control Setting	Sets control of the SYNC output unit. 0: ECAT control 1: PDI control	R	R/W
b3 to b1	—	Reserved	When read, the value returned is undefined.	R	R
b4	LATCH0	Latch Input Unit 0 Control Setting	Sets control of latch input unit 0. 0: ECAT control 1: PDI control Note: Latch interrupt is routed to the ECAT or PDI in accord with this setting.	R	R/W
b5	LATCH1	Latch Input Unit 1 Control Setting	Sets control of latch input unit 1. 0: ECAT control 1: PDI control Note: Latch interrupt is routed to the ECAT or PDI in accord with this setting.	R	R/W
b7, b6	—	Reserved	When read, the value returned is undefined.	R	R

30.17.4 SYNC Output Unit Registers

30.17.4.1 Activation Register (DC_ACT)

This register is used to activate the Sync output unit.

Address(es): A00D 0981h

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGPULSE	NEARFUTURE	STARTTIME	EXTSTARTTIME	AUTOACT	SYNC1	SYNC0	SYNCACT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SYNCACT	Sync Output Unit Activation	Activates the Sync output unit. 0: Deactivated 1: Activated Note: Write 1 after the start time was written.	R/(W)	R/(W)
b1	SYNC0	SYNC0 Output Setting	Sets SYNC0 output. 0: Deactivated 1: SYNC0 pulse output is generated.	R/(W)	R/(W)
b2	SYNC1	SYNC1 Output Setting	Sets SYNC1 output. 0: Deactivated 1: SYNC1 pulse output is generated.	R/(W)	R/(W)
b3	AUTOACT	SYNC Output Unit Activation	Sets whether to activate the Sync output unit automatically by writing to the start time cyclic operation register (DC_CYC_START_TIME at 0990h): 0: Deactivated 1: Activated. Bit 0 is automatically set to 1 in this register after the start time is written.	R/(W)	R/(W)
b4	EXTSTARTTIME	Start Time Cyclic Operation Extension	Extends start time cyclic operation. 0: No extension 1: Extends the start time written with 32 bits to 64 bits	R/(W)	R/(W)
b5	STARTTIME	Start Time Plausibility	Selects whether checking the plausibility of the start time and response to implausible start times is to proceed. 0: Disabled. Sync signal is generated if the start time is reached. 1: Sync signal is generated immediately if the start time is outside the range of the near future.	R/(W)	R/(W)
b6	NEARFUTURE	Near Future Range Setting	Sets the range to be considered the near future. 0: Up to 2^{63} ns from now (1/2 of the DC width) 1: Up to 2^{31} ns from now (about 2.1 s)	R/(W)	R/(W)
b7	DBGPULSE	Debug Pulse Setting	Sets Sync signal debug pulse. 0: Deactivated 1: Immediately generates a single debug ping on the SYNC0 and SYNC1 pins in accord with the setting of bits 2 and 1 of this register. This bit is self-cleared and always read as 0.	R/(W)	R/(W)

Writing to this register depends on the setting of bit 0 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.4.2 SYNC Signal Pulse Length Register (DC_PULSE_LEN)

This register indicates the pulse length of SYNC signals.

Address(es): A00D 0982h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PULSELEN															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b15 to b0	PULSELEN	SYNC Signal Pulse Length Indication	Indicate the pulse length of SYNC signals (in units of 10 ns) 0: Acknowledge mode. In this mode, SYNC signal is cleared by reading the SYNC0 or SYNC1 status register (DC_SYNC0/1_STAT at 098Eh, 098Fh).	R	R

30.17.4.3 Activation Status Register (DC_ACT_STAT)

This register indicates the activation status of SYNC output signals.

Address(es): A00D 0984h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	START TIME	SYNC1 ACT	SYNC0 ACT
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SYNC0ACT	SYNC0 Status Indication	Indicates the activation state of SYNC0. 0: First SYNC0 pulse is not pending. 1: First SYNC0 pulse is pending.	R	R
b1	SYNC1ACT	SYNC1 Status Indication	Indicates the activation state of SYNC1. 0: First SYNC1 pulse is not pending. 1: First SYNC1 pulse is pending.	R	R
b2	STARTTIME	Plausibility Result Indication	Indicates the plausibility check result of the start time cyclic operation register (DC_CYC_START_TIME at 0990h) while the Sync output unit is activated. 0: The start time was within the near future. 1: The start time was out of the near future.	R	R
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

30.17.4.4 SYNC0 Status Register (DC_SYNC0_STAT)

This register indicates the state of SYNC0 output. It is only used in acknowledge mode.

Address(es): A00D 098Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SYNC0 STA
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SYNC0STA	SYNC0 State Indication	Indicates the SYNC0 state for acknowledge mode. SYNC0 in acknowledge mode is cleared by reading this register from the PDI. This bit is only used in acknowledge mode.	R (ack)	R
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.17.4.5 SYNC1 Status Register (DC_SYNC1_STAT)

This register indicates the state of SYNC1 output. It is only used in acknowledge mode.

Address(es): A00D 098Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SYNC1 STA
Value after reset:	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	SYNC1STA	SYNC1 State Indication	Indicates the SYNC1 state for acknowledge mode. SYNC1 in acknowledge mode is cleared by reading this register from the PDI. This bit is only used in acknowledge mode.	R (ack)	R
b7 to b1	—	Reserved	When read, the value returned is undefined.	R	R

30.17.4.6 Start Time Cyclic Operation/Next SYNC0 Pulse Register (DC_CYC_START_TIME)

Writing to this register sets the start time of cyclic operation. Reading this register indicates the system time of the next SYNC0 pulse.

Address(es): A00D 0990h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	STATIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	STATIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	STATIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	STATIM															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	STATIM	Start Time Setting/ System Time Indication	Write: Set the start time (in the system time) of cyclic operation in ns units. Read: Indicate the system time of the next SYNC0 pulse in ns units.	R/(W)	R/(W)

Writing to this register depends on the setting of bit 0 of the cyclic unit control register (DC_CYC_CONT at 0980h). Only writable when bit 0 is 0 in the SYNC activation register (DC_ACT at 0981h).
When auto-activation is enabled, upper 32 bits are automatically extended if only lower 32 bits are written within one frame.

30.17.4.7 Next SYNC1 Pulse Register (DC_NEXT_SYNC1_PULSE)

This register indicates the system time of the next SYNC1 pulse.

Address(es): A00D 0998h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYNC1PULSE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYNC1PULSE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYNC1PULSE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC1PULSE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYNC1PULSE	SYNC1 Pulse System Time Indication	Indicate the system time of the next SYNC1 pulse in ns units.	R	R

30.17.4.8 SYNC0 Cycle Time Register (DC_SYNC0_CYC_TIME)

This register is used to set the time between consecutive SYNC0 pulses.

Address(es): A00D 09A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYNC0CYC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC0CYC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	SYNC0CYC	Time Between Consecutive SYNC0 Pulses	Set the time between two consecutive SYNC0 pulses in ns units. 0: Single shot mode. Only one SYNC0 pulse is generated in single shot mode.	R/(W)	R/(W)

Writing to this register depends on the setting of bit 0 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.4.9 SYNC1 Cycle Time Register (DC_SYNC1_CYC_TIME)

This register is used to set the time between SYNC1 and SYNC0 pulses.

Address(es): A00D 09A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYNC1CYC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC1CYC															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	SYNC1CYC	Time between SYNC1 and SYNC0 Pulses	Set the time between SYNC1 and SYNC0 pulses in ns units.	R/(W)	R/(W)

Writing to this register depends on the setting of bit 0 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5 Latch Input Unit Registers

30.17.5.1 Latch 0 Control Register (DC_LATCH0_CONT)

This register is used to control the edge function of the latch 0 input signal.

Address(es): A00D 09A8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	NEGEDGE	POSEDGE
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	POSEDGE	Latch 0 Positive Edge Function Setting	Sets the function of the rising edge of the latch 0 input signal. 0: Continuous latch active 1: Single event (only first event active)	R/(W)	R/(W)
b1	NEGEDGE	Latch 0 Negative Edge Function Setting	Sets the function of the falling edge of the latch 0 input signal. 0: Continuous latch active 1: Single event (only first event active)	R/(W)	R/(W)
b7 to b2	—	Reserved	When read, the value returned is undefined.	R/(W)	R

Writing to this register depends on the setting of bit 4 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5.2 Latch 1 Control Register (DC_LATCH1_CONT)

This register is used to control the edge function of the latch 1 input signal.

Address(es): A00D 09A9h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	NEGEDGE	POSEDGE
Value after reset:	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	POSEDGE	Latch 1 Positive Edge Function Setting	Sets the function of the rising edge of the latch 1 input signal. 0: Continuous latch active 1: Single event (only first event active)	R/(W)	R/(W)
b1	NEGEDGE	Latch 1 Negative Edge Function Setting	Sets the function of the falling edge of the latch 1 input signal. 0: Continuous Latch active 1: Single event (only first event active)	R/(W)	R/(W)
b7 to b2	—	Reserved	When read, the value returned is undefined.	R/(W)	R

Writing to this register depends on the setting of bit 5 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5.3 Latch 0 Status Register (DC_LATCH0_STAT)

This register indicates the state of the latch 0 input signal.

Address(es): A00D 09AEh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PINSTATE	EVENTNEG	EVENTPOS
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	EVENTPOS	Latch 0 Positive Edge Event Indication	Indicates detection of rising edges of the event latch 0 signal. 0: Rising edge not detected or continuous mode 1: Rising edge detected and mode is single-event. This flag is cleared by reading the latch 0 time positive edge register (DC_LATCH0_TIME_POS at 09B0h).	R	R
b1	EVENTNEG	Latch 0 Negative Edge Event Indication	Indicates detection of falling edges of the event latch 0 signal. 0: Falling edge not detected or continuous mode 1: Falling edge detected and mode is single-event. This flag is cleared by reading the latch 0 time negative edge register (DC_LATCH0_TIME_NEG at 09B8h).	R	R
b2	PINSTATE	Latch 0 Input Pin State Indication	Indicates the state of the latch 0 input pin.	R	R
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

30.17.5.4 Latch 1 Status Register (DC_LATCH1_STAT)

This register indicates the state of the latch 1 input signal.

Address(es): A00D 09AFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PINSTATE	EVENTNEG	EVENTPOS
Value after reset:	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b0	EVENTPOS	Latch 1 Positive Edge Event Indication	Indicates detection of rising edges of the event latch 1 signal. 0: Rising edge not detected or continuous mode 1: Rising edge detected and mode is single-event. This flag is cleared by reading the latch 1 time positive edge register (DC_LATCH1_TIME_POS at 09C0h).	R	R
b1	EVENTNEG	Latch 1 Negative Edge Event Indication	Indicates detection of falling edges of the event latch 1 signal. 0: Falling edge not detected or continuous mode 1: Falling edge detected and mode is single-event. This flag is cleared by reading the latch 1 time negative edge register (DC_LATCH1_TIME_NEG at 09C8h).	R	R
b2	PINSTATE	Latch 1 Input Pin State Indication	Indicates the state of the latch 1 input pin.	R	R
b7 to b3	—	Reserved	When read, the value returned is undefined.	R	R

30.17.5.5 Latch 0 Time Positive Edge Register (DC_LATCH0_TIME_POS)

This register indicates the system time at the rising edge of the latch 0 input signal.

Address(es): A00D 09B0h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIME	System Time Indication	Indicate the system time captured at the rising edge of the latch 0 input signal. Reading this register clears bit 0 of the latch 0 status register (DC_LATCH0_STAT at 09AEh).	R (ack)	R (ack)

Bits 63 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

Clearing the latch 0 status flag function depends on the setting of bit 4 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5.6 Latch 0 Time Negative Edge Register (DC_LATCH0_TIME_NEG)

This register indicates the system time at the falling edge of the latch 0 input signal.

Address(es): A00D 09B8h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIME	System Time Indication	Indicate the system time captured at the falling edge of the latch 0 input signal. Reading this register clears bit 1 of the latch 0 status register (DC_LATCH0_STAT at 09AEh).	R (ack)	R (ack)

Bits 63 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

Clearing the latch 0 status flag function depends on the setting of bit 4 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5.7 Latch 1 Time Positive Edge Register (DC_LATCH1_TIME_POS)

This register indicates the system time at the rising edge of the latch 1 input signal.

Address(es): A00D 09C0h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIME	System Time Indication	Indicate the system time captured at the rising edge of the latch 1 input signal. Reading this register clears bit 0 of the latch 1 status register (DC_LATCH1_STAT at 09AFh).	R (ack)	R (ack)

Bits 63 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

Clearing the latch 1 status flag function depends on the setting of bit 5 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.5.8 Latch 1 Time Negative Edge Register (DC_LATCH1_TIME_NEG)

This register indicates the system time at the falling edge of the latch 1 input signal.

Address(es): A00D 09C8h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYSTIME															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	SYSTIME	System Time Indication	Indicate the system time captured at the falling edge of the latch 1 input signal. Reading this register clears bit 1 of the latch 1 status register (DC_LATCH1_STAT at 09AFh).	R (ack)	R (ack)

Bits 63 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

Clearing the latch 1 status flag function depends on the setting of bit 5 of the cyclic unit control register (DC_CYC_CONT at 0980h).

30.17.6 SyncManager Event Time Registers

30.17.6.1 Buffer Change Event Time Register (DC_ECAT_CNG_EV_TIME)

This register indicates the local time at the beginning of a frame which causes SyncManager to generate an ECAT event (switching the buffers).

Address(es): A00D 09F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECATCHANGE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECATCHANGE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	ECATCHANGE	Local Time Indication	Indicate the local time at the beginning of a frame which causes at least one SyncManager to generate an ECAT event (switching the buffers).	R	R

Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

30.17.6.2 PDI Buffer Start Event Time Register (DC_PDI_START_EV_TIME)

This register indicates the local time when SyncManager has generated a PDI event (access to the address where a buffer starts).

Address(es): A00D 09F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PDISTART															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDISTART															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	PDISTART	Local Time Indication	Indicate the local time when at least one SyncManager has generated a PDI event (access to the address where a buffer starts).	R	R

Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

30.17.6.3 PDI Buffer Change Event Time Register (DC_PDI_CNG_EV_TIME)

This register indicates the local time when SyncManager has generated a PDI event (switching the buffers).

Address(es): A00D 09FCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PDICHANGE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDICHANGE															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	PDICHANGE	Local Time Indication	Indicate the local time when at least one SyncManager has generated a PDI event (switching the buffers).	R	R

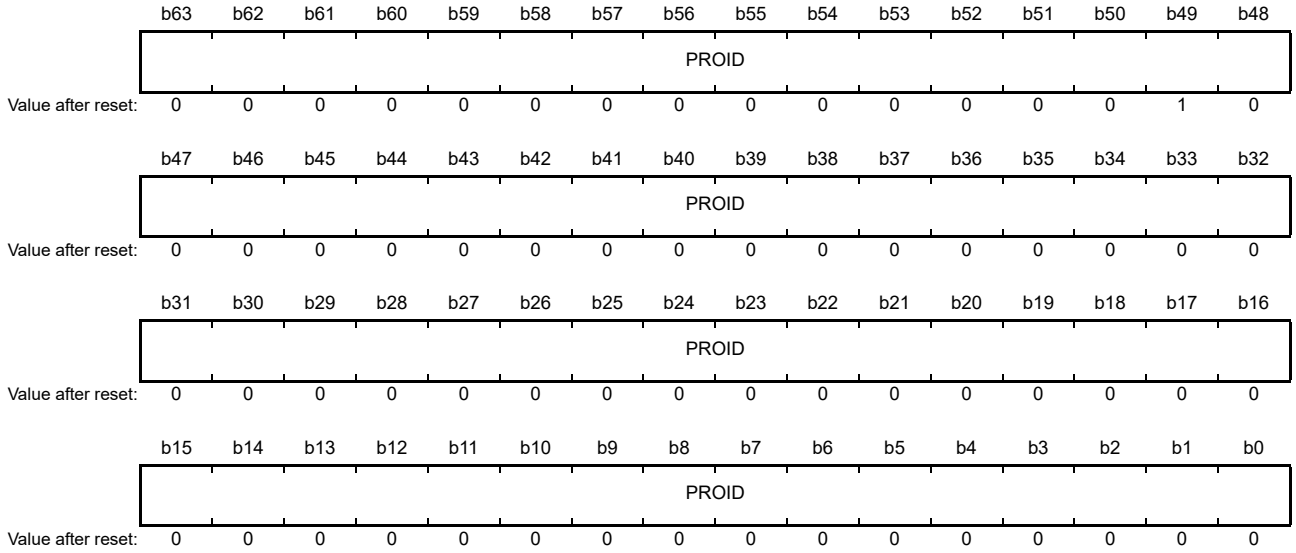
Bits 31 to 8 are internally latched (ECAT/PDI independently) when bits 7 to 0 are read, which guarantees reading a consistent value.

30.18 Other Registers

30.18.1 Product ID Register (PRODUCT_ID)

This register indicates the product ID.

Address(es): A00D 0E00h



Bit	Symbol	Bit Name	Description	PDI	ECAT
b63 to b0	PROID	Product ID Indication	Product ID	R	R

30.18.2 Vendor ID Register (VENDOR_ID)

This register indicates the vendor ID.

Address(es): A00D 0E08h

	b63	b62	b61	b60	b59	b58	b57	b56	b55	b54	b53	b52	b51	b50	b49	b48
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b47	b46	b45	b44	b43	b42	b41	b40	b39	b38	b37	b36	b35	b34	b33	b32
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	VENDORID															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VENDORID															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	PDI	ECAT
b31 to b0	VENDORID	Vendor ID Indication	Vendor ID	R	R
b63 to b32	—	Reserved	When read, the value returned is undefined.	R	R

30.18.3 User RAM (USER_RAM)

This area of RAM indicates the supported features dependent on the IP core configuration, and takes up the 128 bits from A00D 0F80h to A00D 0FFFh. An initial value of 1 means that the implementation of this module supports the corresponding feature, except in the case of bits 7 to 0, which indicate the number of bits defined in the user RAM and the initial value is 33h for this module.

Bit Position	Description	Initial Value
7 to 0	Number of bits for defining extended functionality. The value is 51 (33h) for this module.	33h
8	Extended DL control register (0102h, 0103h)	1
9	AL status code register (0134h, 0135h)	1
10	ECAT event mask (0200h, 0201h)	1
11	Configured station alias (0012h, 0013h)	1
12	General input (0F18h, 0F1Fh)	0
13	General output (0F10h, 0F17h)	0
14	AL event mask (0204h, 0207h)	1
15	Physical read/write offset (0108h, 0109h)	1
16	Watchdog divider writable (0400h, 0401h) and watchdog PDI (0410h, 0f11h)	1
17	Watchdog counter (0442h, 0443h)	1
18	Write protection (0020h, 0031h)	1
19	Reset (0040h, 0041h)	1
20	Reserved	0
21	DC SyncManager event time (09F0h, 09FFh)	1
22	ECAT processing unit/PDI error counter (030Ch, 030Dh)	1
23	EEPROM size configurable (Bit 7 at 0502h) 0: EEPROM size fixed up to 16 Kbits 1: EEPROM Size configurable	1
26 to 24	Reserved	0
27	Lost link counter (0310h, 0313h)	1
28	MII management interface (0510h, 0515h)	1
29	Enhanced link detection MII	1
30	Enhanced link detection EBUS	0
31	Run LED	1
32	Link/activity LED	1
33	Reserved	0
35 to 34	Reserved	1
36	Reserved	0
37	Reserved	1
38	DC Time loop control assigned to PDI	0
39	Link detection and configuration by MI	0
40	MI control by PDI	1
41	Automatic TX shift	1
42	EEPROM emulation	0
49 to 43	Reserved	0
50	ERR LED, RUN/ERR LED override	1
Others	Reserved	Reserved

30.18.4 Process Data RAM (DATA_RAM)

The process data RAM is used for process data and mailbox, and takes up 8 Kbytes from A00D 1000h to A00D 2FFFh. This RAM is only accessible when the EEPROM is correctly loaded (i.e., when bit 0 is 1 in the ESC DL status register, ESC_DL_STATUS, at 0110h).

30.18.5 Setting the Module-Stop Function

EtherCAT modules are stopped in the initial state. If the modules are to be used, set the MSTPCRB.MSTPCRB15 bit for release from the module-stop state. Note that re-setting the module-stop state is prohibited following release from the module-stop state. Operation of the modules if they are stopped following release and then released again is not guaranteed. Release from the module-stop state can proceed again after the modules have been returned to their initial states (stopped) by a reset.

30.19 Initial Settings

To initialize the EtherCAT, follow the procedure below.

- Set the offset address of the PHY module in the CATOFFADD register.
- Set the size of the EEPROM in the CATEMMD register.
- Set the delay time of the TXC pin in the CATTXCSFT register.
- Release the EtherCAT from the module stop state by using the MSTPCRB15 bit in the MSTPCRB register.
- Release the ESC and PHY modules from the reset state by using the CATRST and PHYRST bits in the ETHSFTRST register.

On release from the reset state, the ESC will automatically load the EEPROM data and be activated.

30.20 Configuration of the Reset Circuit

Figure 30.2 shows the configuration of the reset circuit of the ESC. On reception of a reset request (0040h) from the ECAT or a reset request (0041h) from the PDI, the ESC stops and the output of the reset signal from the ESC becomes high. The output of this reset signal from the ESC drives the signal on the PHYRESETOUT# pin to the low level and the externally connected Ethernet PHY chip is reset. An ETHCRSTI interrupt is generated at the same time.

To release the ESC from the reset state, the CATRST bit in the ETHSFTRST register must be switched from 1 to 0 then back to 1. Note that the output of the reset signal from the ESC becomes low when the input of the reset signal to the ESC changes from high to low. Restarting of the ESC begins when the input of the reset signal to the ESC changes from low to high and loading of the EEPROM starts. Loading of the EEPROM is completed in about 1 ms. The timing with which the Ethernet PHY chip is released from the reset state must be set so that it will only recommence operations after the ESC has started. Figure 30.3 shows the timing chart.

Resetting the ESC by using the CATRST bit of the ETHSFTRST register instead of by the ECAT or PDI issuing a reset request (0040h or 0041h) is also possible. In this case, the PHYRESETOUT# pin does not automatically go to the low level, so use the PHYRST bit of the ETHSFTRST register to place the Ethernet PHY chip in the reset state beforehand. Figure 30.4 shows the timing chart.

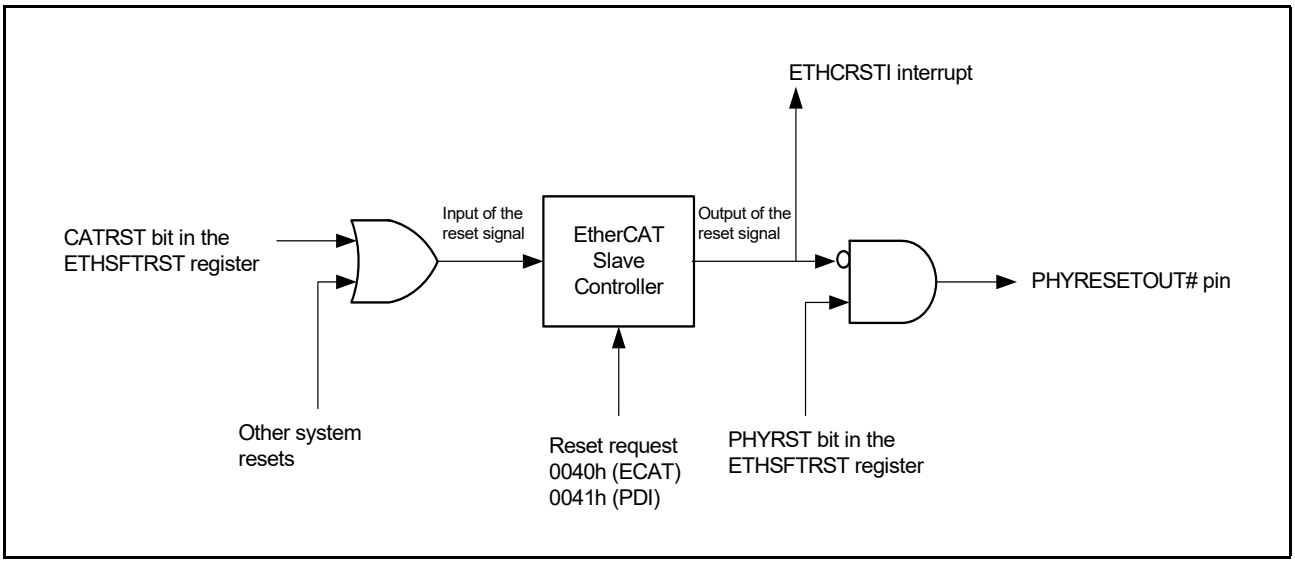


Figure 30.2 Configuration of the Reset Circuit of the EtherCAT Slave Controller

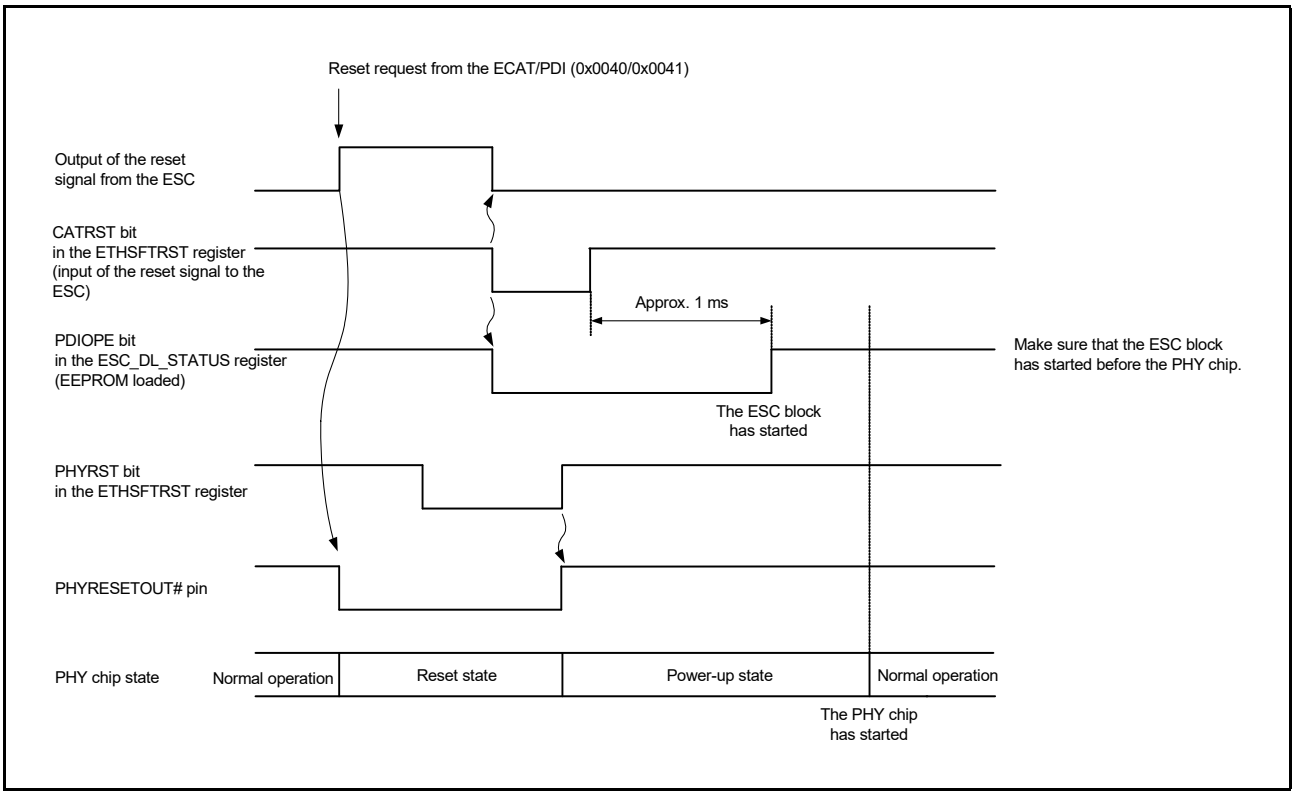


Figure 30.3 Timing with which the EtherCAT Slave Controller is Reset (in the Case of a Reset Requested by the ECAT or PDI)

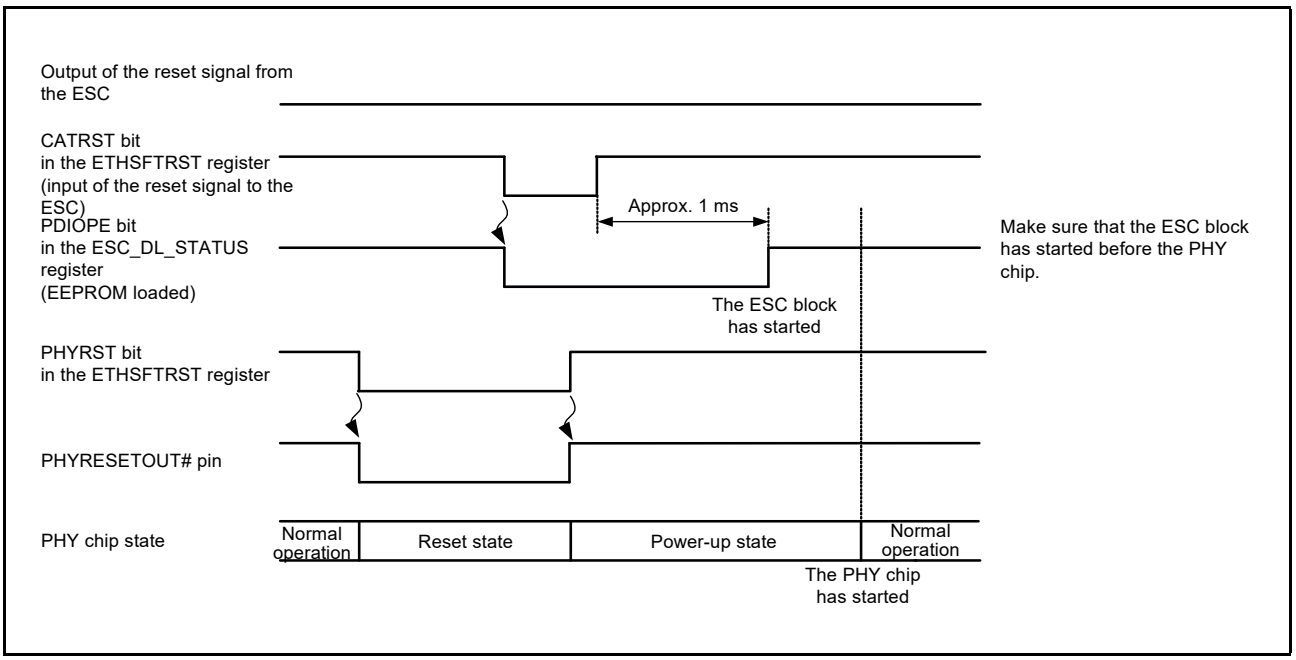


Figure 30.4 Timing with which the EtherCAT Slave Controller is Reset (in the Case of the CATRST Bit of the ETHSFTRST Register being Used to Reset the ESC)

31. USB2.0HS Host Module (USBh)

31.1 Overview

The USB module of this LSI is a dual-role device that has USB 2.0 host and function modules. However, it does not have a facility for detecting the ID and so does not support On-the-Go (OTG) functionality.
This LSI handles a single USB port for either host controller or function controller operation. The port connection path select input signal bits (PHYSET1.P1PORTSEL[1:0]) are used to switch between host controller and function controller operation.
Since operation as a host controller or a function controller are exclusive of each other, dynamic switching between the types of operation is not possible.

This section describes host controller operation.

USB2.0 Host Controller Operation

- Conforms to Universal Serial Bus Specification Revision 2.0.
- Conforms to Open Host Controller Interface (OHCI) Specification for USB Rev 1.0a.
- Conforms to Enhanced Host Controller Interface (EHCI) Specification for USB Rev 1.0.
- Supports USB2.0 high-speed (480 Mbps) and full-speed (12 Mbps) transfer.

Note: Low-speed (1.5 Mbps) is not supported.

- Supports the USB2.0 compliance test function.

Figure 31.1 is a block diagram of the USB module.

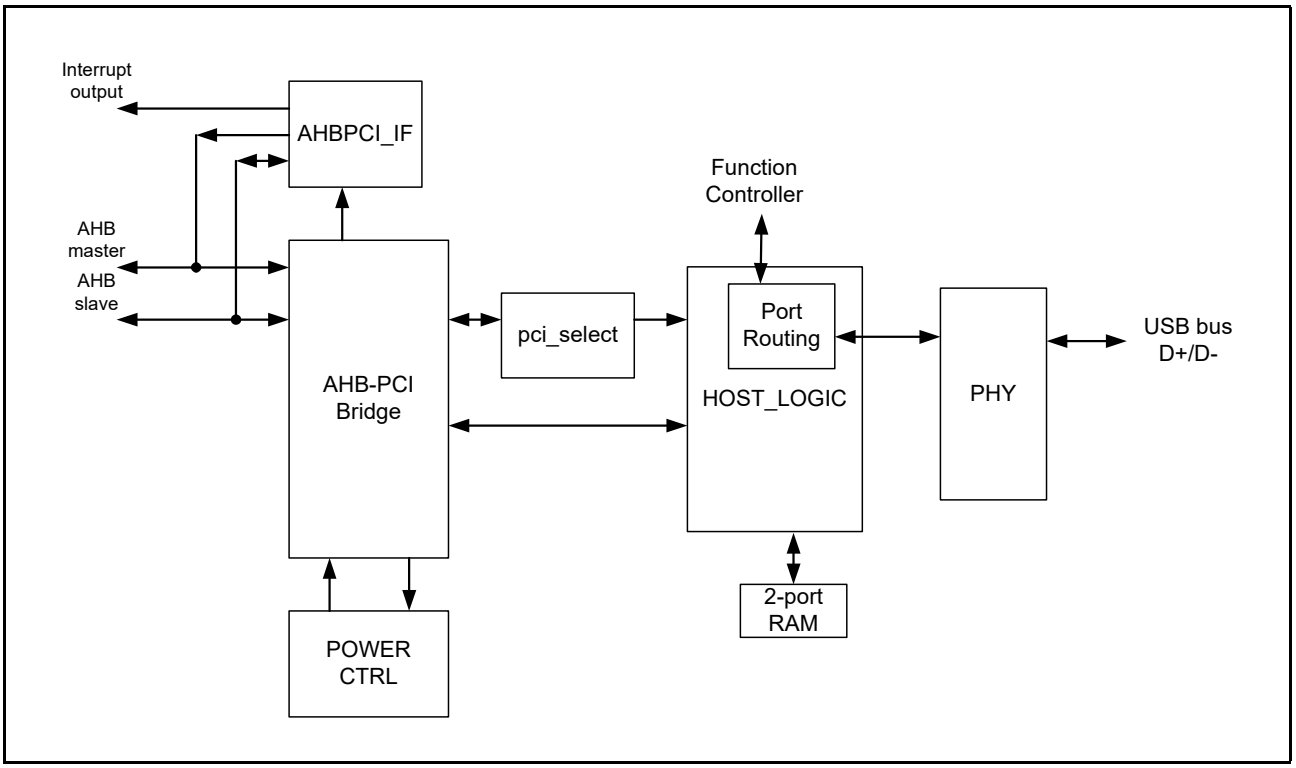


Figure 31.1 Block Diagram of the USB Module

(1) Host Logic

A USB 2.0 logic conforming to the EHCI and OHCI standards. It has control circuits such as a list processing circuit, a serial-parallel circuit, a USB buffer, and executes high-speed, and full-speed USB transfer.

(2) UTMI+ Transceiver

A USB 2.0 UTMI transceiver with an interface conforming to the UTMI+ standard.

(3) AHB-PCI Bridge

A module for conversion between AHB bus cycles and PCI bus cycles to the hot logic. Access from the CPU to registers in the bridge or host logic is performed through the slave interface in the bridge. Access by the host logic with the PCI as the master is transferred to the AHB bus through the master interface in the bridge.

31.1.1 Precautions on Use of USB Host Controller

The following describes precautions on use of the USB host controller.

31.1.1.1 General Precautions

(1) Dynamic changes in PCLKA, USBPCLK, and USBMCLK are not supported except for the clock stop state.
(2) When using isochronous transfer, evaluate performance at the application level to confirm that the expected performance is obtained.
(3) The USB host controller outputs the logical OR of four internal interrupt signals. See section 31.6, Interrupts.
(4) It may take a long time to actually clear an interrupt after a register is accessed to clear the interrupt. For the actionnecessary during this wait time, see section 31.6.3, Time Required to Clear Interrupt Signals.

31.1.1.2 AHB Interface

(1) Only 32-bit access is available for AHB slave access to the USB host controller; 8- or 16-bit access is not allowed.
(2) When using the wait mode with HRESP = RETRY, access the following mode switch register in the AHB bridge first.
- Bit 17 (SMODE_READY_CTR) in the AHB_BUS_CTR register
(3) The read or written data is not guaranteed for register access while the clock is stopped.

31.1.1.3 Operating Procedures

(1) See the operating procedures described in the following sections.
- Initial settings: section 31.8, Operating Procedures
- Mapping in the AHB space and PCI space: section 31.4.1, Register Access.

31.2 Register Mapping

31.2.1 Register Mapping

The register space is broadly divided into the following three areas.

1. OHCI/EHCI operational register area
2. PCI configuration space area
3. AHB-PCI bridge PCI communication area

To access each PICI configuration space, the AHPBPCI_WIN1_CTR register in the AHB-PCI bridge register area should be used. In addition to register mapping in the AHB space, the addresses of the OHCI/EHCI operational registers and PCI communication spaces should be correctly mapped to the PCI space in the USB host controller. For details of access and address mapping of each register, see section 31.4.1, Register Access.
The range of address input is from A004 0000h to A005 FFFFh. Do not access the reserved area (A005 0C00h to A005 FFFFh).

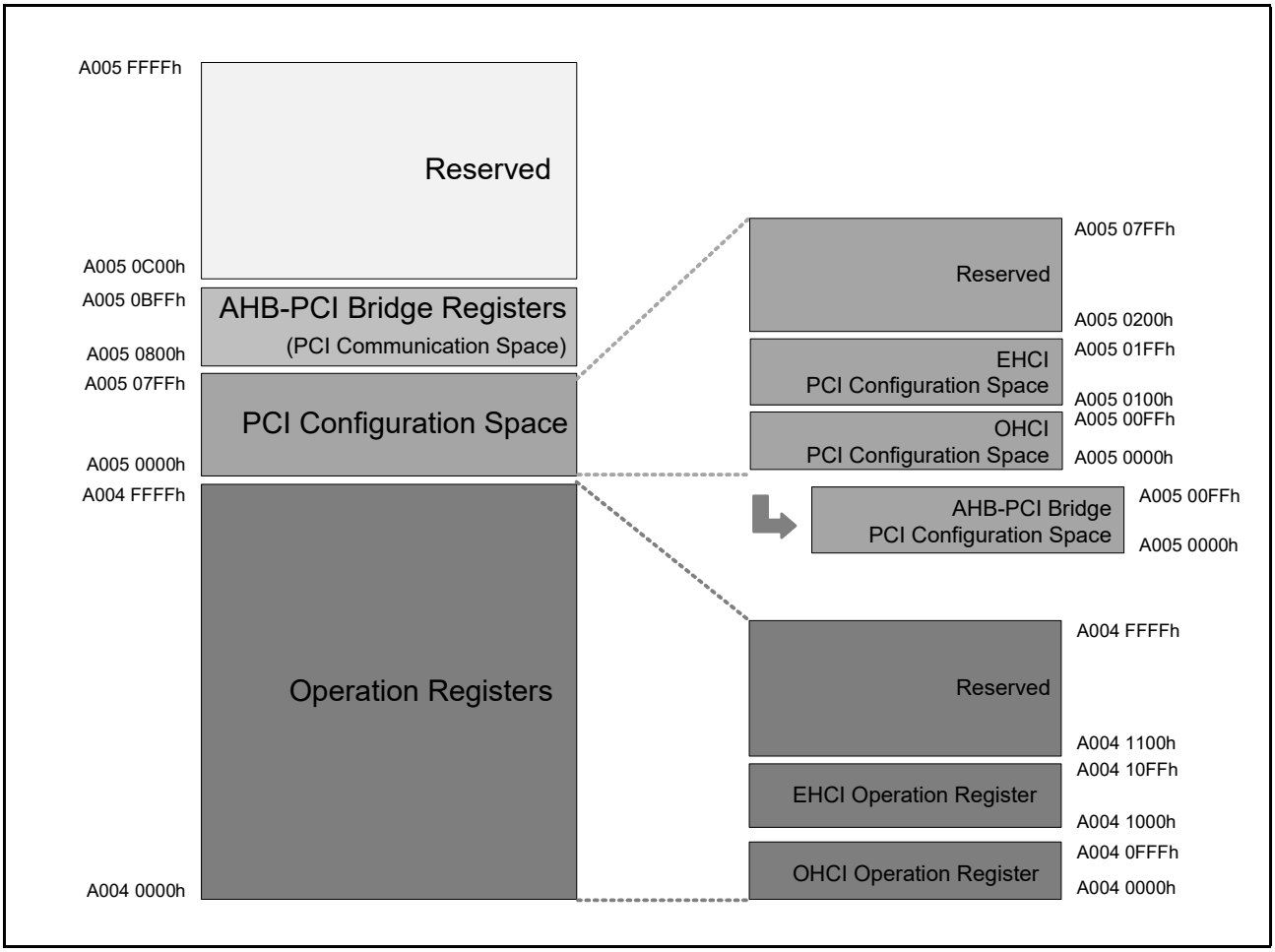


Figure 31.2 Register Mapping Image

Table 31.1 Register Mapping List (1 / 2)

Address	Register Name	Symbol
A004 0000h	HcRevision	HcRevision
A004 0004h	HcControl	HcControl
A004 0008h	HcCommandStatus	HcCommandStatus
A004 000Ch	HcInterruptStatus	HcIntStatus
A004 0010h	HcInterruptEnable	HcIntEnable
A004 0014h	HcInterruptDisable	HcIntDisable
A004 0018h	HcHCCA	HcHCCA
A004 001Ch	HcPeriodicCurrentED	HcPeriodCurED
A004 0020h	HcControlHeadED	HcContHeadED
A004 0024h	HcControlCurrentED	HcContCurrentED
A004 0028h	HcBulkHeadED	HcBulkHeadED
A004 002Ch	HcBulkCurrentED	HcBulkCurrentED
A004 0030h	HcDoneHead	HcDoneHead
A004 0034h	HcFmInterval	HcFmInterval
A004 0038h	HcFmRemaining	HcFmRemaining
A004 003Ch	HcFmNumber	HcFmNumber
A004 0040h	HcPeriodicStart	HcPeriodicStart
A004 0044h	Reserved	—
A004 0048h	HcRhDescriptorA	HcRhDescriptorA
A004 004Ch	HcRhDescriptorB	HcRhDescriptorB
A004 0050h	HcRhStatus	HcRhStatus1_A, HcRhStatus1_B
A004 0054h	HcRhPortStatus1	HcRhPortStatus1_A, HcRhPortStatus1_B
A004 0058Ch to A004 0FFCh	Reserved	—
A004 1000h	HCIVERSION / CAPLENGTH	CAPL_VERSION
A004 1004h	HCSPARAMS	HCSPARAMS
A004 1008h	HCCPARAMS	HCCPARAMS
A004 100Ch	HCSP_PORTROUTE	HCSP_PORTROUTE
A004 1010h to A004 101Ch	Reserved	—
A004 1020h	USBCMD	USBCMD
A004 1024h	USBSTS	USBSTS
A004 1028h	USBINTR	USBINTR
A004 102Ch	FRINDEX	FRINDEX
A004 1030h	CTRLDSSEGMENT	CTRLDSSEGMENT
A004 1034h	PERIODICLISTBASE	PERIODICLIST
A004 1038h	ASYNCLISTADDR	ASYNCLISTADDR
A004 103Ch to A004 105Ch	Reserved	—
A004 1060h	CONFIGFLAG	CONFIGFLAG
A004 1064h	PORTSC1	PORTSC1
A004 1068h to A004FFFCh	Reserved	—
A005 0000h to A005 07FCh	PCI Configuration Space (AHB-PCI Bridge / OHCI / EHCI)	—
A005 0800h	PCIAHB_WIN1_CTR	PCIAHB_WIN1_CTR
A005 0804h	Reserved	—
A005 0808h to A005 080Ch	Reserved	—
A005 0810h	AHBPCI_WIN1_CTR	AHBPCI_WIN1_CTR

Table 31.1 Register Mapping List (2 / 2)

Address	Register Name	Symbol
A005 0814h	AHBPCI_WIN2_CTR	AHBPCI_WIN2_CTR
A005 0818h to A005 081Ch	Reserved	—
A005 0820h	PCI_INT_ENABLE	PCI_INT_ENABLE
A005 0824h	PCI_INT_STATUS	PCI_INT_STATUS
A005 0828h to A005 082Ch	Reserved	—
A005 0830h	AHB_BUS_CTR	AHB_BUS_CTR
A005 0834h	USBCTR	USBCTR
A005 0838h to A005 083Ch	Reserved	—
A005 0840h	PCI_ARBITER_CTR	PCI_ARBITER_CTR
A005 0844h	Reserved	—
A005 0848h	PCI_UNIT_REV	PCI_UNIT_REV
A005 084Ch to A005 FFFCh	Reserved	—

31.2.2 PCI Configuration Space for AHB-PCI Bridge

Table 31.2 shows the register mapping in the PCI configuration space for the AHB-PCI bridge.

Table 31.2 PCI Configuration Space For AHB-PCI Bridge

Offset	31 24	23 16	15 8	7 0	Symbol
000h	Device ID		Vendor ID		VID_DID_A
004h	Status		Command		CMND_STS_A
008h	Class Code			Revision ID	REVID_CC_A
00Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST_A
010h	AHB-PCI Bridge Registers Base Address				BASEAD_A
014h	PCI-AHB Window1 Base Address				WIN1_BASEAD
01Ch	Reserved				—
020h					
024h					
028h					
02Ch	Subsystem ID		Subsystem Vendor ID		SSVID_SSID_A
030h	Reserved				—
034h					
038h					
03Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN_A
040h	Reserved				—
|					
0FCh					

31.2.3 PCI Configuration Space for OHCI Host Logic

Table 31.3 shows the register mapping in the PCI configuration space for the host logic (OHCI).

Table 31.3 PCI Configuration Space for OHCI

Offset	31 24	23 16	15 8	7 0	Symbol
000h	Device ID		Vendor ID		VID_DID_O
004h	Status		Command		CMND_STS_O
008h	Class Code			Revision ID	REVID_CC_O
00Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST_O
010h	OHCI Base Address				BASEAD_O
014h	Reserved				—
018h					
01Ch					
020h					
024h					
028h					
02Ch	Subsystem ID		Subsystem Vendor ID		SSVID_SSID_O
030h	Expansion ROM Base Address				EROM_BASEAD
034h	Reserved			Cap_ptr	CAPPTR
038h	Reserved				—
03Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN_O
040h	PMC		Next_Item_Ptr	Cap_ID	CAPID_NIP_PMCAP
044h	Data	PMCSR_BSE	PMCSR		PMC_STS_PMCSR
048h to 0DCh	Reserved				—
0E0h	EXT1				EXT1
0E4h	EXT2				EXT2
0E8h to 0ECh	Reserved				—
0F0h	Reserved				—
0F4h	Reserved				—
0F8h to 0FCh	Reserved				—

31.2.4 PCI Configuration Space for EHCI Host Logic

Table 31.4 shows the register mapping in the PCI configuration space for the host logic (EHCI).

Table 31.4 PCI Configuration Space for EHCI

Offset	31 24	23 16	15 8	7 0	Symbol
100h	Device ID		Vendor ID		VID_DID_E
104h	Status		Command		CMND_STS_E
108h	Class Code			Revision ID	REVID_CC_E
10Ch	BIST	Header Type	Latency Timer	Cache Line Size	CLS_LT_HT_BIST_E
110h	EHCI Base Address				BASEAD_E
114h	Reserved				—
118h					
11Ch					
120h					
124h					
128h					
12Ch	Subsystem ID		Subsystem Vendor ID		SSVID_SSID_E
130h	Expansion ROM Base Address				EROM_BASEAD_E
134h	Reserved			Cap_ptr	CAPPTR_E
138h	Reserved				—
13Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	INTR_LINE_PIN_E
140h	PMC		Next_Item_Ptr	Cap_ID	CAPID_NIP_PMCAP_E
144h	Data	PMCSR_BSE	PMCSR		PMC_STS_PMCSR_E
148h	Reserved				—
15Ch					
160h	PORTWAKECAP		FLAD	SBRN	SBRN_FLADJ_PW
164h to 1DCh	Reserved				—
1E0h	EXT1				EXT1_E
1E4h	EXT2				EXT2_E
1E8h to 1ECh	Reserved				—
1F0h	Reserved				—
1F4h	Reserved				—
1F8h to 1FCh	Reserved				—

31.3 Register Descriptions

This section describes details of the register functions.

31.3.1 OHCI Operational Registers

Access the OHCI operational registers after starting up the PHY internal PLL. For details, see Figure 31.13, Initial Setting Sequence.

31.3.1.1 HcRevision Register

Address(es) A004 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	Revision[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Revision[7:0]	HCI revision	These bits indicate the version of the HCI specifications implemented in the host logic. As the host logic conforms to OHCI standard 1.0a, this value is set to 10h.	R
b31 to b8	—	Reserved	Don't care	R

31.3.1.2 HcControl Register

Address(es) A004 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	RWE	RWC	—	HCFS[1:0]		BLE	CLE	IE	PLE	CBSR[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CBSR[1:0] (ControlBulk ServiceRatio)	Control / bulk transfer service ratio specifying	These bits specify the service ratio of control transfer to bulk transfer. In periodic list processing, the service ratio specified in these bits is kept during transfer. **CBSR** / **Service Ratio of Bulk ED : Control ED** 00 1:1 01 2:1 10 3:1 11 4:1	R/W
b2	PLE (PeriodicList Enable)	Periodic list setting	This bit specifies whether to perform periodic list processing. The setting of this bit takes effect from the next frame. 0: Periodic list processing is not done. 1: Period list processing is done.	R/W
b3	IE (Isochronous Enable)	Isochronous ED processing setting	This bit specifies whether to perform isochronous ED processing. The setting of this bit takes effect from the next frame. When an isochronous ED is found during list processing, the host logic checks this bit to determine whether to perform isochronous ED processing. 0: Isochronous transfer processing is not done. 1: Isochronous transfer processing is done.	R/W
b4	CLE (ControlListEnable)	Control list processing setting	This bit specifies whether to perform control list processing. The setting of this bit takes effect from the next frame. The control list can be modified only when this value is 0. 0: Control list processing is not done. 1: Control list processing is done.	R/W
b5	BLE (BulkListEnable)	Bulk list processing setting	This bit specifies whether to perform bulk list processing. The setting of this bit takes effect from the next frame. The bulk list can be modified only when this value is 0. 0: Bulk list processing is not done. 1: Bulk list processing is done.	R/W
b7, b6	HCFS[1:0] (Host Controller FunctionalState)	Host logic operation status	These bits indicate the operating state of the host logic. Upon entering the USB operational state, the host logic starts management of frames delimited at 1-ms intervals. The operating state is always controlled by software except for transition to the USB resume state due to remote wakeup in the USB suspend state. These bits indicate the USB reset state after a hard ware reset. After a software reset, the state shifts to the USB suspend state. b7 b6 0 0: USB Reset 0 1: USB Resume 1 0: USB Operational 1 1: USB Suspend	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	—	Reserved	When writing, write 0.	R/W
b9	RWC (RemoteWakeUpConnect)	Remote WakeUp support setting	This bit indicates whether the host logic supports remote wakeup. To support remote wakeup by the system, set this bit during initialization. 0: Remote WakeUp is not supported. 1: Remote WakeUp is supported.	R/W
b10	RWE (RemoteWakeUpEnable)	PME assertion control	This bit controls PME assertion. When this bit is 1, PME is asserted when bit 3 (RD) in the HcInterruptStatus register is set to 1. 0: PME is not asserted when Resume is detected (PME is disabled). 1: PME is asserted when Resume is detected (PME is enabled).	R/W
b31 to b11	—	Reserved	When writing, write 0.	R/W

31.3.1.3 HcCommandStatus Register

Address(es) A004 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOC[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	OCR	BLF	CLF	HCR
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	HCR (HostController Reset)	Host logic software reset start	This bit starts software reset of the host logic. When this bit is set, the USB suspend state is entered regardless of the functional state of the host logic.	W
b1	CLF (ControlList Filled)	Control list TD	This bit indicates whether TD exists in the control list. The host logic checks this bit when beginning the processing of the start ED in the control list. When this bit is 0, the host logic does not begin list processing. When this bit is 1, the host logic starts control list processing and clears this bit to 0. Upon detecting TD, the host logic restores this bit to 1 and continues control list processing. When the host logic completes list processing, it clears this bit to 0. If TD is not found in the list or software does not set this bit to 1, this bit remains at 0 and list processing stops. When creating a list again and executing processing of the list, set this bit before starting list processing by setting bit 4 (CLE) in the HcCommand register.	R/W
b2	BLF (BulkListFilled)	Bulk list TD	This bit indicates whether TD exists in the bulk list. The host logic checks this bit when beginning the processing of the start ED in the bulk list. When this bit is 0, the host logic does not begin list processing. When this bit is 1, the host logic starts bulk list processing and clears this bit to 0. Upon detecting TD, the host logic restores this bit to 1 and continues bulk list processing. When the host logic completes list processing, it clears this bit to 0. If TD is not found in the list or software does not set this bit to 1, this bit remains at 0 and list processing stops. When creating a list again and executing processing of the list, set this bit before starting list processing by setting bit 5 (BLE) in the HcCommand register.	R/W
b3	OCR (Ownership Change Request)	Host logic control right change	This bit changes the control right of the host logic. (For details, check with the OHCI specification).	W
b15 to b4	—	Reserved	When writing, write 0.	R/W
b17, b16	SOC[1:0] (Scheduling OverrunCount)	Schedule overrun count	These bits count the number of times a schedule overrun occurs. This value is incremented every time a schedule overrun occurs. When the value reaches 11b, it returns to 00b. Counting continues even while bit 0 (SO) in the HcInterruptStatus register is set.	R
b31 to b18	—	Reserved	When writing, write 0.	R/W

31.3.1.4 HcInterruptStatus Register

Address(es) A004 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	RHSC	FNO	UE	RD	SF	WDH	SO
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SO (Scheduling Overrun)	USB schedule overrun	This is an interrupt bit for indicating that the USB schedule has overrun in a frame. When the USB schedule overruns, this bit is set after HccaFrameNumber for the next frame is updated. When this bit is set, bits [17:16] (SOC) in the HcCommandStatus register are also incremented. Writing 1 to this bit clears the interrupt. 0: No SO interrupt has occurred. 1: SO interrupt has occurred.	R/W
b1	WDH (Writeback Done Head)	Host logic HccaDoneHead update	This is an interrupt bit for indicating that the host logic has updated the contents of HccaDoneHead. The host logic sets this bit immediately after updating HccaDoneHead, and does not update HccaDoneHead until this bit is cleared. Writing 1 to this bit clears the interrupt. 0: No WDH interrupt has occurred. 1: WDH interrupt has occurred.	R/W
b2	SF (StartOfFrame)	HccaFrameNumber update	This is an interrupt bit for indicating that HccaFrameNumber has been updated at the beginning of a frame. The host logic updates HccaFrameNumber and sets this bit when transmitting an SOF packet. Writing 1 to this bit clears the interrupt. 0: No SF interrupt has occurred. 1: SF interrupt has occurred.	R/W
b3	RD (Resume Detected)	Resume detection	This is an interrupt bit for indicating that Resume has been detected. This bit is set when assertion of the Resume signal by a device on the USB is detected. This bit is not set when software issues USB Resume. Writing 1 to this bit clears the interrupt. 0: No RD interrupt has occurred. 1: RD interrupt has occurred.	R/W
b4	UE (Unrecoverable Error)	USB Non-related system error detection	This is an interrupt bit for indicating that a system error on the PCI bus that is not related to the USB has been detected. Writing 1 to this bit clears the interrupt. 0: No UE interrupt has occurred. 1: UE interrupt has occurred.	R/W
b5	FNO (Frame Number Overflow)	FrameNumber bit MSB change	This is an interrupt bit for indicating that the MSB of bits [15:0] (FrameNumber) in the HcFmNumber register has changed. This bit is set after HccaFrameNumber is updated in the frame where the MSB of the FrameNumber bits changes from 0 to 1 or from 1 to 0. Writing 1 to this bit clears the interrupt. 0: No FNO interrupt has occurred. 1: FNO interrupt has occurred.	R/W

Bit	Symbol	Bit Name	Description	R/W
b6	RHSC (RootHubStatus Change)	HcRhStatus/HcRhPortStatus register status	This is an interrupt bit for indicating that the state of the HcRhStatus register or the HcRhPortStatus register has changed. This bit is set when the HcRhStatus or HcRhPortStatus register state is changed by a hardware source. Writing 1 to this bit clears the interrupt. 0: No RHSC interrupt has occurred. 1: RHSC interrupt has occurred.	R/W
b31 to b7	—	Reserved	When writing, write 0.	R/W

31.3.1.5 HcInterruptEnable Register

Address(es) A004 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	RHSCE	FNOE	UEE	RDE	SFE	WDHE	SOE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SOE (Scheduling OverrunEnable)	SO interrupt source enable	This bit enables SO as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: SO interrupt is enabled.	R/W
b1	WDHE (WritebackDone HeadEnable)	WDH interrupt source enable	This bit enables WDH as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: WDH interrupt is enabled.	R/W
b2	SFE (StartOfFrame Enable)	SF interrupt source enable	This bit enables SF as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: SF interrupt is enabled.	R/W
b3	RDE (Resume DetectedEnable)	RD interrupt source enable	This bit enables RD as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: RD interrupt is enabled.	R/W
b4	UEE (Unrecoverable ErrorEnable)	UE interrupt source enable	This bit enables UE as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: UE interrupt is enabled.	R/W
b5	FNOE (FrameNumber OverflowEnable)	FNO interrupt source enable	This bit specifies FNO as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: FNO interrupt is enabled.	R/W
b6	RHSCE (RootHubStatus ChangeEnable)	RHSC interrupt source enable	This bit enables RHSC as an interrupt source. To set this bit, write 1 to it. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: RHSC interrupt is enabled.	R/W
b30 to b7	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b31	MIE (MasterInterrupt Enable)	Interrupt 7 source enable	This bit enables interrupt source settings in bits [6:0] in this register. When this bit is 0, all interrupts are masked. To clear this bit, write 1 to the corresponding bit in the HcInterruptDisable register. 0: No monitoring and nothing is to be done. 1: The specified interrupt is enabled.	R/W

31.3.1.6 HcInterruptDisable Register

Address(es) A004 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MID	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

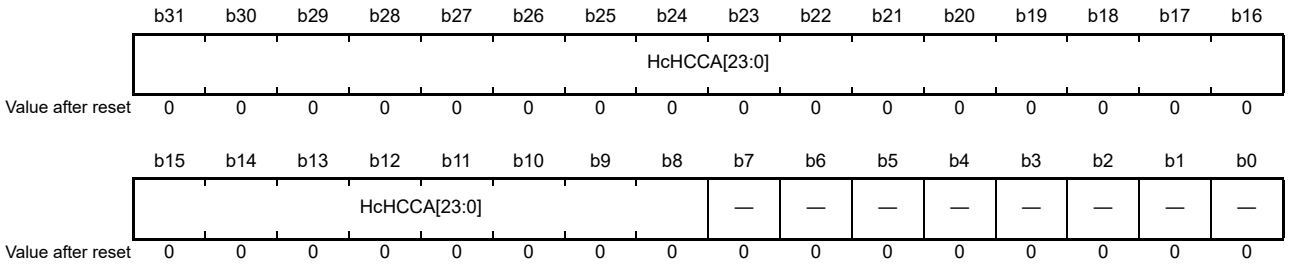
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	RHSCD	FNOD	UED	RDD	SFD	WDHD	SOD
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SOD (Scheduling Overrun Disable)	SO interrupt source disable	This bit disables the interrupt source SO. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source SO is disabled.	R/W
b1	WDHD (Writeback DoneHead Disable)	WDH interrupt source disable	This bit disables the interrupt source WDH. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source WDH is disabled.	R/W
b2	SFD (StartOfFrame Disable)	SF interrupt source disable	This bit disables the interrupt source SF. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source SF is disabled.	R/W
b3	RDD (Resume Detected Disable)	RD interrupt source disable	This bit disables the interrupt source RD. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source RD is disabled.	R/W
b4	UED (Unrecoverable ErrorDisable)	UE interrupt source disable	This bit disables the interrupt source UE. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source UE is disabled.	R/W
b5	FNOD (FrameNumber Overflow Disable)	FNO interrupt source disable	This bit disables the interrupt source FNO. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source FNO is disabled.	R/W

Bit	Symbol	Bit Name	Description	R/W
b6	RHSCD (RootHub StatusChange Disable)	RHSC interrupt source disable	This bit disables the interrupt source RHSC. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt source RHSC is disabled.	R/W
b30 to b7	—	Reserved	When writing, write 0.	R/W
b31	MID (Master Interrupt Disable)	Interrupt 7 source disable	This bit disables interrupt source settings in bits [6:0] in HcInterruptEnable. When this bit is 0, all interrupts are masked. Write 1 to this bit to clear the corresponding bit in the HcInterruptEnable register. To enable the interrupt, write 1 to the corresponding bit in the HcInterruptEnable register. 0: Nothing is to be done. 1: The interrupt set is disabled.	R/W

31.3.1.7 HcHCCA Register

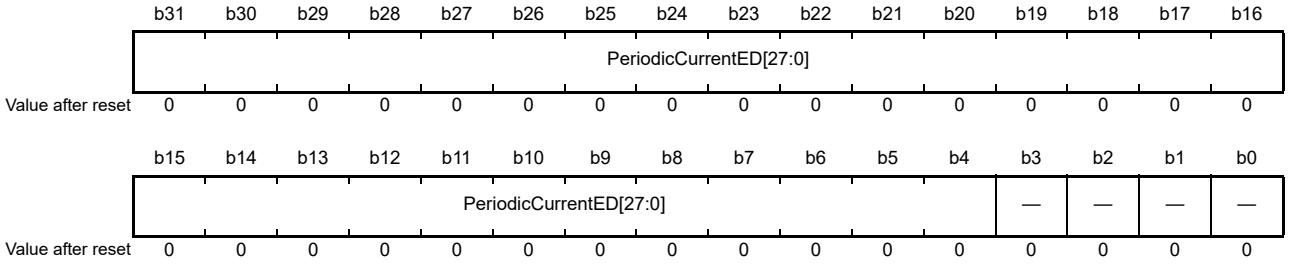
Address(es) A004 0018h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	When writing, write 0.	R/W
b31 to b8	HcHCCA [23:0]	RAM base address setting	These bits specify the base address of the RAM allocated to the host controller communication area. Specify a value in these bits during initialization. The host logic requests a 256-byte area starting from the base address specified in these bits as HCCA.	R/W

31.3.1.8 HcPeriodicCurrentED Register

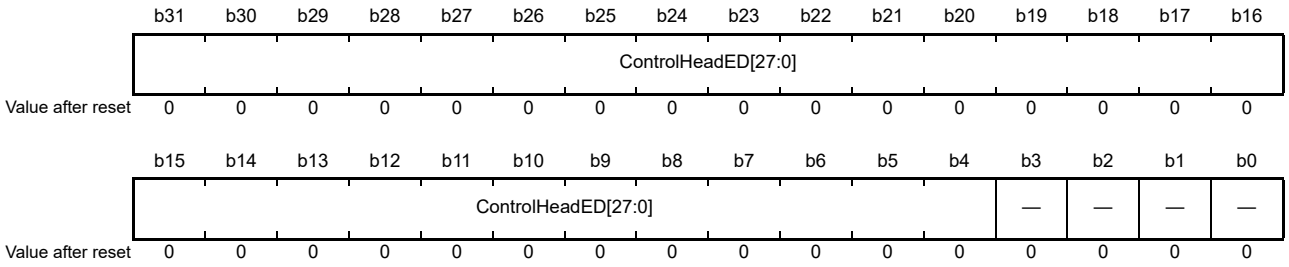
Address(es) A004 001Ch



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	Don't care	R
b31 to b4	Periodic CurrentED [27:0]	ED physical address	These bits indicate the physical address of the current ED being processed in the periodic list. The host logic updates these bits when completing the ED list processing.	R

31.3.1.9 HcControlHeadED Register

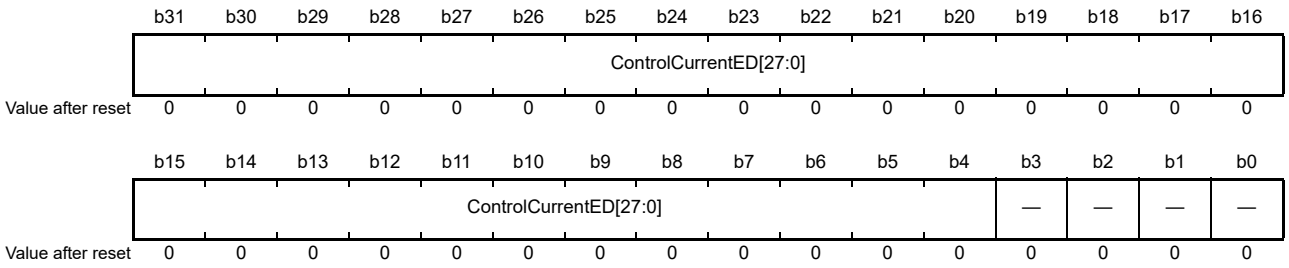
Address(es) A004 0020h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	When writing, always write 0.	R/W
b31 to b4	Control HeadED [27:0]	Start ED physical address specifying	These bits specify the physical address of the start ED in the control list. To execute control transfer, set up these bits before setting the CLE bit in the HcControl register.	R/W

31.3.1.10 HcControlCurrentED Register

Address(es) A004 0024h



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	When writing, always write 0.	R/W
b31 to b4	Control CurrentED [27:0]	ED physical address	These bits indicate the physical address of the current ED being processed in the control list. The host logic updates these bits every time the control ED processing is completed. When creating a new list, set these bits to 0000 0000h, which indicates the end of the list. When transfer is temporarily stopped and then restarted, make sure that the ED indicated by the link pointer in ControlCurrentED exists.	R/W

31.3.1.11 HcBulkHeadED Register

Address(es) A004 0028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BulkHeadED[27:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BulkHeadED[27:0]												—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	When writing, always write 0.	R/W
b31 to b4	BulkHeadED [27:0]	Start ED physical address specifying	These bits specify the physical address of the start ED in the bulk list. To execute bulk transfer, set up these bits before setting bit 5 (BLE) in the HcControl register.	R/W

31.3.1.12 HcBulkCurrentED Register

Address(es) A004 002Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BulkCurrentED[27:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BulkCurrentED[27:0]												—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	When writing, always write 0.	R/W
b31 to b4	BulkCurrentED [27:0]	ED physical address	These bits indicate the physical address of the current ED being processed in the bulk list. The host logic updates these bits every time the bulk ED processing is completed. When creating a new list, set these bits to 0000 0000h, which indicates the end of the list. When transfer is temporarily stopped and then restarted, make sure that the ED indicated by the link pointer in BulkCurrentED exists.	R/W

31.3.1.13 HcDoneHead Register

Address(es) A004 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DoneHead[27:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DoneHead[27:0]												—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	Don't care	R
b31 to b4	DoneHead [27:0]	HcDoneHead physical address	These bits indicate the physical address of HcDoneHead in the host logic. This is the physical address of the last completed TD to be added to the Done queue.	R

31.3.1.14 HcFmInterval Register

Address(es) A004 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FIT	FSMPS[14:0]														
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	FI[13:0]													
Value after reset	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	FI[13:0] (FrameInterval)	Frame interval setting	These bits specify the length (bit time) of a frame used for FS transfer. To conform to the USB standard (one frame = 1 ms), set these bits to 2EDFh.	R/W
b15, b14	—	Reserved	When writing, always write 0.	R/W
b30 to b16	FSMPS[14:0] (FSLagest DataPacket)	FSt transfer packet maximum size setting	These bits specify the maximum amount of data that can be transferred without generating a schedule overrun. This setting is compared with the current location in the frame to determine up to which data in the frame can be transferred. The maximum amount depends on the system bus performance, and it should be specified by the driver.	R/W
b31	FIT (FrameInterval Toggle)	Frame synchronization	This bit is used to match the frame settings between software and the host logic. When updating the FI bits, software should toggle this bit. When loading the FI bit value, the host logic copies the FIT value to bit 31 (FRT) in the HcFmRemaining register. Software can check if the new FI bit setting has been reflected by comparing the value specified in this bit when the FI bits are written to, and the value read from the FRT bit.	R/W

31.3.1.15 HcFmRemaining Register

Address(es) A004 0038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FRT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	FR[13:0]													
Value after reset	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	FR[13:0] (Frame Remaining)	Down counter frame	These are the register bits of a 14-bit down counter which counts down the current remaining time value during transmission of a frame. That is, the value of these bits is decremented over time. When the value reaches 0000h, these bits are reloaded with the frame interval value by copying this value from bits [13:0] (FI) in the HcFmInterval register, after which counting down is restarted.	R
b30 to b14	—	Reserved	Don't care	R
b31	FRT (Frame Remaining Toggle)	Frame synchronization	This bit is used to match the frame settings between software and the host logic. When the FR bits reach 0000h, the host logic copies the value of bits [13:0] (FI) in the HcFmInterval register to the FR bits and also copies the value of bit 31 (FIT) in the HcFmInterval register to this bit. Software can check if the FI bit setting has been copied to the FR bits by comparing the values of the FIT bit and this bit.	R

31.3.1.16 HcFmNumber Register

Address(es) A004 003Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FrameNumber[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	FrameNumber [15:0]	Elapsed frame number	These bits indicate the elapsed frame count. The count in these bits is incremented when the value of bits [13:0] (FR) in the HcFmRemaining register reaches 0000h.	R
b31 to b16	—	Reserved	Don't care	R

31.3.1.17 HcPeriodicStart Register

Address(es) A004 0040h

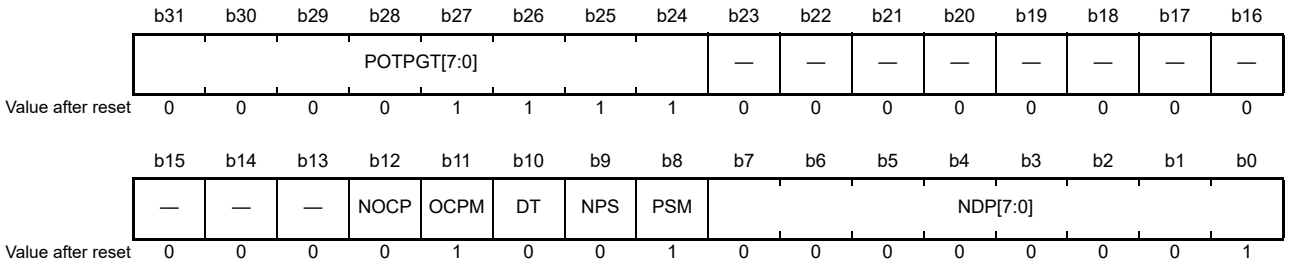
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PeriodicStart[13:0]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	PeriodicStart [13:0]	Periodic list processing start time	These bits indicate the time when the host logic starts periodic list processing in a frame. Specify a value in these bits by software during initialization of the host logic. When the value of bits [13:0] (FR) in the HcFmRemaining register is greater than the value specified in these bits, non-periodic lists take priority over periodic lists. The OHCI standard recommends that this value be set to about 90% of the value of bits [13:0] (FI) in the HcFmInterval register. Therefore, the recommended value is 2A2Fh	R/W
b31 to b14	—	Reserved	When writing, write 0.	R/W

31.3.1.18 HcRhDescriptorA Register

Address(es) A004 0048h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	NDP[7:0] (Number Downstream Port)	Downstream port number	These bits specify the number of downstream ports supported by the root hub in the host logic.	R
b8	PSM (PowerSwitchingMode)	Power switch control	This bit specifies how to control the power switch to each port of the root hub. While bits [31:16] (PPCM) in the HcRhDescriptorB register are set, each port responds only to Set/ClearPortPower. While the bits are cleared, each port is controlled by Set/ClearGlobalPower. This bit setting is valid only when the NPS bit is cleared. 0: Power to all ports is controlled together. 1: Power to each port is separately controlled.	R/W
b9	NPS (NoPower Switching)	Power control	This bit specifies how to control the port power. 0: Port power can be switched on and off. 1: Port power is always turned on while the host logic is operating.	R/W
b10	DT (DeviceType)	Device type	This bit indicates that the root hub is not a compound device. As the root hub is not allowed to be a compound device, this bit is always read as 0.	R
b11	OCPM (OverCurrent Protection Mode)	Overcurrent state reporting	This bit specifies how to report the overcurrent state of the root hub. This bit should be set to the same mode as that specified in the PSM bit. This setting is valid only when the NOCP bit is cleared. 0: Overcurrent state of all ports is collectively reported. 1: Overcurrent state of each port is separately reported.	R/W
b12	NOCP (NoOver Current Protection)	Overcurrent function support	This bit specifies whether to support the overcurrent protection function for the root hub. 0: Overcurrent protection function is supported. 1: Overcurrent protection function is not supported.	R/W
b23 to b13	—	Reserved	When writing, write 0.	R/W
b31 to b24	POTPGT[7:0] (PowerOnTo PowerGood Time)	Wait time	These bits indicate the time that software should wait before accessing a root hub port after power supply to the port is started. The unit of time is 2 ms. Therefore, the wait time is obtained by POTPGT × 2 ms.	R/W

31.3.1.19 HcRhDescriptorB Register

Address(es) A004 004Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PPCM[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DR[15:0] (Device Removable)	Device removable	These bits indicate whether the device connected to each port in the root hub is removable. Each bit is dedicated to a single port. The USB host controller has port 1 only.	R
b1				R/W
b15 to b2				R

Bit	Value	Description
0	—	Reserved
1	0	Device connected to port 1 is not removable.
	1	Device connected to port 1 is removable.
[15:2]	—	Reserved

Bit	Symbol	Bit Name	Description	R/W
b16	PPCM[15:0] (PortPower ControlMask)	Power control command	These bits specify power control commands for each port. This setting is valid when bit 8 (PSM) in the HcRhDescriptorA register is set. Each bit is dedicated to a single port. The USB host controller has port 1 only.	R
b17				R/W
b31 to b18				R

Bit	Value	Description
0	—	Reserved
1	0	All ports are collectively controlled (Set/ClearGlobalPower).
	1	Port 1 is separately controlled (Set/ClearPortlPower).
[15:2]	—	Reserved

31.3.1.20 HcRhStatus_A, HcRhStatus_B Register

(1) HcRhStatus_A Register

Address(es) A004 0050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCIC	SGP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCI	CGP
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CGP (ClearGlobal Power)	Global power clear	Setting this bit to 1 turns off the power to a port. The port to be turned off is determined according to the settings of bit 8 (PSM) in the HcRhDescriptorA register and bits [31:16] (PPCM) in the HcRhDescriptorB register. The USB host controller has port 1 only.	W
b1	OCI (OverCurrent Indicator)	Overcurrent indicator	This bit reports the overcurrent state in global overcurrent detection mode. When overcurrent is reported separately for each port, this value is always 0. 0: Port is in normal state. 1: Port is in overcurrent state.	R
b14 to b2	—	Reserved	When writing, write 0.	R/W
b15	SRWE (SetRemote Wakeup Enable)	DRWE bit enable	This bit sets the DRWE bit. Setting this bit sets the DRWE bit. Writing 0 has no effect.	W
b16	SGP (SetGlobal Power)	Port power setting	Setting this bit to 1 turns on the power to a port. The port to be turned on is determined according to the settings of bit 8 (PSM) in the HcRhDescriptorA register and bits [31:16] (PPCM) in the HcRhDescriptorB register. The USB host controller has port 1 only.	W

value	PSM	PPCM[1]	Description
0	—	—	No Change
1	0	—	The PPS bit in the HcRhPortStatus1 register is cleared.
	1	0	The PPS bit in the HcRhPortStatus1 register is cleared.
		1	No Change

value	PSM	PPCM[1]	Description
0	—	—	No Change
1	0	—	The PPS bit in the HcRhPortStatus1 register is set.
	1	0	The PPS bit in the HcRhPortStatus1 register is set.
		1	No Change

Bit	Symbol	Bit Name	Description	R/W
b17	OCIC (OverCurrent Indicate Change)	OCI bit change report	This bit notifies that the OCI bit value has changed. It is set when the OCI bit changes. Writing 1 to this bit while it is set to 1 clears it. Writing 0 has no effect. 0: Nothing is to be done in case of an overcurrent. 1: OverCurrent state has changed.	R/W
b30 to b18	—	Reserved	When writing, write 0.	R/W
b31	CRWE (Clear Remote Wakeup Enable)	DRWE bit clear	This bit clears the DRWE bit. Setting this bit clears the DRWE bit. Writing 0 has no effect.	W

(2) HcRhStatus_B Register

Address(es) A004 0050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCIC	LPSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCI	LPS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LPS (LocalPower Status)	Local power status	This product does not support the local power status function; this bit is always read as 0.	R
b1	OCI (OverCurrent Indicator)	Overcurrent indicator	This bit reports the overcurrent state in global overcurrent detection mode. When overcurrent is reported separately for each port, this value is always 0. 0: Port is in normal state. 1: Port is in overcurrent state.	R
b14 to b2	—	Reserved	When writing, write 0.	R/W
b15	DRWE (Device Remote Wakeup Enable)	Device remote start enable	This bit specifies whether to include bit 16 (CSC) in the HcRhPortStatus1 register as a remote wakeup event. When a connect status change event occurs while this bit is set, transition from the USB suspend state to the USB resume state occurs and the resume detect interrupt is generated. 0: ConnectStatusChange is not a RemoteWakeup source. 1: ConnectStatusChange is a RemoteWakeup source.	R
b16	LPSC (LocalPower Status Change)	Local power status change	This product does not support the local power status function and this bit is always read as 0.	R
b17	OCIC (OverCurrent Indicate Change)	OCI bit change report	This bit notifies that the OCI bit value has changed. It is set when the OCI bit changes. Writing 1 to this bit while it is set to 1 clears it. Writing 0 has no effect. 0: Nothing is to be done in case of an overcurrent. 1: OverCurrent state has changed.	R/W
b30 to b18	—	Reserved	When writing, write 0.	R/W
b31	CRWE (Clear Remote Wakeup Enable)	DRWE bit clear	This bit clears the DRWE bit. Setting this bit clears the DRWE bit. Writing 0 has no effect.	W

31.3.1.21 HcRhPortStatus1_A, HcRhPortStatus1_B Register

(1) HcRhPortStatus1_A Register

Address(es) A004 0054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	PRSC	OCIC	PSSC	PESC	CSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CPP	SPP	—	—	—	SPR	CSS	SPS	SPE	CPE
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPE (ClearPort Enable)	PES bit clear	This bit is used to clear the PES bit. Writing 1 makes the port enter the disabled state. Writing 0 has no effect.	W
b1	SPE (SetPort Enable)	PES bit enable	This bit is used to set the PES bit. Writing 1 makes the port enter the enabled state. Writing 0 has no effect. Note 1. To control port state transition, use bit 4 (SPR) in the HcRhPortStatus1_A register. The OHCI standard supports use of the SPE bit to make the port enter the enabled state, but the USB standard does not support this.	W
b2	SPS (SetPort Suspend)	Port state Suspend transition	This bit shifts the port to the suspend state. Writing 1 makes the port enter the suspend state. Writing 0 has no effect. If this bit is written to while the CCS bit is cleared, the CSC bit is set to notify the driver of an attempt to suspend a disconnected port.	W
b3	CSS (ClearSuspend Status)	Suspend clear	This bit terminates the suspend state and starts the Resume sequence. Writing 1 starts the Resume sequence. Writing 0 has no effect. The Resume sequence starts only while the PSS bit is set.	W
b4	SPR (SetPortReset)	Port reset issuing	This bit applies a port reset to a downstream port. Writing 1 to this bit starts a 10-ms port reset. If this bit is written to while the CCS bit is cleared, the PRS bit will not be set. Instead, the CSC bit is set to notify software of an attempt to reset a port where no device is connected. Writing 0 has no effect.	W
b7 to b5	—	Reserved	When writing, write 0.	R/W
b8	SPP (SetPort Power)	Port power-on	This bit turns on the port power when power is separately controlled for each port. Writing 1 turns on the port. Writing 0 has no effect.	W
b9	CPP (ClearPort Power)	Port power clear	This bit turns off the port power when power is separately controlled for each port. Writing 1 turns off the port. Writing 0 has no effect.	W
b15 to b10	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b16	CSC (ConnectStatus Change)	CCS bit status	This bit indicates that the CCS bit value has changed. The host logic sets this bit when the CCS bit changes due to device connection or disconnection. In addition, when a request for port reset, port suspension, or port enable is issued in the disconnection state, this bit is set to make software re-evaluate the device connection state. It is cleared when 1 is written by software. 0: Nothing is to be done regarding CCS. 1: CCS has changed.	R/W
b17	PESC (PortEnable StatusChange)	PES bit status	This bit indicates that the PES bit value has changed. It is set when the port state has changed due to a hardware event, such as the overcurrent state, disconnection, power-off, or a babble error. It is cleared when 1 is written by software. 0: Nothing is to be done regarding PES. 1: PES state has changed.	R/W
b18	PSSC (PortSuspend StatusChange)	RESUME sequence complete	This bit indicates that the RESUME sequence has been completed. It is set when all RESUME processing by hardware has been completed. It is cleared when 1 is written by software. In addition, it is cleared when the PRSC bit is set. 0: RESUME has not been completed. 1: RESUME has been completed.	R/W
b19	OCIC (OverCurrent IndicateChange)	Overcurrent state detection	This bit is set when the overcurrent state of the port has been detected. It is valid only while the overcurrent state is reported separately for each port (OCPM = 1 in the HcRhDescriptorA register). It is cleared when 1 is written by software. 0: Nothing is to be done regarding overcurrent state. 1: Overcurrent state has changed.	R/W
b20	PRSC (PortReset StatusChange)	Port reset complete	This bit indicates that a port reset has been completed. It is set when the host logic has completed a 10-ms hardware reset. It is cleared when 1 is written by software. 0: Port reset has not been completed, or nothing is to be done regarding the PRS bit. 1: Port reset has been completed.	R/W
b31 to b21	—	Reserved	When writing, write 0.	R/W

(2) HcRhPortStatus1_B Register

Address(es) A004 0054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	PRSC	OCIC	PSSC	PESC	CSC
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LSDA	PPS	—	—	—	PRS	POCI	PSS	PES	CCS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CCS (Current ConnectStatus)	Connection status indication	This bit indicates the current connection state of the downstream port. 0: No device is connected. 1: Device is connected.	R
b1	PES (PortEnable Status)	Port state enable status	This bit indicates whether the port is enabled or disabled. The host logic automatically clears this bit upon detecting the overcurrent state, disconnection, power-off, or a babble error. At this time, the PESC bit is set. This bit cannot be set while the CCS bit is cleared (no device is connected). The host logic sets this bit when a port reset is completed or suspension of the port is terminated. 0: Port is disabled. 1: Port is enabled.	R
b2	PSS (PortSuspend Status)	Suspend/Resume status	This bit indicates that the port is in the suspend state or the Resume sequence. Writing to the SPS bit sets this bit. This bit is not set while the CCS bit is cleared (no device is connected). This bit is cleared with the following timing: • When the Resume sequence is completed and the PSSC bit is set. • When a port reset is completed and the PRSC bit is set. • In the USB RESUME state. 0: Port is in normal transfer state. 1: Port is in suspend state.	R
b3	POCI (PortOver Current Indicator)	Downstream port overcurrent detection	This bit indicates that a downstream port has entered the overcurrent state. It is valid only while the overcurrent state is reported separately for each port (OCPM = 1 in the HcRhDescriptorA register). While the overcurrent state in all ports is collectively reported, this bit is 0b. 0: Port is in normal state. 1: Port is in overcurrent state.	R
b4	PRS (PortReset Status)	Port reset status	This bit indicates the reset state of the port. It is cleared at the same time as when the PRSC bit is set after a 10-ms port reset is completed. This bit cannot be set while the CCS bit is cleared (device is not connected). 0: Port reset is not in progress. 1: Port reset is in progress.	R
b7 to b5	—	Reserved	When writing, write 0.	R/W
b8	PPS (PortPower Status)	Power status	This bit indicates the power state of the port. It is cleared when an overcurrent is detected. 0: Port power is off. 1: Port power is on.	R

Bit	Symbol	Bit Name	Description	R/W
b9	LSDA (LowSpeed DeviceAttached)	Device speed	This bit indicates the speed of the device connected to the port. This status bit is valid only while the CCS bit is set. 0: FS device is connected. 1: LS device is connected.	R
b15 to b10	—	Reserved	When writing, write 0.	R/W
b16	CSC (ConnectStatus Change)	CCS bit status	This bit indicates that the CCS bit value has changed. The host logic sets this bit when the CCS bit changes due to device connection or disconnection. In addition, when a request for port reset, port suspension, or port enable is issued in the disconnection state, this bit is set to make software re-evaluate the device connection state. It is cleared when 1 is written by software. 0: Nothing is to be done regarding CCS. 1: CCS has changed.	R/W
b17	PESC (PortEnable StatusChange)	PES bit status	This bit indicates that the PES bit value has changed. It is set when the port state has changed due to a hardware event, such as the overcurrent state, disconnection, power-off, or a babble error. It is cleared when 1 is written by software. 0: Nothing is to be done regarding PES. 1: PES state has changed.	R/W
b18	PSSC (PortSuspend StatusChange)	RESUME sequence complete	This bit indicates that the RESUME sequence has been completed. It is set when all RESUME processing by hardware has been completed. It is cleared when 1 is written by software. In addition, it is cleared when the PRSC bit is set. 0: RESUME has not been completed. 1: RESUME has been completed.	R/W
b19	OCIC (OverCurrent IndicateChange)	Overcurrent state detection	This bit is set when the overcurrent state of the port has been detected. It is valid only while the overcurrent state is reported separately for each port (OCPM = 1 in the HcRhDescriptorA register). It is cleared when 1 is written by software. 0: Nothing is to be done regarding overcurrent state. 1: Overcurrent state has changed.	R/W
b20	PRSC (PortReset StatusChange)	Port reset complete	This bit indicates that a port reset has been completed. It is set when the host logic has completed a 10-ms hardware reset. It is cleared when 1 is written by software. 0: Port reset has not been completed, or nothing is to be done regarding the PRS bit. 1: Port reset has been completed.	R/W
b31 to b21	—	Reserved	When writing, write 0.	R/W

31.3.2 EHCI Operational Registers

Access the EHCI operational registers after starting up the PHY internal PLL. For details, see Figure 31.13, Initial Setting Sequence.

31.3.2.1 HCIVERSION/CAPLENGTH Register

Address(es) A004 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Interface Version Number[15:0]															
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	Capability Registers Length[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Capability Registers Length [7:0]	Host logic operational register start address	These bits indicate the start address of the host logic operational registers. As the host logic operational registers are allocated from address 20h, this value is set to 20h.	R
b15 to b8	—	Reserved	Don't care	R
b31 to b16	Interface Version Number [15:0]	EHCI version	These bits indicate the version of the EHCI specifications supported by the host logic. As the host logic conforms to the EHCI Rev. 1.0, this value is set to 0100h.	R

31.3.2.2 HCSPARAMS Register

Address(es) A004 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	Debug Port Number[3:0]				—	—	—	P_INDICATOR
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	N_CC[3:0]				N_PCC[3:0]				Port Routing Rules	—	—	PPC	N_PORTS[3:0]			
Value after reset	0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	N_PORTS [3:0] (Number of Ports)	Number of downstream port	These bits indicate the number of physical downstream ports used by the host logic. These bits reflect the setting of bits [1:0] (Port_no) in the PCI Configuration EXT1 register. As the USB host controller has only one port, this value is set to 1h.	R
b4	PPC (Port Power Control)	Port power control	This bit indicates how to control the port power in the host logic. As the USB host controller supports the power supply control function, this value is set to 1.	R
b6, b5	—	Reserved	Don't care	R
b7	Port Routing Rules	Port routing rules	This bit indicates how ports are mapped in the OHCI host logic. As the value of the HCSP_PORTROUTE register shows the mapping in the host logic, this value is set to 1h.	R
b11 to b8	N_PCC[3:0] (Number of Ports per Companion Controller)	Number of Port	These bits indicate the number of the port supported by one OHCI host logic unit. These bits reflect the setting of bits [1:0] (Port_no) in the PCI Configuration EXT1 register. As the USB host controller has only one port, this value is set to 1h.	R
b15 to b12	N_CC[3:0] (Number of Companion Controller)	Number of OHCI host logic	These bits indicate the number of OHCI host logic units related to the EHCI host logic. As the host logic has one OHCI host logic unit, this value is set to 1h.	R
b16	P_INDICATOR	Port indicator control support	This bit indicates whether the host logic supports the port indicator control function. As the host logic does not support the port indicator control function, this value is set to 0.	R
b19 to b17	—	Reserved	Don't care	R
b23 to b20	Debug Port Number[3:0]	Debug port number	These bits indicate that the host logic ports are debug ports. As the host logic has no debug ports, this value is set to 0000b.	R
b31 to b24	—	Reserved	Don't care	R

31.3.2.3 HCCPARAMS Register

Address(es) A004 1008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EECP[7:0]								IST[3:0]				—	ASPC	PFLF	AC64
Value after reset	1	1	1	0	1	0	0	0	0	0	0	0	0	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	AC64	Memory pointer selection	This bit indicates whether data structures use 32-bit address memory pointers or 64-bit address memory pointers. As the host logic supports data structures using 32-bit address memory pointers, this value is set to 0. 64-bit address memory pointers are not supported.	R
b1	PFLF	Programming frame list flag	This bit indicates the setting regarding the frame list size that software can use. This value is set to 1 in this host logic. When this bit is set to 1, the available frame list size can be specified through bits [3:2] (Frame List Size) in the USBCMD register. A frame list size smaller than 4 Kbytes can be specified.	R
b2	ASPC	Asynchronous schedule park support capability	This bit indicates whether to support the park mode for the high-speed QH (queue head) in the asynchronous schedule. As the host logic supports this function, this value is set to 1.	R
b3	—	Reserved	Don't care	R
b7 to b4	IST[3:0]	Isochronous data structure threshold	As the host logic in this product does not support caching of the isochronous data structure in the entire frame, these bits are set to 0h.	R
b15 to b8	EECP[7:0] (EHCI Extend Capabilities Pointer)	Offset address	These bits indicate the offset address for the EHCI extend capabilities registers. This indicates that extend registers are placed at addresses starting from E8h in the EHCI configuration space. As the host logic does not support the legacy function, the value read from these bits has no meaning.	R
b31 to b16	—	Reserved	Don't care	R

31.3.2.4 HCSP_PORTROUTE Register

Address(es) A004 100Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Companion Port Route[31:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Companion Port Route[31:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	Companion Port Route[31:0]	OHCI Host Port Indication	These bits indicate the ports that the OHCI host logic controls. As the host logic has one OHCI host logic unit, these bits are set to 0000 0000h.	R

31.3.2.5 USBCMD Register

Address(es) A004 1020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	Interrupt Threshold Control[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	Asynchronous Schedule Park Mode Enable	—	ASPMC[1:0]		Light Host Controller Reset	Interrupt on Async Advance Doorbell	ASPME	Periodic Schedule Enable	Frame List Size[1:0]		HCRESET	RS
Value after reset	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RS (Run/Stop)	EHCI host logic run/stop	This bit activates or stops the EHCI host logic. When this bit is set to 1, the host logic starts operation. As long as this value is 1, the host logic continues operation. Note that this bit should be set to 1 only while the host logic is in the halt state. Bit 12 (HCHalted) in the USBSTS register indicates that the host logic has completed transactions and entered the halt state. 0: Stopped (the host logic has completed transactions and halted). 1: Activated (the host logic executes the schedule).	R/W
b1	HCRESET (Host Controller Reset)	Host logic initialization	This bit initializes the host logic. When this bit is set to 1, the host logic initializes the internal pipelines and state machine. Communication through the USB stops immediately. A USB reset is not issued to downstream ports at this time. This reset does not initialize the PCI configuration registers, but it initializes the EHCI operational registers and the port ownership is returned to OHCI. This bit is automatically cleared to 0 by the host logic when the reset is completed. The reset cannot be aborted by software by writing 0 to this bit. This bit should be set only while bit 12 (HCHalted) in the USBSTS register is 1.	R/W
b3, b2	Frame List Size[1:0]	Frame list size	These bits specify the frame list size. The setting in these bits determines the size of the Frame List Current index in the FRINDEX register. b3 b2 0 0: 1024 elements (4096 bytes) 0 1: 512 elements (2048 bytes) 1 0: 256 elements (1024 bytes) 1 1: Reserved	R/W
b4	Periodic Schedule Enable	Periodic schedule enable	This bit specifies whether to advance or skip periodic list processing. 0: Periodic list processing is not executed (skipped). 1: Periodic list processing is executed using the PERIODICLISTBASE register. Note: For transferring data via USB while this bit is being 0, set b12 of the EXT1 register to 0. For details, see section 31.3.3.12, Offset E0h Register (EXT1).	R/W
b5	ASPME	Asynchronous schedule enable	This bit specifies whether to advance or skip asynchronous list processing. 0: Asynchronous list processing is not executed (skipped). 1: Asynchronous list processing is executed using the ASYNCLISTADDR register.	R/W

Bit	Symbol	Bit Name	Description	R/W
b6	Interrupt on Async Advance Doorbell	Doorbell	This bit is used as a doorbell by software. Software sets this bit to 1 to generate an interrupt when processing proceeds with the next QH (queue head). While bit 5 (Interrupt on Async Advance Enable) in the USBINTR register is set to 1, an interrupt is generated with the next interrupt timing after 1 is written to this bit. If this bit is set while bit 5 (Interrupt on Async Advance Enable) in the USBINTR register is 0, correct operation is not guaranteed. This bit is cleared by the host logic. Upon completing the processing of a QH normally, the host logic clears this bit to 0 and sets bit 5 (Interrupt on Async Advance) in the USBSTS register to 1.	R/W
b7	Light Host Controller Reset	Light host controller reset execution status	This bit indicates the state of Light Host Controller Reset execution. As the host logic does not support Light Host Controller Reset, this value is fixed to 0.	R
b9, b8	ASPMC[1:0]	Asynchronous schedule park transaction count	These bits specify the number of transactions that can be executed in succession from one QH (queue head). A value from 1h to 3h can be specified. This setting is valid when bit 11 (Asynchronous Schedule Park Mode Enable) is 1.	R/W
b10	—	Reserved	When writing, write 0.	R/W
b11	Asynchronous Schedule Park Mode Enable	Park mode enable	This bit enables or disables the park mode. 0: Disabled 1: Enabled	R/W
b15 to b12	—	Reserved	When writing, write 0.	R/W
b23 to b16	Interrupt Threshold Control[7:0]	Host logic interrupt generation maximum rate	These bits indicate the maximum rate at which the host logic generates an interrupt. Correct operation is not guaranteed if a value not shown below is written to these bits. 00h: Reserved 01h: 1 micro-frame 02h: 2 micro-frames 04h: 4 micro-frames 08h: 8 micro-frames (1 ms) 10h: 16 micro-frames (2 ms) 20h: 32 micro-frames (4 ms) 40h: 64 micro-frames (8 ms)	R/W
b31 to b24	—	Reserved	When writing, write 0.	R/W

31.3.2.6 USBSTS Register

Address(es) A004 1024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Asynchronous Schedule Status	Periodic Schedule Status	Reclamation	HCHalted	—	—	—	—	—	—	Interrupt on Async Advance	Host System Error	Frame List Rollover	Port Change Detect	USBERRINT	USBINT
Value after reset	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	USBINT (USB Interrupt)	USB transfer complete	This bit indicates that USB transfer has been completed. The host logic sets this bit to 1 when either of the following conditions is satisfied. • USB transfer is completed • A short packet is received Even if USB transfer has ended with an error, this bit is set to 1 when the IOC (Interrupt On Complete) bit in the TD is 1. Writing 1 can clear this bit. Writing 0 has no effect. 0: USB transfer has not been completed. 1: USB transfer has been completed.	R/W
b1	USBERRINT (USB Error Interrupt)	USB transaction status	This bit indicates that a USB transaction has ended with an error. The host logic sets this bit to 1 when a USB transaction has ended with an error. Such an error includes the case when the error counter underflows. Writing 1 can clear this bit. Writing 0 has no effect. 0: USB transaction has been completed normally. 1: USB transaction has ended with an error.	R/W
b2	Port Change Detect	Port state change detection	This bit indicates that the port state has changed. The host logic sets this bit to 1 when any of the following conditions is satisfied in a port for which bit 13 (Port Owner) in the PORTSC[n] register is set to 0. [1 setting condition] • Bit 1 (Connect Status Change) in the PORTSC[n] register has changed from 0 to 1. (Device connection or disconnection has been detected.) • Bit 3 (Port Enable/Disable Change) in the PORTSC[n] register has changed from 0 to 1. (The port enabled state has changed.) • Bit 5 (Over-current Change) in the PORTSC[n] register has changed from 0 to 1. (The overcurrent state has been detected.) • Bit 6 (Force Port Resume) in the PORTSC[n] register has changed from 0 to 1. (indicating detection of a J-to-K transition on a port while suspended.) Writing 1 by software can clear this bit. Writing 0 has no effect.	R/W
b3	Frame List Rollover	Frame list rollover	The host logic sets this bit to 1 when the value of the Frame Index bits in the FRINDEX register returns from the maximum value to 000h (rollover). The maximum value at which rollover occurs depends on bits [3:2] (Frame List Size) in the USBCMD register. Writing 1 can clear this bit. Writing 0 has no effect. 0: Frame list has not returned to 000h. 1: Frame list has returned to 000h.	R/W

Bit	Symbol	Bit Name	Description	R/W
b4	Host System Error	Host system error	This bit is set to 1 when a serious error occurs in the host logic. Such an error includes a parity error in the PCI system. If this error occurs, the host logic clears bit 0 (RS) in the USBCMD register to 0 to stop execution of the remaining TDs. Writing 1 can clear this bit. Writing 0 has no effect. 0: No system error has occurred. 1: System error has occurred.	R/W
b5	Interrupt on Async Advance	Async advance interrupt status	This bit indicates the Async Advance interrupt state. Upon fetching QH, the host logic checks bit 6 (Interrupt on Async Advance Doorbell (IAAD)) in the USBCMD register. When the IAAD bit is 1, the host logic clears the IAAD bit and sets this bit after completing QH processing normally. When bit 5 (Interrupt on Async Advance Enable) in the USBINTR register is 1, an interrupt is generated from this source with the next interrupt timing after this bit is set to 1. Writing 1 can clear this bit. Writing 0 has no effect. 0: No Async Advance interrupt has occurred. 1: Async Advance interrupt state has been detected.	R/W
b11 to b6	—	Reserved	When writing, write 0.	R/W
b12	HCHalted	EHCI host logic status	This bit is set to 0 when bit 0 (RS) in the USBCMD register is 1. When the RS bit is cleared to 0 by the host logic or software, the EHCI host logic stops execution and this bit is set to 1 by the host logic. 0: EHCI host logic is in execution. 1: EHCI host logic is stopped.	R
b13	Reclamation	Empty asynchronous schedule detection	This bit is used to detect an empty asynchronous schedule. The host logic clears this bit to 0 after a reset or when it fetches QH with H = 1. When the host logic executes an asynchronous transaction or has detected a start event, it sets this bit to 1. When the host logic fetches QH with H = 1b while this bit is 0, the Async Sched Sleeping mode is entered.	R
b14	Periodic Schedule Status	Periodic schedule status	This bit indicates the current state of the periodic schedule. The periodic schedule is enabled (1) or disabled (0) when the values of this bit and bit 4 (Periodic Schedule Enable) in the USBCMD register are the same. 0: Periodic schedule is disabled. 1: Periodic schedule is enabled.	R
b15	Asynchronous Schedule Status	Asynchronous schedule status	This bit indicates the current state of the asynchronous schedule. The asynchronous schedule is enabled (1) or disabled (0) when the values of this bit and bit 5 (ASPME) in the USBCMD register are the same. 0: Asynchronous schedule is disabled. 1: Asynchronous schedule is enabled.	R
b31 to b16	—	Reserved	When writing, write 0.	R/W

31.3.2.7 USBINTR Register

Address(es) A004 1028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	Interrupt on Async Advance Enable	Host System Error Enable	Frame List Rollover Enable	Port Change Interrupt Enable	USB Error Interrupt Enable	USB Interrupt Enable
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	USB Interrupt Enable	USB interrupt enable	This bit enables or disables the setting in bit 0 (USBINT) in the USBSTS register. To clear the interrupt, use the USBINT bit. 0: Disabled 1: Enabled	R/W
b1	USB Error Interrupt Enable	USB error interrupt enable	This bit enables or disables the setting in bit 1 (USBERRINT) in the USBSTS register. To clear the interrupt, use the USBERRINT bit. 0: Disabled 1: Enabled	R/W
b2	Port Change Interrupt Enable	Port change interrupt enable	This bit enables or disables the setting in bit 2 (Port Change Detect) in the USBSTS register. To clear the interrupt, use the Port Change Detect bit. 0: Disabled 1: Enabled	R/W
b3	Frame List Rollover Enable	Frame list rollove enable	This bit enables or disables the setting in bit 3 (Frame List Rollover) in the USBSTS register. To clear the interrupt, use the Frame List Rollover bit. 0: Disabled 1: Enabled	R/W
b4	Host System Error Enable	Host system error enable	This bit enables or disables the setting in bit 4 (Host System Error) in the USBSTS register. To clear the interrupt, use the Host System Error bit. 0: Disabled 1: Enabled	R/W
b5	Interrupt on Async Advance Enable	Interrupt on async advance enable	This bit enables or disables the setting in bit 5 (Interrupt on Async Advance) in the USBSTS register. To clear the interrupt, use the Interrupt on Async Advance bit. 0: Disabled 1: Enabled	R/W
b31 to b6	—	Reserved	When writing, write 0.	R/W

31.3.2.8 FRINDEX Register

Address(es) A004 102Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	Frame Index[13:0]													
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	Frame Index[13:0]	Frame index	These bits are used by the host logic to add an index to the periodic frame list. This value is incremented at the end of each micro-frame. Bits [N:3] are used as the Frame List Current index. This means that the current frame list is accessed 8 times before proceeding with the next index number. The value of N is determined as follows according to the setting of bits [3:2] (Frame List Size) in the USBCMD register. **Frame List Size / Number Elements / N** 00 (1024) 12 01 (512) 11 10 (256) 10 11 Reserved This register should be accessed only while the host logic is stopped (bit 12 (HCHalted) = 1 in the USBSTS register). This setting is reflected in the SOF frame number for the SOF token.	R/W
b31 to b14	—	Reserved	When writing, write 0.	R/W

31.3.2.9 CTRLDSSEGMENT Register

Address(es) A004 1030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CTRLDSSEGMENT[31:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTRLDSSEGMENT[31:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CTRLDSSEGMENT[31:0]	—	The host logic does not support 64-bit addressing and does not use this register. Therefore, do not access this register.	R

31.3.2.10 PERIODICLISTBASE Register

Address(es) A004 1034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BaseAddress (Low) [21:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BaseAddress (Low) [21:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	—	Reserved	When writing, write 0.	R/W
b31 to b12	BaseAddress (Low) [21:0]	Periodic frame list start address	These bits indicate the start address of the periodic frame list stored in the system memory. Software should specify the start address in this register before the host logic starts list processing. The host logic uses the values in these bits and bits [13:0] (Frame Index) in the FRINDEX register to determine the frame list to be processed. The address of the periodic frame list should be aligned with a 4-Kbyte boundary. Correct operation cannot be guaranteed if the value in these bits is modified during operation.	R/W

31.3.2.11 ASYNCLISTADDR Register

Address(es) A004 1038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LPL[26:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LPL[26:0]											—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	When writing, write 0.	R/W
b31 to b5	LPL[26:0] (Link Pointer Low)	Asynchronous Queue Head link pointer address	These bits indicate the address of the next asynchronous queue head in the system memory to be processed. The address of the asynchronous queue head should be aligned with a 32-byte boundary.	R/W

31.3.2.12 CONFIGFLAG Register

Address(es) A004 1060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CF
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF (Configure Flag)	Port routing control circuit configuration flag	This bit controls the default setting of the port routing control circuit regarding whether the ports are routed to OHCI or EHCI. Software should set this bit to 1 at the end of host logic configuration process. 0: Port routing control circuit routes each port to the OHCI host logic by default. 1: Port routing control circuit routes each port to the EHCI host logic by default.	R/W
b31 to b1	—	Reserved	When writing, write 0.	R/W

31.3.2.13 PORTSC1 Register

Address(es) A004 1064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	WKOC_E	WKDSCNNT_E	WKCNNT_E	Port Test Control [3:0]			
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Port Indicator Control[1:0]		Port Owner	PP	Line Status[1:0]		—	Port Reset	Suspend	Force Port Resume	Over-current Change	Over-current Active	Port Enable/ Disable Change	Port Enabled/ Disabled	Connect Status Change	Current Connect Status
Value after reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	Current Connect Status	Port connection status	This bit indicates the connection state of the port. Upon detecting device connection, the host logic sets this bit to 1. The host logic also sets this bit to 1 when Port Test Control[3:0] = 0101b (Test FORCE_ENABLE) even if no device is connected. Upon detecting device disconnection, the host logic clears this bit to 0. When the PP bit is 0 or the Port Owner bit is 0, this bit becomes 0. 0: No device is connected to the port. 1: Device is connected to the port.	R
b1	Connect Status Change	Connect status change	This bit indicates that the value of bit 0 (Current Connect Status) has changed. Writing 1 can clear this bit. Writing 0 has no effect. When the PP bit is 0, this bit becomes 0. 0: Nothing is to be done. 1: Value of bit 0 (Current Connect Status) has changed.	R/W
b2	Port Enabled/ Disabled	Port enable/disable status	This bit indicates the enabled/disabled state of the port. After resetting a port and detecting that the connected device is an HS device, the host logic enables the port and sets this bit to 1. Software cannot set this bit to 1. Upon detecting device disconnection or an error, the host logic disables the port and clears this bit to 0. Software can write 0 to disable the port. In this case, however, the bit value changes only after the port state actually changes. While the port is disabled, data transfer to downstream ports is blocked except for a port reset. When the PP bit is 0, this bit becomes 0. Note that when Port Test Control[3:0] = 0101b (Test FORCE_ENABLE), the port is enabled regardless of the port state and this bit is set to 1. 0: Port is disabled. 1: Port is enabled.	R/W
b3	Port Enable/ Disable Change	Port enable/disable status change	This bit indicates that the enabled/disabled state of the port has changed. Upon detecting a frame babble error, the host logic disables the port and sets this bit to 1. Writing 1 can clear this bit. Writing 0 has no effect. When the PP bit is 0, this bit becomes 0. 0: Nothing is to be done. 1: The port state has changed from enabled to disabled.	R/W
b4	Over-current Active	Port overcurrent status	This bit indicates the overcurrent state of the port. Upon detecting an overcurrent, the host logic clears bit 12 (PP) and its related bits and sets this bit to 1b. This bit is automatically cleared from 1 to 0 when the overcurrent state is resolved. 0: Port is not in overcurrent state. 1: Port is in overcurrent state.	R

Bit	Symbol	Bit Name	Description	R/W
b5	Over-current Change	Over-current Change	This bit indicates that the value of bit 4 (Over-current Active) has changed. Writing 1 can clear this bit. Writing 0 has no effect. 0: Nothing is to be done. 1: Value of bit 4 (Over-current Active) has changed.	R/W
b6	Force Port Resume	Port resume detection flag	This bit indicates detection of the resume state at the port. When a transition from the J to the K state (RemoteWakeup) is detected while the port is suspended, the host logic sets this bit and bit 2 (Port Change Detect) in the USBSTS register to 1. Software should also set this bit to 1 when the output of a resume signal is required. In this case, the Port Change Detect bit should not be set. The resume signal (FS K State) is driven on the USB port while this bit is 1. Clear this bit to 0 after an appropriate period has passed. Writing 0 to this bit while it is 1 returns the port to the HS Idle state. Until then, this bit remains at 1. When the PP bit is 0, this bit becomes 0. 0: Resume (K-state) has not been detected or output. 1: Resume (K-state) has been detected or output.	R/W
b7	Suspend	Port suspend	This bit indicates the suspend state of the port. 0: Port is not in suspend state. 1: Port is in suspend state. The combination of the settings of this bit and bit 2 (Port Enabled/Disabled) indicate the port state as follows. **Port Enabled/Disabled / Suspend / Port State** 0 / X / Disabled 1 / 0 / Enabled 1 / 1 / Suspend In the suspend state, data transfer from this port to the downstream port is blocked unless the port is reset. When this bit is set to 1 during data transfer, reflection in the status bit and blocking of transfer follow completion of the current transfer. Software should write 1 to this bit. It can write 1 only while PP bit = 1, Port Owner bit = 0, and Current Connect Status bit = 1 in the register in the host logic. This bit is always cleared to 0 under either of the following conditions. • Software clears the Force Port Resume bit to 0. • Software sets the Port Reset bit to 1. When the PP bit is 0, this bit becomes 0.	R/W
b8	Port Reset	Port reset status	This bit indicates the reset state of the port. 0: Port is not in reset state. 1: Port is in reset state. When software writes 1 to this bit while it is 0, the bus reset sequence defined in the USB2.0 standard begins. Write 0 to this bit to terminate the bus reset sequence. Note that this bit must be retained at 1 for long enough time for the bus reset sequence to be completed according to the USB2.0 standard. When bit 12 (HCHalted) in the USBSTS register is 1, the port should not be reset. This bit becomes 0 when the PP, Port Owner, or Current Connect Status bit satisfies the following conditions. • PP bit = 0, • Port Owner bit = 1, or • Current Connect Status bit = 0	R/W
b9	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b11, b10	Line Status[1:0]	D+/D- logic level	These bits indicate the current logical levels on the D+ and D- lines of the USB port (bit 11: D+; bit 10: D-). They are used to detect an LS device before a port reset or a sequence for enabling the port. Therefore, the values in these bits are valid only while bit 3 (Port Enable/Disable) = 0 and bit 0 (Current Connect Status) = 1. When the PP bit is 0, these bits become 0.	R

bit11 (D+)	bit10 (D-)	USB State	Interpretation
0	0	SE0	Not an LS device. Moves to the EHCI port reset execution process.
0	1	K State	An LS device has been connected. Passes the port ownership from EHCI to OHCI.
1	0	J State	Not an LS device. Moves to the EHCI port reset execution process.
1	1	Un-defined	Not an LS device. Moves to the EHCI port reset execution process.

Bit	Symbol	Bit Name	Description	R/W
b12	PP (Port Power)	Port power supply control	This bit controls power supply to the port. When this bit is 0, power is not supplied to the port; the port does not operate and connection or disconnection cannot be detected. If an overcurrent is detected while this bit is 1, the host logic clears this bit to 0 and stops power supply to the port. 0: No power is supplied to the port. 1: Power is supplied to the port. The function of this bit depends on the setting of bit 4 (PPC) in the HCSPARAMS register.	R/W

PPC	PP	Description
0	1	This bit is fixed to 1, and power is always supplied to the port.
1	0/1	Power supply to the port is determined by this bit.

Bit	Symbol	Bit Name	Description	R/W
b13	Port Owner	Port ownership	This bit indicates whether OHCI or EHCI has the port ownership. 0: EHCI has the port ownership. 1: OHCI has the port ownership. This bit is cleared to 0 when bit 0 (CF) in the CONFIGFLAG register changes from 0 to 1. This bit is set to 1 when the CF bit is 0. Software should set this bit to 1 to pass the port ownership to OHCI when the connected device is not a high-speed device.	R/W
b15, b14	Port Indicator Control[1:0]	—	As the host logic does not support the port indicator control function, these bits are set to 00b. Writing to these bits does not affect the operation.	R
b19 to b16	Port Test Control[3:0]	Pin test control	These bits control the test mode. For details of the test mode, see Chapter 7 in the USB Specification Revision 2.0.	R/W

Port Test Control[3:0]	Mode
0000b	Normal
0001b	Test J_STATE
0010b	Test K_STATE
0011b	Test SE0_NAK
0100b	Test Packet
0101b	Test FORCE_ENABLE
Other than the above	Reserved

Bit	Symbol	Bit Name	Description	R/W
b20	WKCNNT_E (Wake on Connect Enable)	Device connection detection enable	Writing 1 to this bit enables detection of device connection as a wakeup event. This bit setting does not affect the host logic operation. When the PP bit is 0, this bit becomes 0.	R/W
b21	WKDSCNNT_E (Wake on Disconnect Enable)	Device disconnection detection enable	Writing 1 to this bit enables detection of device disconnection as a wakeup event. This bit setting does not affect the host logic operation. When the PP bit is 0, this bit becomes 0.	R/W
b22	WKOC_E (Wake on Over-current Enable)	Overcurrent state detection enable	Writing 1 to this bit enables detection of the overcurrent state as a wakeup event. This bit setting does not affect the host logic operation. When the PP bit is 0, this bit becomes 0.	R/W
b31 to b23	—	Reserved	When writing, write 0.	R/W

31.3.3 PCI Configuration Registers for OHCI

31.3.3.1 Offset 00h Register (Vendor ID, Device ID)

Address(es) A005 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Device ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Vendor ID[15:0]															
Value after reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	Vendor ID [15:0]	Device vendor ID	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R
b31 to b16	Device ID [15:0]	Device ID	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R

31.3.3.2 Offset 04h Register (Command, Status)

Address(es) A005 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]		Data Parity Error Detected	Fast Back to Back Capable	—	—	Capabilities List	—	—	—	—
Value after reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

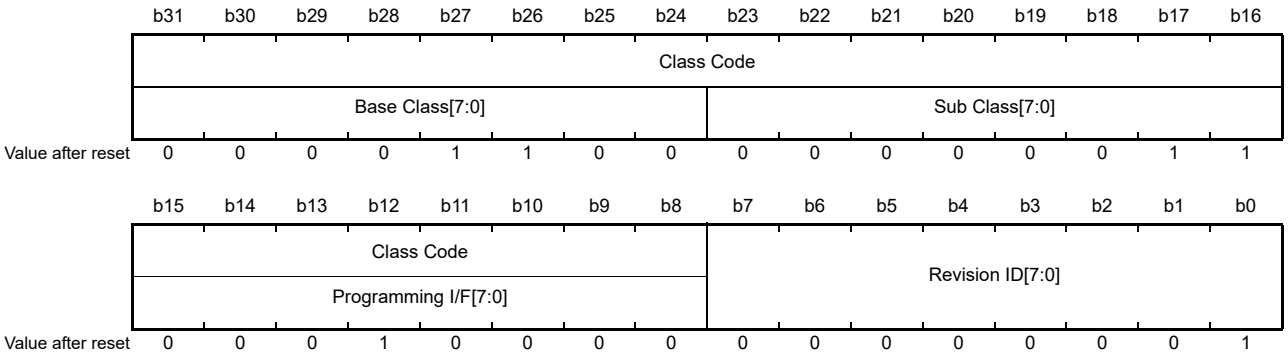
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate Enable	Special Cycle	Bus Master	Memory Space	I/O Space
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	I/O Space	I/O space access enable	This bit enables access to the I/O space. As the host logic does not accept I/O access, this value is always 0.	R
b1	Memory Space	Memory space access enable	This bit enables access to the memory space. This is an enable signal for memory access specified in the PCI standard. Set to 1 when accessing registers. Set this bit to 1 during initial setting of the host logic.	R/W
b2	Bus Master	Bus master enable	This bit enables bus master operation. This is an enable signal for master access to the PCI bus. Set to 1 when accessing the SRAM on the system bus. Set this bit to 1 during initial setting of the host logic.	R/W
b3	Special Cycle	Special cycle enable	This bit enables Special Cycle operation. As the host logic does not support the Special Cycle operation, this value is always 0.	R
b4	Memory Write and Invalidate Enable	Memory write and invalidate enable	This bit enables the Memory Write and Invalidate command. In the USB host controller, do not change this from the value after reset (0). 0: Memory write and invalidate command is disabled. 1: Memory write and invalidate command is enabled.	R/W
b5	VGA Palette Snoop	VGA palette snoop enable	This bit enables VGA palette snooping. As the host logic does not support VGA palette snooping, this value is always 0.	R
b6	Parity Error Response	Parity error response enable	This bit enables parity error response. 0: PERR0 is not asserted. 1: PERR0 is asserted. When a parity error is detected, the Detected Parity Error bit is set to 1 even if this bit is cleared to 0.	R/W
b7	Wait Cycle Control	Wait cycle control enable	This bit enables wait cycle control. As the host logic does not support address and data stepping, this value is always 0.	R
b8	SERR Enable	System error response enable	This bit enables system error response. 0: SERR0 is not asserted. 1: SERR0 is asserted. To notify of a system error through the SERR signal, set this bit to 1.	R/W
b9	Fast Back to Back Enable	Fast back to back enable	This bit enables fast back to back transactions. As the host logic does not support fast back to back transactions, this value is always 0.	R
b19 to b10	—	Reserved	When writing, write 0.	R/W
b20	Capabilities List	Power management mode support	This value is fixed to 1, which indicates that the power management mode is supported.	R
b22, b21	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b23	Fast Back to BackCapable	Fast back to back support	This bit indicates whether Fast Back to Back transactions are supported. As the host logic does not support Fast Back to Back transactions, this value is fixed to 0.	R
b24	Data Parity Error Detected	Data parity error detection flag	This bit is set when a parity error is detected in master operation. Writing 1 from the PCI bus clears this bit. The value is fixed to 0 while the Parity Error Response bit is set as disabled.	R/W
b26, b25	Devsel Timing[1:0]	DEVSEL response speed	These bits indicate the DEVSEL response speed. The value is fixed to 01b (medium-speed response).	R
b27	Signaled Target Abort	Slave/Target abort status	This is a status bit for Slave/Target abort. This bit is set to 1 in slave operation when the host logic has terminated, through Target Abort, the bus cycle in which the host logic is accessed. Writing 1 from the PCI bus clears this bit.	R/W
b28	Received Target Abort	Master/Target abort status	This is a status bit for Master/Target Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Target Abort. Writing 1 from the PCI bus clears this bit.	R/W
b29	Received Master Abort	Master/Master abort status	This is a status bit for Master/Master Abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Master Abort. Writing 1 from the PCI bus clears this bit.	R/W
b30	Signaled System Error	SERR status	This is a status bit for SERR. This bit is set to 1 when a system error occurs. Writing 1 from the PCI bus clears this bit.	R/W
b31	Detected Parity Error	Parity error status	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 from the PCI bus clears this bit.	R/W

31.3.3.3 Offset 08h Register (Revision ID, Class Code)

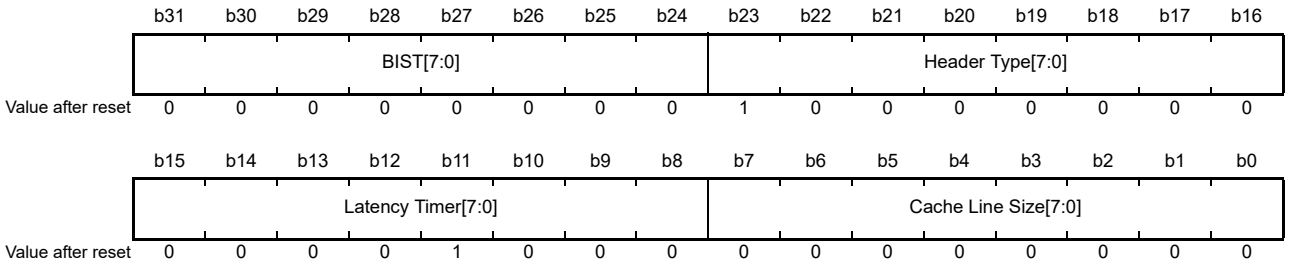
Address(es) A005 0008h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Revision ID [7:0]	Host logic revision	These bits indicate the revision of the host logic. The value is indicated as 01h.	R
b15 to b8	Programming I/F[7:0]	PCI standard program interface	These bits indicate the program interface specified in the PCI standard. The value is 10h, which indicates OHCI.	R
b23 to b16	Sub Class [7:0]	PCI standard subclass	These bits indicate the subclass specified in the PCI standard. The value is 03h, which indicates a USB device.	R
b31 to b24	Base Class [7:0]	PCI standard base class	These bits indicate the base class specified in the PCI standard. The value is 0Ch, which indicates a serial peripheral bus controller.	R

31.3.3.4 Offset 0Ch Register (Cache Line Size, Latency Timer, Header Type, BIST)

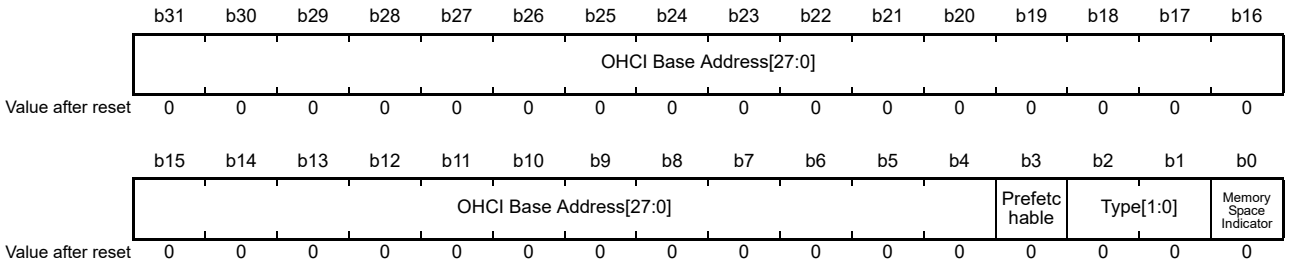
Address(es) A005 000Ch



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Cache Line Size[7:0]	Cache Line Size	These bits notify the system of the cache line size.	R/W
b9, b8	Latency Timer[7:0]	Latency Timer	These bits notify the system of the latency timer. The lowest 2 bits are fixed to 00b.	R
b15 to b10				R/W
b23 to b16	Header Type[7:0]	Header Type	These bits notify the system of the header type. As the header type is Type 0, bits [22:16] are fixed to 00h. As this is a multifunction device, bit 23 is fixed to 1.	R
b31 to b24	BIST[7:0]	Self-test	These bits are used for self testing. As the host logic does not support the self test function, this value is always 00h.	R

31.3.3.5 Offset 10h Register (OHCI Base Address)

Address(es) A005 0010h



Bit	Symbol	Bit Name	Description	R/W
b0	Memory Space Indicator	Memory space indicator	This bit is fixed to 0, which indicates that the OHCI operational registers are mapped to the system memory space.	R
b2, b1	Type[1:0]	Base address type	These bits are fixed to 00b, which indicates that the base address of the OHCI operational registers has a 32-bit width and can be allocated to any location in a 32-bit memory space.	R
b3	Prefetchable	Prefetch setting	As the host logic does not support prefetching in memory read cycles, this bit is fixed to 0.	R
b11 to b4	OHCI Base Address [27:0]	OHCI base address	Bits [31:12] specify the base address of the operational registers. Specify the base address of the operational registers determined by the system during initialization. Bits [11:4] are fixed to 00h, which indicates that the operational registers are allocated to a 4-Kbyte address space.	R
b31 to b12				R/W

31.3.3.6 Offset 2Ch Register (Subsystem Vendor ID, Subsystem ID)

Address(es) A005 002Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Subsystem ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Subsystem Vendor ID[15:0]															
Value after reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	Subsystem Vendor ID [15:0]	Subsystem vendor ID	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R
b31 to b16	Subsystem ID[15:0]	Subsystem ID	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R

31.3.3.7 Offset 30h Register (Expansion ROM Base Address)

Address(es) A005 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Expansion ROM Base Address[21:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Expansion ROM Base Address[21:0]						—	—	—	—	—	—	—	—	—	ROM Decode Enable
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ROM Decode Enable	Expansion ROM decode enable	As decoding of expansion ROM is prohibited, this bit is always read as 0. This bit cannot be written to.	R
b9 to b1	—	Reserved	Don't care	R
b31 to b10	Expansion ROM Base Address[21:0]	Expansion ROM base address	As decoding of expansion ROM is prohibited, these bits are always read as 000000h. These bits cannot be written to.	R

31.3.3.8 Offset 34h Register (Capability Pointer)

Address(es) A005 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	Capability Pointer[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Capability Pointer[7:0]	Capability identifier pointer	These bits hold the pointer to the capability identifier. As the pointer is set to 40h in the host logic, this value is set to 40h.	R
b31 to b8	—	Reserved	Don't care	R

31.3.3.9 Offset 3Ch Register (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Address(es) A005 003Ch

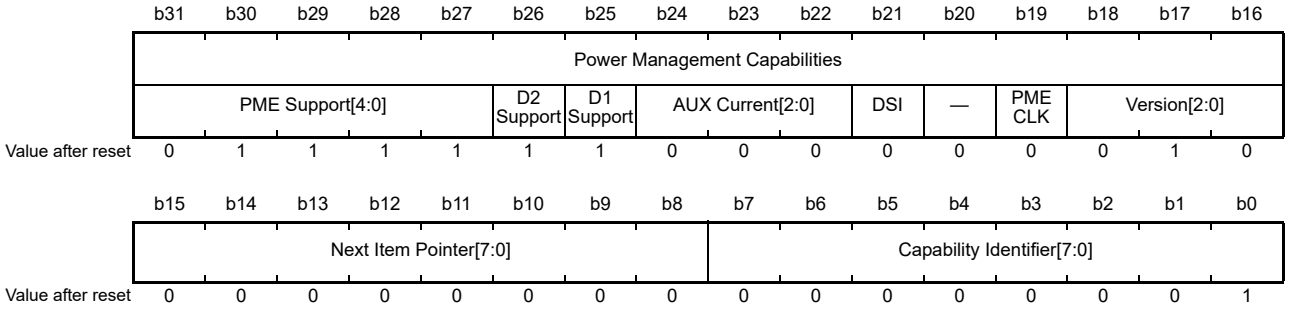
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Max Latency[7:0]								Min Gnt[7:0]							
Value after reset	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Interrupt Pin[7:0]								Interrupt Line[7:0]							
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Interrupt Line [7:0]	Interrupt line	These bits indicate the interrupt line. In the USB host controller, do not change this from the value after reset (00h).	R/W
b15 to b8	Interrupt Pin [7:0]	Interrupt output pin	These bits indicate the pin for outputting interrupts. As INTA is used, this value is fixed to 01h.	R
b23 to b16	Min Gnt[7:0]	Minimum burst transfer time	These bits indicate the minimum burst transfer time. As the minimum time is set to 01h in the host logic, this value is set to 01	R
b31 to b24	Max Latency[7:0]	Maximum frequency of PCI bus acquisition	These bits indicate the maximum frequency of PCI bus acquisition. As the maximum frequency is set to 2Ah in the host logic, this value is set to 2Ah.	R

31.3.3.10 Offset 40h Register (Capability Identifier, Next Item Pointer, Power Management Capabilities)

Address(es) A005 0040h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Capability Identifier [7:0]	PCI power management register ID	These bits indicate the PCI power management register ID. The value is fixed to 01h.	R
b15 to b8	Next Item Pointer[7:0]	Next item non-existence	These bits are fixed to 00h, which indicates that the next item does not exist.	R
b18 to b16	Version[2:0]	Version	These bits are fixed to 010b, which indicates that the host logic conforms to the PCI Power Management Interface Specification Release 1.1.	R
b19	PME CLK	USBPCLK unnecessary	This bit is fixed to 0, which indicates that USBPCLK is not required for PME interrupt generation.	R
b20	—	Reserved	Don't care	R
b21	DSI	Power management initialization unnecessary	This bit is fixed to 0, which indicates that special initialization is not required for power management.	R
b24 to b22	Aux Current[2:0]	Current setting value	These bits indicate the necessary current for 3.3-V auxiliary power supply. As PME interrupt generation from the D3 cold state is not supported, this value is fixed to 000b.	R
b25	D1 Support	PCI power state D1 support	This bit is fixed to 1, which indicates that PCI power state D1 is supported.	R
b26	D2 Support	PCI power state D2 support	This bit is fixed to 1, which indicates that PCI power state D2 is supported.	R
b30 to b27	PME Support[4:0]	PME interrupt support	These bits are fixed to 1111b, which indicates that PME interrupt generation is supported in all PCI power states (D0 to D3).	R
b31		D3 cold state support	This bit indicates whether the D3 cold state is supported. As the D3 cold state is not supported, this value is fixed to 0.	R

31.3.3.11 Offset 44h Register (Power Management Control/Status, PMCSR Bridge Support Extensions)

Address(es) A005 0044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Data								PMCSR Bridge Support Extensions							
	Data[7:0]								BPCC Enable	B2_B3	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Power Management Control/Status															
	PME Status	Data Scale[1:0]		Data Select[3:0]				PME Enable	—	—	—	—	—	—	Power State[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	Power State[1:0]	PCI power status	These bits indicate the power state of the PCI as follows. b1 b0 0 0: D0 State 0 1: D1 State 1 0: D2 State 1 1: D3 hot State	R/W
b7 to b2	—	Reserved	When writing, write 0.	R/W
b8	PME Enable	PME enable	This bit specifies whether to use PME. Setting this bit to 1 generates a PME interrupt when operation returns from the power management state.	R/W
b12 to b9	Data Select[3:0]	Data selection field	The value of these bits is 0h. This is an optional field in the PCI standard, and the host logic does not support it.	R
b14, b13	Data Scale[1:0]	Data scale field	The value of these bits is 00b. This is an optional field in the PCI standard, and the host logic does not support it.	R
b15	PME Status	PME interrupt status	This bit indicates the PME interrupt state. It is set to 1 when the following condition for PME generation is satisfied. [PME generation condition] Bit 3 (RD) in the HcInterruptStatus register is set to 1 while bit 10 (RWE) in the HcControl register is 1. Writing 1 from the PCI bus clears this bit to 0.	R/W
b21 to b16	—	Reserved	When writing, write 0.	R/W
b22	B2_B3	Bit for bridge	The value of this bit is 0. This is a bit for the bridge, and the host logic does not support it.	R
b23	BPCC Enable	BPCC enable	The value of this bit is 0. This is a bit for the bridge, and the host logic does not support it.	R
b31 to b24	Data[7:0]	Data field	The value of these bits is 00h. This is an optional field in the PCI standard, and the host logic does not support it.	R

31.3.3.12 Offset E0h Register (EXT1)

This register is the same as the EXT1 register located in the EHCI configuration space.
Therefore, this register can be accessed also by using the offset address on the EHCI configuration register side.

Address(es) A005 00E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	potpgt								Hyper Speed transfer Control #2					—	—	—
Value after reset	0	0	0	0	1	1	1	1	0	0	0	1	0	1	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	Hyper Speed transfer Control #1	PSD	—	—	—	—	ID_Write _Enable	—	—	—	—	—	Port_no	
Value after reset	0	0	1	1	0	0	1	1	0	0	0	1	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	Port_no	USB downstream port number	These bits specify the number of valid USB downstream ports. **Setting Value** / **Valid Ports** 01b / Port1 10b / Port1 and Port2 Other than the above / Reserved In the USB host controller, do not change this from the value after reset (1h).	R/W
b6 to b2	—	Reserved	Do not change this from the value after reset.	R/W
b7	ID_Write _Enable	Write-protect control	This bit write-protects the Subsystem ID, Subsystem Vendor ID, Max Latency, and Min Gnt bits. 0: Write-protected 1: Can be written to.	R/W
b11 to b8	—	Reserved	Do not change this from the value after reset.	R/W
b12	PSD	Periodic schedule disable	0: For transferring data via USB while the USBCMD.Periodic Schedule Enable bit is being 0, always set this bit to 0. 1: No settings required (initial value) Setting this bit is arbitrary when the USBCMD.Periodic Schedule Enable bit is 1.	R/W
b13	Hyper Speed transfer Control #1 (HS Async OUT advance Mode)	Hyper-speed transfer mode setting	This bit specifies the hyper-speed transfer mode for asynchronous OUT transfer. Setting to 1 enables this function (transfer rate improvement).	R/W
b18 to b14	—	Reserved	Do not change this from the value after reset.	R/W
b23 to b19	Hyper Speed transfer Control #2	HS asynchronous FIFO threshold setting field	Do not specify any value other than 02h (HS asynchronous FIFO threshold = 64 bytes).	R/W
b31 to b24	Potpgt	POTPGT setting field	These bits specify the value for bits [31:24] (PPOTPGT) in the OHCI HcRhDescriptorA register. POTPGT is the time that software should wait before accessing a root hub port after power supply to the port is started.	R/W

31.3.3.13 Offset E4h Register (EXT2)

This register is the same as the EXT2 register located in the EHCI configuration space.
Therefore, this register can be accessed also by using the offset address on the EHCI configuration register side.
However, note that bit 0 (EHCI_mask) can be written to only on the OHCI side.

Address(es) A005 00E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RAM Connect Check Result	RAM Connect Check END Flag	RUN RAM Connect Check
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	Hyper Speed transfer Control #3	EHCI_mask
Value after reset	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	EHCI_mask	EHCI host logic mask	This bit enables or disables the EHCI host logic. 0: EHCI host logic is enabled. 1: EHCI host logic is disabled. When this bit is set to 1, register access in the EHCI PCI configuration space and memory space is disabled and the EHCI host logic does not operate.	R/W
b1	Hyper Speed transfer Control #3	Hyper-speed transfer mode setting	This bit specifies the hyper-speed transfer mode for asynchronous IN/OUT transfer. Setting to 1 enables this function (transfer rate improvement).	R/W
b15 to b2	—	Reserved	Do not change this from the value after reset.	R/W
b16	RUN RAM Connect Check	RAM connection check circuit activation	This bit activates the RAM connection check circuit. Set this bit to 1 to start the RAM connection check. This bit is not cleared even after the check is completed. To check again, write 0 to this bit to clear it, and then write 1 again to start the check. When this bit changes from 0 to 1, the connection check circuit is reset and the RAM Connect Check END Flag bit and RAM Connect Check Result bit are cleared.	R/W
b17	RAM Connect Check END Flag	RAM connection check end flag	This bit indicates the end of RAM connection check. 0: Connection check has not been done or ended. 1: Connection check has ended. This bit is set when a specified time (about 2 µs) has passed after the RAM connection check is started by modifying the RUN RAM check bit from 0 to 1.	R
b18	RAM Connect Check Result	RAM connection check result	This bit indicates the result of RAM connection check. 0: Connection check result is NG. 1: Connection check result is OK. This value is valid when the RAM Connect Check END Flag bit is 1. Once the connection check is done, this value is not cleared until the RUN RAM Connect Check bit changes from 0 to 1.	R
b31 to b19	—	Reserved	Do not change this from the value after reset.	R/W

31.3.4 PCI Configuration Registers for EHCI

31.3.4.1 Offset 00h Register (Vendor ID, Device ID)

Address(es) A005 0100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Device ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Vendor ID[15:0]															
Value after reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	Vendor ID [15:0]	Vendor ID	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R
b31 to b16	Device ID [15:0]	Device ID	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R

31.3.4.2 Offset 04h Register (Command, Status)

Address(es) A005 0104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Detected Parity Error	Signaled System Error	Received Master Abort	Received Target Abort	Signaled Target Abort	Devsel Timing[1:0]		Data Parity Error Detected	Fast Back to Back Capable	—	Capable 66MHz	Capabilities List	—	—	—	—
Value after reset	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0

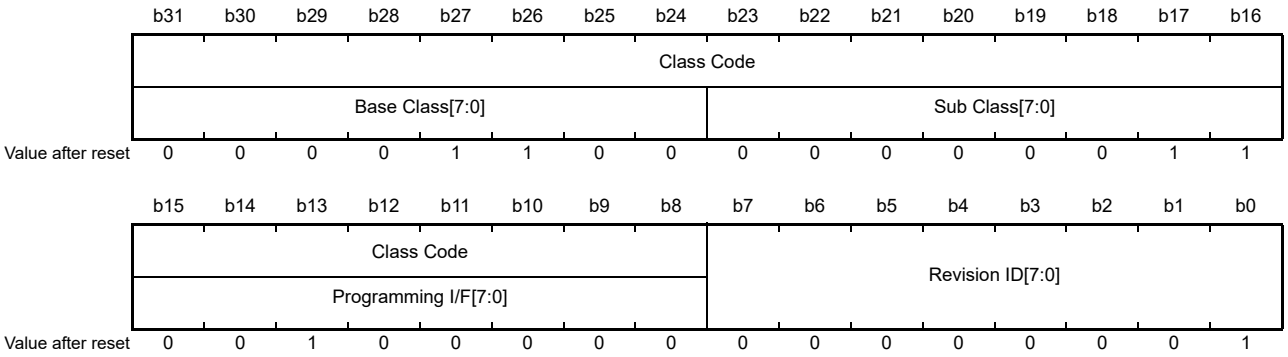
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	Fast Back to Back Enable	SERR Enable	Wait Cycle Control	Parity Error Response	VGA Palette Snoop	Memory Write and Invalidate Enable	Special Cycle	Bus Master	Memory Space	I/O Space
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	I/O Space	I/O space access enable	This bit enables access to the I/O space. As the host logic does not accept I/O access, this value is always 0.	R
b1	Memory Space	Memory space access enable	This bit enables access to the memory space. This is an enable signal for memory access specified in the PCI standard. Set to 1 when accessing registers. Set this bit to 1 during initial setting of the host logic.	R/W
b2	Bus Master	Bus master enable	This bit enables bus master operation. This is an enable signal for master access to the PCI bus. Set to 1 when accessing the SRAM on the system bus. Set this bit to 1 during initial setting of the host logic.	R/W
b3	Special Cycle	Special cycle enable	This bit enables special cycle operation. As the host logic does not support the special cycle operation, this value is always 0.	R
b4	Memory Write and Invalidate Enable	Memory write and invalidate enable	This bit enables the Memory Write and Invalidate command. In the USB host controller, do not change this from the value after reset (0). 0: Memory write and invalidate command is disabled. 1: Memory write and invalidate command is enabled.	R/W
b5	VGA Palette Snoop	VGA palette snoop enable	This bit enables VGA palette snooping. As the host logic does not support VGA palette snooping, this value is always 0.	R
b6	Parity Error Response	Parity error response enable	This bit enables parity error response. 0: PERR0 is not asserted. 1: PERR0 is asserted. When a parity error is detected, the Detected Parity Error bit is set to 1 even if this bit is cleared to 0.	R/W
b7	Wait Cycle Control	Wait cycle control enable	This bit enables wait cycle control. As the host logic does not support address and data stepping, this value is always 0.	R
b8	SERR Enable	System error response enable	This bit enables system error response. 0: SERR0 is not asserted. 1: SERR0 is asserted. To notify of a system error through the SERR signal, set this bit to 1.	R/W
b9	Fast Back to Back Enable	Fast back to back enable	This bit enables fast back to back transactions. As the host logic does not support fast back to back transactions, this value is always 0.	R
b19 to b10	—	Reserved	When writing, write 0.	R/W
b20	Capabilities List	Power management mode support	This value is fixed to 1, which indicates that the power management mode is supported.	R

Bit	Symbol	Bit Name	Description	R/W
b21	Capable 66MHz	66-MHz operation capable	This bit indicates whether 66-MHz operation is available. As the host logic operates only at 33 MHz, this value is fixed to 0.	R
b22	—	Reserved	When writing, write 0.	R/W
b23	Fast Back to Back Capable	Fast back to back capable	This bit indicates whether fast back to back transactions are supported. As the host logic does not support fast back to back transactions, this value is fixed to 0.	R
b24	Data Parity Error Detected	Parity error detection	This bit is set when a parity error is detected in master operation. Writing 1 from the PCI bus clears this bit. The value is fixed to 0 when the Parity Error Response bit is set as disabled.	R/W
b26, b25	Devsel Timing[1:0]	DEVSEL response speed bit field	These bits indicate the DEVSEL response speed. The value is fixed to 01b (medium-speed response).	R
b27	Signaled Target Abort	Slave/Target abort status	This is a status bit for Slave/Target abort. This bit is set to 1 in slave operation when the host logic has terminated the bus cycle in which the host logic is accessed through Target Abort. Writing 1 from the PCI bus clears this bit.	R/W
b28	Received Target Abort	Master/Target abort status	This is a status bit for Master/Target abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Target Abort. Writing 1 from the PCI bus clears this bit.	R/W
b29	Received Master Abort	Master/Master abort status	This is a status bit for Master/Master abort. This bit is set to 1 in master operation when the bus cycle being executed by the host logic is terminated through Master Abort. Writing 1 from the PCI bus clears this bit.	R/W
b30	Signaled System Error	SERR status	This is a status bit for SERR. This bit is set when a system error occurs. Writing 1 from the PCI bus clears this bit.	R/W
b31	Detected Parity Error	Parity error status	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 from the PCI bus clears this bit.	R/W

31.3.4.3 Offset 08h Register (Revision ID, Class Code)

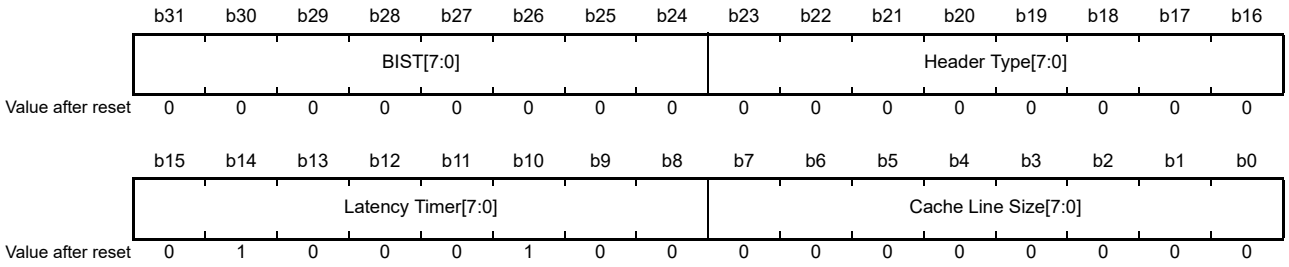
Address(es) A005 0108h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Revision ID [7:0]	Host logic revision	These bits indicate the revision of the host logic. The value is fixed to 01h.	R
b15 to b8	Programming I/F[7:0]	PCI standard program interface bit field	These bits indicate the program interface specified in the PCI standard. The value is 20h, which indicates EHCI.	R
b23 to b16	Sub Class [7:0]	PCI standard subclass	These bits indicate the subclass specified in the PCI standard. The value is 03h, which indicates a USB device.	R
b31 to b24	Base Class [7:0]	PCI standard base class	These bits indicate the base class specified in the PCI standard. The value is 0Ch, which indicates a serial peripheral bus controller.	R

31.3.4.4 Offset 0Ch Register (Cache Line Size, Latency Timer, Header Type, BIST)

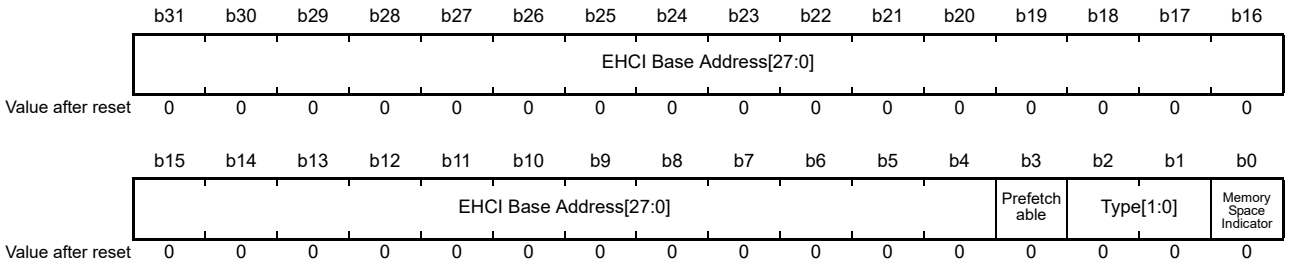
Address(es) A005 010Ch



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Cache Line Size[7:0]	Cache line size	These bits notify the system of the cache line size.	R/W
b9, b8	Latency Timer[7:0]	Latency timer	These bits notify the system of the latency timer. The lowest 2 bits are fixed to 00b.	R
b15 to b10				R/W
b23 to b16	Header Type [7:0]	Header type	These bits notify the system of the header type. As the header type is Type 0, bits [22:16] are fixed to 00h. As the multifunction capability is not supported, bit 23 is fixed to 0.	R
b31 to b24	BIST[7:0]	Self testing field	These bits are used for self testing. As the host logic does not support the self test function, this value is always 00h.	R

31.3.4.5 Offset 10h Register (EHCI Base Address)

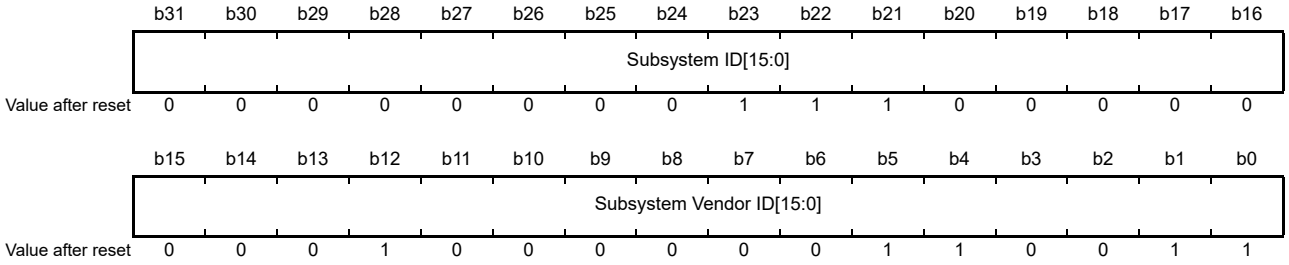
Address(es) A005 0110h



Bit	Symbol	Bit Name	Description	R/W
b0	Memory Space Indicator	System memory space indicator	This bit is fixed to 0, which indicates that the EHCI operational registers are mapped to the system memory space.	R
b2, b1	Type[1:0]	Base address allocation type	These bits are fixed to 00b, which indicates that the base address of the EHCI operational registers has a 32-bit width and can be allocated to any location in a 32-bit memory space.	R
b3	Prefetchable	Prefetch support	As the host logic does not support prefetching in memory read cycles, this bit is fixed to 0.	R
b7 to b4	EHCI Base Address [27:0]	EHCI base address	Bits [31:8] specify the base address of the operational registers. Specify the base address of the operational registers determined by the system during initialization. Bits [7:4] are fixed to 0h, which indicates that the operational registers are allocated to a 256-byte address space.	R
b31 to b8				R/W

31.3.4.6 Offset 2Ch Register (Subsystem Vendor ID, Subsystem ID)

Address(es) A005 012Ch



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	Subsystem Vendor ID [15:0]	Subsystem vendor ID	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R
b31 to b16	Subsystem ID [15:0]	Subsystem ID	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R

31.3.4.7 Offset 30h Register (Expansion ROM Base Address)

Address(es) A005 0130h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Expansion ROM Base Address[21:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Expansion ROM Base Address[21:0]						—	—	—	—	—	—	—	—	—	ROM Decode Enable
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ROM Decode Enable	ROM decode enable	As decoding of expansion ROM is prohibited, this bit is always read as 0. This bit cannot be written to.	R
b9 to b1	—	Reserved	Don't care	R
b31 to b10	Expansion ROM Base Address[21:0]	Expansion ROM base address	As decoding of expansion ROM is prohibited, these bits are always read as 000000h. These bits cannot be written to.	R

31.3.4.8 Offset 34h Register (Capability Pointer)

Address(es) A005 0134h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	Capability Pointer[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Capability Pointer[7:0]	Capability identifier pointer	These bits hold the pointer to the capability identifier. As the pointer is set to 40h in the host logic, this value is set to 40h.	R
b31 to b8	—	Reserved	Don't care	R

31.3.4.9 Offset 3Ch Register (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Address(es) A005 013Ch

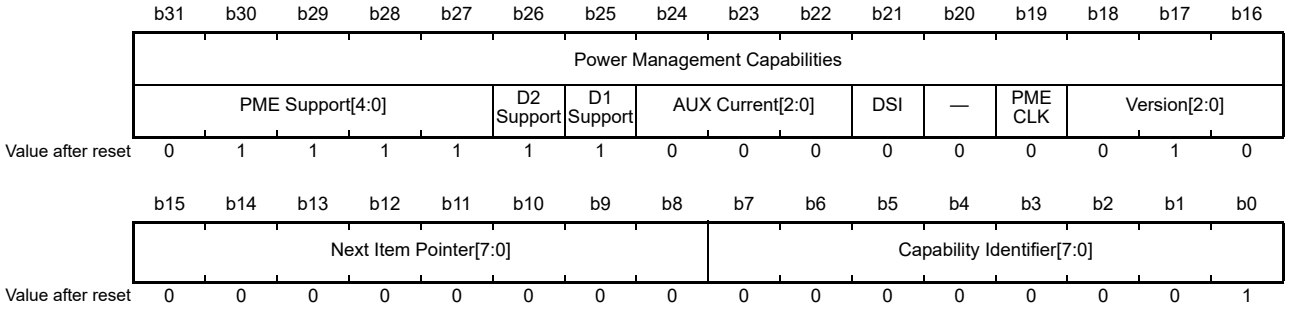
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Max Latency[7:0]								Min Gnt[7:0]							
Value after reset	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Interrupt Pin[7:0]								Interrupt Line[7:0]							
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Interrupt Line [7:0]	Interrupt line	These bits indicate the interrupt line. In the USB host controller, do not change this from the value after reset (00h).	R/W
b15 to b8	Interrupt Pin [7:0]	Interrupt output pin	These bits indicate the pin for outputting interrupts. As INTB is used, this value is fixed to 02h.	R
b23 to b16	Min Gnt[7:0]	Minimum burst transfer time	These bits indicate the minimum burst transfer time. As the minimum time is set to 10h in the host logic, this value is 10h.	R
b31 to b24	Max Latency [7:0]	PCI bus maximum acquisition frequency	These bits indicate the maximum frequency of PCI bus acquisition. As the maximum frequency is set to 22h in the host logic, this value is set to 22h.	R

31.3.4.10 Offset 40h Register (Capability Identifier, Next Item Pointer, Power Management Capabilities)

Address(es) A005 0140h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	Capability Identifier [7:0]	Power management register ID	These bits indicate the power management register ID. The value is fixed to 01h.	R
b15 to b8	Next Item Pointer[7:0]	Next item pointer	These bits are fixed to 00h, which indicates that the next item does not exist.	R
b18 to b16	Version[2:0]	PCI version	These bits are fixed to 010b, which indicates that the host logic conforms to the PCI Power Management Interface Specification Release 1.1.	R
b19	PME CLK	USBPCLKPCLK necessity	This bit is fixed to 0, which indicates that USBPCLKPCLK is not necessary for PME interrupt generation.	R
b20	—	Reserved	—	R
b21	DSI	Special initialization necessity	This bit is fixed to 0, which indicates that special initialization is not necessary for power management.	R
b24 to b22	Aux Current [2:0]	Current setting value	These bits indicate the required current for 3.3-V auxiliary power supply. As PME interrupt generation from the D3 cold state is not supported, this value is fixed to 000b.	R
b25	D1 Support	PCI power state D1 support	This bit is fixed to 1, which indicates that PCI power state D1 is supported.	R
b26	D2 Support	PCI power state D2 support	This bit is fixed to 1, which indicates that PCI power state D2 is supported.	R
b30 to b27	PME Support [4:0]	PME interrupt support bit field	These bits are fixed to 1111b, which indicates that PME interrupt generation is supported in all PCI power states (D0 to D3).	R
b31		D3 cold state support	This bit indicates whether the D3 cold state is supported. As the D3 cold state is not supported, this value is fixed to 0.	R

31.3.4.11 Offset 44h Register (Power Management Control/Status, PMCSR Bridge Support Extensions)

Address(es) A005 0144h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Data								PMCSR Bridge Support Extensions							
	Data[7:0]								BPCC Enable	B2_B3	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Power Management Control/Status															
	PME Status	Data Scale[1:0]		Data Select[3:0]				PME Enable	—	—	—	—	—	—	Power State[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	Power State [1:0]	PCI power status	These bits indicate the power state of the PCI as follows. b1 b0 0 0: D0 State 0 1: D1 State 1 0: D2 State 1 1: D3 hot State	R/W
b7 to b2	—	Reserved	When writing, write 0.	R/W
b8	PME Enable	PME enable	This bit specifies whether to use external pin PME. Setting this bit to 1 generates a PME interrupt when operation returns from the power management state.	R/W
b12 to b9	Data Select [3:0]	Data selection field	The value of these bits is 0h. This is an optional field in the PCI standard, and the host logic does not support it.	R
b14, b13	Data Scale [1:0]	Data scale field	The value of these bits is 00b. This is an optional field in the PCI standard, and the host logic does not support it.	R
b15	PME Status	PME interrupt status	This bit indicates the PME interrupt state. It is set to 1 when the PME generation condition is satisfied. Writing 1 from the PCI bus clears this bit to 0.	R/W
b21 to b16	—	Reserved	When writing, write 0.	R/W
b22	B2_B3	Bridge	The value of this bit is 0. This is a bit for the bridge and the host logic does not support it.	R
b23	BPCC Enable	BPCC enable	The value of this bit is 0. This is a bit for the bridge and the host logic does not support it.	R
b31 to b24	Data[7:0]	PCI standard option field	The value of these bits is 00h. This is an optional field in the PCI standard, and the host logic does not support it.	R

31.3.4.12 Offset 60h Register (SBRN, FLADJ, PORTWAKECAP)

Address(es) A005 0160h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORTWAKECAP[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FLADJ[7:0]								SBRN[7:0]							
Value after reset	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SBRN[7:0]	Serial bus release number	These bits indicate the serial bus release number. The value is fixed to 20h.	R
b13 to b8	FLADJ[7:0]	1 micro frame length	These bits adjust the length of a micro-frame in 16-HS bit time units. The value after reset is 20h (60000d HS bit time).	R/W
b15, b14				R
b31 to b16	PORTWAKECAP[15:0]	Wakeup event mask field	From among the connected devices, these bits specify a mask for which port to be used in response to a wakeup event. This setting does not affect the actual operation of the host logic. The USB host controller only has one port so this register never needs be used.	R/W

31.3.4.13 Offset E0h Register (EXT1)

This register is the same as the EXT1 register located in the OHCI configuration space. See the description of the OHCI configuration register.

31.3.4.14 Offset E4h Register (EXT2)

This register is the same as the EXT2 register located in the OHCI configuration space. See the description of the OHCI configuration register.

Note that bit 0 (EHCI_mask) cannot be accessed from the EHCI side.

31.3.5 PCI Configuration Register for AHB-PCI Bridge

31.3.5.1 Offset 00h Register (Vendor ID, Device ID)

Address(es) A005 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DEVICE_ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VENDOR_ID[15:0]															
Value after reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	VENDOR_ID [15:0]	Vendor ID	This register indicates the vendor of the device. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host. It is always read as 1033h.	R
b31 to b16	DEVICE_ID [15:0]	Device ID	This register indicates the device type. This is used to select a driver that operates the device as specified in the PCI standard. This register does not need to be used in the embedded host.	R

31.3.5.2 Offset 04h Register (Command, Status)

Address(es) A005 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DETPERR	SIGSERR	REMABORT	RETABORT	SIGTABORT	DEVTIM[1:0]		MDPERR	FBTBCAP	—	CAP66M	CAPLIST	—	—	—	—
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

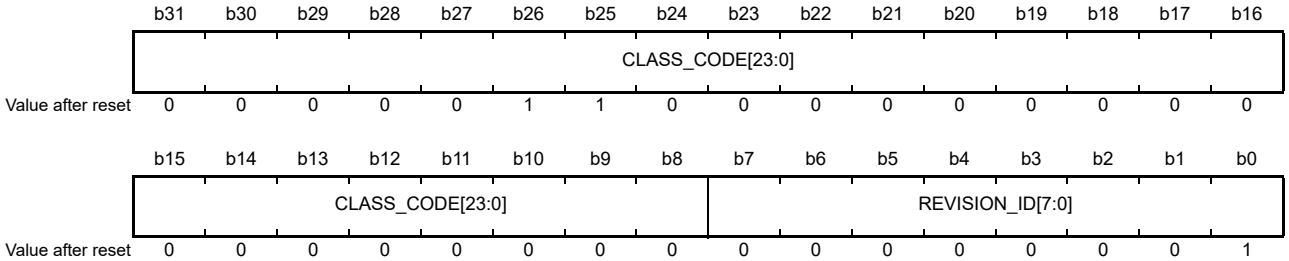
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	FBTBEN	SERREN	STEPCTR	PERREN	VGAPSNP	MWINVEN	SPECIALC	MASTEREN	MEMEN	IOEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IOEN	I/O space access enable	This bit enables access to the I/O space. The value is fixed to 0.	R
b1	MEMEN	PCI slave operation setting	This bit specifies the PCI slave operation. In the USB host controller, set this bit to 1 during the initial settings. 0: Memory cycles cannot be accepted (value after reset) 1: Memory cycles can be accepted.	R/W
b2	MASTEREN	PCI master operation setting	This bit specifies the PCI master operation. In the USB host controller, set this bit to 1 during the initial settings. 0: Master operation is disabled (value after reset). 1: Master operation is enabled.	R/W
b3	SPECIALC	Special cycle enable	This bit enables the special cycle operation. The value is fixed to 0.	R
b4	MWINVEN	Memory write and invalidate enable	This bit enables the Memory Write and Invalidate command. The value is fixed to 0.	R
b5	VGAPSNP	VGA palette snoop enable	This bit enables VGA palette snooping. The value is fixed to 0.	R
b6	PERREN	Parity error detection operation setting	This bit specifies the operation when a parity error is detected. In the USB host controller, set this bit to 1 during the initial settings. 0: Nothing is to be done. (value after reset) 1: PERR# is asserted.	R/W
b7	STEPCTR	Address stepping control	This bit controls address stepping. The value is fixed to 0. (Address stepping is not done.)	R
b8	SERREN	System error detection operation setting	This bit specifies the operation when a system error is detected. In the USB host controller, set this bit to 1 during the initial settings. 0: Nothing is to be done. (value after reset) 1: SERR# is asserted.	R/W
b9	FBTBEN	Fast back to back enable	This bit enables fast back to back transactions. The value is fixed to 0.	R
b19 to b10	—	Reserved	When writing, write 0.	R/W
b20	CAPLIST	Capabilities list support	This bit indicates whether the capabilities list is supported. The value is fixed to 0. (The capabilities list is not supported.)	R
b21	CAP66M	66-MHz operation support	This bit indicates whether 66-MHz operation is supported. The value is fixed to 0. (66-MHz operation is not supported.)	R
b22	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b23	FBTBCAP	Fast back to back capability	This bit indicates whether fast back to back transactions are supported. The value is fixed to 0. (Fast back to back transactions are not supported.)	R
b24	MDPERR	Parity error detection flag	This bit is set when a parity error is detected in master operation. Writing 1 clears this bit. 0: Parity error has not been detected. 1: Parity error has been detected.	R/W
b26, b25	DEVTIM[1:0]	DEVSEL response speed	These bits indicate the DEVSEL response speed. The value is fixed to 01b (Medium Mode).	R
b27	SIGTABORT	Slave Target Abort status	This is a status bit for Slave Target Abort. This bit is set when Target Abort is transmitted. Writing 1 clears this bit. 0: Target Abort has not been transmitted. 1: Target Abort has been transmitted.	R/W
b28	RETABORT	Master Target Abort status	This is a status bit for Master Target Abort. This bit is set when Target Abort is received. Writing 1 clears this bit. 0: Target Abort has not been received. 1: Target Abort has been received.	R/W
b29	REMABORT	Master Abort status	This is a status bit for Master Abort. This bit is set when Master Abort is received. Writing 1 clears this bit. 0: Master Abort has not been received. 1: Master Abort has been received.	R/W
b30	SIGSERR	SERR status	This is a status bit for SERR. This bit is set when a system error occurs. Writing 1 clears this bit. 0: SERR# has not been asserted. 1: SERR# has been asserted.	R/W
b31	DETPERR	Parity error status	This is a status bit for parity error. This bit is set when an address or data parity error is detected. Writing 1 clears this bit. 0: Parity error has not been detected. 1: Parity error has been detected.	R/W

31.3.5.3 Offset 08h Register (Revision ID, Class Code)

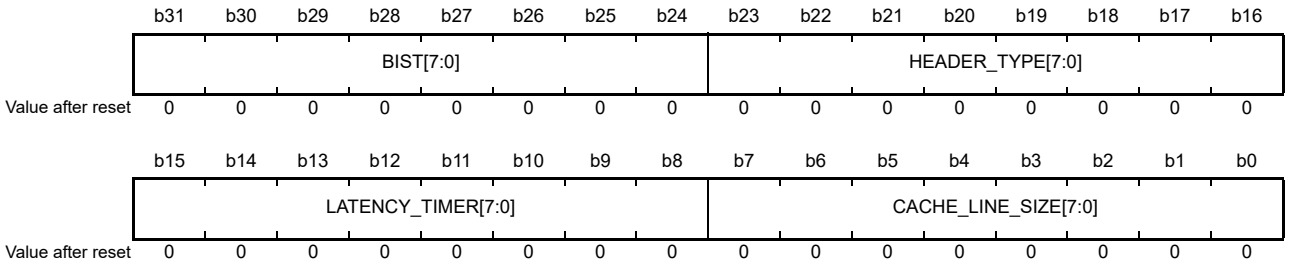
Address(es) A005 0008h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	REVISION_ID[7:0]	Revision ID	The value of these bits is 01h.	R
b31 to b8	CLASS_CODE[23:0]	CLASS CODE	The value of these bits is 060000h.	R

31.3.5.4 Offset 0Ch Register (Cache Line Size, Latency Timer, Header Type, BIST)

Address(es) A005 000Ch



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CACHE_LINE_SIZE[7:0]	CACHE LINE SIZE	The value of these bits is 00h (cache is not supported).	R
b15 to b8	LATENCY_TIMER[7:0]	Latency timer	These bits notify the system of the latency timer. The USB host controller does not use the latency timer; do not change this from the value after reset (00h).	R/W
b23 to b16	HEADER_TYPE[7:0]	HEADER TYPE	The value of these bits is 00h (single function device).	R
b31 to b24	BIST[7:0]	BIST	The value of these bits is 00h (BIST is not implemented).	R

31.3.5.5 Offset 10h Register (AHB-PCI Bridge Base Address)

Address(es) A005 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PCICOM_BASEADR[21:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PCICOM_BASEADR[21:0]						—	—	—	—	—	—	PREFETCH	TYPE[1:0]		MEM
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MEM	Base address specifying memory space	This bit indicates that the bits specified by the base address are in the memory space. The value is fixed to 0.	R
b2, b1	TYPE[1:0]	Base address type	These bits indicate the base address type. The value is 00b. (The base address can be allocated to any location in a 4-Gbyte space.)	R
b3	PREFETCH	Data prefetch capability	This bit indicates whether data can be prefetched. The value is fixed to 0. (Data cannot be prefetched.)	R
b9 to b4	—	Reserved	When writing, write 0.	R/W
b31 to b10	PCICOM_BASEADR[21:0]	AHB-PCI bridge PCI communication register area base address	These bits specify the base address of the AHB-PCI bridge PCI communication register area. A 1-Kbyte area is necessary and the 24 high-order bits specify the base address.	R/W

31.3.5.6 Offset 14h Register (PCI-AHB WIN1 Base Address)

Address(es) A005 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PCI_WIN1_BASEADR [3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PREFETCH	TYPE[1:0]		MEM
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MEM	Base address specifying memory space	This bit indicates that the field specified by the base address is in the memory space. The value is fixed to 0.	R
b2, b1	TYPE[1:0]	Base address type	These bits indicate the base address type. The value is 00b. (The base address can be allocated to any location in a 4-Gbyte space.)	R
b3	PREFETCH	Data prefetch capability	This bit indicates whether data can be prefetched. The value is fixed to 1. (Data can be prefetched.)	R
b27 to b4	—	Reserved	When writing, write 0.	R/W
b31 to b28	PCI_WIN1_ BASEADR[3:0]	PCI-AHB Window1 base address	These bits specify the base address of PCI-AHB Window 1. For the PCI-AHB Window 1 space, a 1-Gbyte area can be accessed through the setting of bits [11:10] (PCI_AHB_WIN1_SIZE) in the USBCTR register. **PCI-AHB Window 1 Space** / **AHB_BASEADR[31:28]** 1 Gbyte: The 2 higher-order bits [31:30] are the base address. Other bits are masked by 0. For details of register setting, see section 31.4.1, Register Access.	R/W

31.3.5.7 Offset 2Ch Register (Subsystem Vendor ID, Subsystem ID)

Address(es) A005 002Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SUBSYS_ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SUBSYS_VENDOR_ID[15:0]															
Value after reset	0	0	0	1	0	0	0	0	0	0	1	1	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	SUBSYS_ VENDOR_ID [15:0]	Subsystem vendor ID	The value of these bits is 1033h.	R
b31 to b16	SUBSYS_ID [15:0]	Subsystem ID	The value of these bits is 0000h.	R

31.3.5.8 Offset 3Ch Register (Interrupt Line, Interrupt Pin, Min gnt, Max Latency)

Address(es) A005 003Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MAX_LAT[7:0]								MIN_GNT[7:0]							
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	INT_PIN[7:0]								INT_LINE[7:0]							
Value after reset	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	INT_LINE[7:0]	Interrupt line	These bits specify the interrupt line. In the USB host controller, do not change this from the value after reset (00h).	R
b15 to b8	INT_PIN[7:0]	Interrupt pin field	The value of these bits is 01h. (INTA# is used).	R
b23 to b16	MIN_GNT[7:0]	Latency timer request field	The value of these bits is 02h. (Requested latency timer: 16 burst).	R
b31 to b24	MAX_LAT[7:0]	Bus use frequency request field	The value of these bits is 00h. (No value is specified for the bus use frequency.)	R

31.3.6 AHB-PCI Bridge PCI Communication Registers

31.3.6.1 PCIAHB_WIN1_CTR Register

This register is used to make settings for access from the host logic to AHB.

Address(es) A005 0800h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	AHB_BASEADR[3:0]				—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PREFETCH[1:0]	
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	PREFETCH [1:0]	AHB bus prefetch setting bit field	These bits specify whether to prefetch data in the AHB bus when the host logic issues a read request. In the USB host controller, set these bits to 11b during the initial settings and do not change the value. b1 b0 0 0: Prefetch is disabled. 0 1: Prefetch is enabled (up to 4 bursts). 1 0: Prefetch is enabled (up to 8 bursts). 1 1: Prefetch is enabled (up to 16 bursts).	R/W
b27 to b2	—	Reserved	When writing, write 0.	R/W
b31 to b28	AHB_BASEADR [3:0]	AHB bus base address	These bits specify the base address of the AHB bus for access from the host logic to PCI-AHB Window 1. For the PCI-AHB Window 1 space, a 1-Gbyte area can be made accessible through the setting of bits [11:10] (PCI_AHB_WIN1_SIZE) in the USBCTR register. Do not modify this value from the value after reset (0000b). **PCI-AHB Window 1 Space** / **AHB_BASEADR[31:28]** 1 Gbyte: The 2 high-order bits (bits [31:30]) specify the base address. For details of register setting, see section 31.4.1, Register Access.	R/W

31.3.6.2 AHBPCI_WIN1_CTR Register

This register is used to make necessary settings for access to the PCI configuration space.

Address(es) A005 0810h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PCIWIN1_BASEADR[20:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PCIWIN1_BASEADR[20:0]					—	—	—	—	—	—	—	PCICMD[2:0]			—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	When writing, write 0.	R/W
b3 to b1	PCICMD[2:0]	PCI bus cycle type	These bits specify the type of PCI bus cycle. In the USB host controller, set these bits to 101b during the initial settings and do not change the value. b3 b1 000: Interrupt Acknowledge / Special Cycle 001: IO Read / IO Write 011: Memory Read / Memory Write 101: Configuration Read / Configuration Write 110: Memory Read Multiple / Memory Write 111: Memory Read Line / Memory Write Setting is prohibited for other than the above.	R/W
b10 to b4	—	Reserved	When writing, write 0.	R/W
b31 to b11	PCIWIN1_BASEADR [20:0]	PCI bus base address	These bits specify the base address of the PCI bus for access from AHB to AHB-PCI Window 1. This register should be set when the PCI configuration space for the host logic or for the AHB-PCI bridge is accessed. For details of settings, see section 31.4.1.1, Access to PCI Configuration Registers.	R/W

31.3.6.3 AHBPCI_WIN2_CTR Register

This register is used to make necessary settings for access to the OHCI operational register area.

Address(es) A005 0814h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PCIWIN2_BASEADR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BURST_EN	—	PCICMD[2:0]			—
Value after reset	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	When writing, write 0.	R/W
b3 to b1	PCICMD[2:0]	PCI bus cycle type	These bits specify the type of PCI bus cycle. In the USB host controller, set these bits to 011b during the initial settings and do not change the value. b3 b1 001: IO Read / IO Write 011: Memory Read / Memory Write 110: Memory Read Multiple / Memory Write 111: Memory Read Line / Memory Write Setting is prohibited for other than the above.	R/W
b4	—	Reserved	When writing, write 0.	R/W
b5	BURST_EN	PCI bus burst transfer enable	This bit enables burst transfer to the PCI bus. In the USB host controller, clear to 0 during the initial settings and do not change the value. 0: Burst transfer is disabled. 1: Burst transfer is enabled.	R/W
b15 to b6	—	Reserved	When writing, write 0.	R/W
b31 to b16	PCIWIN2_BASEADR[15:0]	PCI bus base address	These bits specify the base address of the PCI bus for access from AHB to AHB-PCI Window 2. This register is used for access to the OHCI operational register area. For details of settings, see section 31.4.1.1, Access to PCI Configuration Registers.	R/W

31.3.6.4 PCI_INT_ENABLE Register

This register enables or disables each interrupt source indicated in the PCI_INT_STATUS register. When an interrupt source is disabled, the interrupt signal is not asserted even when the interrupt source is generated and the corresponding bit in the PCI_INT_STATUS register is set to 1.

Address(es) A005 0820h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	USBH_PMEEN	—	USBH_INTBEN	USBH_INTAEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PCIAHB_WIN2_INTEN	PCIAHB_WIN1_INTEN	—	—	—	—	—	—	RESERR_INTEN	SIGSERR_INTEN	PERR_INTEN	REMABORT_INTEN	RETABORT_INTEN	SIGTABORT_INTEN
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SIGTABORT_INTEN	SIGTABORT interrupt enable	This bit enables or disables the interrupt source indicated in bit 0 (SIGTABORT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b1	RETABORT_INTEN	RETABORT interrupt enable	This bit enables or disables the interrupt source indicated in bit 1 (RETABORT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b2	REMABORT_INTEN	REMABORT interrupt enable	This bit enables or disables the interrupt source indicated in bit 2 (REMABORT_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b3	PERR_INTEN	PERR interrupt enable	This bit enables or disables the interrupt source indicated in bit 3 (PERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b4	SIGSERR_INTEN	SIGSERR interrupt enable	This bit enables or disables the interrupt source indicated in bit 4 (SIGSERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b5	RESERR_INTEN	RESERR interrupt enable	This bit enables or disables the interrupt source indicated in bit 5 (RESERR_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b11 to b6	—	Reserved	When writing, write 0.	R/W
b12	PCIAHB_WIN1_INTEN	PCIAHB_WIN1 interrupt enable	This bit enables or disables the interrupt source indicated in bit 12 (PCIAHB_WIN1_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b13	PCIAHB_WIN2_INTEN	PCIAHB_WIN2 interrupt enable	This bit enables or disables the interrupt source indicated in bit 13 (PCIAHB_WIN2_INT) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b15, b14	—	Reserved	When writing, write 0.	R/W
b16	USBH_INTAEN	USBH interrupt enable	This bit enables or disables the interrupt source indicated in bit 16 (USBH_INTA) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b17	USBH_ INTBEN	USBH interrupt enable	This bit enables or disables the interrupt source indicated in bit 17 (USBH_INTB) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b18	—	Reserved	When writing, write 0.	R/W
b19	USBH_ PMEEN	USBH_PME enable	This bit enables or disables the interrupt source indicated in bit 19 (USBH_PME) in PCI_INT_STATUS. 0: Disabled 1: Enabled	R/W
b31 to b20	—	Reserved	When writing, write 0.	R/W

31.3.6.5 PCI_INT_STATUS Register

This register indicates the state of interrupt sources in the AHB-PCI bridge and the state of interrupt signals from the host logic.

Address(es) A005 0824h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	USBH_PME	—	USBH_INTB	USBH_INTA
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PCIAHB_WIN2_INT	PCIAHB_WIN1_INT	—	—	—	—	—	—	RESERR_INT	SIGSERR_INT	PERR_INT	REMABORT_INT	RETABORT_INT	SIGTABORT_INT
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SIGTABORT_INT	Target Abort notification	This bit indicates that Target Abort has been sent in PCI target operation. Writing 1 clears this bit. 0: Target Abort has not been sent. 1: Target Abort has been sent.	R/W
b1	RETABORT_INT	Target Abort reception	This bit indicates that Target Abort has been received in PCI master operation. Writing 1 clears this bit. 0: Target Abort has not been received. 1: Target Abort has been received.	R/W
b2	REMABORT_INT	MasterAbort reception	This bit indicates that Master Abort has been received in PCI master operation. Writing 1 clears this bit. 0: Master Abort has not been received. 1: Master Abort has been received.	R/W
b3	PERR_INT	PERR# Input/Output interrupt source status	This bit indicates the state of the interrupt source caused by PERR# input/output. Writing 1 clears this bit. 0: PERR# has not been asserted. 1: PERR# has been asserted.	R/W
b4	SIGSERR_INT	SERR# Output interrupt source status	This bit indicates the state of the interrupt source caused by SERR# output. Writing 1 clears this bit. 0: SERR# has not been asserted. 1: SERR# has been asserted.	R/W
b5	RESERR_INT	SERR# Input interrupt source status	This bit indicates the state of the interrupt source caused by SERR# input. Writing 1 clears this bit. 0: SERR# assertion has not been detected. 1: SERR# assertion has been detected.	R/W
b11 to b6	—	Reserved	When writing, write 0.	R/W
b12	PCIAHB_WIN1_INT	AHB bus error occurrence flag	This bit indicates that an AHB bus error has occurred in PCIAHB Window 1. Writing 1 clears this bit. 0: AHB bus error has not occurred. 1: AHB bus error has occurred.	R/W
b13	PCIAHB_WIN2_INT	AHB bus error occurrence flag	This bit indicates that an AHB bus error has occurred in PCIAHB Window 2. Writing 1 clears this bit. 0: AHB bus error has not occurred. 1: AHB bus error has occurred.	R/W
b15, b14	—	Reserved	When writing, write 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b16	USBH_INTA	Host logic INTA# interrupt status	This bit indicates the state of the INTA# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: INTA interrupt has not occurred. 1: INTA interrupt has occurred.	R
b17	USBH_INTB	Host logic INTB# interrupt status	This bit indicates the state of the INTB# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: INTB interrupt has not occurred. 1: INTB interrupt has occurred.	R
b18	—	Reserved	When writing, write 0.	R/W
b19	USBH_PME	Host logic PME# interrupt status	This bit indicates the state of the PME# interrupt from the host logic. The interrupt can be cleared from the host logic. 0: PME interrupt has not occurred. 1: PME interrupt has occurred.	R
b31 to b20	—	Reserved	When writing, write 0.	R/W

31.3.6.6 AHB_BUS_CTR Register

This register specifies the AHB master and slave functions of the host logic.

Address(es) A005 0830h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SMODE_READY_CTR	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	MMODE_HBUSREQ	—	—	—	—	MMODE_WR_INCR	MMODE_BYTE_BURST	MMODE_HTRANS
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MMODE_HTRANS	HTRANS signal operation mode setting	This bit specifies the operating mode for the HTRANS signal in AHB master operation. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: For divided cycles, NONSEQ is output continuously. 1: For divided cycles, IDLE is inserted and the bus is requested again through HBUSREQ.	R/W
b1	MMODE_BYTE_BURST	Burst transfer control	This bit controls burst transfer for 16-bit or 8-bit transfer in AHB master operation. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: Burst transfer is enabled for 16-bit or 8-bit transfer. 1: Burst transfer is disabled for 16-bit or 8-bit transfer.	R/W
b2	MMODE_WR_INCR	Condition setting of using undefined-length burst transfer	This bit specifies the condition of using an undefined-length burst for write transfer in AHB master operation. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: INCR is always used except when the transfer count is 4, 8, or 16. 1: INCR4, INCR8, and INCR16 are generally used, and INCR is used only when the remaining data is 2 to 3 beats.	R/W
b6 to b3	—	Reserved	When writing, write 0.	R/W
b7	MMODE_HBUSREQ	HBUSREQ deassertion timing setting	This bit specifies the timing of HBUSREQ deassertion in AHB master operation. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: Deasserted in the last address phase of the cycle. 1: Deasserted with the first timing of HGRANT = 1 and HREADY = 1.	R/W
b16 to b8	—	Reserved	When writing, write 0.	R/W
b17	SMODE_READY_CTR	Wait operation control	This bit controls the wait operation in AHB slave operation. Set this bit to 0 in a system that uses RETRY or SPLIT. Do not modify this value except for initial setting. 0: Wait is controlled with HRESP = RETRY. 1: Wait is controlled with HREADY = 0.	R/W
b31 to b18	—	Reserved	When writing, write 0.	R/W

31.3.6.7 USBCTR Register

This register is used to make settings of the host logic.

Address(es) A005 0834h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PCI_AHB_WIN1_SIZE[1:0]		PCI_AHB_WIN2_EN	—	—	—	—	—	—	—	PCICLK_MASK	USBH_RST
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	USBH_RST	Reset signal control	This bit controls the reset signal supplied to the host logic. The host logic can be accessed a maximum of 3 USBPCLK clock cycles after the reset is canceled. 0: Host logic reset is canceled. 1: Host logic reset is issued.	R/W
b1	PCICLK_MASK	PCI clock supply mask	This bit stops the PCI clock supply in the host logic. Note that the host logic cannot be accessed when this bit is set to 1. 0: PCI clock is supplied. 1: PCI clock is stopped.	R/W
b8 to b2	—	Reserved	When writing, write 0.	R/W
b9	PCI_AHB_WIN2_EN	PCI-AHB Window2 enable	This bit enables operation of PCI-AHB Window 2. For details, see section 31.4.1, Register Access. 0: PCI-AHB Window 2 is not available. Settings other than the above are prohibited. Operation cannot be guaranteed if the setting of this bit is modified.	R/W
b11, b10	PCI_AHB_WIN1_SIZE[1:0]	PCI-AHB Window1 area	These bits control the PCI-AHB Window 1 area. For details, see section 31.4.1, Register Access. Do not modify this value except for initial setting. b11 b10 10: 1 Gbyte	R/W
b31 to b12	—	Reserved	When writing, write 0.	R/W

31.3.6.8 PCI_ARBITER_CTR Register

This register is used to make settings of the PCI bus arbitration function.

Address(es) A005 0840h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCIBP_MODE	—	—	—	—	—	—	—	—	—	—	PCIREQ1	PCIREQ0
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PCIREQ0	PCI bus request signal mask 0	This bit enables or disables the PCI bus request signal from this unit. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: Request signal is disabled. 1: Request signal is enabled.	R/W
b1	PCIREQ1	PCI bus request signal mask 1	This bit enables or disables the PCI bus request signal from the host logic. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: Request signal is disabled. 1: Request signal is enabled.	R/W
b11 to b2	—	Reserved	When writing, always write 0.	R/W
b12	PCIBP_MODE	Master setting	This bit specifies the master while the PCI bus is in the parked state. In the USB host controller, set this bit to 1 during the initial settings and do not change the value. 0: This unit is the master in the bus-parked state. 1: The master that made the last access is the master in the bus-parked state.	R/W
b31 to b13	—	Reserved	Do not change this from the value after reset.	R/W

31.3.6.9 PCI_UNIT_REV Register

This register indicates the version of the AHB-PCI bridge macro.

Address(es) A005 0848h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	Major Revision ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	Minor Revision ID[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	Minor Revision ID [15:0]	Minor revision ID	These bits indicate the minor revision ID of this unit.	R
b31 to b16	Major Revision ID [15:0]	Major revision ID	These bits indicate the major revision ID of this unit.	R

31.4 Register Access

31.4.1 Register Access

Registers are accessed through the internal PCI bus. To access them from the AHB bus correctly, appropriately specify the mapping between the memory space for the AHB bus and that for the internal PCI bus in the USB host controller (see section 31.8.1.1, Sample of Initial Settings). Note that the PCI space is divided into two: the PCI memory space where data transfer is actually done, and the PCI configuration space where PCI bus transfer settings and the settings of the base addresses in the PCI memory space are stored.

Access from the AHB to the host logic and master access from the host logic to the AHB are done through the window areas in the AHB-PCI bridge. Figure 31.3 and Table 31.5 show the functions and relationship of register and window areas.

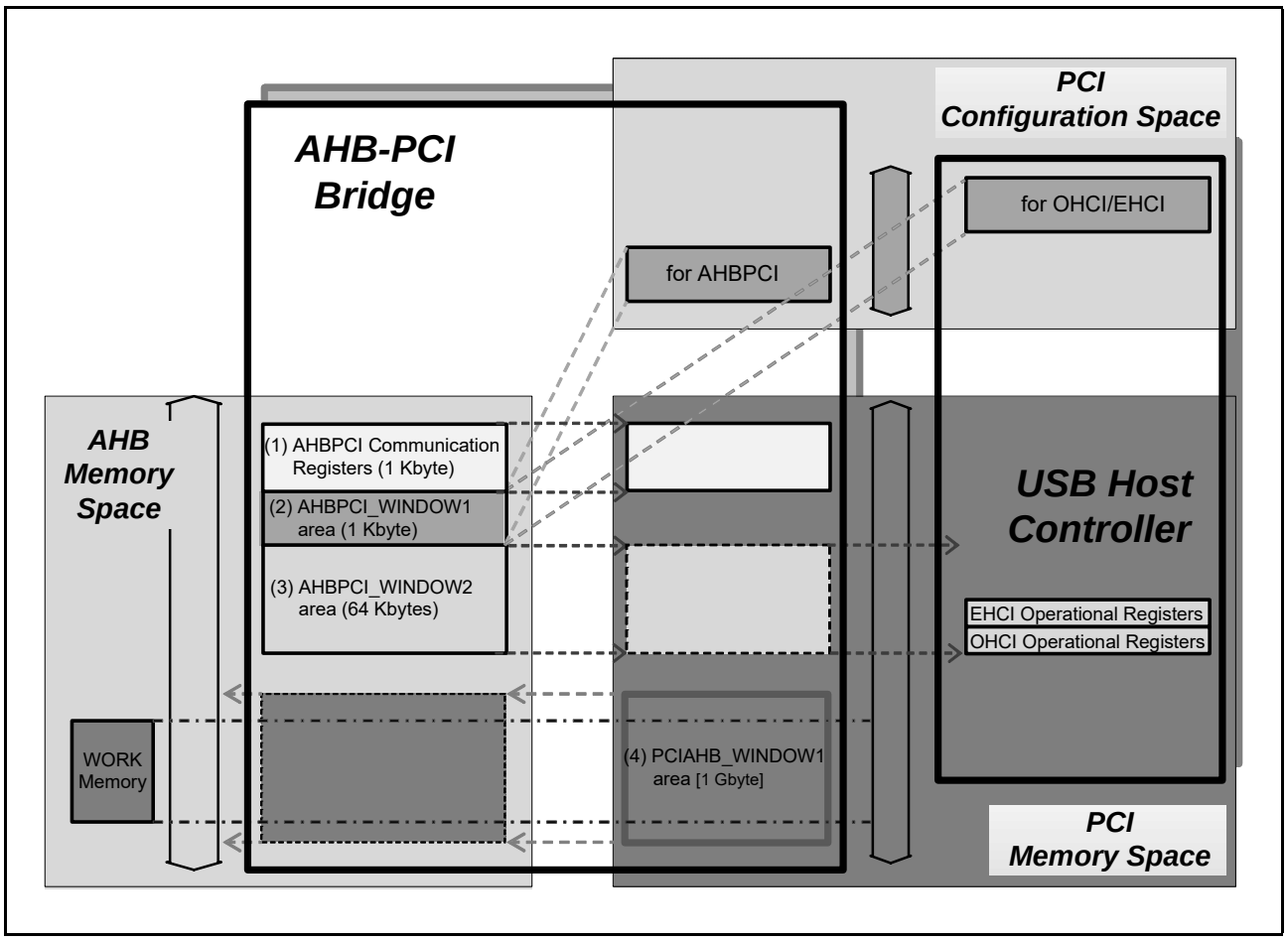


Figure 31.3 Image of AHB and PCI Space Mapping

Table 31.5 Descriptions of Areas

AHB Area Name	Size	Description
(1) AHBPCI communication registers	1 Kbyte	Various AHB settings are stored and the base address of each window area is specified. This area is also allocated in the PCI memory space; make sure that it does not overlap with other areas.
(2) AHBPCI_WINDOW1 area	1 Kbyte	The PCI configuration registers are accessed through this area. Whether to access an OHCI/EHCI configuration register or a register in the AHB-PCI bridge is switched through the AHBPCI_WIN1_CTR register setting.
(3) AHBPCI_WINDOW2 area	64 Kbytes	The OHCI/EHCI operational registers are accessed through this area.
(4) PCIAHB_WINDOW1 area	1 Gbyte	The host logic accesses the work memory on the AHB bus through this area. The size can be selected through the USBCTR register.

Make sure that the AHBPCI communication registers and the AHB-PCI window 2 area (OHCI/EHCI operational registers) do not overlap with the PCIAHB window 1 area in the PCI memory space.
An easy way to do this is to allocate the areas to the same addresses in both the AHB memory space and the PCI memory space.
However, when the above areas overlap due to the memory map for the AHB bus, use the PCI configuration registers (OHCI/EHCI/AHB-PCI Base Address registers) to avoid overlap with the PCI-AHB window 1 area. Figure 31.4 shows an image of mapping in such cases.

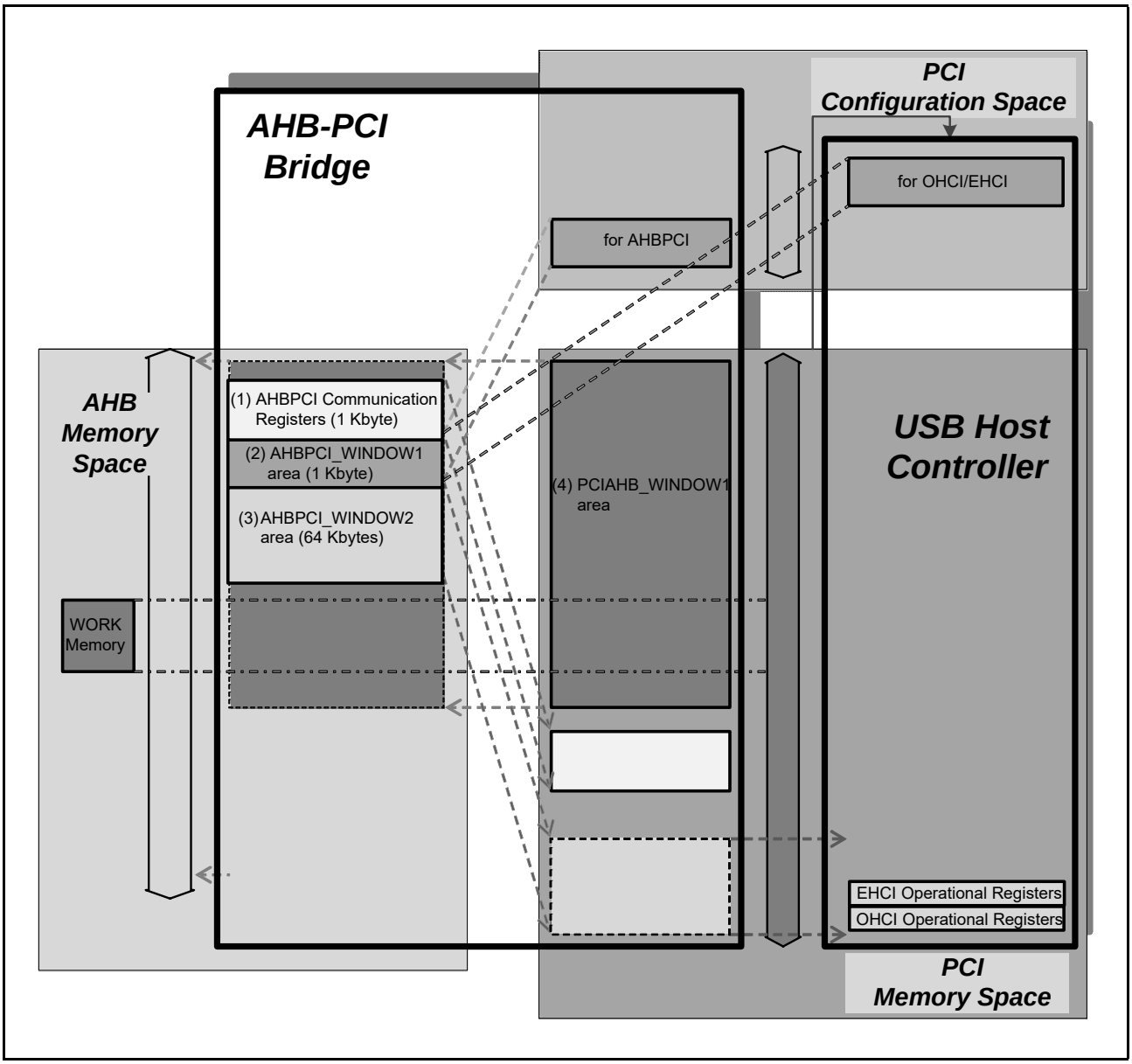


Figure 31.4 Image of AHB and PCI Space Mapping (when Areas Overlap)

Figure 31.5 and Table 31.6 show the registers used for AHB and PCI space mapping and the relationship between the settings in the registers and the mapping in the spaces.

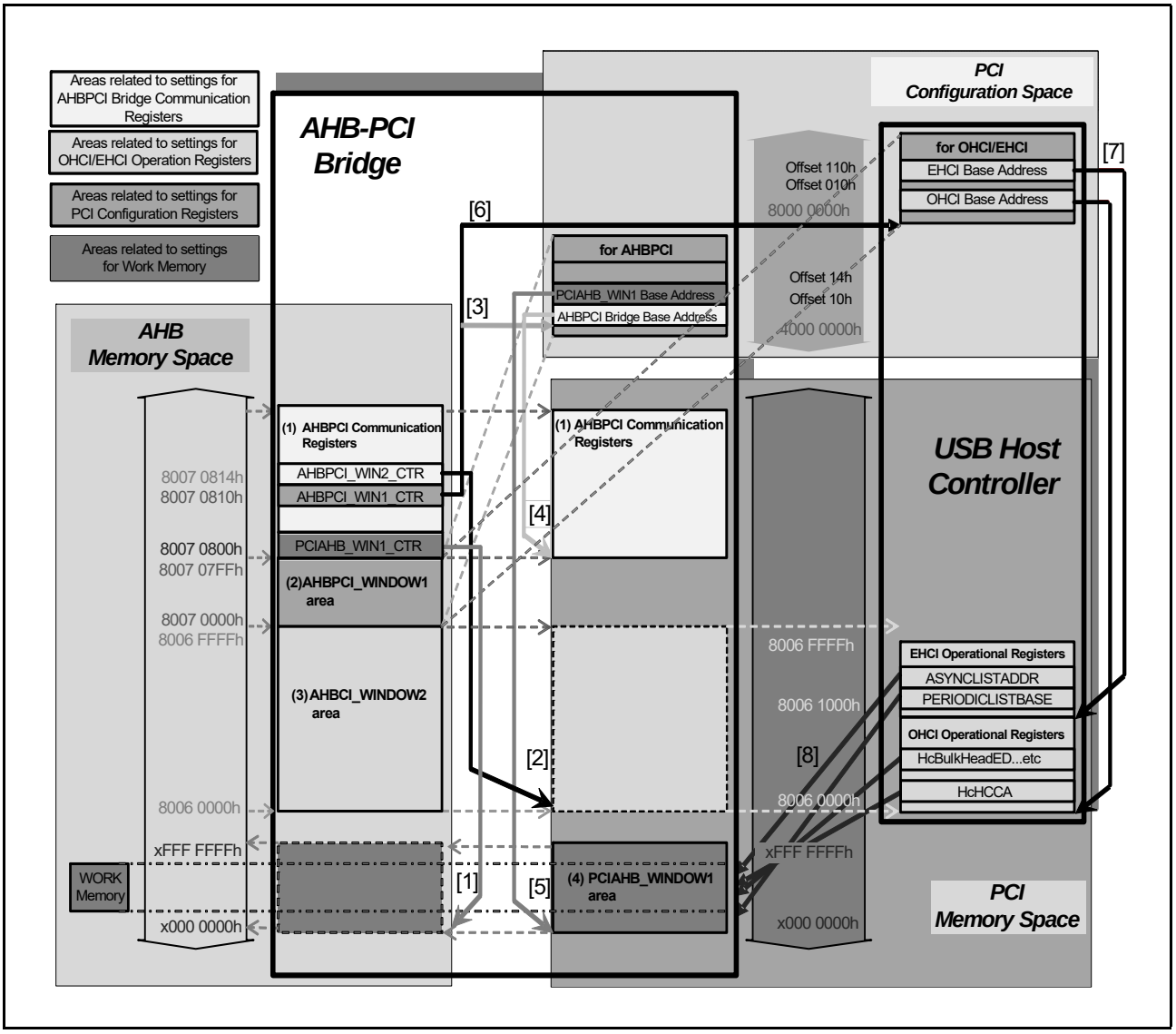


Figure 31.5 Relationship between the Address Setting in the Registers and AHB and PCI Space Mapping

Table 31.6 Descriptions of Address Settings in Registers

Register	Description
[1] PCIAHB_WIN1_CTR	When the host logic performs master access to the PCI-AHB window 1 area, the AHB bus address is converted to the base address specified in this register. In general usage, specify an area including the work memory to be used.
[2] AHBPCI_WIN2_CTR	When the AHB-PCI window 2 area is accessed, the PCI bus address is converted to the base address specified in this register. In general usage, this register can be set to the same value as that for the AHB-PCI window 2 area. However, if this area overlaps the area specified in [1] (the area including work memory), specify an appropriate address to avoid overlap.
[3] AHBPCI_WIN1_CTR	When the base address is set to 4000_0000h in this register, the PCI configuration registers for AHB-PCI are accessed.
[4] AHBPCI Bridge Base Address	This register specifies the base address of the AHB-PCI bridge in the PCI space. This register is not accessed from the PCI bus, but specify an appropriate address to avoid overlap with other areas.
[5] PCIAHB_WIN1 Base Address	This register specifies the base address of the PCI-AHB window 1 area in the PCI space. In general usage, specify the same base address as [1].
[6] AHBPCI_WIN1_CTR	When the base address is set to 8000_0000h in this register, the PCI configuration registers for OHCI/EHCI are accessed.
[7] OHCI/EHCI Base Address	This register specifies the base address of the OHCI/EHCI operational registers in the PCI space. In general usage, the OHCI base address is specified as the same value as specified in [2]. The EHCI base address is set to a value obtained by adding an offset of 1000h to the base address specified in [2].
[8] Various OHCI/EHCI Operational Registers	After settings of [1] to [7] are completed, the host logic can access data (such as descriptors) expanded in the work RAM on the AHB bus through the PCI. The following registers specify the addresses of data stored in work RAM. • OHCI/EHCI operational registers – HcHCCA register – HcPeriodicCurrentED register – HcControlHeadED register – HcControlCurrentED register – HcBulkHeadED register – HcBulkCurrentED register – HcDoneHead register • EHCI operational registers – PERIODICLISTBASE register – ASYNCLISTADDR register

31.4.1.1 Access to PCI Configuration Registers

The registers in the PCI configuration spaces are accessed through the AHB-PCI window 1 area (addresses 10000h to 107FFh: 2-Kbyte space). Before access, make appropriate settings in the AHBPCI_WIN1_CTR register. The following shows the settings of the AHBPCI_WIN1_CTR register to access the PCI configuration spaces for OHCI/EHCI and AHB-PCI bridge.

Table 31.7 AHBPCI_WIN1_CTR Register Setting

	AHBPCI_WIN1_CTR Register Setting	
Area to be Accessed	**PCIWIN1_BASEADR[31:11]**	**PCICMD[2:0]**
OHCI/EHCI PCI Configuration Space	Only bit 31 is set to 1.	101b
AHB-PCI Bridge PCI Configuration Space	Only bit 30 is set to 1.	

31.4.1.2 Access to OHCI/EHCI Operational Registers

When OHCI/EHCI operational registers are accessed, it is necessary to make settings in the OHCI/EHCI PCI configuration register and the AHBPCI_WIN2_CTR register as well as PCI space address mapping. The following shows the necessary settings.

Table 31.8 Necessary Settings for Access to OHCI/EHCI Operational Registers

Locations of Settings	**Settings**
OHCI/EHCI PCI configuration apace Offset 04h (Command, Status) Bit1 (Memory space)	1 (Access to memory space is enabled)
AHBPCI_WIN2_CTR register bit[3:1] PCICMD[2:0]	011b (Memory read or memory write)

31.5 Clock Lines

31.5.1 Externally Supplied Clocks

The following three clock signals are supplied from within the chip to the USB host controller of the RZ/T1.

Table 31.9 List of Externally Supplied Clocks

Clock Signal	Function	Frequency
PCLKA	AHB clock AHB clock for power management	150 MHz
USBMCLK	Reference clock	50 MHz
USBPCLK	PCI clock inside the USB host controller	30 MHz

31.5.2 Clock Distribution Diagram

Figure 31.6 shows the clock distribution diagram of this system.

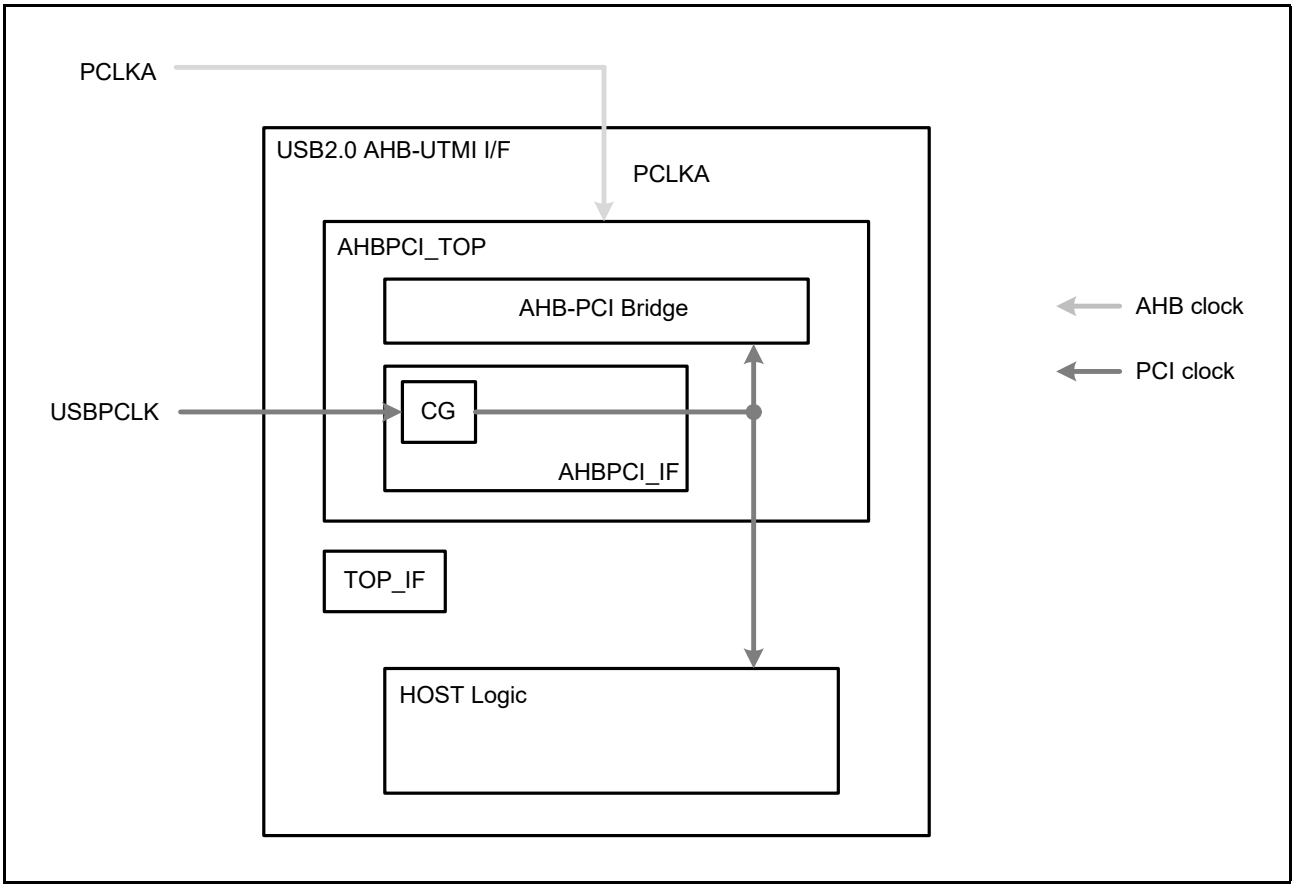


Figure 31.6 Clock Distribution Diagram

31.6 Interrupts

31.6.1 Interrupt Control Registers

31.6.1.1 U2H_INT Control Registers

U2H_INT is an interrupt signal generated by the AHB-PCI bridge. Registers in the AHB-PCI bridge are used to check and clear the interrupt state and to enable interrupts.

Table 31.10 U2H_INT Control Registers

Operation	Control Register
Check and clear interrupt state	PCI_INT_STATUS register
Enable interrupts	PCI_INT_ENABLE register

31.6.1.2 U2H_OHCI_INT Control Registers

U2H_OHCI_INT is the INTA interrupt signal from the host logic. Each interrupt is controlled basically through registers in the host logic, but to assert the interrupt signal, the interrupt enable bit in the AHB-PCI bridge should be set.

Table 31.11 U2H_OHCI_INT Control Registers

Operation	Control Register
Check and clear interrupt state	HcInterruptStatus register
Enable interrupts	HcInterruptEnable register HcInterruptDisable register PCI_INT_ENABLE register (bit 16 (USBH_INTAEN))

31.6.1.3 U2H_EHCI_INT Control Registers

U2H_EHCI_INT is the INTB interrupt signal from the host logic. Each interrupt is controlled basically through registers in the host logic, but to assert the interrupt signal, the interrupt enable bit in the AHB-PCI bridge should be set.

Table 31.12 U2H_EHCI_INT Control Registers

Operation	Control Register
Check and clear interrupt state	USBSTS register
Enable interrupts	USBINTR register PCI_INT_ENABLE register (bit 17 (USBH_INTBEN))

31.6.1.4 U2H_PME_INT Control Registers

U2H_PME_INT is the PME interrupt signal from the host logic. Each interrupt is controlled basically through registers in the host logic, but to assert the interrupt signal, the interrupt enable bit in the AHB-PCI bridge should be set.

Table 31.13 U2H_PME_INT Control Registers

Operation	Control Register
Check and clear interrupt state	PCI Configuration register for OHCI/EHCI offset 44h
Enable interrupts	PCI Configuration register for OHCI/EHCI offset 44h PCI_INT_ENABLE register (bit 19 (USBH_PMEEN))

31.6.2 U2H_BIND_INT

The U2H_BIND_INT interrupt signal is generated as the logical OR of four interrupt source signals (U2H_INT, U2H_OHCI_INT, U2H_EHCI_INT, and U2H_PME_INT).
The states of the U2H_PME_INT, U2H_OHCI_INT, and U2H_EHCI_INT signals are reflected in the PCI_INT_STATUS register in the AHB-PCI bridge. Read the register to check which source was responsible for a generated interrupt.

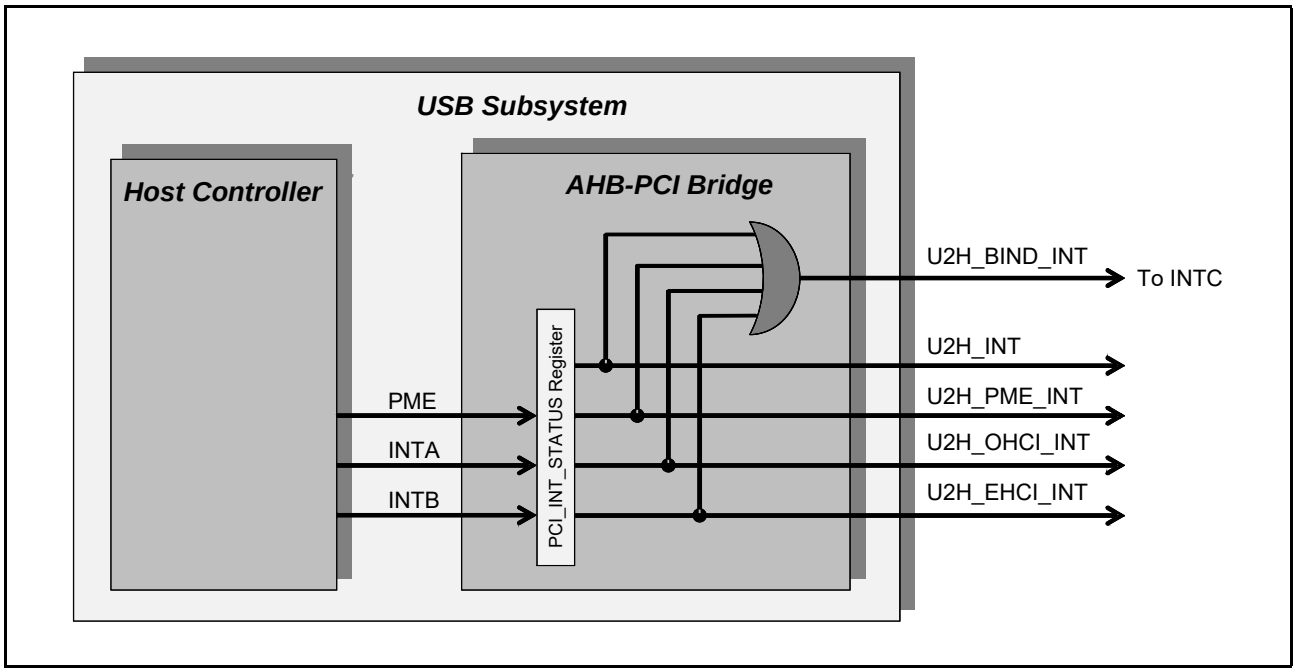


Figure 31.7 Image of Interrupt Signal Integration

31.6.3 Time Required to Clear Interrupt Signals

An interrupt generated in the USB host controller may be falsely detected multiple times because, depending on the access state on the internal bus, it may take a long time to actually clear the interrupt after the register for clearing the interrupt source is written to (see Figure 31.8 Time Required to Clear an Interrupt) due to the posted write operation of the AHB bridge.
A measure should be taken to prevent false detection before the next interrupt is detected after the register access for clearing the interrupt is completed.
For example, after accessing the register for clearing the interrupt source (1), access any register in the host logic (2). Register access (2) waits (SHREADY/MHREADY = 0 or RETRY response) until (1) is completed, and the interrupt is cleared without fail when register access (2) is completed.

(1) Host Logic
It may take time to clear a U2H_OHCI_INT, U2H_EHCI_INT, or U2H_PME_INT interrupt after the register for clearing the interrupt is accessed.
This usually takes approximately 300 ns when PCLKA is 150 MHz, but in the worst case when master transfer is in progress on the internal PCI bus, this takes 36 USBPCLK cycles + 3 PCLKA cycles + two 12-MHz clock cycles; this is approximately 1.4 µs when USBPCLK is 30 MHz.

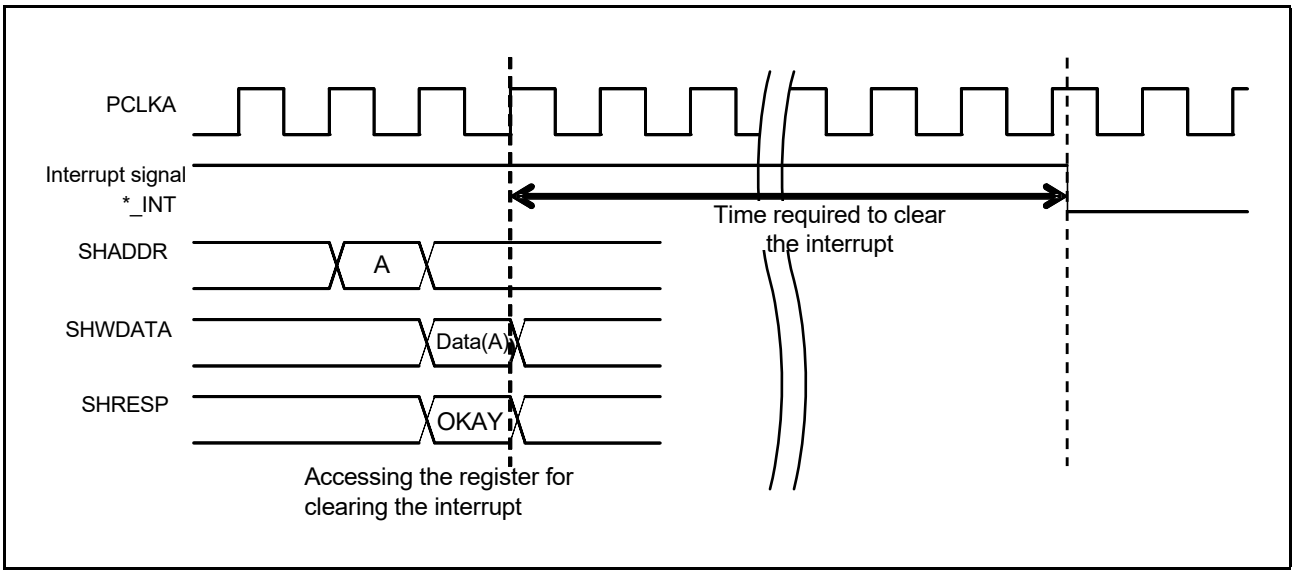


Figure 31.8 Time Required to Clear an Interrupt

31.7 Overcurrent Control and VBUS Control

31.7.1 Overcurrent Control

This section describes the operation of the USB_OVRCUR and USB_VBUSEN signals used for overcurrent detection at the USB port and VBUS control.

31.7.1.1 USB_OVRCUR and USB_VBUSEN Signal Functions

Table 31.14 shows the meaning of the USB_OVRCUR and USB_VBUSEN signals.

Table 31.14 USB_OVRCUR and USB_VBUSEN

Pin	I/O	Level	Meaning
USB_OVRCUR	Input	1	No overcurrent has been detected.
		0	Overcurrent has been detected.
USB_VBUSEN	Output	1	Power supply to VBUS is on.
		0	Power supply to VBUS is off.

31.7.1.2 Conditions for Asserting and Deasserting USB_VBUSEN Output Signal

Figure 31.9 is a timing chart for USB_OVRCUR and USB_VBUSEN assertion and deassertion.

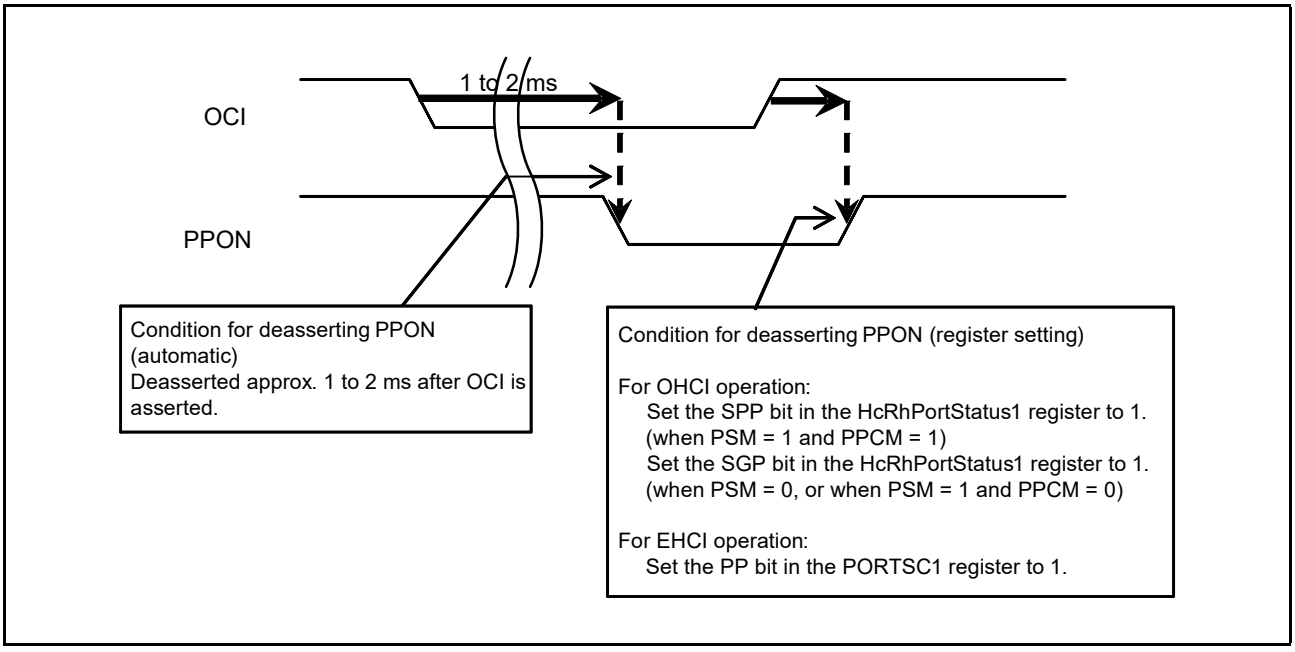


Figure 31.9 Timing Chart for USB_OVRCUR and USB_VBUSEN Assertion and Deassertion

After USB_OVRCUR is deasserted, USB_VBUSEN is not asserted automatically. USB_VBUSEN is asserted when software sets the port power bit after USB_OVRCUR is deasserted.

31.7.2 VBUS Control

When the USB port is not used, VBUS can be stopped to reduce power consumption by connecting the USB_OVRCUR and USB_VBUSEN pins to the high-side switch (although this may not be possible depending on the connections with peripheral circuits).
The relationship between USB_VBUSEN and VBUS is shown below.

Table 31.15 Relationship between USB_VBUSEN and VBUS

USB_VBUSEN	VBUS
0	Stopped
1	Operated

The USB_VBUSEN operation when USB_OVRCUR is asserted depends on the settings in the PCI configuration register and OHCI operational registers as shown below.

Table 31.16 Register Settings and USB_VBUSEN Operation

OHCI Operational Registers				
HcRhDescriptorA Register			HcRhDescriptorB Register	USB_VBUSEN Output Pin Operation
NOCP Bit	NPS Bit	PSM Bit	PPCM[1] Bit	
1	—	—	—	Fixed to 1
—	1	—	—	Fixed to 1
0	0	0	—	Deasserted (0) when USB_OVRCUR is asserted (0)
		1	0	
			1	

Note: When NPS = 1, the host logic detects an overcurrent but does not deassert USB_VBUSEN.

31.7.3 Initial Settings of PPON1

ON and OFF of PPON1 (PortPower) is controlled by the port control register of OHCI/EHCI operational registers listed below in general usage after reset without setting the NOCP and NPS bits in the HcRhDescriptorA register. PPON1 is turned ON when at least one of the following bits (SPP, SGP, and PP) is ON.
In general, the following bits (SPP, SGP, and PP) are cleared to 0 when an overcurrent is detected.

Register		Bit	Symbol
OHCI operation	HcRhPortStatus1 register	8	SPP
	HcRhPortStatus register	16	SGP*1
EHCI operation	PORTSC1 register	12	PP

Note 1. This is not generally used with the single-port version.
For PPON control by this bit, the bit must be in the state of PSM = 0, or PSM = 1 and PPCM = 0.

PPON1 is turned on by setting the NOCP or NPS bit to 1 regardless of the Port Power bit of the above ports.
The initial settings of the PPON1 control bits (SPP, SGP, PP, NOCP, and NPS) mentioned above are all 0 (OFF). Setting these bits to 1 (ON) during initial setting, the procedure in the following flow is required.

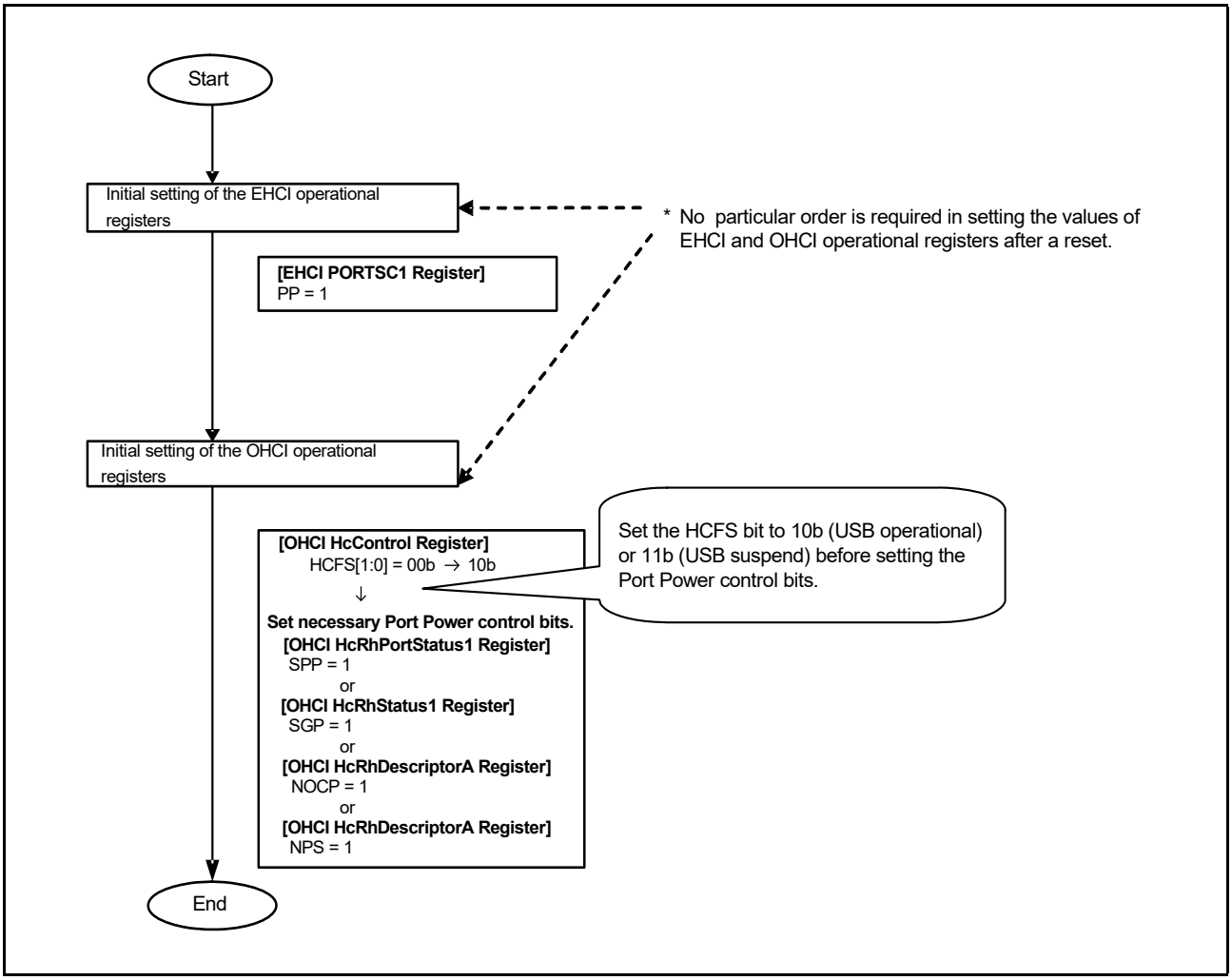


Figure 31.10 Flow of PPON1 Initial Settings

31.7.4 Procedure for USB_VBUSEN Control Regarding Overcurrent Detection

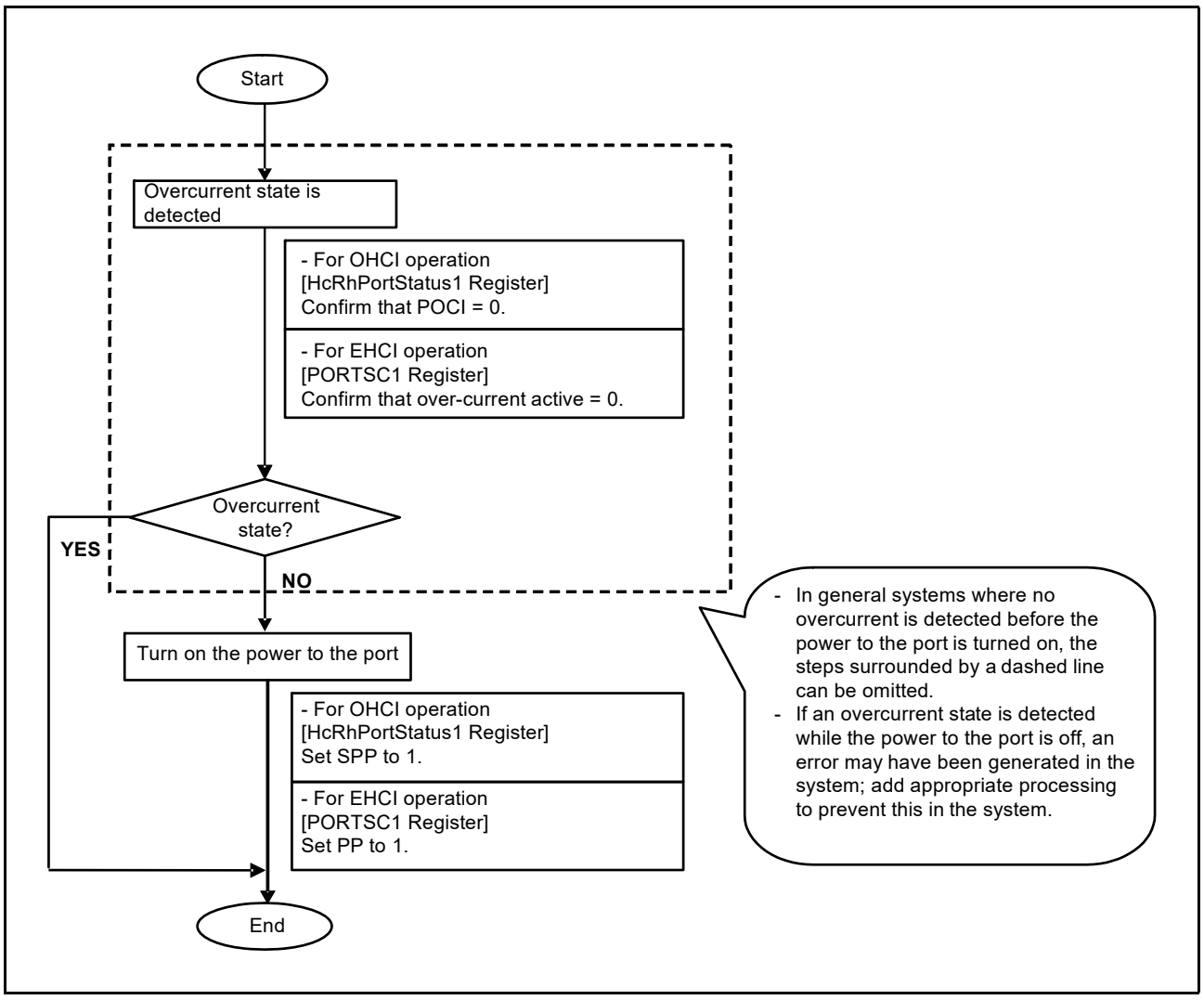


Figure 31.11 Flow for USB_VBUSEN Control Regarding Overcurrent Detection

31.7.5 Procedure for USB_VBUSEN Setting

The following shows the procedure for USB_VBUSEN setting in a system where USB_OVRCUR may be active (0) at system start-up.

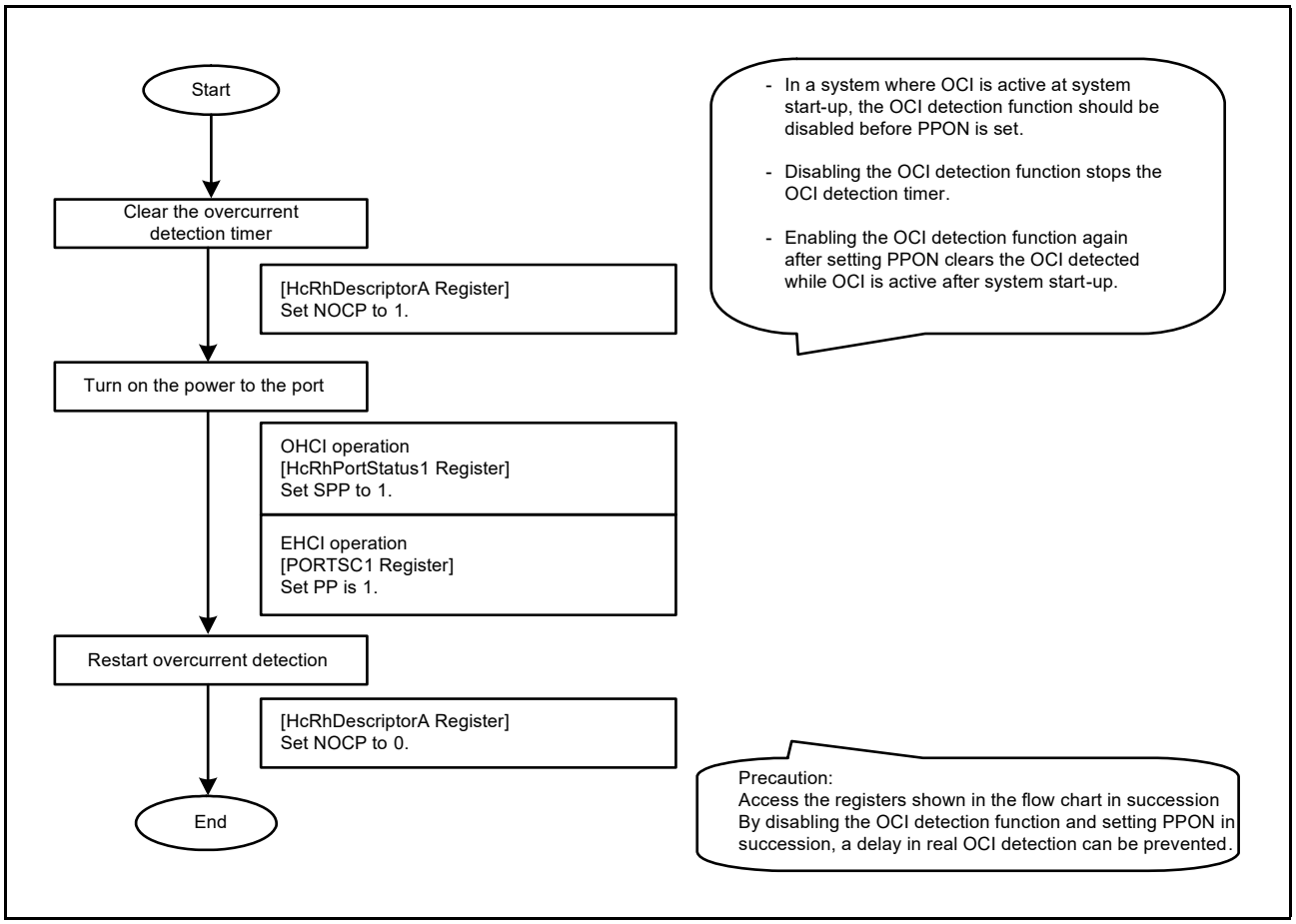


Figure 31.12 Flow for USB_VBUSEN Setting

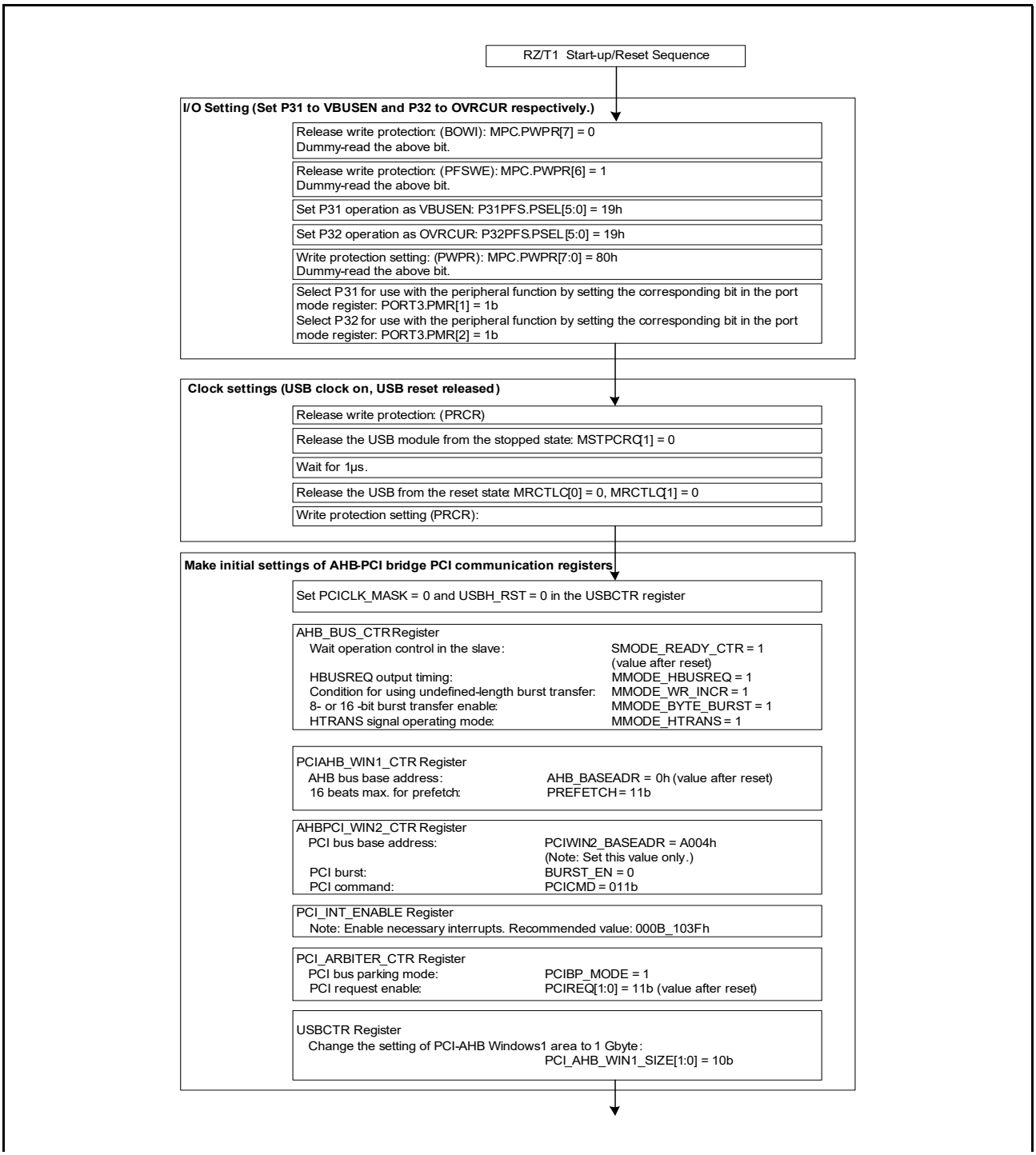
31.8 Operating Procedures

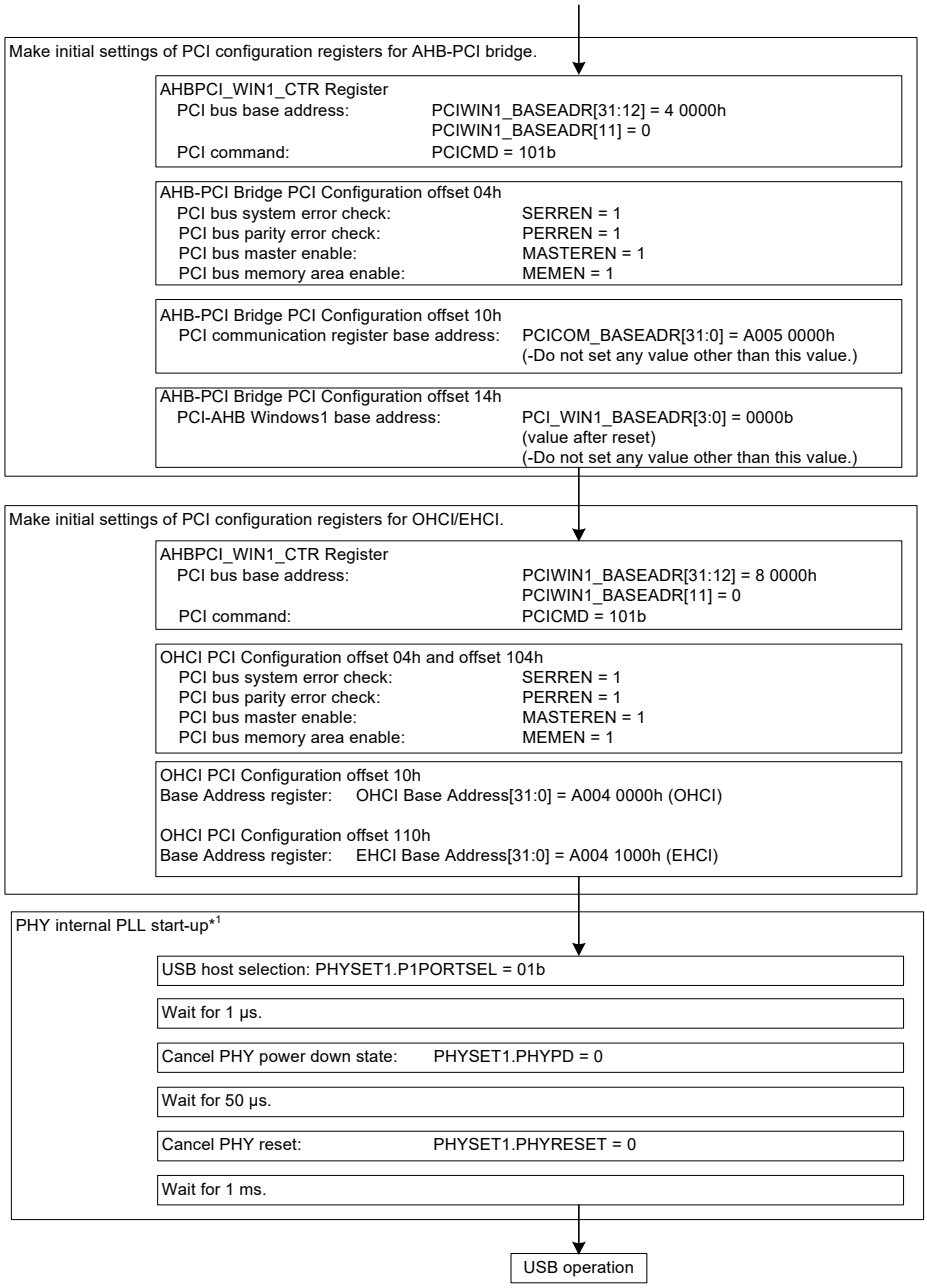
31.8.1 Initial Setting Sequence

31.8.1.1 Sample of Initial Settings

This section shows sample initial settings to implement the following functions.

- Access to OHCI/EHCI operational registers through AHB-PCI window 2 registers.
- Data transfer from the host logic to the AHB bus.





Note 1. A halt of the operation of the PHY internal PLL by setting PHY Power-Down (the PHYSET1.PHYPD bit is 1) and PHY reset (PHYSET1.PHYRESET bit is 1) is prohibited once the PHY internal PLL is activated.

Figure 31.13 Initial Setting Sequence

31.8.2 USB Host Transfer Procedure

For the USB host transfer procedure, see the following OHCI and EHCI specifications.

- Open Host Controller Interface Specification for USB Rev 1.0a
- Enhanced Host Controller Interface Specification for Universal Serial Bus Revision 1.0

This section gives only supplementary information regarding DMA stop.

31.8.2.1 Stopping DMA Transfer

The AHB-PCI Bridge core does not have a function for starting or stopping DMA transfer. The PCI bus cycle started by the host logic working as the master is output to the AHB bus as a DMA transfer without change.
DMA transfer is done in the following two cases.

(1) The current frame number is written to memory.
(2) The descriptors and data expanded in memory are read or written to for list processing.

Note: The frame number is automatically written at frame cycle intervals when the USB state is operational.

To stop DMA transfer, shift the USB state to Suspend or Reset.
To suspend only the list processing in (2), clear the bit for enabling list processing (BLE, CLE, IE, or PLE bit in the HcControl register); the list processing stops at the next frame.

32. USB 2.0 HS Function Module (USBf)

32.1 Overview

The USB module of this LSI is a dual-role device that has USB 2.0 host and function modules. However, it does not have a facility for detecting the ID and so does not support On-the-Go (OTG) functionality.
This LSI handles a single USB port for either host controller or function controller operation. The port connection path select input signal bits (PHYSET1.P1PORTSEL[1:0]) are used to switch between host controller and function controller operation.
Since operation as a host controller or a function controller are exclusive of each other, dynamic switching between the types of operation is not possible.

This section describes function controller operation.

The USBf module supports high-speed transfer and full-speed transfer defined by the USB 2.0 specification.

This LSI supports all transfer types that are defined in the USB specification. It incorporates an 8-Kbyte buffer memory for data transfer and can use up to 10 pipes. Pipes 1 to 9 can be assigned an arbitrary endpoint number according to the user system. The controller is equipped with a dedicated DMA interface as a local bus interface which is independent of the CPU bus interface, making it suitable for systems requiring high-speed, large-capacity data transfer.

Table 32.1 Specifications of the USB Module (1 / 2)

Item	Description
For High-Speed USB	• Built-in USB function controller
For all types of USB transfer	• Support for all types of USB transfer, including isochronous • Control transfer • Bulk transfer • Interrupt transfer (high-bandwidth transfers not supported) • Isochronous transfer (high-bandwidth transfers not supported)
Bus interface	• Two DMA interfaces available - The interface with the DMAC is selectable and DMA transfer is independent of the CPU bus interface • High-speed data transfer for access to the internal FIFOs at 60 Mbytes/second (when the bus width is 32 bits)
Pipe configuration	• 8 Kbytes of buffer memory for USB communications • Up to 10 pipes can be selected (including the default control pipe) • Programmable pipe configuration • Any endpoint number can be assigned to pipes 1 to 9 • Transfer conditions that can be set for each pipe are listed below. Pipe 0: Control transfer, single buffer fixed at 64 bytes Pipes 1 and 2: Bulk transfer or isochronous transfer can be selected, continuous transfer mode, programmable buffer size (specifiable as up to 2 Kbytes, double buffer is also specifiable) Pipes 3 to 5: Bulk transfer, continuous transfer mode, programmable buffer size (specifiable as up to 2 Kbytes, double buffer is also specifiable) Pipes 6 to 9: Interrupt transfer, single buffer fixed at 64 bytes
Features of function controller operation	• High-speed (480 Mbps) and full-speed transfer (12 Mbps) are supported • Automatic recognition of high-speed operation or full-speed operation based on automatic response to the reset handshake • Control transfer stage monitoring • Monitoring of device state • Automatic response to SET_ADDRESS requests • NAK response interrupt function (NRDY) • SOF interpolation

Table 32.1 Specifications of the USB Module (2 / 2)

Item	Description
Other functions	• Judging the end of transfer on the basis of a transaction count • Adjustable timing for BRDY interrupt event notification (BFRE) • Automatic clearing of the buffer memory after the data for the pipe specified in the DxFIFO port has been read (DCLRM) • NAK setting for response PID generated by end of transfer (SHTNAK) • Only self-powered mode is supported (bus-powered mode is not supported).

Figure 32.1 is a block diagram of the USB module.

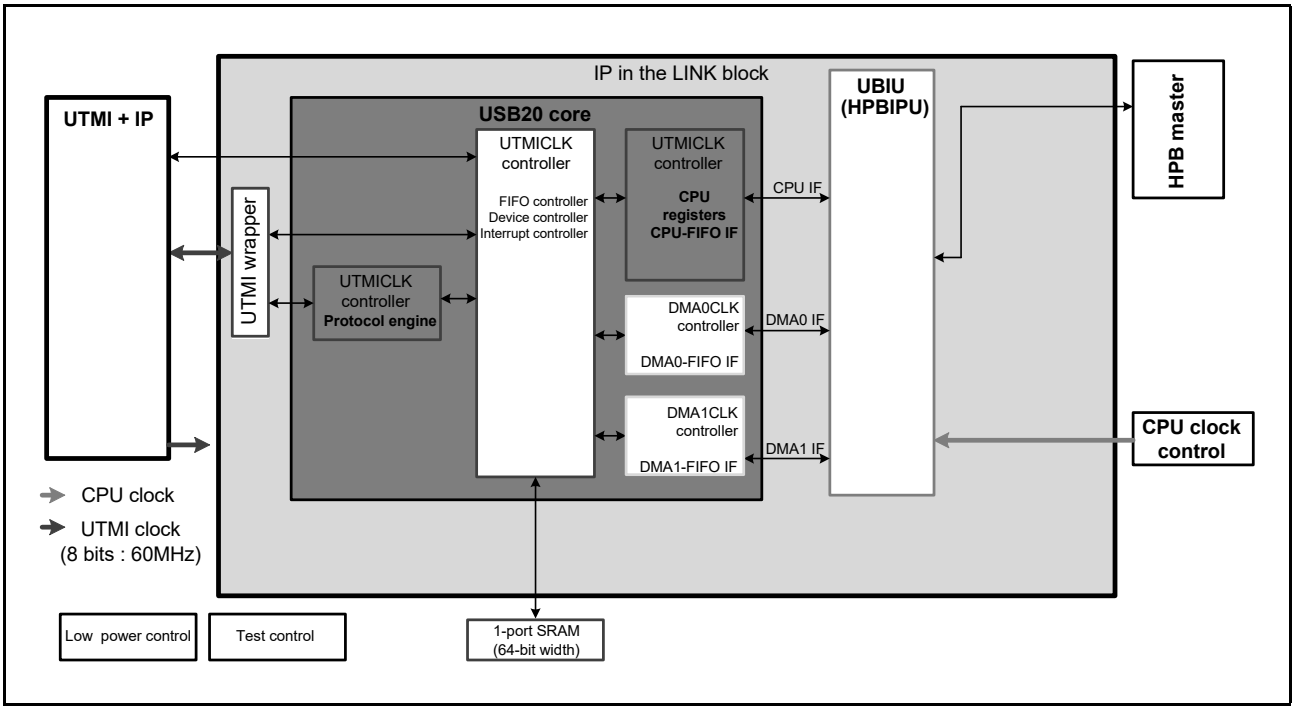


Figure 32.1 Block Diagram of the USB Module

Data transfer between this controller and the host controller connected to the USB bus uses buffer memory assigned to each pipe. For communication between this controller and the host controller, this controller converts the data stored in buffer memory into USB data packets and outputs them to the USB bus serially, and also inputs data packets from the USB bus and stores them in buffer memory.

32.1.1 Functional Overview

32.1.1.1 Identification of the USB Transfer Speed

The hardware can automatically identify the USB transfer speed.

32.1.1.2 Bus interface

(1) How to access the FIFO buffer memory

The following two types of access are available for the FIFO buffer memory for USB data transfers. To read from or write to the FIFO buffer memory, access (read or write) the FIFO ports from the CPU (DMAC).

1. CPU access
   Specify a FIFO port address and write data to the FIFO buffer memory or read data from the FIFO buffer memory.
2. DMA access
   Specify a FIFO port address through the DMAC in the CPU or the dedicated DMAC and write data to the FIFO buffer memory or read data from the FIFO buffer memory.

USB data transfer is done in little endian. The byte endian swap function is available for FIFO port access; for 16-bit or 32-bit access, the endian can be switched through register settings.

32.1.1.3 USB Event

This controller sends an interrupt to the user system to notify an event in USB operation. This controller asserts the UCL_Dx_DREQ (interrupt source [43] or [44]) signal to notify that the pipe selected for the DMA interface has become ready for access.

Sending interrupts for notification can be enabled or disabled separately for each interrupt type and source through software settings.

32.1.1.4 USB Data Transfer

This controller performs all types of USB data transfer: control transfer, bulk transfer, interrupt transfer, and isochronous transfer. The following numbers of pipes are available for each transfer type.
One pipe dedicated to control transfer
Four pipes dedicated to interrupt transfer
Three pipes dedicated to bulk transfer
Two pipes selectively used for bulk transfer or isochronous transfer

Each pipe should be set up as necessary for the desired USB transfer in accordance with the user system; for example, transfer type, endpoint number, or maximum packet size.

This controller has an 8-byte buffer memory. For pipes dedicated for bulk transfer or selective pipes for bulk transfer or isochronous transfer, buffer memory assignment, buffer operating mode setting, or other necessary settings should be made in accordance with the user system. By setting the buffer operating mode, such as double buffer structure or continuous data packet transfer mode, fast data transfer is achieved with fewer interrupts.

CPU and DMA controller access to the buffer memory is made through three FIFO port registers.

32.1.1.5 Functions for Access from Direct Memory Access Controller (DMAC)

This controller provides two channels of the DMA interface having the following functions.
(1) Notification of the end of transfer using a transfer end signal
(2) Automatic clearing of the FIFO buffer when a zero-length packet is received
(3) Judging the end of transfer using the transaction counter

32.2 Register Descriptions

32.2.1 System Configuration Control

32.2.1.1 System Configuration Control Register 0 (SYSCFG0)

Address(es): A006 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	HSE	—	DRPD	DPRPU	—	—	—	USBE
Value after hardware reset:	x	x	x	x	x	x	x	0	0	0	1	0	x	x	x	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b0	USBE	USB Block Operation Enable	Enables or disables operation of the USB block. 0: USB block operation is disabled. 1: USB block operation is enabled.	R/W	R
b3 to b1	—	Reserved	When writing to these bits, write 0.	R/W	—
b4	DPRPU	D+ Line Resistor Control	Enables or disables pulling up the D+ line in function controller operation. 0: Pulling up the line is disabled. 1: Pulling up the line is enabled.	R/W	R
b5	DRPD	D+/D- Line Resistor Control	Always set 0 at initialization.	R/W	R
b6	—	Reserved	When writing to this bit, write 0.	R/W	—
b7	HSE	High-Speed Operation Enable	Enables or disables high-speed operation. 0: High-speed operation is disabled (full-speed). 1: High-speed operation is enabled (the controller detects the communication speed)	R/W	R
b15 to b8	—	Reserved	When writing to these bits, write 0.	R/W	—

Note: Writing to this register is possible even while the UTMI clock (output of the clock signal from the PLL in the USB) is stopped. Note however that any values that are set while the UTMI clock is stopped are reflected after oscillation of the UTMI clock is restarted.

USB Block Operation Enable Bit (USBE)

The setting of the USBE bit enables or disables operation of the USB block.
When the USBE bit is modified from 1 to 0, this controller initializes the bits listed in Table 32.2.

Table 32.2 Registers Initialized by Writing USBE = 0

Register Name	Bit Name
SYSSTS0	LNST
DVSTCTR0	RHST
INTSTS0	DVSQ
USBADDR	USBADDR
USBREQ	bRequest bmRequestType
USBVAL	wValue
USBINDX	wIndex
USBLENG	wLength

The value of this bit must be changed when SUSPM = 1 and after the UTMI clock oscillation is started.

D+/D- Line Resistor Control (DRPD and DPRPU)

Settings related to USB data bus resistance are given in Table 32.3, USB Data Bus Resistance Control. Use the DRPD and DPRPU bits to select USB data bus resistance.

Table 32.3 USB Data Bus Resistance Control

Settings		USB Data Bus Resistance Control		
DRPD	DPRPU	D- Line	D+ Line	Remarks
0	0	Open	Open	
0	1	Open	Pull-up	Make these settings when the module is used as a function controller.
1	0	Pull-down	Pull-down	Setting prohibited
1	1	Pull-down	Pull-up	Setting prohibited

- D+ pull-up resistance control for function controller operation (DPRPU)

When this bit set to 1, this controller pulls up the D+ line to 3.3V and can notify the USB host that the function module is attached.
The controller cancels pulling-up of the D+ line by modifying this bit from 1 to 0, and the state for the USB host can be shown as detached.

Settings in these bits should be made set at the same time as that of PHYSET1.PHYVBUSIN.

Hi-Speed Operation Enable Bit (HSE)

Setting this bit to 1 enables high-speed operation. Setting the HSE bit to 1 lets this controller perform high-speed or full-speed operation based on the results of reset handshake.

Setting the HSE bit to 0 lets this controller perform full-speed operation.
On the other hand, setting the HSE bit to 1 lets this controller perform the reset handshake protocol and then perform high-speed or full-speed operation automatically according to the results.

This bit can be modified when DPRPU = 0.

32.2.1.2 System Configuration Control Register 1 (SYSCFG1)

Address(es): A006 0002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BWAIT[5:0]					
Value after hardware reset:	x	x	0	0	0	0	0	0	x	x	0	0	1	1	1	1
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b5 to b0	BWAIT[5:0]	CPU Bus Access Wait Specification	Specify the number of wait cycles for access to this controller. b5 b0 000000: 0 wait cycles (2 access cycles) : : 000010: 2 wait cycles (4 access cycles) : : 000100: 4 wait cycles (6 access cycles) : : 001111: 15 wait cycles (17 access cycles) (value after a reset) : : 111111: 63 wait cycles (65 access cycles)	R/W	R
b15 to b6	—	Reserved	When writing to these bits, write 0.	R/W	—

CPU Bus Access Wait Specification Bit (BWAIT)

For continuous access to the registers at addresses of this controller beginning at A006 0004h, at least 67 ns must be secured.

To satisfy this restriction, control wait cycles using the frequency of CPU clock. The value after a reset is the maximum value (17 clock cycles), so select an appropriate value no greater than this.

This setting is the same as that for waiting in access to a FIFO port register. The maximum speeds of access to the FIFO ports are as follows:
MBW = 10b (32-bit width): Max 60 Mbytes/sec
MBW = 01b (16-bit width): Max 30 Mbytes/sec
MBW = 00b (8-bit width): Max 15 Mbytes/sec

32.2.1.3 System Configuration Status Register (SYSSTS0)

Address(es): A006 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LNST[1:0]	
Value after hardware reset:	x	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	Indicate the state of the USB line.	R	W
b15 to b2	—	Reserved	These bits are read as an undefined value.	R	—

Line Status Monitor Bits (LNST)

The states of USB data bus line of this controller is shown in Table 32.4. The controller monitors the states of USB data bus lines (D+ and D- lines) in the LNST bits of the SYSSTS0 register.
Reference to the LNST bits must be made following attach processing (DPRPU = 1) after USBE has been set to 1.

Table 32.4 States of USB Data Bus Line

LNST[1]	LNST[0]	Full-Speed Operations	High-Speed Operations	Chirp Operations*1
0	0	SE0	Squelch*2	Squelch*2
0	1	J state	Unsquelch*3	Chirp J*4
1	0	K state	Invalid	Chirp K*5
1	1	SE1	Invalid	Invalid

Note 1. Chirp: Reset handshake protocol being executed in high-speed operations enabled state (HSE = “1”)
Note 2. Squelch: SE0 or idle state
Note 3. Unsquelch: High-speed J state or high-speed K state
Note 4. Chirp J: Chirp J-state
Note 5. Chirp K: Chirp K-state

32.2.2 USB Signal Control

32.2.2.1 Device State Control Register 0 (DVSTCTR0)

Address(es): A006 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	WKUP	—	—	—	—	—	RHST[2:0]		
Value after hardware reset:	x	x	x	x	x	0	0	0	0	0	0	0	x	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b2 to b0	RHST[2:0]	Reset Handshake	Indicate the state of reset handshake.	R	W
b7 to b3	—	Reserved	When writing to these bits, write 0.	R/W	—
b8	WKUP	Wakeup Output	Enables or disables the remote wakeup (resume signal output). Only 1 can be written to this bit. 0: Remote wakeup signal is not output. 1: Remote wakeup signal is output.	R/W	R/W
b15 to b9	—	Reserved	When writing to these bits, write 0.	R/W	—

Reset Handshake Status Bits (RHST)

These bits indicate the result of reset handshake. Table 32.5 lists the results of reset handshake.

Table 32.5 State of Reset Handshake

Bus State	RHST Bit Value
Powered or no connection	000b
Reset handshake in progress	100b
Full-speed connection	010b
High-speed connection	011b

When the HSE bit is set to 1, the RHST bits indicate 100b when this controller detects a USB bus reset. Then, these bits indicate 011b when this controller outputs Chirp-K and detects Chirp-JK from the USB host three times. If the connection speed is not fixed to high speed within 2.5 ms after Chirp-K output, these bits indicate 010b.

When the HSE bit is set to 0, these bits indicate 010b when the controller detects a USB bus reset.

A DVST interrupt is generated when the value of the RHST bits is 010b or 011b after the USB bus reset is detected by the controller.

Remote Wakeup (Resume Signal Output) Enable/Disable Bit (WKUP)

With the WKUP bit set to 1, this controller outputs the remote wakeup signal to the USB bus.
This controller controls the output time of a remote wakeup signal. When this bit is set to 1 by software, the controller clears this bit to 0 after outputting the 10-ms K-state.
According to the USB Specifications, the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If this controller writes 1 to this bit right after detection of the suspended state, the K-state will be output after 2 ms.

Do not write 1 to this bit unless the device is in the suspended state (bits DVSQ = 1xxb) and the USB host enables the remote wakeup signal.
When this bit is set to 1, the internal clock must not be stopped even in the suspended state (write 1 to this bit while the SUSPM bit = 1).

32.2.3 Test Mode

32.2.3.1 USB Test Mode Register (TESTMODE)

Address(es): A006 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Value after hardware reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	UTST[3:0]	Test Mode	* See the detailed description below.	R/W	R
b15 to b4	—	Reserved	When writing to these bits, write 0.	R/W	—

Test Mode Bits (UTST)

Writing values to these bits allows this controller to output a USB test signal during high-speed operations. Table 32.6 shows the test mode operations of the controller.

Table 32.6 Test Mode Operations

Test Mode	UTST Settings
Normal operation	0000b
Test_J	0001b
Test_K	0010b
Test_SE0_NAK	0011b
Test_Packet	0100b
Test_Force_Enable	—
Reserved	0101b to 0111b

Write to these bits according to the SetFeature request from the USB host during high-speed communication.
This controller does not enter the suspended state while these bits are 0001h to 0100h.
To perform normal USB communications after the test mode is set, apply a hardware reset.

32.2.4 DMA-FIFO Bus Access Control

The D0FBCFG and D1FBCFG registers control bus access to DMA0-FIFO and DMA1-FIFO, respectively.

32.2.4.1 DMA0-FIFO Bus Configuration Register (D0FBCFG)
DMA1-FIFO Bus Configuration Register (D1FBCFG)

Address(es): D0FBCFG: A006 0010h
D1FBCFG: A006 0012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DFACC[1:0]		—	—	—	—	—	—	—	TENDE	—	—	—	—
Value after hardware reset:	x	x	0	0	x	x	x	x	x	x	x	0	x	x	x	x
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	—	Reserved	When writing to these bits, write 0.	R/W	—
b4	TENDE	TENDx_N Signal Enable	Enables or disables the TENDx_N signal for input. 0: TENDx_N signal is disabled. 1: TENDx_N signal is enabled. Set this bit to 0 when DFACC = 01b or 10b.	R/W	R
b11 to b5	—	Reserved	When writing to these bits, write 0.	R/W	—
b13, b12	DFACC[1:0]	DMAx-FIFO Access Mode	Specify the access mode of the selected FIFO port. b13 b12 00: Cycle stealing mode (value after a reset) 01: 16-byte continuous access mode 10: 32-byte continuous access mode 11: Invalid	R/W	R
b15, b14	—	Reserved	When writing to these bits, write 0.	R/W	—

TENDx_N Input Signal Enable Bit (TENDE)

This bit selects enabling or disabling of the TEND input for write access to a FIFO buffer in DMA mode.
Set this bit to 0 when DFACC = 01b or 10b.

DMA Transfer FIFO Access Mode Select Bits (DFACC)

These bits specify the transfer mode for DMA transfer.

(a) When cycle stealing mode is set, use the DxFIFO port for access to the FIFO buffer.

(b) When 16- or 32-byte continuous access mode is set, use the DxFIFO continuous transfer port for access to the FIFO buffer. The MBW bits of DxFIFOSEL can only be set to 10b (32-bit width).

32.2.5 FIFO Ports

32.2.5.1 CFIFO Port Register (CFIFO)
D0FIFO Port Register (D0FIFO)
D1FIFO Port Register (D1FIFO)

Address(es): CFIFO: A006 0014h
D0FIFO: A006 0018h
D1FIFO: A006 001Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FIFOPORT[31:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[31:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit Name	Description	S/W	H/W
b31 to b0	FIFOPORT [31:0]	FIFO Port	Accessing these bits allows reading the received data from the FIFO buffer or writing the transmit data to the FIFO buffer.	R/W	R/W

- FIFO port control

The transmission/reception buffer of this controller is made up of a FIFO structure (FIFO buffer). Use the FIFO port register for access to the FIFO buffer. There are three FIFO ports: CFIFO, D0FIFO, and D1FIFO ports. Also, there is a DxFIFO continuous transfer port for continuous transfer. Each FIFO port consists of a port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer memory and writing of data to the FIFO buffer memory, a port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that is used to select the pipe assigned to the FIFO port, and a port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR).

The FIFO ports have the following restrictions.

(1) Access to an FIFO buffer for DCP should be through the CFIFO port.
(2) Access to an FIFO buffer by DMA transfer when DFACC = 00b (cycle stealing mode) should be through the DxFIFO port.
(3) Access to an FIFO buffer by DMA transfer when DFACC = 01b or 10b (16-byte or 32-byte continuous access mode) should be through the DxFIFO continuous transfer port.
(4) The DxFIFO ports can also be accessed by the CPU.
(5) When using functions specific to the FIFO port, the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed (when the DMA transfer function is used, etc.).
(6) Registers containing the FIFO port do not affect the other FIFO ports.
(7) Do not assign the same pipe to separate FIFO ports.
(8) In the FIFO buffer state, there are two types of access rights: one assigned to the CPU, and the other to SIE. Access from the CPU is not possible when SIE has the rights to access the FIFO buffer.

FIFO Port Bits (CFIFO, D0FIFO, and D1FIFO)

This controller accesses the FIFO buffer assigned to the pipe number written to the CURPIPE bits of the corresponding select registers (CFIFOSEL, D0FIFOSEL, and D1FIFOSEL) through access to any of these registers by software.

This register can only be accessed when the FRDY bit of each control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) indicates 1 (or while this controller asserts UCL_Dx_DREQ (interrupt sources [43] and [44]) output signals).
The valid bits of this register depend on the settings of the corresponding MBW and BIGEND bits.
Table 32.7 to Table 32.9 list the valid bits.

Table 32.7 Endian Operation in 32-Bit Access (MBW = 10)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	N+3 address	N+2 address	N+1 address	N+0 address
1	N+0 address	N+1 address	N+2 address	N+3 address

Table 32.8 Endian Operation in 16-Bit Access (MBW = 01)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	N+1 address	N+0 address	Writing: Invalid Reading: Prohibited*1	
1	Writing: Invalid Reading: Prohibited*1		N+0 address	N+1 address

Table 32.9 Endian Operation in 8-Bit Access (MBW = 00)

BIGEND	b31 to b24	b23 to b16	b15 to b8	b7 to b0
0	N+0 address	Writing: Invalid Reading: Prohibited*1		
1	Writing: Invalid Reading: Invalid*1			N+0 address

Note 1. Reading data from the invalid bits in a word or byte unit is prohibited.

32.2.5.2 CFIFO Port Select Register (CFIFOSEL)

Address(es): A006 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	MBW[1:0]		—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after hardware reset:	0	0	x	x	0	0	x	0	x	x	0	x	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	CURPIPE [3:0]	FIFO Port Access Pipe Specification	Specify the pipe number to access the CFIFO port. b3 b0 0000: DCP 0001: Pipe 1 0010: Pipe 2 1000: Pipe 8 1001: Pipe 9	R/W	R
b4	—	Reserved	When writing to this bit, write 0.	R/W	—
b5	ISEL	FIFO Port Access Direction when DCP is Selected	Specifies access direction of the FIFO port when DCP is selected in CURPIPE bits. 0: Reading from the buffer memory 1: Writing to the buffer memory	R/W	R
b7, b6	—	Reserved	When writing to these bits, write 0.	R/W	—
b8	BIGEND	FIFO Port Endian Control	Specifies the CFIFO port byte endian. 0: Little endian 1: Big endian	R/W	R
b9	—	Reserved	When writing to this bit, write 0.	R/W	—
b11, b10	MBW[1:0]	CFIFO Port Access Bit Width	Specify the bit width for accessing the CFIFO port. b11b10 00: 8-bit width 01: 16-bit width 10: 32-bit width 11: Setting prohibited	R/W	R
b13, b12	—	Reserved	When writing to these bits, write 0.	R/W	—
b14	REW	Buffer Pointer Rewind	Specifies 1 when rewinding the buffer pointer. This bit is read as 0. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound.	R/W	R
b15	RCNT	Read Count Mode	Specifies the read mode for the value in the DTLN bits in CFIFOCTR. 0: The DTLN bits are cleared when all of the received data has been read from the CFIFO. 1: The DTLN bits are decremented each time the received data is read from the CFIFO.	R/W	R

FIFO Port Access Pipe Specification Bits (CURPIPE)

Write the pipe number for the data to be read or written through the CFIFO port.

When modifying this bit field, write this bit first and then read this bit. Only when the written value matches the read one, proceed to the next process.

Do not specify the same pipe in the CURPIPE bits of the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers.

Even if the setting of these bits is modified during access to the FIFO buffer, the state of the FIFO buffer is retained, with continued access proceeding after these bits are re-set to the value before the modification.

FIFO Port Access Direction Bit when DCP is Selected (ISEL)

To change this bit when the specified pipe is DCP, first write the data to this bit and then read it. Proceed to the next process after checking if the written value matches with the read value.

When the settings of this bit are modified during access to the FIFO buffer, access up to then is saved. Access to the buffer can be continued after rewriting the settings.

Settings in this bit should be made at the same as that of the CURPIPE bits.

FIFO Port Endian Control Bit (BIGEND)

In this bit, set the byte endian for the CFIFO port.
For details, see the description of FIFO Port Bits (CFIFO, D0FIFO, and D1FIFO).

CFIFO Port Access Bit Width Bits (MBW)

In this bit field, set the bit width for accessing the CFIFO port.

When the pipe specified in the CURPIPE bits is in the receiving direction, if reading is started after setting this bit field, do not modify the value of the MBW bits until all data is read.
When the specified pipe is in the receiving direction, modify the value of the CURPIPE bit once and then set the CURPIPE and MBW bits at the same time.
For the procedure for changing the CURPIPE bit, see the description for the same.

When the specified pipe is in the transmitting direction, to switch the bit width from 8 bits to 16 or 32 bits, or from 16 bits to 32 bits is not allowed while writing to the buffer memory is in progress.
With the 16-bit or 32-bit width setting, writing to odd bytes is possible by exercising byte access control.

Buffer Pointer Rewind (REW)

When the selected pipe is in the receiving direction, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double-buffer operation, re-reading the currently-read FIFO buffer plane from the first data is allowed).

Do not set REW to 1 simultaneously with modifying the CURPIPE bits. Before setting REW to 1, be sure to check that FRDY is 1.

To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

Read Count Mode (RCNT)

When 0 is written to this bit, if all received data of the FIFO buffer assigned to the pipe specified in the CURPIPE bits (selected pipe) is read (when the data is read on one side of a double buffer), this controller clears the DTLN bits in the CFIFOCTR register to 0.

When 1 is written to this bit, the controller decrements the value of the DTLN bits in the CFIFOCTR register whenever the received data is read from the FIFO buffer assigned to the specified pipe.

32.2.5.3 D0FIFO Port Select Register (D0FIFOSEL)
D1FIFO Port Select Register (D1FIFOSEL)

Address(es): D0FIFOSEL: A006 0028h
D1FIFOSEL: A006 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after hardware reset:	0	0	0	0	0	0	x	0	x	x	x	x	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	CURPIPE [3:0]	FIFO Port Access Pipe Specification	b3 b0 0000: Not specified 0001: Pipe 1 0010: Pipe 2 1000: Pipe 8 1001: Pipe 9	R/W	R
b7 to b4	—	Reserved	When writing to these bits, write 0.	R/W	—
b8	BIGEND	FIFO Port Endian Control	Specifies the CFIFO port byte endian. 0: Little endian 1: Big endian	R/W	R
b9	—	Reserved	When writing to this bit, write 0.	R/W	—
b11, b10	MBW[1:0]	FIFO Port Access Bit Width	Specify the bit width for accessing the FIFO port. b11b10 00: 8-bit width 01: 16-bit width 10: 32-bit width 11: Setting prohibited	R/W	R
b12	DREQE	UCL_Dx_DREQ Signal Output Enable	Enables or disables the output of the UCL_Dx_DREQ (interrupt sources [43] and [44]) signals. 0: Output is disabled 1: Output is enabled	R/W	R
b13	DCLRM	Auto Buffer Memory Clear Mode after Specified Pipe Data is Read	Enables or disables automatic clearing of the buffer memory after data has been read out using the selected pipe. 0: Auto buffer clear mode is disabled 1: Auto buffer clear mode is enabled	R/W	R
b14	REW	Buffer Pointer Rewind	Specifies 1 when rewinding the buffer pointer. This bit is read as 0. 0: The buffer pointer is not rewound 1: The buffer pointer is rewound	R/W	R
b15	RCNT	Read Count Mode	Specifies the read mode for the value in the DTLN bits in Dx_FIFOCTR. 0: The DTLN bits are cleared when all of the received data has been read. 1: The DTLN bits are decremented each time the received data is read.	R/W	R

FIFO Port Access Pipe Specification Bits (CURPIPE)

Write the pipe number for the data to be read or written through the DxFIFO port.

When modifying this bit field, first write a value to this bit field and then read it. Check if the write value matches the read value and then proceed to the next process.

Do not specify the same pipe in the CURPIPE bits of the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers.

Even if the setting of these bits is modified during access to the FIFO buffer, the state of the FIFO buffer is retained, with continued access proceeding after these bits are re-set to the value before the modification.

DxFIFO Port Byte Endian Control Bit (BIGEND)

Write the byte endian for the DxFIFO port in this bit.
For details, see the description of FIFO Port Bits (CFIFO, D0FIFO, and D1FIFO).

DxFIFO Port Access Bit Width (MBW)

Write the bit width for accessing the DxFIFO port in this bit.

When the pipe specified in the CURPIPE bits is in the receiving direction, if reading is started after setting this bit field, do not modify the value of the MBW bits until all data is read.
When the specified pipe is in the receiving direction, set the CURPIPE and MBW bits at the same time.
For the procedure for changing the CURPIPE bit, see the description for the same.

For details, see the description of FIFO Port Access Pipe Specification Bits (CURPIPE).

UCL_Dx_DREQ Output Disable/Enable Bit (DREQE)

Use this bit to enable or disable the output of the UCL_Dx_DREQ signals.

When enabling the output of the UCL_Dx_DREQ signals, set this bit to 1 after setting the CURPIPE bits.

When modifying the setting of the CURPIPE bits, do so after setting this bit to 0.

Auto FIFO Buffer Clear Disable/Enable Bit (DCLRM)

After reading data in the specified pipe, disable or enable automatic clearing of the FIFO buffer. When 1 is written to this bit, this controller sets the BCLR bit to 1 for a FIFO buffer if a zero-length packet is received when the FIFO buffer assigned to the specified pipe is empty, or when a short packet is received and the data is completely read while BFRE = 1 .

When using this controller with the BRDYM bit set to 1, be sure to set this bit to 0.

Buffer Pointer Rewind (REW)

When the selected pipe is in the receiving direction, setting the REW bit to 1 while the FIFO buffer is being read allows re-reading the FIFO buffer from the first data (in double-buffer operation, re-reading the currently-read FIFO buffer plane from the first data is allowed).

Do not set the REW bit to 1 simultaneously with modifying the CURPIPE bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.
To re-write to the FIFO buffer again from the first data for the pipe in the transmitting direction, use the BCLR bit.

Read Count Mode (RCNT)

When 0 is written to this bit, if all received data of the FIFO buffer assigned to the pipe specified in the CURPIPE bits (selected pipe) is read (when the data is read on one side of a double buffer), this controller clears the DTLN bits in the DxFIFOCTR register to 0.

When 1 is written to this bit, the controller decrements the value of the DTLN bits in the DxFIFOCTR register whenever the received data is read from the FIFO buffer assigned to the specified pipe.

32.2.5.4 CFIFO Port Control Register (CFIFOCTR)
D0FIFO Port Control Register (D0FIFOCTR)
D1FIFO Port Control Register (D1FIFOCTR)

Address(es): CFIFOCTR: A006 0022h
D0FIFOCTR: A006 002Ah
D1FIFOCTR: A006 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Value after hardware reset:	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b11 to b0	DTLN[11:0]	Receive Data Length	Indicate the length of the receive data.	R	W
b12	—	Reserved	When writing to this bit, write 0.	R/W	—
b13	FRDY	FIFO Port Ready	Indicates whether the FIFO port can be accessed. 0: FIFO port is not accessible. 1: FIFO port is accessible.	R	W
b14	BCLR	CPU Buffer Clear	Specifies 1 to clear the FIFO buffer on the CPU side for the selected pipe. Only 1 can be written to this bit. This bit is read as 0. 0: Invalid 1: Clears the CPU buffer memory on the CPU side.	R/W	R
b15	BVAL	Buffer Memory Valid Flag	Specifies 1 when writing has ended in the CPU-side FIFO buffer for the pipe specified in CURPIPE (selected pipe). Only 1 can be written to this bit. 0: Invalid 1: Writing ended	R/W	R/W

Receive Data Length Bits (DTLN)

The DTLN bits indicate the length of the receive data. While the FIFO buffer is being read, the DTLN bits indicate different values depending on the RCNT bit value as described below.

(1) When RCNT = 0:
The length of received data is set in these bits, and the value is retained until all received data has been read from a single FIFO buffer plane.
While BFRE is 1, these bits retain the length of the receive data until BCLR is set to 1 even after all data has been read.

(2) When RCNT = 1:
This controller decrements the value indicated by these bits each time data is read from the FIFO buffer.
(The value is decremented by 1 when MBW is 00, by 2 when MBW is 01b, and by 4 when MBW is 10b.)

This controller sets these bits to 0 when all data has been read from one FIFO buffer plane. However, in double-buffer operation, if data has been received in one FIFO buffer plane before all data has been read from the other plane, this controller sets these bits to indicate the length of the receive data in the latter plane when all data has been read from the former plane.

When reading these bits during FIFO buffer reading while RCNT = 1, note that these bits are updated within 150 ns after a read cycle for the FIFO port.

FIFO Port Ready Bit (FRDY)

This bit indicates whether the FIFO port can be accessed from the CPU (DMAC).

In the following cases, the controller sets FRDY to 1, but data cannot be read via the FIFO port because there is no data to be read. In these cases, set BCLR to 1, clear the FIFO buffer, and then enable transmission and reception of the next data.

(1) A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty.
(2) A short packet is received and the data is completely read while BFRE is 1.

CPU Buffer Clear Bit (BCLR)

When this bit is set to 1, this controller clears the FIFO buffer on the CPU for the selected pipe.

When double-buffer operation is set for the FIFO buffer assigned to the selected pipe, this controller clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the selected pipe is the DCP, setting BCLR to 1 allows this controller to clear the FIFO buffer regardless of whether the FIFO buffer is on the CPU side or SIE side. When clearing the buffer on the SIE side, set the PID bits for the DCP to NAK before setting BCLR to 1.

When the selected pipe is not the DCP, writing 1 to this bit should be done while FRDY indicates 1. When checking the FRDY bit after executing BCLR, allow an interval of at least 80 ns after executing BCLR before referencing FRDY.

Buffer Memory Valid Flag (BVAL)

When the pipe specified in the CURPIPE bits (selected pipe) is for transmission, write 1 to this bit in the following cases. This controller sets the FIFO buffer from the CPU side to the SIE side, enabling transmission.

(1) To transmit the short packet, set this bit to 1 after data has been written.
(2) To transmit a zero-length packet, set this bit to 1 before writing data to FIFO.
(3) Set this bit to 1 after the number of data bytes has been written for the pipe in continuous transfer mode, where the number is a natural integral multiple of the maximum packet size and less than the buffer size.

When the data of the maximum packet size has been written for the pipe in non-continuous transfer mode, this controller sets this bit to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When 1 is written to the BVAL and BCLR bits at the same time when the specified pipe is in the transmitting direction, the controller clears the old data and enables the transmission of a zero-length packet.

Writing 1 to this bit should be done while FRDY indicates 1. When checking the FRDY bit after executing BVAL, allow an interval of at least 80 ns after executing BVAL before referencing FRDY.

When the specified pipe is in the receiving direction, do not write 1 to this bit.

32.2.6 Enabling Interrupts

32.2.6.1 Interrupt Enable Register 0 (INTENB0)

Address(es): A006 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after hardware reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b7 to b0	—	Reserved	When writing to these bits, write 0.	R/W	—
b8	BRDYE	Buffer Ready Interrupt Enable	Enables or disables the USB interrupt output when the BRDY interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	Enables or disables the USB interrupt output when the NRDY interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b10	BEMPE	Buffer Empty Interrupt Enable	Enables or disables the USB interrupt output when the BEMP interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b11	CTRE	Control Transfer Stage Transition Interrupt Enable	Enables or disables the USB interrupt output when the CTRT interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b12	DVSE	Device State Transition Interrupt Enable	Enables or disables the USB interrupt output when the DVST interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b13	SOFE	Frame Number Update Interrupt Enable	Enables or disables the USB interrupt output when the SOF interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b14	RSME	Resume Interrupt Enable	Enables or disables the USB interrupt output when the RESM interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b15	VBSE	VBUS Interrupt Enable	Enables or disables the USB interrupt output when the VBINT interrupt is detected. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R

32.2.6.2 BRDY Interrupt Enable Register (BRDYENB)

Address(es): A006 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDYE[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPEBRDYE [9:0]	BRDY Interrupt Enable for Each Pipe	Enable or disable the BRDY interrupt for each pipe. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note: The bit number corresponds to the pipe number.

BRDY Interrupt Enable Bit for Each Pipe (PIPEBRDYE)

On detecting the BRDY interrupt for the pipe corresponding to the bit in this register which has been set to 1 by software, this controller sets 1 to the corresponding PIPEBRDY bit in BRDYSTS and the BRDY bit in INTSTS0, and asserts the interrupt signal through the INT_N (interrupt source [42]) pin.

While at least one PIPEBRDY bit in BRDYSTS indicates 1, this controller asserts the interrupt signal through the INT_N pin when the corresponding interrupt enable bit of this register is changed from 0 to 1 by software.

32.2.6.3 NRDY Interrupt Enable Register (NRDYENB)

Address(es): A006 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDYE[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPENRDYE [9:0]	NRDY Interrupt Enable for Each Pipe	Enable or disable the NRDY interrupt for each pipe. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note: The bit number corresponds to the pipe number.

NRDY Interrupt Enable Bit for Each Pipe (PIPENRDYE)

On detecting the NRDY interrupt for the pipe corresponding to the bit in this register which has been set to 1 by software, this controller sets 1 to the corresponding PIPENRDY bit in NRDYSTS and the NRDY bit in INTSTS0, and asserts the interrupt signal through the INT_N pin.

While at least one PIPENRDY bit in NRDYSTS indicates 1, this controller asserts the interrupt signal through the INT_N pin when the corresponding interrupt enable bit of this register is changed from 0 to 1 by software.

32.2.6.4 BEMP Interrupt Enable Register (BEMPENB)

Address(es): A006 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMPE[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPEBEMPE [9:0]	BEMP Interrupt Enable for Each Pipe	Enable or disable the BEMP interrupt for each pipe. 0: Interrupt output disabled 1: Interrupt output enabled	R/W	R
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note: The bit number corresponds to the pipe number.

BEMP Interrupt Enable Bit for Each Pipe (PIPEBEMPE)

On detecting the BEMP interrupt for the pipe corresponding to the bit in this register which has been set to 1 by software, this controller sets 1 to the corresponding PIPEBEMP bit in BEMPSTS and the BEMP bit in INTSTS0, and asserts the interrupt signal through the INT_N pin.

While at least one PIPEBEMP bit in BEMPSTS indicates 1, this controller asserts the interrupt signal through the INT_N pin when the corresponding interrupt enable bit of this register is changed from 0 to 1 by software.

32.2.7 SOF Control Register

32.2.7.1 SOF Pin Configuration Register (SOFCFG)

Address(es): A006 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	BRDYM	INTL	EDGESTS	—	—	—	—
Value after hardware reset:	x	x	x	x	x	x	x	0	x	0	0	0	0	0	x	x
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	—	Reserved	When writing to these bits, write 0.	R/W	—
b4	EDGESTS	Interrupt Edge Processing Status	Indicates the state of processing in response to interrupts when edge-sensing has been selected. 0: Processing in response to an edge-sensed interrupt is not in progress. 1: Processing in response to an edge-sensed interrupt is in progress	R	W
b5	INTL	Interrupt Output Sense Select	Selects sense mode for USB interrupt output. 0: Edge sense 1: Level sense	R/W	R
b6	BRDYM	PIPEBRDY Interrupt Status Clear Timing	Specifies the timing for clearing the PIPEBRDY interrupt state. 0: Software clears the state. 1: Hardware clears the state by reading from the FIFO buffer or by writing to the FIFO buffer This bit can be set only in the initial setting (before communications). The setting cannot be changed once communication starts.	R/W	R
b15 to b7	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. When setting the BRDYM bit to 1, set the INTL bit to 1 (level sense).
Note 2. With the INTL bit set to 0, to stop the system clock (SUSPM = 0) after clearing the interrupt state, write 0 to the SUSPM bit after checking that the EDGESTS bit is set to 0.

32.2.8 Interrupt Status

32.2.8.1 Interrupt Status Register 0 (INTSTS0)

Address(es): A006 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after hardware reset:	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	1	x	x	x	x	x	0	0	1	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	Indicate the control transfer stage. b2 b0 000: Idle or setup stage 001: Control read data stage 010: Control read status stage 011: Control write data stage 100: Control write status stage 101: Control write (no data) status stage 110: Control transfer sequence error 111: Reserved	R	W
b3	VALID	USB Request Reception	Indicates whether reception of the USB request has been detected. When writing to this bit, only 0 can be written. 0: Not detected 1: Setup packet reception	R/W	W
b6 to b4	DVSQ[2:0]	Device State	Indicate the device state. b6 b4 000: Powered state 001: Default state 010: Address state 011: Configured state 1xx: Suspended state	R	W
b7	VBSTS	VBUS Input Status	Indicates the input state of the VBUS pin. 0: VBUS pin is at the low level 1: VBUS pin is at the high level	R	W
b8	BRDY	BRDY Interrupt Status	Indicates the BRDY interrupt state. 0: BRDY interrupts not generated 1: BRDY interrupts generated	R	W
b9	NRDY	NRDY Interrupt Status	Indicates the NRDY interrupt state. 0: NRDY interrupts not generated 1: NRDY interrupts generated	R	W
b10	BEMP	BEMP Interrupt Status	Indicates the BEMP interrupt state. 0: BEMP interrupts not generated 1: BEMP interrupts generated	R	W
b11	CTRT	Control Transfer Stage Transition Interrupt Status	Indicates the control transfer stage transition interrupt state. When writing to this bit, only 0 can be written. 0: Control transfer stage transition interrupts not generated 1: Control transfer stage transition interrupts generated	R/W	W
b12	DVST	Device State Transition Interrupt Status	Indicates the device state transition interrupt state. When writing to this bit, only 0 can be written. 0: Device state transition interrupts not generated 1: Device state transition interrupts generated	R/W	W

Bit	Symbol	Bit Name	Description	S/W	H/W
b13	SOFR	Frame Number Update Interrupt Status	Indicates the frame number update interrupt state. When writing to this bit, only 0 can be written. 0: SOF interrupts not generated 1: SOF interrupts generated	R/W	W
b14	RESM	Resume Interrupt Status	Indicates the resume detection interrupt state. When writing to this bit, only 0 can be written. 0: Resume interrupts not generated 1: Resume interrupts generated	R/W	W
b15	VBINT	VBUS Change Detect Interrupt Status	Indicates the VBUS change detection interrupt state. When writing to this bit, only 0 can be written. 0: VBUS interrupts not generated 1: VBUS interrupts generated	R/W	W

Note 1. To clear the state indicated by the VBINT, RESM, SOFR, DVST, or CTRT bits, write 0 only to the bit to be cleared, and write 1 to the other bits. Do not write 0 to the status bit set to 0.
Note 2. The controller detects the change in state indicated by the VBINT and RESM bits of this register, even while the clock is being stopped (SUSPM = 0), and conveys the interrupt if the corresponding interrupt is enabled. When the clock is enabled, clear the state using software.

Buffer Ready Interrupt Status Bit (BRDY)

This controller sets a BRDY bit to 1 when, among the PIPEBRDY bits for which the corresponding PIPEBRDYE bits in BRDYENB have been set to 1, at least one PIPEBRDY bit in BRDYSTS is set to 1 (that is, when this controller detects the BRDY interrupt state in at least one pipe among the pipes for which software has enabled the output of BRDY interrupts).

For the conditions for the setting of PIPEBRDY bits, refer to the description of the BRDYSTS register.

When a BRDY bit has been set to 1, the controller clears the bit in response to software writing 0 to all PIPEBRDY bits corresponding to PIPEBRDYE bits which have been set to 1.
A BRDY bit will not be cleared to 0 in response to software only writing 0 to individual bits that have been set to 1.

Buffer Not Ready Interrupt Status Bit (NRDY)

This controller sets an NRDY bit to 1 when, among the PIPEBRDY bits for which the corresponding PIPENRDYE bits in NRDYENB have been set to 1, at least one PIPENRDY bit in BNRDYSTS is set to 1 (that is, when this controller detects the NRDY interrupt state in at least one pipe among the pipes for which software has enabled the output of NRDY interrupts).

For the conditions for the setting of PIPENRDY bits, refer to the description of the NRDYSTS register.

When an NRDY bit has been set to 1, the controller clears the bit in response to software writing 0 to all PIPENRDY bits corresponding to PIPENRDYE bits which have been set to 1.
An NRDY bit will not be cleared to 0 in response to software only writing 0 to individual bits that have been set to 1.

Buffer Empty Interrupt Status Bit (BEMP)

This controller sets a BEMP bit to 1 when, among the PIPEBRDY bits for which the corresponding PIPEBEMPE bits in BEMPENB have been set to 1, at least one PIPEBEMP bit in BEMPSTS is set to 1 (that is, when this controller detects the BEMP interrupt state in at least one pipe among the pipes for which software has enabled the output of BEMP interrupts).

For the conditions for the setting of PIPEBEMP bits, refer to the description of the BEMPSTS register.

When a BEMP bit has been set to 1, the controller clears the bit in response to software writing 0 to all PIPEBEMP bits corresponding to PIPEBEMPE bits which have been set to 1.
A BEMP bit will not be cleared to 0 in response to software only writing 0 to individual bits that have been set to 1.

Control Transfer Stage Transition Interrupt Status Bit (CTRT)

If this controller detects the stage transition of control transfer, it updates the CTSQ value and sets 1 to this bit.

When this interrupt occurs, clear the state before the controller detects the next control transfer stage transition.

Device State Transition Interrupt Status Bit (DVST)

If this controller detects a change in the device state, it updates the DVSQ value and sets 1 to this bit.

When this interrupt occurs, clear the state before the controller detects the next device state transition.

Frame Number Update Interrupt Status Bit (SOFR)

The conditions when the controller sets 1 in this bit are below.
When updating the frame number, this controller sets 1 to this bit (this interrupt is detected every 1 ms).
The controller detects the SOFR interrupt by internal interpolation even if the SOF packet from the USB host is corrupted.

Resume Interrupt Status Bit (RESM)

If this controller is in the suspended state (DVSQ = 1xxb) and the DP pin falling edge is detected, 1 is set to this bit.

VBUS Change Interrupt Status Bit (VBINT)

When this controller detects a change in the VBUS pin input value (from high to low and from low to high), 1 is written to this bit. The controller writes the input value of the VBUS pin to the VBSTS bit. When the VBINT interrupt occurs, use the software to execute a consistency check several times during reading the VBSTS bit, and remove the chattering effect.

32.2.8.2 BRDY Interrupt Status Register (BRDYSTS)

Address(es): A006 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDY[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPEBRDY [9:0]	BRDY Interrupt Status for Each Pipe	Indicate the BRDY interrupt state for each pipe. When writing to these bits, only 0 can be written. 0: Interrupts not generated 1: Interrupts generated	R/W	W
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. The bit number corresponds to the pipe number.
Note 2. When BRDYM = 0, to clear the state of each bit of this register, write 0 only to the bit to be cleared and 1 to other bits.
Note 3. When BRDYM = 0, clearing these interrupt status bits should be done before accessing the FIFO.

BRDY Interrupt Status Bit for Each Pipe (PIPEBRDY)

When the BRDY interrupt is detected for a pipe by this controller, the controller sets 1 in the corresponding PIPEBRDY bit of the BRDYSTS register. Here, when 1 is written to the corresponding bit of BRDYENB register by using the software, the controller sets 1 to the BRDY bit of the INTSTS0 register.

The conditions for generating and clearing the BRDY interrupt depend on the settings of the SOFCFG.BRDYM bit and PIPECFG.BFRE bit for each pipe as described below.

- When BRDYM = 0 and BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.
On any of the following conditions, this controller generates the internal BRDY interrupt request trigger and sets 1 to the PIPEBRDY bit corresponding to the selected pipe.

(1) For the pipe in the transmitting direction
  (a) When the software has modified the DIR bit from 0 to 1
  (b) When the controller ends the packet transmission of the selected pipe in the condition where writing is not possible from the CPU to the FIFO buffer that has been assigned to the selected pipe (when the BSTS bit is read as 0).
  In continuous transmission/reception mode, the request trigger is generated when data of one plane of the FIFO buffer is complete.
  (c) In double-buffer operation, one FIFO buffer being empty on completion of the writing of data to the other FIFO buffer.
  The request trigger is not generated until completion of writing data to the currently-written FIFO buffer plane even if transmission to the other FIFO buffer is completed.
  (d) When the hardware flushes the buffer of the pipe for isochronous transfers.

(e) The FIFO buffer making the transition from the write-disabled to the write-enabled state in response to writing of 1 to the ACLRM bit.
The request trigger is not generated for the DCP (that is, during data transmission for control transfers).

(2) For the pipe in the receiving direction

(a) When packet reception is completed successfully thus enabling the FIFO buffer to be read when read-access from the CPU to the FIFO buffer for the selected pipe is disabled (when the BSTS bit is read as 0).
The request trigger is not generated for the transaction in which DATA-PID disagreement occurs.
When a short packet is received, the request trigger is generated even if the FIFO buffer has available space.
When the transaction counter is used, the request trigger is generated on receiving the specified number of packets.
In this case, the request trigger is generated even if the FIFO buffer has available space.

(b) In double-buffer operation, one FIFO buffer being ready for reading on completion of the reading of data from the other FIFO buffer.
The request trigger is not generated until completion of reading data from the currently-read FIFO buffer plane even if reception by the other FIFO buffer is completed.
The BRDY interrupt is not generated in the status stage of control transfers.
The PIPEBRDY interrupt state of the selected pipe can be cleared to 0 by writing 0 to the corresponding PIPEBRDY interrupt status bit in the BRDYSTS register. In this case, 1s should be written to the PIPEBRDY interrupt status bits for the other pipes.
Be sure to clear the BRDY state before accessing the FIFO buffer.

- When BRDYM = 0 and BFRE = 1

With these settings, this controller generates the BRDY interrupt on completion of the reading of all data for a single transfer using the pipe in the receiving direction, and sets 1 to the PIPEBRDY bit corresponding to the selected pipe.

On any of the following conditions, this controller determines that the last data for a single transfer has been received.

(1) When a short packet including a zero-length packet is received.

(2) When the transaction counter register (TRNCNT bits) is used and the number of packets specified by the TRNCNT bits is completely received.

When the pertinent data is completely read out after any of the above determination conditions has been satisfied, this controller determines that all data for a single transfer has been completely read out.

When a zero-length packet is received when the FIFO buffer is empty, the controller determines that all data for a single transfer has been completely read out upon the FRDY and the DTLN bits of the FIFO port control register are set to 1 and 0, respectively.
In this case, write 1 to the BCLR bit of the corresponding FIFOCTR register by software to start the next transfer.

With these settings, this controller does not detect the BRDY interrupt for the pipe in the transmitting direction.

The PIPEBRDY interrupt state of the selected pipe can be cleared to 0 by writing 0 to the corresponding PIPEBRDY interrupt status bit. In this case, 1s should be written to the PIPEBRDY interrupt status bits for the other pipes.

In this mode, the BFRE bit setting should not be modified until all data for a single transfer has been processed.
When it is necessary to modify the BFRE bit before completion of processing, all the FIFO buffers for the selected pipe should be cleared using the ACLRM bit.

- When BRDYM = 1 and BFRE = 0

With these settings, the PIPEBRDY values are linked to the BSTS bit settings for each pipe. In other words, the BRDY interrupt status bits (PIPEBRDY) are set to 1 or 0 by this controller depending on the FIFO buffer state.

(1) For the pipe in the transmitting direction
The setting of a BRDY interrupt status bit is 1 while the port register of the corresponding FIFO buffer is ready for written data and 0 when it is not able to accept written data.
However, the BRDY interrupt is not generated in response to setting of the bit to 1 if writing to the DCP in the transmitting direction can proceed.

(2) For the pipe in the receiving direction
The setting of a BRDY interrupt status bit is 1 while the port register of the FIFO buffer is ready for reading and 0 when all data have been read.

When a zero-length packet is received when the FIFO buffer is empty, the corresponding bit is set to 1 and the BRDY interrupt continues to be effective until 1 is written to BCLR.

With this setting, the PIPEBRDY bit cannot be cleared to 0.

When BRDYM is set to 1, all of the BFRE bits (for all pipes) should be cleared to 0.
When BRDYM is set to 1, the INTL bit should be set to 1 (level control).

32.2.8.3 NRDY Interrupt Status Register (NRDYSTS)

Address(es): A006 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDY[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPENRDY [9:0]	NRDY Interrupt Status for Each Pipe	Indicate the NRDY interrupt state for each pipe. When writing to these bits, only 0 can be written. 0: Interrupts not generated 1: Interrupts generated	R/W	W
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. The bit number corresponds to the pipe number.
Note 2. To clear the state indicated by each bit of this register, write 0 only to the bit to be cleared and 1 to the other bits.

NRDY Interrupt Status Bit for Each Pipe (PIPENRDY)

On generating the internal NRDY interrupt request for the pipe whose PID bits are set to BUF, this controller sets the corresponding PIPENRDY bit in NRDYSTS in the register to 1. If the corresponding bit in the NRDYENB register is set to 1, this controller sets the NRDY bit in INTSTS0 in the register to 1.
The conditions on which this controller generates the internal NRDY interrupt request for a given pipe are described below.
However, the internal NRDY interrupt request is not generated during status stage execution of the control transfer.

(1) When the pipe is in the transmitting direction
  (a) When an IN Token is received while there is no transmission data in the FIFO buffer and the corresponding PIPE PID bit is set to BUF (01):
  In this case, this controller generates an NRDY interrupt request at the reception of the IN token, setting the PIPENRDY bit to 1.
  For the pipe for the isochronous transfers in which an interrupt is generated, this controller transmits a zero-length packet, setting the OVRN bit to 1.

(2) For the pipe in the receiving direction

(a) When the PID bits for the corresponding pipe are set to BUF (01) and an OUT token is received while there is no open space in the FIFO buffer:
For the pipe for the isochronous transfers in which an interrupt is generated, this controller generates an NRDY interrupt request at the reception of the OUT token, setting the PIPENRDY bit to 1 and OVRN bit to 1.
For the pipe for the transfers other than isochronous transfers in which an interrupt is generated, this controller generates an NRDY interrupt request when an NAK handshake is transferred after the data following the OUT token was received, setting the PIPENRDY bit to 1.
However, during re-transmission (due to DATA-PID disagreement), the NRDY interrupt request is not generated. In addition, if an error occurs in the DATA packet, the NRDY interrupt request is not generated.

(b) When the PID bits for the corresponding pipe are set to BUF (01) and a PING token is received while there is no open space in the FIFO buffer:
In this case, this controller generates an NRDY interrupt request at the reception of the PING token, setting the PIPENRDY bit to 1.

(c) In an isochronous transfer pipe, when the PID bits are set to BUF (01) and data is not received successfully within the interval frame:
In this case, this controller generates an NRDY interrupt request at the reception of an SOF, and sets the PIPENRDY bit to 1.

32.2.8.4 BEMP Interrupt Status Register (BEMPSTS)

Address(es): A006 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMP[9:0]									
Value after hardware reset:	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b9 to b0	PIPEBEMP [9:0]	BEMP Interrupt Status for Each Pipe	Indicate the BEMP interrupt state for each pipe. When writing to these bits, only 0 can be written. 0: Interrupts not generated 1: Interrupts generated	R/W	W
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. The bit number corresponds to the pipe number.
Note 2. To clear the state indicated by each bit of this register, write 0 only to the bit to be cleared and 1 to the other bits.

BEMP Interrupt Status Bit for Each Pipe (PIPEBEMP)

On detecting the BEMP interrupt for the pipe whose PID bits are set to BUF by software, this controller sets the corresponding PIPEBEMP bit in BEMPSTS to 1. If the corresponding bit in BEMPENB is set to 1 by software, this controller sets the BEMP bit in INTSTS0 to 1.

The following describes the conditions on which this controller generates the internal BEMP interrupt request.

(1) For the pipe in the transmitting direction, when the FIFO buffer of the corresponding pipe is empty on completion of transmission (including zero-length packet transmission).
In single-buffer operation, the internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for the pipe other than DCP.
However, the internal BEMP interrupt request is not generated on any of the following conditions.
  (a) When writing data to the FIFO buffer on the CPU (DMAC) side is started by software on completion of transmitting data of one plane in double-buffer operation.
  (b) When the buffer is cleared (emptied) by setting the ACLRM or BCLR bit to 1.
  (c) When IN transfer (zero-length packet transmission) is performed during the control transfer status stage.

(2) For the pipe in the receiving direction
When the successfully-received data packet size exceeds the specified maximum packet size.
In this case, this controller generates the BEMP interrupt request, setting the corresponding PIPEBEMP bit to 1, and discards the received data and modifies the setting of the PID bits of the corresponding pipe to STALL (11).
However, the internal BEMP interrupt request is not generated on any of the following conditions.
  (a) When a CRC error or bit stuffing error is detected in the received data.
  (b) When a setup transaction is being performed.

Writing 0 to the PIPEBEMP bit clears the state; writing 1 to the PIPEBEMP bit has no effect.

32.2.9 Frame Number Registers

32.2.9.1 Frame Number Register (FRMNUM)

Address(es): A006 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after hardware reset:	0	0	x	x	x	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b10 to b0	FRNM[10:0]	Frame Number	Indicate the latest frame number.	R	W
b13 to b11	—	Reserved	When writing to these bits, write 0.	R/W	—
b14	CRCE	CRC Error Detection Status	Indicates whether a CRC error has been detected in the pipe during isochronous transfer. When writing to this bit, only 0 can be written. 0: No error 1: An error occurred.	R/W	W
b15	OVRN	Overrun/Underrun Detection Status	Indicates whether an overrun/underrun error has been detected in the pipe during isochronous transfer. When writing to this bit, only 0 can be written. 0: No error 1: An error occurred.	R/W	W

Note 1. The OVRN bit is for use in debugging. When designing a system, control the timing so that neither overrun nor underrun occurs.

Frame Number Bits (FRNM)

This controller sets these bits to indicate the latest frame number, which is updated every time an SOF packet is issued or received (every 1 ms).

When reading these bits by software, repeat reading until the same value is read twice.

CRC Error Detection Status Bit (CRCE)

In an isochronous transfer pipe, this controller sets 1 to this bit when a CRC error or bit stuffing error has been detected.

This bit can be cleared by writing 0 to it by software. In this case, write 80h when OVRN is not to be cleared at the same time.

This controller generates an internal NRDY interrupt request when it detects a CRC error. For details, see NRDY Interrupt Enable Bit for Each Pipe (PIPENRDYE).

Overrun/Underrun Detection Status Bit (OVRN)

For the isochronous transfer pipe, this controller sets 1 to this bit when an overrun/underrun is detected.
When an overrun/underrun is detected, the controller issues an internal NRDY request. Refer to NRDY Interrupt Enable Bit for Each Pipe (PIPENRDYE) for details.

This bit can be cleared writing 0 to it by software. In this case, write 40h when CRCE is not to be cleared at the same time.

This controller sets this bit to 1 on any of the following conditions.

(1) For the isochronous transfer pipe in the transmitting direction, the IN token is received before all the transmit data has been written to the FIFO buffer.
(2) For the isochronous transfer pipe in the receiving direction, the OUT token is received when no FIFO buffer planes are empty.

32.2.9.2 µFrame Number Register (UFRMNUM)

Address(es): A006 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
Value after hardware reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b2 to b0	UFRNM[2:0]	Microframe Number	Indicate the µframe number.	R	W
b15 to b3	—	Reserved	These bits are read as an undefined value.	R	—

Microframe Number Bits (UFRNM)

This controller sets these bits to indicate the µframe number during high-speed operation. During operation other than high-speed operation, this controller sets these bits to 00h.

When reading these bits, repeat reading until the same value is read twice.

32.2.10 USB Address

32.2.10.1 USB Address Register (USBADDR)

Address(es): A006 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	USBADDR[6:0]						
Value after hardware reset:	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b6 to b0	USBADDR [6:0]	USB Address	Indicate the USB address assigned by the host.	R	R/W
b15 to b7	—	Reserved	These bits are read as an undefined value.	R	—

USB Address Bits (USBADDR)

These bits indicate the USB address assigned by the host when the SetAddress request is successfully processed.
If a USB bus reset is detected by the controller, 00h is set to this bit.

32.2.11 USB Request Registers

The USB request registers are used to store the setup requests for control transfers. The values of the USB request that have been received are stored.

32.2.11.1 USB Request Type Register (USBREQ)

Address(es): A006 0054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	bRequest[7:0]								bmRequestType[7:0]							
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b7 to b0	bmRequestType [7:0]	Request Type	USB request bmRequestType value	R	W
b15 to b8	bRequest[7:0]	Request	USB request bRequest value	R	W

USB Request Type Bits (bmRequestType)

These bits indicate the USB request data value received by this controller in the setup transaction. Writing to these bits by software has no effect.

USB Request Bits (bRequest)

These bits indicate the USB request data value received by this controller in the setup transaction. Writing to these bits by software has no effect.

32.2.11.2 USB Request Value Register (USBVAL)

Address(es): A006 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	wValue[15:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b15 to b0	wValue[15:0]	Value	USB request wValue value	R	W

Value Bits (wValue)

These bits are used to read the value of the USB request wValue. Bits 7 to 0 are lower-order byte.

These bits indicate the USB request wValue value received by this controller in the setup transaction. Writing to these bits by software has no effect.

32.2.11.3 USB Request Index Register (USBINDX)

Address(es): A006 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	wIndex[15:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b15 to b0	wIndex[15:0]	Index	USB request wIndex value	R	W

Index Bits (wIndex)

These bits are used to read the value of the USB request wIndex. Bits 7 to 0 are lower-order byte.

These bits indicate the USB request wIndex value received by this controller in the setup transaction. Writing to these bits by software has no effect.

32.2.11.4 USB Request Length Register (USBLENG)

Address(es): A006 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	wLength[15:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b15 to b0	wLength [15:0]	Length	USB request wLength value	R	W

Length Bit (wLength)

These bits are used to read the value of the USB request wLength. Bits 7 to 0 are lower-order byte.

These bits indicate the USB request wLength value received in setup transaction by the controller. Writing to these bits by software has no effect.

32.2.12 DCP Configuration

32.2.12.1 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): A006 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	MXPS[6:0]						
Value after hardware reset:	0	0	0	0	x	x	x	x	x	1	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b6 to b0	MXPS[6:0]	Maximum Packet Size	Specify the maximum data payload (maximum packet size) for the DCP.	R	R/W
b15 to b7	—	Reserved	These bits are read as an undefined value.	R	—

Maximum Packet Size Bits (MXPS)

Set the maximum data payload (maximum packet size) for the DCP in these bits. 40h (64 bytes) is the value after a reset.

The MXPS bits should be set to the value based on the USB specification.
The MXPS bits should be set while PID = NAK and before setting the CURPIPE bits.
Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

While MXPS is 0, do not write to the FIFO buffer or do not set PID to BUF.

32.2.12.2 DCP Control Register (DCPCTR)

Address(es): A006 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after hardware reset:	0	0	0	0	0	x	x	0	0	1	0	0	x	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b1, b0	PID[1:0]	Response PID	These bits control the response type of this controller during control transfer. b1 b0 00: NAK response 01: BUF response (depending on the buffer state) 10: STALL response 11: STALL response	R/W	R/W
b2	CCPL	Control Transfer End Enable	Setting this bit to 1 enables the status stage of the control transfer to be completed. 0: End of the control transfer disabled 1: End of the control transfer enabled	R/W	R/W
b4, b3	—	Reserved	When writing to these bits, write 0.	R/W	—
b5	PBUSY	PIPE Busy	Indicates whether the selected pipe is currently being used by the USB bus. 0: The pipe is not being used by the USB bus. 1: The pipe is being used by the USB bus.	R	W
b6	SQMON	Sequence Toggle Bit Monitor	Indicates the expected value of the sequence toggle bit for the next transaction during the DCP transfer. 0: DATA0 1: DATA1	R	W
b7	SQSET	Toggle Bit Set	Specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer. This bit is read as 0. When writing to this bit, only 1 can be written. 0: Writing has no effect 1: Specifies DATA1	R/W	R
b8	SQCLR	Toggle Bit Clear	Specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during the DCP transfer. This bit is read as 0. When writing to this bit, only 1 can be written. 0: Writing has no effect 1: Specifies DATA0	R/W	R
b10, b9	—	Reserved	When writing to these bits, write 0.	R/W	—
b11			When writing to this bit, write 1. However, this bit is read as 0.	R/W	—
b12			When writing to this bit, write 0.	R/W	—
b14, b13			When writing to these bits, write 1. However, these bits are read as 0.	R/W	—
b15	BSTS	Buffer Status	Indicates whether access to the DCP FIFO buffer is enabled or disabled. 0: Buffer access disabled 1: Buffer access enabled	R	W

Response PID Bits (PID)

Change the setting of these bits from NAK to BUF by software during data stage or status stage of control transfers.

This controller changes the setting of these bits in the following conditions:

(1) This controller changes the setting of the PID bits to select NAK response (00) on receiving the setup packet. Here, this controller sets VALID to 1. The setting of the PID bits cannot be changed until VALID is set to 0.
(2) This controller sets the PID bits to select STALL response (11) on receiving the data of the size exceeding the maximum packet size when the PID bits have been set to select BUF response.
(3) This controller sets the PID bits to select STALL response (1x) on detecting the control transfer sequence error.
(4) This controller sets the PID bits to select NAK response on detecting the USB bus reset.

This controller does not reference to the setting of the PID bits while the SET_ADDRESS request is processed (auto processing).

Control Transfer End Enable Bit (CCPL)

Setting this bit to 1 while the corresponding PID bits are set to BUF enables the stage of the control transfer to be completed.
Specifically, during control read transfer, this controller transmits the ACK handshake in response to the OUT transaction from the USB host, and outputs the zero-length packet in response to the IN transaction from the USB host during control writing or no-data control transfer. However, on detecting the SET_ADDRESS request, this controller operates in auto response mode from the setup stage up to the status stage completion irrespective of the setting of this bit.

This controller modifies this bit from 1 to 0 on receiving the new setup packet.

1 cannot be written by software to this bit while VALID is 1.

PIPE Busy Bit (PBUSY)

This controller modifies this bit from 0 to 1 upon start of the USB transaction for the selected pipe, and modifies the bit from 1 to 0 upon completion of one transaction.

Reading this bit after the PID bits have been set to NAK allows checking that modification of the pipe settings is possible.

Sequence Toggle Bit Monitor Bit (SQMON)

This bit indicates the expected value of the sequence toggle bit of the selected pipe.

This bit is toggled upon normal completion of the transaction. However, this bit is not toggled when a DATA-PID disagreement occurs during the receiving transfer.

This controller sets this bit to 1 (specifies DATA1 as the expected value) upon normal reception of the setup packet. This controller does not reference to this bit during the IN/OUT transaction of the status stage, and does not allow this bit to toggle upon normal completion.

Sequence Toggle Bit Set Bit (SQSET)

Setting this bit to 1 by software allows this controller to set DATA1 as the expected value of the sequence toggle bit of the selected pipe. This bit always indicates 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

Set this bit to 1 while PID is NAK and before setting the CURPIPE bits.
Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY is 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Clear Bit of Sequence Toggle Bit (SQCLR)

Setting this bit to 1 by software allows this controller to set DATA0 as the expected value of the sequence toggle bit of the selected pipe. This bit always indicates 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

Set this bit to 1 while PID is NAK and before setting the CURPIPE bits.
Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Buffer Status Bit (BSTS)

This bit indicates whether access from the CPU to the FIFO buffer assigned to the DCP is possible.
The meaning of the BSTS bit depends on the ISEL bit setting as follows.

(1) When ISEL = 0: indicates whether the received data can be read from the buffer.
(2) When ISEL = 1: indicates whether the data for transmission can be written to the buffer.

32.2.13 Pipe Configuration Register

Pipes 1 to 9 should be set using the PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPExCTR, PIPExTRE and PIPExTRN registers.

After selecting the pipe using the PIPESEL register, functions of the pipe should be set using the PIPECFG, PIPEBUF, PIPEMAXP and PIPEPERI registers. The PIPExCTR, PIPExTRE and PIPExTRN registers can be set regardless of the pipe selection in the PIPESEL register.

32.2.13.1 Pipe Window Select Register (PIPESEL)

Address(es): A006 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after hardware reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	PIPESEL [3:0]	Pipe Window Select	Specify the pipe corresponding to the registers allocated at address ranges from 68H to 6EH. b3 b0 0000: No pipe selected 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9	R/W	R
b15 to b4	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. When 0000b is set in PIPESEL, 0 is read from all of the bits in the PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI registers. When 0000b is set in PIPESEL, writing to the bits in these registers (at address ranges from 68H to 6EH) has no effect.

Pipe Window Select Bits (PIPESEL)

When a value between 0001b and 1001b is set in these bits, the information and settings for the corresponding pipe can be read from the registers at address ranges from A006 0068h to A006 006Eh. After a pipe is specified by setting these bits, the values set by software to the registers at address ranges from A006 0068h to A006 006Eh are reflected in the corresponding pipe transfer type by this controller.

When 0000b is set in PIPESEL, 0 is read from all of the bits from the registers at address ranges from A006 0068h to A006 006Eh. When 0000b is set in PIPESEL, writing to the bits in these registers has no effect.

32.2.13.2 Pipe Configuration Register (PIPECFG)

Address(es): A006 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after hardware reset:	0	0	x	x	x	0	0	0	0	x	x	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b3 to b0	EPNUM[3:0]	Endpoint Number	Specify endpoint number for the selected pipe.	R/W	R
b4	DIR	Transfer Direction	Specifies pipe transfer direction for the selected pipe. 0: Receiving direction 1: Transmitting direction	R/W	R
b6, b5	—	Reserved	When writing to these bits, write 0.	R/W	—
b7	SHTNAK	Pipe Disable at the End of Transfer	Specifies whether to change PID to NAK at the end of transfer when the selected pipe is in the receiving direction. 0: Pipe continued at end of transfer 1: Pipe disabled at end of transfer	R/W	R
b8	CNTMD	Continuous Transfer Mode	Specifies whether to use the selected pipe in continuous transfer mode. 0: Non-continuous transfer mode 1: Continuous transfer mode	R/W	R
b9	DBLB	Double Buffer Mode	Selects either single- or double-buffer operation for the FIFO buffer used by the selected pipe. 0: Single-buffer operation 1: Double-buffer operation	R/W	R
b10	BFRE	BRDY Interrupt Operation Specification	Specifies the BRDY interrupt generation timing from this controller to the CPU with respect to the selected pipe. 0: BRDY interrupt notification upon transmitting or receiving data 1: BRDY interrupt notification upon reading data	R/W	R
b13 to b11	—	Reserved	When writing to these bits, write 0.	R/W	—
b15, b14	TYPE[1:0]	Transfer Type	Specify the transfer type for the pipe selected by the PIPESEL bits (selected pipe). b15 b14 00: Pipe is not in use. 01: Bulk transfer 10: Interrupt transfer 11: Isochronous transfer	R/W	R

Endpoint Number Bits (EPNUM)

Specify the endpoint number for the selected pipe in these bits by software.
Setting 0000b indicates that the pipe is not being used.

These bits should be modified while PID is NAK, and the pipe is not selected by the CURPIPE bits.

Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Do not make the settings such that the combination of the set values in the DIR and EPNUM bits should be the same for two or more pipes (EPNUM = 0000b (the selected pipe is not in use) can be set for all the pipes).

Transfer Direction Bit (DIR)

When this bit is set to 0 by software, this controller uses the selected pipe in the receiving direction, and when this bit is set to 1, this controller uses the selected pipe in the transmitting direction.

This bit should be modified while PID is NAK and the pipe is not selected by the CURPIPE bits.
To modify this bit after completing USB communication using the selected pipe, write 1 and then 0 to ACLRM continuously to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the above-described state.

Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Pipe Disable Bit at the End of Transfer (SHTNAK)

This bit is valid when pipes 1 to 5 are selected in the receiving direction.
When this bit is set to 1 for the selected pipe in the receiving direction, this controller modifies the PID bits for the selected pipe to NAK on determining the end of the transfer. This controller determines that the transfer has ended on any of the following conditions.

(1) A short packet (including a zero-length packet) is successfully received.
(2) The transaction counter is used and the number of packets specified for the counter is successfully received.

This bit should be modified while PID is NAK.

Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

This bit should be cleared to 0 for the pipe in the transmitting direction.

Continuous Transfer Mode Bit (CNTMD)

This bit is valid when pipes 1 to 5 are selected and the transfer type of the selected pipe is set to bulk.

According to the setting value of this bit, this controller determines transmission/reception completion for the FIFO buffer assigned to the selected pipe. See Table 32.10.

Table 32.10 Relationship between Transfer Mode Settings by CNTMD Bit and Timings at which Reading Data or Transmitting Data from FIFO Buffer is Enabled

CNTMD Bit Setting	When Reading Data or Transmitting Data is Enabled
0	In the receiving direction (DIR = 0), the FIFO buffer is ready for reading in the following case. This controller receives one packet.
	In the transmitting direction (DIR = 1), the FIFO buffer is ready for transmission in either of the following cases. (1) Data of the maximum packet size is written to the FIFO buffer by software (or DMAC). (2) Data of the short packet size (including 0-byte data) is written to the FIFO buffer and then 1 is written to BVAL by software (or DMAC).
1	In the receiving direction (DIR = 0), the FIFO buffer is ready for reading in any of the following cases. (1) The number of the data bytes received in the FIFO buffer assigned to the selected pipe is equal to the number of assigned data bytes ((BUFSIZE + 1) × 64). (2) This controller receives a short packet other than a zero-length packet. (3) This controller receives a zero-length packet when data is already stored in the FIFO buffer assigned to the selected pipe. (4) This controller receives the number of packets equal to the transaction counter value specified for the selected pipe by software.
	In the transmitting direction (DIR = 1), the FIFO buffer is ready for transmission in any of the following cases (1) to (3). (1) The number of the data bytes written to the FIFO buffer by software (or DMAC) is equal to the number of data bytes in a single FIFO buffer plane assigned to the selected pipe. (2) The number of data bytes less than the size of a single FIFO buffer plane (including 0-byte data) assigned to the selected pipe is written to the FIFO buffer and then 1 is written to BVAL by software (or DMAC) . (3) The number of data bytes less than the size of a single FIFO buffer plane (including 0-byte data) assigned to the selected pipe is written to the FIFO buffer and then the DENDx_N signal is asserted at the same time as writing the last data by software (or DMAC).

This bit should be modified while PID is NAK and the pipe is not selected by the CURPIPE bits.
To modify this bit after completing USB communication using the selected pipe, write 1 and then 0 to ACLRM continuously to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the above-described state.

Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Double Buffer Mode Bit (DBLB)

This bit is valid when pipes 1 to 5 are selected.

When this bit is set to 1, this controller assigns two planes of the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe.
Specifically, the following expression determines the FIFO buffer size assigned to the selected pipe by this controller.
(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

This bit should be modified while PID is NAK and the pipe is not selected by the CURPIPE bits.
To modify this bit after completing USB communication using the selected pipe, write 1 and then 0 to ACLRM continuously by software to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the above-described state.

Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

BRDY Interrupt Operation Specification Bit (BFRE)

This bit is valid when pipes 1 to 5 are selected.

When this bit is set to 1 and the selected pipe is in the receiving direction (the DIR bit is set to 0), this controller detects the transfer completion and generates the BRDY interrupt on having read the pertinent packet.
When the BRDY interrupt is generated with the above conditions, 1 must be written to BCLR. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to BCLR.

When this bit is set to 1 and the selected pipe is in the transmitting direction (the DIR bit is set to 1), this controller does not generate the BRDY interrupt. For details, refer to the description of the PIPEBRDY interrupt register.

This bit should be modified while PID is NAK and the pipe is not selected by the CURPIPE bits.
To modify this bit after completing USB communication using the selected pipe, write 1 and then 0 to ACLRM continuously to clear the FIFO buffer assigned to the selected pipe while the PID and CURPIPE bits are in the above-described state.

Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Transfer Type Bits (TYPE)

Specify the USB transfer type for the pipe selected by the PIPESEL bits (selected pipe) in the TYPE bits.
Table 32.11 lists the selected pipes and transfer types that can be set in the TYPE bits.

Table 32.11 Selected Pipes and Transfer Types that can be Set in TYPE Bits

Selected Pipe	TYPE Bits	USB Transfer Type
Pipe 1 or Pipe 2	01b or 11b	Bulk or isochronous transfer
Pipe 3 to Pipe 5	01b	Bulk transfer
Pipe 6 to Pipe 9	10b	Interrupt transfer

Before setting PID to BUF for the selected pipe (before starting USB communication using the selected pipe), be sure to set these bits to the value other than 00b.

These bits should be modified while the PID bits for the selected pipe are set to NAK. Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY is 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

32.2.13.3 Pipe Buffer Specification Register (PIPEBUF)

Address(es): A006 006Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Value after hardware reset:	x	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b7 to b0	BUFNMB[7:0]	Buffer number	Specify the pipe FIFO buffer number for the selected pipe. (4h to 80h)	R/W	R
b9, b8	—	Reserved	When writing to these bits, write 0.	R/W	—
b14 to b10	BUFSIZE[4:0]	Buffer size	Specify the FIFO buffer size for the pipe specified in PIPESEL bits (selected pipe). 00h: 64 bytes 01h: 128 bytes | 1Fh: 2 Kbytes	R/W	R
b15	—	Reserved	When writing to this bit, write 0.	R/W	—

Note 1. The bits in this register should be modified while PID is NAK and the pipe is not selected by the CURPIPE bits.
Note 2. Before modifying the bits of this register after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Buffer Number Bits (BUFNMB)

The first block number in the FIFO buffer to be allocated for the selected pipe should be set in these bits. The FIFO buffer blocks allocated for the selected pipe by this controller are determined as follows:
Block number: BUFNMB to block number of BUFNMB + (BUFSIZE + 1) × (DBLB + 1) - 1

These bits must be set to a value that does not exceed the size of installed memory (0 [00h] to 8192 [0x80] for 8-Kbyte memory). Observe the following conditions:
00h is used exclusively for DCP.
04h is used exclusively for pipe 6. However, when pipe 6 is not used, 04h can be used for other pipes. When pipe 6 is selected, writing to these bits has no effect and 04h is automatically assigned by this controller.
05h is used exclusively for pipe 7. However, when pipe 7 is not used, 05h can be used for other pipes. When pipe 7 is selected, writing to these bits has no effect and 05h is automatically assigned by this controller.
06h is used exclusively for pipe 8. However, when pipe 8 is not used, 06h can be used for other pipes. When pipe 8 is selected, writing to these bits has no effect and 06h is automatically assigned by this controller.
07h is used exclusively for pipe 9. However, when pipe 9 is not used, 07h can be used for other pipes. When pipe 9 is selected, writing to these bits has no effect and 07h is automatically assigned by this controller.

Buffer Size Bits (BUFSIZE)

Specify the size of the FIFO buffer for the selected pipe in these bits in terms of blocks, where one block comprises 64 bytes. When the DBLB bit is set to 1 by software, this controller assigns two planes of the FIFO buffer size specified by the BUFSIZE bits to the selected pipe. Specifically, the following expression determines the FIFO buffer size assigned to the selected pipe by this controller.
(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

Set the following value in these bits.
(1) When pipes 1 to 5 are selected, any value from 0h to 1Fh can be set.
(2) When pipes 6 to 9 are selected, only 0h should be set.

When used with CNTMD = 1, set an integral multiple of the maximum packet size to the BUFSIZE bits.

32.2.13.4 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): A006 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	MXPS[10:0]										
Value after hardware reset:	0	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b10 to b0	MXPS[10:0]	Maximum Packet Size	Specify the maximum data payload (maximum packet size) of the selected pipe. Pipes 6 to 9 can be set to 01h to 40h bytes.	R/W	R
b15 to b11	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. The value after a reset of the MXPS bit is 00h when no pipe is selected with the PIPESEL bits in PIPESEL and 40h when a pipe is selected with the PIPESEL bits in PIPESEL.

Maximum Packet Size Bits (MXPS)

Set the maximum data payload (maximum packet size) for the selected pipe in these bits.
For pipes 1 and 2, a value between 1 byte (1h) to 1024 bytes (400h) can be set.
For pipes 3 to 5, any value from 8 bytes (8h), 16 bytes (10h), 32 bytes (20h), 64 bytes (40h) and 512 bytes (200h) can be set (bits [2:0] are not provided).
The value after a reset is 040h (64 bytes).

These bits should be set to the appropriate value for each transfer type based on the USB specification.
Set these bits to 1 while PID is NAK and before setting the CURPIPE bits.
Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

While MXPS is 0, do not write to the FIFO buffer or set PID to BUF.

32.2.13.5 Pipe Timing Control Register (PIPEPERI)

Address(es): A006 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after hardware reset:	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b2 to b0	IITV[2:0]	Interval Error Detection Spacing	Specify the interval error detection timing for the selected pipe in terms of frames, which is expressed as n-th power of 2.	R/W	R
b11 to b3	—	Reserved	When writing to these bits, write 0.	R/W	—
b12	IFIS	Isochronous IN Buffer Flush	Specifies whether to flush the buffer when the pipe selected by the PIPESEL bits (selected pipe) is used for isochronous IN transfers. 0: The buffer is not flushed 1: The buffer is flushed	R/W	R
b15 to b13	—	Reserved	When writing to these bits, write 0.	R/W	—

Interval Error Detection Spacing Bits (IITV)

Specify the interval error detection timing in terms of frames, which is expressed as n-th power of 2, in these bits.

These bits should be modified while PID is NAK and before setting the CURPIPE bits.
Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Before modifying these bits after USB communication has been completed with these bits set to a certain value, set PID to NAK and then set ACLRM to 1 to initialize the interval timer.

The IITV bits are invalid for pipes 3 to 5; set these bits to 0 for these pipes.

These bits can be set when the selected pipe transfer is for isochronous transfers.

(1) When the selected pipe is for isochronous OUT transfers

This controller generates the NRDY interrupt when it fails to receive a data packet within the interval set for (μ) frames by the IITV bits.

This controller generates the NRDY interrupt when this controller fails to receive a data packet because of a CRC error or other errors contained in the packet, or because of the FIFO buffer being full (because reading data from the FIFO buffer by software (DMAC) is slow).

This controller generates the NRDY interrupt on receiving an SOF packet. Even if the SOF packet is corrupted, the internal interpolation is used and allows the interrupt to be generated at the timing to receive the SOF packet. However, when the IITV bits are set to the value other than 0, this controller generates the NRDY interrupt on receiving an SOF packet for every interval after starting interval counting operation.

When the PID bits are set to NAK by software after starting the interval timer, this controller does not generate the NRDY interrupt on receiving an SOF packet.

The interval counting starts at the different timing depending on the IITV bit setting as follows.

(a) When IITV = 0: The interval counting starts when the PID bits for the selected pipe are set to BUF.

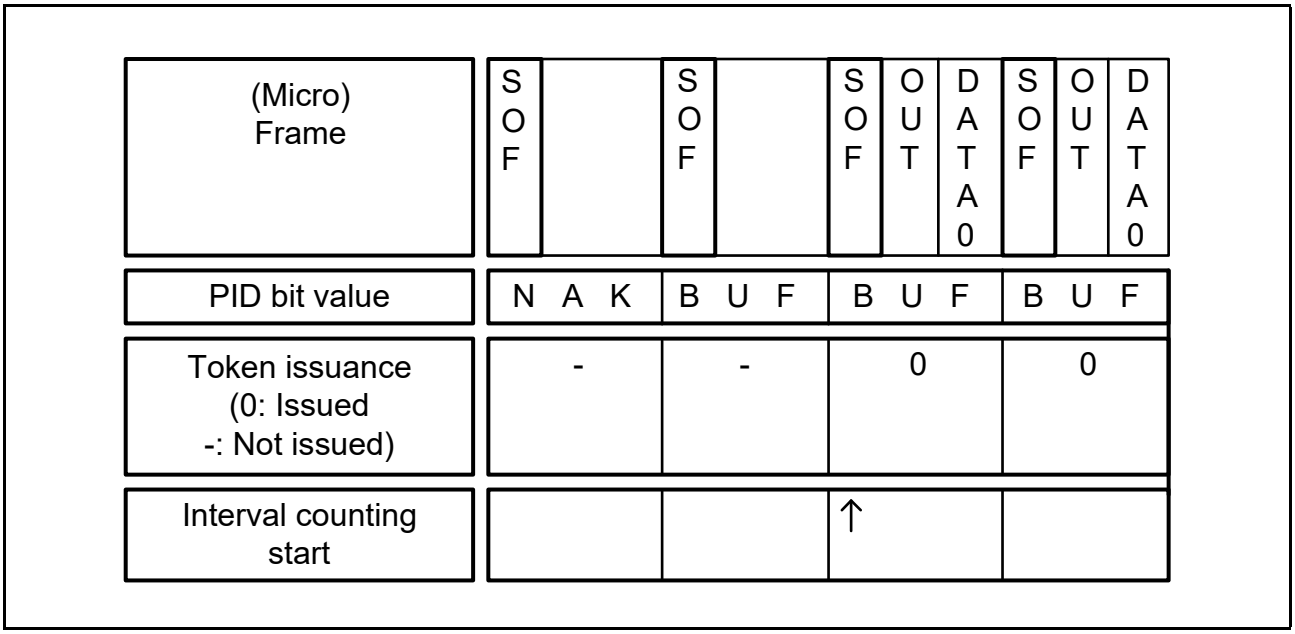


Figure 32.2 Relationship between (μ) Frames and Expected Token Reception when IITV = 0

(b) When IITV ≠ 0: The interval counting starts on completion of successful reception of the first data packet after the PID bits for the selected pipe have been modified to BUF.

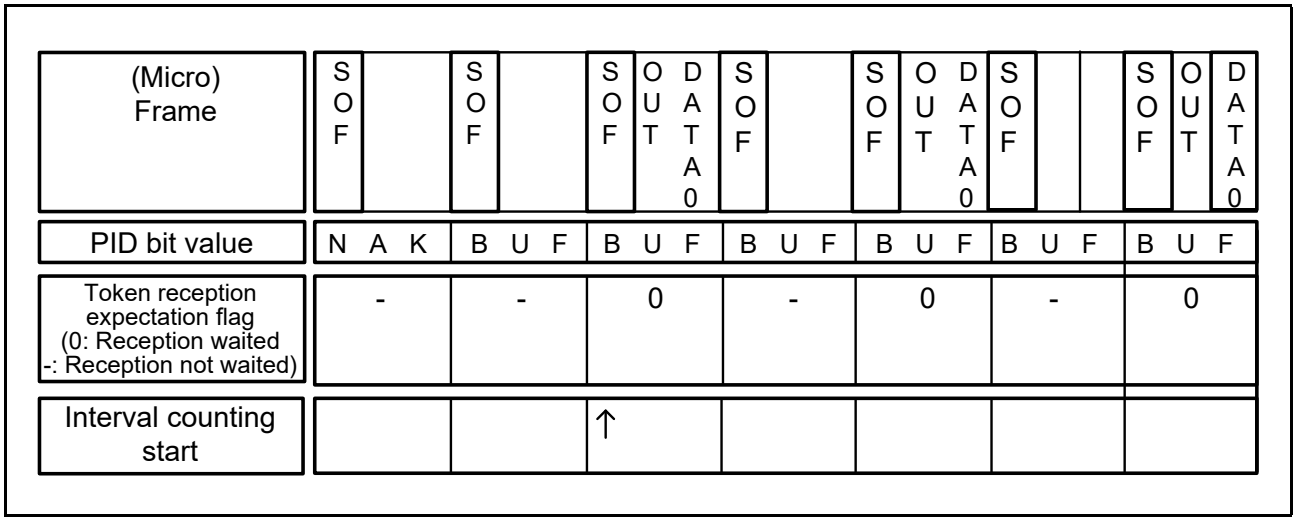


Figure 32.3 Relationship between (μ) Frames and Expected Token Reception when IITV = 1

(2) When the selected pipe is for isochronous IN transfers

The IFIS bit should be 1 for this use. When IFIS = 0, this controller transmits a data packet in response to the received IN token irrespective of the IITV bit setting.

When IFIS = 1, this controller clears the FIFO buffer when this controller fails to receive an IN token within the interval set for (μ) frames by the IITV bits in a state in which there is data to be transmitted in the FIFO buffer.
This controller also clears the FIFO buffer when this controller fails to receive an IN token successfully because of a bus error such as a CRC error contained in the token.
This controller clears the FIFO buffer on receiving an SOF packet. Even if the SOF packet is corrupted, the internal interpolation is used and allows the FIFO buffer to be cleared at the timing to receive the SOF packet.

The interval counting starts at the different timing depending on the IITV bit setting (similar to the timing during OUT transfers).

The counting conditions for the interval counter are any of the following.

(1) When a hardware reset is applied to this controller (at this point, the value of the IITV bits is also cleared to 0).
(2) When the ACLRM bit is set to 1 by software.
(3) When the controller detects a USB bus reset.

Isochronous IN Buffer Flush Bit (IFIS)

When the selected pipe is for isochronous IN transfers, this controller automatically clears the FIFO buffer when this controller fails to receive the IN token from the USB host within the interval set by the IITV bits in terms of (μ) frames. In double-buffer operation (DBLB = 1), this controller only clears the data in the plane used earlier.
This controller clears the FIFO buffer on receiving the SOF packet immediately after the (μ) frame in which this controller has expected to receive the IN token. Even if the SOF packet is corrupted, this controller also clears the FIFO buffer at the right timing to receive the SOF packet by using the internal interpolation.

When the selected pipe is not for the isochronous transfer, set this bit to 0.

32.2.14 Pipe Control Registers

32.2.14.1 PIPE1 Control Register (PIPE1CTR)
PIPE2 Control Register (PIPE2CTR)
PIPE3 Control Register (PIPE3CTR)
PIPE4 Control Register (PIPE4CTR)
PIPE5 Control Register (PIPE5CTR)

Address(es): PIPE1CTR: A006 0070h
PIPE2CTR: A006 0072h
PIPE3CTR: A006 0074h
PIPE4CTR: A006 0076h
PIPE5CTR: A006 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after hardware reset:	0	0	0	0	x	0	0	0	0	0	0	x	x	x	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b1, b0	PID[1:0]	Response PID	Specify the response type for the next transaction of the selected pipe. b1 b0 00: NAK response 01: BUF response (depending on the buffer state) 10: STALL response 11: STALL response	R/W	R/W
b4 to b2	—	Reserved	When writing to these bits, write 0.	R/W	—
b5	PBUSY	PIPE Busy	Indicates whether or not the selected pipe is being currently used for the USB bus. 0: The pipe is not being currently used for the USB bus. 1: The pipe is being currently used for the USB bus.	R	W
b6	SQMON	Toggle Bit Confirm	Sets the expected value of the sequence toggle bit in the next transaction of the selected pipe. 0: DATA0 1: DATA1	R	W
b7	SQSET	Toggle Bit Set	Specifies 1 when setting the expected value of the sequence toggle bit in the next transaction of the selected pipe, to DATA1. This bit is read as 0. When writing to this bit, only 1 can be written. 0: Writing has no effect. 1: Specifies DATA1	R/W	R
b8	SQCLR	Toggle Bit Clear	Specifies 1 when clearing the expected value of the sequence toggle bit in the next transaction of the selected pipe, to DATA0. This bit is read as 0. When writing to this bit, only 1 can be written. 0: Writing has no effect. 1: Specifies DATA0	R/W	R
b9	ACLRM	Auto Buffer Clear Mode	Enables or disables automatic buffer clear mode for the selected pipe. 0: Disabled 1: Enabled (all buffers are initialized)	R/W	R

Bit	Symbol	Bit Name	Description	S/W	H/W
b10	ATREPM	Auto Response Mode	Enables or disables auto response mode for the selected pipe. 0: Disabled 1: Enabled (a zero-length packet response while sending, NAK response and an NRDY interrupt is issued while receiving)	R/W	R
b12, b11	—	Reserved	When writing to these bits, write 0.	R/W	—
b13			When writing to this bit, write 1. However, this bit is read as 0.	R/W	—
b14	INBUFM	Transfer Buffer Monitor	Indicates the selected FIFO buffer state when the selected pipe is in the transmitting direction. 0: FIFO buffer contains no transmittable data. 1: FIFO buffer contains transmittable data.	R	W
b15	BSTS	Buffer Status	Indicates the FIFO buffer state of the selected pipe. 0: Buffer access is disabled. 1: Buffer access is enabled.	R	W

Response PID Bits (PID)

Set a response of the controller in each pipe in this bit by the software.

The default value of this bit is NAK. When executing a USB transfer through the selected pipe, change the setting of the PID bits to select BUF. The basic operations (operations when there is no error in the communication packet) of this controller for each value of the PID bit are given in Table 32.12.

To change the PID bits from BUF to NAK by a software while USB communications through the selected pipe is in progress, confirm that the USB transfer status of the known pipe has changed to NAK by reading PBUSY = 0. Note that reading of the PBUSY bit by a software is not required if the setting of the PID bits was changed to NAK by the controller.

In following cases, the controller modifies the value of this bit:

(1) When the selected pipe is for receiving and when the software has written 1 to the SHTNAK bit of the selected pipe, the controller sets PID = NAK upon identifying the transfer end.

(2) For the selected pipe, when the data packet of payload exceeding the maximum packet size is received, the controller sets PID = STALL (11b).

(3) When the USB bus reset is detected, the controller sets PID = NAK.

Write 10b to shift from PID = NAK (00b) to PID = STALL.
Write 11b to shift from BUF (01b) to STALL.
First write 10b and then write 00b to shift form STALL (11b) to NAK.
First, shift to NAK and then to BUF to shift from STALL to BUF.

Table 32.12 List of Controller Operations According to the PID Bit

PID Bit Value	Transfer Type (TYPE Bits Value)	Transfer Direction (DIR Bit Value)	Controller Operations
00b (NAK)	Bulk (TYPE = 01b) or Interrupt (TYPE = 10b)	Not dependent on setup value	NAK response is sent to the token from the USB host.
	Isochronous (TYPE = 11b)	Reception (DIR = 0)	Does not respond to the token from the USB host.
		Transmission (DIR = 1)	A zero-length packet is sent to the token from the USB host.
01b (BUF)	Bulk (TYPE = 01b)	Reception (DIR = 0)	When an OUT token is sent from the USB host, if the FIFO buffer for the selected pipe is ready for reception, the data is received and an ACK or NYET response is returned. A NAK response is returned if not ready. When a PING token is sent from the USB host, if the FIFO buffer of the selected pipe is ready for reception, an ACK response is returned. A NAK response is returned if not ready.
	Interrupt (TYPE = 10b)	Reception (DIR = 0)	For the Out token from the USB host, if the FIFO buffer of the selected pipe is ready for reception, the data is received and an ACK response is sent. A NAK response is returned if not ready.
	Bulk (TYPE = 01b) or Interrupt (TYPE = 10b)	Transmission (DIR = 1)	If the corresponding FIFO buffer is ready for transmission, the data is sent for the token from the USB. A NAK response is returned if not ready.
	Isochronous (TYPE = 11b)	Reception (DIR = 0)	For the Out token from the USB host, if the FIFO buffer of the selected pipe is ready for reception, the data is received. The data is deleted if not ready.
		Transmission (DIR = 1)	If the corresponding FIFO buffer is ready for transmission, the data is sent for the token from the USB. A zero-length packet is sent if not ready.
10b (STALL) or 11b (STALL)	Bulk (TYPE = 01b) or Interrupt (TYPE = 10)	Not dependent on setup value	A STALL response is sent to the token from the USB host.
	Isochronous (TYPE = 11b)	Not dependent on setup value	Returns nothing in response to the token from the USB host.

PIPE Busy Bit (PBUSY)

This controller modifies this bit from 0 to 1 upon start of the USB transaction for the selected pipe, and modifies the bit from 1 to 0 upon completion of one transaction.

Reading this bit after PID has been set to NAK allows checking that modification of the pipe settings is possible.

Sequence Toggle Bit Monitor Bit (SQMON)

This bit indicates the expected value of the sequence toggle bit of the selected pipe.

When the selected pipe is not for the isochronous transfer, this bit is toggled upon normal completion of the transaction. However, this bit is not toggled when a DATA-PID disagreement occurs during the receiving transfer.

Sequence Toggle Bit Set Bit (SQSET)

Setting this bit to 1 by software allows this controller to set DATA1 as the expected value of the sequence toggle bit of the selected pipe. This bit always indicates 0.

Set this bit to 1 while PID is NAK.
Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Sequence Toggle Bit Clear Bit (SQCLR)

Setting this bit to 1 by software allows this controller to set DATA0 as the expected value of the sequence toggle bit of the selected pipe. This bit always indicates 0.

Set this bit to 1 while PID is NAK.
Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Auto Buffer Clear Mode Bit (ACLRM)

To clear the contents in the FIFO buffer assigned to the selected pipe completely, write 1 and then 0 to this bit continuously.
Table 32.13 shows the contents cleared by writing 1 and 0 to this bit continuously.
Table 32.14 shows the cases in which clearing the contents is necessary.

Table 32.13 Contents Cleared by this Controller by Setting ACLRM = 1

No.	Contents Cleared by ACLRM Bit Manipulation
(1)	All the contents in the FIFO buffer assigned to the selected pipe (all the information in two FIFO buffer planes in double-buffer operation)
(2)	The interval count value when the selected pipe is for isochronous transfer

Table 32.14 Cases where Setting ACLRM = 1 is Required

No.	Case where Clearing is Required
(1)	All the contents in the FIFO buffer assigned to the selected pipe are to be cleared.
(2)	The interval counter is to be reset.
(3)	When the BFRE setting is modified
(4)	When the DBLB setting is modified
(5)	When the transaction count function is forcibly terminated

Set this bit to 1 while PID is NAK and before specifying the pipe in CURPIPE bits. Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Auto Response Mode Bit (ATREPM)

When the selected pipe is for bulk transfer, this bit can be set to 1.
When this bit is set to 1, this controller responds to the token from the USB host as described below.

(1) When the selected pipe is for bulk IN transfer (when TYPE = 01b and DIR = 1)
When ATREPM = 1 and PID = BUF, this controller transmits a zero-length packet in response to the IN token. This controller updates (toggles) the sequence toggle bit (DATAPID) each time this controller receives the ACK from the USB host (in a single transaction, IN token is received, zero-length packet is transmitted, and then ACK is received). In this case, this controller does not generate the BRDY or BEMP interrupt.

(2) When the selected pipe is for bulk OUT transfer (when TYPE = 01b and DIR = 0)
When ATREPM = 1 and PID = BUF, this controller returns NAK in response to the OUT token (or PING token) and generates the NRDY interrupt.

This bit should be modified while PID is NAK. Before setting this bit to 1 after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

For USB communication in auto response mode, set this bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode.

When the selected pipe is for isochronous transfer, be sure to set this bit to 0.

Transmission Buffer Monitor Bit (INBUFM)

When the selected pipe is in the transmitting direction (DIR = 1), this controller sets this bit to 1 when writing to at least one FIFO buffer plane is completed by software (or DMAC).
This controller sets this bit to 0 when this controller completes transmitting the data from the FIFO buffer plane to which all data has been written. In double-buffer operation (DBLB = 1), this controller sets this bit to 0 after this controller has completed transmitting the data from both FIFO buffer planes but before it has completed writing data to a single FIFO buffer plane.

This bit indicates the same value as the BSTS bit when the selected pipe is in the receiving direction (DIR = 0).

Buffer Status Bit (BSTS)

This bit indicates whether access from the CPU to the FIFO buffer assigned to the selected pipe is enabled or disabled.
The meaning of the BSTS bit depends on the setting of the DIR, BFRE and DCLRM bits as follows.

Table 32.15 BSTS Bit Operations

DIR Bit Value	BFRE Bit Value	DCLRM Bit Value	Meaning of BSTS Bit
0	0	0	1: The received data can be read from the FIFO buffer. 0: The received data has been completely read from the FIFO buffer.
		1	Setting prohibited
	1	0	1: The received data can be read from the FIFO buffer. 0: The BCLR bit has been set to 1 after the received data has been completely read from the FIFO buffer.
		1	1: The received data can be read from the FIFO buffer. 0: The received data has been completely read from the FIFO buffer.
1	0	0	1: The transmit data can be written to the FIFO buffer. 0: The transmit data has been completely written to the FIFO buffer.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

32.2.14.2 PIPE6 Control Register (PIPE6CTR)
PIPE7 Control Register (PIPE7CTR)
PIPE8 Control Register (PIPE8CTR)
PIPE9 Control Register (PIPE9CTR)

Address(es): PIPE6CTR: A006 007Ah
PIPE7CTR: A006 007Ch
PIPE8CTR: A006 007Eh
PIPE9CTR: A006 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after hardware reset:	0	x	0	0	x	x	0	0	0	0	0	x	x	x	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b1, b0	PID[1:0]	Response PID	Specify the response type for the next transaction of the selected pipe. b1 b0 00: NAK response 01: BUF response (depending on the buffer state) 10: STALL response 11: STALL response	R/W	R/W
b4 to b2	—	Reserved	When writing to these bits, write 0.	R/W	—
b5	PBUSY	PIPE Busy	Indicates whether or not the selected pipe is being currently used for the USB bus. 0: The pipe is not being currently used for the USB bus. 1: The pipe is being currently used for the USB bus.	R	W
b6	SQMON	Toggle Bit Confirm	Sets the expected value of the sequence toggle bit in the next transaction of the selected pipe. 0: DATA0 1: DATA1	R	W
b7	SQSET	Toggle Bit Set	Specifies 1 while clearing the expected value of the sequence toggle bit in the next transaction of the selected pipe to DATA1.This bit is read as 0. When writing to this bit, write 1. 0: Writing has no effect. 1: Specifies DATA1	R/W	R
b8	SQCLR	Toggle Bit Clear	Specifies 1 while clearing the expected value of the sequence toggle bit in the next transaction of the selected pipe to DATA0. This bit is read as 0. When writing to this bit, write 1. 0: Writing has no effect. 1: Specifies DATA0	R/W	R
b9	ACLRM	Auto Buffer Clear Mode	Enables or disables automatic buffer clear mode for the selected pipe. 0: Disabled 1: Enabled (all buffers are initialized)	R/W	R
b12 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—
b13			When writing to this bit, write 1. However, this bit is read as 0.	R/W	—
b14			When writing to this bit, write 0.	R/W	—
b15	BSTS	Buffer Status	Indicates the FIFO buffer state of the selected pipe. 0: Buffer access is disabled 1: Buffer access is enabled	R	W

As for the bits listed below, see the description of each bit in section 32.2.14.1, PIPE1 Control Register (PIPE1CTR) PIPE2 Control Register (PIPE2CTR) PIPE3 Control Register (PIPE3CTR) PIPE4 Control Register (PIPE4CTR) PIPE5 Control Register (PIPE5CTR).

- Response PID Bits (PID)
- PIPE Busy Bit (PBUSY)
- Buffer Status Bit (BSTS)
- Sequence Toggle Bit Monitor Bit (SQMON)
- Sequence Toggle Bit Set Bit (SQSET)
- Sequence Toggle Bit Clear Bit (SQCLR)

Auto Buffer Clear Mode Bit (ACLRM)

To clear all contents from the FIFO buffer allocated to the selected pipe, write 1 and 0 sequentially in the ACLRM bit. Table 32.16 shows the contents of data to be cleared by the controller when 1 and 0 are written to this bit sequentially. The cases that require this processing are listed in Table 32.17.

Table 32.16 Contents Cleared by the Controller when ACLRM = 1

No.	Contents Cleared by ACLRM Bit Manipulation
(1)	Entire contents of the FIFO buffer allocated to the selected pipe

Table 32.17 Cases where Setting ACLRM = 1 is Required

No.	Cases where Clearing is Required
(1)	All the contents in the FIFO buffer assigned to the selected pipe are to be cleared.
(2)	The interval counter is to be reset.
(3)	The value of the BFRE bit is changed.
(4)	The transaction count function is forcibly terminated.

The ACLRM bit should be set while PID = NAK and before specifying the pipe in the CURPIPE bits.
Before modifying this bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY is 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

32.2.15 Transaction Counters

32.2.15.1 PIPE1 Transaction Counter Enable Register (PIPE1TRE)
PIPE2 Transaction Counter Enable Register (PIPE2TRE)
PIPE3 Transaction Counter Enable Register (PIPE3TRE)
PIPE4 Transaction Counter Enable Register (PIPE4TRE)
PIPE5 Transaction Counter Enable Register (PIPE5TRE)

Address(es): PIPE1TRE: A006 0090h
PIPE2TRE: A006 0094h
PIPE3TRE: A006 0098h
PIPE4TRE: A006 009Ch
PIPE5TRE: A006 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after hardware reset:	x	x	x	x	x	x	0	0	x	x	x	x	x	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b7 to b0	—	Reserved	When writing to these bits, write 0.	R/W	—
b8	TRCLR	Transaction Counter Clear	The transaction counter can be cleared to 0 by writing 1 to this bit. This bit is read as 0. When writing to this bit, write 1. 0: Invalid 1: The current counter value is cleared	R/W	R
b9	TRENB	Transaction Counter Enable	Enable or disables the transaction counter 0: The transaction counter is disabled 1: The transaction counter is enabled	R/W	R
b15 to b10	—	Reserved	When writing to these bits, write 0.	R/W	—

Note 1. Modify each bit in this register while PID is NAK.
Before modifying each bit after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.

Transaction Counter Clear Bit (TRCLR)

When this bit is set to 1 by software, this controller clears the current counter value of the transaction counter corresponding to the selected pipe and then sets this bit to 0.

Transaction Counter Enable Bit (TRENB)

For the pipe in the receiving direction, setting this bit is set to 1 by software after setting the total number of the packets to be received in the TRNCNT bits allows the following control on having received the number of packets equal to the set value in the TRNCNT bits.

(1) In continuous transmission/reception mode (CNTMD = 1), this module switches the FIFO buffer to the CPU side even if the FIFO buffer is not full on completion of reception.
(2) While SHTNAK is 1, this module changes the setting of the PID bits to NAK for the corresponding pipe on having received the number of packets equal to the set value in the TRNCNT bits.
(3) While DENDE is 1 and PKTMD is 0, the DEND signal is asserted when the number of packets specified in the TRNCNT bits is received and the last data is to be read.
(4) While BFRE is 1, this module asserts the BRDY interrupt on having received the number of packets equal to the set value in the TRNCNT bits and then reading out the last received data.

For the pipe in the transmitting direction, set this bit to 0.
When the transaction counter is not used, set this bit to 0.
When the transaction counter is used, set the TRNCNT bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

32.2.15.2 PIPE1 Transaction Counter Register (PIPE1TRN)
PIPE2 Transaction Counter Register (PIPE2TRN)
PIPE3 Transaction Counter Register (PIPE3TRN)
PIPE4 Transaction Counter Register (PIPE4TRN)
PIPE5 Transaction Counter Register (PIPE5TRN)

Address(es): PIPE1TRN: A006 0092h
PIPE2TRN: A006 0096h
PIPE3TRN: A006 009Ah
PIPE4TRN: A006 009Eh
PIPE5TRN: A006 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b15 to b0	TRNCNT [15:0]	Transaction Counter	When written to: Specify the total number of reception packets (number of transactions) to be received by the selected pipe. When read from: Indicate the specified number of transactions if TRENB is 0. Indicate the number of currently counted transaction if TRENB is 1.	R/W	R/W

Transaction Counter Bits (TRNCNT)

For the pipe in the receiving direction, setting these bits to 1 by software after setting the total number of the packets to be received in the TRNCNT bits allows the control of the transaction counter clear bit (TRCLR).
When TRENB = 0, these bits indicate the number of transactions set by software.
When TRENB = 1, these bits indicate the number of transactions being currently counted.

This controller increments the value of these bits by one when all of the following conditions are satisfied on receiving the packet.

(a) TRENB = 1
(b) (TRNCNT setting ≠ current counter value +1) on receiving the packet
(c) The payload of the received packet agrees with the set value in the MXPS bits.

This module clears the value of these bits to 0 when any of the following conditions are satisfied.

(1) When all the following conditions are satisfied:
(a) TRENB = 1
(b) (TRNCNT setting = current counter value +1) on receiving the packet
(c) The payload of the received packet agrees with the set value in the MXPS bits.

(2) When both of the following conditions are satisfied:
(a) TRENB = 1
(b) A short packet is received.

(3) When the following condition is satisfied:
(a) When the TRCLR bit is set to 1 by software

For the pipe in the transmitting direction, set these bits to 0. When the transaction counter is not used, set these bits to 0.

These bits should be modified while PID is NAK and TRENB is 0.
Before modifying these bits after changing the setting of the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, checking of the PBUSY bit is not required if the setting of the PID bits has been changed to select NAK response by the controller.
To modify the value of these bits, set TRCLR to 1 before setting TRENB to 1.

32.2.16 Low-Power Status Register (LPSTS)

Address(es): A006 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SUSPM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after hardware reset:	x	0	x	0	x	x	x	0	x	x	x	x	0	x	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b13 to b0	—	Reserved	When writing to these bits, write 0.	R/W	—
b14	SUSPM	UTMI SuspendM Control	Controls the SuspendM signal to the UTMI. 0: UTMI suspend mode 1: UTMI normal mode	R/W	R/W
b15	—	Reserved	When writing to this bit, write 0.	R/W	—

UTMI SuspendM Control Bit (SUSPM)

The USBf module controls output of the clock signal from the PLL in the USB-PHY layer. Accordingly, supply of the clock signal to the USBf module is stopped while SUSPM = 0.
After setting this bit to 1, wait for at least 100 us to allow oscillation of the UTMI clock to become stable.

Writing to this controller is disabled when the SUSPM bit is set to 0 (the UTMI clock is stopped). Reading from the controller area is allowed. However, writing to the registers listed in Table 32.18 is enabled even when the SUSPM bit is set to 0.

Table 32.18 List of Registers that can be Written by Software when SUSPM = 0

Address	Register Name
A006 0000h	SYSCFG0
A006 0002h	SYSCFG1
A006 0102h	LPSTS

However, the value written to the SYSCFG0 register while the UTMI clock is stopped (SUSPM = 0) is reflected after the UTMI clock oscillation is started (SUSPM = 1).

32.2.17 FIFO Continuous Transfer Ports

32.2.17.1 D0FIFO Continuous Transfer Port Register n (D0FIFOBn) (n = 0 to 7)
D1FIFO Continuous Transfer Port Register n (D1FIFOBn) (n = 0 to 7)

Address(es): D0FIFOBn: A006 0160h
D1FIFOBn: A006 0180h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	FIFOPORT[31:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[31:0]															
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit Name	Description	S/W	H/W
b31 to b0	FIFOPORT [31:0]	FIFO Port	Accessing these bits allows reading the received data from the FIFO buffer or writing the transmit data to the FIFO buffer.	R/W	R/W

FIFO Port Control

When DFACC is set to 01b or 10b (16-byte/32-byte continuous access mode), use the DxFIFO continuous transfer port registers for access to the DxFIFO buffers.

32.2.18 PHY Setting Register 1

32.2.18.1 PHY Setting Register 1 (PHYSET1)

Address(es): A006 01A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	PHYVBUSIN	PHYRESET	PHYPD	P1PORTSEL[1:0]	
Value after hardware reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Value after USB bus reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	S/W	H/W
b1, b0	P1PORTSEL[1:0]	Port Connection Path Select Input Signal	b1 b0 00: Signals are not driven. 01: USB host controller 10: Setting prohibited 11: USB function controller	R/W	R/W
b2	PHYPD	USB PHY Power-Down Signal	0: Normal mode 1: Power-down mode	R/W	R/W
b3	PHYRESET	USB PHY Reset	0: Release from the reset state 1: The reset signal is asserted.	R/W	R/W
b4	PHYVBUSIN	Setting for VBUS Input to USB PHY	Enables the pull-up resistors for the D+ signal. 0: No VBUS input (D+ pull-up resistor disabled) 1: VBUS input (D+ pull-up resistor enabled)	R/W	R/W
b15 to b5	—	Reserved	When writing to these bits, write 0.	R/W	—

Note: Placing the PLL in the PHY layer in power-down mode is prohibited once the PHY-PLL has been activated.

P1PORTSEL[1:0]

Port connection path selection input signals
00b: Signals are not driven.
01b: USB host controller
10b: Setting prohibited
11b: USB function controller

PHYPD

USB PHY power-down signal
0: Normal mode
1: Power-down mode

PHYRESET

USB PHY reset input
0: Release from the reset state
1: The reset signal is asserted.

PHYVBUSIN

This bit sets the VBUS input to the USB PHY layer. The setting of this bit enables the pull-up resistor for the D+ signal.
0: No VBUS input (D+ pull-up resistor disabled)
1: VBUS input (D+ pull-up resistor enabled)

32.3 Operation

32.3.1 System Controls and Oscillation Controls

This section describes the register operations required for initial settings of this module, and the registers necessary for power consumption control. The startup sequence is as follows.

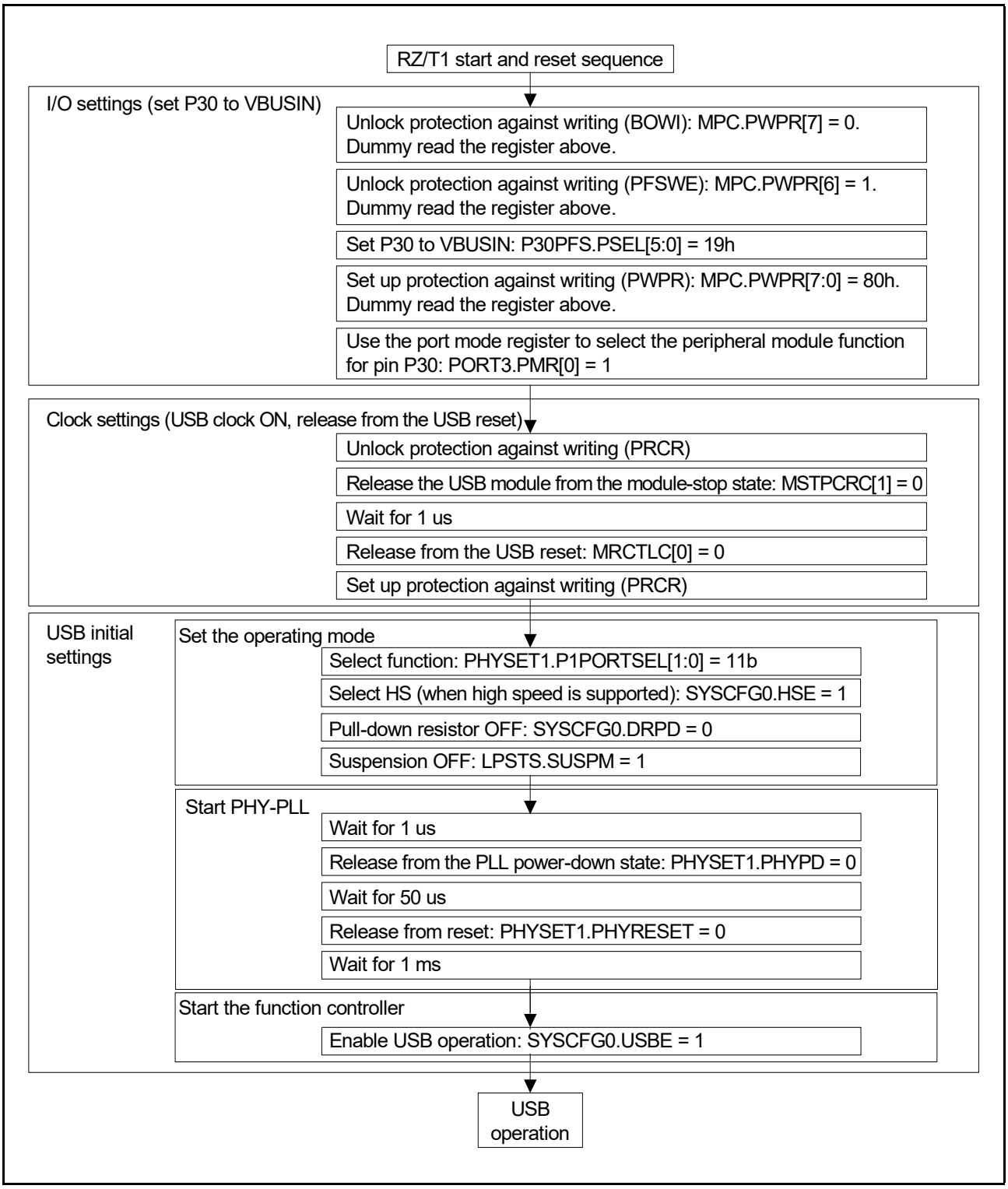


Figure 32.4 Startup Sequence

32.3.2 Resets

Table 32.19 lists the types of reset for this controller. For the initial states of the registers following the reset operations, refer to section 5, I/O Registers.

Table 32.19 Types of Reset

Name	Operation
USB bus reset	Automatically detected by this module from the D+ and D- lines

32.3.3 USB Data Bus Resistor Controller

This controller controls the pull-up resistors for the D+ signal of the USB2.0-PHY port.
Make pull-up setting for the D+ signal using the DPRPU and DRPD bits of the SYSCFG0 register.

Confirm the connection to the USB Host before setting the DPRPU bit of the SYSCFG0 register to 1 to pull up D+.
Set PHYSET1.PHYVBUSIN to 1 at the same time.

This controller incorporates termination resistors for the D+ and D- signals (in high-speed operation mode) and output resistors (in full-speed operation mode). The switching of the internal resistors following the connection to the PC is automatically done by the controller during reset handshake, suspend, and resume processing.

If the DPRPU bit of the SYSCFG0 register is set to 0 during communication with the PC, the controller disables the pull-up resistors (or termination resistors) of the USB data lines, so that it can notify the host controller of the disconnection of the device. At that time, set PHYSET1.PHYVBUSIN to 0 at the same time.

32.3.4 Supply of Clocks

Table 32.20 lists two clocks required for this controller.

Table 32.20 Input Clocks

Input Clock Name	Description
CPU clock (CPUCLK)	CPU clock input There are no restrictions on the clock frequency.
PHY clock (UTMI clock)	PHY clock input 60 MHz is internally supplied.

32.3.5 Notes on Stopping Clocks

- The PHY clock can be stopped with the SUSPM register in suspend mode.
- If a clock is to be stopped while the controller is in USB suspended state, however, it is necessary to resume the supply of the clock during resume processing. The resumption of the PHY clock need be accomplished within 5.5 ms after a resume interrupt occurs.
- After starting the PLL in the USB-PHY, do not stop it by setting the PHY power down bit (PHYSET1.PHYPD) or the PHY reset bit (PHYSET1.PHYRESET).
- When the USB function is not in use, place the USB module in the module-stop state (MSTPCRC[1] = 1 (MRCTLC[0] = 1 for making the USB reset setting)).

32.4 Interrupt Functions

32.4.1 Overview of Interrupt Functions

Table 32.21 lists the interrupt functions of this controller.

Table 32.21 List of Interrupt Functions

Bit	Interrupt Name	Interrupt Source	Related Status
VBINT	VBUS interrupt	When a change in the state of the VBUS input pin has been detected (low to high or high to low).	VBSTS
RESM	Resume interrupt	When a change in the state of the USB bus has been detected in the suspended state (J-state to K-state or J-state to SE0)	—
SOFR	Frame number update interrupt	If SOFRM = 0: When an SOF packet with a different frame number is received. If SOFRM = 1: When an SOF packet for a µ frame number of 0 cannot be received due to a corrupted packet.	—
DVST	Device state transition interrupt	When transition in device state is detected: A USB bus reset detected The suspended state detected Set Address request received Set Configuration request received	DVSQ
CTRT	Control transfer stage transition interrupt	When a stage transition is detected in control transfer: Setup stage completed Control write transfer status stage transition Control read transfer status stage transition Control transfer completed A control transfer sequence error occurred	CTSQ
BEMP	Buffer empty interrupt	When the buffer becomes empty after all data in the buffer memory has been transmitted. When a packet exceeding the maximum packet size is received.	PIPEBEMP
NRDY	Buffer not ready interrupt	When a token is received when PID = BUF and the buffer memory is not ready to transmit or receive data. When a CRC error or bit stuff error occurs while receiving data in isochronous transfer. When an interval error occurs while receiving data in isochronous transfer.	PIPENRDY
BRDY	Buffer ready interrupt	When the buffer is ready (readable or writable).	PIPEBRDY

Table 32.22 shows operations for a USBf interrupt output from this controller. In case more than one interrupt source is generated, the USBf interrupt output method can be set by using the INTL bit in the SOFCFG register. Set the USBf interrupt output operation according to the user system.

Table 32.22 Operations for USBf Interrupt Output

USBf Interrupt output pin operation / INTL Setting	When One Interrupt Source is Generated	When More than One interrupt Source is Generated
Edge sense (INTL = 0)	Holds the pin low until the interrupt source is cleared.	Negated (H pulse output) for 32 clock cycles at 48 MHz when one source is cleared.
Level sense (INTL = 1)	Holds the pin low until the interrupt source is cleared.	Holds the pin low until all sources are cleared.

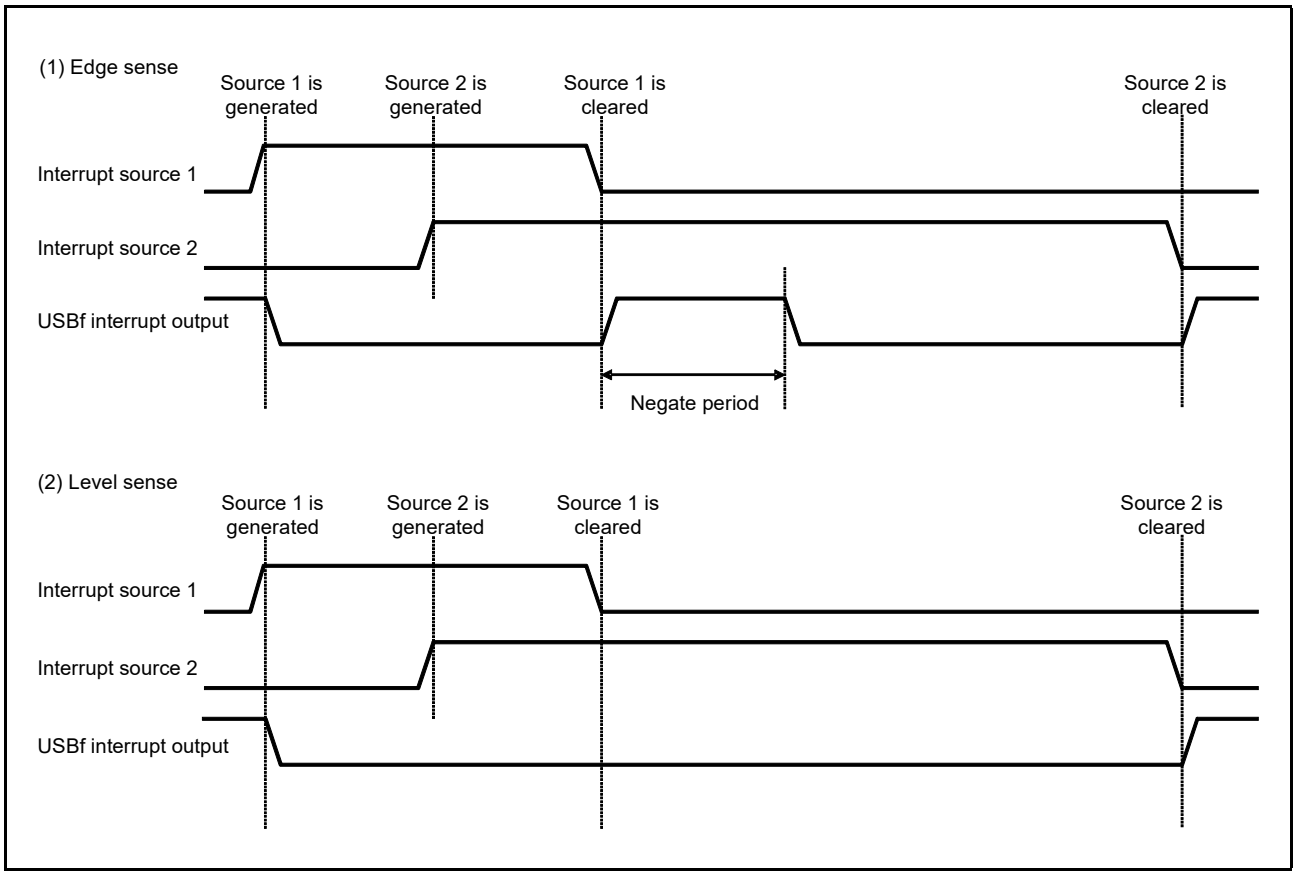


Figure 32.5 USBf Interrupt Output Operation Diagram

Figure 32.6 shows the interrupt configurations for the controller.

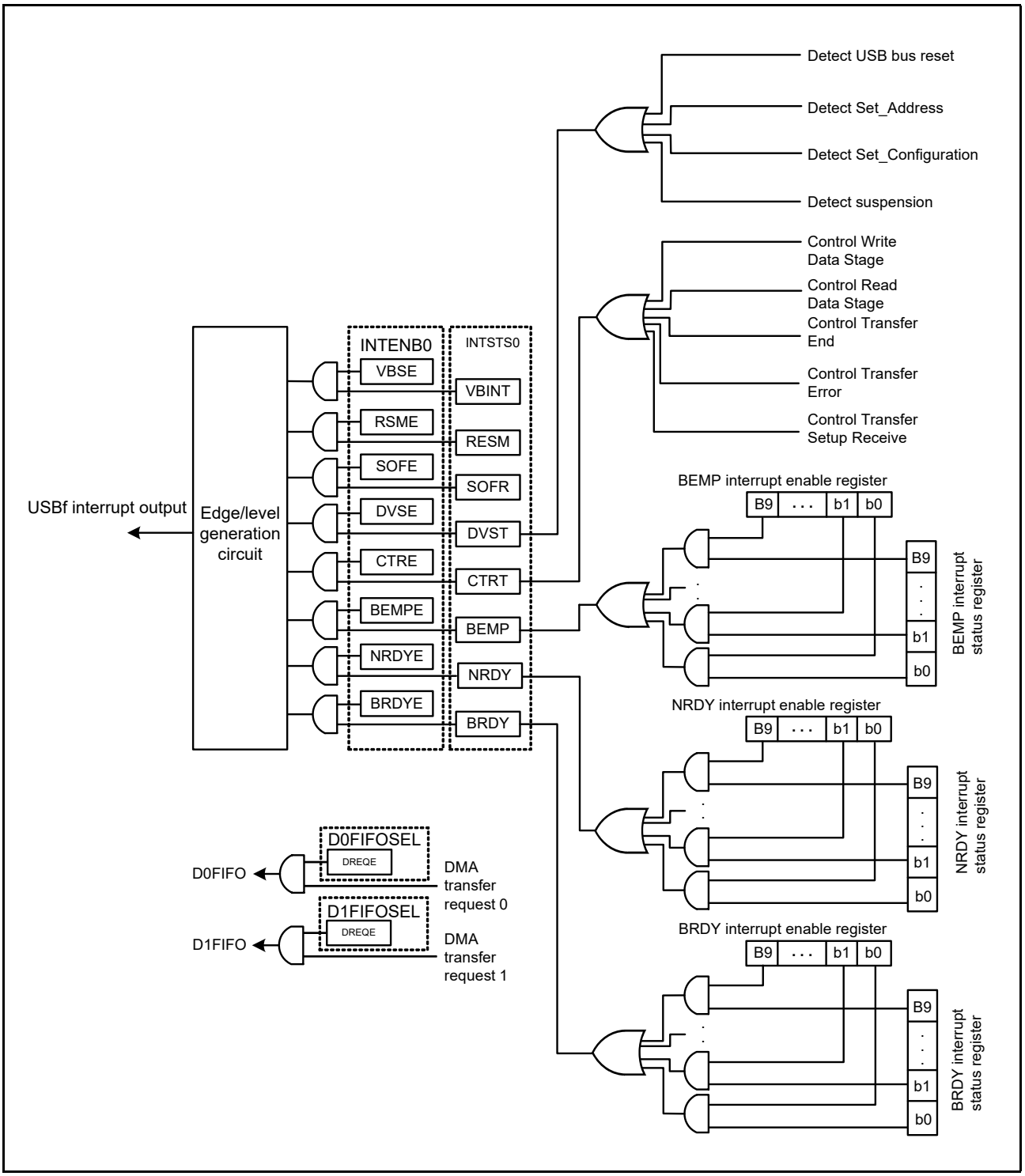
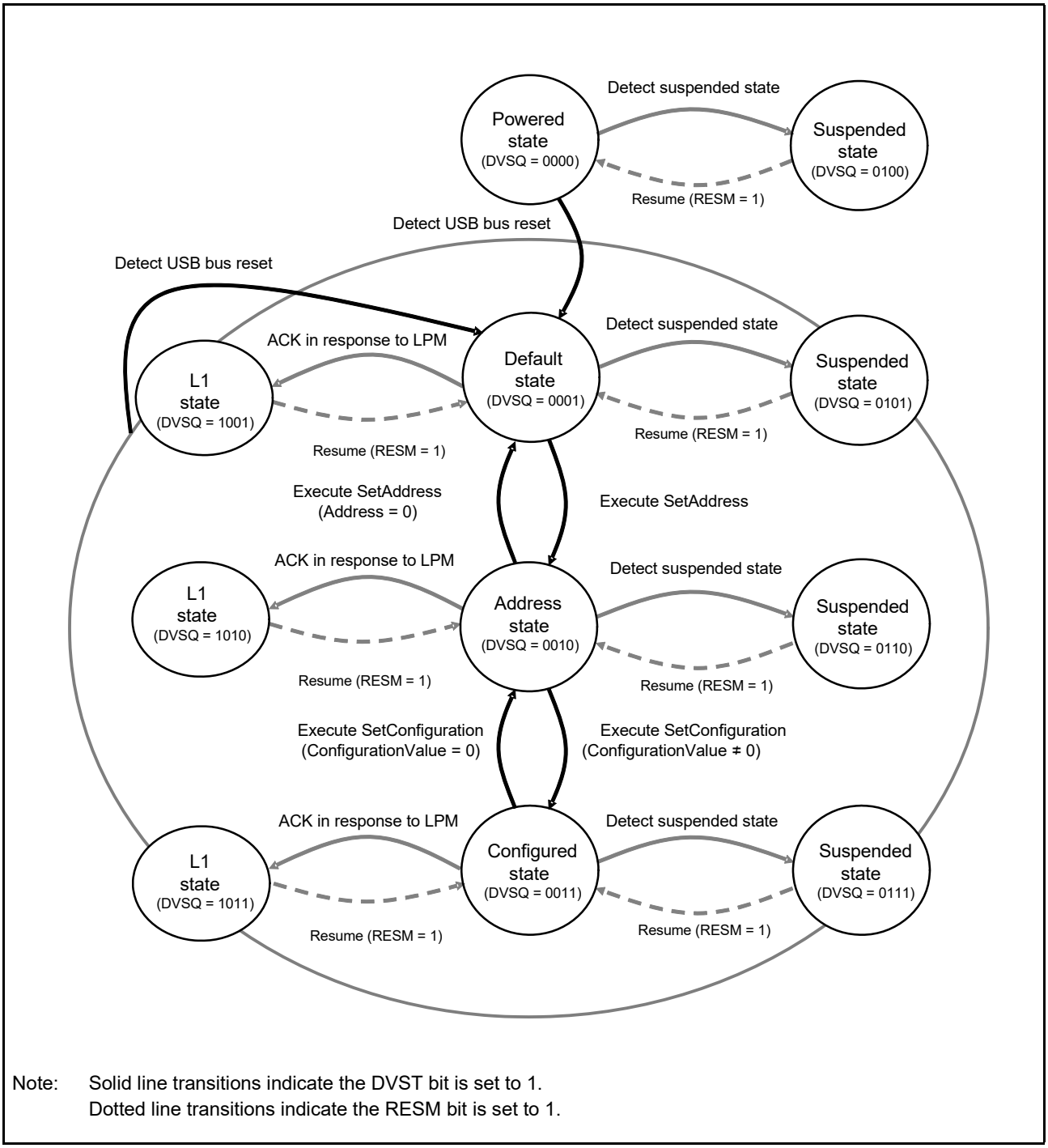


Figure 32.6 Interrupt Configuration Diagram

32.4.2 Device State Transition Interrupt

Figure 32.7 shows a diagram of how this module handles the device state transitions. The controller monitors the device states and generates the device state transition interrupts. However, recovery from the suspended state (resume signal detection) is detected by the resume interrupt. The device state transition interrupts can be enabled or disabled individually by setting the INTENB0 register. The device state after a transition can be confirmed using the DVSQ bits in the INTSTS0 register.

When making a transition to the default state, the device state transition interrupt is generated after the reset handshake protocol has been completed.



Note: Solid line transitions indicate the DVST bit is set to 1.
Dotted line transitions indicate the RESM bit is set to 1.

Figure 32.7 Device State Transitions

32.4.3 Control Transfer Stage Transition Interrupt

Figure 32.8 shows a diagram of how this module handles the control transfer stage transition. The controller monitors the control transfer sequence and generates the control transfer stage transition interrupts. The control transfer stage transition interrupts can be enabled or disabled individually in the INTENB0 register. The control transfer stage after a transition can be confirmed in the CTSQ bits in the INTSTS0 register.

The control transfer sequence errors are described below. If an error occurs, the PID bits in DCPCTR are set to 1xb (STALL).

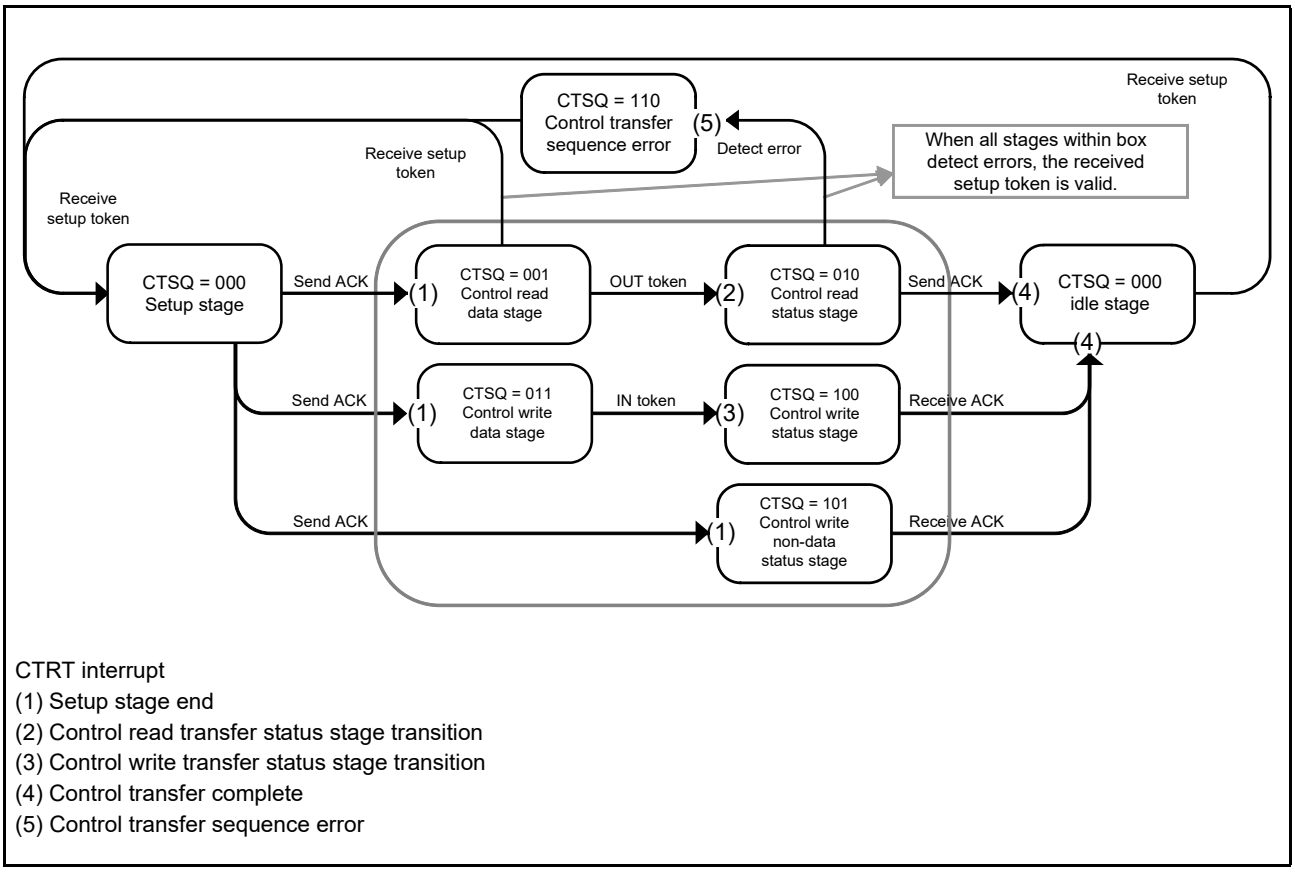
(1) During control read transfers
   (a) At the IN token of the data stage, an OUT or PING token is received when there have been no data transfers at all.
   (b) An IN token is received at the status stage.
   (c) A packet is received at the status stage for which the data packet is DATAPID = DATA0.

(2) During control write transfers
   (a) At the OUT token of the data stage, an IN token is received when there have been no ACK response at all.
   (b) A packet is received at the data stage for which the first data packet is DATAPID = DATA0.
   (c) At the status stage, an OUT or PING token is received.

(3) During control write no-data transfers
   (a) At the status stage, an OUT or PING token is received.

Note that in the control write transfer data stage, if the number of received data is more than the USB request wLength value, the control transfer sequence error cannot be recognized. Also, in the control read transfer status stage, when a packet other than a zero-length packet is received, an ACK response is returned and the transfer is successfully completed.

When a CTRT interrupt is generated due to a sequence error (SERR = 1), the value of CTSQ = 110b is retained until CTRT = 0 is written by the user system (clearing the interrupt state). Therefore, while CTSQ = 110 is retained, the CTRT interrupt for the completion of the setup stage is not generated, even when a new USB request is received. Events occurring after the setup stage are saved by the controller and the CTRT interrupt is generated after the interrupt state is cleared by software.



CTRT interrupt
(1) Setup stage end
(2) Control read transfer status stage transition
(3) Control write transfer status stage transition
(4) Control transfer complete
(5) Control transfer sequence error

Figure 32.8 Control Transfer Stage Transition

32.5 Pipe Control

Table 32.23 provides a list of pipe settings for the controller. In USB data transfers, data transmission is executed in logic pipes called endpoints. This controller comes with ten pipes for data transfer. Each pipe can be set to meet the requirements of the user system.

Table 32.23 Pipe Settings

Register Name	Bit Name	Setting	Remark
PIPECFG	TYPE	Specifies the transfer type	Can be set for pipes 1 to 9.
	BFRE	Selects BRDY interrupt mode	Can be set for pipes 1 to 5.
	DBLB	Selects double buffer configuration	Can be set for pipes 1 to 5.
	CNTMD	Selects continuous transfer or non-continuous transfer	Can be set for pipes 1 and 2 only in bulk transfers. Can be set for pipes 3 to 5.
	DIR	Selects transfer direction	Set to IN or OUT
	EPNUM	Endpoint number	Can be set for pipes 1 to 9. Set to a value other than 0000 when a pipe is in use.
	SHTNAK	Disables pipe when transfer is completed.	Can be set for pipes 1 and 2 only in bulk transfers. Can be set for pipes 3 to 5.
PIPEBUF	BUFSIZE	Buffer memory size	Cannot be set for DCP (fixed to 256 bytes). Up to 2 Kbytes can be set for pipes 1 to 5. Cannot be set for pipes 6 to 9 (fixed to 64 bytes).
	BUFNMB	Buffer memory number	Cannot be set for DCP (fixed at areas 0 to 3hex). Can be set for pipes 1 to 5 (specifiable in area ranging from 8 to 80hex). Cannot be set for pipes 6 to 9 (fixed at areas ranging from 4 to 7hex).
DCPMAXP PIPEMAXP	MXPS	Maximum packet size	Setting conforming to the USB standard
PIPEPERI	IFIS	Buffer flush	Can be set for pipes 1 and 2 only in isochronous transfers. Cannot be set for pipes 3 to 5. Cannot be set for pipes 6 to 9.
	IITV	Interval counter	Can be set for pipes 1 and 2 only in isochronous transfers. Cannot be set for pipes 3 to 5. Cannot be set for pipes 6 to 9.
DCPCTR PIPExCTR	BSTS	Buffer status	DCP state switched between receive and transmission buffer by ISEL bit
	INBUFM	IN buffer monitor	Available only for pipes 3 to 5.
	ATREPM	Auto response mode	Can be set for pipes 1 to 5.
	ACLRM	Auto buffer clear	Can be set for pipes 1 to 9.
	SQCLR	Sequence clear	Clears data toggle bit.
	SQSET	Sequence set	Sets data toggle bit.
	SQMON	Sequence check	Monitors data toggle bit.
	PBUSY	Pipe busy check	
	PID	Response PID	
PIPExTRE	TRENB	Transaction count enable	Can be set for pipes 1 to 5.
	TRCLR	Current transaction counter clear	Can be set for pipes 1 to 5.
PIPExTRN	TRNCNT	Transaction counter	Can be set for pipes 1 to 5.

32.5.1 Maximum Packet Size Setting

The MXPS bits in DCPMAXP and PIPEMAXP are used to specify the maximum packet size for each pipe. DCP and PIPE1 to PIPE5 can be set to any of the maximum packet sizes defined by the USB Specification. For PIPE6 to PIPE9, 64 bytes are the upper limit of the maximum packet size. The maximum packet size should be set before beginning the transfer (PID = BUF).
DCP: 64 should be set when using high-speed operation.
DCP: Select and set 8, 16, 32, or 64 when using full-speed operation.
Pipes 1 to 5: 512 should be set when using high-speed bulk transfer.
Pipes 1 to 5: Select and set 8, 16, 32, or 64 when using full-speed bulk transfer.
Pipes 1 to 2: Set a value between 1 and 1024 when using high-speed isochronous transfer.
Pipes 1 to 2: Set a value between 1 and 1023 when using full-speed isochronous transfer.
Pipes 6 to 9: Set a value between 1 and 64.

The high bandwidth transfers used with interrupt transfers and isochronous transfers are not supported.

32.5.2 Response PID

Set the response PID for each pipe with the PID bits of the DCPCTR and PIPExCTR registers.

(1) Response PID setting
The response PID specifies the response to a transaction from the Host.
(a) NAK setting: Always sends a NAK response when a transaction is issued.
(b) BUF setting: Responds to the transaction in accordance with the buffer memory state.
(c) STALL setting: Always sends a STALL response when a transaction is issued.
Regardless of the value set in the PID bit, an ACK is always sent as a response to a setup transaction and the USB request is stored in corresponding registers.

Based on the results of the transaction, the controller may trigger the PID bits to be written.
The controller will trigger a write event to the PID bit in the following cases.

- Hardware setting of response PID

(a) NAK setting:
1) When SETUP token is received normally (only DCP)
2) In bulk transfers when the SHTNAK bit of the PIPECFG register is set to 1 and short packet is received
3) In bulk transfers when SHTNAK bit is set to 1 and the transaction counter is completed.
(b) BUF setting: The BUF cannot be written by the controller.
(c) STALL setting:
1) When a maximum packet size over error is detected in the received data packet
2) When a control transfer sequence error is detected

32.5.3 Pipe Control Register Switching Procedures

The bits in the following pipe control registers can be re-written only when USB transmission is disabled (PID = NAK). Figure 32.9 shows the procedure for switching the pipe control register from the USB transmission enabled (PID = BUF) state.

Registers for which settings are prohibited when the USB transmission is enabled (PID = BUF):

- All bits of the DCPMAXP register
- Bits SQCLR and SQSET of the DCPCTR register
- All bits of the PIPECFG, PIPEBUF, PIPEMAXP and PIPEPERI registers
- ATREPM, ACLRM, SQCLR, and SQSET bits of the PIPExCTR register
- All bits of the PIPExTRE and PIPExTRN registers

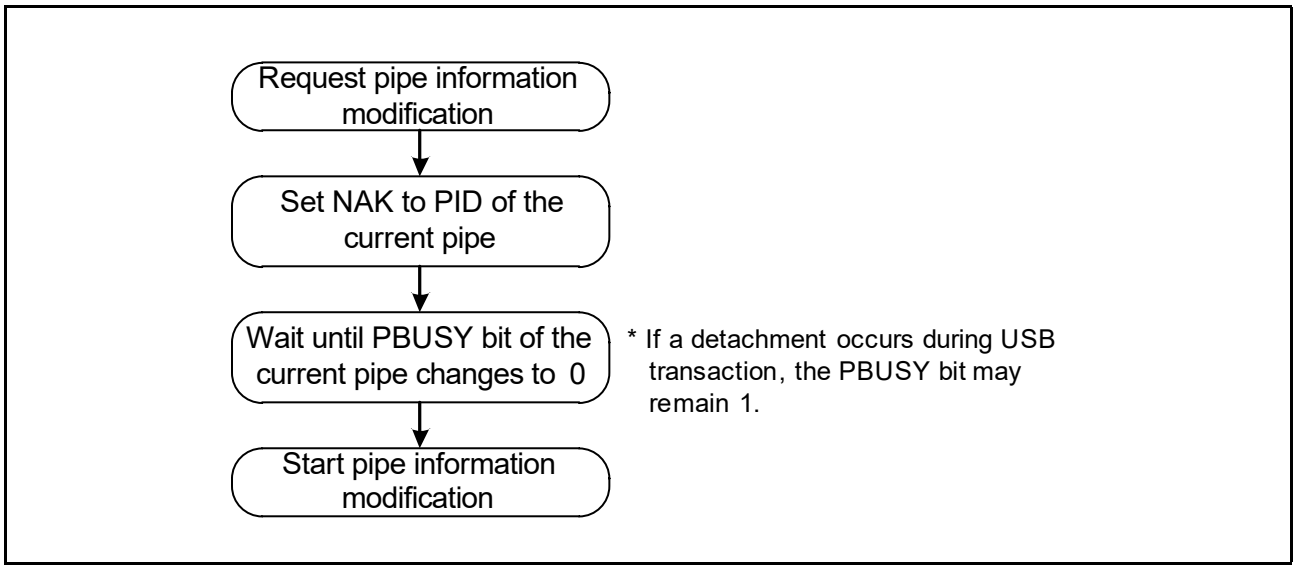


Figure 32.9 Procedure for Changing Pipe Information from USB Transmission Enabled (PID = BUF) State

In addition, the following bits of the pipe control registers can only be re-written with pipe information that is not set in the CURPIPE bits of CPU/DMA0/DMA1-FIFO ports.

Register for which settings are prohibited during setting of the CURPIPE bits in the FIFO port register:

- All bits of the DCPMAXP register
- All bits of the PIPECFG, PIPEBUF, PIPEMAXP and PIPEPERI registers
- Bit ACLRM of the PIPExCTR register

When modifying information of a pipe, specify other pipe number in the CURPIPE bits. Also, after setting the DCP pipe information, clear the buffer using the BCLR bit.

32.5.4 Data PID Sequence Bit

When a normal data transfer occurs in the control transfer data stage, bulk transfer or interrupt transfer, the controller automatically toggles the data PID sequence bit. The next data PID sequence bit for data transfer can be confirmed in the SQMON bit in the DCPCTR or PIPExCTR registers. The sequence bit is switched in the ACK handshake receive timing when data is sent or in the ACK handshake send timing when data is received. The data PID sequence bit can also be modified for the SQCLR and SQSET bits of the DCPCTR and PIPExCTR registers.
In control transfers, the controller automatically sets the sequence bit for stage transitions. DATA1 is established at the end of the setup stage. In the status stage, the controller does not reference the sequence bit and returns a response with PID = DATA1. Therefore, the bit does not need to be set with software. Note that the data PID sequence bit must be set with software when a ClearFeature request is received.
Finally, the sequence bit cannot be manipulated through the SQSET bit for the isochronous transfer setup pipe.

32.6 FIFO Buffers

This section describes the operation of the FIFO buffers in this controller.

32.6.1 FIFO Buffer Allocation

Figure 32.10 shows an example of memory map for the FIFO buffers of this controller. The FIFO buffer area is shared by the CPU controlling the user system and this controller. The access right of the FIFO buffers may be given to the user system (CPU side) or to this controller (SIE side).

An independent FIFO buffer area is allocated for each pipe. The memory area is made up of memory blocks of 64 bytes and defined by the starting block number (1 block is 64 bytes long) and the number of blocks (specified by the BUFNMB and BUFSIZE bits of the PIPEBUF register). If the CNTMD bit of the PIPExCFG register is set to continuous transfer mode, the value specified in the BUFSIZE bits must be an integral multiple of the maximum packet size. If the double buffer configuration is selected through the DBLB bit of the PIPExCFG register, two planes of memory area the size of which is specified by the BUFSIZE bits of the PIPEBUF register are allocated to a single pipe.

Two FIFO ports are used to access an FIFO buffer (data read/write). The pipe to be assigned to an FIFO port is designated by specifying the pipe number in the CURPIPE bits of the CFIFOSEL or DxFIFOSEL register.

The FIFO buffer state of each pipe can be confirmed by using the BSTS and INBUFM bits of the DCPCTR and PIPExCTR registers. The access right of a FIFO port can be confirmed by using the FRDY bit of the CFIFOCTR or DxFIFOCTR register.

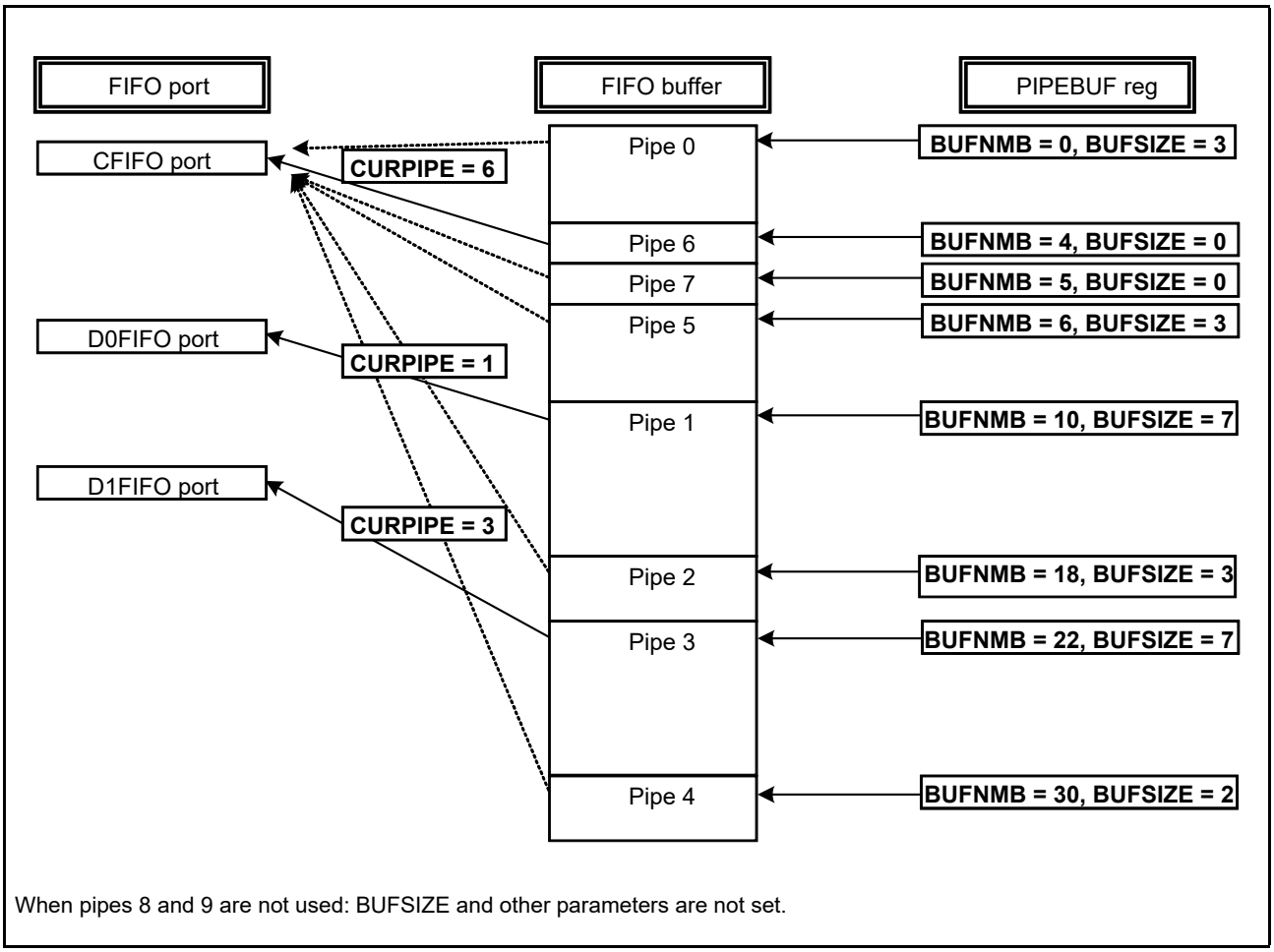


Figure 32.10 Example of FIFO Buffer Memory Map

32.6.2 Clearing FIFO Buffers

Table 32.24 shows a list of modes of clearing the FIFO buffers by this controller. The FIFO buffers can be cleared by the 3 bits that are listed in the table.

Table 32.24 List of FIFO Buffer Clearing Modes

Bit Name	BCLR	DCLRM	ACLRM
Register	CFIFOCTR register DxFIFOCTR register	DxFIFOSEL register	PIPExCTR register
Function	The FIFO buffer on the CPU side is cleared.	The FIFO buffer is automatically cleared after the data is read from the designated pipe.	The buffer is automatically cleared to discard all the received packets.
Clearing method	Write 1 to clear.	1: Mode valid 0: Mode invalid	1: Mode valid 0: Mode invalid

32.7 FIFO Port Function

This section describes FIFO port functions. Table 32.25 lists settings of FIFO port functions of this controller. If writing data is continued until the buffer becomes full (up to the maximum packet size in discontinuous transfer mode) during the data write access, the FIFO port automatically enters the state where data can be transmitted to the USB bus. To make data with a size less than the buffer full (the maximum packet size in discontinuous transfer mode) transmittable, write completion must be set by the BVAL bit in the CFIFOCTR or DxFIFOCTR register (DMA transfer: TEND signal of the DMAC (for details, see section 15, DMA Controller (DMACAa)). Furthermore, to transmit a zero-length packet, clear the buffer by the BCLR bit in the CFIFOCTR or DxFIFOCTR register and set write completion by the BVAL bit.
When all data has been read during the read access, the FIFO port automatically enters the state where a new packet can be received. However, when a zero-length packet is received (DTLN = 0), the data cannot be read. In that case, clear the buffer by the BCLR bit in the CFIFOCTR or DxFIFOCTR register. The receive data length is checked by the DTLN bits in the CFIFOCTR or DxFIFOCTR register.

Table 32.25 FIFO Port Function Settings

Register Name	Bit Name	Function	Notes
C/DxFIFOSEL	RCNT	DTLN read mode selection	
	REW	Buffer memory rewind (re-read, re-write)	
	DCLRM	Automatic clearing of buffer memory after specified pipe received data is read	DxFIFO only
	DREQE	DREQ signal assertion	DxFIFO only
	MBW	FIFO port access bit width	
	BIGEND	FIFO port endian selection	
	ISEL	FIFO port access direction	DCP only
	CURPIPE	Current pipe selection	
C/DxFIFOCTR	BVAL	Buffer memory write completion	
	BCLR	Clearing of CPU-side buffer memory	
	FRDY	Monitoring of FIFO port ready	
	DTLN	Confirmation of received data length	

32.7.1 FIFO Port Selection

Table 32.26 shows the list of pipes that can be selected in each FIFO port. The pipes to be accessed are selected with the CURPIPE bits of the CFIFOSEL or DxFIFOSEL register. After selecting the pipes, confirm that the value of the CURPIPE bits written was read correctly (if the previous pipe number is read out, this indicates the controller is still changing the pipe), then confirm that FRDY = 1 and access the FIFO port. Figure 32.11 shows the procedure for switching pipes for access to the FIFO port.
Also, select the bus width for the FIFO port access with the MBW bit. The buffer memory access direction is determined by the ISEL bit for DCP, and the DIR bit of the PIPExCFG register for all other pipes.

Table 32.26 FIFO Port Access by Pipe

Pipe	Access Method	Usable Ports
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	CFIFO port register
	DMA access	DxFIFO port register

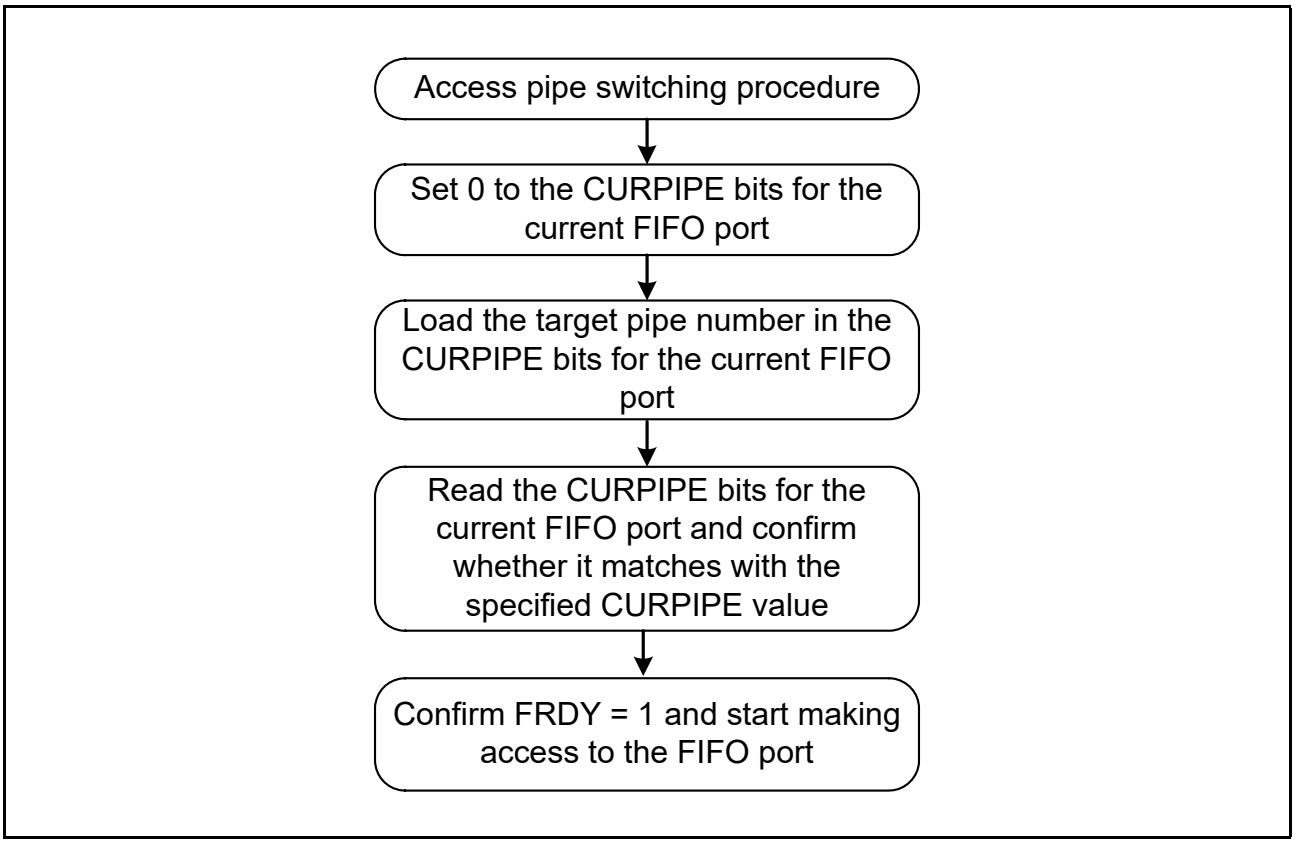


Figure 32.11 Pipe Switching Procedure for FIFO Port Access

32.7.2 DxFIFO Automatic Clear Mode (DxFIFO Port Read Direction)

When a data read event of the controller buffer memory is completed with setting the DCLRM bit of the DxFIFOSEL register to 1, the buffer memory of the corresponding pipe is automatically cleared.

Table 32.27 shows the correspondence between packet reception and buffer memory clearing by software in each setting.

As indicated in Table 32.27, the buffer clear conditions differ according to the set value of the BFRE bit, even for states in which clear is normally required, using the DCLRM bit eliminates the need for clearing of the buffer by software, enabling DMA transfers without the use of software.

Note that this function only supports the buffer memory read direction setting.

Table 32.27 Correspondence of Packet Reception and Buffer Memory Clearing by Software

Register Setting / Buffer State when Packet is Received	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Clearing not required	Clearing not required	Clearing not required	Clearing not required
Zero-length packet received	Clearing required	Clearing required	Clearing not required	Clearing not required
Normal short packet received	Clearing not required	Clearing required	Clearing not required	Clearing not required
Transaction count end	Clearing not required	Clearing required	Clearing not required	Clearing not required

32.7.3 BRDY Interrupt Timing Selection

The BFRE bit of the PIPECFG register can be set so that the BRDY interrupt is not generated when a data packet of maximum packet size is received.

When using a DMA transfer, this function enables an interrupt to be generated only when the last data is received. The last data indicates either a short packet reception or the transaction count end. By setting BFRE = 1, the BRDY interrupt will be generated after the received data is read. By reading the DTLN bit of the DnFIFOCTR register, the receive data length of last data packet received just before the BRDY interrupt was generated can be confirmed.

Table 32.28 shows the timing of the BRDY interrupt.

Table 32.28 BRDY Interrupt Generation Timing

Register Setting / Buffer State when Packet is Received	BFRE = 0	BFRE = 1
Buffer full (normal packet received)	When packet is received	No interrupt generated
Zero-length packet received	When packet is received	When packet is received
Normal short packet received	When packet is received	When read event of data received from buffer memory is completed
Transaction count end	When packet is received	When read event of data received from buffer memory is completed

The BFRE bit function is only valid in reading direction of the buffer memory. When in writing direction, fix the BFRE bit to 0.

32.8 Control Transfer (DCP)

Data transfers of the data stage of control transfers are done using the default control pipe (DCP). The DCP buffer memory is a 64-byte single buffer, and is a fixed area that is shared for both control reading and control writing. The buffer memory can be accessed only through the CFIFO port.

32.8.1 Setup Stage

The controller always responds with an ACK when it receives a normal setup packet. The controller operations in the setup stage are as follows.

(1) When a new setup packet is received, the controller sets the following bits.
  (a) Sets the VALID bit of the INTSTS0 register to 1.
  (b) Sets the PID bits of the DCPCTR register to NAK.
  (c) Sets the CCPL bit of the DCPCTR register to 0.
(2) When a data packet is received following the setup packet, the USB request parameters are stored in the following registers: USBREQ, USBVAL, USBINDX and USBLENG.

Always set VALID = 0 before the response process to a control transfer. While VALID = 1, PID = BUF will not be set and the data stage cannot be completed.
The function of the VALID bit allows the controller to temporarily stop a request in-process when it receives a new USB request during a control transfer, and respond to the newest request.

In addition, the controller automatically judges the direction bit (bmRequestType bit 8) and the request data length (wLength) of the received USB request and determines whether it is a control read transfer, control write transfer or control write no-data transfer, and then handles the stage transition. If the sequence is incorrect, a sequence error for the control transfer stage transition interrupt is generated and is notified to the software. For more information concerning the controller stage management, see Figure 32.8.

32.8.2 Data Stage

Use the DCP for data transfers in response to receiving a USB request. Before accessing the DCP buffer memory, set the access direction in the ISEL bit of the CFIFOSEL register.
The transaction is executed by setting the PID bits of the DCPCTR register to BUF.
Data transfer completion is detected by the BRDY and BEMP interrupts. Use the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.
For control write transfers in high-speed operation, a NYET handshake is sent in accordance with the buffer memory state.

32.8.3 Status Stage

When the setting of the PID bits of the DCPCTR register is BUF, set the CCPL bit to 1 to complete the control transfer. After the above settings, the controller automatically executes the status stage in accordance with the data transfer direction fixed in the setup stage. The detailed process is as follows.

(1) Control read transfers:
  The controller receives a zero-length packet from the USB host and sends an ACK response.
(2) Control write transfers and no-data control transfers:
  The controller sends a zero-length packet and receives an ACK response from the USB host controller.

32.8.4 Control Transfer Automatic Response

The controller automatically sends a response to a normal SET_ADDRESS request. If one of the following errors occurs, a response must be sent by software.

(1) bmRequestType ≠ 00h
(2) wIndex ≠ 00h
(3) wLength ≠ 00h
(4) wValue > 7Fh
(5) DVSQ = 011b (configured)

All requests other than the SET_ADDRESS request must be responded to by software.

32.9 Bulk Transfer (Pipes 1 to 5)

The user can select the buffer memory usage method (single/double buffer, continuous/non-continuous transfer mode) for bulk transfer. The maximum size that can be set for the buffer memory is 2 Kbytes. The controller manages the buffer memory state and automatically responds to PING packets and NYET handshakes.

32.9.1 NYET Handshake Control

Table 32.29 shows the list of responses to a token received in a bulk or control transfer. When an OUT token is received in a bulk or control transfer and there is only enough open space for one packet in the buffer memory, the controller sends a NYET response. However, when a short packet is received, the controller sends an ACK response instead of a NYET response, even under these conditions.

Table 32.29 List of Responses to Received Tokens

PID Bits Setting	Buffer Memory State	Received Token	Response	Notes
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY*1	OUT/PING	ACK	When OUT token is received, data packet is received.
	RCV-BRDY*2	OUT	NYET	Data packet is received.
	RCV-BRDY*2	OUT (Short)	ACK	Data packet is received.
	RCV-BRDY*2	PING	ACK	
	RCV-NRDY*3	OUT / PING	NAK	
	TRN-BRDY*4	IN	DATA0 / 1	Data packet is transmitted.
	TRN-NRDY*5	IN	NAK	

Note 1. RCV-BRDY: Buffer memory has enough space for 2 packets or more when an OUT or PING token is received.
Note 2. RCV-BRDY: Buffer memory has only enough space for one packet when an OUT token is received.
Note 3. RCV-NRDY: Buffer memory has not enough space when a PING token is received.
Note 4. TRN-BRDY: Buffer memory has data for transmission when an IN token is received.
Note 5. TRN-NRDY: Buffer memory does not have data for transmission when an IN token is received.

32.10 Interrupt Transfer (Pipes 6 to 9)

This controller executes an interrupt transfer in accordance with the period managed by the host controller. The controller ignores (no response) PING packets in interrupt transfers. In addition, the controller does not send a NYET handshake, but responds with ACK, NAK, or STALL.
The controller does not support high-bandwidth interrupt transfers.

32.11 Isochronous Transfer (Pipes 1 and 2)

The controller provides the following functions for isochronous transfers.

(1) Isochronous transfer error information notification
(2) Interval counter (IITV bit setting)
(3) Isochronous IN transfer data setup control (IDLY function)
(4) Isochronous IN transfer buffer flush function (IFIS bit setting)
(5) SOF pulse output function

The controller does not support high-bandwidth isochronous transfers.

32.11.1 Isochronous Transfer Error Detection

The controller manages isochronous transfer errors by software and therefore has the following error information detection functions. Table 32.30 and Table 32.31 describe the procedure in which errors are confirmed and the interrupts that are generated.

(1) PID error
When PID of the received packet is corrupted
(2) CRC error and bit stuffing error
When an error occurs in CRC of the received packet or when the bit stuffing is corrupted
(3) Maximum packet size over
This indicates the data size of the received packet is larger than the value set for the maximum packet size.
(4) Overrun and underrun
When there is no data in the buffer memory when an IN token is received in an IN-direction (send) transfer
When there is no empty space in the buffer memory when an OUT token is received in an OUT-direction (receive) transfer
(5) Interval error
The following will generate interval errors.
(a) When an IN token could not be received in the interval frame of an isochronous IN transfer
(b) When an OUT token could not be received in the interval frame of an isochronous OUT transfer

Table 32.30 Errors Detected in Token Reception/Transmission

Detection Priority	Error Type	Generated Interrupts and States at Time of Error Detection
1	PID error	No interrupt generated (ignored as corrupted packet)
2	CRC error or bit stuffing error	No interrupt generated (ignored as corrupted packet)
3	Overrun or underrun errors	NRDY interrupt is generated and OVRN bit is set. A zero-length packet is sent in response to an IN token. A data packet is not received in response to an OUT token.
4	Interval error	NRDY interrupt generated

Table 32.31 Errors Detected in Data Packet Reception

Detection Priority	Error Type	Generated Interrupts and States
1	PID error	No interrupt generated (ignored as corrupted packet)
2	CRC error or bit stuffing error	NRDY interrupt is generated and CRCE bit is set.
3	Maximum packet size over error	BEMP interrupt is generated and PID is set to STALL.

32.11.2 DATA-PID

This controller does not support high-bandwidth transfers. The following occurs in response to a received PID.

(1) IN direction:
  (a) DATA0: Transmitted as PID of the data packet
  (b) DATA1: Not transmitted
  (c) DATA2: Not transmitted
  (d) mDATA: Not transmitted

(2) OUT direction (in full-speed operation):
  (a) DATA0: Received successfully as PID of the data packet
  (b) DATA1: Received successfully as PID of the data packet
  (c) DATA2: The packet is ignored.
  (d) mDATA: The packet is ignored.

(3) OUT direction (in high-speed operation):
  (a) DATA0: Received successfully as PID of the data packet
  (b) DATA1: Received successfully as PID of the data packet
  (c) DATA2: Received successfully as PID of the data packet
  (d) mDATA: Received successfully as PID of the data packet

32.11.3 Interval Counter

32.11.3.1 Overview of Operation

The isochronous transfer interval can be set in the IITV bit of the PIPEPERI register. Table 32.32 shows the functions of the interval counter.

Table 32.32 Interval Counter Functions

Transfer Direction	Function	Detection Conditions
IN	Transfer buffer flush function	Cannot successfully receive IN token in interval frame during isochronous IN transfer.
OUT	Notifies that a token not being received	Cannot successfully receive OUT token in interval frame during isochronous OUT transfer.

Since the interval counting is performed upon reception of SOF or by the complemented SOF, the isochronism can be maintained even if the SOF is damaged. Frame intervals are set as 2^{IITV} (μ) frames.

32.11.3.2 Interval Counter Initialization

The controller initializes the interval counter under the following conditions.

(1) Hardware reset
Initializes the IITV bit.

(2) Clearing of the buffer memory by the ACLRM bit
This initializes the counter but not the IITV bit.

(3) USB bus reset

After the interval counter is initialized and a packet is successfully transferred, the interval count starts under the following conditions.

(1) SOF is received after data is sent in response to an IN token when PID = BUF.

(2) SOF is received after data is received in response to an OUT token when PID = BUF.

Note that the interval counter is not initialized in the following conditions.

(1) When the PID is set to NAK or STALL
The interval timer is not stopped at this time. The transaction will be attempted at the next interval.

(2) USB bus reset or USB suspend
The IITV bit is not initialized at this time. When the SOF is received, the count starts from the value before the reception.

32.11.4 Isochronous Transfer Transmission Data Setup

In the isochronous data transmission by this controller, after data is written to the buffer memory, the data packet can be sent out in the next frame after the SOF packet is detected. This function, called the isochronous transfer transmission data setup, allows specification of the frame that started transmission.
When the buffer memory is used for double buffering and writing to both buffers has been completed, only transfer from the first buffer to have received data can proceed. Therefore, even when several IN tokens are received in the same frame, only one packet of data is sent by the buffer memory.

When an IN token is received, if the buffer memory is ready for transmission, the data is transferred and a normal response is returned. However, if the buffer memory is not ready for transmission, a zero-length packet is sent and an underrun error occurs.

Figure 32.12 shows an example of transmission using the isochronous transfer transmission data setup function with this controller when IITV = 0 (for each frame) is set.

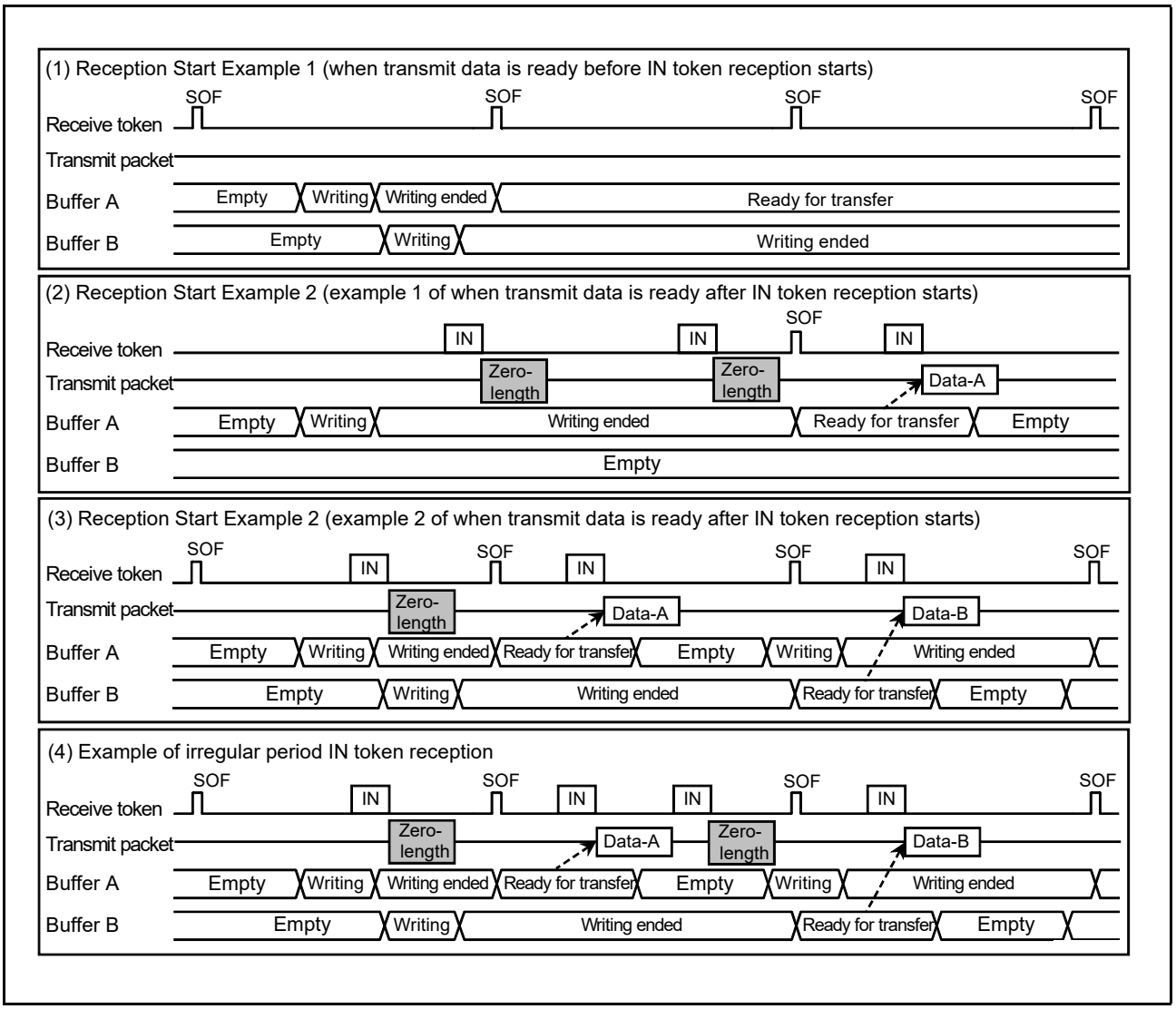


Figure 32.12 Example of Data Setup Function Operation

32.11.5 Isochronous Transfer Transmission Buffer Flush

When an SOF packet or a µSOF packet of the next frame is received without receiving an IN token in the interval frame during isochronous data transmission, this controller operates as if a corrupted IN token was received, and clears the buffer which is ready for transmission, making that buffer ready for writing.
If a double buffer is being used and writing to both buffers has been completed, data are considered to have been sent from the buffer memory that was cleared in the same interval frame, and transmission is enabled for the buffer memory that is not discarded with SOF or µSOF packets reception.
The timing at which the buffer flush function is activated varies depending on the setting of the IITV bits.

(1) When IITV = 0
The buffer flush operation proceeds from the first frame after the pipe becomes valid.

(2) When IITV ≠ 0
The buffer flush operation proceeds after the first successful transaction.

Figure 32.13 shows an operation example of the buffer flush function of this controller. When an unanticipated token is received prior to the interval frame, this controller sends the written data or a zero-length packet as an underrun error according to the data setup state.

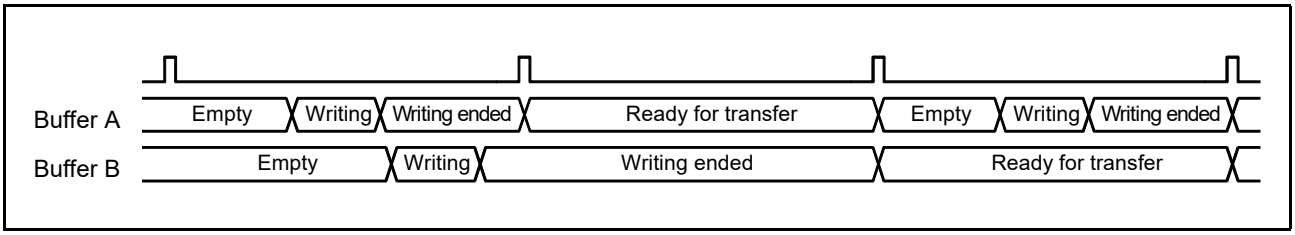


Figure 32.13 Buffer Flush Function Operation Example

Figure 32.14 shows an example of an interval error generated in the controller. There are five types of interval errors, as listed below. Timing 1 in the figure shows when the interval error occurs and how the buffer flush function operates.
When an interval error occurs during an IN transfer, the buffer flush function goes into operation; during an OUT transfer, the NRDY interrupt is generated.
Use the OVRN bit to determine whether an error is an NRDY interrupt, such as a receive packet error, or an overrun error.
Responses to the tokens in the shaded boxes are executed in accordance to the buffer memory state.

(1) IN direction:
  (a) If the buffer is ready for transfer, data is transferred as a normal response.
  (b) If the buffer is not ready for transfer, a zero-length packet is sent and an underrun error occurs.

(2) OUT direction:
  (a) If the buffer is ready for reception, data is received as a normal response.
  (b) If the buffer is not ready for reception, data is discarded and an overrun error occurs.

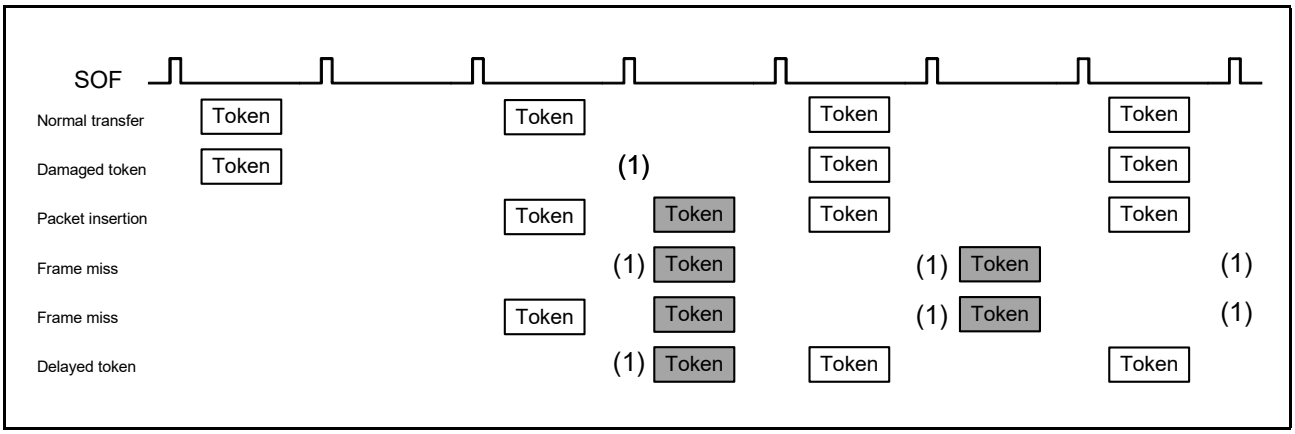


Figure 32.14 Example of Interval Error When IITV = 1

32.12 SOF Interpolation

If an SOF packet could not be received at intervals of 1 ms (in full-speed operation) or 125 µs (in high-speed operation) because of corruption or missing, this controller interpolates the SOF. The SOF interpolation operation begins when both the USBE and SUSPM bits have been set to 1 and an SOF packet is received. The interpolation is initialized under the following conditions.

(1) Hardware reset
(2) USB bus reset
(3) Suspended state detected

The SOF interpolation operates according to the following specifications.

(1) The frame interval (125 µs or 1 ms) is based on the results of the reset handshake protocol.
(2) The interpolation does not operate until the SOF packet is received.
(3) After a first SOF packet is received, interpolation of another SOF packet proceeds after a 125-µs or 1-ms interval counted in cycles of the internal clock running at 48 MHz clock has elapsed.
(4) Interpolation is performed in the previous reception intervals after the 2nd and subsequent SOF packets are received.
(5) Interpolation is not performed in the suspended state or during reception of a USB bus reset.
When the controller goes to the suspended state in high-speed operation, interpolation continues for 3 ms from the last packet.

The SOF interpolation works for the following.

(1) Updating of the frame number or micro-frame number
(2) SOFR interrupt and µSOF lock
(3) SOF pulse output
(4) Isochronous transfer interval count

When an SOF packet is lost during full-speed operation, the FRNM bit of the FRMNUM register is not updated.
When a µSOF packet is lost during high-speed operation, the UFRNM bit of the UFRMNUM register is updated. However, when a µSOF packet when µFRNM = 000b is lost, the FRNM bit is not updated. At this time, even if µSOF packets when µFRNM ≠ 000b are received successfully, the FRNM bit is not updated.

33. Serial Communications Interface with FIFO (SCIFA)

This LSI has five channels of serial communication interface (SCIFA) with FIFO that support both asynchronous and clock synchronous serial communication. The SCIFA has 16-stage FIFO buffers for transmission and reception, respectively, for each channel that enable this LSI to perform efficient high-speed continuous communication.

33.1 Overview

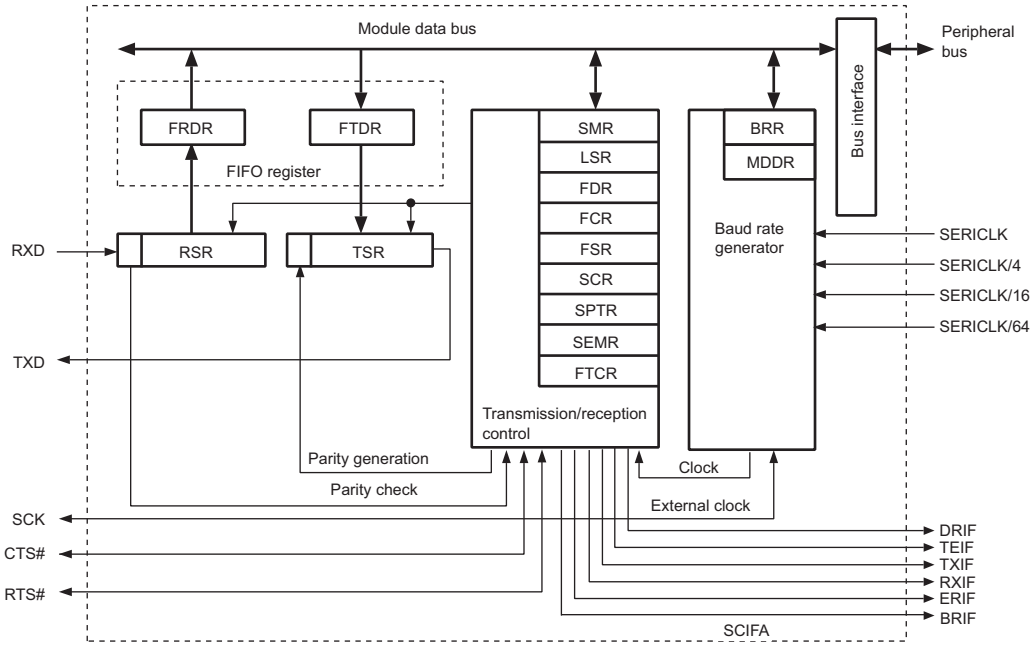
Table 33.1 lists the specifications of the SCIFA.

Table 33.1 Specifications of SCIFA

Item		Description
Channel		5 channels
Serial communication method		Asynchronous communication mode and clock synchronous communication mode
Transfer speed		Selectable bit rate with an on-chip baud rate generator
Full duplex communication		Transmitting section: realizes continuous data transmission using 16-stage FIFO buffer Receiving section: realizes continuous data reception using 16-stage FIFO buffer
Data transmission		Selectable either LSB-first or MSB-first transfer
Interrupt source		The following six sources: • Transmit-end (TEIF) • Transmit-FIFO-data-empty (TXIF) • Receive-FIFO-data-full (RXIF) • Receive-data-ready (DRIF)*1 • Framing error or parity error (ERIF) • Break or overrun (BRIF)
Asynchronous communication mode	Character length	7 or 8 bits
	Transmission stop bit length	1 or 2 bits
	Parity	Even, odd, or none
	Receive error detection	Detects following errors as receive error: parity error, overrun error, and framing error
	Hardware flow control	Controls data transmission and reception using the CTS# and RTS# pins.
	Break detection	Break signal detection function by hardware.
	Clock source	Selectable from internal or external clock
	Noise cancellation	Incorporates a digital noise filter in the RXD pin input path.
Clock synchronous communication mode	Character length	8 bits
	Receive error detection	Detects an overrun error as a receive error.
	Clock source	Selectable either internal or external clock
Bit rate modulation		Enables errors to be decreased by correcting the output of the on-chip baud rate generator.

Note 1. Effective only for asynchronous communication mode

Figure 33.1 shows a block diagram of the SCIFA.



RSR:	Receive shift register	BRR:	Bit rate register
FRDR:	Receive FIFO data register	SPTR:	Serial port register
TSR:	Transmit shift register	FCR:	FIFO control register
FTDR:	Transmit FIFO data register	FDR:	FIFO data count register
SMR:	Serial mode register	LSR:	Line status register
SCR:	Serial control register	SEMR:	Serial extended mode register
FSR:	Serial status register	FTCR:	FIFO trigger control register
MDDR:	Modulation duty register		

Figure 33.1 Block Diagram of SCIFA

Table 33.2 lists the input/output pins of the SCIFA.

Table 33.2 Pin Configuration of the SCIFA

Item	Pin Name	I/O	Function
Serial clock pin	SCK	I/O	Transmission/reception clock input/output, general output
Receive data pin	RXD	Input	Receive data input
Transmit data pin	TXD	Output	Transmit data output
Transmission/reception start control pin	CTS#	I/O	Input for hardware flow control (transmission enable signal) / general output
	RTS#	Output	Output for hardware flow control (transmission request signal) / general output

Note: Channels of each pin is omitted.

33.2 Register Descriptions

33.2.1 Receive Shift Register (RSR)

The RSR register receives serial data and temporally stores the data. The SCIFA stores the serial data input via the RXD pin into the RSR register. When one byte of data has been received, it is automatically transferred to the receive FIFO data register (FRDR).
The CPU cannot read from or write to the RSR register directly.

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

33.2.2 Receive FIFO Data Register (FRDR)

The FRDR register is an 8-bit, 16-stage FIFO register that stores the received serial data. When the SCIFA receives one byte of serial data, it transfers the received data from the receive shift register (RSR) to the FRDR register and completes the receive operation. Continuous reception is possible until the received 16 bytes of data are stored. If the FRDR register is read when there is no received data in the FRDR register, an undefined value is read.
When the FRDR register is full of received data, subsequently received serial data is lost.
The CPU can read the FRDR register but cannot write to it.

Address(es): SCIFA0.FRDR A006 500Ah, SCIFA1.FRDR A006 540Ah, SCIFA2.FRDR A006 580Ah, SCIFA3.FRDR A006 5C0Ah, SCIFA4.FRDR A006 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

33.2.3 Transmit Shift Register (TSR)

The SCIFA transfers the transmit data from the transmit FIFO data register (FTDR) to the TSR register, and then transmits the data serially to the TXD pin. After transmitting one byte of data, the SCIFA automatically transfers the next transmit data from the FTDR register into the TSR register and starts transmission.
The CPU cannot read from or write to the TSR register directly.

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

33.2.4 Transmit FIFO Data Register (FTDR)

The FTDR register is an 8-bit, 16-stage FIFO register that stores serial transmission data. When the SCIFA detects that the transmit shift register (TSR) is empty, it transmits data written in the FTDR register to the TSR register and starts serial transmission. Continuous serial transmission is executed until there is no transmit data left in the FTDR register. Writing the transmit data to the FTDR register should be done when a transmit data empty interrupt (TXIF) request is generated.

When the FTDR register becomes full of transmit data (16 bytes), no more data can be written. Even if new data is written, the data is ignored.

CPU can read from the FTDR register but cannot write to it.

Address(es): SCIFA0.FTDR A006 5006h, SCIFA1.FTDR A006 5406h, SCIFA2.FTDR A006 5806h, SCIFA3.FTDR A006 5C06h, SCIFA4.FTDR A006 6006h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

33.2.5 Serial Mode Register (SMR)

The SMR register specifies the SCIFA serial communication format and selects the clock source for the baud rate generator.

The CPU can always read and write to the SMR register.

Address(es): SCIFA0.SMR A006 5000h, SCIFA1.SMR A006 5400h, SCIFA2.SMR A006 5800h, SCIFA3.SMR A006 5C00h, SCIFA4.SMR A006 6000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CM	CHR	PE	PM	STOP	—	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1b0 0 0: 1 × SERICLK*1 0 1: 1/4 × SERICLK*1 1 0: 1/16 × SERICLK*1 1 1: 1/64 × SERICLK*1	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	STOP	Stop Bit Length	0: One stop bit 1: Two stop bits	R/W
b4	PM	Parity Mode	0: Even parity 1: Odd parity	R/W
b5	PE	Parity Enable	0: Parity bit addition or check is disabled. 1: Parity bit addition or check is enabled.	R/W
b6	CHR	Character Length	0: 8-bit data 1: 7-bit data*2	R/W
b7	CM	Communication Mode	0: Asynchronous mode 1: Clock synchronous mode	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. SERICLK: Peripheral clock

Note 2. When 7-bit data is selected, the MSB (bit 7) of the transmit FIFO data register is not transmitted.

CKS[1:0] Bits (Clock Select)

Select an internal clock source for the on-chip baud rate generator. For further information on the clock source, bit rate register settings, and baud rates, see section 33.2.8, Bit Rate Register (BRR).

STOP Bit (Stop Bit Length)

Selects one bit or two bits as the stop bit length in asynchronous mode. This setting is used only in asynchronous mode. It is ignored in clock synchronous mode because no stop bits are added. When receiving, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit, but if the second stop bit is 0, it is treated as the start bit of the next incoming character.

Note: When transmitting with one stop bit, a single 1 bit (stop bit) is added at the end of each transmission character.

Note: When transmitting with two stop bits, two 1 bits (stop bits) are added at the end of each transmission character.

PM Bit (Parity Mode)

Selects either the even or odd parity check. The setting of this bit is effective only when the parity enable (PE) bit of this register is set to 1 in asynchronous mode. The setting of this bit is ignored in clock synchronous mode, or when parity addition/check is disabled in asynchronous mode.

Note: If even parity is selected, the parity bit is added to data to be transmitted to make the total number of 1s even in the transmission character and parity bit combined. When receiving, the SCIFA verifies that the total number of 1s in the received character and parity bit combined is even.

Note: If odd parity is selected, the parity bit is added to data to be transmitted to make the total number of 1s odd in the transmission character and parity bit combined. When receiving, the SCIFA verifies that the total number of 1s in the received character and parity bit combined is odd.

PE Bit (Parity Enable)

Selects whether to add a parity bit on data transmission and whether to enable/disable the parity check on data reception in asynchronous mode. In clock synchronous mode, a parity bit is neither added nor checked, regardless of the setting of this bit.

Note: When this bit is set to 1, an even or odd parity bit specified in the PM bit is added to data to be transmitted. The SCIFA verifies whether the parity bit of the received data is even or odd as specified in the PM bit when receiving.

CHR Bit (Character Length)

Selects 7- or 8-bit data length in asynchronous mode. In clock synchronous mode, the data length is always 8 bits, regardless of the CHR setting.

CM Bit (Communication Mode)

Selects whether the SCIFA operates in asynchronous or clock synchronous mode.

33.2.6 Serial Control Register (SCR)

The SCR register enables or disables the SCIFA transmission/reception and interrupt requests, and selects the transmit/receive clock source. The CPU can always read from and write to the SCR register.

Address(es): SCIFA0.SCR A006 5004h, SCIFA1.SCR A006 5404h, SCIFA2.SCR A006 5804h, SCIFA3.SCR A006 5C04h, SCIFA4.SCR A006 6004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TIE	RIE	TE	RE	REIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	In asynchronous mode: b1 b0 0 0: Internal clock or SCK pin is used for input pin (input signal is ignored). The SCK pin state depends on the SCKIO and SCKDT bits in SPTR. 0 1: Internal clock or SCK pin is used for clock output (The output clock frequency is 16 or 8 times of the bit rate). 1 0: External clock or SCK pin is used for clock input (The input clock frequency is 16 or 8 times of the bit rate). 1 1: Setting prohibited In clock synchronous mode: b1 b0 0 0: Internal clock or SCK pin is used for synchronous clock output. 0 1: Internal clock or SCK pin is used for synchronous clock output. 1 0: External clock or SCK pin is used for synchronous clock input. 1 1: Setting prohibited	R/W
b2	TEIE*1	Transmit End Interrupt Enable	0: Transmit end interrupt (TEIF) request is disabled. 1: Transmit end interrupt (TEIF) request is enabled.	R/W
b3	REIE	Receive Error Interrupt Enable	0: Receive-error interrupt (ERIF) and break interrupt (BRIF) requests are disabled. 1: Receive-error interrupt (ERIF) and break interrupt (BRIF) requests are enabled.	R/W
b4	RE	Receive Enable	0: Data reception is disabled. 1: Data reception is enabled.	R/W
b5	TE	Transmit Enable	0: Data transmission is disabled. 1: Data transmission is enabled.	R/W
b6	RIE	Receive Interrupt Enable	0: Receive-FIFO-data-full interrupt (RXIF), receive-data ready interrupt (DRIF), receive-error interrupt (ERIF), and break interrupt (BRIF) requests are disabled. 1: Receive-FIFO-data-full interrupt (RXIF), receive-data ready interrupt (DRIF), receive-error interrupt (ERIF), and break interrupt (BRIF) requests are enabled.	R/W
b7	TIE	Transmit Interrupt Enable	0: Transmit-FIFO-data-empty interrupt request (TXIF) is disabled. 1: Transmit-FIFO-data-empty interrupt request (TXIF) is enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. TEIF interrupt requests can be cleared by reading 1 from the TEND flag, and then clearing the setting to 0, or by setting the TEIE bit to 0.

CKE[1:0] Bits (Clock Enable)

Select the SCIFA clock source and enable or disable clock output from the SCK pin. Depending on the settings of these bits, the SCK pin can be used for serial clock output or serial clock input. If the SCK pin is set for the synchronous clock output in the clock synchronous mode, set the CM bit in the SMR register to 1, and then set the CKE[1:0] bits. The settings of the CKE[1:0] bits are listed in Table 33.15.

REIE Bit (Receive Error Interrupt Enable)

Specifies whether to enable or disable a receive-error interrupt (ERIF) request and a break interrupt (BRIF) request. The setting of this bit is only valid when the RIE bit is set to 0.

Note: ERIF interrupt requests can be cleared by reading 1 from the ER bit in the FSR register, and then clearing the setting to 0, or by clearing both the RIE and REIE bits in this register to 0. BRIF interrupt requests can be cleared by reading 1 from the BRK bit in the FSR register, or from the ORER flag in the LSR register, and then clearing the setting to 0, or by clearing both the RIE and REIE bits in this register to 0.

RE Bit (Receive Enable)

Specifies whether to enable or disable the serial data reception.

Note: Setting this bit to 0 does not affect the receive flags (DR, ER, BRK, RDF, FER, and PER in the FSR register, and ORER in the LSR register). These flags retain their previous values.

Note: Serial reception starts when a start bit is detected in asynchronous mode, or a synchronous clock input is detected in clock synchronous mode. Before setting this bit to 1, be sure to set the serial mode register (SMR) and the FIFO control register (FCR) to select the receive format and reset the receive FIFO.

TE Bit (Transmit Enable)

Specifies whether to enable or disable the serial data transmission.

Note: Serial transmission starts after writing of data to be transmitted into the FTDR register under this condition. Before setting this bit to 1, be sure to set the serial mode register (SMR) and the FIFO control register (FCR) to select the transmit format and reset the transmit FIFO.

RIE Bit (Receive Interrupt Enable)

Specifies whether to enable or disable a receive-FIFO-data-full (RXIF) interrupt request when the RDF flag in the serial status register (FSR) is set to 1, a receive-data ready (DRIF) interrupt request when the DR flag in the FSR register is set to 1, a receive-error (ERIF) interrupt request when the ER flag in the FSR register is set to 1, and a break (BRIF) interrupt request when the BRK flag in the FSR register or the ORER flag in the line status register (LSR) is set to 1.

Note: RXIF interrupt requests can be cleared by reading 1 from the DR or RDF flag in the FSR register, then clearing the flag to 0, or by clearing the RIE bit to 0. DRIF interrupt requests can be cleared by reading 1 from the DR flag in the FSR register, and then clearing the setting to 0, or by clearing the RIE bit in this register to 0. Receive error interrupt (ERIF) requests and break interrupt (BRIF) requests can be cleared by clearing both the RIE and REIE bits in this register to 0.

TIE Bit (Transmit Interrupt Enable)

Specifies whether to enable or disable a transmit-FIFO-data-empty interrupt (TXIF) request when the serial transmit data is transferred from the transmit FIFO data register (FTDR) into the transmit shift register (TSR), the quantity of data in the transmit FIFO data register falls below the specified trigger number for transmission, and the TDFE flag in the serial status register (FSR) is set to 1.

Note: TXIF interrupt requests can be cleared either by writing a greater quantity of transmit data than the specified transmission trigger number into the FTDR register, reading 1 from the TDFE flag, and then clearing the TDFE flag to 0, or by clearing this bit to 0.

33.2.7 Serial Status Register (FSR)

The FSR register is a 16-bit register. The 8 lower-order bits indicate the status flag representing the SCIFA operating state.

The CPU can always read and write to the FSR register, but cannot write 1 to the status flags (ER, TEND, TDFE, BRK, RDF, and DR bits) in this register. These flags can be only cleared to 0 when they have first been read (after being set to 1). b3 (FER) and b2 (PER) are read-only bits that cannot be written.

Address(es): SCIFA0.FSR A006 5008h, SCIFA1.FSR A006 5408h, SCIFA2.FSR A006 5808h, SCIFA3.FSR A006 5C08h, SCIFA4.FSR A006 6008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DR	Receive Data Ready Flag	0: Reception is in progress, or no received data has remained in the FRDR register after normally completed receiving. 1: Next receive data has not been received.	R/(W) *1
b1	RDF	Receive FIFO Data Full Flag	0: The quantity of receive data in the FRDR register falls below the specified reception trigger number. 1: The quantity of receive data written in the FRDR register is equal to or greater than the specified reception trigger number.	R/(W) *1
b2	PER	Parity Error Flag	0: No receive parity error occurred in the next receive data read from the FRDR register. 1: A receive parity error occurred in the next receive data read from the FRDR register.	R
b3	FER	Framing Error Flag	0: No receive framing error occurred in the next data read from the FRDR register. 1: A receive framing error occurred in the next data read from the FRDR register.	R
b4	BRK	Break Detect Flag	0: No break signal is received. 1: A break signal is received.*2	R/(W) *1
b5	TDFE	Transmit FIFO Data Empty Flag	0: The quantity of transmit data written in the FTDR register exceeds the specified transmission trigger number. 1: The quantity of transmit data written in the FTDR register is equal to or less than the specified transmission trigger number.*3	R/(W) *1
b6	TEND	Transmit End Flag	0: Transmission is in the waiting state or in progress. 1: Transmission is completed.	R/(W) *1
b7	ER	Receive Error Flag	0: Reception is in progress or has normally completed. 1: A framing error or parity error has occurred during reception.	R/(W) *1
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. 0 can be only written to clear the flag after 1 is read.

Note 2. When a break signal is detected, transfer of the receive data (00h) to the FRDR register stops after the detection. When the break ends and the receive signal becomes mark state (high level), the transfer of receive data resumes.

Note 3. Since the FTDR register is a 16-byte FIFO register, the maximum quantity of data that can be written when TDFE is 1 is “16 minus the number of non-transmitted data units”. If additional data is written, the data is ignored. The quantity of data in the FTDR register is indicated by the 8 higher-order bits of the FDR register.

DR Bit (Receive Data Ready Flag)

Indicates that the quantity of data stored in the receive FIFO data register (FRDR) falls below the specified reception trigger number, and that no next data has been received yet after the elapse of 15 ETUs*1 from the last stop bit in asynchronous mode. In clock synchronous mode, this bit is not set to 1.

[Setting condition]

- DR is set to 1 when the FRDR register contains less data than the specified reception trigger number*2, and no next data has been received yet after the elapse of 15 ETUs*1 from the last stop bit.

[Clearing conditions]

When either of the following is satisfied:

- DR is cleared to 0 when DR = 1 is read and then 0 is written to the DR flag.
- DR is cleared to 0 when all received data in the FRDR register are read.

Note 1. This is equivalent to one and a half (1.5) frames in the 8-bit format with one stop bit (ETU: elementary time unit).
Note 2. The clearing condition takes precedence when all received data in the FRDR register are read.
Note: When the RE bit in SCR is cleared to 0, the DR bit is not affected and retains its previous value.

RDF Bit (Receive FIFO Data Full Flag)

Indicates that receive data has been transferred to the receive FIFO data register (FRDR), and the quantity of data in FRDR becomes equal to or greater than the specified reception trigger number.

[Setting condition]

- RDF is set to 1 when the quantity of receive data which is equal to or greater than the specified reception trigger number are stored in the FRDR register*1.

[Clearing condition]

- RDF is cleared to 0 when the FRDR register is read until the quantity of receive data in the FRDR register falls below the specified reception trigger number after 1 is read from RDF and then 0 is written to this bit.

Note 1. Since the FRDR register is a 16-byte FIFO register, the maximum quantity of data that can be read when this bit is 1 is equivalent to the specified reception trigger number. If an attempt is made to read after all the data in the FRDR register has been read, the read data is undefined. The quantity of receive data in the FRDR register is indicated by the 8 lower-order bits of the FDR register.

PER Bit (Parity Error Flag)

Indicates whether there is a parity error in the data read from the receive FIFO data register (FRDR) in asynchronous mode.

[Setting condition]

- PER is set to 1 when a parity error is present in the next data read from the FRDR register.

[Clearing condition]

- PER is cleared to 0 when no parity error is present in the next data read from the FRDR register.

FER Bit (Framing Error Flag)

Indicates whether there is a framing error in the data read from the receive FIFO data register (FRDR) in asynchronous mode.

[Setting condition]

- FER is set to 1 when a framing error is present in the next data read from the FRDR register.

[Clearing condition]

- FER is cleared to 0 when no framing error is present in the next data read from the FRDR register.

BRK Bit (Break Detect Flag)

Indicates that a break signal has been detected in receive data.

[Setting condition]

- BRK is set to 1 when data including a framing error is received, and the framing error is followed by at least one frame of data received at the space 0 level (low level).

[Clearing condition]

- BRK is cleared to 0 when software reads BRK after it has been set to 1 and then writes 0 to BRK.

TDFE Bit (Transmit FIFO Data Empty Flag)

Indicates that data has been transferred from the transmit FIFO data register (FTDR) into the transmit shift register (TSR), the quantity of data in the FTDR register becomes equal to or less than the specified transmission trigger number, and writing of transmit data to the FTDR register is enabled.

[Setting conditions]

When either of the following is satisfied:

- TDFE is set to 1 when the TE bit in SCR is 0.
- TDFE is set to 1 when the quantity of transmit data written in the FTDR register is equal to or less than the specified transmission trigger number.

[Clearing condition]

- TDFE is cleared to 0 when 0 is written in the TDFE bit after reading TDFE = 1.

TEND Bit (Transmit End Flag)

Indicates that the FTDR register contains no more valid data and transmission is completed when transmitting the last bit of the transmit data.

[Setting condition]

- TEND is set to 1 when the FTDR register does not contain transmit data when the last bit of the serial transmission data is transmitted.

[Clearing conditions]

When either of the following is satisfied:

- When transmit data is written to the FTDR register
- When 0 is written to TEND after it has been read as 1

ER Bit (Receive Error Flag)

Indicates the occurrence of a framing error, or of a parity error when receiving the parity-added data*1.

[Setting conditions]

When either of the following is satisfied:

- ER is set to 1 when the stop bit is found to be 0 after checking whether the stop bit of the received data is 1 at the end of one data receive operation*2.
- ER is set to 1 when the total number of 1s in the received data and parity bit combined does not match the even or odd parity setting specified by the PM bit in the SMR register.

[Clearing condition]

- When 0 is written to ER after it has been read as 1

Note 1. Clearing the RE bit to 0 in the SCR register does not affect this bit, which retains its previous value. Even if a receive error occurs, the receive data is transferred to the FRDR register and the receive operation is continued. Whether the data read from the FRDR register includes a receive error can be detected by the FER and PER bits in the FSR register.

Note 2. In two stop bits mode, only the first stop bit is checked; the second stop bit is not checked.

33.2.8 Bit Rate Register (BRR)

The BRR register is an 8-bit register that, together with the baud rate generator clock source selected by the CKS[1:0] bits in the serial mode register (SMR), determines the serial transmit/receive bit rate.
This register is located in the same address as that of the MDDR register and selected when the MDDRS bit in SEMR is 0. The CPU can read and write to BRR. Writing to BRR should be executed when TE = RE = 0 in the SCR register.

Address(es): SCIFA0.BRR A006 5002h, SCIFA1.BRR A006 5402h, SCIFA2.BRR A006 5802h, SCIFA3.BRR A006 5C02h, SCIFA4.BRR A006 6002h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The BRR setting is calculated using the following formulae.
[Asynchronous mode]

- When the baud rate generator is in normal mode (SEMR.BGDM = 0):

$$N = \frac{SERICLK}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$N = \frac{SERICLK}{32 \times 2^{2n-1} \times B} \times 10^6 - 1$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

- When the baud rate generator is in double-speed mode (SEMR.BGDM = 1):

$$N = \frac{SERICLK}{32 \times 2^{2n-1} \times B} \times 10^6 - 1$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$N = \frac{SERICLK}{16 \times 2^{2n-1} \times B} \times 10^6 - 1$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

[Clock synchronous mode]

$$N = \frac{SERICLK}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B: Bit rate (bit/s)
N: Setting of the BRR register (0 ≤ N ≤ 255) (The setting must satisfy the electrical characteristics).
SERICLK: Operating frequency for peripheral modules (MHz)
n: Baud rate generator clock source (n = 0, 1, 2, 3) (For the clock sources and values of n, see Table 33.3).

Note: The MDDR register is used to adjust the bit rate. For details, see section 33.2.9, Modulation Duty Register (MDDR).

Table 33.3 SMR Register Setting

		Setting of SMR.CKS [1:0] Bits	
n	**Clock Source**	**b1**	**b0**
0	SERICLK	0	0
1	SERICLK/4	0	1
2	SERICLK/16	1	0
3	SERICLK/64	1	1

The bit rate error in asynchronous mode is calculated using the following formulae.

- When the baud rate generator is in normal mode (SEMR.BGDM = 0):

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{(N + 1) \times B \times 32 \times 2^{2n-1}} - 1 \right\} \times 100$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

- When the baud rate generator is in double-speed mode (SEMR.BGDM = 1):

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{(N + 1) \times B \times 32 \times 2^{2n-1}} - 1 \right\} \times 100$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{(N + 1) \times B \times 16 \times 2^{2n-1}} - 1 \right\} \times 100$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

Table 33.4 list the examples of the BRR register setting in asynchronous mode, and Table 33.5 list the examples of the BRR register setting in clock synchronous mode.

Table 33.4 Bit Rates and BRR Register Settings in Asynchronous Mode

Bit Rate (bps)	SERICLK (MHz)					
	120			150		
	n	N	Error (%)	n	N	Error (%)
150						
300	3	194	0.16	3	243	0.06
600	3	97	-0.35	3	121	0.06
1200	2	194	0.16	2	243	0.06
2400	2	97	-0.35	2	121	0.06
4800	1	194	0.16	1	243	0.06
9600	1	97	-0.35	1	121	0.06
14400	1	64	0.16	1	80	0.47
19200	0	194	0.16	0	243	0.06
28800	0	129	0.16	0	162	-0.15
31250	0	119	0	0	149	0
38400	0	97	-0.35	0	121	0.06
115200				0	40	-0.76
500000						

Note: These values assume bits SEMR.ABCS0 and SEMR.BGDM are both 0. When either the SEMR.ABCS0 bit or SEMR.BGDM bit is set to 1, the bit rate is doubled. When bits SEMR.ABCS0 and SEMR.BGDM are both 1, the bit rate is quadrupled. Configure settings so the range of error is no greater than 1%.
Values for the blank cells in the table can be set using the MDDR register. For details, see section 33.2.9, Modulation Duty Register (MDDR) and the Table 33.10.

Table 33.5 Bit Rates and BRR Register Settings in Clock Synchronous Mode

Bit Rate (bps)	SERICLK (MHz)			
	120		150	
	n	N	n	N
250				
500				
1000				
2500	3	187	3	233
5000	3	93	3	116
10000	2	187	2	233
25000	2	74	2	93
50000	1	149	1	187
100000	1	74	1	93
250000	0	119	0	149
500000	0	59	0	74
1000000	0	29	0	37
2500000	0	11	0	14
5000000	0	5	0	7

Blank: Setting is prohibited.
Note: Set the BRR register so that the range of error can fall within 1% or less.

Table 33.6 lists the maximum bit rates for various frequencies in asynchronous mode when the baud rate generator is used. Table 33.7 lists the maximum bit rates for various frequencies in clock synchronous mode when the baud rate generator is used. Table 33.8 and Table 33.9 list the maximum rates for external clock inputs in asynchronous mode and clock synchronous mode, respectively.

Table 33.6 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (in Asynchronous Mode)

SERICLK (MHz)	Maximum Bit Rate (bit/s)	Settings	
		n	N
120	15000000	0	0
150	18750000	0	0

Note: These values assume bits SEMR.ABCS0 and SEMR.BGDM are both 1. When either the SEMR.ABCS0 bit or SEMR.BGDM bit is set to 1, the bit rate is 1/2. When bits SEMR.ABCS0 and SEMR.BGDM are both 0, the bit rate is 1/4.

Table 33.7 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (in Clock Synchronous Mode)

SERICLK (MHz)	Discontinuous Transmission/Reception			Continuous Transmission/Reception		
	Maximum Bit Rate (bit/s)	Settings		Maximum Bit Rate (bit/s)	Settings	
		n	N		n	N
120	30000000	0	0	15000000	0	1
150	37500000	0	0	18750000	0	1

Table 33.8 Maximum Bit Rates with External Clock Input (in Asynchronous Mode)

SERICLK (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
120	30	3750000
150	37.5	4687500

Note: This is an example when the SEMR.ABCS0 bit is 1. When the ABCS0 bit is set to 0, the bit rate is 1/2 .

Table 33.9 Maximum Bit Rates with External Clock Input (in Clock Synchronous Mode)

SERICLK (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
120	10	10000000
150	12.5	12500000

33.2.9 Modulation Duty Register (MDDR)

The MDDR register corrects the bit rate adjusted by the BRR register. The value after reset of this register is FFh. When the BRME bit in SEMR is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected according to the settings of MDDR (MDDR/256). The relationship between the MDDR register setting and the bit rate (B) is given by the following formula. The MDDR register is located in the same address as that of the BRR register and is selected when the MDDRS bit in SEMR is 1. This register is only writable when TE = RE = 0 in the SCR register. b7 in this register is fixed to 1.

Address(es): SCIFA0.MDDR A006 5002h, SCIFA1.MDDR A006 5402h, SCIFA2.MDDR A006 5802h, SCIFA3.MDDR A006 5C02h, SCIFA4.MDDR A006 6002h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The formulae below show the relationships between the MDDR setting and the bit rate (B) when the bit rate modulation function is used.

[Asynchronous mode]

- When the baud rate generator is in normal mode (SEMR.BGDM = 0):

$$B = \frac{SERICLK \times 10^6}{64 \times 2^{2n-1} \times (256/MDDR) \times (N + 1)}$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$B = \frac{SERICLK \times 10^6}{32 \times 2^{2n-1} \times (256/MDDR) \times (N + 1)}$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

- When the baud rate generator is in double-speed mode (SEMR.BGDM = 1):

$$B = \frac{SERICLK \times 10^6}{32 \times 2^{2n-1} \times (256/MDDR) \times (N + 1)}$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$B = \frac{SERICLK \times 10^6}{16 \times 2^{2n-1} \times (256/MDDR) \times (N + 1)}$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

[Clock synchronous mode]

$$B = \frac{SERICLK \times 10^6}{8 \times 2^{2n-1} \times (256/MDDR) \times (N + 1)}$$

When the bit rate modulation is used, the bit rate average error is given by the following formulae.

- When the baud rate generator is in normal mode (SEMR.BGDM = 0):

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/\text{MDDR}) \times (N+1)} - 1 \right\} 100$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/\text{MDDR}) \times (N+1)} - 1 \right\} 100$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

- When the baud rate generator is in double-speed mode (SEMR.BGDM = 1):

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/\text{MDDR}) \times (N+1)} - 1 \right\} 100$$

(When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0))

$$\text{Error (\%)} = \left\{ \frac{\text{SERICLK} \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/\text{MDDR}) \times (N+1)} - 1 \right\} 100$$

(When operating on the base clock with a frequency 8 times the bit rate (SEMR.ABCS0 = 1))

B: Bit rate (bits/s)
N: BRR register setting (0 ≤ N ≤ 255)
(The setting must satisfy the electrical characteristics).
SERICLK: Operating frequency for peripheral modules (MHz)
MDDR: MDDR setting (128 ≤ MDDR ≤ 255)
n: Baud rate generator clock source (n = 0, 1, 2, 3) (For the clock sources and values of n, see Table 33.3).

Table 33.10 Bit Rates and Settings of BRR and MDDR Registers in Asynchronous Mode

Bit Rate (bps)	SERICLK (MHz)							
	120				150			
	n	N	MDDR	Error (%)	n	N	MDDR	Error (%)
150	3	205	135	-0.003	3	247	130	-0.018
300	3	176	232	0.001	3	205	216	-0.003
600	2	205	135	-0.003	3	102	216	-0.003
1200	2	176	232	0.001	2	205	216	-0.003
2400	1	205	135	-0.003	2	102	216	-0.003
4800	1	176	232	0.001	1	205	216	-0.003
9600	0	205	135	-0.003	1	102	216	-0.003
14400	0	176	174	0.001	0	205	162	-0.003
19200	0	176	232	0.001	0	205	216	-0.003
28800	0	117	232	0.001	0	102	162	-0.003
31250	0	59	128	0.000	0	74	128	0.000
38400	0	73	194	0.007	0	102	216	-0.003
115200	0	21	173	-0.009	0	23	151	0.003
500000	0	6	239	0.028	0	6	151	-0.077

Note: These values assume bits SEMR.ABCS0 and SEMR.BGDM are both 0. When either the SEMR.ABCS0 bit or SEMR.BGDM bit is set to 1, the bit rate is doubled. When bits SEMR.ABCS0 and SEMR.BGDM are both 1, the bit rate is quadrupled. Configure settings so the range of error is no greater than 1%.

33.2.10 FIFO Control Register (FCR)

The FCR register resets the quantity of data in the transmit FIFO data register (FTDR) and the receive FIFO data register (FRDR) and specifies the number of triggers. This register also specifies whether to enable the loop-back test.
The CPU can always read and write to the FCR register.

Address(es): SCIFA0.FCR A006 500Ch, SCIFA1.FCR A006 540Ch, SCIFA2.FCR A006 580Ch, SCIFA3.FCR A006 5C0Ch, SCIFA4.FCR A006 600Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	RSTRG[2:0]			RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RFRST	LOOP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LOOP	Loop-Back Test	0: Loop back test is disabled. 1: Loop back test is enabled.	R/W
b1	RFRST	Receive FIFO Data Register Reset	0: Normal operation 1: Resets the FRDR register.	R/W
b2	TFRST	Transmit FIFO Data Register Reset	0: Normal operation 1: Resets the FTDR register.	R/W
b3	MCE	Modem Control Enable	0: Modem signal is disabled.*1 1: Modem signal is enabled.	R/W
b5, b4	TTRG[1:0]	Transmit FIFO Data Trigger Number Select	b5 b4 0 0: 8 (8)*2 0 1: 4 (12)*2 1 0: 2 (14)*2 1 1: 0 (16)*2	R/W
b7, b6	RTRG[1:0]	Receive FIFO Data Trigger Number Select	In asynchronous mode: b7 b6 0 0: 1 0 1: 4 1 0: 8 1 1: 14 In clock synchronous mode: b7 b6 0 0: 1 0 1: 2 1 0: 8 1 1: 14	R/W
b10 to b8	RSTRG[2:0]	RTS# Output Active Trigger Number Select	b10 b8 0 0 0: 15 0 0 1: 1 0 1 0: 4 0 1 1: 6 1 0 0: 8 1 0 1: 10 1 1 0: 12 1 1 1: 14	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The CTS# input level does not affect the transmit operation. Similarly, the RTS# input level does not affect the receive operation.
Note 2. Values in parentheses mean the number of empty bytes in the FTDR register when the TDFE flag is set to 1 and a transmit FIFO data empty interrupt (TXIF) request is generated.

LOOP Bit (Loop-Back Test)

Internally connects between the transmit output pin (TXD) and the receive input pin (RXD) and between the RTS# pin and the CTS# pin, to perform loop-back testing.

RFRST Bit (Receive FIFO Data Register Reset)

Disables the receive data in the receive FIFO data register (FRDR) and makes the data to the empty state. If you set this bit to 1, be sure to clear it to 0 afterward.

TFRST Bit (Transmit FIFO Data Register Reset)

Disables the transmit data in the transmit FIFO data register (FTDR) and makes the data to the empty state. If you set this bit to 1, be sure to clear it to 0 afterward.

MCE Bit (Modem Control Enable)

Specifies whether to enable or disable the modem control signals, CTS# and RTS#.
In clock synchronous mode, this bit should always be set to 0.

TTRG[1:0] Bits (Transmit FIFO Data Trigger Number Select)

Specify the reference quantity of data for transmission (i.e., the threshold number of entries to trigger the writing of further data for transmission) for setting of the TDFE flag in the serial status register (FSR). When the number of entries for transmission in the transmission FIFO, i.e. the number of entries written to the transmit FIFO data register (FTDR) that are yet to be transmitted, falls to or below the number specified by the TTRG[1:0] bits, the TDFE flag is set to 1 and a transmit FIFO data empty interrupt (TXIF) request is generated.
The setting in these bits is valid when the TTRGS bit in the FTCR register is 0. When the TTRGS bit in the FTCR register is 1, the setting of the TFTC[4:0] bits in the FTCR register is valid.

RTRG[1:0] Bits (Receive FIFO Data Trigger Number Select)

Specify the reference quantity of receive data (i.e., the threshold number of entries to trigger the reading of received data) for setting of the RDF flag in the serial status register (FSR). When the number of entries in the reception FIFO, i.e. the number of entries yet to be read from the receive FIFO data register (FRDR), rises to or above the number specified by the RTRG[1:0] bits, the RDF flag is set to 1 and a receive FIFO data full interrupt (RXIF) request is generated.
The setting in these bits is valid when the RTRGS bit in the FTCR register is 0. When the RTRGS bit in the FTCR register is 1, the setting of the RFTC[4:0] bits in the FTCR register is valid.

RSTRG[2:0] Bits (RTS# Output Active Trigger Number Select)

When the number of entries in the reception FIFO, i.e. the number of entries yet to be read from the receive FIFO data register (FRDR), rises to or above the trigger number specified by the RSTRG[2:0] bits, the RTS# signal is in the high state.
The setting in these bits is only valid when a modem signal is enabled by the MCE bit in this register in asynchronous mode.

33.2.11 FIFO Data Count Register (FDR)

The FDR register indicates the quantity of data stored in the transmit FIFO data register (FTDR) and the receive FIFO data register (FRDR).

This register indicates the quantity of transmit data in the FTDR register with the 8 higher-order bits, and the quantity of receive data in the FRDR register with the 8 lower-order bits. The CPU can always read the FDR register but cannot write to it.

Address(es): SCIFA0.FDR A006 500Eh, SCIFA1.FDR A006 540Eh, SCIFA2.FDR A006 580Eh, SCIFA3.FDR A006 5C0Eh, SCIFA4.FDR A006 600Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	R[4:0]	Receive Data Quantity in FRDR	Indicate the quantity of receive data stored in the FRDR register.	R
b7 to b5	—	Reserved	These bits are read as 0.	R
b12 to b8	T[4:0]	Non-Transmitted Data Quantity in FTDR	Indicate the quantity of non-transmitted data stored in the FTDR register.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

R[4:0] Bits

Indicate the quantity of receive data stored in the FRDR register.

00h means no received data, and 10h means that all of the received data is stored in the FRDR register.

T[4:0] Bits

Indicate the quantity of non-transmitted data stored in the FTDR register.

00h means no transmit data, and 10h means that all of the data for transmission is stored in the FTDR register.

33.2.12 Serial Port Register (SPTR)

The SPTR register controls input/output and data of the pins multiplexed to SCIFA function.
The CPU can always read and write to the SPTR register.

Note: b6, b4, b2, and b0 of this register respectively indicate the input status of their corresponding pins. See the descriptions for each bit for details. Writings to these bits in 1-bit unit are handled as read-modify-write, which may lead to undesired values to be written. To avoid this, when modifying the SPB2DT or SPB2IO bit, for example, write the other bit (the bit used in combination) at the same time.

Address(es): SCIFA0.SPTR A006 5010h, SCIFA1.SPTR A006 5410h, SCIFA2.SPTR A006 5810h, SCIFA3.SPTR A006 5C10h, SCIFA4.SPTR A006 6010h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RTS2IO	RTS2DT	CTS2IO	CTS2DT	SCKIO	SCKDT	SPB2IO	SPB2DT
Value after reset:	0	0	0	0	0	0	0	0	0	x	0	x	0	x	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	SPB2DT	Serial Port Break Data Select	Controls the TXD pin in combination with the TE bit in the SCR register and the SPB2IO bit. See Table 33.13.	R/W
b1	SPB2IO	Serial Port Break Input/Output	Controls the TXD pin in combination with the TE bit in the SCR register and the SPB2DT bit.	R/W
b2	SCKDT	SCK Port Data Select	Controls the SCK pin in combination with the CM bit in the SMR register, the SCKIO bit, and the CKE1 and CKE0 bits in the SCR register. See Table 33.15.	R/W
b3	SCKIO	SCK Port Input/Output	Controls the SCK pin in combination with the CM bit in the SMR register, the SCKDT bit, and the CKE1 and CKE0 bits in the SCR register. See Table 33.15.	R/W
b4	CTS2DT	CTS# Port Data Select	Controls the CTS# pin in combination with MCE bit in FCR and CTS2IO bit. See Table 33.12.	R/W
b5	CTS2IO	CTS# Port Output Specify		R/W
b6	RTS2DT	RTS# Port Data Select	Controls the RTS# pin in combination with MCE bit in FCR and RTS2IO bit. See Table 33.11.	R/W
b7	RTS2IO	RTS# Port Output Specify		R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPB2DT Bit (Serial Port Break Data Select)

This bit specifies the output level of the TXD pin when the setting of the SCR.TE bit is 0. The RXD pin input status can be read from this bit regardless of the SPB2IO bit setting. However, the RXD pin function must have been selected with the multi-function pin controller (MPC).

SPB2IO Bit (Serial Port Break Input/Output)

Controls the TXD pin in combination with the TE bit in the SCR register and the SPB2DT bit.

SCKDT Bit (SCK Port Data Select)

The SCK pin status can be read from this bit regardless of the SCKIO bit setting. (When the SCK pin is used for input, the input signal is invalid (has no means) but the pin status can be read.) However, the SCK pin function must have been selected with the multi-function pin controller (MPC).

SCKIO Bit (SCK Port Input/Output)

Specifies input or output status of the SCK pin. This bit controls the SCK pin in combination with the SCKDT bit, the CM bit in the SMR register, and the CKE1 and CKE0 bits in the SCR register.

CTS2DT Bit (CTS# Port Data Select)

The status of the CTS# pin can be read from this bit regardless of the CTS2IO bit setting. However, the CTS# pin function must have been selected with the multi-function pin controller (MPC).

RTS2DT Bit (RTS# Port Data Select)

The status of the RTS# pin can be read from this bit regardless of the RTS2IO bit setting. However, the RTS# pin function must have been selected with the multi-function pin controller (MPC).

Table 33.11 RTS# Pin Status

FCR.MCE Bit Setting	RTS2IO Bit Setting	RTS2DT Bit Setting	RTS# Pin Status
0	0	×	Setting prohibited*1
0	1	0	Low output
0	1	1	High output
1	×	×	Modem control output

×: Don't care

Note 1. There is no problem with the initial setting if the RTS# pin is not used.

Table 33.12 CTS# Pin Status

FCR.MCE Bit Setting	CTS2IO Bit Setting	CTS2DT Bit Setting	CTS# Pin Status
0	0	×	Setting prohibited*1
0	1	0	Low output
0	1	1	High output
1	×	×	Modem control input

×: Don't care

Note 1. There is no problem with the initial setting if the CTS# pin is not used.

Table 33.13 TXD Pin Status

SCR.TE Bit Setting	SPB2IO Bit Setting	SPB2DT Bit Setting	TXD Pin Status
0	0	×	Setting prohibited
0	1	0	Low output
0	1	1	High output
1	×	×	Transmit data output

×: Don't care

33.2.13 Line Status Register (LSR)

The LSR register is a 16-bit register. The PER and FER bits indicate the number of receive errors in the receive FIFO data register. 1 cannot be written to the ORER status flag. The flag should be read as 1 prior to clearing it to 0.

Address(es): SCIFA0.LSR A006 5012h, SCIFA1.LSR A006 5412h, SCIFA2.LSR A006 5812h, SCIFA3.LSR A006 5C12h, SCIFA4.LSR A006 6012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PER[3:0]				—	—	FER[3:0]				—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ORER	Overrun Error Flag	0: Reception is in progress or has normally completed. 1: An overrun error has occurred during reception.	R/(W) *1
b1	—	Reserved	This bit is read as 0.	R
b5 to b2	FER[3:0]	Framing Error Count	Indicates the quantity of data with a framing error among the receive data stored in the receive FIFO data register (FRDR).	R
b7, b6	—	Reserved	These bits are read as 0.	R
b11 to b8	PER[3:0]	Parity Error Count	Indicates the quantity of data with a parity error among the receive data stored in the receive FIFO data register (FRDR).	R
b15 to b12	—	Reserved	These bits are read as 0.	R

Note 1. To clear the flag, 0 can be only written after 1 is read.

ORER Bit (Overrun Error Flag)

Indicates that receive operation abnormally stops due to occurrence of an overrun error. This flag is not affected and retains its previous state if the RE bit in the serial control register (SCR) is cleared to 0. The receive FIFO data register (FRDR) retains the data before an overrun error occurred, and newly received data is lost. When the ORER bit is set to 1, the SCIFA cannot continue subsequent serial reception.

[Setting condition]

- When the next serial reception is completed with the receive FIFO in full state (16-byte data is received)

[Clearing condition]

- When 0 is written to ORER after being read as 1.

Note: When the internal clock is selected while the SCIFA is in clock synchronous mode, the amount of receive data can be controlled, so no overrun occurs.

FER[3:0] Bits (Framing Error Count)

The values of bits 5 to 2 indicate the quantity of data with a framing error after the ER bit in the FSR register is set. Reading 0000 from the FER[3:0] bits means all 16-byte receive data in the FRDR register have a framing error.

PER[3:0] Bits (Parity Error Count)

The values of bits 11 to 8 indicate the quantity of data with a parity error after the ER bit in the FSR register is set. Reading 0000 from the PER[3:0] bits means all 16-byte receive data in the FRDR register have a parity error.

33.2.14 Serial Extended Mode Register (SEMR)

The SEMR register specifies either LSB or MSB first, enables the noise cancellation, operation in normal or double-speed mode of the baud rate generator, and bit rate modulation, and selects the modulation register and the sampling count (either 8 or 16 times).

Address(es): SCIFA0.SEMR A006 5014h, SCIFA1.SEMR A006 5414h, SCIFA2.SEMR A006 5814h, SCIFA3.SEMR A006 5C14h, SCIFA4.SEMR A006 6014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BGDM	—	BRME	MDDRS	DIR	NFEN	—	ABCS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ABCS0	Asynchronous Base Clock Select	0: Operates on a frequency 16 times the transfer rate as the base clock. 1: Operates on a frequency 8 times the transfer rate as the base clock.	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	NFEN	Noise Cancellation Enable	0: Noise cancellation for the RxD pin is disabled. 1: Noise cancellation for the RxD pin is enabled.	R/W
b3	DIR	Data Transfer Direction Select	0: Transmits the data in the FTDR register by the LSB-first method. The received data is stored in the FRDR register by the LSB-first method. 1: Transmits the data in the FTDR register by the MSB-first method. The received data is stored in the FRDR register by the MSB-first method.	R/W
b4	MDDRS	Modulation Duty Register Select	0: BRR register is accessible. 1: MDDR register is accessible.	R/W
b5	BRME	Bit Rate Modulation Enable	0: Bit rate modulation is disabled. 1: Bit rate modulation is enabled.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	BGDM	Baud Rate Generator Double-Speed Mode Select	0: Baud rate generator normal mode: Baud rate generator operates on the clock signal produced by dividing the clock source by two. 1: Baud rate generator double-speed mode: Baud rate generator operates on the clock signal produced by the clock source (no frequency division).	R/W

ABCS0 Bit (Asynchronous Base Clock Select)

Selects the base clock for 1-bit period in asynchronous mode.

This bit setting is valid only in asynchronous mode (i.e., when the CM bit in the SMR register is 0).

NFEN Bit (Noise Cancellation Enable)

Reduces noise of the input to the RxD pin. This function is only valid in asynchronous mode. For details, see section 33.7, Noise Cancellation.

In clock synchronous mode, this bit should always be set to 0.

DIR Bit (Data Transfer Direction Select)

Selects the serial communication format. This bit is valid only when the transmit/receive data is in 8-bit formats.*1

Note 1. Asynchronous mode or clock synchronous mode with the 8-bit data length

MDDRS Bit (Modulation Duty Register Select)

Selects the register to be enabled access to it.

BRME Bit (Bit Rate Modulation Enable)

Specifies whether to enable or disable the bit rate modulation.

BGDM Bit (Baud Rate Generator Double-Speed Mode Select)

Selects operating mode of the baud rate generator. When setting 1 in this bit, the baud rate generator included in the SCIFA operates in double-speed mode. The setting of this bit is only effective in asynchronous mode (SMR.CM bit = 0) when the internal clock is selected as the clock source (SCR.CKE[1:0] = 00b). Use normal mode under any other settings.

33.2.15 FIFO Trigger Control Register (FTCR)

The FTCR register is a 16-bit register that specifies FIFO trigger conditions. The CPU can always read from and write to the FTCR register.

Address(es): SCIFA0.FTCR A006 5016h, SCIFA1.FTCR A006 5416h, SCIFA2.FTCR A006 5816h, SCIFA3.FTCR A006 5C16h, SCIFA4.FTCR A006 6016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RTRGS	—	—	RFTC[4:0]					TTRGS	—	—	TFTC[4:0]				
Value after reset:	0	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	TFTC[4:0]	Transmit FIFO Data Trigger Number	00h: Transmit data trigger number is 0. 0Fh: Transmit data trigger number is 15. Do not set 10h to 1Fh in these bits.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TTRGS	Transmit Trigger Select	0: TTRG[1:0] bits in FCR are valid. 1: TFTC[4:0] bits in FTCR are valid.	R/W
b12 to b8	RFTC[4:0]	Receive FIFO Data Trigger Number	01h: Receive data trigger number is 1. 10h: Receive data trigger number is 16. Do not set 00h and 11h to 1Fh in these bits.	R/W
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	RTRGS	Receive Trigger Select	0: RTRG[1:0] bits in FCR are valid. 1: RFTC[4:0] bits in FTCR are valid.	R/W

TFTC[4:0] Bits (Transmit FIFO Data Trigger Number)

Specify the reference quantity of data for transmission (i.e., the threshold number of entries to trigger the writing of further data for transmission) for setting of the TDFE flag in the serial status register (FSR).

When the number of entries for transmission in the transmission FIFO, i.e. the number of entries written to the transmit FIFO data register (FTDR) that are yet to be transmitted, falls to or below the specified trigger number for transmission, the TDFE flag is set to 1 and a transmit FIFO data empty interrupt (TXIF) request is generated.

RFTC[4:0] Bits (Receive FIFO Data Trigger Number)

Specify the reference quantity of receive data (i.e., the threshold number of entries to trigger the reading of received data) for setting of the RDF flag in the serial status register (FSR).

When the number of entries in the reception FIFO, i.e. the number of entries yet to be read from the receive FIFO data register (FRDR), rises to or above the specified trigger number for reception, the RDF flag is set to 1 and a receive FIFO data full interrupt (RXIF) request is generated.

33.3 Operation

33.3.1 Overview

For serial communication, the SCIFA can select either asynchronous mode in which characters are synchronized individually or a clock synchronous mode in which communication is synchronized with clock pulses.
The SCIFA has a 16-stage FIFO buffer for both transmission and receptions, reducing the overhead of the CPU and enabling continuous high-speed communication. The RTS# and CTS# signals are provided as modem control signals.
Selection of a transmission/reception format is enabled with the serial mode register (SMR). Table 33.14 shows the transmission format which can be selected in the serial mode register (SMR). As shown in Table 33.15, the SCIFA clock source can be set by using the CKE[1:0] bits of the serial control register (SCR).

(1) Asynchronous Mode

- Data length is selectable either 7 or 8 bits
- Parity addition and 1- or 2-bit stop bit addition are selectable.
  (The combination of the preceding selections determines the transmission/reception format and character length).
- In reception, it is possible to detect framing errors, parity errors, receive FIFO data full, overrun errors, receive data ready, and breaks.
- The stored data quantities are indicated in the FIFO data count register (FDR), respectively for transmit and receive FIFO data.
- An internal or external clock can be selected as the SCIFA clock source.
  When an internal clock is selected, the SCIFA operates using the clock of on-chip baud rate generator and can output the clock with a frequency 16 (or 8) times the bit rate.
  When an external clock is selected, the external clock input must have a frequency 16 (or 8) times the bit rate. (The on-chip baud rate generator is not used.)

(2) Clock Synchronous Mode

- The transmission/reception format is fixed to the 8-bit data length.
- In reception, it is possible to detect overrun errors (ORER).
- An internal or external clock can be selected as the SCIFA clock source.
  When an internal clock is selected, the SCIFA operates using the clock of the on-chip baud rate generator, and outputs this clock to external devices as the synchronous clock.
  When an external clock is selected, the SCIFA operates on the input synchronous clock not using the on-chip baud rate generator.

Table 33.14 SMR Register Settings and SCIFA Communication Formats

SMR Register					SCIFA Transmission/Reception Format		
b7	b6	b5	b3				
CM	CHR	PE	STOP	Mode	Data Length	Parity Bit	Stop Bit Length
0	0	0	0	Asynchronous mode	8 bits	Not set	1 bit
			1				2 bits
		1	0			Set	1 bit
			1				2 bits
	1	0	0		7 bits	Not set	1 bit
			1				2 bits
		1	0			Set	1 bit
			1				2 bits
1	×	×	×	Clock synchronous mode	8 bits	Not set	None

×: Don't care

Table 33.15 SMR, SCR, and SPTR Register Settings and SCIFA Clock Source Selection

SMR Register	SCR Register		SPTR Register				
b7	b1	b0	b3	b2			
CM	CKE[1:0]		SCKIO	SCKDT	Mode	Clock Source	SCK Pin Function
0	0	0	0	×	Asynchronous mode	Internal	Input pin (input signal invalid) (Initial state)
			1	0			SCK pin state: Low
			1	1			SCK pin state: High
		1	×	×			Outputs a clock with frequency 16/8 times the bit rate*1
	1	0	×	×		External	Inputs a clock with frequency 16/8 times the bit rate*2
		1	×	×		Setting prohibited	
1	0	×	×	×	Clock synchronous mode	Internal	Outputs the synchronous clock
	1	0	×	×		External	Inputs the synchronous clock
		1	×	×		Setting prohibited	

×: Don't care

Note 1. SEMR.ABCS0 = 0: Output a clock that has a frequency 16 times the bit rate.
SEMR.ABCS0 = 1: Output a clock that has a frequency 8 times the bit rate.

Note 2. SEMR.ABCS0 = 0: Input a clock that has a frequency 16 times the bit rate.
SEMR.ABCS0 = 1: Input a clock that has a frequency 8 times the bit rate.

33.3.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCIFA are independent, so full duplex communication is possible. The transmitter and receiver are 16-stage FIFO buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmission and reception.

Figure 33.2 shows the general format of asynchronous serial communication.

In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCIFA monitors the line and starts serial communication when the line goes to the space (low) state, considered as a start bit. One serial character consists of a start bit (low), data (LSB first when LSB-first transfer is selected), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCIFA synchronizes at the falling edge of the start bit. The SCIFA samples each data bit on the eighth pulse of a clock with a frequency 16 or 8 times the bit rate*1. Receive data is latched at the center of each bit.

Note 1. When the SEMR.ABCS0 bit = 0, data is sampled on the eighth pulse of a clock with a frequency 16 times the bit rate.
When the SEMR.ABCS0 bit = 1, data is sampled on the fourth pulse of a clock with a frequency 8 times the bit rate.

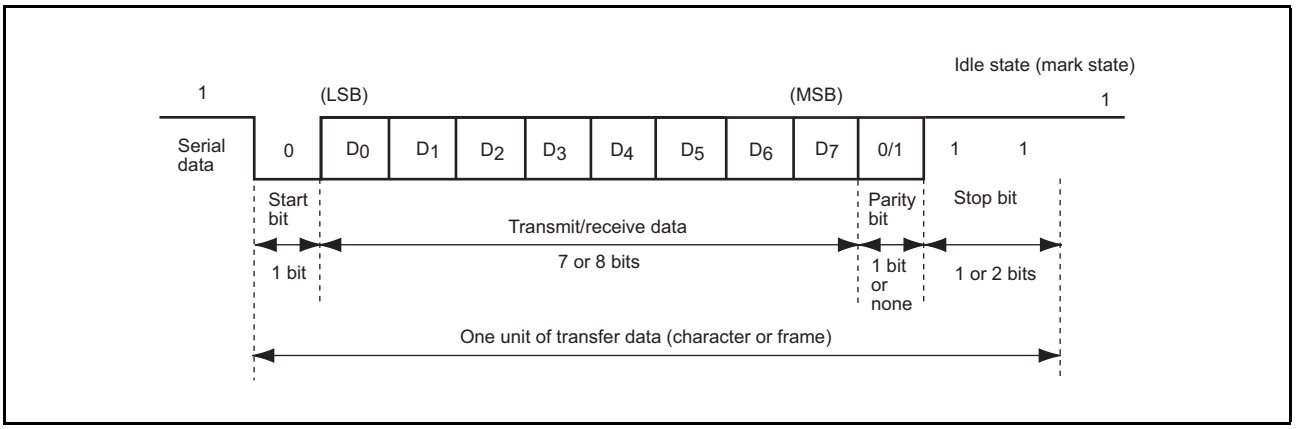


Figure 33.2 Data Format in Asynchronous Communication (8-Bit Data with Parity and Two Stop Bits when LSB-First Transfer is Selected)

(1) Transmit/Receive Formats

Table 33.16 lists the eight communications formats that can be selected in asynchronous mode. The format is selected by setting in the serial mode register (SMR).

Table 33.16 Serial Communications Formats (in Asynchronous Mode)

SMR Setting			Serial Transmit/Receive Format and Frame Length											
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	START	8-bit data								STOP		
		1	START	8-bit data								STOP	STOP	
	1	0	START	8-bit data								P	STOP	
		1	START	8-bit data								P	STOP	STOP
1	0	0	START	7-bit data							STOP			
		1	START	7-bit data							STOP	STOP		
	1	0	START	7-bit data							P	STOP		
		1	START	7-bit data							P	STOP	STOP	

START: Start bit
STOP: Stop bit
P: Parity bit

(2) Clock

An SCIFA transmit/receive clock can be selected from two types of clock sources: the internal clock generated by the on-chip baud rate generator or the external clock input from the SCK pin. The clock source is selected by the settings of the CM bit in the serial mode register (SMR), the CKE[1:0] bits in the serial control register (SCR), and the ACS0 bit in the serial extended mode register (SEMR). For clock source selection, refer to Table 33.15.

When an external clock is input at the SCK pin, it must have a frequency equal to 16/8 times the desired bit rate.

When the SCIFA operates on an internal clock, it can output a clock signal on the SCK pin. The frequency of this output clock is 16/8 times the desired bit rate.

(3) Transmitting and Receiving Data

- SCIFA Initialization (in Asynchronous Mode)

Before transmitting or receiving data, clear the TE and RE bits to 0 in the serial control register (SCR), and then initialize the SCIFA as follows.

When changing operating mode or communication format, always clear the TE and RE bits in the SCR register to 0 before following the procedure given below. Clearing TE to 0 initializes the transmit shift register (TSR). Clearing TE and RE to 0, however, does not initialize the serial status register (FSR), transmit FIFO data register (FTDR), or receive FIFO data register (FRDR), which retain their previous contents. Clear TE to 0 after all transmit data has been transmitted and the TEND flag in the FSR register is set. The TE bit can be cleared to 0 during transmission, but the transmit data (the TXD pin output level) after the TE bit is cleared to 0 depends on the settings of the SPB2IO and SPB2DT bits in the SPTR register. Set the TFRST bit in the FCR register to 1 and reset the FTDR register before TE is set to 1 again to start transmission.

When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCIFA operation becomes unreliable if the clock is stopped. Figure 33.3 shows a sample flowchart for initializing the SCIFA in asynchronous mode.

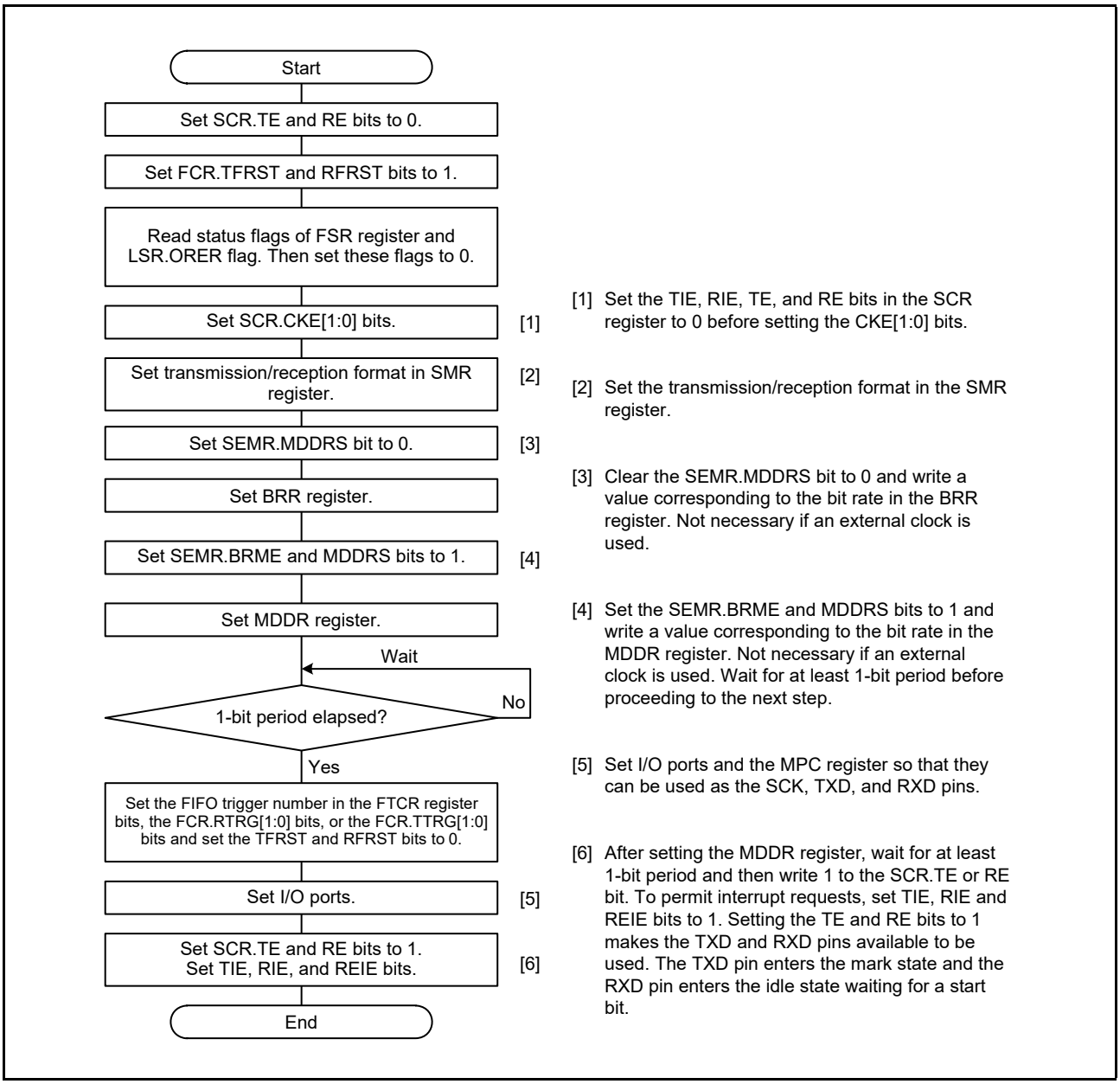
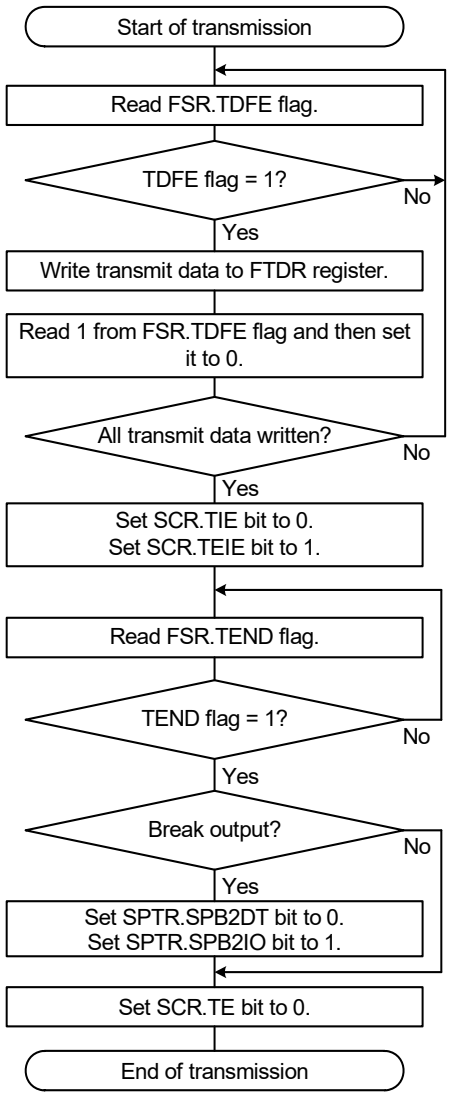


Figure 33.3 Sample Flowchart for SCIFA Initialization in Asynchronous Mode

- Transmitting Serial Data (in Asynchronous Mode)

Figure 33.4 shows a sample flowchart for serial transmission in asynchronous mode.
Follow the procedure given below for serial data transmission after enabling the SCIFA for transmission.



[1] Check the SCIFA status and write the transmit data:
Read the FSR register, confirm that the TDFE flag is set to 1, and then write the transmit data to the FTDR register. The transmit data quantity that can be written is "16 - FDR.T[4:0]".
A change of the TDFE flag from 0 to 1 can be known by a TXIF interrupt request.

[2] Serial transmission continuation procedure (when the FTDR register is written by the CPU):
To continue serial transmission, confirm that the TDFE flag in the FSR register is set to 1, and then write 0 to the flag.

[3] Serial transmission end procedure (when TXIF or TEIF interrupt is used):
After the last transmission data is written to the FTDR register, set the TIE bit to 0 and the TEIE bit to 1 in the SCR register. If the DMAC is activated to write the transmit data to the FTDR register, enable the transmit end interrupt. This will generate a CPU interrupt request when the last transmit data is written in the FTDR register. The TIE and TEIE bit settings will be changed by the CPU interrupt process.
This procedure is unnecessary if the TXIF or TEIF interrupt is not used.

[4] Serial transmission end confirmation:
Read the FSR register and confirm that the TEND flag has changed to 1.
A change of the TEND flag from 0 to 1 can be known by a TEIF interrupt request.

[5] Break output during serial transmission:
To cause a break to be output during serial transmission, set the SPB2DT bit to 0 and the SPB2IO bit to 1 in the SPTR register. Then set the SCR.TE bit to 0.*1

In Step [1], the number of data bytes that can be written can be checked by the FDR.T[4:0] flag (non-transmitted data quantity in the FTDR register).

Note 1. The SPB2DT bit of the SPTR register indicates the input status of the RXD pin. Writings to the SPB2DT and SPB2IO bits of this register in 1-bit unit are handled as read-modify-write, which may lead to undesired values to be written to the SPB2DT bit. To avoid this, when modifying the SPB2DT or SPB2IO bit, for example, write the other bit (the bit used in combination) at the same time.

Figure 33.4 Sample Flowchart for Transmitting Serial Data in Asynchronous Mode

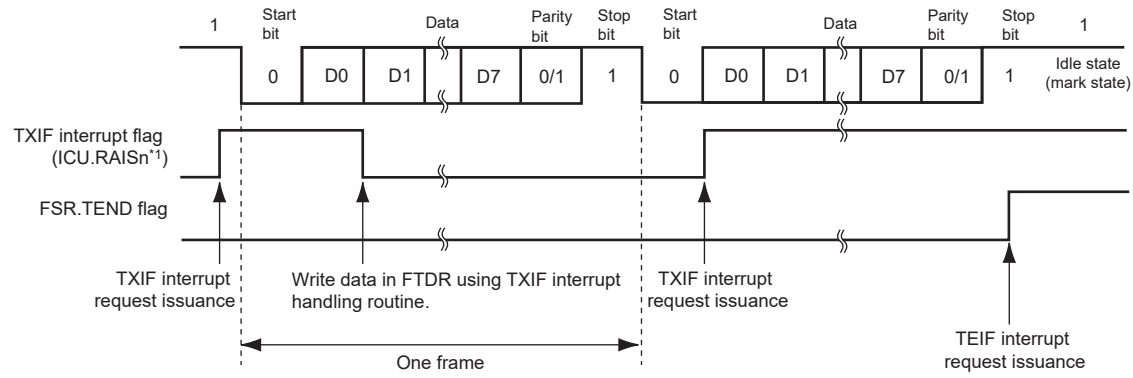
In asynchronous mode, the SCIFA performs serial transmission as described below.

1. When data is written into the transmit FIFO data register (FTDR) by the TXIF interrupt processing routine, the SCIFA transfers the data from the FTDR register to the transmit shift register (TSR) and starts transmission. Confirm that the TDFE flag in the serial status register (FSR) is set to 1 before writing transmit data to the FTDR register. The number of data bytes that can be written is “16 minus the number of non-transmitted data units”.
2. When data is transferred from the FTDR register to the TSR register and transmission is started, consecutive transmit operations are performed until there is no transmit data left in the FTDR register. When the number of transmit data bytes in the FTDR register becomes equal to or less than the transmission trigger number specified in the FIFO control register (FCR) or FIFO trigger control register (FTCR), the TDFE flag is set. If the TIE bit in the serial control register (SCR) is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXIF) request is generated.

   The serial transmit data is output from the TXD pin in the following order.

   (a) Start bit: One-bit 0 is output.
   (b) Transmit data: 8- or 7-bit data is output in LSB-first order (when LSB-first transfer is selected).
   (c) Parity bit: One parity bit (even or odd parity) is output. (A format in which a parity bit is not output can also be selected.)
   (d) Stop bit(s): One or two 1 bits (stop bits) are output.
   (e) Mark state: 1 is output continuously until the start bit that starts the next transmission is output.
3. The SCIFA checks the transmit data of the FTDR register at the timing for sending the stop bit. If data is present, the data is transferred from the FTDR register to the TSR register, the stop bit is output, and then serial transmission of the next frame is started. If there is no data to be transmitted, the TEND flag in the FSR register is set to 1, the stop bit is output, and then the SCIFA enters the mark state (high level) in which 1 is output continuously.

Figure 33.5 shows an example of the operation for transmission in asynchronous mode.



Note 1. For the corresponding interrupt number, see section 12, Interrupt Controller (ICUA).

Figure 33.5 Example of Transmit Operation in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit when LSB-First Transfer is Selected)

4. When modem control is enabled, transmission can be stopped/resumed by the input level to the CTS# pin. When a high level is input to the CTS# pin during transmission, the SCIFA enters the mark state (high level) after completion of one-frame data transmission. When a low level is input to the CTS# pin, output of the next data to be transmitted begins with a start bit. Figure 33.6 shows an example of the operation for transmission when using the modem control function.

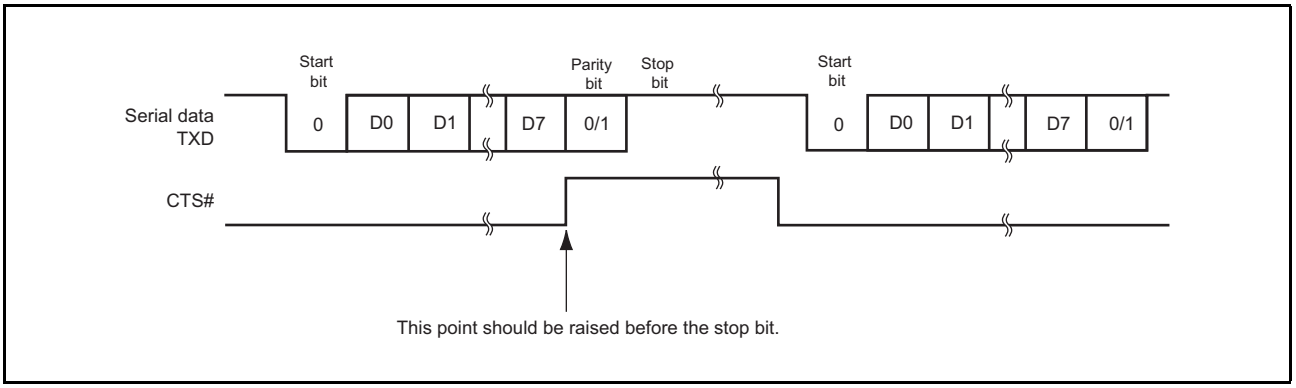
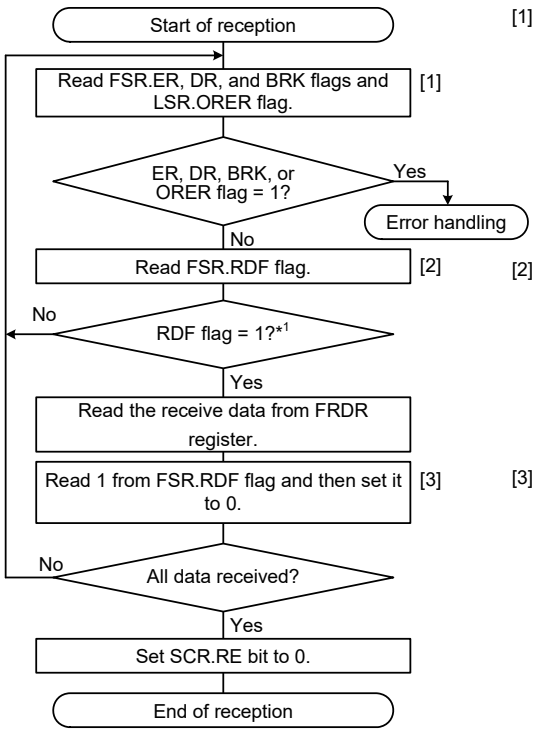


Figure 33.6 Example of Transmit Operation in Asynchronous Mode Using Modem Control Function (CTS#)

- Receiving Serial Data (in Asynchronous Mode)

Figure 33.7 and Figure 33.8 show sample flowcharts for serial reception in asynchronous mode.
Follow the procedure given below for serial data reception after enabling the SCIFA for reception.



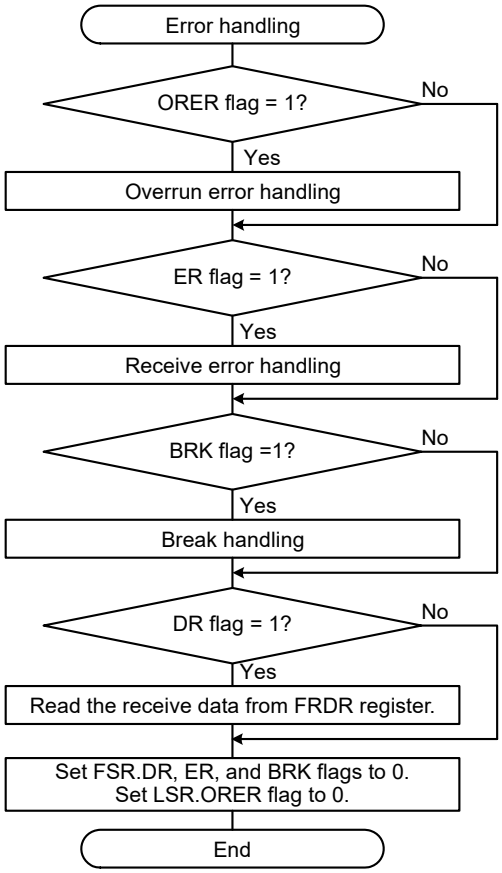
[1] Receive error handling and break detection:
When a receive error occurs, read the ER, DR, and BRK flags in the FSR register and the LSR.ORER flag to identify the error. After handling the error as specified, clear the ER, DR, BRK, and ORER flags to 0.
In the case where a framing error occurs, a break can be detected by reading the value of the RXD pin.
Error occurrence can be known by a BRIF, ERIF, or DRIF interrupt request.

[2] Check the SCIFA status and read the receive data:
Read the FSR register, confirm that the RDF flag is set to 1, and then read the receive data at least as much as the amount specified as the receive data trigger number from those stored in the FRDR register. The receive data quantity that can be read can be checked by the FDR.R[4:0] flag.
A change of the RDF flag from 0 to 1 can be known by an RXIF interrupt request.

[3] Serial reception continuation procedure (when the FRDR register is read by the CPU):
To continue serial reception, confirm that the RDF flag in the FSR register is set to 1, and then write 0 to the flag.

Note 1. The number of all the received data units should be an integral multiple of the receive data trigger number. If not, process returns to Step [1] and enters an infinite loop. In this case, it is necessary to set the timeout processing using a timer.

Figure 33.7 Sample Flowchart for Receiving Serial Data in Asynchronous Mode (1)



- Whether a framing error or parity error has occurred in the received data that is read from the FRDR register can be checked with the FER and PER flags in the FSR register.
- When a break signal is received, the received data is not transferred to the FRDR register while the BRK flag is set to 1. However, note that the last data in the FRDR register is 00h and the break data in which a framing error occurred is stored.

Figure 33.8 Sample Flowchart for Receiving Serial Data in Asynchronous Mode (2)

In asynchronous mode, the SCIFA performs serial reception as described below.

1. The SCIFA monitors the communication line, and if a 0 start bit is detected, it performs internal synchronization to start reception.
2. The received data is stored into the RSR register in LSB-to-MSB order (when LSB-first transfer is selected).
3. The parity bit and stop bit are received.
   After receiving these bits, the SCIFA carries out the following checks.
   (a) Stop bit check: The SCIFA checks whether the stop bit is 1. If there are two stop bits, only the first is checked.
   (b) The SCIFA checks whether receive data can be transferred from the receive shift register (RSR) to the receive FIFO data register (FRDR).
   (c) Parity bit check: The SCIFA checks whether the parity bit is an expected value.
   (d) Overrun error check: The SCIFA checks whether the ORER flag is 0, indicating that the overrun error has not occurred.
   (e) Break check: The SCIFA checks whether the BRK flag is 0, indicating that the break state is not set.

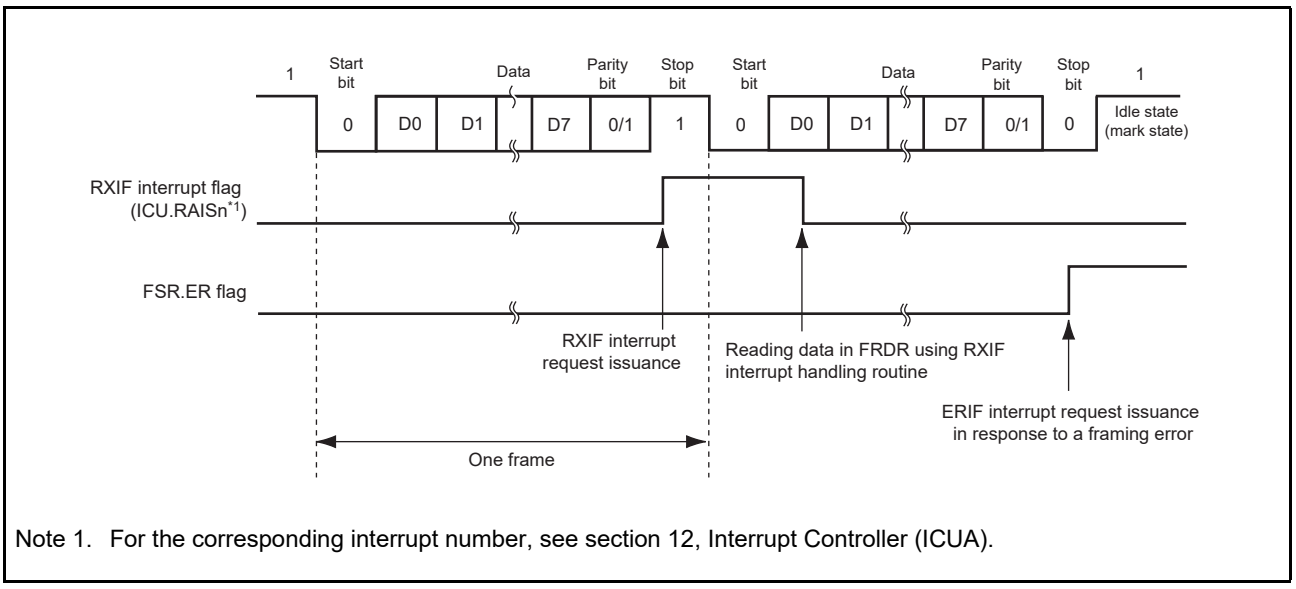
If all the above checks are passed, the receive data is stored in the FRDR register.

Note: When a parity error or a framing error occurs, reception is not suspended.

4. When receive data units equaling or exceeding the specified reception trigger number are stored in the receive FIFO data register (FRDR) and the RDF flag is changed to 1, a receive FIFO data full interrupt (RXIF) request is generated while the RIE bit in the SCR register is set to 1. When the quantity of data in the FRDR register falls below the specified reception trigger number and the RIE bit in the SCR register is set to 1, a receive data ready interrupt (DRIF) request is generated if no next data is received after the elapse of 15 ETUs*1 from the last stop bit (the DR flag in the FSR register is 1). When the ER flag in the FSR register is changed to 1, a receive error interrupt (ERIF) request is generated while the RIE or REIE bit in the SCR register is set to 1. When the BRK or ORER flag is changed to 1 in the FSR register, a break reception interrupt (BRIF) request is generated while the RIE or REIE bit in the SCR register is set to 1.

Note 1. It is equivalent to 1 and half frames of 8-bit format with one stop bit (ETU: Element Time Unit).

Figure 33.9 shows an example of the operation for reception in asynchronous mode.



Note 1. For the corresponding interrupt number, see section 12, Interrupt Controller (ICUA).

Figure 33.9 Example of SCIFA Receive Operation in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit when LSB-First Transfer is Selected)

5. When modem control is enabled, the RTS# signal that indicates the FRDR register has space is output. When the RTS# pin is at low level, reception is possible. The RTS# pin being at the high level indicates that the number of entries in the FRDR register is equal to or greater than the threshold for output of the active level of the RTS# signal and that the transmission of further data needs to be suspended until the FRDR register has enough space. Figure 33.10 shows an example of the operation for reception in asynchronous mode when using the modem control function.

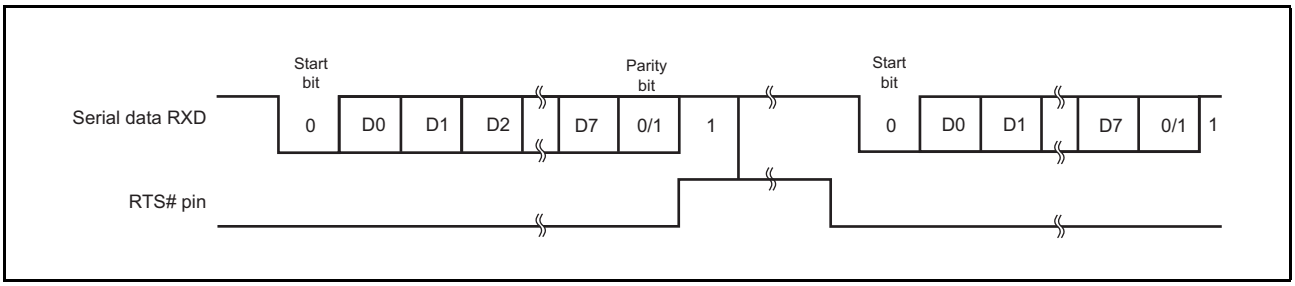
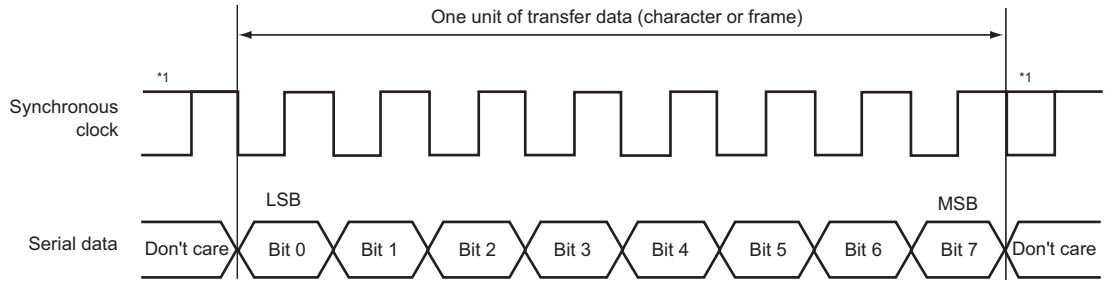


Figure 33.10 Example of SCIFA Receive Operation in Asynchronous Mode Using Modem Control Function (RTS#)

33.3.3 Operation in Clock Synchronous Mode

In clock synchronous mode, the SCIFA transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication.
Full-duplex communication is possible because the SCIFA transmitter and receiver are independent and share the same clock. Since the transmitter and the receiver have 16-stage FIFO buffers, respectively, continuous transmission or reception is possible by reading or writing data while transmission or reception is in progress.
Figure 33.11 shows the general format in clock synchronous serial communication.



Note 1. High level except in continuous transmission/reception

Figure 33.11 Data Format in Clock Synchronous Communication (when LSB-First Transfer is Selected)

In clock synchronous serial communication, each data bit is output on the communication line from one falling edge of the synchronous clock to the next. Data is guaranteed valid at the rising edge of the synchronous clock.
In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB (when LSB-first transfer is selected).
In clock synchronous mode, the SCIFA receives data by synchronizing with the rising edge of the synchronous clock.

(1) Transmit/Receive Formats

The data length is fixed at eight bits.
No parity bit can be added.

(2) Clock

An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCIFA transmit/receive clock according to the settings of the CM bit in the serial mode register (SMR), the CKE[1:0] bits in the serial control register (SCR), and the ACS0 bit in the serial extended mode register (SEMR).
When the SCIFA operates on an internal clock, it outputs the synchronous clock signal at the SCK pin. Eight synchronous clock pulses are output per transmitted or received character. Unless the SCIFA is transmitting or receiving, the synchronous clock signal remains in the high state. When the SCIFA only receives data on an internal clock, the internal clock signal outputs while the RE bit in the SCR register is 1 until the number of data units in the receive FIFO reaches the specified reception trigger number.

(3) Transmitting and Receiving Data

- SCIFA Initialization (in Clock Synchronous Mode)

Before transmitting or receiving, clear the TE and RE bits to 0 in the serial control register (SCR), and then initialize the SCIFA by performing the following procedure.
Similarly, before changing the mode or communication format, clear the TE and RE bits to 0, and then change it by performing the following procedure. Clearing TE to 0 initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDF, PER, FER, and ORER flags and the receive FIFO data register (FRDR), which retain their previous contents.

Figure 33.12 shows a sample flowchart for initializing the SCIFA in clock synchronous mode.

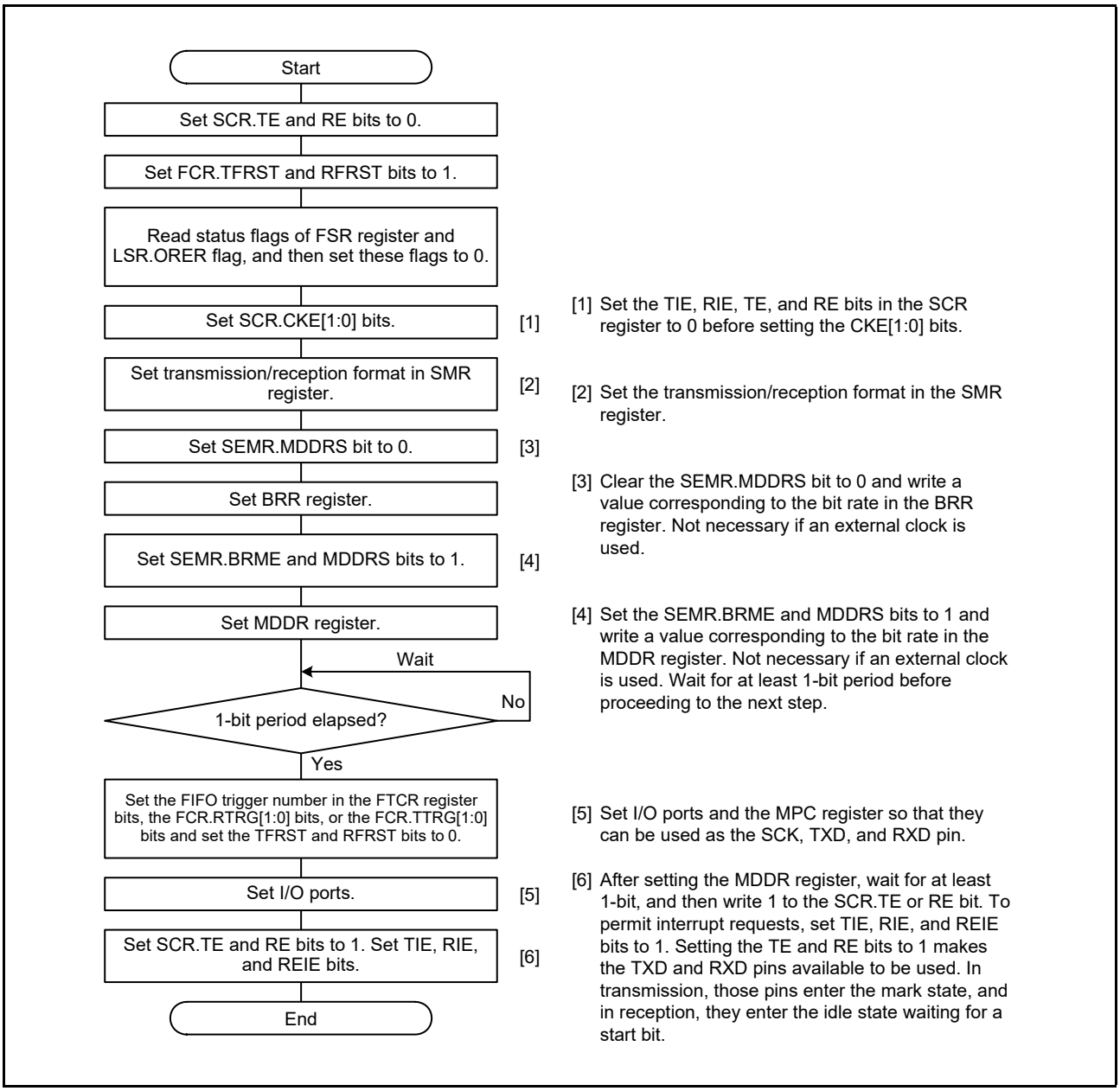


Figure 33.12 Sample Flowchart for SCIFA Initialization in Clock Synchronous Mode

- Transmitting Serial Data (in Clock Synchronous Mode)

Figure 33.13 shows a sample flowchart for transmitting serial data in clock synchronous mode.
Follow the procedure given below for serial data transmission after enabling the SCIFA for transmission.

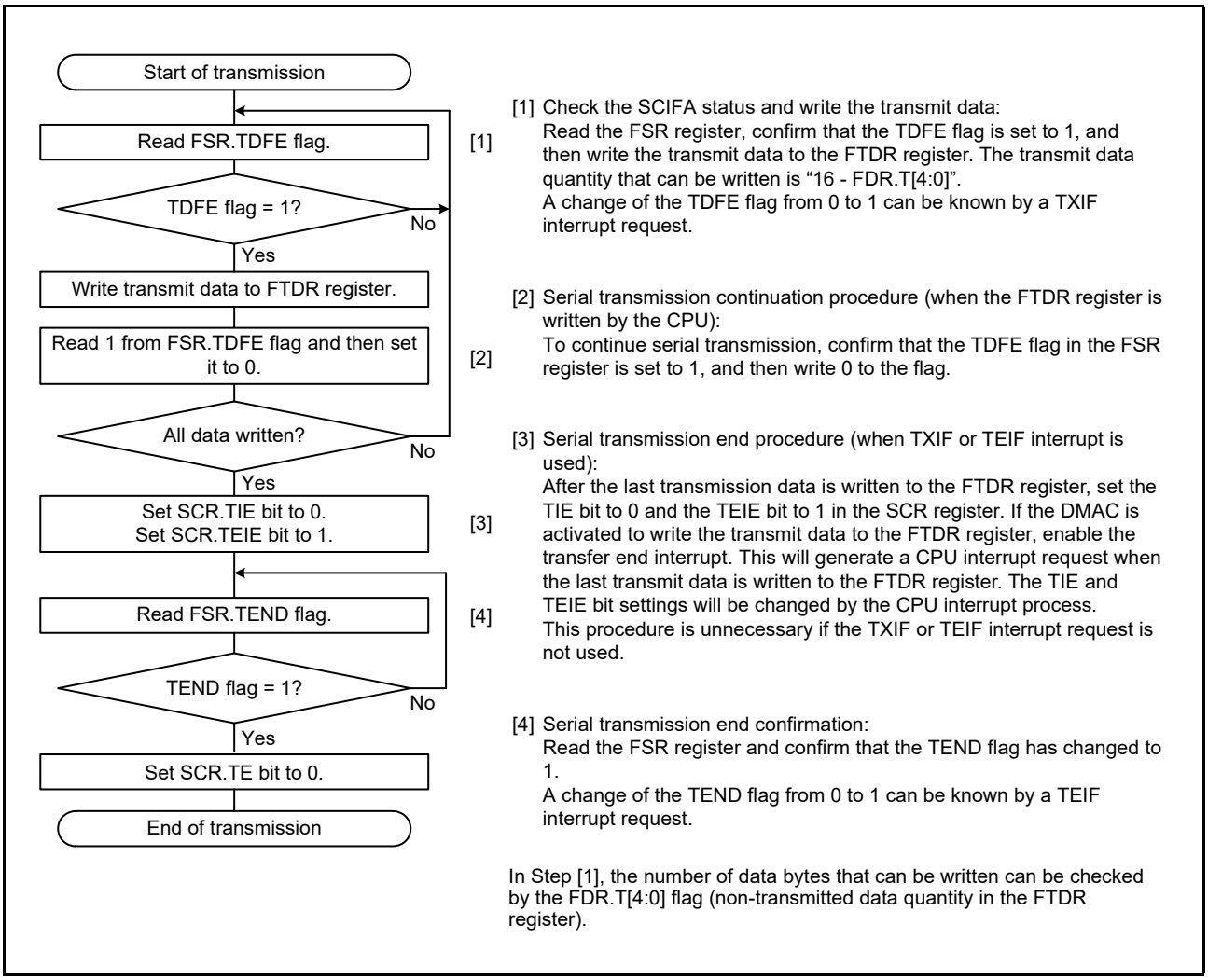
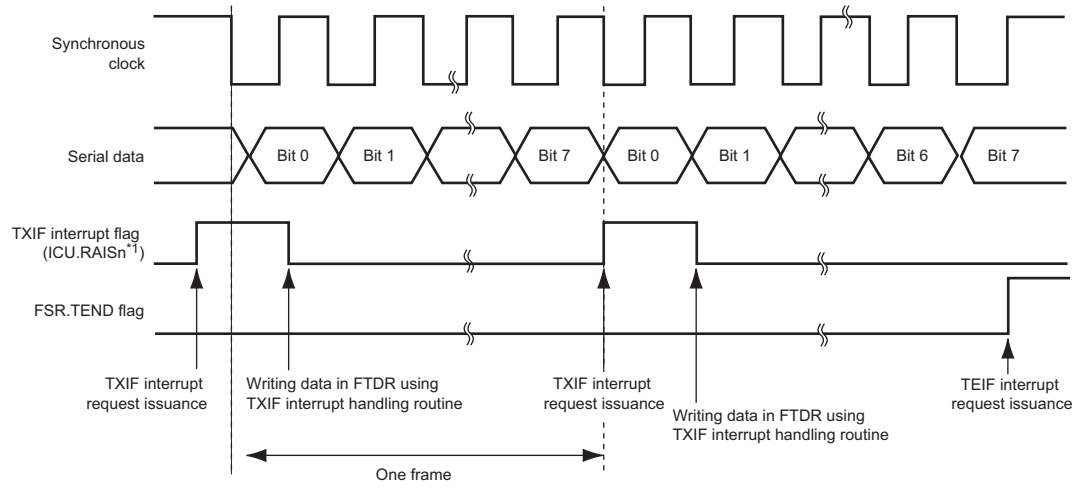


Figure 33.13 Sample Flowchart for Transmitting Serial Data in Clock Synchronous Mode

In clock synchronous mode, the SCIFA performs serial transmission as described below.

1. When data is written into the transmit FIFO data register (FTDR) by the TXIF interrupt processing routine, the SCIFA transfers the data from the FTDR register to the transmit shift register (TSR) and starts transmission. Confirm that the TDFE flag in the serial status register (FSR) is set to 1 before writing transmit data to the FTDR register. The number of data bytes that can be written is “16 minus the specified number of non-transmitted data units”.
2. When data is transferred from the FTDR register to the TSR register and transmission is started, consecutive transmit operations are performed until there is no transmit data left in the FTDR register. When the number of transmit data bytes in the FTDR register becomes equal to or less than the transmission trigger number set in the FIFO control register (FCR) or FIFO trigger control register (FTCR), the TDFE flag in the FSR register is set. If the TIE bit in the serial control register (SCR) is set to 1 at this time, a transmit-FIFO-data-empty interrupt (TXIF) request is generated.
   If clock output mode is selected, the SCIFA outputs eight synchronous clock pulses. If an external clock source is selected, the SCIFA outputs data in synchronization with the input clock. Data is output from the TXD pin in order from the LSB (b0) to the MSB (b7) (when LSB-first transfer is selected).
3. The SCIFA checks the transmit data of the FTDR register at the timing for sending the MSB (bit 7). If data is present, the data is transferred from the FTDR register to the TSR register, and then serial transmission of the next frame is started. If there is no data, the TXD pin holds the output level of the last data after the TEND flag in the FSR register is set to 1 and the MSB (bit 7) is output.
4. After the end of serial transmission, the SCK pin is held in the high state.

Figure 33.14 shows an example of SCIFA transmit operation in clock synchronous mode.

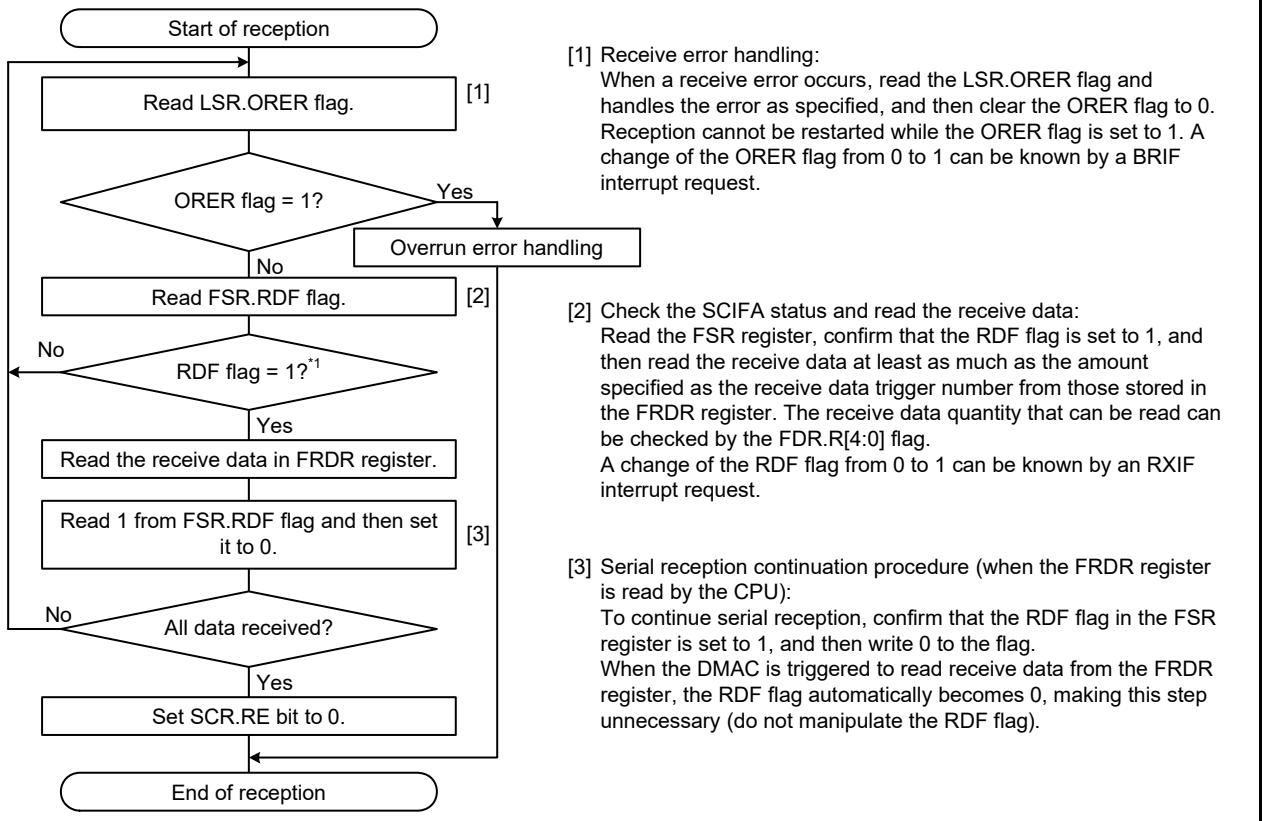


Note 1. For the corresponding interrupt number, see section 12, Interrupt Controller (ICUA).

Figure 33.14 Example of SCIFA Transmit Operation in Clock Synchronous Mode (when LSB-First Transfer is Selected)

- Receiving Serial Data (in Clock Synchronous Mode)

Figure 33.15 shows sample flowcharts for receiving serial data in clock synchronous mode.
Follow the procedure given below for serial data reception after enabling the SCIFA for reception. When switching from asynchronous mode to clock synchronous mode without SCIFA initialization, make sure that the ORER, PER, and FER flags in the line status register (LSR) are cleared to 0.



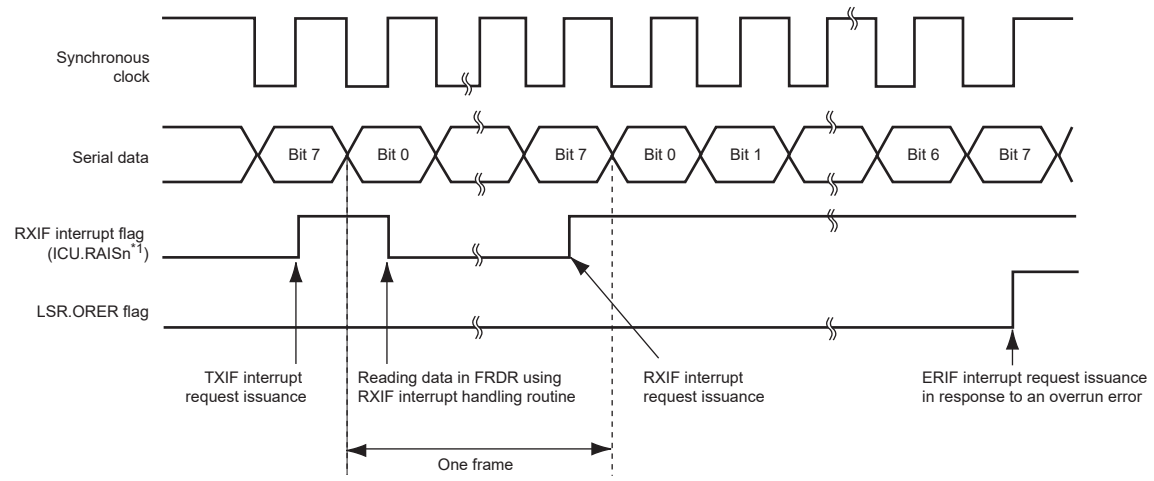
Note 1. The number of all the received data units should be an integral multiple of the receive data trigger number. If not, process returns to Step [1] and enters an infinite loop. In this case, it is necessary to set the timeout processing using a timer.

Figure 33.15 Sample Flowchart for Receiving Serial Data in Clock Synchronous Mode

In clock synchronous mode, the SCIFA performs serial reception as described below.

1. The SCIFA synchronizes with the synchronous clock input or output and starts reception.
2. Receive data is stored into the receive shift register (RSR) in order from the LSB to the MSB (when LSB-first transfer is selected). After receiving the data, the SCIFA checks whether the receive data can be transferred from the RSR register to the FRDR register. If data can be transferred, the SCIFA stores the received data in the FRDR register. If an overrun error is detected during the error check, further reception is not performed.
3. After the received data units equaling or exceeding the specified reception trigger number are stored in the FRDR register and the RDF flag is set to 1, a receive-data-full interrupt (RXIF) request is generated when the RIE bit in the serial control register (SCR) is set to 1. When the ORER flag in the line status register (LSR) is set to 1 and the RIE or REIE bit in the SCR register is also set to 1, a break interrupt (BRIF) request is generated.

Figure 33.16 shows an example of SCIFA receive operation in clock synchronous mode.



Note 1. For the corresponding interrupt number, see section 12, Interrupt Controller (ICUA).

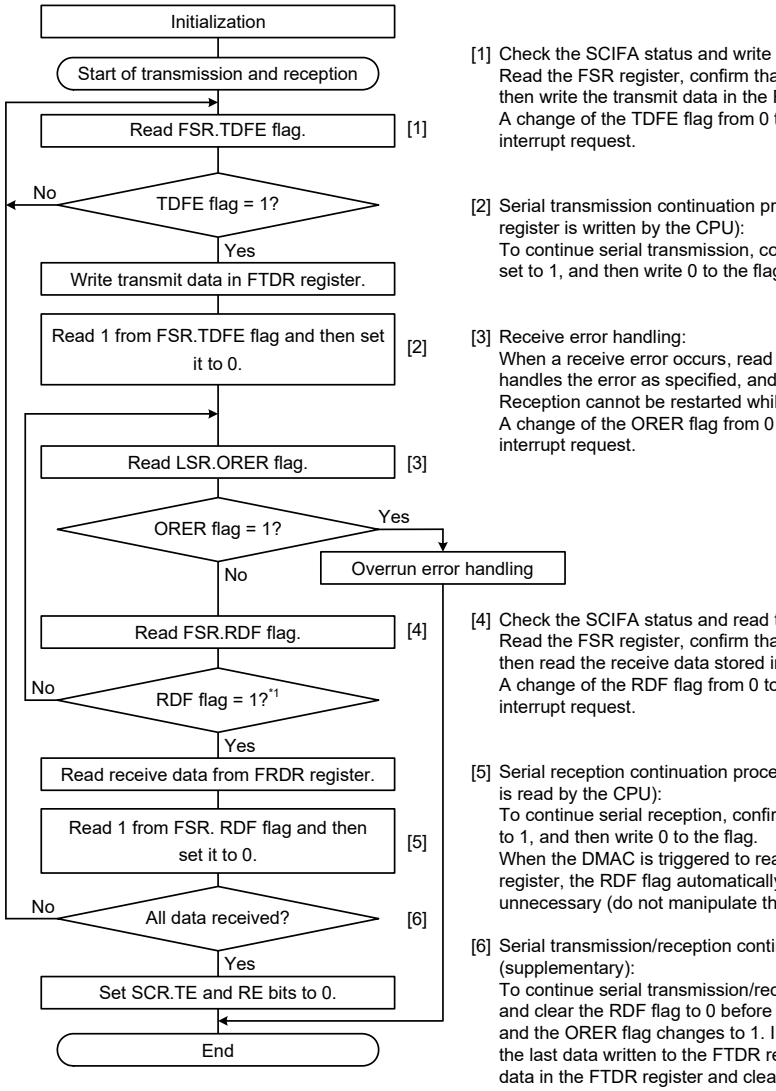
Figure 33.16 Example of SCIFA Receive Operation (when LSB-First Transfer is Selected)

- Transmitting and Receiving Serial Data Simultaneously (in Clock Synchronous Mode)

Figure 33.17 shows a sample flowchart for transmitting and receiving serial data simultaneously in clock synchronous mode.

In simultaneous transmission/reception of serial data, number of receive data = number of transmit data = number of transmit data to be written to the FTDR register.

Follow the procedure given below for the simultaneous transmission/reception of serial data, after enabling the SCIFA for transmission/reception.



[1] Check the SCIFA status and write the transmit data:
Read the FSR register, confirm that the TDFE flag is set to 1, and then write the transmit data in the FTDR register.
A change of the TDFE flag from 0 to 1 can be known by a TXIF interrupt request.

[2] Serial transmission continuation procedure (when the FTDR register is written by the CPU):
To continue serial transmission, confirm that the FSR.TDFE flag is set to 1, and then write 0 to the flag.

[3] Receive error handling:
When a receive error occurs, read the LSR.ORER flag and handles the error as specified, and then clear the ORER flag to 0.
Reception cannot be restarted while the ORER flag is set to 1.
A change of the ORER flag from 0 to 1 can be known by a BRIF interrupt request.

[4] Check the SCIFA status and read the receive data:
Read the FSR register, confirm that the RDF flag is set to 1, and then read the receive data stored in the FRDR register.
A change of the RDF flag from 0 to 1 can be known by an RXIF interrupt request.

[5] Serial reception continuation procedure (when the FRDR register is read by the CPU):
To continue serial reception, confirm that the FSR.RDF flag is set to 1, and then write 0 to the flag.
When the DMAC is triggered to read receive data from the FRDR register, the RDF flag automatically becomes 0, making this step unnecessary (do not manipulate the RDF flag).

[6] Serial transmission/reception continuation procedure (supplementary):
To continue serial transmission/reception, read the FRDR register and clear the RDF flag to 0 before the FRDR register overflows and the ORER flag changes to 1. In addition, before the last bit of the last data written to the FTDR register is transmitted, write the data in the FTDR register and clear the TDFE flag to 0.
When the DMAC is triggered to write data to the FTDR register or read data from the FRDR register, the TDFE and RDF flags automatically become 0, making this step unnecessary (do not manipulate the TDFE or RDF flag).

Note: When switching the operation from transmission or reception to the simultaneous transmission and reception, clear the TE and RE bits to 0 and then simultaneously set these bits to 1.

Note 1. The number of all the received data units should be an integral multiple of the receive data trigger number. If not, process returns to Step [1] and enters an infinite loop. In this case, it is necessary to set the timeout processing using a timer.

Figure 33.17 Sample Flowchart for Simultaneous Transmitting/Receiving Serial Data in Clock Synchronous Mode

33.4 Bit Modulation

Using the bit rate modulation, the bit rate can be corrected by skipping the specified number of clock pulses input to the baud rate generator. To correct the bit rate, only the number of clock pulses specified in the MDDR register are enabled among 256 internal clock pulses specified by the CKS[1:0] bits in the SMR register in a way that forms average intervals.

Figure 33.18 shows an example where SERICLK is selected by the CKS[1:0] bits in SMR and BRR and MDDR are set to 0 and 160, respectively, in asynchronous mode. In this example, the cycle of the base clock is evenly corrected (256/160) and the bit rate is also corrected (160/256). Note that skipping an internal clock causes bias and expansion or contraction is generated in the pulse width of the base clock.

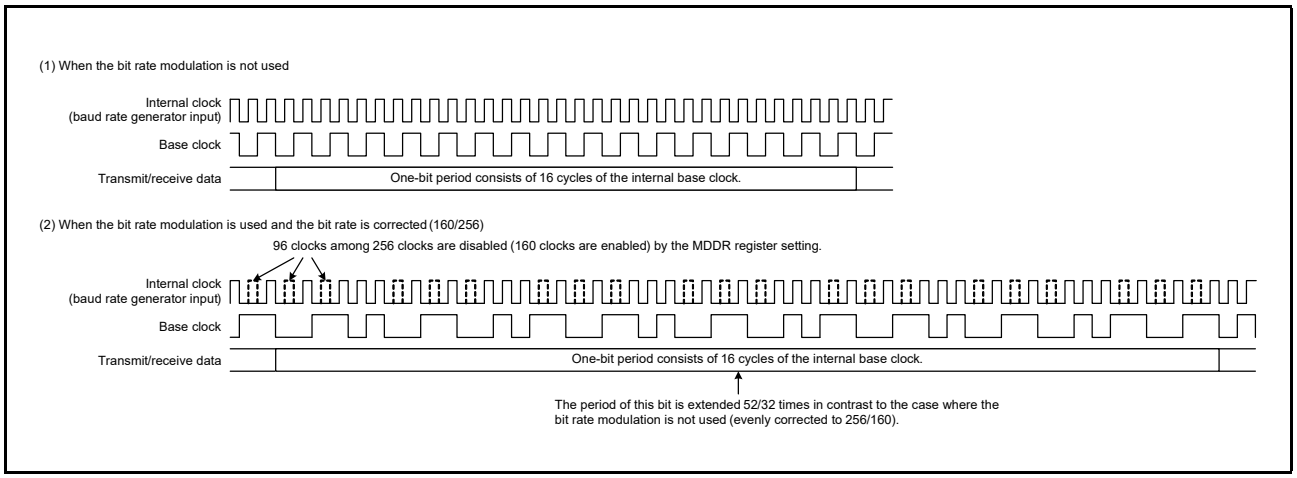


Figure 33.18 Example of Internal Base Clock when Bit Modulation is Used

33.5 Interrupt Sources

The SCIFA has six interrupt sources: transmit-FIFO-data-empty (TXIF), receive-error (ERIF), receive-FIFO-data-full (RXIF), break (BRIF), transmit-end (TEIF), receive-data-ready (DRIF). The TEIF and DRIF interrupts, the ERIF and BRIF interrupts share the same vector numbers, respectively.

Table 33.17 shows the interrupt sources and priority. The interrupt sources can be enabled or disabled using the TIE, RIE, REIE, TEIE bits in the SCR register and are separately input to the interrupt controller.

When the quantity of transmit data written in the FTDR register as a result of transmission is equal to or less than the specified transmission trigger number, the TDFE flag in the serial status register (FSR) is set to 1 and a TXIF interrupt request is generated.

When the data units equaling or exceeding the specified transmission trigger number are stored in the receive FIFO register (FRDR) and the RDF flag in the FSR register is set to 1, a receive data full interrupt (RXIF) request is generated.

When the quantity of received data in the FRDR register is below the specified reception trigger number and no next data has been received yet even after the period of 15 ETUs elapsed*1 from the last stop bit, the DR flag in the FSR register is set to 1 and a receive data ready interrupt (DRIF) request is generated. In clock synchronous mode, a DRIF interrupt request is not generated.

When the BRK flag in the FSR register or the ORER flag in the LSR register is set to 1, a BRIF interrupt request is issued.

When the ER flag in the FSR register is set to 1, an ERIF interrupt request is issued.

When the TEND flag in the FSR register is set to 1, a TEIF interrupt request is issued.

When the RIE bit is cleared to 0 and the REIE bit in the SCR register is set to 1, an ERIF and BRIF interrupt requests are issued but an RXIF and a DRIF interrupt requests are not.

An TXIF interrupt indicates that transmit data can be written and an RXIF interrupt indicates that receive data is stored in the FRDR register.

Note 1. It is equivalent to 1 and half frames of 8-bit format with one stop bit (ETU: Element Time Unit).

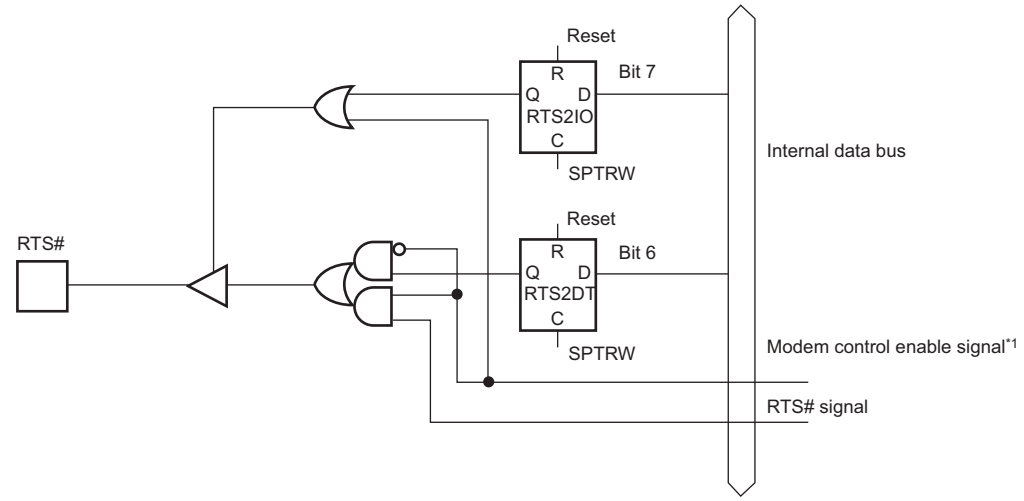
Table 33.17 SCIFA Interrupt Sources

Name	Level/ Edge	Interrupt Source	Interrupt Enable Bit	DMAC Activation	Priority
BRIF	Level	Interrupt caused by break (BRK) or overrun (ORER).	RIE or REIE	Impossible	High
ERIF	Level	Interrupt caused by framing or parity (ER).	RIE or REIE	Impossible	
RXIF	Level	Interrupt caused by receive FIFO data full (RDF).	RIE	Possible	
TXIF	Level	Interrupt caused by transmit FIFO data empty (TDFE).	TIE	Possible	
TEIF	Level	Interrupt caused by transmit end (TEND).	TEIE	Impossible	
DRIF	Level	Interrupt caused by receive data ready (DR).	RIE	Impossible	Low

Note: The TEIF and DRIF interrupts share the same vector number.

33.6 Serial Port Register (SPTR) and SCIFA-Related Pins

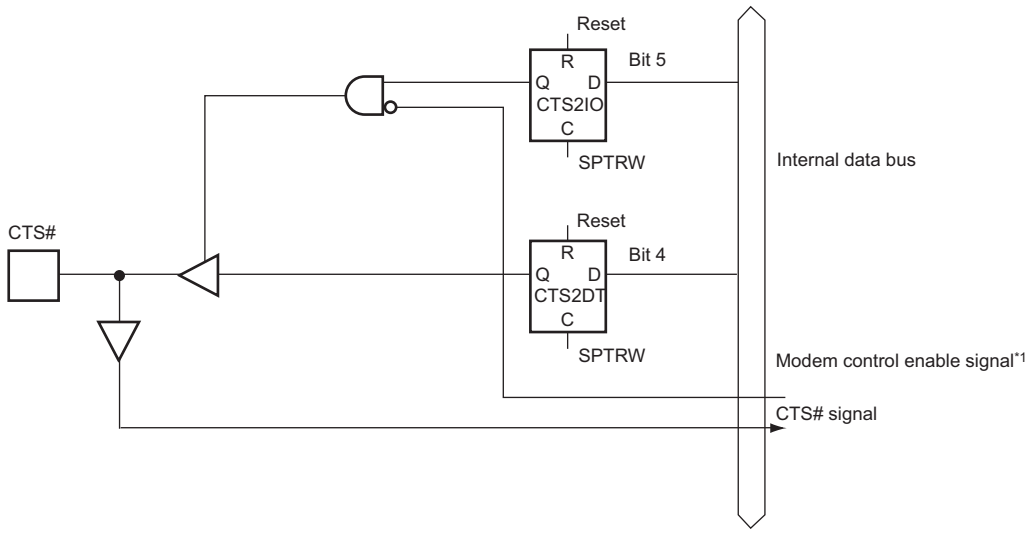
Figure 33.19 to Figure 33.22 show the relationships between the SPTR register and the SCIFA-related pins.



SPTRW: SPTR write

Note 1. These signals allow the RTS# pin to enter the modem control state with the MCE bits in FCR.

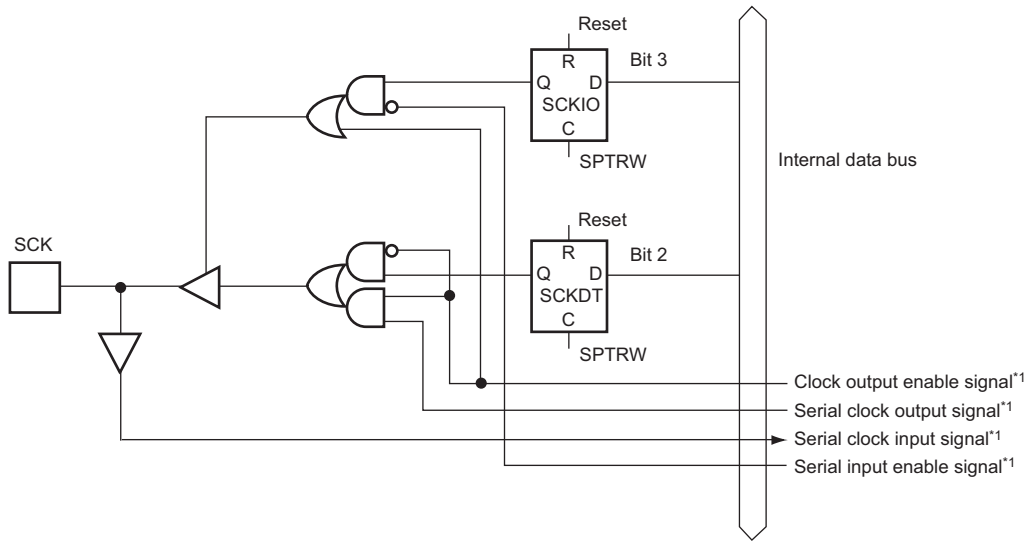
Figure 33.19 RTS2IO Bit and RTS2DT Bit in the SPTR Register, and RTS# Pin



SPTRW: SPTR write

Note 1. These signals allow the CTS# pin to enter the modem control state with the MCE bits in FCR.

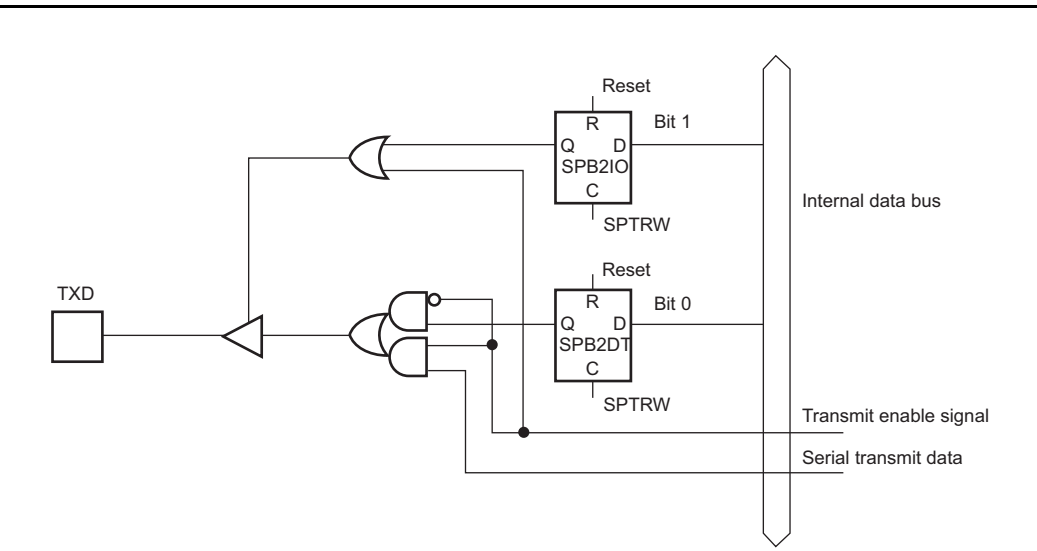
Figure 33.20 CTS2IO Bit and CTS2DT Bit in the SPTR Register, and CTS# Pin



SPTRW: SPTR write

Note 1. These signals control the SCK pin according to the settings of the CM bit in SMR and CKE[1:0] bits in SCR.

Figure 33.21 SCKIO Bit and SCKDT Bit in the SPTR Register, and SCK Pin



SPTRW: SPTR write

Figure 33.22 SPB2IO Bit and SPB2DT Bit in the SPTR Register, and TXD Pin

33.7 Noise Cancellation

Figure 33.23 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a two-stage flip-flop circuits and a match detection circuit. When the input signals of the noise filter and the output signals of the two-stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. (When the levels sampled on three consecutive cycles of the sampling clock of the noise filter match, the signal is considered valid. If three consecutive sampled values do not match, the signal is considered to be noise rather than a received signal).

In asynchronous mode, the noise cancellation can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn pin is taken in the flip-flop circuit of the noise filter on the base clock (the clock with a frequency 16, 8, or 4 times the transfer rate*1).

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.RE is set to 0 during input of the base clock, the noise filter outputs 0 as the internal RxDn signal. The internal match detector continues operating even while operations for reception are stopped, and the result from the last time previous consecutive samples matched is output at the same time as operations for reception are resumed.

Note 1. A frequency 16 times bit rate when the SEMR.ABCS0 bit and the SEMR.BGDM bit are both 0, a frequency 8 times bit rate when either the SEMR.ABCS0 bit or the SEMR.BGDM bit is 1, and a frequency 4 times bit rate when the SEMR.ABCS0 bit and the SEMR.BGDM bit are both 1.

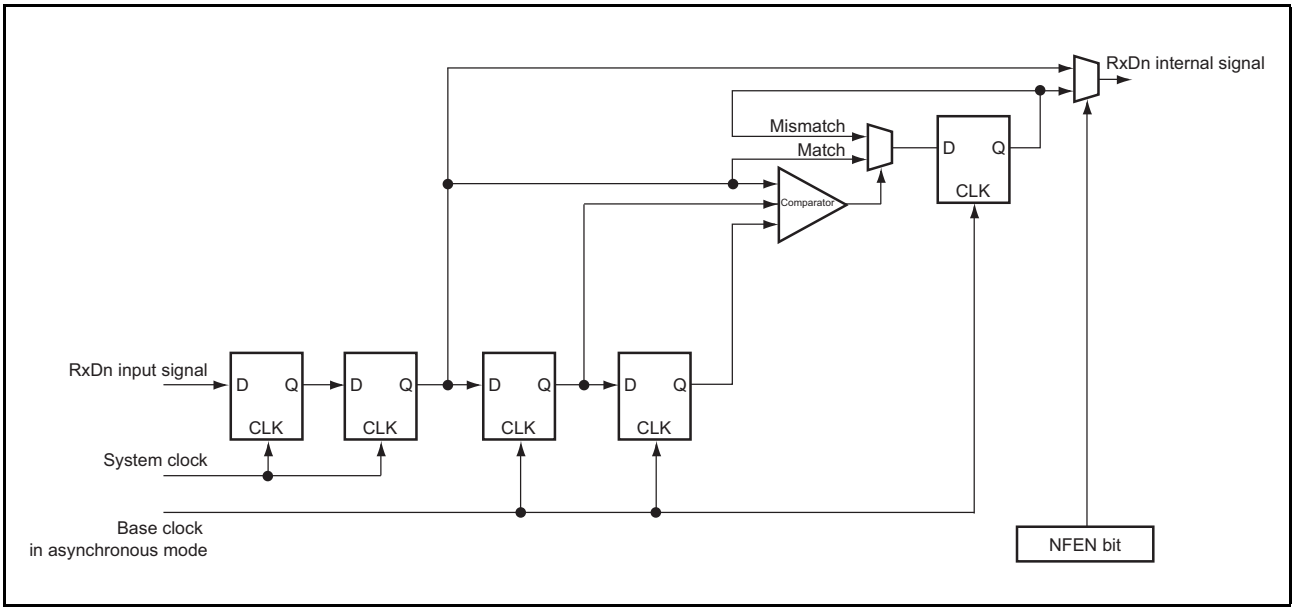


Figure 33.23 Block Diagram of Digital Noise Filter Circuit

33.8 Usage Notes

The following is the notes on using the SCIFA.

33.8.1 FTDR Register Writing and TDFE Flag

The TDFE flag in the serial status register (FSR) is set when the number of transmit data bytes written in the transmit FIFO data register (FTDR) has fallen below the transmission trigger number set by bits TTRG[1:0] in the FIFO control register (FCR) or bits TFTC[4:0] in the FIFO trigger control register (FTCR). After the TDFE flag is set, transmit data up to the number of empty bytes in the FTDR register can be written, allowing efficient continuous transmission.
However, if the number of data bytes written in the FTDR register is equal to or less than the specified transmission trigger number, the TDFE flag will be set to 1 again even after being read as 1 and cleared to 0.
In case of data writing to the FTDR register by the DMAC, the FSR.TDFE flag remains 1 after the DMAC transfer completes. However, DMAC transfer is possible regardless of the FSR.TDFE flag setting.
The number of transmit data bytes in the FTDR register can be checked by the 8 higher-order bits of the FIFO data count register (FDR).

33.8.2 FRDR Register Reading and RDF Flag

The RDF flag in the serial status register (FSR) is set when the number of receive data bytes in the receive FIFO data register (FRDR) has become equal to or greater than the reception trigger number set by bits RTRG[1:0] in the FIFO control register (FCR) or bits RFTC[4:0] in the FIFO trigger control register (FTCR). After the RDF flag is set, receive data equivalent to the trigger number can be read from the FRDR register, allowing efficient continuous reception.
However, if the number of data bytes in the FRDR register exceeds the reception trigger number, the RDF flag will be set to 1 again even after being read as 1 and cleared to 0.
In case of data reading from the FRDR register by the DMAC, the FSR.RDF flag remains 1 after the DMAC transfer completes. However, DMAC transfer is possible regardless of the FSR.RDF flag setting.
The number of receive data bytes in the FRDR register can be checked by the 8 lower-order bits of the FIFO data count register (FDR).

33.8.3 Break Detection and Processing

When a framing error (FER) is detected, a break signal can be detected by reading the RXD pin value directly. In a break, the input from the RXD pin becomes all low. Therefore, the FER flag in the serial status register (FSR) is set to 1 and the parity error flag (PER) may also be set to 1.
Upon detection of a break signal, the SCIFA stops the received data transfer to the FRDR register but continues the receive operation.

33.8.4 Writing to the SPTR Register

b6, b4, b2, and b0 of the SPTR register respectively indicate the input status of their corresponding pins. (See the description of each bit of section 33.2.12, Serial Port Register (SPTR) for details.)
Writings to these bits in 1-bit unit are handled as read-modify-write, which may lead to undesired values to be written. To avoid this, when modifying the SPB2DT or SPB2IO bit, for example, write the other bit (the bit used in combination) at the same time.

33.8.5 Break Signal Transmission

The output signal from the TXD pin is determined by the SPB2IO bit and the SPB2DT bit in the serial port register (SPTR). The break signal can be sent by using these bits.
The TXD pin does not function as a transmit data output pin during the period from when the SCIFA is initialized to when the TE bit in the SCR register is set to 1 (transmission possible). The TXD pin status during this period is replaced by the SPB2DT bit value. Therefore, the SPB2IO and SPB2DT bits in the SPTR register must have been set to 1 (high output) at first (mark (high) status).

To transmit the break signal during serial transmission, set the SPB2IO bit in the SPTR register to 1, clear the SPB2DT bit to 0 (specify a low level), and then clear the TE bit in the SCR register to 0 (transmission stop). Clearing the TE bit to 0 initializes the transmitter regardless of the current transmission status, and outputs a low level from the TXD pin.

33.8.6 Receive Data Sampling Timing and Receive Margin in Asynchronous Mode

The SCIFA operates on a base clock with a frequency 16 times the transfer rate*1. In reception, the SCIFA internally latches the received data at the rising edge of the eighth base clock pulse*1. The timing is shown in Figure 33.24.

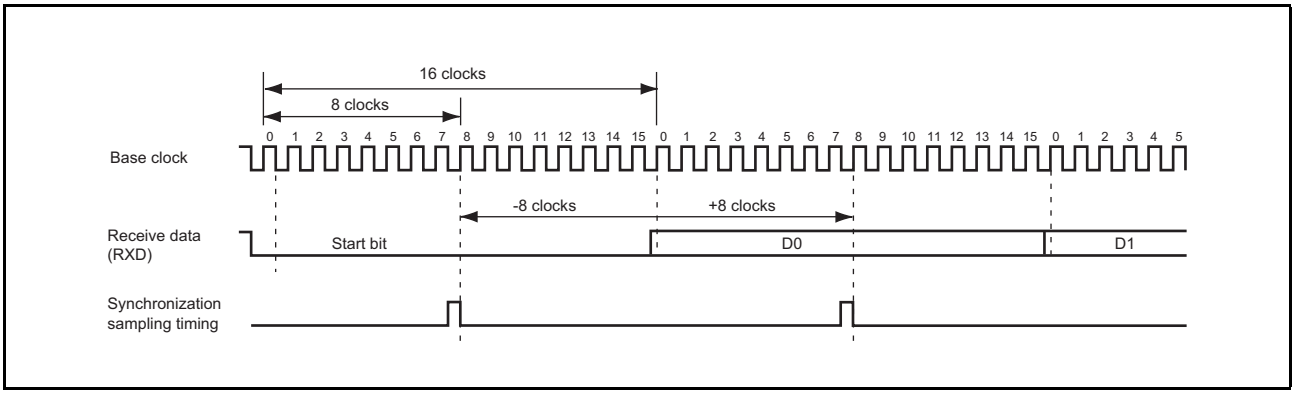


Figure 33.24 Receive Data Sampling Timing in Asynchronous Mode

Note 1. This is an example when the SEMR.ABCS0 bit is 0. When the ABCS0 bit is 1, a frequency of 8 times the bit rate is used as a base clock and receive data is sampled at the rising edge of the 4th pulse of the base clock. The receive margin in asynchronous mode can therefore be expressed as shown in equation 1.

Equation 1:

$$M = \{(0.5 - \frac{1}{2N}) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F)\} \times 100[\%]$$

Where: M: Receive margin (%)
N: Ratio of clock frequency to bit rate (N = 16)
D: Clock duty (D = 0 to 1.0)
L: Frame length (L = 9 to 12)
F: Absolute deviation of clock frequency

From equation 1, if F = 0 and D = 0.5, the receive margin is 46.875%, as given by equation 2.

Equation 2:

When D = 0.5 and F = 0:
M = (0.5 - 1/(2 ×16)) ×100% = 46.875%

This is a theoretical value. A reasonable margin to allow in system designs is 20% to 30%.

33.8.7 Note on FER Flag and PER Flag in Serial Status Register (FSR)

The FER flag and PER flag in the serial status register (FSR) are status flags that apply to next entry to be read from the receive FIFO data register (FRDR). After the CPU reads the receive FIFO data register, the flags of framing errors and parity errors in the receive data will be cleared. To check the received data for the states of framing errors and parity errors, only read the receive FIFO data register after reading the serial status register.

33.8.8 Notes on External Clock Input in Clock Synchronous Mode

Before setting the TE and RE bits in the serial control register (SCR) to 1, wait for four or more cycles of the peripheral operating clock after the external clock (SCK) is changed from 0 (low) to 1 (high). To input the external clock (SCK) (to start communication), wait for one or more cycles of the external clock after the TE and RE bits in the SCR register are set to 1.

33.8.9 Module Standby Mode Setting

SCIFA operation can be disabled or enabled using the standby control register. As the initial setting, the SCIFA operation is halted. Register access is enabled by clearing module standby mode. For details, refer to section 9, Low-Power Consumption Function.

33.8.10 Notes on Operation for Reception when an Internal Clock is Selected in Clock Synchronous Mode

When an internal clock is selected as the clock for reception in clock-synchronous mode, if the number of data stored through the receive FIFO data register (FRDR) becomes equal to or greater than the specified reception trigger number, the RDF flag is set, the RXIF interrupt request is generated and, at the same time, output of the synchronizing clock and reception of serial data are stopped. Once the number of data are again less than the specified reception trigger number, output of the synchronizing clock and the reception of serial data are restarted. In addition, if an internal clock is selected for reception in clock synchronous mode, the ORER flag is not set to 1 since no overrun occurs. Accordingly, overruns (indicated by the ORER flag) cannot be used as a BRIF interrupt source.

33.8.11 Notes on Initialization of the SCIFA

In the SCIFA initialization process, clearing of the TE and RE bits of the serial control register (SCR) should be taken place at the same time or the clearing of the RE bit should precede that of the TE bit. This is because clearing the TE bit to 0 while the RE bit remains 1 enables data reception and may lead to start of unintended data reception.

34. I²C Bus Interface (RIICa)

This LSI has two I²C bus interfaces (RIIC modules).
The RIIC module conforms with and provides a subset of the NXP I²C bus (Inter-IC-Bus) interface functions.

34.1 Overview

Table 34.1 lists the specifications of the RIIC, Figure 34.1 shows a block diagram of the RIIC, and Figure 34.2 shows an example of I/O pin connections to external circuits (I²C bus configuration example). Table 34.2 lists the I/O pins of the RIIC.

Table 34.1 RIIC Specifications (1 / 2)

Item	Description
Communications format	• I²C bus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Up to 400 kbps: fast mode
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%.
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses and device ID addresses are detectable.
Acknowledgement	• For transmission, the acknowledge bit is automatically loaded. Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: Waiting between the eighth and ninth clock cycles Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• Synchronized operation of multiple SCL clocks to avoid contention with other masters (providing support for multiple masters). • Loss in arbitration as a master Detection of mismatches of state between the SDA signal and another signal on the SDA line when a start condition is issued. Detection of a start condition being issued while in the bus busy state. Detection of mismatches of state between the data being transmitted and the signal on the SDA line in transmission as a master. • Loss in arbitration on NACK transmission Detection of mismatches of state between the data being transmitted and the signal on the SDA line in transmission of a not-acknowledge signal. • Loss in arbitration as a slave Detection of mismatches of state between the data being transmitted and the signal on the SDA line in transmission as a slave.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete
Low-power consumption function	Module-stop state can be set.

Table 34.1 RIIC Specifications (2 / 2)

Item	Description
RIIC operating modes	• Four modes: Master transmission mode, master reception mode, slave transmission mode, and slave reception mode
Event link function (output)	Four sources: • Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition • Receive-data-full (including matching with a slave address) • Transmit-data-empty (including matching with a slave address) • Transmission complete

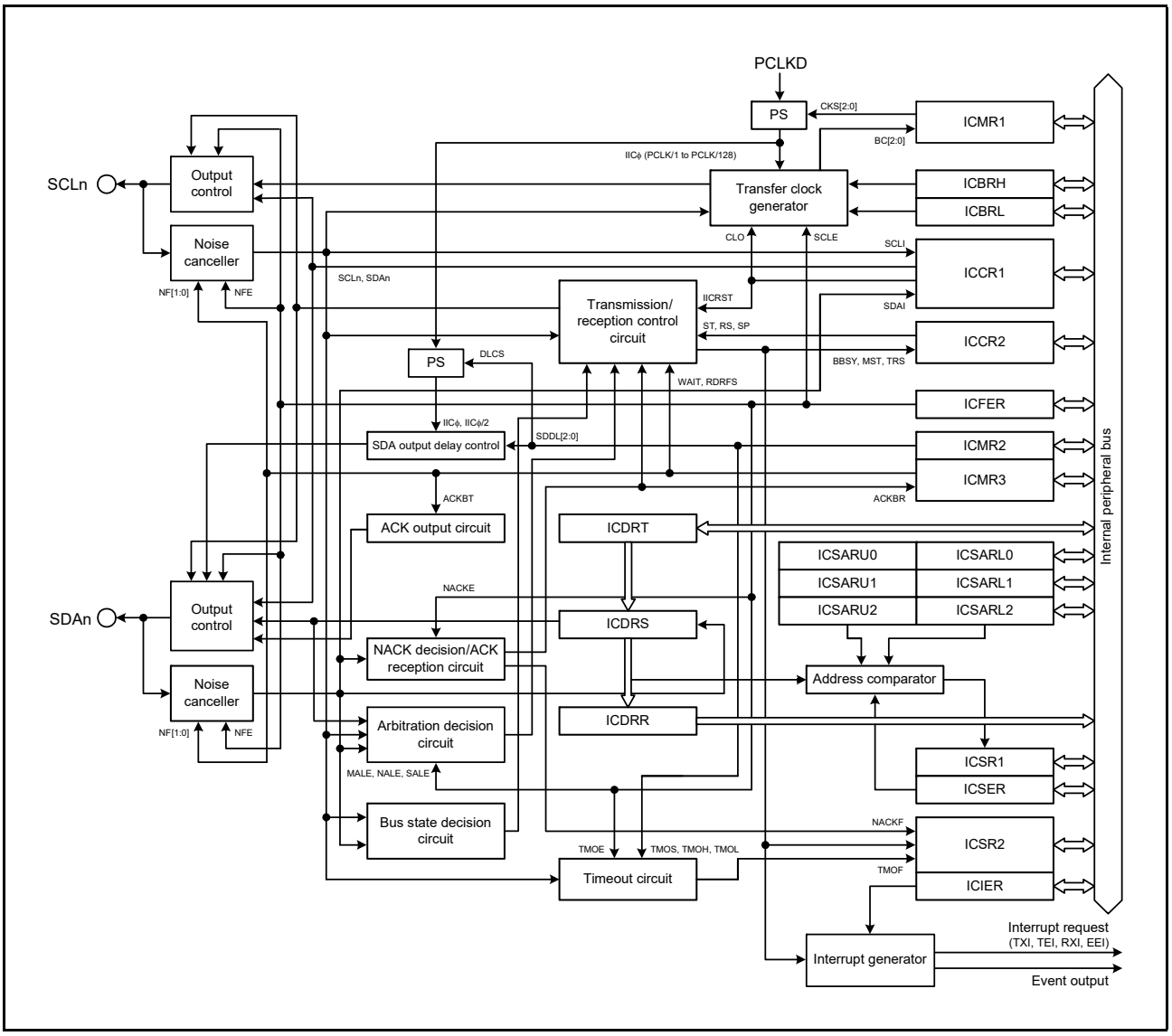


Figure 34.1 RIIC Block Diagram

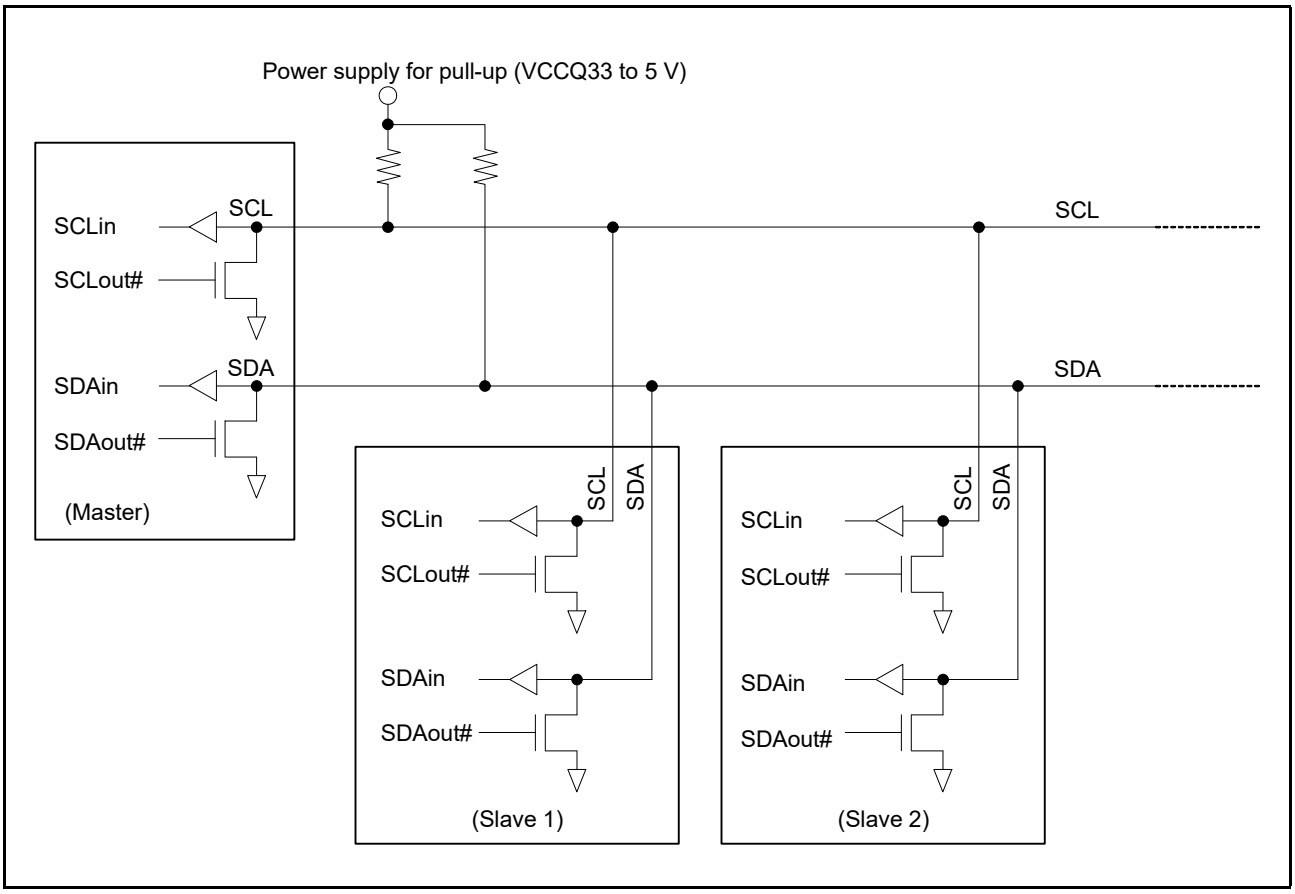


Figure 34.2 Connections to the External Circuit by the I/O Pins (I²C Bus Configuration Example)

The input level of the signals for RIIC is CMOS.

Table 34.2 Pin Configuration

Channel	Pin Name	I/O	Function
RIIC0	SCL0	I/O	RIIC0 serial clock I/O pin
	SDA0	I/O	RIIC0 serial data I/O pin
RIIC1	SCL1	I/O	RIIC1 serial clock I/O pin
	SDA1	I/O	RIIC1 serial data I/O pin

34.2 Register Descriptions

34.2.1 I²C Bus Control Register 1 (ICCR1)

The ICCR1 register controls the SDAn and SCLn signals output by the RIIC (n = 0, 1).

Address(es): RIIC0.ICCR1 A008 0900h, RIIC1.ICCR1 A008 0940h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low. 1: SDAn line is high.	R
b1	SCLI	SCL Line Monitor	0: SCLn line is low. 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: SDAn pin output is low. 1: SDAn pin output is high. • Write: 0: SDAn pin output is set to low. 1: SDAn pin output is changed to high impedance. (High level output is achieved through an external pull-up resistor.)	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: SCLn pin output is low. 1: SCLn pin output is high. • Write: 0: SCLn pin output is set to low. 1: SCLn pin output is changed to high impedance. (High level output is achieved through an external pull-up resistor.)	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Bits SCLO and SDAO can be written. 1: Bits SCLO and SDAO are protected. (This bit is always read as 1.)	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Does not output an extra SCL clock cycle (default). 1: Outputs an extra SCL clock cycle. (The CLO bit is cleared automatically after one clock cycle is output.)	R/W
b6	IICRST	I²C Bus Interface Internal Reset	0: Releases the RIIC reset or internal reset. 1: Initiates the RIIC reset or internal reset. (Clears the bit counter and the SCLn/SDAn output latch)	R/W
b7	ICE	I²C Bus Interface Enable	0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state) (Combined with the IICRST bit to select either RIIC or internal reset.)	R/W

SDAO Bit (SDA Output Control/Monitor) and SCLO Bit (SCL Output Control/Monitor)

These bits are used to directly control the SDAn and SCLn signals output from the RIIC.

When writing to these bits, also write 0 to the SOWP bit.

The result of setting these bits is input to the RIIC via the input buffer. When slave mode is selected, a start condition may be detected and the bus may be released depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, or during transmission or reception. Operation after rewriting under the above conditions is not guaranteed.

When reading these bits, the state of signals output from the RIIC can be read.

CLO Bit (Extra SCL Clock Cycle Output)

This bit is used to output an extra SCL clock cycle for debugging or error processing.
Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error.
For details on this function, refer to section 34.11.2, Extra SCL Clock Cycle Output Function.

IICRST Bit (I²C Bus Interface Internal Reset)

This bit is used to reset the internal states of the RIIC.
Setting this bit to 1 initiates an RIIC reset or internal reset.
Whether an RIIC reset or internal reset is initiated is determined according to the combination with the ICE bit. Table 34.3 lists the resets of the RIIC.
The RIIC reset resets all registers and internal states of the RIIC, and the internal reset resets the bit counter (ICMR1.BC[2:0] bits), the I²C bus shift register (ICDRS), and the I²C bus status registers (ICSR1 and ICSR2) as well as the internal states of the RIIC. For the reset conditions for each register, refer to section 34.13, Resets and Register and Function States When Issuing Each Condition.
An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the RIIC without initializing the port settings and the control and setting registers of the RIIC when the bus or RIIC hangs up due to a communication error.
If the RIIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCLn pin and SDAn pin at a high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up occurred during communication with the master device in slave mode, the states may become different between the slave device and the master device (due to the difference in the bit counter information). For this reason, do not initiate an internal reset in slave mode, but initiate restoration processing from the master device. If an internal reset is necessary because the RIIC hangs up with the SCLn line in a low level output state in slave mode, initiate an internal reset and then issue a restart condition from the master device or resume communication from the start condition issuance after issuing a stop condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start condition or restart condition from the master device, synchronization will be lost because the master and slave devices operate asynchronously.

Table 34.3 RIIC Resets

IICRST	ICE	State	Specifications
1	0	RIIC reset	Resets all registers and internal states of the RIIC.
	1	Internal reset	Resets the ICMR1.BC[2:0] bits, the ICSR1, ICSR2, and ICDRS registers, and the internal states of the RIIC.

ICE Bit (I²C Bus Interface Enable)

This bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 34.3, RIIC Resets, for the types of resets.
Set the ICE bit to 1 when using the RIIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1.
Set the ICE bit to 0 when the RIIC is not to be used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0.

34.2.2 I²C Bus Control Register 2 (ICCR2)

The ICCR2 register controls start condition issuance, restart condition issuance, and stop condition issuance.

Address(es): RIIC0.ICCR2 A008 0901h, RIIC1.ICCR2 A008 0941h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Does not request to issue a start condition. 1: Requests to issue a start condition.	R/W
b2	RS	Restart Condition Issuance Request	0: Does not request to issue a restart condition. 1: Requests to issue a restart condition.	R/W
b3	SP	Stop Condition Issuance Request	0: Does not request to issue a stop condition. 1: Requests to issue a stop condition.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmission/Reception Mode	0: Reception mode 1: Transmission mode	R/W *1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode	R/W *1
b7	BBSY	Bus Busy Detection Flag	0: The I²C bus is released (bus free state). 1: The I²C bus is occupied (bus busy state).	R

Note 1. When the ICMR1.MTWP bit is set to 1, the MST and TRS bits can be written to.

ST Bit (Start Condition Issuance Request)

This bit is used to request transition to master mode and issuance of a start condition.

When this bit is set to 1 to request to issue a start condition, a start condition is issued when the BBSY flag is set to 0 (bus free state).

For details on the start condition issuance, refer to section 34.10, Start Condition/Restart Condition/Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the ST bit
- When a start condition has been issued (A start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: Set the ST bit to 1 (start condition issuance request) when the BBSY flag is set to 0 (bus free state). Note that setting the ST bit to 1 (start condition issuance request) when the BBSY flag is set to 1 (bus busy state) is handled as a start condition issuance error and arbitration may be lost.

RS Bit (Restart Condition Issuance Request)

This bit is used to request that a restart condition be issued in master mode.

When this bit is set to 1 to request to issue a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode).

For details on the restart condition issuance, refer to section 34.10, Start Condition/Restart Condition/Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1 (1 cannot be written with the BBSY flag in ICCR2 set to 0)

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the RS bit
- When a restart condition has been issued (A start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: Do not set the RS bit to 1 while issuing a stop condition.

Note: We recommend that you issue the restart condition in master transmission mode. If 1 (requests to issue a restart condition) is written to the RS bit in slave mode, the restart condition is not issued but the RS bit remains set to 1. If the operating mode changes to master mode with the bit not being cleared, note that the restart condition may be issued.

SP Bit (Stop Condition Issuance Request)

This bit is used to request that a stop condition be issued in master mode.

When this bit is set to 1 to request to issue a stop condition, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode).

For details on the stop condition issuance, refer to section 34.10, Start Condition/Restart Condition/Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the SP bit
- When a stop condition has been issued (A stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: Writing to the SP bit is not possible while the setting of the BBSY flag is 0 (bus free state).

Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS Bit (Transmission/Reception Mode)

This bit indicates transmit or reception mode.
The RIIC is in reception mode when the TRS bit is set to 0 and is in transmission mode when the bit is set to 1.
Combination of this bit and the MST bit indicates the operating mode of the RIIC.
The value of TRS bit is automatically changed to 1 for transmission mode or 0 for reception mode by issuing or detection of a start condition and setting of the R/W# bit. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.
[Setting conditions] One of the following conditions is satisfied:

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the BBSY flag set to 0 (bus free state) and the ST bit set to 1)
- When a restart condition is issued normally according to the restart condition issuance request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit added to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1

[Clearing conditions] One of the following conditions is satisfied:

- When a stop condition is detected
- The AL (arbitration-lost) flag in ICSR2 being set to 1
- In master mode, reception of a slave address to which an R/W# bit with the value 1 is appended
- In slave mode, a match between the received address and the address enabled in ICSER when the value of the received R/W# bit is 0 (including cases where the received address is the general call address)
- In slave mode, a restart condition is detected (a start condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

The R/W# bit, which is contained in transmit data, indicates the transmit and receive direction. Data is transferred from the slave device to the master device when the R/W# bit is 1, or from the master device to the slave device when the R/W# bit is 0.

MST Bit (Master/Slave Mode)

This bit indicates master or slave mode.
The RIIC is in slave mode when the MST bit is set to 0 and is in master mode when the bit is set to 1. Combination of this bit and the TRS bit indicates the operating mode of the RIIC.
The value of the MST bit is automatically changed to 1 for master mode or 0 for slave mode by issuing of a start condition and issuing or detection of a stop condition, etc. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.
[Setting conditions] One of the following conditions is satisfied:

- When a start condition is issued normally according to the start condition issuance request (when a start condition is detected with the BBSY flag set to 0 (bus free state) and the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1

[Clearing conditions] One of the following conditions is satisfied:

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

BBSY Flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C bus is occupied (bus busy state) or released (bus free state).
This bit is set to 1 when the SDAn line changes from high to low under the condition of SCLn line = high, assuming that a start condition has been issued.
When the SDAn line changes from low to high under the condition of SCLn line = high, this bit is set to 0 after the bus free time (specified in ICBRL) start condition is not detected, assuming that a stop condition has been issued.
[Setting condition]

- When a start condition is detected

[Clearing conditions] One of the following conditions is satisfied:

- When the bus free time (specified in ICBRL) start condition is not detected after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (RIIC reset)

34.2.3 I²CBus Mode Register 1 (ICMR1)

The ICMR1 register specifies the number of bits of the down counter and the reference clock source.

Address(es): RIIC0.ICMR1 A008 0902h, RIIC1.ICMR1 A008 0942h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits	R/W *1
b3	BCWP	BC Write Protect	0: Enables a value to be written in the BC[2:0] bits. (This bit is read as 1.)	R/W *1
b6 to b4	CKS[2:0]	Internal Reference Clock Selection	Selects the internal reference clock source (IICϕ) for the RIIC. b6 b4 0 0 0: PCLKD/1 clock 0 0 1: PCLKD/2 clock 0 1 0: PCLKD/4 clock 0 1 1: PCLKD/8 clock 1 0 0: PCLKD/16 clock 1 0 1: PCLKD/32 clock 1 1 0: PCLKD/64 clock 1 1 1: PCLKD/128 clock	R/W
b7	MTWP	MST/TRS Write Protect	0: Disables writing to the MST and TRS bits in ICCR2. 1: Enables writing to the MST and TRS bits in ICCR2.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] Bits (Bit Counter)

These bits function as a counter that indicates the number of bits remaining to be transferred at the detection of a rising edge on the SCLn line. Although these bits are writable and readable, it is not necessary to access these bits under normal conditions.

To write to these bits, specify the number of bits to be transferred plus one (data is transferred with an additional acknowledge bit) between transferred frames when the SCLn line is at a low level.

The values of the BC[2:0] bits return to 000b at the end of a data transfer including the acknowledge bit or when a start condition including a restart condition is detected.

34.2.4 I²C Bus Mode Register 2 (ICMR2)

The ICMR2 register specifies various settings regarding the timeout detection function and SDA output delay function.

Address(es): RIIC0.ICMR2 A008 0903h, RIIC1.ICMR2 A008 0943h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOS	Timeout Detection Time Selection	0: Long mode is selected. 1: Short mode is selected.	R/W
b1	TMOL	Timeout L Count Control	0: Count is disabled while the SCLn line is at a low level. 1: Count is enabled while the SCLn line is at a low level.	R/W
b2	TMOH	Timeout H Count Control	0: Count is disabled while the SCLn line is at a high level. 1: Count is enabled while the SCLn line is at a high level.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles	R/W
b7	DLCS	SDA Output Delay Clock Source Selection	0: The internal reference clock (IICϕ) is selected as the clock source of the SDA output delay counter. 1: The internal reference clock divided by 2 (IICϕ/2) is selected as the clock source of the SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) only becomes valid when SCL is at the low level. When SCL is at the high level, the setting DLCS = 1 becomes invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS Bit (Timeout Detection Time Selection)

This bit is used to select long mode or short mode for the timeout detection time when the timeout function is enabled (TMOE bit = 1 in ICFER). When this bit is set to 0, long mode is selected. When this bit is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14 bit-counter. While the SCLn line is in the state that enables this counter as specified by bits TMOH and TMOL, the counter counts up in synchronization with the internal reference clock (IICϕ) as a count source.
For details on the timeout function, refer to section 34.11.1, Timeout Function.

TMOL Bit (Timeout L Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held low when the timeout function is enabled (TMOE bit = 1 in ICFER).

TMOH Bit (Timeout H Count Control)

This bit is used to enable or disable the internal counter of the timeout function to count up while the SCLn line is held high when the timeout function is enabled (TMOE bit = 1 in ICFER).

SDDL[2:0] Bits (SDA Output Delay Counter)

The SDA output can be delayed by the SDDL[2:0] setting. This counter works with the clock source selected by the DLCS bit. The setting of this function can be used for all types of SDA output, including the transmission of the acknowledge bit.

Set the SDA output delay time to meet the I^{2}C bus standard (within the data enable time/acknowledge enable time*1) and to be within 250 ns (SCL-clock low-level period - the data setup time). Note that, if a value outside the standard is set, communication with communication devices may malfunction or it may seemingly become a start condition or stop condition depending on the bus state.

For details on this function, refer to section 34.5, Facility for Delaying SDA Output.

Note 1. Data enable time/acknowledge enable time
900 ns (up to 400 kbps: fast mode [Fm])

34.2.5 I²CBus Mode Register 3 (ICMR3)

The ICMR3 register specifies the settings for acknowledgement and wait and digital noise filter.

Address(es): RIIC0.ICMR3 A008 0904h, RIIC1.ICMR3 A008 0944h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Selection	b1 b0 0 0: Noise of up to one IICϕ cycle is filtered out (single-stage filter). 0 1: Noise of up to two IICϕ cycles is filtered out (2-stage filter). 1 0: Noise of up to three IICϕ cycles is filtered out (3-stage filter). 1 1: Noise of up to four IICϕ cycles is filtered out (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: A 0 is received as the acknowledge bit (ACK reception). 1: A 1 is received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: A 0 is sent as the acknowledge bit (ACK transmission). 1: A 1 is sent as the acknowledge bit (NACK transmission).	R/W *1
b4	ACKWP	ACKBT Write Protect	0: Modification of the ACKBT bit is disabled. 1: Modification of the ACKBT bit is enabled.	W*1
b5	RDRFS	RDRF Flag Set Timing Selection	0: The RDRF flag is set at the rising edge of the ninth SCL clock cycle. (The SCLn line is not held low at the falling edge of the eighth clock cycle.) 1: The RDRF flag is set at the rising edge of the eighth SCL clock cycle. (The SCLn line is held low at the falling edge of the eighth clock cycle.) Low-hold is released at the ninth cycle since a value is written to the ACKBT bit.	R/W *2
b6	WAIT	WAIT	0: No WAIT (The period between ninth clock cycle and first clock cycle is not held low.) 1: WAIT (The period between ninth clock cycle and first clock cycle is held low.) Low-hold is released by reading ICDRR.	R/W *2
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Write to the ACKBT bit only while the ACKWP bit is already 1. If it is attempted to write 1 to both the ACKWP and ACKBT bits at the same time, the ACKBT bit will not be set to 1.

Note 2. The WAIT and RDRFS bits are valid only in reception mode. These bits are invalid in transmission mode.

NF[1:0] Bits (Number of Noise Filter Stages Select)

These bits are used to select the number of stages in the digital noise filter.

For details on the digital noise filter function, refer to section 34.6, Digital Noise-Filter Circuits.

ACKBR Bit (Receive Acknowledge)

This bit is used to store the acknowledge bit information received from the receive device in transmission mode.
[Setting condition]

- When 1 (Not Acknowledge) is received as the acknowledge bit with the TRS bit in ICCR2 set to 1

[Clearing conditions] One of the following conditions is satisfied:

- When 0 (Acknowledge) is received as the acknowledge bit with the TRS bit in ICCR2 set to 1
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (RIIC reset)

ACKBT Bit (Transmit Acknowledge)

This bit is used to set the bit to be sent at the acknowledge timing in reception mode.
[Setting condition]

- When 1 (Not Acknowledge) is written to this bit with the ACKWP bit set to 1

[Clearing conditions] One of the following conditions is satisfied:

- When 0 (Acknowledge) is written to this bit with the ACKWP bit set to 1
- When stop condition issuance is detected (when a stop condition is detected with the SP bit in ICCR2 set to 1)
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (RIIC reset)

ACKWP Bit (ACKBT Write Protect)

This bit is used to control the modification of the ACKBT bit.

RDRFS Bit (RDRF Flag Set Timing Selection)

This bit is used to select the RDRF flag set timing in reception mode and also to select whether to hold the SCLn line low at the falling edge of the eighth SCL clock cycle.
When the RDRFS bit is 0, the SCLn line is not held low at the falling edge of the eighth SCL clock cycle, and the RDRF flag is set to 1 at the rising edge of the ninth SCL clock cycle.
When the RDRFS bit is 1, the RDRF flag is set to 1 at the rising edge of the eighth SCL clock cycle and the SCLn line is held low at the falling edge of the eighth SCL clock cycle. Low-hold state is released at the ninth clock cycle or later, by writing the ACKBT bit.
After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1) according to receive data.

WAIT Bit (WAIT)

This bit is used to control whether to hold the period between the ninth SCL clock cycle and the first SCL clock cycle low until the receive data buffer (ICDRR) is completely read each time single-byte data is received in reception mode.
When the WAIT bit is 0, the receive operation is continued without holding the period between the ninth and the first SCL clock cycle low. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.
When the WAIT bit is 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When writing 0 to the WAIT bit, be sure to read the ICDRR beforehand.

34.2.6 I²CBus Function Enable Register (ICFER)

The ICFER register specifies the settings for various arbitration functions.

Address(es): RIIC0.ICFER A008 0905h, RIIC1.ICFER A008 0945h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOE	Timeout Function Enable	0: The timeout function is disabled. 1: The timeout function is enabled.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Master arbitration-lost detection is disabled. (Disables the arbitration-lost detection function and does not clear the MST and TRS bits in ICCR2 automatically when arbitration is lost.) 1: Master arbitration-lost detection is enabled. (Enables the arbitration-lost detection function and clears the MST and TRS bits in ICCR2 automatically when arbitration is lost.)	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: NACK transmission arbitration-lost detection is disabled. 1: NACK transmission arbitration-lost detection is enabled.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Slave arbitration-lost detection is disabled. 1: Slave arbitration-lost detection is enabled.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Transfer operation is not suspended during NACK reception (transfer suspension disabled). 1: Transfer operation is suspended during NACK reception (transfer suspension enabled).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: No digital noise filter circuit is used. 1: A digital noise filter circuit is used.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: No SCL synchronous circuit is used. 1: An SCL synchronous circuit is used.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

TMOE Bit (Timeout Function Enable)

This bit is used to enable or disable the timeout function.
For details on the timeout function, refer to section 34.11.1, Timeout Function.

MALE Bit (Master Arbitration-Lost Detection Enable)

This bit is used to specify whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.
For details on master arbitration lost detection function, see section 34.9.1, Master Arbitration-Lost Detection (MALE Bit).

NALE Bit (NACK Transmission Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when ACK is detected during transmission of NACK in reception mode (such as when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with different number of receive bytes).
For details on NACK transmission arbitration-lost detection function, section 34.9.2, Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit).

SALE Bit (Slave Arbitration-Lost Detection Enable)

This bit is used to specify whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmission mode (such as when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs due to noise).
For details on slave arbitration-lost detection function, see section 34.9.3, Slave Arbitration-Lost Detection (SALE Bit).

NACKE Bit (NACK Reception Transfer Suspension Enable)

This bit is used to specify whether to continue or discontinue the transfer operation when NACK is received from the slave device in transmission mode. Normally, set this bit to 1.
When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended.
When the NACKE bit is 0, the next transfer operation is continued regardless of the received acknowledge content.
For details on the NACK reception transfer suspension function, refer to section 34.8.2, NACK Reception Transfer Suspension Function.

SCLE Bit (SCL Synchronous Circuit Enable)

This bit is used to specify whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.
When the SCLE bit is set to 0 (no SCL synchronous circuit used), the RIIC does not synchronize the SCL clock with the SCL input clock. In this setting, the RIIC outputs the SCL clock with the transfer rate set in ICBRH and ICBRL regardless of the SCLn line state. For this reason, if the bus load of the I^2C bus line is much larger than the specification value or if the SCL clock output overlaps in multiple masters, the short-cycle SCL clock that does not meet the specification may be output. When no SCL synchronous circuit is used, it also affects the issuance of a start condition, restart condition, and stop condition, and the continuous output of extra SCL clock cycles.
This bit must not be set to 0 except for checking the output of the set transfer rate.
For details on SCL synchronous circuit function, see section 34.4, SCL Synchronization Circuit.

34.2.7 I²C Bus Status Enable Register (ICSER)

The ICSER register specifies the settings for enabling slave addresses and ID address detection.

Address(es): RIIC0.ICSER A008 0906h, RIIC1.ICSER A008 0946h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Slave address in ICSARL0 and ICSARU0 is disabled. 1: Slave address in ICSARL0 and ICSARU0 is enabled.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Slave address in ICSARL1 and ICSARU1 is disabled. 1: Slave address in ICSARL1 and ICSARU1 is enabled.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Slave address in ICSARL2 and ICSARU2 is disabled. 1: Slave address in ICSARL2 and ICSARU2 is enabled.	R/W
b3	GCAE	General Call Address Enable	0: General call address detection is disabled. 1: General call address detection is enabled.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device-ID Address Detection Enable	0: Device-ID address detection is disabled. 1: Device-ID address detection is enabled.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SARyE Bit (Slave Address Register y Enable) (y = 0 to 2)

This bit is used to enable or disable the slave address set in ICSARLy and ICSARUy.

When this bit is set to 1, the slave address set in ICSARLy and ICSARUy is enabled and is compared with the received slave address.

When this bit is set to 0, the slave address set in ICSARLy and ICSARUy is disabled and is ignored even if it matches the received slave address.

GCAE Bit (General Call Address Enable)

This bit is used to specify whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the RIIC recognizes the received slave address as the general call address independently of the slave addresses set in ICSARLy and ICSARUy (y = 0 to 2) and performs data receive operation.

When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE Bit (Device-ID Address Detection Enable)

This bit is used to specify whether to recognize and execute the Device-ID address when a device ID (1111 100b) is received in the first frame after a start condition or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the RIIC recognizes that the Device-ID address has been received. When the following R/W# bit is 0 [W], the RIIC recognizes the second and the following frames as slave addresses and continues the receive operation.

When this bit is set to 0, the RIIC ignores the received first frame even if it matches the device ID address and recognizes the first frame as a normal slave address.

For details on the device-ID address detection, refer to section 34.7.3, Device-ID Address Detection.

34.2.8 I²C Bus Interrupt Enable Register (ICIER)

The ICIER register enables or disables interrupt requests regarding RIIC.

Address(es): RIIC0.ICIER A008 0907h, RIIC1.ICIER A008 0947h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Timeout interrupt request (TMOI) is disabled. 1: Timeout interrupt request (TMOI) is enabled.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Arbitration-lost interrupt request (ALI) is disabled. 1: Arbitration-lost interrupt request (ALI) is enabled.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Start condition detection interrupt request (STI) is disabled. 1: Start condition detection interrupt request (STI) is enabled.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Stop condition detection interrupt request (SPI) is disabled. 1: Stop condition detection interrupt request (SPI) is enabled.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: NACK reception interrupt request (NAKI) is disabled. 1: NACK reception interrupt request (NAKI) is enabled.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Receive data full interrupt request (RXI) is disabled. 1: Receive data full interrupt request (RXI) is enabled.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Transmit end interrupt request (TEI) is disabled. 1: Transmit end interrupt request (TEI) is enabled.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Transmit data empty interrupt request (TXI) is disabled. 1: Transmit data empty interrupt request (TXI) is enabled.	R/W

TMOIE Bit (Timeout Interrupt Request Enable)

This bit is used to enable or disable timeout interrupt requests (TMOI) when the TMOF flag in ICSR2 is set to 1. A TMOI interrupt request is canceled by setting the TMOF flag or the TMOIE bit to 0.

ALIE Bit (Arbitration-Lost Interrupt Request Enable)

This bit is used to enable or disable arbitration-lost interrupt requests (ALI) when the AL flag in ICSR2 is set to 1. An ALI interrupt request is canceled by setting the AL flag or the ALIE bit to 0.

STIE Bit (Start Condition Detection Interrupt Request Enable)

This bit is used to enable or disable start condition detection interrupt requests (STI) when the START flag in ICSR2 is set to 1. An STI interrupt request is canceled by setting the START flag or the STIE bit to 0.

SPIE Bit (Stop Condition Detection Interrupt Request Enable)

This bit is used to enable or disable stop condition detection interrupt requests (SPI) when the STOP flag in ICSR2 is set to 1. An SPI interrupt request is canceled by setting the STOP flag or the SPIE bit to 0.

NAKIE Bit (NACK Reception Interrupt Request Enable)

This bit is used to enable or disable NACK reception interrupt requests (NAKI) when the NACKF flag in ICSR2 is set to 1. An NAKI interrupt request is canceled by setting the NACKF flag or the NAKIE bit to 0.

RIE Bit (Receive Data Full Interrupt Request Enable)

This bit is used to enable or disable receive data full interrupt requests (RXI) when the RDRF flag in ICSR2 is set to 1.

TEIE Bit (Transmit End Interrupt Request Enable)

This bit is used to enable or disable transmit end interrupt requests (TEI) when the TEND flag in ICSR2 is set to 1. An TEI interrupt request is canceled by setting the TEND flag or the TEIE bit to 0.

TIE Bit (Transmit Data Empty Interrupt Request Enable)

This bit is used to enable or disable transmit data empty interrupt requests (TXI) when the TDRE flag in ICSR2 is set to 1.

34.2.9 I²C Bus Status Register 1 (ICSR1)

The ICSR1 register is a status register that indicates the status of detection of various addresses.

Address(es): RIIC0.ICSR1 A008 0908h, RIIC1.ICSR1 A008 0948h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 is not detected. 1: Slave address 0 is detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 is not detected. 1: Slave address 1 is detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 is not detected. 1: Slave address 2 is detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address is not detected. 1: General call address is detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device-ID Address Detection Flag	0: Device-ID address is not detected. 1: Device-ID address is detected. • This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID address (1111 100b) + 0[W]).	R/(W) *1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag.

AASy Flag (Slave Address y Detection Flag) (y = 0 to 2)

[Setting conditions]

For 7-bit address format: ICSARUy.FS = 0

- When the received slave address matches the SVA[6:0] value in ICSARLy with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format: ICSARUy.FS = 1

- When the received slave address matches a value of (11110b + SVA[1:0] in ICSARUy) and the following address matches the ICSARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the AASy bit after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

For 7-bit address format: ICSARUy.FS = 0

- When the received slave address does not match the SVA[6:0] value in ICSARLy with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format: ICSARUy.FS = 1

- When the received slave address does not match a value of (11110b + SVA[1:0] in ICSARUy) with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in ICSARUy) and the following address does not match the ICSARLy value with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.

GCA Flag (General Call Address Detection Flag)

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]) with the GCAE bit in ICSER set to 1 (general call address detection is enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the GCA bit after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]) with the GCAE bit in ICSER set to 1 (general call address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

DID Flag (Device-ID Address Detection Flag)

[Setting condition]

- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID address (1111 100b) + 0 [W]) with the DIDE bit in ICSER set to 1 (Device-ID address detection is enabled)
  This flag is set to 1 at the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the DID bit after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start condition or restart condition is detected does not match a value of (device ID address (1111 100b)) with the DIDE bit in ICSER set to 1 (Device-ID address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When the first frame received immediately after a start condition or restart condition is detected matches a value of (device ID address (1111 100b) + 0 [W]) and the second frame does not match any of slave addresses 0 to 2 with the DIDE bit in ICSER set to 1 (Device-ID address detection is enabled)
  This flag is set to 0 at the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

34.2.10 I²C Bus Status Register 2 (ICSR2)

The ICSR2 register is a status register that indicates the status of detection of various conditions.

Address(es): RIIC0.ICSR2 A008 0909h, RIIC1.ICSR2 A008 0949h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout is not detected. 1: Timeout is detected.	R/(W) *1
b1	AL	Arbitration-Lost Flag	0: Arbitration is not lost. 1: Arbitration is lost.	R/(W) *1
b2	START	Start Condition Detection Flag	0: Start condition is not detected. 1: Start condition is detected.	R/(W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition is not detected. 1: Stop condition is detected.	R/(W) *1
b4	NACKF	NACK Detection Flag	0: NACK is not detected. 1: NACK is detected.	R/(W) *1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data. 1: ICDRR contains receive data.	R/(W) *1
b6	TEND	Transmit End Flag	0: Data is being transmitted. 1: Data has been transmitted.	R/(W) *1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data. 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written to clear the flag.

TMOF Flag (Timeout Detection Flag)

This flag is set to 1 when the RIIC recognizes timeout after the SCLn line state remains unchanged for a certain period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified by the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (the timeout function is enabled) in master mode or in slave mode and the received slave address matches.

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the TMOF bit after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

AL Flag (Arbitration-Lost Flag)

This flag shows that bus mastership has been lost (loss in arbitration) due to a bus conflict or some other reason when a start condition is issued or an address and data are transmitted. The RIIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, sets the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The RIIC can also set the flag to indicate the detection of loss of arbitration during NACK transmission in master mode or during data transmission in slave mode.

[Setting conditions] One of the following conditions is satisfied:

When master arbitration-lost detection is enabled: ICFER.MALE = 1

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock except for the ACK period during data (including slave address) transmission in master transmission mode (when the SDAn line is driven low while the internal SDA output is at a high level (the SDAn pin is in the high-impedance state))
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition issuance request) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is set to 1 (start condition issuance request) with the BBSY flag in ICCR2 set to 1.

When NACK transmission arbitration-lost detection is enabled: ICFER.NALE = 1

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock in the ACK period during NACK transmission in reception mode

When slave arbitration-lost detection is enabled: ICFER.SALE = 1

- When the internal SDA output state does not match the SDAn line level at the rising edge of SCL clock except for the ACK period during data transmission in slave transmission mode

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the AL bit after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Table 34.4 Relationship between Arbitration-Lost Generation Sources and Arbitration-Lost Enable Functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-Lost Generation Source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 with BBSY in ICCR2 set to 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmission mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master reception mode or slave reception mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmission mode

×: Don't care

START Flag (Start Condition Detection Flag)

[Setting condition]

- When a start condition (or a restart condition) is detected

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the START bit after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

STOP Flag (Stop Condition Detection Flag)

[Setting condition]

- When a stop condition is detected

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the STOP bit after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

NACKF Flag (NACK Detection Flag)

[Setting condition]

- When acknowledge is not received (NACK is received) from the receive device in transmission mode with the NACKE bit in ICFER set to 1 (transfer suspension enabled)

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the NACKF bit after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: When the NACKF flag is set to 1, the RIIC suspends data transmission/reception. Writing to ICDRT in transmission mode or reading from ICDRR in reception mode with the NACKF flag set to 1 does not enable data transmit/receive operation. To restart data transmission/reception, set the NACKF flag to 0.

RDRF Flag (Receive Data Full Flag)

[Setting conditions] One of the following conditions is satisfied:

- When receive data has been transferred from ICDRS to ICDRR
  This flag is set to 1 at the rising edge of the eighth or ninth SCL clock cycle (selected by the RDRFS bit in ICMR3)
- When the received slave address matches after a start condition (or a restart condition) is detected with the TRS bit in ICCR2 set to 0

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the RDRF bit after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

TEND Flag (Transmit End Flag)

[Setting condition]

- At the rising edge of the ninth SCL clock cycle while the TDRE flag is 1

[Clearing conditions] One of the following conditions is satisfied:

- When 0 is written to the TEND bit after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

TDRE Flag (Transmit Data Empty Flag)

[Setting conditions] One of the following conditions is satisfied:

- When data has been transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1 (including when 1 is written to the bit)
- When the received slave address matches while the TRS bit is 1

[Clearing conditions] One of the following conditions is satisfied:

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0 (including when 0 is written to the bit)
- When 1 is written to the IICRST bit in ICCR1 to apply an RIIC reset or an internal reset

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the RIIC suspends data transmission/reception. Here, if the TDRE flag is 0 (next transmit data has been written), data is transferred to the ICDRS register and the ICDRT register becomes empty at the rising edge of the ninth clock cycle, but the TDRE flag is not set to 1.

34.2.11 I²C Slave Address Register Ly (ICSARLy) (y = 0 to 2)

The ICSARLy register specifies the settings for the slave address.

Address(es): RIIC0.ICSARL0 A008 090Ah, RIIC1.ICSARL0 A008 094Ah, RIIC0.ICSARL1 A008 090Ch, RIIC1.ICSARL1 A008 094Ch, RIIC0.ICSARL2 A008 090Eh, RIIC1.ICSARL2 A008 094Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SVA0	10-Bit Address LSB	A slave address is set.	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	A slave address is set.	R/W

SVA0 Bit (10-Bit Address LSB)

When the 10-bit address format is selected (ICSARUy.FS = 1), this bit functions as the LSB of a 10-bit address and forms the lower 8 bits of a 10-bit address in combination with the SVA[6:0] bits.
When the SARyE bit in ICSER is set to 1 (ICSARLy and ICSARUy enabled) and the ICSARUy.FS bit is 1, this bit is valid. While the ICSARUy.FS bit or SARyE bit is 0, the setting of this bit is ignored.

SVA[6:0] Bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (ICSARUy.FS = 0), these bits function as a 7-bit address. When the 10-bit address format is selected (ICSARUy.FS = 1), these bits function as the lower 8 bits of a 10-bit address in combination with the SVA0 bit.
While the SARyE bit in ICSER is 0, the setting of these bits is ignored.

34.2.12 I²C Slave Address Register Uy (ICSARUy) (y = 0 to 2)

The ICSARUy register specifies the format of the slave address.

Address(es): RIIC0.ICSARU0 A008 090Bh, RIIC1.ICSARU0 A008 094Bh, RIIC0.ICSARU1 A008 090Dh, RIIC1.ICSARU1 A008 094Dh, RIIC0.ICSARU2 A008 090Fh, RIIC1.ICSARU2 A008 094Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Selection	0: The 7-bit address format is selected. 1: The 10-bit address format is selected.	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	A slave address is set.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS Bit (7-Bit/10-Bit Address Format Selection)

This bit is used to select 7-bit address or 10-bit address for slave address y (in ICSARLy and ICSARUy).

When the SARyE bit in ICSER is set to 1 (ICSARLy and ICSARUy enabled) and the ICSARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in ICSARLy is valid, and the settings of the SVA[1:0] bits and the SVA0 bit in ICSARLy are ignored.

When the SARyE bit in ICSER is set to 1 (ICSARLy and ICSARUy enabled) and the ICSARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the settings of the SVA[1:0] bits and ICSARLy are valid.

While the SARyE bit in ICSER is 0 (ICSARLy and ICSARUy disabled), the setting of the ICSARUy.FS bit is invalid.

SVA[1:0] Bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), these bits function as the upper 2 bits of a 10-bit address.

When the SARyE bit in ICSER is set to 1 (ICSARLy and ICSARUy enabled) and the ICSARUy.FS bit is 1, these bits are valid. While the ICSARUy.FS bit or SARyE bit is 0, the setting of these bits is ignored.

34.2.13 I²C Bus Bit Rate Low-Level Register (ICBRL)

The ICBRL register specifies the low-level period of SCL clock and the delay cycle to which the SDA signal is added.

Address(es): RIIC0.ICBRL A008 0910h, RIIC1.ICBRL A008 0950h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRL works to generate the data setup time for automatic SCL low-hold operation (refer to section 34.8, Automatic Low-Hold Function for SCL); when the RIIC is used only in slave mode, this register needs to be set to a value longer than the data setup time*1.
ICBRL counts the low-level period with the internal reference clock source (IICϕ) specified by the CKS[2:0] bits in ICMR1.
If the digital noise filter is enabled (the NFE bit in ICFER is 1), set the ICBRL register to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the ICMR3.NF[1:0] bits.

Note 1. Data setup time (tSU: DAT)
100 ns (up to 400 Kbps: fast mode [Fm])

34.2.14 I²C Bus Bit Rate High-Level Register (ICBRH)

The ICBRH register is a 5-bit register to set the high-level period of SCL clock, and ICBRH is valid in master mode. If the RIIC is used only in slave mode, this register need not set the high-level period.
ICBRH counts the high-level period with the internal reference clock source (IICϕ) specified by the CKS[2:0] bits in ICMR1.

Address(es): RIIC0.ICBRH A008 0911h, RIIC1.ICBRH A008 0951h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

If the digital noise filter is enabled (the NFE bit in ICFER is 1), set the ICBRH register to a value at least one greater than the number of stages in the noise filter. Regarding the number of stages in the noise filter, see the description of the ICMR3.NF[1:0] bits.

The I²C transfer rate and the SCL clock duty are calculated using the following expression.
Transfer rate = 1 / {[(ICBRH + 1) + (ICBRL + 1)] / IICϕ*1 + SCLn line rising time [tr] + SCLn line falling time [tf]}
Duty cycle = {SCLn line rising time [tr]*2 + (ICBRH + 1) / IICϕ} / {SCLn line falling time [tf]*2 + (ICBRL + 1) / IICϕ}

Note 1. IICϕ = Set value in ICMR1.CKS[2:0]
Note 2. The SCLn line rising time [tr] and SCLn line falling time [tf] depend on the total bus line capacitance [Cb] and the pull-up resistor [Rp]. For details, see the I²C bus standard from NXP Semiconductors.

Table 34.5 lists examples of ICBRH/ICBRL settings.

Table 34.5 Examples of ICBRH/ICBRL Settings for Transfer Rate

	Operating Frequency PCLKD (MHz)		
	75		
Transfer Rate (Kbps)	**CKS[2:0]**	**ICBRH**	**ICBRL**
10	111b	26 (FAh)	30(FEh)
50	101b	20 (F4h)	23(F7h)
100	100b	19 (F3h)	23(F7h)
400	010b	11 (EBh)	24(F8h)

Note: This is an example of the setting when the rising time (tr) of the SCLn line is 300 ns and the falling time (tf) of the SCLn line is 300 ns. For the specified values of the rising time (tr) and the falling time (tf) of the SCLn line, see the I²C bus specifications from NXP Semiconductors.

34.2.15 I²C Bus Transmit Data Register (ICDRT)

The ICDRT register stores transmit data.

Address(es): RIIC0.ICDRT A008 0912h, RIIC1.ICDRT A008 0952h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the I2C bus shift register (ICDRS), it transfers the transmit data that has been written to ICDRT to ICDRS and starts transmitting data in transmission mode.
The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data has been written to ICDRT while the ICDRS data is being transmitted.
ICDRT can always be read and written. Write transmit data to ICDRT once when a transmit data empty interrupt (TXI) request is generated.

34.2.16 I²C Bus Receive Data Register (ICDRR)

The ICDRR register stores receive data.

Address(es): RIIC0.ICDRR A008 0913h, RIIC1.ICDRR A008 0953h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data has been received, the received data is transferred from the I2C bus shift register (ICDRS) to ICDRR to enable the next data to be received.
The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data has been read from ICDRR while ICDRS is receiving data.
ICDRR cannot be written. Read data from ICDRR once when a receive data full interrupt (RXI) request is generated.
If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the RIIC automatically holds the SCLn clock low one cycle before the RDRF flag is set to 1 next.

34.2.17 I²CBus Shift Register (ICDRS)

The ICDRS register is a shift register to transmit and receive data.

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—

During transmission, transmit data is transferred from ICDRT to ICDRS and is sent from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data has been received.
ICDRS cannot be accessed directly.

34.3 Operation

34.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start condition or restart condition is an address frame used to specify a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.
Figure 34.3 shows the I2C bus format, and Figure 34.4 shows the I2C bus timing.

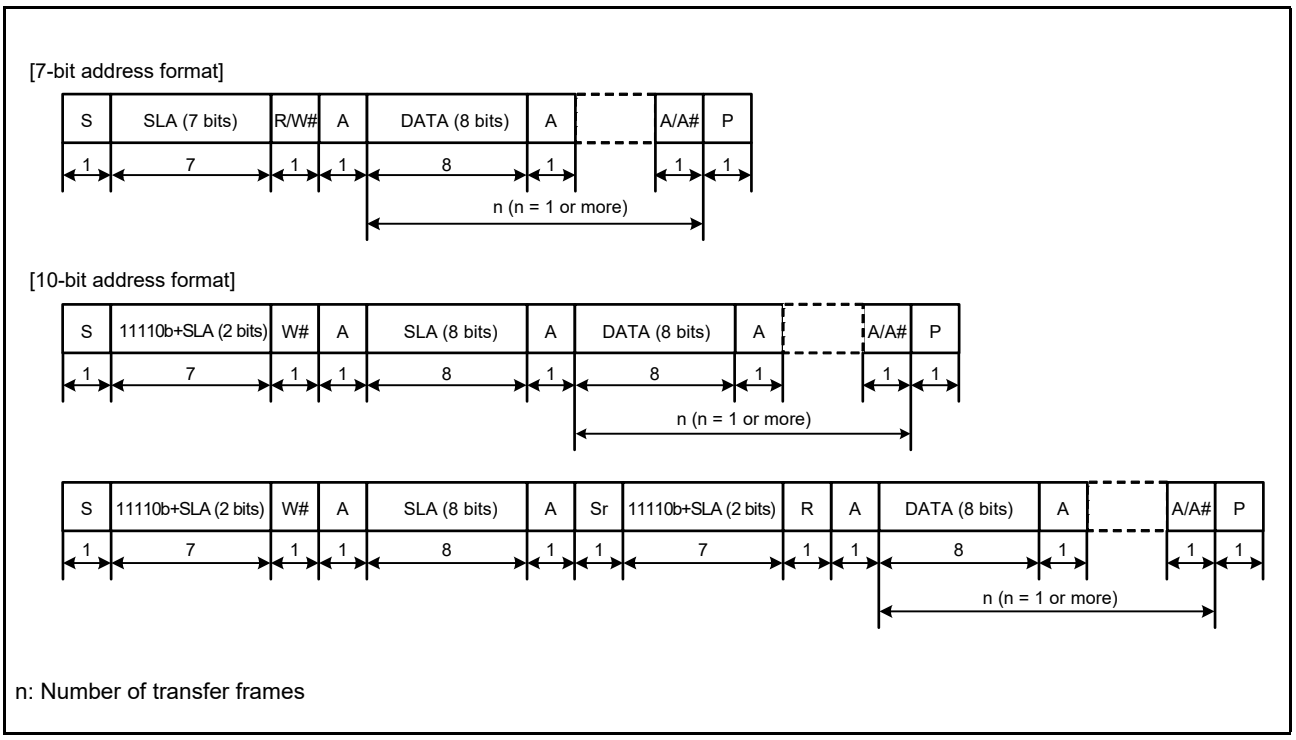


Figure 34.3 I2C Bus Format

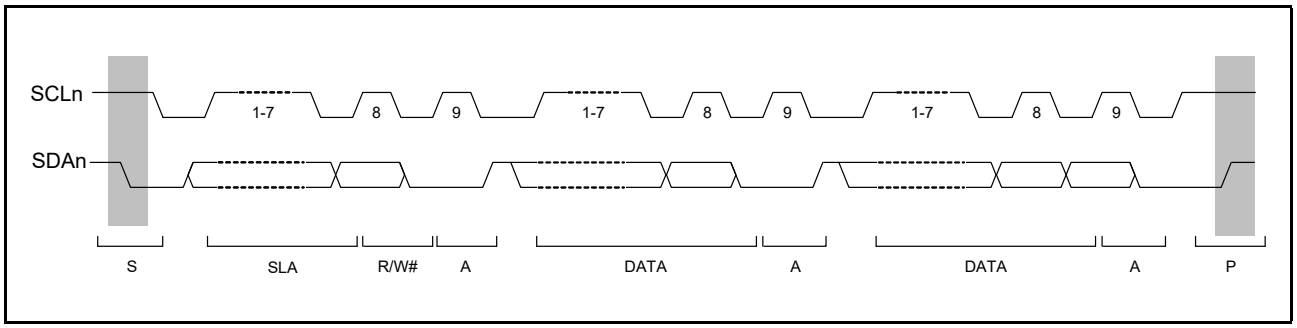


Figure 34.4 I²C Bus Timing (SLA = 7 Bits)

S: Start condition. The SDAn line is changed from the high level to the low level while the SCLn line of the master device is at a high level.

SLA: Slave address, by which the master device selects a slave device.

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0.

A: Acknowledge. The receive device drives the SDAn line low. (In master transmission mode, the slave device returns acknowledge. In master reception mode, the master device returns acknowledge.)

A#: Not Acknowledge. The receive device drives the SDAn line high.

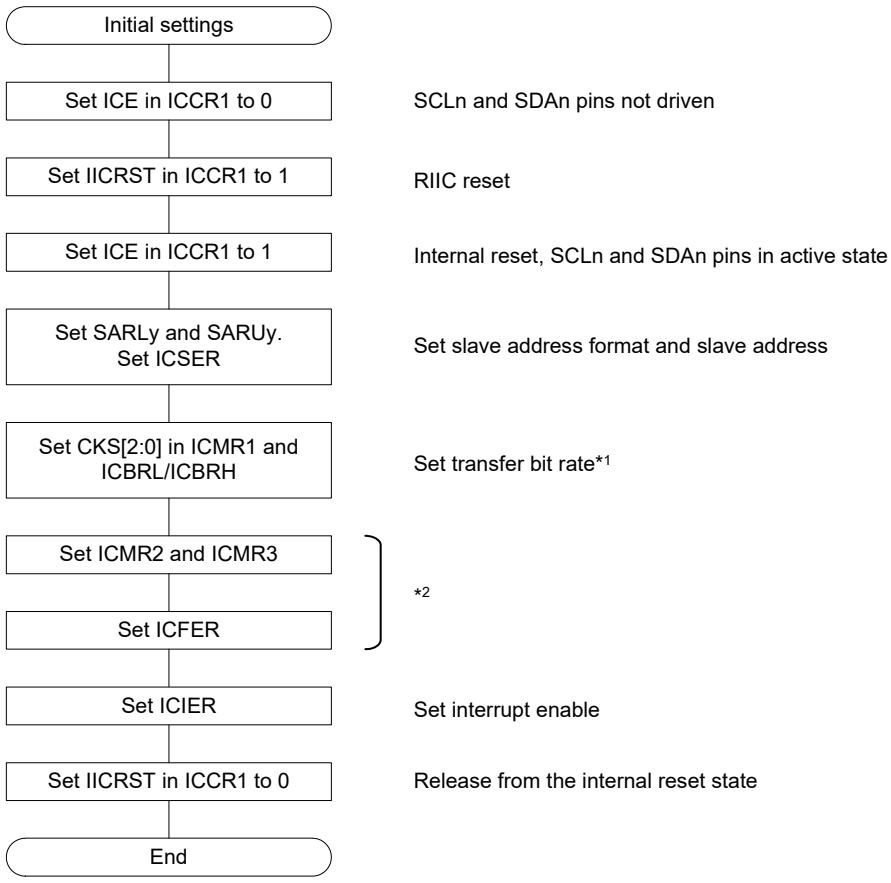
Sr: Restart condition. The SDAn line is changed from the high level to the low level after the setup time has elapsed with the SCLn line at the high level.

DATA: Transmitted or received data. The bit length of the transmitted or received data is set in ICMR1.BC[2:0].

P: Stop condition. The SDAn line is changed from the low level to the high level while the SCLn line is at a high level.

34.3.2 Initial Settings

Before starting data transmission and reception, initialize the RIIC according to the procedure in Figure 34.5.
Set the ICCR1.ICE bit to 1 (internal reset) after setting the ICCR1.IICRST bit to 1 (RIIC reset) with the ICCR1.ICE bit set to 0 (SCLn and SDAn pins in inactive state). This initializes the various flags and internal state of the ICSR1 register. After that, set registers ICSARLy, ICSARUy, ICSER, ICMR1, ICBRH, and ICBRL (y = 0 to 2), and set the other registers as necessary (for initial settings of the RIIC, see Figure 34.5). When the necessary register settings have been completed, set the ICCR1.IICRST bit to 0 (releases the RIIC reset). This step is not necessary if initialization of the RIIC has already been completed.



y = 0 to 2
Note 1. When the RIIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as necessary.

Figure 34.5 Example of RIIC Initialization Flowchart

34.3.3 Master Transmit Operation

In master transmit operation, the RIIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgements. Figure 34.6 shows an example of usage of master transmission and Figure 34.7 to Figure 34.9 show the timing of operations in master transmission.
The following describes the procedure and operations for master transmission.

(1) Initial settings. For details, refer to section 34.3.2, Initial Settings.
(2) Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. At the same time, the BBSY flag and the START flag in ICSR2 are automatically set to 1 and the ST bit is automatically set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and the MST and TRS bits in ICCR2 are automatically set to 1, placing the RIIC in master transmission mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the TRS bit to 1.
(3) Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. Once the data for transmission are written to ICDRT, the TDRE flag is automatically set to 0, the data are transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master reception mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the RIIC continues in master transmission mode.
Since the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For data transmission with an address in the 10-bit format, start by writing 1111 0b, the 2 higher-order bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.
(4) After confirming that the TDRE flag in ICSR2 is 1, write the data for transmission to the ICDRT register. The RIIC automatically holds the SCLn line low until the data for transmission are ready or a stop condition is issued.
(5) After all bytes of data for transmission have been written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition issuance request). Upon receiving a stop condition issuance request, the RIIC issues the stop condition.
(6) Upon detecting the stop condition, the RIIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave reception mode. Furthermore, it automatically sets the TDRE and TEND flags in ICSR2 to 0, and sets the STOP flag in ICSR2 to 1.
(7) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

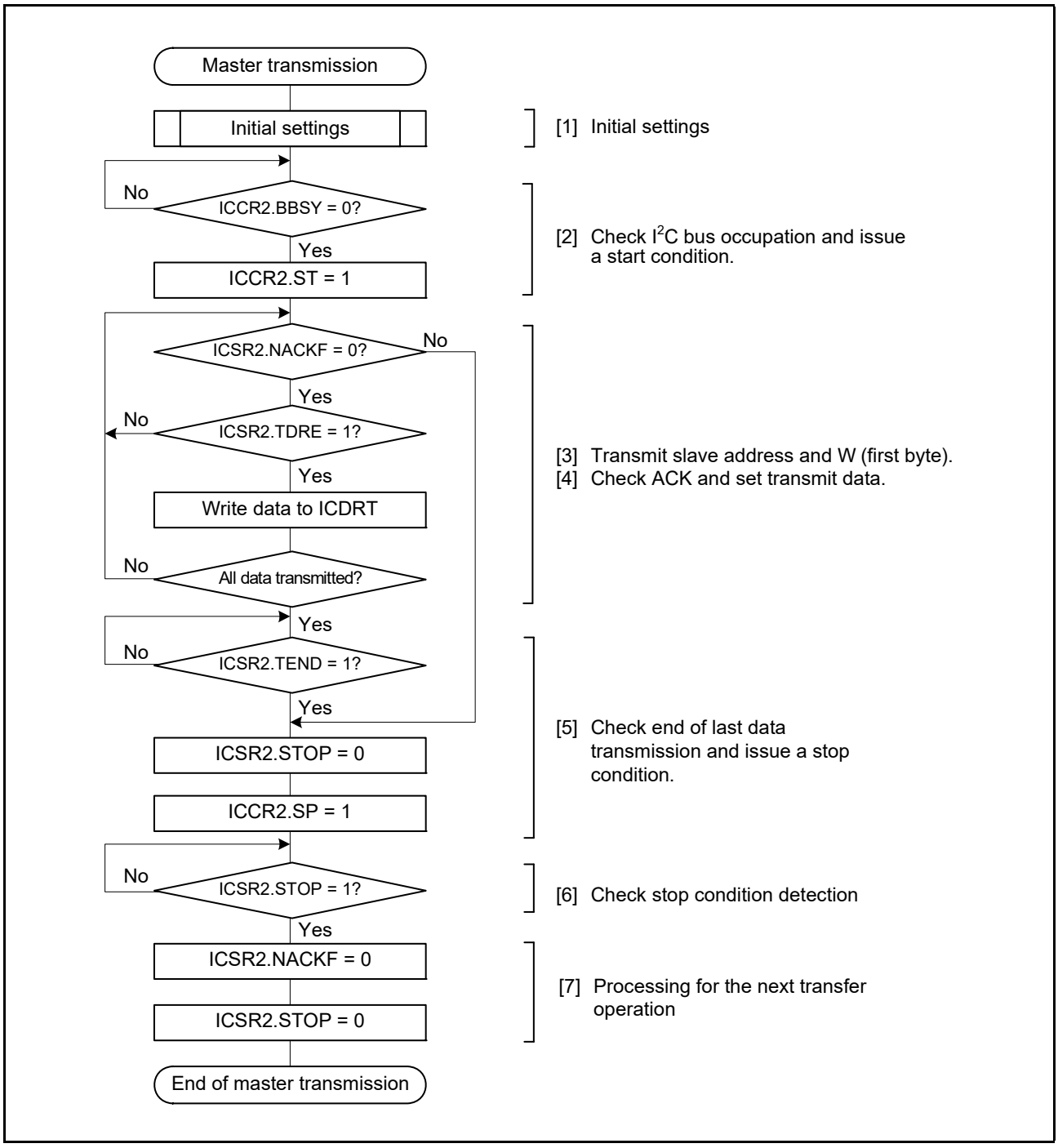


Figure 34.6 Example of Master Transmission Flowchart

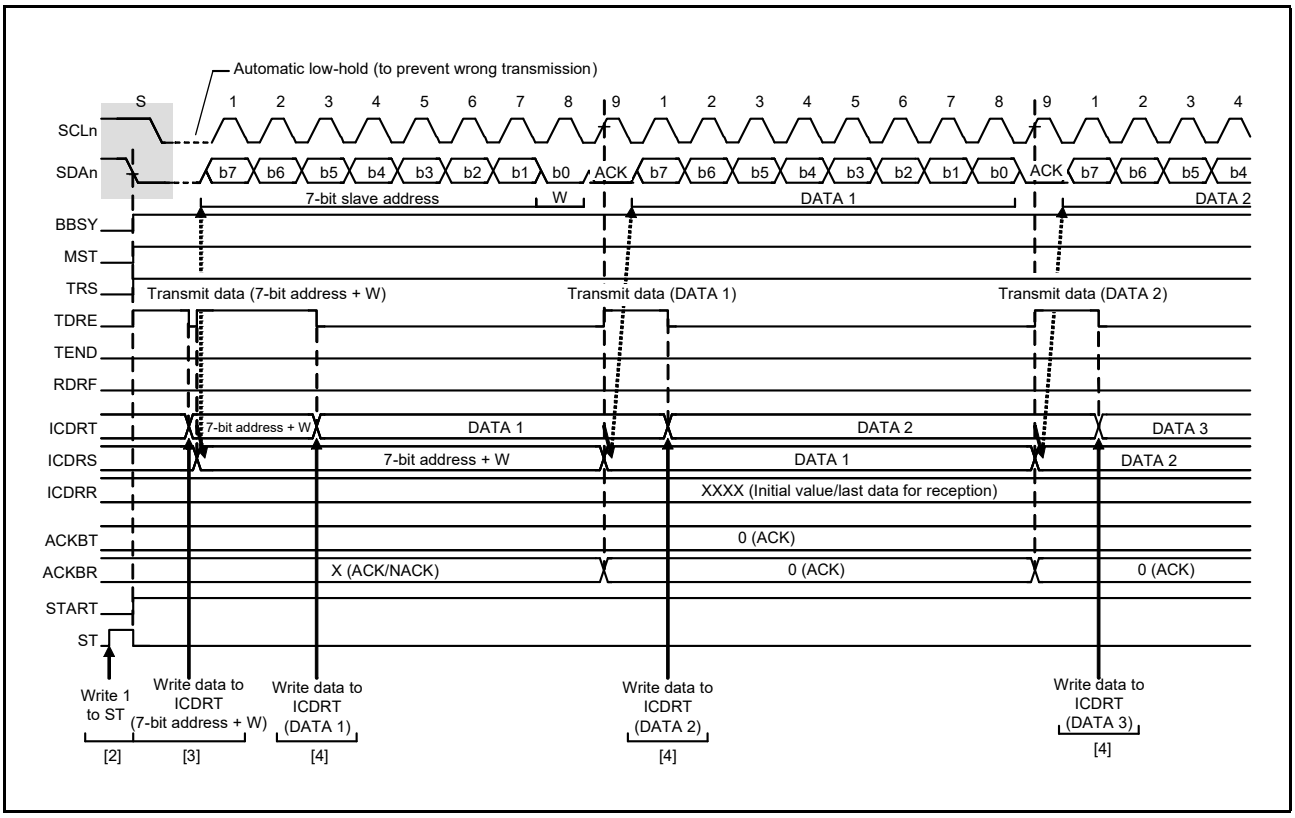


Figure 34.7 Master Transmit Operation Timing (1) (7-Bit Address Format)

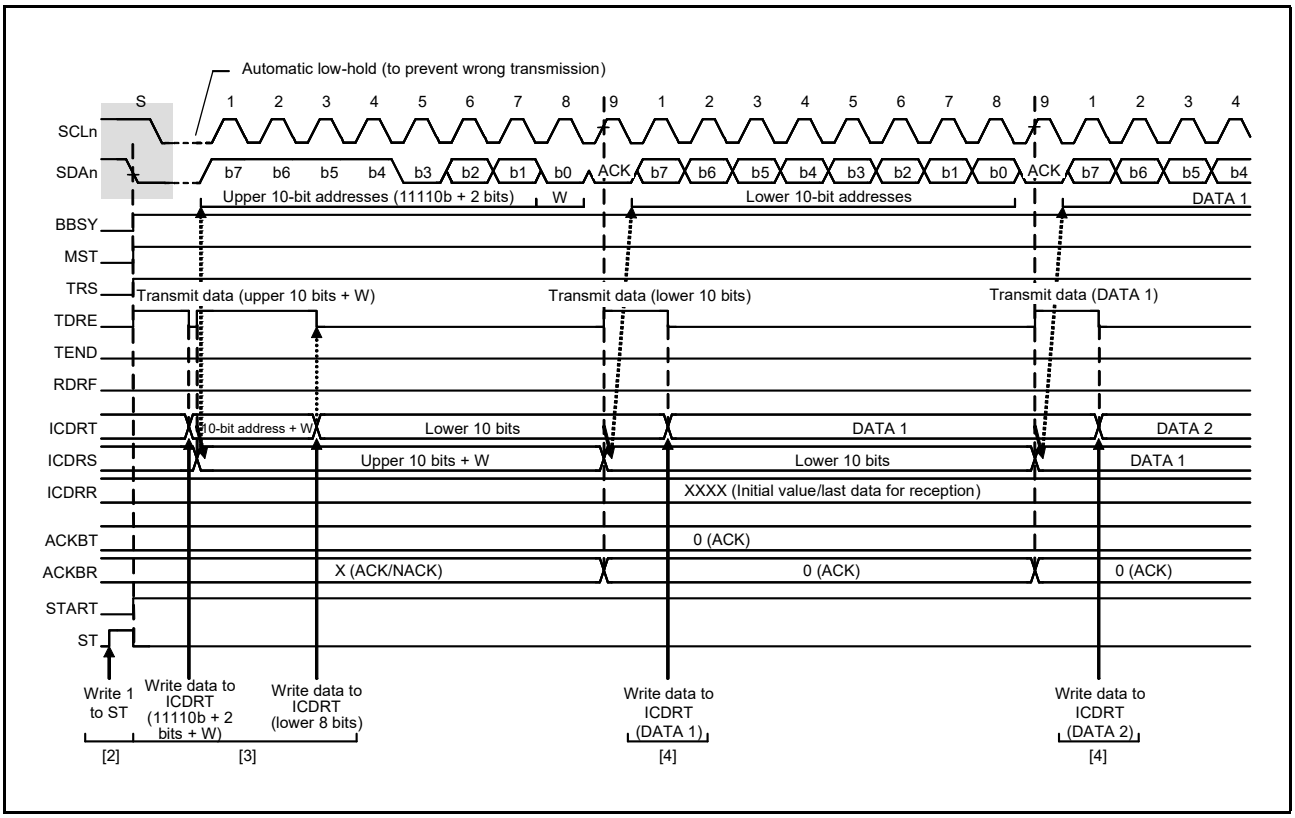


Figure 34.8 Master Transmit Operation Timing (2) (10-Bit Address Format)

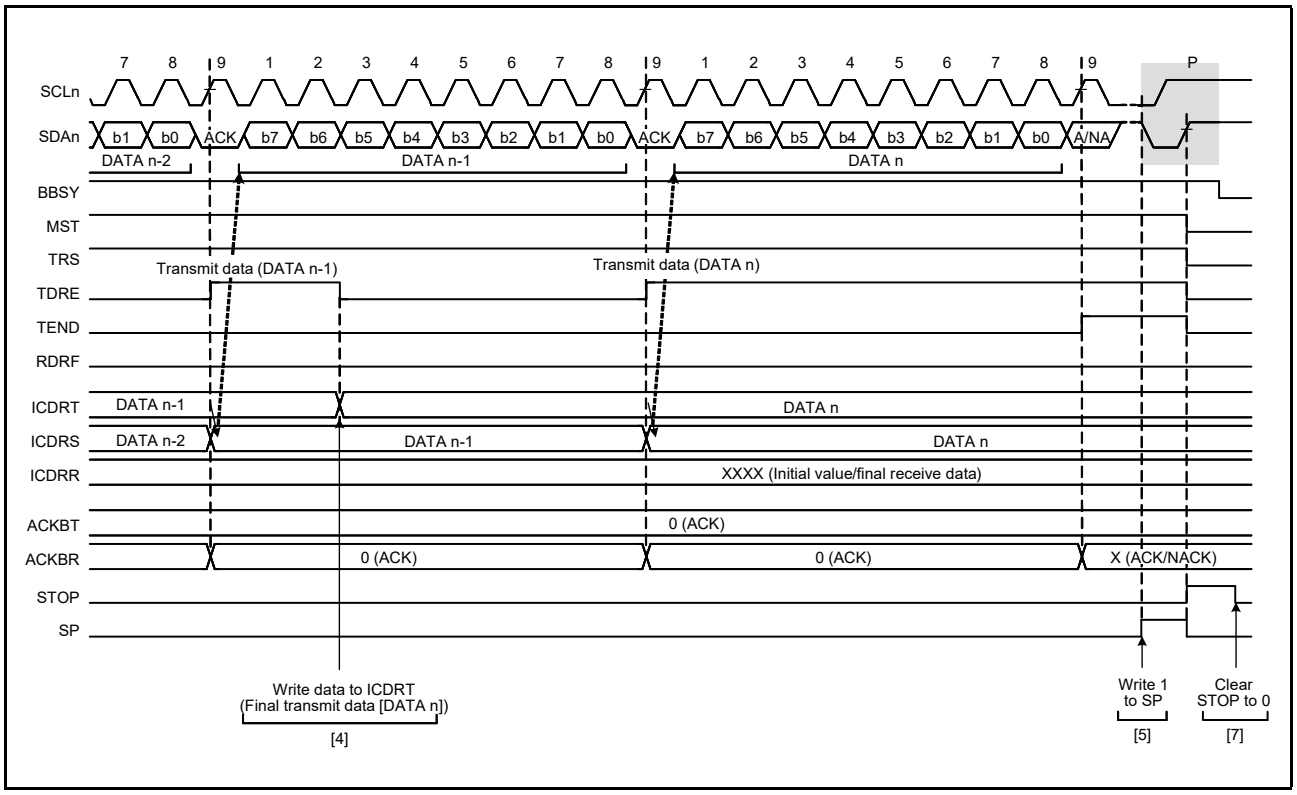


Figure 34.9 Master Transmit Operation Timing (3)

34.3.4 Master Receive Operation

In master receive operation, the RIIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgements. Since the RIIC must start by sending a slave address to the corresponding slave device, this part of the procedure is performed in master transmission mode, but the subsequent steps are in master reception mode. Figure 34.10 and Figure 34.11 show examples of usage of master reception in the 7-bit address format and Figure 34.12 to Figure 34.14 show the timing of operations in master reception.
The following describes the procedure and operations for master reception.

(1) Initial settings. For details, refer to section 34.3.2, Initial Settings.
(2) Read the BBSY flag in ICCR2 to check that the bus is open, and then set the ST bit in ICCR2 to 1 (start condition issuance request). Upon receiving the request, the RIIC issues a start condition. When the RIIC detects the start condition, the BBSY flag and the START flag in ICSR2 are automatically set to 1 and the ST bit is automatically set to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDAn line have matched while the ST bit is 1, the RIIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and the MST and TRS bits in ICCR2 are automatically set to 1, placing the RIIC in master transmission mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the TRS bit to 1.
(3) Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. Once the data for transmission are written to ICDRT, the TDRE flag is automatically set to 0, the data are transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. Once the byte containing the slave address and R/W# bit has been transmitted, the value of the ICCR2.TRS bit is automatically updated to select transmit or reception mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of SCL clock, placing the RIIC in master reception mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag is automatically set to 1.
Since the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 1111 0b, the two higher-order bits of the slave address, and the R bit places the RIIC in master reception mode.
(4) Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1; this makes the RIIC start output of the SCL clock and start data reception.
(5) After 1 byte of data has been received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of SCL clock (the clock signal) as selected by the RDRFS bit in ICMR3. Reading out ICDRR at this time will produce the received data, and the RDRF flag is automatically set to 0 at the same time. Furthermore, the value of the acknowledgement field received during the ninth cycle of SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the next to last byte, set the ICMR3.WAIT bit to 1 (for wait insertion) before reading the ICDRR (containing the second byte from last). As well as enabling NACK output even in the case of delays in processing to set the ICMR3.ACKBT bit to 1 (NACK) in step (6), due to other interrupts, etc., this fixes the SCLn line to the low level on the falling edge of the ninth clock cycle in reception of the last byte, so the state is such that issuing a stop condition is possible.
(6) When the ICMR3.RDRFS bit is 0 and the slave device must be notified that it is to end transfer for data reception after transfer of the next (final) byte, set the ICMR3.ACKBT bit to 1 (NACK).

(7) After reading out the byte before last from the ICDRR register, if the value of the ICSR2.RDRF flag is confirmed to be 1, write 1 to the SP bit in ICCR2 (stop condition issuance request) and then read the last byte from ICDRR. When ICDRR is read, the RIIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is completed or the SCLn line is released from the low-hold state.

(8) Upon detecting the stop condition, the RIIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave reception mode. Furthermore, detection of the stop condition leads to setting of the ICSR2.STOP flag to 1.

(9) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

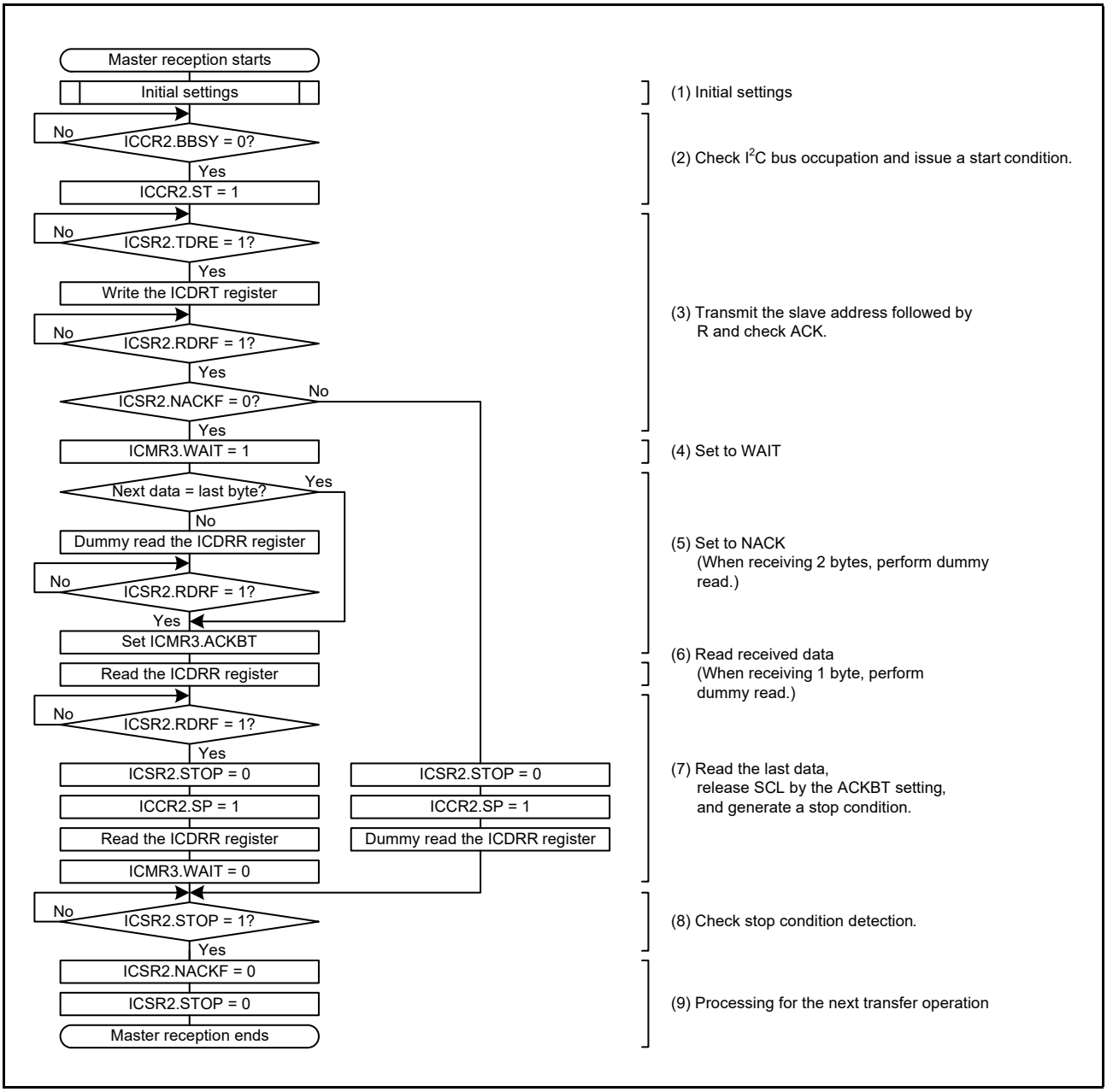


Figure 34.10 Example of Master Reception (7-Bit Address Format, 1 or 2 bytes)

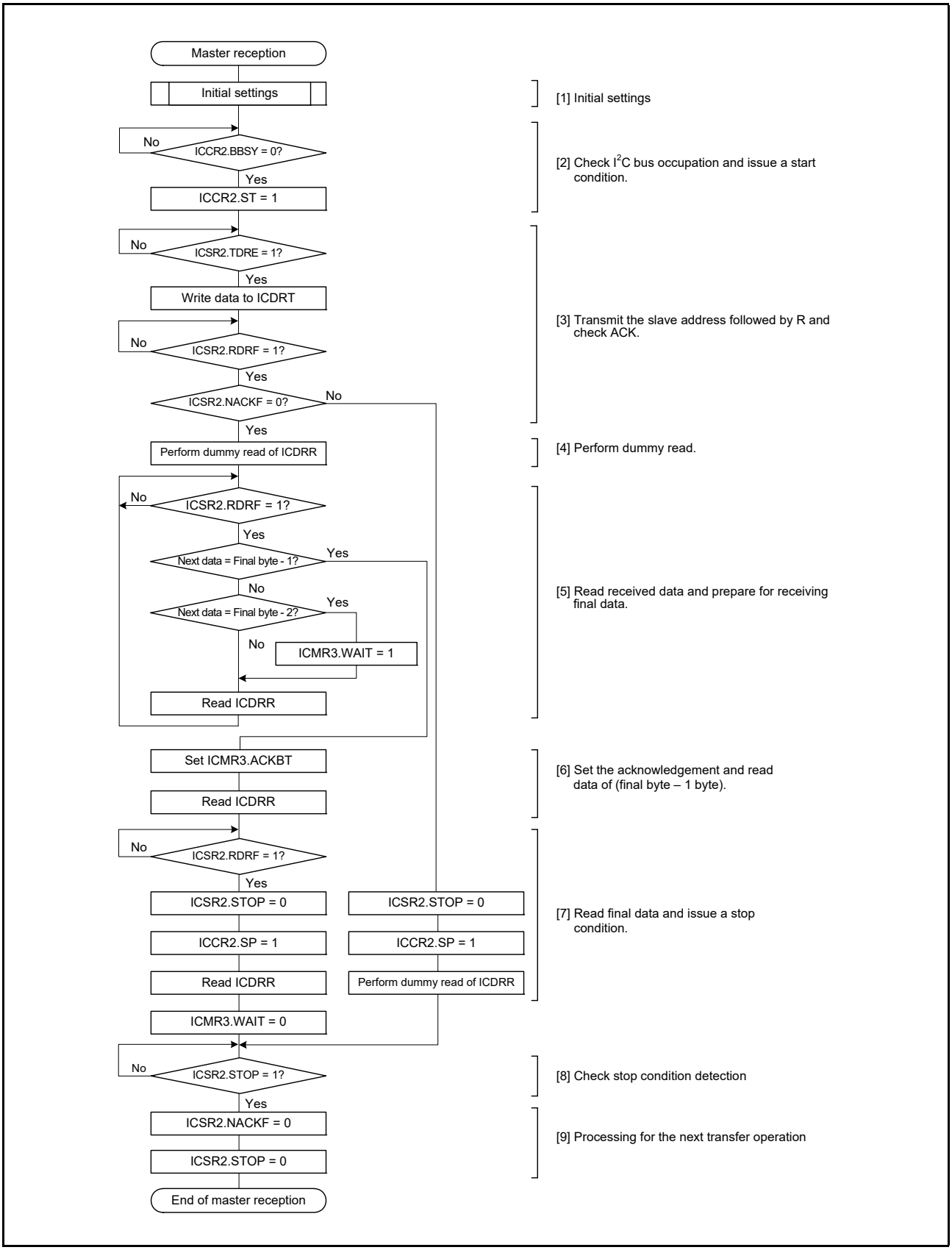


Figure 34.11 Example of Master Reception (7-Bit Address Format, 3 Bytes or More)

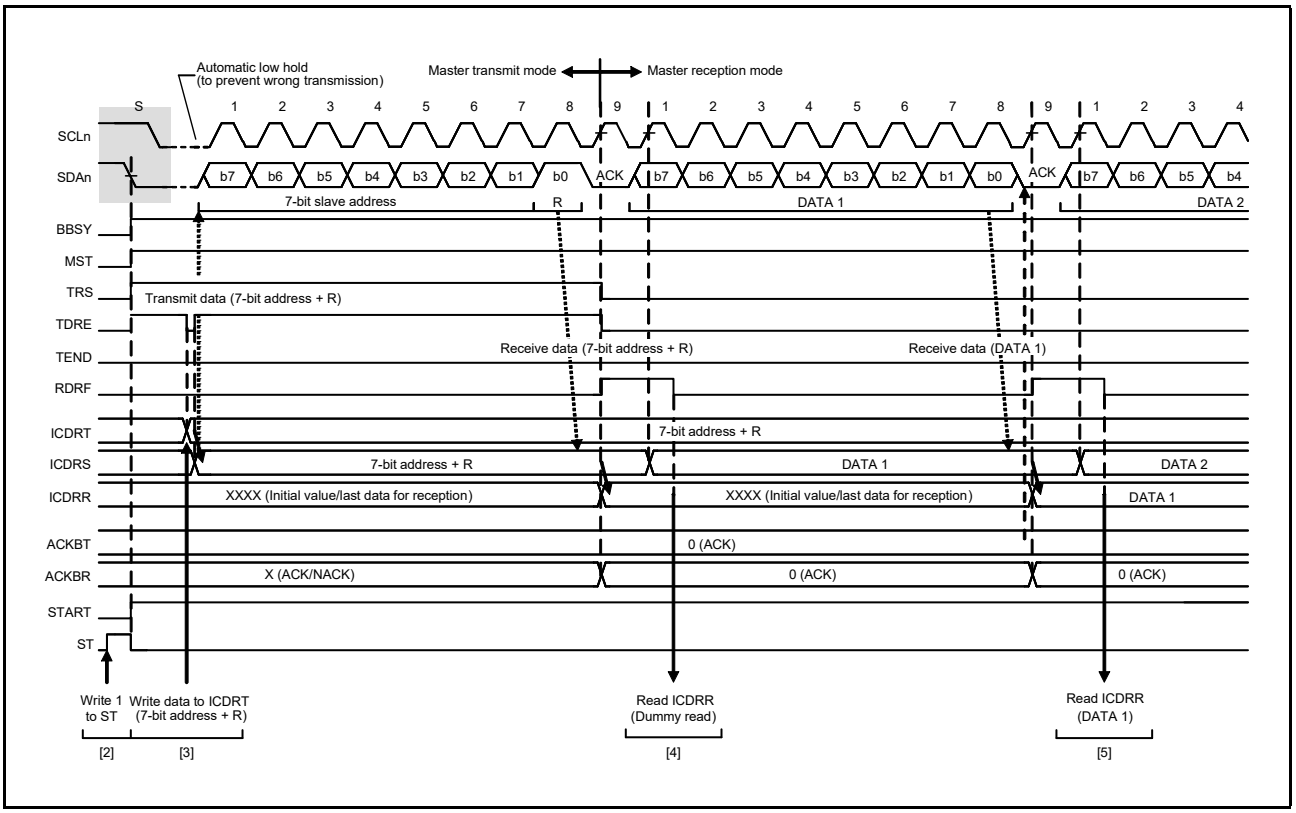


Figure 34.12 Master Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0)

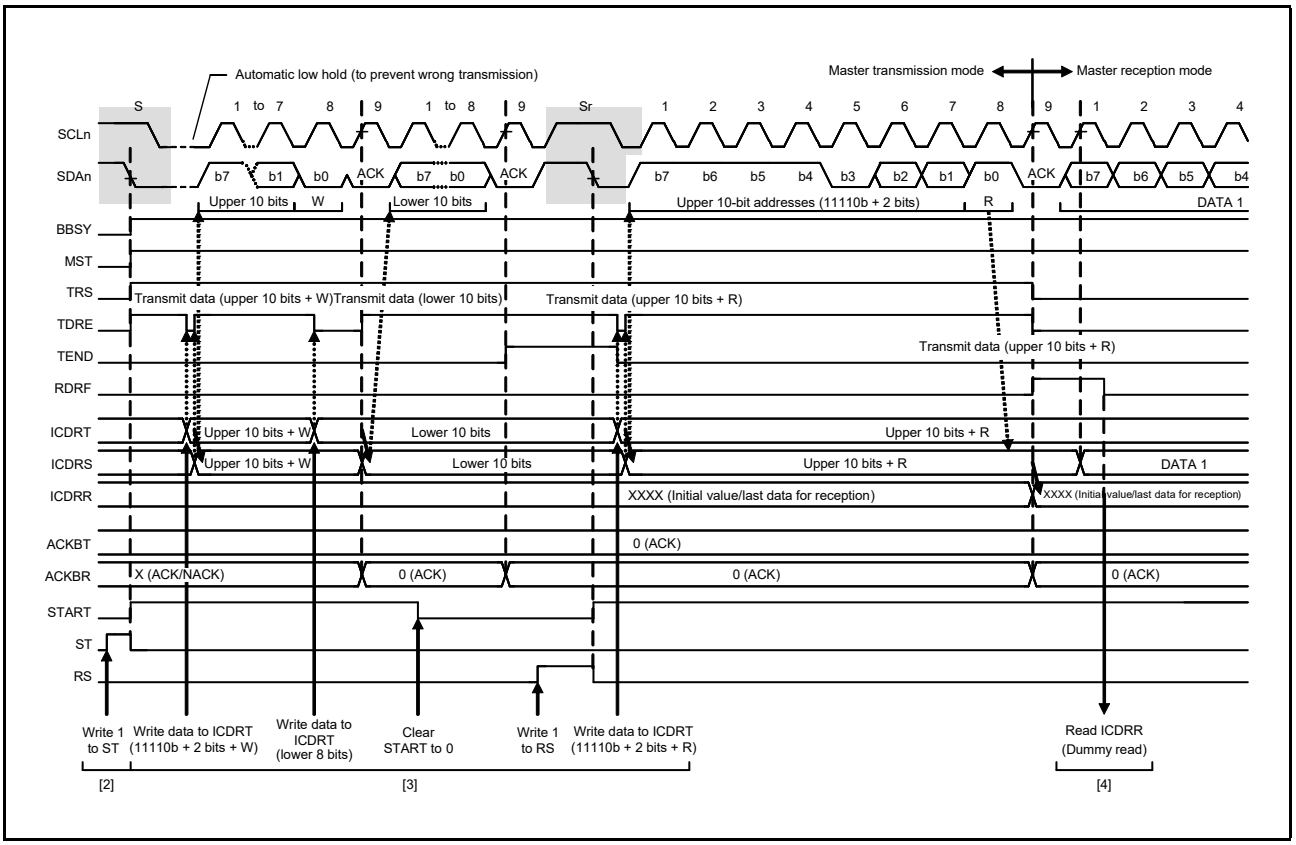


Figure 34.13 Master Receive Operation Timing (2) (10-Bit Address Format, when RDRFS = 0)

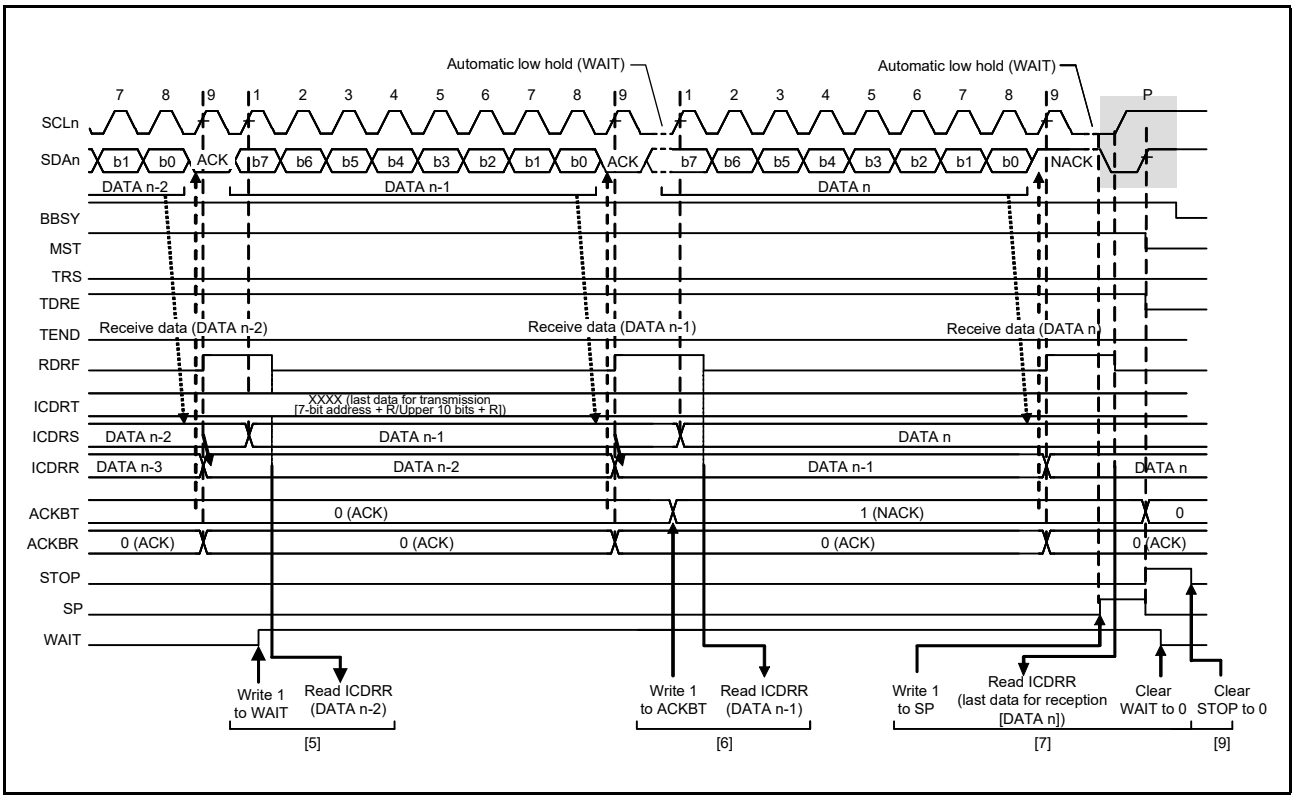


Figure 34.14 Master Receive Operation Timing (3) (when RDRFS = 0)

34.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the RIIC transmits data as a slave device, and the master device returns acknowledgements.
Figure 34.15 shows an example of usage of slave transmission and Figure 34.16 and Figure 34.17 show the timing of operations in slave transmission.
The following describes the procedure and operations for slave transmission.

(1) Initial settings. For details, refer to section 34.3.2, Initial Settings.
After initial settings, the RIIC will stay in the standby state in slave reception mode until it receives a slave address that it matches.

(2) After receiving a matching slave address, the RIIC sets the corresponding bit among ICSR1.GCA and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit as the acknowledge bit on the ninth cycle of the SCL clock.
With the 7-bit address format, if the value of the R/W# bit that was also received at this time is 1, the RIIC automatically places itself in slave transmission mode by setting both the TRS bit and the TDRE flag in ICSR2 to 1.
With the 10-bit address format, after receiving a matching slave address, check that the ICSR2.STOP flag and the ICSR2.RDRF flag are 0 and 1, respectively, and dummy-read the ICDRR register. Here, the received value that is dummy read is the lower-order 8 bits of the address. Following the dummy read, data reception is restarted on detection of a restart condition. If the value of the R/W# bit that was also received at this time is 1, the RIIC automatically places itself in slave transmission mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.

(3) After the ICSR2.TDRE flag is confirmed to be 1, write the data for transmission to the ICDRT register. At this time, if the RIIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the RIIC suspends transfer of the next data.

(4) Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the RIIC drives the SCLn line low on the ninth falling edge of SCL clock.

(5) When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.

(6) Upon detecting the stop condition, the RIIC automatically sets bits ICSR1.GCA and AASy (y = 0 to 2), flags ICSR2.TDRE and TEND, and the ICCR2.TRS bit to 0, and enters slave reception mode.

(7) After checking that the ICSR2.STOP flag is 1, set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

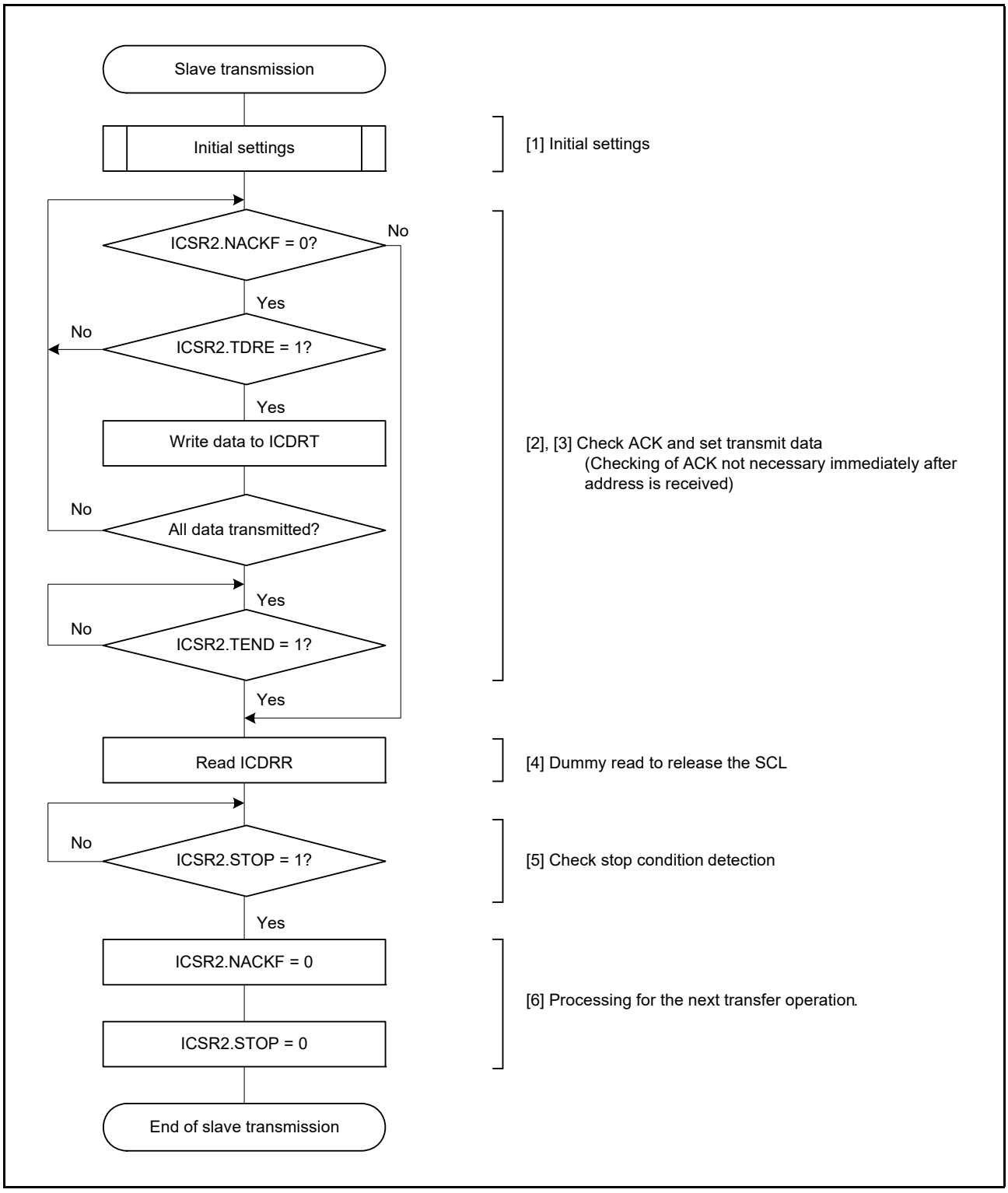


Figure 34.15 Example of Slave Transmission Flowchart

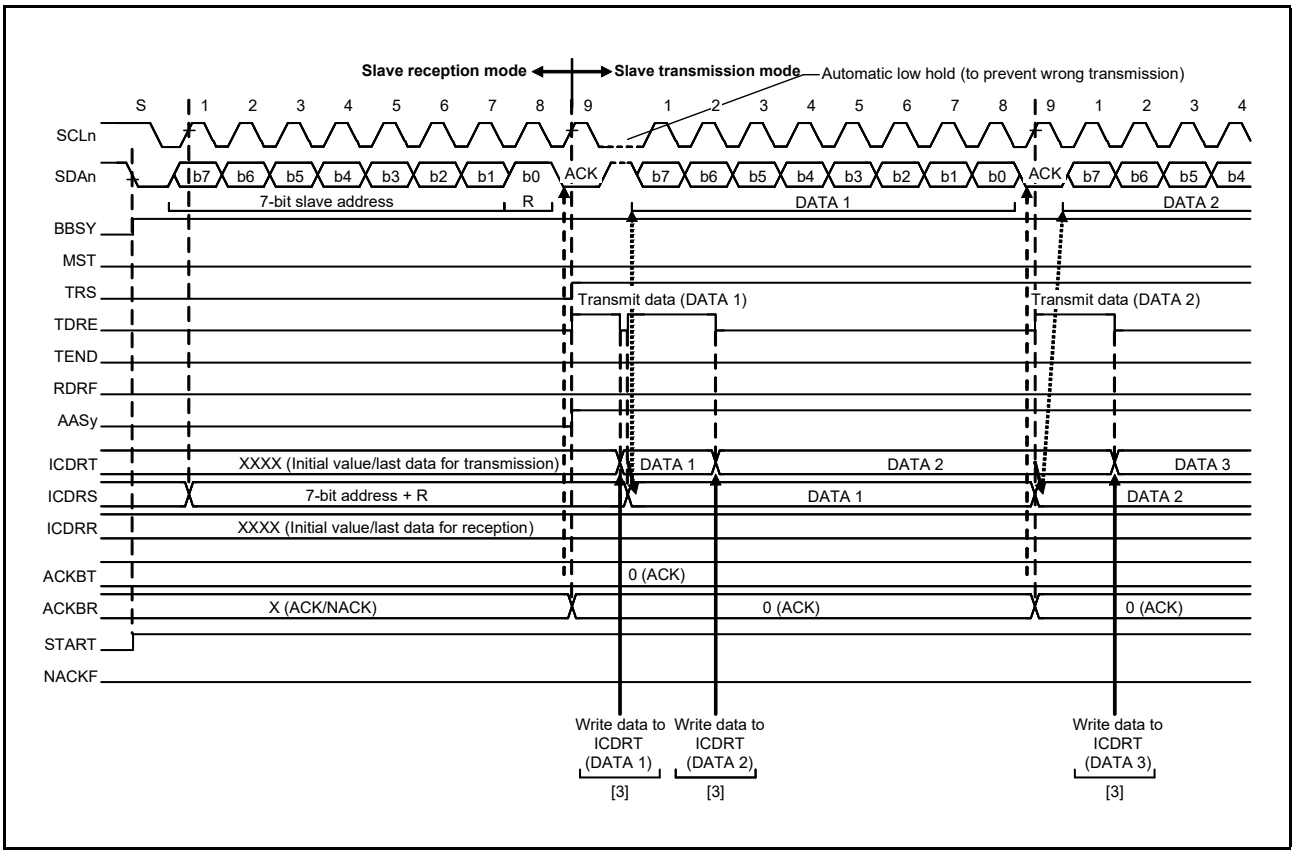


Figure 34.16 Slave Transmit Operation Timing (1) (7-Bit Address Format)

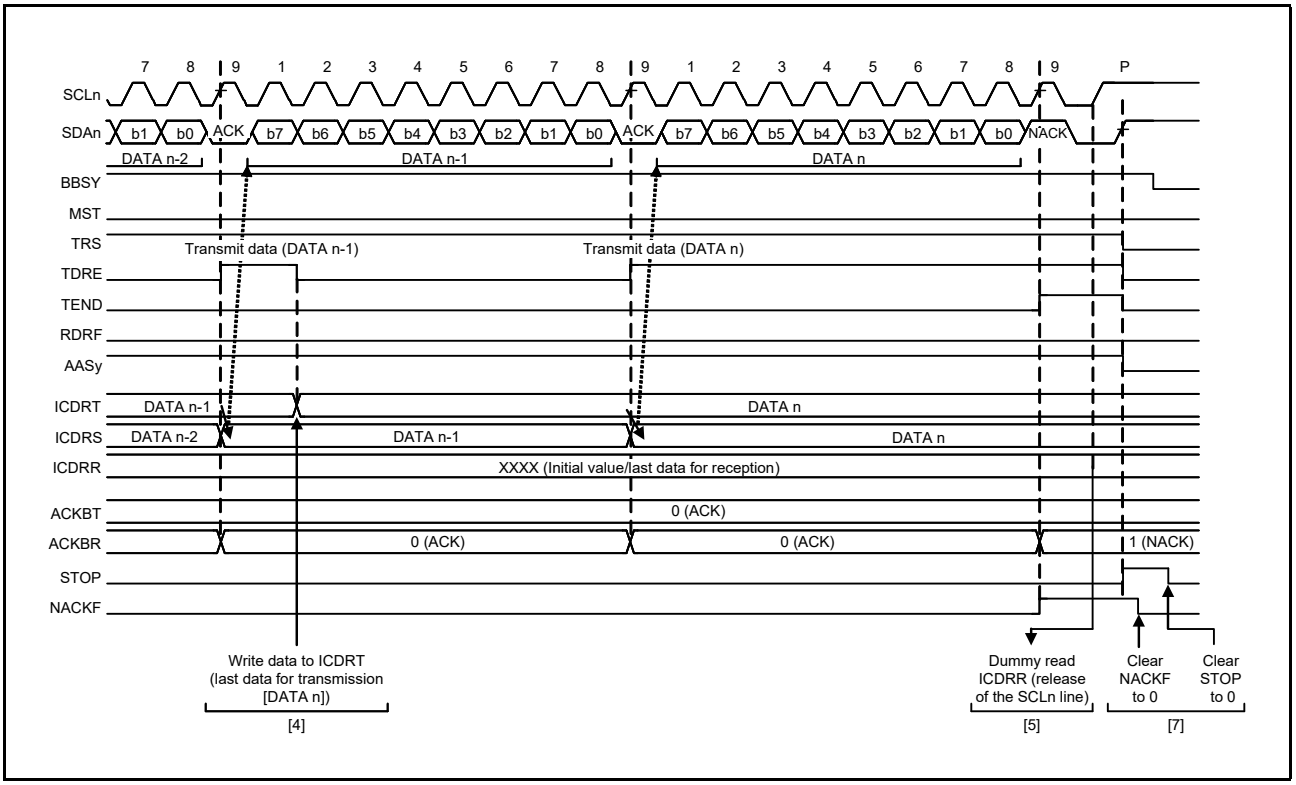


Figure 34.17 Slave Transmit Operation Timing (2)

34.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the RIIC returns acknowledgements as a slave device.

Figure 34.18 shows an example of usage of slave reception and Figure 34.19 and Figure 34.20 show the timing of operations in slave reception.

The following describes the procedure and operations for slave reception.

(1) Initial settings. For details, refer to section 34.3.2, Initial Settings.
After initial settings, the RIIC will stay in the standby state in slave reception mode until it receives a slave address that it matches.

(2) After receiving a matching slave address, the RIIC sets one of the corresponding bits ICSR1.GCA and AASy (y = 0 to 2) to 1 on the rising edge of the ninth cycle of SCL clock (the clock signal) and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of SCL clock. If the value of the R/W# bit that was also received at this time is 0, the RIIC continues to place itself in slave reception mode and sets the RDRF flag in ICSR2 to 1.

(3) After the ICSR2.STOP flag is confirmed to be 0 and the ICSR2.RDRF flag to be 1, dummy read ICDRR (the dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected). After the dummy-read, the RIIC clears the RDRF flag to 0 and starts reception of data.

(4) On completion of the reception of 1 byte of data, the value of the ICSR2.RDRF flag becomes 1 on the rising edge of the 8th or 9th clock cycle of the SCL clock, according to the setting made in the ICMR3.RDRFS bit. At this time, reading the ICDRR register returns the received value and the RDRF flag is automatically cleared to 0 in response. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the RIIC holds the SCLn line low from the falling edge of one SCL cycle before the timing with which RDRF should be set. In this case, reading ICDRR releases the SCLn line from being held at the low level.
When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.

(5) Upon detecting the stop condition, the RIIC automatically clears bits ICSR1.GCA and AASy (y = 0 to 2) to 0.

(6) After checking that the ICSR2.STOP flag is 1, set the ICSR2.STOP flag to 0 for the next transfer operation.

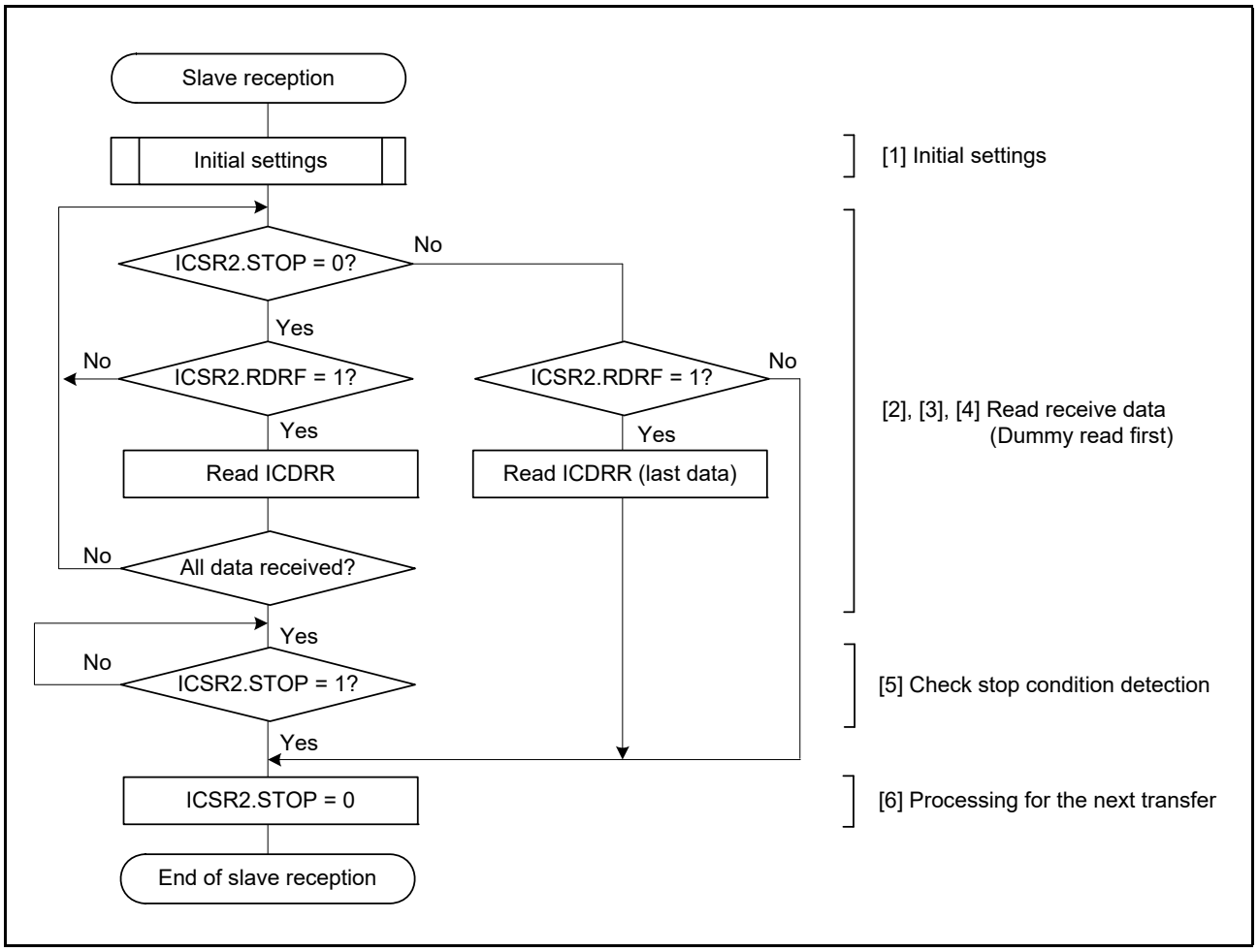


Figure 34.18 Example of Slave Reception Flowchart

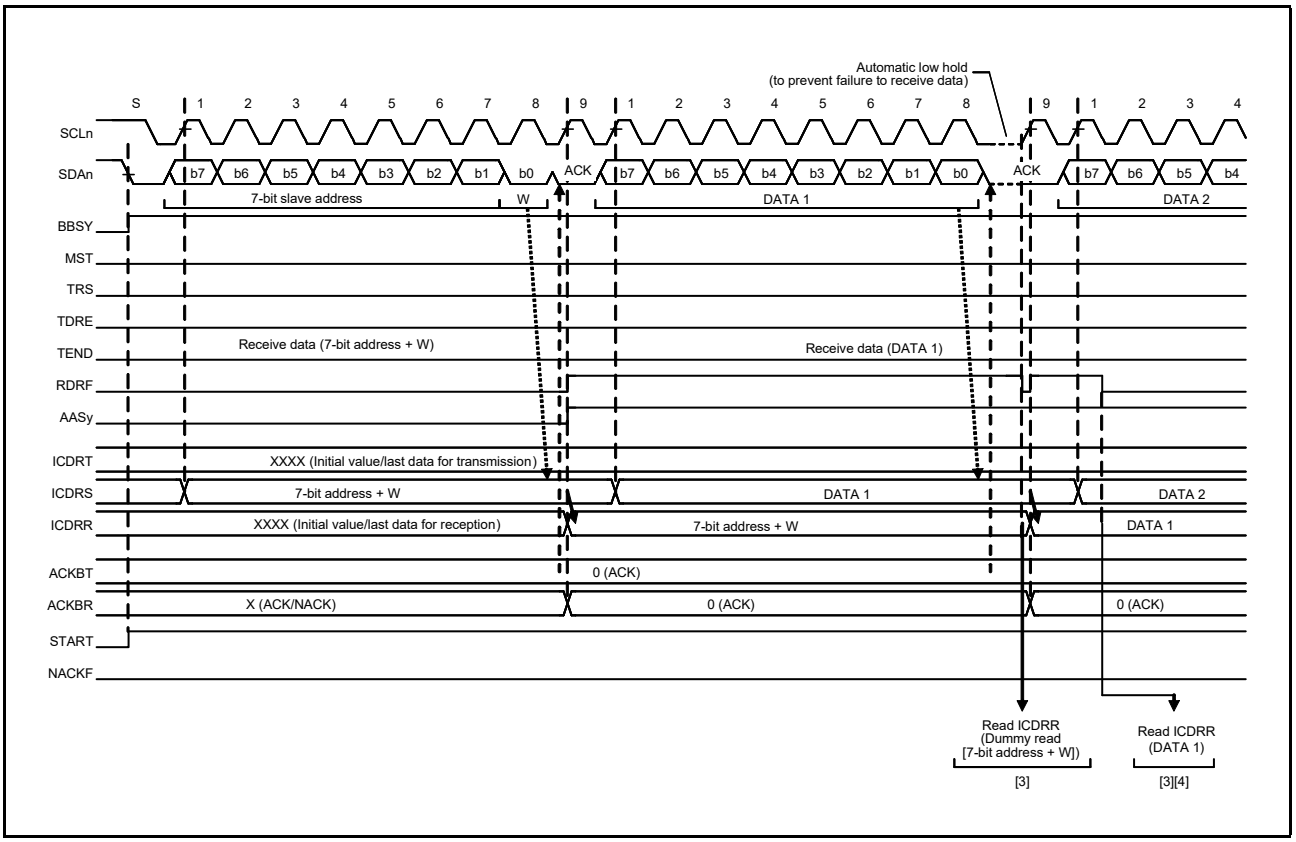


Figure 34.19 Slave Receive Operation Timing (1) (7-Bit Address Format, when RDRFS = 0)

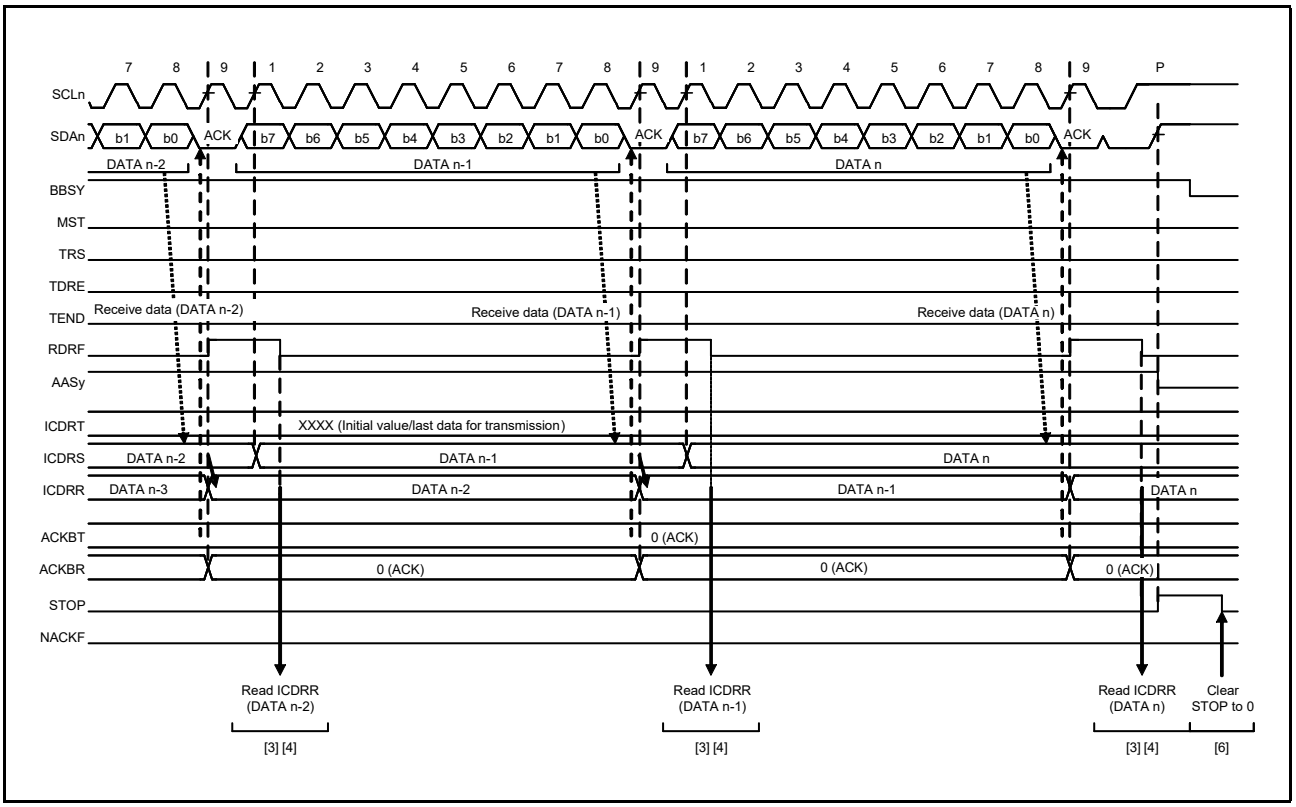


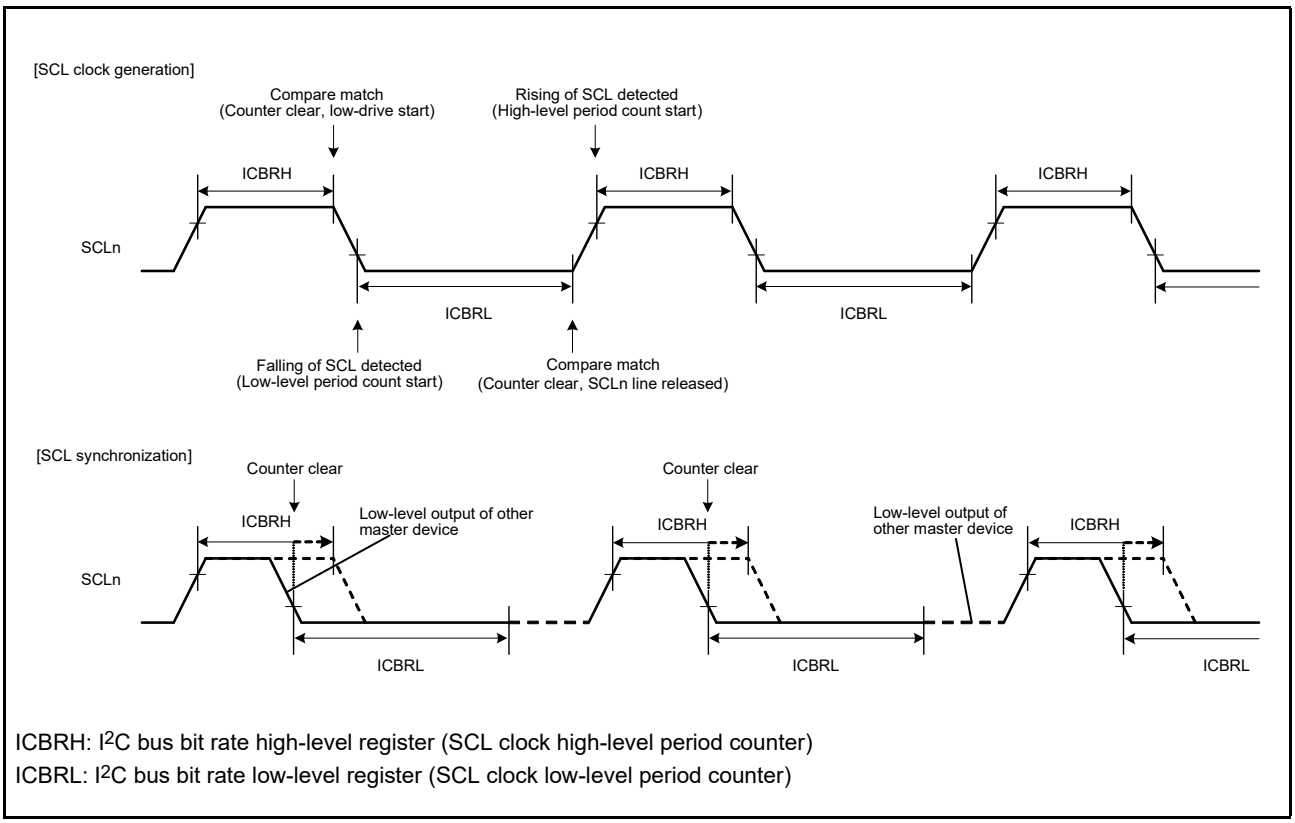
Figure 34.20 Slave Receive Operation Timing (2) (when RDRFS = 0)

34.4 SCL Synchronization Circuit

The RIIC starts counting out the value for width at high level specified in ICBRH when it detects a rising edge on the SCLn line, drives the SCLn line low once counting of the width at high level is complete, and then generates the SCL clock. When the RIIC detects the falling edge of the SCLn line, it starts counting out the width at low level period specified in ICBRL, stops driving the SCLn line (releases the line) once counting of the width at low level is complete, and then generates the SCL clock.

If multiple master devices are connected to the I²C bus, a collision of SCL signals may arise due to contention with another master device. In such cases, the master devices have to synchronize their SCL signals. Since this synchronization of SCL signals must be bit by bit, the RIIC is equipped with a facility (the SCL synchronization circuit) to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the RIIC has detected a rising edge on the SCLn line and thus started counting out the width at high level specified in ICBRH, and the level on the SCLn line falls because an SCL signal is being generated by another master device, the RIIC stops counting when it detects the falling edge, drives the level on the SCLn line low, and starts counting out the width at low level specified in ICBRL. When the RIIC finishes counting out the width at low level, it stops driving the SCLn line to the low level (i.e. releases the line). At this time, if the width at low level of the SCL clock signal from the other master device is longer than the width at low level set in the RIIC, the width at low level of the SCL signal will be extended. Once the width at low level for the other master device has ended, the SCL signal rises because the SCLn line has been released. When the RIIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, in cases of contention of SCL signals from more than one master, the width at high level of the SCL signal is synchronized with that of the clock having the narrower width, and the width at low level of the SCL signal is synchronized with that of the clock having the broader width. However, such synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.



ICBRH: I²C bus bit rate high-level register (SCL clock high-level period counter)
ICBRL: I²C bus bit rate low-level register (SCL clock low-level period counter)

Figure 34.21 Generation and Synchronization of the SCL Signal from the RIIC

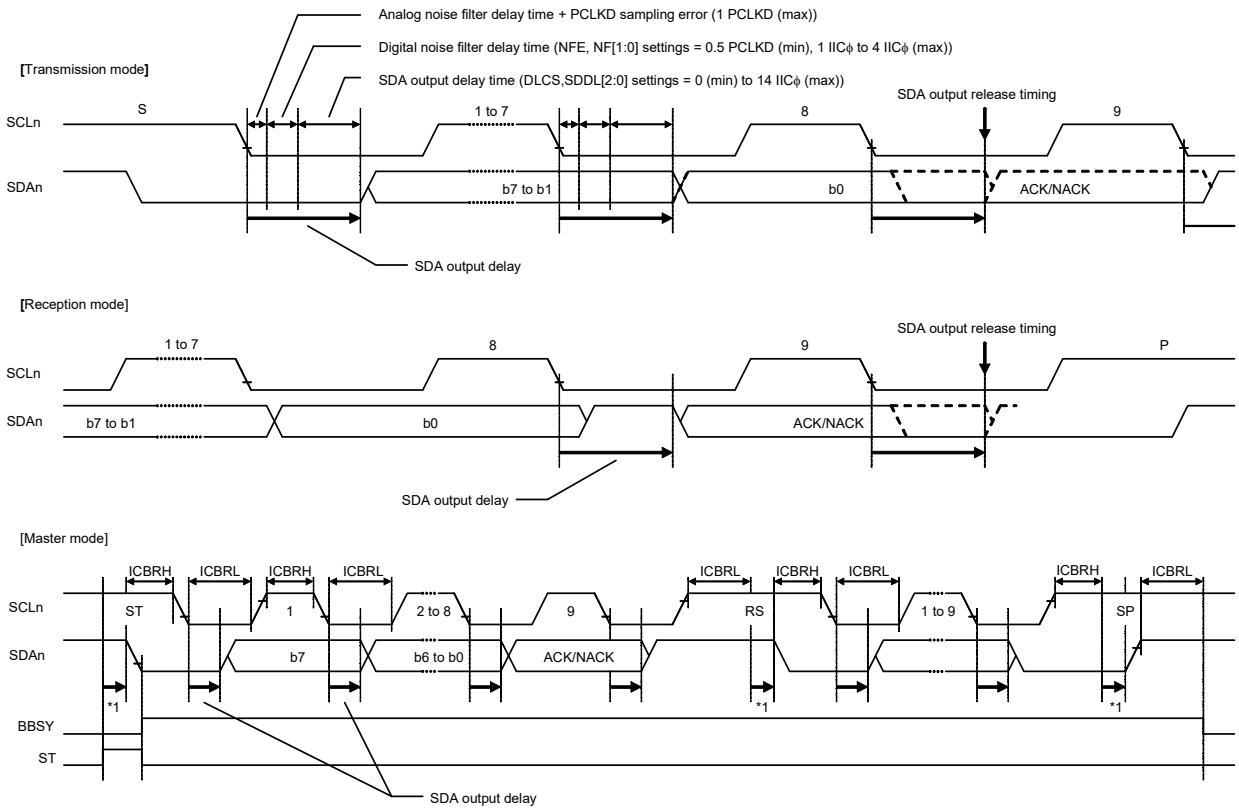
34.5 Facility for Delaying SDA Output

The RIIC module incorporates a facility for delaying output on the SDA line. The delay can be applied to all output (issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals) on the SDA line.

With the SDA output delay facility, SDA output is delayed from detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval over which the SCL clock is at the low level. Doing this leads to usage with the aim of preventing erroneous operation of communications devices.

The output delay facility is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay facility is enabled (i.e. while the SDDL[2:0] bits in ICMR2 are set to any value other than 000b), the DLCS bit in ICMR2 selects the clock source for counting by the SDA output delay counter as the internal base clock (IICϕ) for the RIIC module or as a clock signal derived by dividing the frequency of the internal base clock by 2 (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. After counting of the set number of cycles of delay is completed, the RIIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note 1. The output delay facility is set by the DLCS, and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

Figure 34.22 SDA Output Delay Facility

34.6 Digital Noise-Filter Circuits

The states of the SCLn and SDAn pins are conveyed to the internal circuitry through analog noise-filter and digital noise-filter circuits. Figure 34.23 is a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the RIIC consists of four flip-flop circuit stages connected in series and a match-detection circuit.

The number of effective stages in the digital noise filter is selected by the NF[1:0] bits in ICMR3. The selected number of effective stages determines the noise-filtering capability as a period from one to four IICϕ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal level matches the output level of the number of effective flip-flop circuit stages as selected by the NF[1:0] bits in ICMR3, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is retained.

If the ratio between the frequency of the internal operating clock (PCLKD) and the transfer rate is small (e.g. data transfer at 400 Kbps with PCLKD = 4 MHz), the characteristics of the digital noise filter may lead to the elimination of needed signals as noise. In such cases, it is possible to disable the digital noise-filter circuit (by setting the ICFER.NFE bit to 0) and use only the analog noise-filter circuit.

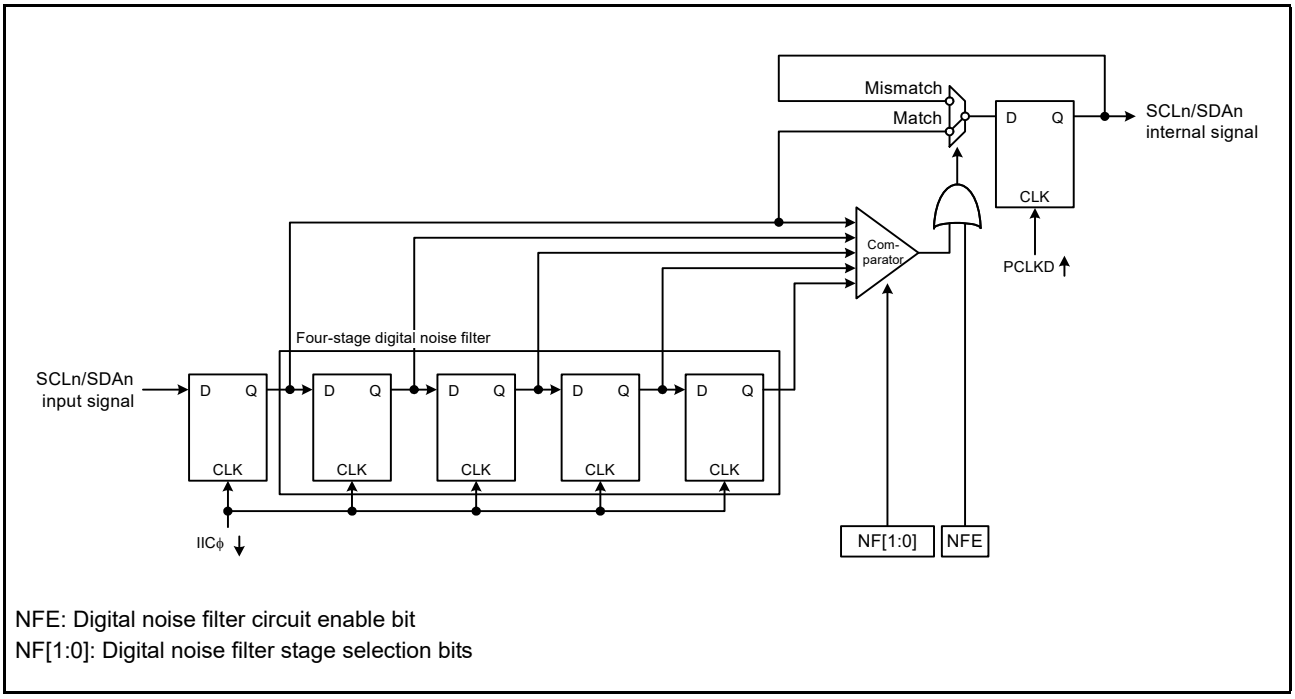


Figure 34.23 Block Diagram of Digital Noise Filter Circuit

34.7 Address Match Detection

The RIIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7-bit or 10-bit slave addresses.

34.7.1 Slave-Address Match Detection

The RIIC can set three unique slave addresses, and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in ICSARUy and ICSARLy (y = 0 to 2) can be detected.

When the RIIC detects a match of the set slave address, the corresponding AASy flag (y = 0 to 2) in ICSR1 is set to 1 at the rising edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the following R/W# bit. This causes a receive data full interrupt (RXI) or transmit data empty interrupt (TXI) to be generated. The AASy flag is used to identify which slave address has been specified.

Figure 34.24 to Figure 34.26 show the AASy flag set timing in three cases.

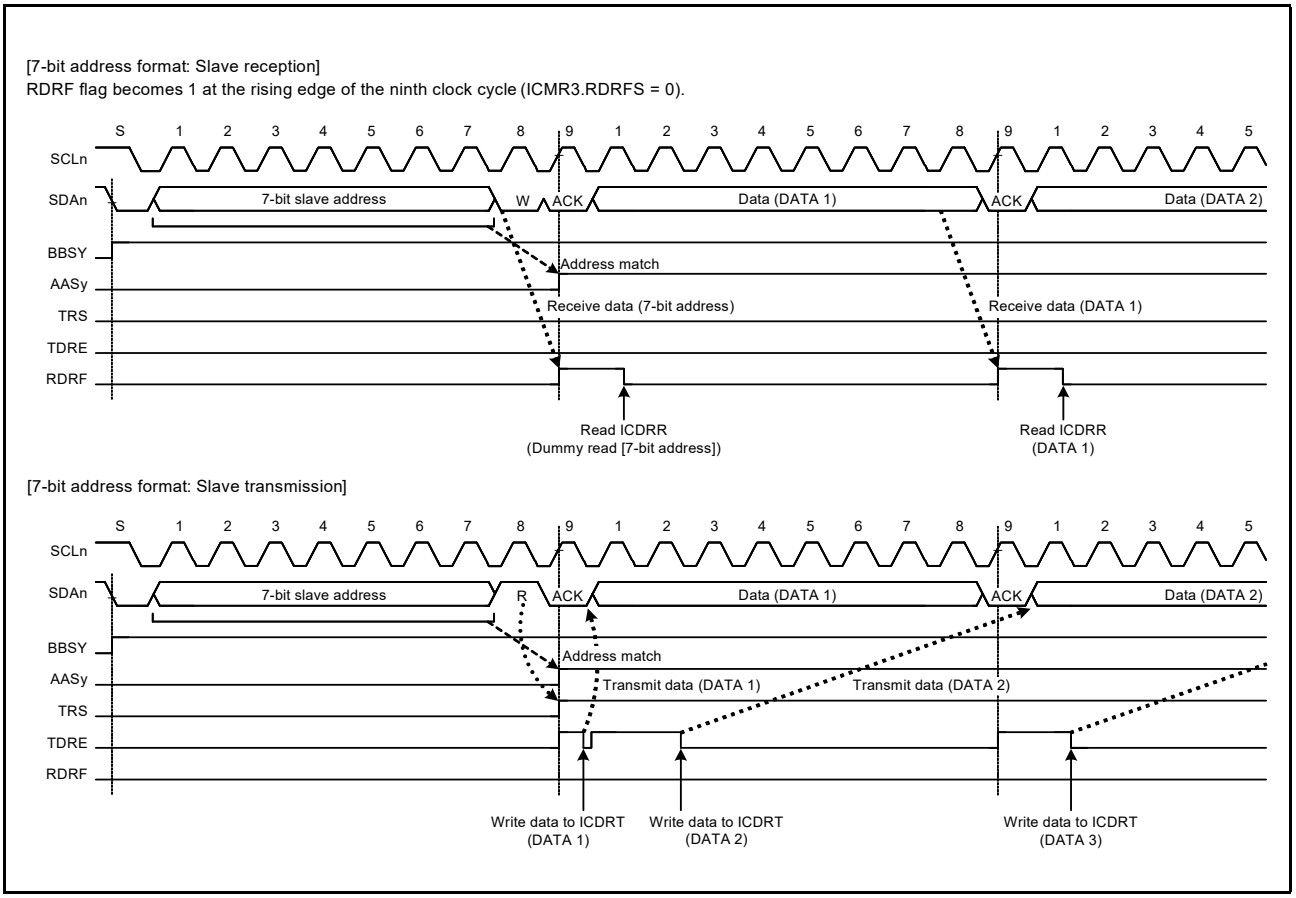


Figure 34.24 AASy Flag Set Timing with 7-Bit Address Format Selected

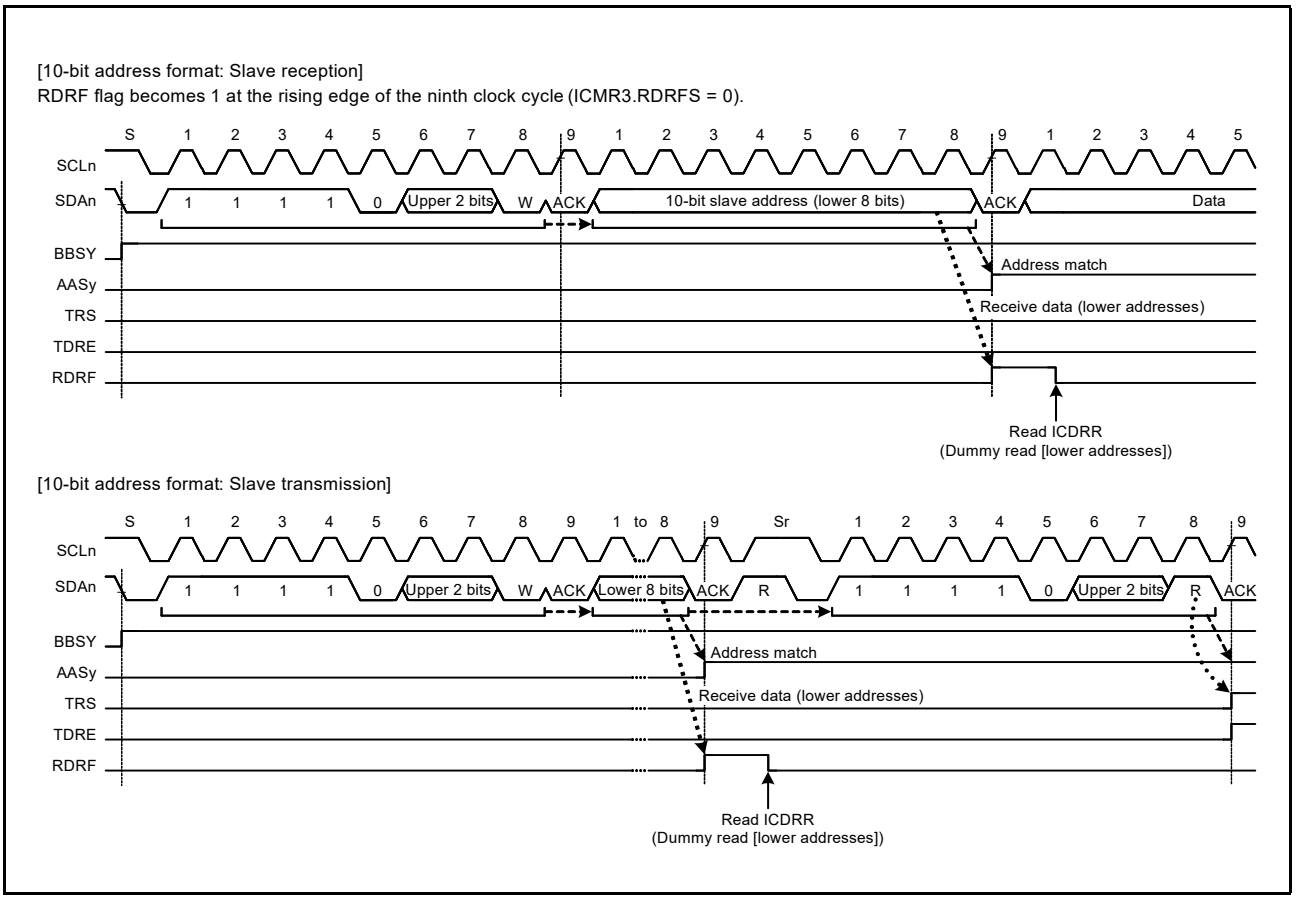


Figure 34.25 AASy Flag Set Timing with 10-Bit Address Format Selected

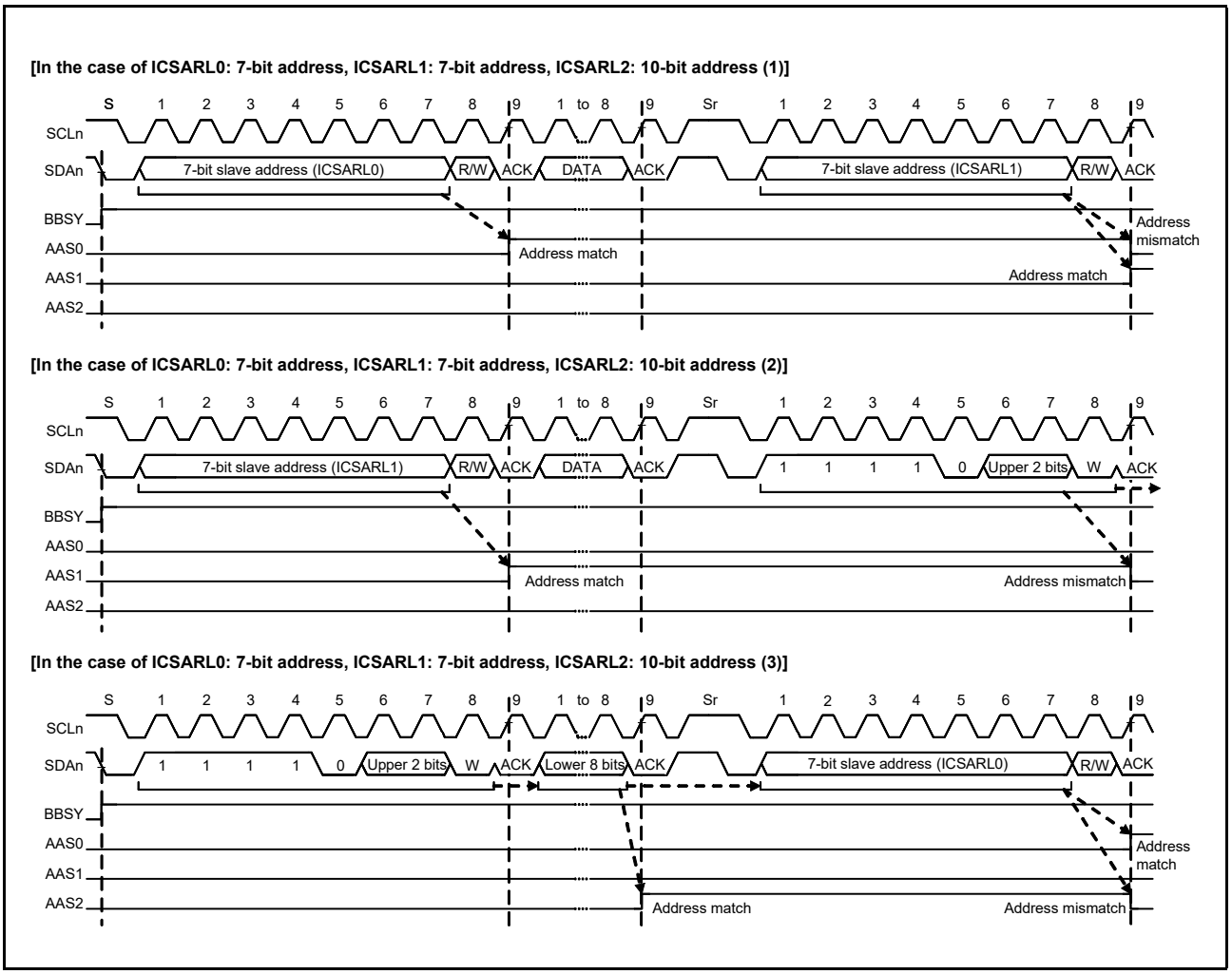


Figure 34.26 AASy Flag Set/Clear Timing with 7-Bit/10-Bit Address Formats Mixed

34.7.2 Detection of the General Call Address

The RIIC has a facility for detecting the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the RIIC recognizes this as the address of a slave device with an “all-zero” address but not as the general call address.

When the RIIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 are set to 1 on the rising edge of the ninth cycle of SCL clock. This leads to the generation of a receive data full interrupt (RXI). The value of the GCA flag can be confirmed to recognize that the general call address has been transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

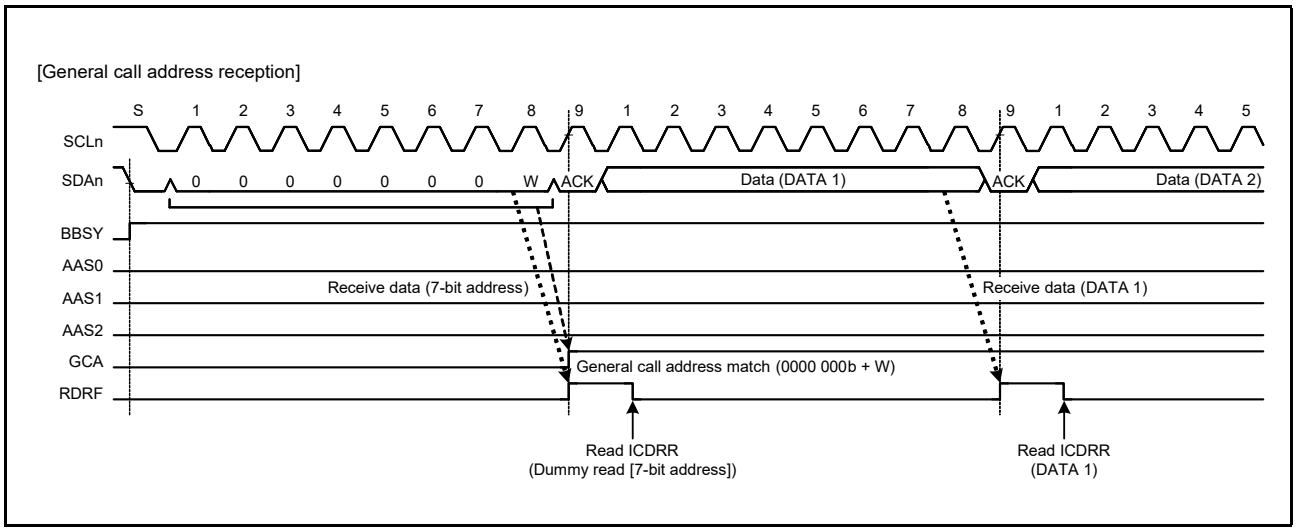


Figure 34.27 Timing of GCA Flag Setting during Reception of General Call Address

34.7.3 Device-ID Address Detection

The RIIC module has a facility for detecting device-ID addresses conforming with the I2C bus specification (Rev. 03). When the RIIC receives 1111 100b as the first byte after a start condition or restart condition was issued with the DIDE bit in ICSER set to 1, the RIIC recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the eighth SCL clock cycle when the following R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the RIIC sets the corresponding AASy flag (y = 0 to 2) in ICSR1 to 1.

After that, when the first byte received after a start or restart condition is issued matches the device ID address (1111 100b) again and the following R/W# bit is 1, the RIIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device-ID address detection function, the RIIC sets the DID flag to 0 if a match with the RIIC's own slave address is not obtained or a match with the device ID address is not obtained after a match with the RIIC's own slave address and the detection of a restart condition. In this case, if the first byte after detection of a start or restart condition matches the device ID address (1111 100b) and the R/W# bit is 0, the RIIC sets the DID flag to 1 and compares the second and subsequent bytes with the RIIC's slave address. If the R/W# bit is 1, the DID flag holds the previous value and the RIIC does not compare the second and subsequent bytes. Therefore, the reception of a device-ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Furthermore, prepare the device-ID fields (three bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal data for transmission. For details of the information that must be included in device-ID fields, contact NXP Semiconductors.

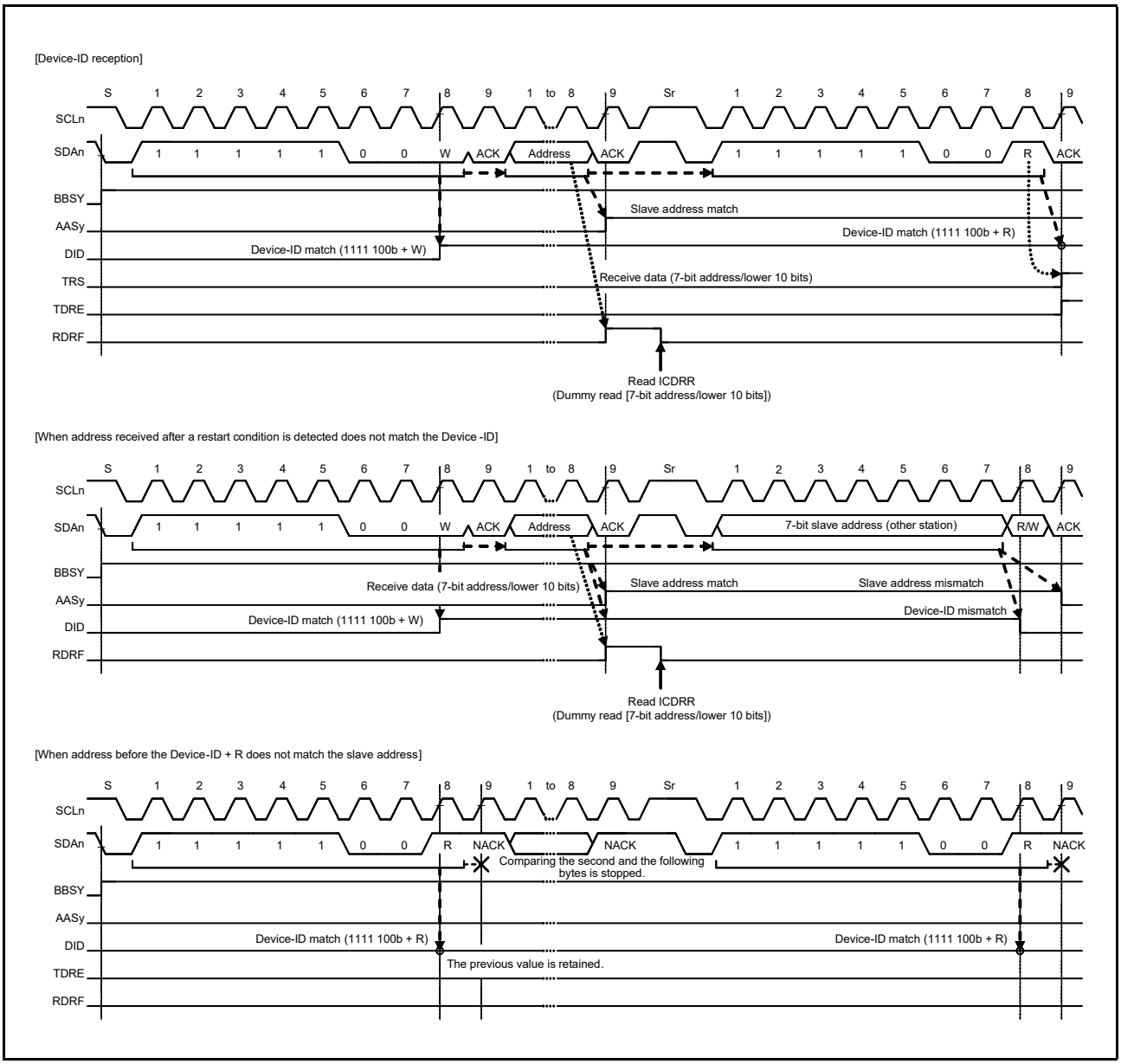


Figure 34.28 AASy/DID Flag Set/Clear Timing during Reception of Device-ID

34.8 Automatic Low-Hold Function for SCL

34.8.1 Function to Prevent Wrong Transmission of Transmit Data

If the shift register (ICDRS) is empty when data have not been written to the I2C bus transmit data register (ICDRT) with the RIIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn line is automatically held at the low level over the intervals shown below. This low-hold period is extended until data for transmission have been written, which prevents the unintended transmission of erroneous data.

Master transmission mode

- Low-level interval after a start condition or restart condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

Slave transmission mode

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next

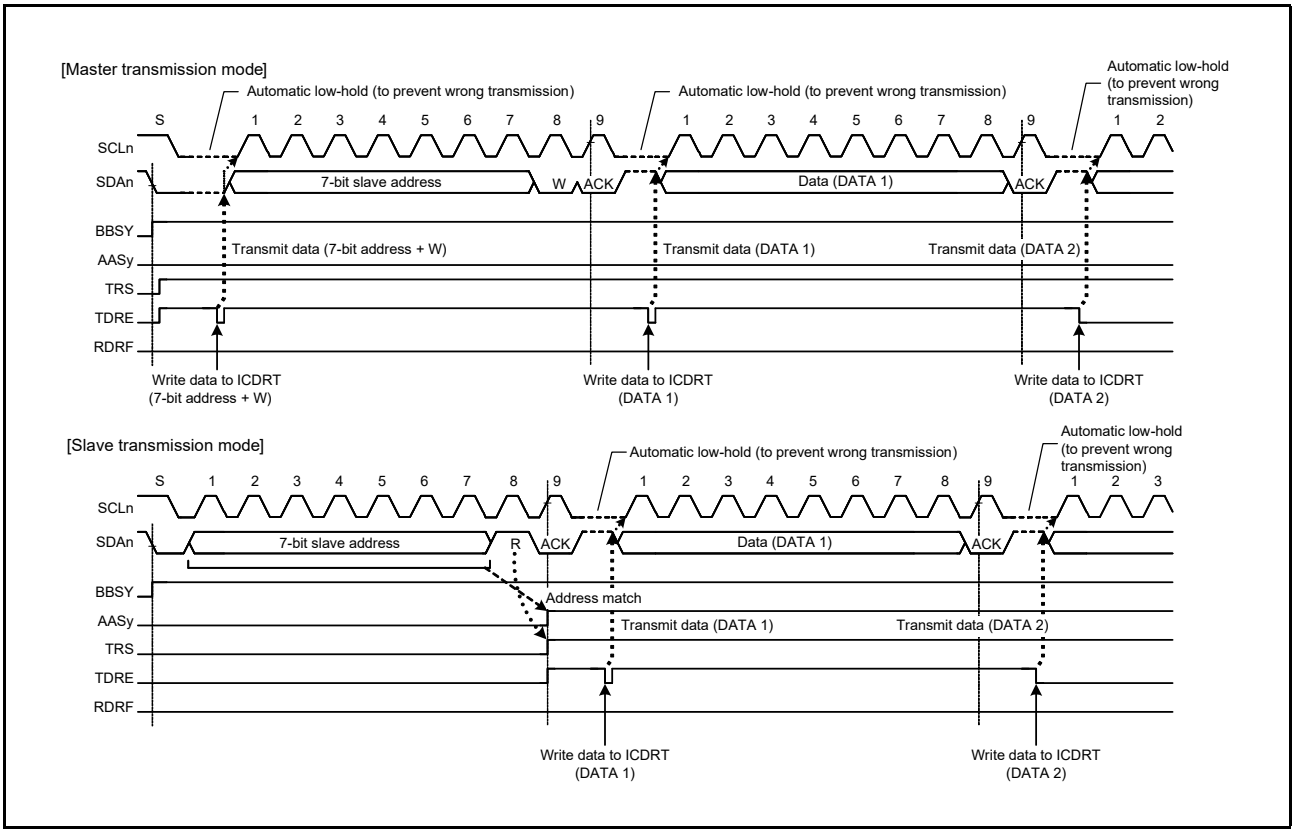


Figure 34.29 Automatic Low-Hold Operation in Transmission Mode

34.8.2 NACK Reception Transfer Suspension Function

The RIIC has a function to suspend transfer operation when NACK is received in transmission mode (TRS bit = 1 in ICCR2). This function is enabled when the NACKE bit in ICFER is set to 1 (transfer suspension enabled). If the next transmit data has already been written (TDRE flag = 0 in ICSR2) when NACK is received, next data transmission at the falling edge of the ninth SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit operation and receive operation are discontinued. To restore transmit/receive operation, be sure to set the NACKF flag to 0. In master transmission mode, set the NACKF flag to 0, issue a restart or stop condition, and then issue a start condition again.

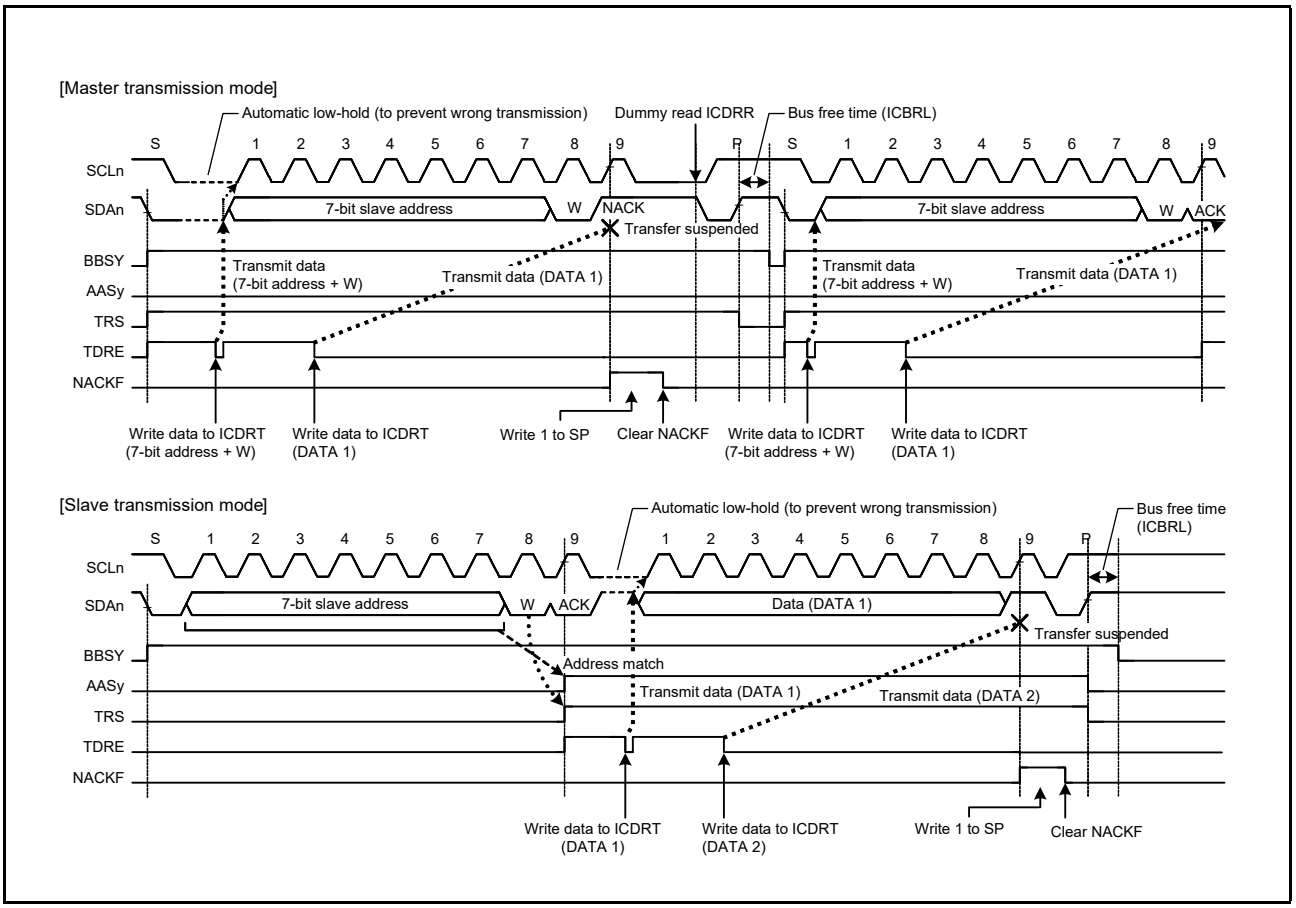


Figure 34.30 Suspension of Data Transfer When NACK is Received (NACKE = 1)

34.8.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in reception mode (TRS = 0 in ICCR2), the RIIC holds the SCLn line low automatically immediately before the next data is received to prevent failure to receive data.
This function to prevent failure to receive data using the automatic low-hold function is also enabled even if the read processing of the final receive data is delayed and, in the meantime, the RIIC's own slave address is designated after a stop condition is issued. This function does not disturb other communication because the RIIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.
Sections in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-Byte Receive Operation and Automatic Low-Hold Function Using the WAIT Bit

When the WAIT bit in ICMR3 is set to 1, the RIIC performs 1-byte receive operation using the WAIT bit function. When the ICMR3.RDRFS bit is 0, the ACKBT bit value in ICMR3 is automatically sent to the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle. When the falling edge of the ninth SCL clock cycle is detected, the SCLn line is automatically held low by the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables bytewise receive operation.
The WAIT bit function is enabled for receive frames after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master reception mode or slave reception mode.

(2) 1-Byte Receive Operation (ACK/NACK Transmission Control) and Automatic Low-Hold Function Using the RDRFS Bit

When the RDRFS bit in ICMR3 is set to 1, the RIIC performs 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag (receive data full) in ICSR2 is set to 1 at the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low at the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation by the ACK/NACK transmission control according to the data received in byte units.
The RDRFS bit function is enabled for receive frames after a match with the RIIC's own slave address (including the general call address and host address) is obtained in master reception mode or slave reception mode.

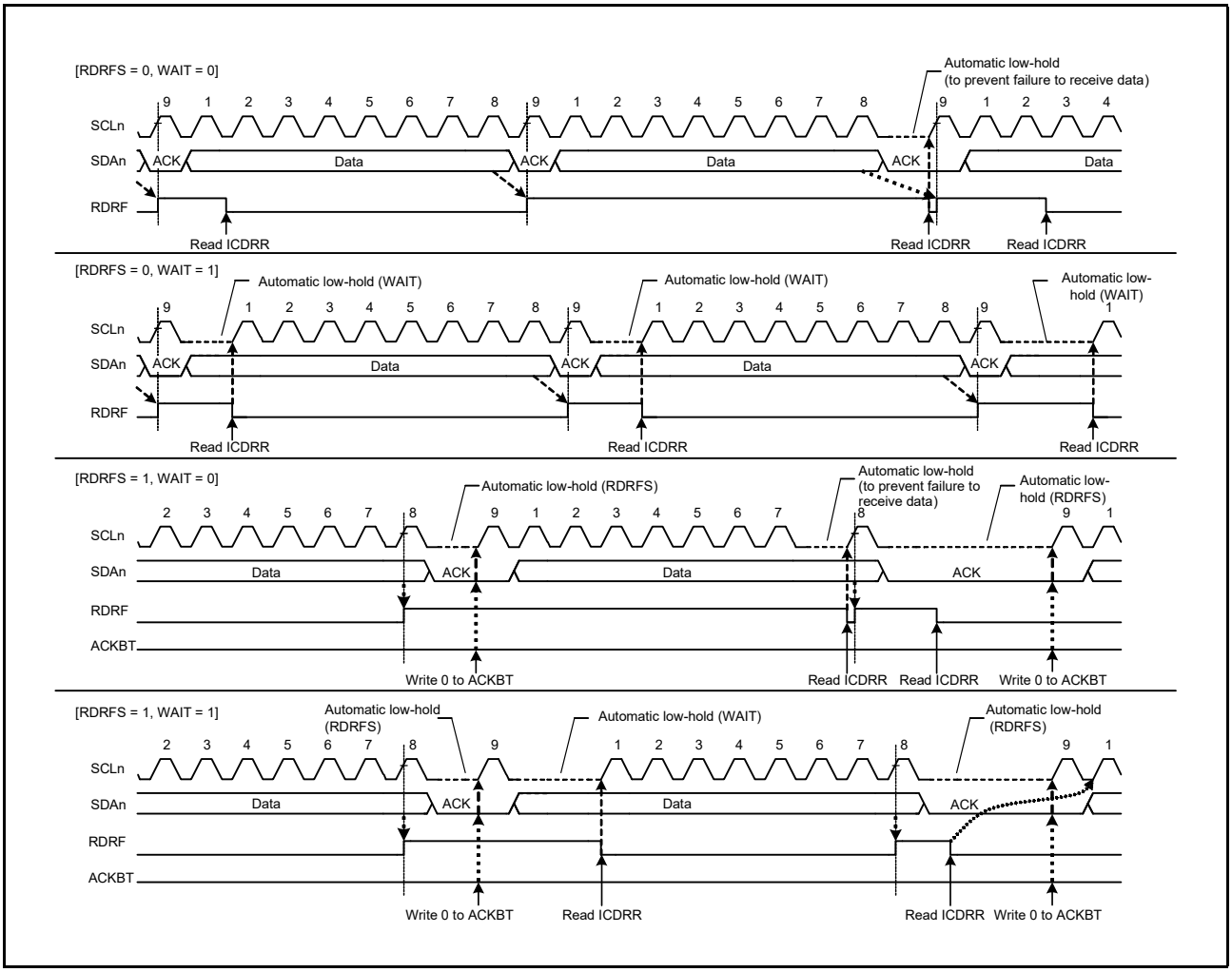


Figure 34.31 Automatic Low-Hold Operation in Reception Mode (Using RDRFS and WAIT Bits)

34.9 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the RIIC has functions to prevent double-issue of a start condition, to detect arbitration-lost during transmission of NACK, and to detect arbitration-lost in slave transmission mode.

34.9.1 Master Arbitration-Lost Detection (MALE Bit)

The RIIC drives the SDAn line low to issue a start condition. However, if the SDAn line has already been driven low by another master device issuing a start condition, the RIIC regards its own issuing of a start condition as an error and considers this a loss in arbitration, so priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the RIIC regards this as a double-issuing-of-start-condition error and considers itself to have lost in arbitration, thus preventing a failure of transfer due to issuing of a start condition while transfer is in progress.
When a start condition is issued successfully, the data for transmission including the address bits (i.e. the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state, and the low level is detected on the SDAn line), the RIIC loses in arbitration.
After a loss in arbitration of mastership, the RIIC immediately enters slave reception mode. If a slave address (including the general call address) matches its own address at this time, the RIIC continues in slave operation.
A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).
[Master arbitration-lost conditions]

- Non-matching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the BBSY flag in ICCR2 was set to 0 (erroneous issuing of a start condition)
- Setting of the ST bit in ICCR2 to 1 (start condition double-issue error) while the BBSY flag in ICCR2 is set to 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmission mode (MST and TRS bits = 11b in ICCR2)

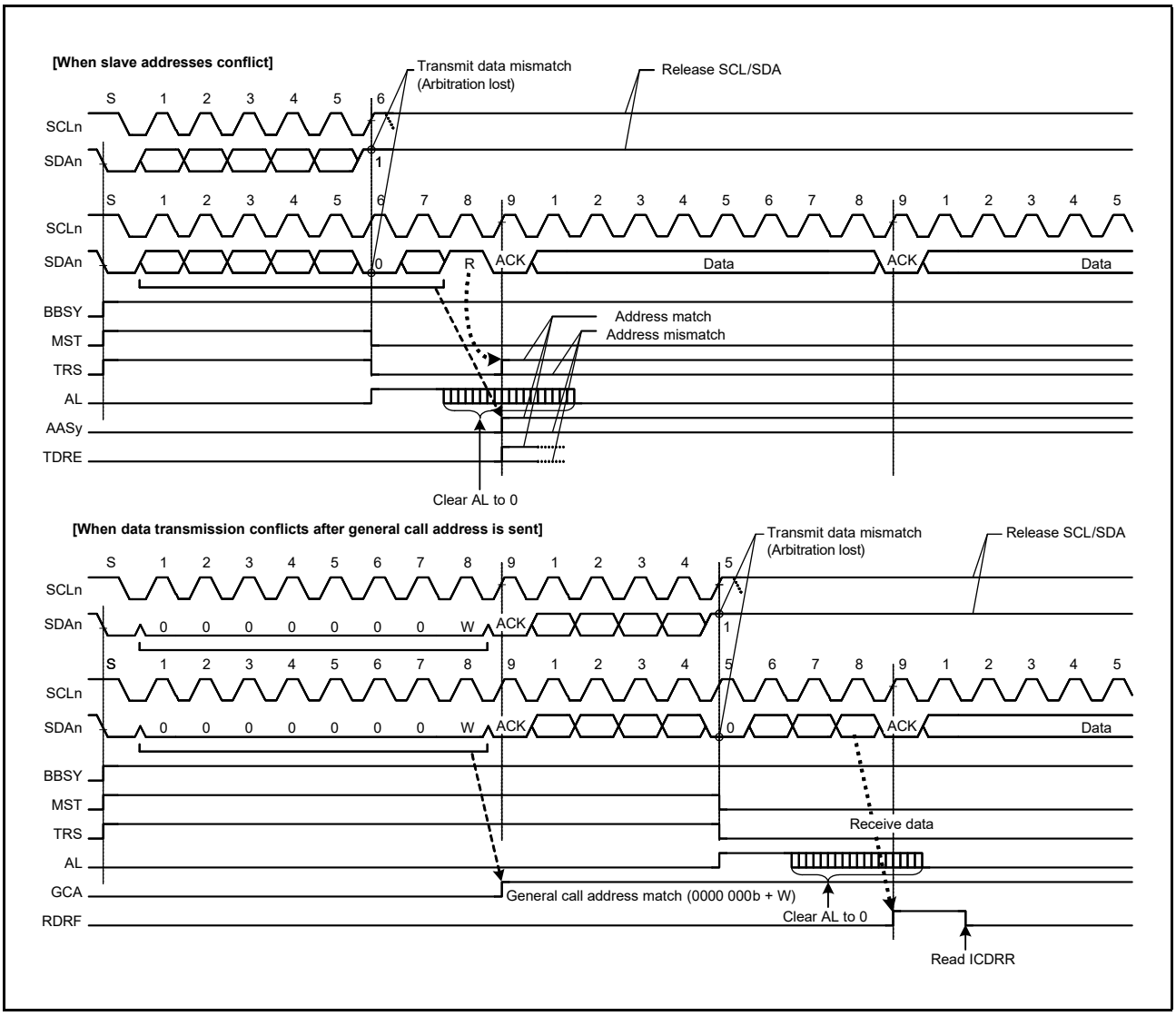


Figure 34.32 Examples of Master Arbitration-Lost Detection (MALE = 1)

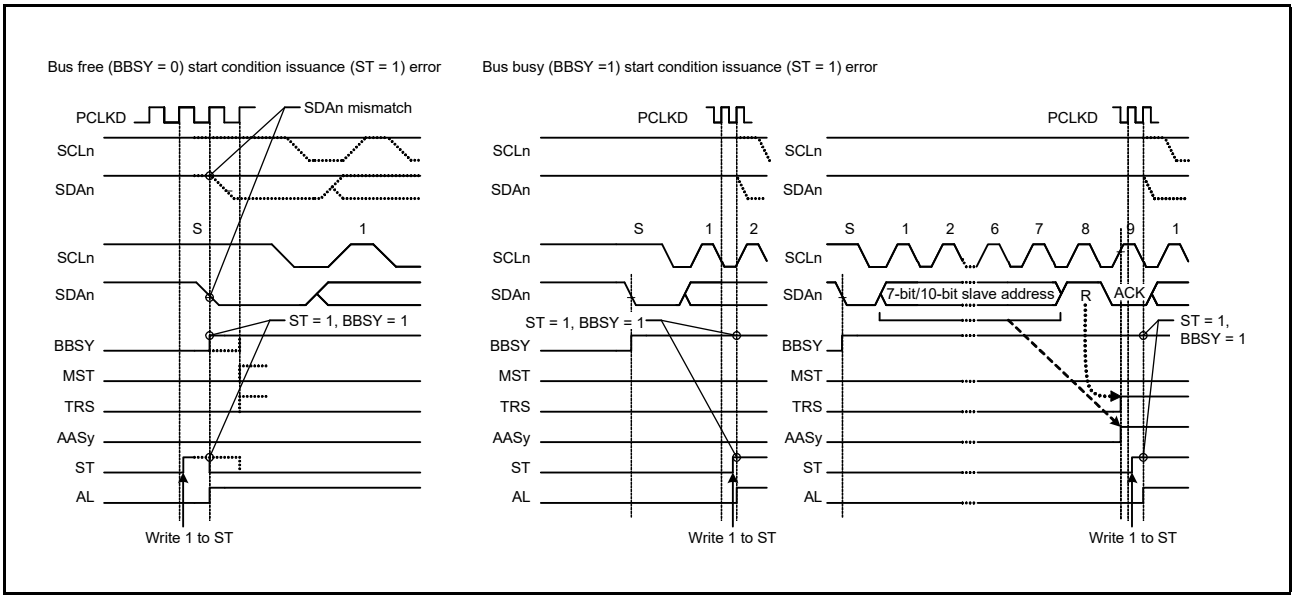


Figure 34.33 Arbitration-Lost When a Start Condition is Issued (MALE = 1)

34.9.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

The RIIC has a function to cause arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state, and the low level is detected on the SDAn line) during transmission of NACK in reception mode. Arbitration is lost due to a conflict of NACK transmission and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send/receive the same information through a single slave device. Figure 34.34 shows an example of arbitration-lost detection during transmission of NACK.

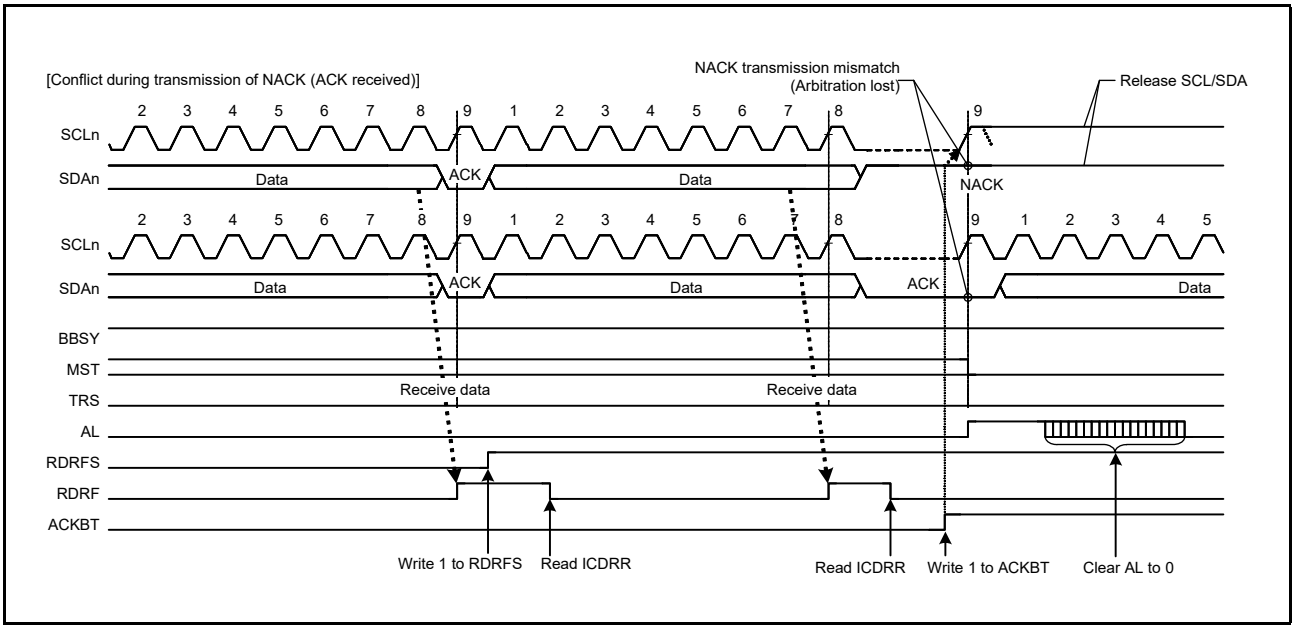


Figure 34.34 Example of Arbitration-Lost Detection during Transmission of NACK (NALE = 1)

The following explains arbitration-lost detection using an example where two master devices (master A and master B) and a single slave device are connected through the bus. In this example, master A receives two bytes of data from the slave device, and master B receives four bytes of data from the slave device.

If master A and master B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in both master A and master B during access to the slave device. Therefore, both master A and master B recognize that they have obtained the bus mastership and operate as such. Here, master A sends NACK when it has received two final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received necessary four bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect ACK transmitted by master B and issues a stop condition. Therefore, the issuance of the stop condition conflicts with the SCL clock output of master B, which disturbs communication.

When the RIIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost.

If arbitration is lost during transmission of NACK, the RIIC immediately cancels the slave match condition and enters slave reception mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

The RIIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3)

34.9.3 Slave Arbitration-Lost Detection (SALE Bit)

The RIIC has a function to cause arbitration to be lost if the data for transmission (i.e. the internal SDA output level) and the level on the SDAn line do not match (the high output as the internal SDA output; i.e. the SDAn pin is in the high-impedance state, and the low level is detected on the SDAn line) in slave transmission mode.
When it loses slave arbitration, the RIIC is immediately released from the slave-matched state and enters slave reception mode.
The RIIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmission mode (MST and TRS bits = 01b in ICCR2)

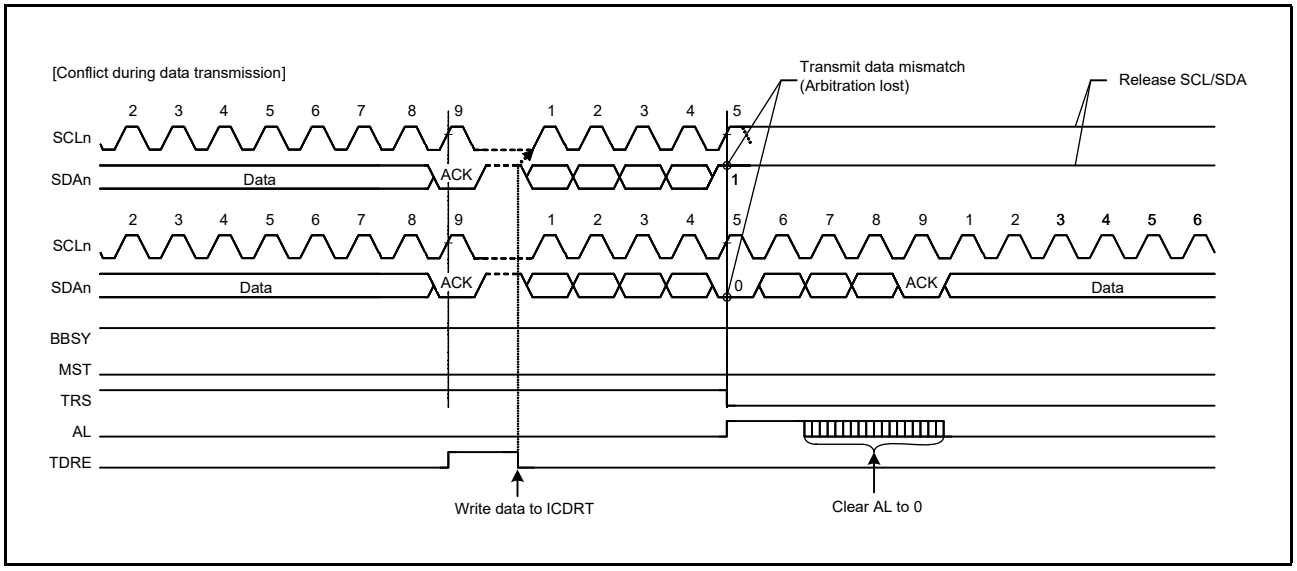


Figure 34.35 Example of Slave Arbitration-Lost Detection (SALE = 1)

34.10 Start Condition/Restart Condition/Stop Condition Issuing Function

34.10.1 Issuing a Start Condition

The RIIC issues a start condition when the ST bit in ICCR2 is set to 1.
When the ST bit is set to 1, a start condition issuance request is made and the RIIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the RIIC automatically shifts to the master transmission mode.
A start condition is issued in the following sequence.

[Start condition issuance]
(1) Drive the SDAn line low (high level to low level).
(2) Ensure the start condition hold time set in ICBRH.
(3) Drive the SCLn line low (high level to low level).
(4) Detect low level of the SCLn line and ensure the low-level period of SCLn line set in ICBRL.

34.10.2 Issuing a Restart Condition

The RIIC issues a restart condition when the RS bit in ICCR2 is set to 1.
When the RS bit is set to 1, a restart condition issuance request is made and the RIIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).
A restart condition is issued in the following sequence.

[Restart condition issuance]
(1) Release the SDAn line.
(2) Ensure the low-level period of SCLn line set in ICBRL.
(3) Release the SCLn line (low level to high level).
(4) Detect a high level of the SCLn line and ensure the restart condition setup time set in ICBRL.
(5) Drive the SDAn line low (high level to low level).
(6) Ensure the restart condition hold time set in ICBRH.
(7) Drive the SCLn line low (high level to low level).
(8) Detect a low level of the SCLn line and ensure the low-level period of SCLn line set in ICBRL.

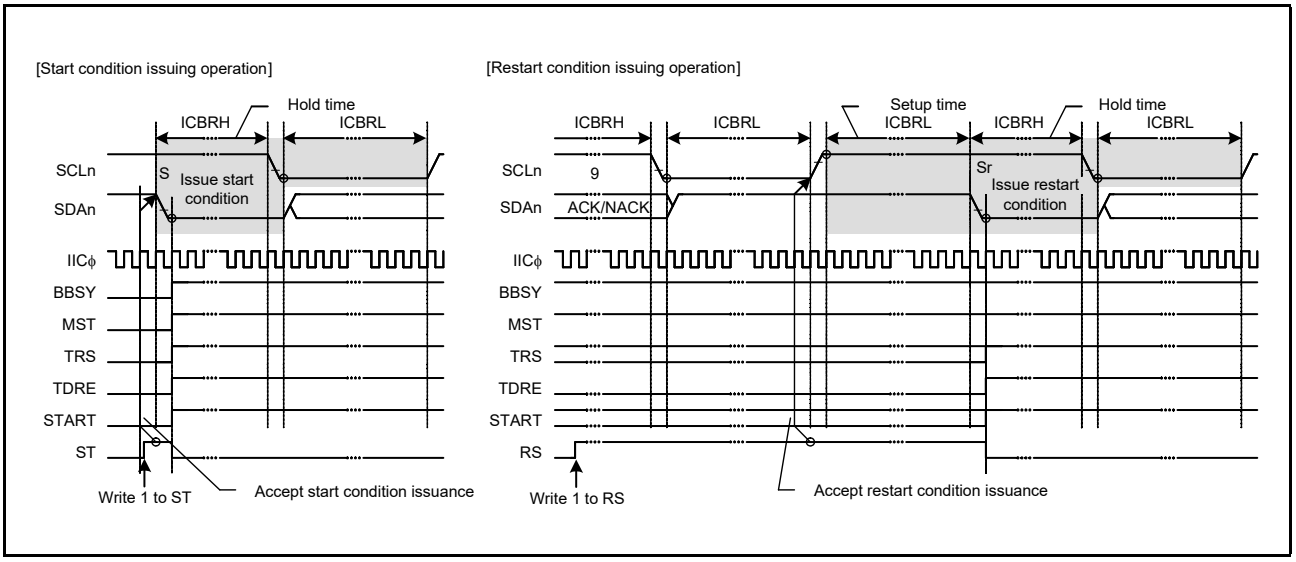


Figure 34.36 Start Condition/Restart Condition Issue Timing (ST and RS Bits)

34.10.3 Issuing a Stop Condition

The RIIC issues a stop condition when the SP bit in ICCR2 is set to 1.
When the SP bit is set to 1, a stop condition issuance request is made and the RIIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).
A stop condition is issued in the following sequence.

[Stop condition issuance]

- Drive the SDAn line low (high level to low level).
- Ensure the low-level period of SCLn line set in ICBRL.
- Release the SCLn line (low level to high level).
- Detect a high level of the SCLn line and ensure the stop condition setup time set in ICBRH.
- Release the SDAn line (low level to high level).
- Ensure the bus free time set in ICBRL.
- Clear the BBSY flag to 0 (to release the bus mastership).

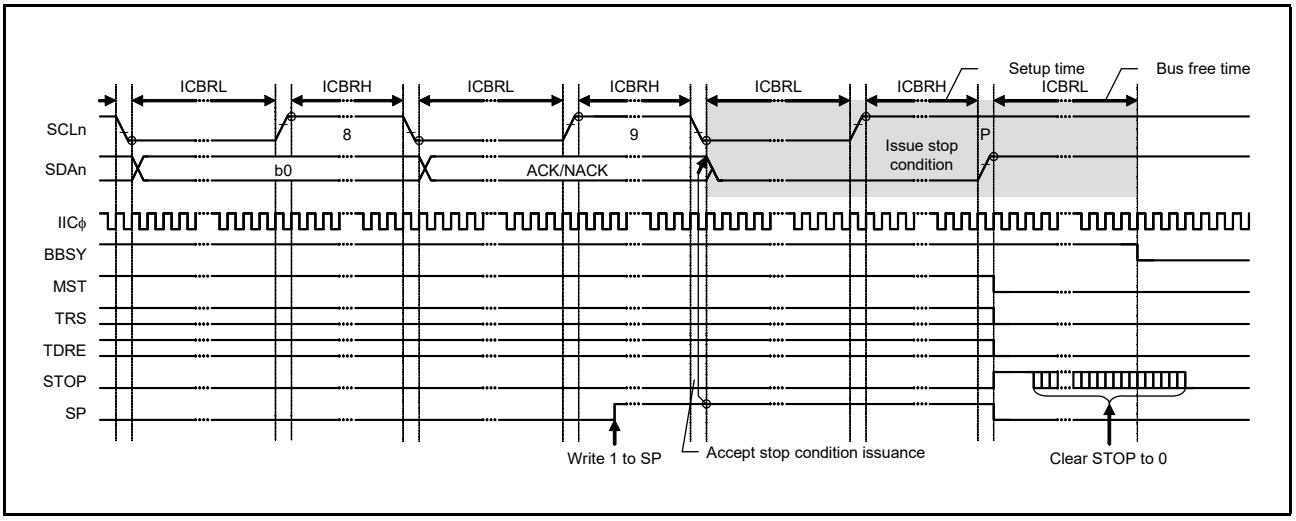


Figure 34.37 Stop Condition Issue Timing (SP Bit)

34.11 Bus Hanging

If the clock signals from the master and slave devices go out of synchronization due to noise or other factors, the I²C bus might hang with a fixed level on the SCLn line and/or SDAn line.
As measures against the bus hanging, the RIIC has a timeout function to detect hanging by monitoring the SCLn line, a function for the output of an extra SCL clock cycle to release the bus from a hung state due to clock signals being out of synchronization, the RIIC reset function, and internal reset function.
By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the RIIC or its partner in communications is placing the low level on the SCLn or SDAn line.

34.11.1 Timeout Function

The RIIC includes a timeout function for detecting when the SCLn line has been stuck longer than the predetermined time. The RIIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.
The timeout function monitors the SCLn line state and counts the low-level period or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rising or falling), but continues to count unless the SCLn line changes. If the internal counter overflows due to no SCLn line change, the RIIC can detect the timeout and report the bus hung state.
This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state that the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1).
- The RIIC's own slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0).
- The bus is free (ICCR2.BBSY flag is 0) while generation of a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function works using the internal reference clock (IICϕ) set by the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).
The SCLn line level (low/high or both levels) during which this counter is activated can be selected by the setting of the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter does not work.

Note: When the timeout function for detecting is to be used, see section 34.2.4, I²C Bus Mode Register 2 (ICMR2), section 34.3, Operation, and section 34.3.2, Initial Settings.

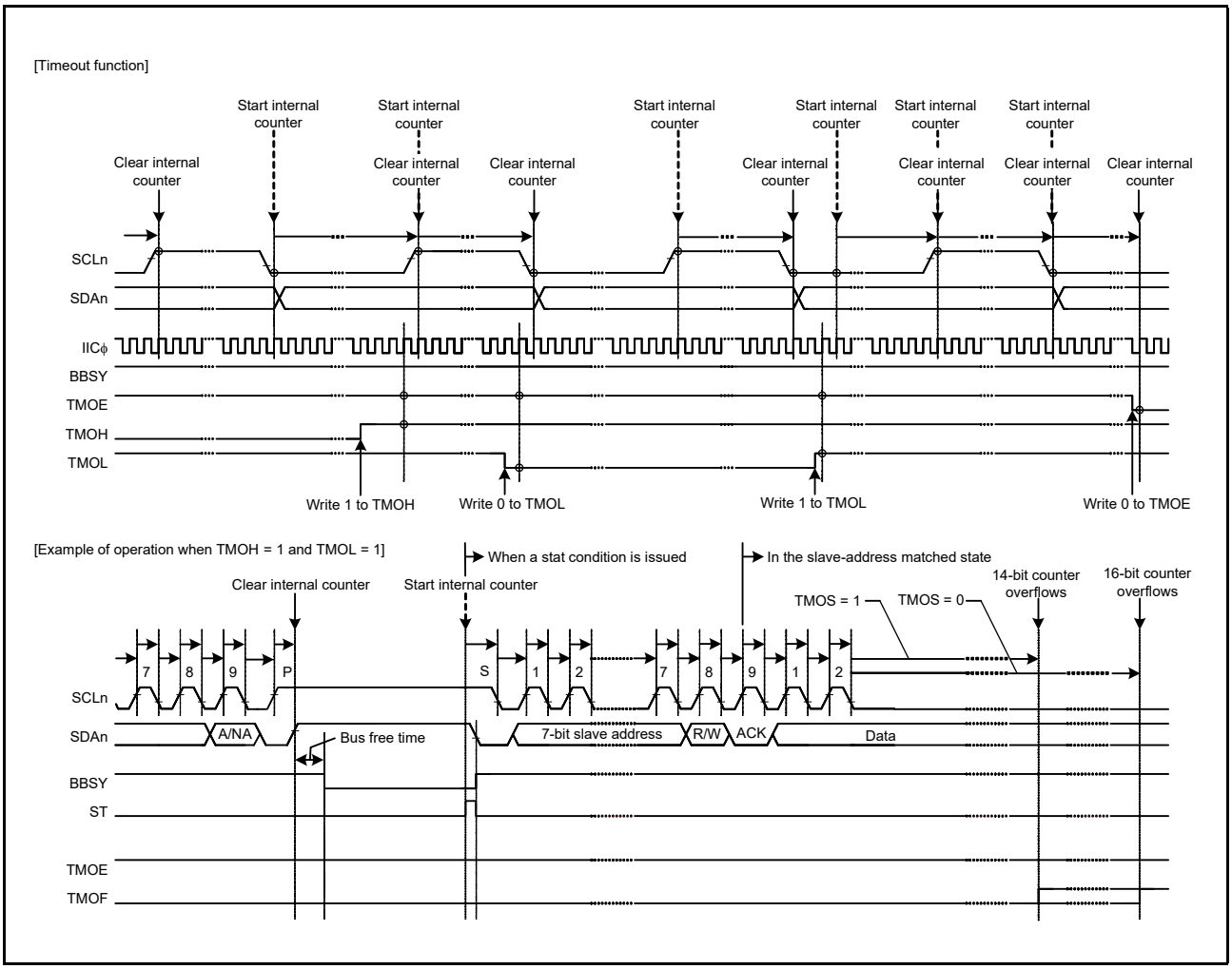


Figure 34.38 Timeout Function (TMOE, TMOS, TMOH, and TMOL Bits)

34.11.2 Extra SCL Clock Cycle Output Function

In master mode, the RIIC module has a facility for the output of extra SCL clock cycles to release the SDAn line of the slave device from being held at the low level due to the master being out of synchronization with the slave device.
This function is mainly used in master mode to release the SDAn line of the slave device from the state of being fixed to the low level by including extra cycles of SCL output from the RIIC with single cycles of the SCL clock as the unit in the case of a bus error where the RIIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this facility in normal situations. Using it when communications are proceeding correctly will lead to malfunctions.
When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the frequency corresponding to the transfer rate settings (settings of the CKS[2:0] bits in ICMR1, and of the ICBRH and ICBRL registers) is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit is automatically set to 0. Therefore, further extra clock cycles can be output consecutively by the software program writing 1 to the CLO bit after having read CLO = 0.
When the RIIC module is in master mode and the slave device is holding the SDAn line at the low level because synchronization with the slave device has been lost due to the effects of noise, etc., the output of a stop condition is not possible. The facility for output of an extra cycle of the SCL clock can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held at the low level, thus recovering the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming release of the SDAn line by the slave device, complete communications by reissuing the stop condition.
Use this facility with the MALE bit (master arbitration-lost detection disabled) in ICFER set to 0. If the MALE bit is set to 1 (master arbitration-lost detection enabled), arbitration is lost when the value of the SDAO bit in ICCR1 does not match the state of the SDAn line, so take care on this point.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is free (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low

Figure 34.39 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

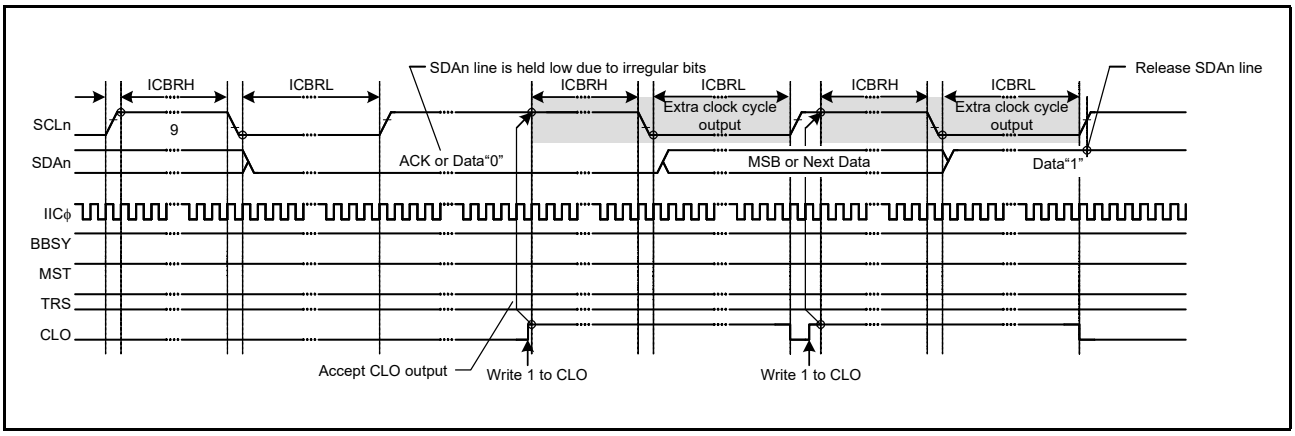


Figure 34.39 Extra SCL Clock Cycle Output Function (CLO Bit)

34.11.3 RIIC Reset and Internal Reset

The RIIC module incorporates a function for resetting itself. There are two types of reset. One is referred to as an RIIC reset; this initializes all registers including the BBSY flag in ICCR2. The other is referred to as an internal reset; this releases the RIIC from the slave-address matched state and initializes the internal counter while retaining other settings. After issuing a reset, be sure to set the IICRST bit in ICCR1 to 0.

Both types of reset are effective for release from bus-hung states since both restore the output state of the SCLn and SDAn pins to the high impedance state.

Do not issue a reset during slave operation because it may lead to a loss of synchronization between the master device clock and the slave device clock. Note that monitoring of the bus state, such as for the presence of a start condition, is not possible during an RIIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the RIIC and internal resets, refer to section 34.13, Resets and Register and Function States When Issuing Each Condition.

34.12 Interrupt Sources

The RIIC issues four types of interrupt request: transfer error or event generation (arbitration-lost, NACK detection, timeout detection, start condition detection, and stop condition detection), receive data full, transmit data empty, and transmit end.

Table 34.6 lists details of the several interrupt requests. The receive data full and transmit data empty are both capable of activating data transfer by the DMAC.

Table 34.6 Interrupt Sources

Symbol	Interrupt Source	Interrupt Flag	DMAC Activation	Interrupt Condition
EEI	Transfer error/ event generation	AL	Not possible	AL = 1 • ALIE = 1
		NACKF		NACKF = 1 • NAKIE = 1
		TMOF		TMOF = 1 • TMOIE = 1
		START		START = 1 • STIE = 1
		STOP		STOP = 1 • SPIE = 1
RXI*1	Receive data full	—	Possible	RDRF = 1 • RIE = 1
TXI*2	Transmit data empty	—	Possible	TDRE = 1 • TIE = 1
TEI*3	Transmit end	TEND	Not possible	TEND = 1 • TEIE = 1

Note: There is a delay time between the execution of a write instruction for a peripheral module by the CPU and actual writing to the module. Thus, when an interrupt flag has been cleared or masked, read the relevant flag again to check whether clearing or masking has been completed, and then return from interrupt handling. Returning from interrupt handling without checking that writing to the module has been completed creates a possibility of repeated processing of the same interrupt.

Note 1. The RDRF flag in ICSR2 (a condition for RXI) is automatically set to 0 when data are read from ICDRR.

Note 2. The TDRE flag in ICSR2 (a condition for TXI) is automatically set to 0 when data for transmission are written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Note 3. When using the TEI interrupt, clear the TEND flag in ICSR2 in the TEI interrupt handling.
Note that the TEND flag in ICSR2 is automatically set to 0 when data for transmission are written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).

Clear or mask the each flag during interrupt handling.

34.13 Resets and Register and Function States When Issuing Each Condition

The RIIC has reset, RIIC reset, and internal reset functions. Table 34.7 lists the resets and register and function states when issuing each condition.

Table 34.7 Resets and Register and Function States When Issuing Each Condition

		Chip Reset	RIIC Reset (ICE = 0, IICRST = 1)	Internal Reset (ICE = 1, IICRST = 1)	Start Condition/ Restart Condition Detection	Stop Condition Detection
ICCR1	ICE, IICRST	At a reset	Retained	Retained	Retained	Retained
	SCLO, SDAO		At a reset	At a reset		
	Others			Retained		
ICCR2	BBSY	At a reset	At a reset	Retained	Retained	Retained
	ST			At a reset	At a reset	Retained
	Others					At a reset
ICMR1	BC[2:0]	At a reset	At a reset	At a reset	At a reset	Retained
	Others			Retained	Retained	
ICMR2		At a reset	At a reset	Retained	Retained	Retained
ICMR3		At a reset	At a reset	Retained	Retained	Retained
ICFER		At a reset	At a reset	Retained	Retained	Retained
ICSER		At a reset	At a reset	Retained	Retained	Retained
ICIER		At a reset	At a reset	Retained	Retained	Retained
ICSR1		At a reset	At a reset	At a reset	Retained	At a reset
ICSR2	TDRE, TEND	At a reset	At a reset	At a reset	Retained	At a reset
	START				Retained	
	STOP				Retained	Retained
	Others				Retained	Retained
ICSARL0, ICSARL1, ICSARL2 ICSARU0, ICSARU1, ICSARU2		At a reset	At a reset	Retained	Retained	Retained
ICBRH, ICBRL		At a reset	At a reset	Retained	Retained	Retained
ICDRT		At a reset	At a reset	Retained	Retained	Retained
ICDRR		At a reset	At a reset	Retained	Retained	Retained
ICDRS		At a reset	At a reset	At a reset	Retained	Retained
Timeout function		At a reset	At a reset	Operation	Operation	Operation
Bus free time measurement		At a reset	At a reset	Operation	Operation	Operation

34.14 Event Link Output

The RIIC0 handles event output for the event link controller (ELC) corresponding to the following sources.

(1) Transfer error event

When a transfer error event occurs, the corresponding event signal can be output for another module via the ELC.

(2) Receive data full

When a receive data register becomes full, the corresponding event signal can be output for another module via the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the corresponding event signal can be output for another module via the ELC.

(4) Transmit end

On completion of transfer, the corresponding event signal can be output for another module via the ELC.

34.14.1 Interrupt Handling and Event Linking

The RIIC module produces four kinds of interrupt: transfer error or event generation (arbitration-lost detection, detection of NACK, detection of timeout, detection of a start condition, or detection of a stop condition), receive data full, transmit data empty, and transmit end interrupts. Each of these has an enable bit to control enabling and disabling of the interrupt signal. An interrupt request signal is output for the CPU when an interrupt source condition is satisfied while the setting of the corresponding enable bit is enabled.

The corresponding event link output signals are sent to other modules as event signals via the ELC when the interrupt source conditions are satisfied, regardless of the settings of the interrupt enable bits.

For details on interrupt sources, see Table 34.6.

34.15 Usage Notes

34.15.1 Setting Module Stop Function

Module-stop state can be entered or canceled using module stop control register B (MSTPCRB). The initial setting is for operation of the RIIC to be stopped. RIIC register access is enabled by clearing the module-stop state.
For details on module stop control registers B, refer to section 9, Low-Power Consumption Function.

35. CAN Interface (RSCAN)

This section contains a generic description of the CAN Interface (RSCAN).

35.1 Overview

35.1.1 Functional Overview

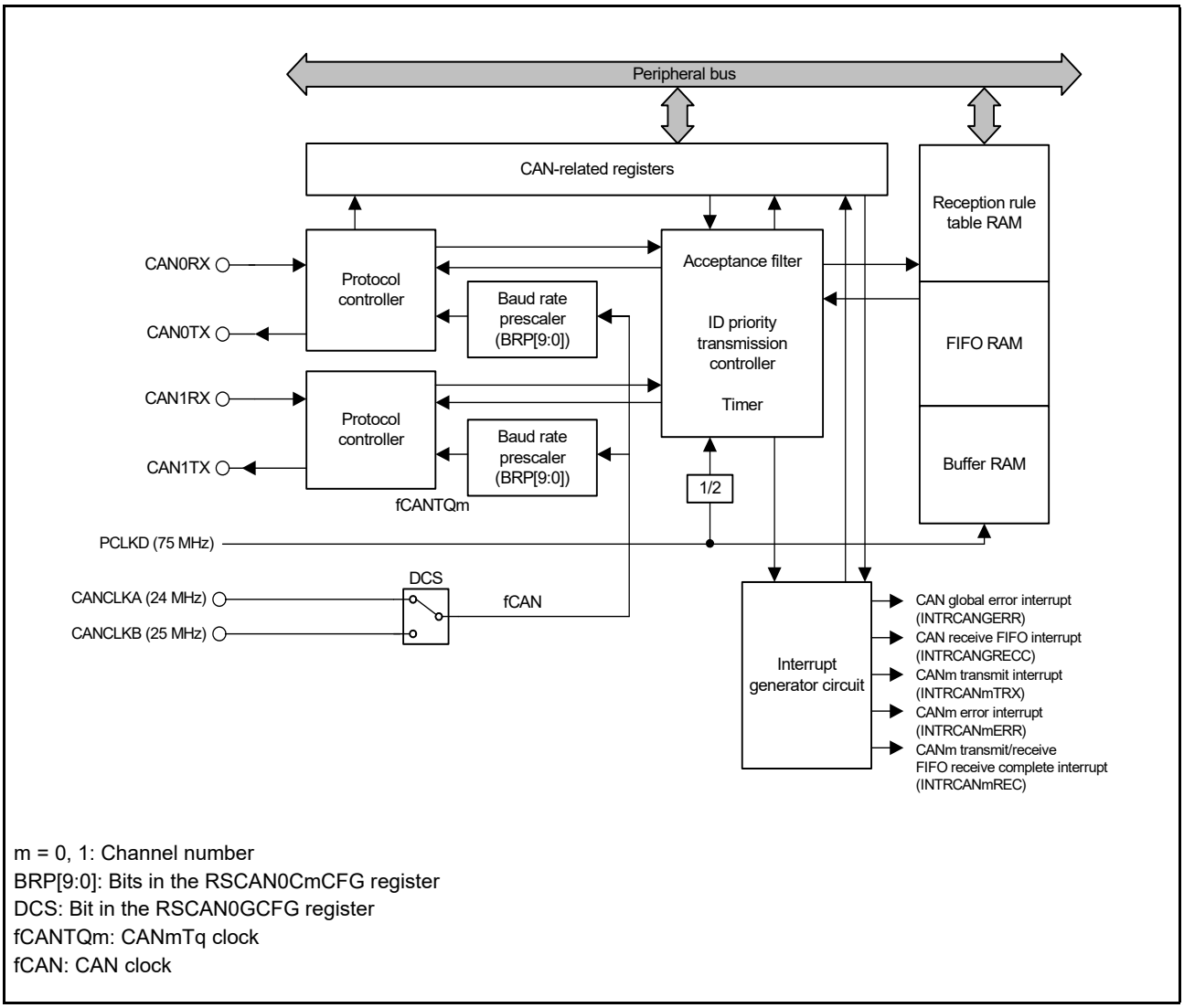
This LSI incorporates one unit of the CAN interface (RSCAN) which consists of two channels (CAN0 and CAN1) of the CAN controller conforming to the ISO11898-1 specifications. Table 35.1 shows the specifications of the RSCAN and Figure 35.1 shows a block diagram of the RSCAN.

Table 35.1 Specifications of the RSCAN (1 / 2)

Item	Specification
Number of channels	2
Protocol	ISO11898-1 compliant (standard or extended frame)
Communication speed	• Maximum 1 Mbps $\text{Communication speed (CANm bit time clock)} = \frac{1}{\text{CANm bit time}}$ CANm bit time = CANmTq × Tq count per bit $\text{CANmTq} = \frac{\text{(BRP[9:0] bits in the RSCAN0CmCFG register + 1)}}{\text{fCAN}}$ m = 0, 1 (channel number) Tq: Time quantum (1 Tq per bit = 1 + TSEG1 + TSEG2) fCAN: Frequency of CAN clock (selected by the DCS bit in the RSCAN0GCFG register)
Buffer	160 buffers in total • Individual buffers: 32 buffers (16 buffers × 2 channels) Transmission buffer: 16 buffers per channel Transmission queue: Single queue per channel (shared with the transmission buffer; up to 16 buffers allocatable) • Shared buffers: 128 buffers for all channels (64 buffers × 2 channels) Reception buffer: 32 buffers (16 buffers × 2 channels) Reception FIFO buffer: 8 FIFO buffers (up to 128 buffers allocatable to each) Transmission/reception FIFO buffer: 3 FIFO buffers per channel (up to 128 buffers allocatable to each) • ECC included
Reception function	• Receives data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be received. • Sets interrupt enable/disable for each FIFO. • Mirror function (reception of messages transmitted from the own CAN node) • Timestamp function (to record message reception time as a 16-bit timer value)
Reception filter function	• Selects received messages according to 128 reception rules. • Sets the number of reception rules (0 to 128) for each channel. • Acceptance filter processing: Sets ID and mask for each reception rule. • DLC filter processing: Enables DLC filter check for each reception rule.
Received message transfer function	• Routing function Transfers received messages to arbitrary destinations (can be transferred to up to 8 buffers) Transfer destination: Reception buffer, reception FIFO buffer, and/or transmission/reception FIFO buffer • Label addition function Stores label information together with a message in a reception buffer and FIFO buffer.
Transmission function	• Transmits data frames and remote frames. • Selects ID format (standard ID, extended ID, or both IDs) to be transmitted. • Sets interrupt enable/disable for each transmission buffer and transmission/reception FIFO buffer. • Selects ID priority transmission or transmission buffer number priority transmission. • Transmission request can be aborted (possible to confirm with a flag) • One-shot transmission function
Interval transmission function	Transmit messages at configurable intervals (transmission mode or gateway mode of transmission/reception FIFO buffers)

Table 35.1 Specifications of the RSCAN (2 / 2)

Item	Specification
Transmission queue function	Transmits all stored messages according to the ID priority.
Transmission history function	Stores the history information of transmission-completed messages
Gateway function	Transmits a received message automatically.
Bus off recovery mode selection	• Selects the method for returning from bus off state. • ISO11898-1 compliant • Automatic entry to channel halt mode at bus-off entry • Automatic entry to channel halt mode at bus-off end • Transition to channel standby mode by program request • Transition to the error-active state by program request (forcible return from the bus off state)
Error status monitoring	• Monitors CAN protocol errors (stuff error, form error, ACK error, CRC error, bit error, ACK delimiter error, and bus dominant lock). • Detects error status transitions (error warning, error passive, bus off entry, and bus off recovery) • Reads the error counter. • Monitors DLC errors.
Interrupt source	8 sources • Global Interrupts (2 sources) CAN receive FIFO interrupt CAN global error interrupt • Channel interrupts (3 sources/channel) (m = 0, 1) CANm transmit interrupt (CANm transmission complete, CANm transmission abort, etc.) CANm transmit/receive FIFO receive complete interrupt CANm error interrupt (bus error, bus lock, etc.)
Error source	An ECC error in the buffer RAM is detected and conveyed to the error control module (ECM). • 1-bit ECC error in the RSCAN RAM. • 2-bit ECC error in the RSCAN RAM. • RSCAN overflow error
Low-power consumption function	The module-stop state can be set.
CAN clock source	PLL0 frequency-division of CANCLKA (24 MHz) or the main clock signal (CANCLKB; 25 MHz) is selectable
Test function	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test) • Inter-channel communication test



m = 0, 1: Channel number
BRP[9:0]: Bits in the RSCAN0CmCFG register
DCS: Bit in the RSCAN0GCFG register
fCANTQm: CANmTq clock
fCAN: CAN clock

Figure 35.1 Block Diagram of the RSCAN

Table 35.2 lists the I/O pins used in the RSCAN.

Table 35.2 RSCAN Pin Configuration

Channel	Pin Name	I/O	Function
CAN0	CRXD0	Input	CAN0 receive data input pin
	CTXD0	Output	CAN0 transmit data output pin
CAN1	CRXD1	Input	CAN1 receive data input pin
	CTXD1	Output	CAN1 transmit data output pin

Table 35.3 lists the meanings of indices used throughout this section.

Table 35.3 Index

Index	Meaning
m	Throughout this section, the individual channels of RSCAN units are generically indicated by the index “m” (m = 0, 1); for example, RSCAN0CmSTS is the channel m status register.
j	The individual registers associated with reception rule table are generically indicated by the index “j” (j = 0 to 15); for example, RSCAN0GAFLIDj is the reception rule ID register.
k	The individual transmission/reception FIFO buffers are generically indicated by the index “k” (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1); for example, RSCAN0CFCCk is the transmission/reception FIFO buffer configuration/control register.
x	The individual reception FIFO buffers in the RSCAN units are identified by the index “x” (x = 0 to 7): for example, RSCAN0RFSTSx is the reception FIFO buffer status register in the RSCAN0 unit.
q	The individual reception buffers are generically indicated by the index “q” (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1); for example, RSCAN0RMIDq is the reception buffer ID register.
p	The individual transmission buffers are generically indicated by the index “p” (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1); for example, RSCAN0TMCp is the transmission buffer control register.
r	The individual RAM tests for CAN are generically indicated by the index “r” (r = 0 to 63); for example, RSCAN0RPGACCr is the RAM test page access register.
z	The individual ECC error address registers for CAN are generically indicated by the index “z” (z = 0 to 7).

35.2 Register Descriptions

35.2.1 Channel Configuration Registers (RSCAN0CmCFG) (m = 0, 1)

The RSCAN0CmCFG registers control the settings for clock timing on each channel.
Modify the RSCAN0CmCFG registers in channel reset mode or channel halt mode. Set these registers in channel reset mode before shifting to channel communication mode or channel wait mode. For a description of the bit timing parameters and settings, see section 35.9.1, Initial Settings.

Address(es): RSCAN.RSCAN0C0CFG A007 8000h, RSCAN.RSCAN0C1CFG A007 8010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	SJW[1:0]		—	TSEG2[2:0]			TSEG1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	BRP[9:0]	Prescaler Division Ratio Set	When these bits are set to P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b19 to b16	TSEG1[3:0]	Time Segment 1 Control	b19 b18 b17 b16 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq Settings other than above are prohibited.	R/W
b22 to b20	TSEG2[2:0]	Time Segment 2 Control	b22 b21 b20 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq Settings other than above are prohibited.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b25, b24	SJW[1:0]	Resynchronization Jump Width Control	b25 b24 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

BRP[9:0] Bits (Prescaler Division Ratio Set)

The CANmTq clock (fCANTQm) is calculated by dividing the CAN clock (fCAN) by the baud rate prescaler, ((BRP[9:0]) + 1). One clock cycle of the CANmTq clock is 1 Time Quantum (Tq) (m = 0, 1).

TSEG1[3:0] Bits (Time Segment 1 Control)

These bits are used to specify a Tq value for the total length of the propagation segment (PROP_SEG) and phase segment 1 (PHASE_SEG1).
Allowed values are 4 Tq to 16 Tq, inclusive.

TSEG2[2:0] Bits (Time Segment 2 Control)

These bits are used to specify a Tq value for the length of phase segment 2 (PHASE_SEG2).
Allowed values are 2 Tq to 8 Tq, inclusive.
Set a value smaller than the value of the TSEG1 bits.

SJW[1:0] Bits (Resynchronization Jump Width Control)

These bits are used to specify a Tq value for the resynchronization jump width. Allowed values are 1 Tq to 4 Tq, inclusive.
Set a value less than or equal to the value of the TSEG2 bits. For the Tq value, see the description of BRP[9:0] bits.

35.2.2 Channel Control Registers (RSCAN0CmCTR) (m = 0, 1)

The RSCAN0CmCTR registers control the operating mode of and the settings for interrupts from each channel.

Address(es): RSCAN.RSCAN0C0CTR A007 8004h, RSCAN.RSCAN0C1CTR A007 8014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	CTMS[1:0]		CTME	ERRD	BOM[1:0]		—	—	—	—	TAIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ALIE	BLIE	OLIE	BORIE	BOEIE	EPIE	EWIE	BEIE	—	—	—	—	RTBO	CSLPR	CHMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	CHMDC[1:0]	Mode Select	b1 b0 0 0: Channel communication mode 0 1: Channel reset mode 1 0: Channel halt mode Settings other than above are prohibited.	R/W
b2	CSLPR	Channel Stop Mode	0: Other than channel stop mode 1: Channel stop mode	R/W
b3	RTBO	Forcible Return from Bus-off	When this bit is set to 1, forcible return from the bus off state is made. This bit is always read as 0.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BEIE	Bus Error Interrupt Enable	0: Bus error interrupt is disabled. 1: Bus error interrupt is enabled.	R/W
b9	EWIE	Error Warning Interrupt Enable	0: Error warning interrupt is disabled. 1: Error warning interrupt is enabled.	R/W
b10	EPIE	Error Passive Interrupt Enable	0: Error passive interrupt is disabled. 1: Error passive interrupt is enabled.	R/W
b11	BOEIE	Bus Off Entry Interrupt Enable	0: Bus off entry interrupt is disabled. 1: Bus off entry interrupt is enabled.	R/W
b12	BORIE	Bus Off Recovery Interrupt Enable	0: Bus off recovery interrupt is disabled. 1: Bus off recovery interrupt is enabled.	R/W
b13	OLIE	Overload Frame Transmit Interrupt Enable	0: Overload frame transmit interrupt is disabled. 1: Overload frame transmit interrupt is enabled.	R/W
b14	BLIE	Bus Lock Interrupt Enable	0: Bus lock interrupt is disabled. 1: Bus lock interrupt is enabled.	R/W
b15	ALIE	Arbitration Lost Interrupt Enable	0: Arbitration lost interrupt is disabled. 1: Arbitration lost interrupt is enabled.	R/W
b16	TAIE	Transmission Abort Interrupt Enable	0: Transmission abort interrupt is disabled. 1: Transmission abort interrupt is enabled.	R/W
b20 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22, b21	BOM[1:0]	Bus Off Recovery Mode Select	b22 b21 0 0: ISO11898-1 compliant 0 1: Entry to channel halt mode automatically at bus-off entry 1 0: Entry to channel halt mode automatically at bus-off end 1 1: Entry to channel halt mode (in bus-off state) by program request	R/W
b23	ERRD	Error Display Mode Select	0: Error flags are displayed only for the first error information after bits 14 to 8 in RSCAN0CmERFL are all cleared. 1: Error flags for all error information are displayed.	R/W

Bit	Symbol	Bit Name	Description	R/W
b24	CTME	Communication Test Mode Enable	0: Communication test mode is disabled. 1: Communication test mode is enabled.	R/W
b26, b25	CTMS[1:0]	Communication Test Mode Select	b26 b25 0 0: Standard test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback mode) 1 1: Self-test mode 1 (internal loopback mode)	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CHMDC[1:0] Bits (Mode Select)

These bits are used to select a channel mode (channel communication mode, channel reset mode, or channel halt mode). For details, see section 35.4.2, Channel Modes. Setting the CSLPR bit to 1 in channel reset mode allows transition to channel stop mode. Do not set the CHMDC[1:0] bits to 11b. When the CAN module has automatically transitioned to channel halt mode based on the setting of the BOM[1:0] bits, the CHMDC[1:0] bits automatically become 10b.

CSLPR Bit (Channel Stop Mode)

Setting this bit to 1 places the channel into channel stop mode.
Clearing this bit to 0 makes the channel exit channel stop mode.
This bit should not be modified in channel communication mode or channel wait mode.

RTBO Bit (Forcible Return from Bus-off)

Setting this bit to 1 in the bus off state forcibly returns the state from the bus off state to the error active state. This bit is automatically cleared to 0. Setting this bit to 1 clears the TEC[7:0] and REC[7:0] bits in the RSCAN0CmSTS register to 00h and also clears the BOSTS flag in the RSCAN0CmSTS register to 0 (not in bus off state). The other registers remain unchanged. No bus off recovery interrupt request is generated upon return from the bus off state in this case. Use this bit only when the BOM[1:0] bits in the RSCAN0CmCTR register are 00b (ISO11898-1 compliant).
A delay of up to one CANm bit time occurs after the RTBO bit is set to 1 until the RSCAN module transitions to the error active state. Set this bit to 1 in channel communication mode.

BEIE Bit (Bus Error Interrupt Enable)

When the BEF flag in the RSCAN0CmERFL register is set to 1 with the BEIE bit set to 1, a CANm error interrupt request (bus error interrupt) is generated. Modify this bit in channel reset mode.

EWIE Bit (Error Warning Interrupt Enable)

When the EWF flag in the RSCAN0CmERFL register is set to 1 with the EWIE bit set to 1, a CANm error interrupt request (error warning interrupt) is generated. Modify this bit in channel reset mode.

EPIE Bit (Error Passive Interrupt Enable)

When the EPF flag in the RSCAN0CmERFL register is set to 1 with the EPIE bit set to 1, a CANm error interrupt request (error passive interrupt) is generated. Modify this bit in channel reset mode.

BOEIE Bit (Bus Off Entry Interrupt Enable)

When the BOEF flag in the RSCAN0CmERFL register is set to 1 with the BOEIE bit set to 1, a CANm error interrupt request (bus off entry interrupt) is generated. Modify this bit in channel reset mode.

BORIE Bit (Bus Off Recovery Interrupt Enable)

When the BORF flag in the RSCAN0CmERFL register is set to 1 with the BORIE bit set to 1, a CANm error interrupt request (bus off recovery interrupt) is generated. Modify this bit in channel reset mode.

OLIE Bit (Overload Frame Transmit Interrupt Enable)

When the OVLF flag in the RSCAN0CmERFL register is set to 1 with the OLIE bit set to 1, a CANm error interrupt request (overload frame interrupt) is generated. Modify this bit in channel reset mode.

BLIE Bit (Bus Lock Interrupt Enable)

When the BLF flag in the RSCAN0CmERFL register is set to 1 with the BLIE bit set to 1, a CANm error interrupt request (bus lock interrupt) is generated. Modify this bit in channel reset mode.

ALIE Bit (Arbitration Lost Interrupt Enable)

When the ALF flag in the RSCAN0CmERFL register is set to 1 with the ALIE bit set to 1, a CANm error interrupt request (arbitration lost interrupt) is generated. Modify this bit in channel reset mode.

TAIE Bit (Transmission Abort Interrupt Enable)

When transmission abort of the transmission buffer is completed with the TAIE bit set to 1, a CANm transmission interrupt request (transmission abort interrupt) is generated. Modify this bit only in channel reset mode.

BOM[1:0] Bits (Bus Off Recovery Mode Select)

These bits are used to select the bus off recovery mode of the RSCAN module.

When the BOM[1:0] bits are set to 00b, return from the bus off state to the error active state is compliant with the CAN specifications. That is, the RSCAN module reenters the CAN communication (error active state) after 11 consecutive recessive bits are detected 128 times. A bus off recovery interrupt request is generated at the time of return from the bus off state. Even if the CHMDC[1:0] bits are set to 10b (channel halt mode) before recessive bits are detected 128 times, the RSCAN module does not transition to channel halt mode until recessive bits are detected 128 times.

When the RSCAN module reaches the bus off state when the BOM[1:0] bits are set to 01b, the CHMDC[1:0] bits in the RSCAN0CmCTR register (m = 0, 1) are set to 10b and the RSCAN module transitions to channel halt mode. No bus off recovery interrupt request is generated at the time of return from the bus off state and the TEC[7:0] and REC[7:0] bits in the RSCAN0CmSTS register are cleared to 00h.

When the RSCAN module reaches the bus off state when the BOM[1:0] bits are set to 10b, the CHMDC[1:0] bits are set to 10b and the RSCAN module transitions to channel halt mode after return from the bus off state (11 consecutive recessive bits are detected 128 times). A bus off recovery interrupt request is generated at the time of return from the bus off state and the TEC[7:0] and REC[7:0] bits are cleared to 00h.

When the BOM[1:0] bits are set to 11b and the CHMDC[1:0] bits are set to 10b while the RSCAN module is in the bus off state, the RSCAN module transitions to channel halt mode. No bus off recovery interrupt request is generated at the time of return from the bus off state and the TEC[7:0] and REC[7:0] bits are cleared to 00h. However, if 11 consecutive recessive bits are detected 128 times and the RSCAN module has recovered to the error active state from the bus off state before the CHMDC[1:0] bits are set to 10b, a bus off recovery interrupt request is generated.

If a program writes to the CHMDC[1:0] bit at the same time as the RSCAN module transition to channel halt mode (at bus off entry when the BOM[1:0] bits are 01b or at bus off end when the BOM[1:0] bits are 10b), the program's writing takes precedence. Modify the BOM[1:0] bits in channel reset mode.

ERRD Bit (Error Display Mode Select)

This bit is used to control the display mode of bits 14 to 8 in the RSCAN0CmERFL register.
When this bit is clear to 0, only the flags of the first error event are set to 1. If two or more errors occur in the first error event, all the flags of the detected errors are set to 1.
When this bit is set to 1, all the flags of errors that have occurred are set to 1 regardless of the error occurrence order.
Modify this bit in channel reset mode or channel halt mode.

CTMS[1:0] Bits (Communication Test Mode Select)

These bits are used to select a communication test mode. Modify these bits in channel halt mode. These bits are set to 0 in channel reset mode.

35.2.3 Channel Status Register (RSCAN0CmSTS) (m = 0, 1)

The RSCAN0CmSTS registers are status registers that indicate the state of transfer on each channel.

Address(es): RSCAN.RSCAN0C0STS A007 8008h, RSCAN.RSCAN0C1STS A007 8018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TEC[7:0]								REC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	COMSTS	RECSTS	TRMSTS	BOSTS	EPSTS	CSLPSTS	CHLTSTS	CRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CRSTSTS	Channel Reset Status Flag	0: Not in channel reset mode 1: In channel reset mode	R
b1	CHLTSTS	Channel Halt Status Flag	0: Not in channel halt mode 1: In channel halt mode	R
b2	CSLPSTS	Channel Stop Status Flag	0: Not in channel stop mode 1: In channel stop mode	R
b3	EPSTS	Error Passive Status Flag	0: Not in error passive state 1: In error passive state	R
b4	BOSTS	Bus Off Status Flag	0: Not in bus off state 1: In bus off state	R
b5	TRMSTS	Transmission Status Flag	0: Bus idle or in reception 1: In transmission or bus off state	R
b6	RECSTS	Reception Status Flag	0: Bus idle, in transmission or bus off state 1: In reception	R
b7	COMSTS	Communication Status Flag	0: Communication is not ready. 1: Communication is ready.	R
b15 to b8	—	Reserved	These bits are read as 0.	R
b23 to b16	REC[7:0]	Receive Error Counter	The receive error counter (REC) can be read.	R
b31 to b24	TEC[7:0]	Transmit Error Counter	The transmit error counter (TEC) can be read.	R

CRSTSTS Flag (Channel Reset Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel reset mode, and is cleared to 0 when the CAN module has transitioned to channel communication mode or channel halt mode. This flag remains 1 when the CAN module transitions from channel reset mode to channel stop mode.

CHLTSTS Flag (Channel Halt Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel halt mode, and is cleared to 0 when the CAN module has returned from channel halt mode.

CSLPSTS Flag (Channel Stop Status Flag)

This flag is set to 1 when the CAN module has transitioned to channel stop mode, and is cleared to 0 when the CAN module has returned from channel stop mode.

EPSTS Flag (Error Passive Status Flag)

This flag is set to 1 when the RSCAN module has entered the error passive state ((128 ≤ TEC[7:0] ≤ 255) or (128 ≤ REC[7:0])). It is cleared to 0 when the RSCAN module has exited the error passive state or has entered channel reset mode.

BOSTS Flag (Bus Off Status Flag)

This flag is set to 1 when the bus off state (TEC[7:0] > 255) is entered. It is cleared to 0 when the CAN module has exited the bus off state.

TRMSTS Flag (Transmission Status Flag)

This flag is set to 1 when transmission has started, and is cleared to 0 when the bus has become idle or reception has started. This flag remains 1 in the bus off state.

RECSTS Flag (Reception Status Flag)

This flag is set to 1 when reception has started, and is cleared to 0 when the bus has become idle or transmission has started.

COMSTS Flag (Communication Status Flag)

This bit indicates that communication is ready.
This flag becomes 1 when the CAN module has detected 11 consecutive recessive bits after it has transitioned from channel reset mode or channel halt mode to channel communication mode. This flag is cleared to 0 in channel reset mode or channel halt mode.

REC[7:0] Bits (Receive Error Counter)

These bits contain the receive error counter value. For receive error counter increment/decrement conditions, see the CAN specifications (ISO11898-1).
These bits are cleared to 0 in channel reset mode.

TEC[7:0] Bits (Transmit Error Counter)

These bits contain the transmit error counter value. For transmit error counter increment/decrement conditions, see the CAN specification (ISO11898-1).
These bits are cleared to 0 in channel reset mode.

35.2.4 Channel Error Flag Registers (RSCAN0CmERFL) (m = 0, 1)

The RSCAN0CmERFL registers are status registers that indicate the state of error detection on each channel.
See the CAN specification (ISO11898-1) for a description of error occurrence conditions. To clear each flag of these registers, the program must write a 0 to the corresponding bit. Writing 1 to these flags does not change them to 1. If any of these flags is set to 0 at the same time that the program writes 0 to the flag, the flag is still set to 1. The channel reset mode transition clears all of these flags to 0.
If the ERRD bit in the RSCAN0CmCTR registers is set to 0 (i.e., only the flags for the first error event are displayed) and an error related to bits 14 to 8 of RSCAN0CmERFL is detected, the flag bits are only set by the error event if bits 14 to 8 were all 0 at the when time the error occurred.

Address(es): RSCAN.RSCAN0C0ERFL A007 800Ch, RSCAN.RSCAN0C1ERFL A007 801Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CRCREG[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADERR	B0ERR	B1ERR	CERR	AERR	FERR	SERR	ALF	BLF	OVLF	BORF	BOEF	EPF	EWF	BEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BEF	Bus Error Flag	0: No channel bus error is detected. 1: Channel bus error is detected.	R/W *1
b1	EWF	Error Warning Flag	0: No error warning is detected. 1: Error warning is detected.	R/W *1
b2	EPF	Error Passive Flag	0: No error passive is detected. 1: Error passive is detected.	R/W *1
b3	BOEF	Bus Off Entry Flag	0: No bus off entry is detected. 1: Bus off entry is detected.	R/W *1
b4	BORF	Bus Off Recovery Flag	0: No bus off recovery is detected. 1: Bus off recovery is detected.	R/W *1
b5	OVLF	Overload Flag	0: No overload is detected. 1: Overload is detected.	R/W *1
b6	BLF	Bus Lock Flag	0: No channel bus lock is detected. 1: Channel bus lock is detected.	R/W *1
b7	ALF	Arbitration-lost Flag	0: No arbitration-lost is detected. 1: Arbitration-lost is detected.	R/W *1
b8	SERR	Stuff Error Flag	0: No stuff error is detected. 1: Stuff error is detected.	R/W *1
b9	FERR	Form Error Flag	0: No form error is detected. 1: Form error is detected.	R/W *1
b10	AERR	ACK Error Flag	0: No ACK error is detected. 1: ACK error is detected.	R/W *1
b11	CERR	CRC Error Flag	0: No CRC error is detected. 1: CRC error is detected.	R/W *1
b12	B1ERR	Recessive Bit Error Flag	0: No recessive bit error is detected. 1: Recessive bit error is detected.	R/W *1
b13	B0ERR	Dominant Bit Error Flag	0: No dominant bit error is detected. 1: Dominant bit error is detected.	R/W *1
b14	ADERR	ACK Delimiter Error Flag	0: No ACK delimiter error is detected. 1: ACK delimiter error is detected.	R/W *1
b15	—	Reserved	This bit is read as 0.	R

Bit	Symbol	Bit Name	Description	R/W
b30 to b16	CRCREG [14:0]	CRC Calculation Data	A CRC value calculated based on the transmitted or received message is indicated.	R
b31	—	Reserved	This bit is read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

BEF Flag (Bus Error Flag)

This flag is set to 1 when any one of the ADERR, B0ERR, B1ERR, CERR, AERR, FERR, and SERR flags in the RSCAN0CmERFL register is set to 1.

EWF Flag (Error Warning Flag)

This flag is set to 1 only when the REC[7:0] or TEC[7:0] value first exceeds 95. Therefore, if the program writes 0 to this flag while the value of REC[7:0] or TEC[7:0] remains over 95, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 95 or less and then the REC[7:0] or TEC[7:0] value exceeds 95 again.

EPF Flag (Error Passive Flag)

This flag becomes 1 when the error passive state is reached (REC[7:0] or TEC[7:0] value > 127).
This flag becomes 1 only when the REC[7:0] or TEC[7:0] value first exceeds 127. Therefore, if the program writes 0 to this flag while the value of REC[7:0] or TEC[7:0] remains over 127, this bit is not set to 1 until both REC [7:0] and TEC[7:0] values become 127 or less and then the REC[7:0] or TEC[7:0] value exceeds 127 again.

BOEF Flag (Bus Off Entry Flag)

This flag is set to 1 when the bus off state is reached (TEC[7:0] value > 255). This flag is also set to 1 if the bus off state is reached when the BOM[1:0] bits in the RSCAN0CmCTR register (m = 0, 1) set to 01b (transition to channel halt mode at bus off entry).

BORF Flag (Bus Off Recovery Flag)

This flag is set to 1 when 11 consecutive recessive bits have been detected 128 times and the CAN module returns from the bus off state. However, this flag is not set to 1 if the CAN module returns from the bus off state in any of the following ways before 11 consecutive recessive bits are detected 128 times.

- The CHMDC[1:0] bits in the RSCAN0CmCTR register are set to 01b (channel reset mode).
- The RTBO bit in the RSCAN0CmCTR register is set to 1 (forcible return from the bus off state is made).
- The BOM[1:0] bits in the RSCAN0CmCTR register are set to 01b (transition to channel halt mode at bus off entry).
- The CHMDC[1:0] bits in the RSCAN0CmCTR register are set to 10b (channel halt mode) before 11 consecutive recessive bits are detected 128 times with the BOM[1:0] bits set to 11b (transition to channel halt mode upon a request from the program during bus off).

OVLF Flag (Overload Flag)

This flag is set to 1 when the overload frame transmit condition has been detected when performing reception or transmission.

BLF Flag (Bus Lock Flag)

This flag is set to 1 when 32 consecutive dominant bits have been detected on the CAN bus in channel communication mode. After that, detection of a dominant lock is restarted when either of the following conditions is met.

- A recessive bit is detected after the BLF bit has been cleared from 1 to 0.
- The CAN module transitions to channel reset mode and returns to channel communication mode after the BLF bit has been cleared from 1 to 0.

ALF Flag (Arbitration-lost Flag)

This flag is set to 1 when an arbitration-lost has been detected.

SERR Flag (Stuff Error Flag)

This flag is set to 1 when a stuff error has been detected.

FERR Flag (Form Error Flag)

This flag is set to 1 when a form error has been detected.

AERR Flag (ACK Error Flag)

This flag is set to 1 when an ACK error has been detected.

CERR Flag (CRC Error Flag)

This flag is set to 1 when a CRC error has been detected.

B1ERR Flag (Recessive Bit Error Flag)

This flag is set to 1 when a dominant bit has been detected though a recessive bit was transmitted.

B0ERR Flag (Dominant Bit Error Flag)

This flag is set to 1 when a recessive bit has been detected though a dominant bit was transmitted.

ADERR Flag (ACK Delimiter Error Flag)

This flag is set to 1 when a form error has been detected in the ACK delimiter during transmission.

CRCREG[14:0] Flag (CRC Calculation Data)

When the CTME bit in the RSCAN0CmCTR register is set to 1 (communication test mode is enabled), the CRC value calculated based on the transmitted or received message can be read. When the CTME bit is set to 0 (communication test mode is disabled), these bits are always read as 0.

35.2.5 Global Configuration Register (RSCAN0GCFG)

The RSCAN0GCFG register controls the settings for the clock signals in the RSCAN module as a whole, interval timers, etc.

Modify the RSCAN0GCFG register in global reset mode.

Address(es): RSCAN.RSCAN0GCFG A007 8084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ITRCP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSBTCS[2:0]			TSSS	TSP[3:0]				—	—	—	DCS	MME	DRE	DCE	TPRI
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TPRI	Transmit Priority Select	0: ID priority 1: Transmission buffer number priority	R/W
b1	DCE	DLC Check Enable	0: DLC check is disabled. 1: DLC check is enabled.	R/W
b2	DRE	DLC Replacement Enable	0: DLC replacement is disabled. 1: DLC replacement is enabled.	R/W
b3	MME	Mirror Function Enable	0: Mirror function is disabled. 1: Mirror function is enabled.	R/W
b4	DCS	CAN Clock Source Select	0: CANCLKA (24 MHz) 1: CANCLKB (25 MHz)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	TSP[3:0]	Timestamp Clock Source Division	b11 b10 b9 b8 0 0 0 0: Not divided 0 0 0 1: Divided by 2 0 0 1 0: Divided by 4 0 0 1 1: Divided by 8 0 1 0 0: Divided by 16 0 1 0 1: Divided by 32 0 1 1 0: Divided by 64 0 1 1 1: Divided by 128 1 0 0 0: Divided by 256 1 0 0 1: Divided by 512 1 0 1 0: Divided by 1024 1 0 1 1: Divided by 2048 1 1 0 0: Divided by 4096 1 1 0 1: Divided by 8192 1 1 1 0: Divided by 16384 1 1 1 1: Divided by 32768	R/W
b12	TSSS	Timestamp Source Select	0: PCLKD (75 MHz)/2*1 1: Bit time clock (clock selected by the DCS bit)	R/W
b15 to b13	TSBTCS[2:0]	Timestamp Clock Source Select	b15 b14 b13 0 0 0: Channel 0 bit time clock 0 0 1: Channel 1 bit time clock Settings other than above are prohibited.	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b16	ITRCP[15:0]	Interval Timer Prescaler Set	When these bits are set to M, the PCLKD (75 MHz) is divided by M. Setting 0000h is prohibited when the interval timer is in use.	R/W

Note 1. When specifying PCLKD/2 as the timestamp counter count source, set bits TSBTCS[2:0] to 000b.

TPRI Bit (Transmit Priority Select)

This bit is used to set the transmit priority.
When this bit is set to 0, ID priority is selected and the transmit priority complies with the CAN bus arbitration rule (ISO11898-1 specifications). When this bit is set to 1, transmission buffer number priority is selected and the lowest transmission buffer number of those has the highest priority.
While the transmission queue is in use, this bit should be set to 0.

DCE Bit (DLC Check Enable)

Setting this bit to 1 makes the DLC check function available. When disabling the DLC check function, set the GAFLDLC[3:0] bits in the RSCAN0GAFLP0j register to 0000b before clearing the DCE bit in the RSCAN0GCFG register to 0.

DRE Bit (DLC Replacement Enable)

When the DRE bit is set to 1, the DLC value of the reception rule is stored in the buffer instead of the DLC value of the received message after the DLC value has passed through the DLC filter. In this case, a value of 00h is stored in each data byte beyond the DLC value of the reception rule.
The DLC replacement function is only available when the DCE bit is set to 1 (DLC check is enabled).

MME Bit (Mirror Function Enable)

Setting this bit to 1 makes the mirror function available.

DCS Bit (CAN Clock Source Select)

When this bit is set to 0, CANCLKA (24 MHz) is used as the clock source of the CAN clock (fCAN).
When this bit is set to 1, CANCLKB (25 MHz) is used as the clock source of the CAN clock (fCAN).

TSP[3:0] Bits (Timestamp Clock Source Division)

A clock obtained by dividing the clock source selected with the TSBTCS[2:0] bits and TSSS bit according to the TSP[3:0] bits is used as the timestamp counter count source.

TSSS Bit (Timestamp Source Select)

This bit is used to select a clock source of the timestamp counter.

TSBTCS[2:0] Bits (Timestamp Clock Source Select)

When the TSSS bit is 1, these bits are used to select the channel of the bit time clock that will be the clock source of the timestamp counter.

ITRCP[15:0] Bits (Interval Timer Prescaler Set)

These bits are used to set a clock source division value of the interval timer for FIFO buffers. See section 35.6.3.1, Interval Transmission Function.

35.2.6 Global Control Register (RSCAN0GCTR)

The RSCAN0GCTR register controls the operating mode of the RSCAN module and global interrupts.

Address(es): RSCAN.RSCAN0GCTR A007 8088h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TSRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	THLEIE	MEIE	DEIE	—	—	—	—	—	GSLPR	GMDC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	GMDC[1:0]	Global Mode Select	b1 b0 0 0: Global operating mode 0 1: Global reset mode 1 0: Global test mode Setting other than above is prohibited.	R/W
b2	GSLPR	Global Stop Mode	0: Other than global stop mode 1: Global stop mode	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DEIE	DLC Error Interrupt Enable	0: DLC error interrupt is disabled. 1: DLC error interrupt is enabled.	R/W
b9	MEIE	FIFO Message Lost Interrupt Enable	0: FIFO message lost interrupt is disabled. 1: FIFO message lost interrupt is enabled.	R/W
b10	THLEIE	Transmission History Buffer Overflow Interrupt Enable	0: Transmission history buffer overflow interrupt is disabled. 1: Transmission history buffer overflow interrupt is enabled.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	TSRST	Timestamp Counter Reset	Setting the TSRST bit to 1 resets the timestamp counter. This bit is always read as 0.	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GMDC[1:0] Bits (Global Mode Select)

These bits are used to select the mode of entire RSCAN module (global operating mode, global reset mode, or global test mode). For details, see section 35.4.1, Global Modes. Setting the GSLPR bit to 1 when in global reset mode places the RSCAN module into global stop mode.

GSLPR Bit (Global Stop Mode)

Setting this bit to 1 places the RSCAN module into global stop mode.
Clearing this bit to 0 makes the RSCAN module leave from global stop mode.
This bit should not be modified in global operating mode or global test mode.

DEIE Bit (DLC Error Interrupt Enable)

When the DEIE bit is set to 1 and the DEF flag in the RSCAN0GERFL register is set to 1, a CAN global error interrupt request (DLC error interrupt) is generated. Modify this bit in global reset mode.

MEIE Bit (FIFO Message Lost Interrupt Enable)

When the MEIE bit is set to 1 and the MES flag in the RSCAN0GERFL register is set to 1, a CAN global error interrupt request (FIFO message lost interrupt) is generated. Modify this bit in global reset mode.

THLEIE Bit (Transmission History Buffer Overflow Interrupt Enable)

When the THLEIE bit is set to 1 and the THLES flag in the RSCAN0GERFL register is set to 1, a CAN global error interrupt request (transmission history buffer overflow interrupt) is generated. Modify this bit in global reset mode.

TSRST Bit (Timestamp Counter Reset)

This bit is used to reset the timestamp counter. When this bit is set to 1, the RSCAN0GTSC register is cleared to 0000h.

35.2.7 Global Status Register (RSCAN0GSTS)

The RSCAN0GSTS register is a status register that indicates the operating state of the RSCAN module as a whole.

Address(es): RSCAN.RSCAN0GSTS A007 808Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	GRAMINIT	GSLPSTS	GHLTSTS	GRSTSTS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	GRSTSTS	Global Reset Status Flag	0: Not in global reset mode 1: In global reset mode	R
b1	GHLTSTS	Global Test Status Flag	0: Not in global test mode 1: In global test mode	R
b2	GSLPSTS	Global Stop Status Flag	0: Not in global stop mode 1: In global stop mode	R
b3	GRAMINIT	CAN RAM Initialization Status Flag	0: CAN RAM initialization is completed. 1: CAN RAM initialization is ongoing.	R
b31 to b4	—	Reserved	These bits are read as 0.	R

GRSTSTS Flag (Global Reset Status Flag)

This flag is set to 1 when the CAN module has transitioned to global reset mode, and is cleared to 0 when the CAN module has exited global reset mode. This flag remains 1 even when the CAN module has transitioned from global reset mode to global stop mode.

GHLTSTS Flag (Global Test Status Flag)

This flag is set to 1 when the CAN module has transitioned to global test mode, and is cleared to 0 when the CAN module has exited global test mode.

GSLPSTS Flag (Global Stop Status Flag)

This flag is set to 1 when the CAN module has transitioned to global stop mode, and is cleared to 0 when the CAN module has returned from global stop mode.

GRAMINIT Flag (CAN RAM Initialization Status Flag)

This flag indicates the initialization status of the CAN RAM.
This flag is set to 1 after the MCU has been reset, and is cleared to 0 when CAN RAM initialization is completed.

35.2.8 Global Error Flag Register (RSCAN0GERFL)

The RSCAN0GERFL register is a status register that indicates the error state of the RSCAN module as a whole.
All flags in the RSCAN0GERFL register are cleared to 0 in global reset mode.

Address(es): RSCAN.RSCAN0GERFL A007 8090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	THLES	MES	DEF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DEF	DLC Error Flag	0: No DLC error has occurred. 1: A DLC error has occurred.	R/W *1
b1	MES	FIFO Message Lost Status Flag	0: No FIFO message lost error has occurred. 1: A FIFO message lost error has occurred.	R
b2	THLES	Transmission History Buffer Overflow Status Flag	0: No transmission history buffer overflow has occurred. 1: A transmission history buffer overflow has occurred.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

DEF Flag (DLC Error Flag)

The DEF flag is set to 1 when an error has been detected during the DLC check. This flag can be cleared by writing 0 to it.

MES Flag (FIFO Message Lost Status Flag)

The MES flag is set to 1 when any one of the RFMLT flags in the RSCAN0RFSTSx register (x = 0 to 7) or the CFMLT flags in the RSCAN0CFSTSk register (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1) is set to 1.
This flag is cleared to 0 when all RFMLT flags and CFMLT flags are set to 0.

THLES Flag (Transmission History Buffer Overflow Status Flag)

The THLES flag is set to 1 when any one of the THLELT flags in the RSCAN0THLSTSm register (m = 0, 1) is set to 1.
This flag is cleared to 0 when the THLELT flags of all channels are set to 0.

35.2.9 Global TX Interrupt Status Register 0 (RSCAN0GTINTSTS0)

The RSCAN0GTINTSTS0 register is a status register that indicates the state of interrupts in CANm transmission by the RSCAN module (m = 0, 1).

Address(es): RSCAN.RSCAN0GTINTSTS0 A007 8460h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	THIF1	CFTIF1	TQIF1	TAIF1	TSIF1	—	—	—	THIF0	CFTIF0	TQIF0	TAIF0	TSIF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSIF0	Channel 0 Transmission Buffer Interrupt Status Flag	0: Transmission buffer transmission complete interrupt is not requested. 1: Transmission buffer transmission complete interrupt is requested.	R*1
b1	TAIF0	Channel 0 Transmission Buffer Transmission Abort Interrupt Status Flag	0: Transmission buffer transmission abort interrupt is not requested. 1: Transmission buffer transmission abort interrupt is requested.	R*1
b2	TQIF0	Channel 0 Transmission Queue Interrupt Status Flag	0: Transmission queue interrupt is not requested. 1: Transmission queue interrupt is requested.	R*1
b3	CFTIF0	Channel 0 Transmit/Receive FIFO Transmit Interrupt Status Flag	0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.	R*1
b4	THIF0	Channel 0 Transmission History Interrupt Status Flag	0: Transmission history interrupt is not requested. 1: Transmission history interrupt is requested.	R*1
b7 to b5	—	Reserved	These bits are read as 0.	R
b8	TSIF1	Channel 1 Transmission Buffer Interrupt Status Flag	0: Transmission buffer transmission complete interrupt is not requested. 1: Transmission buffer transmission complete interrupt is requested.	R*1
b9	TAIF1	Channel 1 Transmission Buffer Transmission Abort Interrupt Status Flag	0: Transmission buffer transmission abort interrupt is not requested. 1: Transmission buffer transmission abort interrupt is requested.	R*1
b10	TQIF1	Channel 1 Transmission Queue Interrupt Status Flag	0: Transmission queue interrupt is not requested. 1: Transmission queue interrupt is requested.	R*1
b11	CFTIF1	Channel 1 Transmit/Receive FIFO Transmit Interrupt Status Flag	0: Transmit/receive FIFO transmit interrupt is not requested. 1: Transmit/receive FIFO transmit interrupt is requested.	R*1
b12	THIF1	Channel 1 Transmission History Interrupt Status Flag	0: Transmission history interrupt is not requested. 1: Transmission history interrupt is requested.	R*1
b31 to b13	—	Reserved	These bits are read as 0.	R

Note 1. This bit is automatically cleared in the global reset or channel reset mode.

TSIFm Bits (Channel m Transmission Buffer Interrupt Status Flag) (m = 0, 1)

The TSIFm bit is set to 1 when the TMIE bit in the RSCAN0TMIEC0 register is set to 1 (transmission buffer interrupt enabled) and the TMTRF[1:0] flag in the RCAN0TMSTSp (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1) register are set to 10b (transmission completed without abort request) or 11b (transmission completed with abort request).
When the TMTRF[1:0] flag are cleared to 00b under the condition that the TSIFm bit can be set to 1, this flag is cleared to 0. In addition, clearing the TMIE bit to 0 also clears this flag to 0.

TAIFm Bits (Channel m Transmission Buffer Transmission Abort Interrupt Status Flag) (m = 0, 1)

The TAIFm bit is set to 1 when the TAIE bit in the RSCAN0CmCTR register is 1 (transmission abort interrupt enabled) and the TMTRF[1:0] flag in the RCAN0TMSTSp (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1) register are set to 01b (transmission abort completed).
This flag is cleared to 0 when the TMTRF[1:0] flag are cleared to 00b after the transmission abort is completed.

TQIFm Bits (Channel m Transmission Queue Interrupt Status Flag) (m = 0, 1)

When the TXQIE bit in the RSCAN0TXQCCm register is set to 1 (transmission queue interrupt enabled) and the TXQIF bit in the RSCAN0TXQSTSm register is set to 1 (transmission queue interrupt request), the TQIFm bit is set to 1.
When the TXQIF bit (transmission queue interrupt request) in the RSCAN0TXQSTSm register is cleared to 0, this bit is cleared to 0. This flag is also cleared to 0 when the TXQIE bit is cleared to 0.

CFTIFm Bits (Channel m Transmit/Receive FIFO Transmit Interrupt Status Flag) (m = 0, 1)

When the CFTXIE bit in the RSCAN0CFCCk register is set to 1 (transmit/receive FIFO transmit interrupt enabled) and the CFTXIF bit in the RSCAN0CFSTSk (k = 0 to 2 for channel 0; p = 3 to 5 for channel 1) register is set to 1 (transmit/receive FIFO transmit interrupt request), the CFTIFm bit is set to 1.
When the CFTXIF bit is cleared to 0 under the conditions that the CFTIFm bit can be set to 1, this bit is cleared to 0. This flag is also cleared to 0 when the CFTXIE bit is cleared to 0.

THIFm Bits (Channel m Transmission History Interrupt Status Flag) (m = 0, 1)

When the THLIE bit in the RSCAN0THLCCm register is set to 1 (transmission history interrupt enabled) and the THLIF bit in the RSCAN0THLSTSm register is set to 1 (transmission history interrupt request), the THIFm bit is set to 1.
When the THLIF bit in the RSCAN0THLSTSm register is cleared to 0, this bit is cleared to 0. This flag is also cleared to 0 when the THLIE bit is cleared to 0.

35.2.10 Global Timestamp Counter Register (RSCAN0GTSC)

The RSCAN0GTSC register is a 32-bit counter that indicates the timestamp counter value.

Address(es): RSCAN.RSCAN0GTSC A007 8094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TS[15:0]	Timestamp Value	The timestamp counter value can be read. Counter Value: 0000h to FFFFh	R
b31 to b16	—	Reserved	These bits are read as 0.	R

TS[15:0] Bits (Timestamp Value)

When the TS[15:0] bits are read, the read value shows the timestamp counter (16-bit free-running counter) value at that time. When the SOF is detected, the TS[15:0] value is captured and later stored in the reception buffer or the FIFO buffer. The timestamp counter is initialized in global reset mode.

The timestamp counter starts and stops counting differently, depending on the count source.

- When the TSSS bit in the RSCAN0GCFG register is 0 (PCLKD/2):
  The timestamp counter starts counting when the RSCAN module has transitioned to global operating mode.
  This counter stops counting when the RSCAN module has transitioned to global stop mode or global test mode.
- When the TSSS bit is 1 (CANm bit time clock):
  The timestamp counter starts counting when the corresponding channel has transitioned to channel communication mode.
  This counter stops counting when the corresponding channel has transitioned to channel reset mode or channel halt mode.

35.2.11 Reception Rule Entry Control Register (RSCAN0GAFLECTR)

The RSCAN0GAFLECTR register controls the reception rule table.

Address(es): RSCAN.RSCAN0GAFLECTR A007 8098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	AFLDAE	—	—	—	AFLPN[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	AFLPN[4:0]	Reception Rule Table Page Number Configuration	A page number can be selected from a range of page 0 (00000b) to page 7 (00111b).	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	AFLDAE	Reception Rule Table Write Enable	0: Writing to the reception rule table is disabled. 1: Writing to the reception rule table is enabled.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

AFLPN[4:0] Bits (Reception Rule Table Write Enable)

These bits are used to set the page number of the reception rule table. Sixteen reception rules can be set per page.
Set these bits to a value within the range of 00000b to 00111b.

AFLDAE Bit (Reception Rule Table Page Number Configuration)

Setting this bit to 0 disables writing to the reception rule table. After writes to the reception rule table are completed, set this bit to 0 to disable writing to the table. The reception rule table can be read regardless of the value of this bit.
Set the AFLDAE bit to 1 only in global reset mode.

35.2.12 Reception Rule Configuration Register 0 (RSCAN0GAFLCFG0)

The RSCAN0GAFLCFG0 register controls the settings for the number of reception rules for each channel.
Modify the RSCAN0GAFLCFG0 register in global reset mode.
Up to 64 × (number of channels) rules can be registered in the reception rule table as the entire unit. The number of reception rules per channel should meet the following conditions.

- The maximum number of rules per channel is 128.
- The total of the number of rules allocated to each channel does not exceed 128 rules that can be registered in the entire unit.

Address(es): RSCAN.RSCAN0GAFLCFG0 A007 809Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RNC0[7:0]								RNC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23 to b16	RNC1[7:0]	Channel 1 Rule Number Set	Set the number of reception rules exclusively used for channel 1.	R/W
b31 to b24	RNC0[7:0]	Channel 0 Rule Number Set	Set the number of reception rules exclusively used for channel 0.	R/W

RNC1[7:0] Bits (Channel 1 Rule Number Set)

These bits are used to set the number of rules to be registered in the channel 1 reception rule table.
Set these bits to a value within the range of 00h to 80h.

RNC0[7:0] Bits (Channel 0 Rule Number Set)

These bits are used to set the number of rules to be registered in the channel 0 reception rule table.
Set these bits to a value within the range of 00h to 80h.

35.2.13 Reception Rule ID Register (RSCAN0GAFLIDj) (j = 0 to 15)

The RSCAN0GAFLIDj registers control the ID and frame formats of the reception rule.
Modify the RSCAN0GAFLIDj registers when the AFLDAE bit in the RSCAN0GAFLECTR register is set to 1 (enabling writing to the reception rule table) in global reset mode.

Address(es): RSCAN.RSCAN0GAFLID0 A007 8500h, RSCAN.RSCAN0GAFLID1 A007 8510h, RSCAN.RSCAN0GAFLID2 A007 8520h, RSCAN.RSCAN0GAFLID3 A007 8530h, RSCAN.RSCAN0GAFLID4 A007 8540h, RSCAN.RSCAN0GAFLID5 A007 8550h, RSCAN.RSCAN0GAFLID6 A007 8560h, RSCAN.RSCAN0GAFLID7 A007 8570h, RSCAN.RSCAN0GAFLID8 A007 8580h, RSCAN.RSCAN0GAFLID9 A007 8590h, RSCAN.RSCAN0GAFLID10 A007 85A0h, RSCAN.RSCAN0GAFLID11 A007 85B0h, RSCAN.RSCAN0GAFLID12 A007 85C0h, RSCAN.RSCAN0GAFLID13 A007 85D0h, RSCAN.RSCAN0GAFLID14 A007 85E0h, RSCAN.RSCAN0GAFLID15 A007 85F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	GAFLIDE	GAFLRTR	GAFLLB	GAFLID[28:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLID[28:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b28 to b0	GAFLID[28:0]	ID Configuration	Set the ID of the reception rule. For the standard ID, set the ID in bits b10 to b0 and set bits b28 to b11 to 0.	R/W
b29	GAFLLB	Reception Rule Target Message Select	0: When a message transmitted from another CAN node is received 1: When the own transmitted message is received	R/W
b30	GAFLRTR	RTR Select	0: Data frame 1: Remote frame	R/W
b31	GAFLIDE	IDE Select	0: Standard ID 1: Extended ID	R/W

GAFLID[28:0] Bits (ID Configuration)

These bits are used to set the ID field of the reception rule. The ID value set by these bits is compared with the ID of the received message during the acceptance filter processing.

GAFLLB Bit (Reception Rule Target Message Select)

When this bit is set to 0, data processing using the reception rule is performed when receiving messages transmitted from another CAN node.
When this bit is set to 1 when the mirror function is used, data processing using the reception rule is performed when the CAN node is receiving its own transmitted messages.

GAFLRTR Bit (RTR Select)

This bit is used to select the frame format (data frame or remote frame) of the reception rule. This bit is compared with the RTR bit in the received message during the acceptance filter processing.

GAFLIDE Bit (IDE Select)

This bit is used to select the ID format (standard ID or extended ID) of the reception rule. This bit is compared with the IDE bit in the received message during the acceptance filter processing.

35.2.14 Reception Rule Mask Registers (RSCAN0GAFLMj) (j = 0 to 15)

The RSCAN0GAFLMj registers control the settings for masking of the reception rule.
Modify the RSCAN0GAFLMj registers when the AFLDAE bit in the RSCAN0GAFLECTR register is set to 1 (enabling writing to the reception rule table) in global reset mode.

Address(es): RSCAN.RSCAN0GAFLM0 A007 8504h, RSCAN.RSCAN0GAFLM1 A007 8514h, RSCAN.RSCAN0GAFLM2 A007 8524h, RSCAN.RSCAN0GAFLM3 A007 8534h, RSCAN.RSCAN0GAFLM4 A007 8544h, RSCAN.RSCAN0GAFLM5 A007 8554h, RSCAN.RSCAN0GAFLM6 A007 8564h, RSCAN.RSCAN0GAFLM7 A007 8574h, RSCAN.RSCAN0GAFLM8 A007 8584h, RSCAN.RSCAN0GAFLM9 A007 8594h, RSCAN.RSCAN0GAFLM10 A007 85A4h, RSCAN.RSCAN0GAFLM11 A007 85B4h, RSCAN.RSCAN0GAFLM12 A007 85C4h, RSCAN.RSCAN0GAFLM13 A007 85D4h, RSCAN.RSCAN0GAFLM14 A007 85E4h, RSCAN.RSCAN0GAFLM15 A007 85F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	GAFLIDEM	GAFLRTRM	—	GAFLIDM[28:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLIDM[28:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b28 to b0	GAFLIDM [28:0]	ID Mask	0: The corresponding ID bit is not compared. 1: The corresponding ID bit is compared.	R/W
b29	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30	GAFLRTRM	RTR Mask	0: The RTR bit is not compared. 1: The RTR bit is compared	R/W
b31	GAFLIDEM	IDE Mask	0: The IDE bit is not compared. 1: The IDE bit is compared.	R/W

GAFLIDM[28:0] Bits (ID Mask)

These bits are used to mask the corresponding ID bit of the reception rule.

GAFLRTRM Bit (RTR Mask)

This bit is used to mask the RTR bit of the reception rule.

GAFLIDEM Bit (IDE Mask)

When this bit is set to 1, filter processing is performed only for messages of the ID format specified by the GAFLIDE bit in the RSCAN0GAFLIDj register.
When this bit is cleared to 0, the IDs of all the received messages and the specified IDs are regarded as matched. To set the GAFLIDEM bit to 0, set the GAFLIDM[28:0] bits to all 0 at the same time.

35.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j) (j = 0 to 15)

The RSCAN0GAFLP0j registers control the minimum data length and labels for received messages and the settings for the reception buffer.

Modify the RSCAN0GAFLP0j registers when the AFLDAE bit in the RSCAN0GAFLECTR register is set to 1 (enabling writing to the reception rule table) in global reset mode.

Address(es): RSCAN.RSCAN0GAFLP00 A007 8508h, RSCAN.RSCAN0GAFLP01 A007 8518h, RSCAN.RSCAN0GAFLP02 A007 8528h, RSCAN.RSCAN0GAFLP03 A007 8538h, RSCAN.RSCAN0GAFLP04 A007 8548h, RSCAN.RSCAN0GAFLP05 A007 8558h, RSCAN.RSCAN0GAFLP06 A007 8568h, RSCAN.RSCAN0GAFLP07 A007 8578h, RSCAN.RSCAN0GAFLP08 A007 8588h, RSCAN.RSCAN0GAFLP09 A007 8598h, RSCAN.RSCAN0GAFLP010 A007 85A8h, RSCAN.RSCAN0GAFLP011 A007 85B8h, RSCAN.RSCAN0GAFLP012 A007 85C8h, RSCAN.RSCAN0GAFLP013 A007 85D8h, RSCAN.RSCAN0GAFLP014 A007 85E8h, RSCAN.RSCAN0GAFLP015 A007 85F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	GAFLDLC[3:0]				GAFLPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLRMV	GAFLRMDP[6:0]							—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14 to b8	GAFLRMDP [6:0]	Reception Buffer Number Select	Set the reception buffer number to store received messages.	R/W
b15	GAFLRMV	Reception Buffer Enable	0: No reception buffer is used. 1: A reception buffer is used.	R/W
b27 to b16	GAFLPTR [11:0]	Reception Rule Label	Set the 12-bit label information.	R/W
b31 to b28	GAFLDLC [3:0]	Reception Rule DLC	b31 b30 b29 b28 0 0 0 0: DLC check is disabled. 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 X X X: 8 data bytes	R/W

GAFLRMDP[6:0] Bits (Reception Buffer Number Select)

These bits are used to select the number of the reception buffer that stores received messages that have passed through the filter when the GAFLRMV bit is set to 1. Set these bits to a value smaller than the value set by the NRXMB[7:0] bits in the RSCAN0RMNB register.

GAFLRMV Bit (Reception Buffer Enable)

When this bit is set to 1, received messages that have passed through the filter are stored in the reception buffer selected by the GAFLRMDP[6:0] bits.

GAFLPTR[11:0] Bits (Reception Rule Label)

These bits are used to set a 12-bit label to be attached to messages that have passed through the filter. A label is attached when a message is stored in the reception buffer or the FIFO buffer.

GAFLDLC[3:0] Bits (Reception Rule DLC)

These bits are used to set the minimum data length necessary for receiving messages. If the data length of a message that is being filtered is equal to or larger than the value set by the GAFLDLC[3:0] bits, the message passes the DLC check. Setting these bits to 0000b disables the DLC check function allowing messages with any data length to pass the DLC check.

35.2.16 Reception Rule Pointer 1 Registers (RSCAN0GAFLP1j) (j = 0 to 15)

The RSCAN0GAFLP1j registers control the settings for the FIFO buffers for storing received messages that have passed through the filter.

Modify the RSCAN0GAFLP1j registers when the AFLDAE bit in the RSCAN0GAFLECTR register is set to 1 (enabling writing to the reception rule table) in global reset mode.

Address(es): RSCAN.RSCAN0GAFLP10 A007 850Ch, RSCAN.RSCAN0GAFLP11 A007 851Ch, RSCAN.RSCAN0GAFLP12 A007 852Ch, RSCAN.RSCAN0GAFLP13 A007 853Ch, RSCAN.RSCAN0GAFLP14 A007 854Ch, RSCAN.RSCAN0GAFLP15 A007 855Ch, RSCAN.RSCAN0GAFLP16 A007 856Ch, RSCAN.RSCAN0GAFLP17 A007 857Ch, RSCAN.RSCAN0GAFLP18 A007 858Ch, RSCAN.RSCAN0GAFLP19 A007 859Ch, RSCAN.RSCAN0GAFLP110 A007 85ACh, RSCAN.RSCAN0GAFLP111 A007 85BCh, RSCAN.RSCAN0GAFLP112 A007 85CCh, RSCAN.RSCAN0GAFLP113 A007 85DCh, RSCAN.RSCAN0GAFLP114 A007 85ECh, RSCAN.RSCAN0GAFLP115 A007 85FCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	GAFLFDP[17:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GAFLFDP[17:0]								GAFLFDPr[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	GAFLFDPr [7:0]	Reception FIFO Buffer x Select	(Bit position = target reception FIFO buffer number x) 0: Reception FIFO buffer is not selected. 1: Reception FIFO buffer is selected.	R/W
b25 to b8	GAFLFDP [17:0]	Transmission/Reception FIFO Buffer k Select	(Bit position – 8 = target transmission/reception FIFO buffer number k) 0: Transmission/reception FIFO buffer is not selected. 1: Transmission/reception FIFO buffer is selected.	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GAFLFDP[17:0] and GAFLFDPr[7:0] Bits

These bits are used to specify FIFO buffers for storing received messages that have passed through the filter. Up to eight FIFO buffers are selectable. However, when the GAFLRMV bit in the RSCAN0GAFLP0j (j = 0 to 15) register is set to 1 (storing a message in the reception buffer), up to seven FIFO buffers can be selected. Only reception FIFO buffers and the transmission/reception FIFO buffer for which the CFM[1:0] bits in the RSCAN0CFCCk (k = 0 to 5) register are set to 00b (receive mode) or 10b (gateway mode) are selectable.

35.2.17 Reception Buffer Number Register (RSCAN0RMNB)

The RSCAN0RMNB register controls the number of reception buffers of the RSCAN module.
Modify the RSCAN0RMNB register in global reset mode.

Address(es): RSCAN.RSCAN0RMNB A007 80A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	NRXMB[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	NRXMB[7:0]	Reception Buffer Number Configuration	Set the number of reception buffers. Set a value between 0 to 32.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NRXMB[7:0] Bits (Reception Buffer Number Configuration)

These bits are used to set the total number of reception buffers of the RSCAN module. The maximum value is 32 (16 for each channel).
Setting these bits all to 0 makes reception buffers unavailable.

35.2.18 Reception Buffer New Data Register 0 (RSCAN0RMND0)

The RSCAN0RMND0 register is a status register that indicates completion of the reception of messages by the reception buffer.

Write 0 to the RSCAN0RMND0 register in global operating mode or global test mode.

Address(es): RSCAN.RSCAN0RMND0 A007 80A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RMNSq_h (q = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMNSq_l (q = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RMNSq_l	Reception Buffer Reception Complete Flag q_l (q = 15 to 0)	0: There is no new message in reception buffer q. 1: There is a new message in reception buffer q.	R/W
b31 to b16	RMNSq_h	Reception Buffer Reception Complete Flag q _h(q = 31 to 16)	0: There is no new message in reception buffer q. 1: There is a new message in reception buffer q.	R/W

RMNSq_l, RMNSq_h Flags (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1)

Each RMNS flag is set to 1 when the processing for storing a message in the corresponding reception buffer starts.

To clear a flag to 0, the program must write 0 to the flag. Use a store instruction to write “0” to the flag and “1” to other flags. These bits cannot be set to 0 while a message is being stored. It takes ten clock cycles of PCLKD to store a message.

These flags are cleared to 0 in global reset mode.

35.2.19 Reception Buffer ID Registers (RSCAN0RMIDq) (q = 0 to 31)

The RSCAN0RMIDq registers are status registers that indicate the state of the ID and frame formats of the messages stored in the reception buffers (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1).

Address(es): RSCAN.RSCAN0RMID0 A007 8600h, RSCAN.RSCAN0RMID1 A007 8610h, RSCAN.RSCAN0RMID2 A007 8620h, RSCAN.RSCAN0RMID3 A007 8630h, RSCAN.RSCAN0RMID4 A007 8640h, RSCAN.RSCAN0RMID5 A007 8650h, RSCAN.RSCAN0RMID6 A007 8660h, RSCAN.RSCAN0RMID7 A007 8670h, RSCAN.RSCAN0RMID8 A007 8680h, RSCAN.RSCAN0RMID9 A007 8690h, RSCAN.RSCAN0RMID10 A007 86A0h, RSCAN.RSCAN0RMID11 A007 86B0h, RSCAN.RSCAN0RMID12 A007 86C0h, RSCAN.RSCAN0RMID13 A007 86D0h, RSCAN.RSCAN0RMID14 A007 86E0h, RSCAN.RSCAN0RMID15 A007 86F0h, RSCAN.RSCAN0RMID16 A007 8700h, RSCAN.RSCAN0RMID17 A007 8710h, RSCAN.RSCAN0RMID18 A007 8720h, RSCAN.RSCAN0RMID19 A007 8730h, RSCAN.RSCAN0RMID20 A007 8740h, RSCAN.RSCAN0RMID21 A007 8750h, RSCAN.RSCAN0RMID22 A007 8760h, RSCAN.RSCAN0RMID23 A007 8770h, RSCAN.RSCAN0RMID24 A007 8780h, RSCAN.RSCAN0RMID25 A007 8790h, RSCAN.RSCAN0RMID26 A007 87A0h, RSCAN.RSCAN0RMID27 A007 87B0h, RSCAN.RSCAN0RMID28 A007 87C0h, RSCAN.RSCAN0RMID29 A007 87D0h, RSCAN.RSCAN0RMID30 A007 87E0h, RSCAN.RSCAN0RMID31 A007 87F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RMIDE	RMRTR	—	RMID[28:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMID[28:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b28 to b0	RMID[28:0]	Reception Buffer ID Data	These bits contain the standard ID or extended ID of the received messages. Read bits b10 to b0 for standard ID. Bits b28 to b11 are read as 0.	R
b29	—	Reserved	This bit is read as 0.	R
b30	RMRTR	Reception Buffer RTR	0: Data frame 1: Remote frame	R
b31	RMIDE	Reception Buffer IDE	0: Standard ID 1: Extended ID	R

RMID[28:0] Bits (Reception Buffer ID Data)

These bits contain the ID of the messages stored in the reception buffers.

RMRTR Bit (Reception Buffer RTR)

This bit indicates the frame format (data frame or remote frame) of the messages stored in the reception buffers.

RMIDE Bit (Reception Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the messages stored in the reception buffers.

35.2.20 Reception Buffer Pointer Registers (RSCAN0RMPTRq) (q = 0 to 31)

The RSCAN0RMPTRq registers are status registers that indicate the data length, label information, and timestamp value of the messages stored in the reception buffers (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1).

Address(es): RSCAN.RSCAN0RMPTR0 A007 8604h, RSCAN.RSCAN0RMPTR1 A007 8614h, RSCAN.RSCAN0RMPTR2 A007 8624h, RSCAN.RSCAN0RMPTR3 A007 8634h, RSCAN.RSCAN0RMPTR4 A007 8644h, RSCAN.RSCAN0RMPTR5 A007 8654h, RSCAN.RSCAN0RMPTR6 A007 8664h, RSCAN.RSCAN0RMPTR7 A007 8674h, RSCAN.RSCAN0RMPTR8 A007 8684h, RSCAN.RSCAN0RMPTR9 A007 8694h, RSCAN.RSCAN0RMPTR10 A007 86A4h, RSCAN.RSCAN0RMPTR11 A007 86B4h, RSCAN.RSCAN0RMPTR12 A007 86C4h, RSCAN.RSCAN0RMPTR13 A007 86D4h, RSCAN.RSCAN0RMPTR14 A007 86E4h, RSCAN.RSCAN0RMPTR15 A007 86F4h, RSCAN.RSCAN0RMPTR16 A007 8704h, RSCAN.RSCAN0RMPTR17 A007 8714h, RSCAN.RSCAN0RMPTR18 A007 8724h, RSCAN.RSCAN0RMPTR19 A007 8734h, RSCAN.RSCAN0RMPTR20 A007 8744h, RSCAN.RSCAN0RMPTR21 A007 8754h, RSCAN.RSCAN0RMPTR22 A007 8764h, RSCAN.RSCAN0RMPTR23 A007 8774h, RSCAN.RSCAN0RMPTR24 A007 8784h, RSCAN.RSCAN0RMPTR25 A007 8794h, RSCAN.RSCAN0RMPTR26 A007 87A4h, RSCAN.RSCAN0RMPTR27 A007 87B4h, RSCAN.RSCAN0RMPTR28 A007 87C4h, RSCAN.RSCAN0RMPTR29 A007 87D4h, RSCAN.RSCAN0RMPTR30 A007 87E4h, RSCAN.RSCAN0RMPTR31 A007 87F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RMDLC[3:0]				RMPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RMTS[15:0]	Reception Buffer Timestamp Data	Timestamp value of the received messages	R
b27 to b16	RMPTR[11:0]	Reception Buffer Label Data	Label information of the received messages	R
b31 to b28	RMDLC[3:0]	Reception Buffer DLC Data	b31 b30 b29 b28 0 0 0 0: No data byte 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 X X X: 8 data bytes	R

RMTS[15:0] Bits (Reception Buffer Timestamp Data)

These bits indicate the timestamp value of the message stored in the reception buffer.

RMPTR[11:0] Bits (Reception Buffer Label Data)

These bits indicate the label information of the message stored in the reception buffer.

RMDLC[3:0] Bits (Reception Buffer DLC Data)

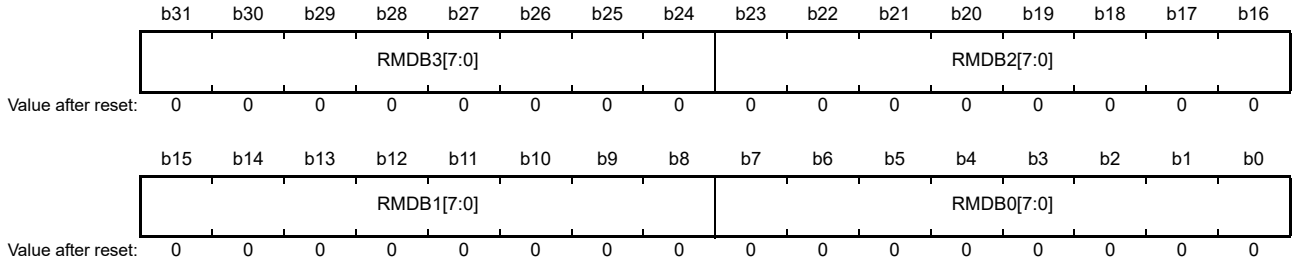
These bits indicate the data length of the message stored in the reception buffer.

35.2.21 Reception Buffer Data Field 0 Registers (RSCAN0RMDF0q) (q = 0 to 31)

The RSCAN0RMDF0q registers are data registers that hold the values in the reception buffers (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1).

When the value of the RMDLC[3:0] bits in the RSCAN0RMPTRq register is less than 1000b, data bytes for which no value is set are read as 00h.

Address(es): RSCAN.RSCAN0RMDF00 A007 8608h, RSCAN.RSCAN0RMDF01 A007 8618h, RSCAN.RSCAN0RMDF02 A007 8628h, RSCAN.RSCAN0RMDF03 A007 8638h, RSCAN.RSCAN0RMDF04 A007 8648h, RSCAN.RSCAN0RMDF05 A007 8658h, RSCAN.RSCAN0RMDF06 A007 8668h, RSCAN.RSCAN0RMDF07 A007 8678h, RSCAN.RSCAN0RMDF08 A007 8688h, RSCAN.RSCAN0RMDF09 A007 8698h, RSCAN.RSCAN0RMDF010 A007 86A8h, RSCAN.RSCAN0RMDF011 A007 86B8h, RSCAN.RSCAN0RMDF012 A007 86C8h, RSCAN.RSCAN0RMDF013 A007 86D8h, RSCAN.RSCAN0RMDF014 A007 86E8h, RSCAN.RSCAN0RMDF015 A007 86F8h, RSCAN.RSCAN0RMDF016 A007 8708h, RSCAN.RSCAN0RMDF017 A007 8718h, RSCAN.RSCAN0RMDF018 A007 8728h, RSCAN.RSCAN0RMDF019 A007 8738h, RSCAN.RSCAN0RMDF020 A007 8748h, RSCAN.RSCAN0RMDF021 A007 8758h, RSCAN.RSCAN0RMDF022 A007 8768h, RSCAN.RSCAN0RMDF023 A007 8778h, RSCAN.RSCAN0RMDF024 A007 8788h, RSCAN.RSCAN0RMDF025 A007 8798h, RSCAN.RSCAN0RMDF026 A007 87A8h, RSCAN.RSCAN0RMDF027 A007 87B8h, RSCAN.RSCAN0RMDF028 A007 87C8h, RSCAN.RSCAN0RMDF029 A007 87D8h, RSCAN.RSCAN0RMDF030 A007 87E8h, RSCAN.RSCAN0RMDF031 A007 87F8h



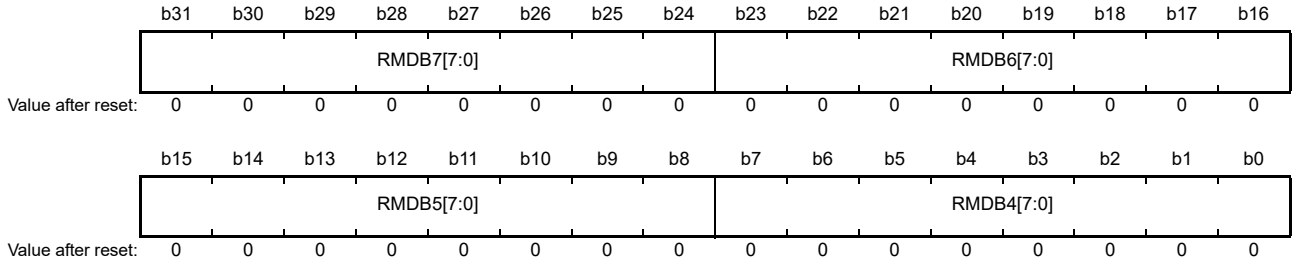
Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB0[7:0]	Reception Buffer Data Byte 0	Values of messages stored in the corresponding reception buffer can be read from these bits.	R
b15 to b8	RMDB1[7:0]	Reception Buffer Data Byte 1		R
b23 to b16	RMDB2[7:0]	Reception Buffer Data Byte 2		R
b31 to b24	RMDB3[7:0]	Reception Buffer Data Byte 3		R

35.2.22 Reception Buffer Data Field 1 Registers (RSCAN0RMDF1q) (q = 0 to 31)

The RSCAN0RMDF1q registers are data registers that hold the values in the reception buffers (q = 0 to 15 for channel 0; q = 16 to 31 for channel 1).

When the value of the RMDLC[3:0] bits in the RSCAN0RMPTRq register is less than 1000b, data bytes for which no value is set are read as 00h.

Address(es): RSCAN.RSCAN0RMDF10 A007 860Ch, RSCAN.RSCAN0RMDF11 A007 861Ch, RSCAN.RSCAN0RMDF12 A007 862Ch, RSCAN.RSCAN0RMDF13 A007 863Ch, RSCAN.RSCAN0RMDF14 A007 864Ch, RSCAN.RSCAN0RMDF15 A007 865Ch, RSCAN.RSCAN0RMDF16 A007 866Ch, RSCAN.RSCAN0RMDF17 A007 867Ch, RSCAN.RSCAN0RMDF18 A007 868Ch, RSCAN.RSCAN0RMDF19 A007 869Ch, RSCAN.RSCAN0RMDF110 A007 86ACh, RSCAN.RSCAN0RMDF111 A007 86BCh, RSCAN.RSCAN0RMDF112 A007 86CCh, RSCAN.RSCAN0RMDF113 A007 86DCh, RSCAN.RSCAN0RMDF114 A007 86ECh, RSCAN.RSCAN0RMDF115 A007 86FCh, RSCAN.RSCAN0RMDF116 A007 870Ch, RSCAN.RSCAN0RMDF117 A007 871Ch, RSCAN.RSCAN0RMDF118 A007 872Ch, RSCAN.RSCAN0RMDF119 A007 873Ch, RSCAN.RSCAN0RMDF120 A007 874Ch, RSCAN.RSCAN0RMDF121 A007 875Ch, RSCAN.RSCAN0RMDF122 A007 876Ch, RSCAN.RSCAN0RMDF123 A007 877Ch, RSCAN.RSCAN0RMDF124 A007 878Ch, RSCAN.RSCAN0RMDF125 A007 879Ch, RSCAN.RSCAN0RMDF126 A007 87ACh, RSCAN.RSCAN0RMDF127 A007 87BCh, RSCAN.RSCAN0RMDF128 A007 87CCh, RSCAN.RSCAN0RMDF129 A007 87DCh, RSCAN.RSCAN0RMDF130 A007 87ECh, RSCAN.RSCAN0RMDF131 A007 87FCh



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RMDB4[7:0]	Reception Buffer Data Byte 4	Values of messages stored in the corresponding reception buffer can be read from these bits.	R
b15 to b8	RMDB5[7:0]	Reception Buffer Data Byte 5		R
b23 to b16	RMDB6[7:0]	Reception Buffer Data Byte 6		R
b31 to b24	RMDB7[7:0]	Reception Buffer Data Byte 7		R

35.2.23 Reception FIFO Buffer Configuration and Control Registers (RSCAN0RFCCx) (x = 0 to 7)

The RSCAN0RFCCx registers control reception FIFO buffer interrupts and the number of reception FIFO buffer stages.

Address(es): RSCAN.RSCAN0RFCC0 A007 80B8h, RSCAN.RSCAN0RFCC1 A007 80BCh, RSCAN.RSCAN0RFCC2 A007 80C0h, RSCAN.RSCAN0RFCC3 A007 80C4h, RSCAN.RSCAN0RFCC4 A007 80C8h, RSCAN.RSCAN0RFCC5 A007 80CCh, RSCAN.RSCAN0RFCC6 A007 80D0h, RSCAN.RSCAN0RFCC7 A007 80D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFIGCV[2:0]			RFIM	—	RFDC[2:0]			—	—	—	—	—	—	RFIE	RFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RFE	Reception FIFO Buffer Enable	0: No reception FIFO buffer is used. 1: Reception FIFO buffers are used.	R/W
b1	RFIE	Receive FIFO Interrupt Enable	0: Receive FIFO interrupt is disabled. 1: Receive FIFO interrupt is enabled.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	RFDC[2:0]	Reception FIFO Buffer Depth Configuration	b10 b9 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: 128 messages	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	RFIM	Receive FIFO Interrupt Source Select	0: An interrupt occurs when the condition set by the RFIGCV[2:0] bits is met. 1: An interrupt occurs each time a message has been received.	R/W
b15 to b13	RFIGCV[2:0]	Receive FIFO Interrupt Request Timing Select	b15 b14 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RFE Bit (Reception FIFO Buffer Enable)

Setting the RFE bit to 1 makes reception FIFO buffers available. Clearing this bit to 0 sets the RFEMP flag in the RSCAN0RFSTSx register to 1 (buffer empty). Modify this bit in global operating mode or global test mode.

RFIE Bit (Receive FIFO Interrupt Enable)

Setting the RFIE bit to 1 enables receive FIFO interrupts. Modify this bit when the RFE bit set to 0 (no reception FIFO buffer is used).

RFDC[2:0] Bits (Reception FIFO Buffer Depth Configuration)

These bits are used to select the number of messages that can be stored in a single reception FIFO buffer. When these bits are set to 000b, no reception FIFO buffer should be used. Modify these bits only in global reset mode.

RFIM Bit (Receive FIFO Interrupt Source Select)

This bit is used to select a FIFO interrupt source. Modify this bit only in global reset mode.

RFIGCV[2:0] Bits (Receive FIFO Interrupt Request Timing Select)

These bits are used to specify the number of received messages for generating a receive FIFO interrupt request when the RFIM bit is set to 0 with a fraction for the total number of buffers (the setting of RFDC[2:0]).
When the RFDC[2:0] bits are set to 001b (4 messages), set the RFIGCV[2:0] bits to 001b, 011b, 101b, or 111b. Modify these bits only in global reset mode.

35.2.24 Reception FIFO Buffer Status Registers (RSCAN0RFSTSx) (x = 0 to 7)

The RSCAN0RFSTSx registers are status registers that indicate whether the reception FIFO buffers are empty, the number of unread messages, etc.

Address(es): RSCAN.RSCAN0RFSTS0 A007 80D8h, RSCAN.RSCAN0RFSTS1 A007 80DCh, RSCAN.RSCAN0RFSTS2 A007 80E0h, RSCAN.RSCAN0RFSTS3 A007 80E4h, RSCAN.RSCAN0RFSTS4 A007 80E8h, RSCAN.RSCAN0RFSTS5 A007 80ECh, RSCAN.RSCAN0RFSTS6 A007 80F0h, RSCAN.RSCAN0RFSTS7 A007 80F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFMC[7:0]								—	—	—	—	RFIF	RFMLT	RFFLL	RFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	RFEMP	Reception FIFO Buffer Empty Status Flag	0: The reception FIFO buffer contains unread message. 1: The reception FIFO buffer contains no unread messages (buffer empty).	R
b1	RFFLL	Reception FIFO Buffer Full Status Flag	0: The reception FIFO buffer is not full. 1: The reception FIFO buffer is full.	R
b2	RFMLT	Receive FIFO Message Lost Flag	0: No receive FIFO message is lost. 1: A receive FIFO message is lost.	R/W *1
b3	RFIF	Receive FIFO Interrupt Request Flag	0: No receive FIFO interrupt request is present. 1: A receive FIFO interrupt request is present.	R/W *1
b7 to b4	—	Reserved	These bits are read as 0.	R
b15 to b8	RFMC[7:0]	Receive FIFO Unread Message Counter	The number of unread messages stored in the reception FIFO buffer is displayed.	R
b31 to b16	—	Reserved	These bits are read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

RFEMP Flag (Reception FIFO Buffer Empty Status Flag)

This flag is set to 1 when all messages in the reception FIFO buffer have been read. This flag is also set to 1 when the RFE bit in the RSCAN0RFCCx register is 0 or in global reset mode.

This flag is cleared to 0 when even a single received message has been stored in the reception FIFO buffer.

RFFLL Flag (Reception FIFO Buffer Full Status Flag)

This flag is set to 1 when the number of messages stored in the reception FIFO buffer matches the FIFO buffer depth set by the RFDC[2:0] bits in the RSCAN0RFCCx register.

If the number of messages stored in the reception FIFO buffer becomes smaller than the FIFO buffer depth set by the RFDC[2:0] bits, this flag is cleared to 0. This flag is also cleared to 0 when the RFE bit in the RSCAN0RFCCx register is set to 0 (no reception FIFO buffer is used) or in global reset mode.

RFMLT Flag (Receive FIFO Message Lost Flag)

This flag is set to 1 when an attempt is made to store a new message while the reception FIFO buffer is full. In this case, the new message is discarded.
This flag is cleared to 0 in global reset mode or by writing 0 to this flag.
Modify this bit in global operating mode or global test mode.
To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

RFIF Flag (Receive FIFO Interrupt Request Flag)

This flag is set to 1 when the receive FIFO interrupt request generation conditions set by the RFIGCV[2:0] bits and the RFIM bit in the RSCAN0RFCCx register are met. This flag is cleared to 0 in global reset mode or by writing 0 to this flag. Modify this bit in global operating mode or global test mode.
To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

RFMC[7:0] Flag (Receive FIFO Unread Message Counter)

This flag indicates the number of unread messages in the reception FIFO buffer. These flags become 00h when the RFE bit in the RSCAN0RFCCx register is set to 0.

35.2.25 Reception FIFO Buffer Pointer Control Registers (RSCAN0RFPCTRx) (x = 0 to 7)

The RSCAN0RFPCTRx registers control the pointer to the reception FIFO buffer.

Address(es): RSCAN.RSCAN0RFPCTR0 A007 80F8h, RSCAN.RSCAN0RFPCTR1 A007 80FCh, RSCAN.RSCAN0RFPCTR2 A007 8100h, RSCAN.RSCAN0RFPCTR3 A007 8104h, RSCAN.RSCAN0RFPCTR4 A007 8108h, RSCAN.RSCAN0RFPCTR5 A007 810Ch, RSCAN.RSCAN0RFPCTR6 A007 8110h, RSCAN.RSCAN0RFPCTR7 A007 8114h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFPC[7:0]	Receive FIFO Pointer Control	When these bits are set to FFh, the read pointer moves to the next unread message in the reception FIFO buffer.	W
b31 to b8	—	Reserved	The write value should be 0.	W

RFPC[7:0] Bits (Receive FIFO Pointer Control)

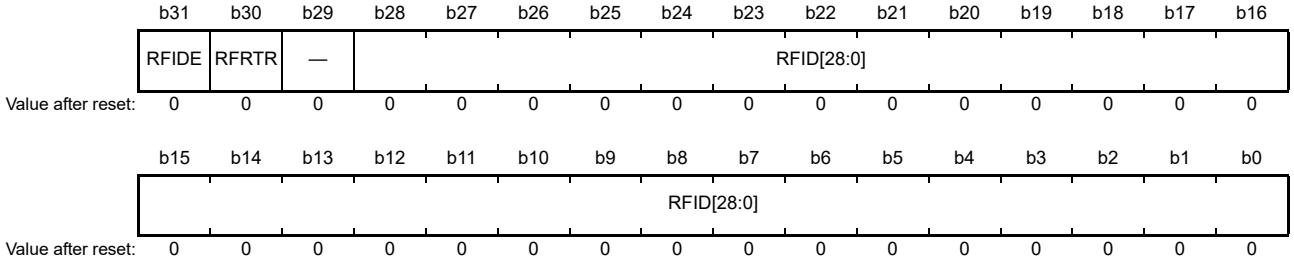
When the RFPC[7:0] bits are set to FFh, the read pointer moves to the next unread message in the reception FIFO buffer. At this time, the RFMC[7:0] (receive FIFO unread message counter) value in the RSCAN0RFSTSx register is decremented. Read the RSCAN0RFID, RSCAN0RFPTR, RSCAN0RFDF0, and RSCAN0RFDF1 registers to read messages in the reception FIFO buffer, and then write FFh to the RFPC[7:0] bits.

When writing FFh to these bits, make sure that the RFE bit in the RSCAN0RFCCx register is set to 1 (reception FIFO buffers are used) and the RFEMP flag in the RSCAN0RFSTSx register is 0 (the reception FIFO buffer contains unread messages).

35.2.26 Reception FIFO Buffer Access ID Registers (RSCAN0RFIDx) (x = 0 to 7)

The RSCAN0RFIDx registers are status registers that indicate the state of the ID and frame formats of the messages stored in the reception FIFO buffers.

Address(es): RSCAN.RSCAN0RFID0 A007 8E00h, RSCAN.RSCAN0RFID1 A007 8E10h, RSCAN.RSCAN0RFID2 A007 8E20h, RSCAN.RSCAN0RFID3 A007 8E30h, RSCAN.RSCAN0RFID4 A007 8E40h, RSCAN.RSCAN0RFID5 A007 8E50h, RSCAN.RSCAN0RFID6 A007 8E60h, RSCAN.RSCAN0RFID7 A007 8E70h



Bit	Symbol	Bit Name	Description	R/W
b28 to b0	RFID[28:0]	Reception FIFO Buffer ID Data	The standard ID or extended ID of received message can be read. Read bits b10 to b0 for standard ID. Bits b28 to b11 are read as 0.	R
b29	—	Reserved	This bit is read as 0.	R
b30	RFRTR	Reception FIFO Buffer RTR	0: Data frame 1: Remote frame	R
b31	RFIDE	Reception FIFO Buffer IDE	0: Standard ID 1: Extended ID	R

RFID[28:0] Bits (Reception FIFO Buffer ID Data)

These bits indicate the ID of the messages stored in the reception FIFO buffers.

RFRTR Bit (Reception FIFO Buffer RTR)

This bit indicates the frame format (data frame or remote frame) of the messages stored in the reception FIFO buffers.

RFIDE Bit (Reception FIFO Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the messages stored in the reception FIFO buffers.

35.2.27 Reception FIFO Buffer Access Pointer Registers (RSCAN0RFPTRx) (x = 0 to 7)

The RSCAN0RFPTRx registers are status registers that indicate the data length, label information, and timestamp value of the messages stored in the reception FIFO buffers.

Address(es): RSCAN.RSCAN0RFPTR0 A007 8E04h, RSCAN.RSCAN0RFPTR1 A007 8E14h, RSCAN.RSCAN0RFPTR2 A007 8E24h, RSCAN.RSCAN0RFPTR3 A007 8E34h, RSCAN.RSCAN0RFPTR4 A007 8E44h, RSCAN.RSCAN0RFPTR5 A007 8E54h, RSCAN.RSCAN0RFPTR6 A007 8E64h, RSCAN.RSCAN0RFPTR7 A007 8E74h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RFDLC[3:0]				RFPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	RFTS[15:0]	Reception FIFO Buffer Timestamp Data	Timestamp value of the received messages can be read.	R
b27 to b16	RFPTR[11:0]	Reception FIFO Buffer Label Data	Label information of the received messages can be read.	R
b31 to b28	RFDLC[3:0]	Reception FIFO Buffer DLC Data	b31 b30 b29 b28 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 X X X: 8 data bytes	R

RFTS[15:0] Bits (Reception FIFO Buffer Timestamp Data)

These bits contain the timestamp value of the messages stored in the reception FIFO buffers.

RFPTR[11:0] Bits (Reception FIFO Buffer Label Data)

These bits contain the label information of the messages stored in the reception FIFO buffers.

RFDLC[3:0] Bits (Reception FIFO Buffer DLC Data)

These bits contain the data length of the messages stored in the reception FIFO buffers.

35.2.28 Reception FIFO Buffer Access Data Field 0 Registers (RSCAN0RFDF0x) (x = 0 to 7)

The RSCAN0RFDF0x registers are data registers that hold the values in the reception FIFO buffers.
When the value of the RMDLC[3:0] bits in the RSCAN0RFPTRx register is less than 1000b, data bytes for which no value is set are read as 00h.

Address(es): RSCAN.RSCAN0RFDF00 A007 8E08h, RSCAN.RSCAN0RFDF01 A007 8E18h, RSCAN.RSCAN0RFDF02 A007 8E28h, RSCAN.RSCAN0RFDF03 A007 8E38h, RSCAN.RSCAN0RFDF04 A007 8E48h, RSCAN.RSCAN0RFDF05 A007 8E58h, RSCAN.RSCAN0RFDF06 A007 8E68h, RSCAN.RSCAN0RFDF07 A007 8E78h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RFDB3[7:0]								RFDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB1[7:0]								RFDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB0[7:0]	Reception FIFO Buffer Data Byte 0	Values of messages stored in the corresponding reception FIFO buffer can be read from these bits.	R
b15 to b8	RFDB1[7:0]	Reception FIFO Buffer Data Byte 1		R
b23 to b16	RFDB2[7:0]	Reception FIFO Buffer Data Byte 2		R
b31 to b24	RFDB3[7:0]	Reception FIFO Buffer Data Byte 3		R

35.2.29 Reception FIFO Buffer Access Data Field 1 Registers (RSCAN0RFDF1x) (x = 0 to 7)

The RSCAN0RFDF1x registers are data registers that hold the values in the reception FIFO buffers.
When the value of the RMDLC[3:0] bits in the RSCAN0RFPTRx register is less than 1000b, data bytes for which no value is set are read as 00h.

Address(es): RSCAN.RSCAN0RFDF10 A007 8E0Ch, RSCAN.RSCAN0RFDF11 A007 8E1Ch, RSCAN.RSCAN0RFDF12 A007 8E2Ch, RSCAN.RSCAN0RFDF13 A007 8E3Ch, RSCAN.RSCAN0RFDF14 A007 8E4Ch, RSCAN.RSCAN0RFDF15 A007 8E5Ch, RSCAN.RSCAN0RFDF16 A007 8E6Ch, RSCAN.RSCAN0RFDF17 A007 8E7Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RFDB7[7:0]								RFDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFDB5[7:0]								RFDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	RFDB4[7:0]	Reception FIFO Buffer Data Byte 4	Values of messages stored in the corresponding reception FIFO buffer can be read from these bits.	R
b15 to b8	RFDB5[7:0]	Reception FIFO Buffer Data Byte 5		R
b23 to b16	RFDB6[7:0]	Reception FIFO Buffer Data Byte 6		R
b31 to b24	RFDB7[7:0]	Reception FIFO Buffer Data Byte 7		R

35.2.30 Transmission/Reception FIFO Buffer Configuration and Control Registers k (RSCAN0CFCCk) (k = 0 to 5)

The RSCAN0CFCCk registers control the settings for the transmission/reception FIFO buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).

Address(es): RSCAN.RSCAN0CFCC0 A007 8118h, RSCAN.RSCAN0CFCC1 A007 811Ch, RSCAN.RSCAN0CFCC2 A007 8120h, RSCAN.RSCAN0CFCC3 A007 8124h, RSCAN.RSCAN0CFCC4 A007 8128h, RSCAN.RSCAN0CFCC5 A007 812Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CFITT[7:0]								CFTML[3:0]				CFITR	CFITSS	CFM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFIGCV[2:0]			CFIM	—	CFDC[2:0]			—	—	—	—	—	CFTXIE	CFRXIE	CFE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CFE	Transmission/Reception FIFO Buffer Enable	0: No transmission/reception FIFO buffer is used. 1: Transmission/reception FIFO buffers are used.	R/W
b1	CFRXIE	Transmit/Receive FIFO Receive Interrupt Enable	0: Transmit/receive FIFO receive interrupt is disabled. 1: Transmit/receive FIFO receive interrupt is enabled.	R/W
b2	CFTXIE	Transmit/Receive FIFO Transmit Interrupt Enable	0: Transmit/receive FIFO transmit interrupt is disabled. 1: Transmit/receive FIFO transmit interrupt is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CFDC[2:0]	Transmission/Reception FIFO Buffer Depth Configuration	b10 b9 b8 0 0 0: 0 messages 0 0 1: 4 messages 0 1 0: 8 messages 0 1 1: 16 messages 1 0 0: 32 messages 1 0 1: 48 messages 1 1 0: 64 messages 1 1 1: 128 messages	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	CFIM	Transmit/Receive FIFO Interrupt Source Select	0: • Reception mode/gateway mode When the number of received messages has met the condition set by the CFIGCV[2:0] bits, a FIFO receive interrupt request is generated. • Transmission mode/gateway mode When the buffer becomes empty upon completion of message transmission, a FIFO transmit interrupt request is generated. 1: • Reception mode/gateway mode A FIFO receive interrupt request is generated each time a message has been received. • Transmission mode/gateway mode A FIFO transmit interrupt request is generated each time a message has been transmitted.	R/W

Bit	Symbol	Bit Name	Description	R/W
b15 to b13	CFIGCV[2:0]	Transmit/Receive FIFO Receive Interrupt Request Timing Select	b15 b14 b13 0 0 0: When FIFO is 1/8 full. 0 0 1: When FIFO is 2/8 full. 0 1 0: When FIFO is 3/8 full. 0 1 1: When FIFO is 4/8 full. 1 0 0: When FIFO is 5/8 full. 1 0 1: When FIFO is 6/8 full. 1 1 0: When FIFO is 7/8 full. 1 1 1: When FIFO is full.	R/W
b17, b16	CFM[1:0]	Transmit/Receive FIFO Mode Select	b17 b16 0 0: Reception mode 0 1: Transmission mode 1 0: Gateway mode Setting other than above is prohibited.	R/W
b18	CFITSS	Transmit/Receive FIFO Interval Timer Clock Source Select	0: Interval timer clock source selected by the CFITR bit 1: Interval timer clock source is the bit time clock for the channel to which the FIFO is linked.	R/W
b19	CFITR	Transmit/Receive FIFO Interval Timer Resolution Select	0: PCLKD/2 clock divided by the value of the ITRCP [15:0] bits 1: PCLKD/2 clock divided by (the value of the ITRCP [15:0] bits × 10)	R/W
b23 to b20	CFTML[3:0]	Transmission Buffer Link Configuration	Set the transmission buffer number to be linked to the transmission/reception FIFO buffer.	R/W
b31 to b24	CFITT[7:0]	Message Transmission Interval Configuration	Set Value: 00h to FFh	R/W

CFE Bit (Transmission/Reception FIFO Buffer Enable)

Setting this bit to 1 makes transmission/reception FIFO buffers available.

When this bit is set to 0 in transmission mode or gateway mode, if a message in the transmission/reception FIFO buffer is being transmitted or will be transmitted next, the transmission/reception FIFO buffer becomes empty after completion of transmission of that message, or upon detection of a CAN bus error, or arbitration-lost. In other cases or in reception mode, the transmission/reception FIFO buffer becomes empty immediately.

This bit is cleared to 0 when the following conditions are met.

- Reception mode: Global reset mode
- Transmission mode or gateway mode: Channel reset mode

Modify this bit in the following mode.

- Reception mode: Global operating mode or global test mode
- Transmission mode or gateway mode: Channel communication mode or channel halt mode

CFRXIE Bit (Transmit/Receive FIFO Receive Interrupt Enable)

When this bit is set to 1 and the CFRXIF flag in the RSCAN0CFSTSk register is set to 1, a transmit/receive FIFO receive interrupt request is generated.

Modify this bit with the CFE bit set to 0.

CFTXIE Bit (Transmit/Receive FIFO Transmit Interrupt Enable)

When this bit is set to 1 and the CFTXIF flag in the RSCAN0CFSTSk register is set to 1, a transmit/receive FIFO transmit interrupt request is generated.

Modify this bit with the CFE bit set to 0 (no transmission/reception FIFO buffer is used).

CFDC[2:0] Bits (Transmission/Reception FIFO Buffer Depth Configuration)

These bits are used to set the number of messages that can be stored in a single transmission/reception FIFO buffer.

When these bits are set to 000b, do not use a transmission/reception FIFO buffer. Modify these bits only in global reset mode.

CFIM Bit (Transmit/Receive FIFO Interrupt Source Select)

This bit is used to select a transmit/receive FIFO interrupt source. Modify this bit only in global reset mode.

CFIGCV[2:0] Bits (Transmit/Receive FIFO Receive Interrupt Request Timing Select)

These bits are used to specify the number of received messages for generating a transmit/receive FIFO receive interrupt request when the CFM[1:0] bits are set to 00b (reception mode) or 10b (gateway mode) and the CFIM bit is set to 0 with a fraction for the total number of buffers (the setting of CFDC[2:0]).
When the CFDC[2:0] bits are set to 001b (4 messages), set the CFIGCV[2:0] bits to 001b, 011b, 101b, or 111b.
Modify these bits only in global reset mode.

CFM[1:0] Bits (Transmit/Receive FIFO Mode Select)

These bits are used to select transmit/receive FIFO mode. Modify these bits only in global reset mode.

CFITSS Bit (Transmit/Receive FIFO Interval Timer Clock Source Select)

When this bit is 0, the clock selected by the CFITR bit is the count source of the interval timer.
When this bit is 1, the bit time clock of the channel to which the FIFO is linked is the count source of the interval timer.
Modify this bit while the CFE bit is set to 0 (no transmission/reception FIFO buffer is used).

CFITR Bit (Transmit/Receive FIFO Interval Timer Resolution Select)

This bit is enabled when the CFITSS bit is 0.
When this bit is 0, the interval timer clock source is the PCLKD/2 clock divided by the value of the ITRCP[15:0] bits in the RSCAN0GCFG register.
When this bit is 1, the interval timer clock source is the PCLKD/2 clock divided by (the value of the ITRCP[15:0] bits in the RSCAN0GCFG register × 10).
Modify this bit while the CFE bit is set to 0 (no transmission/reception FIFO buffer is used).

CFTML[3:0] Bits (Transmission Buffer Link Configuration)

These bits are used to set the number of transmission buffer on the channel which will be linked to transmission/reception FIFO buffer k when the CFM[1:0] bits are set to 01b (transmission mode) or 10b (gateway mode). There are three transmission/reception FIFO buffers per channel (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1). Table 35.4 lists the actual transmission buffer numbers p linked to FIFO buffers k.

See section 35.6, Transmission Functions, for operations of transmission/reception FIFO buffers k and transmission buffers p.

Setting the CFDC[2:0] bits to 001b or more enables the setting of the CFTML[3:0] bits.

Do not link to any transmission buffer which is already allocated to a transmission queue on the identical channel or to another transmission/reception FIFO buffer. Modify these bits only in global reset mode.

Table 35.4 Settings of the CFTML[3:0] Bits and Linking of Transmission Buffers p to Transmission/Reception FIFO Buffers k

Settings of CFTML[3:0] Bits (setting for each transmission/reception FIFO buffer k)	Transmission Buffers p Linked to Transmission/Reception FIFO Buffers (p = 0 to 31)	
	Channel 0 (m = 0)	Channel 1 (m = 1)
0000b	Transmission buffer 0	Transmission buffer 16
0001b	Transmission buffer 1	Transmission buffer 17
0010b	Transmission buffer 2	Transmission buffer 18
0011b	Transmission buffer 3	Transmission buffer 19
0100b	Transmission buffer 4	Transmission buffer 20
0101b	Transmission buffer 5	Transmission buffer 21
0110b	Transmission buffer 6	Transmission buffer 22
0111b	Transmission buffer 7	Transmission buffer 23
1000b	Transmission buffer 8	Transmission buffer 24
1001b	Transmission buffer 9	Transmission buffer 25
1010b	Transmission buffer 10	Transmission buffer 26
1011b	Transmission buffer 11	Transmission buffer 27
1100b	Transmission buffer 12	Transmission buffer 28
1101b	Transmission buffer 13	Transmission buffer 29
1110b	Transmission buffer 14	Transmission buffer 30
1111b	Transmission buffer 15	Transmission buffer 31

CFITT[7:0] Bits (Message Transmission Interval Configuration)

These bits are used to set a message transmission interval when transmitting messages continuously from a transmission/reception FIFO buffer whose CFM[1:0] bits are set to 01b (transmission mode) or 10b (gateway mode).

Clear the CFE bit to 0 (no transmission/reception FIFO buffer is used) before modifying the CFITT[7:0] bits.

35.2.31 Transmission/Reception FIFO Buffer Status Registers (RSCAN0CFSTSk) (k = 0 to 5)

The RSCAN0CFSTSk registers are status registers that indicate the state of the transmission/reception FIFO buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).

Address(es): RSCAN.RSCAN0CFSTS0 A007 8178h, RSCAN.RSCAN0CFSTS1 A007 817Ch, RSCAN.RSCAN0CFSTS2 A007 8180h, RSCAN.RSCAN0CFSTS3 A007 8184h, RSCAN.RSCAN0CFSTS4 A007 8188h, RSCAN.RSCAN0CFSTS5 A007 818Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFMC[7:0]								—	—	—	CFTXIF	CFRXIF	CFMLT	CFFLL	CFEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CFEMP	Transmission/Reception FIFO Buffer Empty Status Flag	0: The transmission/reception FIFO buffer contains messages. 1: The transmission/reception FIFO buffer contains no message (buffer empty).	R
b1	CFFLL	Transmission/Reception FIFO Buffer Full Status Flag	0: The transmission/reception FIFO buffer is not full. 1: The transmission/reception FIFO buffer is full.	R
b2	CFMLT	Transmit/Receive FIFO Message Lost Flag	0: No transmit/receive FIFO message is lost. 1: A transmit/receive FIFO message is lost.	R/W *1
b3	CFRXIF	Transmit/Receive FIFO Receive Interrupt Request Flag	0: No transmit/receive FIFO receive interrupt request is present. 1: A transmit/receive FIFO receive interrupt request is present.	R/W *1
b4	CFTXIF	Transmit/Receive FIFO Transmit Interrupt Request Flag	0: No transmit/receive FIFO transmit interrupt request is present. 1: A transmit/receive FIFO transmit interrupt request is present.	R/W *1
b7 to b5	—	Reserved	These bits are read as 0.	R
b15 to b8	CFMC[7:0]	Transmit/Receive FIFO Message Counter	The number of messages stored in the transmission/ reception FIFO buffer.	R
b31 to b16	—	Reserved	These bits are read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

CFEMP Flag (Transmission/Reception FIFO Buffer Empty Status Flag)

The CFEMP flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00b: All messages have been read, or in global reset mode
- When the CFM[1:0] bits are set to 01b or 10b: All messages have been transmitted, or in channel reset mode
- When the CFE bit is 0 (no transmission/reception FIFO buffer is used): Not in the transmission abort

The CFEMP flag is cleared to 0 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00b or 10b: At least one received message has been stored in the transmission/ reception FIFO buffer.
- When the CFM[1:0] bits are set to 01b: A value of FFh has been written to the RSCAN0CFPCTRk register after data was written to the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers.

CFFLL Flag (Transmission/Reception FIFO Buffer Full Status Flag)

The CFFLL flag is set to 1 when any of the following conditions is met.

- When the number of messages stored in the transmission/reception FIFO buffer matches the FIFO buffer depth set by the CFDC[2:0] bits in the RSCAN0CFCCk register.

The CFFLL flag is cleared to 0 when any of the following conditions is met.

- When the number of messages stored in the transmission/reception FIFO buffer becomes smaller than the FIFO buffer depth set by the CFDC[2:0] bits.
- When the CFE bit in the RSCAN0CFCCk register is 0 (no transmission/reception FIFO buffer is used): When not in the transmission abort
- When the CFM[1:0] bits are set to 00b: In global reset mode
  When the CFM[1:0] bits are set to 01b or 10b: In channel reset mode

CFMLT Flag (Transmit/Receive FIFO Message Lost Flag)

The CFMLT flag is set to 1 when any of the following conditions is met.

- When an attempt is made to store a new message while the transmission/reception FIFO buffer is full. In this case, the new message is discarded.

The CFMLT flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFMLT flag
- When the CFM[1:0] bits are set to 00b: In global reset mode
- When the CFM[1:0] bits are set to 01b or 10b: In channel reset mode

Write 0 to this flag in global operating mode or global test mode

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFRXIF Flag (Transmit/Receive FIFO Receive Interrupt Request Flag)

The CFRXIF flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 00b or 10b, and the factor selected by the CFIM bit in the RSCAN0CFCCk register occurs

The CFRXIF flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFRXIF flag
- When the CFM[1:0] bits are set to 00b: In global reset mode
- When the CFM[1:0] bits are set to 01b or 10b: In channel reset mode

Write 0 to this flag in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared.

When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFTXIF Flag (Transmit/Receive FIFO Transmit Interrupt Request Flag)

The CFTXIF flag is set to 1 when any of the following conditions is met.

- When the CFM[1:0] bits are set to 01b or 10b, and the factor selected by the CFIM bit in the RSCAN0CFCCk register occurs

The CFTXIF flag is cleared to 0 when any of the following conditions is met.

- When 0 is written to the CFTXIF flag
- When the CFM[1:0] bits are set to 00b: In global reset mode
- When the CFM[1:0] bits are set to 01b or 10b: In channel reset mode

Write 0 to this flag in global operating mode or global test mode.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared. When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

CFMC[7:0] Bits (Transmit/Receive FIFO Message Counter)

The CFMC[7:0] bits indicate the following values that depend on the setting of the CFM[1:0] bits in the RSCAN0CFCCk register.

- When CFM[1:0] value is 01b (transmission mode): Number of untransmitted messages in the buffer
- When CFM[1:0] value is 00b (reception mode): Number of unread received messages in the buffer
- When CFM[1:0] value is 10b (gateway mode): Number of untransmitted received messages in the buffer

These bits are cleared to 0 when any of the following conditions is met.

- When CFM[1:0] value is 00b: In global reset mode
- When CFM[1:0] value is 01b or 10b: In channel reset mode

35.2.32 Transmission/Reception FIFO Buffer Pointer Control Registers (RSCAN0CFPCTRk) (k = 0 to 5)

The RSCAN0CFPCTRk registers control the pointers to the transmission/reception FIFO buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).

Address(es): RSCAN.RSCAN0CFPCTR0 A007 81D8h, RSCAN.RSCAN0CFPCTR1 A007 81DCh, RSCAN.RSCAN0CFPCTR2 A007 81E0h, RSCAN.RSCAN0CFPCTR3 A007 81E4h, RSCAN.RSCAN0CFPCTR4 A007 81E8h, RSCAN.RSCAN0CFPCTR5 A007 81ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CFPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFPC[7:0]	Transmit/Receive FIFO Pointer Control	• Reception mode: Writing FFh to these bits moves the read pointer to the next unread message in the transmission/reception FIFO buffer. • Transmission mode: Writing FFh to these bits moves the write pointer to the next stage of the transmission/reception FIFO buffer. • Gateway mode: Setting prohibited	W
b31 to b8	—	Reserved	The write value should be 0.	W

CFPC[7:0] Bits (Transmit/Receive FIFO Pointer Control)

- Reception mode (CFM[1:0] value in the RSCAN0CFCCk register is 00b):
  Writing FFh to the CFPC[7:0] bits moves the read pointer to the next unread message in the transmission/reception FIFO buffer. At this time, the CFMC[7:0] value (transmit/receive FIFO message counter) in the RSCAN0CFSTSk register is decremented. Read the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers to read messages from the transmission/reception FIFO buffer, and then write FFh to the CFPC[7:0] bits.
  When writing FFh to these bits, make sure that the CFE bit in the RSCAN0CFCCk register is set to 1 (transmission/reception FIFO buffers are used) and the CFEMP flag in the RSCAN0CFSTSk register is 0 (the transmission/reception FIFO buffer contains messages).
- Transmission mode (CFM[1:0] value in the RSCAN0CFCCk register is 01b):
  Writing FFh to the CFPC[7:0] bits stores the data written to the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers in the transmission/reception FIFO buffer and moves the write pointer to the next stage of the transmission/reception FIFO buffer. At this time, the CFMC[7:0] value is incremented. Write messages for transmission to the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers before writing FFh to the CFPC[7:0] bits.
  When writing FFh to these bits, make sure that the CFE bit in the RSCAN0CFCCk register is set to 1 and the CFFLL flag in the RSCAN0CFSTSk register is 0 (the transmission/reception FIFO buffer is not full).
- Gateway mode (CFM[1:0] value in the RSCAN0CFCCk register is 10b):
  Setting prohibited

35.2.33 Transmission/Reception FIFO Buffer Access ID Registers (RSCAN0CFIDk) (k = 0 to 5)

The RSCAN0CFIDk registers are status registers that indicate the state of the ID and data formats of the received messages stored in the transmission/reception FIFO buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).
These registers are writable only when the CFM[1:0] value in the RSCAN0CFCCk register is 01b (transmission mode) and readable only when the CFM[1:0] value is 00b (reception mode). These registers should not be read or written when the CFM[1:0] value is 10b (gateway mode).

Address(es): RSCAN.RSCAN0CFID0 A007 8E80h, RSCAN.RSCAN0CFID1 A007 8E90h, RSCAN.RSCAN0CFID2 A007 8EA0h, RSCAN.RSCAN0CFID3 A007 8EB0h, RSCAN.RSCAN0CFID4 A007 8EC0h, RSCAN.RSCAN0CFID5 A007 8ED0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CFIDE	CFRTR	THLEN	CFID[28:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFID[28:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b28 to b0	CFID[28:0]	Transmission/Reception FIFO Buffer ID Data Set	• When CFM[1:0] value is 01b (transmission mode): Set standard ID or extended ID. For standard ID, write an ID to bits 10 to 0 and write 0 to bits 28 to 11. • When CFM[1:0] value is 00b (reception mode): Standard ID or extended ID in the received message can be read. For standard ID, read bits 10 to 0. Bits 28 to 11 are read as 0.	R/W
b29	THLEN	Transmission History Data Storage Enable	This bit is valid only when the CFM[1:0] value is 01b (transmission mode). 0: Transmission history data is not stored in the buffer. 1: Transmission history data is stored in the buffer.	R/W
b30	CFRTR	Transmission/Reception FIFO Buffer RTR	0: Data frame 1: Remote frame	R/W
b31	CFIDE	Transmission/Reception FIFO Buffer IDE	0: Standard ID 1: Extended ID	R/W

CFID[28:0] Bits (Transmission/Reception FIFO Buffer ID Data Set)

These bits contain the ID of the received message stored in the transmission/reception FIFO buffer when the CFM[1:0] value is 00b.
When the CFM[1:0] value is 01b, this bit is used to set the ID of the message to be transmitted from the transmission/reception FIFO buffer.

THLEN Bit (Transmission History Data Storage Enable)

When this bit is set to 1, the transmission history data (label information, buffer number, and buffer type) of transmitted messages is stored in the transmission history buffer after transmission is completed.
This bit is enabled when the CFM[1:0] value is 01b (transmission mode).

CFRTR Bit (Transmission/Reception FIFO Buffer RTR)

This bit indicates the data format (data frame or remote frame) of the received message stored in the transmission/reception FIFO buffer when the CFM[1:0] value is 00b. When the CFM[1:0] value is 01b, this bit is used to set the data format of the message to be transmitted from the transmission/reception FIFO buffer.

CFIDE Bit (Transmission/Reception FIFO Buffer IDE)

This bit indicates the ID format (standard ID or extended ID) of the received message stored in the transmission/reception FIFO buffer when the CFM[1:0] value is 00b. When the CFM[1:0] value is 01b, these bits are used to set the ID format of the message to be transmitted from the transmission/reception FIFO buffer.

35.2.34 Transmission/Reception FIFO Buffer Access Pointer Registers (RSCAN0CFPTRk) (k = 0 to 5)

The RSCAN0CFPTRk registers are status registers that indicate the data length, label information, and timestamp value of the received messages stored in the transmission/reception buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1). These registers are writable only when the CFM[1:0] value in the RSCAN0CFCCk register is 01b (transmission mode) and readable only when the CFM[1:0] value is 00b (reception mode). These registers should not be read or written when the CFM[1:0] value is 10b (gateway mode).

Address(es): RSCAN.RSCAN0CFPTR0 A007 8E84h, RSCAN.RSCAN0CFPTR1 A007 8E94h, RSCAN.RSCAN0CFPTR2 A007 8EA4h, RSCAN.RSCAN0CFPTR3 A007 8EB4h, RSCAN.RSCAN0CFPTR4 A007 8EC4h, RSCAN.RSCAN0CFPTR5 A007 8ED4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CFDLC[3:0]				CFPTR[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFTS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CFTS[15:0]	Transmission/Reception FIFO Buffer Timestamp Data Indication	These bits are valid only when the CFM[1:0] value is 00b (reception mode). The timestamp value of the received message can be read.	R/W
b27 to b16	CFPTR[11:0]	Transmission/Reception FIFO Buffer Label Data Indication	• When CFM[1:0] value is 01b (transmission mode): Set the label information to be stored in the transmission history buffer. Only bits CFPTR[7:0] are valid. • When CFM[1:0] value is 00b (reception mode): The label information of the received message can be read.	R/W
b31 to b28	CFDLC[3:0]	Transmission/Reception FIFO Buffer DLC Data Indication	b31 b30 b29 b28 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 X X X: 8 data bytes	R/W

CFTS[15:0] Bits

These bits indicate the timestamp value of the message stored in the transmission/reception FIFO buffer.
These bits are valid when the CFM[1:0] value is 00b.

CFPTR[11:0] Bits

These bits indicate the label information attached to the received message stored in the transmission/reception FIFO buffer when the CFM[1:0] value is 00b. When the CFM[1:0] value is 01b, the CFPTR[7:0] value is stored in the transmission history buffer when message transmission has been completed.

CFDLC[3:0] Bits

These bits indicate the data length of the received message stored in the transmission/reception FIFO buffer when the CFM[1:0] value is 00b. When the CFM[1:0] value is 01b, these bits are used to set the data length of the message to be transmitted from the transmission/reception FIFO buffer. If the data length is set to 9 bytes or more, the actual transmit data defaults to 8 bytes.

35.2.35 Transmission/Reception FIFO Buffer Access Data Field 0 Registers (RSCAN0CFDF0k) (k = 0 to 5)

The RSCAN0CFDF0k registers are data registers that hold the values in the transmission/reception FIFO buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).

These registers are writable only when the CFM[1:0] value in the RSCAN0CFCCk register is 01b (transmission mode) and readable only when the CFM[1:0] value is 00b (reception mode). When the CFDLC[3:0] value in the RSCAN0CFPTRk register is smaller than 1000b, data bytes for which no data is set are read as 00h.

These registers should not be read or written when the CFM[1:0] value is 10b (gateway mode).

Address(es): RSCAN.RSCAN0CFDF00 A007 8E88h, RSCAN.RSCAN0CFDF01 A007 8E98h, RSCAN.RSCAN0CFDF02 A007 8EA8h, RSCAN.RSCAN0CFDF03 A007 8EB8h, RSCAN.RSCAN0CFDF04 A007 8EC8h, RSCAN.RSCAN0CFDF05 A007 8ED8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CFDB3[7:0]								CFDB2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB1[7:0]								CFDB0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB0[7:0]	Transmission/Reception FIFO Buffer Data Byte 0	• When CFM[1:0] value is 01b (transmission mode): Set the transmission/reception FIFO buffer data. • When CFM[1:0] value is 00b (reception mode): Values of messages stored in the corresponding transmission/reception FIFO buffer can be read from these bits.	R/W
b15 to b8	CFDB1[7:0]	Transmission/Reception FIFO Buffer Data Byte 1		R/W
b23 to b16	CFDB2[7:0]	Transmission/Reception FIFO Buffer Data Byte 2		R/W
b31 to b24	CFDB3[7:0]	Transmission/Reception FIFO Buffer Data Byte 3		R/W

35.2.36 Transmission/Reception FIFO Buffer Access Data Field 1 Registers (RSCAN0CFDF1k) (k = 0 to 5)

The RSCAN0CFDF1k registers are data registers that hold the values in the transmission/reception buffers (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1).

These registers are writable only when the CFM[1:0] value in the RSCAN0CFCCk register is 01b (transmission mode) and readable only when the CFM[1:0] value is 00b (reception mode). When the CFDLC[3:0] value in the RSCAN0CFPTRk register is smaller than 1000b, data bytes for which no data is set are read as 00h.

These registers should not be read or written when the CFM[1:0] value is 10b (gateway mode).

Address(es): RSCAN.RSCAN0CFDF10 A007 8E8Ch, RSCAN.RSCAN0CFDF11 A007 8E9Ch, RSCAN.RSCAN0CFDF12 A007 8EACh, RSCAN.RSCAN0CFDF13 A007 8EBCh, RSCAN.RSCAN0CFDF14 A007 8ECCh, RSCAN.RSCAN0CFDF15 A007 8EDCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CFDB7[7:0]								CFDB6[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CFDB5[7:0]								CFDB4[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CFDB4[7:0]	Transmission/Reception FIFO Buffer Data Byte 4	• When CFM[1:0] value is 01b (transmission mode): Set the transmission/reception FIFO buffer data. • When CFM[1:0] value is 00b (reception mode): Values of messages stored in the corresponding transmission/reception FIFO buffer can be read from these bits.	R/W
b15 to b8	CFDB5[7:0]	Transmission/Reception FIFO Buffer Data Byte 5		R/W
b23 to b16	CFDB6[7:0]	Transmission/Reception FIFO Buffer Data Byte 6		R/W
b31 to b24	CFDB7[7:0]	Transmission/Reception FIFO Buffer Data Byte 7		R/W

35.2.37 FIFO Empty Status Register (RSCAN0FESTS)

The RSCAN0FESTS register is a status register that indicates whether receive FIFOx (x = 0 to 7) and transmit/receive FIFOk (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1) are empty.
The RSCAN0FESTS register is set to 03FF FFFFh in global reset mode.

Address(es): RSCAN.RSCAN0FESTS A007 8238h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CF5EMP	CF4EMP	CF3EMP	CF2EMP	CF1EMP	CF0EMP	RF7EMP	RF6EMP	RF5EMP	RF4EMP	RF3EMP	RF2EMP	RF1EMP	RF0EMP
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b0	RF0EMP	Reception FIFO Buffer Empty Status Flag	0: Reception FIFO buffer x contains an unread message. 1: Reception FIFO buffer x contains no unread message. (x = 0 to 7)	R
b1	RF1EMP			R
b2	RF2EMP			R
b3	RF3EMP			R
b4	RF4EMP			R
b5	RF5EMP			R
b6	RF6EMP			R
b7	RF7EMP			R
b8	CF0EMP	Transmission/Reception FIFO Buffer Empty Status Flag	0: Transmission/reception FIFO buffer k contains a message. 1: Transmission/reception FIFO buffer k contains no message. (k = 0 to 5)	R
b9	CF1EMP			R
b10	CF2EMP			R
b11	CF3EMP			R
b12	CF4EMP			R
b13	CF5EMP			R
b16 to b14	—	Reserved	These bits are read as 1.	R
b31 to b17	—	Reserved	These bits are read as 0.	R

RFxEMP Flag (x = 0 to 7)

The RFxEMP flag is set to 1 when the RFEMP flag in the RSCAN0RFSTSx register is set to 1 (the reception FIFO buffer contains no unread message). When the RFEMP flag is cleared to 0 (the reception FIFO buffer contains unread messages), the RFxEMP flag is cleared to 0.

CFkEMP Flag (k = 0 to 5)

The CFkEMP flag is set to 1 when the CFEMP flag in the RSCAN0CFSTSk register is set to 1 (the transmission/reception FIFO buffer contains no message (buffer empty)). When the CFEMP flag is cleared to 0 (the transmission/reception FIFO buffer contains messages), the CFkEMP flag is cleared to 0.

35.2.38 FIFO Full Status Register (RSCAN0FFSTS)

The RSCAN0FFSTS register is a status register that indicates whether receive FIFOx (x = 0 to 7) and transmit/receive FIFOk (k = 0 to 2 for channel 0; k = 3 to 5 for channel 1) are full.
The RSCAN0FFSTS register is cleared to 0000 0000h in global reset mode.

Address(es): RSCAN.RSCAN0FFSTS A007 823Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CF5FLL	CF4FLL	CF3FLL	CF2FLL	CF1FLL	CF0FLL	RF7FLL	RF6FLL	RF5FLL	RF4FLL	RF3FLL	RF2FLL	RF1FLL	RF0FLL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RF0FLL	Reception FIFO Buffer Full Status Flag	0: Reception FIFO buffer x is not full. 1: Reception FIFO buffer x is full. (x = 0 to 7)	R
b1	RF1FLL			R
b2	RF2FLL			R
b3	RF3FLL			R
b4	RF4FLL			R
b5	RF5FLL			R
b6	RF6FLL			R
b7	RF7FLL			R
b8	CF0FLL	Transmission/Reception FIFO Buffer Full Status Flag	0: Transmission/reception buffer k is not full. 1: Transmission/reception buffer k is full. (k = 0 to 5)	R
b9	CF1FLL			R
b10	CF2FLL			R
b11	CF3FLL			R
b12	CF4FLL			R
b13	CF5FLL			R
b31 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)

RFxFLL Flag (x = 0 to 7)

The RFxFLL flag is set to 1 when the RFFLL flag in the RSCAN0RFSTSx register is set to 1 (the reception FIFO buffer is full). When the RFFLL flag is cleared to 0 (the reception FIFO buffer is not full), the RFxFLL flag is cleared to 0.

CFkFLL Flag (k = 0 to 5)

The CFkFLL flag is set to 1 when the CFFLL flag in the RSCAN0CFSTSk register is set to 1 (the transmission/reception FIFO buffer is full). When the CFFLL flag is cleared to 0 (the transmission/reception FIFO buffer is not full), the CFkFLL flag is cleared to 0.

35.2.39 FIFO Message Lost Status Register (RSCAN0FMSTS)

The RSCAN0FMSTS register is a status register that indicates whether messages in receive FIFOx (x = 0 to 7) and transmit/receive FIFOk (k 0 to 2 for channel 0; k = 3 to 5 for channel 1) have been lost.
The RSCAN0FMSTS register is cleared to 0000 0000h in global reset mode.

Address(es): RSCAN.RSCAN0FMSTS A007 8240h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CF5MLT	CF4MLT	CF3MLT	CF2MLT	CF1MLT	CF0MLT	RF7MLT	RF6MLT	RF5MLT	RF4MLT	RF3MLT	RF2MLT	RF1MLT	RF0MLT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RF0MLT	Reception FIFO Buffer Message Lost Status Flag	0: No reception FIFO buffer x message is lost. 1: A reception FIFO buffer x message is lost. (x = 0 to 7)	R
b1	RF1MLT			R
b2	RF2MLT			R
b3	RF3MLT			R
b4	RF4MLT			R
b5	RF5MLT			R
b6	RF6MLT			R
b7	RF7MLT			R
b8	CF0MLT	Transmission/Reception FIFO Buffer Message Lost Status Flag	0: No transmission/reception FIFO buffer k message is lost. 1: A transmission/reception FIFO buffer k message is lost. (k = 0 to 5)	R
b9	CF1MLT			R
b10	CF2MLT			R
b11	CF3MLT			R
b12	CF4MLT			R
b13	CF5MLT			R
b31 to b14	—	Reserved	These bits are read as 0.	R

RFxMLT Flag (x = 0 to 7)

The RFxMLT flag is set to 1 when the RFMLT flag in the RSCAN0RFSTSx register is set to 1 (a receive FIFO message is lost). When the RFMLT flag is cleared to 0, the RFxMLT flag is cleared to 0.

CFkMLT Flag (k = 0 to 5)

The CFkMLT flag is set to 1 when the CFMLT flag in the RSCAN0CFSTSk register is set to 1 (a transmit/receive FIFO message is lost). When the CFMLT flag is cleared to 0, the CFkMLT flag is cleared to 0.

35.2.40 Reception FIFO Buffer Interrupt Flag Status Register (RSCAN0RFISTS)

The RSCAN0RFISTS register is a flag register that indicates interrupts from the reception FIFO buffer.
The RSCAN0RFISTS register is cleared to 0000 0000h in global reset mode.

Address(es): RSCAN.RSCAN0RFISTS A007 8244h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RF7IF	RF6IF	RF5IF	RF4IF	RF3IF	RF2IF	RF1IF	RF0IF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RF0IF	Reception FIFO Buffer Interrupt Request Status Flag	0: No reception FIFO buffer x interrupt request is present. 1: A reception FIFO buffer x interrupt request is present. (x = 0 to 7)	R
b1	RF1IF			R
b2	RF2IF			R
b3	RF3IF			R
b4	RF4IF			R
b5	RF5IF			R
b6	RF6IF			R
b7	RF7IF			R
b31 to b8	—	Reserved	These bits are read as 0.	R

RFxIF Flag (x = 0 to 7)

The RFxIF flag is set to 1 when the RFIF flag in the RSCAN0RFSTSx register is set to 1 (a receive FIFO interrupt request is present). When the RFIF flag is cleared to 0, the RFxIF flag is cleared to 0.

35.2.41 Transmission/Reception FIFO Buffer Receive Interrupt Flag Status Register (RSCAN0CFRISTS)

The RSCAN0CFRISTS register is a flag register that indicates reception interrupts from the transmission/reception FIFO buffer.

The RSCAN0CFRISTS register is cleared to 0000 0000h in global reset mode.

Address(es): RSCAN.RSCAN0CFRISTS A007 8248h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CF5RXIF	CF4RXIF	CF3RXIF	CF2RXIF	CF1RXIF	CF0RXIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF0RXIF	Transmission/Reception FIFO Buffer Receive Interrupt Request Status Flag	0: No transmission/reception FIFO buffer k receive interrupt request is present. 1: A transmission/reception FIFO buffer k receive interrupt request is present. (k = 0 to 5)	R
b1	CF1RXIF			R
b2	CF2RXIF			R
b3	CF3RXIF			R
b4	CF4RXIF			R
b5	CF5RXIF			R
b31 to b6	—	Reserved	These bits are read as 0.	R

CFkRXIF Flag (k = 0 to 5)

The CFkRXIF flag is set to 1 when the CFRXIF flag in the RSCAN0CFSTSk register is set to 1 (a transmit/receive FIFO receive interrupt request is present). When the CFRXIF flag is cleared to 0, the CFkRXIF flag is cleared to 0.

35.2.42 Transmission/Reception FIFO Buffer Transmit Interrupt Flag Status Register (RSCAN0CFTISTS)

The RSCAN0CFTISTS register is a flag register that indicates transmission interrupts from the transmission/reception FIFO buffer.

The RSCAN0CFTISTS register is cleared to 0000 0000h in global reset mode.

Address(es): RSCAN.RSCAN0CFTISTS A007 824Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	CF5TXIF	CF4TXIF	CF3TXIF	CF2TXIF	CF1TXIF	CF0TXIF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CF0TXIF	Transmission/Reception FIFO Buffer Transmit Interrupt Request Status Flag	0: No transmission/reception FIFO buffer k transmit interrupt request is present. 1: A transmission/reception FIFO buffer k transmit interrupt request is present. (k = 0 to 5)	R
b1	CF1TXIF			R
b2	CF2TXIF			R
b3	CF3TXIF			R
b4	CF4TXIF			R
b5	CF5TXIF			R
b31 to b6	—	Reserved	These bits are read as 0.	R

CFkTXIF Flag (k = 0 to 5)

The CFkTXIF flag is set to 1 when the CFTXIF flag in the RSCAN0CFSTSk register is set to 1 (a transmit/receive FIFO transmit interrupt request is present). When the CFTXIF flag is cleared to 0, the CFkTXIF flag is cleared to 0.

35.2.43 Transmission Buffer Control Register (RSCAN0TMCp) (p = 0 to 31)

The RSCAN0TMCp registers control the settings for the transmission buffers (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Set the RSCAN0TMCp registers to 00h when any of the following conditions is met.

- The RSCAN0TMCp register corresponds to the transmission buffer number selected by the CFTML[3:0] bits in the RSCAN0CFCCk register (p = m × 16 + the value of CFTML[3:0] bits) (m = 0, k = 0 to 2 for channel 0; m = 1, k = 3 to 5 for channel 1).
- The RSCAN0TMCp register corresponds to the transmission buffer allocated to the transmission queue by the TXQDC[3:0] bits in the RSCAN0TXQCCm register (p = (m × 16 + 15) to (m × 16 + 15 – the value of TXQDC[3:0] bits)).

Bits in the RSCAN0TMCp registers are all cleared to 0 in channel reset mode.

Modify the RSCAN0TMCp registers in channel communication mode or channel halt mode.

Address(es): RSCAN.RSCAN0TMC0 A007 8250h, RSCAN.RSCAN0TMC1 A007 8251h, RSCAN.RSCAN0TMC2 A007 8252h, RSCAN.RSCAN0TMC3 A007 8253h, RSCAN.RSCAN0TMC4 A007 8254h, RSCAN.RSCAN0TMC5 A007 8255h, RSCAN.RSCAN0TMC6 A007 8256h, RSCAN.RSCAN0TMC7 A007 8257h, RSCAN.RSCAN0TMC8 A007 8258h, RSCAN.RSCAN0TMC9 A007 8259h, RSCAN.RSCAN0TMC10 A007 825Ah, RSCAN.RSCAN0TMC11 A007 825Bh, RSCAN.RSCAN0TMC12 A007 825Ch, RSCAN.RSCAN0TMC13 A007 825Dh, RSCAN.RSCAN0TMC14 A007 825Eh, RSCAN.RSCAN0TMC15 A007 825Fh, RSCAN.RSCAN0TMC16 A007 8260h, RSCAN.RSCAN0TMC17 A007 8261h, RSCAN.RSCAN0TMC18 A007 8262h, RSCAN.RSCAN0TMC19 A007 8263h, RSCAN.RSCAN0TMC20 A007 8264h, RSCAN.RSCAN0TMC21 A007 8265h, RSCAN.RSCAN0TMC22 A007 8266h, RSCAN.RSCAN0TMC23 A007 8267h, RSCAN.RSCAN0TMC24 A007 8268h, RSCAN.RSCAN0TMC25 A007 8269h, RSCAN.RSCAN0TMC26 A007 826Ah, RSCAN.RSCAN0TMC27 A007 826Bh, RSCAN.RSCAN0TMC28 A007 826Ch, RSCAN.RSCAN0TMC29 A007 826Dh, RSCAN.RSCAN0TMC30 A007 826Eh, RSCAN.RSCAN0TMC31 A007 826Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TMOM	TMTAR	TMTR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTR	Transmission Request	0: Transmission is not requested. 1: Transmission is requested.	R/W *1
b1	TMTAR	Transmission Abort Request	0: Transmission abort is not requested. 1: Transmission abort is requested.	R/W *1
b2	TMOM	One-Shot Transmission Enable	0: One-shot transmission is disabled. 1: One-shot transmission is enabled.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The only effective value for writing to this bit is 1, which sets the bit. Otherwise writing to the bit results in retention of its state.

TMTR Bit (Transmission Request)

Setting this bit to 1 transmits the message stored in the transmission buffer.

The TMTR bit is cleared to 0 when any of the following conditions is met, but cannot be cleared by the program writing 0 to the bit.

- Transmission has been completed.
- Transmission abort has been completed after the TMTAR bit was set to 1.
- An error or arbitration-lost has been detected with the TMOM bit set to 1.

Set the TMTR bit to 1 when the value of TMTRF[1:0] in the RSCAN0TMSTSp register is 00b.

TMTAR Bit (Transmission Abort Request)

Setting this bit to 1 generates a transmission abort request for the message stored in the transmission buffer. However, a message that is being transmitted or one that will be transmitted next cannot be aborted.
The TMTAR bit can be set to 1 when TMTR bit is 1.
The TMTAR bit is cleared to 0 when any of the following conditions is met, but cannot be cleared by the program writing 0 to the bit.

- Transmission has been completed.
- Transmission abort has been completed.
- An error or arbitration loss has been detected.

If this bit becomes 0 at the same time as the program writes 1 to this bit, this bit becomes 0.

TMOM Bit (One-Shot Transmission Enable)

Setting this bit to 1 enables one-shot transmission. When transmission fails, retransmission defined in the CAN protocol is not performed.
Modify the TMOM bit when the TMTRM flag in the RSCAN0TMSTSp register is set to 0. Set the TMOM bit to 1 together with the TMTR bit.

35.2.44 Transmission Buffer Status Registers (RSCAN0TMSTSp) (p = 0 to 31)

The RSCAN0TMSTSp registers are status registers that indicate the state of the transmission buffers (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Bits in the RSCAN0TMSTSp registers are all cleared to 0 in channel reset mode.

Address(es): RSCAN.RSCAN0TMSTS0 A007 82D0h, RSCAN.RSCAN0TMSTS1 A007 82D1h, RSCAN.RSCAN0TMSTS2 A007 82D2h, RSCAN.RSCAN0TMSTS3 A007 82D3h, RSCAN.RSCAN0TMSTS4 A007 82D4h, RSCAN.RSCAN0TMSTS5 A007 82D5h, RSCAN.RSCAN0TMSTS6 A007 82D6h, RSCAN.RSCAN0TMSTS7 A007 82D7h, RSCAN.RSCAN0TMSTS8 A007 82D8h, RSCAN.RSCAN0TMSTS9 A007 82D9h, RSCAN.RSCAN0TMSTS10 A007 82DAh, RSCAN.RSCAN0TMSTS11 A007 82DBh, RSCAN.RSCAN0TMSTS12 A007 82DCh, RSCAN.RSCAN0TMSTS13 A007 82DDh, RSCAN.RSCAN0TMSTS14 A007 82DEh, RSCAN.RSCAN0TMSTS15 A007 82DFh, RSCAN.RSCAN0TMSTS16 A007 82E0h, RSCAN.RSCAN0TMSTS17 A007 82E1h, RSCAN.RSCAN0TMSTS18 A007 82E2h, RSCAN.RSCAN0TMSTS19 A007 82E3h, RSCAN.RSCAN0TMSTS20 A007 82E4h, RSCAN.RSCAN0TMSTS21 A007 82E5h, RSCAN.RSCAN0TMSTS22 A007 82E6h, RSCAN.RSCAN0TMSTS23 A007 82E7h, RSCAN.RSCAN0TMSTS24 A007 82E8h, RSCAN.RSCAN0TMSTS25 A007 82E9h, RSCAN.RSCAN0TMSTS26 A007 82EAh, RSCAN.RSCAN0TMSTS27 A007 82EBh, RSCAN.RSCAN0TMSTS28 A007 82ECh, RSCAN.RSCAN0TMSTS29 A007 82EDh, RSCAN.RSCAN0TMSTS30 A007 82EEh, RSCAN.RSCAN0TMSTS31 A007 82EFh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TMTARM	TMTRM	TMTRF[1:0]		TMTSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TMTSTS	Transmission Buffer Transmission Status Flag	0: Transmission is not in progress. 1: Transmission is in progress.	R
b2, b1	TMTRF[1:0]	Transmission Buffer Transmission Result Status Flag	b2 b1 0 0: Transmission is in progress or no transmission request is present. 0 1: Transmission abort has been completed. 1 0: Transmission has been completed (without transmission abort request). 1 1: Transmission has been completed (with transmission abort request).	R/W
b3	TMTRM	Transmission Buffer Transmission Request Status Flag	0: No transmission request is present. 1: A transmission request is present.	R
b4	TMTARM	Transmission Buffer Transmission Abort Request Status Flag	0: No transmission abort request is present. 1: A transmission abort request is present.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TMTSTS Flag (Transmission Buffer Transmission Status Flag)

This flag is set to 1 when transmission from the transmission buffer starts, and is cleared to 0 when transmission from the transmission buffer has been completed or terminated due to a bus error or arbitration lost.

TMTRF[1:0] Flag (Transmission Buffer Transmission Result Status Flag)

This flag indicates the result of transmission from the transmission buffer.

00b: Transmission is in progress or no transmission request is present.

01b: Transmission from the transmission buffer was aborted.

10b: Transmission has been completed with the TMTAR bit in the RSCAN0TMCp register set to 0 (transmission abort is not requested).

11b: Transmission has been completed with the TMTAR bit in the RSCAN0TMCp register set to 1 (transmission abort is requested).

Write 00b to the TMTRF[1:0] flag in channel communication mode or channel halt mode. Do not write any value other than 00b to this flag.

TMTRM Flag (Transmission Buffer Transmission Request Status Flag)

The TMTRM flag is set to 1 when the TMTR bit in the RSCAN0TMCp register is set to 1.
The TMTRM flag is set to 0 when the TMTR bit in the RSCAN0TMCp register is set to 0.

TMTARM Flag (Transmission Buffer Transmission Abort Request Status Flag)

The TMTARM flag is set to 1 when the TMTAR bit in the RSCAN0TMCp register is set to 1.
The TMTARM flag is set to 0 when the TMTAR bit in the RSCAN0TMCp register is set to 0.

35.2.45 Transmission Buffer Transmission Request Status Register 0 (RSCAN0TMTRSTS0)

The RSCAN0TMTRSTS0 register is a status register that indicates requests for the transmission by the transmission buffer.

Address(es): RSCAN.RSCAN0TMTRSTS0 A007 8350h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMTRSTSp (p = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMTRSTSp (p = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMTRSTSp	Transmission Buffer Transmission Request Status Flag p (p = 15 to 0)	0: No transmission request is present. 1: A transmission request is present.	R
b31 to b16	TMTRSTSp	Transmission Buffer Transmission Request Status Flag p (p = 31 to 16)	0: No transmission request is present. 1: A transmission request is present.	R

TMTRSTSp Flags (p = 0 to 31) (Transmission Buffer Transmission Request Status Flags p)

These flags indicate the status of the TMTR bit in the RSCAN0TMCp register (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

When the TMTR bit is set to 1 (transmission is requested), the corresponding TMTRSTSp flag is set to 1.

The corresponding TMTRSTSp flag is cleared to 0 when the TMTR bit is set to 0 (transmission is not requested) or in channel reset mode.

Table 35.5 shows the bit assignment.

Table 35.5 TMTRSTSp Bit Assignment

Bit	Channel	Transmission Buffer Number
0	0	0
1	0	1
. .	. .	. .
15	0	15
16	1	16
. .	. .	. .
30	1	30
31	1	31

35.2.46 Transmission Buffer Transmission Abort Request Status Register 0 (RSCAN0TMTARSTS0)

The RSCAN0TMTARSTS0 register is a status register that indicates requests for aborting transmission by the transmission buffers.

Address(es): RSCAN.RSCAN0TMTARSTS0 A007 8360h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMTARSTSp (p = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMTARSTSp (p = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMTARSTSp	Transmission Buffer Transmission Abort Request Status Flag p (p = 15 to 0)	0: No transmission abort request is present. 1: A transmission abort request is present.	R
b31 to b16	TMTARSTSp	Transmission Buffer Transmission Abort Request Status Flag p (p = 31 to 16)	0: No transmission abort request is present. 1: A transmission abort request is present.	R

TMTARSTSp Flags (Transmission Buffer Transmission Abort Request Status Flags p) (p = 0 to 31)

These flags indicate the status of the TMTAR bit in the RSCAN0TMCp register (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

When the TMTAR bit is set to 1 (transmission abort is requested), the corresponding TMTARSTSp flag is set to 1.

The corresponding TMTARSTSp flag is cleared to 0 when the TMTAR bit is set to 0 (transmission abort is not requested) or in channel reset mode.

Table 35.6 shows the bit assignment.

Table 35.6 TMTARSTSp Bit Assignment

Bit	Channel	Transmission Buffer Number
0	0	0
1	0	1
. .	. .	. .
15	0	15
16	1	16
. .	. .	. .
30	1	30
31	1	31

35.2.47 Transmission Buffer Transmission Complete Status Register 0 (RSCAN0TMTCSTS0)

The RSCAN0TMTCSTS0 register is a status register that indicates requests for the completion of transmission by the transmission buffer.

Address(es): RSCAN.RSCAN0TMTCSTS0 A007 8370h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMTCSTSp (p = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMTCSTSp (p = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMTCSTSp	Transmission Buffer Transmission Complete Status Flag p (p = 15 to 0)	0: Transmission has not been completed. 1: Transmission has been completed.	R
b31 to b16	TMTCSTSp	Transmission Buffer Transmission Complete Status Flag p (p = 31 to 16)	0: Transmission has not been completed. 1: Transmission has been completed.	R

TMTCSTSp Flags (Transmission Buffer Transmission Complete Status Flags p) (p = 0 to 31)

When the TMTRF[1:0] flag in the RSCAN0TMSTSp register is set to 10b (transmission has been completed (without transmission abort request)) or 11b (transmission has been completed (with transmission abort request)), the corresponding TMTCSTSp flag is set to 1 (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).
A TMTCSTSp flag is cleared to 0 when the corresponding TMTRF[1:0] flag is set to 00b or in channel reset mode.
Table 35.7 shows the bit assignment.

Table 35.7 TMTCSTSp Bit Assignment

Bit	Channel	Transmission Buffer Number
0	0	0
1	0	1
. .	. .	. .
15	0	15
16	1	16
. .	. .	. .
30	1	30
31	1	31

35.2.48 Transmission Buffer Transmission Abort Status Register 0 (RSCAN0TMTASTS0)

The RSCAN0TMTASTS0 register is a status register that indicates requests for aborting transmission by the transmission buffers.

Address(es): RSCAN.RSCAN0TMTASTS0 A007 8380h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMTASTSp (p = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMTASTSp (p = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMTASTSp	Transmission Buffer Transmission Abort Status Flag p (p = 15 to 0)	0: Transmission is not aborted. 1: Transmission is aborted.	R
b31 to b16	TMTASTSp	Transmission Buffer Transmission Abort Status Flag p (p = 31 to 16)	0: Transmission is not aborted 1: Transmission is aborted	R

TMTASTSp Flags (Transmission Buffer Transmission Abort Status Flags p) (p = 0 to 31)

When the TMTRF[1:0] flag in the RSCAN0TMSTSp register is set to 01b (transmission abort has been completed), the corresponding TMTASTSp flag is set to 1 (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

A TMTASTSp flag is cleared to 0 when the corresponding TMTRF[1:0] flag is set to 00b or in channel reset mode.

Table 35.8 shows the bit assignment.

Table 35.8 TMTASTSp Bit Assignment

Bit	Channel	Transmission Buffer Number
0	0	0
1	0	1
. .	. .	. .
15	0	15
16	1	16
. .	. .	. .
30	1	30
31	1	31

35.2.49 Transmission Buffer Interrupt Enable Configuration Register 0 (RSCAN0TMIEC0)

The RSCAN0TMIEC0 register enables or disables requests for transmission buffer interrupts.

Address(es): RSCAN.RSCAN0TMIEC0 A007 8390h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TMIEp (p = 31 to 16)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TMIEp (p = 15 to 0)															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	TMIEp	Transmission Buffer Interrupt Enable p (p = 15 to 0)	0: Transmission buffer interrupt is disabled. 1: Transmission buffer interrupt is enabled.	R/W
b31 to b16	TMIEp	Transmission Buffer Interrupt Enable p (p = 31 to 16)	0: Transmission buffer interrupt is disabled 1: Transmission buffer interrupt is enabled	R/W

TMIEp Bits (Transmission Buffer Interrupt Enable p) (p = 0 to 31)

When any of these bits is set to 1 and the corresponding transmission has been completed, a CANm transmission interrupt request (transmission buffer interrupt) is generated (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).
Modify these bits when the TMTRM flag in the corresponding RSCAN0TMSTSp register is 0 (no transmission request is present).
Write 0 to bits corresponding to transmission buffers linked to transmission/reception FIFO buffers or transmission buffers allocated to the transmission queue.
Table 35.9 shows the bit assignment.

Table 35.9 TMIEp Bit Assignment

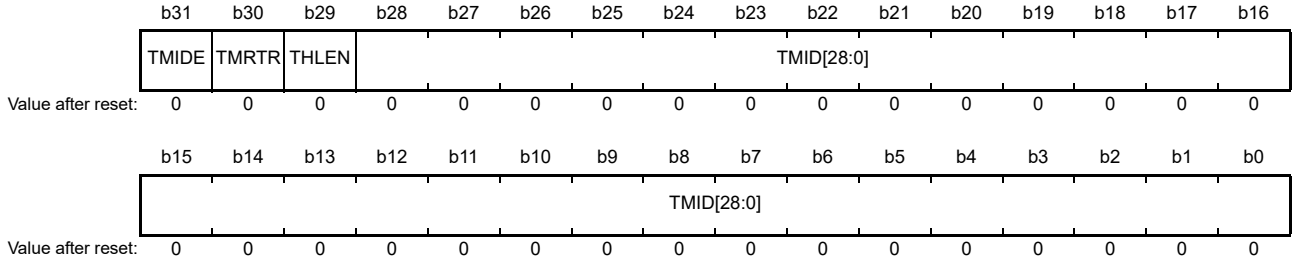
Bit	Channel	Transmission Buffer Number
0	0	0
1	0	1
. .	. .	. .
15	0	15
16	1	16
. .	. .	. .
30	1	30
31	1	31

35.2.50 Transmission Buffer ID Registers (RSCAN0TMIDp) (p = 0 to 31)

The RSCAN0TMIDp registers control the ID and data formats of the messages for transmission (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Modify these registers when the TMTRM bit in the corresponding RSCAN0TMSTSp register is set to 0 (no transmission request is present). If these registers are linked to transmission/reception FIFO buffers, do not write data to them. If these registers are allocated to the transmission queue, write data only to transmission buffers p (p = m × 16 + 15) for the corresponding channel m (m = 0, 1).

Address(es): RSCAN.RSCAN0TMID0 A007 9000h, RSCAN.RSCAN0TMID1 A007 9010h, RSCAN.RSCAN0TMID2 A007 9020h, RSCAN.RSCAN0TMID3 A007 9030h, RSCAN.RSCAN0TMID4 A007 9040h, RSCAN.RSCAN0TMID5 A007 9050h, RSCAN.RSCAN0TMID6 A007 9060h, RSCAN.RSCAN0TMID7 A007 9070h, RSCAN.RSCAN0TMID8 A007 9080h, RSCAN.RSCAN0TMID9 A007 9090h, RSCAN.RSCAN0TMID10 A007 90A0h, RSCAN.RSCAN0TMID11 A007 90B0h, RSCAN.RSCAN0TMID12 A007 90C0h, RSCAN.RSCAN0TMID13 A007 90D0h, RSCAN.RSCAN0TMID14 A007 90E0h, RSCAN.RSCAN0TMID15 A007 90F0h, RSCAN.RSCAN0TMID16 A007 9100h, RSCAN.RSCAN0TMID17 A007 9110h, RSCAN.RSCAN0TMID18 A007 9120h, RSCAN.RSCAN0TMID19 A007 9130h, RSCAN.RSCAN0TMID20 A007 9140h, RSCAN.RSCAN0TMID21 A007 9150h, RSCAN.RSCAN0TMID22 A007 9160h, RSCAN.RSCAN0TMID23 A007 9170h, RSCAN.RSCAN0TMID24 A007 9180h, RSCAN.RSCAN0TMID25 A007 9190h, RSCAN.RSCAN0TMID26 A007 91A0h, RSCAN.RSCAN0TMID27 A007 91B0h, RSCAN.RSCAN0TMID28 A007 91C0h, RSCAN.RSCAN0TMID29 A007 91D0h, RSCAN.RSCAN0TMID30 A007 91E0h, RSCAN.RSCAN0TMID31 A007 91F0h



Bit	Symbol	Bit Name	Description	R/W
b28 to b0	TMID[28:0]	Transmission Buffer ID Data Configuration	Set standard ID or extended ID. For standard ID, write an ID to bits 10 to 0 and write 0 to bits 28 to 11.	R/W
b29	THLEN	Transmission History Data Storage Enable	0: Transmission history data is not stored in the buffer. 1: Transmission history data is stored in the buffer.	R/W
b30	TMRTR	Transmission Buffer RTR	0: Data frame 1: Remote frame	R/W
b31	TMIDE	Transmission Buffer IDE	0: Standard ID 1: Extended ID	R/W

TMID[28:0] Bits (Transmission Buffer ID Data Configuration)

These bits are used to set the ID of the message to be transmitted from the transmission buffer.

THLEN Bit (Transmission History Data Storage Enable)

With this bit set to 1, the transmission history data of the message transmitted (label information and the number and type) are stored in the transmission history buffer after transmission is completed.

TMRTR Bit (Transmission Buffer RTR)

This bit is used to set the data format of the message to be transmitted from the transmission buffer.

TMIDE Bit (Transmission Buffer IDE)

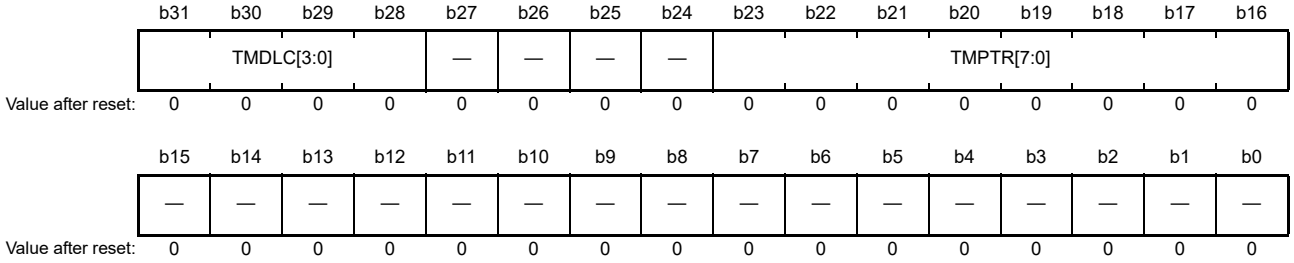
This bit is used to set the ID format of the message to be transmitted from the transmission buffer.

35.2.51 Transmission Buffer Pointer Registers (RSCAN0TMPTRp) (p = 0 to 31)

The RSCAN0TMPTRp registers control the data length and label information for the messages for transmission (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Modify these registers when the TMTRM bit in the corresponding RSCAN0TMSTSp register is set to 0 (no transmission request is present). If these registers are linked to transmission/reception FIFO buffers, do not write data to them. If these registers are allocated to the transmission queue, write data only to transmission buffers p (p = m × 16 + 15) for the corresponding channel m (m = 0, 1).

Address(es): RSCAN.RSCAN0TMPTR0 A007 9004h, RSCAN.RSCAN0TMPTR1 A007 9014h, RSCAN.RSCAN0TMPTR2 A007 9024h, RSCAN.RSCAN0TMPTR3 A007 9034h, RSCAN.RSCAN0TMPTR4 A007 9044h, RSCAN.RSCAN0TMPTR5 A007 9054h, RSCAN.RSCAN0TMPTR6 A007 9064h, RSCAN.RSCAN0TMPTR7 A007 9074h, RSCAN.RSCAN0TMPTR8 A007 9084h, RSCAN.RSCAN0TMPTR9 A007 9094h, RSCAN.RSCAN0TMPTR10 A007 90A4h, RSCAN.RSCAN0TMPTR11 A007 90B4h, RSCAN.RSCAN0TMPTR12 A007 90C4h, RSCAN.RSCAN0TMPTR13 A007 90D4h, RSCAN.RSCAN0TMPTR14 A007 90E4h, RSCAN.RSCAN0TMPTR15 A007 90F4h, RSCAN.RSCAN0TMPTR16 A007 9104h, RSCAN.RSCAN0TMPTR17 A007 9114h, RSCAN.RSCAN0TMPTR18 A007 9124h, RSCAN.RSCAN0TMPTR19 A007 9134h, RSCAN.RSCAN0TMPTR20 A007 9144h, RSCAN.RSCAN0TMPTR21 A007 9154h, RSCAN.RSCAN0TMPTR22 A007 9164h, RSCAN.RSCAN0TMPTR23 A007 9174h, RSCAN.RSCAN0TMPTR24 A007 9184h, RSCAN.RSCAN0TMPTR25 A007 9194h, RSCAN.RSCAN0TMPTR26 A007 91A4h, RSCAN.RSCAN0TMPTR27 A007 91B4h, RSCAN.RSCAN0TMPTR28 A007 91C4h, RSCAN.RSCAN0TMPTR29 A007 91D4h, RSCAN.RSCAN0TMPTR30 A007 91E4h, RSCAN.RSCAN0TMPTR31 A007 91F4h



Bit	Symbol	Bit Name	Description	R/W
b15 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23 to b16	TMPTR[7:0]	Transmission Buffer Label Data Configuration	Set the label information to be stored in the transmission history buffer.	R/W
b27 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b28	TMDLC[3:0]	Transmission Buffer DLC Data Configuration	b31 b30 b29 b28 0 0 0 0: 0 data bytes 0 0 0 1: 1 data byte 0 0 1 0: 2 data bytes 0 0 1 1: 3 data bytes 0 1 0 0: 4 data bytes 0 1 0 1: 5 data bytes 0 1 1 0: 6 data bytes 0 1 1 1: 7 data bytes 1 X X X: 8 data bytes	R/W

TMPTR[7:0] Bits (Transmission Buffer Label Data Configuration)

When message transmission has been completed, the TMPTR[7:0] value is stored in the transmission history buffer.

TMDLC[3:0] Bits (Transmission Buffer DLC Data Configuration)

These bits are used to set the data length of the message to be transmitted from the transmission buffer when the TMRTR bit in the RSCAN0TMIDp register is set to 0 (data frame). If the data length is set to 9 bytes or more, the transmit data is 8 bytes long.

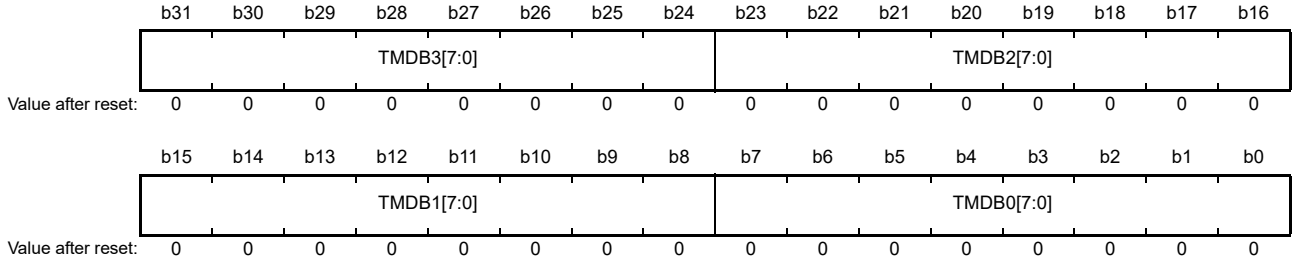
When the TMRTR bit is set to 1 (remote frame), set the data length of messages to be requested.

35.2.52 Transmission Buffer Data Field 0 Registers (RSCAN0TMDF0p) (p = 0 to 31)

The RSCAN0TMDF0p registers are data registers for writing data for transmission from the transmission buffer (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Modify these registers when the TMTRM bit in the corresponding RSCAN0TMSTSp register is set to 0 (no transmission request is present). If these registers are linked to transmission/reception FIFO buffers, do not write data to them. If these registers are allocated to the transmission queue, write data only to transmission buffers p (p = m × 16 + 15) for the corresponding channel m (m = 0, 1).

Address(es): RSCAN.RSCAN0TMDF00 A007 9008h, RSCAN.RSCAN0TMDF01 A007 9018h, RSCAN.RSCAN0TMDF02 A007 9028h, RSCAN.RSCAN0TMDF03 A007 9038h, RSCAN.RSCAN0TMDF04 A007 9048h, RSCAN.RSCAN0TMDF05 A007 9058h, RSCAN.RSCAN0TMDF06 A007 9068h, RSCAN.RSCAN0TMDF07 A007 9078h, RSCAN.RSCAN0TMDF08 A007 9088h, RSCAN.RSCAN0TMDF09 A007 9098h, RSCAN.RSCAN0TMDF010 A007 90A8h, RSCAN.RSCAN0TMDF011 A007 90B8h, RSCAN.RSCAN0TMDF012 A007 90C8h, RSCAN.RSCAN0TMDF013 A007 90D8h, RSCAN.RSCAN0TMDF014 A007 90E8h, RSCAN.RSCAN0TMDF015 A007 90F8h, RSCAN.RSCAN0TMDF016 A007 9108h, RSCAN.RSCAN0TMDF017 A007 9118h, RSCAN.RSCAN0TMDF018 A007 9128h, RSCAN.RSCAN0TMDF019 A007 9138h, RSCAN.RSCAN0TMDF020 A007 9148h, RSCAN.RSCAN0TMDF021 A007 9158h, RSCAN.RSCAN0TMDF022 A007 9168h, RSCAN.RSCAN0TMDF023 A007 9178h, RSCAN.RSCAN0TMDF024 A007 9188h, RSCAN.RSCAN0TMDF025 A007 9198h, RSCAN.RSCAN0TMDF026 A007 91A8h, RSCAN.RSCAN0TMDF027 A007 91B8h, RSCAN.RSCAN0TMDF028 A007 91C8h, RSCAN.RSCAN0TMDF029 A007 91D8h, RSCAN.RSCAN0TMDF030 A007 91E8h, RSCAN.RSCAN0TMDF031 A007 91F8h



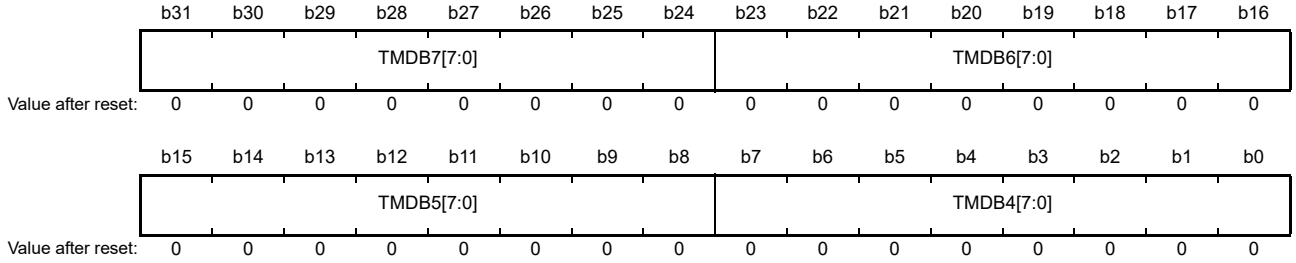
Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB0[7:0]	Transmission Buffer Data Byte 0	Set the transmission buffer data.	R/W
b15 to b8	TMDB1[7:0]	Transmission Buffer Data Byte 1		R/W
b23 to b16	TMDB2[7:0]	Transmission Buffer Data Byte 2		R/W
b31 to b24	TMDB3[7:0]	Transmission Buffer Data Byte 3		R/W

35.2.53 Transmission Buffer Data Field 1 Registers (RSCAN0TMDF1p) (p = 0 to 31)

The RSCAN0TMDF1p registers are data registers for writing data for transmission from the transmission buffer (p = 0 to 15 for channel 0; p = 16 to 31 for channel 1).

Modify these registers when the TMTRM bit in the corresponding RSCAN0TMSTSp register is set to 0 (no transmission request is present). If these registers are linked to transmission/reception FIFO buffers, do not write data to them. If these registers are allocated to the transmission queue, write data only to transmission buffers p (p = m × 16 + 15) for the corresponding channel m (m = 0, 1).

Address(es): RSCAN.RSCAN0TMDF10 A007 900Ch, RSCAN.RSCAN0TMDF11 A007 901Ch, RSCAN.RSCAN0TMDF12 A007 902Ch, RSCAN.RSCAN0TMDF13 A007 903Ch, RSCAN.RSCAN0TMDF14 A007 904Ch, RSCAN.RSCAN0TMDF15 A007 905Ch, RSCAN.RSCAN0TMDF16 A007 906Ch, RSCAN.RSCAN0TMDF17 A007 907Ch, RSCAN.RSCAN0TMDF18 A007 908Ch, RSCAN.RSCAN0TMDF19 A007 909Ch, RSCAN.RSCAN0TMDF110 A007 90ACh, RSCAN.RSCAN0TMDF111 A007 90BCh, RSCAN.RSCAN0TMDF112 A007 90CCh, RSCAN.RSCAN0TMDF113 A007 90DCh, RSCAN.RSCAN0TMDF114 A007 90ECh, RSCAN.RSCAN0TMDF115 A007 90FCh, RSCAN.RSCAN0TMDF116 A007 910Ch, RSCAN.RSCAN0TMDF117 A007 911Ch, RSCAN.RSCAN0TMDF118 A007 912Ch, RSCAN.RSCAN0TMDF119 A007 913Ch, RSCAN.RSCAN0TMDF120 A007 914Ch, RSCAN.RSCAN0TMDF121 A007 915Ch, RSCAN.RSCAN0TMDF122 A007 916Ch, RSCAN.RSCAN0TMDF123 A007 917Ch, RSCAN.RSCAN0TMDF124 A007 918Ch, RSCAN.RSCAN0TMDF125 A007 919Ch, RSCAN.RSCAN0TMDF126 A007 91ACh, RSCAN.RSCAN0TMDF127 A007 91BCh, RSCAN.RSCAN0TMDF128 A007 91CCh, RSCAN.RSCAN0TMDF129 A007 91DCh, RSCAN.RSCAN0TMDF130 A007 91ECh, RSCAN.RSCAN0TMDF131 A007 91FCh



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TMDB4[7:0]	Transmission Buffer Data Byte 4	Set the transmission buffer data.	R/W
b15 to b8	TMDB5[7:0]	Transmission Buffer Data Byte 5		R/W
b23 to b16	TMDB6[7:0]	Transmission Buffer Data Byte 6		R/W
b31 to b24	TMDB7[7:0]	Transmission Buffer Data Byte 7		R/W

35.2.54 Transmission Queue Configuration and Control Registers (RSCAN0TXQCCm) (m = 0, 1)

The RSCAN0TXQCCm registers control the settings for the transmission queue of each channel.

Address(es): RSCAN.RSCAN0TXQCC0 A007 83A0h, RSCAN.RSCAN0TXQCC1 A007 83A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TXQIM	TXQIE	TXQDC[3:0]				—	—	—	—	—	—	—	TXQE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TXQE	Transmission Queue Enable	0: The transmission queue is not used. 1: The transmission queue is used.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	TXQDC[3:0]	Transmission Queue Depth Configuration	Setting these bits to g (g = 2 to 15) makes the (g + 1)-buffer transmission queue available. Setting these bits to 0 disables the transmission queue. Setting these bits to 1 is prohibited.	R/W
b12	TXQIE	Transmission Queue Interrupt Enable	0: Transmission queue interrupt is disabled. 1: Transmission queue interrupt is enabled.	R/W
b13	TXQIM	Transmission Queue Interrupt Source Select	0: When the transmission queue becomes empty upon completion of message transmission, a transmission queue interrupt request is generated. 1: A transmission queue interrupt request is generated each time a message has been transmitted.	R/W
b31 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TXQE Bit (Transmission Queue Enable)

Setting this bit to 1 makes the transmission queue available. Modify this bit in channel communication mode or channel halt mode. This bit is cleared to 0 in channel reset mode.

Before setting the TXQE bit to 1, set the TXQDC[3:0] bits to 0010b or more.

TXQDC[3:0] Bits (Transmission Queue Depth Configuration)

These bits are used to specify the number of transmission buffers to be allocated to the transmission queues. Transmission buffers are allocated to transmission queues in descending order of buffer number, that is, from 15 to 0 (CAN0) or 31 to 16 (CAN1), as shown in Table 35.10. For examples of how buffer allocation is done, see Figure 35.9 in section 35.6, Transmission Functions. Modify these bits only in channel reset mode.

Table 35.10 Transmission Buffers p Allocated to the Transmission Queue of Each Channel

	Transmission Buffers p Allocated to the Transmission Queue (p = 0 to 31)	
Settings of TXQDC[3:0] Bits	**Channel 0 (m = 0)**	**Channel 1 (m = 1)**
0000b	Setting prohibited	Setting prohibited
0001b	Setting prohibited	Setting prohibited
0010b	Transmission buffers 15 to 13	Transmission buffers 31 to 29
0011b	Transmission buffers 15 to 12	Transmission buffers 31 to 28
0100b	Transmission buffers 15 to 11	Transmission buffers 31 to 27
0101b	Transmission buffers 15 to 10	Transmission buffers 31 to 26
0110b	Transmission buffers 15 to 9	Transmission buffers 31 to 25
0111b	Transmission buffers 15 to 8	Transmission buffers 31 to 24
1000b	Transmission buffers 15 to 7	Transmission buffers 31 to 23
1001b	Transmission buffers 15 to 6	Transmission buffers 31 to 22
1010b	Transmission buffers 15 to 5	Transmission buffers 31 to 21
1011b	Transmission buffers 15 to 4	Transmission buffers 31 to 20
1100b	Transmission buffers 15 to 3	Transmission buffers 31 to 19
1101b	Transmission buffers 15 to 2	Transmission buffers 31 to 18
1110b	Transmission buffers 15 to 1	Transmission buffers 31 to 17
1111b	Transmission buffers 15 to 0	Transmission buffers 31 to 16

TXQIE Bit (Transmission Queue Interrupt Enable)

When the TXQIE bit is set to 1 and the source selected by the TXQIM bit occurs, a CANm transmission interrupt request (transmission queue interrupt) is generated.
Set the TXQE bit to 0 before modifying the TXQIE bit.

TXQIM Bit (Transmission Queue Interrupt Source Select)

This bit is used to select a transmission queue interrupt source. Modify this bit in channel reset mode.

35.2.55 Transmission Queue Status Registers (RSCAN0TXQSTSm) (m = 0, 1)

The RSCAN0TXQSTSm registers are status registers that indicate the state of the transmission queue.

Address(es): RSCAN.RSCAN0TXQSTS0 A007 83C0h, RSCAN.RSCAN0TXQSTS1 A007 83C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TXQIF	TXQFLL	TXQEMP
Value after reset:	0	0	0	x	x	x	x	x	0	0	0	0	0	0	0	1

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	TXQEMP	Transmission Queue Empty Status Flag	0: The transmission queue contains messages. 1: The transmission queue contains no message (transmission queue empty).	R
b1	TXQFLL	Transmission Queue Full Status Flag	0: The transmission queue is not full. 1: The transmission queue is full.	R
b2	TXQIF	Transmission Queue Interrupt Request Flag	0: No transmission queue interrupt request is present. 1: A transmission queue interrupt request is present.	R/W *1
b7 to b3	—	Reserved	These bits are read as 0.	R
b12 to b8	—	Reserved	These bits are read as an undefined value.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

TXQEMP Flag (Transmission Queue Empty Status Flag)

The TXQEMP flag is cleared to 0 when even a single message is set for the transmission queue.
This flag is set to 1 in any of the following cases.

- The TXQE bit is set to 0 (the transmission queue is not used).
- The transmission queue becomes empty.
- In channel reset mode

TXQFLL Flag (Transmission Queue Full Status Flag)

The TXQFLL flag is set to 1 when the number of messages set for the transmission queue matches the transmission queue depth set by the TXQDC[3:0] bits in the RSCAN0TXQCCm register.
This flag is cleared to 0 in any of the following cases.

- The number of messages set for the transmission queue is smaller than the transmission queue depth set by the TXQDC[3:0] bits.
- In channel reset mode

TXQIF Flag (Transmission Queue Interrupt Request Flag)

The TXQIF flag is set to 1 when the event specified by the TXQIM bit in the RSCAN0TXQCCm register has occurred. The TXQIF flag is cleared to 0 in channel reset mode or by writing 0 to this flag. This flag is not cleared to 0 by setting the TXQE bit in the RSCAN0TXQCCm register to 0 (the transmission queue is not used).

35.2.56 Transmission Queue Pointer Control Registers (RSCAN0TXQPCTRm) (m = 0, 1)

The RSCAN0TXQPCTRm registers control the pointers to the transmission queue.

Address(es): RSCAN.RSCAN0TXQPCTR0 A007 83E0h, RSCAN.RSCAN0TXQPCTR1 A007 83E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TXQPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TXQPC[7:0]	Transmission Queue Pointer Control	Writing FFh to these bits moves the write pointer to the transmission queue to the next queue buffer.	W
b31 to b8	—	Reserved	The write value should be 0.	W

TXQPC[7:0] Bits (Transmission Queue Pointer Control)

Writing FFh to the TXQPC[7:0] bits moves the write pointer to the next transmission queue buffer and generates a transmission request of the message. Write messages for transmission to the RSCAN0TMIDp, RSCAN0TMPTRp, RSCAN0TMDF0p, and RSCAN0TMDF1p registers (p = 15, 31) before writing FFh to the TXQPC[7:0] bits.
When writing FFh to these bits, make sure that the TXQE bit in the RSCAN0TXQCCm register is set to 1 (the transmission queue is used) and the TXQFLL flag in the RSCAN0TXQSTSm register is 0 (the transmission queue is not full).

35.2.57 Transmission History Configuration and Control Registers (RSCAN0THLCCm) (m = 0, 1)

The RSCAN0THLCCm registers control the settings for transmission history.

Address(es): RSCAN.RSCAN0THLCC0 A007 8400h, RSCAN.RSCAN0THLCC1 A007 8404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	THLDTE	THLIM	THLIE	—	—	—	—	—	—	—	THLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	THLE	Transmission History Buffer Enable	0: Transmission history buffer is not used. 1: Transmission history buffer is used.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	THLIE	Transmission History Interrupt Enable	0: Transmission history interrupt is disabled. 1: Transmission history interrupt is enabled.	R/W
b9	THLIM	Transmission History Interrupt Source Select	0: When 12 sets of data have been stored in the transmission history buffer 1: When a single set of transmission history data has been stored	R/W
b10	THLDTE	Transmission History Target Buffer Select	0: Entry from transmission/reception FIFO buffers and transmission queue 1: Entry from transmission buffers, transmission/reception FIFO buffers, and transmission queue	R/W
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

THLE Bit (Transmission History Buffer Enable)

Setting this bit to 1 makes the transmission history buffer available. When data transmission from the buffer selected by the THLDTE bit has been completed, the transmission history data of transmitted messages is stored in the transmission history buffer.

Modify this bit in channel communication mode or channel halt mode.

THLIE Bit (Transmission History Interrupt Enable)

When the THLIE bit is set to 1 and the source selected by the THLIM bit has occurred, a CANm transmission interrupt request (transmission history interrupt) is generated. Modify the THLIE bit only when the THLE bit set to 0.

THLIM Bit (Transmission History Interrupt Source Select)

This bit is used to select a transmission history interrupt source.

Modify this bit only in channel reset mode.

THLDTE Bit (Transmission History Target Buffer Select)

When this bit is set to 0, the transmission history data of messages transmitted from transmission/reception FIFO buffers and the transmission queue is stored in the transmission history buffer. When this bit is set to 1, the transmission history data of messages transmitted from transmission buffers, transmission/reception FIFO buffers, and the transmission queue is stored in the transmission history buffer.

Modify this bit only in channel reset mode.

35.2.58 Transmission History Status Registers (RSCAN0THLSTSm) (m = 0, 1)

The RSCAN0THLSTSm registers are status registers that indicate the state of transmission history.

Address(es): RSCAN.RSCAN0THLSTS0 A007 8420h, RSCAN.RSCAN0THLSTS1 A007 8424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	THLMC[4:0]					—	—	—	—	THLIF	THLELT	THLFLL	THLEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	THLEMP	Transmission History Buffer Empty Status Flag	0: Transmission history buffer contains unread data. 1: Transmission history buffer contains no unread data (buffer empty).	R
b1	THLFLL	Transmission History Buffer Full Status Flag	0: Transmission history buffer is not full. 1: Transmission history buffer is full.	R
b2	THLELT	Transmission History Buffer Overflow Flag	0: Transmission history buffer overflow has not occurred. 1: Transmission history buffer overflow has occurred.	R/W *1
b3	THLIF	Transmission History Interrupt Request Flag	0: No transmission history interrupt request is present. 1: A transmission history interrupt request is present.	R/W *1
b7 to b4	—	Reserved	These bits are read as 0.	R
b12 to b8	THLMC[4:0]	Transmission History Buffer Unread Data Counter	These bits indicate the number of unread data sets stored in the transmission history buffer.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

Note 1. The only effective value for writing to this flag bit is 0, which clears the bit. Otherwise writing to the bit results in retention of its state.

THLEMP Flag (Transmission History Buffer Empty Status Flag)

The THLEMP flag is cleared to 0 when even a single set of transmission history data has been stored in the transmission history buffer.

This flag is set to 1 when all the data in the transmission history buffer has been read. This flag is also set to 1 in channel reset mode or when the THLE bit in the RSCAN0THLCCm register is set to 0 (the transmission history buffer is not used).

THLFLL Flag (Transmission History Buffer Full Status Flag)

The THLFLL flag is set to 1 when 16 data sets have been stored in the transmission history buffer, and is cleared to 0 when the number of data sets stored in the transmission history buffer has decreased to less than 16. This bit is also cleared to 0 in channel reset mode or when the THLE bit in the RSCAN0THLCCm register is set to 0 (the transmission history buffer is not used).

THLELT Flag (Transmission History Buffer Overflow Flag)

The THLELT flag is set to 1 when an attempt is made to store new transmission history data while the transmission history buffer is full. In this case, the new data is discarded. This flag becomes 0 in channel reset mode or by the program writing 0 to this flag.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared.

When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

THLIF Flag (Transmission History Interrupt Request Flag)

The THLIF flag is set to 1 when the interrupt source specified with the THLIM bit in the RSCAN0THLCCm register occurs.

This flag is cleared to 0 in channel reset mode or by the program writing 0 to this flag.

To clear the flags of the register to 0, the program must write 0 to the corresponding flag to be cleared.

When writing 0, using store instruction, set the bit to be set to “0” to “0”, and the bits not to be set to “0” to “1”.

THLMC[4:0] Bits (Transmission History Buffer Unread Data Counter)

These bits indicate the number of unread data sets stored in the transmission history buffer.

35.2.59 Transmission History Access Registers (RSCAN0THLACCm) (m = 0, 1)

The RSCAN0THLACCm registers are status registers that indicate the contents of the transmission history data held in the transmission history buffer.

Address(es): RSCAN.RSCAN0THLACC0 A007 9800h, RSCAN.RSCAN0THLACC1 A007 9804h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TID[7:0]								—	BN[3:0]				BT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	BT[2:0]	Buffer Type Data Indication	b2 b1 b0 0 0 1: Transmission buffer 0 1 0: Transmission/reception FIFO buffer 1 0 0: Transmission queue	R
b6 to b3	BN[3:0]	Buffer Number Data Indication	The buffer number of transmit source (transmission buffer, transmit/receive FIFO or transmission queue) can be read.	R
b7	—	Reserved	This bit is read as 0.	R
b15 to b8	TID[7:0]	Label Data Indication	The label information of stored data can be read.	R
b31 to b16	—	Reserved	These bits are read as 0.	R

BT[2:0] Bits (Buffer Type Data Indication)

These bits indicate the type of the transmit source buffer in the transmission history data stored in the transmission history buffer.

BN[3:0] Bits (Buffer Number Data Indication)

These bits indicate the transmit source buffer number in the transmission history data stored in the transmission history buffer.

TID[7:0] Bits (Label Data Indication)

These bits indicate the label information of transmission history data stored in the transmission history buffer.

35.2.60 Transmission History Pointer Control Registers (RSCAN0THLPCTRm) (m = 0, 1)

The RSCAN0THLPCTRm registers control the pointers to the transmission history buffer.

Address(es): RSCAN.RSCAN0THLPCTR0 A007 8440h, RSCAN.RSCAN0THLPCTR1 A007 8444h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	THLPC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	THLPC[7:0]	Transmission History List Pointer Control	Writing FFh to these bits moves the read pointer to the next unread data in the transmission history buffer.	W
b31 to b8	—	Reserved	The write value should be 0.	W

THLPC[7:0] Bits (Transmission History List Pointer Control)

When the THLPC[7:0] bits are set to FFh, the read pointer moves to the next data in the transmission history buffer. At this time, the THLMC[4:0] (transmission history buffer unread data counter) value in the RSCAN0THLSTSm register is decremented. Write FFh to the THLPC[7:0] bits after reading from the RSCAN0THLACCm register.

When writing FFh to these bits, make sure that the THLE bit in the RSCAN0THLCCm register is set to 1 (the transmission history buffer is used) and the THLEMP flag in the RSCAN0THLSTSm register is 0.

35.2.61 Global Test Configuration Register (RSCAN0GTSTCFG)

The RSCAN0GTSTCFG register controls the test settings for the entire RSCAN module.
Modify the RSCAN0GTSTCFG register only in global test mode.

Address(es): RSCAN.RSCAN0GTSTCFG A007 8468h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	RTMPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	C1ICBCE	C0ICBCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	C0ICBCE	CAN0 Inter-Channel Communication Test Enable	0: CAN0 inter-channel communication test is disabled. 1: CAN0 inter-channel communication test is enabled.	R/W
b1	C1ICBCE	CAN1 Inter-Channel Communication Test Enable	0: CAN1 inter-channel communication test is disabled. 1: CAN1 inter-channel communication test is enabled.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22 to b16	RTMPS[6:0]	RAM Test Page Configuration	Set a value within a range of page 0 (00h) to page 28 (1Ch).	R/W
b31 to b23	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

C0ICBCE Bit (CAN0 Inter-Channel Communication Test Enable)

Setting this bit to 1 enables the channel 0 inter-channel communication test.

C1ICBCE Bit (CAN1 Inter-Channel Communication Test Enable)

Setting this bit to 1 enables the channel 1 inter-channel communication test.

RTMPS[6:0] Bits (RAM Test Page Configuration)

These bits are used to set the RAM test target page number for RAM test. Set a value in the range of 00h to 1Ch, inclusive.

35.2.62 Global Test Control Register (RSCAN0GTSTCTR)

The RSCAN0GTSTCTR register controls operations for the RAM test and inter-channel communication test.

Address(es): RSCAN.RSCAN0GTSTCTR A007 846Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RTME	—	ICBCTME
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ICBCTME	Inter-Channel Communication Test Enable	0: Inter-channel communication test disabled 1: Inter-channel communication test enabled	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	RTME	RAM Test Enable	0: RAM test is disabled. 1: RAM test is enabled.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ICBCTME Bit (Inter-Channel Communication Test Enable)

When this bit is set to 1, a communication test is enabled between the channels for which the CmICBCE bit (m = 0, 1) in the RSCAN0GTSTCFG register has been set to 1. Modify the ICBCTME bit only in global test mode.

RTME Bit (RAM Test Enable)

Setting this bit to 1 enables the RAM test. Modify this bit only in global test mode.

1. Set the GMDC[1:0] bits in the RSCAN0GCTR register to 10b (Global test mode).
2. Set the RTME bit to 1.
3. Check that the RTME bit is set to 1.

For writing the RTME bit, unlock the write protection on this bit by the global lock key register (RSCAN0GLOCKK).

35.2.63 Global Lock Key Register (RSCAN0GLOCKK)

The RSCAN0GLOCKK register unlocks protection of the special test bit and is write only.
For the protection unlock data, see section 35.9.4.2, Procedure for Unlocking the Protection.

Address(es): RSCAN.RSCAN0GLOCKK A007 847Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LOCK[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	LOCK[15:0]	Lock Key	These bits are key bits to unlock protection of test mode.	W*1
b31 to b16	—	Reserved	The write value should be 0.	W

Note 1. Writing to these bits is effective only when the RSCAN module is in global test mode.

LOCK[15:0] Bits (Lock Key)

Writing the sequence of protection unlock data to the LOCK[15:0] bits enables writing 1 to the RTME bit in the RSCAN0GTSTCTR register.
After the protection has been unlocked, writing to the I/O register area (A007 8000h to A007 84FFh) of the CAN (i.e. to a location that is not in the RAM) leads to re-enabling of protection.
Reading from the I/O register area of the CAN or reading from or writing to other areas does not lead to re-enabling of protection.

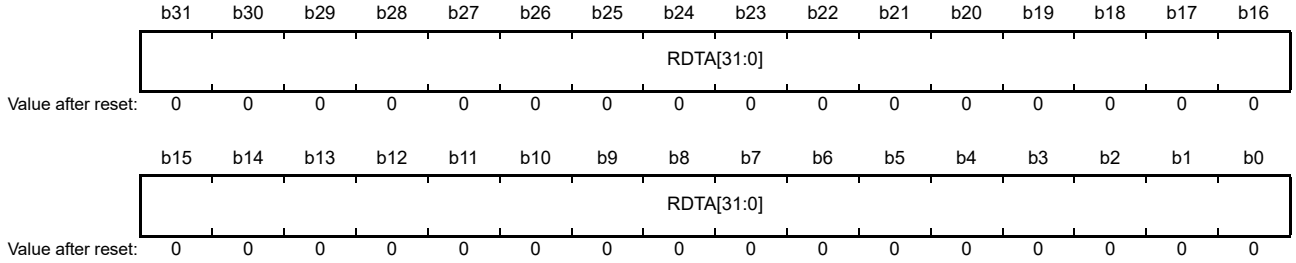
35.2.64 RAM Test Page Access Registers (RSCAN0RPGACCr) (r = 0 to 63)

The RSCAN0RPGACCr register controls test access to RAM data.

Modify the RSCAN0RPGACCr register in global test mode with the RTME bit in the RSCAN0GTSTCTR register set to 1 (RAM test is enabled).

The RSCAN0RPGACCr register is readable and writable when the RTME bit is set to 1.

Address(es): RSCAN.RSCAN0RPGACC0 A007 9900h, RSCAN.RSCAN0RPGACC1 A007 9904h,
RSCAN.RSCAN0RPGACC2 A007 9908h, RSCAN.RSCAN0RPGACC3 A007 990Ch,
RSCAN.RSCAN0RPGACC4 A007 9910h, RSCAN.RSCAN0RPGACC5 A007 9914h,
RSCAN.RSCAN0RPGACC6 A007 9918h, RSCAN.RSCAN0RPGACC7 A007 991Ch,
RSCAN.RSCAN0RPGACC8 A007 9920h, RSCAN.RSCAN0RPGACC9 A007 9924h,
RSCAN.RSCAN0RPGACC10 A007 9928h, RSCAN.RSCAN0RPGACC11 A007 992Ch,
RSCAN.RSCAN0RPGACC12 A007 9930h, RSCAN.RSCAN0RPGACC13 A007 9934h,
RSCAN.RSCAN0RPGACC14 A007 9938h, RSCAN.RSCAN0RPGACC15 A007 993Ch,
RSCAN.RSCAN0RPGACC16 A007 9940h, RSCAN.RSCAN0RPGACC17 A007 9944h,
RSCAN.RSCAN0RPGACC18 A007 9948h, RSCAN.RSCAN0RPGACC19 A007 994Ch,
RSCAN.RSCAN0RPGACC20 A007 9950h, RSCAN.RSCAN0RPGACC21 A007 9954h,
RSCAN.RSCAN0RPGACC22 A007 9958h, RSCAN.RSCAN0RPGACC23 A007 995Ch,
RSCAN.RSCAN0RPGACC24 A007 9960h, RSCAN.RSCAN0RPGACC25 A007 9964h,
RSCAN.RSCAN0RPGACC26 A007 9968h, RSCAN.RSCAN0RPGACC27 A007 996Ch,
RSCAN.RSCAN0RPGACC28 A007 9970h, RSCAN.RSCAN0RPGACC29 A007 9974h,
RSCAN.RSCAN0RPGACC30 A007 9978h, RSCAN.RSCAN0RPGACC31 A007 997Ch,
RSCAN.RSCAN0RPGACC32 A007 9980h, RSCAN.RSCAN0RPGACC33 A007 9984h,
RSCAN.RSCAN0RPGACC34 A007 9988h, RSCAN.RSCAN0RPGACC35 A007 998Ch,
RSCAN.RSCAN0RPGACC36 A007 9990h, RSCAN.RSCAN0RPGACC37 A007 9994h,
RSCAN.RSCAN0RPGACC38 A007 9998h, RSCAN.RSCAN0RPGACC39 A007 999Ch,
RSCAN.RSCAN0RPGACC40 A007 99A0h, RSCAN.RSCAN0RPGACC41 A007 99A4h,
RSCAN.RSCAN0RPGACC42 A007 99A8h, RSCAN.RSCAN0RPGACC43 A007 99ACh,
RSCAN.RSCAN0RPGACC44 A007 99B0h, RSCAN.RSCAN0RPGACC45 A007 99B4h,
RSCAN.RSCAN0RPGACC46 A007 99B8h, RSCAN.RSCAN0RPGACC47 A007 99BCh,
RSCAN.RSCAN0RPGACC48 A007 99C0h, RSCAN.RSCAN0RPGACC49 A007 99C4h,
RSCAN.RSCAN0RPGACC50 A007 99C8h, RSCAN.RSCAN0RPGACC51 A007 99CCh,
RSCAN.RSCAN0RPGACC52 A007 99D0h, RSCAN.RSCAN0RPGACC53 A007 99D4h,
RSCAN.RSCAN0RPGACC54 A007 99D8h, RSCAN.RSCAN0RPGACC55 A007 99DCh,
RSCAN.RSCAN0RPGACC56 A007 99E0h, RSCAN.RSCAN0RPGACC57 A007 99E4h,
RSCAN.RSCAN0RPGACC58 A007 99E8h, RSCAN.RSCAN0RPGACC59 A007 99ECh,
RSCAN.RSCAN0RPGACC60 A007 99F0h, RSCAN.RSCAN0RPGACC61 A007 99F4h,
RSCAN.RSCAN0RPGACC62 A007 99F8h, RSCAN.RSCAN0RPGACC63 A007 99FCh



Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RDTA[31:0]	RAM Data Test Access	Data can be read and written in RSCAN RAM.	R/W

35.2.65 RSCAN ECC Control Register (ECCRCANCTL)

The ECCRCANCTL register controls the mode of the ECC for the RSCAN.
Bits 7 and 3 should be set (written) while the RSCAN is not operating.
Before writing to bit 7, set the EMCA1 and EMCA0 bits to 01b.

Address(es): RSCAN.ECCRCANCTL A007 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECDEDF7	ECSEDF7	ECDEDF6	ECSEDF6	ECDEDF5	ECSEDF5	ECDEDF4	ECSEDF4	ECDEDF3	ECSEDF3	ECDEDF2	ECSEDF2	ECDEDF1	ECSEDF1	ECDEDF0	ECSEDF0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EMCA1	EMCA0	—	—	ECOVFF	ECER2C	ECER1C	—	ECTHM	ECERVF	EC1ECP	EC2EDIC	EC1EDIC	ECER2F	ECER1F	ECEMF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECEMF	ECC Error Indication Flag	This flag indicates whether an error exists in the current read data. This bit is updated whenever the RAM reads data. This bit might be set if it is read before initialization of the RAM. This bit is cleared at the time of through mode enable selection (ECTHM = 1) and when there is no 1 bit error in the decode circuit input data. 0: The currently-read RAM data does not have bit errors. 1: The currently-read RAM data have bit errors.	R
b1	ECER1F	1-Bit Error Detection/Correction Flag	This flag indicates whether 1-bit error is detected during read access to the RAM when error detection is enabled (ECTHM = 0). Write 1 to the ECER1C bit (bit 9) to clear the flag. This bit is cleared at the time of through mode enable selection (ECTHM = 1). 0: 1-bit error has not occurred since this bit was cleared. 1: 1-bit error has occurred.	R
b2	ECER2F	2-Bit Error Detection Flag	This flag indicates whether 2-bit error is detected during read access to the RAM when error detection is enabled (ECTHM = 0). When 2-bit error interrupt is enabled (EC2EDIC = 1) and this flag is set, a 2-bit ECC error interrupt (INTECCDCNRAM) is output. Write 1 to the ECER2C bit (bit 10) to clear the flag. This bit is cleared at the time of through mode enable selection (ECTHM = 1). If 2-bit error is detected again while this bit is set, an interrupt signal will not be generated. 0: 2-bit error has not occurred since this bit was cleared. 1: 2-bit error has occurred.	R
b3	EC1EDIC	1-Bit Error Detection Interrupt Control	This bit controls whether to output a 1-bit ECC error source signal to the ECM when a 1-bit error is detected. 0: When a 1-bit error is detected, the error source signal is not output. 1: When a 1-bit error is detected, the error source signal is output.	R/W
b4	EC2EDIC	2-Bit Error Detection Interrupt Control	This bit controls whether to output a 2-bit ECC error source signal to the ECM when a 2-bit error is detected. 0: When a 2-bit error is detected, the error source signal is not output. 1: When a 2-bit error is detected, the error source signal is output.	R/W

Bit	Symbol	Bit Name	Description	R/W
b5	EC1ECP	1-Bit Error Correction Enable	This bit specifies whether to enable or disable 1-bit error correction when the ECC error detection/correction is enabled. 0: When a 1-bit error is detected, the error will be corrected. 1: When a 1-bit error is detected, the error will not be corrected.	R/W
b6	ECERVF	ECC Error Detection Enable Flag	This bit selects enabling or disabling of error detection. When writing to this bit, (0, 1) must be written to (EMCA1, EMCA0) at the same time. 0: Error detection is disabled. 1: Error detection is enabled.	R/W
b7	ECTHM	ECC Function Through Mode Select	This bit is used to set enabling and disabling of ECC. Setting this bit to 1 disables ECC. When writing to this bit, (0, 1) must be written to (EMCA1, EMCA0) at the same time. 0: Through mode is disabled (normal operation mode). 1: Through mode is enabled (ECC disabled).	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b9	ECER1C	1-Bit ECC Error Correction Accumulation Flag Clear	This bit is used to clear the 1 bit error detection/correction flag of ECER1F (bit 1). This bit is always read as 0. Writing 0 is ignored. Write 1 to this bit while the ECER1F bit is set to clear the ECER1F bit. When a conflict between this bit writing and ECER1F bit setting occurs, writing to this bit is given priority.	R/W *1
b10	ECER2C	2-Bit ECC Error Detection Flag Clear	This bit is used to clear the 2 bit error detection flag of ECER2F (bit 2). This bit is always read as 0. Writing 0 is ignored. Write 1 to this bit while the ECER2F bit is set to clear the ECER2F bit. When a conflict between this bit writing and ECER2F bit setting occurs, writing to this bit is given priority.	R/W *1
b11	ECOVFF	ECC Overflow Detection Flag	When an ECC error is detected while all ECCRCANEADz registers (z = 0 to 7) hold addresses at which errors were detected, this bit is set and the RSCAN overflow error signal is output. 0: ECC overflow is not detected. 1: ECC overflow is detected.	R
b13, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	EMCA0	Access Control 0 to ECC Mode Selection	These bits specify whether modifying the ECTHM bit (bit 7) is disabled or enabled. The value written to these bits is not retained. When these bits are read, the read value is always 0. When these bits are 01b, writing to bits 7 and 6 is enabled.	R/W *1
b15	EMCA1	Access Control 1 to ECC Mode Selection		R/W *1
b31 to b16	ECDEDFz	2-Bit ECC Error Detection Flag	This flag bit indicates whether the error stored in the ECCRCANEADz register (z = 0 to 7) is a 2-bit error. 0: 2-bit error has not occurred. 1: 2-bit error has occurred.	R
	ECSEDFz	1-Bit ECC Error Detection Flag	This flag bit indicates whether the error stored in the ECCRCANEADz register (z = 0 to 7) is a 1-bit error. 0: 1-bit error has not occurred. 1: 1-bit error has occurred.	R

Note 1. These bits are always read as 0.
Note: Bits 2 and 1 should be cleared when the ECC error indication flag (ECEMF) is not set.
We recommend initializing the RAM before clearing bits 2 and 1.

ECERVF Bit (ECC Error Detection Enable Flag)

This bit selects enabling or disabling of error detection. When writing to this bit, (0, 1) must be written to (EMCA1, EMCA0) at the same time. Error detection is disabled when the ECTHM bit is set to enable through mode. Table 35.11 shows the relationship between the ECERVF and ECTHM bits and the error detection setting.

Table 35.11 ECERVF and ECTHM Bits and Error Detection Setting

ECTHM Bit	ECERVF Bit	Error Detection Setting
0	0	Error detection disabled
0	1	Error detection enabled
1	0	Error detection disabled (through mode)
1	1	Error detection disabled (through mode)

ECOVFF Bit (ECC Overflow Detection Flag)

When a further ECC error is detected while all ECCRCANEADz registers (z = 0 to 7) hold addresses at which errors were detected, this bit is set and the RSCAN overflow error signal is output to the error control module (ECM). For details of the ECM, see section 42, Error Control Module (ECM).
Furthermore, if an overflow error is detected while this bit is set to 1, the RSCAN overflow error signal is output again.
This bit is cleared by writing 1 to both the ECER2C and ECER1C bits.

ECDEDFz Bit (2-Bit ECC Error Detection Flag) (z = 0 to 7)

This flag bit indicates the detection of 2-bit ECC errors and the address where the error was found is stored in the ECCRCANEADz register.
When an ECC overflow is detected (i.e., the ECOVFF bit = 1), this bit is not set even if the error is a 2-bit error.
This bit is cleared by writing 1 to both the ECER2C and ECER1C bits.

ECSEDFz Bit (1-Bit ECC Error Detection Flag) (z = 0 to 7)

This flag bit indicates the detection of 1-bit ECC errors and the address where the error was found is stored in the ECCRCANEADz register.
When an ECC overflow is detected (i.e., the ECOVFF bit = 1), this bit is not set even if the error is a 1-bit error.
This bit is cleared by writing 1 to both the ECER2C and ECER1C bits.

35.2.66 RSCAN ECC Error Address Register z (ECCRCANEADz) (z = 0 to 7)

ECCRCANEADz (z = 0 to 7) are read-only registers that automatically store and retain the values of addresses where ECC errors have occurred. If an ECC error occurs while ECC error detection is enabled, the buffer RAM addresses where errors are found are captured in order from z = 0.

Note 1. If an ECC error is detected again at the same address as that currently stored in the ECCRCANEADz register, the detected address is simply discarded.

Note 2. When 1-bit errors occur multiple times and all ECCRCANEADz registers hold only addresses where 1-bit errors were detected, if an overflow occurs due to the detection of a 2-bit error, the ECCRCANEAD7 register is overwritten with the address where the 2-bit error was detected and the value is retained.
Even if all ECCRCANEADz registers overflow due to the detection of a 1-bit error while only the addresses where 2-bit errors were detected are being held, the address where a 1-bit error was detected is discarded.

Address(es): RSCAN.ECCRCANEAD0 A007 B010h, RSCAN.ECCRCANEAD1 A007 B014h, RSCAN.ECCRCANEAD2 A007 B018h, RSCAN.ECCRCANEAD3 A007 B01Ch, RSCAN.ECCRCANEAD4 A007 B020h, RSCAN.ECCRCANEAD5 A007 B024h, RSCAN.ECCRCANEAD6 A007 B028h, RSCAN.ECCRCANEAD7 A007 B02Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ECEADz[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b10 to b0	ECEADz [10:0]	ECC Error Address Storage	When an ECC error is detected in the buffer RAM of the RSCAN, the RAM address where the error was detected is stored and retained in these bits. The ECCRCANCTL.ECDEDFz and ECSEDFz bits can be used to judge whether the ECC error at the address was a 1-bit error or 2-bit error.	R
b31 to b11	—	Reserved	These bits are read as 0.	R

35.3 Interrupt Sources

The RSCAN module has 8 interrupt signals connected to the interrupt controller, and these are grouped into global interrupts and channel interrupts. Also, multiple interrupt sources in the RSCAN module are grouped into each of these 8 interrupt signals. Table 35.12 lists the CAN interrupt sources.

- Global interrupts (2 sources):
  1. CAN receive FIFO interrupt
  2. CAN global error interrupt
- Channel interrupts (3 sources for each channel m, 6 in total) (m = 0, 1):
  1. CANm transmit interrupt
     - CANm transmission complete interrupt
     - CANm transmission abort interrupt
     - CANm transmit/receive FIFO transmission complete interrupt (in transmission mode, gateway mode)
     - CANm transmission history interrupt
     - CANm transmission queue Interrupt
  2. CANm transmit/receive FIFO receive complete interrupt (in transmission mode, gateway mode)
  3. CANm error interrupt

When an interrupt request is generated, the corresponding interrupt request flag is set to 1 (interrupt request present). In that case, when the interrupt enable bit is set to 1 (enabling interrupts), an interrupt request is output from the RSCAN module to the interrupt controller. (Generation of interrupts also depends on the interrupt control register settings of the interrupt controller.)

Setting the interrupt request flag to 0 (no interrupt request present) or setting the interrupt enable bit to 0 (disabling interrupts) clears the current interrupt request. The current interrupt request is still output until the interrupt request flag is cleared.

Figure 35.2 shows the CAN global interrupt block diagram. Figure 35.3 shows the CAN channel interrupt block diagram.

Table 35.12 List of CAN Interrupt Sources

Interrupt Source			Corresponding Interrupt Request Flag	Corresponding Interrupt Enable Bit
Global interrupts	Receive FIFO	Receive FIFO 0	RFIF in the RSCAN0RFSTS0 register	RFIE in the RSCAN0RFCC0 register
		Receive FIFO 1	RFIF in the RSCAN0RFSTS1 register	RFIE in the RSCAN0RFCC1 register
		Receive FIFO 2	RFIF in the RSCAN0RFSTS2 register	RFIE in the RSCAN0RFCC2 register
		Receive FIFO 3	RFIF in the RSCAN0RFSTS3 register	RFIE in the RSCAN0RFCC3 register
		Receive FIFO 4	RFIF in the RSCAN0RFSTS4 register	RFIE in the RSCAN0RFCC4 register
		Receive FIFO 5	RFIF in the RSCAN0RFSTS5 register	RFIE in the RSCAN0RFCC5 register
		Receive FIFO 6	RFIF in the RSCAN0RFSTS6 register	RFIE in the RSCAN0RFCC6 register
		Receive FIFO 7	RFIF in the RSCAN0RFSTS7 register	RFIE in the RSCAN0RFCC7 register
	Global error		DEF in the RSCAN0GERFL register MES in the RSCAN0GERFL register THLES in the RSCAN0GERFL register	DEIE in the RSCAN0GCTR register MEIE in the RSCAN0GCTR register THLEIE in the RSCAN0GCTR register
Channel interrupts (m = 0, 1)	CANm transmit	CANm transmission complete	TMTRF[1:0] in the RSCAN0TMSTSp register	TMIE in the RSCAN0TMIECy register
		CANm transmission abort	TMTRF[1:0] in the RSCAN0TMSTSp register	TAIE in the RSCAN0CmCTR register
		CANm transmit/ receive FIFO transmission complete	CFTXIF in the RSCAN0CFSTSk register	CFTXIE in the RSCAN0CFCCk register
		CANm transmission queue	TXQIF in the RSCAN0TXQSTSm register	TXQIE in the RSCAN0TXQCCm register
		CANm transmission history	THLIF in the RSCAN0THLSTSm register	THLIE in the RSCAN0THLCCm register
	CANm transmit/receive FIFO receive complete		CFRXIF in the RSCAN0CFSTSk register	CFRXIE in the RSCAN0CFCCk register
	CANm error		BEF in the RSCAN0CmERFL register ALF in the RSCAN0CmERFL register BLF in the RSCAN0CmERFL register OVLF in the RSCAN0CmERFL register BORF in the RSCAN0CmERFL register BOEF in the RSCAN0CmERFL register EPF in the RSCAN0CmERFL register EWF in the RSCAN0CmERFL register	BEIE in the RSCAN0CmCTR register ALIE in the RSCAN0CmCTR register BLIE in the RSCAN0CmCTR register OLIE in the RSCAN0CmCTR register BORIE in the RSCAN0CmCTR register BOEIE in the RSCAN0CmCTR register EPIE in the RSCAN0CmCTR register EWIE in the RSCAN0CmCTR register

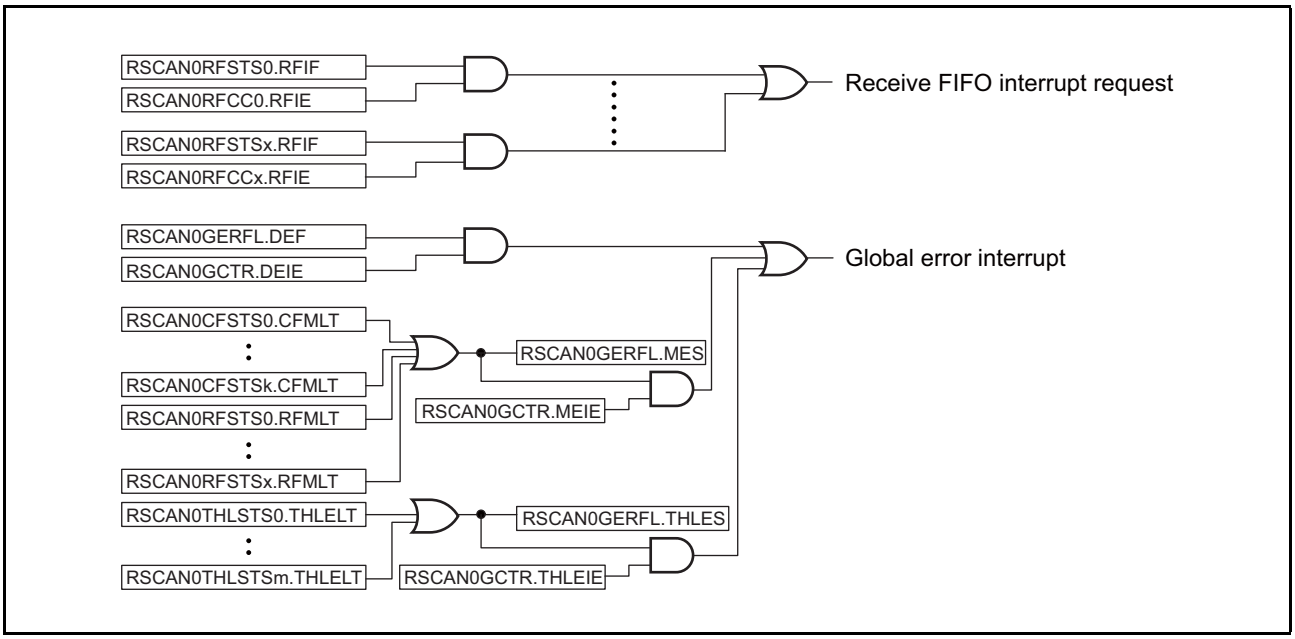


Figure 35.2 CAN Global Interrupt Block Diagram

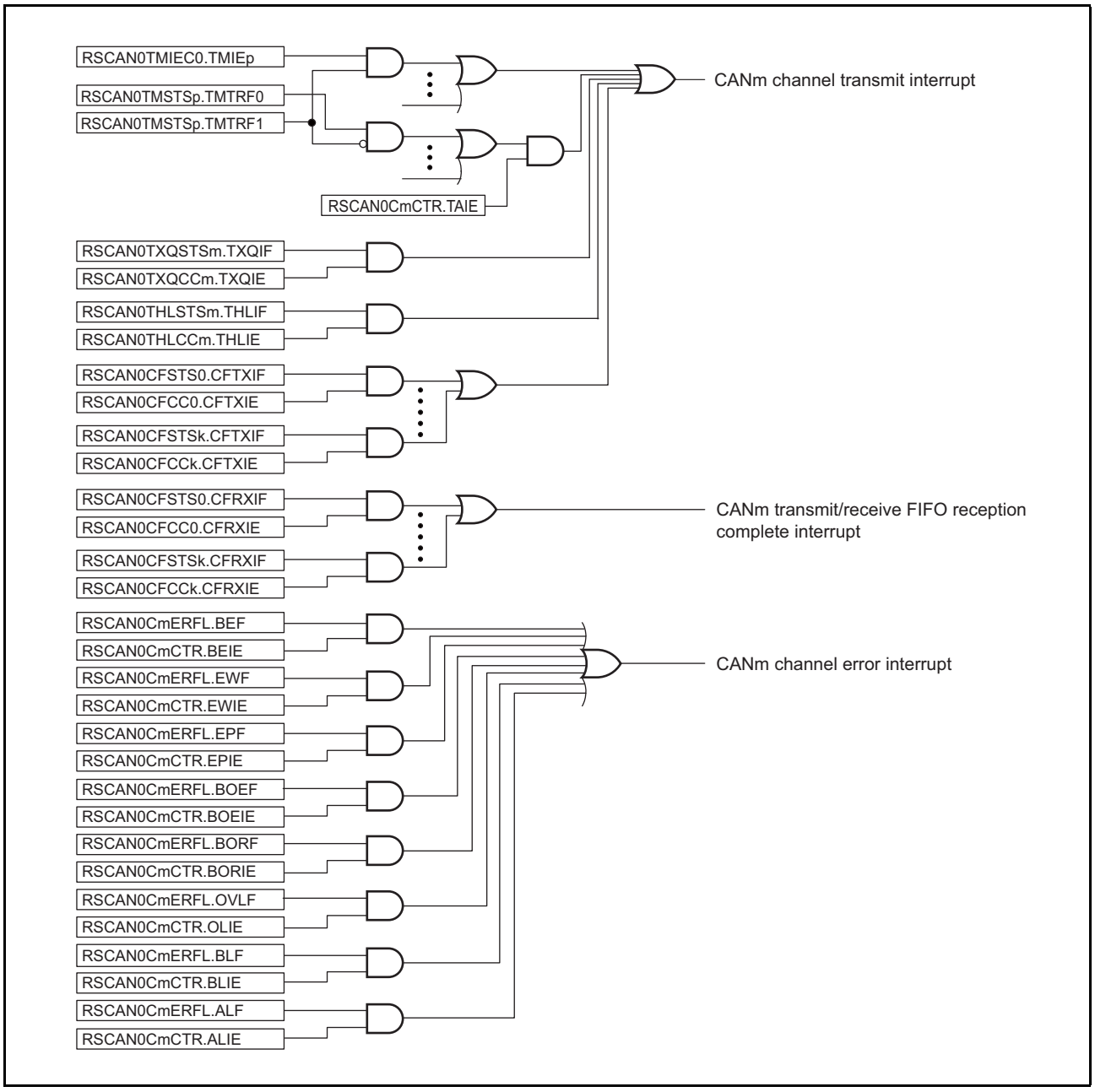


Figure 35.3 CAN Channel Interrupt Block Diagram

35.4 CAN Modes

The RSCAN module has four global modes to control the entire RSCAN module status and four channel modes to control individual channel status. Details of global modes are described in section 35.4.1, Global Modes, and details of channel modes are described in section 35.4.2, Channel Modes.

- Global stop mode: Stops the clocks of the entire module to achieve low power consumption.
- Global reset mode: Performs initial settings for the entire module.
- Global test mode: Performs test settings and performs the RAM test.
- Global operating mode: Makes the entire module operable.
- Channel stop mode: Stops the channel clock.
- Channel reset mode: Performs initial settings for the channels.
- Channel halt mode: Stops CAN communication and allows channel testing.
- Channel communication mode: Performs CAN communication.

35.4.1 Global Modes

Figure 35.4 shows the transitions of global modes.

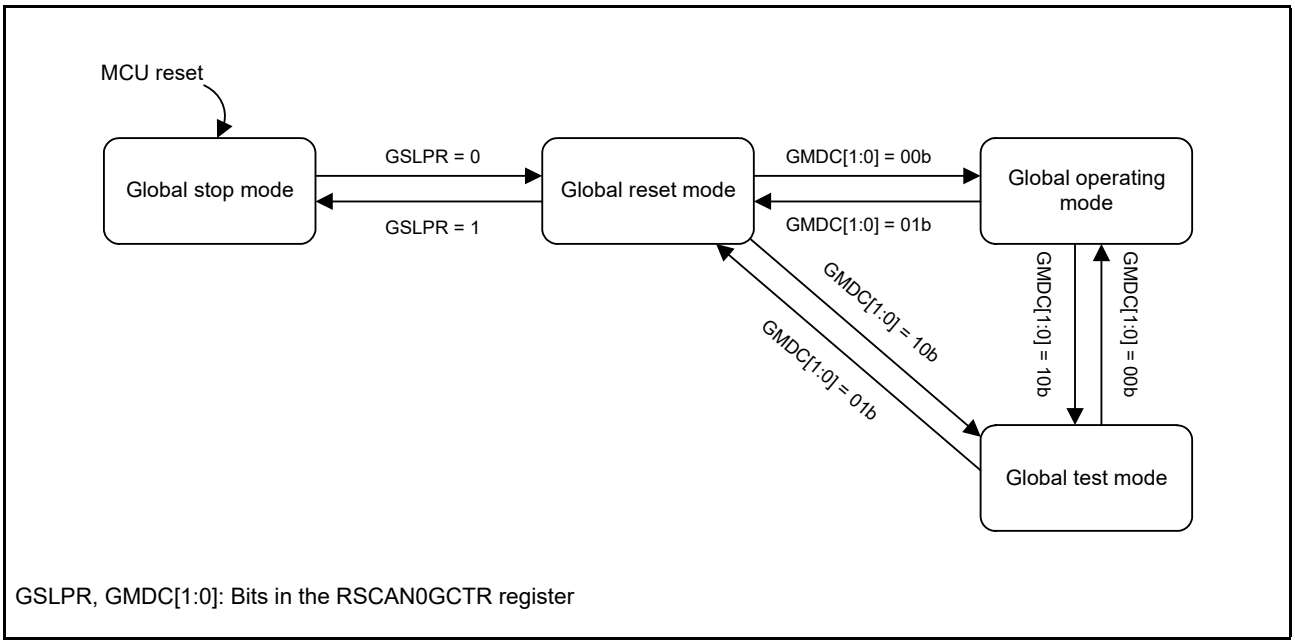


Figure 35.4 Transitions of Global Modes

In some cases, global mode transitions also force channel mode transitions. Table 35.13 shows the channel mode transitions depending on the global mode setting dictated by the GMDC[1:0] bits and the GSLPR bit.

Table 35.13 Transitions of Channel Modes Depending on Global Mode Setting (GMDC[1:0] and GSLPR Bits)

Channel Mode before Setting	Channel Mode after Setting			
	GMDC[1:0] = 00b GSLPR = 0 (Global Operation)	GMDC[1:0] = 10b GSLPR = 0 (Global Test)	GMDC[1:0] = 01b GSLPR = 0 (Global Reset)	GMDC[1:0] = 01b GSLPR = 1 (Global Stop)
Channel communication	Channel communication	Channel halt	Channel reset	Transition prohibited
Channel halt	Channel halt	Channel halt	Channel reset	Transition prohibited
Channel reset	Channel reset	Channel reset	Channel reset	Channel stop
Channel stop	Channel stop	Channel stop	Channel stop	Channel stop

Note 1. GMDC[1:0], GSLPR: Bits in the RSCAN0GCTR register

Table 35.14 shows the global mode transition time.

Table 35.14 Global Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Global stop	Global reset	Three PCLKD cycles
Global reset	Global stop	Three PCLKD cycles
Global reset	Global test	Ten PCLKD cycles
Global reset	Global operating	Ten PCLKD cycles
Global test	Global reset	Three PCLKD cycles
Global test	Global operating	Three PCLKD cycles
Global operating	Global reset	Three PCLKD cycles
Global operating	Global test	Two CANm frames*1

Note 1. CANm frame (1 message) time of the lowest communication speed of the channels in use.

35.4.1.1 Global Stop Mode

In global stop mode, clocks of the CAN do not run and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained. Only the clock used by the CPU for writing to the GSLPR bit runs in this mode.

After the MCU is reset, the CAN module transitions to global stop mode. Setting the GSLPR bit in the RSCAN0GCTR register to 1 (in global stop mode) in global reset mode sets the CSLPR bit in each of the RSCAN0CmCTR registers (m = 0, 1) to 1 (channel stop mode). If all channels are forced to transition to channel stop mode, the CAN module transitions to global stop mode. The GSLPR bit should not be modified in global operating mode or global test mode.

35.4.1.2 Global Reset Mode

In global reset mode, RSCAN module settings are performed. When the RSCAN module transitions to global reset mode, some registers are initialized. Table 35.17 and Table 35.18 list the registers to be initialized.

Setting the GMDC[1:0] bits in the RSCAN0GCTR register to 01b sets the CHMDC[1:0] bits in each of the RSCAN0CmCTR registers (m = 0, 1) to 01b (channel reset mode). If all channels are forced to transition to channel reset mode, the CAN module transitions to global reset mode. Channels that are already in channel reset mode or channel stop mode do not transition (because the CHMDC[1:0] bits have already been set to 01b).

35.4.1.3 Global Test Mode

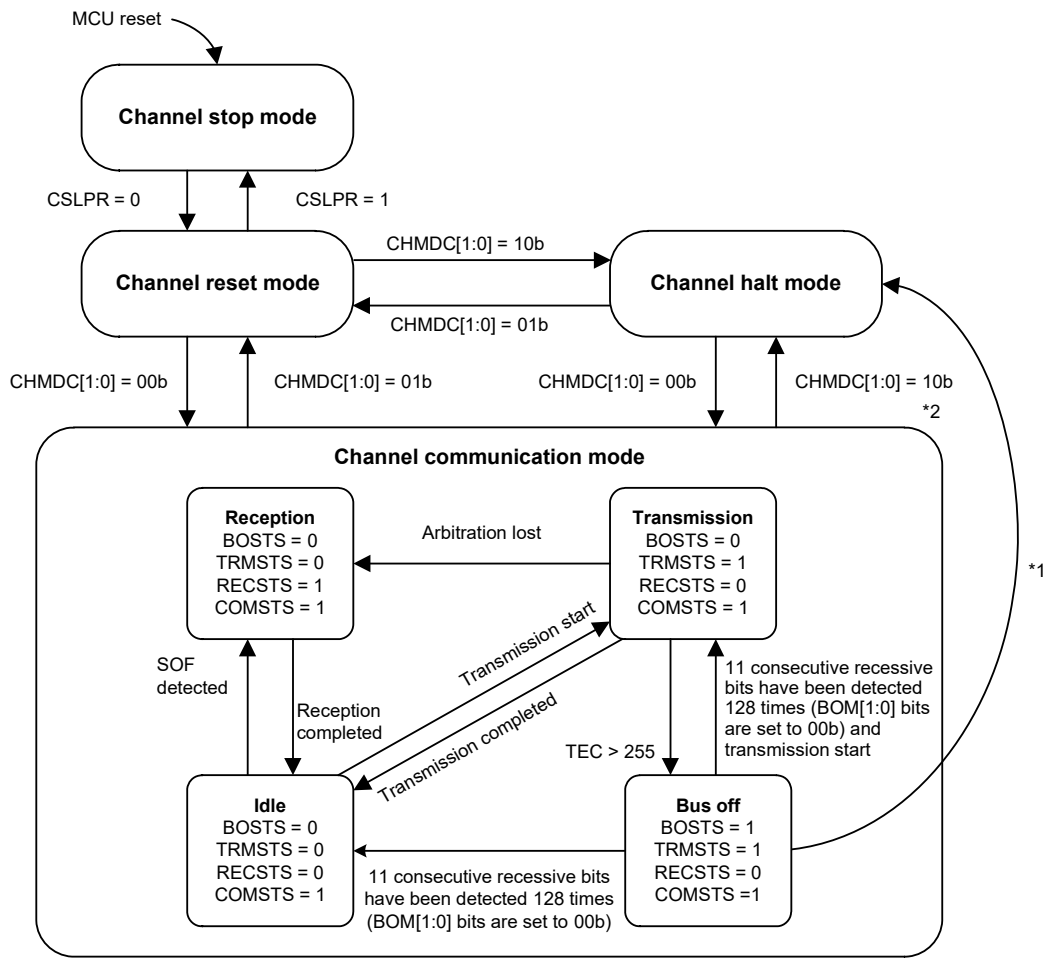
In global test mode, settings for test-related registers are performed. When the CAN module transitions to global test mode, all CAN communications are disabled.
Setting the GMDC[1:0] bits in the RSCAN0GCTR register to 10b sets the CHMDC[1:0] bits in each of the RSCAN0CmCTR registers to 10b (channel halt mode). If all channels are forced to transition to channel halt mode, the CAN module transitions to global test mode. Channels that are in channel stop mode, channel reset mode, or channel halt mode do not transition.

35.4.1.4 Global Operating Mode

The RSCAN module operates in global operating mode.
When the GMDC[1:0] bits in the RSCAN0GCTR register are set to 00b, the RSCAN module transitions to global operating mode.

35.4.2 Channel Modes

Figure 35.5 shows a channel mode state transition chart. Table 35.15 shows the channel mode transition time.



CHMDC[1:0], CSLPR, BOM[1:0]: Bits in the RSCAN0CmCTR register (m = 0, 1)
BOSTS, TRMSTS, RECSTS, COMSTS: Bits in the RSCAN0CmSTS register

Note 1. Timing of transition from bus off state to channel halt mode
- When BOM[1:0] = 01b: Transition to channel halt mode when TEC exceeds 255
- When BOM[1:0] = 10b: Transition to channel halt mode when 11 consecutive recessive bits have been detected 128 times
- When BOM[1:0] = 11b: Transition to channel halt mode when the CHMDC[1:0] bits are set to 10b

Note 2. While the CAN bus is locked at the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode.

Figure 35.5 Channel Mode State Transition Chart

Table 35.15 Channel Mode Transition Time

Mode before Transition	Mode after Transition	Maximum Transition Time
Channel stop	Channel reset	Three PCLKD cycles
Channel reset	Channel stop	Three PCLKD cycles
Channel reset	Channel halt	Three CANm bit times
Channel reset	Channel communication	Two CANm bit times
Channel halt	Channel reset	Three PCLKD cycles
Channel halt	Channel communication	Three CANm bit times
Channel communication	Channel reset	Three PCLKD cycles
Channel communication	Channel halt	Two CANm frames (1 message)

35.4.2.1 Channel Stop Mode

In channel stop mode, clocks are not supplied to channels and therefore power consumption is reduced. CAN registers can be read, but writing data to them is prohibited. Register values are retained.
Each channel enters channel stop mode after the MCU is reset. Channels also transition to channel stop mode when the GSLPR bit in the RSCAN0CmCTR register (m = 0, 1) is set to 1 (channel stop mode) in channel reset mode. The GSLPR bit should not be modified in channel communication mode and channel halt mode.

35.4.2.2 Channel Reset Mode

In channel reset mode, channel settings are performed. When a channel transitions to channel reset mode, some channel-related registers are initialized. Table 35.17 lists the registers to be initialized.
When the CHMDC[1:0] bits in the RSCAN0CmCTR register are set to 01b (channel reset mode) during CAN communication, communication is terminated before it is completed and the channel transitions to channel reset mode. Table 35.16 shows the operation when the CHMDC[1:0] bits are set to 01b (channel reset mode) during CAN communication.

35.4.2.3 Channel Halt Mode

In channel halt mode, settings for test-related registers of channels are performed. When a channel transitions to channel halt mode, CAN communication of the channel stops.
Table 35.16 shows operation when the CHMDC[1:0] bits are set to 10b (channel halt mode) during CAN communication.

Table 35.16 Operation a Channel Transitions to Channel Reset Mode/Channel Halt Mode

Mode	During Reception	During Transmission	Bus Off State
Channel reset (CHMDC[1:0] = 01b)	Transitions to channel reset mode before reception is completed.*1	Transitions to channel reset mode before transmission is completed.*1	Transitions to channel reset mode before bus off recovery.
Channel halt*3 (CHMDC[1:0] = 10b)	Transitions to channel halt mode after reception is completed.*2	Transitions to channel halt mode after transmission is completed.	[When BOM[1:0] = 00b] Transitions to channel halt mode (CHMDC[1:0] = 10b) only after bus off recovery. [When BOM[1:0] = 01b] Transitions to channel halt mode automatically when the condition for transition to bus off state is met. [When BOM[1:0] = 10b] Transitions to channel halt mode automatically after bus off recovery. [When BOM[1:0] = 11b] Transitions to channel halt mode immediately after the CHMDC[1:0] bits are set to 10b before bus off recovery.

Note 1. To allow transition to channel reset mode after communication is completed, set the CHMDC[1:0] bits to 10b and confirm that communication has been completed and transition to channel halt mode has been made, and then set the CHMDC[1:0] bits to 01b.
Note 2. While the CAN bus is locked at the dominant level, transition to channel halt mode is not made. In that case, enter channel reset mode. The CAN bus status can be confirmed with the BLF flag of the RSCAN0CmERFL register that becomes 1 when dominant lock is detected.
Note 3. When the transition from channel reset mode to channel wait mode is to be made, set the RSCAN0CmCFG register in channel reset mode and then shift to channel wait mode.

35.4.2.4 Channel Communication Mode

In channel communication mode, CAN communication is performed. Each channel has the following communication states during CAN communication.

- Idle: Neither reception nor transmission is in progress.
- Reception: Receiving a message sent from another node.
- Transmission: Transmitting a message.
- Bus off: Isolated from CAN communication.

When the CHMDC[1:0] bits in the RSCAN0CmCTR register are set to 00b, the channel transitions to channel communication mode. After that, once 11 consecutive recessive bits have been detected, the COMSTS flag in the RSCAN0CmSTS register (m = 0, 1) is set to 1 (communication is ready) and transmission and reception are enabled on the CAN network as an active node. At this time, transmission and reception of messages can be started.

35.4.2.5 Bus Off State

A channel transitions to the bus off state according to the transmit/receive error counter increment/decrement rules of the CAN specifications.
The conditions for returning from the bus off state are determined by the BOM[1:0] bits in the RSCAN0CmCTR register (m = 0, 1).

- When BOM[1:0] = 00b:
  Bus off recovery is compliant with the CAN specifications. After 11 consecutive recessive bits have been detected 128 times, a channel returns from the bus off state to the CAN communication ready state (error active state). At that time, the TEC[7:0] and REC[7:0] bits in the RSCAN0CmSTS register are initialized to 00h, the BORF flag in the RSCAN0CmERFL register is set to 1 (bus off recovery is detected), and a CANm error interrupt request (bus off recovery interrupt) is generated. When the CHMDC[1:0] bits in the RSCAN0CmCTR register are set to 10b (channel halt mode) in the bus off state, the channel transitions to channel halt mode after bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times).
- When BOM[1:0] = 01b:
  When a channel transitions to the bus off state, the CHMDC[1:0] bits are set to 10b and the channel transitions to channel halt mode. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00h, but the BORF flag is not set to 1. Also, a bus off recovery interrupt request is not generated.
- When BOM[1:0] = 10b:
  When a channel has transitioned to the bus off state, the CHMDC[1:0] bits are set to 10b. After bus off recovery has been completed (11 consecutive recessive bits have been detected 128 times), the channel transitions to channel halt mode. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00h, the BORF flag is set to 1, and a CANm error interrupt request (bus off recovery interrupt) is generated.
- When BOM[1:0] = 11b:
  When the CHMDC[1:0] bits are set to 10b in the bus off state, the channel transitions to channel halt mode before bus off recovery is completed. At that time, the TEC[7:0] and REC[7:0] bits are initialized to 00h, but the BORF flag is not set to 1. Also, a bus off recovery interrupt is not generated.
  However, the BORF flag becomes 1 and a CANm error interrupt request (bus off recovery interrupt) is generated if a CAN module transitions to error active state (by detecting 128 times of 11 consecutive recessive bits) before CHMDC[1:0] bits are set to 10b.

If the RSCAN module causes the channel to transition to channel halt mode simultaneously with a program write to the CHMDC[1:0] bits, the program write takes precedence. An automatic transition to channel halt mode when the BOM[1:0] bits are set to 01b or 10b is made only when the CHMDC[1:0] bits are 00b (channel communication mode).
Furthermore, setting the RTBO bit in the RSCAN0CmCTR register to 1 allows a forced return from the bus off state. As soon as the RTBO bit is set to 1, the state changes to the error active state. After 11 consecutive recessive bits have been detected, the CAN module becomes ready for communication. In this case, the BORF flag is not set to 1 and the TEC[7:0] and REC[7:0] bits are initialized to 00h. Write 1 to the RTBO bit only when the BOM[1:0] value is 00b. Writing the RTBO bit to 1 in a state other than the bus off state is ignored, and the RTBO bit is immediately set to 0.

Table 35.17 Registers Initialized in Global Reset Mode or Channel Reset Mode

Register	Bit / Flag
RSCAN0CmCTR register	CTMS[1:0], CTME, CHMDC[1:0]
RSCAN0CmSTS register	CHLTSTS, EPSTS, BOSTS, TRMSTS, RECSTS, COMSTS, REC[7:0], TEC[7:0]
RSCAN0CmERFL register	CRCREG[14:0], ADERR, B0ERR, B1ERR, CERR, AERR, FERR, SERR, ALF, BLF, OVLF, BORF, BOEF, EPF, EWF, BEF
RSCAN0CFCCk register	When transmission/reception FIFO buffer is in transmission mode or gateway mode: CFE
RSCAN0CFSTSk register	When transmission/reception FIFO buffer is in transmission mode or gateway mode: CFMC[7:0], CFFLL, CFEMP, CFMLT, CFRXIF, CFTXIF
RSCAN0CFTISTS register	CFkTXIF
RSCAN0TMCp register	TMOM, TMTAR, TMTR
RSCAN0TMSTSp register	TMTARM, TMTRM, TMTRF[1:0], TMTSTS
RSCAN0TMTRSTS0 register	TMTRSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCAN0TMTARSTS0 register	TMTARSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCAN0TMTCSTS0 register	TMTCSTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCAN0TMTASTS0 register	TMTASTSp (Bits of corresponding channel are initialized in channel reset mode.)
RSCAN0TXQCCm register	TXQE
RSCAN0TXQSTSm register	TXQIF, TXQFLL, TXQEMP
RSCAN0THLCCm register	THLE
RSCAN0THLSTSm register	THLMC[4:0], THLIF, THLELT, THLFLL, THLEMP
RSCAN0GTINTSTS0 register	TSIFm, TAIFm, TQIFm, CFTIFm, THIFm (m = 0, 1)

Note 1. Number of channels: m = 0, 1
Note 2. Transmission/reception FIFO buffer: k = 0 to 2 (channel 0), 3 to 5 (channel 1)
Note 3. Transmission buffer number: p = 0 to 15 (channel 0), 16 to 31 (channel 1)

Table 35.18 Registers Initialized Only in Global Reset Mode

Register	Bit / Flag
RSCAN0GSTS register	GHLTSTS
RSCAN0GERFL register	THLES, MES, DEF
RSCAN0GTSC register	TS[15:0]
RSCAN0RMND0 register	RMNSq
RSCAN0RFCCx register	RFE
RSCAN0RFSTSx register	RFMC[7:0], RFIF, RFMLT, RFFLL, RFEMP
RSCAN0CFCCk register	When transmission/reception FIFO buffer is in reception mode: CFE
RSCAN0CFSTSk register	When transmission/reception FIFO buffer is in reception mode: CFMC[7:0], CFFLL, CFEMP, CFTXIF, CFRXIF, CFMLT
RSCAN0FESTS register	CFkEMP, RFxEMP
RSCAN0FFSTS register	CFkFLL, RFxFLL
RSCAN0FMSTS register	CFkMLT, RFxMLT
RSCAN0RFISTS register	RFxIF
RSCAN0CFRISTS register	CFkRXIF
RSCAN0GTSTCFG register	RTMPS[6:0], C0ICBCE, C1ICBCE, C2ICBCE, C3ICBCE, C4ICBCE, C5ICBCE
RSCAN0GTSTCTR register	RTME, ICBCTME

Note 1. Reception buffer number: q = 0 to 15 (channel 0), 16 to 31 (channel 1)
Note 2. Reception FIFO buffer number: x = 0 to 7

35.5 Reception Function

There are two reception types.

- Reception by reception buffers:
  Zero to 31 reception buffers can be shared by all channels. Since messages stored in reception buffers are overwritten at each reception, the latest receive data can always be read.
- Reception by reception FIFO buffers and transmission/reception FIFO buffers (reception mode):
  Eight reception FIFO buffers can be shared by all channels and three dedicated transmission/reception FIFO buffers are provided for each channel. Messages of up to the number of buffer stages specified with the RFDC[2:0] and CFDC[2:0] bits can be stored in FIFO buffers and can be read sequentially from the oldest.

35.5.1 Data Processing Using the Reception Rule Table

Data processing using the reception rule table allows dispatching of selected messages to the specified buffer. Data processing includes acceptance filter processing, DLC filter processing, routing processing, label addition processing, and mirror function processing.

Up to 128 reception rules can be registered per channel and up to (64 × number of channels) total reception rules can be registered in the entire module. (Up to 128 reception rules can be registered in this module that has two channels.) Set reception rules for each channel. Reception rules cannot be shared with other channels. If reception rules are not set, no messages can be received. Figure 35.6 illustrates how reception rules are registered.

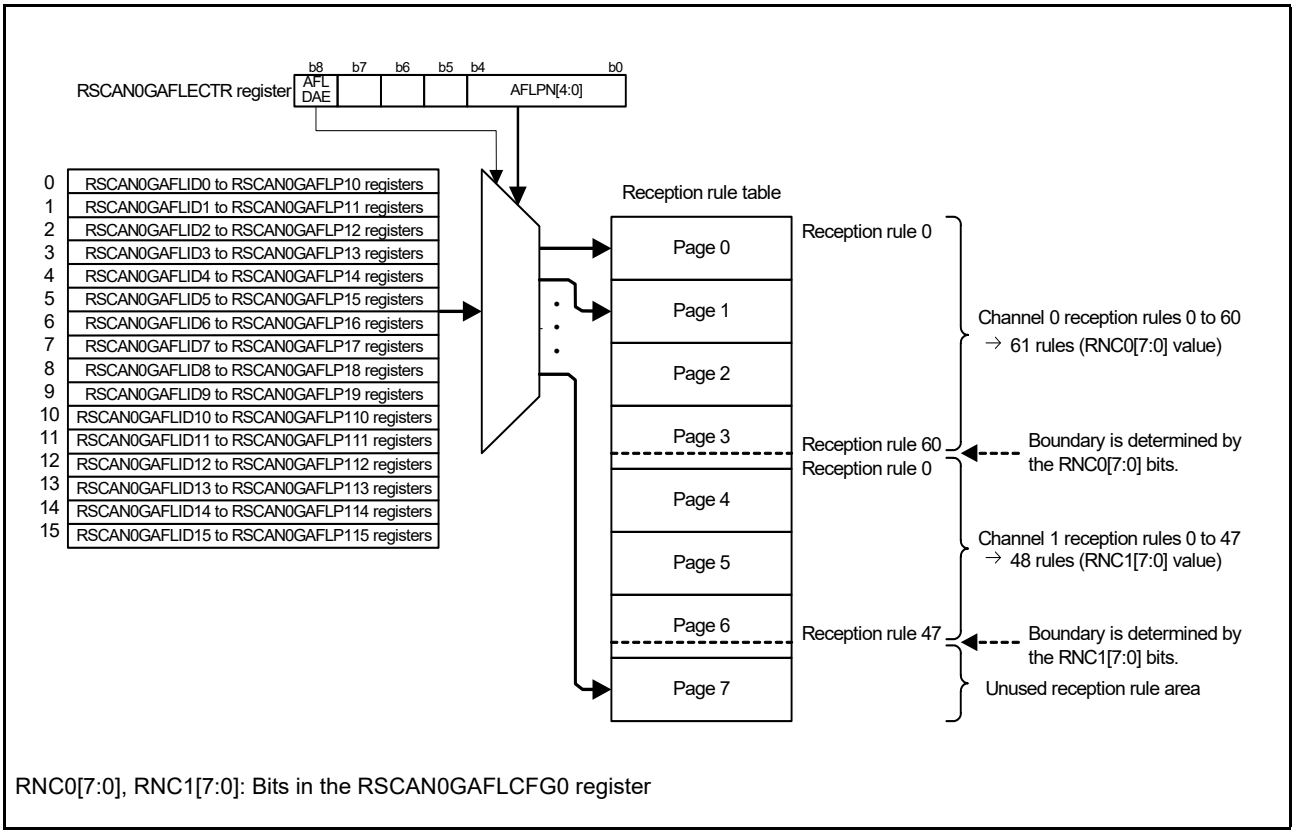


Figure 35.6 Entry of Reception Rules (for Setting Channels 0 and 1)

Note: Reception rules for each channel must be set in contiguous blocks.
Channel 1 rules and channel 0 rules must be set separately.

Each reception rule consists of 16 bytes in the RSCAN0GAFLIDj, RSCAN0GAFLMj, RSCAN0GAFLP0j, and RSCAN0GAFLP1j registers (j = 0 to 15). The RSCAN0GAFLIDj register is used to set GAFLID, GAFLIDE bit, GAFLRTR bit, and the mirror function, the RSCAN0GAFLMj register is used to set mask, the RSCAN0GAFLP0j register is used to set label information to be added, DLC value, and storage reception buffer, and the RSCAN0GAFLP1j register is used to set storage FIFO buffer. Up to 16 reception rules can be set per page.

35.5.1.1 Acceptance Filter Processing

In the acceptance filter processing, the ID data, IDE bit, and RTR bit in a received message are compared with the ID data, IDE bit, and RTR bit set in the reception rule of the corresponding channel. When all these bits match, the message passes through the acceptance filter processing. The ID data, IDE bit, and RTR bit in the received message which correspond to the bits set to 0 (bits are not compared) in the RSCAN0GAFLMj register are not compared and are regarded as matched.

Check begins with the reception rule of the minimum number for the corresponding channel. When all the bits to be compared in a received message match the bits set in the reception rule or when all the reception rules are compared without any match, filter processing stops. If there is no matching reception rule, the received message is not stored in the reception buffer or FIFO buffer.

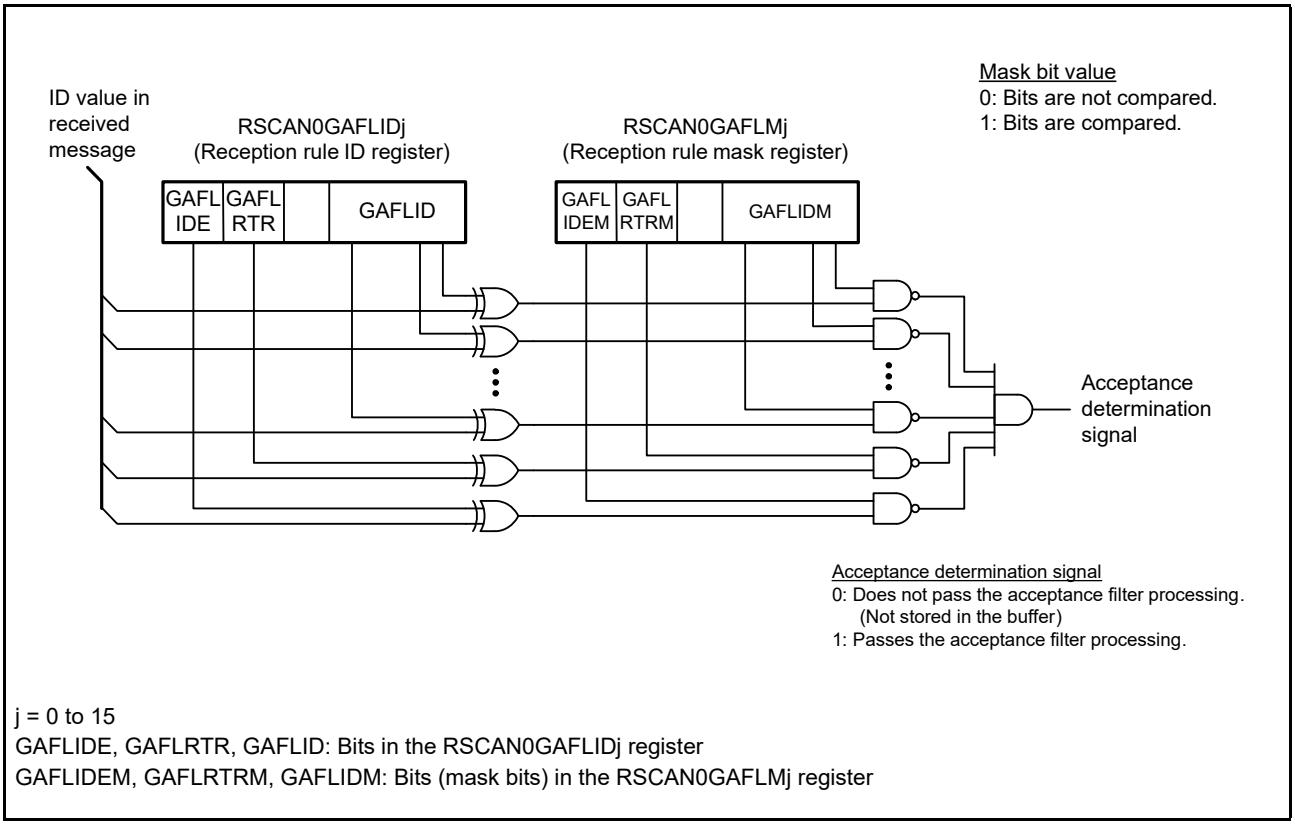


Figure 35.7 Acceptance Filter Function

35.5.1.2 DLC Filter Processing

When the DCE bit in the RSCAN0GCFG register is set to 1 (DLC check is enabled), DLC filter processing is added to messages that passed through the acceptance filter processing. When the DLC value in a message is equal to or larger than the DLC value set in the reception rule, the message passes through the DLC filter processing.
When a message has passed through the DLC filter processing with the DRE bit in the RSCAN0GCFG register set to 0 (DLC replacement is disabled), the DLC value in the received message is stored in the buffer. In this case, all the data bytes in the received message are stored in the buffer.
When a message has passed through the DLC filter processing with the DRE bit in the RSCAN0GCFG register set to 1 (DLC replacement is enabled), the DLC value in the reception rule is stored in the buffer instead of the DLC value in the received message. In this case, a value of 00h is stored in each data byte beyond the number of bytes which is indicated by the DLC value in the reception rule.
When the DLC value in the received message is smaller than that in the reception rule, the message does not pass through the DLC filter processing. In this case, the message is not stored in the reception buffer or the FIFO buffer and the DEF flag in the RSCAN0GERFL register is set to 1 (a DLC error is present).

35.5.1.3 Routing Processing

Messages that passed through the acceptance filter processing and the DLC filter processing are stored in reception buffers, reception FIFO buffers, or transmission/reception FIFO buffers (set to reception mode or gateway mode). Message storage destination is set by the GAFLRMV and GAFLRMDP[6:0] bits in the RSCAN0GAFLP0j register (j = 0 to 15) and by the RSCAN0GAFLP1j register. Messages that passed through the acceptance filter processing and the DLC filter processing can be stored in up to eight buffers.

35.5.1.4 Label Addition Processing

It is possible to add 12-bit label information to messages that passed through the filter processing and store them in buffers. This label information is set in the GAFLPTR[11:0] bits in the RSCAN0GAFLP0j register.

35.5.1.5 Mirror Function Processing

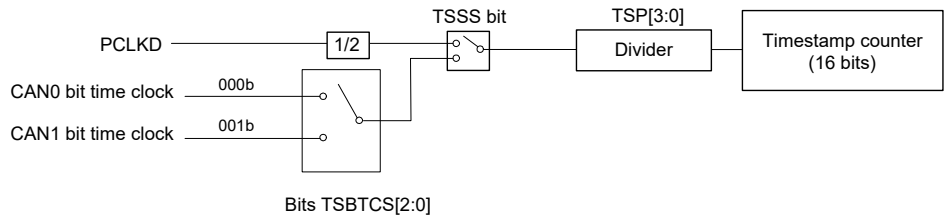
The mirror function allows the CAN node to receive its own transmitted messages. The mirror function is made available by setting the MME bit in the RSCAN0GCFG register to 1 (mirror function is enabled).
When the mirror function is in use, reception rules for which the GAFLLB bit in the RSCAN0GAFLIDj register is set to 0 are used for data processing when receiving messages transmitted from other CAN nodes. When the CAN node is receiving its own transmitted messages, reception rules for which the GAFLLB bit is set to 1 are used for data processing.

35.5.1.6 Timestamp

The timestamp counter is a 16-bit free-running counter used for recording message receive time. The timestamp counter value is fetched at the start-of-frame (SOF) timing of a message and is then stored in a reception buffer or a FIFO buffer together with the message ID and data. Either PCLKD/2 or the CANm bit time clock (m = 0, 1) may be selected as a timestamp counter clock source using the TSBTCS[2:0] and TSSS bits in the RSCAN0GCFG register. The timestamp counter count source is obtained by dividing the selected clock source by the TSP[3:0] value in the RSCAN0GCFG register.

When the CANm bit time clock is used as a clock source, the timestamp counter stops when the corresponding channel transitions to channel reset mode or channel halt mode. When the PCLKD/2 is used as a clock source, the timestamp function is not affected by channel mode.

The timestamp counter value is reset to 0000h by setting the TSRST bit in the RSCAN0GCTR register to 1.



TSBTCS[2:0], TSSS, TSP[3:0]: Bits in the RSCAN0GCFG register

Note: When specifying PCLKD/2 as the timestamp counter count source, set bits TSBTCS[2:0] to 000b.

Figure 35.8 Timestamp Function Block Diagram

35.6 Transmission Functions

There are three types of transmission.

- Transmission using transmission buffers:
  Each channel has 16 buffers.
- Transmission using transmission/reception FIFO buffers (transmission mode):
  Each channel has three FIFO buffers. Up to 128 messages can be contained in a single FIFO buffer. Each FIFO buffer is used with a link to a transmission buffer. Only the message to be transmitted next in a FIFO buffer becomes the target of transmit priority determination. Messages are transmitted sequentially on a first-in, first-out basis.
- Transmission using transmission queues:
  Up to 16 transmission buffers per channel can be allocated to the transmission queues. Transmission buffer ((16 × m) + 15) is used as an access window of a corresponding channel. Transmission buffers are allocated to transmission queues in descending order of buffer number. All messages in transmission queues, which are targets of priority determination, are transmitted in the order of ID number.

Table 35.19 Transmission Buffers p Allocated to Each Channel (p = 0 to 31)

Channel	Allocation of Transmission Buffers
CAN0	Transmission buffers 0 to 15
CAN1	Transmission buffers 16 to 31

Table 35.20 Transmission/Reception FIFO Buffers k Allocated to Each Channel (k = 0 to 5)

Channel	Allocation of Transmission Buffers
CAN0	Transmission/reception FIFO buffers 0 to 2
CAN1	Transmission/reception FIFO buffers 3 to 5

Figure 35.9 shows the allocation of transmission queues and transmission/reception FIFO buffer link.

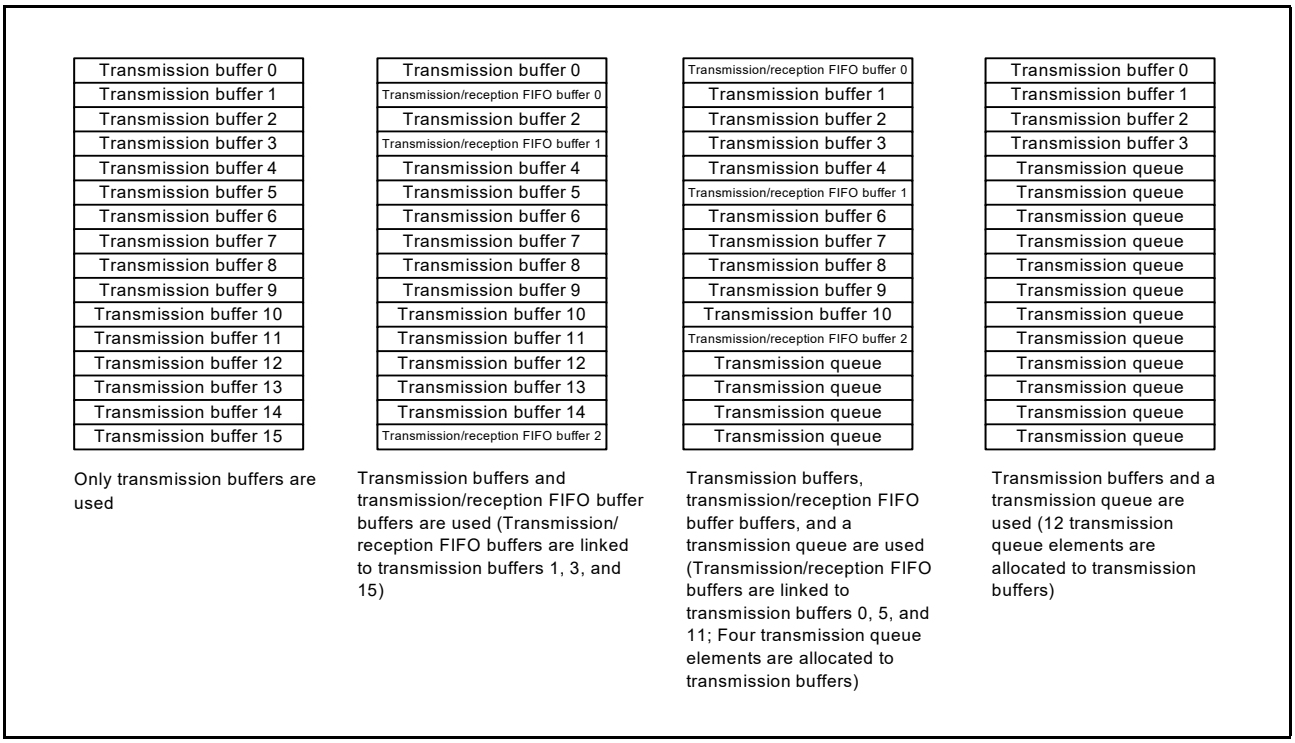


Figure 35.9 Allocation of Transmission Queues and Transmission/Reception FIFO Buffer Links

35.6.1 Transmit Priority Determination

If transmission requests are issued from multiple buffers or from the queue on the same channel, transmit priority is determined using one of the following methods.
The priority is determined by using one of the following methods.

- ID priority (TPRI bit = 0)
- Transmission buffer number priority (TPRI bit = 1)

All CAN channels use the setting of the TPRI bit in the RSCAN0GCFG register.
When the TPRI bit is set to 0, messages are transmitted according to the priority of stored message IDs. ID priority conforms to the CAN bus arbitration specification defined in the CAN specifications. All IDs of pending messages for transmission are targets of priority determination, regardless of whether they are stored in transmission buffers, transmission/reception FIFO buffers (set to transmission mode or gateway mode), or the transmission queue. If even a single transmission queue is used, select ID priority. When transmission/reception FIFO buffers are used, the oldest message in a FIFO buffer becomes the target of priority determination. When a message is being transmitted from a transmission/reception FIFO buffer, the next message in the FIFO buffer becomes the target of priority determination. When a transmission queue is used, all messages in the transmission queue are targets of priority determination. If the same ID is set for two or more buffers, the buffer with the smaller buffer number takes precedence.
When the TPRI bit is set to 1, the message in the transmission buffer with the minimum buffer number among all buffers with a transmission request is transmitted first. When transmission/reception FIFO buffers are linked to transmission buffers, transmit priority is determined according to linked transmission buffer numbers.
When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again regardless of the TPRI bit.

35.6.2 Transmission Using Transmission Buffers

Setting the transmission request bit (TMTR bit in the RSCAN0TMCp register) in a transmission buffer to 1 (transmission is requested) allows transmission of data frames or remote frames.
The transmission result is shown by the TMTRF[1:0] flag in the corresponding RSCAN0TMSTSp register (p = 0 to 31).
When transmission completes successfully, the TMTRF[1:0] flag is set to 10b (transmission has been completed (without transmission abort request)) or 11b (transmission has been completed (with transmission abort request)).

35.6.2.1 Transmission Abort Function

With respect to transmission buffers for which the TMTRM bit in the RSCAN0TMSTSp register is set to 1 (a transmission request is present), when the TMTAR bit in the RSCAN0TMCp register is set to 1 (transmission abort is requested), the transmission request is canceled. When transmission abort is completed, the TMTRF[1:0] flag in the RSCAN0TMSTSp register is set to 01b (transmission abort has been completed) and the transmission request is canceled (clearing the TMTRM bit to 0).
A message that is being transmitted or a message to be transmitted next according to the transmit priority determination cannot be aborted. However, when an arbitration-lost or an error occurs during transmission of a message for which the TMTAR bit is set to 1, retransmission is not performed.

35.6.2.2 One-Shot Transmission Function (Retransmission Disabling Function)

When the TMOM bit in the RSCAN0TMCp register is set to 1 (one-shot transmission is enabled), transmission is performed only once. Even if an arbitration-lost or an error occurs, retransmission is not performed.
The one-shot transmission result is shown by the TMTRF[1:0] flag in the corresponding RSCAN0TMSTSp register.
When one-shot transmission completes successfully, the TMTRF[1:0] flag is set to 10b or 11b. When an arbitration-lost or an error occurs, the TMTRF[1:0] flag is set to 01b (transmission abort has been completed).

35.6.3 Transmission Using FIFO Buffers

Multiple messages can be stored in a single transmission/reception FIFO buffers, up to the number specified by the FIFO buffer depth, which is set by the CFDC[2:0] bits in the RSCAN0CFCCk register (k = 0 to 5). Messages are transmitted sequentially on a first-in, first-out basis.
Each transmission/reception FIFO buffer is linked to a transmission buffer selected by the CFTML[3:0] bits in the RSCAN0CFCCk register. When the CFE bit in the RSCAN0CFCCk register is set to 1 (transmission/reception FIFO buffers are used), transmission/reception FIFO buffers become targets of transmit priority determination. Priority of only the next message for transmission is determined in the FIFO buffer.
When the CFE bit is set to 0 (no transmission/reception FIFO buffer is used), the CFEMP flag is set to 1 (the transmission/reception FIFO buffer contains no message (buffer empty)) at the timing below.

- The transmission/reception FIFO buffer becomes empty immediately if the message in it is not being transmitted or is not to be transmitted next.
- The transmission/reception FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration-lost in the case that a message in it is being transmitted or to be transmitted next.

When the CFE bit is cleared to 0, all messages in transmission/reception FIFO buffers are lost and messages cannot be stored in FIFO buffers. Confirm that the CFEMP flag is set to 1 before setting the CFE bit to 1 again.

35.6.3.1 Interval Transmission Function

A message transmission interval time can be set to space the transmission of messages from the same FIFO buffer when using a transmission/reception FIFO buffer set to transmission mode or gateway mode.
Immediately after the first message has been transmitted successfully from the FIFO buffer with the CFE bit in the RSCAN0CFCCk register set to 1, the interval timer starts counting (after EOF7 of the CAN protocol). After that, when the interval time has passed, the next message is transmitted. The interval timer stops in channel reset mode or by clearing the CFE bit to 0.
The interval time is set by the CFITT[7:0] bits in the RSCAN0CFCCk register. When the interval timer is not used, set the CFITT[7:0] bits to 00h.
Select an interval timer count source using the CFITR and CFITSS bits in the RSCAN0CFCCk register. When the CFITR and CFITSS bits are set to 00b, the count source is obtained by dividing PCLKD/2 by the value of the ITRCP[15:0] bits. When the CFITR and CFITSS bits are set to 10b, the count source is obtained by dividing PCLKD/2 by (the value of the ITRCP[15:0] bits in the RSCAN0GCFG register × 10). When the CFITR and CFITSS bits are set to x1b, the CANm bit time clock is used as a count source.
The interval time is calculated by the following equations where M is the value of ITRCP[15:0] and N is the value of CFITT[7:0].

- When CFITR and CFITSS = 00b (fPBA is the frequency of PCLKD):

$$\frac{1}{f_{PBA}} \times 2 \times M \times N$$

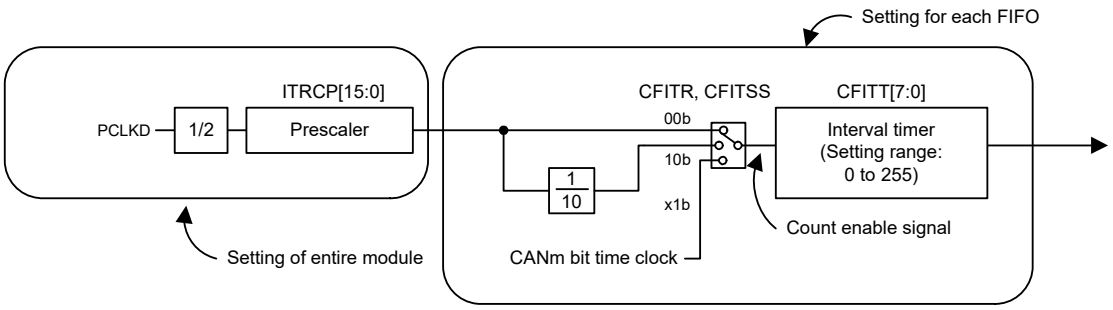
- When CFITR and CFITSS = 10b:

$$\frac{1}{f_{PBA}} \times 2 \times M \times 10 \times N$$

- When CFITR and CFITSS = x1b (fCANBIT is the frequency of CANm bit time clock):

$$\frac{1}{f_{CANBIT}} \times N$$

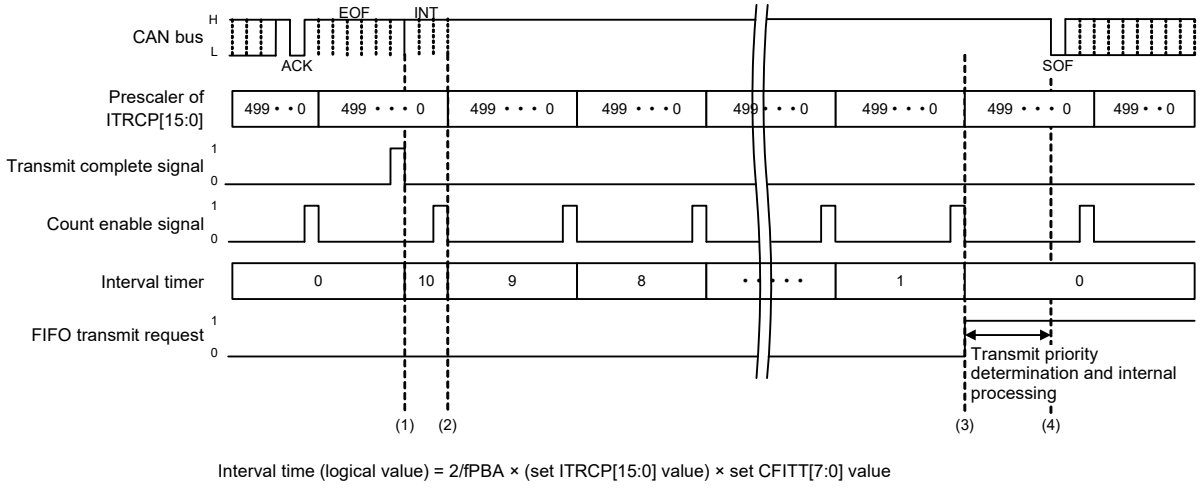
Figure 35.10 shows the interval timer block diagram.



ITRCP[15:0]: Bits in the RSCAN0GCFG register
CFITR, CFITSS, CFITT[7:0]: Bits in the RSCAN0CFCCk register
m = 0,1 , k = 0 to 5

Figure 35.10 Interval Timer Block Diagram

Figure 35.11 shows the interval timer timing diagram.



Interval time (logical value) = 2/fPBA × (set ITRCP[15:0] value) × set CFITT[7:0] value

fPBA: Frequency of PCLKD
ITRCP[15:0]: Bits in the RSCAN0GCFG register (The set value is 500 in this figure.)
CFITT[7:0]: Bits in the RSCAN0CFCCk register (The set value is 10 in this figure.)

Figure 35.11 Interval Timer Timing Chart

(1) The interval timer starts counting upon completion of transmission. Since the prescaler is not initialized at the time of transmission completion, the first interval time contains an error of up to one count of the interval timer.
(2) The interval timer is decremented by the next count enable signal.
(3) When the interval timer has decreased to 0, the transmission/reception FIFO buffer issues a transmission request.
(4) The transmission/reception FIFO buffer is determined for the next transmission by the priority determination, it starts transmitting data. Transmission starts usually with a delay of three CANm bit time clock cycles or less from the issue of transmission request. If multiple internal processes (such as receive filter processing, message routing, and transmit priority determination) take place in all channels, a delay of up to 582 cycles of the PCLKD may be generated.

35.6.4 Transmission Using Transmission Queues

Three to sixteen buffers are allocated to a transmission queue of each channel, and transmission buffer ((16 × m) + 15) (m = 0, 1) is used as an access window of a corresponding channel.
All messages in a transmission queue are targets of transmit priority determination and are transmitted in the ID priority order regardless of storage sequence. If two messages having the same ID are stored in a transmission queue, these messages are not always transmitted in the order of their storage in the transmission queue.
Setting the TXQE bit in the RSCAN0TXQCCm register to 0 disables transmission queues. When the TXQE bit is set to 0, the TXQEMP flag in the RSCAN0TXQSTSm register is set to 1 (the transmission queue contains no messages (transmission queue empty)) at the timing below.

- The transmission queue becomes empty immediately when no message in it is being transmitted or will be transmitted next.
- The transmission queue becomes empty after transmission completion, CAN bus error detection, or arbitration-lost when a message in it is being transmitted or will be transmitted next.

When the TXQE bit is cleared to 0, all messages in transmission queues are lost and messages cannot be stored in transmission queues. Confirm that the TXQEMP flag is set to 1 before setting the TXQE bit to 1 again.

35.6.5 Transmission History Function

Information about transmission-completed messages can be stored in the transmission history buffer. Each channel has a single transmission history buffer that can contain 16 sets of transmission history data.
A message transmit source buffer type can be selected by the THLDTE bit in the RSCAN0THLCCm register. The THLEN bit in the RSCAN0CFIDk register (k = 0 to 5) determines whether transmission history data is stored for each message.
The following information on a transmitted message will be stored in the transmission history buffer after the successful completion of transmission.
Storage of the transmission history data after the successful completion of transmission may take up to 150 cycles of pclk.

- Buffer type 001b: Transmission buffer
  010b: Transmission/reception FIFO buffer
  100b: Transmission queue
- Buffer number Number of source transmission buffer, transmission queue, or transmission/reception FIFO buffer. This number depends on buffer types. See Table 35.21.
- Label data Label information of the transmitted message

Table 35.21 Transmission History Data Buffer Numbers

Buffer No. / Buffer type	001b	010b	100b
0000b	Transmission buffer 16 × m + 0	Buffer numbers of the transmission buffer linked to the transmission/ reception FIFO buffer by the CFTML[3:0] bits in the RSCAN0CFCCk register (k = 0 to 5)	Buffer numbers of the transmission buffer allocated to the transmit queue that performed transmission
0001b	Transmission buffer 16 × m + 1		
0010b	Transmission buffer 16 × m + 2		
0011b	Transmission buffer 16 × m + 3		
0100b	Transmission buffer 16 × m + 4		
0101b	Transmission buffer 16 × m + 5		
0110b	Transmission buffer 16 × m + 6		
0111b	Transmission buffer 16 × m + 7		
1000b	Transmission buffer 16 × m + 8		
1001b	Transmission buffer 16 × m + 9		
1010b	Transmission buffer 16 × m + 10		
1011b	Transmission buffer 16 × m + 11		
1100b	Transmission buffer 16 × m + 12		
1101b	Transmission buffer 16 × m + 13		
1110b	Transmission buffer 16 × m + 14		
1111b	Transmission buffer 16 × m + 15		

Label data is used to identify each message. Unique label data can be added to each message transmitted from a transmission buffer, transmission queue, or transmission/reception FIFO buffer.
Transmission history data can be read from the RSCAN0THLACCm register. If an attempt is made to store new transmission history data while the buffer is full, the buffer overflows and the new data is discarded.

35.7 Gateway Function

When a transmission/reception FIFO buffer is set to gateway mode, received messages can be transmitted from an arbitrary channel without CPU intervention.

When a transmission/reception FIFO buffer for which the CFM[1:0] bits in the RSCAN0CFCCk register are set to 10b (gateway mode) is selected by the RSCAN0GAFLP1j register (j = 0 to 15), messages that passed through the filter processing of the reception rule are stored in the specified transmission/reception FIFO buffer and are automatically transmitted from the buffer.

Messages stored in a transmission/reception FIFO buffer are transmitted sequentially on a first-in, first-out basis. Only the message to be transmitted next becomes the target of transmit priority determination.

Transmission/reception FIFO buffers in the gateway mode are disabled by setting the CFE bit in the RSCAN0CFCCk register to 0 and the CFEMP flag becomes 1 according to the timing below.

- The transmission/reception FIFO buffer becomes empty immediately when the message in it is not being transmitted and will not to be transmitted next.
- The transmission/reception FIFO buffer becomes empty after transmission completion, CAN bus error detection, or arbitration-lost when the message in it is being transmitted or will be transmitted next.

When the CFE bit is cleared to 0, all messages in transmission/reception FIFO buffers are lost and messages can no longer be stored in transmission/reception FIFO buffers. Confirm that the CFEMP flag is set to 1 before setting the CFE bit to 1 again.

35.8 Test Function

The test function is classified into communication tests and global tests.

- Communication tests: Performed for each channel.
  - Standard test mode
  - Listen-only mode
  - Self-test mode 0 (external loopback mode)
  - Self-test mode 1 (internal loopback mode)
- Global tests: Performed for the entire module
  - RAM test (read/write test)
  - Inter-channel communication test

35.8.1 Standard Test Mode

Standard test mode allows CRC test.

35.8.2 Listen-Only Mode

Listen-only mode allows reception of data frames and remote frames. Only recessive bits are transmitted on the CAN bus, and the ACK bit, overload flag, and active error flag are not transmitted.
Listen-only mode is available for detecting the communication speed.
Do not make a transmission request from any buffer or queue in listen-only mode.
Figure 35.12 shows the connection when listen-only mode is selected.

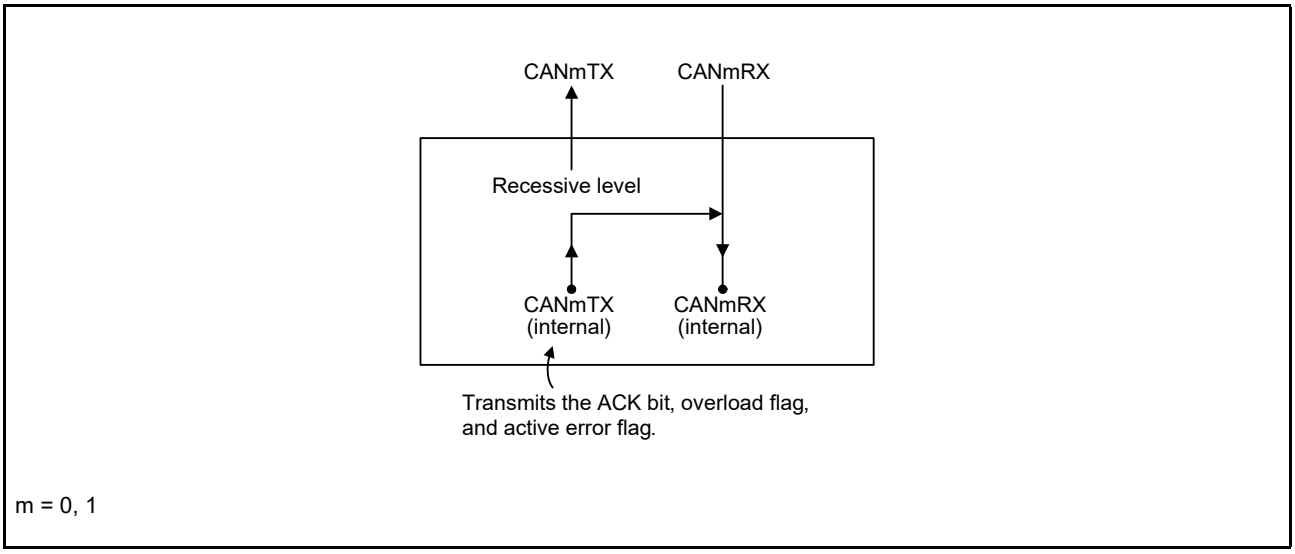


Figure 35.12 Connection when Listen-Only Mode is Selected

35.8.3 Self-Test Mode (Loopback Mode)

In self-test mode, transmitted messages are compared with the reception rule of the own channel and the messages are stored in a buffer if they have passed through the filter processing. Messages transmitted from other CAN nodes are compared only with the reception rule for which the GAFLLB bit in the RSCAN0GAFLIDj register (j = 0 to 15) is set to 0 (when a message transmitted from another CAN node is received).
If the mirror function and self-test mode are both enabled, the self-test mode setting takes precedence.

35.8.3.1 Self-Test Mode 0 (External Loopback Mode)

Self-test mode 0 is used to perform a loopback test within a channel including the CAN transceiver.
In self-test mode 0, transmitted messages are handled as messages received through the CAN transceiver and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.
Figure 35.13 shows the connection when self-test mode 0 is selected.

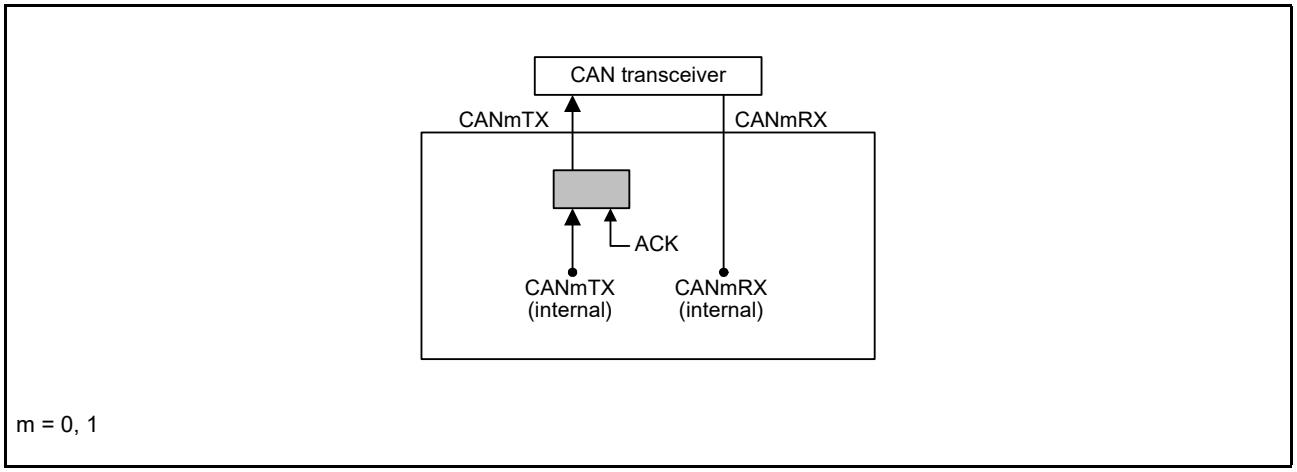


Figure 35.13 Connection when Self-Test Mode 0 is Selected

35.8.3.2 Self-Test Mode 1 (Internal Loopback Mode)

In self-test mode 1, transmitted messages are handled as received messages and are stored in a buffer. An ACK bit is generated to receive messages transmitted from the own CAN node.
In self-test mode 1, internal feedback from the internal CANmTX pin (m = 0, 1) to the internal CANmRX pin is performed. The external CANmRX pin input is isolated. The external CANmTX pin outputs only recessive bits.
Figure 35.14 shows the connection when self-test mode 1 is selected.

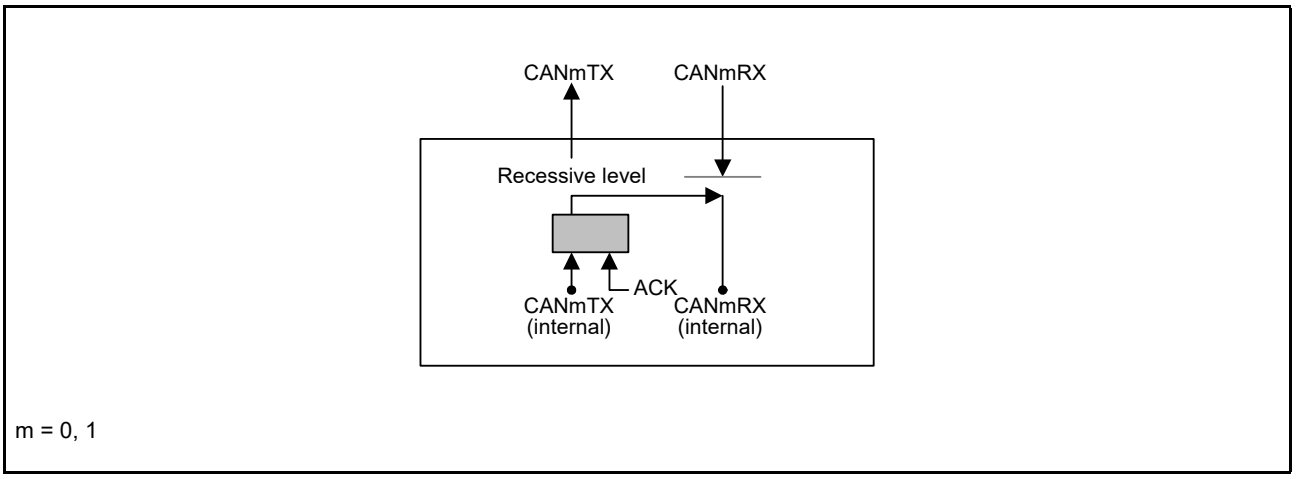


Figure 35.14 Connection when Self-Test Mode 1 is Selected

35.8.4 RAM Test

The RAM test function allows accesses to all CAN RAM addresses.
When the RAM test function is used, the RAM is divided into pages of 256 bytes each. RAM test page is set by the RTMPS[6:0] bits in the RSCAN0GTSTCFG register. Data in the set page can be read from and written to the RSCAN0RPGACCr register (r = 0 to 63). The available total RAM size is 14592 bytes (3900h).

35.8.5 Inter-Channel Communication Test

The inter-channel communication test function allows communication test by internally connecting CAN channels to each other. During this test, channels are isolated from the external CAN bus.
Before starting data transmission/reception in channel communication mode, make transmission/reception settings for each channel.
Figure 35.15 shows the connection for inter-channel communication test.

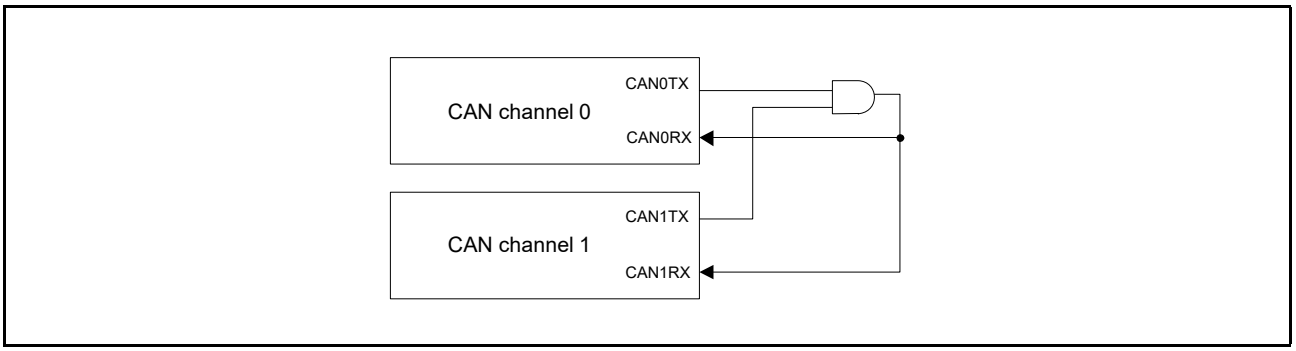


Figure 35.15 Connection for Inter-Channel Communication Test

35.9 RSCAN Setting Procedure

35.9.1 Initial Settings

The RSCAN module initializes the CAN RAM after the MCU is reset. The RAM initialization time is 7298 cycles of PCLKD. The GRAMINIT flag in the RSCAN0GSTS register is set to 1 (CAN RAM initialization is ongoing) during the RAM initialization and is cleared to 0 (CAN RAM initialization is finished) when the initialization is completed. Make CAN settings after the GRAMINIT flag is cleared to 0. Figure 35.16 shows the CAN setting procedure after the MCU is reset.

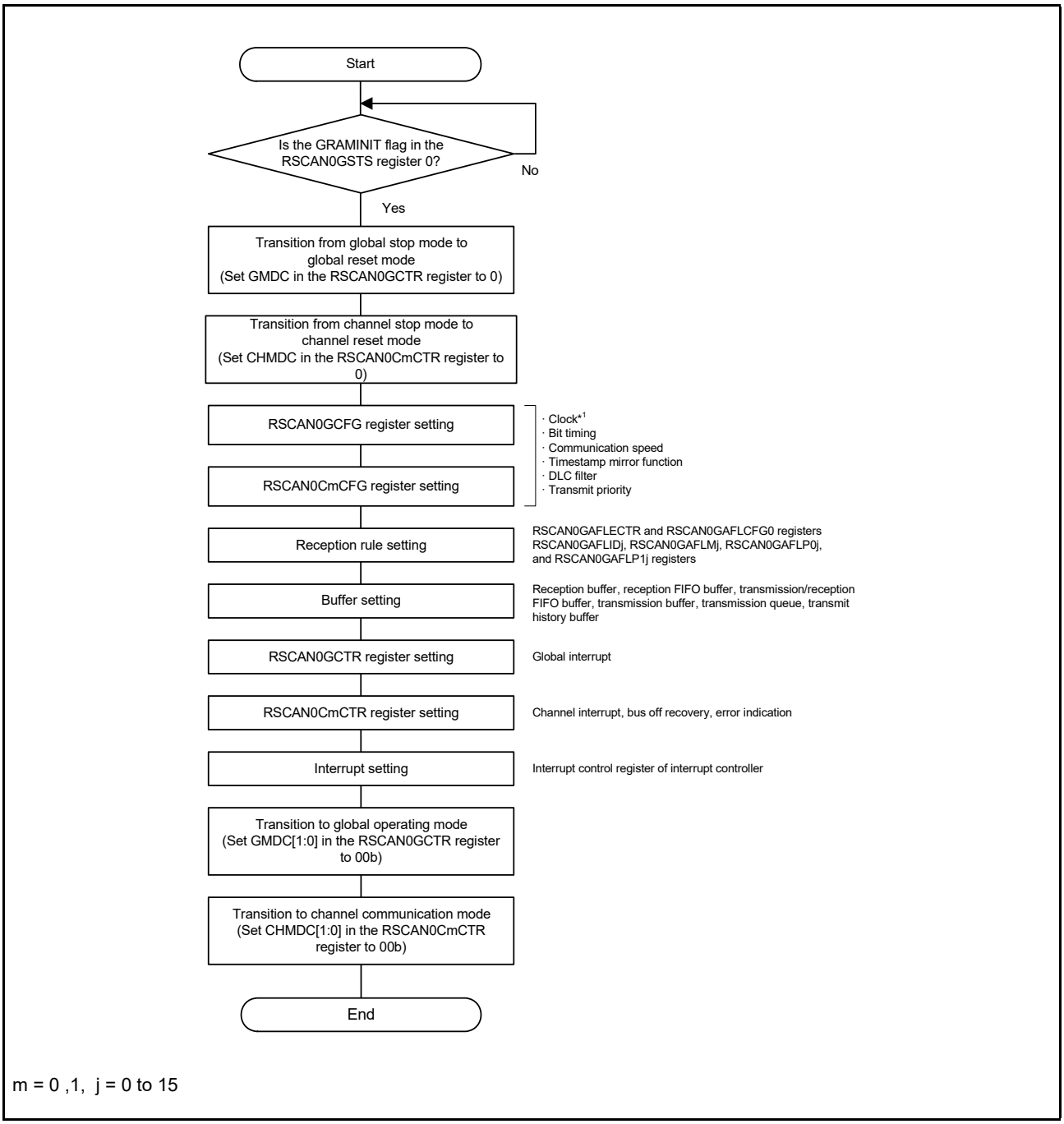


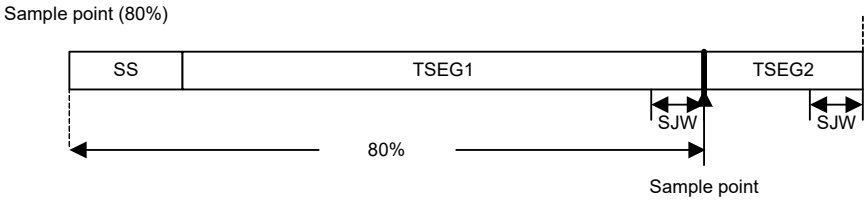
Figure 35.16 CAN Setting Procedure after the MCU is Reset

35.9.1.1 Clock Setting

Set the CAN clock (fCAN) as a clock source of the RSCAN module. Select CANCLKA (24 MHz) or CANCLKB (25 MHz) using the DCS bit in the RSCAN0GCFG register.

35.9.1.2 Bit Timing Setting

In the CAN protocol, one bit of a communication frame consists of three segments SS, TSEG1, and TSEG2, of which two segments TSEG1 and TSEG2 can be set by the RSCAN0CmCFG register for each channel. Sample point timing can be determined by setting these two segments. This timing can be adjusted in units of 1 Time Quantum (hereafter referred to as Tq). 1 Tq is equal to one CANmTq clock cycle. The CANmTq clock is obtained by selecting the clock source with the DCS bit in the RSCAN0GCFG register and selecting the clock division ratio with the BRP[9:0] bits in the RSCAN0CmCFG register.
Figure 35.17 shows the bit timing chart. Table 35.22 shows an example of bit timing setting.



SS = 1 Tq fixed
Set TSEG1 to a range of 4 Tq to 16 Tq
Set TSEG2 to a range of 2 Tq to 8 Tq
Set SJW to a range of 1 Tq to 4 Tq
Set SS + TSEG1 + TSEG2 to a range of 8 Tq to 25 Tq
TSEG1 > TSEG2 > SJW

- SS (synchronization segment):
  The SS is a segment that performs synchronization by monitoring the edge from recessive to dominant bits in the Interframe Space. Interframe Space consists of Intermission, Suspend Transmission, and Bus Idle. All nodes can start transmission during Bus Idle.
- TSEG1 (Time segment 1):
  TSEG1 is a segment that absorbs physical delay on the CAN network. The physical delay on the CAN network is twice the total of the delay on the CAN bus, the delay in the input comparator, and the delay in the output driver.
- TSEG2 (Time segment 2):
  TSEG2 is a segment that compensates phase error due to an error in frequency.
- SJW (Resynchronization jump width):
  The SJW is a length to extend or reduce the time segment to compensate for an error in phase due to phase error.

Figure 35.17 Bit Timing Chart

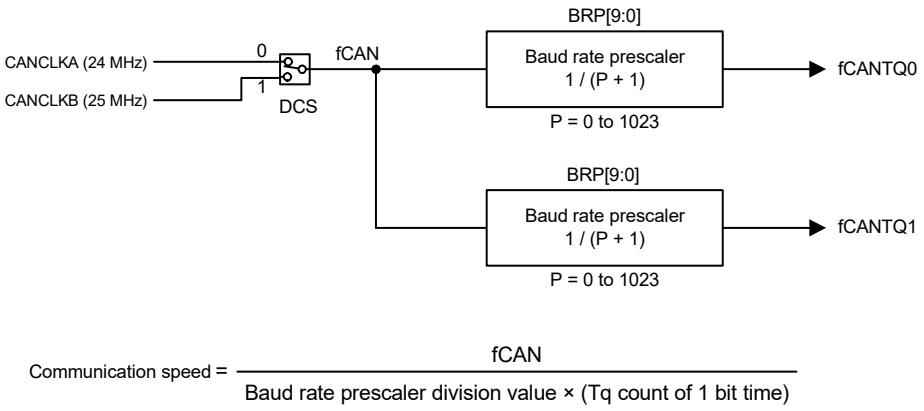
Table 35.22 Example of Bit Timing Setting

1 Bit	Set Value (Tq)				Sample Point (%) Note: See Figure 35.17.
	SS	TSEG1	TSEG2	SJW	
8 Tq	1	4	3	1	62.50
	1	5	2	1	75.00
10 Tq	1	6	3	1	70.00
	1	7	2	1	80.00
12 Tq	1	8	3	1	75.00
	1	9	2	1	83.33
16 Tq	1	10	5	1	68.75
	1	11	4	1	75.00
20 Tq	1	12	7	1	65.00
	1	13	6	1	70.00
24 Tq	1	15	8	1	66.67
	1	16	7	1	70.83
25 Tq	1	16	8	1	68.00

35.9.1.3 Communication Speed Setting

Set the CAN communication speed for each channel using the fCAN, baud rate prescaler division value (BRP[9:0] bits in the RSCAN0CmCFG register), and Tq count per bit time.

Figure 35.18 shows the CAN clock control block diagram, and Table 35.23 shows an example of the communication speed setting.



m = 0, 1
DCS: Bit in the RSCAN0GCFG register
BRP[9:0]: Bits in the RSCAN0CmCFG register
fCAN: CAN clock

Figure 35.18 CAN Clock Control Block Diagram

Table 35.23 Example of Communication Speed Setting

Communication Speed \ fCAN	25 MHz	24 MHz
1 Mbps	25 Tq (1)	8 Tq (3) 12 Tq (2) 24 Tq (1)
500 Kbps	25 Tq (2) 10 Tq (5)	8 Tq (6) 12 Tq (4) 24 Tq (2)
250 Kbps	25 Tq (4) 10 Tq (10)	8 Tq (12) 12 Tq (8) 24 Tq (4)
125 Kbps	25 Tq (8) 10 Tq (20)	8 Tq (24) 12 Tq (16) 24 Tq (8)

Note: Values in ( ) are baud rate prescaler division values.

35.9.1.4 Reception Rule Setting

Reception rules can be set using reception rule-related registers.
Up to 16 reception rules can be registered per page. Specify pages 0 to 7 by the AFLPN[4:0] bits in the RSCAN0GAFLECTR register. Enable or disable writing to the reception rule table using the AFLDAE bit.
Figure 35.19 shows the reception rule setting procedure.

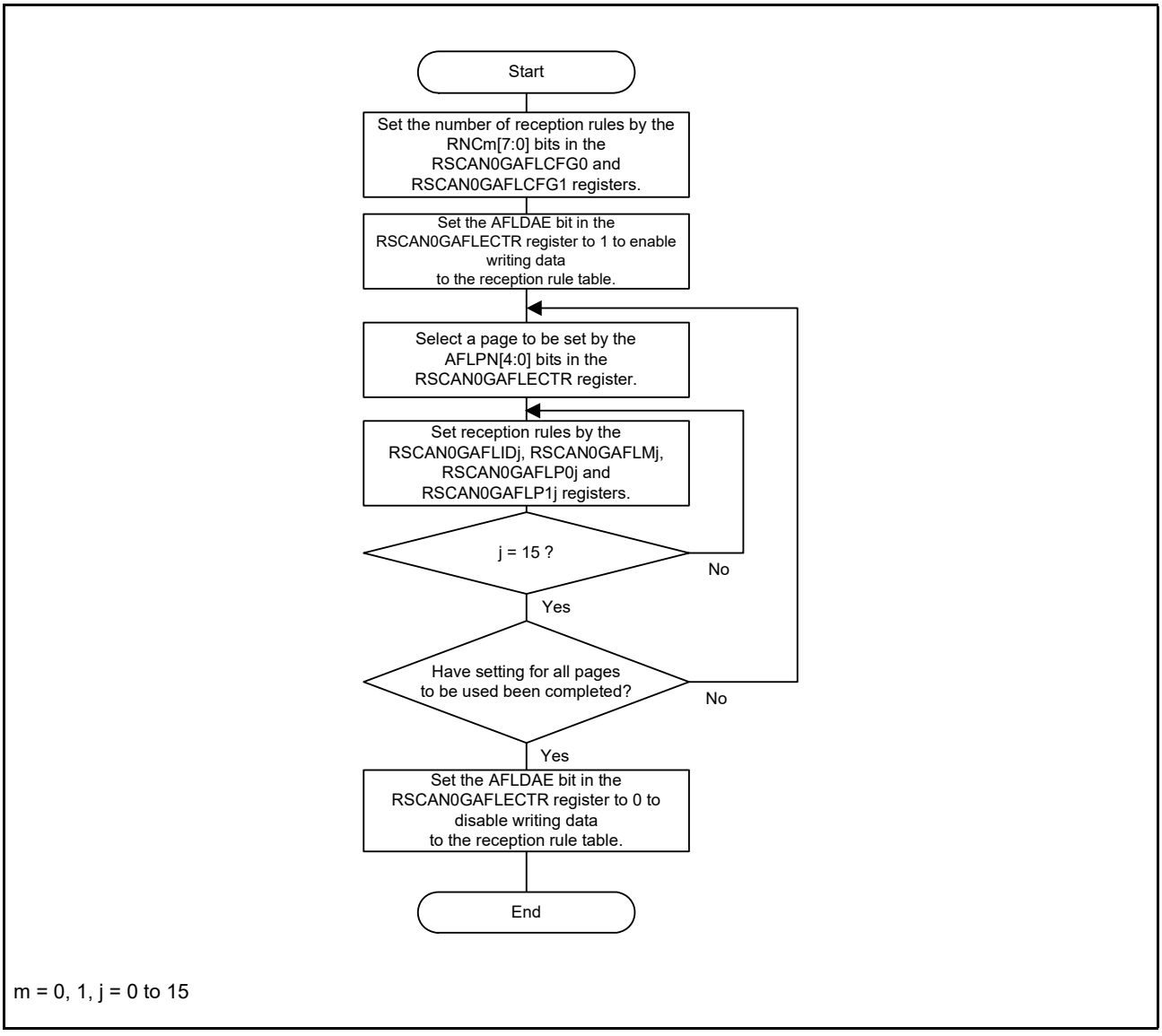


Figure 35.19 Reception Rule Setting Procedure

35.9.1.5 Buffer Setting

Set sizes and interrupt sources of buffers. For transmission/reception FIFO buffers that are set to transmission mode, set transmission buffers to be linked.

Figure 35.20 shows the buffer configuration. Figure 35.21 shows the buffer setting procedure.

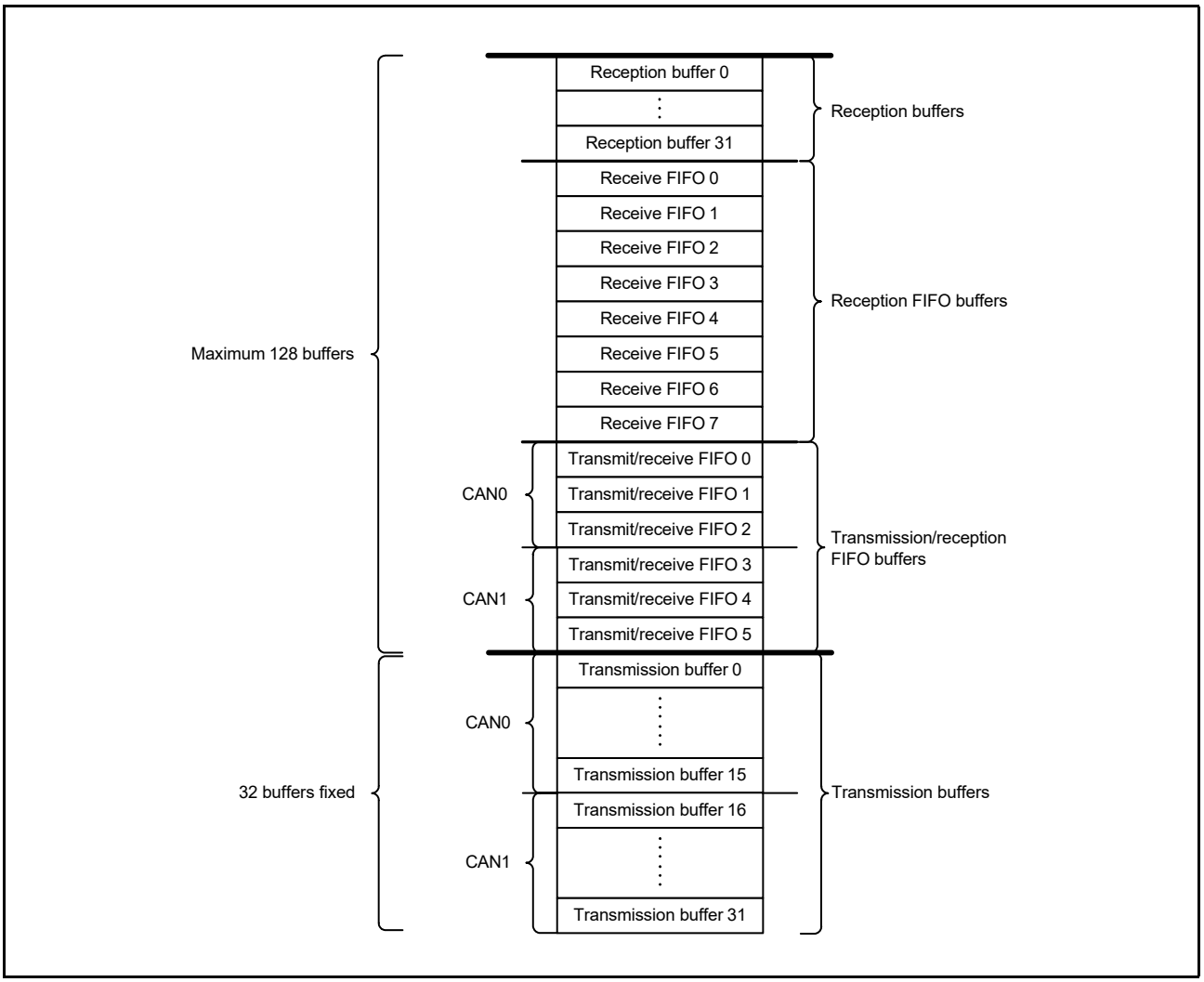


Figure 35.20 Buffer Configuration

Note: Reception buffers, reception FIFO buffers, transmission/reception FIFO buffers, and transmission buffers are located in succession.

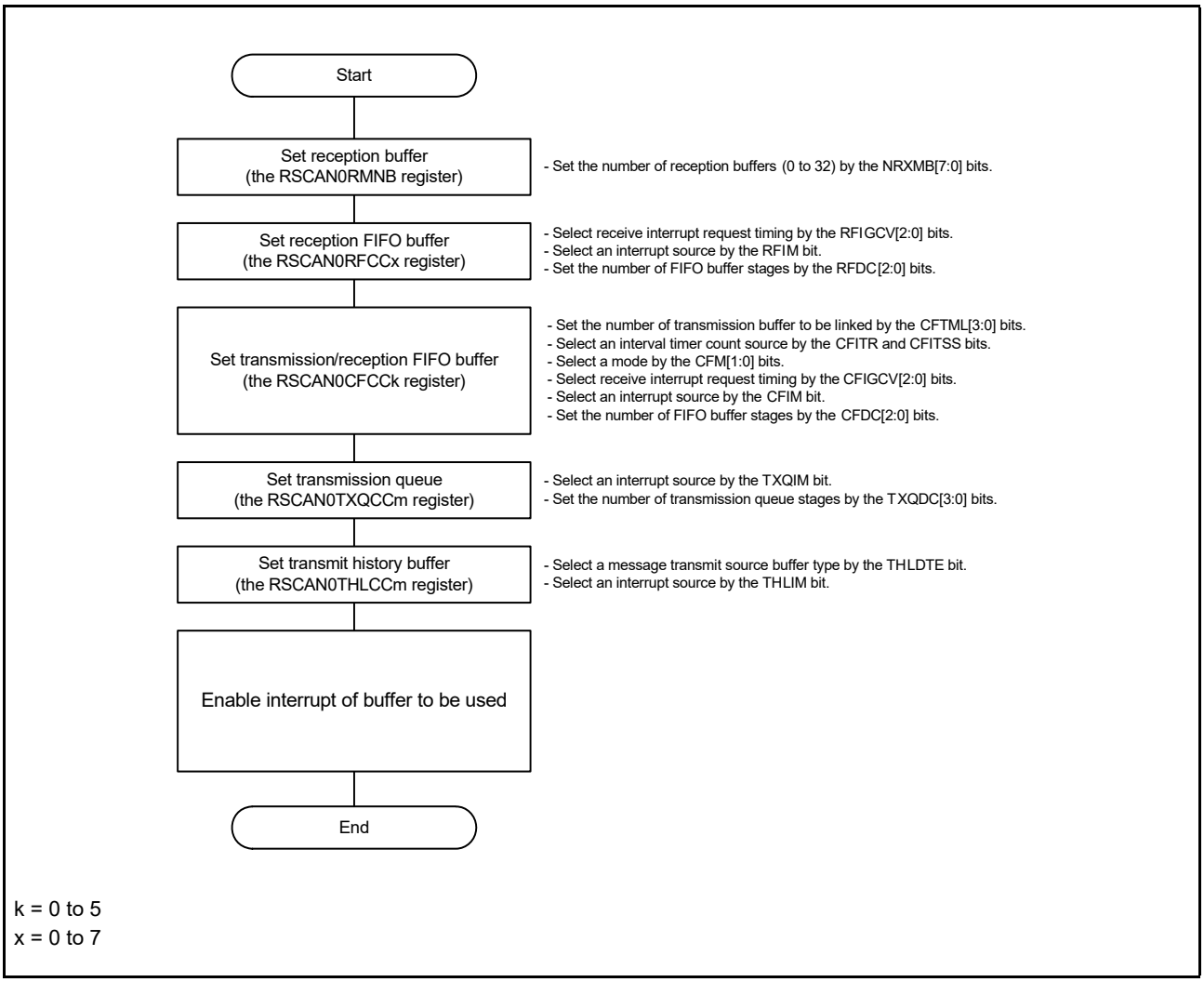


Figure 35.21 Buffer Setting Procedure

35.9.2 Reception Procedure

35.9.2.1 Reception Buffer Reading Procedure

When the processing to store received messages in a reception buffer starts, the RMNSq flag in the RSCAN0RMND0 register (q = 0 to 31) is set to 1 (reception buffer q contains a new message). Messages can be read from the RSCAN0RMIDq, RSCAN0RMPTRq, RSCAN0RMDF0q, and RSCAN0RMDF1q registers. If the next message has been received before the current message is read from the reception buffer, the message is overwritten. Figure 35.22 shows the reception buffer reading procedure.

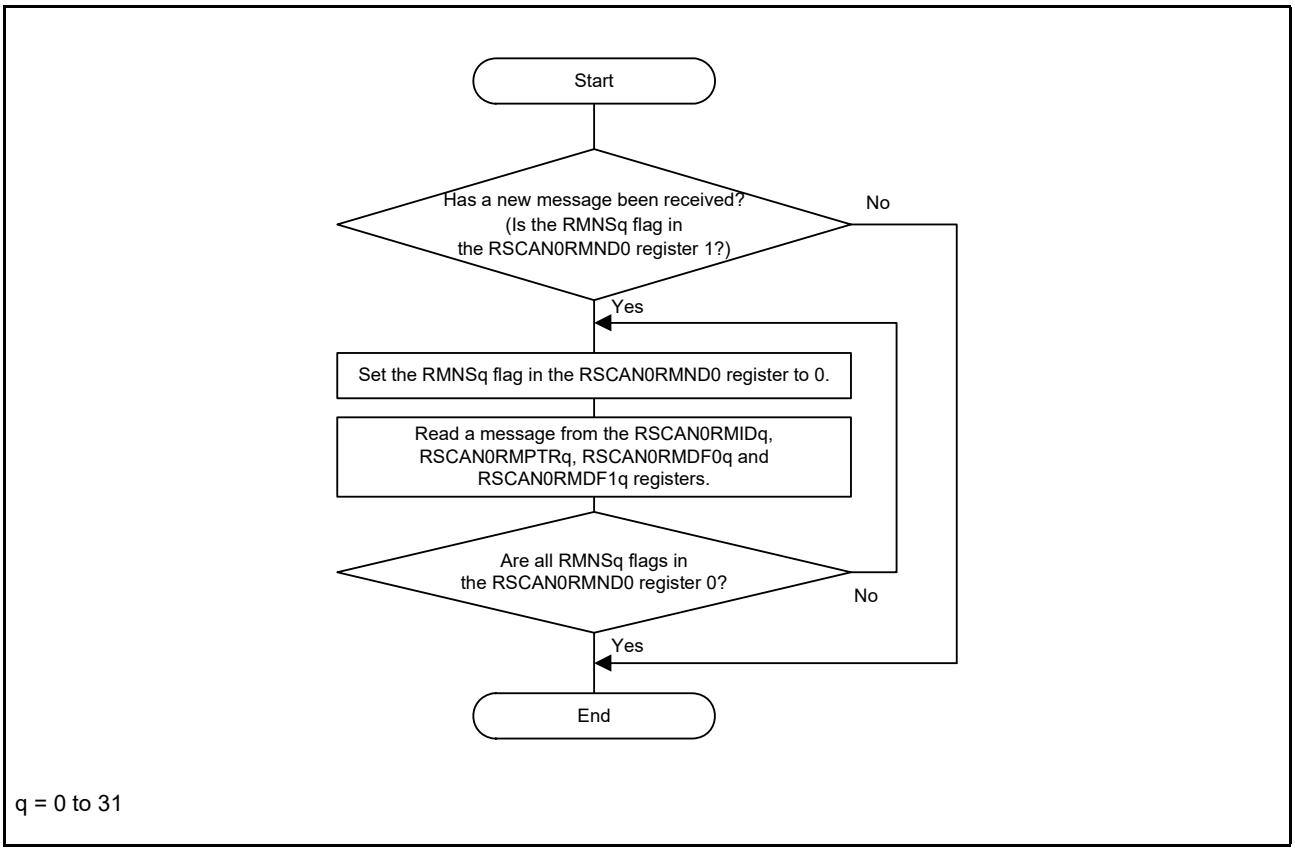
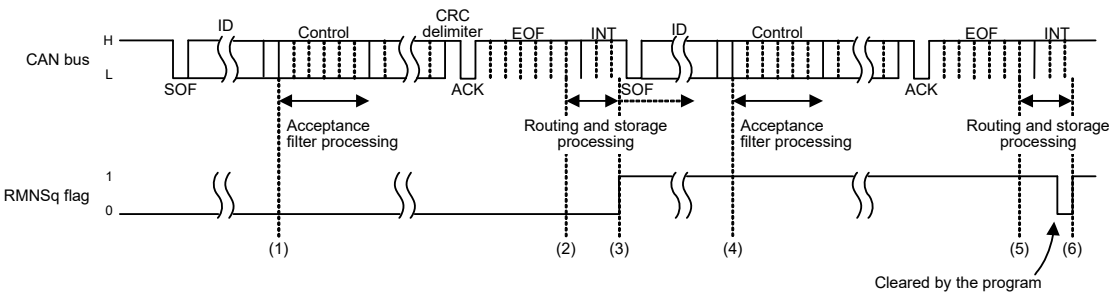


Figure 35.22 Reception Buffer Reading Procedure



q = 0 to 31
RMNSq: Flag in the RSCAN0RMND0 register

Figure 35.23 Reception Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.

(2) When the message matches the reception rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RSCAN0GCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(3) When the message has passed through the DLC filter processing, the processing to store the message in the specified reception buffer starts.
When the message storage processing starts, the RMNSq flag in the corresponding RSCAN0RMND0 register is set to 1 (the reception buffer contains a new message). If other channels are performing filter processing or transmit priority determination processing, the routing processing and the storage processing may be delayed.

(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) When the message matches the reception rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RSCAN0GCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(6) When the corresponding RMNSq flag is cleared to 0 (the reception buffer contains no new message), this flag is set to 1 again when the message storage processing starts. Even if the RMNSq flag remains 1, a new message is overwritten to the reception buffer. The RMNSq flag should not be cleared to 0 during storage of messages.

35.9.2.2 FIFO Buffer Reading Procedure

When received messages have been stored in one or more reception FIFO buffers or a transmission/reception FIFO buffer that is set to reception mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCAN0RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCAN0CFSTSk register (k = 0 to 5)) is incremented. At this time, when the RFIE bit (receive FIFO interrupt is enabled) in the RSCAN0RFCCx register or the CFRXIE bit (transmit/receive FIFO receive interrupt is enabled) in the RSCAN0CFCCk register is set to 1, an interrupt request is generated. Received messages can be read from the RSCAN0RFIDx, RSCAN0RFPTRx, RSCAN0RFDF0x, and RSCAN0RFDF1x registers for reception FIFO buffers, or from the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers for transmission/reception FIFO buffers. Messages in FIFO buffers can be read sequentially on a first-in, first-out basis.

When the message count display counter value matches the FIFO buffer depth (a value set by the RFDC[2:0] bits in the RSCAN0RFCCx register or the CFDC[2:0] bits in the RSCAN0CFCCk register), the RFFLL or CFFLL flag is set to 1 (the reception FIFO buffer is full).

When all messages have been read out of the FIFO buffer, the RFEMP flag in the RSCAN0RFSTSx register or the CFEMP flag in the RSCAN0CFSTSk register is set to 1 (the reception FIFO buffer contains no unread message (buffer empty)).

If the RFE bit or the CFE bit is cleared to 0 (no reception FIFO buffer is used) with the interrupt request flag (RFIF flag in the RSCAN0RFSTSx register or CFRXIF flag in the RSCAN0CFSTSk register) set to 1 (a receive FIFO interrupt request is present), the interrupt request flag is not automatically cleared to 0. The program must clear the interrupt request flag to 0.

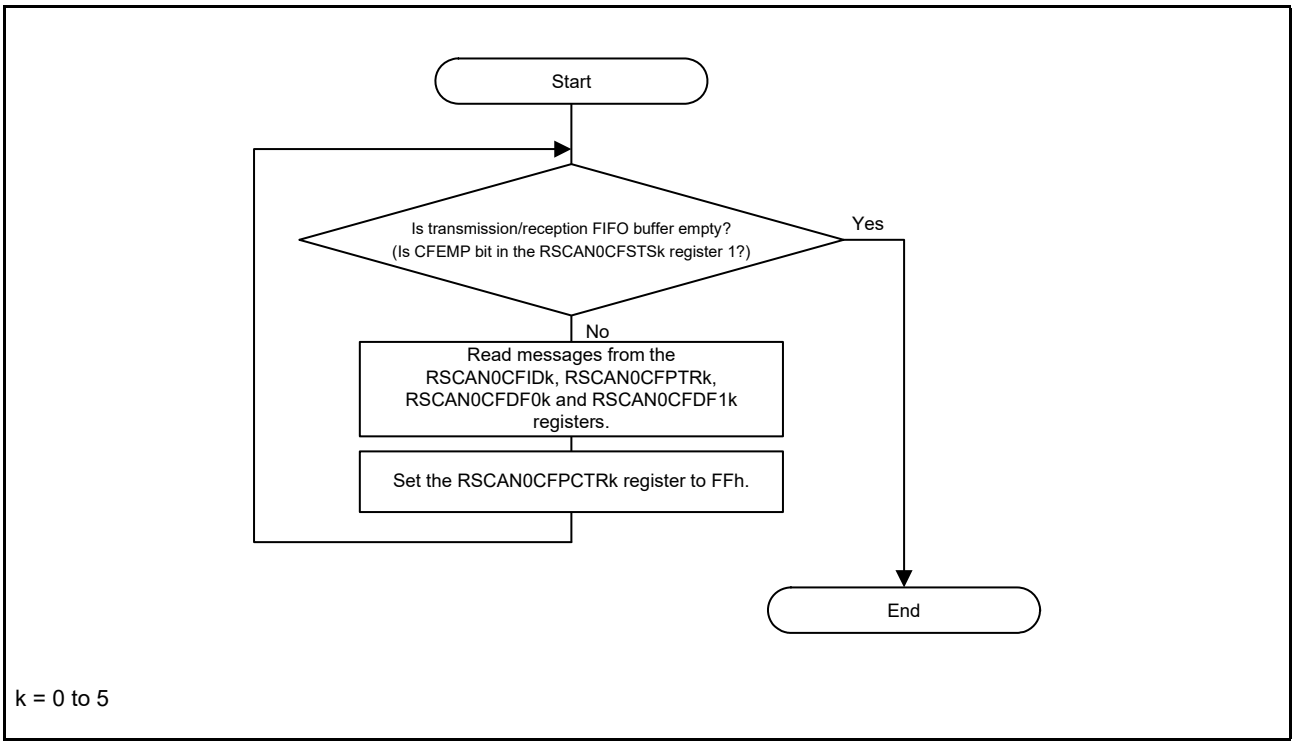
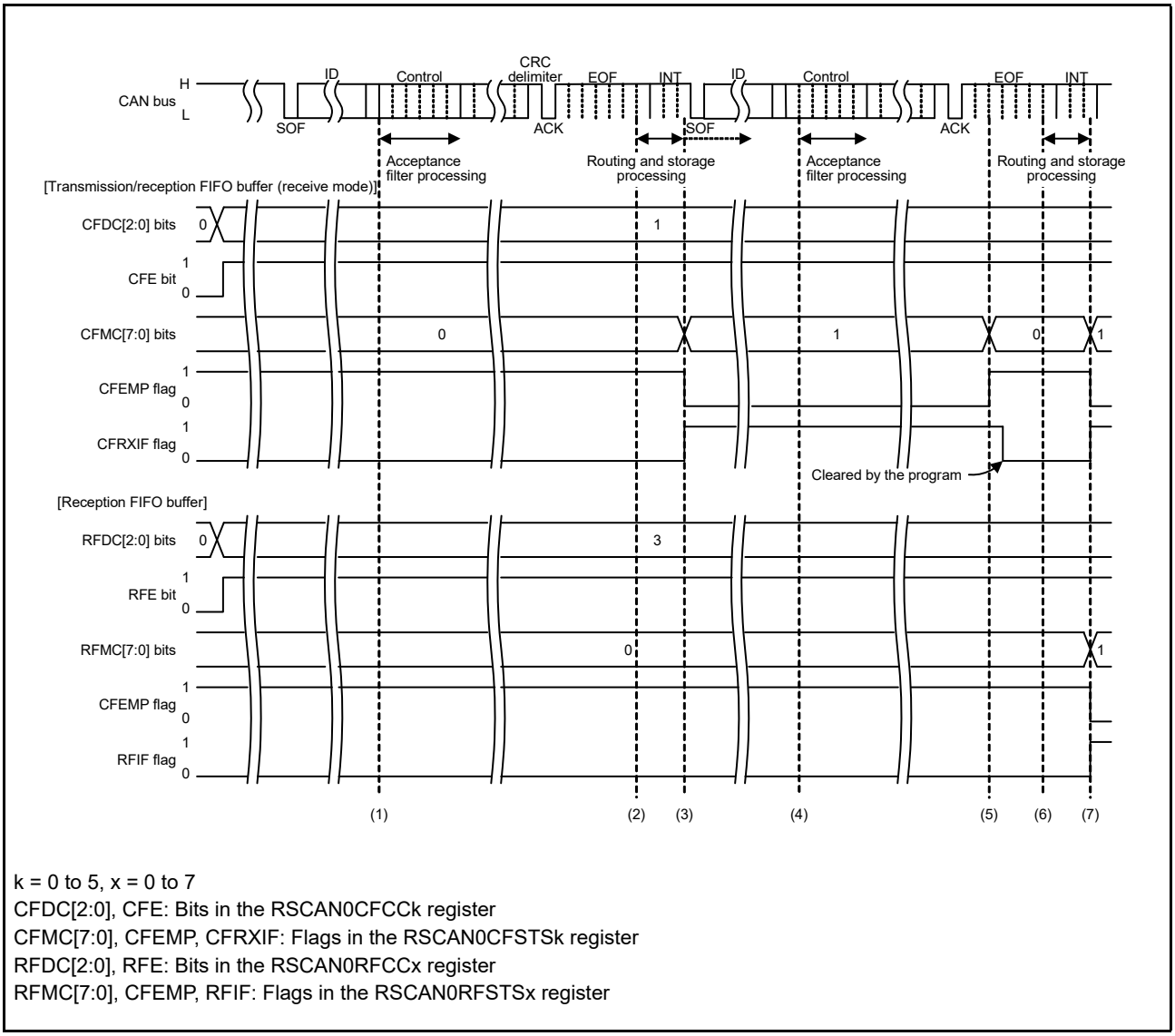


Figure 35.24 Transmission/Reception FIFO Buffer Reading Procedure



k = 0 to 5, x = 0 to 7
CFDC[2:0], CFE: Bits in the RSCAN0CFCCk register
CFMC[7:0], CFEMP, CFRXIF: Flags in the RSCAN0CFSTSk register
RFDC[2:0], RFE: Bits in the RSCAN0RFCCx register
RFMC[7:0], CFEMP, RFIF: Flags in the RSCAN0RFSTSx register

Figure 35.25 FIFO Buffer Reception Timing Chart

(1) When the ID field in a message has been received, the acceptance filter processing starts.
(2) When the message matches the reception rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RSCAN0GCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.
(3) When the message has passed through the DLC filter processing and the CFE bit in the RSCAN0CFCCk register is 1 (transmission/reception FIFO buffers are used) and the CFDC[2:0] value in the RSCAN0CFCCk register is 001b or more, the message is stored in the transmission/reception FIFO buffer that is set to reception mode. The CFMC[7:0] value in the RSCAN0CFSTSk register is incremented and becomes 01h. When the CFIM bit in the RSCAN0CFCCk register is set to 1 (a FIFO receive interrupt request is generated each time a message has been received), the CFRXIF flag in the RSCAN0CFSTSk register is set to 1 (a transmit/receive FIFO receive interrupt request is present). The CFRXIF flag can be reset to 0 by the program.
(4) When the ID field of the next message has been received, the acceptance filter processing starts.

(5) Read received messages from the RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers and write FFh to the RSCAN0CFPCTRk register. This causes the CFMC[7:0] bits in the RSCAN0CFSTSk register to be decremented. When CFMC[7:0] becomes 00h, the CFEMP flag in the RSCAN0CFSTSk register becomes 1 (the transmission/reception FIFO buffer contains no message (buffer empty)).

(6) When the message matches the reception rule of the corresponding channel and the message has been successfully received, the routing processing to transfer the message to the specified buffer starts. When the DCE bit in the RSCAN0GCFG register is set to 1 (DLC check is enabled), the DLC filter processing starts at this time.

(7) The message is stored in the transmission/reception FIFO buffer set in reception mode when the message has passed through the DLC filter process if the CFE bit is set to 1 (transmission/reception FIFO buffers are used), and the CFDC[2:0] bits are set to 001b or more. The CFMC[7:0] bit value is incremented by 1 to be 01h. When the CFIM bit is set to 1 (an interrupt occurs each time a message has been received), the CFRXIF flag is set to 1 (a transmit/receive FIFO receive interrupt request is present).
The message is stored in the reception FIFO buffer if the RFE bit in the RSCAN0RFCCx register is set to 1 (reception FIFO buffers are used), and the RFDC[2:0] bits in the RSCAN0RFCCx register are set to 001b or more. The RFMC[7:0] bits in the RSCAN0RFSTSx register are set to 01h by being incremented by 1. When the RFIM bit in the RSCAN0RFCCx register is set to 1 (an interrupt occurs each time a message has been received), the RFIF flag in the RSCAN0RFSTSx register is set to 1 (a receive FIFO interrupt request is present).

35.9.3 Transmission Procedure

35.9.3.1 Procedure for Transmission from Transmission Buffers

Figure 35.26 shows the procedure for transmission from transmission buffers.
Figure 35.27 shows a timing chart where messages are transmitted from two transmission buffers in the same channel and transmission has been successfully completed. Figure 35.28 shows a timing chart where messages are transmitted from two transmission buffers in the same channel and transmission abort has been completed.

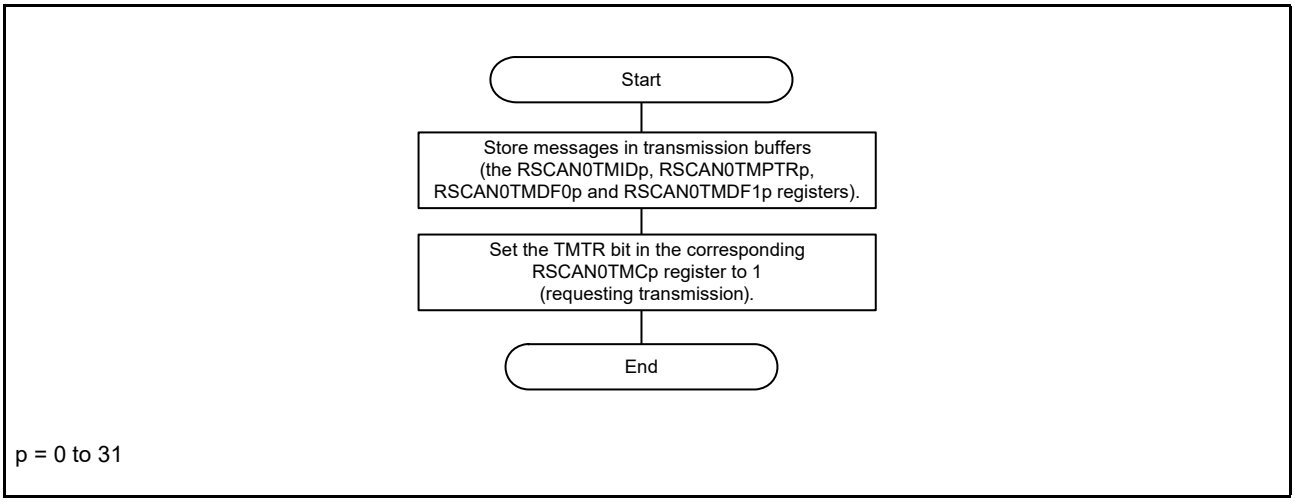
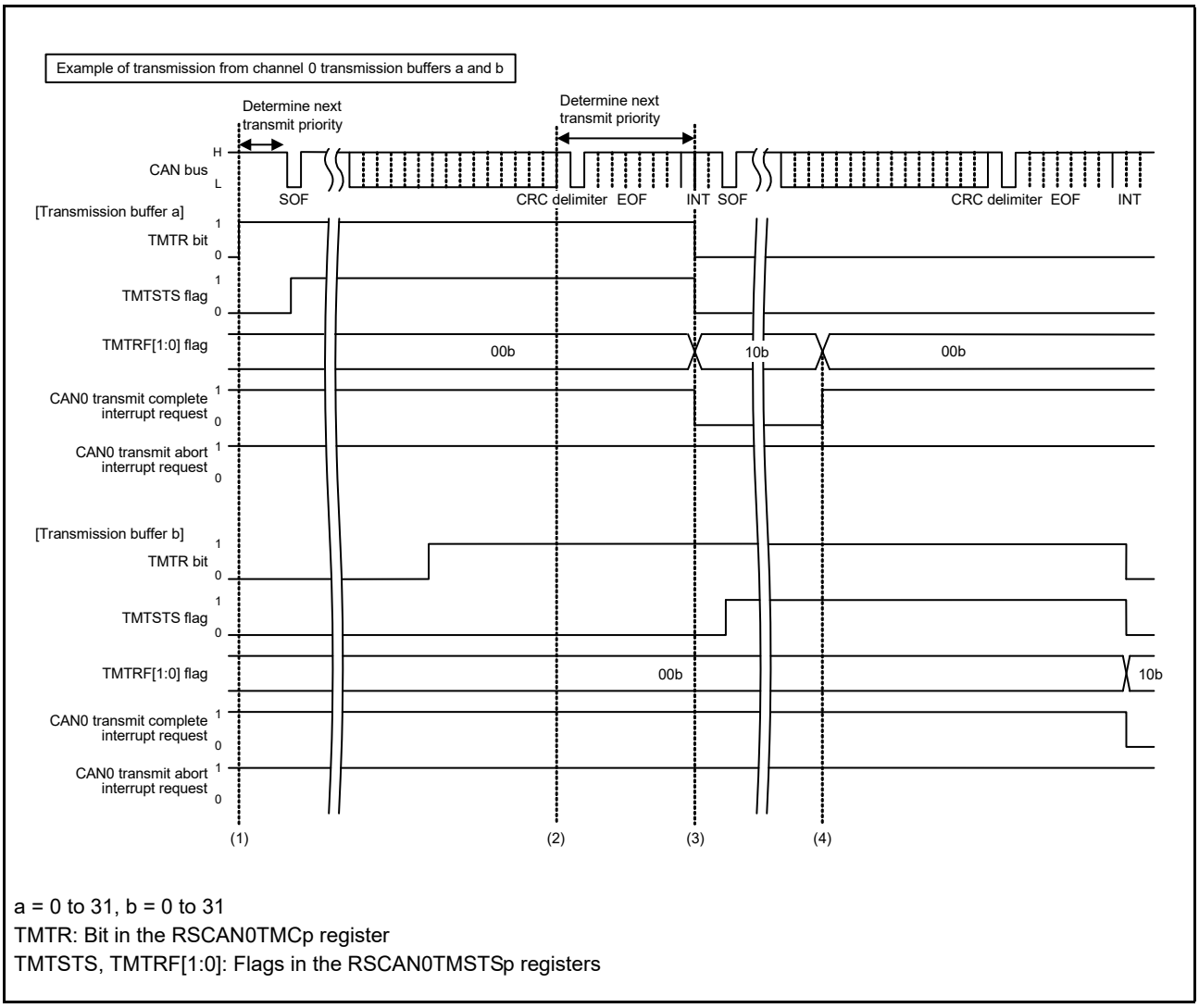


Figure 35.26 Procedure for Transmission from Transmission Buffers



a = 0 to 31, b = 0 to 31
TMTR: Bit in the RSCAN0TMCp register
TMTSTS, TMTRF[1:0]: Flags in the RSCAN0TMSTSp registers

Figure 35.27 Transmission Buffer Transmission Timing Chart (Transmission Completed Successfully)

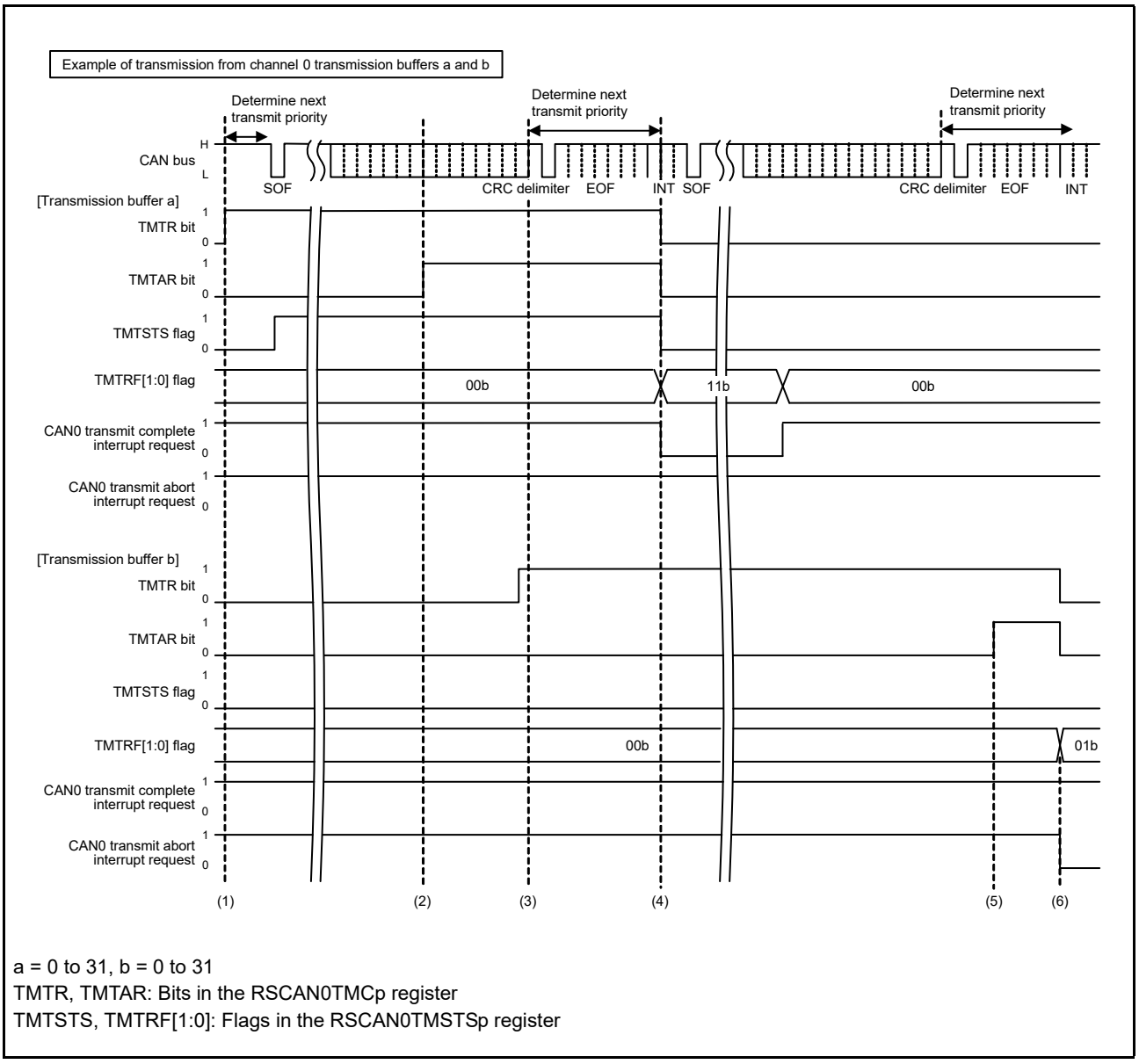
(1) When the TMTR bit in the RSCAN0TMCa register is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmission buffer. If transmission buffer a is determined to be the highest-priority transmission buffer, the TMTSTS flag in the corresponding RSCAN0TMSTSa register is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

(2) When a transmission request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(3) When transmission completes successfully, the TMTRF[1:0] flag in the RSCAN0TMSTSa register is set to 10b (transmission has been completed (without transmission abort request)) and the TMTSTS flag and the TMTR bit in the RSCAN0TMCa register are cleared to 0. When the TMIEa bit in the RSCAN0TMIEC0 register is 1 (transmission buffer interrupt is enabled), a CAN0 transmission complete interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00b (transmission is in progress or no transmission request is present).

(4) Before starting the next transmission, set the TMTRF[1:0] flag to 00b. Write the next message to the transmission buffer, and then set the TMTR bit to 1 (transmission is requested). The TMTR bit can be set to 1 only when the TMTRF[1:0] flag value is 00b.

If an arbitration-lost has occurred after transmission is started, the TMTSTS flag is cleared to 0. The transmit priority determination is reexecuted at the beginning of the CRC delimiter to search the highest-priority transmission buffer. If an error has occurred during transmission or after arbitration loss, the priority determination processing is reexecuted during transmission of an error frame.



a = 0 to 31, b = 0 to 31
TMTR, TMTAR: Bits in the RSCAN0TMCp register
TMTSTS, TMTRF[1:0]: Flags in the RSCAN0TMSTSp register

Figure 35.28 Transmission Buffer Transmission Timing Chart (Transmission Abort Completed)

(1) When the TMTR bit in the RSCAN0TMCa register is set to 1 while the CAN bus is idle, the transmit priority determination processing starts to determine the highest-priority transmission buffer. If transmission buffer a is determined to be the highest-priority transmission buffer, the TMTSTS flag in the corresponding RSCAN0TMSTSa register is set to 1 (transmission is in progress) and the CAN channel starts transmitting data.

(2) When it is determined that the transmission buffer is used for the next transmission or transmission is in progress, message transmission is not aborted unless an error or arbitration loss occurs even if the TMTAR bit is set to 1 (transmission abort is requested).

(3) The priority determination starts with the CRC delimiter for the next transmission. In this timing chart, buffer b is not selected as the next transmission buffer. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(4) When transmission completes successfully, the TMTRF[1:0] flag in the RSCAN0TMSTSa register is set to 11b (transmission has been completed (with transmission abort request)) and the TMTSTS flag and the TMTR bit in the RSCAN0TMCa register are cleared to 0. When the TMIEa value in the RSCAN0TMIEC0 register is 1 (transmission buffer interrupt is enabled), a CAN0 transmission complete interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00b (transmission is in progress or no transmission request is present).

(5) While another CAN node is transmitting data on the CAN bus (TMTSTS flag = 0), if the TMTAR bit is set to 1 while the corresponding channel is determining transmit priority, the TMTR bit cannot be cleared to 0.

(6) After the internal processing time has passed, the transmission is terminated and the TMTRF[1:0] flag is set to 01b. When the transmission buffer is not transmitting data and is not selected as the next transmission buffer and priority determination is not being made, an abort request is immediately accepted and the TMTRF[1:0] flag is set to 01b. At this time, the TMTR and TMTAR bits are cleared to 0. When transmission abort is completed with the TAIE bit in the RSCAN0CmCTR register set to 1 (transmission abort interrupt is enabled), an interrupt request is generated. To clear the interrupt request, set the TMTRF[1:0] flag to 00b.

If an arbitration loss has occurred after the CAN channel started transmission, the TMTSTS bit is cleared to 0. The transmit priority determination is reexecuted at the beginning of the CRC delimiter to find the highest-priority transmission buffer. If an error has occurred during transmission or after arbitration loss, the priority determination processing is reexecuted during transmission of an error frame.

35.9.3.2 Procedure for Transmission from Transmission/Reception FIFO Buffer

Figure 35.29 shows the procedure for transmission from transmission/reception FIFO buffers.
Figure 35.30 shows a timing chart where messages are transmitted from two transmission/reception FIFO buffers in the same channel and transmission has been successfully completed. Figure 35.31 shows a timing chart where messages are transmitted from two transmission/reception FIFO buffers in the same channel and transmission abort has been completed.

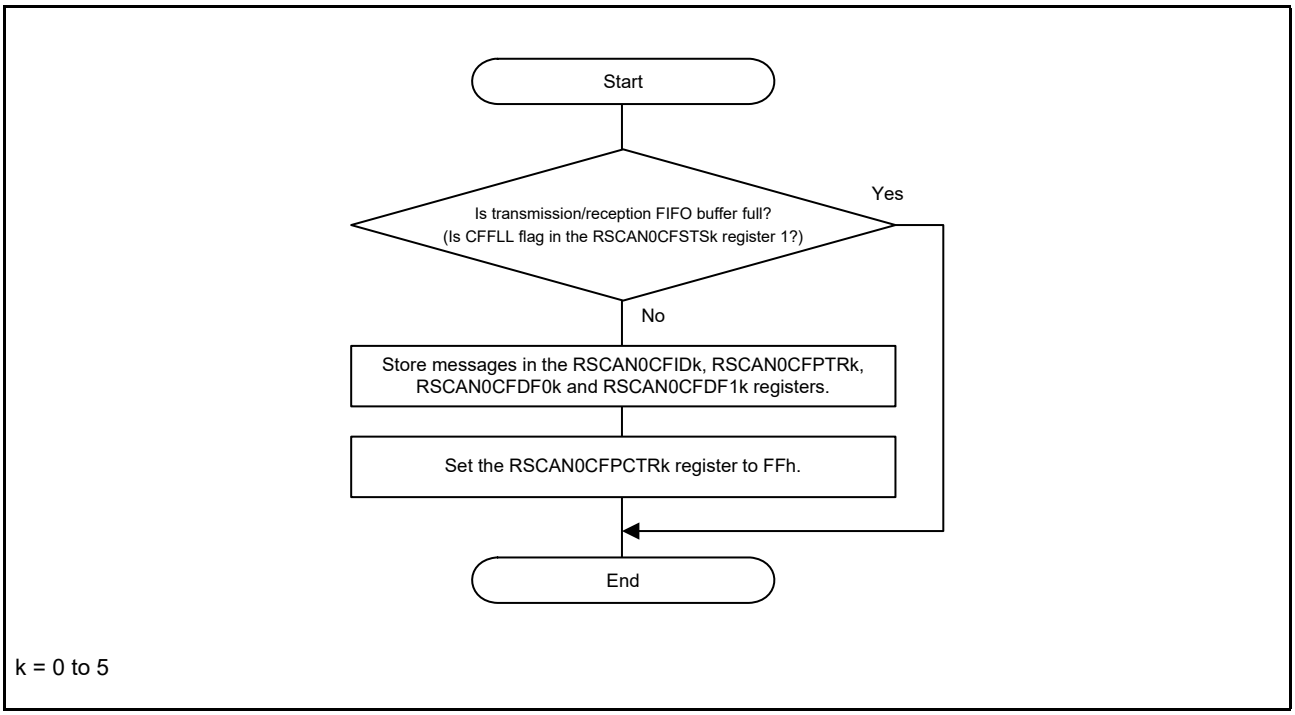


Figure 35.29 Procedure for Transmission from Transmission/Reception FIFO Buffers

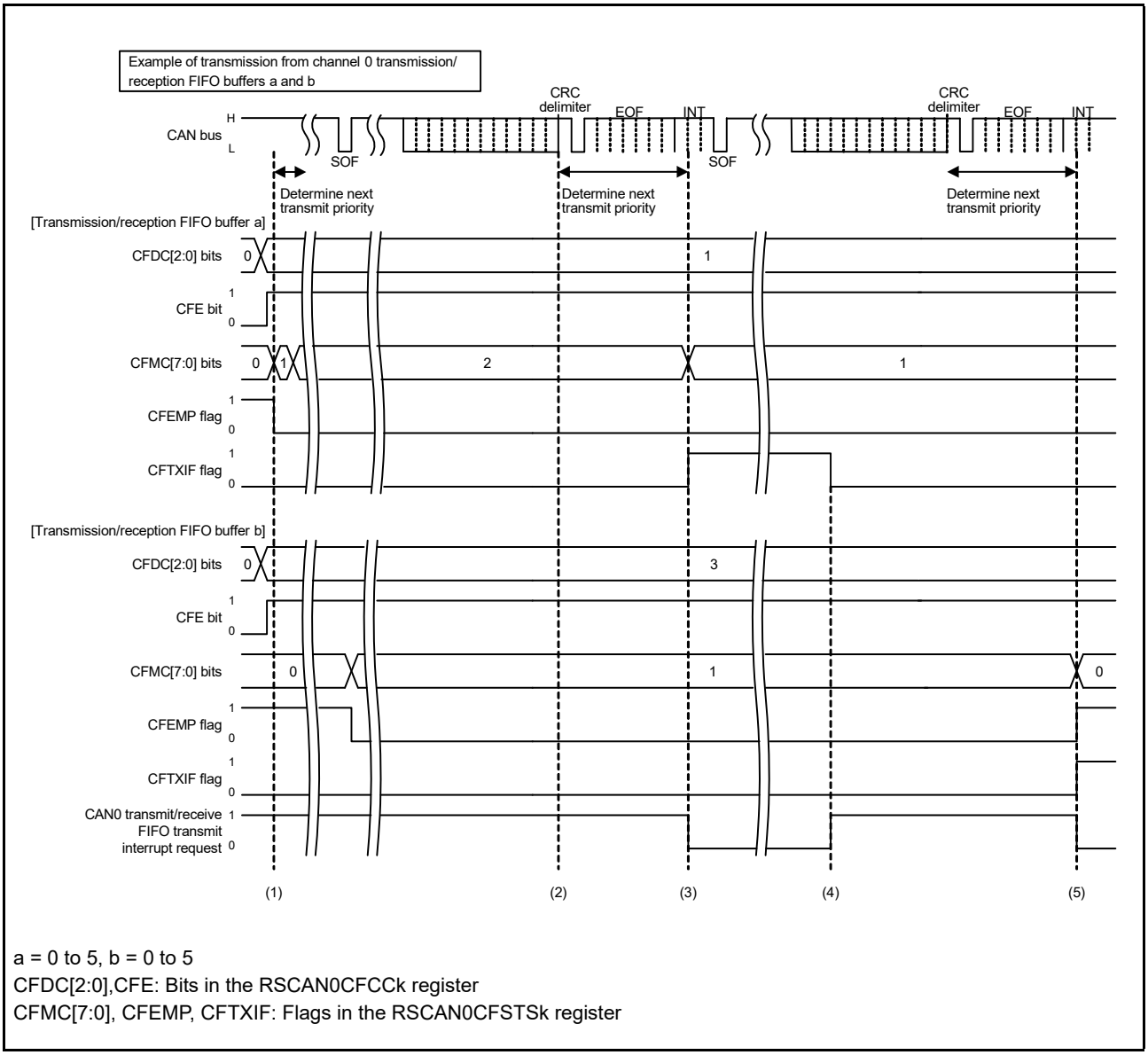


Figure 35.30 Transmission/Reception FIFO Buffer Transmission Timing Chart (Transmission Completed Successfully)

(1) While the CAN bus is idle, when the CFE bit in the RSCA0CFCCa register is 1 (transmission/reception FIFO buffers are used) and the CFDC[2:0] value in the RSCAN0CFCCa register is 001b (4 messages) or more and the CFMC[7:0] value in the RSCAN0CFSTSa register is 01h or more, the priority determination processing starts to determine the highest-priority message for transmission. When the highest-priority message for transmission has been determined, transmission of the message starts. In this figure, the message is transmitted from transmission/ reception FIFO buffer a of channel 0.

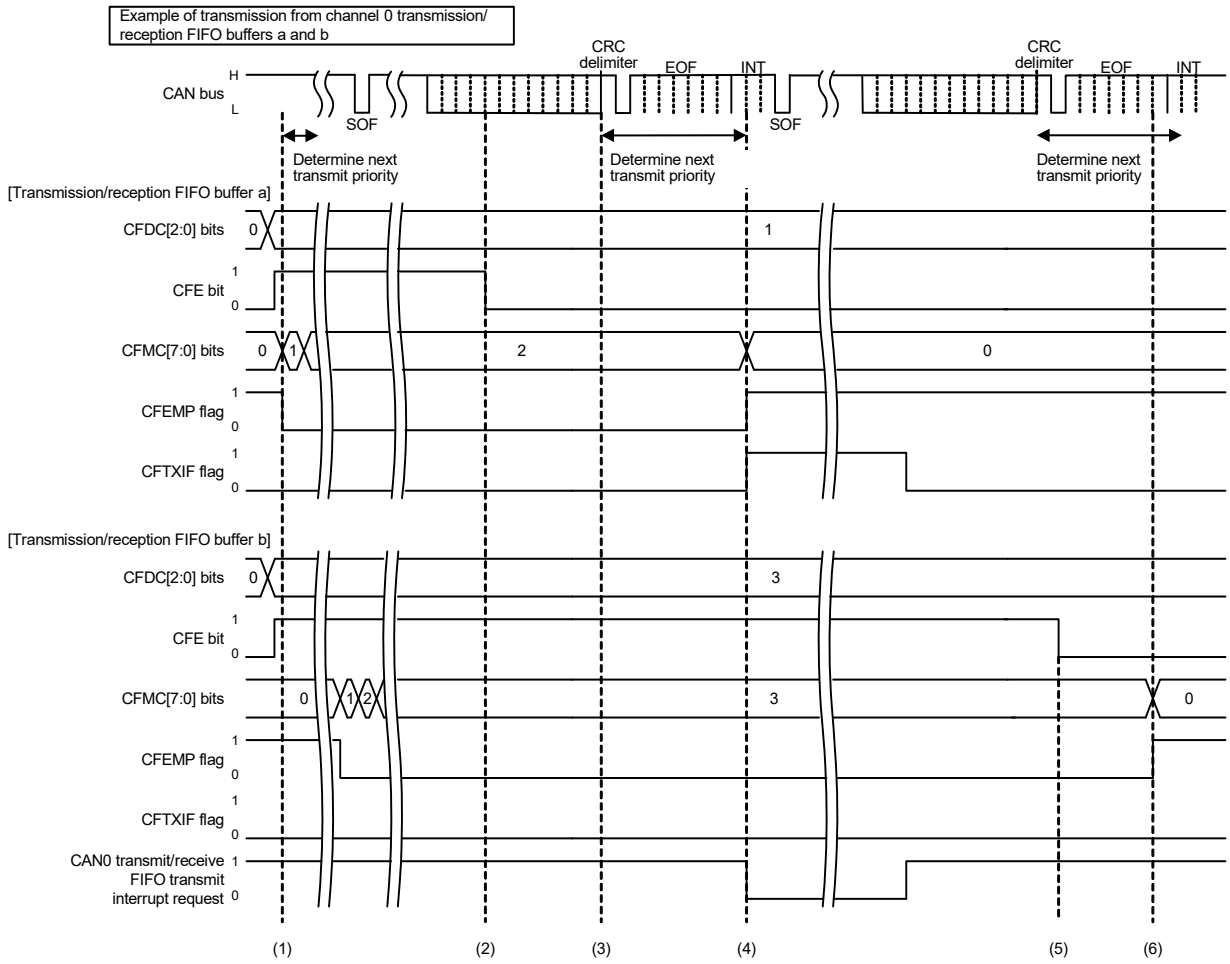
(2) When a transmission request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(3) When transmission completes successfully, the CFMC[7:0] value in the RSCAN0CFSTSa register is decremented. Setting the CFIM bit in the RSCAN0CFCCa register to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFTXIF flag in the RSCAN0CFSTSk register to 1 (a transmit/receive FIFO transmit interrupt request is present).

(4) The program can clear the CFTXIF flag.

(5) Message transmission from transmission/reception FIFO buffer b of channel 0 has been completed and the CFMC[7:0] value in the RSCAN0CFSTSb register is decremented. The CFMC[7:0] bits are cleared to 00h and therefore the CFEMP flag in the RSCAN0CFSTSk register is set to 1 (the transmission/reception FIFO buffer contains no message (buffer empty)).

Transmission is continued until the CFEMP flag is set to 1. It is possible to continuously store messages for transmission in FIFO buffers until the CFFLL flag in the RSCAN0CFSTSa and RSCAN0CFSTSb register is set to 1 (the transmission/reception FIFO buffer is full).



a = 0 to 5, b = 0 to 5
CFDC[2:0], CFE: Bits in the RSCAN0CFCCk register
CFMC[7:0], CFEMP, CFTXIF: Flags in the RSCAN0CFSTSk register

Figure 35.31 Transmission/Reception FIFO Buffer Transmission Timing Chart (Transmission Abort Completed)

(1) While the CAN bus is idle, when the CFE bit in the RSCAN0CFCCa register (a = 0 to 5) is 1 (transmission/reception FIFO buffers are used) and the CFDC[2:0] value in the RSCAN0CFCCa register is 001b (4 messages) or more and the CFMC[7:0] value in the RSCAN0CFSTSa register is 01h or more, the priority determination processing starts to determine the highest-priority message for transmission. When the highest-priority message for transmission has been determined, transmission of the message starts. In this figure, the message is transmitted from transmission/reception FIFO buffer a of channel 0.

(2) When transmission is in progress or it is determined that the transmission/reception FIFO buffer is used for the next transmission, message transmission is not aborted unless an error or arbitration loss occurs even if the CFE bit is set to 0 (no transmission/reception FIFO buffer is used).

(3) When a transmission request from a buffer is present, the priority determination starts with the CRC delimiter for the next transmission. In this figure, transmission/reception FIFO buffer b is not selected as a buffer for the next transmission. The determination time may delay if the transmit priority determination processing is performed on another channel. However, the delay does not occur during transmission because the determination processing is completed by the third bit of the intermission.

(4) When transmission completes successfully, the CFMC[7:0] value is cleared to 00h. Setting the CFIM bit to 1 (a FIFO transmit interrupt request is generated each time a message has been transmitted) sets the CFTXIF flag in the RSCAN0CFSTSa register to 1 (a transmit/receive FIFO transmit interrupt request is present). The program can clear the CFTXIF flag.

(5) If another CAN node on the CAN bus is transmitting data (not from transmission/reception FIFO buffer b), transmission/reception FIFO buffers cannot be disabled immediately even if the CFE bit in the RSCAN0CFCCb register is cleared to 0 (no transmission/reception FIFO buffer is used) during transmit priority determination. (The CFEMP flag in the RSCAN0CFSTSb register is not set to 1 (the transmission/reception FIFO buffer contains no message (buffer empty)) immediately.)

(6) After the internal processing time has passed, transmission/reception FIFO buffers are disabled and the CFMC[7:0] bits in the RSCAN0CFSTSb register are cleared to 00h and the CFEMP flag is set to 1. When the transmission/reception FIFO buffer is not transmitting data and is not selected as the next transmission buffer and priority determination is not in progress, the transmission/reception FIFO buffer is immediately disabled. (The CFMC[7:0] bits are cleared to 00h and the CFEMP flag is set to 1.)

35.9.3.3 Procedure for Transmission from the Transmission Queue

Figure 35.32 shows the procedure for transmission from the transmission queue.

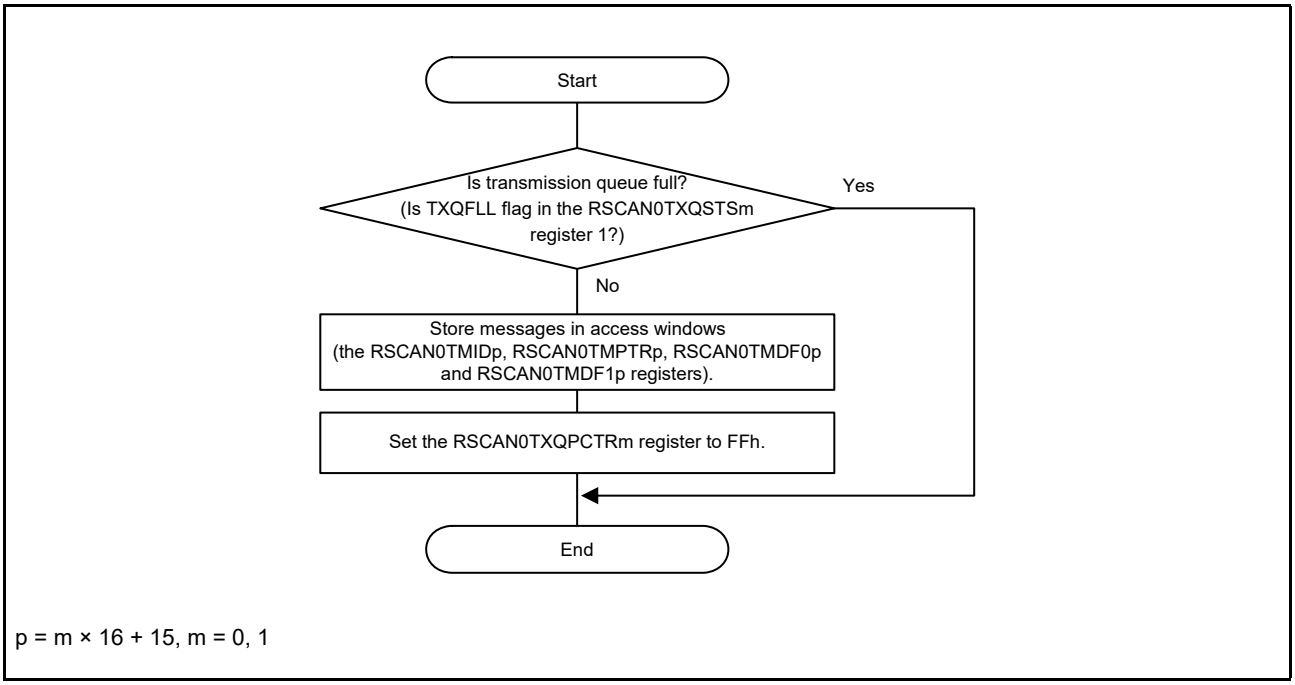


Figure 35.32 Procedure for Transmission from the Transmission Queue

35.9.3.4 Transmission History Buffer Reading Procedure

Transmission history data can be read from the RSCAN0THLACCm register. The next data can be accessed by writing FFh to the corresponding RSCAN0THLPCTRm register (m = 0, 1) after reading a set of data. Figure 35.33 shows the transmission history buffer reading procedure.

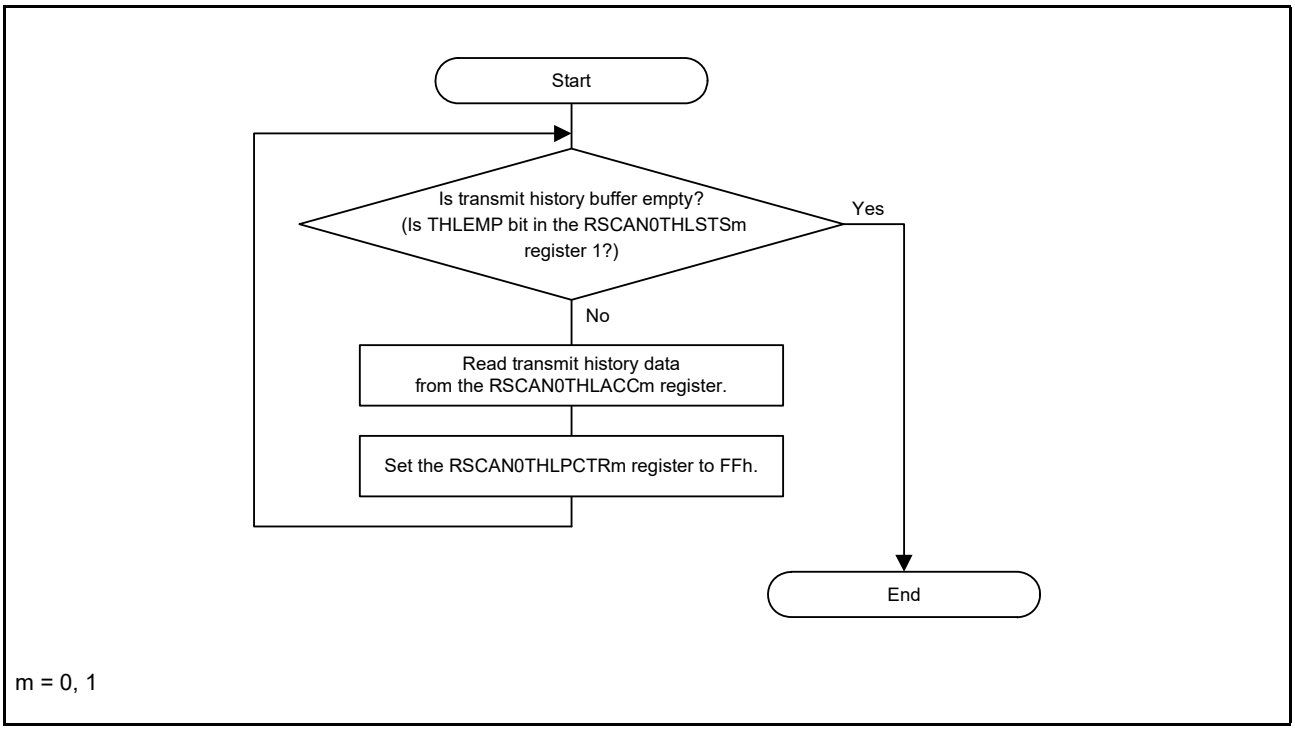


Figure 35.33 Transmission History Buffer Reading Procedure

35.9.4 Test Settings

35.9.4.1 Self-Test Mode Setting Procedure

Self-test mode allows communication test on a channel basis by enabling a CAN node to receive its own transmitted messages.

Figure 35.34 shows the self-test mode setting procedure.

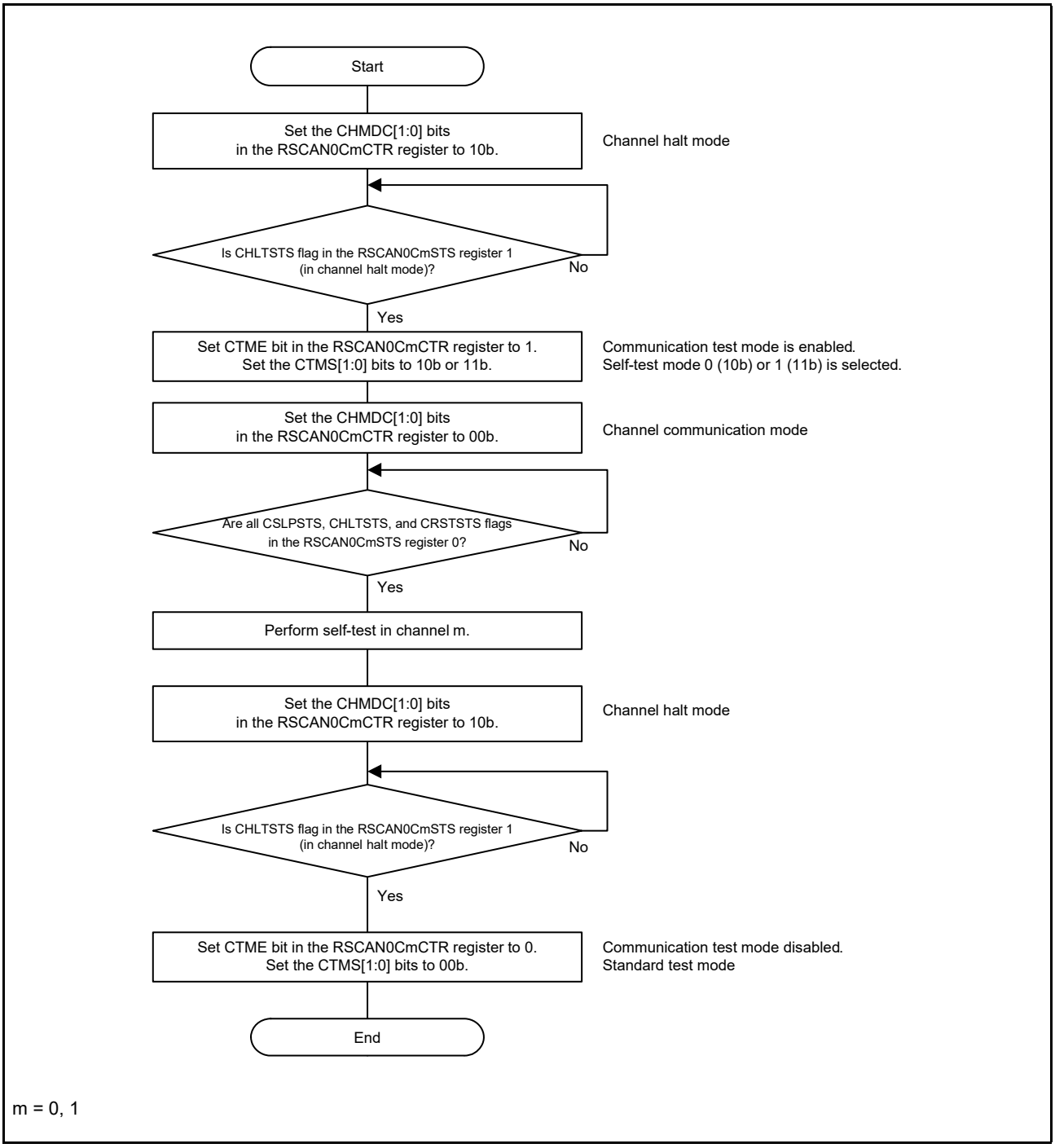


Figure 35.34 Self-Test Mode Setting Procedure

35.9.4.2 Procedure for Unlocking the Protection

Since the global test function in Table 35.24 is protected, write the protection unlock data 1 and unlock data 2 in succession to the LOCK[15:0] bits in the RSCAN0GLOCKK register, then set the target test bit to 1.

Table 35.24 Protection Unlock Data for Test Function

Test Function	Protection Unlock Data 1	Protection Unlock Data 2	Target Bit
RAM test	7575h	8A8Ah	RTME bit in the RSCAN0GTSTCTR register

If an incorrect value is written to the LOCK[15:0] bits, restart from writing the protection unlock data 1. Figure 35.35 shows the procedure for unlocking the protection.

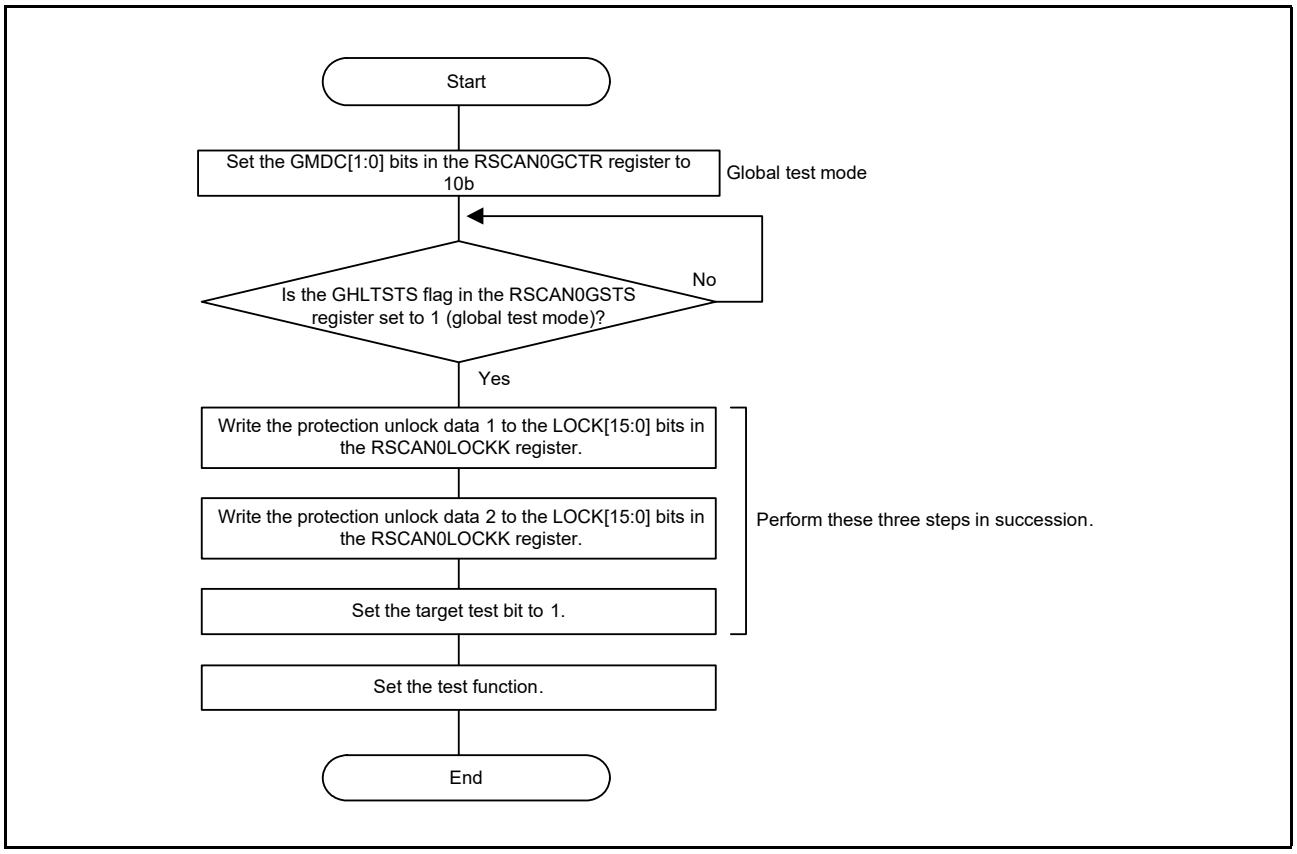


Figure 35.35 Protection Unlock Procedure

35.9.4.3 RAM Test Setting Procedure

RAM tests include CAN RAM read/write test. The read/write test verifies that data written to the RAM is read correctly. Before closing the RAM test, write 0000 0000h to all pages of the CAN RAM.
Figure 35.36 shows the RAM test setting procedure.

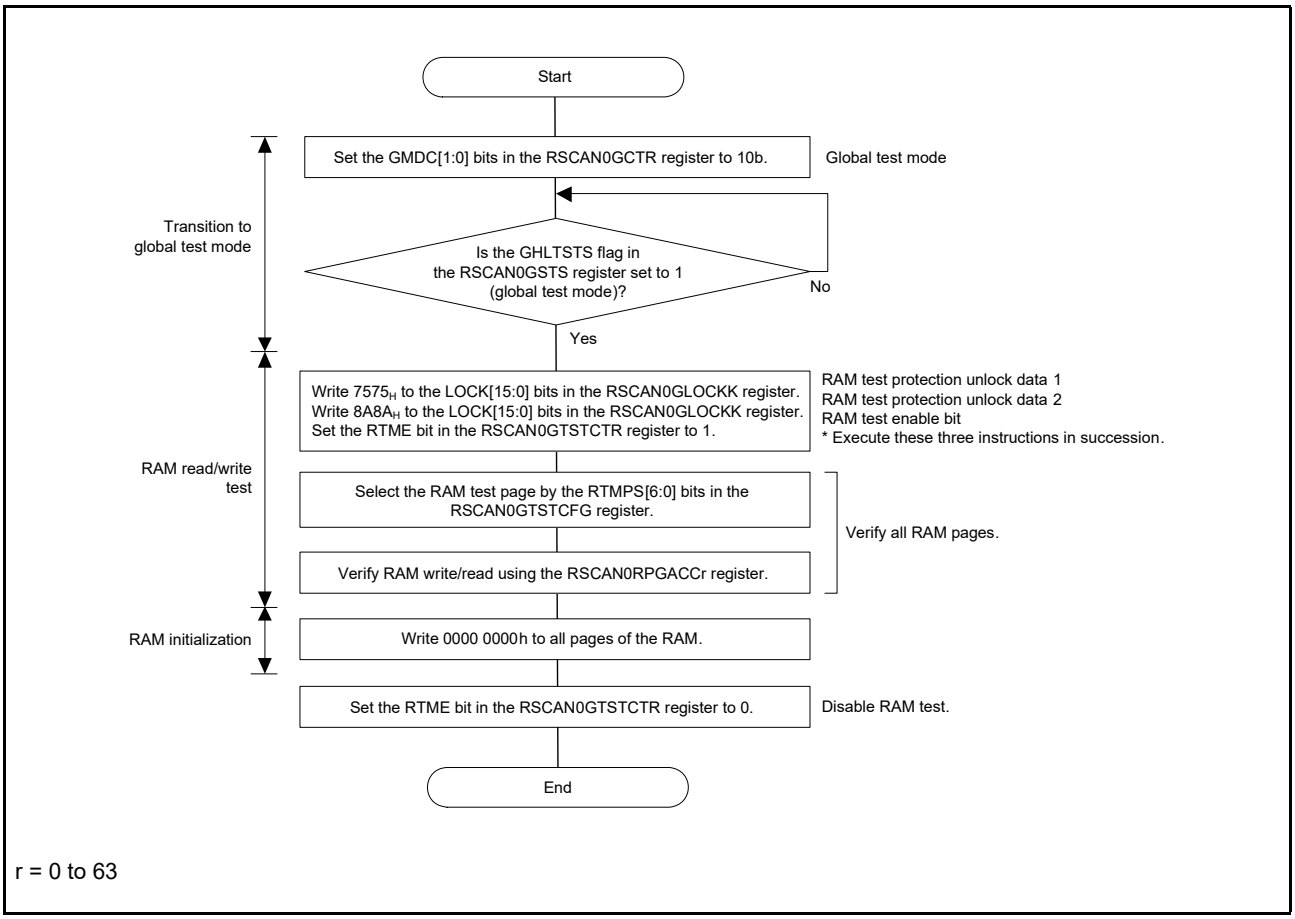


Figure 35.36 RAM Test Setting Procedure

35.9.4.4 Inter-Channel Communication Test Setting Procedure

Communication testing can be performed by transmitting and receiving data between different channels.
Figure 35.37 shows the inter-channel communication test setting procedure.

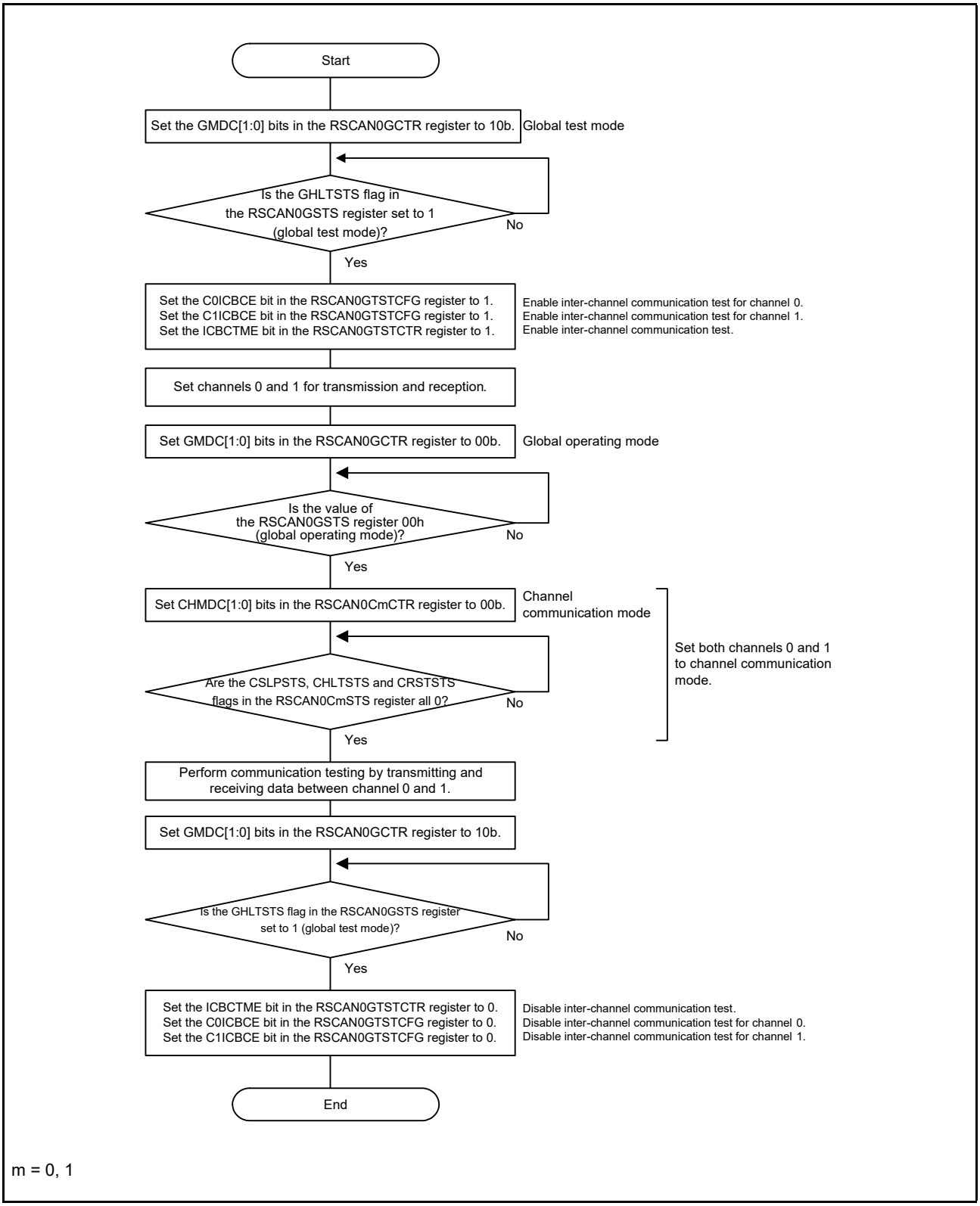


Figure 35.37 Inter-Channel Communication Test Setting Procedure (Example of Communication Test between Channel 0 and Channel 1)

35.10 Detection and Correction of Errors in RSCAN RAM

35.10.1 ECC for the RSCAN RAM

Each buffer RAM of the RSCAN has the following ECC functions.

- ECC error detection/correction
  The RAM is checked for ECC errors. The following options are selectable.
  - 2-bit error detection and 1-bit error detection/correction
  - 2-bit error detection and 1-bit error detection
  The ECC error detection/correction can be disabled by using through mode.
  With the initial settings, error detection/correction is enabled.
- Error notification
  When any of the following errors occurs, it is conveyed to the error control module (ECM).
  - 1-bit ECC error in the RSCAN RAM
  - 2-bit ECC error in the RSCAN RAM
  - RSCAN overflow error
  In the initial setting, 2-bit error notification is enabled. However, if an interrupt is masked by the FEINTFMSK register, interrupt processing does not proceed.
- Error status
  Detection of 2- and 1-bit ECC errors can be monitored.
  A bit for clearing the error status is provided.

Note: When ECC error detection/correction is performed, initialize the RSCAN RAM by the RSCAN module before it is used.

35.10.2 Output of Errors

The RSCAN outputs the following errors to the error control module (ECM) on detection of a 1-bit or 2-bit ECC error and on overflows of the ECCRCANEADz registers (z = 0 to 7), which hold the addresses where ECC errors were detected. For details, see section 42, Error Control Module (ECM).

- 1-bit ECC error in the RSCAN RAM
- 2-bit ECC error in the RSCAN RAM
- RSCAN overflow error

35.11 Notes on the RSCAN Module

- When changing a global mode, check the GSLPSTS, GHLTSTS, and GRSTSTS flags in the RSCAN0GSTS register for transitions. When changing a channel mode, check the CSLPSTS, CHLTSTS, and CRSTSTS flags in the RSCAN0CmSTS register (m = 0, 1) for transitions.
- The acceptance filter processing checks reception rules sequentially in ascending order from the minimum rule number. If the same ID, IDE bit, or RTR bit value is set for multiple reception rules, the minimum number of reception rule is used for the acceptance filter processing. If the message does not pass through the subsequent DLC filter processing, the data processing is terminated without returning to the acceptance filter processing and the message is not stored in the buffer.
- When linking transmission buffers to transmission/reception FIFO buffers or allocating transmission buffers to transmission queues, set the control register (RSCAN0TMCp) of the corresponding transmission buffer to 00h. The status register (RSCAN0TMSTSp) of the corresponding transmission buffer should not be used. Flags in other status registers (registers RSCAN0TMTRSTS0 to RSCAN0TMTRSTS2, RSCAN0TMTARSTS0 to RSCAN0TMTARSTS2, RSCAN0TMTCSTS0 to RSCAN0TMTCSTS2, and RSCAN0TMTASTS0 to RSCAN0TMTASTS2), which correspond to transmission buffers linked to transmission/reception FIFO buffers or allocated to transmission queues remain unchanged. Set the enable bit in the corresponding interrupt enable register (registers RSCAN0TMIEC0 to RSCAN0TMIEC2) to 0 (transmission buffer interrupt is disabled).
- Transmission buffers that are linked to transmission/reception FIFO buffers must not bet allocated to transmission queues.
- Only a single transmission/reception FIFO buffer can be linked to a transmission buffer. Do not link two or more transmission/reception FIFO buffers to transmission buffers of the same number.
- When the CANm bit time clock is selected as a timestamp counter clock source, the timestamp counter stops when the corresponding channel has transitioned to channel reset mode or channel halt mode.
- In case of an attempt to store a new received message when the reception FIFO buffer and the transmission/reception FIFO buffer are full, the new message is discarded. If you wish to store a new message for transmission in the transmission/reception FIFO buffer or the transmission queue, check that the transmission/reception FIFO buffer or the transmission queue is not full.
- The values of unused reception buffers (RSCAN0RMIDq, RSCAN0RMPTRq, RSCAN0RMDF0q, and RSCAN0RMDF1q registers), reception FIFO buffer access registers (RSCAN0RFIDx, RSCAN0RFPTRx, RSCAN0RFDF0x, and RSCAN0RFDF1x registers), and transmission/reception FIFO buffer access registers (RSCAN0CFIDk, RSCAN0CFPTRk, RSCAN0CFDF0k, and RSCAN0CFDF1k registers) are undefined when the RSCAN module transitions to global operation mode or global test mode after exiting from global reset mode.

36. Serial Peripheral Interface (RSPIa)

36.1 Overview

This LSI includes four channels of serial peripheral interface (RSPI).
The RSPI channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices.
Table 36.1 lists the specifications of the RSPI, and Figure 36.1 shows a block diagram of the RSPI.
In this section, a lower-case letter m in RSPI command register m (SPCMDm) indicates a value from 0 to 7.

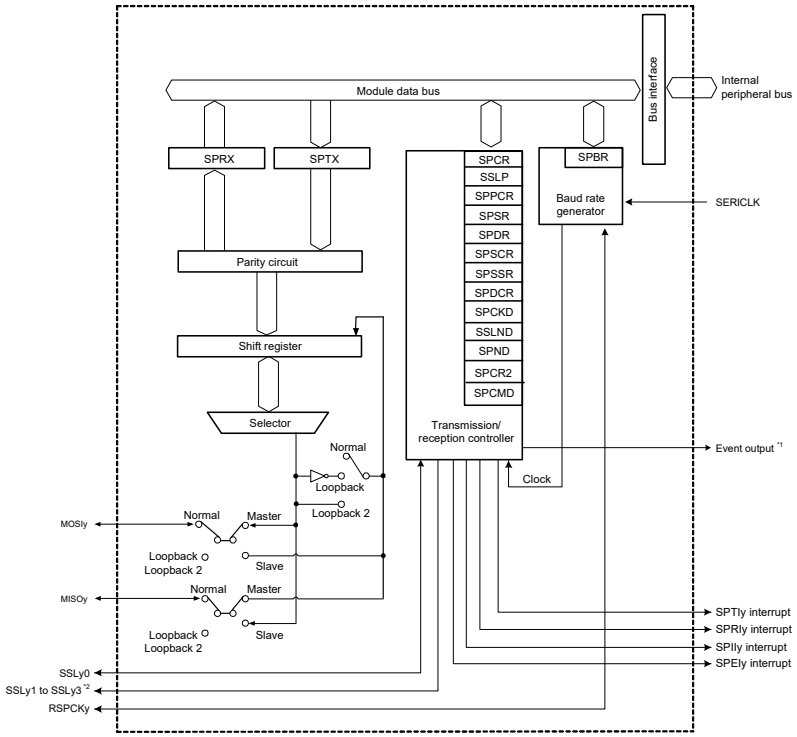
Table 36.1 RSPI Specifications (1 / 2)

Item	Description
Number of channels	Four channels
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (four-wire method) or clock synchronous operation (three-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmission/reception buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing SERICLK (the division ratio ranges from divided by 4 to divided by 4096). • In slave mode, the minimum SERICLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of SERICLK divided by 8). Width at high level: 4 cycles of SERICLK; width at low level: 4 cycles of SERICLK
Buffer configuration	• Double buffer configuration for the transmission/reception buffers • 128 bits for the transmission/reception buffers
Error detection	• Mode fault error detection • Overrun error detection*1 • Parity error detection
SSL control function	• Four SSL pins for channel 0 (SSL00 to SSL03), two SSL pins for channel 1 (SSL10, SSL11), and one SSL pin for each of channels 2 and 3 (SSL20, SSL30) • In single-master mode, SSL00 to SSL03, SSL10, SSL11, SSL20, and SSL30 pins are output. • In multi-master mode: SSL00, SSL10, SSL20, and SSL30 pins for input, and SSL01 to SSL03 and SSL11 pins for either output or unused. • In slave mode: SSL00, SSL10, SSL20, and SSL30 pins for input, and SSL01 to SSL03 and SSL11 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmission buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Table 36.1 RSPI Specifications (2 / 2)

Item	Description
Interrupt sources	• Interrupt sources Reception buffer full interrupt Transmission buffer empty interrupt RSPI error interrupt (mode fault, overrun, parity error) RSPI idle interrupt (RSPI idle)
Event link function*2 (output)	• The following events can be output to the event link controller. Reception buffer full signal Transmission buffer empty signal Mode fault, overrun, or parity error signal RSPI idle signal Transmission-completed signal
Others	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low-power consumption function	Module-stop state can be set.

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped at the timing of overrun error detection.
Note 2. Only for channel 0 (RSPI0)



SPCR:	RSPI control register	SPDCR:	RSPI data control register
SPCR2:	RSPI control register 2	SPCKD:	RSPI clock delay register
SSLP:	RSPI slave select polarity register	SSLND:	RSPI slave select negation delay register
SPPCR:	RSPI pin control register	SPND:	RSPI next-access delay register
SPSR:	RSPI status register	SPCMD:	RSPI command registers 0 to 7 (eight registers)
SPDR:	RSPI data register		
SPSCR:	RSPI sequence control register	SPBR:	RSPI bit rate register
SPSSR:	RSPI sequence status register	SPTX:	RSPI transmission buffer
		SPRX:	RSPI reception buffer

Note 1. Only for channel 0.
Note 2. The number of pins differs for each channel (SSL01 to SSL03 for channel 0; SSL11 for channel 1).
y = 0, 1, 2, 3 (for all channels)

Figure 36.1 RSPI Block Diagram

Table 36.2 lists the I/O pins used in the RSPI.
The RSPI automatically switches the I/O direction of the SSLy0 pin. SSLy0 is set as an output when the RSPI is a single master and as an input when the RSPI is a multi-master or a slave. Pins RSPCKy, MOSIy, and MISOy are automatically set as inputs or outputs according to the setting of master or slave and the level input on the SSLy0 pin.
Refer to section 36.3.2, Controlling RSPI Pins.

Table 36.2 RSPI Pin Configuration

Channel	Pin Name	I/O	Function
RSPI0	RSPCK0	I/O	Clock I/O
	MOSI0	I/O	Master transmit data I/O
	MISO0	I/O	Slave transmit data I/O
	SSL00	I/O	Slave selection signal I/O
	SSL01	Output	Slave selection signal output
	SSL02	Output	Slave selection signal output
	SSL03	Output	Slave selection signal output
RSPI1	RSPCK1	I/O	Clock I/O
	MOSI1	I/O	Master transmit data I/O
	MISO1	I/O	Slave transmit data I/O
	SSL10	I/O	Slave selection signal I/O
	SSL11	Output	Slave selection signal output
RSPI2	RSPCK2	I/O	Clock I/O
	MOSI2	I/O	Master transmit data I/O
	MISO2	I/O	Slave transmit data I/O
	SSL20	I/O	Slave selection signal I/O
RSPI3	RSPCK3	I/O	Clock I/O
	MOSI3	I/O	Master transmit data I/O
	MISO3	I/O	Slave transmit data I/O
	SSL30	I/O	Slave selection signal I/O

Note: The number of SSL pins differs from channel to channel. The indices to identify the channels are from 0 to 3.

36.2 Register Descriptions

36.2.1 RSPI Control Register (SPCR)

The SPCR register controls the settings for operation of the RSPI.
The SPCR.MSTR, SPCR.MODFEN, and SPCR.TXMD bits should be set while the setting of the SPCR.SPE bit is 0. Writing to these bits is prohibited while the setting of the SPCR.SPE bit is 1.

Address(es): RSPI0.SPCR A006 8000h, RSPI1.SPCR A006 8400h, RSPI2.SPCR A006 8800h, RSPI3.SPCR A006 8C00h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODFEN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPMS	RSPI Mode Select	0: SPI operation (four-wire method) 1: Clock synchronous operation (three-wire method)	R/W
b1	TXMD	Communications Operating Mode Select	0: Full-duplex synchronous serial communications 1: Serial communications consisting of only transmit operations	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disables the detection of mode fault error 1: Enables the detection of mode fault error	R/W
b3	MSTR	Master/Slave Mode Select	0: Slave mode 1: Master mode	R/W
b4	SPEIE	Error Interrupt Enable	0: Disables the generation of error interrupt requests 1: Enables the generation of error interrupt requests	R/W
b5	SPTIE	Transmission Buffer Empty Interrupt Enable	0: Disables the generation of transmission buffer empty interrupt requests 1: Enables the generation of transmission buffer empty interrupt requests	R/W
b6	SPE	RSPI Function Enable	0: Disables the RSPI function 1: Enables the RSPI function	R/W
b7	SPRIE	Reception Buffer Full Interrupt Enable	0: Disables the generation of reception buffer full interrupt requests 1: Enables the generation of reception buffer full interrupt requests	R/W

SPMS Bit (RSPI Mode Select)

The SPMS bit selects SPI operation (four-wire method) or clock synchronous operation (three-wire method).
The SSLy0 to SSLy3 pins are not used in clock synchronous operation. The three pins RSPCKy, MOSIy, and MISOy handle communications. If clock synchronous operation is to proceed in master mode (SPCR.MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. Set the CPHA bit to 1 if clock synchronous operation is to proceed in slave mode (SPCR.MSTR = 0). Do not set the CPHA bit to 0 when clock synchronous operation is to proceed in slave mode (SPCR.MSTR = 0). (y = 0, 1, 2, 3)

TXMD Bit (Communications Operating Mode Select)

The TXMD bit selects the operation for full-duplex synchronous serial communications or the operation for transmission only.
When performing communications with the TXMD bit set to 1, the RSPI performs only transmit operations and not receive operations (refer to section 36.3.6, Communications Operating Mode).
When the TXMD bit is set to 1, reception buffer full interrupt requests cannot be used.

MODFEN Bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault error (refer to section 36.3.8, Error Detection). In addition, the RSPI determines the I/O direction of the SSLy0 to SSLy3 (y = 0, 1, 2, 3) pins based on combinations of the MODFEN and MSTR bits (refer to section 36.3.2, Controlling RSPI Pins).

MSTR Bit (RSPI Master/Slave Mode Select)

The MSTR bit selects master/slave mode of the RSPI. According to MSTR bit settings, the RSPI determines the direction of pins RSPCKy, MOSIy, and MISOy, and SSLy0 to SSLy3 (y = 0, 1, 2, 3).

SPEIE Bit (RSPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of RSPI error interrupt requests when the RSPI detects a mode fault error and sets the SPSR.MODF flag to 1, when the RSPI detects an overrun error and sets the SPSR.OVRF flag to 1, or when the RSPI detects a parity error and sets the SPSR.PERF flag to 1 (refer to section 36.3.8, Error Detection).

SPTIE Bit (Transmission Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables a transmission buffer empty interrupt request generated when the RSPI detects that the transmission buffer is empty.
If the RSPI function is disabled (i.e. the SPE bit is set to 0), the transmission buffer being empty is detected. If the SPTIE bit is set to 1 at this time, a transmission buffer empty interrupt is generated.
Note that a transfer buffer empty interrupt request is also generated when the SPTIE and SPE bits are set to 1 at the same time at the start of transmission.

SPE Bit (RSPI Function Enable)

The SPE bit enables or disables the RSPI function.
When the SPSR.MODF bit is 1, the SPE bit cannot be set to 1. For details, refer to section 36.3.8, Error Detection.
Setting the SPE bit to 0 disables the RSPI function, and initializes a part of the module function. For details, refer to section 36.3.9, Initializing RSPI. Furthermore, when the setting of the SPTIE bit is 1 (enabling the generation of transmission buffer empty interrupts), a transmission buffer empty interrupt request is generated by the state of the SPE bit changing from 0 to 1 or from 1 to 0.

SPRIE Bit (RSPI Reception Buffer Full Interrupt Enable)

The SPRIE bit enables or disables RSPI reception buffer full interrupt requests when the RSPI has detected the reception buffer being full after the completion of a serial transfer.

36.2.2 RSPI Slave Select Polarity Register (SSLP)

The SSLP register controls the active sense of the RSPIy (y = 0, 1, 2, 3) slave select signals.
The SSLP register should be set while the setting of the SPCR.SPE bit is 0. Writing to this register is prohibited while the setting of the SPCR.SPE bit is 1.

Address(es): RSPI0.SSLP A006 8001h, RSPI1.SSLP A006 8401h, RSPI2.SSLP A006 8801h, RSPI3.SSLP A006 8C01h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: SSLy0 signal is active low 1: SSLy0 signal is active high	R/W
b1	SSL1P	SSL1 Signal Polarity Setting*1	0: SSLy1 signal is active low 1: SSLy1 signal is active high	R/W
b2	SSL2P	SSL2 Signal Polarity Setting*2	0: SSLy2 signal is active low 1: SSLy2 signal is active high	R/W
b3	SSL3P	SSL3 Signal Polarity Setting*2	0: SSLy3 signal is active low 1: SSLy3 signal is active high	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Bits for channels 2 and 3 are reserved. These bits are read as 0. The write value should be 0.
Note 2. Bits for channels 1, 2, and 3 are reserved. These bits are read as 0. The write value should be 0.

36.2.3 RSPI Pin Control Register (SPPCR)

The SPPCR register controls the output setting for RSPI output pins.

The SPPCR register should be set while the setting of the SPCR.SPE bit is 0. Writing to this register is prohibited while the setting of the SPCR.SPE bit is 1.

Address(es): RSPI0.SPPCR A006 8002h, RSPI1.SPPCR A006 8402h, RSPI2.SPPCR A006 8802h, RSPI3.SPPCR A006 8C02h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	SPOM	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPLP	RSPI Loopback	0: Normal mode 1: Loopback mode (data is inverted for transmission)	R/W
b1	SPLP2	RSPI Loopback 2	0: Normal mode 1: Loopback mode (data is not inverted for transmission)	R/W
b2	SPOM	Output Pin Mode	0: CMOS output 1: Open-drain output	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: The level output on the MOSIy pin during MOSI idling corresponds to low. 1: The level output on the MOSIy pin during MOSI idling corresponds to high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: MOSI output value equals final data from previous transfer 1: MOSI output value equals the value set in the MOIFV bit	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPLP Bit (RSPI Loopback)

The SPLP bit selects the mode of the RSPI pins.

When the SPLP bit is set to 1, the RSPI shuts off the path between the MISOy pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIy pin and the shift register if the SPCR.MSTR bit is 0, and connects (inverts) the input path and output path for the shift register (loopback mode).

(y = 0, 1, 2, 3)

SPLP2 Bit (RSPI Loopback 2)

The SPLP2 bit selects the mode of the RSPI pins.

When the SPLP2 bit is set to 1, the RSPI shuts off the path between the MISOy pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIy pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path for the shift register (loopback mode).

(y = 0, 1, 2, 3)

SPOM Bit (Output Pin Mode)

The SPOM bit is used to set the RSPI output pins to CMOS output or open-drain output. For details, see section 36.3.2, Controlling RSPI Pins.

MOIFV Bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIy pin output value as low or high during the SSL negation period (including the SSL retention period during a burst transfer).

MOIFE Bit (MOSI Idle Value Fixing Enable)

The MOIFE bit selects whether the MOSIy output level is to be fixed over the SSL negation period (including the SSL retention period during a burst transfer) when the RSPI is in master mode. When the MOIFE bit is 0, the RSPI continues to output the value of the last bit from the previous serial transfer during the SSL negation period to the MOSIy pin. When the MOIFE bit is 1, the RSPI outputs a fixed low or high level on the MOSIy pin according to the setting of the MOIFV bit.
(y = 0, 1, 2, 3)

36.2.4 RSPI Status Register (SPSR)

The SPSR register indicates the state of RSPI transfer.

Address(es): RSPI0.SPSR A006 8003h, RSPI1.SPSR A006 8403h, RSPI2.SPSR A006 8803h, RSPI3.SPSR A006 8C03h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	PERF	MODF	IDLNF	OVRF
Value after reset:	x	0	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurs 1: An overrun error occurs	R/(W) *1
b1	IDLNF	RSPI Idle Flag	0: RSPI is in the idle state 1: RSPI is in the transfer state	R
b2	MODF	Mode Fault Error Flag	0: No mode fault error occurs 1: A mode fault error occurs	R/(W) *1
b3	PERF	Parity Error Flag	0: No parity error occurs 1: A parity error occurs	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/(W)
b5	—	Reserved	The read value is undefined. The write value should be 1.	R/(W)
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/(W)
b7	—	Reserved	The read value is undefined. The write value should be 1.	R/(W)

Note 1. Only 0 can be written to clear the flag after reading 1.

OVRF Flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (when the SPCR.MSTR bit is 1) and when the RSPCK clock auto-stop function is enabled (the SPCR1.SCKASE bit is 1), an overrun error does not occur; accordingly this flag does not become 1. For details, see section 36.3.8.1, Overrun Error.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the reception buffer is full.

[Clearing condition]

- When SPSR is read while the OVRF flag is 1, and then writes the value 0 to the OVRF flag.

IDLNF Flag (RSPI Idle Flag)

The IDLNF flag indicates the transfer status of the RSPI.
[Setting condition]
Master mode

- Condition 1 and condition 2 are not satisfied in master mode under the [Clearing condition] below.

Slave mode

- The SPCR.SPE bit is 1 (RSPI function is enabled)

[Clearing condition]
Master mode
The following 1 is satisfied (condition 1) or all of the following 2 to 4 are satisfied (condition 2).

1. The SPCR.SPE bit is 0 (RSPI is initialized)
2. The transmission buffer (SPTX) is empty (data for the next transfer is not set)
3. The SPSSR.SPCP[2:0] bits are 000b (beginning of sequence control)
4. The RSPI internal sequencer has entered the idle state (status in which operations up to the next-access delay have finished)

Slave mode

- The SPCR.SPE bit is 0 (RSPI is initialized)

MODF Flag (Mode Fault Error Flag)

Indicates the occurrence of a mode fault error.
[Setting condition]
Multi-master mode

- When the input level of the SSLyi pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error

Slave mode

- When the SSLyi pin is negated before the RSPCK cycle necessary for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled), the RSPI detects a mode fault error

The active level of the SSLyi signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting bit).
(y = 0, 1, 2, 3 (for all channels); i = 0 to 3)
[Clearing condition]

- When SPSR is read while the MODF flag is 1, and then writes the value 0 to the MODF flag

PERF Flag (Parity Error Flag)

Indicates the occurrence of a parity error.
[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1, the RSPI detects a parity error

[Clearing condition]

- When SPSR is read while the PERF flag is 1, and then writes the value 0 to the PERF flag

36.2.5 RSPI Data Register (SPDR)

SPDR is the interface with the buffers that hold data for transmission and reception by the RSPI.
When accessing in longwords (the SPLW bit is 1), access SPDR.
When accessing in words (the SPLW bit is 0), access the higher-order 16 bits (H) of SPDR.

Address(es): RSPI0.SPDR A006 8004h, RSPI1.SPDR A006 8404h, RSPI2.SPDR A006 8804h, RSPI3.SPDR A006 8C04h

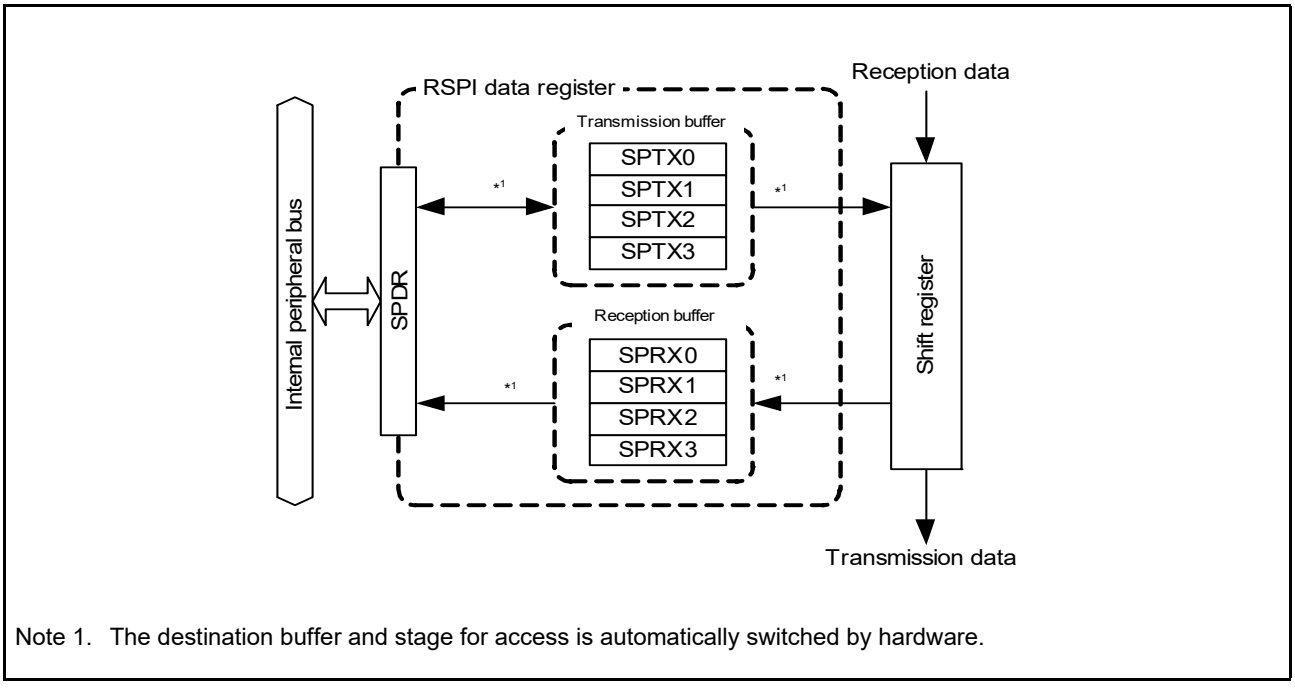
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): RSPI0.SPDR A006 8004h, RSPI1.SPDR A006 8404h, RSPI2.SPDR A006 8804h, RSPI3.SPDR A006 8C04h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	H															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The transmission buffer (SPTX) and reception buffer (SPRX) are independent but are both mapped to SPDR. Figure 36.2 shows the configuration of SPDR.



Note 1. The destination buffer and stage for access is automatically switched by hardware.

Figure 36.2 Configuration of SPDR

The transmit and reception buffers each have four stages. The number of stages to be used is selectable by the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]). The eight stages of the buffer are all mapped to the single address of SPDR.
Data written to SPDR are written to a transmission-buffer stage (SPTXn) (n = 0 to 3) and then transmitted from the buffer. The reception buffer holds received data on completion of reception. The reception buffer is not updated if an overrun is generated.
Furthermore, if the data length is other than 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the corresponding bits in SPRXn (n = 0 to 3). For example, if the data length is 9 bits, received data are stored in the SPRXn[8:0] bits and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus Interface

SPDR is the interface with 32-bit wide transmit and reception buffers, each of which has four stages, for a total of 32 bytes. In other words, the 32 bytes are mapped to the 4-byte address space for SPDR. Furthermore, the unit of access for SPDR is selected by the RSPI longword access/word access specification bit in the RSPI data control register (SPDCR.SPLW).
Data for transmission should be flush with the LSB end of the register. Received data are stored flush with the LSB end.
Operations involved in writing to and reading from SPDR are described below.

(a) Writing

Data written to SPDR are written to a transmission buffer (SPTXn). This is not influenced by the value of the SPDCR.SPRDTD bit unlike when reading from SPDR.
The transmission buffer includes a transmission buffer write pointer which is automatically updated to indicate the next stage each time data are written to SPDR.
Figure 36.3 shows the configuration of the bus interface with the transmission buffer in the case of writing to SPDR.

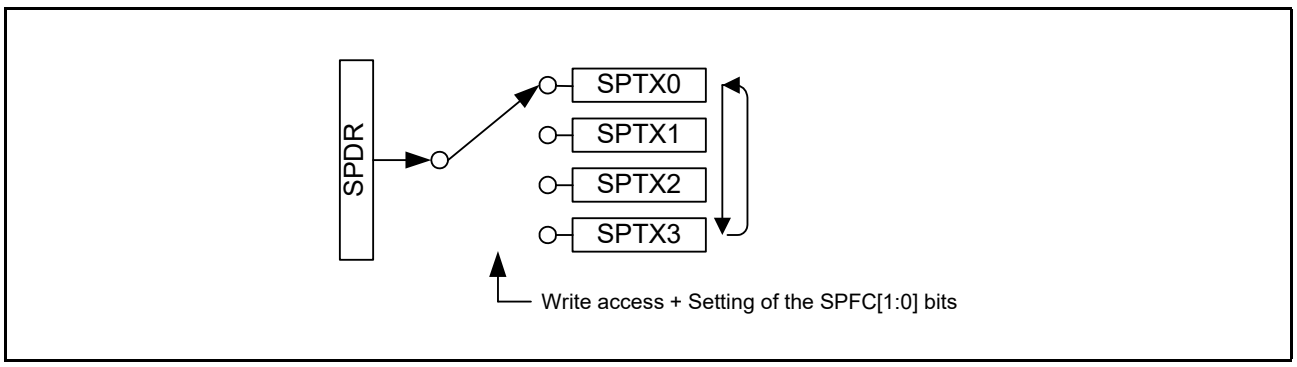


Figure 36.3 Configuration of SPDR (Writing)

The sequence for switching the transmission buffer write pointer differs with the setting of the number of frames specification bits in the RSPI data control register (SPDCR.SPFC[1:0]).

- Settings of the SPFC[1:0] bits and sequence of switching the pointer among SPTX0 to SPTX3.
  When the SPFC[1:0] bits are 00b: SPTX0 → SPTX0 → SPTX0 → …
  When the SPFC[1:0] bits are 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
  When the SPFC[1:0] bits are 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the RSPI function enable bit in the RSPI control register (SPCR.SPE) while the bit's current value is 0, SPTX0 will be the destination the next time writing proceeds.
When writing to the transmission buffer (SPTXn) after generation of the transmission buffer empty interrupt, write the number of frames set by the number of frames specification bits (SPFC[1:0]) in the RSPI data control register (SPDCR). Even if the number of frames is written to the transmission buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before generation of the next transmission buffer empty interrupt.

(b) Reading

SPDR can be read to read the value of a reception buffer (SPRXn) or a transmission buffer (SPTXn). The setting of the RSPI receive/transmit data selection bit in the RSPI data control register (SPDCR.SPRDTD) selects whether reading is of the receive or transmission buffer.
The sequence of reading the SPDR register is controlled by independent pointers, reception buffer read pointer and transmission buffer read pointer.
Figure 36.4 shows the configuration of the bus interface with the receive and transmission buffers in the case of reading from SPDR.

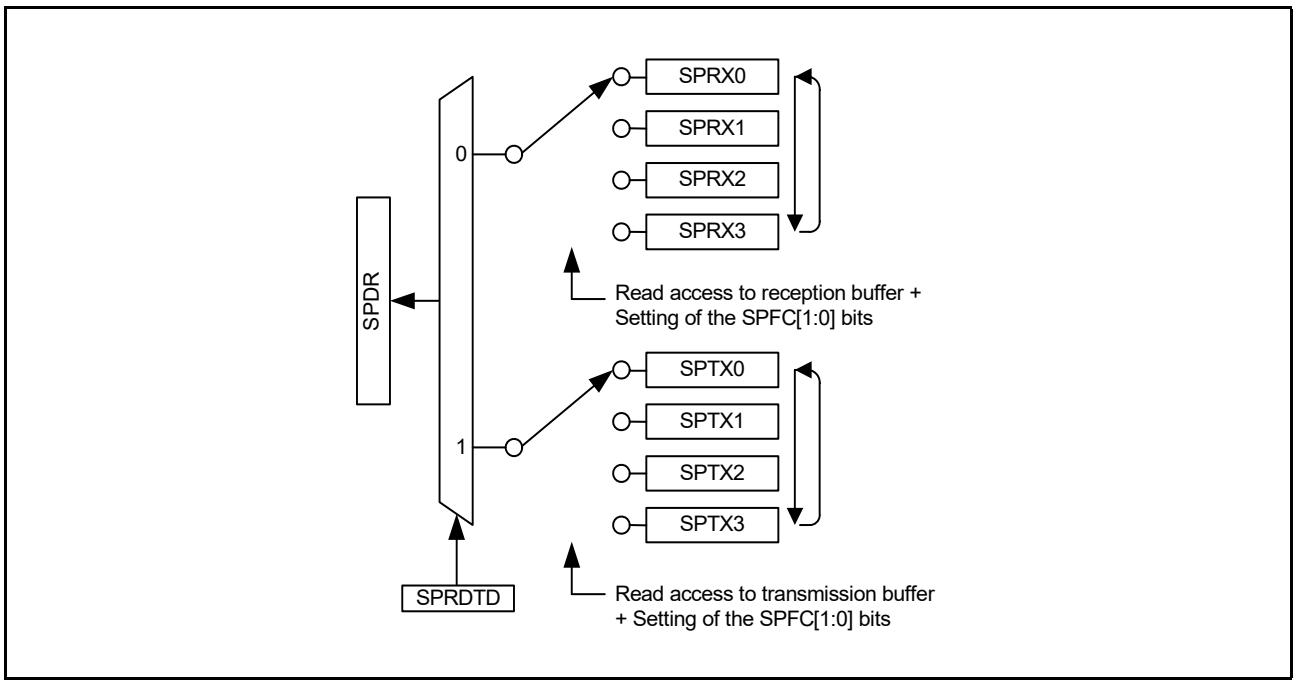


Figure 36.4 Configuration of SPDR (Reading)

Reading the reception buffer switches the reception buffer read pointer to the next buffer automatically.
The sequence of switching the reception buffer read pointer is the same as that for the transmission buffer write pointer. However, when 1 is written to the RSRI function enable bit in the RSPI control register (SPCR.SPE) while the bit's current value is 1, SPRX0 will be indicated by the buffer read pointer the next time reading proceeds.
The transmission buffer read pointer is updated when writing to SPDR, and not updated when reading from the transmission buffer. When reading from the transmission buffer, the value most recently written to SPDR is read. However, after generation of the transmission buffer empty interrupt, the values read from the transmission buffer are all 0 in the interval after completion of writing the number of frames of data specified in the number of frames specification bits (SPDCR.SPFC[1:0]) and before generation of the next buffer empty interrupt.

36.2.6 RSPI Sequence Control Register (SPSCR)

SPSCR sets the sequence length when the RSPI operates in master mode. When changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, the bits should be changed while the SPSR.IDLNF flag is 0.

Address(es): RSPI0.SPSCR A006 8008h, RSPI1.SPSCR A006 8408h, RSPI2.SPSCR A006 8808h, RSPI3.SPSCR A006 8C08h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPSLN[2:0]	RSPI Sequence Length Specification	b2 b1 b0: Sequence Length — Referenced SPCMD0 to SPCMD7 (No.) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… The order in which the SPCMD0 to SPCMD07 registers are to be referenced is changed in accordance with the sequence length that is set in these bits. The relationship among the setting of these bits, sequence length, and SPCMD0 to SPCMD7 registers referenced by the RSPI is shown above. However, the RSPI in slave mode always references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPSLN[2:0] Bits (RSPI Sequence Length Specification)

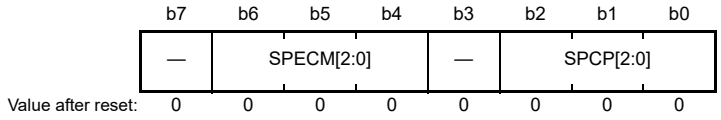
The SPSLN[2:0] bits specify a sequence length when the RSPI in master mode performs sequential operations. The RSPI in master mode changes SPCMD0 to SPCMD7 registers to be referenced and the order in which they are referenced according to the sequence length that is set in the SPSLN[2:0] bits.

In slave mode, SPCMD0 is always referred to.

36.2.7 RSPI Sequence Status Register (SPSSR)

SPSSR indicates the sequence control status when the RSPI operates in master mode.
Any writing to SPSSR is ignored.

Address(es): RSPI0.SPSSR A006 8009h, RSPI1.SPSSR A006 8409h, RSPI2.SPSSR A006 8809h, RSPI3.SPSSR A006 8C09h



Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPCP[2:0]	RSPI Command Pointer	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b3	—	Reserved	This bit is read as 0.	R
b6 to b4	SPECM[2:0]	RSPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7	R
b7	—	Reserved	This bit is read as 0.	R

SPCP[2:0] Bits (RSPI Command Pointer)

The SPCP[2:0] bits indicate SPCMDm that is currently pointed to by the pointer during sequence control by the RSPI. For the RSPI's sequence control, refer to section 36.3.10.1, Master Mode Operation.

SPECM[2:0] Bits (RSPI Error Command)

The SPECM[2:0] bits indicate SPCMDm that is specified by the SPCP[2:0] bits when an error is detected during sequence control by the RSPI. The RSPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF bits are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning. For the RSPI's error detection function, refer to section 36.3.8, Error Detection. For the RSPI's sequence control, refer to section 36.3.10.1, Master Mode Operation.

36.2.8 RSPI Bit Rate Register (SPBR)

SPBR controls the bit rate settings in master mode. Writing to SPBR is prohibited while both the SPCR.MSTR and SPCR.SPE bits are 1.

Address(es): RSPI0.SPBR A006 800Ah, RSPI1.SPBR A006 840Ah, RSPI2.SPBR A006 880Ah, RSPI3.SPBR A006 8C0Ah



When the RSPI is used in slave mode, the bit rate depends on the bit rate of the input clock (bit rate satisfying the electrical characteristics should be used) regardless of the settings of SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting bits).
The bit rate is determined by combinations of the SPBR setting and the SPCMDm.BRDV[1:0] bit setting. The equation for calculating the bit rate is given below. In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] bit setting (0, 1, 2, 3) (m = 0 to 7). However, setting n = 0 (SPR[7:0] = 0) and N = 0 (BRDV[1:0] = 0) is prohibited.

$$\text{Bit rate} = \frac{f\,(\text{SERICLK})}{2 \times (n + 1)\, 2^{N}}$$

Table 36.3 lists examples of the relationship among the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 36.3 Relationship among SPBR Settings, BRDV[1:0] Settings, and Bit Rates

			Bit Rate	
SPBR (n)	**BRDV[1:0] Bits (N)**	**Division Ratio**	**SERICLK = 120 MHz**	**SERICLK = 150 MHz**
0	0	2	Setting prohibited	Setting prohibited
1	0	4	30.0 Mbps	37.5 Mbps
2	0	6	20.0 Mbps	25.0 Mbps
3	0	8	15.0 Mbps	18.8 Mbps
4	0	10	12.0 Mbps	15.0 Mbps
5	0	12	10.0 Mbps	12.5 Mbps
5	1	24	5.00 Mbps	6.25 Mbps
5	2	48	2.50 Mbps	3.13 Mbps
5	3	96	1.25 Mbps	1.56 Mbps
255	3	4096	29.3 kbps	36.6 kbps

Note: The settings must not exceed the range of electrical characteristics.

36.2.9 RSPI Data Control Register (SPDCR)

SPDCR controls data in the SPDR register.

Up to four frames can be transmitted or received in one round of transmission or reception activation (m = 0 to 7). The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits.

When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, the bits should be changed while the SPSR.IDLNF flag is 0.

Address(es): RSPI0.SPDCR A006 800Bh, RSPI1.SPDCR A006 840Bh, RSPI2.SPDCR A006 880Bh, RSPI3.SPDCR A006 8C0Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	RSPI Receive/Transmit Data Selection	0: SPDR values are read from the reception buffer 1: SPDR values are read from the transmission buffer (but only if the transmission buffer is empty)	R/W
b5	SPLW	RSPI Longword Access/ Word Access Specification	0: SPDR is accessed in words 1: SPDR is accessed in longwords	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPFC[1:0] Bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR (per transfer activation). Up to four frames can be transmitted or received in one round of transmission or reception, and the amount of data is determined by the combination of the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits. Furthermore, the setting of the SPFC[1:0] bits adjusts the number of frames for generation of RSPI reception buffer full interrupt, and start of transmission or generation of transmission buffer empty interrupts. Table 36.4 lists the frame configurations that can be stored in SPDR and examples of combinations of settings for transmission and reception. Combinations of settings other than those shown in the examples should not be made.

Table 36.4 Settable Combinations of SPSLN[2:0] Bits and SPFC[1:0] Bits

Setting	SPSLN[2:0]	SPFC[1:0]	Number of Frames in a Single Sequence	Number of Frames at which Reception Buffer Full Interrupt Occurs or Transmission Buffer Holding Data is Recognized
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD Bit (RSPI Receive/Transmit Data Selection)

The SPRDTD bit selects whether the SPDR reads values from the reception buffer or from the transmission buffer.
If reading is from the transmission buffer, the value written to SPDR register immediately beforehand is read.
When reading the transmission buffer, do so before writing of the number of frames set in the SPFC[1:0] bits is finished and after generation of the transmission buffer empty interrupt.
For details, refer to section 36.2.5, RSPI Data Register (SPDR).

SPLW Bit (RSPI Longword Access/Word Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR is in words when the SPLW bit is 0 and in longwords when the SPLW bit is 1.
Also, when the SPLW bit is 0, set the SPCMDm.SPB[3:0] bits (RSPI data length setting bits) to 8 to 16 bits. Setting these bits to 20, 24, or 32 bits is prohibited.

36.2.10 RSPI Clock Delay Register (SPCKD)

SPCKD sets a period from the beginning of SSLyi signal assertion to RSPCK oscillation (RSPCK delay) when the SPCMDm.SCKDEN bit is 1. While both the SPCR.MSTR and SPCR.SPE bits are 1, do not change the value of the SPCKD register (m = 0 to 7; y = 0, 1, 2, 3 (for all channels); i = 0 to 3).

Address(es): RSPI0.SPCKD A006 800Ch, RSPI1.SPCKD A006 840Ch, RSPI2.SPCKD A006 880Ch, RSPI3.SPCKD A006 8C0Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SCKDL[2:0] Bits (RSPCK Delay Setting)

The SCKDL[2:0] bits set an RSPCK delay value when the SPCMDm.SCKDEN bit is 1.
When using the RSPI in slave mode, set the SCKDL[2:0] bits to 000b.

36.2.11 RSPI Slave Select Negation Delay Register (SSLND)

SSLND sets a period (SSL negation delay) from the transmission of a final RSPCK edge to the negation of the SSLyi signal during a serial transfer by the RSPI in master mode. Writing to SSLND is prohibited while both the SPCR.MSTR and SPCR.SPE bits are 1 (y = 0, 1, 2, 3 (for all channels); i = 0 to 3).

Address(es): RSPI0.SSLND A006 800Dh, RSPI1.SSLND A006 840Dh, RSPI2.SSLND A006 880Dh, RSPI3.SSLND A006 8C0Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SLNDL[2:0] Bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits set an SSL negation delay value when the RSPI is in master mode.
When using the RSPI in slave mode, set the SLNDL[2:0] bits to 000b.

36.2.12 RSPI Next-Access Delay Register (SPND)

SPND sets a non-active period (next-access delay) of the SSLyi signal after termination of a serial transfer when the SPCMDm.SPNDEN bit is 1. Writing to SPND is prohibited while both the SPCR.MSTR and SPCR.SPE bits are 1 (m = 0 to 7, y = 0, 1, 2, 3 (for all channels); i = 0 to 3).

Address(es): RSPI0.SPND A006 800Eh, RSPI1.SPND A006 840Eh, RSPI2.SPND A006 880Eh, RSPI3.SPND A006 8C0Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SPNDL[2:0]	RSPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 SERICLK 0 0 1: 2 RSPCK + 2 SERICLK 0 1 0: 3 RSPCK + 2 SERICLK 0 1 1: 4 RSPCK + 2 SERICLK 1 0 0: 5 RSPCK + 2 SERICLK 1 0 1: 6 RSPCK + 2 SERICLK 1 1 0: 7 RSPCK + 2 SERICLK 1 1 1: 8 RSPCK + 2 SERICLK	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPNDL[2:0] Bits (RSPI Next-Access Delay Setting)

The SPNDL[2:0] bits set a next-access delay when the SPCMDm.SPNDEN bit is 1.

When using the RSPI in slave mode, set the SPNDL[2:0] bits to 000b.

36.2.13 RSPI Control Register 2 (SPCR2)

The SPCR2 register controls the settings for operation of the RSPI.
Changing the value of SPPE, SPOE, or SCKASE bit in the SPCR2 register is prohibited while the setting of the SPCR.SPE bit is 1.

Address(es): RSPI0.SPCR2 A006 800Fh, RSPI1.SPCR2 A006 840Fh, RSPI2.SPCR2 A006 880Fh, RSPI3.SPCR2 A006 8C0Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPPE	Parity Enable	0: Does not add the parity bit to transmit data and does not check the parity bit of receive data 1: Adds the parity bit to transmit data and checks the parity bit of receive data (when SPCR.TXMD = 0) Adds the parity bit to transmit data but does not check the parity bit of receive data (when SPCR.TXMD = 1)	R/W
b1	SPOE	Parity Mode	0: Selects even parity for use in transmission and reception 1: Selects odd parity for use in transmission and reception	R/W
b2	SPIIE	RSPI Idle Interrupt Enable	0: Disables the generation of idle interrupt requests 1: Enables the generation of idle interrupt requests	R/W
b3	PTE	Parity Self-Testing	0: Disables the self-diagnosis function of the parity circuit 1: Enables the self-diagnosis function of the parity circuit	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: Disables the RSPCK auto-stop function 1: Enables the RSPCK auto-stop function	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPPE Bit (Parity Enable)

The SPPE bit enables or disables the parity function.
The parity bit is added to transmit data and parity checking is performed for receive data when the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1.
The parity bit is added to transmit data but parity checking is not performed for receive data when the SPCR.TXMD bit is 1 and the SPCR2.SPPE bit is 1.

SPOE Bit (Parity Mode)

The SPOE bit specifies odd or even parity.
When even parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit/receive character plus the parity bit is odd.
The SPOE bit is valid only when the SPPE bit is 1.

SPIIE Bit (RSPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of RSPI idle interrupt requests when the RSPI being in the idle state is detected and the SPSR.IDLNF flag is set to 0.

PTE Bit (Parity Self-Testing)

The PTE bit enables the self-diagnosis function of the parity circuit in order to check whether the parity function is operating correctly.

SCKASE Bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs when data is received in master mode. For details, see section 36.3.8.1, Overrun Error.

36.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)

SPCMDm registers control a transfer format for the RSPI in master mode. Each channel has eight RSPI command registers (m = 0 to 7).

Some of the bits in the SPCMD0 register is used to set a transfer format for the RSPI in slave mode. The RSPI in master mode refers to SPCMDm registers in sequence according to the settings in the SPSCR.SPSLN[2:0] bits, and executes the serial transfer that is set in respective SPCMDm registers.

SPCMDm registers should be set while the transmission buffers are empty (data for the next transfer is not set) and before setting of the data that are to be transmitted as a result of reference to the SPCMDm registers.

SPCMDm currently being referred to by the RSPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits. Writing to SPCMDm is prohibited while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1.

Address(es): RSPI0.SPCMD0 A006 8010h, RSPI0.SPCMD1 A006 8012h, RSPI0.SPCMD2 A006 8014h, RSPI0.SPCMD3 A006 8016h, RSPI0.SPCMD4 A006 8018h, RSPI0.SPCMD5 A006 801Ah, RSPI0.SPCMD6 A006 801Ch, RSPI0.SPCMD7 A006 801Eh, RSPI1.SPCMD0 A006 8410h, RSPI1.SPCMD1 A006 8412h, RSPI1.SPCMD2 A006 8414h, RSPI1.SPCMD3 A006 8416h, RSPI1.SPCMD4 A006 8418h, RSPI1.SPCMD5 A006 841Ah, RSPI1.SPCMD6 A006 841Ch, RSPI1.SPCMD7 A006 841Eh, RSPI2.SPCMD0 A006 8810h, RSPI2.SPCMD1 A006 8812h, RSPI2.SPCMD2 A006 8814h, RSPI2.SPCMD3 A006 8816h, RSPI2.SPCMD4 A006 8818h, RSPI2.SPCMD5 A006 881Ah, RSPI2.SPCMD6 A006 881Ch, RSPI2.SPCMD7 A006 881Eh, RSPI3.SPCMD0 A006 8C10h, RSPI3.SPCMD1 A006 8C12h, RSPI3.SPCMD2 A006 8C14h, RSPI3.SPCMD3 A006 8C16h, RSPI3.SPCMD4 A006 8C18h, RSPI3.SPCMD5 A006 8C1Ah, RSPI3.SPCMD6 A006 8C1Ch, RSPI3.SPCMD7 A006 8C1Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLy[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Data sampling on odd edge, data variation on even edge 1: Data variation on odd edge, data sampling on even edge	R/W
b1	CPOL	RSPCK Polarity Setting	0: RSPCK is low when idle 1: RSPCK is high when idle	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: These bits select the base bit rate 0 1: These bits select the base bit rate divided by 2 1 0: These bits select the base bit rate divided by 4 1 1: These bits select the base bit rate divided by 8	R/W
b6 to b4	SSLy[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSLy0 (y = 0, 1, 2, 3) 0 0 1: SSLy1 (y = 0, 1 only) 0 1 0: SSL02 0 1 1: SSL03 Settings other than above are prohibited.	R/W
b7	SSLKP	SSL Signal Level Keeping	0: Negates all SSL signals upon completion of transfer 1: Keeps the SSL signal level from the end of transfer until the beginning of the next access	R/W
b11 to b8	SPB[3:0]	RSPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits	R/W
b12	LSBF	RSPI LSB First	0: MSB first 1: LSB first	R/W

Bit	Symbol	Bit Name	Description	R/W
b13	SPNDEN	RSPI Next-Access Delay Enable	0: A next-access delay of 1 RSPCK + 2 SERICLK 1: A next-access delay is equal to the setting of the RSPI next-access delay register (SPND)	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: An SSL negation delay of 1 RSPCK 1: An SSL negation delay is equal to the setting of the RSPI slave select negation delay register (SSLND)	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay is equal to the setting of the RSPI clock delay register (SPCKD)	R/W

CPHA Bit (RSPCK Phase Setting)

The CPHA bit sets an RSPCK phase of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK phase setting between the modules.

CPOL Bit (RSPCK Polarity Setting)

The CPOL bit sets an RSPCK polarity of the RSPI in master mode or slave mode. Data communications between RSPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] Bits (Bit Rate Division Setting)

The BRDV[1:0] bits are used to determine the bit rate. A bit rate is determined by combinations of the settings in the BRDV[1:0] bits and SPBR (refer to section 36.2.8, RSPI Bit Rate Register (SPBR)). The settings in SPBR determine the base bit rate. The settings in the BRDV[1:0] bits are used to select a bit rate which is obtained by dividing the base bit rate by 1, 2, 4, or 8. In SPCMDm register, different BRDV[1:0] bit settings can be specified. This permits the execution of serial transfers at a different bit rate for each command (m = 0 to 7).

SSLy[2:0] Bits (SSL Signal Assertion Setting)

The SSLy[2:0] bits control the SSLyi signal assertion when the RSPI performs serial transfers in master mode.
Setting the SSLy[2:0] bits controls the assertion for the SSLyi signal. When an SSLyi signal is asserted, its polarity is determined by the set value in the corresponding SSLP. When the SSLy[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLy0 pin acts as input).
When using the RSPI in slave mode, set the SSLy[2:0] bits to 000b.
(y = 0, 1, 2, 3 (for all channels); i = 0 to 3)

SSLKP Bit (SSL Signal Level Keeping)

When the RSPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLyi signal level for the current command is to be kept or negated between the SSL negation timing associated with the current command and the SSL assertion timing associated with the next command.
Setting the SSLKP bit to 1 enables a burst transfer. For details, refer to section 36.3.10.1, (4) Burst Transfer.
When using the RSPI in slave mode, the SSLKP bit should be set to 0.
(y = 0, 1, 2, 3 (for all channels); i = 0 to 3)

SPB[3:0] Bits (RSPI Data Length Setting)

The SPB[3:0] bits set a transfer data length for the RSPI in master mode or slave mode.

LSBF Bit (RSPI LSB First)

The LSBF bit sets the data format of the RSPI in master mode or slave mode to MSB first or LSB first.

SPNDEN Bit (RSPI Next-Access Delay Enable)

The SPNDEN bit sets the period from the time the RSPI in master mode terminates a serial transfer and sets the SSLyi signal inactive until the RSPI enables the SSLyi signal assertion for the next access (next-access delay) (y = 0, 1, 2, 3 (for all channels); i = 0 to 3). If the SPNDEN bit is 0, the RSPI sets the next-access delay to 1 RSPCK + 2 SERICLK. If the SPNDEN bit is 1, the RSPI inserts a next-access delay in compliance with the SPND setting.
When using the RSPI in slave mode, the SPNDEN bit should be set to 0.

SLNDEN Bit (SSL Negation Delay Setting Enable)

The SLNDEN bit sets the period from the time the RSPI in master mode stops RSPCK oscillation until the RSPI sets the SSLyi signal inactive (SSL negation delay). If the SLNDEN bit is 0, the RSPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the RSPI negates the SSL signal at an SSL negation delay in compliance with the SSLND setting.
When using the RSPI in slave mode, the SLNDEN bit should be set to 0.

SCKDEN Bit (RSPCK Delay Setting Enable)

The SCKDEN bit sets the period from the point when the RSPI in master mode activates the SSLyi signal until the RSPCK starts oscillation (RSPI clock delay). If the SCKDEN bit is 0, the RSPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the RSPI starts the oscillation of RSPCK at an RSPCK delay in compliance with the SPCKD setting.
When using the RSPI in slave mode, the SCKDEN bit should be set to 0.

36.3 Operation

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data.

36.3.1 Overview of RSPI Operations

The RSPI is capable of synchronous serial transfers in slave mode (SPI operation), single-master mode (SPI operation), multi-master mode (SPI operation), slave mode (clock synchronous operation), and master mode (clock synchronous operation). A particular mode of the RSPI can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 36.5 lists the relationship between RSPI modes and SPCR settings, and a description of each mode.

Table 36.5 Relationship between RSPI Modes and SPCR Settings and Description of Each Mode

Mode	Slave (SPI Operation)	Single-Master (SPI Operation)	Multi-Master (SPI Operation)	Slave (Clock Synchronous Operation)	Master (Clock Synchronous Operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKy signal	Input	Output	Output/Hi-Z	Input	Output
MOSIy signal	Input	Output	Output/Hi-Z	Input	Output
MISOy signal	Output/Hi-Z	Input	Input	Output	Input
SSLy0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLy1 to SSLy3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity modification function	Supported	Supported	Supported	—	—
Transfer rate	Up to SERICLK/8	Up to SERICLK/4	Up to SERICLK/4	Up to SERICLK/8	Up to SERICLK/4
Clock source	RSPCK input	On-chip baud rate generator	On-chip baud rate generator	RSPCK input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	—	—
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer activation method	SSL input active or RSPCK oscillation	Transmission buffer is written to at generation of a transmission buffer empty interrupt request	Transmission buffer is written to at generation of a transmission buffer empty interrupt request	RSPCK oscillation	Transmission buffer is written to at generation of a transmission buffer empty interrupt request
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmission buffer empty detection	Supported				
Reception buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, receiver buffer full detection, overrun error detection, and parity error detection are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection does not proceed.
y = 0, 1, 2, 3 (for all channels)

36.3.2 Controlling RSPI Pins

According to the SPCR.MSTR, MODFEN, SPMS, and SPPCR.SPOM bits, the RSPI can switch pin states. Table 36.6 lists the relationship between pin states and bit settings. Setting the SPPCR.SPOM bit to 0 selects CMOS output; setting it to 1 selects open-drain output. The I/O port settings should follow this relationship.

Table 36.6 Relationship between Pin States and Bit Settings

		Pin State*2	
Mode	**Pin**	**SPOM = 0**	**SPOM = 1**
Single-master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKy	CMOS output	Open-drain output
	SSLy0 to SSLy3	CMOS output	Open-drain output
	MOSIy	CMOS output	Open-drain output
	MISOy	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKy*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLy0	Input	Input
	SSLy1 to SSLy3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIy*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOy	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKy	Input	Input
	SSLy0	Input	Input
	SSLy1 to SSLy3*5	Hi-Z*1	Hi-Z*1
	MOSIy	Input	Input
	MISOy*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (Clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKy	CMOS output	Open-drain output
	SSLy0 to SSLy3*5	Hi-Z*1	Hi-Z*1
	MOSIy	CMOS output	Open-drain output
	MISOy	Input	Input
Slave mode (Clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKy	Input	Input
	SSLy0 to SSLy3*5	Hi-Z*1	Hi-Z*1
	MOSIy	Input	Input
	MISOy	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. RSPI settings are not reflected in the multiplex pins for which the RSPI function is not selected.
Note 3. When SSLy0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLy0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.
y = 0, 1, 2, 3 (for all channels)

The RSPI in single-master mode (SPI operation) or multi-master mode (SPI operation) determines MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) according to MOIFE and MOIFV bit settings in SPPCR, as listed in Table 36.7.

Table 36.7 MOSI Signal Value Determination during SSL Negation Period

MOIFE Bit	MOIFV Bit	MOSIy Signal Value during SSL Negation Period
0	0, 1	Final data from previous transfer
1	0	Always low
1	1	Always high

Note: During the period of SSL negation, the RSPI function must be enabled (i.e. SPCR.SPE bit = 1) for control over the levels of the MOSIy signals.

36.3.3 RSPI System Configuration Examples

36.3.3.1 Single Master/Single Slave (with This LSI Acting as Master)

Figure 36.5 shows a single-master/single-slave RSPI system configuration example when this LSI is used as a master. In the single-master/single-slave configuration, the SSLy0 to SSLy3 output of this LSI (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is always maintained in a select state.*1
This LSI (master) always drives RSPCKy and MOSIy. The SPI slave always drives the MISO.
(y = 0, 1, 2, 3 (for all channels))

Note 1. In the transfer format corresponding to the case where the SPCMDm.CPHA bit is 0, there are slave devices for which the SSL signal cannot be fixed to the active level. In situations where the SSL signal cannot be fixed, the SSLyi output of this LSI should be connected to the SSL input of the slave device.

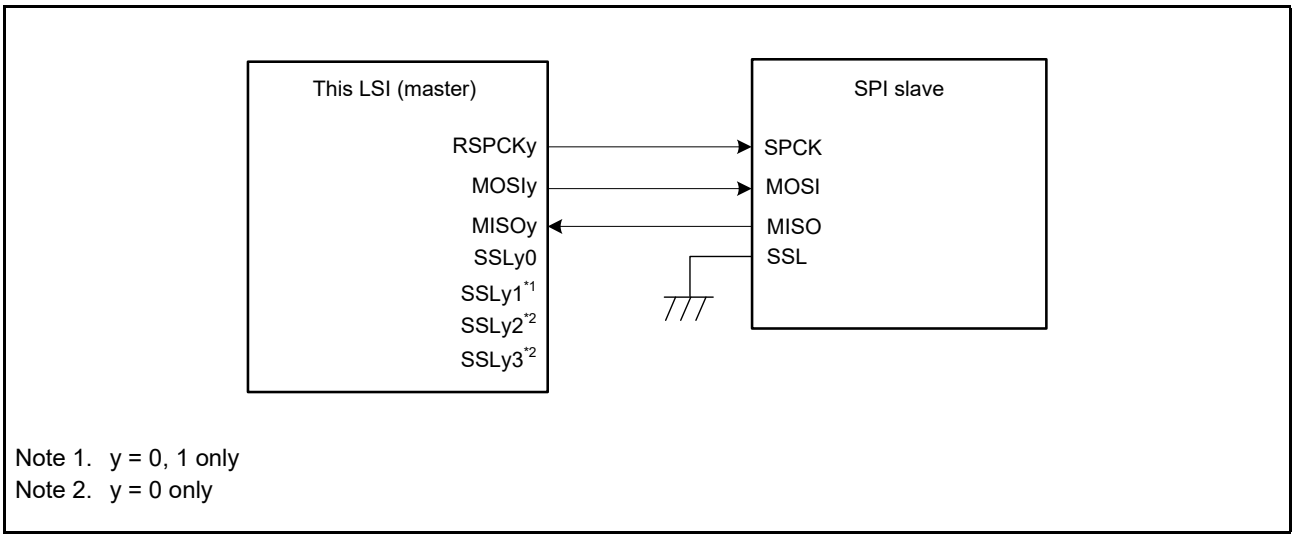


Figure 36.5 Single-Master/Single-Slave Configuration Example (This LSI = Master)

36.3.3.2 Single Master/Single Slave (with This LSI Acting as Slave)

Figure 36.6 shows a single-master/single-slave RSPI system configuration example when this LSI is used as a slave. When this LSI is to operate as a slave, the SSLy0 pin is used as SSL input. The SPI master always drives the RSPCK and MOSI. This LSI (slave) always drives the MISOy.*1

In the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, the SSLy0 input of this LSI (slave) is fixed to the low level, this LSI (slave) is always maintained in a select state, and in this manner it is possible to execute serial transfer (Figure 36.7).

(y = 0, 1, 2, 3 (for all channels))

Note 1. When SSLy0 is at the non-active level, the pin state is Hi-Z.

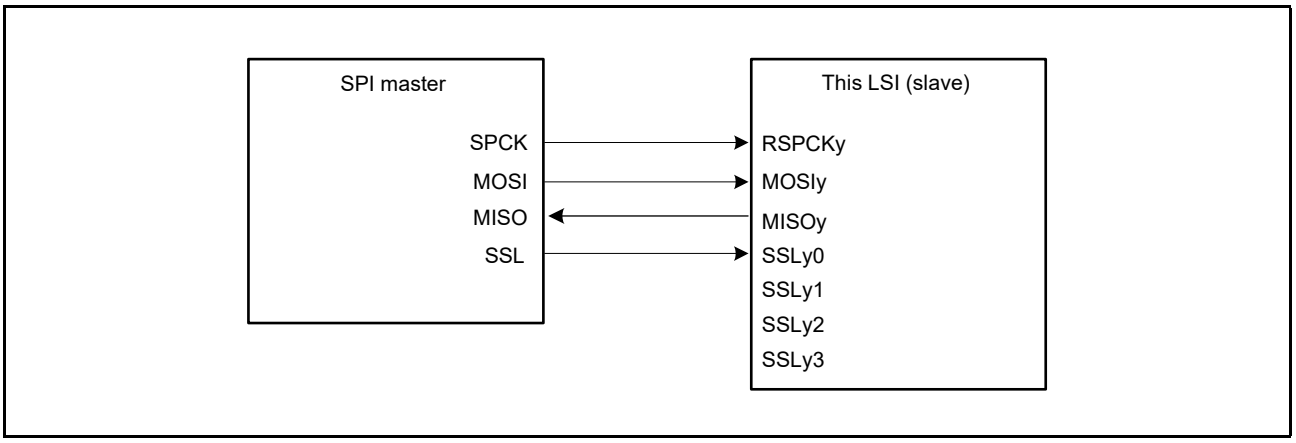


Figure 36.6 Single-Master/Single-Slave Configuration Example (This LSI = Slave, CPHA = 0)

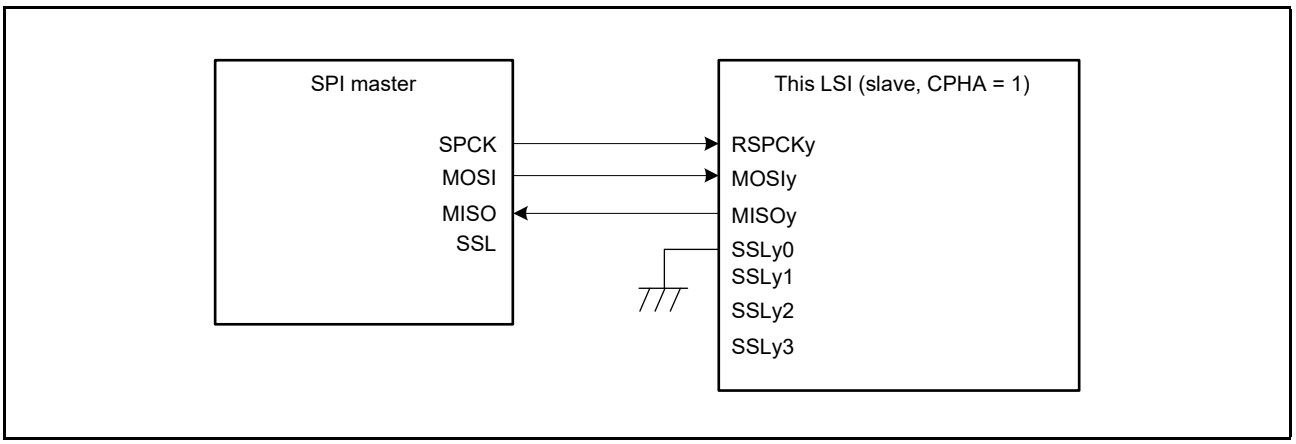


Figure 36.7 Single-Master/Single-Slave Configuration Example (This LSI = Slave, CPHA = 1)

36.3.3.3 Single Master/Multi-Slave (with This LSI Acting as Master)

Figure 36.8 shows a single-master/multi-slave RSPI system configuration example when this LSI is used as a master. In the example of Figure 36.8, the RSPI system is comprised of this LSI (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKy and MOSIy outputs of this LSI (master) are connected to the RSPCK and MOSI inputs of SPI slave 0 to SPI slave 3. The MISO outputs of SPI slave 0 to SPI slave 3 are all connected to the MISOy input of this LSI (master). SSLy0 to SSLy3 outputs of this LSI (master) are connected to the SSL inputs of SPI slave 0 to SPI slave 3, respectively. This LSI (master) always drives RSPCK, MOSI, and SSLy0 to SSLy3. Of the SPI slave 0 to SPI slave 3, the slave that receives low-level input into the SSL input drives MISO.

(y = 0, 1, 2, 3 (for all channels))

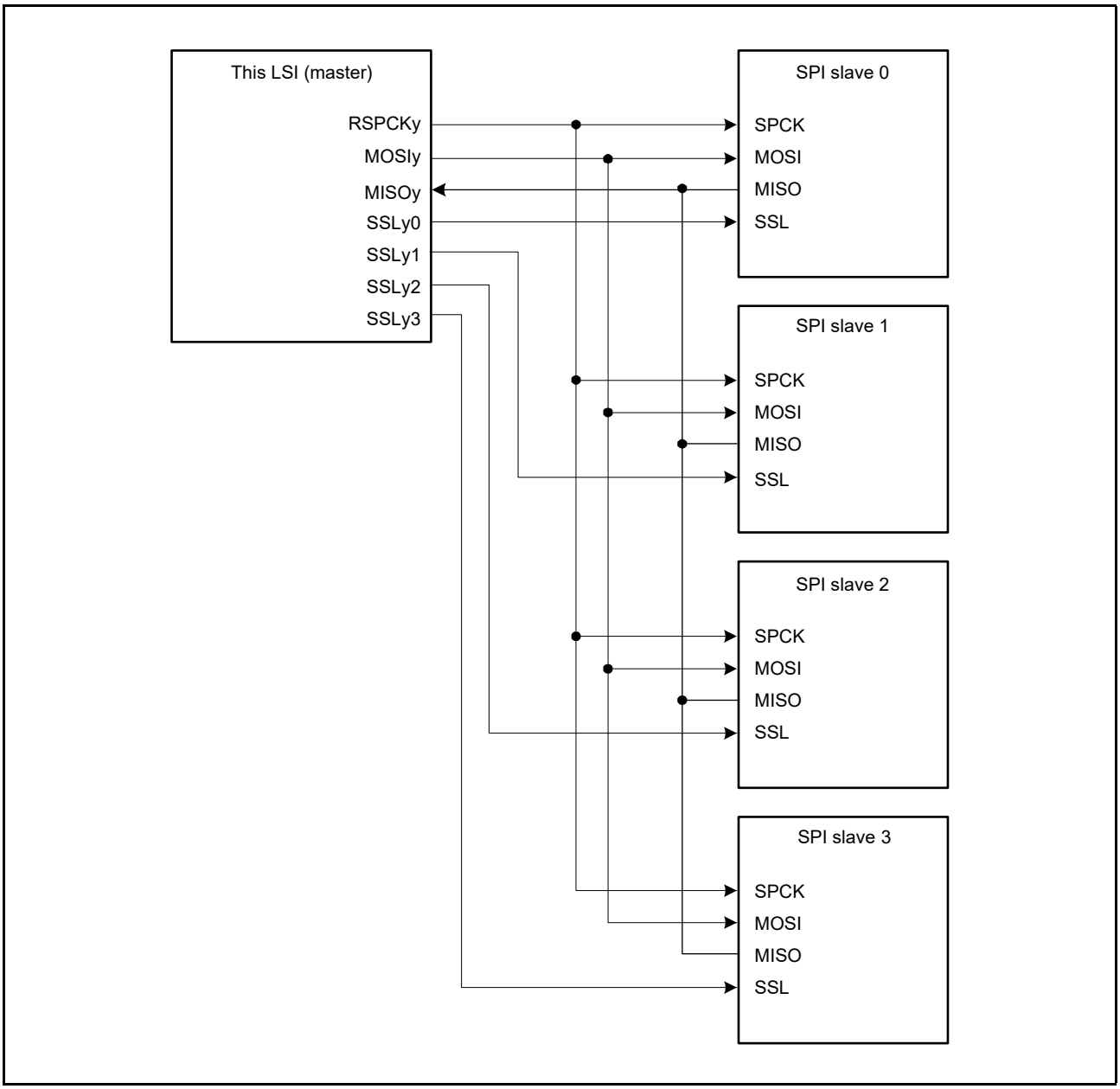


Figure 36.8 Single-Master/Multi-Slave Configuration Example (This LSI = Master)

36.3.3.4 Single Master/Multi-Slave (with This LSI Acting as Slave)

Figure 36.9 shows a single-master/multi-slave RSPI system configuration example when this LSI is used as a slave. In the example of Figure 36.9, the RSPI system is comprised of an SPI master and two LSIs (slave X and slave Y).
The SPCK and MOSI outputs of the SPI master are connected to the RSPCKy and MOSIy inputs of the LSIs (slave X and slave Y). The MISOy outputs of the LSIs (slave X and slave Y) are all connected to the MISO input of the SPI master. SSLX and SSLY outputs of the SPI master are connected to the SSLy0 inputs of the LSIs (slave X and slave Y), respectively.
The SPI master always drives SPCK, MOSI, SSLX, and SSLY. Of the LSIs (slave X and slave Y), the slave that receives low-level input into the SSLy0 input drives MISOy.
(y = 0, 1, 2, 3 (for all channels))

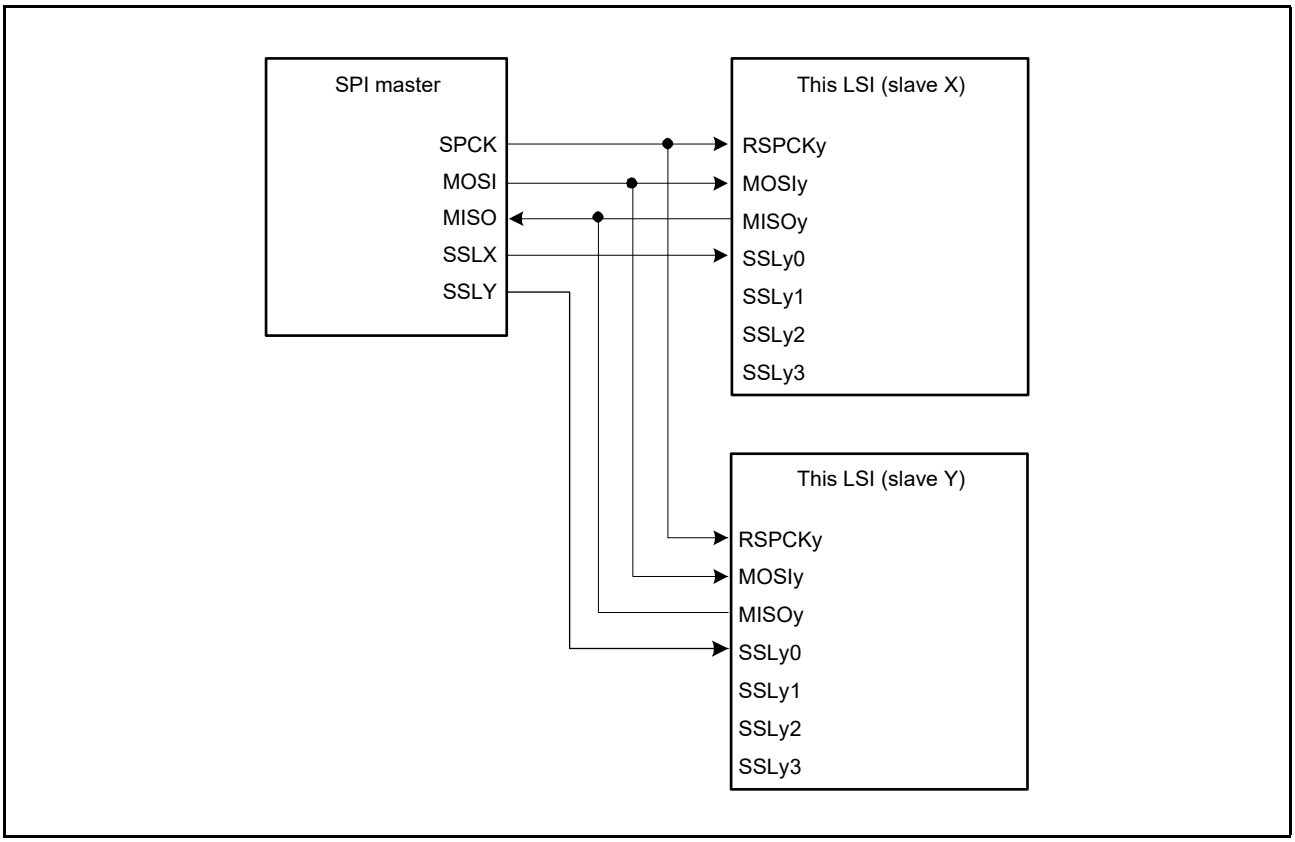


Figure 36.9 Single-Master/Multi-Slave Configuration Example (This LSI = Slave)

36.3.3.5 Multi-Master/Multi-Slave (with This LSI Acting as Master)

Figure 36.10 shows a multi-master/multi-slave RSPI system configuration example when this LSI is used as a master. In the example of Figure 36.10, the RSPI system is comprised of two LSIs (master X and master Y) and two SPI slaves (SPI slave 1 and SPI slave 2).

The RSPCKy and MOSIy outputs of the LSIs (master X and master Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOy inputs of the LSIs (master X and master Y). Any generic port Y output from this LSI (master X) is connected to the SSLy0 input of this LSI (master Y). Any generic port X output of this LSI (master Y) is connected to the SSLy0 input of this LSI (master X). The SSLy1 and SSLy2 outputs of the LSIs (master X and master Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, since the system can be comprised solely of SSLy0 input, and SSLy1 and SSLy2 outputs for slave connections, the SSLy3 output of this LSI is not required.

This LSI drives RSPCKy, MOSIy, SSLy1, and SSLy2 when the SSLy0 input level is high. When the SSLy0 input level is low, this LSI detects a mode fault error, sets RSPCKy, MOSIy, SSLy1, and SSLy2 to Hi-Z, and releases the RSPI bus right to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives MISO.

(y = 0, 1, 2, 3 (for all channels))

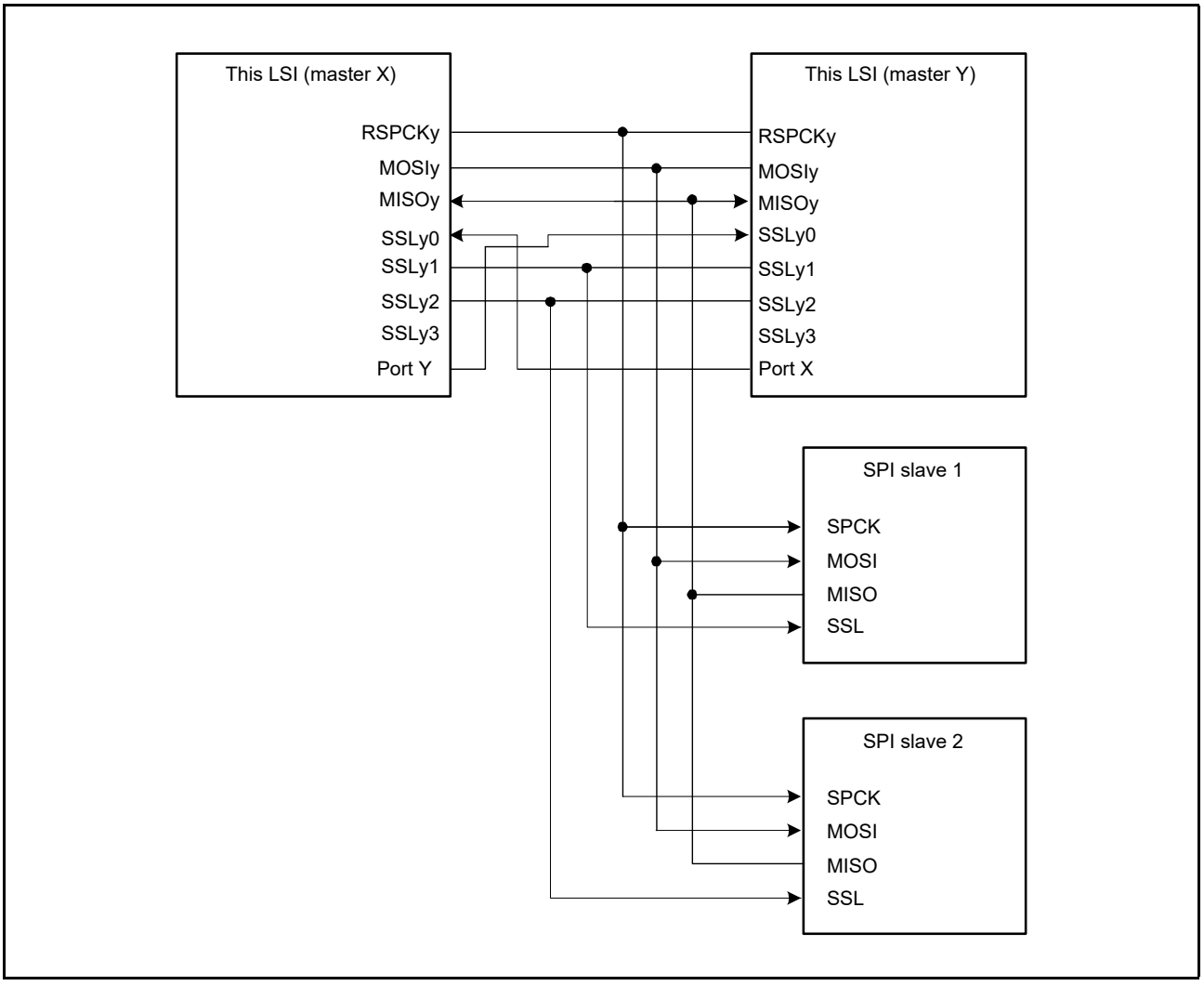


Figure 36.10 Multi-Master/Multi-Slave Configuration Example (This LSI = Master)

36.3.3.6 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This LSI Acting as Master)

Figure 36.11 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this LSI is used as a master. In the master (clock synchronous operation)/slave (clock synchronous operation) configuration, SSLy0 to SSLy3 of this LSI (master) are not used.
This LSI (master) always drives the RSPCKy and MOSIy. The SPI slave always drives the MISO.
(y = 0, 1, 2, 3 (for all channels))

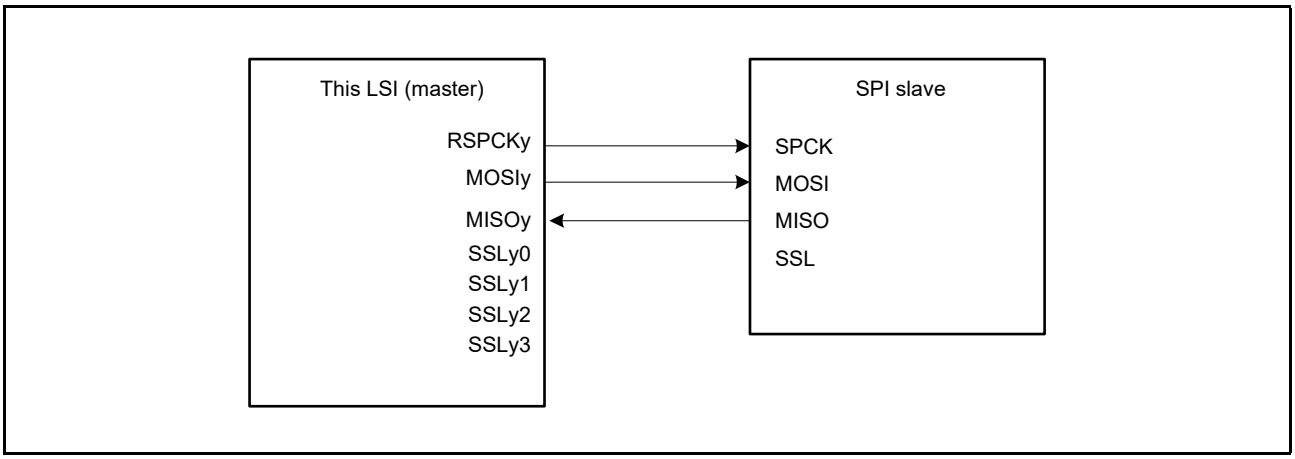


Figure 36.11 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This LSI = Master)

36.3.3.7 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) (with This LSI Acting as Slave)

Figure 36.12 shows a master (clock synchronous operation)/slave (clock synchronous operation) RSPI system configuration example when this LSI is used as a slave. When this LSI is to operate as a slave (clock synchronous operation), this LSI (slave) always drives the MISOy and the SPI master always drives the SPCK and MOSI. In addition, SSLy0 to SSLy3 of this LSI (slave) are not used.
Only in the single-slave configuration in which the SPCMDm.CPHA bit is set to 1, this LSI (slave) can execute serial transfer.
(y = 0, 1, 2, 3 (for all channels))

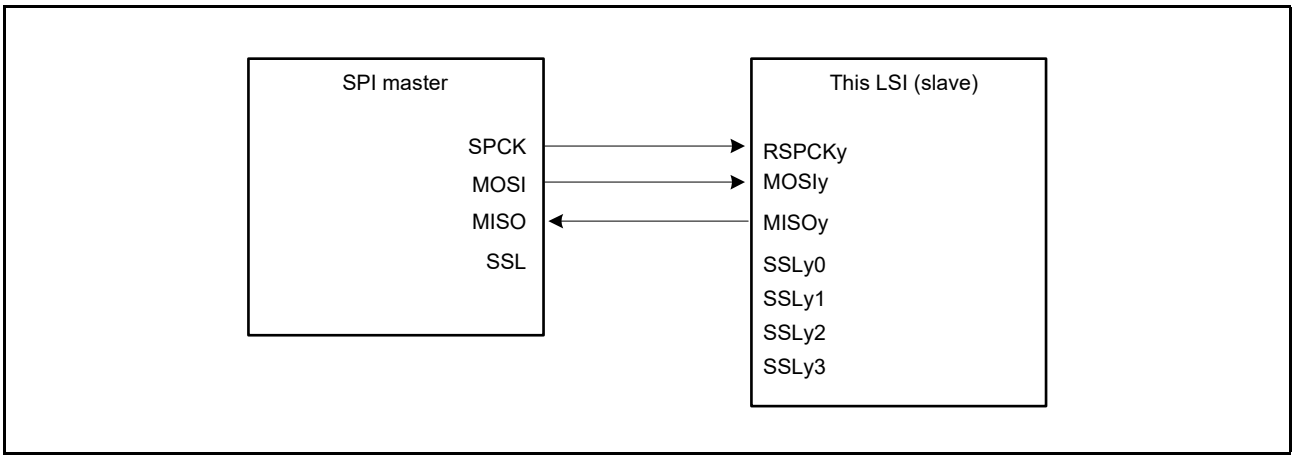


Figure 36.12 Master (Clock Synchronous Operation)/Slave (Clock Synchronous Operation) Configuration Example (This LSI = Slave, CPHA = 1)

36.3.4 Data Format

The RSPI's data format depends on the settings in RSPI command register m (SPCMDm) (m = 0 to 7) and the parity enable bit of RSPI control register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the RSPI treats the range from the LSB bit of the RSPI data register (SPDR) to the selected data length as transfer data.
The format of one frame of data before or after transfer is shown below.

(a) With Parity Disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the RSPI data length setting bits in RSPI command register m (SPCMDm.SPB[3:0]).

(b) With Parity Enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the RSPI data length setting bits in RSPI command register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

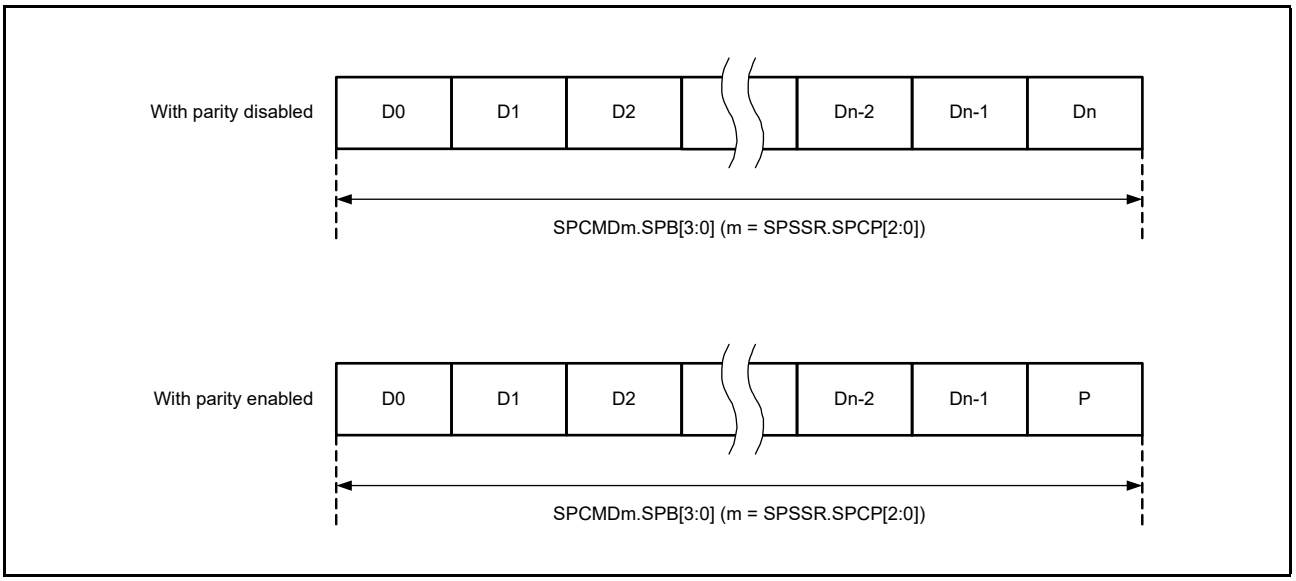


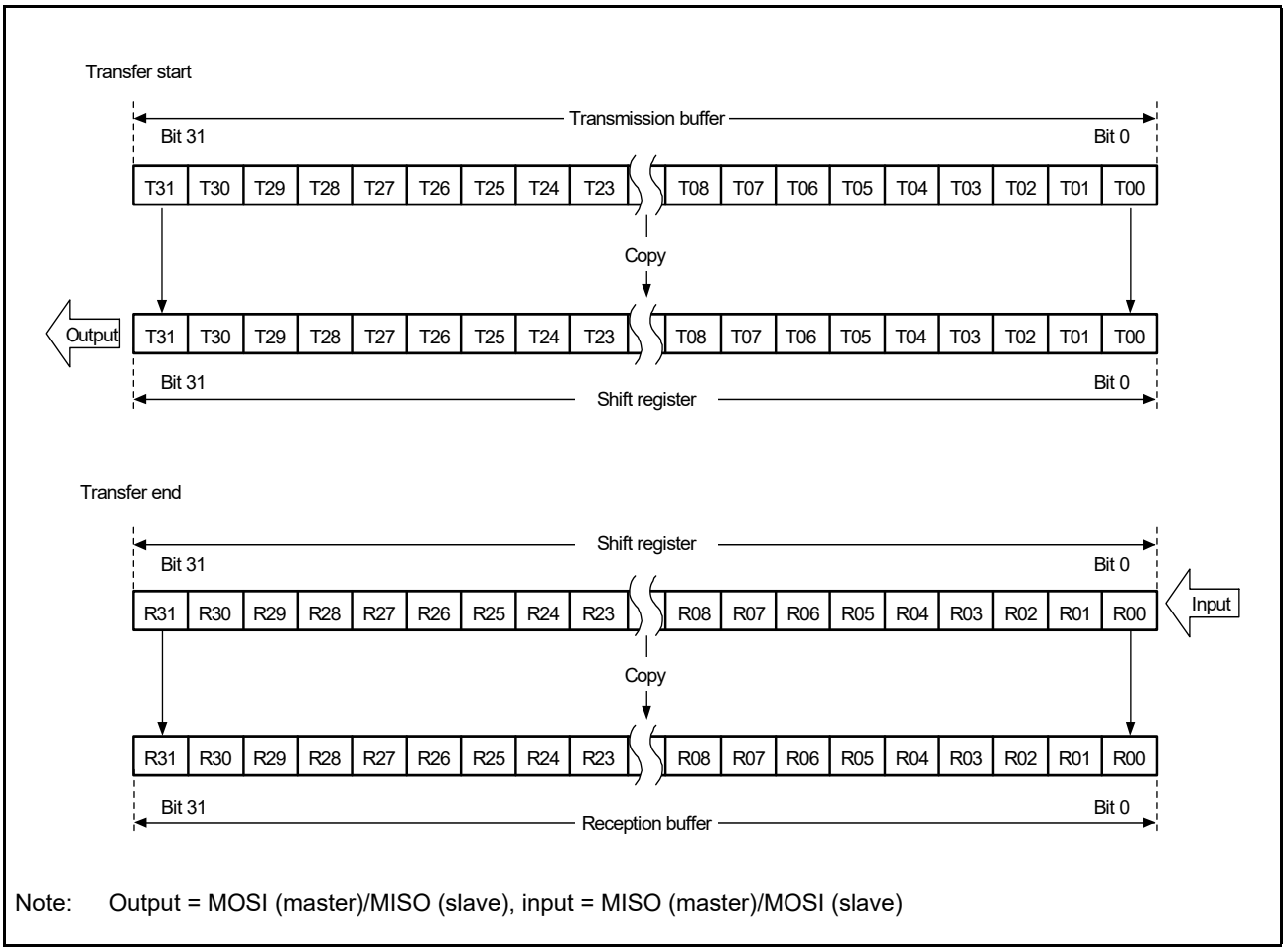
Figure 36.13 Outline of the Data Format (with Parity Disabled/Enabled)

36.3.4.1 When Parity is Disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission are copied to the shift register with no prior processing. A description of the connection between the RSPI data register (SPDR) and the shift register in terms of the combination of MSB or LSB first and data length is given below.

(1) MSB First Transfer (32-Bit Data)

Figure 36.14 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and MSB first selected.
In transmission, bits T31 to T00 from the current stage of the transmission buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T31, through T30, and so on to T00.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

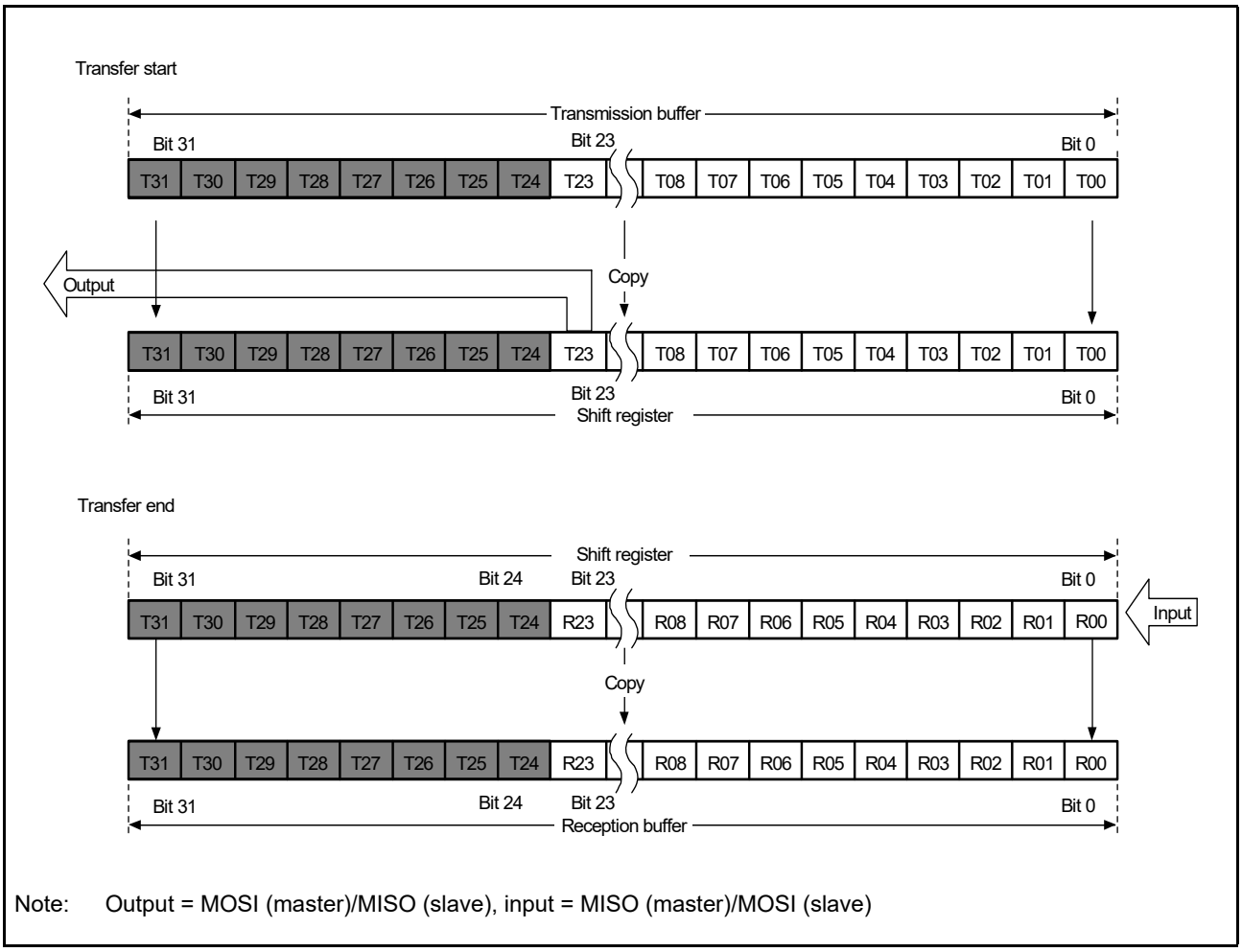
Figure 36.14 MSB First Transfer (32-Bit Data, Parity Disabled)

(2) MSB First Transfer (24-Bit Data)

Figure 36.15 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB first selected.

In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmission buffer are copied to the shift register. Data for transmission are shifted out from the shift register in order from T23, through T22, and so on to T00.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to R00 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer. At this time, the higher-order 8 bits of the transmission buffer are stored in the higher-order 8 bits of the reception buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

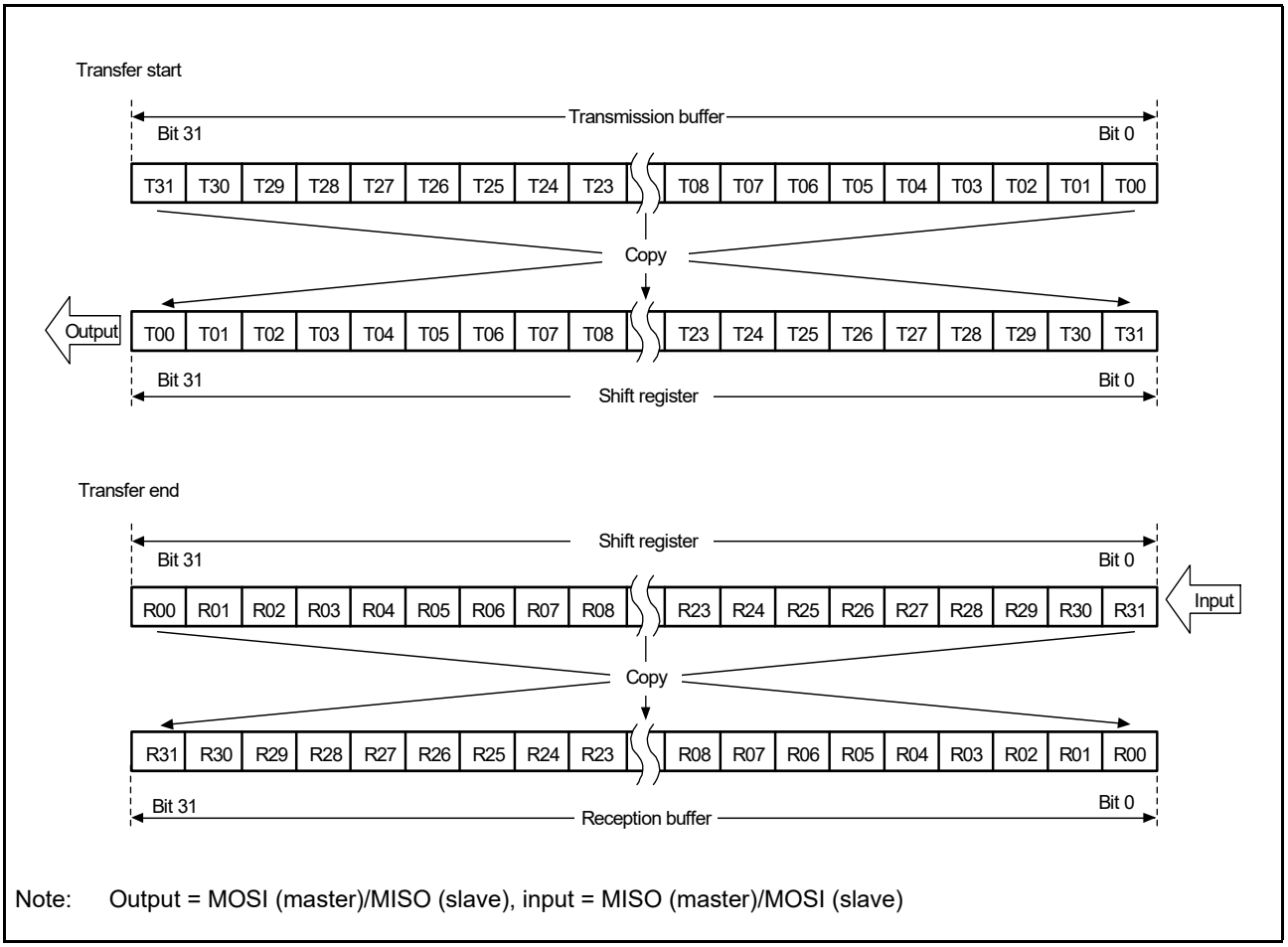
Figure 36.15 MSB First Transfer (24-Bit Data, Parity Disabled)

(3) LSB First Transfer (32-Bit Data)

Figure 36.16 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, an RSPI data length of 32 bits, and LSB first selected.

In transmission, bits T31 to T00 from the current stage of the transmission buffer are reordered bit by bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T31.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to R31 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 36.16 LSB First Transfer (32-Bit Data, Parity Disabled)

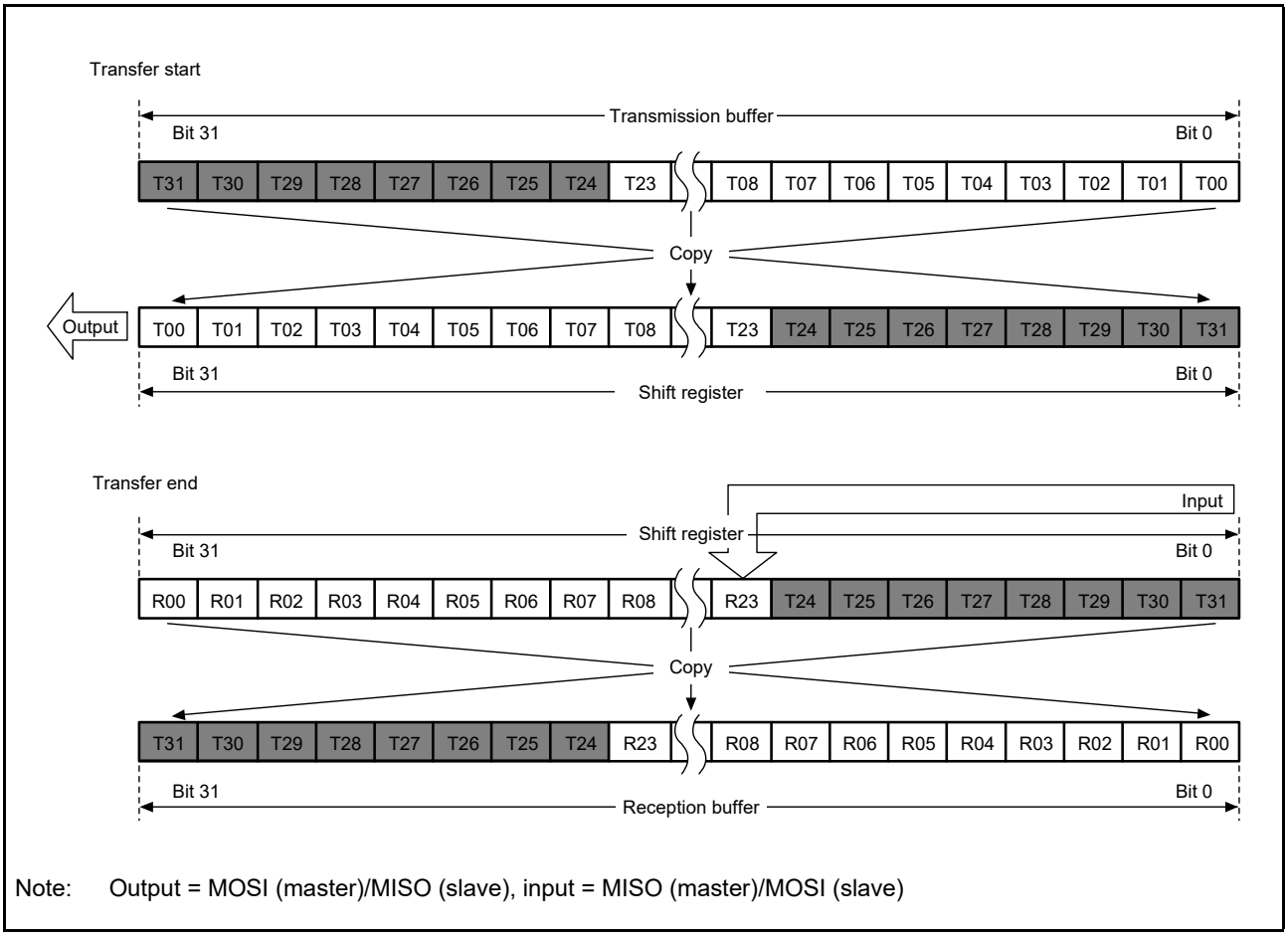
(4) LSB First Transfer (24-Bit Data)

Figure 36.17 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity disabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB first selected.

In transmission, the lower-order 24 bits (T23 to T00) from the current stage of the transmission buffer are reordered bit by bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission are shifted out from the shift register in order from T00, through T01, and so on to T23.

In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R00 to R23 have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer.

At this time, the higher-order 8 bits of the transmission buffer are stored in the higher-order 8 bits of the reception buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

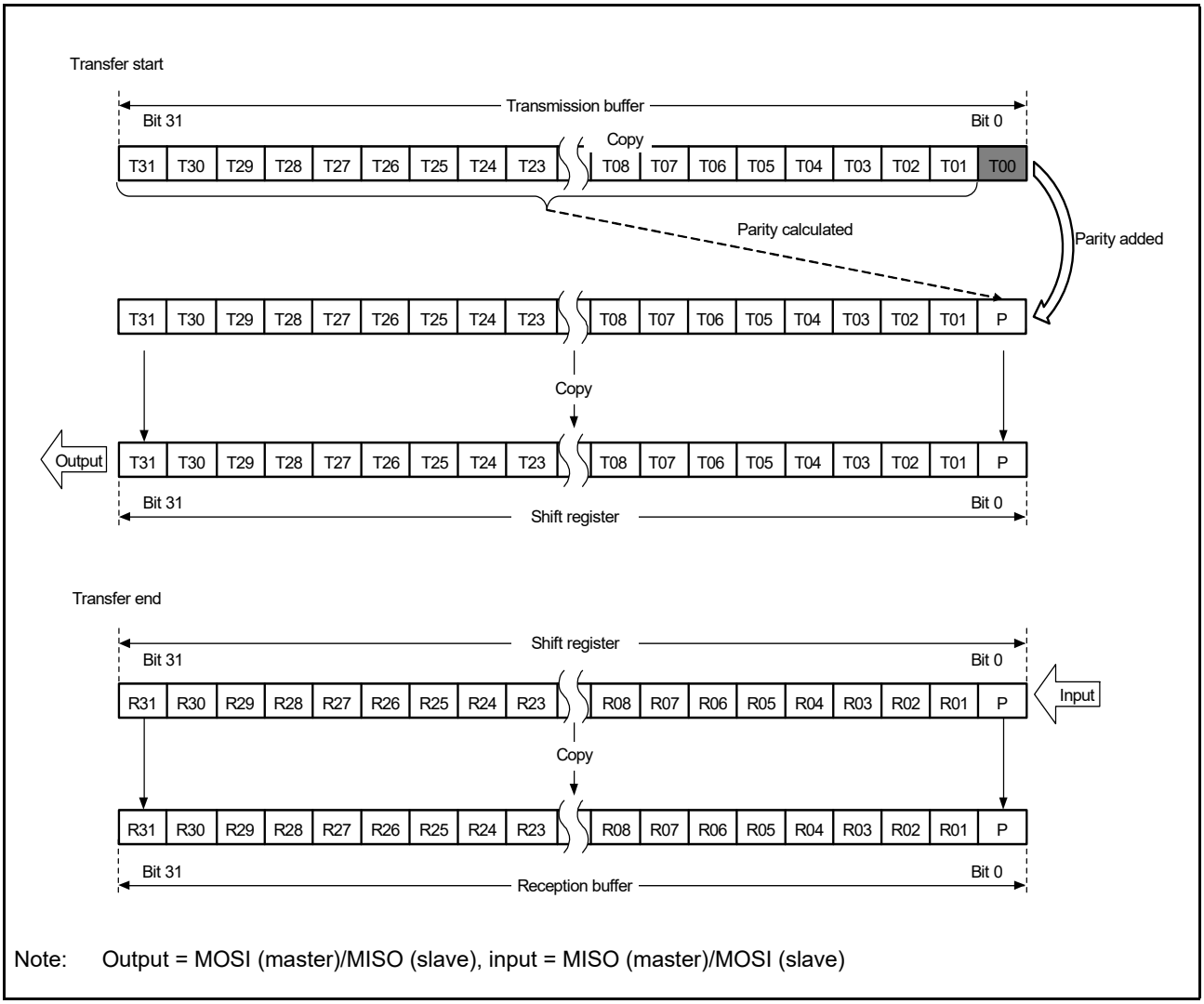
Figure 36.17 LSB First Transfer (24-Bit Data, Parity Disabled)

36.3.4.2 When Parity is Enabled (SPCR2.SPPE = 1)

When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB First Transfer (32-Bit Data)

Figure 36.18 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and MSB first selected.
In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T31, T30, …, T01, and P.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R31 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer. On copying of data to the shift register, the data from R31 to P are checked by judging the parity.

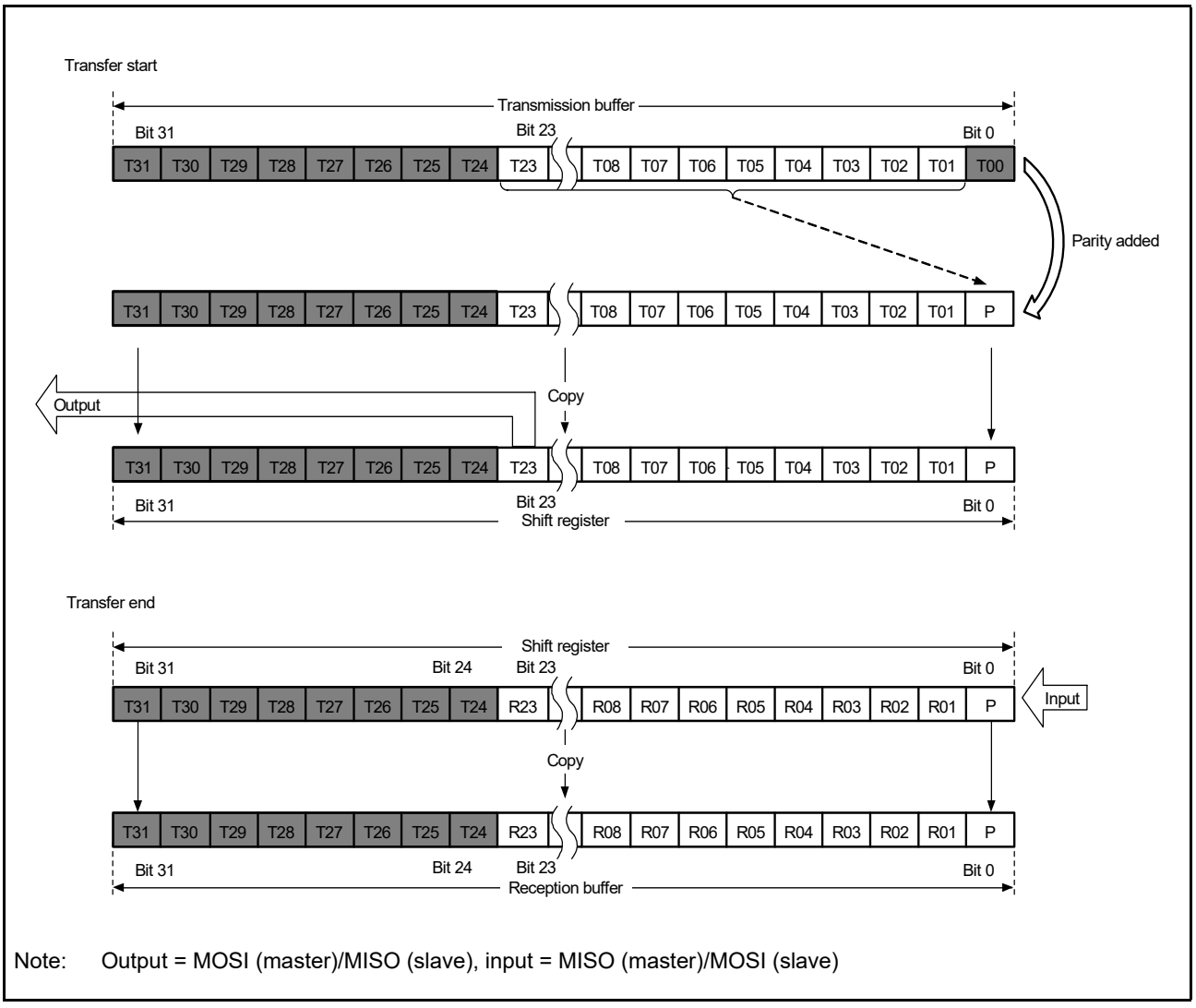


Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 36.18 MSB First Transfer (32-Bit Data, Parity Enabled)

(2) MSB First Transfer (24-Bit Data)

Figure 36.19 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and MSB first selected.
In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data are transmitted in the order T23, T22, …, T01, and P.
In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R23 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer. On copying of data to the shift register, the data from R23 to P are checked by judging the parity. At this time, the higher-order 8 bits of the transmission buffer are stored in the higher-order 8 bits of the reception buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

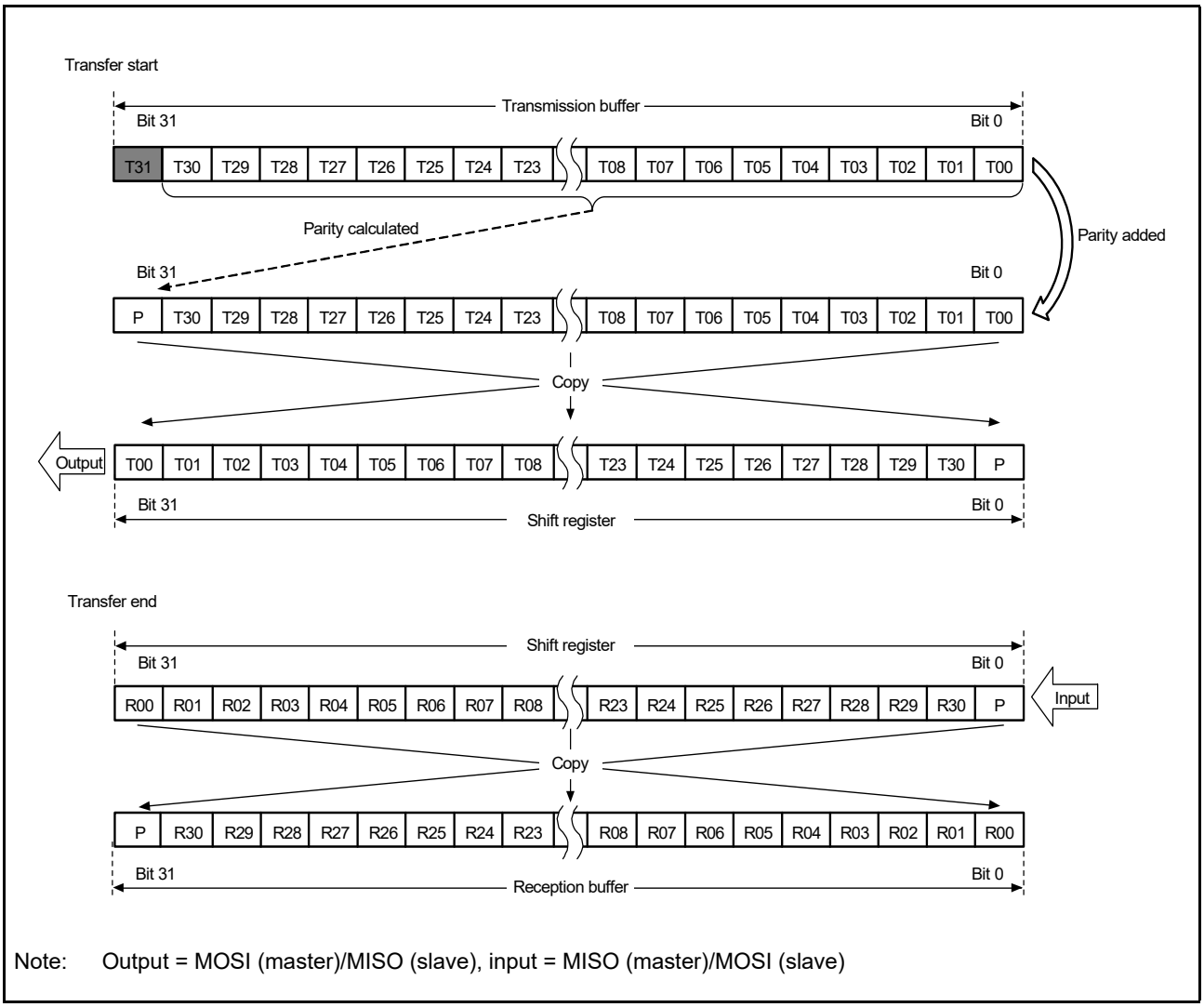
Figure 36.19 MSB First Transfer (24-Bit Data, Parity Enabled)

(3) LSB First Transfer (32-Bit Data)

Figure 36.20 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, an RSPI data length of 32 bits, and LSB first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T30, and P.

In reception, received data are shifted in bit by bit through bit 0 of the shift register. When bits R00 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity.

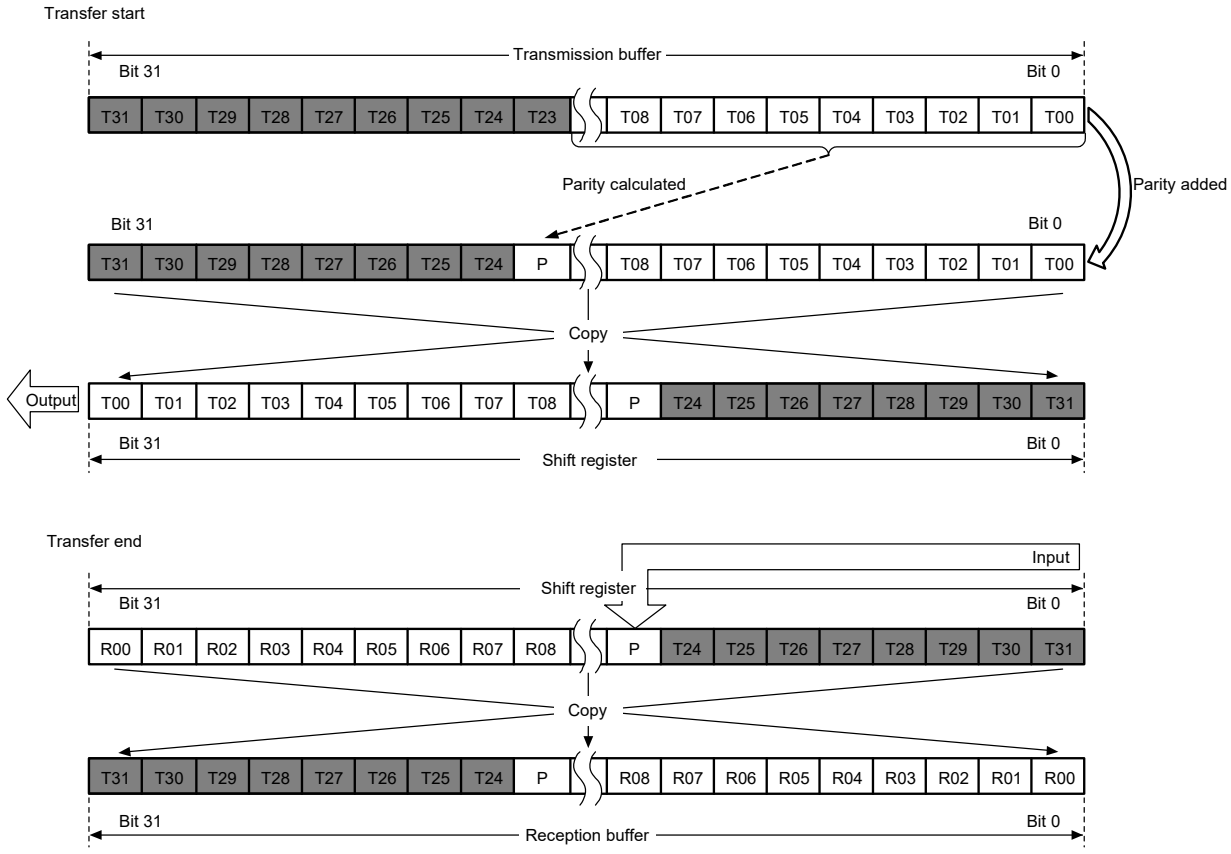


Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 36.20 LSB First Transfer (32-Bit Data, Parity Enabled)

(4) LSB First Transfer (24-Bit Data)

Figure 36.21 shows details of operations by the RSPI data register (SPDR) and the shift register in transfer with parity enabled, 24 bits as the RSPI data length for an example that is not 32 bits, and LSB first selected.
In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole is copied to the shift register. Data are transmitted in the order T00, T01, …, T22, and P.
In reception, received data are shifted in bit by bit through bit 8 of the shift register. When bits R00 to P have been collected after input of the required number of cycles of RSPCK, the value in the shift register is copied to the reception buffer. On copying of data to the shift register, the data from R00 to P are checked by judging the parity. At this time, the higher-order 8 bits of the transmission buffer are stored in the higher-order 8 bits of the reception buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the higher-order 8 bits of the reception buffer.



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 36.21 LSB First Transfer (24-Bit Data, Parity Enabled)

36.3.5 Transfer Format

36.3.5.1 CPHA = 0

Figure 36.22 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Note that clock synchronous operation (the SPCR.SPMS bit is 1) should not be set when the RSPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In Figure 36.22, RSPCKy (CPOL = 0) indicates the RSPCKy signal waveform when the SPCMDm.CPOL bit is 0; RSPCKy (CPOL = 1) indicates the RSPCKy signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the RSPI settings. For details, refer to section 36.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIy and MISOy signals commences at an SSLyi signal assertion timing. The first RSPCKy signal change timing that occurs after the SSLyi signal assertion becomes the first transfer data fetch timing. After this timing, data is sampled at every 1 RSPCK cycle. The change timing for MOSIy and MISOy signals is always 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing; it only affects the signal polarity.

t1 denotes a period from an SSLyi signal assertion to RSPCKy oscillation (RSPCK delay). t2 denotes a period from the termination of RSPCKy oscillation to an SSLyi signal negation (SSL negation delay). t3 denotes a period in which SSLyi signal assertion is suppressed for the next transfer after the end of serial transfer (next-access delay). t1, t2, and t3 are controlled by a master device running on the RSPI system. For a description of t1, t2, and t3 when the RSPI of this LSI is in master mode, refer to section 36.3.10.1, Master Mode Operation.

(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

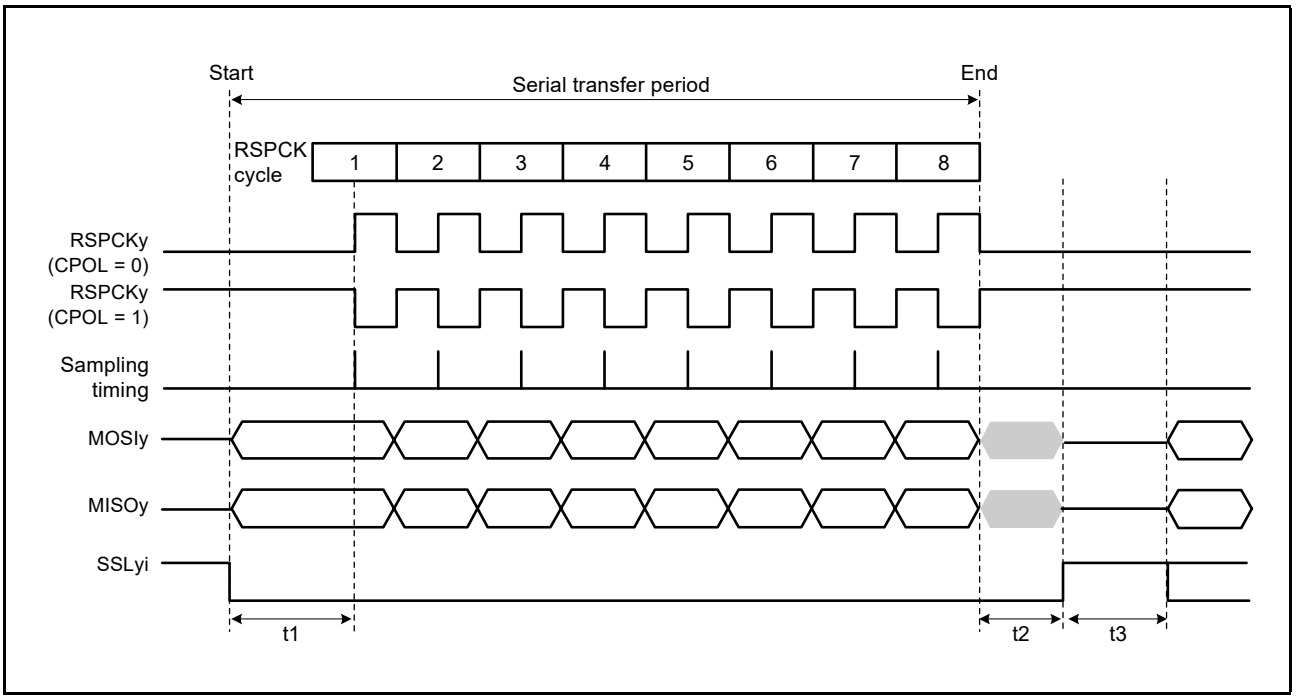


Figure 36.22 RSPI Transfer Format (CPHA = 0)

36.3.5.2 CPHA = 1

Figure 36.23 shows a sample transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLyi signals are not used, and only the three signals RSPCKy, MOSIy, and MISOy handle communications. In Figure 36.23, RSPCK (CPOL = 0) indicates the RSPCKy signal waveform when the SPCMDm.CPOL bit is 0; RSPCK (CPOL = 1) indicates the RSPCKy signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the RSPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the RSPI mode (master or slave). For details, refer to section 36.3.2, Controlling RSPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOy signal commences at an SSLyi signal assertion timing. The output of valid data to the MOSIy and MISOy signals commences at the first RSPCKy signal change timing that occurs after the SSLyi signal assertion. After this timing, data is updated at every 1 RSPCK cycle. The transfer data fetch timing is always 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKy signal operation timing; it only affects the signal polarity.

t1, t2, and t3 are the same as those in the case of CPHA = 0. For a description of t1, t2, and t3 when the RSPI of this LSI is in master mode, refer to section 36.3.10.1, Master Mode Operation.

(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

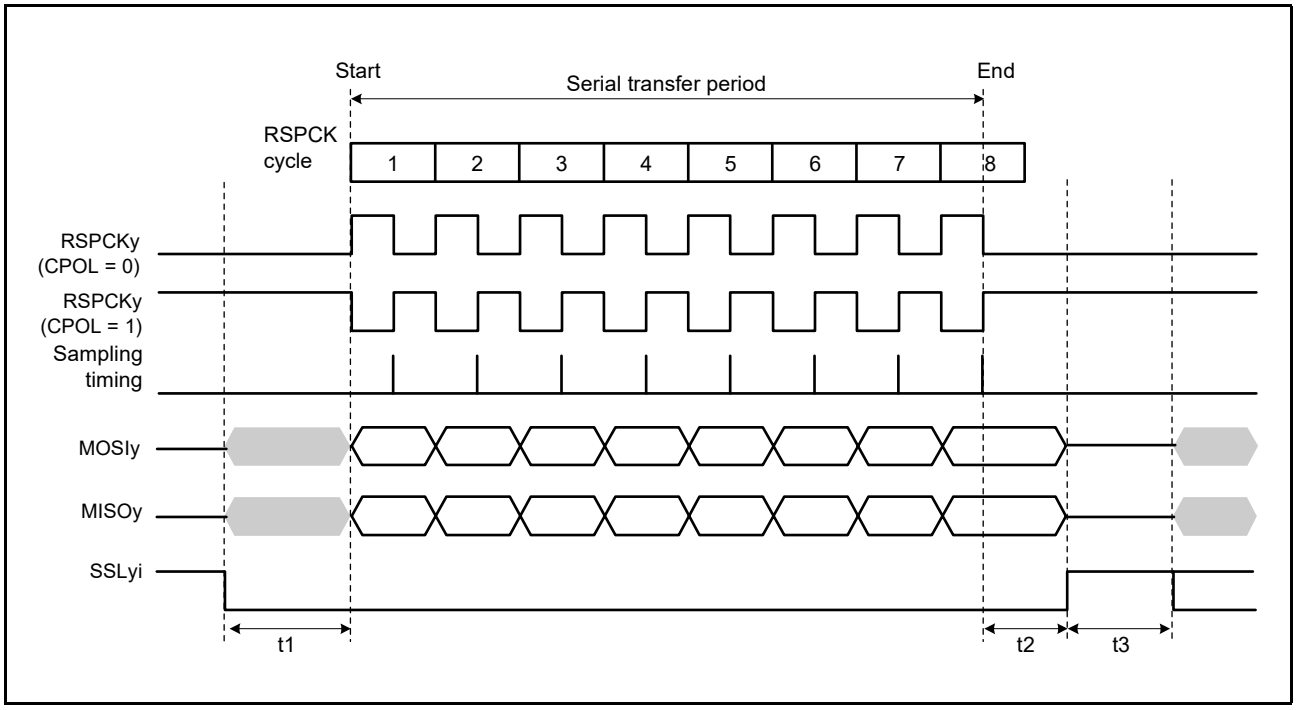


Figure 36.23 RSPI Transfer Format (CPHA = 1)

36.3.6 Communications Operating Mode

Full-duplex synchronous serial communications or transmit operations only can be selected by the communications operating mode select bit (SPCR.TXMD). The SPDR access shown in Figure 36.24 and Figure 36.25 indicates the condition of access to the SPDR register, where W denotes a write cycle.

36.3.6.1 Full-Duplex Synchronous Serial Communications (SPCR.TXMD = 0)

Figure 36.24 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 0. In the example in Figure 36.24, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKy waveform represent the number of RSPCK cycles (i.e., the number of transferred bits) (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

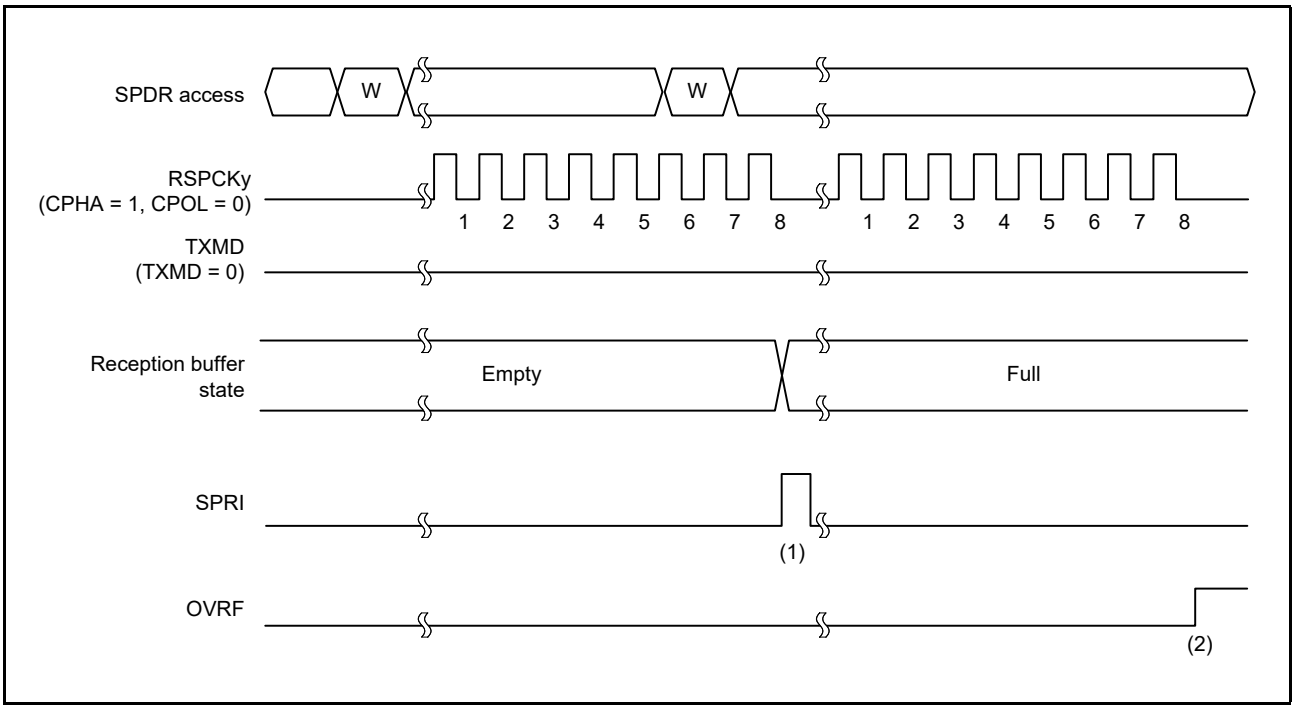


Figure 36.24 Operation Example of SPCR.TXMD = 0

The operation of the flags at timings shown in steps (1) and (2) in the figure is described below.

(1) When a serial transfer ends with the reception buffer of SPDR empty, the RSPI generates a reception buffer full interrupt request (SPRI) and copies the received data in the shift register to the reception buffer.

(2) When a serial transfer ends with the reception buffer of SPDR holding data that was received in the previous serial transfer, the RSPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

36.3.6.2 Transmit Operations Only (SPCR.TXMD = 1)

Figure 36.25 shows an example of operation when the communications operating mode select bit (SPCR.TXMD) is set to 1. In the example in Figure 36.25, the RSPI performs an 8-bit serial transfer in which the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKy waveform represent the number of RSPCK cycles (i.e., the number of transferred bits) (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

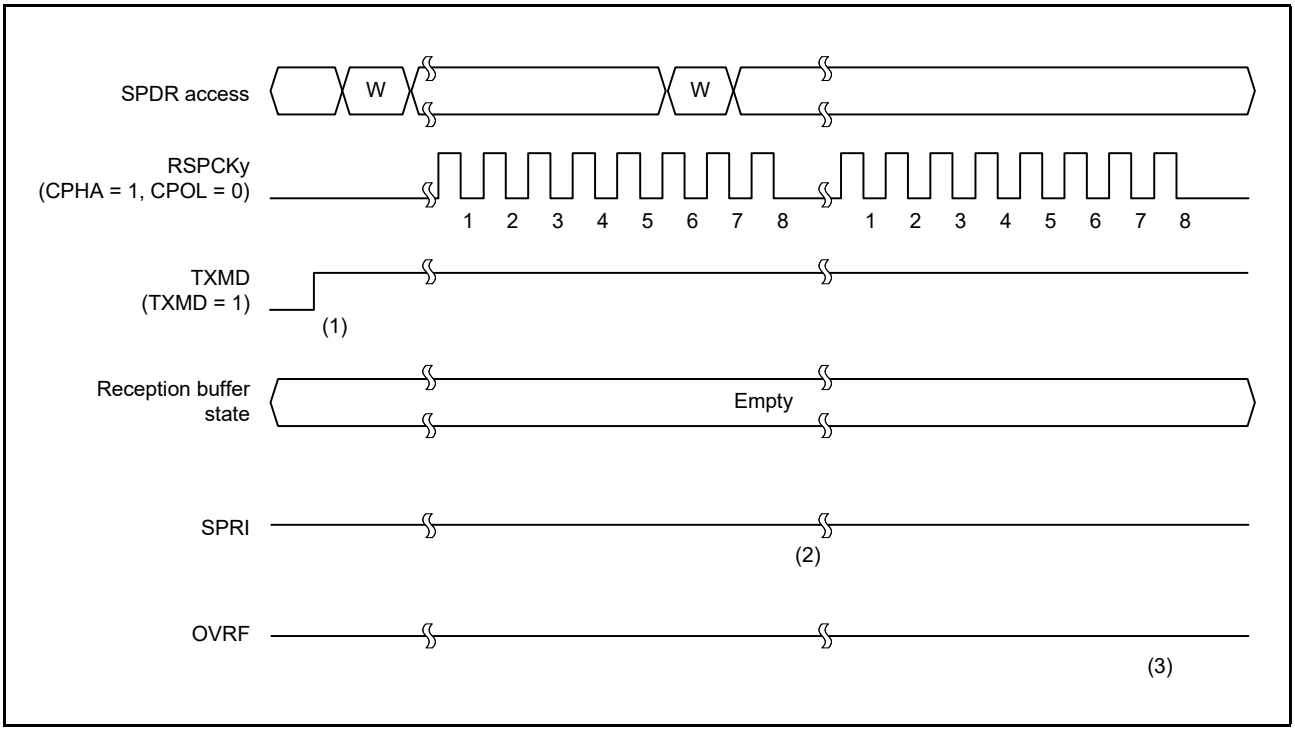


Figure 36.25 Operation Example of SPCR.TXMD = 1

The operation of the flags at timings shown in steps (1) to (3) in the figure is described below.

(1) Make sure there is no data left in the reception buffer and the SPSR.OVRF flag is 0 before entering the mode of transmit operations only (SPCR.TXMD = 1).

(2) When a serial transfer ends with the reception buffer of SPDR empty, if the mode of transmit operations only is selected (SPCR.TXMD = 1), the RSPI does not copy the data in the shift register to the reception buffer.

(3) Since the reception buffer of SPDR does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the reception buffer.

When performing transmit operations only (SPCR.TXMD = 1), the RSPI transmits transmit data but does not receive received data. Therefore, the SPSR.OVRF flag remains 0 at the timings of (1) to (3).

36.3.7 Transmission Buffer Empty/Reception Buffer Full Interrupts

Figure 36.26 shows an example of operation of the transmission buffer empty interrupt (SPTI) and the reception buffer full interrupt (SPRI). The SPDR register access shown in Figure 36.26 indicates the condition of access to the SPDR register, where W denotes a write cycle, and R a read cycle. In the example in Figure 36.26, the RSPI performs an 8-bit serial transfer in which the SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKy waveform represent the number of RSPCK cycles (i.e., the number of transferred bits) (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

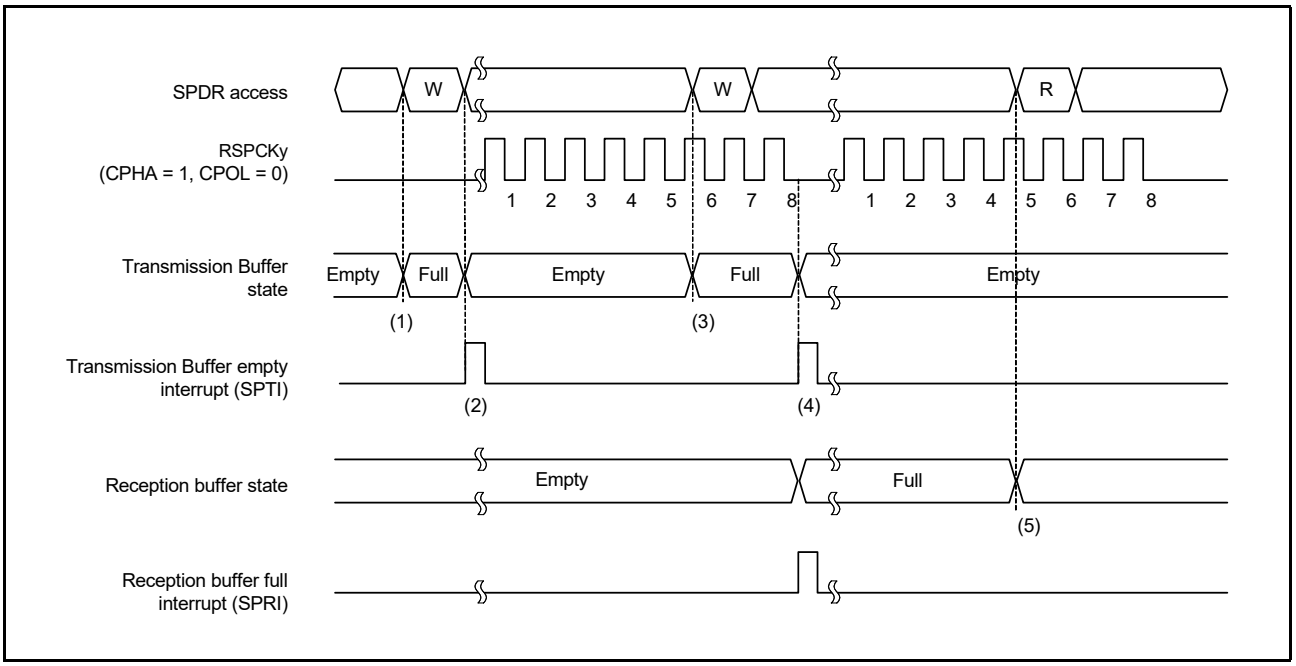


Figure 36.26 Operation Example of Transmission Buffer Empty Interrupt (SPTI) and Reception Buffer Full Interrupt (SPRI)

The operation of the interrupts at timings shown in steps (1) to (5) in the figure is described below.

1. When transmit data is written to SPDR when the transmission buffer of SPDR is empty (data for the next transfer is not set), the RSPI writes data to the transmission buffer.
2. If the shift register is empty, the RSPI copies the data in the transmission buffer to the shift register and generates a transmission buffer empty interrupt request (SPTI). How a serial transfer is started depends on the mode of the RSPI. For details, refer to section 36.3.10, SPI Operation, and section 36.3.11, Clock Synchronous Operation.
3. When transmit data is written to SPDR by the transmission buffer empty interrupt routine, the data is transferred to the transmission buffer. Because the data being transferred serially is stored in the shift register, the RSPI does not copy the data in the transmission buffer to the shift register.
4. When the serial transfer ends with the reception buffer of SPDR being empty, the RSPI copies the receive data in the shift register to the reception buffer and generates a reception buffer full interrupt request (SPRI). Since the shift register becomes empty upon completion of serial transfer, when the transmission buffer had been full before the serial transfer ended, the RSPI copies the data in the transmission buffer to the shift register. Even when received data is not copied from the shift register to the reception buffer in an overrun error status, upon completion of the serial transfer, the RSPI determines that the shift register is empty, thus data transfer from the transmission buffer to the shift register is enabled.
5. When SPDR is read by the reception buffer full interrupt routine, the receive data can be read.

If SPDR is written to when the transmission buffer holds data that has not yet been transmitted, the RSPI does not update the data in the transmission buffer. When writing to SPDR, make sure to use a transmission buffer empty interrupt request. To use a transmission buffer empty interrupt, set the SPTIE bit in SPCR to 1.
If the RSPI function is disabled (the SPCR.SPE bit being 0), set the SPTIE bit to 0.
When serial transfer ends with the reception buffer being full, the RSPI does not copy data from the shift register to the reception buffer, and detects an overrun error (refer to section 36.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a reception buffer full interrupt request before the next serial transfer ends. To use an RSPI reception buffer full interrupt, set the SPCR.SPRIE bit to 1.
For the states of the transmit and reception buffers, transmission buffer empty and reception buffer interrupts or the corresponding IRQ status register (IRQSn) can be used to confirm the generation of interrupt requests. For the IRQ status register (IRQSn), see section 12.4.2.1, IRQ Status Register n (IRQSn) (n = 0 to 9).

36.3.8 Error Detection

In the normal RSPI serial transfer, the data written to the transmission buffer of SPDR is transmitted, and the received data can be read from the reception buffer of SPDR. If access is made to SPDR, depending on the status of the transmission/reception buffer or the status of the RSPI at the beginning or end of serial transfer, in some cases non-normal transfers can be executed.
If a non-normal transfer operation occurs, the RSPI detects the event as an overrun error, parity error, or mode fault error. Table 36.8 lists the relationship between non-normal transfer operations and the RSPI's error detection function.

Table 36.8 Relationship between Non-Normal Transfer Operations and RSPI Error Detection Function

	Occurrence Condition	RSPI Operation	Error Detection
1	SPDR is written when the transmission buffer is full.	• The contents of the transmission buffer are kept. • Missing write data.	None
2	Serial transfer is started in slave mode when transmit data is still not loaded on the shift register.	Data received in previous serial transfer is transmitted.	None
3	SPDR is read when the reception buffer is empty.	Previously received data is output.	None
4	Serial transfer terminates when the reception buffer is full.	• The contents of the reception buffer are kept. • Missing receive data.	Overrun error
5	An incorrect parity bit is received when performing full-duplex synchronous serial communications with the parity function enabled.	The parity error flag is asserted.	Parity error
6	The SSLy0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Driving of the RSPCKy, MOSIy, SSLy1 to SSLy3 output signals is stopped. • RSPI function is disabled.	Mode fault error
7	The SSLy0 input signal is asserted during serial transfer in multi-master mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the RSPCKy, MOSIy, SSLy1 to SSLy3 output signals is stopped. • RSPI function is disabled.	Mode fault error
8	The SSLy0 input signal is negated during serial transfer in slave mode.	• Serial transfer is suspended. • Missing transmit/receive data. • Driving of the MISOy output signal is stopped. • RSPI function is disabled.	Mode fault error

y = 0, 1, 2, 3 (for all channels)

On operation 1 described in Table 36.8, the RSPI does not detect an error. To prevent data omission during the writing to SPDR, write operations to SPDR should be executed using a transmission buffer empty interrupt request.
Likewise, the RSPI does not detect an error on operation 2. In a serial transfer that was started before the shift register was updated, the RSPI sends the data that was received in the previous serial transfer, and does not treat the operation indicated in 2 as an error. Note that the received data from the previous serial transfer is retained in the reception buffer of SPDR, thus it can be correctly read (if SPDR is not read before the end of the serial transfer, an overrun error may occur).
Similarly, the RSPI does not detect an error on operation 3. To prevent extraneous data from being read, SPDR read operation should be executed using an RSPI reception buffer full interrupt request.
An overrun error shown in 4 is described in section 36.3.8.1, Overrun Error. A parity error shown in 5 is described in section 36.3.8.2, Parity Error. A mode fault error shown in 6 to 8 is described in section 36.3.8.3, Mode Fault Error. For the transmit and receive interrupts, refer to section 36.3.7, Transmission Buffer Empty/Reception Buffer Full Interrupts.

36.3.8.1 Overrun Error

If a serial transfer ends when the reception buffer of SPDR is full, the RSPI detects an overrun error, and sets the OVRF flag in SPSR to 1. When the OVRF flag is 1, the RSPI does not copy data from the shift register to the reception buffer so that the data prior to the occurrence of the error is retained in the reception buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU has read SPSR with the OVRF flag set to 1.

Figure 36.27 shows an example of operation of the OVRF flag. The SPSR and SPDR accesses shown in Figure 36.27 indicate the condition of accesses to SPSR and SPDR, respectively, where W denotes a write cycle, and R a read cycle. In the example in Figure 36.27, the RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKy waveform represent the number of RSPCK cycles (i.e., the number of transferred bits) (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

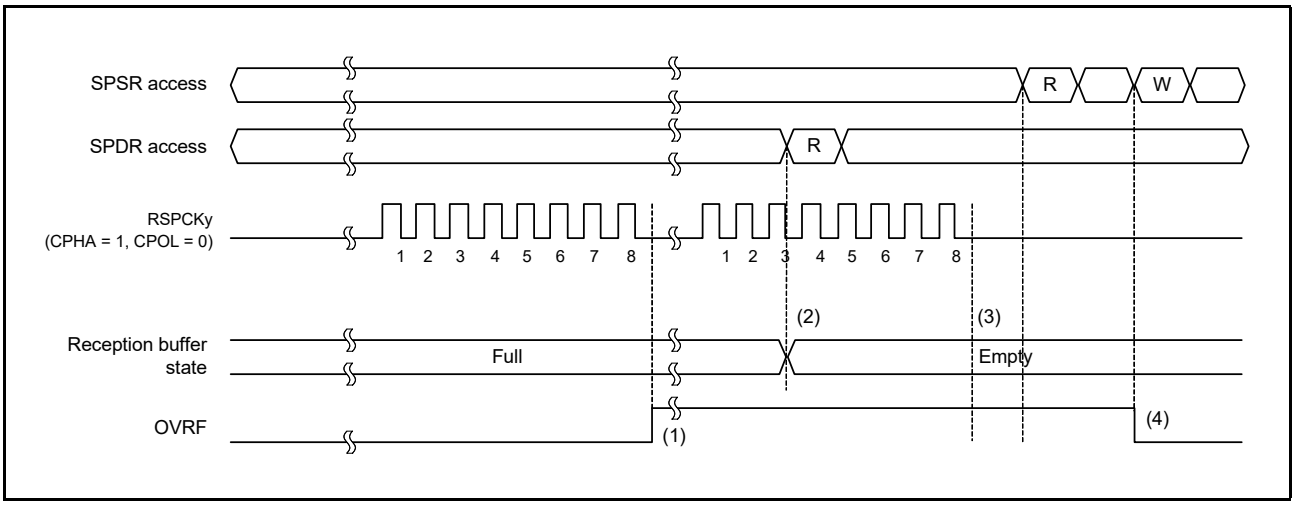


Figure 36.27 Operation Example of OVRF Flag

The operation of the flags at the timing shown in steps (1) to (4) in the figure is described below.

1. If a serial transfer terminates with the reception buffer full, the RSPI detects an overrun error, and sets the OVRF flag to 1. The RSPI does not copy the data in the shift register to the reception buffer. Even if the SPPE bit is 1, parity errors are not detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.
2. When SPDR is read, the RSPI can read the data in the reception buffer. The reception buffer becoming empty does not set the OVRF flag to 0.
3. If the serial transfer ends with the OVRF flag being 1 (an overrun error occurs), the RSPI does not copy the data in the shift register to the reception buffer. A reception-buffer interrupt is not generated. Even if the SPPE bit is 1, parity errors are not detected. When in master mode, the RSPI does not update the SPSSR.SPECM[2:0] bits. When in an overrun error state and the RSPI does not copy the received data from the shift register to the reception buffer, upon termination of the serial transfer, the RSPI determines that the shift register is empty; in this manner, data transfer from the transmission buffer to the shift register is enabled.
4. If the value 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag is set to 0.

The occurrence of an overrun can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. When executing a serial transfer, measures should be taken to ensure the early detection of overrun errors, such as reading SPSR immediately after SPDR is read. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

If an overrun error occurs and the OVRF flag is set to 1, normal reception operations cannot be performed until the OVRF flag is set to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 36.28 and Figure 36.29 show the clock stop waveform when a serial transfer continues while the reception buffer is full in master mode.

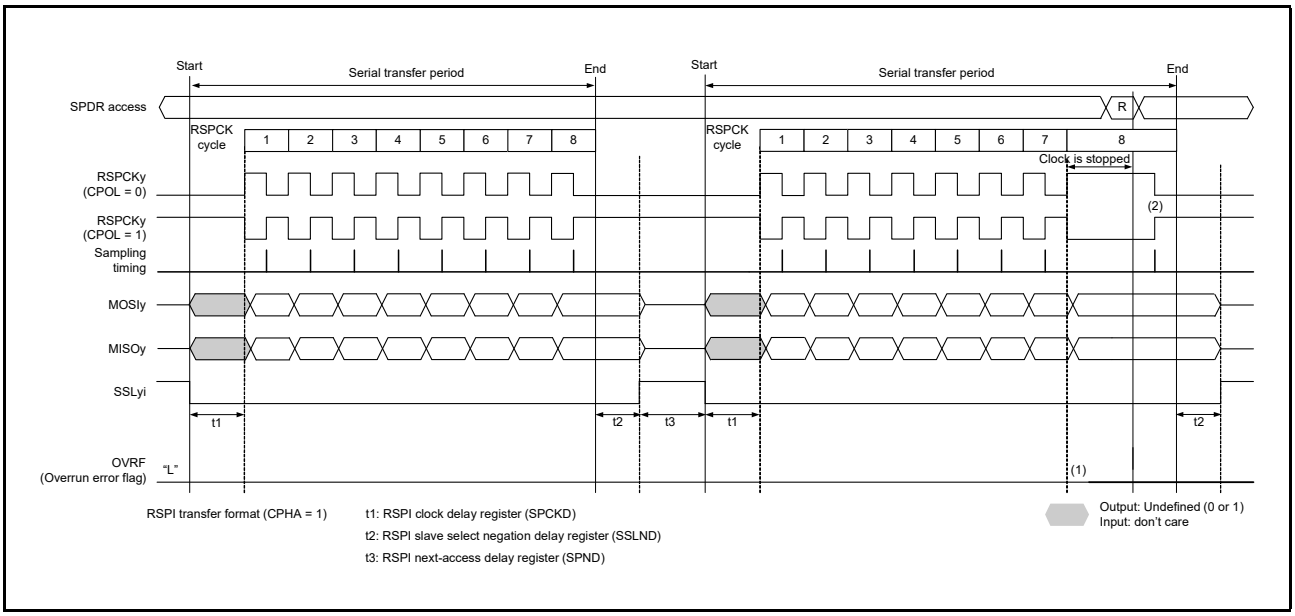


Figure 36.28 Clock Stop Waveform When a Serial Transfer Continues While the Reception Buffer is Full in Master Mode (CPHA = 1)

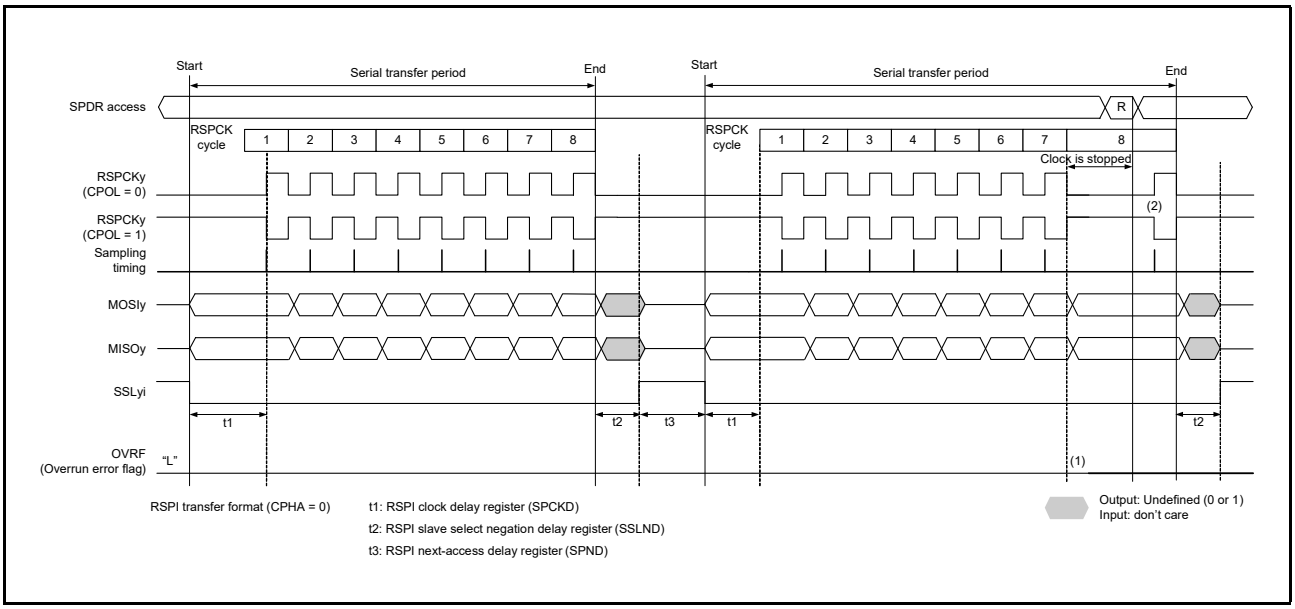


Figure 36.29 Clock Stop Waveform When a Serial Transfer Continues While the Reception Buffer is Full in Master Mode (CPHA = 0)

The operation of the flags at the timings shown in steps (1) and (2) in the figure is described below.

(1) When the reception buffer is full, an overrun error to stop the reception buffer does not occur.

(2) If SPDR is read while the clock is stopped, data in the reception buffer can be read. The RSPCK clock restarts after reading the reception buffer.

36.3.8.2 Parity Error

If full-duplex synchronous serial communications is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, when serial transfer ends, the RSPI checks whether there are parity errors. Upon detecting a parity error in the received data, the RSPI sets the SPSR.PERF flag to 1. Since the RSPI does not copy the data in the shift register to the reception buffer when the SPSR.OVRF flag is set to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after SPSR register is read with the PERF flag set to 1.
Figure 36.30 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 36.30 indicates the condition of access to SPSR register, where W denotes a write cycle, and R a read cycle. In the example of Figure 36.30, full-duplex synchronous serial communications is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The RSPI performs an 8-bit serial transfer in which the SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given under the RSPCKy waveform represent the number of RSPCK cycles (i.e., the number of transferred bits) (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

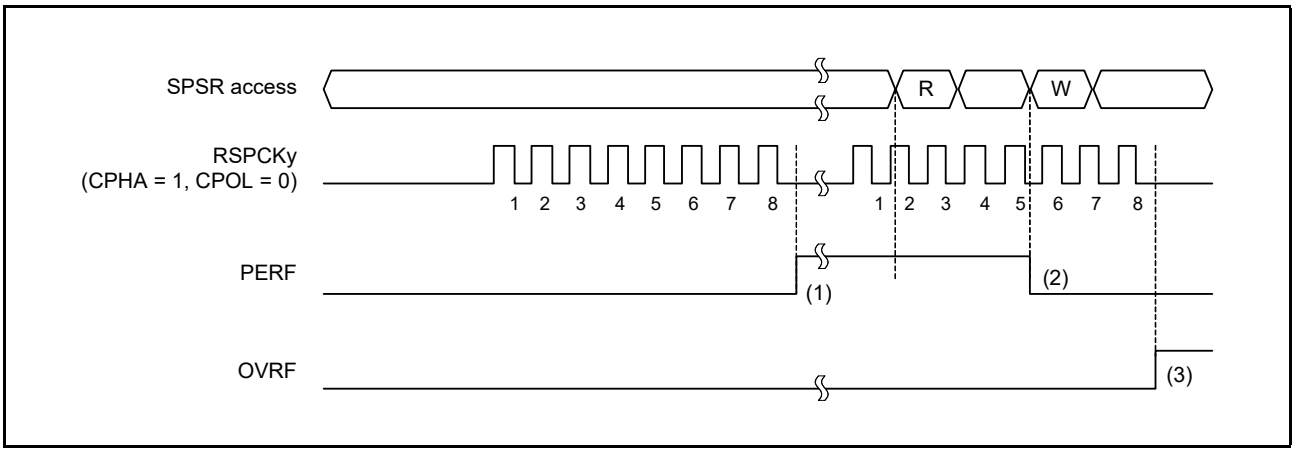


Figure 36.30 Operation Example of PERF Flag

The operation of the flags at the timing shown in steps (1) to (3) in the figure is described below.

1. If a serial transfer terminates with the RSPI not detecting an overrun error, the RSPI copies the data in the shift register to the reception buffer. The RSPI judges the received data at this timing, and sets the PERF flag to 1 if a parity error is detected. In master mode, the RSPI copies the pointer value to SPCMDm register to the SPSSR.SPECM[2:0] bits.
2. If the value 0 is written to the PERF flag after SPSR register is read when the PERF flag is 1, the PERF flag is set to 0.
3. When the RSPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the reception buffer. The RSPI does not perform parity error detection at this timing.

The occurrence of a parity error can be checked either by reading SPSR register or by using an RSPI error interrupt and reading SPSR register. When executing a serial transfer, measures should be taken to ensure the early detection of parity errors, such as reading SPSR. When the RSPI is used in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

36.3.8.3 Mode Fault Error

The RSPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input with respect to the SSLy0 input signal of the RSPI in multi-master mode, the RSPI detects a mode fault error irrespective of the status of the serial transfer, and sets the MODF bit in the RSPI status register (SPSR) to 1. Upon detecting the mode fault error, the RSPI copies the value of the pointer to SPCMDm to the SPSSR.SPECM[2:0] bits. The active level of the SSLy0 signal is determined by the SSL0P bit in the RSPI slave select polarity register (SSLP).

When the MSTR bit is 0, the RSPI operates in slave mode. The RSPI detects a mode fault error if the MODFEN bit in the RSPI in slave mode is 1, and the SPMS bit is 0, and if the SSLy0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

Upon detecting a mode fault error, the RSPI stops driving of the output signals and clears the SPCR.SPE bit to 0 (refer to section 36.3.9, Initializing RSPI). In the case of multi-master configuration, detection of a mode fault error is used to stop driving of the output signals and the RSPI function, which allows the master right to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an RSPI error interrupt and reading SPSR. Detecting mode-fault errors without utilizing the RSPI error interrupt requires polling of SPSR. When using the RSPI in master mode, the pointer value to SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF bit is 1, writing of the value 1 to the SPE bit is ignored by the RSPI. To enable the RSPI function after the detection of a mode fault error, the MODF bit must be set to 0 (m = 0 to 7; y = 0, 1, 2, 3 (for all channels)).

36.3.9 Initializing RSPI

If the value 0 is written to the SPCR.SPE bit or the RSPI sets the SPE bit to 0 because of the detection of a mode fault error, the RSPI disables the RSPI function, and initializes some of the module functions. When a system reset is generated, the RSPI initializes all of the module functions. The following describes initialization by the clearing of the SPCR.SPE bit and initialization by a system reset.

36.3.9.1 Initialization by Clearing the SPE Bit

When the SPCR.SPE bit is set to 0, the RSPI performs the following initialization:

- Suspending any serial transfer that is being executed
- Stopping the driving of output signals (Hi-Z) in slave mode
- Initializing the internal state of the RSPI
- Initializing the transmission buffer of the RSPI

Initialization by the clearing of the SPE bit does not initialize the control bits of the RSPI. For this reason, the RSPI can be started in the same transfer mode as prior to the initialization if the SPE bit is set to 1 again.
The SPSR.OVRF and SPSR.MODF flags are not initialized, nor is the value of the RSPI sequence status register (SPSSR) initialized. For this reason, even after the RSPI is initialized, data from the reception buffer can be read in order to check the status of error occurrence during an RSPI transfer.
The transmission buffer is initialized to an empty state. Therefore, if the SPCR.SPTIE bit is set to 1 after RSPI initialization, a transmission buffer empty interrupt is generated. When the RSPI is initialized, in order to disable any transmission buffer empty interrupt, the value 0 should be written to the SPTIE bit simultaneously with the writing of the value 0 to the SPE bit. To disable any transmission buffer empty interrupt after a mode fault error is detected, use an error handling routine to write the value 0 to the SPTIE bit.

36.3.9.2 System Reset

The initialization by a system reset completely initializes the RSPI through the initialization of all bits for controlling the RSPI, initialization of the status bits, and initialization of data registers, in addition to the requirements described in section 36.3.9.1, Initialization by Clearing the SPE Bit. For details, see section 6, Reset.

36.3.10 SPI Operation

36.3.10.1 Master Mode Operation

The only difference between single-master mode operation and multi-master mode operation lies in mode fault error detection (refer to section 36.3.8, Error Detection). When operating in single-master mode, the RSPI does not detect mode fault errors whereas the RSPI running in multi-master mode does detect mode fault errors. This section explains operations that are common to single-master mode and multi-master mode.

(1) Starting a Serial Transfer

The RSPI updates the data in the transmission buffer (SPTX) when data is written to the RSPI data register (SPDR) with the RSPI transmission buffer being empty (data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmission buffer to the shift register and starts serial transfer. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format. The polarity of the SSLyi output pins depends on the SSLP register settings (i = 0 to 3; y = 0, 1, 2, 3 (for all channels)).

(2) Terminating a Serial Transfer

Irrespective of the SPCMDm.CPHA bit the RSPI terminates the serial transfer after transmitting an RSPCKy edge corresponding to the final sampling timing. If free space is available in the reception buffer (SPRX), upon termination of serial transfer, the RSPI copies data from the shift register to the reception buffer of the RSPI data register (SPDR).
It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLyi output pin depends on the SSLP register settings. For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format.
(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

(3) Sequence Control

The transfer format that is employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLyi pin output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCK polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.

According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0, and in this manner the sequence is executed repeatedly.

(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

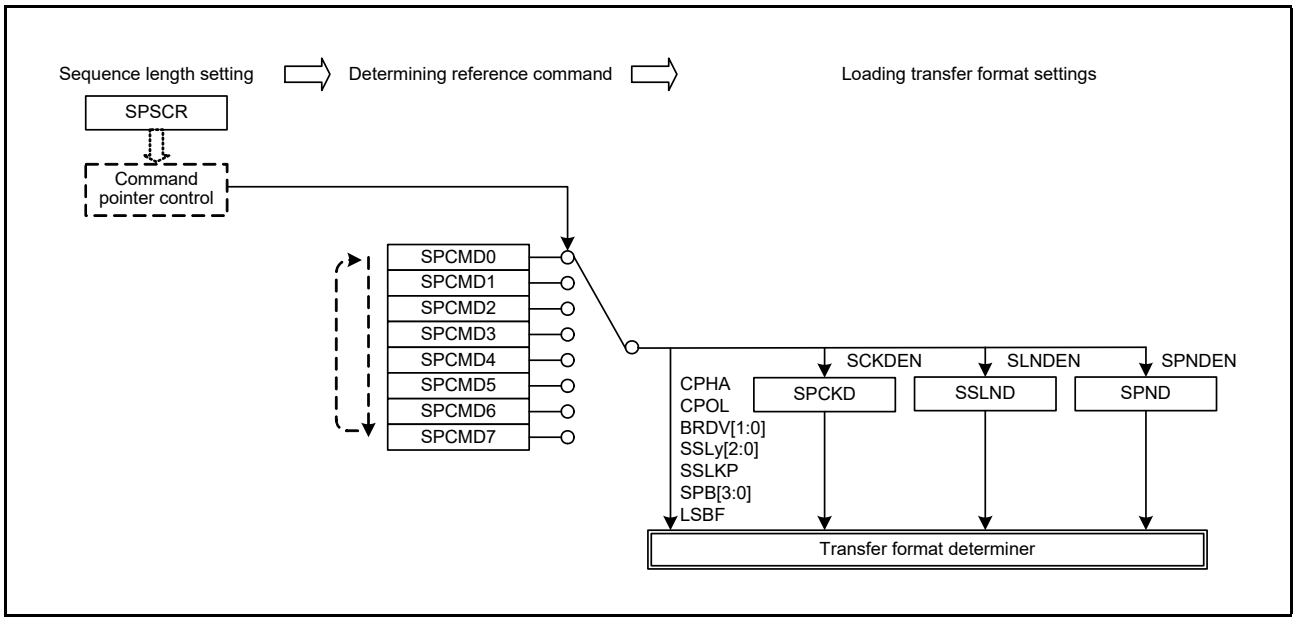


Figure 36.31 Procedure for Determining the Form of Serial Transfer in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm).

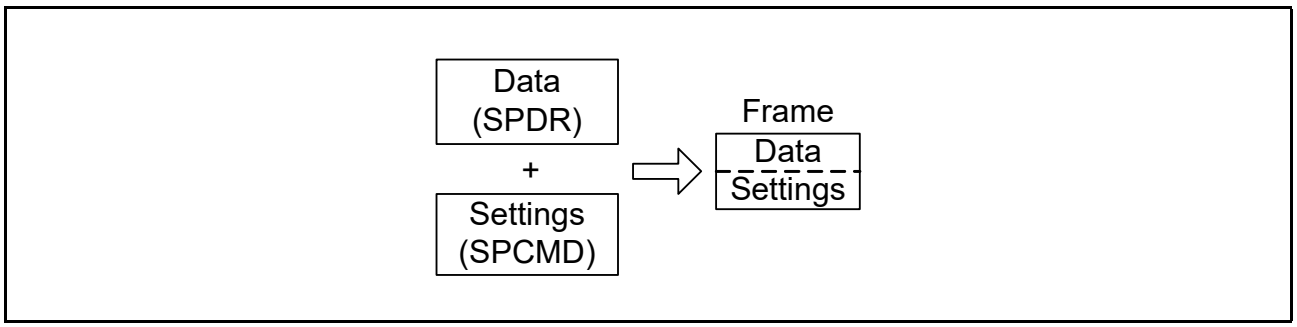


Figure 36.32 Concept of a Frame

Figure 36.33 shows the relationship between the command and the transmit and reception buffers in the sequence of operations specified by the settings in Table 36.4.

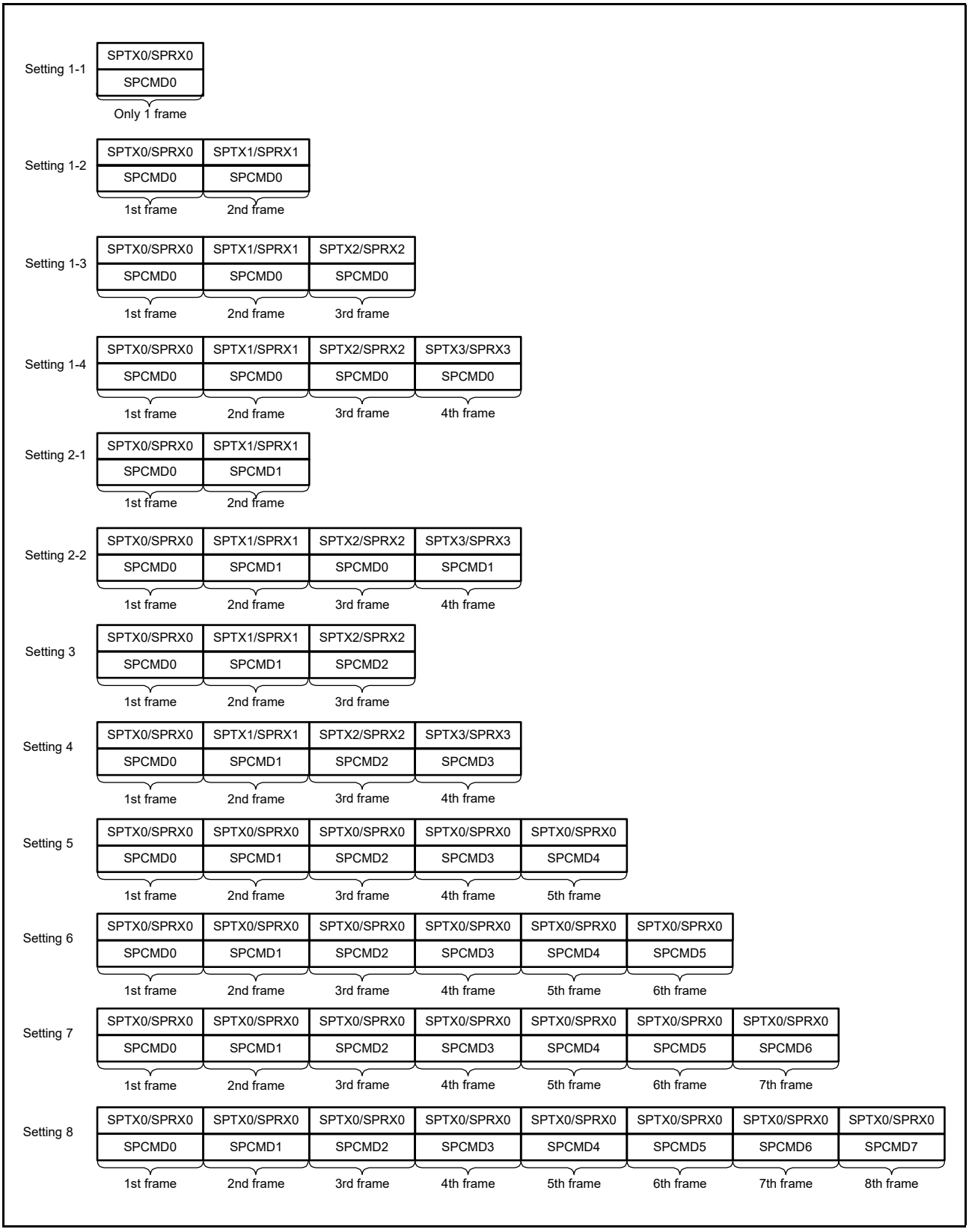


Figure 36.33 Correspondence between the RSPI Command Register and Transmission/Reception Buffers in Sequence Operations

(4) Burst Transfer

If the SPCMDm.SSLKP bit that the RSPI references during the current serial transfer is 1, the RSPI keeps the SSLyi signal level during the serial transfer until the beginning of the SSLyi signal assertion for the next serial transfer. If the SSLyi signal level for the next serial transfer is the same as the SSLyi signal level for the current serial transfer, the RSPI can execute continuous serial transfers while keeping the SSLyi signal assertion status (burst transfer).
Figure 36.34 shows an example of an SSLyi signal operation for the case where a burst transfer is implemented using SPCMD0 and SPCMD1 register settings. The text below explains the RSPI operations (1) to (7) as shown in Figure 36.34. It should be noted that the polarity of the SSLyi output signal depends on the SSLP register settings.

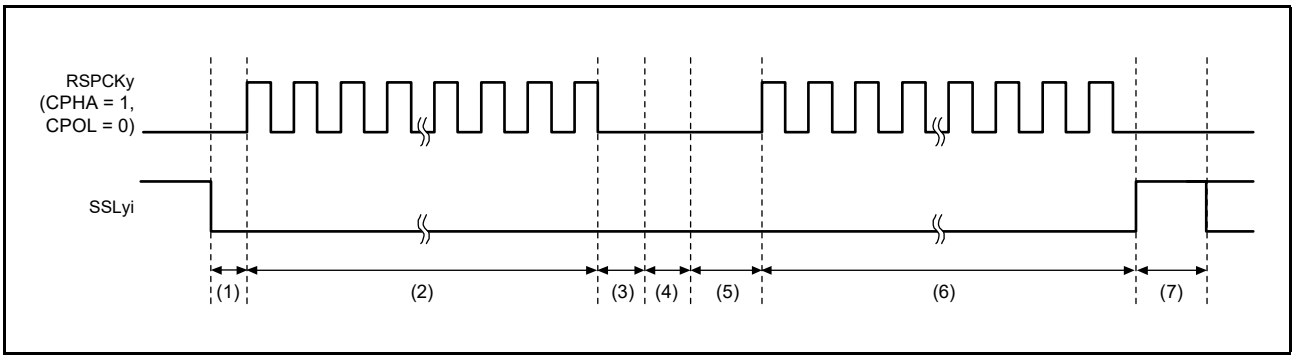


Figure 36.34 Example of Burst Transfer Operation Using SSLKP Bit

(1) Based on SPCMD0, the RSPI asserts the SSLyi signal and inserts RSPCK delays.
(2) The RSPI executes serial transfers according to SPCMD0.
(3) The RSPI inserts SSL negation delays.
(4) Since the SPCMD0.SSLKP bit is 1, the RSPI keeps the SSLyi signal value on SPCMD0. This period is sustained, at the shortest, for a period equal to the next-access delay of SPCMD0. If the shift register is empty after the passage of a minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
(5) Based on SPCMD1, the RSPI asserts the SSLyi signal and inserts RSPCK delays.
(6) The RSPI executes serial transfers according to SPCMD1.
(7) Because the SPCMD1.SSLKP bit is 0, the RSPI negates the SSLyi signal. In addition, a next-access delay is inserted according to SPCMD1.

If the SSLyi signal output settings in the SPCMDm register in which 1 is assigned to the SSLKP bit are different from the SSLyi signal output settings in the SPCMDm register to be used in the next transfer, the RSPI switches the SSLyi signal status to SSLyi signal assertion ((5) in Figure 36.34) corresponding to the command for the next transfer. Note that if such an SSLyi signal switching occurs, the slaves that drive the MISOy signal compete, and collision of signal levels may occur.
The RSPI in master mode references the SSLyi signal operation within the module for the case where the SSLKP bit is not used. Even when the SPCMDm.CPHA bit is 0, the RSPI can accurately start serial transfers by using the SSLyi signal assertion for the next transfer that is detected internally.
(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

(5) RSPCK Delay (t1)

The RSPCK delay value of the RSPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an RSPCK delay value during serial transfer by using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 36.9. For a definition of RSPCK delay, refer to section 36.3.5, Transfer Format.

Table 36.9 Relationship among SCKDEN Bit, SPCKD, and RSPCK Delay Value

SPCMDm.SCKDEN Bit	SPCKD.SCKDL[2:0] Bits	RSPCK Delay Value
0	000 to 111	1 RSPCK
1	000	1 RSPCK
	001	2 RSPCK
	010	3 RSPCK
	011	4 RSPCK
	100	5 RSPCK
	101	6 RSPCK
	110	7 RSPCK
	111	8 RSPCK

(6) SSL Negation Delay (t2)

The SSL negation delay value of the RSPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines an SSL negation delay value during serial transfer by using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 36.10. For a definition of SSL negation delay, refer to section 36.3.5, Transfer Format.

Table 36.10 Relationship among SLNDEN Bit, SSLND, and SSL Negation Delay Value

SPCMDm.SLNDEN Bit	SSLND.SLNDL[2:0] Bits	SSL Negation Delay Value
0	000 to 111	1 RSPCK
1	000	1 RSPCK
	001	2 RSPCK
	010	3 RSPCK
	011	4 RSPCK
	100	5 RSPCK
	101	6 RSPCK
	110	7 RSPCK
	111	8 RSPCK

(7) Next-Access Delay (t3)

The next-access delay value of the RSPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND setting. The RSPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines a next-access delay value during serial transfer by using the SPCMDm.SPNDEN bit and SPND, as listed in Table 36.11. For a definition of next-access delay, refer to section 36.3.5, Transfer Format.

Table 36.11 Relationship among SPNDEN Bit, SPND, and Next-Access Delay Value

SPCMDm.SPNDEN Bit	SPND.SPNDL[2:0] Bits	Next-Access Delay Value
0	000 to 111	1 RSPCK + 2 SERICLK
1	000	1 RSPCK + 2 SERICLK
	001	2 RSPCK + 2 SERICLK
	010	3 RSPCK + 2 SERICLK
	011	4 RSPCK + 2 SERICLK
	100	5 RSPCK + 2 SERICLK
	101	6 RSPCK + 2 SERICLK
	110	7 RSPCK + 2 SERICLK
	111	8 RSPCK + 2 SERICLK

(8) Initialization Flowchart

Figure 36.35 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, refer to the descriptions given in the individual blocks.

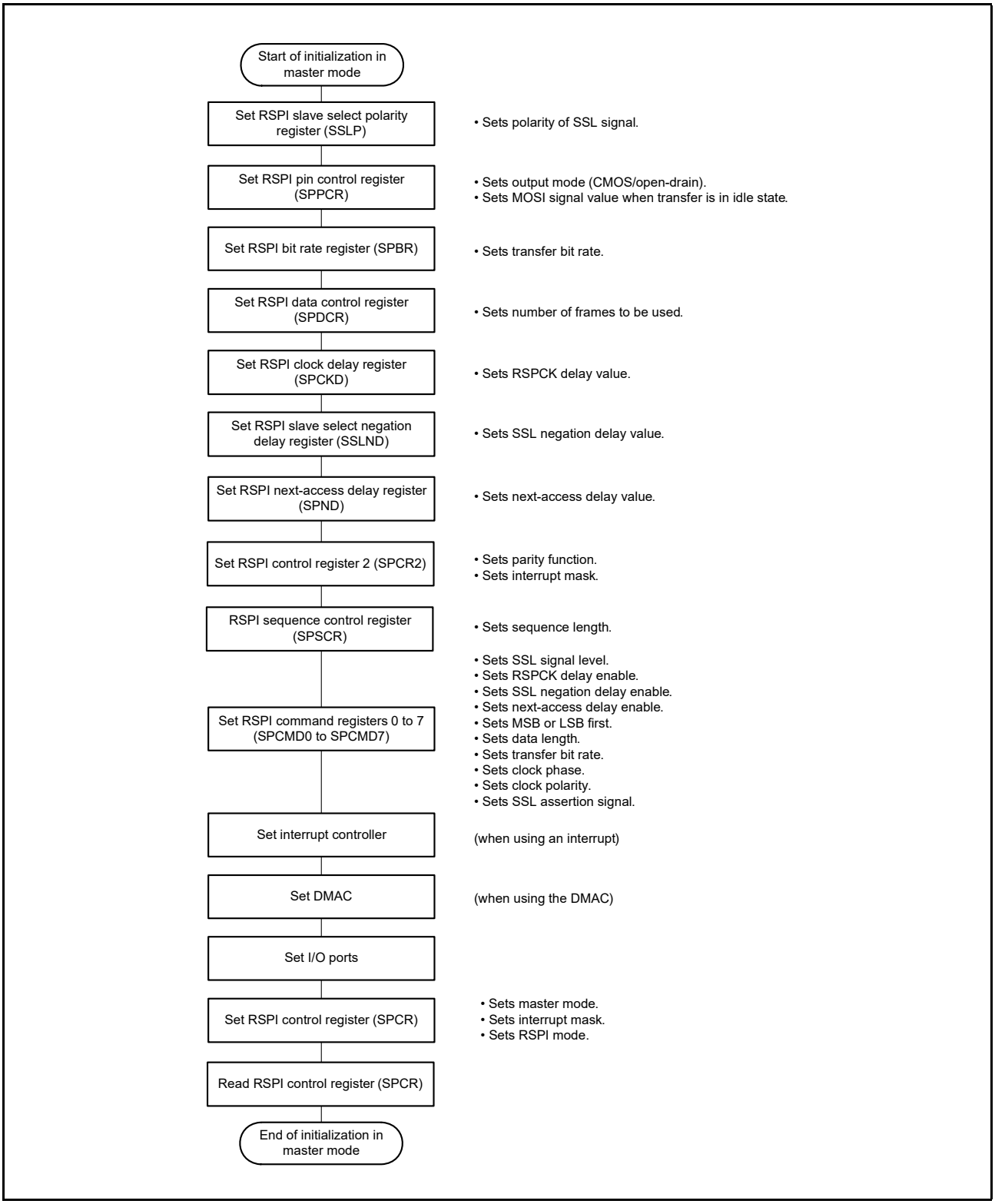


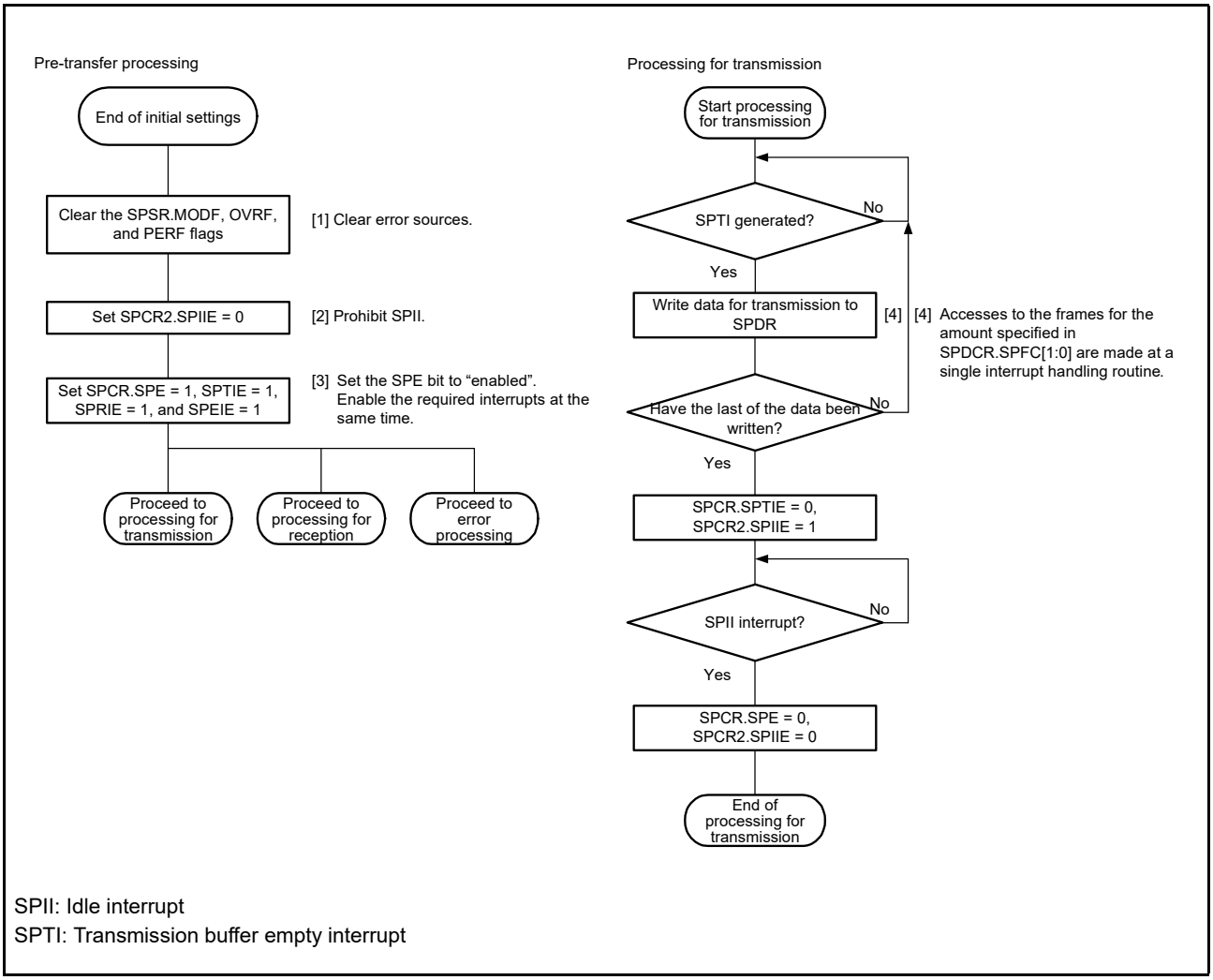
Figure 36.35 Example of Initialization Flowchart in Master Mode (SPI Operation)

(9) Software Processing Flow

Figure 36.36 to Figure 36.38 show examples of the flow of software processing.

(a) Transmit Processing Flow

When transmitting data, the CPU will be notified of the completion of data transmission after the last writing of data for transmission if the idle interrupt (SPII) is enabled.



SPII: Idle interrupt
SPTI: Transmission buffer empty interrupt

Figure 36.36 Flowchart in Master Mode (Transmission)

(b) Receive Processing Flow

The RSPI does not handle receive-only operation, so processing for transmission is required if reception is to proceed.

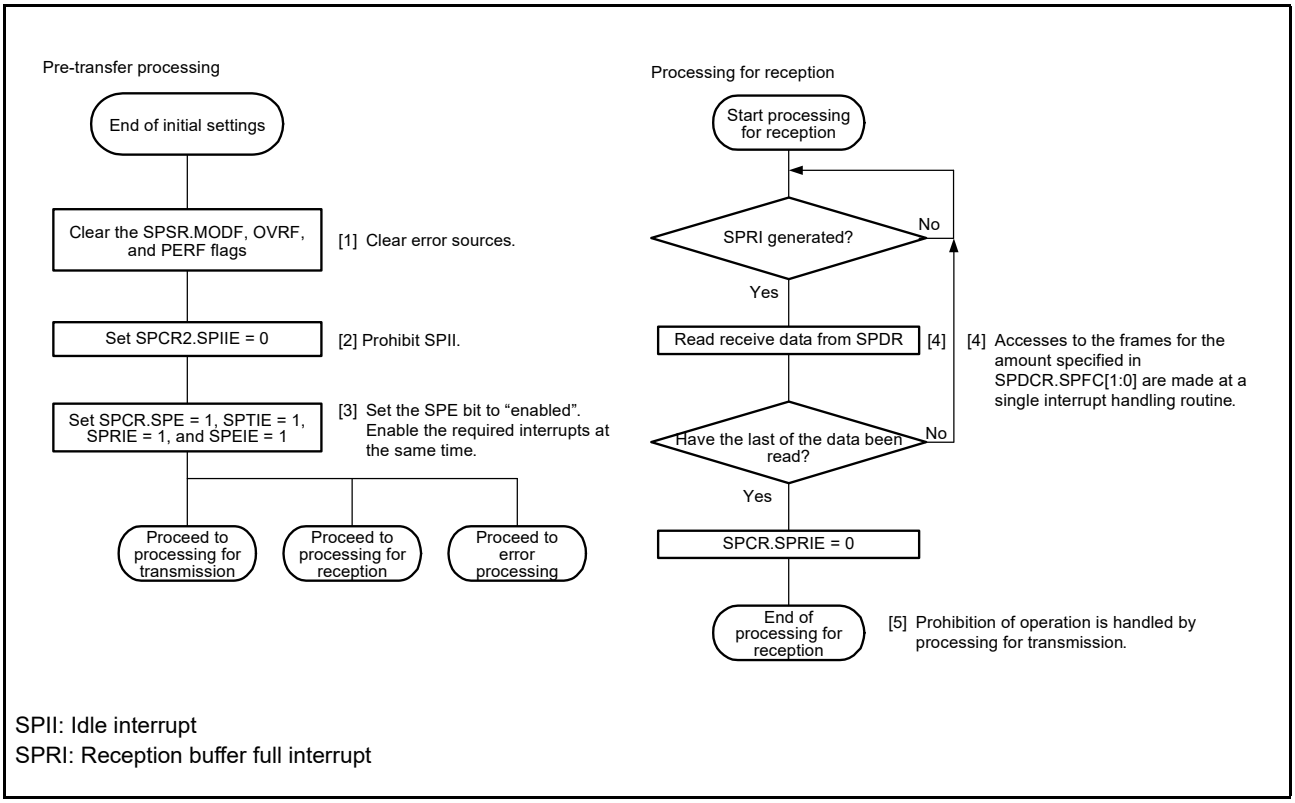
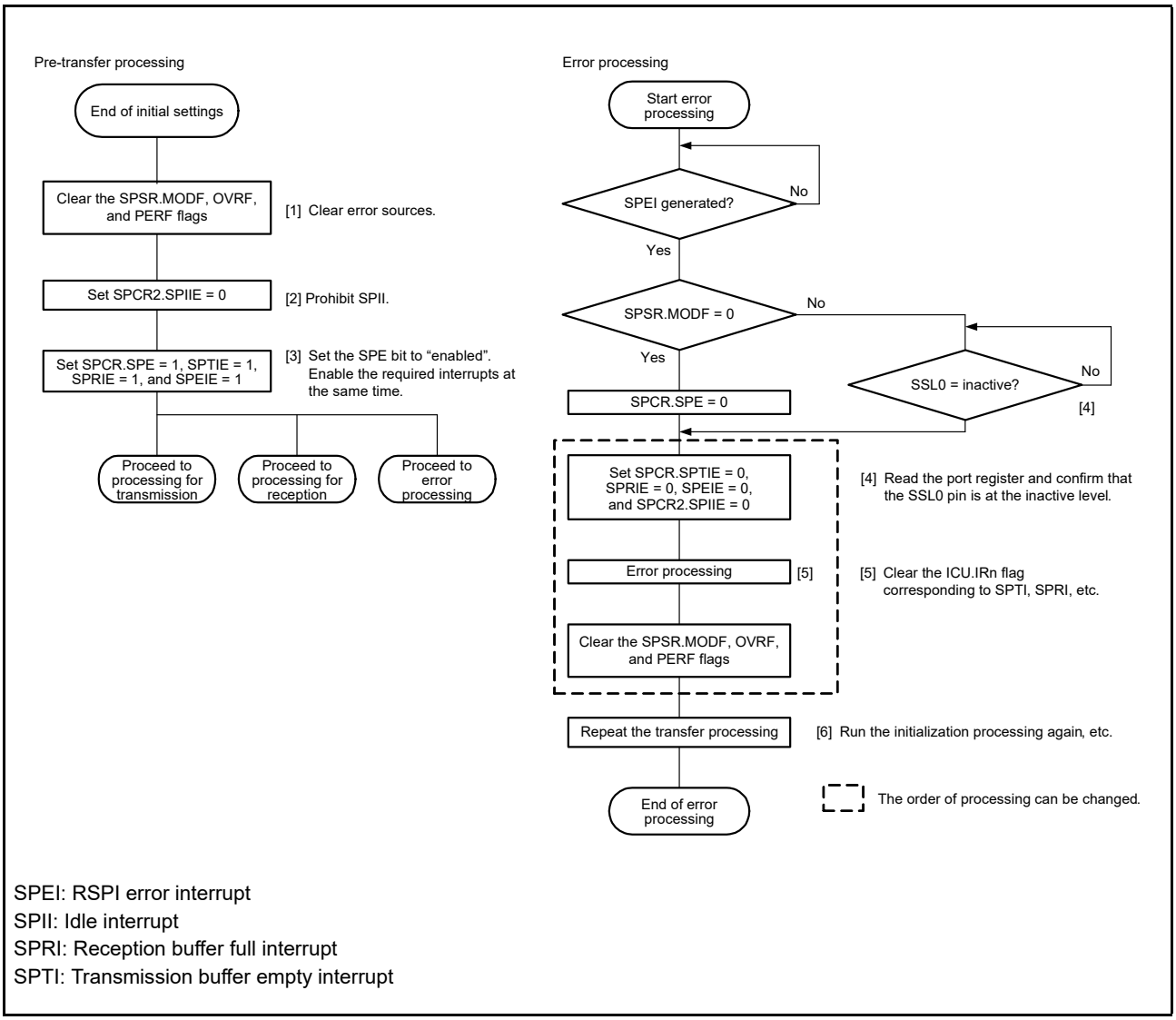


Figure 36.37 Flowchart in Master Mode (Reception)

(c) Flow of error processing

The RSPI has three types of error. When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, however, the SPCR.SPE bit is not cleared and operations for transmission and reception continue; accordingly, we recommend clearing of the SPCR.SPE bit to stop operations in the case of errors other than mode-fault errors. Not doing so will lead to updating of the SPSSR.SPECM[2:0] bits.

When an error occurs, clear the corresponding flag of the IRQ status register from within the error processing routine. If this is not done, the corresponding interrupt request flag in the IRQ status register may continue to indicate a transmission buffer empty interrupt (SPTI) or reception buffer full interrupt (SPRI) request. If the reception buffer full interrupt (SPRI) request is indicated, read the reception buffer and initialize the sequencer in the RSPI.



SPEI: RSPI error interrupt
SPII: Idle interrupt
SPRI: Reception buffer full interrupt
SPTI: Transmission buffer empty interrupt

Figure 36.38 Flowchart for Master Mode (Error Processing)

36.3.10.2 Slave Mode Operation

(1) Starting a Serial Transfer

If the SPCMD0.CPHA bit is 0, when detecting an SSLy0 input signal assertion, the RSPI needs to start driving valid data to the MISOy output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLy0 input signal triggers the start of a serial transfer.
If the CPHA bit is 1, when detecting the first RSPCKy edge in an SSLy0 signal asserted condition, the RSPI needs to start driving valid data to the MISOy output signal. For this reason, when the CPHA bit is 1, the first RSPCKy edge in an SSLy0 signal asserted condition triggers the start of a serial transfer.
When detecting the start of a serial transfer in a condition in which the shift register is empty, the RSPI changes the status of the shift register to “full”, so that data cannot be copied from the transmission buffer to the shift register when serial transfer is in progress. If the shift register was full before the serial transfer started, the RSPI leaves the status of the shift register unchanged, in the full state.
Irrespective of CPHA bit setting, the timing at which the RSPI starts driving of the MISOy output signal is the SSLy0 signal assertion timing. The data which is output by the RSPI is either valid or invalid, depending on the CPHA bit setting.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format. The polarity of the SSLy0 input signal depends on the setting of the SSLP.SSL0P bit.
(y = 0, 1, 2, 3 (for all channels))

(2) Terminating a Serial Transfer

Irrespective of the SPCMD0.CPHA bit, the RSPI terminates the serial transfer after detecting an RSPCKy edge corresponding to the final sampling timing. When free space is available in the reception buffer, upon termination of serial transfer the RSPI copies received data from the shift register to the reception buffer of the RSPI data register (SPDR). Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty”, regardless of the reception buffer state. A mode fault error occurs if the RSPI detects an SSLy0 input signal negation from the beginning of serial transfer to the end of serial transfer (refer to section 36.3.8, Error Detection).
The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLy0 input signal depends on the SSLP.SSL0P bit setting.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format.
(y = 0, 1, 2, 3 (for all channels))

(3) Notes on Single-Slave Operations

If the SPCMD0.CPHA bit is 0, the RSPI starts serial transfers when it detects the assertion edge for an SSLy0 input signal. In the type of configuration shown in Figure 36.7 as an example, if the RSPI is used in single-slave mode, the SSLy0 signal is always fixed at the active state. Therefore, when the CPHA bit is set to 0, the RSPI cannot correctly start a serial transfer. To correctly execute transmit/receive operations by the RSPI in slave mode in a configuration in which the SSLy0 input signal is fixed at the active state, the CPHA bit should be set to 1. If there is a need for setting the CPHA bit to 0, the SSLy0 input signal should not be fixed.
(y = 0, 1, 2, 3 (for all channels))

(4) Burst Transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLy0 input signal. If the CPHA bit is 1, the period from the first RSPCKy edge to the sampling timing for the reception of the final bit in an SSLy0 signal active state corresponds to a serial transfer period. Even when the SSLy0 input signal remains at the active level, the RSPI can accommodate burst transfers because it can detect the start of an access.

If the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization Flowchart

Figure 36.39 is a flowchart illustrating an example of initialization in SPI operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, refer to the descriptions given in the individual blocks.

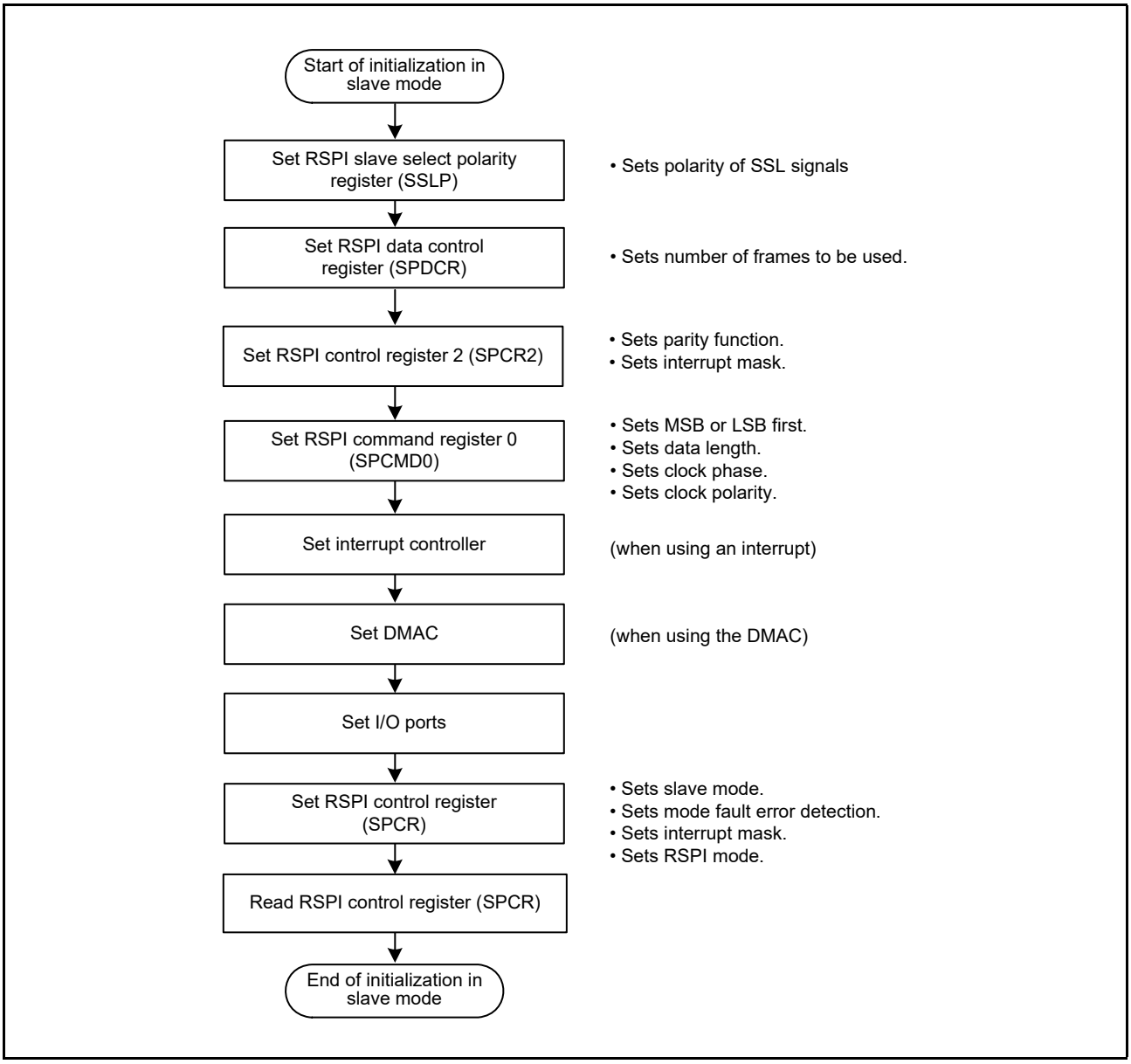


Figure 36.39 Example of Initialization Flowchart in Slave Mode (SPI Operation)

(6) Software Processing Flow

Figure 36.40 to Figure 36.42 show examples of the flow of software processing.

(a) Transmit Processing Flow

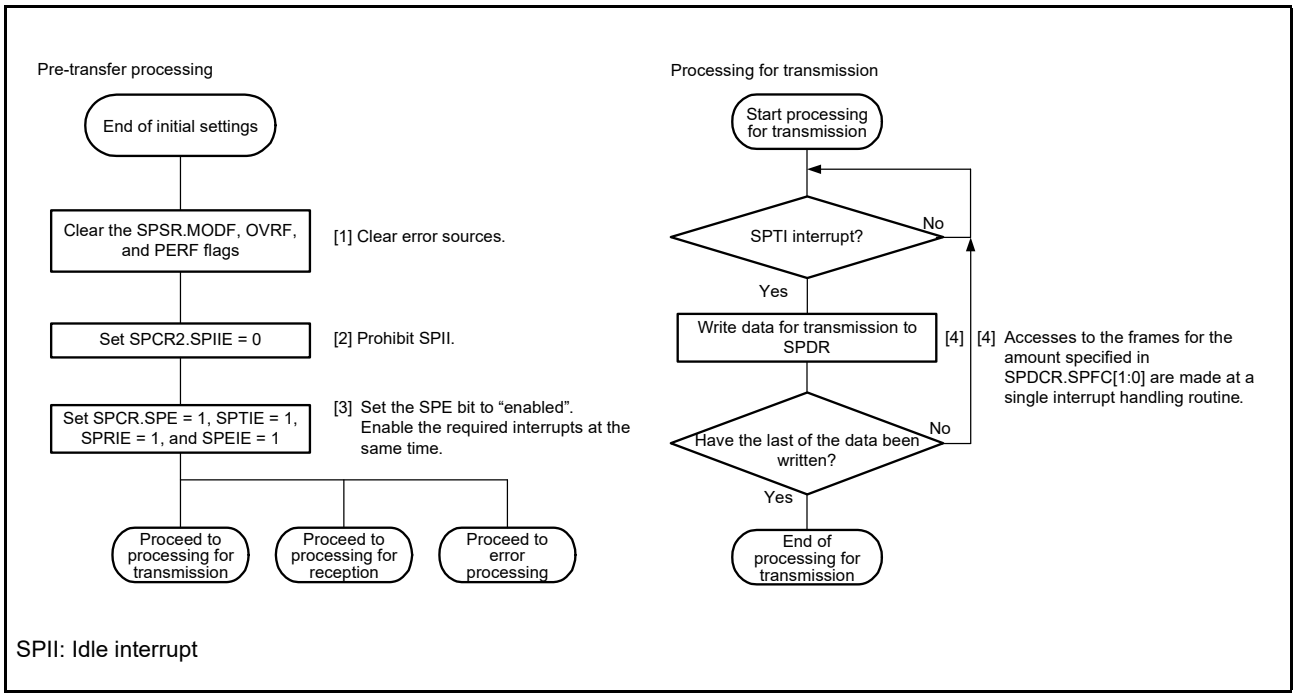


Figure 36.40 Flowchart in Slave Mode (Transmission)

(b) Receive Processing Flow

The RSPI does not handle receive-only operation, so processing for transmission is required if reception is to proceed.

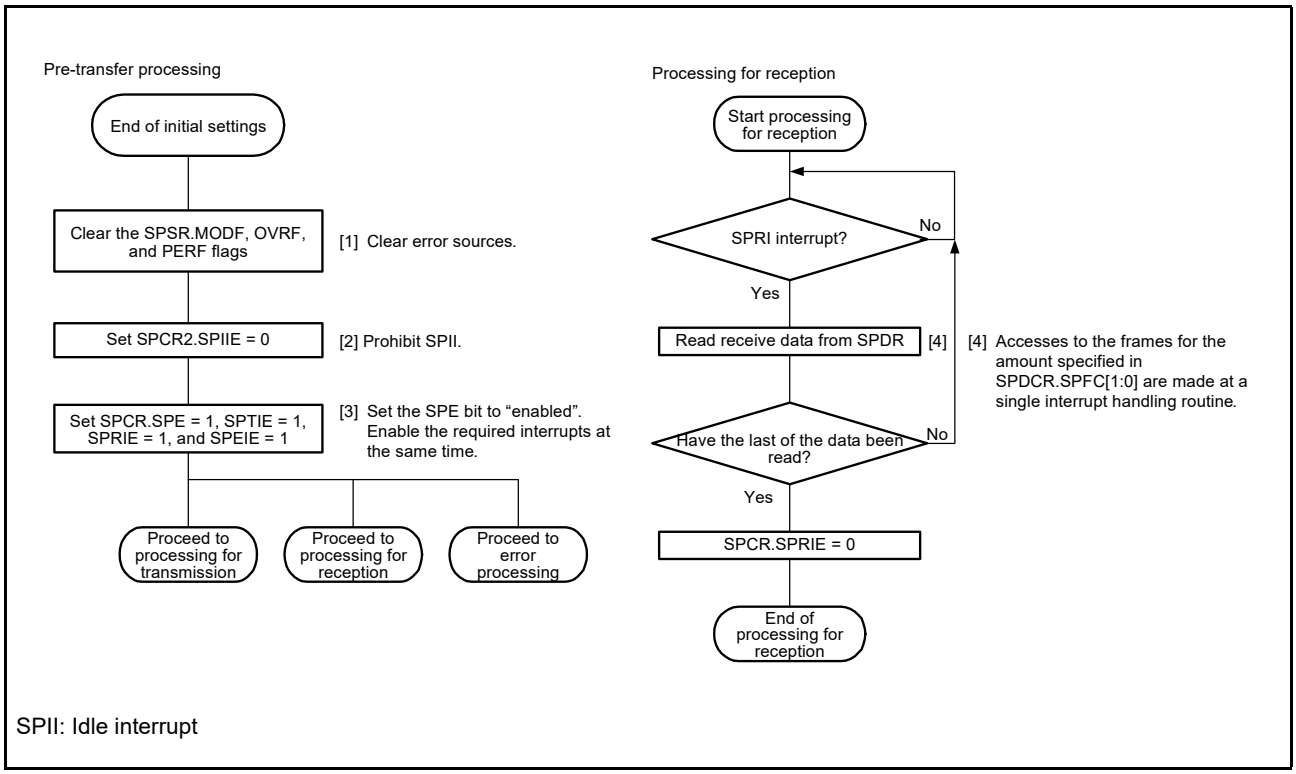
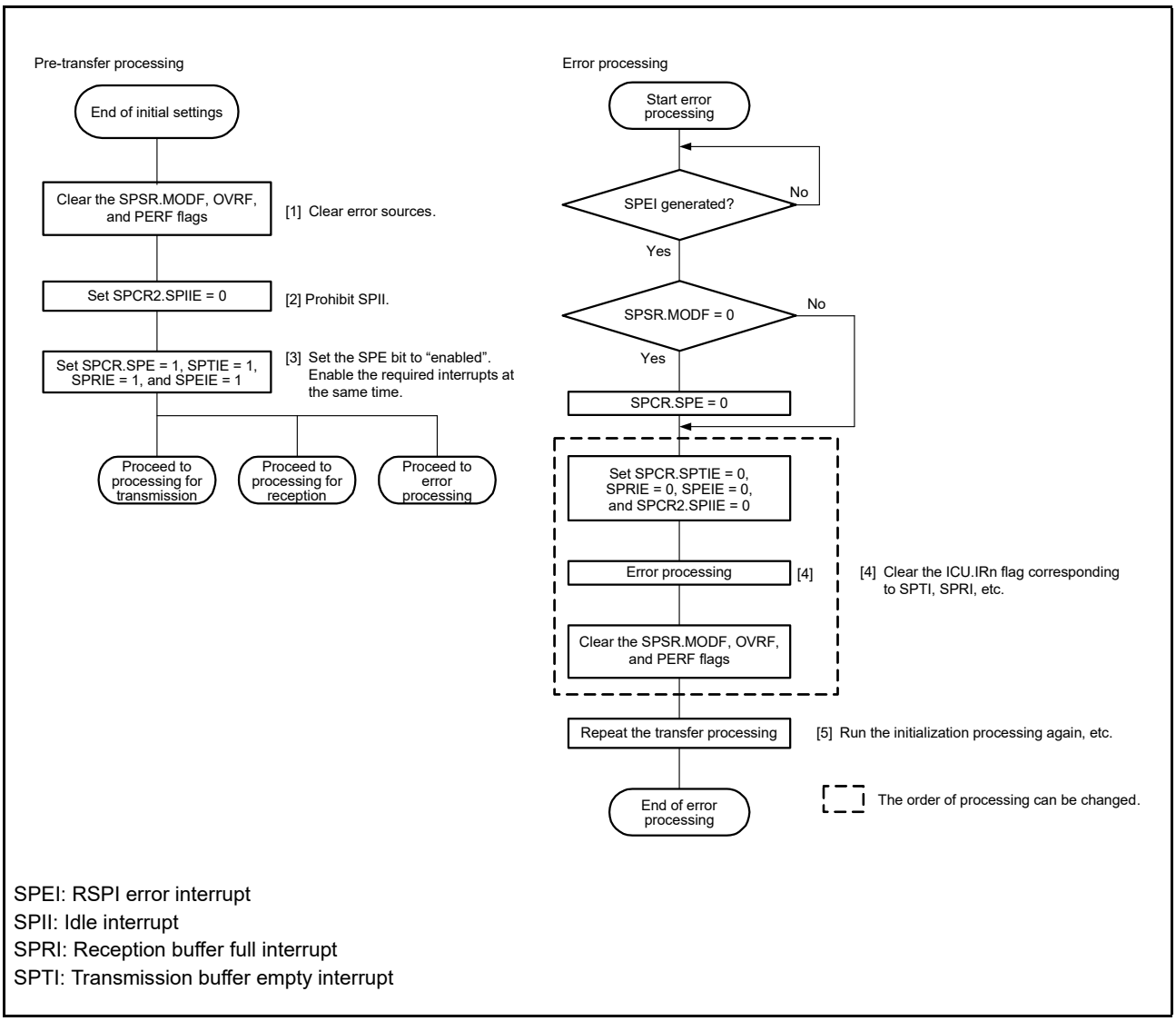


Figure 36.41 Flowchart in Slave Mode (Reception)

(c) Flow of error processing

In slave operation, even when a mode-fault error is generated, the SPSR.MODF flag can be cleared without de-asserting the pin.

When an error occurs, clear the corresponding flag of the IRQ status register (IRQSn) from within the error processing routine. If this is not done, the corresponding interrupt request flag in the IRQ status register (IRQSn) may continue to indicate a transmission buffer empty interrupt (SPTI) or reception buffer full interrupt (SPRI) request. If the reception buffer full interrupt (SPRI) request is indicated, read the reception buffer and initialize the sequencer in the RSPI.



SPEI: RSPI error interrupt
SPII: Idle interrupt
SPRI: Reception buffer full interrupt
SPTI: Transmission buffer empty interrupt

Figure 36.42 Flowchart for Slave Mode (Error Processing)

36.3.11 Clock Synchronous Operation

Setting the SPMS bit in the RSPI control register (SPCR) to 1 selects clock synchronous operation of the RSPI. In clock synchronous operation, the SSLyi pin is not used, and the three pins of RSPCKy, MOSIy, and MISOy handle communications. The SSLyi pin is available as I/O port pins.
Although clock synchronous operation does not require use of the SSLyi pin, operation of the module is the same as in SPI operation. That is, in both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected because the SSLyi pin is not used.
Furthermore, operation should not be performed if clock synchronous operation proceeds when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).
(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

36.3.11.1 Master Mode Operation

(1) Starting a Serial Transfer

The RSPI updates the data in the transmission buffer (SPTX) of SPDR when data is written to the RSPI data register (SPDR) with the transmission buffer being empty (data for the next transfer is not set). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR, the RSPI copies data from the transmission buffer to the shift register and starts serial transmission. Upon copying transmit data to the shift register, the RSPI changes the status of the shift register to “full”, and upon termination of serial transfer, it changes the status of the shift register to “empty”. The status of the shift register cannot be referenced.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format.
However, transfer in clock synchronous operation is conducted without the SSLy0 output signal (y = 0, 1, 2, 3 (for all channels)).

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after transmitting an RSPCKy edge corresponding to the sampling timing. If free space is available in the reception buffer (SPRX), upon termination of serial transfer, the RSPI copies data from the shift register to the reception buffer of the RSPI data register (SPDR).
It should be noted that the final sampling timing varies depending on the bit length of transfer data. In master mode, the RSPI data length depends on the SPCMDm.SPB[3:0] bit setting.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format.
However, transfer in clock synchronous operation is conducted without the SSLy0 output signal (y = 0, 1, 2, 3 (for all channels)).

(3) Sequence Control

The transfer format employed in master mode is determined by SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLyi signals are not output in clock synchronous operation, these settings are valid.
SPSCR is a register used to determine the sequence configuration for serial transfers that are executed by the RSPI in master mode. The following items are set in SPCMDm register: SSLyi output signal value, MSB/LSB first, data length, some of the bit rate settings, RSPCKy polarity/phase, whether SPCKD is to be referenced, whether SSLND is to be referenced, and whether SPND is to be referenced. SPBR holds some of the bit rate settings; SPCKD, an RSPI clock delay value; SSLND, an SSL negation delay; and SPND, a next-access delay value.
According to the sequence length that is assigned to SPSCR, the RSPI makes up a sequence comprised of a part or all of SPCMDm register. The RSPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the RSPI function is enabled, the RSPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The RSPI increments the pointer each time the next-access delay period for a data transfer ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, the RSPI sets the pointer in SPCMD0 register, and in this manner the sequence is executed repeatedly.
(i = 0 to 3; m = 0 to 7; y = 0, 1, 2, 3 (for all channels))

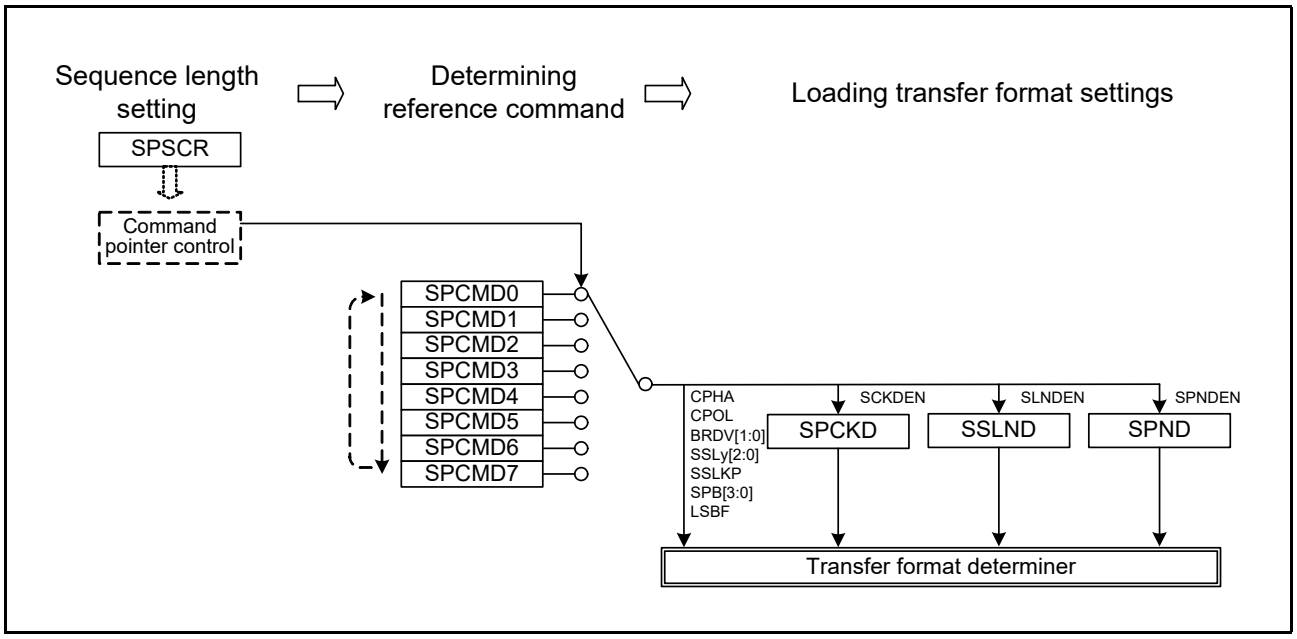


Figure 36.43 Procedure for Determining the Form of Serial Transmission in Master Mode

In this section, a frame is the combination of the data (SPDR) and the settings (SPCMDm) (m = 0 to 7).

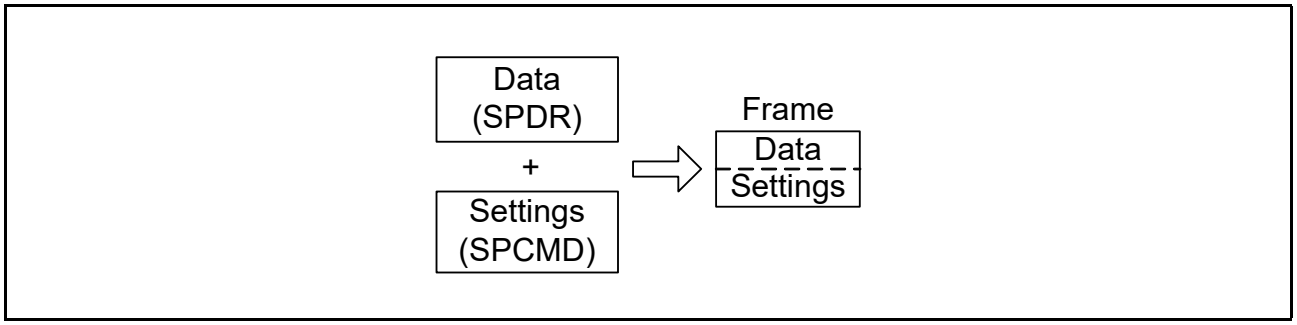


Figure 36.44 Concept of a Frame

Figure 36.45 shows the relationship between the command and the transmit and reception buffers in the sequence of operations specified by the settings in Table 36.4.

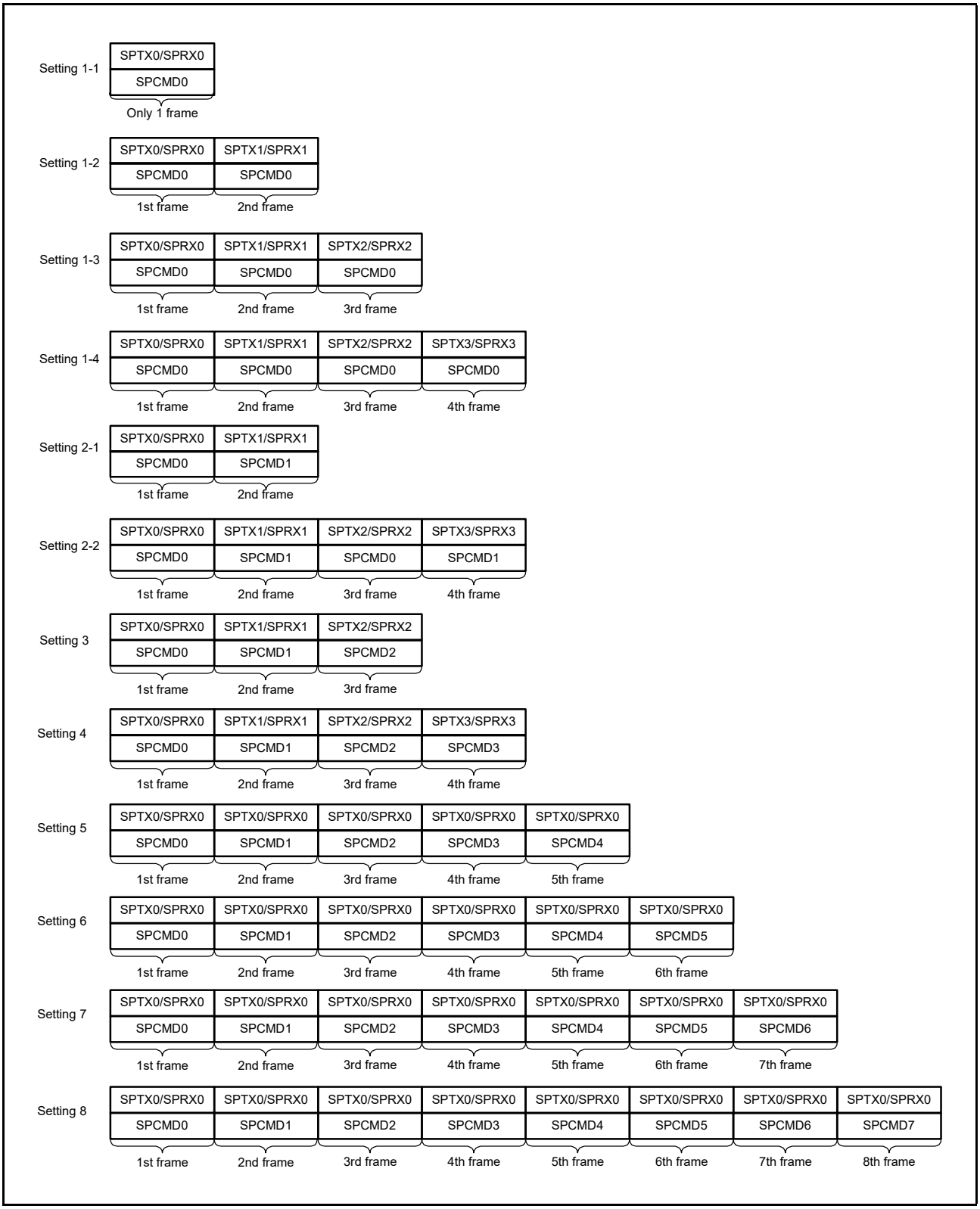


Figure 36.45 Correspondence between the RSPI Command Register and Transmission/Reception Buffers in Sequence Operations

(4) Initialization Flowchart

Figure 36.46 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in master mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, refer to the descriptions given in the individual blocks.

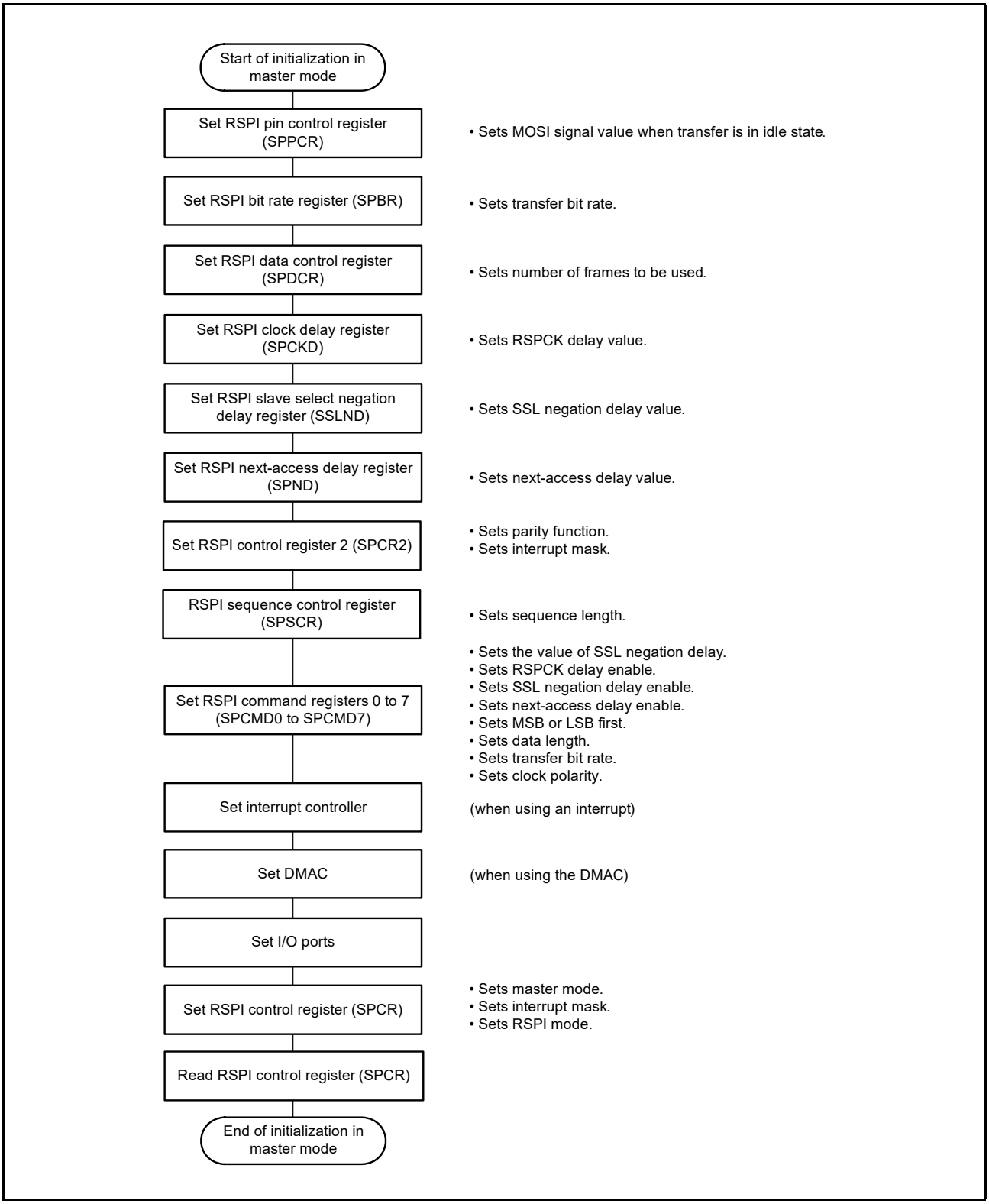


Figure 36.46 Example of Initialization Flowchart in Master Mode (Clock Synchronous Operation)

(5) Flow of Software Processing

Software processing during clock-synchronous master operation is the same as that for SPI master operation. For details, refer to section 36.3.10.1, (9) Software Processing Flow. Note that mode-fault errors will not occur.

36.3.11.2 Slave Mode Operation

(1) Starting a Serial Transfer

When the SPCR.SPMS bit is 1, the first RSPCKy edge triggers the start of a serial transfer in the RSPI.
When detecting the start of a serial transfer in a condition in which the shift register is empty, the RSPI changes the status of the shift register to “full”, so that data cannot be copied from the transmission buffer to the shift register when serial transfer is in progress. If the shift register was full before the serial transfer started, the RSPI keeps the status of the shift register unchanged, in the full state.
When the SPMS bit is 1, the RSPI always drives the MISOy output signal.
For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format.
It should be noted that the SSL0 input signal is not used in clock synchronous operation (y = 0, 1, 2, 3 (for all channels)).

(2) Terminating a Serial Transfer

The RSPI terminates the serial transfer after detecting an RSPCKy edge corresponding to the final sampling timing. When free space is available in the reception buffer, upon termination of serial transfer the RSPI copies received data from the shift register to the reception buffer of the RSPI data register (SPDR). Upon termination of a serial transfer the RSPI changes the status of the shift register to “empty”. The final sampling timing changes depending on the bit length of transfer data. In slave mode, the RSPI data length depends on the SPCMD0.SPB[3:0] bit setting. For details on the RSPI transfer format, refer to section 36.3.5, Transfer Format. (y = 0, 1, 2, 3 (for all channels))

(3) Initialization Flowchart

Figure 36.47 is a flowchart illustrating an example of initialization in clock synchronous operation when the RSPI is used in slave mode. For a description of how to set up the interrupt controller, DMAC, and I/O ports, refer to the descriptions given in the individual blocks.

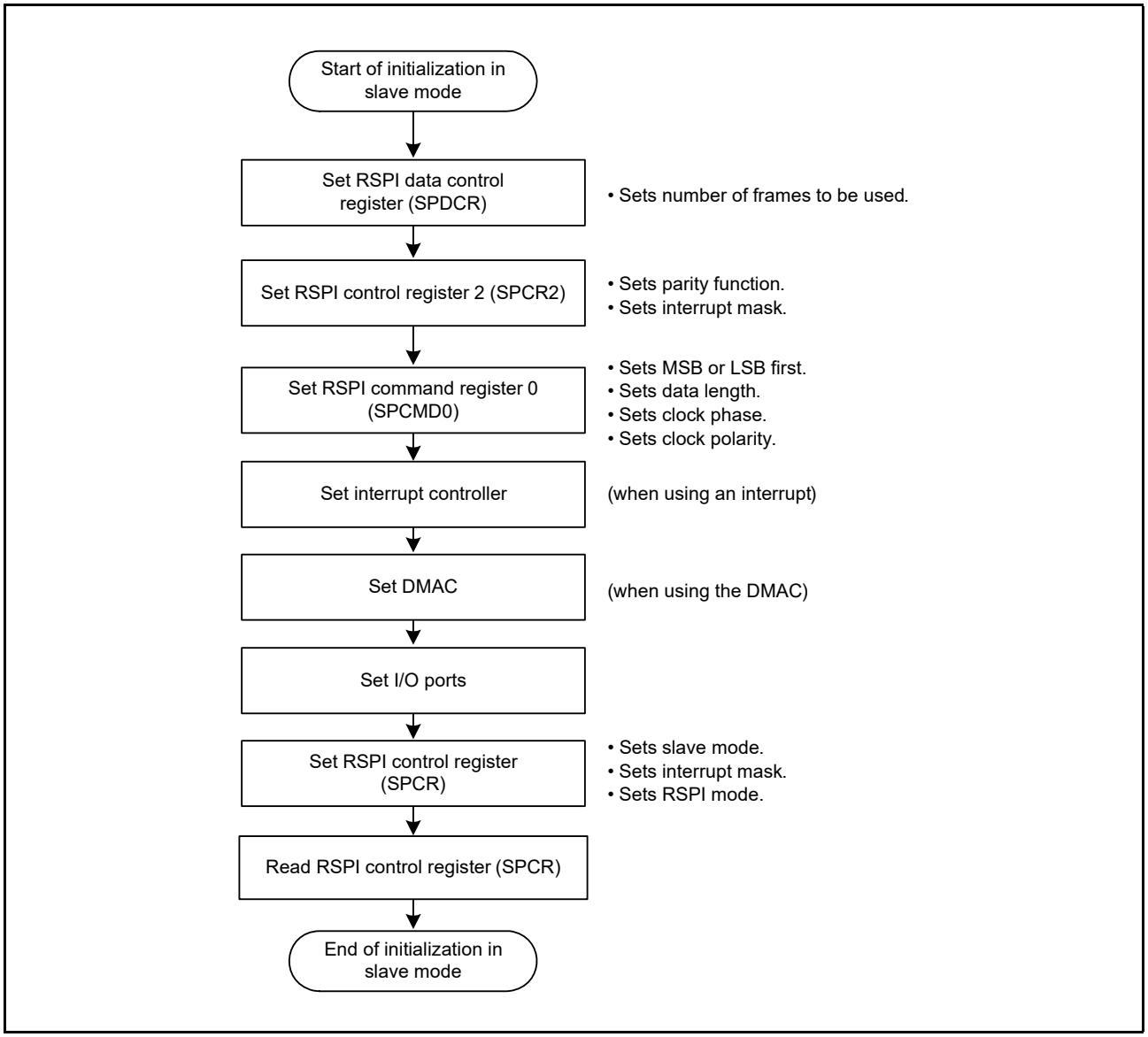


Figure 36.47 Example of Initialization Flowchart in Slave Mode (Clock Synchronous Operation)

(4) Flow of Software Processing

Software processing during clock-synchronous slave operation is the same as that for SPI slave operation. For details, refer to section 36.3.10.2, (6) Software Processing Flow. Note that mode-fault errors will not occur.

36.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the RSPI shuts off the path between the MISOy pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIy pin and the shift register if the SPCR.MSTR bit is 0, and connects the input path and output path of the shift register. The RSPI does not shut off the path between the MOSIy pin and the shift register if the SPCR.MSTR bit is 1, and between the MISOy pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the RSPI or the inversed transmit data becomes the received data for the RSPI.
Table 36.12 lists the relationship among the SPLP2 and SPLP bits and the received data. Figure 36.48 shows the configuration of the shift register I/O paths for the case where the RSPI in master mode is set in loopback mode (SPPCR.SPLP2 = 0, SPPCR.SPLP = 1) (y = 0, 1, 2, 3 (for all channels)).

Table 36.12 SPLP2 and SPLP Bit Settings and Received Data

SPPCR.SPLP2 Bit	SPPCR.SPLP Bit	Received Data
0	0	Input data from the MOSIy pin or MISOy pin
0	1	Inversed transmit data
1	0	Transmit data
1	1	Transmit data

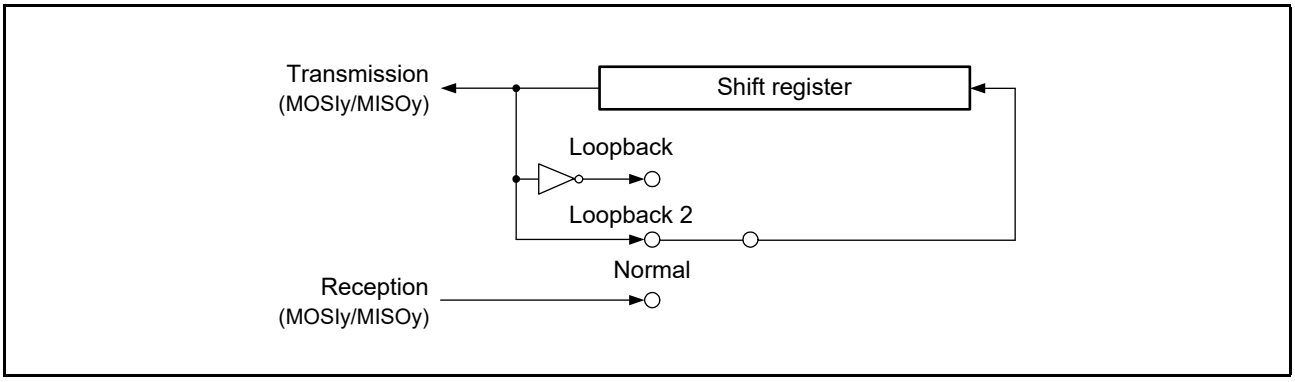


Figure 36.48 Configuration of Shift Register I/O Paths in Loopback Mode (Master Mode)

36.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. In order to detect defects in the parity bit adding unit and error detecting unit of the parity circuit, self-diagnosis is executed for the parity circuit following the flowchart shown in Figure 36.49.

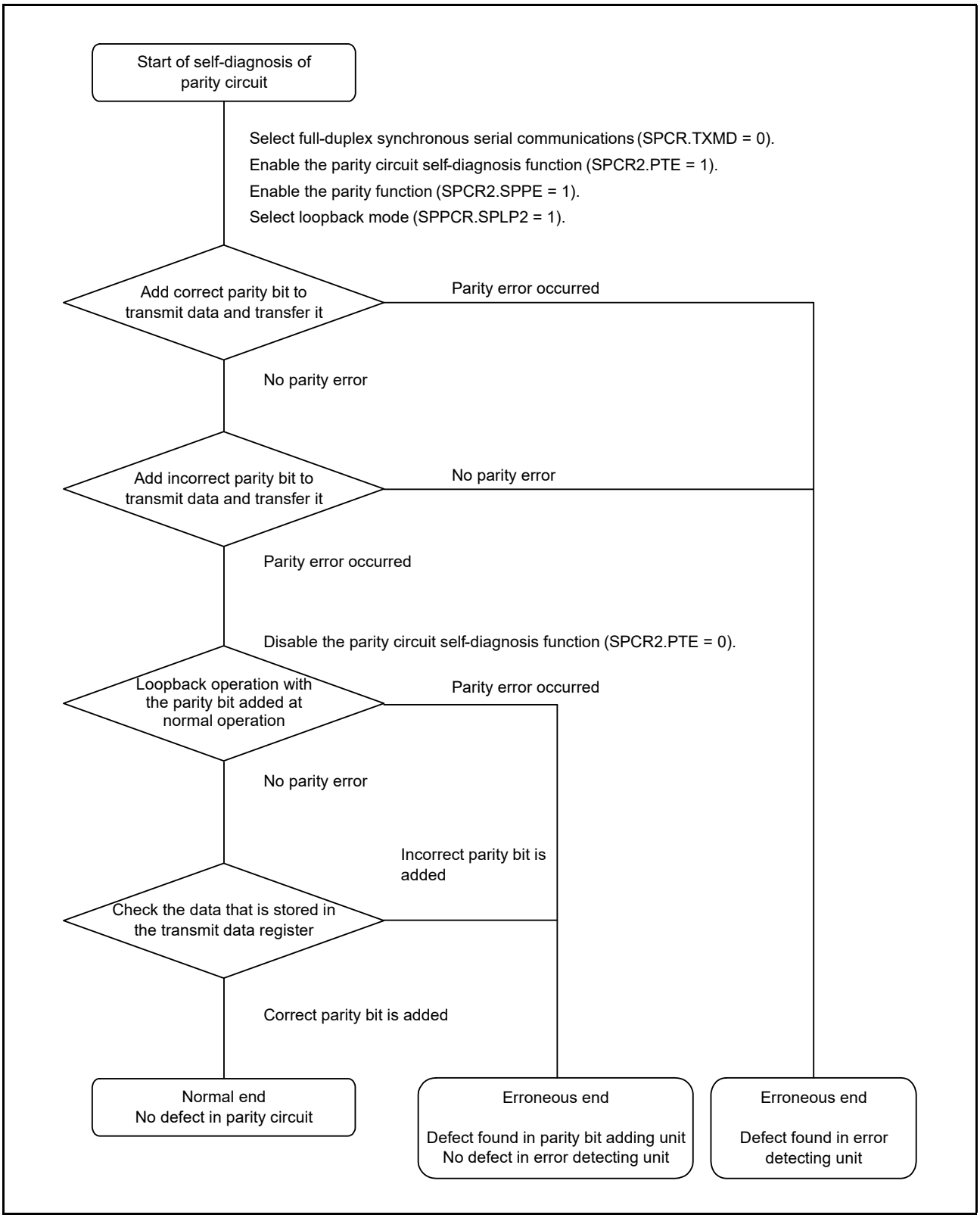


Figure 36.49 Flowchart for Self-Diagnosis of Parity Circuit

36.3.14 Interrupt Sources

The RSPI has interrupt sources of reception buffer full, transmission buffer empty, mode fault, overrun, parity error, and RSPI idle. In addition, the DMAC can be activated by the reception buffer full or transmission buffer empty interrupt to perform data transfer.

Since the common vector address is allocated to interrupt requests due to mode-fault, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the RSPI are listed in Table 36.13. An interrupt is generated on satisfaction of an interrupt condition in Table 36.13. Clear the reception buffer full and transmission buffer empty sources through data transfer.

When using the DMAC to perform data transmission/reception, the DMAC must be set up first to be in a status in which transfer is enabled before making the RSPI settings. For the method for setting the DMAC, refer to section 15, DMA Controller (DMACAa).

Table 36.13 Interrupt Sources of RSPI

Interrupt Source	Symbol	Interrupt Condition	DMAC/DTC Activation
Reception buffer full	SPRI	The reception buffer becomes full while the SPCR.SPRIE bit is 1.	Possible
Transmission buffer empty	SPTI	The transmission buffer becomes empty while the SPCR.SPTIE bit is 1.	Possible
RSPI errors (mode fault, overrun and parity error)	SPEI	The SPSR.MODF, OVRF, or PERF flag is set to 1 while the SPCR.SPEIE bit is 1.	Impossible
RSPI idle	SPII	The SPSR.IDLNF flag is set to 0 while the SPCR2.SPIIE bit is 1.	Impossible

36.4 Link Operation by Event Linking (only for RSPI channel 0)

The event link controller (ELC) is capable of producing the following event output signals. The event link output signal is output regardless of the setting of the corresponding interrupt enable bit (SPCR.SPEIE, SPCR.SPTIE or SPCR.SPRIE).

36.4.1 Reception Buffer Full Event Output

This event signal is output when received data have been transferred from the shift register to the SPDR on completion of serial transfer.

36.4.2 Transmission Buffer Empty Event Output

This event signal is output when data for transmission have been transferred from the transmission buffer to the shift register and when the value of the SPE bit has changed from 0 to 1.

36.4.3 Mode Fault, Overrun, or Parity Error Event Output

(1) Mode Fault

Table 36.14 lists the occurrence conditions of a mode fault event.

Table 36.14 Occurrence Conditions of Mode Fault Event

	SPCR.MODFEN Bit	SSLy0 Pin (y = 0, 1, 2, 3)	Remarks
Master (SPCR.MSTR bit = 1)	1	Active	When the setting of the SPCR.SPMS bit is 0 while the MSTR and SPCR.MODFEN bits are 1, mode fault error, overrun error, and parity error event output cannot be used. Do not set the ELSRn register to 52h.
Slave (SPCR.MSTR bit = 0)	1	Not active	Event is output only when the pin is deactivated during transmission.

(2) Overrun

The condition for this event signal being output in response to an overrun is completion of serial transfer while the reception buffer contains data that have not been read and the value of the SPCR.TXMD bit is 0, in which case the OVRF flag is set to 1.

(3) Parity Error

The condition for this event signal being output in response to a parity error is detection of a parity error on completion of serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

36.4.4 RSPI Idle Event Output

(1) In Master Mode

In master mode, an event is output when the condition for setting the IDLNF flag (RSPI idle flag) to 0 is satisfied.

(2) In Slave Mode

In slave mode, an event is output when the SPE bit in the SPCR is set to 0 (RSPI is initialized).

36.4.5 Transmission-Completed Event Output

During both SPI operation and clock synchronous operation in master mode, an event is output under the condition for setting the IDLNF flag (RSPI idle flag) from 1 to 0.

Table 36.15 Conditions for Generation of a Transmission-Completed Event (Slave)

	Transmission Buffer State	Shift Register State	Others
SPI operation (SPCR.SPMS = 0)	Empty	Empty	Negation of SSL0 input
Clock synchronous operation (SPCR.SPMS = 1)	Empty	Empty	Edge detection of the last RSPCK

Regardless of whether the operation is in master mode or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in transmission or the SPCR.SPE bit is cleared because of a mode fault error.

36.5 Usage Notes

36.5.1 Setting Module Stop Function

Module stop control register B (MSTPCRB) is used to enable or disable operation of the RSPI. The RSPI is stopped after a reset. The registers become accessible on release from the module-stop state. For details, refer to section 9, Low-Power Consumption Function.

36.5.2 Note on Low-Power Consumption Functions

Set the SPCR.SPE bit to 0 and terminate communications prior to entering module-stop state.

36.5.3 Notes on Starting Transfer

If the corresponding interrupt request flag in the IRQ status register (IRQSn) is 1 at the time transfer is to be started, the next interrupt request is generated after the start of transfer and an interrupt request is retained in the module. This can lead to unanticipated behavior of the interrupt request flag.
When the request flag for the RSPI interrupt request is 1 at the time transfer is to start, follow the procedure below to clear interrupt requests in the module or the IRQ status register (IRQSn) before enabling operations (by setting the SPCR.SPE bit to 1).

1. Confirm that transfer has stopped (i.e. that the SPCR.SPE bit is 0).
2. Set the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) to 0.
3. Read the relevant interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) and confirm that its value is 0.
4. Set the relevant interrupt request flag in the IRQ status register (IRQSn) to 0.

37. SPI Multi I/O Bus Controller (SPIBSC)

The SPI multi I/O bus controller outputs control signals to the serial flash memory connected to the SPI multi I/O bus space, thus enabling direct connection of the serial flash memory.
This LSI incorporates one channel of SPI multi I/O bus controller.

37.1 Overview

This module allows using direct reading or SPI operating mode to transmit and receive data with the serial flash memory connected to the SPI multi I/O bus space. The specification of the SPIBSC is listed in Table 37.1.

Table 37.1 SPIBSC Specifications

Item	Description
Serial flash interface	• One serial flash memory can be connected. • A data bus size of 1 bit, 2 bits, or 4 bits can be selected.
External address space read mode	• A maximum of 4 Gbytes of address space is supported. • The SPBSSL pin can be automatically controlled by access address monitoring. • Efficient data reception is possible due to the internal read cache (line size: 64 bits × 16 entries).
SPI operating mode	• Any read and write operations are available for a serial flash memory.
Bit rate	• The internal baud rate generator divides the frequency of PCLKA to generate SPBCLK. • The frequency division ratio of SPBCLK can be set in the range from 2 to 4080.
SPBSSL pin control	• The delay from the time the SPBSSL signal is activated to the time SPBCLK starts operating (clock delay) can be set. Setting range: 1 to 8 SPBCLK; Unit of the setting: 1 SPBCLK • The delay from the time SPBCLK stops to the time the SPBSSL output is inactivated (SPBSSL negation delay) can be set. Setting range: 1.5 to 8.5 SPBCLK; Unit of the setting: 1 SPBCLK • The wait of the SPBSSL output for the next access (next access delay) can be set. Setting range: 1 to 8 SPBCLK; Unit of the setting: 1 SPBCLK • The polarity of the SPBSSL signal can be changed.

Figure 37.1 is a block diagram of this module.

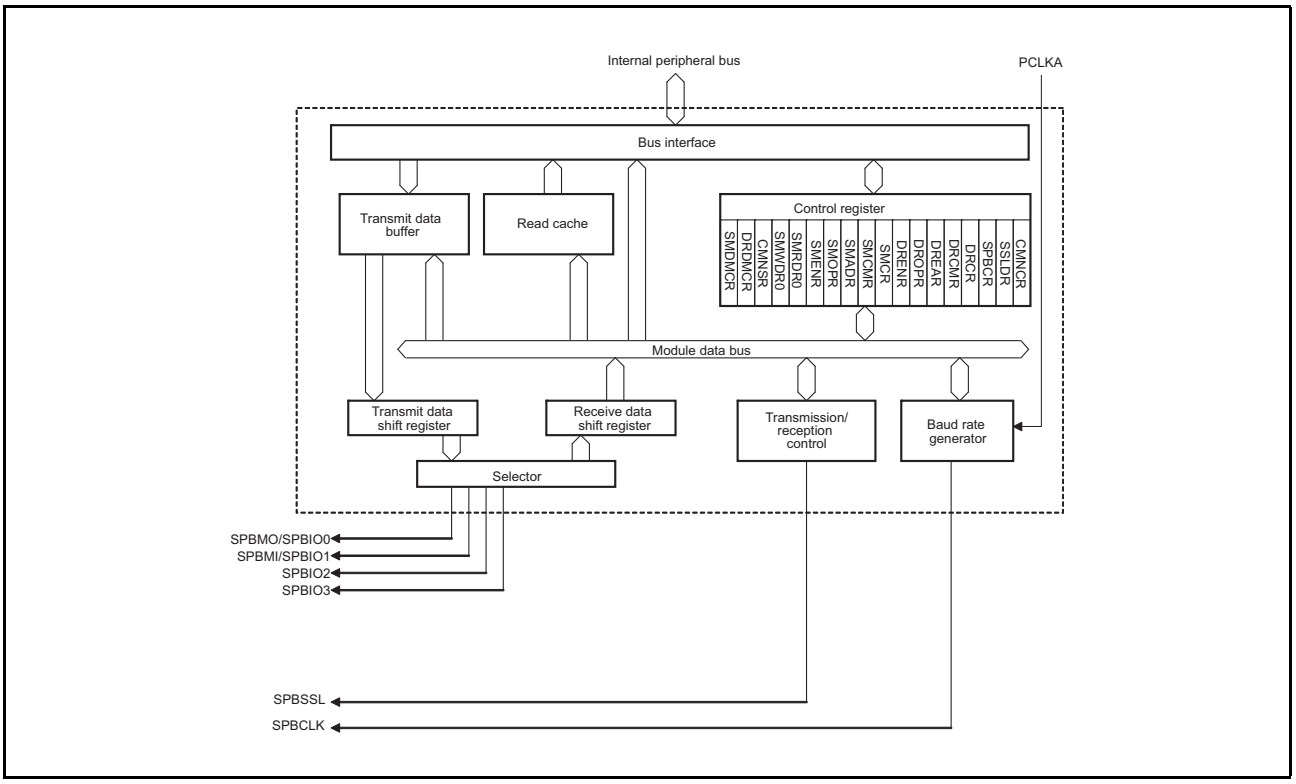


Figure 37.1 Block Diagram of SPIBSC

Table 37.2 lists the input/output pins of this module.

Table 37.2 Pin Configuration of the SPIBSC

Pin Name	Symbol	I/O	Function
Clock pin	SPBCLK	Output	Clock output
Slave select pin	SPBSSL	Output	Slave selection
Port data 0 pin	SPBMO/SPBIO0	I/O	Port master transmit data/data 0
Port data 1 pin	SPBMI/SPBIO1	I/O	Port master input data/data 1
Port data 2 pin	SPBIO2	I/O	Port data 2
Port data 3 pin	SPBIO3	I/O	Port data 3

37.2 Register Descriptions

37.2.1 Common Control Register (CMNCR)

The CMNCR register is a 32-bit register that controls the SPI multi I/O bus controller. The settings of this register are reflected both in external address space read mode and SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MD	—	—	—	—	—	—	SFDE	MOIIO3[1:0]		MOIIO2[1:0]		MOIIO1[1:0]		MOIIO0[1:0]	
Value after reset:	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IO3FV[1:0]		IO2FV[1:0]		—	—	IO0FV[1:0]		—	CPHAT	CPHAR	SSLP	CPOL	—	BSZ[1:0]	
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BSZ[1:0]	Data Bus Size	Specifies the number of serial flash memories to be connected. This bit must be set to 00b because only one memory can connect to this product. If another value is set, the operation cannot be guaranteed. b1 b0 0 0: 1 memory 0 1: Setting prohibited 1 X: Setting prohibited	R/W
b2	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b3	CPOL	SPBSSL Negation Period SPBCLK Output Direction	Sets the output level of the SPBCLK pin during inactive period of the SPBSSL signal. 0: The output of the SPBCLK pin is 0 during inactive period of the SPBSSL signal. 1: The output of the SPBCLK pin is 1 during inactive period of the SPBSSL signal.	R/W
b4	SSLP	SPBSSL Signal Polarity	Sets the polarity of SPBSSL signal. 0: Active low SPBSSL signal 1: Active high SPBSSL signal	R/W
b5	CPHAR	Input Latch	Sets the edge of the SPBCLK signal for the reception data. The CPHAT bit and this bit should be set according to the following table. 0: Data reception at odd edge 1: Data reception at even edge Settings of the CPHAT and CPHAR Bits CPHAT / CPHAR: 0/0 Setting enabled; 0/1 Setting enabled; 1/0 Setting prohibited; 1/1 Setting enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b6	CPHAT	Output Shift	Sets the edge of the SPBCLK signal for data transmission. This bit and the CPHAR bit should be set according to the description of the CPHAR bit. 0: Data transmission at even edge 1: Data transmission at odd edge	R/W
b7	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b9, b8	IO0FV[1:0]	SPBIO0 Fixed Value for 1-bit Size Input	Fixes the output value of the SPBIO0 pins for 1-bit size input. b9 b8 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b11, b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b13, b12	IO2FV[1:0]	SPBIO2 Fixed Value for 1-bit/2-bit Size	Fixes the output value of the SPBIO2 pins for 1-bit/2-bit size. b13 b12 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b15, b14	IO3FV[1:0]	SPBIO3 Fixed Value for 1-bit/2-bit Size	Fixes the output value of the SPBIO3 pins for 1-bit/2-bit size. b15 b14 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b17, b16	MOIIO0[1:0]	SPBIO0 Fixed Value for SPBSSL Idle	Fixes output values of the SPBIO0 pins during inactive period of the SPBSSL signal. b17 b16 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b19, b18	MOIIO1[1:0]	SPBIO1 Fixed Value for SPBSSL Idle	Fixes output values of the SPBIO1 pins during inactive period of the SPBSSL signal. b19 b18 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b21, b20	MOIIO2[1:0]	SPBIO2 Fixed Value for SPBSSL Idle	Fixes output values of the SPBIO2 pins during inactive period of the SPBSSL signal. b21 b20 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W

Bit	Symbol	Bit Name	Description	R/W
b23, b22	MOIIO3[1:0]	SPBIO3 Fixed Value for SPBSSL Idle	Fixes output values of the SPBIO3 pins during inactive period of the SPBSSL signal. b23 b22 0 0: Output value 0 0 1: Output value 1 1 0: Output value is the last bit value of the previous transfer (or the state is Hi-Z, if Hi-Z was the state in the last bit period of the previous transfer). 1 1: Output value Hi-Z	R/W
b24	SFDE	Data Swap Setting for Serial Flash Memory	Specifies whether or not swapping of data in serial flash memory is performed. 0: Swapping is not performed. 1: Swapping is performed in 8-bit units. For details, see section 37.3.4, Data Alignment.	R/W
b30 to b25	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b31	MD	Operating Mode Switch	Switches the operating modes. 0: External address space read mode 1: SPI operating mode	R/W

37.2.2 SSL Delay Register (SSLDR)

The SSLDR register is a 32-bit register that adjusts the timing between the SPBSSL signal and the SPBCLK signal. The settings of this register are reflected both in external address space read mode and SPI operating mode.
The settings of this register should be changed when the TEND flag in the CMNSR register is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]			—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	SCKDL[2:0]	Clock Delay	Sets the period from the time the SPBSSL signal is activated to the time the clock is output from the SPBCLK signal (clock delay). b2 b0 000: 1 SPBCLK cycle 001: 2 SPBCLK cycles 010: 3 SPBCLK cycles 011: 4 SPBCLK cycles 100: 5 SPBCLK cycles 101: 6 SPBCLK cycles 110: 7 SPBCLK cycles 111: 8 SPBCLK cycles	R/W
b7 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b10 to b8	SLNDL[2:0]	SPBSSL Negation Delay	Sets the period from the time the last edge of the SPBCLK signal is transferred to the time the SPBSSL signal is inactivated (SPBSSL negation delay). b10 b8 000: 1.5 SPBCLK cycles 001: 2.5 SPBCLK cycles 010: 3.5 SPBCLK cycles 011: 4.5 SPBCLK cycles 100: 5.5 SPBCLK cycles 101: 6.5 SPBCLK cycles 110: 7.5 SPBCLK cycles 111: 8.5 SPBCLK cycles	R/W
b15 to b11	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b18 to b16	SPNDL[2:0]	Next Access Delay	Sets the period from transfer end to next transfer start (next access). b18 b16 000: 1 SPBCLK cycle 001: 2 SPBCLK cycles 010: 3 SPBCLK cycles 011: 4 SPBCLK cycles 100: 5 SPBCLK cycles 101: 6 SPBCLK cycles 110: 7 SPBCLK cycles 111: 8 SPBCLK cycles	R/W
b31 to b19	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.3 Bit Rate Register (SPBCR)

The SPBCR register is a 32-bit register that sets the bit rate.
The settings of this register are reflected both in external address space read mode and SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SPBR[7:0]								—	—	—	—	—	—	BRDV[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit Name	Description	R/W
b1, b0	BRDV[1:0]	Bit Rate Frequency Division	Sets the bit rate. The bit rate is determined by a combination of these bits with the SPBR[7:0] bits. The setting value of the SPBR bit determines the base bit rate. This bit is used to select a division ratio of the base bit rate from among no division, 2, 4, and 8. b1 b0 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8	R/W
b7 to b2	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b15 to b8	SPBR[7:0]	Bit Rate	Sets the bit rate. The bit rate is determined by a combination of these bits with the BRDV[1:0] bits. For details, see Table 37.3, Relationship between SPBR[7:0] and BRDV[1:0] Settings.	R/W
b31 to b16	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

(1) Bit Rate

The SPBR[7:0] and BRDV[1:0] bits are used for setting the bit rate.
The following formula is used to calculate the bit rate when SPBR[7:0] ≠ 0:

Bit rate = PCLKA / ($2 \times n \times 2^N$)

n: SPBR[7:0] setting (1, …, 255)

N: BRDV[1:0] setting (0 to 3)

The following formula is used to calculate the bit rate when SPBR[7:0] = 0:

Bit rate = PCLKA / 2^N

Setting both the SPBR[7:0] and BRDV[1:0] bits to 0 is prohibited.

Table 37.3 Relationship between SPBR[7:0] and BRDV[1:0] Settings

SPBR[7:0] (n)	BRDV[1:0] (N)	Division Ratio	Bit Rate PCLKA = 150 MHz
0	0	1	Setting prohibited
0	1	2	75 Mbps
0	2	4	37.5 Mbps
0	3	8	18.75 Mbps
1	0	2	75 Mbps
2	0	4	37.5 Mbps
3	0	6	25 Mbps
4	0	8	18.75 Mbps
5	0	10	15 Mbps
6	0	12	12.5 Mbps
6	1	24	6.25 Mbps
6	2	48	3.13 Mbps
6	3	96	1.56 Mbps
255	3	4080	36.76 Kbps

Note: The bit rate should be set so that it will satisfy the AC characteristics of this module.

37.2.4 Data Read Control Register (DRCR)

The DRCR register is a 32-bit register that sets the operation in external address space read mode.
The bits except the SSLN bit should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 500Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	SSLN	—	—	—	—	RBURST[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	RCF	RBE	—	—	—	—	—	—	—	SSLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SSLE	SPBSSL Negation	Sets the inactivation conditions for the SPBSSL signal during read burst. The SPBSSL signal is inactivated for each access during normal read. 0: The SPBSSL signal is inactivated after transfer of data set in burst length. 1: The SPBSSL signal is inactivated when the accessed address is not continuous with the previously transferred address.	R/W
b7 to b1	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	RBE	Read Burst	Turns burst read ON or OFF. 0: Data is read according to the access size. 1: Read cache is enabled, and as many data units as the burst count specified in RBURST[3:0] bits is read.	R/W
b9	RCF	Read Cache Flush	When 1 is written to this bit, all the entries in the read cache are cleared. This bit is always read as 0. Note: After flushing the read cache by writing 1 to this bit, read the DRCR register before proceeding to read from the external address space.	R/W
b15 to b10	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b19 to b16	RBURST [3:0]	Read Data Burst Length	Sets the burst length (data unit count) when reading. This bit is enabled when the RBE bit of this register is set to 1. b19 b16 0000: 1 data unit 0001: 2 continuous data units : 1110: 15 continuous data units 1111: 16 continuous data units One data unit is 64 bits long.	R/W
b23 to b20	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b24	SSLN	SPBSSL Negation	Writing 1 to this bit when both the RBE and SSLE bits of this register are 1 inactivates the active SPBSSL signal. This bit is always read as 0. Note: To start next access after the SPBSSL signal is inactivated by this bit, read the SSLF bit of the CMNSR register = 0 to confirm that the SPBSSL signal has been inactivated.	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b25	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.5 Data Read Command Setting Register (DRCMR)

The DRCMR register is a 32-bit register that sets the commands issued in external address space read mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OCMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	OCMD[7:0]	Optional Command	Sets the optional command.	R/W
b15 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b23 to b16	CMD[7:0]	Command	Sets the command. For details, see the details about the serial flash memory to be used.	R/W
b31 to b24	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.6 Data Read Extended Address Setting Register (DREAR)

The DREAR register is an address setting register when the serial flash address is output in 32-bit mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	EAV[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EAC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	EAC[2:0]	32-Bit Extended External Address Valid Range	Sets the range of the external address to be used as serial flash address when the serial flash address is output in 32-bit mode. This setting is valid when the ADE[3] bit in DRENR is 1. b2 b0 000: External address bits [24:0] enabled 001: External address bits [25:0] enabled Other than above: Setting prohibited	R/W
b15 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b23 to b16	EAV[7:0]	32-Bit Extended Upper Address Fixed Value	The upper address of the external address specified by the EAC[2:0] bits of this register are set to these bits when the serial flash address is output in 32-bit mode. Bit 0 corresponds to the serial flash address bit [25], and bit 7 corresponds to the bit [32]. This setting is valid only when the ADE[3] bit in DRENR is 1. When EAC[2:0] are 000, serial flash address [32:25] are set to EAV[7:0]. When EAC[2:0] are 001, serial flash address [32:26] are set to EAV[7:1].	R/W
b31 to b24	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.7 Data Read Option Setting Register (DROPR)

The DROPR register is a 32-bit register that sets the option data in external address space read mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	OPD3[7:0]								OPD2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OPD1[7:0]								OPD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	OPD0[7:0]	Option Data 0	Sets the option data 0.	R/W
b15 to b8	OPD1[7:0]	Option Data 1	Sets the option data 1.	R/W
b23 to b16	OPD2[7:0]	Option Data 2	Sets the option data 2.	R/W
b31 to b24	OPD3[7:0]	Option Data 3	Sets the option data 3.	R/W

Note: OPD3, OPD2, OPD1, and OPD0 are output in this order.

37.2.8 Data Read Enable Setting Register (DRENR)

The DRENR register is a 32-bit register that sets the bit size of the command, optional command, address, option data, and read data in external address space read mode and enables outputting them other than read data.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 501Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CDB[1:0]		OCDB[1:0]		—	—	ADB[1:0]		—	—	OPDB[1:0]		—	—	DRDB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DME	CDE	—	OCDE	ADE[3:0]				OPDE[3:0]				—	—	—	—
Value after reset:	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b7 to b4	OPDE[3:0]	Option Data Enable	Sets the option data to be output. Be sure to use the following setting; otherwise, the operation is not guaranteed. b7 b4 0000: Output disabled 1000: OPD3 1100: OPD3, OPD2 1110: OPD3, OPD2, OPD1 1111: OPD3, OPD2, OPD1, OPD0 Other than above: Setting prohibited	R/W
b11 to b8	ADE[3:0]	Address Enable	Sets the address to be output. Be sure to use the following setting; otherwise, the operation is not guaranteed. b11 b8 0000: Output disabled 0111: Address[23:0] 1111: Address[31:0] Other than above: Setting prohibited	R/W
b12	OCDE	Optional Command Enable	Sets the optional command to be output. 0: Optional command output disabled 1: Optional command output enabled	R/W
b13	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14	CDE	Command Enable	Sets the command to be output. 0: Command output disabled 1: Command output enabled	R/W
b15	DME	Dummy Cycle Enable	Enables insertion of the dummy cycle before the read data. Note: A setting is prohibited for a transfer starting with a dummy cycle. 0: Dummy cycle insertion disabled 1: Dummy cycle insertion enabled	R/W
b17, b16	DRDB[1:0]	Data Read Bit Size	Sets the data read size in bit units. b17 b16 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W

Bit	Symbol	Bit Name	Description	R/W
b19, b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b21, b20	OPDB[1:0]	Option Data Bit Size	Sets the option data size in bit units. b21 b20 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b23, b22	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b25, b24	ADB[1:0]	Address Bit Size	Sets the address size in bit units. b25 b24 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b27, b26	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b29, b28	OCDB[1:0]	Optional Command Bit Size	Sets the optional command size in bit units. b29 b28 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b31, b30	CDB[1:0]	Command Bit Size	Sets the command size in bit units. For details, see the details about the serial flash memory to be used. b31 b30 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W

37.2.9 SPI Mode Control Register (SMCR)

The SMCR register is a 32-bit register that sets the operation in SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SSLKP	—	—	—	—	—	SPIRE	SPIWE	SPIE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	SPIE	SPI Data Transfer Enable	Data is transferred by setting this bit to 1. This bit is enabled only when the TEND bit in CMNSR is set to 1. The operation cannot be guaranteed when this bit is set to 1 with the TEND bit set to 0. This bit is always read as 0. Note: When the SPBSSL signal is inactive, the command, optional command, address, and option data that are set as the output by the DRENR register are output even if the SPIRE and SPIWE bits are set to 0. When the SPBSSL signal is active, follow the notes described in section 37.4.2, Notes on Starting Transfer from the SPBSSL Signal Retained State in SPI Operating Mode.	R/W
b1	SPIWE	Data Write Enable	Sets write operation in SPI operating mode. 0: Data writing disabled 1: Data writing enabled Note: When the transfer data bit size is set to 2 bits or 4 bits with the SPIDB[1:0] bits, the SPIRE and SPIWE bits should not be set to 1 at the same time.	R/W
b2	SPIRE	Data Read Enable	Sets read operation in SPI operating mode. 0: Data reading disabled 1: Data reading enabled Note: When the transfer data bit size is set to 2 bits or 4 bits with the SPIDB[1:0] bits, the SPIRE and SPIWE bits should not be set to 1 at the same time.	R/W
b7 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b8	SSLKP	SPBSSL Signal Level	Determines the status of the SPBSSL signal after the end of transfer. 0: SPBSSL signal is inactivated at the end of transfer. 1: SPBSSL signal level is maintained from the end of transfer to the start of next access.	R/W
b31 to b9	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.10 SPI Mode Command Setting Register (SMCMR)

The SMCMR register is a 32-bit register that sets the commands issued in SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	OCMD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	OCMD[7:0]	Optional Command	Sets the optional command.	R/W
b15 to b8	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b23 to b16	CMD[7:0]	Command	Sets the command. For details, see the details about the serial flash memory to be used.	R/W
b31 to b24	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.11 SPI Mode Address Setting Register (SMADR)

The SMADR register is a 32-bit register that sets the addresses of the serial flash memory in SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ADRE[7:0]								ADR[23:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADR[23:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b23 to b0	ADR[23:0]	Address	Sets the address of the serial flash memory.	R/W
b31 to b24	ADRE[7:0]	Address	Sets the value of bits 31 to 24 when the serial flash address is output in 32-bit units. This setting is valid when ADE[3] in SMENR is 1.	R/W

37.2.12 SPI Mode Option Setting Register (SMOPR)

The SMOPR register is a 32-bit register that sets the option data in SPI operating mode.
The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 502Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	OPD3[7:0]								OPD2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OPD1[7:0]								OPD0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	OPD0[7:0]	Option Data 0	Sets the option data 0.	R/W
b15 to b8	OPD1[7:0]	Option Data 1	Sets the option data 1.	R/W
b23 to b16	OPD2[7:0]	Option Data 2	Sets the option data 2.	R/W
b31 to b24	OPD3[7:0]	Option Data 3	Sets the option data 3.	R/W

Note: OPD3, OPD2, OPD1, and OPD0 are output in this order.

37.2.13 SPI Mode Enable Setting Register (SMENR)

The SMENR register is a 32-bit register that sets the bit size of the command, optional command, address, option data, and transfer data in SPI operating mode and enables various outputs. Disabling output of all of the command, optional command, address, option data, dummy cycle, and transfer data is prohibited. At least one of them except dummy cycle must be enabled.

The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CDB[1:0]		OCDB[1:0]		—	—	ADB[1:0]		—	—	OPDB[1:0]		—	—	SPIDB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DME	CDE	—	OCDE	ADE[3:0]				OPDE[3:0]				SPIDE[3:0]			
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	SPIDE[3:0]	Transfer Data Enable	Sets transfer data. The settings below must be used. Otherwise, the operation is not guaranteed. b3 b0 0000: Not transferred 1000: 8 bits transferred (enables data at address 0 of the SPI mode read/write data registers 0) 1100: 16 bits transferred (enables data at addresses 0 and 1 of the SPI mode read/write data registers 0) 1111: 32 bits transferred (enables data at addresses 0 to 3 of the SPI mode read/write data registers 0) Other than above: Setting prohibited	R/W
b7 to b4	OPDE[3:0]	Option Data Enable	Sets the option data to be output. Use only the settings given below. Otherwise, the operation cannot be guaranteed. b7 b4 0000: Output disabled 1000: OPD3 1100: OPD3, OPD2 1110: OPD3, OPD2, OPD1 1111: OPD3, OPD2, OPD1, OPD0 Other than above: Setting prohibited	R/W
b11 to b8	ADE[3:0]	Address Enable	Sets the address to be output. Use only the settings given below. Otherwise, the operation cannot be guaranteed. b11 b8 0000: Output disabled 0100: ADR[23:16] 0110: ADR[23:8] 0111: ADR[23:0] 1111: ADR[31:0] Other than above: Setting prohibited	R/W
b12	OCDE	Optional Command Enable	Sets the optional command to be output. 0: Optional command output disabled 1: Optional command output enabled	R/W
b13	—	Reserved	This bit is always read as 0. The write value should always be 0.	R/W
b14	CDE	Command Enable	Sets the command to be output. 0: Command output disabled 1: Command output enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b15	DME	Dummy Cycle Enable	Enables insertion of the dummy cycle before the read data. Note 1. Dummy cycle insertion is prohibited for write in SPI operating mode including the case in which a transfer ends with a dummy cycle. Note 2. A setting is prohibited for a transfer starting with a dummy cycle. 0: Dummy cycle insertion disabled 1: Dummy cycle insertion enabled	R/W
b17, b16	SPIDB[1:0]	Transfer Data Bit Size	Sets the transfer data size in bit units. b17 b16 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b19, b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b21, b20	OPDB[1:0]	Option Data Bit Size	Sets the option data size in bit units. b21 b20 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b23, b22	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b25, b24	ADB[1:0]	Address Bit Size	Sets the address size in bit units. b25 b24 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b27, b26	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b29, b28	OCDB[1:0]	Optional Command Bit Size	Sets the optional command size in bit units. b29 b28 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b31, b30	CDB[1:0]	Command Bit Size	For details, see the details about the serial flash memory to be used. b31 b30 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W

37.2.14 SPI Mode Read Data Register 0 (SMRDR0)

The SMRDR0 register is a 32-bit register that stores the read data in SPI operating mode.
The setting of this register should be read when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.
The alignment of data depends on the access size. For details, see section 37.3.4, Data Alignment.
This register must be accessed in the same unit as the transfer size set in the SPIDE[3:0] bits in the SPI mode enable register (SMENR). It must also be accessed from its own address 0.

Address(es): A000 5038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RDATA0[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RDATA0[31:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	RDATA0 [31:0]	Read Data	Holds the data read in SPI operating mode.	R

The contents of this register are modified upon completion of reception in SPI operating mode. Be sure to read data when reception in SPI operating mode is completed.

37.2.15 SPI Mode Write Data Register 0 (SMWDR0)

The SMWDR0 register is a 32-bit register that sets the write data in SPI operating mode.
The setting of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.
The alignment of data depends on the access size. For details, see section 37.3.4, Data Alignment.
This register must be accessed in the same unit as the transfer size set in the SPIDE[3:0] bits in the SPI mode enable register (SMENR). It must also be accessed from its own address 0.

Address(es): A000 5040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	WDATA0[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WDATA0[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	WDATA0 [31:0]	Write Data	Holds the data to be written in SPI operating mode.	R/W

37.2.16 Common Status Register (CMNSR)

The CMNSR register is a 32-bit register that holds flags indicating the operating state.
The settings of this register are reflected both in external address space read mode and SPI operating mode.

Address(es): A000 5048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSLF	TEND
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	TEND	Transfer End Flag	Indicates whether the data transfer has ended. 0: Indicates that data transfer is in progress. 1: Indicates that data transfer has ended.	R
b1	SSLF	SPBSSL Pin Monitor	0: SPBSSL pin is inactive. 1: SPBSSL pin is active.	R
b31 to b2	—	Reserved	These bits are always read as 0.	R

37.2.17 Data Read Dummy Cycle Setting Register (DRDMCR)

The DRDMCR register is a 32-bit register that sets the size and number of dummy cycles to be inserted in external address space read mode.

The settings of this register are enabled when the DME bit in the data read enable setting register (DRENR) is 1.

The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMDB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMCYC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	DMCYC [2:0]	Number of Dummy Cycles	Sets the number of dummy cycles to be inserted when the DME bit in the data read enable setting register (DRENR) is 1. b2 b0 000: 1 cycle 001: 2 cycles 010: 3 cycles 011: 4 cycles 100: 5 cycles 101: 6 cycles 110: 7 cycles 111: 8 cycles	R/W
b15 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	DMDB [1:0]	Dummy Cycle Bit Size	Sets the dummy cycle size in bit units. The setting of these bits is combined with the setting of the IO0FV, IO2FV, and IO3FV bits in the common control register (CMNCR) to determine the state of the unused pins during the dummy cycles. The state of the used pins is Hi-Z. b17 b16 0 0: 1 bit 0 1: 2 bits 1 0: 4 bits 1 1: Setting prohibited	R/W
b31 to b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.2.18 SPI Mode Dummy Cycle Setting Register (SMDMCR)

The SMDMCR register is a 32-bit register that sets the size and number of dummy cycles to be inserted in SPI operating mode.

The settings of this register are enabled when the DME bit in the SPI mode enable setting register (SMENR) is 1.

The settings of this register should be changed when the TEND flag in CMNSR is 1; otherwise, the operation cannot be guaranteed.

Address(es): A000 5060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMDB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMCYC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	DMCYC[2:0]	Number of Dummy Cycles	Sets the number of dummy cycles to be inserted when the DME bit in the SPI mode enable setting register (SMENR) is 1. b2 b0 000: 1 cycle 001: 2 cycles 010: 3 cycles 011: 4 cycles 100: 5 cycles 101: 6 cycles 110: 7 cycles 111: 8 cycles	R/W
b15 to b3	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b17, b16	DMDB [1:0]	Dummy Cycle Bit Size	Sets the dummy cycle size in bit units. The setting of these bits is combined with the setting of the IO0FV, IO2FV, and IO3FV bits in the common control register (CMNCR) to determine the state of the unused pins during the dummy cycles. The state of the used pins is Hi-Z. b17 b16 00: 1 bit 01: 2 bits 10: 4 bits 11: Setting prohibited	R/W
b31 to b18	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

37.3 Operation

37.3.1 System Configuration

With this module, one serial flash memory can be directly connected (data size of 1, 2, and 4 bits).
Figure 37.2 shows a system configuration example.

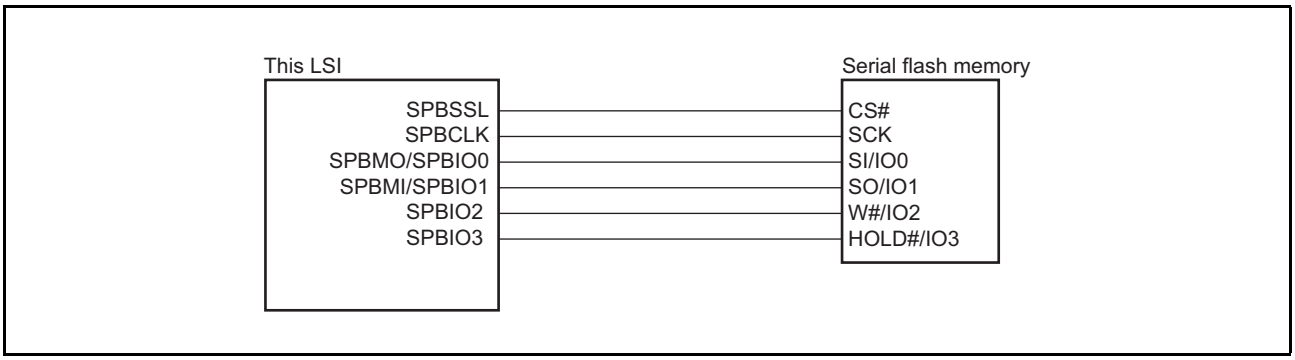


Figure 37.2 System Configuration Example with 4-Bit Data Size of a Serial Flash Memory Connected (BSZ[1:0] Bits in CMNCR = 00)

37.3.2 Address Map

In external address space read mode, the serial flash connected is assigned in the SPI multi I/O bus space. By the DREAR register setting, a maximum of 4 Gbytes can be accessed.

Table 37.4 Address Map

Number of Serial Flash Memories Connected	Internal Address	Max. Access Area
1	1000 0000h to 13FF FFFFh	4 Gbytes
	3000 0000h to 33FF FFFFh (mirror area)	

37.3.3 32-Bit Serial Flash Addresses

Since the SPI multi I/O bus space is 64 Mbytes, only a part of the 32-bit serial flash address area can be directly accessed. Here, the fixed value set in the DREAR register is used as the upper bit value of a 32-bit address.

To output serial flash addresses in 32 bits, set the ADE[3] bit in DRENR to 1, set the range of the external addresses used as the serial flash addresses to the EAC[2:0] bits in DREAR, and set the upper bit value of the 32-bit address as the fixed value to the EAV[7:0] bits in DREAR.

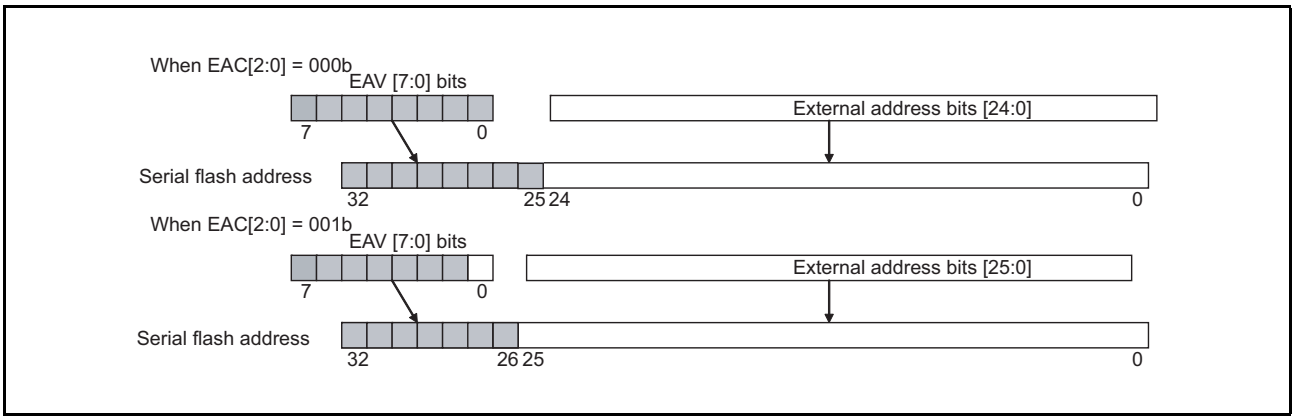


Figure 37.3 32-Bit Address Setting

Setting the ADE[3] bit in DRENR to 1 allows the serial flash address to be output using [31:0] bits.

When EAC[2:0] = 000b, external address bits [24:0] are valid; set the value for [32:25] bits to EAV[7:0].

When EAC[2:0] = 001b, external address bits [25:0] are valid; set the value for [32:26] bits to EAV[7:1].

When one serial flash memory is connected, address bits [31:0] are used.

37.3.4 Data Alignment

Data alignment can be set by using the SFDE bit in the common control register (CMNCR). Data alignment in data read mode and in SPI mode are shown in Figure 37.4 and Figure 37.5, respectively.

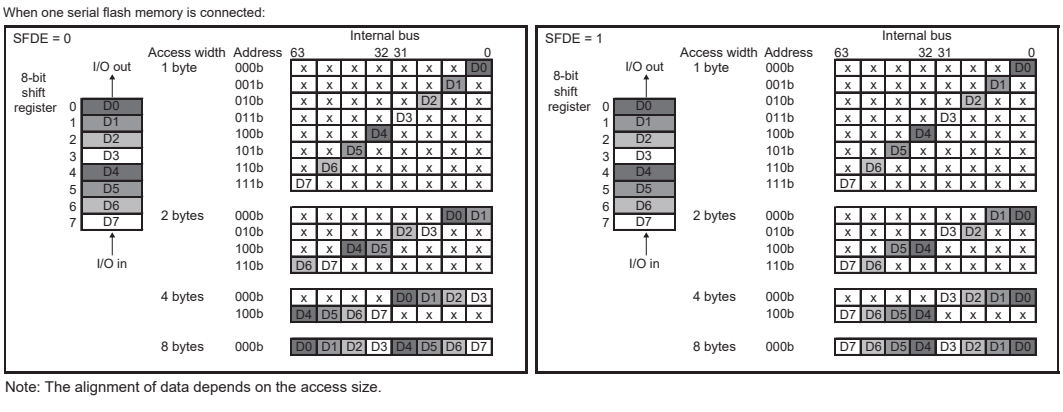


Figure 37.4 Data Alignment in External Address Space Read Mode

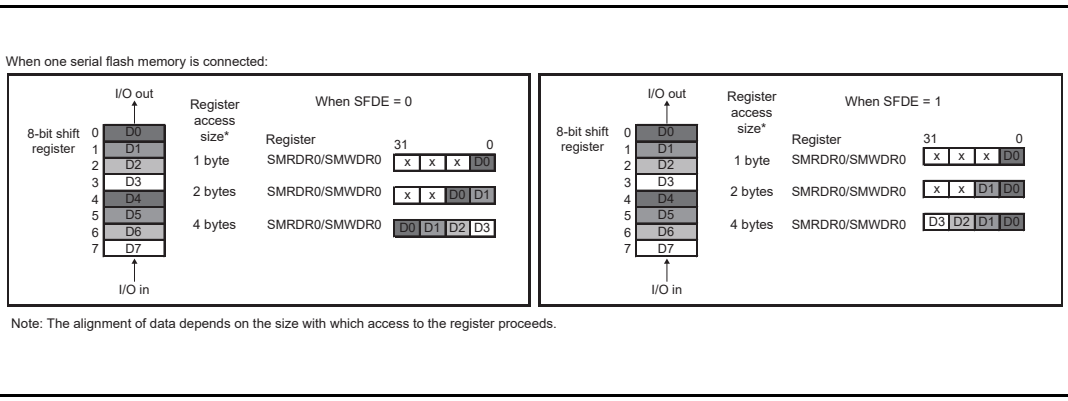


Figure 37.5 Data Alignment in SPI Operating Mode

37.3.5 Operating Modes

This module has two operating modes: external address space read mode and SPI operating mode.
In external address space read mode, a read access to the SPI multi I/O bus space is converted into SPI communication and data is received. After data acquisition, data is returned to the bus master that is the issuing source. For details, see section 37.3.6, External Address Space Read Mode.
In SPI operating mode, arbitrary SPI communication is carried out based on the register settings. For details, see section 37.3.8, SPI Operating Mode.

37.3.6 External Address Space Read Mode

A read access to the SPI multi I/O bus space can be converted into SPI communication in external address space read mode. Further, the commands, optional commands, option data, and dummy cycle issued for reading can be modified by the register settings.
In external address space read mode, either normal read operation or burst read operation can be selected. The transfer format is determined by the settings of the common control register (CMNCR), SSL delay register (SSLDR), bit rate setting register (SPBCR), data read control register (DRCR), data read command setting register (DRCMR), data read extended address setting register (DREAR), data read option setting register (DROPR), data read enable setting register (DRENR), and data read dummy cycle setting register (DRDMCR).

(1) Normal Read Operation

When the RBE bit in DRCR is set to 0, normal read operation is performed.
In the normal read operation, the data of 8 bits, 16 bits, and 32 bits are read for respectively a byte, a word, and a longword read access. After reading, the SPBSSL signal is inactivated.
The normal read operation timing is shown in Figure 37.6.
t1 is the time period from the time the SPBSSL signal is activated to the time the clock is output from the SPBCLK signal (clock delay). t2 is the time period from transmission of the last edge of the SPBCLK signal of a transfer to the time the SPBSSL signal is inactivated (SPBSSL negation delay). t3 is the time period from one transfer end to the next transfer start (next access). For details of t1, t2, and t3, see section 37.3.9, Transfer Format.

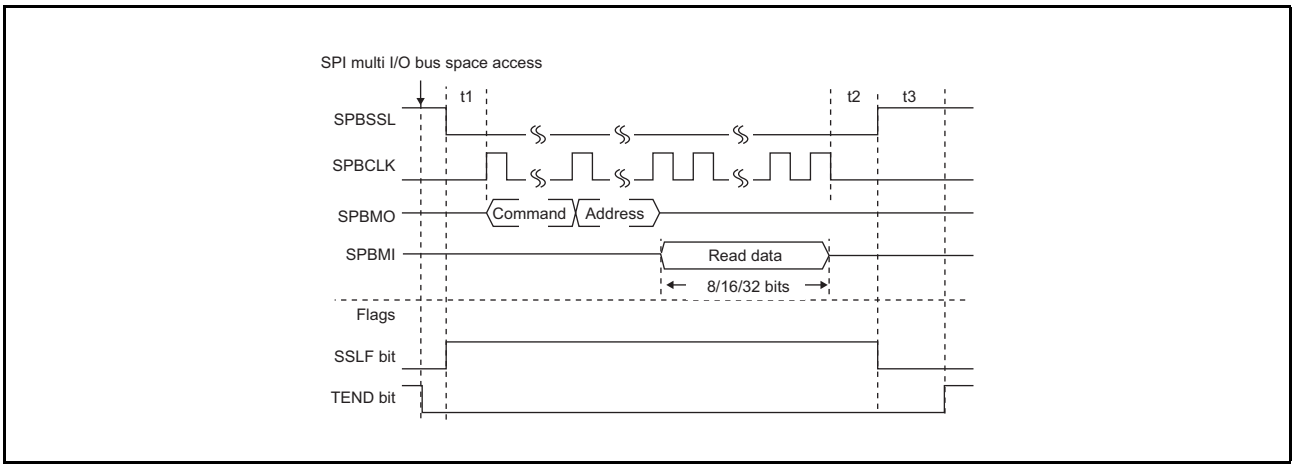


Figure 37.6 Normal Read Operation Timing

(2) Burst Read Operation

When the RBE bit in DRCR is set to 1, burst read operation is performed. Read cache is enabled in the burst read operation. For read cache operation, see section 37.3.7, Read Cache.

For reading bytes, words, or longwords, the read cache is first referred to for the data. When the read cache contains the data, the data is read from the read cache without accessing the serial flash memory. When the read cache does not contain the data, burst read operation is performed in the serial flash memory and the read data is stored in the read cache. The data transfer length at that time is 64 bits × RBURST[3:0] bits and the data is always read from the 64-bit boundary.

The status of the SPBSSL signal after data transfer can be selected by using the SSLE bit in DRCR. When the SSLE bit is set to 0, the SPBSSL signal is always inactivated after data transfer. For an operation performed when the SSLE bit is set to 1, see section 37.3.6, (3) Burst Read Operation with Automatic SPBSSL Inactivation, just below.

A pattern diagram of this operation and a burst read operation timing diagram when SSLE bit is set to 0 are shown in Figure 37.7 and Figure 37.8.

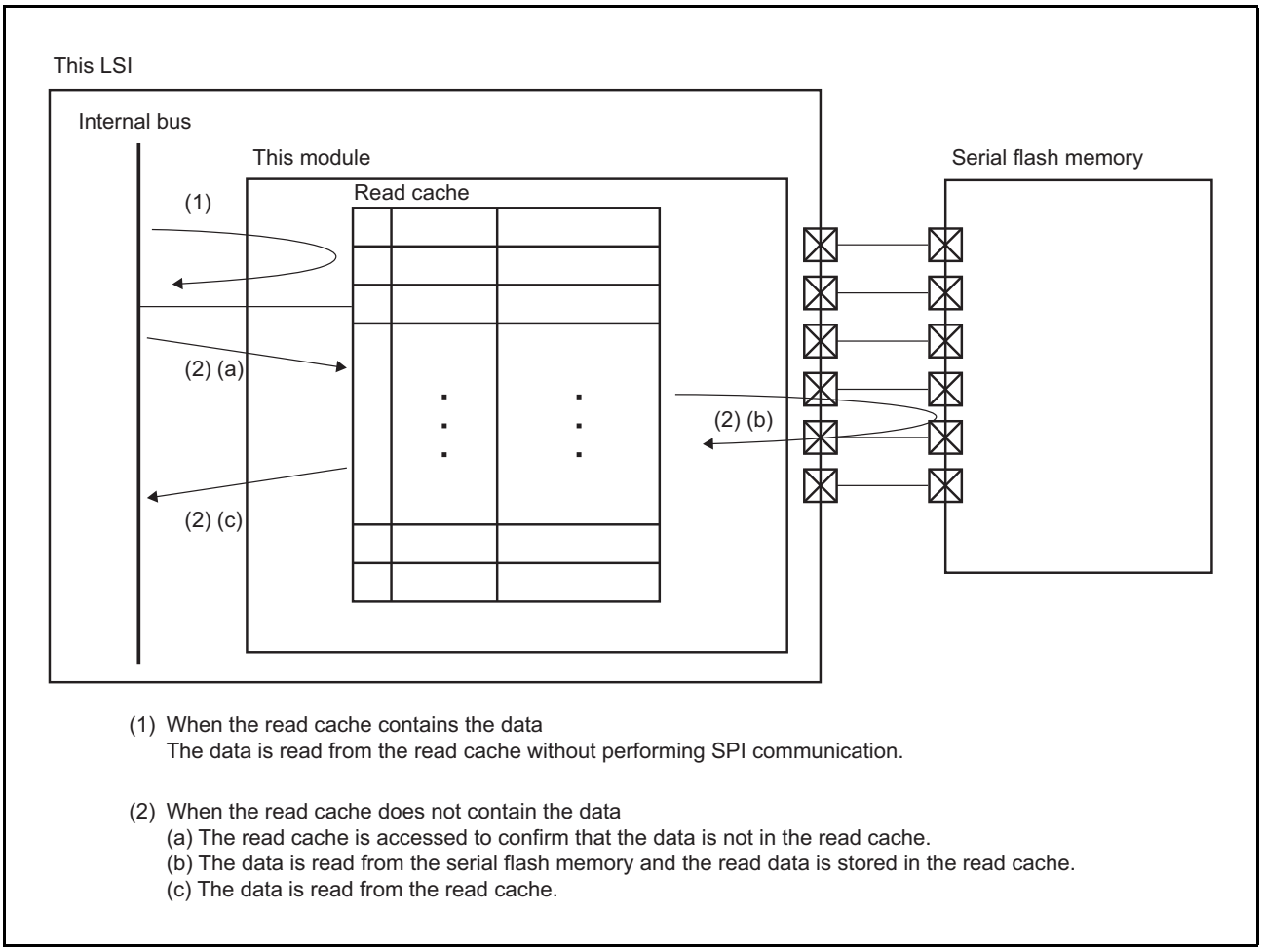


Figure 37.7 Burst Read Operation

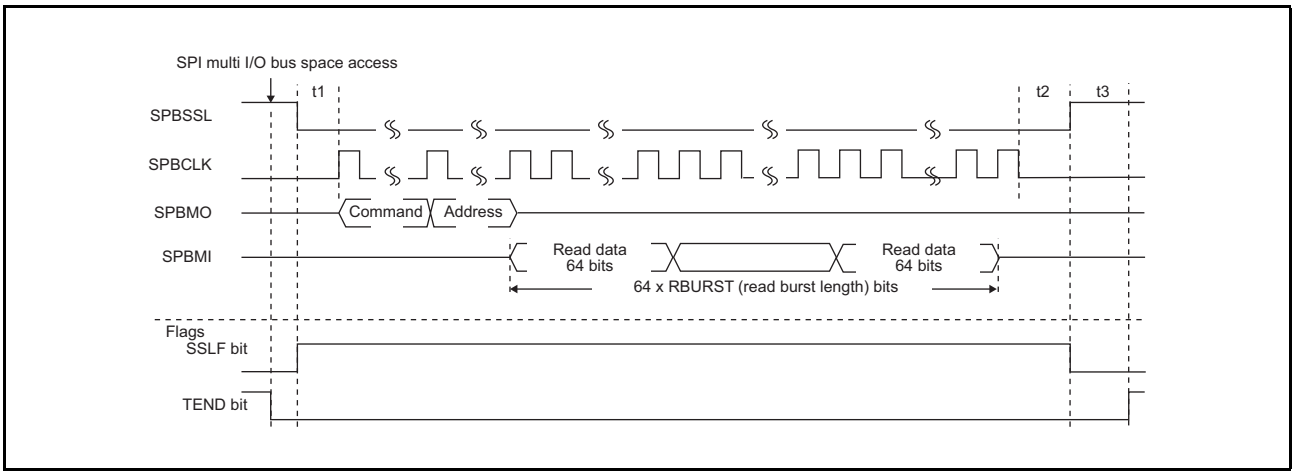


Figure 37.8 Burst Read Operation Timing (SSLE Bit = 0)

(3) Burst Read Operation with Automatic SPBSSL Inactivation

When SSLE bit in DRCR is set to 1, this module does not inactivate the SPBSSL signal after the burst read transfer. When accessing the next time, if the address is continuous with the previous read address, the burst read operation is performed without issuing the command, optional command, address, option data, or dummy cycle. If the address is not continuous with the previous read address, the SPBSSL signal is once inactivated and the burst read operation is performed after issuing the command, optional command, address, option data, or dummy cycle.
Burst read timing diagrams for continuous address and non-continuous address are shown in Figure 37.9 and Figure 37.10.

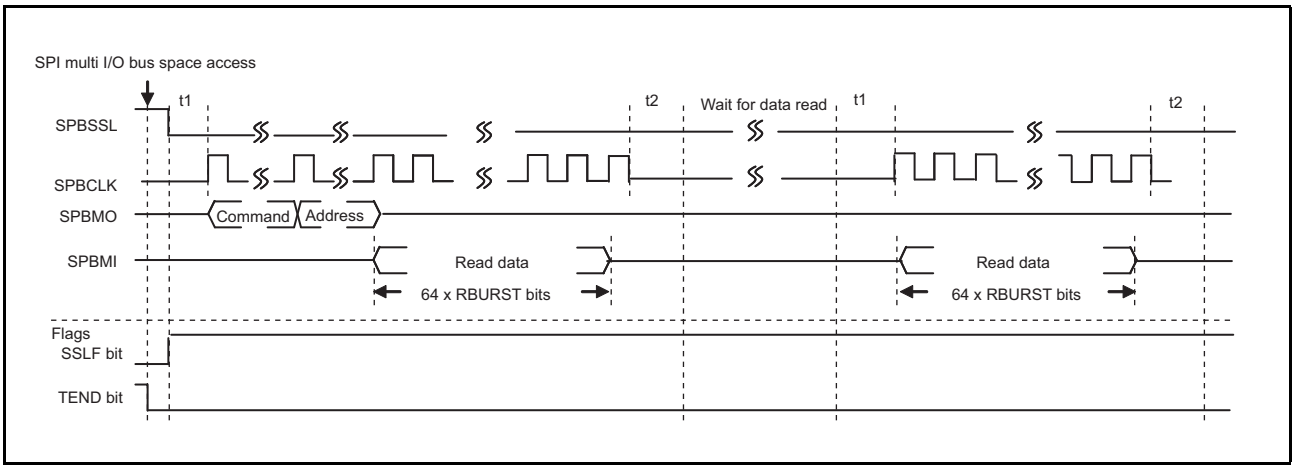


Figure 37.9 Burst Read Timing for Continuous Address (SSLE Bit = 1)

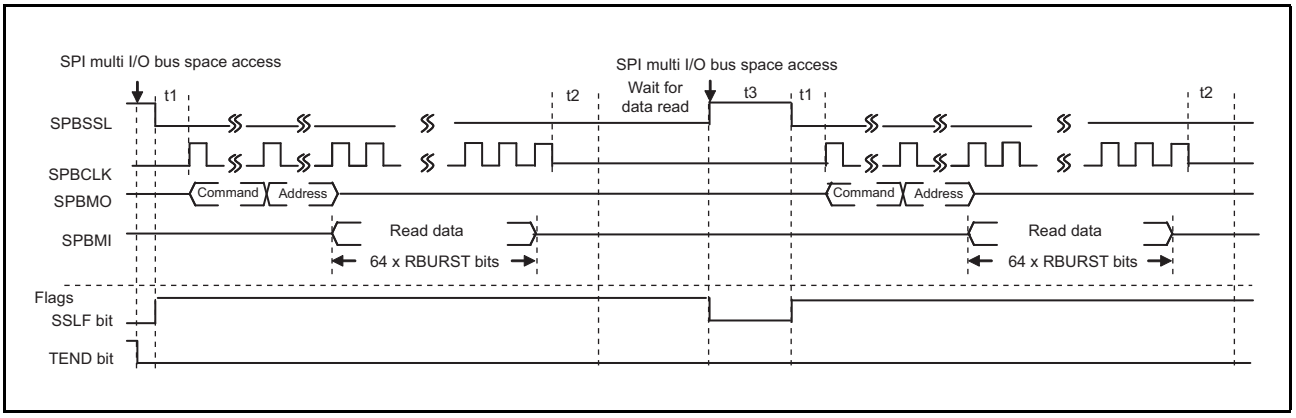


Figure 37.10 Burst Read Timing for Non-Continuous Address (SSLE Bit = 1)

For the next access after inactivation of the SPBSSL signal with the SSLN bit in DRCR with this operation, read SSLF = 0 in CMNSR to confirm that the SPBSSL signal has been inactivated.

(4) Initial Setting Flow

An example of an initial setting flow in external address space read mode is shown in Figure 37.11.

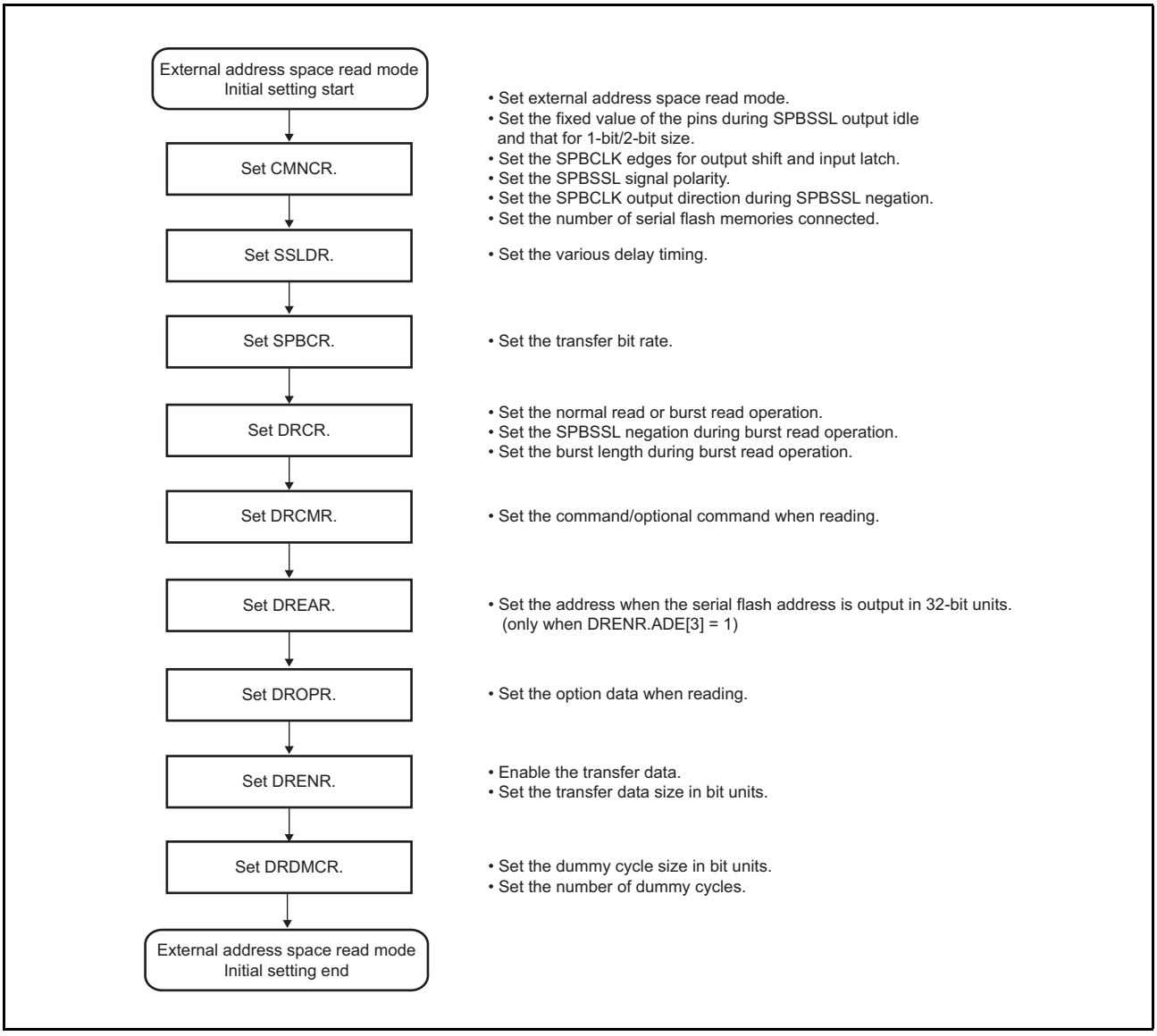


Figure 37.11 Example of Initial Setting Flow in External Address Space Read Mode

37.3.7 Read Cache

This module has a simple built-in read cache. The read cache can be used during external address space read mode and burst read operation. The read cache is configured with a line size of 64 bits and 16 entries.
Read cache configuration is shown in Figure 37.12.

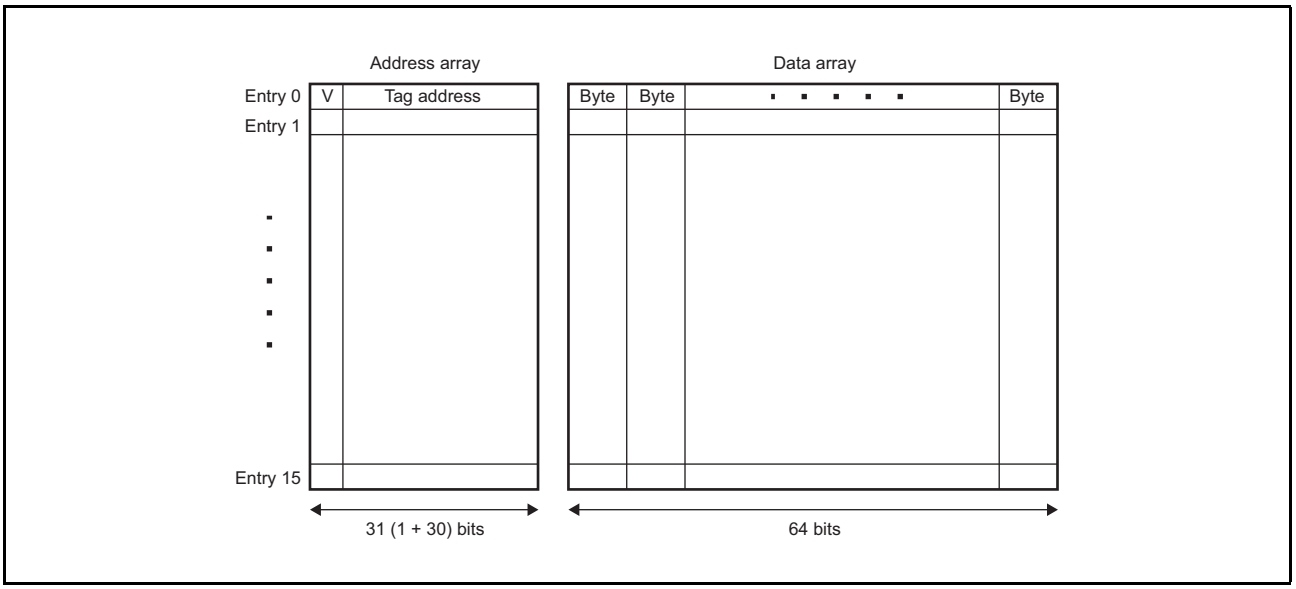


Figure 37.12 Read Cache Configuration

(1) Address Array

The V bit in Figure 37.12 indicates whether the entry data is valid. When the V bit is 1, the data is valid and when V bit is 0, the data is invalid.
The tag address bits hold the address used by the serial flash memory. An address is composed of bits 32 to 3. Address bits 23 to 3 are enabled when address output is 24 bits.
Address bits 31 to 3 are enabled when address output is 32 bits.

(2) Data Array

It retains the 64-bit read data. Registration in the read cache is performed in line units.

(3) Read Operation

If read data is hit in the cache, data is read from the read cache. In case of miss-hit, after the 64 × RBURST (read burst length) data is read from the serial flash memory and the read cache is updated, the data is returned to the bus master.

(4) Data Replacement

Data update is managed by the write pointer. In case of miss-hit of read data, the RBURST (read burst length) portion data is replaced starting at the entry specified by the write pointer. In other words, the data is replaced in the storage order of the data. Whether data is referred to or not will not affect the replacement order of data.

37.3.8 SPI Operating Mode

This module can carry out an arbitrary SPI operation by using the register settings.
The transfer format is determined by the settings of the common control register (CMNCR), SSL delay register (SSLDR), bit rate setting register (SPBCR), SPI mode control register (SMCR), SPI mode command setting register (SMCMR), SPI mode address setting register (SMADR), SPI mode option setting register (SMOPR), and SPI mode enable setting register (SMENR), SPI mode read data register (SMRDR), SPI mode write data register (SMWDR), and SPI mode dummy cycle setting register (SMDMCR).
SPI operating mode can be used for reading the status of the serial flash memory and writing to the serial flash memory. In this mode, one transfer refers to the operation from when the SPIE bit in SMCR is set to 1 to when the TEND bit is set to 1.

(1) Transfer Start

The transfer of data is started in the set transfer format by setting the SPIE bit in SMCR to 1. When write operation is enabled, the SPI mode write data register is transmitted to the serial flash memory. When read operation is enabled, data read from the serial flash memory is stored into the SPI mode read data register.
The SPI operation timing is shown in Figure 37.13.

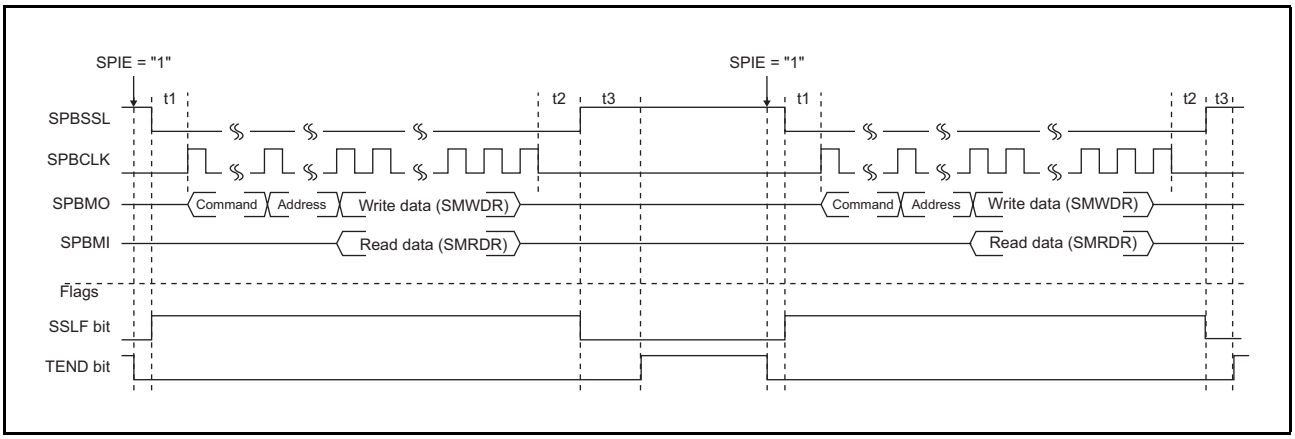


Figure 37.13 SPI Operation Timing

(2) Read/Write Enable

- Read operation: Data can be read by setting the SPIRE bit in SMCR to 1. The read data is stored into SMRDR.
- Write operation: Data can be written by setting the SPIWE bit in SMCR to 1. The data stored in SMWDR is output.

When the data size is set to 1 bit using the SPIDB[1:0] bits in SMENR, data can be transmitted and received by setting the SPIRE and SPIWE bits to 1. However, when the data size is set to 2 or 4 bits by using the SPIDB[1:0] bits, only one of the SPIRE and SPIWE bits should be enabled. The operation is not guaranteed if both the bits are enabled.

(3) Retention of SPBSSL Pin Activation

By setting the SSLKP bit in SMCR to 1, activation of the SPBSSL signal can be continued till the next transfer. With this function, the transfer can be carried out continuously with the SPBSSL signal kept in the active state.
The data transfer timing using the SSLKP bit is shown in Figure 37.14.

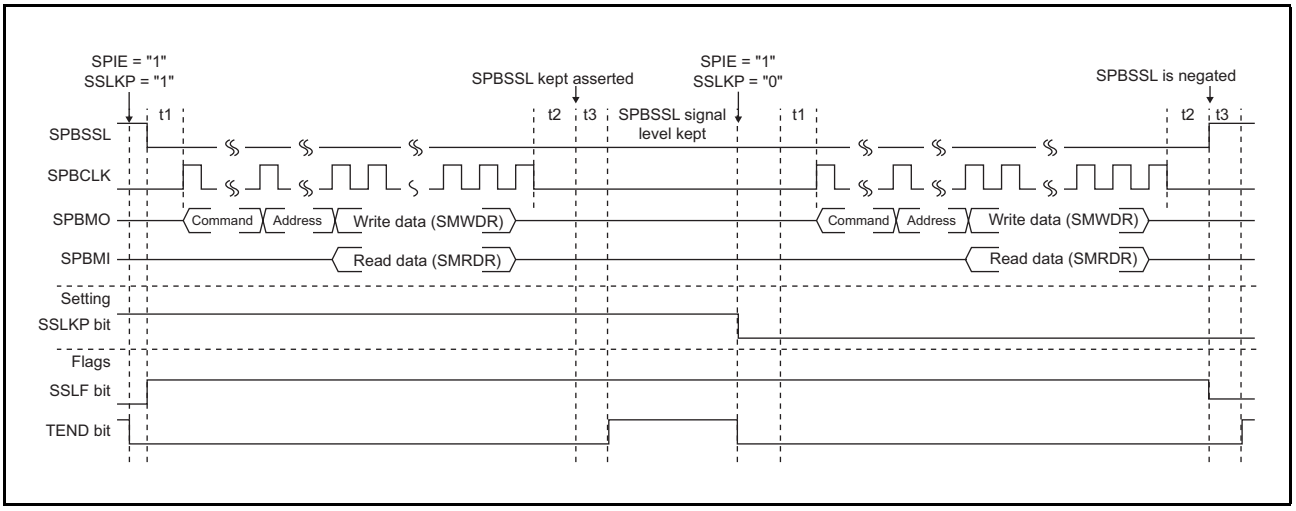


Figure 37.14 Data Transfer Timing using the SSLKP Bit

(4) Initial Setting Flow

An example of an initial setting flow in SPI operating mode is shown in Figure 37.15.

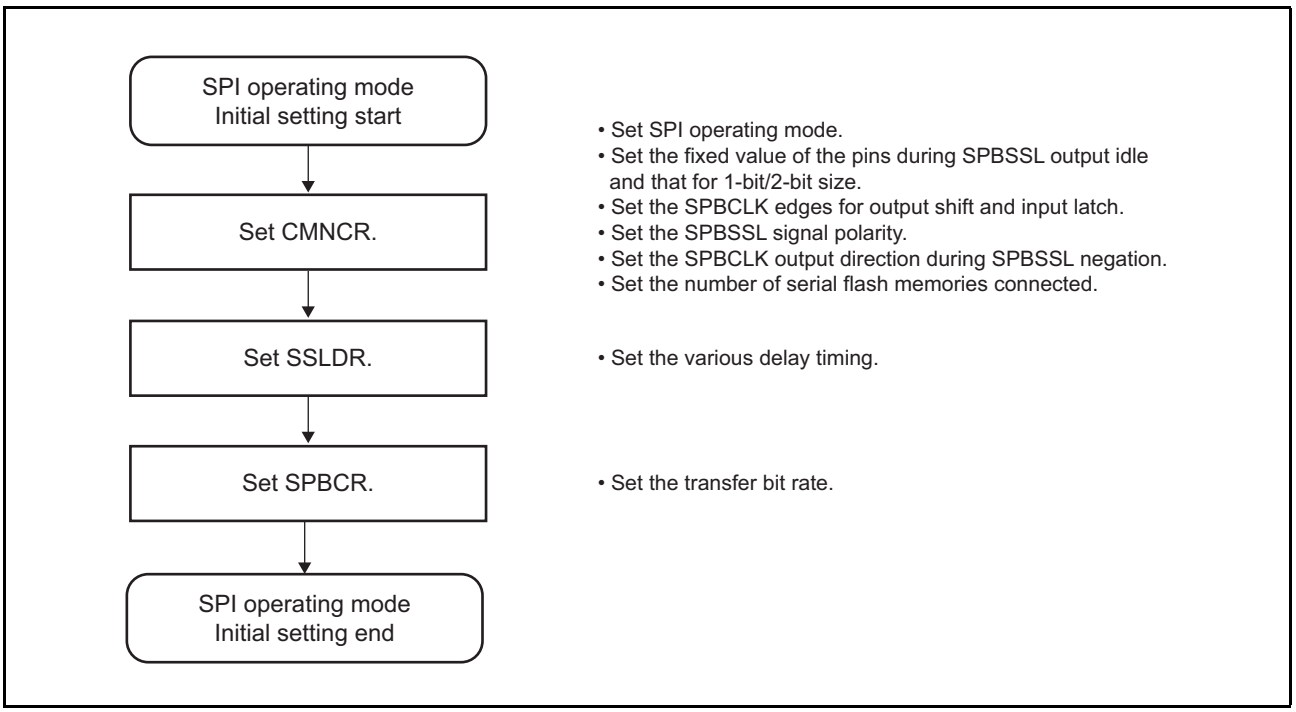


Figure 37.15 Example of Initial Setting Flow in SPI Operating Mode

(5) Data Transfer Setting Flow

An example of a data transfer setting flow in SPI operating mode is shown in Figure 37.16.

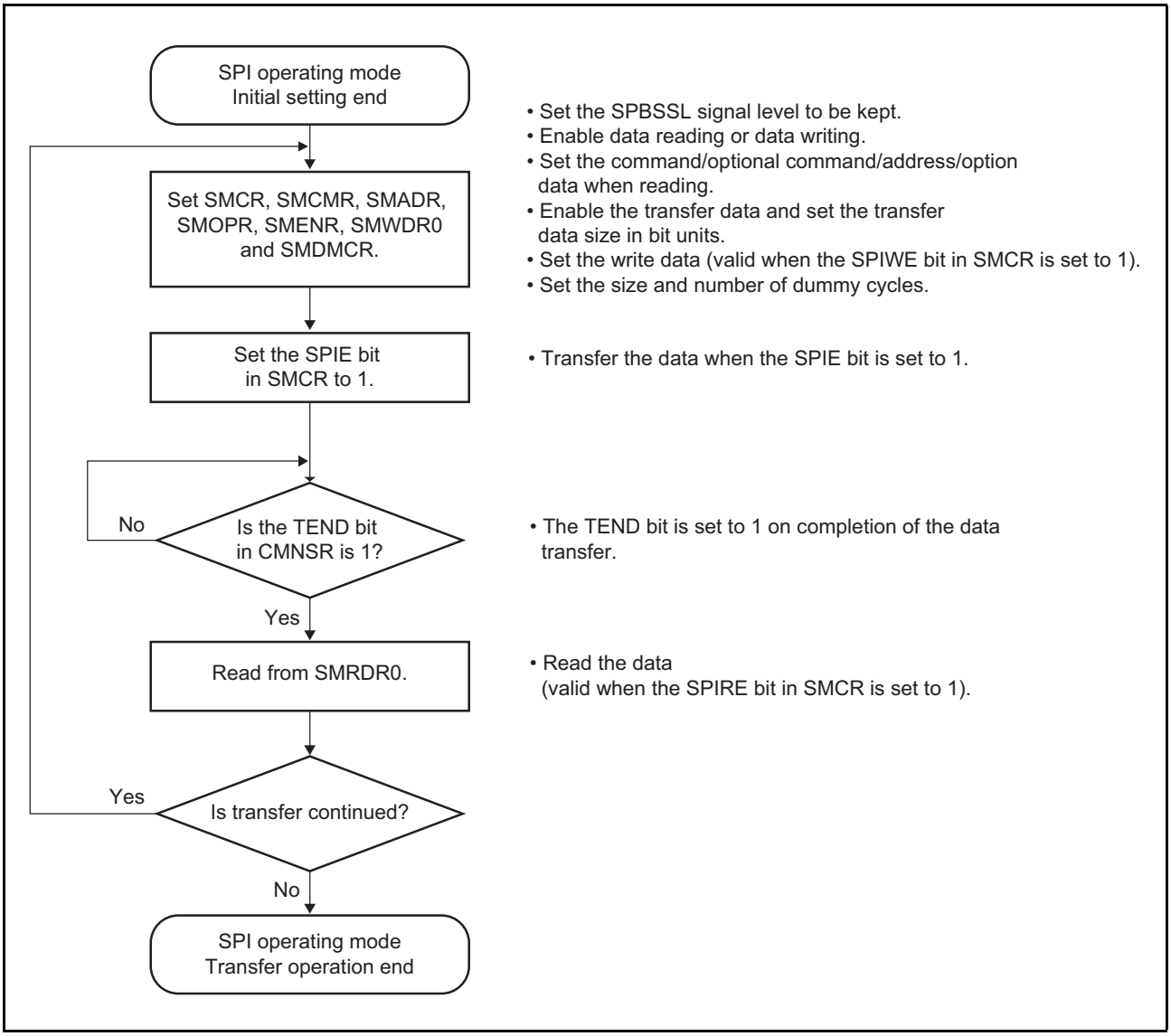


Figure 37.16 Example of a Data Transfer Setting Flow in SPI Operating Mode

37.3.9 Transfer Format

(1) SPBSSL Pin Enable Polarity Control

The enable polarity of the SPBSSL signal can be changed with the SSLP bit in CMNCR.

(2) SPBCLK Output

The output level of the SPBCLK signal while the SPBSSL signal is inactive can be set with the CPOL bit in CMNCR.

(3) Data Transmission and Reception Timing

Data is transmitted and received at either the odd or even edges. The data transmission timing can be set to the odd or even edge with the CPHAT bit in CMNCR. Similarly, the data reception timing can be set to the odd or even edge with the CPHAR bit in CMNCR.

(4) Delay Settings

t1 is the time period from the time the SPBSSL signal is activated to the clock output of the SPBCLK signal (clock delay). It can be set with the SCKDL[2:0] bits in SSLDR. t2 is the time period from the time the clock output of the SPBCLK signal is stopped to the time the SPBSSL signal is inactivated (SPBSSL negation delay). It can be set with the SLNDL[2:0] bits in SSLDR. t3 is the time period required to prevent SPBSSL signal activation for the next transfer after the end of the previous transfer (next access delay). It can be set with the SPNDL[2:0] bits in SSLDR.

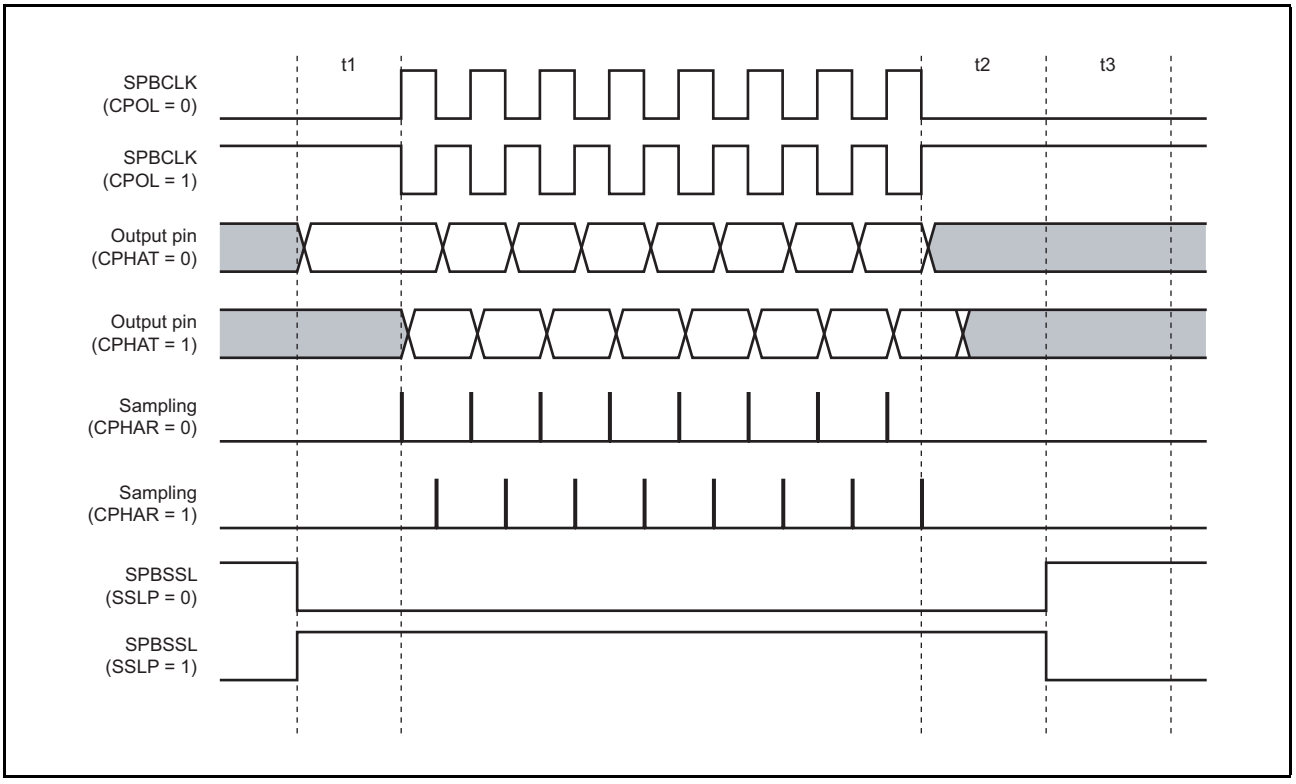


Figure 37.17 SDR Transfer Format

37.3.10 Data Format

This module can input and output data in the order of command, optional command, address, option data, dummy cycle, and data.

(1) Data Registers

Table 37.5 shows the input and output data.

Table 37.5 Data Registers

Data	External Address Space Read Mode	SPI Operating Mode
Command (8 bits)	CMD[7:0] bits in DRCMR	CMD[7:0] bits in SMCMR
Optional command (8 bits)	OCMD[7:0] bits in DRCMR	OCMD[7:0] bits in SMCMR
Address (32/24 bits)	32 bits: DREAR.EAV[6:1 to 0] bits + lower [25 to 24:0] bits of the read address. 24 bits: Lower [23:0] bits of the read address	32 bits: ADR[31:0] bits in SMADR 24 bits: ADR[23:0] bits in SMADR
Option data (8 bits × 4)	DROPR	SMOPR
Dummy cycle (1 to 8 cycles)	DRDMCR	SMDMCR (only when read)
Transfer data	Normal read: 8/16/32 bits Burst read: 64 × RBURST bits	Read: SMRDR0, SMRDR1 Write: SMWDR0, SMWDR1

(2) Data Enable

In external address space read mode, transfer enable of the command, optional command, address, option data, and dummy cycle can be controlled with the CDE, OCDE, ADE[3:0], OPDE[3:0], and DME bits in DRENR, respectively. The size and number of dummy cycles can be controlled with the data read dummy cycle setting register (DRDMCR). Similarly, in SPI operating mode, enable of the command, optional command, address, option data, dummy cycle, and transfer data can be controlled with the CDE, OCDE, ADE[3:0], OPDE[3:0], DME, and SPIDE[3:0] bits in SMENR, respectively. However, disabling all the above parameters is prohibited in SPI operating mode. At least one of them except dummy cycle must be enabled. The size and number of dummy cycles can be controlled with the SPI mode dummy cycle setting register (SMDMCR).

For the address and option data in external address space read mode; and the address, option data, and transfer data in SPI operating mode, the enable bit setting allowed is determined according to the transfer data size. For the allowed setting combinations of the enable bits and transfer data size, refer to the description of the pertinent register.

If these enable bits are disabled, the data is not output, and input and output of the next data is carried out. The command, optional command, address, and option data are always output. During dummy cycles, the state of the used pins is Hi-Z. In external address space read mode, data is always input; and in SPI operating mode, input and output of data is determined based on the settings of the SPIRE and SPIWE bits in SMCR.

There are some restrictions on dummy cycle insertion; refer to the description of the DME bits in DRENR and SMENR for details.

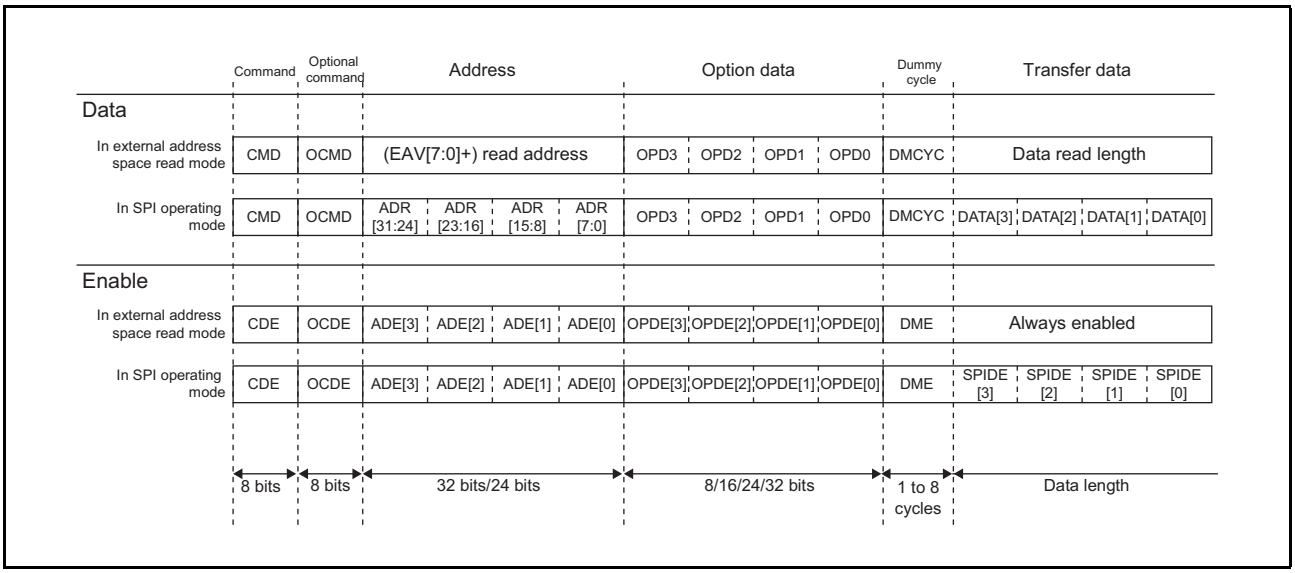


Figure 37.18 Data and Enable

(3) Bit Size

In external address space read mode, the size of the command, optional command, address, option data, and the read data in bit units is respectively controlled with the CDB[1:0], OCDB[1:0], ADB[1:0], OPDB[1:0], and DRDB[1:0] bits in DRENR. The size of the dummy cycle in bit units is also controlled with the DMDB[1:0] bits in DRDMCR.
Similarly, in SPI operating mode, the size of the command, optional command, address, option data, and read write data in bit units is controlled with the CDB[1:0], OCDB[1:0], ADB[1:0], OPDB[1:0], and SPIDB[1:0] bits in SMENR. The size of the dummy cycle in bit units is also controlled with the DMDB[1:0] bits in SMDMCR.

(a) 1-bit size

When the size is set to 1 bit, SPBMI pin will be the input pins and SPBMO pin will be the output pins. SPBIO2, and SPBIO3 pins are not used.
Figure 37.19 show the transfer format example.

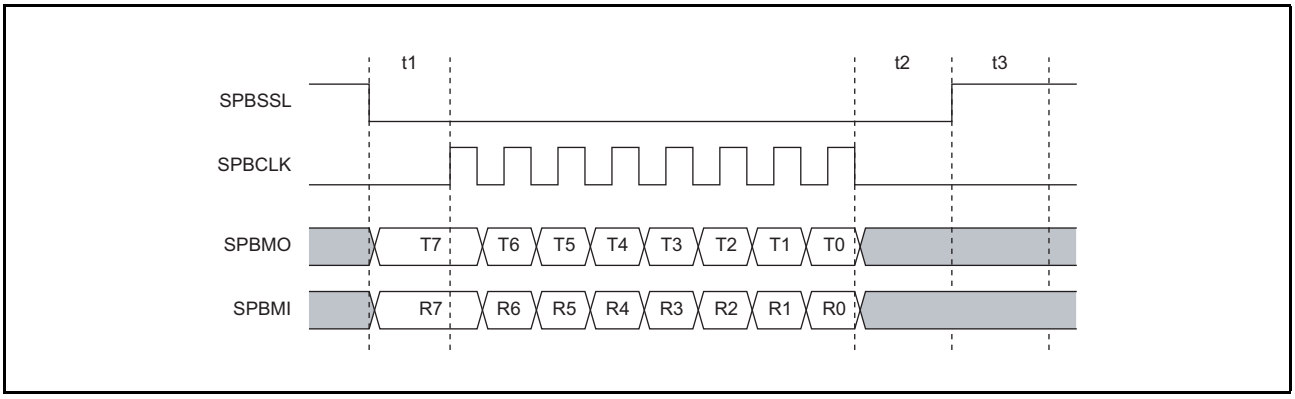


Figure 37.19 Transfer Format Example with 1-Bit Data Size and One Serial Flash Memory Connected

(b) 2-bit size

When the size is set to 2 bits, SPBIO0 and SPBIO1 pins will be either the input pins or the output pins. SPBIO2, and SPBIO3 pins are not used.
Figure 37.20 show the transfer format example.

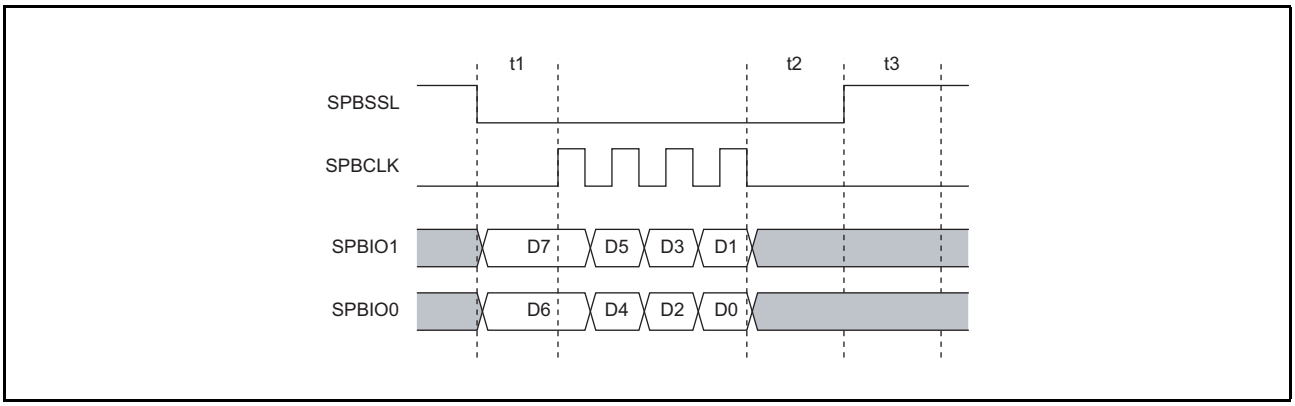


Figure 37.20 Transfer Format Example with 2-Bit Data Size and One Serial Flash Memory Connected

(c) 4-bit size

When the size is set to 4 bits, SPBIO0, SPBIO1, SPBIO2, and SPBIO3 pins will be either the input pins or the output pins.

Figure 37.21 show the transfer format examples.

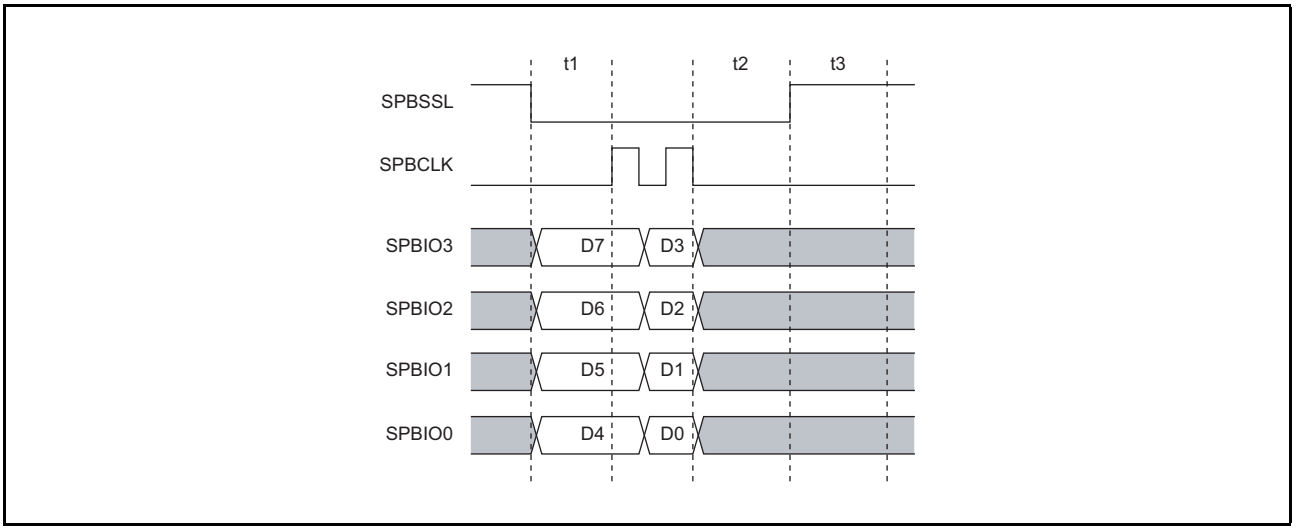


Figure 37.21 Transfer Format Example with 4-Bit Data Size and One Serial Flash Memory Connected

37.3.11 Data Pin Control

With this module, the status of pins can be automatically changed based on the data size to be used and the read/write settings. The inactivation status of the SPBSSL signal can be set with the MOIIO3, MOIIO2, MOIIO1, and MOIIO0 bits in CMNCR. The SPBSSL and SPBCLK pins are always output pins. The status of respective pins is specified in Table 37.6 to Table 37.9.

Table 37.6 Pin Status (1)

		SPBSSL Activation		
		Command, Optional Command, Address, Option Data		
Pin	**SPBSSL Inactivation**	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**
SPBMO/SPBIO0	MOIIO0 bit value	Output	Output	Output
SPBMI/SPBIO1	MOIIO1 bit value	Hi-Z	Output	Output
SPBIO2	MOIIO2 bit value	IO2FV bit value	IO2FV bit value	Output
SPBIO3	MOIIO3 bit value	IO3FV bit value	IO3FV bit value	Output

Table 37.7 Pin Status (2)

	Transfer Data					
	External Address Space Read Mode			SPI Operating Mode		
				SPIRE Bit = 1, SPIWE Bit = 0		
Pin	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**
SPBMO/SPBIO0	IO0FV bit value	Input	Input	IO0FV bit value	Input	Input
SPBMI/SPBIO1	Input	Input	Input	Input	Input	Input
SPBIO2	MOIIO2 bit value	MOIIO2 bit value	Input	MOIIO2 bit value	MOIIO2 bit value	Input
SPBIO3	MOIIO3 bit value	MOIIO3 bit value	Input	MOIIO3 bit value	MOIIO3 bit value	Input

Table 37.8 Pin Status (3)

	Transfer Data					
	SPI Operating Mode					
	SPIRE Bit = 0, SPIWE Bit = 1			SPIRE Bit = 1, SPIWE Bit = 1		
Pin	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**
SPBMO/SPBIO0	Output	Output	Output	Output	Setting prohibited	Setting prohibited
SPBMI/SPBIO1	Hi-Z	Output	Output	Input	Setting prohibited	Setting prohibited
SPBIO2	MOIIO2 bit value	MOIIO2 bit value	Output	MOIIO2 bit value	Setting prohibited	Setting prohibited
SPBIO3	MOIIO3 bit value	MOIIO3 bit value	Output	MOIIO3 bit value	Setting prohibited	Setting prohibited

Table 37.9 Pin Status (4)

	Dummy Cycle		
Pin	**1-Bit Size**	**2-Bit Size**	**4-Bit Size**
SPBMO/SPBIO0	IO0FV bit value	Hi-Z	Hi-Z
SPBMI/SPBIO1	Hi-Z	Hi-Z	Hi-Z
SPBIO2	IO2FV bit value	IO2FV bit value	Hi-Z
SPBIO3	IO3FV bit value	IO3FV bit value	Hi-Z

37.3.12 SPBSSL Pin Control

Inactivation conditions of the SPBSSL signal are as follows.

(1) External Address Space Read Mode

(a) Normal read operation (RBE bit in DRCR = 0)

SPBSSL inactivated after the data transfer and t2 cycle are completed.

(b) Burst read without automatic SPBSSL inactivation (RBE bit in DRCR = 1, SSLE bit in DRCR = 0)

SPBSSL inactivated after the data transfer and t2 cycle are completed.

(c) Burst read with automatic SPBSSL inactivation (RBE bit in DRCR = 1, SSLE bit in DRCR = 1)

- SPBSSL inactivated after t2 cycle when the read address is not continuous with the previously read address
- SPBSSL inactivated after the SSLN bit in DRCR is set to 1

(2) SPI Operating Mode

(a) SPBSSL pin activation not retained (SSLKP bit in SMCR = 0)

SPBSSL inactivated after the data transfer and t2 cycle are completed.

(b) SPBSSL pin activation retained (SSLKP bit in SMCR = 1)

SPBSSL not inactivated.
When to be inactivated, data should be transferred after setting the SSLKP bit to 0.

37.3.13 Flags

This module has two flag bits SSLF and TEND in CMNSR. These bits are read-only bits.

(1) SSLF Bit

This bit indicates the SPBSSL pin status. The status is 1 when the SPBSSL signal is active, and the status is 0 when the SPBSSL signal is inactive.

(2) TEND Bit

This bit indicates whether transfer of data is in progress or the transfer of data has ended.
During t1 time period, data transfer, t2 time period, t3 time period, and waiting for read access by burst read and SPBSSL automatic inactivation, the TEND bit is read as 0 to indicate that the transfer of data is in progress.
When other than the above, the TEND bit is read as 1 to indicate that transfer of data has ended.

(3) Register Re-writing Timing

The status of the TEND bit determines the rewritable registers.
The registers which can be written to, except the SSLN bit in DRCR, should be modified when TEND = 1.
Read SMRDR0 when TEND = 1.
CMNSR can always be read.

37.4 Usage Notes

37.4.1 Notes on Transfer to Read Data in SPI Operating Mode

If the setting for the bit mode is for division by two or more in SPI operating mode, take note of the following points for caution when setting the SPI mode enable setting register (SMENR) to enable transfer only for reading data.
“Transfer only for reading data” indicates transfer to read data while the CDE, OCDE, ADE[3:0], and OPDE[3:0] bits in SMENR are all 0.

(1) Transfer to read data while the signal on the SPBSSL pin is inactivated

Set the SMENR.SPIDE[3:0] bits to 1100b or 1111b when transfer only for reading data is to proceed.
Transfer will not proceed normally if the setting of the SMENR.SPIDE[3:0] bits is 1000b.

(2) Transfer to read data while the signal on the SPBSSL pin is activated

When transfer only for reading data is to proceed, set the SMENR.SPIDE[3:0] bits to 1100b or 1111b, or end the immediately preceding transfer with reading data.
When the immediately preceding transfer is of a command, optional command, address, or option data, or is transfer for writing data, the subsequent transfer only for reading data will not proceed normally if the setting of the SMENR.SPIDE[3:0] bits is 1000b.

37.4.2 Notes on Starting Transfer from the SPBSSL Signal Retained State in SPI Operating Mode

Be sure to set the SPIWE bit in the SMCR register to 1 when the transfer of a command, optional command, address, or option data is started while the SPBSSL signal is active in SPI operating mode.

37.4.3 Note on Initialization

When using this module, do not set both SPBR[7:0] = 00h and BRDV[1:0] = 00b in the bit rate setting register (SPBCR).

38. CRC Operation Units (CRC)

Cyclic redundancy check (CRC) operation units generate CRC codes.

38.1 Overview

Table 38.1 describes the CRC operation unit specifications. Figure 38.1 shows a block diagram of a CRC operation unit.

Table 38.1 CRC Operation Unit (CRC) Specifications

Item	Specifications
Data subject to CRC operation	A CRC code can be generated for any data that is 8, 16, or 32 bits long.
CRC generation polynomial expression	One of the following polynomials can be selected: • 32-bit Ethernet CRC (32-Ethernet) $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ • 16-bit CCITT CRC (16-CCITT) $X^{16} + X^{12} + X^5 + 1$ • 8-bit SAE J1850 CRC (8-SAE J1850) $X^8 + X^4 + X^3 + X^2 + 1$ • 8-bit 0x2F CRC (8-0x2F) $X^8 + X^5 + X^3 + X^2 + X + 1$
Low-power consumption function	Module-stop state can be set.

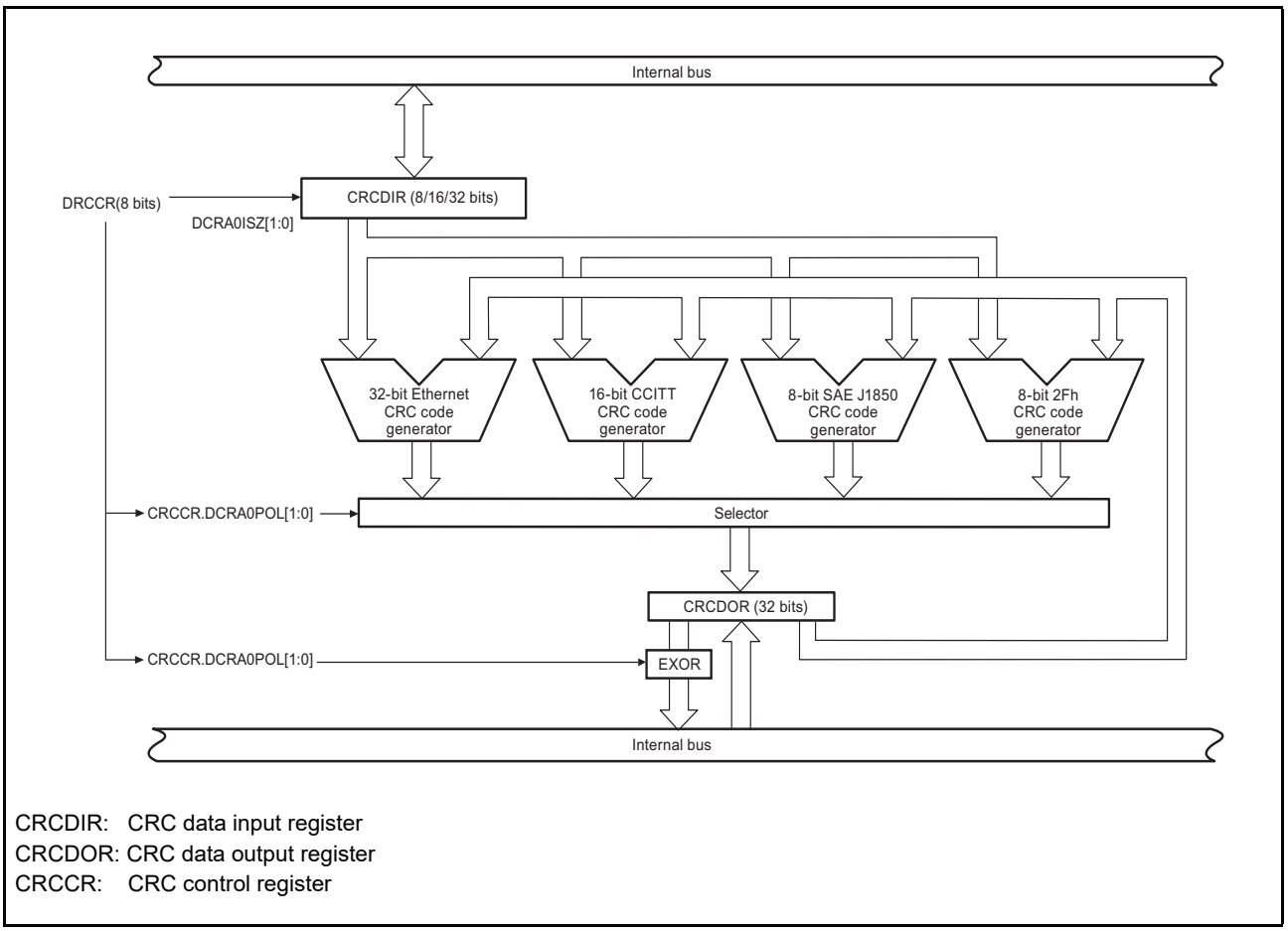


Figure 38.1 Block Diagram of a CRC Operation Unit (CRC)

38.2 Register Descriptions

38.2.1 CRC Data Input Register (CRCDIR)

The CRCDIR register stores the input data for CRC calculation. CRC calculation starts when data is written to this register.

The valid bit width used for CRC calculation must be set for CRCCR.DCRA0ISZ[1:0]. Before the first data is written to this register, the CRCDOR register must be initialized by writing the initial starting value. For details on initialization, see section 38.3.1, Initializing the CRC Data Output Register (CRCDOR).

Address(es): A007 C000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRCDIR[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CRCDIR[31:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRCDIR[31:0]	Input Data for CRC Calculation	The following bit widths are supported: • CRC input bit width of 32 bits: CRCDIR[31:0] • CRC input bit width of 16 bits: CRCDIR[15:0] • CRC input bit width of 8 bits: CRCDIR[7:0]	R/W

Byte order

The byte order of the CRCDIR register differs depending on the selected CRC generation method.

- If the 32-Ethernet CRC polynomial expression is used to generate a code (CRCCR.DCRA0POL[1:0] = 00b), the LSB-first order is used (LSB: least significant byte). For example, if the CRC input bit width is 8 bits (DCRA0ISZ[1:0] = 10b), the bits 7 to 0 of the CRCDIR register are the LSB.
- If the 16-CCITT CRC polynomial expression is used to generate a code (CRCCR.DCRA0POL[1:0] = 01b), the MSB-first order is used (MSB: most significant byte). For example, if the CRC input bit width is 8 bits (DCRA0ISZ[1:0] = 10b), the bits 7 to 0 of the CRCDIR register are the MSB.
- If the 8-SAE J1850 CRC polynomial expression is used to generate a code (CRCCR.DCRA0POL[1:0] = 10b), the MSB-first order is used (MSB: most significant byte). For example, if the CRC input bit width is 8 bits (DCRA0ISZ[1:0] = 10b), the bits 7 to 0 of the CRCDIR register are the MSB.
- If the 8-0x2F CRC polynomial expression is used to generate a code (CRCCR.DCRA0POL[1:0] = 11b), the MSB-first order is used (MSB: most significant byte). For example, if the CRC input bit width is 8 bits (DCRA0ISZ[1:0] = 10b), the bits 7 to 0 of the CRCDIR register are the MSB.

38.2.2 CRC Data Output Register (CRCDOR)

The CRCDOR register stores the CRC code calculated based on the selected CRC generation polynomial expression.

Address(es): A007 C004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CRCDOR[31:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CRCDOR[31:0]															
Value after reset: *1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note 1. After a reset, 32-bit Ethernet CRC is selected as the CRC generation polynomial expression. Therefore, when the bits are read, 0000 0000h is obtained as the result of EXOR operation.

Bit	Symbol	Bit Name	Description	R/W
b31 to b0	CRCDOR[31:0]	Resulting CRC Code	• 32-Ethernet: CRCDOR[31:0] • 16-CCITT: CRCDOR[15:0] (Bits 31 to 16 are undefined.) • 8-SAE J1850/8-0x2F: CRCDOR[7:0] (Bits 31 to 8 are undefined.) The value read from this register is the result of EXOR operation with the following value: • 32-Ethernet: FFFF FFFFh • 16-CCITT: 0000h • 8-SAE J1850/8-0x2F: FFh	R/W

Note: This register must be initialized (by setting the initial starting value) before the first data for CRC calculation is written to the CRCDIR register. For details on initialization, see section 38.3.1, Initializing the CRC Data Output Register (CRCDOR).

CRCDOR[31:0] Bits

The CRC code calculated based on the CRC generation polynomial expression selected by CRCCR.DCRA0POL[1:0] is stored.

Resulting CRC code:

- If 32-Ethernet is used, the resulting CRC code is returned to CRCDOR[31:0].
- If 16-CCITT is used, the resulting CRC code is returned to CRCDOR[15:0].
  The settings of bits 31 to 16 are undefined.
- If 8-SAE J1850/8-0x2F is used, the resulting CRC code is returned to CRCDOR[7:0].
  The settings of bits 31 to 8 are undefined.

The value read from the bits is the result of EXOR operation with the following EXOR value:

EXOR value:

- 32-Ethernet: FFFF FFFFh
- 16-CCITT: 0000h
- 8-SAE J1850/8-0x2F: FFh

After a reset, 32-bit Ethernet is selected as the CRC generation polynomial expression. Therefore, when the bits are read, 0000 0000h is obtained as the result of EXOR operation of FFFF FFFFh (initial value stored in the bits) and FFFF FFFFh (EXOR value).

Example:

Assume that the value of the CRCDOR[31:0] bits is 5555 5555h as the CRC code produced by the 32-bit Ethernet CRC algorithm. In this case, when these bits are read, AAAA AAAAh is obtained as the result of EXOR operation with the EXOR value for this algorithm, i.e. FFFF FFFFh.

38.2.3 CRC Control Register (CRCCR)

The CRCCR register controls the CRC generation polynomial expression and the CRC input bit width.

Address(es): A007 C020h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DCRA0ISZ[1:0]		—	—	DCRA0POL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DCRA0POL [1:0]	CRC Generation Mode Specification	Specify the mode in which to generate a CRC code. b1 b0 0 0: 32-Ethernet ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 0 1: 16-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0: 8-SAE J1850 ($X^8 + X^4 + X^3 + X^2 + 1$) 1 1: 8-0x2F ($X^8 + X^5 + X^3 + X^2 + X + 1$)	R/W
b3, b2	—	Reserved	These bits are read as 0.	R
b5, b4	DCRA0ISZ [1:0]	CRC Input Bit Width Specification	Specify the CRC input bit width. b1 b0 0 0: 32 bits (CRCDIR[31:0]) 0 1: 16 bits (CRCDIR[15:0]) 1 0: 8 bits (CRCDIR[7:0]) 1 1: Setting prohibited	R/W
b7, b6	—	Reserved	These bits are read as 0.	R

Note 1. If the CRC generation mode (CRCCR.DCRA0POL) is changed or the CRC input bit width (CRCCR.DCRA0ISZ) is changed, the CRCDOR register must be initialized (by setting the initial starting value). For details, see section 38.3.1, Initializing the CRC Data Output Register (CRCDOR).

Note 2. The CRC input bit width (CRCCR.DCRA0ISZ[1:0]) must be set according to the block unit of data for CRC calculation. The CRC input bit width must not be changed during CRC calculation. The CRC input bit width can be changed after the final CRC calculation result is read from the CRCDOR register. In this case, before the next data for CRC calculation is written to the CRCDIR register, the CRCDOR register must be initialized (by setting the initial starting value).

38.3 Operation

The CRC operation unit calculates and generates the CRC code for a block of a specific length. Data for which the CRC is to be calculated can be set in the CRC data input register (CRCDIR) in 8-, 16-, or 32- bit units. When data are written to the CRC data input register (CRCDIR), CRC calculation based on the selected CRC generation polynomial expression starts. Before writing the first value to the CRC data input register (CRCDIR), the CRCDOR register must be initialized by setting it to its initial value.
The following shows an overview of using the CRC operation unit.

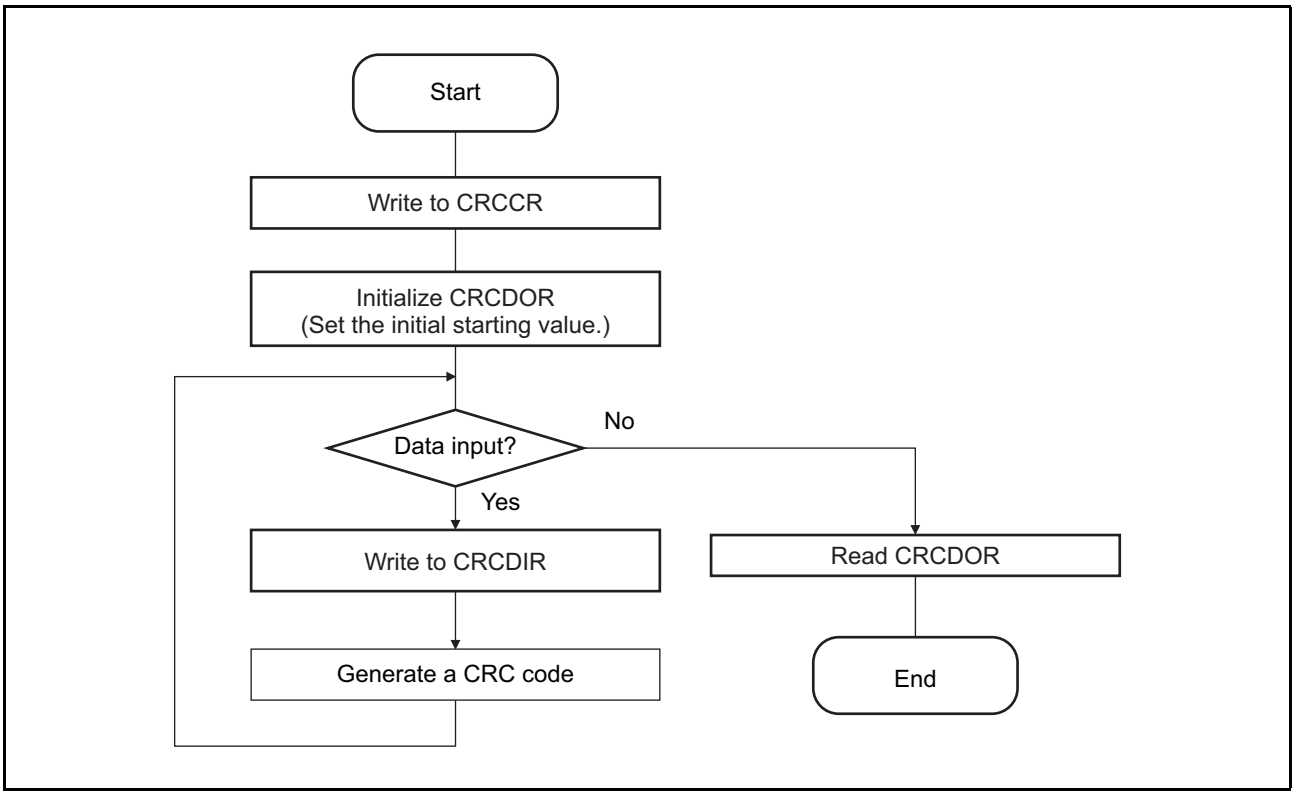


Figure 38.2 Use of the CRC Operation Unit

Note: If the CRC generation polynomial expression is changed by changing the value of CRCCR.DCRA0POL[1:0], the CRC data output register (CRCDOR) must be re-initialized (by setting the initial starting value).

38.3.1 Initializing the CRC Data Output Register (CRCDOR)

Before the first data is written to the CRC data input register (CRCDIR), the CRC data output register (CRCDOR) must be initialized by setting the initial starting value. Table 38.2 lists the initial starting value for each CRC generation polynomial expression.

Table 38.2 also shows the value obtained from the CRCDOR register after the initial starting value is set, as well as the EXOR value used for EXOR operation during a read. For details on the value obtained from the CRCDOR register, see section 38.2.2, CRC Data Output Register (CRCDOR).

Table 38.2 Initial Starting Value for Each CRC Generation Polynomial Expression

CRC Generation Polynomial Expression	Initial Starting Value	EXOR Value	Value Obtained from CRCDOR after the Initial Starting Value Is Set
32-Ethernet (DCRA0POL[1:0] = 00b)	FFFF FFFFh	FFFF FFFFh	0000 0000h
16-CCITT (DCRA0POL[1:0] = 01b)	0000 FFFFh	0000 0000h	0000 FFFFh
8-SAE J1850 (DCRA0POL[1:0] = 10b)	0000 00FFh	0000 00FFh	0000 0000h
8-0x2F (DCRA0POL[1:0] = 11b)	0000 00FFh	0000 00FFh	0000 0000h

39. Serial Sound Interface (SSI)

This LSI integrates one channel of the serial sound interface (SSI) compliant to the I^{2}S bus standard. The SSI supports I^{2}S bus compatibility and MSB-first and left-aligned/right-aligned formats, so it can be used to send or receive audio data with various devices.

39.1 Overview

Table 39.1 SSI Specifications

Item	Specifications
Number of channels	One channel
Operating mode	Non-compressed mode
Transfer formats	• I^{2}S format supported • MSB-first supported Left-aligned/right-aligned formats selectable
Function	• Serves as both a transmitter and a receiver Supports full-duplex communications. • Capable of various audio formats • SSISCK (serial bit clock) can be selected from among 16, 32, 48, and 64 fs (fs: Sampling rate) • Master clock is input from the external clock for SSI (AUDIO_CLK) (Max. 50 MHz) • Includes 8-stage FIFO buffers in transmitter and receiver • Capable of selecting whether to stop word select (SSIWS) or not when data transfer is stopped
Interrupt sources	Three sources • Communication error Transmit underflow, transmit overflow, receive underflow, receive overflow, and idle • Receive data full • Transmit data empty
Low-power consumption function	Module stop state can be set.

Figure 39.1 shows a block diagram of SSI.

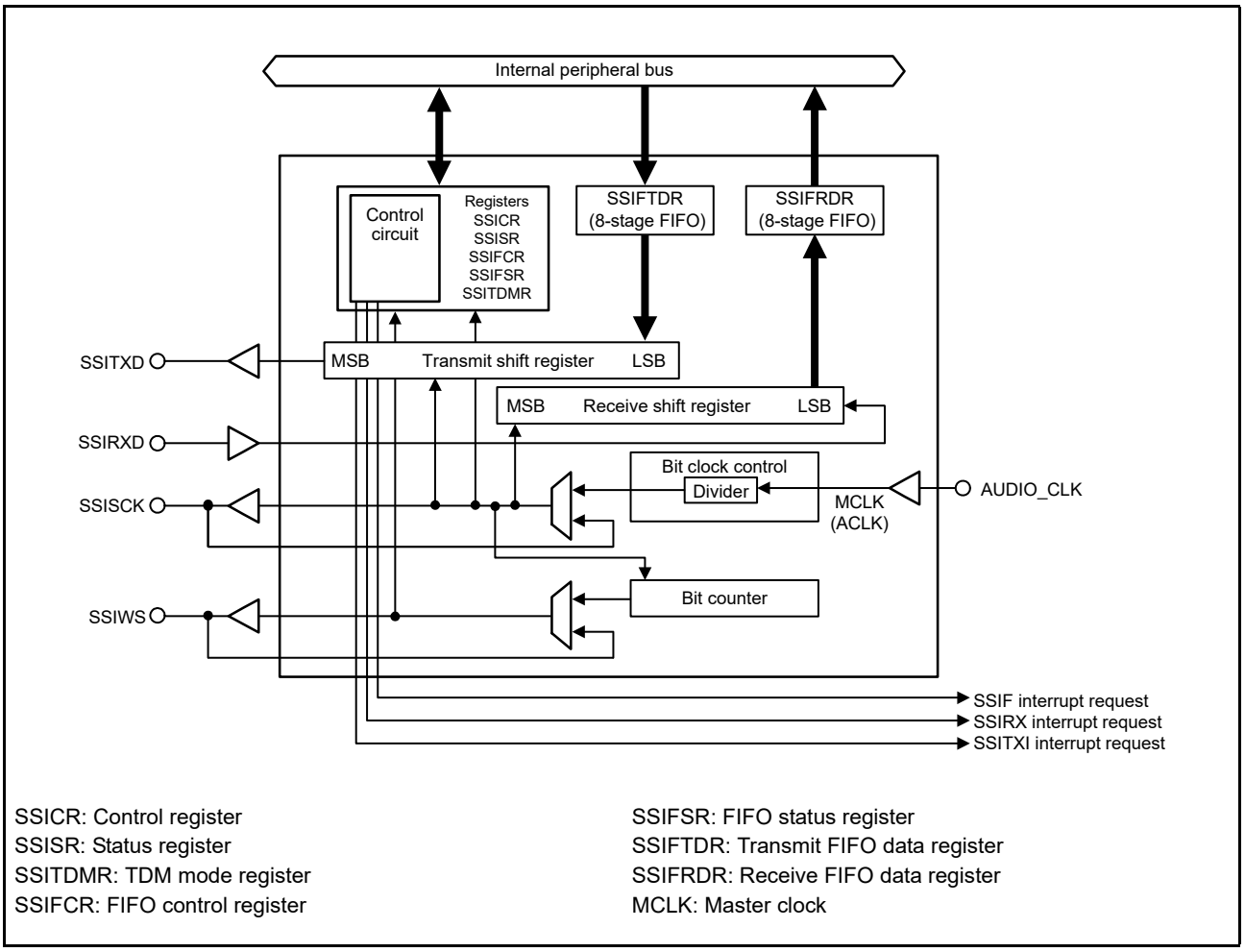


Figure 39.1 Block Diagram of SSI

Table 39.2 lists the I/O pins of the SSI.

Table 39.2 SSI I/O Pins

Pin Name	I/O	Description
SSISCK	I/O	Serial bit clock pin
SSIWS	I/O	Word selection pin
SSITXD	Output	Serial data output pin
SSIRXD	Input	Serial data input pin
AUDIO_CLK	Input	Master clock for audio pin (input master clock)

39.2 Register Description

39.2.1 Control Register (SSICR)

The SSICR register controls the operating mode, polarity setting, and various interrupts.

Address(es): A008 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	CHNL[1:0]		DWL[2:0]			SWL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKD	SWSD	SCKP	SWSP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	REN	Receive Enable	0: Disables receive operation. 1: Enables receive operation.	R/W
b1	TEN	Transmit Enable	0: Disables transmit operation. 1: Enables transmit operation.	R/W
b2	—	Reserved	This bit is read as undefined. The write value should be 0.	R/W
b3	MUEN	Mute Enable*1	0: Not muted. 1: Muted.	R/W
b7 to b4	CKDV[3:0]	Serial Bit Clock Frequency Setting*3	b7 b4 0 0 0 0: MCLK 0 0 0 1: MCLK/2 0 0 1 0: MCLK/4 0 0 1 1: MCLK/8 0 1 0 0: MCLK/16 0 1 0 1: MCLK/32 0 1 1 0: MCLK/64 0 1 1 1: MCLK/128 1 0 0 0: MCLK/6 1 0 0 1: MCLK/12 1 0 1 0: MCLK/24 1 0 1 1: MCLK/48 1 1 0 0: MCLK/96 Settings other than above are prohibited.	R/W
b8	DEL	Serial Data Delay*3	0: I2S format compatibility One clock cycle delay between SSIWS and SSITXD/SSIRXD 1: MSB-first left-aligned/right-aligned format compatibility No delay between SSIWS and SSITXD/SSIRXD	R/W
b9	PDTA	Parallel Data Allocation*3	When data word length is 8 or 16 bits: 0: The lower bits of parallel data (SSIFTDR, SSIFRDR) are transferred prior to the upper bits. 1: The upper bits of parallel data (SSIFTDR, SSIFRDR) are transferred prior to the lower bits. When data word length is 18, 20, 22, or 24 bits: 0: Parallel data (SSIFTDR, SSIFRDR) is left-aligned. 1: Parallel data (SSIFTDR, SSIFRDR) is right-aligned.	R/W
b10	SDTA	Serial Data Alignment*3	0: Transmitting and receiving in the order of serial data and padding bits 1: Transmitting and receiving in the order of padding bits and serial data	R/W
b11	SPDP	Serial Padding Polarity*3	0: Padding data is 0. 1: Padding data is 1.	R/W

Bit	Symbol	Bit Name	Description	R/W
b12	SWSP	Word Select Polarity	0: SSIWS is low for 1st system word, high for 2nd system word. 1: SSIWS is high for 1st system word, low for 2nd system word.	R/W
b13	SCKP	Serial Bit Clock Polarity*3	0: SSIWS and SSITXD/SSIRXD change at the SSISCK falling edge (sampled at the SCK rising edge). 1: SSIWS and SSITXD/SSIRXD change at the SSISCK rising edge (sampled at the SCK falling edge).	R/W
b14	SWSD	Word Select Direction*2, *3	0: SSIWS pin is input (slave mode). 1: SSIWS pin is output (master mode).	R/W
b15	SCKD	Serial Bit Clock Direction*2, *3	0: SSISCK pin is input (slave mode). 1: SSISCK pin is output (master mode).	R/W
b18 to b16	SWL[2:0]	System Word Length*3	Set the system word length to the bit clock frequency/2 fs. b18 b16 0 0 0: 8 bits (serial bit clock frequency = 16 fs) 0 0 1: 16 bits (serial bit clock frequency = 32 fs) 0 1 0: 24 bits (serial bit clock frequency = 48 fs) 0 1 1: 32 bits (serial bit clock frequency = 64 fs) Settings other than above are prohibited.	R/W
b21 to b19	DWL[2:0]	Data Word Length*3	b21 b19 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 18 bits 0 1 1: 20 bits 1 0 0: 22 bits 1 0 1: 24 bits Settings other than above are prohibited.	R/W
b23, b22	CHNL[1:0]	Channels*3	b23 b22 0 0: One channel Settings other than above are prohibited.	R/W
b24	—	Reserved	This bit is read as undefined. The write value should be 0.	R/W
b25	IIEN	Idle Interrupt Enable	0: Disables an idle interrupt. 1: Enables an idle interrupt.	R/W
b26	ROIEN	Receive FIFO Overflow Interrupt Enable	0: Disables a receive FIFO overflow interrupt. 1: Enables a receive FIFO overflow interrupt.	R/W
b27	RUIEN	Receive FIFO Underflow Interrupt Enable	0: Disables a receive FIFO underflow interrupt. 1: Enables a receive FIFO underflow interrupt.	R/W
b28	TOIEN	Transmit FIFO Overflow Interrupt Enable	0: Disables a transmit FIFO overflow interrupt. 1: Enables a transmit FIFO overflow interrupt.	R/W
b29	TUIEN	Transmit FIFO Underflow Interrupt Enable	0: Disables a transmit FIFO underflow interrupt. 1: Enables a transmit FIFO underflow interrupt.	R/W
b30	CKS	Audio Clock Select*3	0: AUDIO_CLK input 1: Setting prohibited	R/W
b31	—	Reserved	This bit is read as undefined. The write value should be 0.	R/W

	SCKP bit = 0	SCKP bit = 1
SSITXD/SSIRXD input sampling timing for reception	SSISCK rising edge	SSISCK falling edge
SSITXD/SSIRXD output changing timing for transmission	SSISCK falling edge	SSISCK rising edge
SSIWS input sampling timing in slave mode (SWSD bit = 0)	SSISCK rising edge	SSISCK falling edge
SSIWS output changing timing in master mode (SWSD bit = 1)	SSISCK falling edge	SSISCK rising edge

Note 1. While this module is muted, 0 is transmitted regardless of the value of serial data, but data transfer is not stopped. Since the number of data in the transmit FIFO decreases, write dummy data to the SSIFTDR register to prevent the generation of a transmit underflow. When the MUEN bit is set to 1, the SSITXD pin is immediately set to 0 without synchronizing SSIWS.
Note 2. Set the SCKD and SWSD bits to the same value. Other settings are prohibited.
Note 3. Rewriting is allowed only in the idle state.

REN Bit (Receive Enable)

This bit enables or disables receive operation. Setting this bit to 1 starts receive operation.

TEN Bit (Transmit Enable)

This bit enables or disables transmit operation. Setting this bit to 1 starts transmit operation.
SSITXD of SSI is set as output while the I/O port function is selected, regardless of the TEN bit setting.

Table 39.3 SSITXD and SSIRXD Pin States

	Register Settings		SSI	
MPC setting	TEN	REN	SSITXD	SSIRXD
SSI selected	0	0	Output	Input
	0	1	Output	Input
	1	0	Output	Input
	1	1	Output	Input
SSI deselected	x	x	I/O port	I/O port

x: Don't care
I/O port: Depends on the settings of the I/O port and multi-function pin controller.

CKDV[3:0] Bits (Serial Bit Clock Frequency Setting)

These bits are used to select a division ratio of the master clock to set the serial bit clock frequency in the master mode. Since the input clock from the SSISCK pin is used in slave mode, the setting of these bits is ignored. The serial bit clock is used as the operating clock of the shift register.

Calculation Example:
When fs (sampling rate) = the SSIWS frequency = 96 kHz and the system word length = 32 bits
The bit clock frequency = 96 kHz × 32 bits × 2 = 6.144 MHz is necessary, so set CKDV[3:0] = 0001b when MCLK = 12.288 MHz.

PDTA Bit (Parallel Data Allocation)

The setting of this bit specifies the allocation of data to be stored in the SSIFRDR register in reception mode and the SSIFTDR register in transmission mode.

During receive operation, the SSI stores the data received from the serial audio bus in SSIFRDR according to the PDTA bit setting.

During transmit operation, the SSI stores the data stored in SSIFTDR in the transmit shift register, and transmits the data to the audio serial bus according to the PDTA bit setting.

When PDTA = 0

DWL[2:0] Bits	SSIFTDR/SSIFRDR[31:0] Registers
000b	31 24 23 16 15 8 7 0 4th word | 3rd word | 2nd word | 1st word
001b	31 16 15 0 2nd word | 1st word
010b	31 14 13 0 Valid | Invalid
011b	31 12 11 0 Valid | Invalid
100b	31 10 9 0 Valid | Invalid
101b	31 8 7 0 Valid | Invalid

When PDTA = 1

DWL[2:0] Bits	SSIFTDR/SSIFRDR[31:0] Registers
000b	31 24 23 16 15 8 7 0 1st word | 2nd word | 3rd word | 4th word
001b	31 16 15 0 1st word | 2nd word
010b	31 18 17 0 Invalid | Valid
011b	31 20 19 0 Invalid | Valid
100b	31 22 21 0 Invalid | Valid
101b	31 24 23 0 Invalid | Valid

CHNL[1:0] Bits (Channels)

These bits select the number of channels in the system word. Set these bits to 00b.

39.2.2 Status Register (SSISR)

The SSISR register indicates the operating status of SSI.

Address(es): A008 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	0	0	0	0	1	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	TSWNO	—	—	RSWNO	IDST
Value after reset:	x	x	x	x	x	x	x	x	x	0	0	1	0	0	1	1

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	IDST	Idle Status Flag	0: SSI communication is in progress. 1: SSI communication is idle.	R
b1	RSWNO	Receive System Word Number	Receive word number	R
b3, b2	—	Reserved	These bits are read as 00b.	R
b4	TSWNO	Transmit System Word Number	Transmit word number	R
b6, b5	—	Reserved	These bits are read as 00b.	R
b24 to b7	—	Reserved	These bits are read as undefined.	R
b25	IIRQ	Idle Interrupt Status Flag	0: Not in idle state 1: In idle state	R
b26	ROIRQ	Receive Overflow Interrupt Status Flag	0: No receive overflow has occurred. 1: A receive overflow has occurred.	R/(W) *1
b27	RUIRQ	Receive Underflow Interrupt Status Flag	0: No receive underflow has occurred. 1: A receive underflow has occurred.	R/(W) *1
b28	TOIRQ	Transmit Overflow Interrupt Status Flag	0: No transmit overflow has occurred. 1: A transmit overflow has occurred.	R/(W) *1
b29	TUIRQ	Transmit Underflow Interrupt Status Flag	0: No transmit underflow has occurred. 1: A transmit underflow has occurred.	R/(W) *1
b31, b30	—	Reserved	These bits are read as undefined.	R

Note 1. This bit can be set to 0 by writing 0 after reading it as 1.

IDST Flag (Idle Status Flag)

This status flag indicates that the SSI is in idle state where communication is stopped.

This flag is set to 0 when communication starts after the SSICR.TEN bit or SSICR.REN bit is set to 1. Also, this flag is set to 1 if both the SSICR.TEN and SSICR.REN bits are set to 0 and system word communication is completed.

If the external device stops inputting the serial bit clock before communication is completed, this flag is not set to 1.

RSWNO Bit (Receive System Word Number)

The initial value of this bit is 1, and its value is inverted when the data is transferred from the receive shift register to the SSIFRDR register.

This bit is initialized to 1 when the REN bit value is changed from 0 to 1.

When the data word length specified by the SSICR.DWL[2:0] bits is 18 bits or more, this bit indicates which system word the data in the SSIFRDR register represents.

TSWNO Bit (Transmit System Word Number)

This status bit indicates the current word number.
The initial value of this is 1, and its value is inverted when the data is transferred from the SSIFTDR register to the transmit shift register.
This bit is initialized to 1 when the TEN bit value is changed from 0 to 1.
When the data word length specified by the SSICR.DWL[2:0] bits is 18 bits or more, this bit indicates the system word that is in the data transferred from the SSIFTDR register to the transmit shift register.

IIRQ Flag (Idle Interrupt Status Flag)

This status flag indicates whether this module is in idle state.
This flag is set regardless of the value of the SSICR.IIEN bit to allow polling.
The interrupt can be masked by setting the SSICR.IIEN bit to 0, but cannot be cleared by writing to this flag.
If IIRQ flag = 1 and SSICR.IIEN bit = 1, an interrupt occurs.

ROIRQ Flag (Receive Overflow Interrupt Status Flag)

This status flag indicates that receive data was supplied at a higher rate than was required. If a receive overflow occurs, stop reception and start from the beginning of the flowchart again.
This flag is set to 1 regardless of the setting of the SSICR.ROIEN bit. This flag can be set to 0 by writing 0 after reading it as 1.
If ROIRQ flag = 1 and SSICR.ROIEN bit = 1, an interrupt occurs.
The ROIRQ flag being 1 indicates that the data has been transferred from the receive shift register to the SSIFRDR register before the previous unread data is read out while the receive FIFO is full (SSIFSR.RDC[3:0] flag = 8h). This may lead to the loss of data.

Note: When an overflow occurs, the current data in the data buffer of this module is overwritten by the next incoming data from the SSI interface.

RUIRQ Flag (Receive Underflow Interrupt Status Flag)

This status flag indicates that receive data was supplied at a lower rate than was required. If a receive underflow occurs, stop reception and start the flowchart again from the beginning.
This flag is set to 1 regardless of the setting of the SSICR.RUIEN bit. This flag can be set to 0 by writing 0 after reading it as 1.
If RUIRQ flag = 1 and SSICR.RUIEN bit = 1, an interrupt occurs.
If RUIRQ flag = 1, the SSIFRDR register was read while the receive FIFO is empty (SSIFSR.RDC[3:0] flags = 0h). This may cause invalid receive data to be stored.

TOIRQ Flag (Transmit Overflow Interrupt Status Flag)

This status flag indicates that transmit data was supplied at a higher rate than was required. If a transmit overflow occurs, stop transmission and start from the beginning of the flowchart again.
This flag is set to 1 regardless of the setting of the SSICR.TOIEN bit. This flag can be set to 0 by writing 0 after reading it as 1.
If TOIRQ flag = 1 and SSICR.TOIEN bit = 1, an interrupt occurs.
If TOIRQ flag = 1, the SSIFTDR register had data written to it while the transmit FIFO is full (SSIFSR.TDC[3:0] flags = 8h). This may lead to the loss of data.

TUIRQ Flag (Transmit Underflow Interrupt Status Flag)

This status flag indicates that transmit data was supplied at a lower rate than was required. If a transmit underflow occurs, stop transmission and start from the beginning of the flowchart again.

This flag is set to 1 regardless of the setting of the SSICR.TUIEN bit. This flag can be set to 0 by writing 0 after reading it as 1.

If TUIRQ flag = 1 and SSICR.TUIEN bit = 1, an interrupt occurs.

If TUIRQ flag = 1, the SSIFTDR register did not have data written to it before it was required for transmission. This may lead to the same data being transmitted once more.

Note: When a transmit underflow occurs, the last data input to SSIFTDR is transmitted until this module is in the idle state after transmission is stopped.

39.2.3 FIFO Control Register (SSIFCR)

The SSIFCR register controls settings of the transmit FIFO register and the receive FIFO register.

Address(es): A008 1010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TTRG[1:0]		RTRG[1:0]		TIE	RIE	TFRST	RFRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RFRST	Receive FIFO Data Register Reset*4	0: Clears the receive FIFO data reset. 1: Initiates the receive FIFO data reset.	R/W
b1	TFRST	Transmit FIFO Data Register Reset	0: Clears the transmit FIFO data reset. 1: Initiates the transmit FIFO data reset.	R/W
b2	RIE	Receive FIFO Data Full Interrupt Enable	0: Receive FIFO data full interrupt (RXI) request is disabled. 1: Receive FIFO data full interrupt (RXI) request is enabled.*1	R/W
b3	TIE	Transmit FIFO Data Empty Interrupt Enable	0: Transmit FIFO data empty interrupt (TXI) request is disabled. 1: Transmit FIFO data empty interrupt (TXI) request is enabled.*2	R/W
b5, b4	RTRG[1:0]	Receive FIFO Threshold Setting Trigger*4	b5 b4 0 0: 1 0 1: 2 1 0: 4 1 1: 6	R/W
b7, b6	TTRG[1:0]	Transmit FIFO Threshold Setting Trigger*4	b7 b6 0 0: 7 (1)*3 0 1: 6 (2)*3 1 0: 4 (4)*3 1 1: 2 (6)*3	R/W
b30 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	AUCKE	Master Clock Enable*4	0: The master clock is disabled. 1: The master clock is enabled.	R/W

Note 1. The RXI request can be cleared by setting the SSIFSR.RDF flag to 0 (see the description of the SSIFSR.RDF flag for details) or RIE bit to 0.
Note 2. The TXI request can be cleared by setting the SSIFSR.TDE flag to 0 (see the description of the SSIFSR.TDE flag for details) or TIE bit to 0.
Note 3. The values in parenthesis are the number of empty stages in SSIFTDR at which the SSIFSR.TDE flag is set.
Note 4. Rewriting is allowed only in the idle state.

The SSIFCR register resets the number of the data bytes stored in the SSIFTDR and SSIFRDR registers, and specifies transmit FIFO and receive FIFO threshold values.

RFRST Bit (Receive FIFO Data Register Reset)

This bit invalidates the data in the SSIFRDR register to reset the FIFO to an empty state.

TFRST Bit (Transmit FIFO Data Register Reset)

This bit invalidates the data in the SSIFTDR register to reset the FIFO to an empty state.

RIE Bit (Receive FIFO Data Full Interrupt Enable)

This bit enables or disables generation of receive FIFO data full interrupt (RXI) requests when the SSIFSR.RDF flag is set to 1 during reception.

TIE Bit (Transmit FIFO Data Empty Interrupt Enable)

This bit enables or disables generation of transmit FIFO data empty interrupt (TXI) requests when the SSIFSR.TDE flag is set to 1 during transmit operation.

RTRG[1:0] Bits (Receive FIFO Threshold Setting Trigger)

These bits specify the receive FIFO threshold value. When the number of received data bytes stored in the SSIFRDR register (receive FIFO) has become equal to or greater than the value specified by the RTRG[1:0] bits, the SSIFSR.RDF flag is set to 1 and reading the received data is requested. If the SSIFCR.RIE bit is 1 at this time, a receive FIFO data full interrupt (RXI) request is generated.

TTRG[1:0] Bits (Transmit FIFO Threshold Setting Trigger)

These bits specify the transmit FIFO threshold value. When the number of transmit data bytes stored in the SSIFTDR register (transmit FIFO) has become equal to or less than the value specified by the TTRG[1:0], the SSIFSR.TDE flag is set to 1 and writing the transmit data is requested. If the SSIFCR.TIE bit is 1 at this time, a transmit FIFO data empty interrupt (TXI) request is generated.

39.2.4 FIFO Status Register (SSIFSR)

The SSIFSR register indicates the operating status of the SSIFTDR register and the SSIFRDR register.

Address(es): A008 1014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	TDC[3:0]				—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	RDC[3:0]				—	—	—	—	—	—	—	RDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	RDF	Receive Data Full Flag	0: Number of received data bytes in the SSIFRDR register is less than the set receive trigger number. 1: Number of received data bytes in the SSIFRDR register is equal to or greater than the set receive trigger number.	R/(W) *1
b7 to b1	—	Reserved	These bits are read as 0.	R
b11 to b8	RDC[3:0]	Receive Data Indicate Flag	Indicate the number of data units stored in the SSIFRDR register.	R
b15 to b12	—	Reserved	These bits are read as 0.	R
b16	TDE	Transmit Data Empty Flag	0: Number of data bytes for transmission in the SSIFTDR register is greater than the set transmit trigger number. 1: Number of data bytes for transmission in the SSIFTDR register is equal to or less than the set transmit trigger number.*2	R/(W) *1
b23 to b17	—	Reserved	These bits are read as 0.	R
b27 to b24	TDC[3:0]	Transmit Data Indicate Flag	Indicate the number of data units stored in the SSIFTDR register.	R
b31 to b28	—	Reserved	These bits are read as 0.	R

Note 1. This bit can be set to 0 by writing 0 after reading it as 1.
Note 2. Since the SSIFTDR register is an 8-stage FIFO register, the amount of data that can be written to it while TDE flag = 1 is “8 - transmit trigger number to be specified” bytes at maximum. Writing more data will be ignored. The number of data bytes in the SSIFTDR register is indicated in the TDC[3:0] flags.

RDF Flag (Receive Data Full Flag)

This flag indicates that, when the received data is transferred to the SSIFRDR register, the number of data bytes in the SSIFRDR register has become equal to or greater than the receive FIFO threshold value, and thus reading the received data from the SSIFRDR register has been enabled.

[Setting condition]

- The number of receive data bytes that is equal to or greater than the receive FIFO threshold value is stored in the SSIFRDR register.*1

[Clearing condition]

- 0 is written to the RDF flag after the RDF flag is confirmed to be 1.

Note 1. Since the SSIFRDR register is a 32-byte FIFO register, the maximum number of data bytes that can be read from it while the RDF flag is 1 is indicated in the RDC[3:0] flags. If reading data from the SSIFRDR register is continued after all the data is read, undefined values will be read.

RDC[3:0] Flags (Receive Data Indicate Flag)

These flags indicate the number of data bytes stored in the SSIFRDR register.
RDC[3:0] flags = 0h indicates no received data. RDC[3:0] flags = 8h indicates that 32 bytes of received data is stored in the SSIFRDR register.

TDE Flag (Transmit Data Empty Flag)

This flag indicates that, when data is transferred from the SSIFTDR register to the transmit shift register, the number of data bytes in the SSIFTDR register has become less than the transmit FIFO threshold value, and thus writing transmit data to the SSIFTDR register has been enabled.
[Setting condition]

- The number of the transmit data bytes written to the SSIFTDR register is equal to or less than the transmit FIFO threshold value.*1

[Clearing condition]

- 0 is written to the TDE flag after the TDE flag is confirmed to be 1.

Note 1. Since the SSIFTDR register is a 32-bit FIFO register, the maximum number of bytes that can be written to it while the TDE flag is 1 is 8 - TDC[3:0]. If writing data to the SSIFTDR register is continued after all the data is written, writing will be invalid and an overflow occurs.

TDC[3:0] Flags (Transmit Data Indicate Flag)

These flags indicate the number of data bytes stored in the SSIFTDR register.
TDC[3:0] flags = 0h indicates no data for transmission. TDC[3:0] flags = 8h indicates that 32 bytes of data for transmission is stored in the SSIFTDR register.

39.2.5 Transmit FIFO Data Register (SSIFTDR)

The SSIFTDR register is a write-only FIFO register consisting of eight 32-bit stages for storing data to be serially transmitted.

Address(es): A008 1018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Write transmit data to the SSIFTDR register in 64-bit (two-stage FIFO) units regardless of the data word length setting. If transmit data ends on a 32-bit boundary, write 32-bit 0-data (0000 0000h) after the last transmit data is written, and stop transmission while 64-bit writing is completed. When the transmit shift register is empty, the SSI transfers the transmit data written to the SSIFTDR register to start serial transmission, which can be continued until the SSIFTDR register becomes empty.

Note that when the SSIFTDR register is full of data (32 bytes), the next data cannot be written to it. If writing is attempted, it will be ignored and an overflow occurs.

39.2.6 Receive FIFO Data Register (SSIFRDR)

The SSIFRDR register is a read-only FIFO register consisting of eight 32-bit stages for storing serially received data.

Address(es): A008 101Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Each time 4 bytes of serial data is received, the SSI stores the received serial data in the SSIFRDR register from the receive shift register according to the PDTA bit setting. Receive operation can be continued until a maximum 32 bytes of data have been stored to in the SSIFRDR register. The SSIFRDR register can be read but cannot be written to. Note that when the SSIFRDR register is read when it stores no received data, undefined values will be read and a receive underflow occurs.

After the SSIFRDR register becomes full of received data, the data received thereafter will be lost and a receive overflow occurs.

39.2.7 TDM Mode Register (SSITDMR)

The SSITDMR register is a readable/writable 32-bit register that enables or disables WS continue mode.

Address(es): A008 1020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CONT	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CONT	WS Continue Mode*1	0: Disables WS continue mode. 1: Enables WS continue mode.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit can be set only in master mode (SSICR.SCKD bit = 1 and SSICR.SWSD bit = 1).

39.3 Operation

39.3.1 Bus Format

This module can operate as a transmitter or a receiver and can be configured into many serial bus formats in either mode. The bus format can be selected from one of the six modes shown in Table 39.4.

Table 39.4 Bus Format

	TEN	REN	SCKD	SWSD	MUEN	IIEN	TOIEN	TUIEN	ROIEN	RUIEN	CONT	SWSP	DEL	PDTA	SDTA	SPDP	SCKP	SWL[2:0]	DWL[2:0]	CHNL[1:0]
Non-Compression Slave Receiver	0	1	0	0	Control Bits							Configuration Bits								
Non-Compression Slave Transmitter	1	0	0	0																
Non-Compression Slave Transceiver	1	1	0	0																
Non-Compression Master Receiver	0	1	1	1																
Non-Compression Master Transmitter	1	0	1	1																
Non-Compression Master Transceiver	1	1	1	1																

39.3.2 Non-Compressed Mode

The non-compressed mode supports all serial audio streams split into channels. It supports the I^2S compatible format as well as MSB-first and left-aligned/right-aligned.

(1) Slave Receiver

This mode allows the module to receive serial data from another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of this module, operation is not guaranteed.

(2) Slave Transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of this module, operation is not guaranteed.

(3) Slave Transceiver

This mode allows serial data transmission and reception between this module and another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of this module, operation is not guaranteed.

(4) Master Receiver

This mode allows the module to receive serial data from another device. The clock and word select signals are internally derived from the master clock. The format of these signals is defined in the configuration fields of this module. If the incoming data does not follow the configured format, operation is not guaranteed.

(5) Master Transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signals are internally derived from the master clock. The format of these signals is defined in the configuration fields of this module.

(6) Master Transceiver

This mode allows serial data transmission and reception between this module and another device. The clock and word select signals are internally derived from the master clock. The format of these signals is defined in the configuration fields of this module.

(7) Operating Setting Related to Word Length

All bits related to the SSICR register's word length are valid in non-compressed modes. There are many configurations this module supports, but some of the combinations are shown below for the I²S compatible format, MSB-first and left-aligned format, and MSB-first and right-aligned format.

- I²S Compatible Format

Figure 39.2 and Figure 39.3 show the I²S compatible format both without and with padding.
Padding occurs when the data word length is smaller than the system word length.

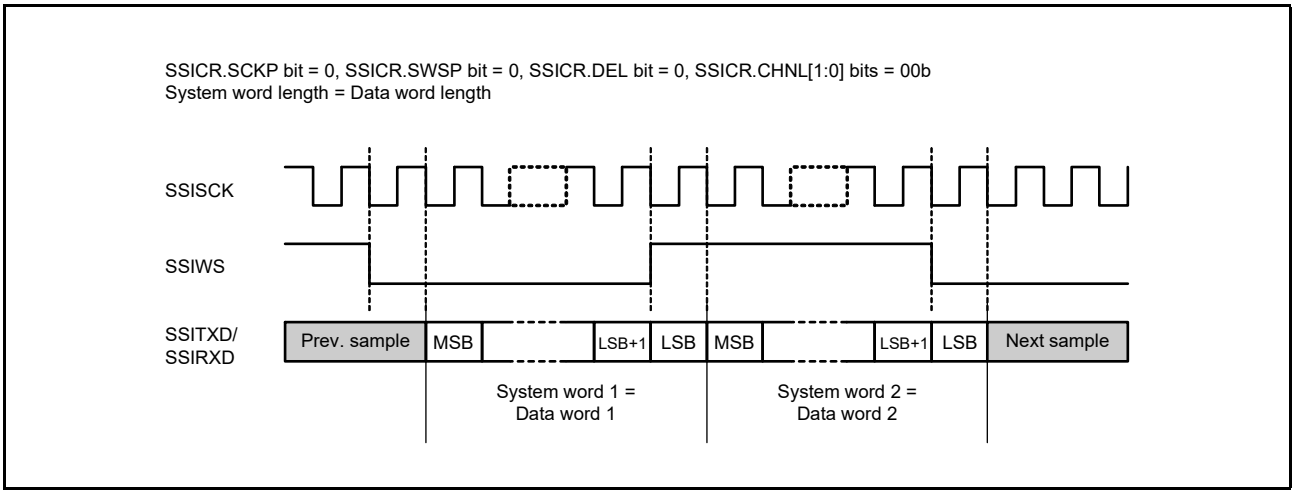


Figure 39.2 I²S Compatible Format (without Padding)

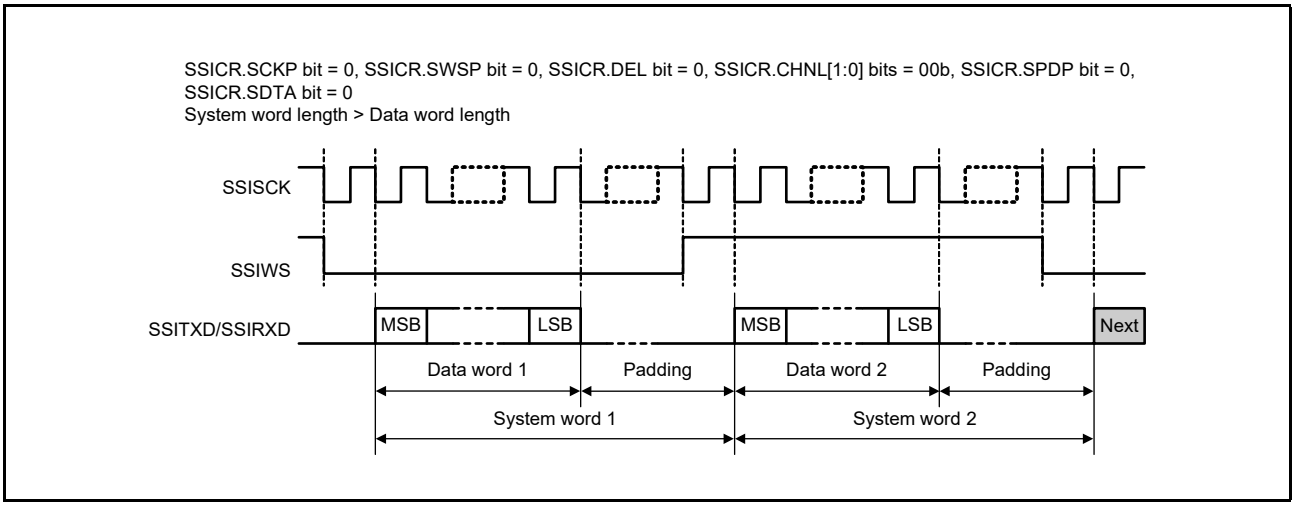


Figure 39.3 I²S Compatible Format (with Padding)

Figure 39.4 shows the MSB-first and left-aligned format and Figure 39.5 shows the MSB-first and right-aligned format.

- MSB-First and Left-Aligned Format

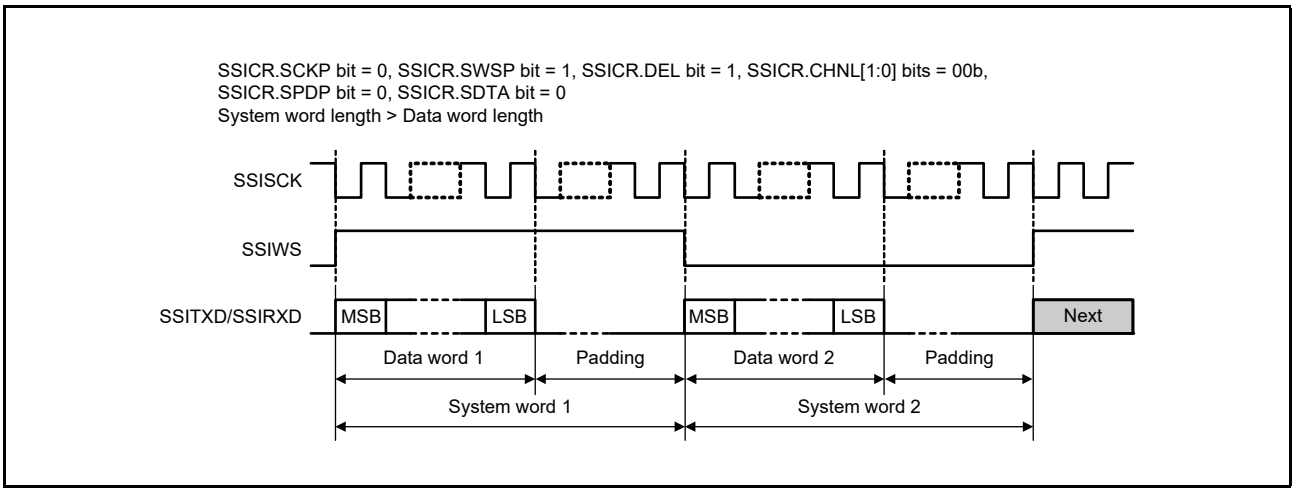


Figure 39.4 MSB-First and Left-Aligned Format (Transmitted and Received in the Order of Serial Data and Padding Bits)

- MSB-First and Right-Aligned Format

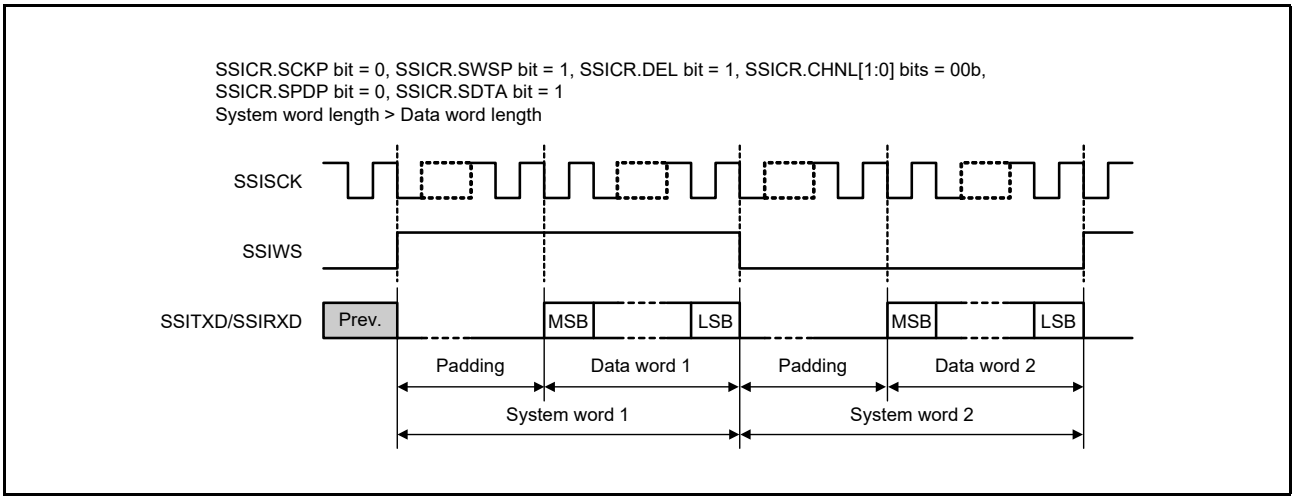


Figure 39.5 MSB-First and Right-Aligned Format (Transmitted and Received in the Order of Padding Bits and Serial Data)

Table 39.5 shows the number of padding bits for each of the valid setting.

Table 39.5 Number of Padding Bits for Each Valid Setting

Padding Bits per System Word			SSICR.DWL[2:0] Bits	000b	001b	010b	011b	100b	101b
SSICR.CHNL[1:0] Bits	Decoded Channels per System Word	SSICR.SWL[2:0] Bits	Data Word Length / System Word Length	8	16	18	20	22	24
00b	1	000b	8	0	—	—	—	—	—
		001b	16	8	0	—	—	—	—
		010b	24	16	8	6	4	2	0
		011b	32	24	16	14	12	10	8

(8) Operating Setting Format Configuration Bit

Several more configuration bits in non-compressed mode are shown below. These bits are not mutually exclusive, but some combinations may not be useful for any other device.

These configuration bits are described below with reference to the basic sample format in Figure 39.6.
In Figure 39.6 to Figure 39.14, a system word length of 6 bits and a data word length of 4 bits are used for simplification of these figures.

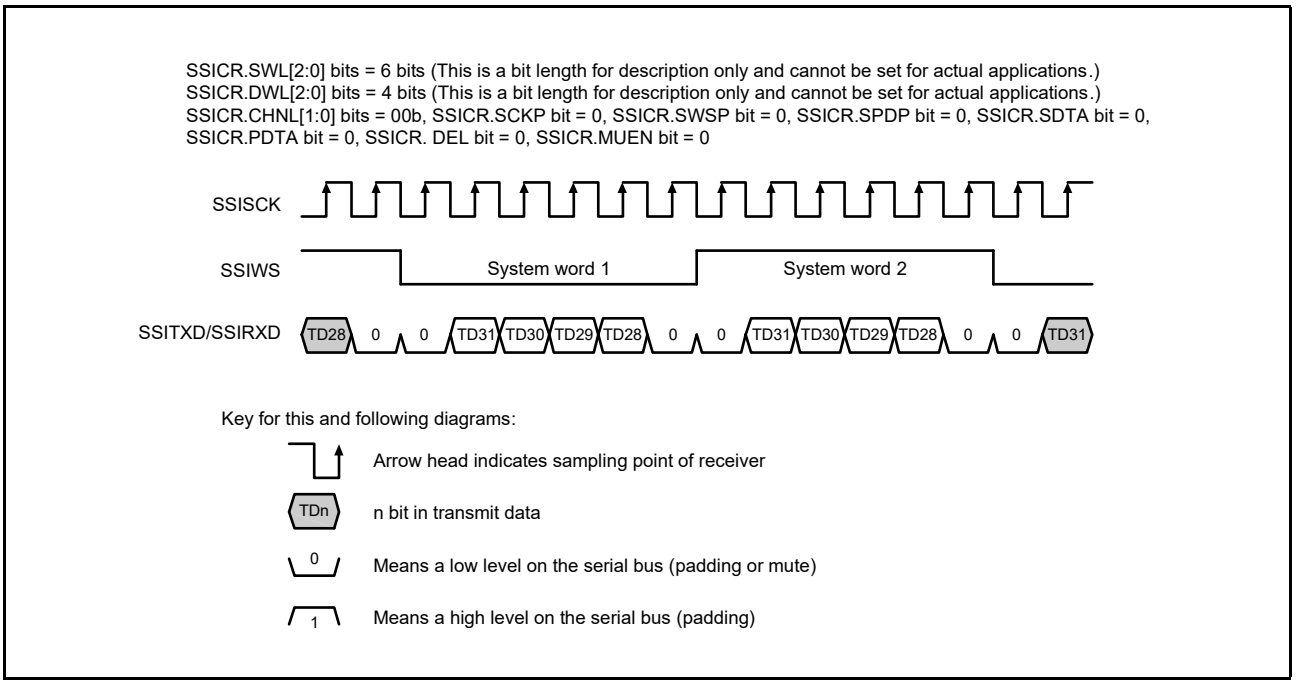


Figure 39.6 Basic Sample Format (Transmit Mode with Example System/Data Word Length)

- Inverted Clock

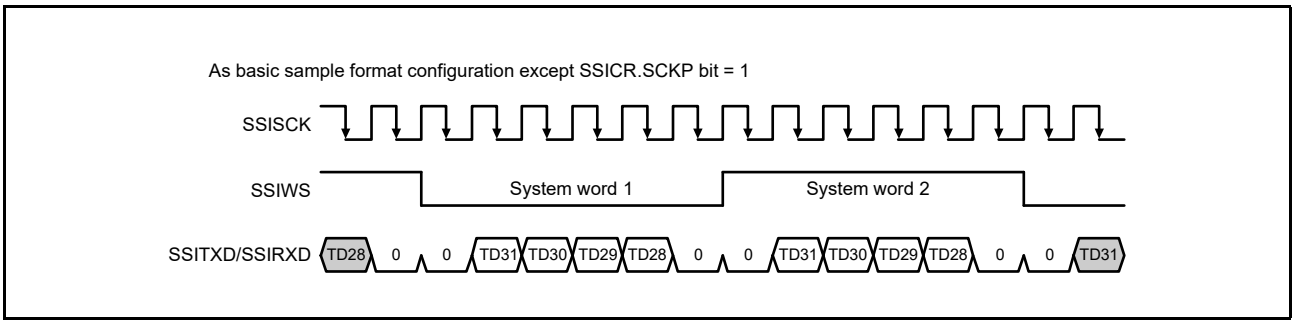


Figure 39.7 Inverted Clock

- Inverted Word Select

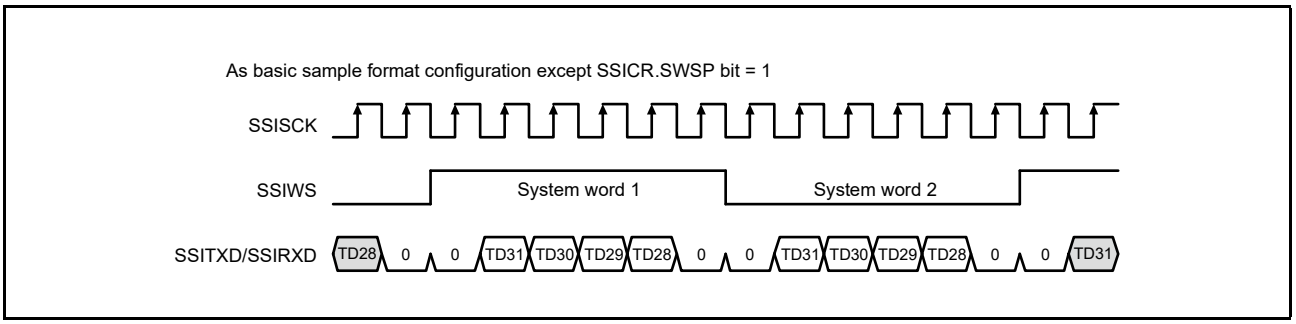


Figure 39.8 Inverted Word Select

- Inverted Padding Polarity

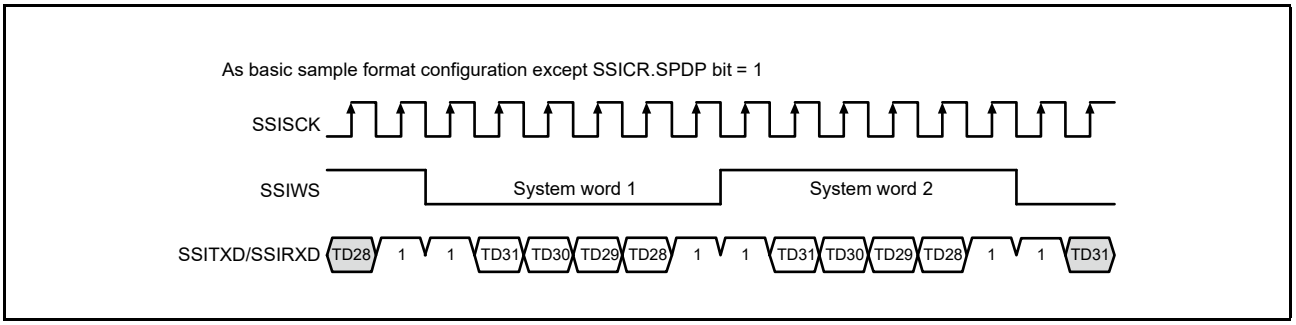


Figure 39.9 Inverted Padding Polarity

- Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Delay

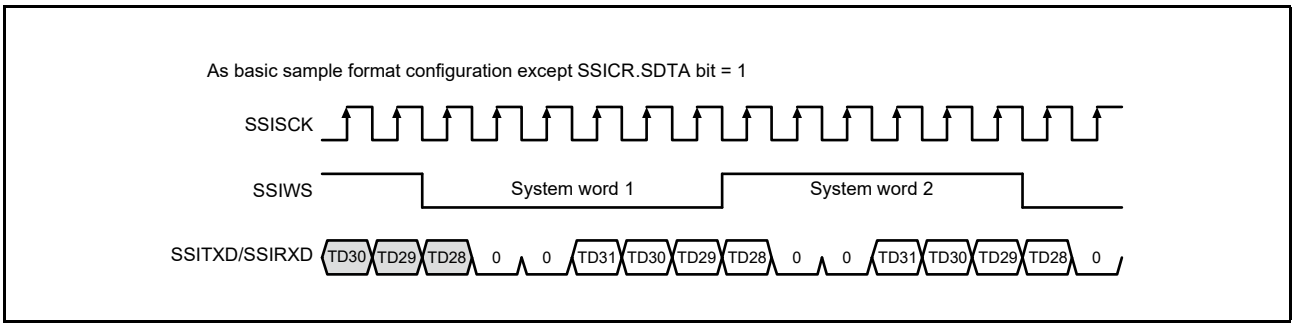


Figure 39.10 Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Delay

- Transmitting and Receiving in the Order of Padding Bits and Serial Data; without Delay

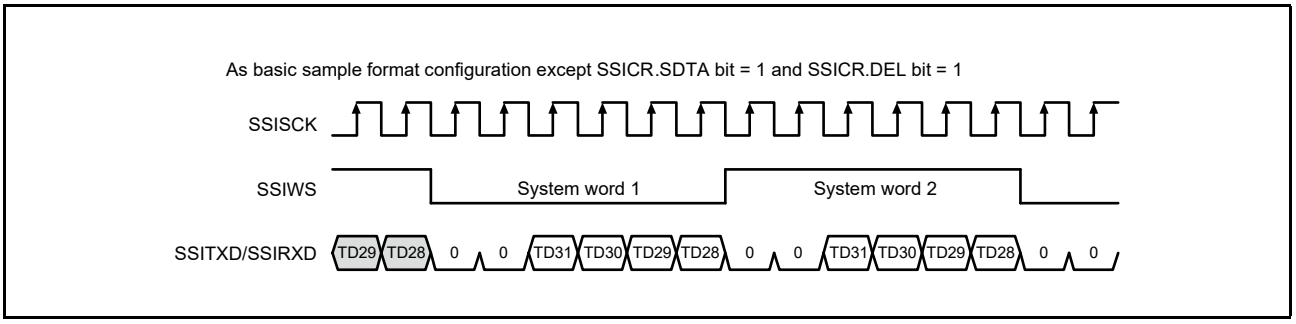


Figure 39.11 Transmitting and Receiving in the Order of Padding Bits and Serial Data; without Delay

- Transmitting and Receiving in the Order of Serial Data and Padding Bits; without Delay

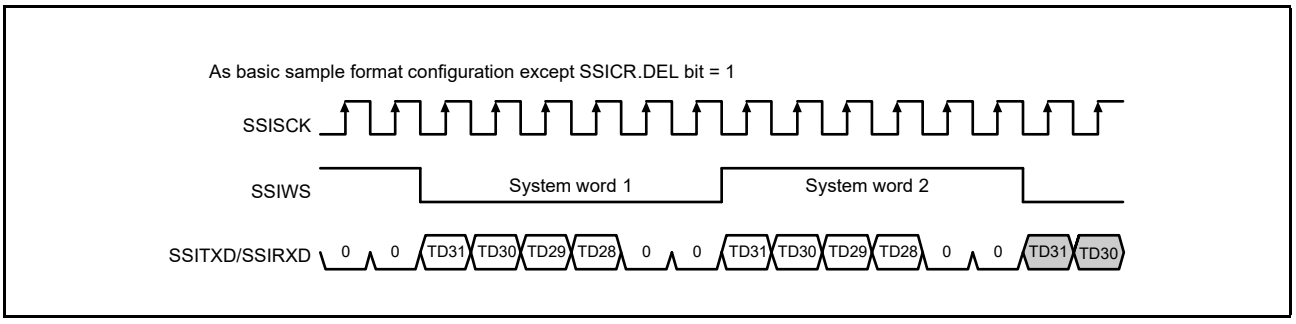


Figure 39.12 Transmitting and Receiving in the Order of Serial Data and Padding Bits; without Delay

- Parallel Right-Aligned with Delay

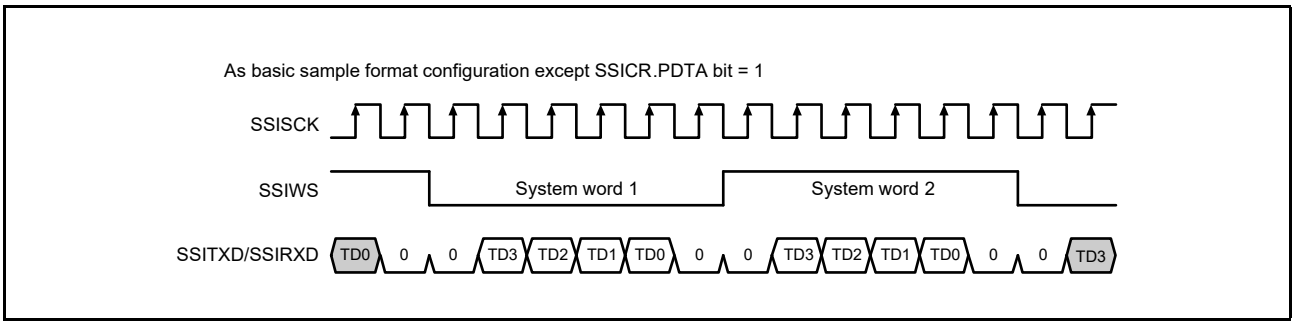


Figure 39.13 Parallel Right-Aligned with Delay

- Mute Enabled

When the SSICR.MUEN bit is set to 1, the SSITXD pin is set to 0 without synchronizing SSIWS.

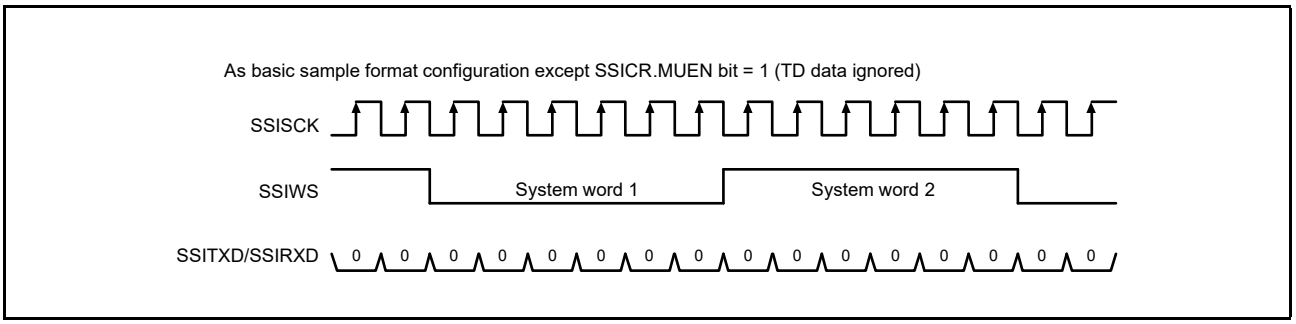


Figure 39.14 Mute Enabled

39.3.3 WS Continue Mode

In WS continue mode, the SSIWS signal continues to be output irrespective whether data transfer is enabled or disabled. This mode can be set using the SSITDMR.CONT bit. With this mode enabled, the SSIWS signal does not stop but continues operating even if the SSICR.TEN and REN bits are both set to 0 (transfer disabled). With this mode disabled, the SSIWS signal stops if the SSICR.TEN and REN bits are both set to 0.

Figure 39.15 and Figure 39.16 show the operations with WS continue mode enabled and disabled, respectively.

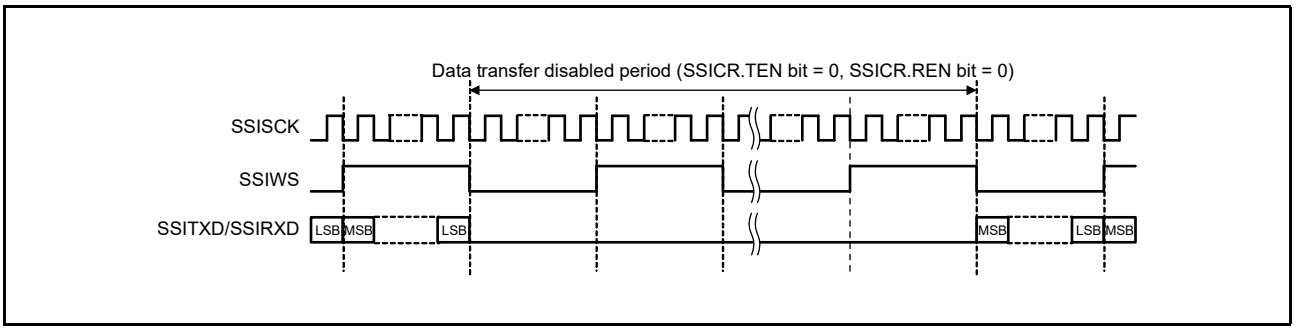


Figure 39.15 WS Continue Mode Enabled

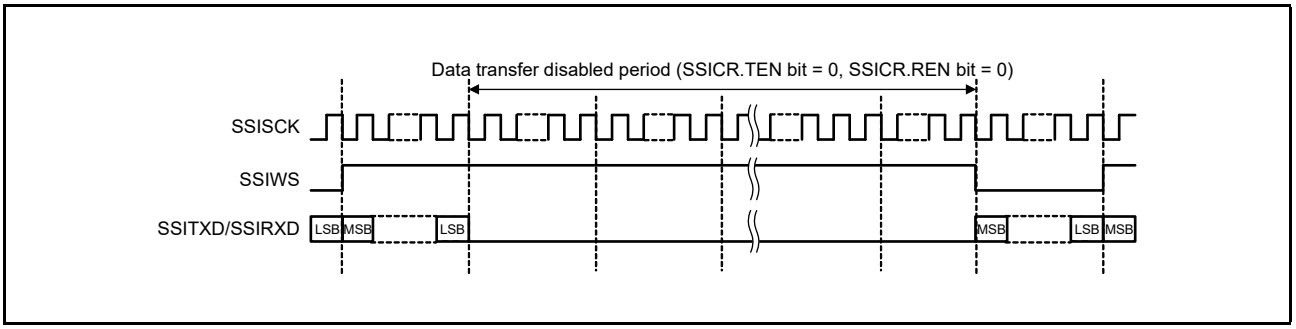


Figure 39.16 WS Continue Mode Disabled

39.3.4 Operating States

There are three states of operation: idle, communication, and waiting for idle. Figure 39.17 shows the operating state transitions.

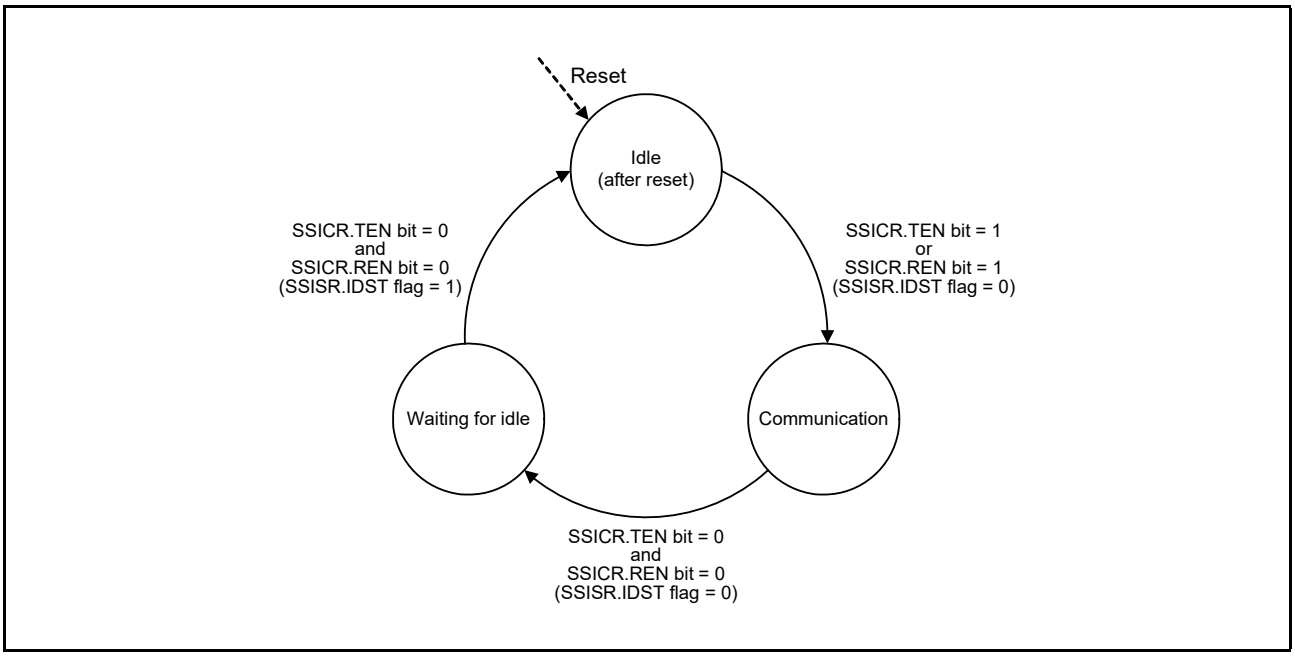


Figure 39.17 Operating State Transitions

(1) Idle State

This module enters this state when the MSTPCRD.MSTPD10, MSTPD11, and MSTPD15 bits are set to 0 after a reset is released. All required configuration fields in the control register should be defined in this state. After the settings are made, the module enters communication enabled state when the SSICR.TEN bit or SSICR.REN bit is set to 1.

(2) Communication State

Communication in this state depends on the selected operating state. For details, refer to section 39.3.5, Transmit Operation and section 39.3.6, Receive Operation.

(3) Waiting for Idle

This module enters this state when both the SSICR.TEN and SSICR.REN bits are set to 0 in communication state. If system word communication is completed in this state, the SSISR.IDST flag is set to 1 and this module enters the idle state.

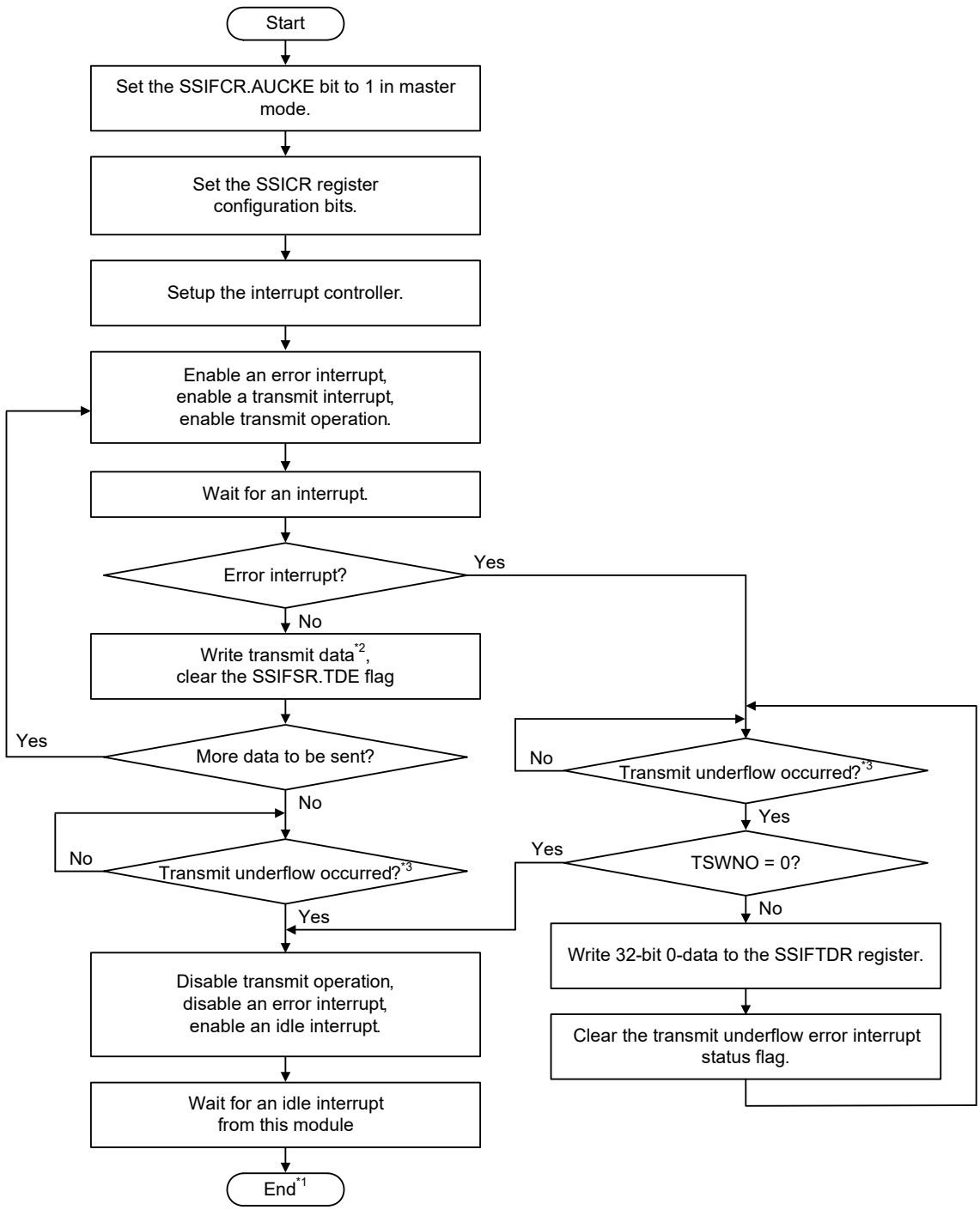
39.3.5 Transmit Operation

Transmission can be controlled by an interrupt that the SSI generates to supply data. In transmission using interrupts, write transmit data in 64-bit units regardless of the data format. If transmit data ends on a 32-bit boundary, write 32-bit 0-data (0000 0000h) after the last transmit data is written, and complete writing on a 64-bit boundary.
When stopping transmission, stop writing to the SSIFTDR register while 64-bit writing is completed. After writing is stopped, wait until a transmit underflow occurs before setting the TEN bit to 0. During transmit underflow, the last data input to SSIFTDR is continuously transmitted until this module enters the idle state. After the TEN bit is set to 0, the clock*1 should continue to be supplied until the SSISR.IIRQ flag indicates that the module is in the idle state. If a transmit underflow error or transmit overflow error occurs during data transmission, transmit data to SSIFTDR may not be written in a 64-bit units. In that case, stop writing data, wait until a transmit underflow error occurs, and check the TSWNO when the transmit underflow has occurred. When the TSWNO bit is 1, write 32-bit 0-data (0000 0000h) to SSIFTDR and wait until an underrun occurs again. Once the TSWNO bit is confirmed to be 0, after the TEN bit is set to 0, the clock*1 continue to be supplied until the SSISR.IIRQ flag indicates that the module is in the idle state.

Figure 39.18 shows transmission using interrupts.

Note 1. Input clock from the SSISCK pin when SSICR.SCKD bit = 0.
Master clock when SSICR.SCKD bit = 1.

(1) Transmission Using Interrupts



Note 1. If an error interrupt (underflow/overflow) occurs, go back to the start in the flowchart again.
Note 2. Write transmit data in 64-bit units regardless of the data word setting.
Note 3. Stop writing transmit data to the SSIFTDR register and wait until a transmit underflow occurs. During transmit underflow, the last data input to SSIFTDR is continuously transmitted until the module is in the idle state.

Figure 39.18 Transmission Using Interrupts

39.3.6 Receive Operation

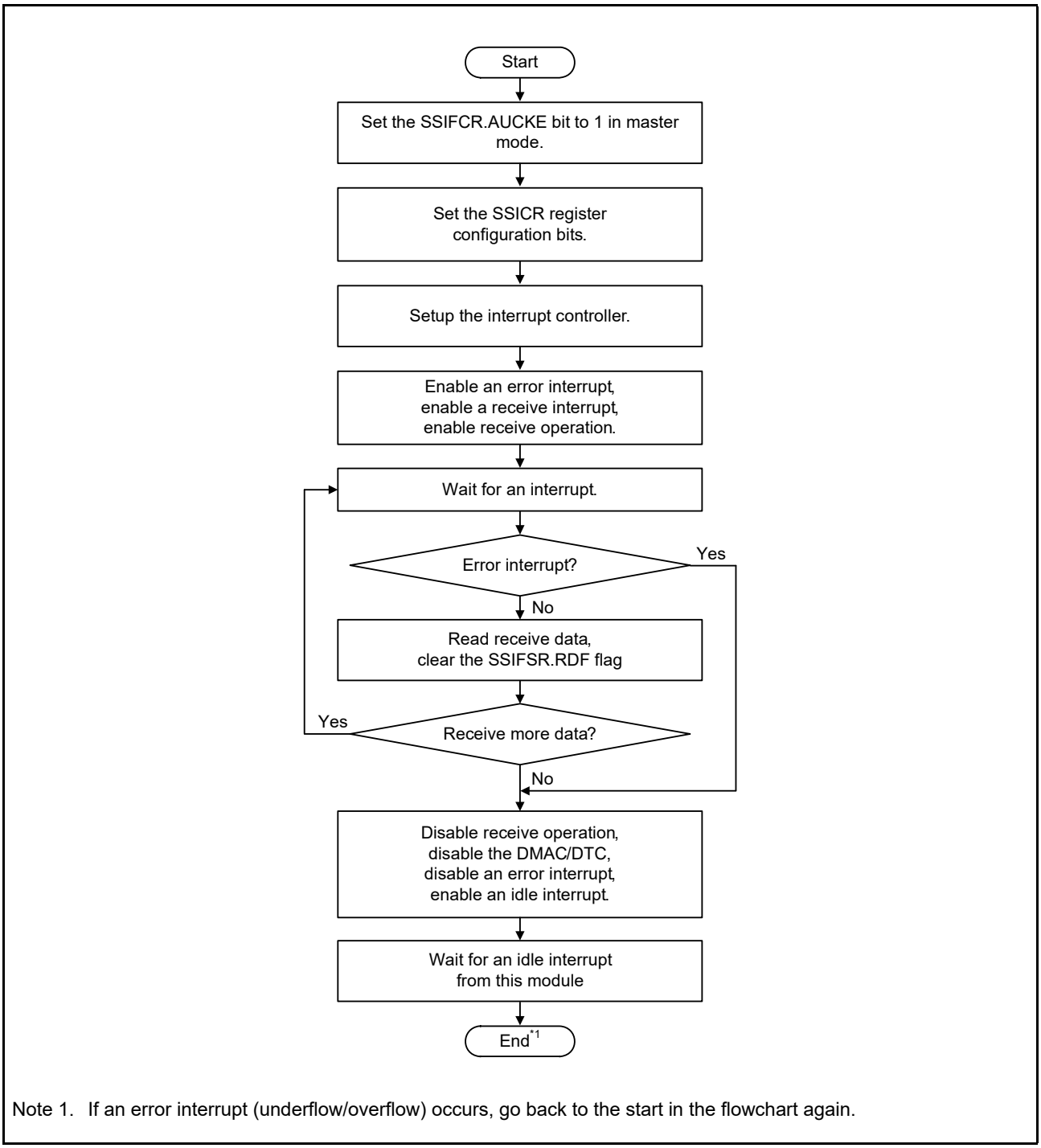
Like transmission, reception can be controlled by interrupt.

Figure 39.19 shows the flow of operation.

When disabling this module, the clock*1 continue to be supplied to this module until the SSISR.IIRQ bit indicates that the module is in the idle state.

Note 1. Input clock from the SSISCK pin when SSICR.SCKD bit = 0.
Master clock when SSICR.SCKD bit = 1.

(1) Reception Using Interrupt-Driven Data Flow Control



Note 1. If an error interrupt (underflow/overflow) occurs, go back to the start in the flowchart again.

Figure 39.19 Reception Using Interrupts

39.3.7 Serial Bit Clock Control

The SSI controls and selects the clock to be used for the serial bus interface, according to the SCKD and CKDV bit setting.
If the serial bit clock direction is set to input (SSICR.SCKD bit = 0), this module is in clock slave mode and the shift register uses the bit clock that was input to the SSISCK pin.

If the serial bit clock direction is set to output (SSICR.SCKD bit = 1), this module is in clock master mode, and the shift register uses the master clock or a divided master clock as the bit clock. The master clock is divided by the ratio specified by the SSICR.CKDV[3:0] bits for use as the bit clock by the shift register.
In either case the module pin, SSISCK, is the same as the bit clock.

39.4 Interrupt Sources

Table 39.6 lists the interrupt sources of the SSI. Each interrupt source can be enabled or disabled by the SSICR.TUIEN, TOIEN, RUIEN, ROIEN and IIEN bits, and the SSIFCR.TIE and RIE bits.

Table 39.6 SSI Interrupt Sources

Interrupt Source	Description	Interrupt Flag
SSIF	Transmit underflow interrupt, Transmit overflow interrupt, Receive underflow interrupt, Receive overflow interrupt, Idle interrupt	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ
SSIRXI	Receive data full interrupt	SSIFSR.RDF
SSITXI	Transmit data empty interrupt	SSIFSR.TDE

39.5 Usage Notes

39.5.1 Setting the Module Stop Function

Module stop state can be entered or released using the MSTPCRD register. The initial setting is for operation of the SSI to be stopped. SSI register access is enabled by releasing the module stop state.
For details on the MSTPCRD register, refer to section 9, Low-Power Consumption Function.

39.5.2 Notes on Changing Transfer Modes

For mode transitions between the transmitter, receiver, and transceiver while WS continue mode is disabled (SSITDMR.CONT = 0), set the SSICR.TEN and SSICR.REN bits to 0 and make a transition to the idle state once. Set the SSICR.TEN and SSICR.REN bits again while the module is in the idle state and restart transfer.

39.5.3 Limits on WS Continue Mode

If WS continue mode setting is changed, the operation of the SSISCK and SSIWS signals immediately after switching are not guaranteed. If it affects the device to be connected, do not change the setting dynamically.

40. Boundary Scan

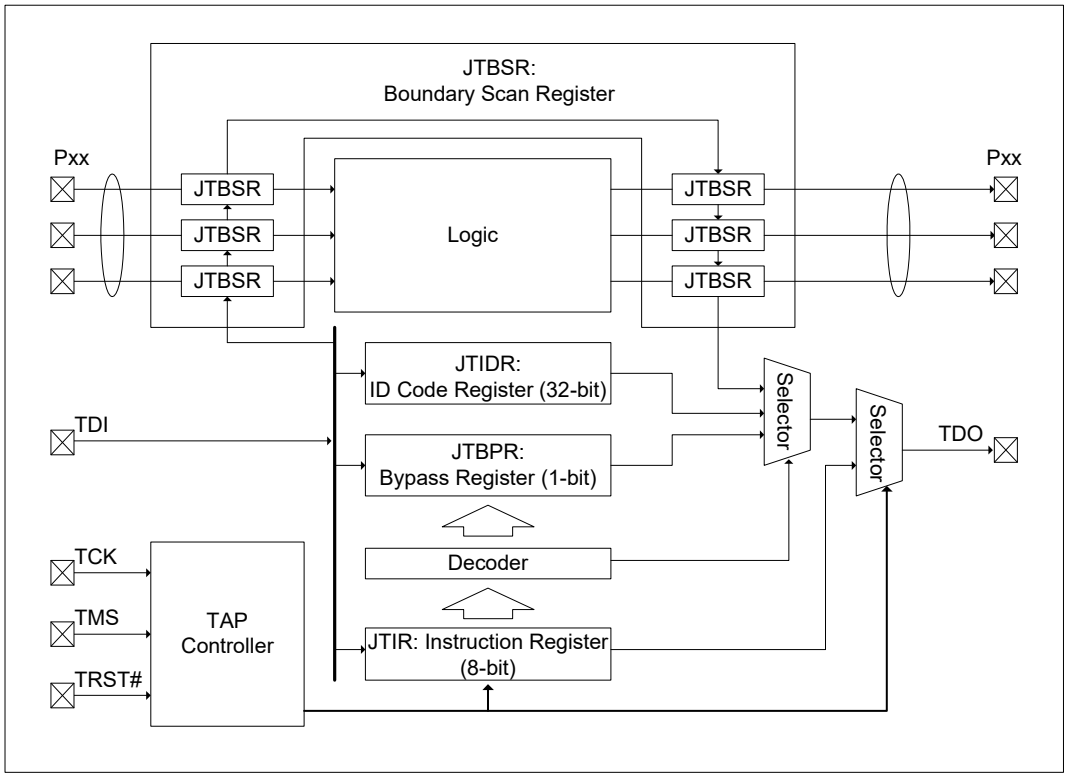
This LSI has the boundary scan function.
The boundary scan is a serial I/O interface based on the JTAG (Joint Test Action Group, IEEE Std.1149.1 and IEEE Standard Test Access Port and Boundary-Scan Architecture).

40.1 Overview

Table 40.1 lists the specifications of boundary scan.
Figure 40.1 shows a block diagram of the boundary scan function.

Table 40.1 Specifications of Boundary Scan

Item	Specifications
Boundary scan enabled/disabled	Boundary scan is enabled when the BSCANP pin is driven high.
Dedicated boundary scan pins	The TDO, TCK, TDI, TMS, and TRST# pins are dedicated for the JTAG when the boundary scan function is enabled.
Six test modes	BYPASS mode EXTEST mode SAMPLE/PRELOAD mode CLAMP mode HIGHZ mode IDCODE mode



JTBPR: Bypass register
JTBSR: Boundary scan register
JTIR: Instruction register
JTDIR: ID code register

Figure 40.1 JTAG Block Diagram

Table 40.2 shows the I/O pins used in the boundary scan function.

Table 40.2 Pin Configuration of JTAG

Pin Name	I/O	Description
TCK	Input	Test clock input pin Clock signal for boundary scan. Input the clock the duty cycle of which is 50% when boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin
TRST#	Input	Test reset input pin

40.2 Register Descriptions

Instructions can be input to the instruction register via the TDI pin by serial transfer.
The bypass register, which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode.
The boundary scan register, which is configured according to Table 40.5, is connected between the TDI and TDO pins when test data are being shifted in.
None of the registers is accessible from the CPU. Table 40.3 shows the availability of serial transfer for the registers.

Table 40.3 Serial Transfer for the Registers

Register	Serial Input	Serial Output
Instruction register	Available	Available
ID code register	Available	Available
Bypass register	Available	Available
Boundary scan register	Available	Available

Note: Any serial transfer is available if standards for the boundary scan function are satisfied.

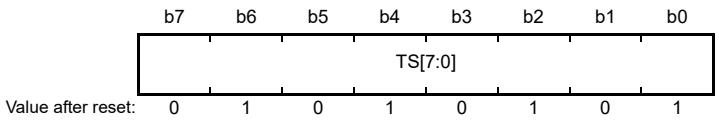
40.2.1 Instruction Register (JTIR)

The JTIR register is an 8-bit register.

Boundary scan instructions can be transferred to the instruction register by serial input from the TDI pin.

The instruction register is initialized when the TRST# pin is driven to the low level, or when the TAP controller is in the Test-Logic-Reset state.

Address(es): —



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	TS[7:0]	Test Bit Set	The command configuration is as shown in Table 40.4.	—

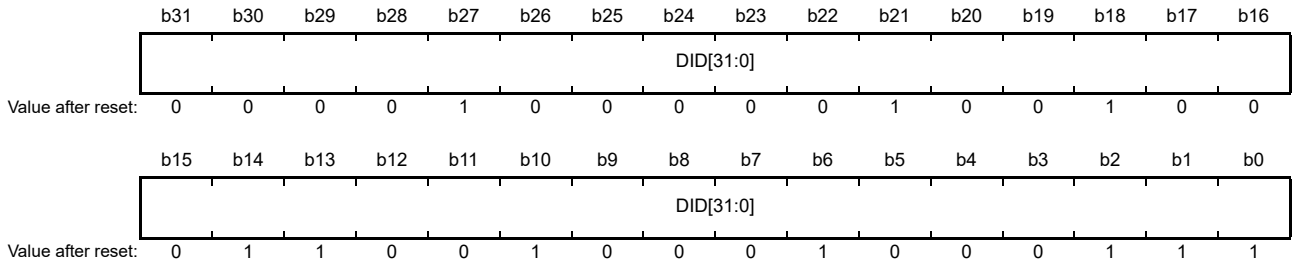
Table 40.4 Command Configuration

TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	Instruction
0	0	0	0	0	0	0	0	EXTEST
0	1	0	0	0	0	0	0	SAMPLE/PRELOAD
0	1	0	1	0	1	0	1	IDCODE (value after reset)
1	1	0	1	0	0	0	0	CLAMP
1	0	0	0	0	0	0	0	HIGHZ
1	1	1	1	1	1	1	1	BYPASS
Other than above								Reserved

40.2.2 ID Code Register (JTIDR)

The JTIDR register is a 32-bit register.
ID code register data is output from the TDO pin when the IDCODE instruction is executed.

Address(es): —



Bit	Symbol	Bit Name	Description	R/W
b31-b0	DID[31:0]	Reserved	This register has the fixed value that indicates the device IDCODE.	—

40.2.3 Bypass Register (JTBPR)

The JTBPR register is a 1-bit register.
This register is connected between the TDI and TDO pins when BYPASS mode is set.
The JTBPR register cannot be read from or written to by the CPU.

40.2.4 Boundary Scan Register (JTBSR)

The JTBSR register is a shift register which is located in the pad to control the external input and output pins of this LSI chip.
The EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ commands can be used to perform boundary-scan testing.
Table 40.5 shows the correspondence between the pins of this LSI chip and the bits of the boundary scan register.
The value is undefined after a reset.

Table 40.5 Boundary Scan Register (320FBGA) (1 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
R3	P30	Input	643
R5	PN0	Output	642
		Output enable	641
		Input	640
P5	P31	Output	639
		Output enable	638
		Input	637
U3	PN1	Output	636
		Output enable	635
		Input	634
T3	P32	Output	633
		Output enable	632
		Input	631
U1	P60	Output	630
		Output enable	629
		Input	628
R6	PN2	Output	627
		Output enable	626
		Input	625
V1	P61	Output	624
		Output enable	623
		Input	622
W1	P62	Output	621
		Output enable	620
		Input	619
V3	PN3	Output	618
		Output enable	617
		Input	616
U2	P63	Output	615
		Output enable	614
		Input	613
V4	PN4	Output	612
		Output enable	611
		Input	610
V2	P64	Output	609
		Output enable	608
		Input	607
W2	P65	Output	606
		Output enable	605
		Input	604
Y3	P66	Output	603
		Output enable	602
		Input	601
W3	PN5	Output	600
		Output enable	599
		Input	598

Table 40.5 Boundary Scan Register (320FBGA) (2 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
Y2	P67	Output	597
		Output enable	596
		Input	595
W4	PN6	Output	594
		Output enable	593
		Input	592
T5	PC6	Input	590
Y4	PN7	Output	589
		Output enable	588
		Input	587
V5	PC7	Input	585
T7	P36	Output	584
		Output enable	583
		Input	582
W5	PP0	Output	581
		Output enable	580
		Input	579
T6	P37	Output	578
		Output enable	577
		Input	576
Y5	PP1	Output	575
		Output enable	574
		Input	573
R7	PG0	Output	572
		Output enable	571
		Input	570
V6	PG1	Output	569
		Output enable	568
		Input	567
R8	PG2	Output	566
		Output enable	565
		Input	564
W6	PP2	Output	563
		Output enable	562
		Input	561
T8	PG3	Output	560
		Output enable	559
		Input	558
Y6	PP3	Output	557
		Output enable	556
		Input	555
V7	PG4	Output	554
		Output enable	553
		Input	552
V8	PG5	Output	551
		Output enable	550
		Input	549

Table 40.5 Boundary Scan Register (320FBGA) (3 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
W7	PP4	Output	548
		Output enable	547
		Input	546
T9	PG6	Output	545
		Output enable	544
		Input	543
Y7	PP5	Output	542
		Output enable	541
		Input	540
R9	PG7	Output	539
		Output enable	538
		Input	537
V9	PH0	Output	536
		Output enable	535
		Input	534
V10	PH1	Output	533
		Output enable	532
		Input	531
W8	PP6	Output	530
		Output enable	529
		Input	528
R10	PH2	Output	527
		Output enable	526
		Input	525
W9	PP7	Output	524
		Output enable	523
		Input	522
T10	PH3	Output	521
		Output enable	520
		Input	519
R11	PH4	Output	518
		Output enable	517
		Input	516
Y9	PR0	Output	515
		Output enable	514
		Input	513
T12	PH5	Output	512
		Output enable	511
		Input	510
W10	PR1	Output	509
		Output enable	508
		Input	507
R12	PH6	Output	506
		Output enable	505
		Input	504
V11	PH7	Output	503
		Output enable	502
		Input	501

Table 40.5 Boundary Scan Register (320FBGA) (4 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
W13	P24	Output	500
		Output enable	499
		Input	498
V13	P21	Output	497
		Output enable	496
		Input	495
Y10	PR2	Output	494
		Output enable	493
		Input	492
W14	P22	Output	491
		Output enable	490
		Input	489
W11	PR3	Output	488
		Output enable	487
		Input	486
R13	P23	Output	485
		Output enable	484
		Input	483
V12	P20	Output	482
		Output enable	481
		Input	480
Y14	P25	Output	479
		Output enable	478
		Input	477
Y11	PR4	Output	476
		Output enable	475
		Input	474
T14	P26	Output	473
		Output enable	472
		Input	471
W12	PR5	Output	470
		Output enable	469
		Input	468
R14	P27	Output	467
		Output enable	466
		Input	465
W15	P44	Output	464
		Output enable	463
		Input	462
Y15	P41	Output	461
		Output enable	460
		Input	459
Y12	PR6	Output	458
		Output enable	457
		Input	456
Y16	P42	Output	455
		Output enable	454
		Input	453

Table 40.5 Boundary Scan Register (320FBGA) (5 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
Y13	PR7	Output	452
		Output enable	451
		Input	450
Y17	P40	Output	449
		Output enable	448
		Input	447
W16	P43	Output	446
		Output enable	445
		Input	444
V15	P45	Output	443
		Output enable	442
		Input	441
Y18	PS0	Output	440
		Output enable	439
		Input	438
V16	P46	Output	437
		Output enable	436
		Input	435
W17	PS1	Output	434
		Output enable	433
		Input	432
R15	P47	Output	431
		Output enable	430
		Input	429
Y19	P10	Output	428
		Output enable	427
		Input	426
U18	P00	Output	425
		Output enable	424
		Input	423
V17	PS2	Output	422
		Output enable	421
		Input	420
V19	P01	Output	419
		Output enable	418
		Input	417
W18	PS3	Output	416
		Output enable	415
		Input	414
V20	P02	Output	413
		Output enable	412
		Input	411
U20	P03	Output	410
		Output enable	409
		Input	408
W19	PS4	Output	407
		Output enable	406
		Input	405

Table 40.5 Boundary Scan Register (320FBGA) (6 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
U19	P04	Output	404
		Output enable	403
		Input	402
V18	P05	Output	401
		Output enable	400
		Input	399
W20	PS5	Output	398
		Output enable	397
		Input	396
P15	P06	Output	395
		Output enable	394
		Input	393
R19	PS6	Output	392
		Output enable	391
		Input	390
P16	P07	Output	389
		Output enable	388
		Input	387
T19	PE0	Output	386
		Output enable	385
		Input	384
R20	PS7	Output	383
		Output enable	382
		Input	381
T20	PE1	Output	380
		Output enable	379
		Input	378
N15	PE2	Output	377
		Output enable	376
		Input	375
P19	PT0	Output	374
		Output enable	373
		Input	372
P18	PE3	Output	371
		Output enable	370
		Input	369
P20	PT1	Output	368
		Output enable	367
		Input	366
N16	PE4	Output	365
		Output enable	364
		Input	363
N18	PE5	Output	362
		Output enable	361
		Input	360
N19	PT2	Output	359
		Output enable	358
		Input	357

Table 40.5 Boundary Scan Register (320FBGA) (7 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
M16	PE6	Output	356
		Output enable	355
		Input	354
L16	PE7	Output	353
		Output enable	352
		Input	351
M18	P70	Output	350
		Output enable	349
		Input	348
N20	PT3	Output	347
		Output enable	346
		Input	345
M20	P71	Output	344
		Output enable	343
		Input	342
M19	PT4	Output	341
		Output enable	340
		Input	339
L18	P72	Output	338
		Output enable	337
		Input	336
L19	P73	Output	335
		Output enable	334
		Input	333
L20	P74	Output	332
		Output enable	331
		Input	330
K19	P75	Output	329
		Output enable	328
		Input	327
K20	PT5	Output	326
		Output enable	325
		Input	324
K18	P76	Output	323
		Output enable	322
		Input	321
J20	PT6	Output	320
		Output enable	319
		Input	318
K16	P77	Output	317
		Output enable	316
		Input	315
J18	PA0	Output	314
		Output enable	313
		Input	312
J19	PT7	Output	311
		Output enable	310
		Input	309

Table 40.5 Boundary Scan Register (320FBGA) (8 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
J16	PA1	Output	308
		Output enable	307
		Input	306
H18	PA2	Output	305
		Output enable	304
		Input	303
H19	PK0	Output	302
		Output enable	301
		Input	300
G19	PA3	Output	299
		Output enable	298
		Input	297
H20	PK1	Output	296
		Output enable	295
		Input	294
G18	PA4	Output	293
		Output enable	292
		Input	291
G20	P11	Output	290
		Output enable	289
		Input	288
G15	PK3	Output	287
		Output enable	286
		Input	285
H16	PA5	Output	284
		Output enable	283
		Input	282
F20	P12	Output	281
		Output enable	280
		Input	279
H15	PA6	Output	278
		Output enable	277
		Input	276
F15	PK2	Output	275
		Output enable	274
		Input	273
G16	PA7	Output	272
		Output enable	271
		Input	270
F16	P90	Output	269
		Output enable	268
		Input	267
F19	P91	Output	266
		Output enable	265
		Input	264
F18	P92	Output	263
		Output enable	262
		Input	261

Table 40.5 Boundary Scan Register (320FBGA) (9 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
E20	P93	Output	260
		Output enable	259
		Input	258
E19	P94	Output	257
		Output enable	256
		Input	255
D20	P95	Output	254
		Output enable	253
		Input	252
D19	P96	Output	251
		Output enable	250
		Input	249
E18	P97	Output	248
		Output enable	247
		Input	246
C20	P13	Output	245
		Output enable	244
		Input	243
D18	PD0	Output	242
		Output enable	241
		Input	240
C19	P14	Output	239
		Output enable	238
		Input	237
E16	PD1	Output	236
		Output enable	235
		Input	234
B20	P15	Output	233
		Output enable	232
		Input	231
B19	P16	Output	230
		Output enable	229
		Input	228
C18	PD2	Output	227
		Output enable	226
		Input	225
A19	P17	Output	224
		Output enable	223
		Input	222
F14	PD3	Output	221
		Output enable	220
		Input	219
E14	PD4	Output	218
		Output enable	217
		Input	216
F13	P50	Output	215
		Output enable	214
		Input	213

Table 40.5 Boundary Scan Register (320FBGA) (10 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
C13	P51	Output	212
		Output enable	211
		Input	210
B12	P52	Output	209
		Output enable	208
		Input	207
C12	P53	Output	206
		Output enable	205
		Input	204
A11	P54	Output	203
		Output enable	202
		Input	201
F12	P55	Output	200
		Output enable	199
		Input	198
E13	P56	Output	197
		Output enable	196
		Input	195
E12	PD5	Output	194
		Output enable	193
		Input	192
C11	PD6	Output	191
		Output enable	190
		Input	189
B11	PD7	Output	188
		Output enable	187
		Input	186
B10	P86	Output	185
		Output enable	184
		Input	183
C10	P87	Output	182
		Output enable	181
		Input	180
C9	PF5	Output	179
		Output enable	178
		Input	177
F11	PK4	Output	176
		Output enable	175
		Input	174
A9	PF6	Output	173
		Output enable	172
		Input	171
E11	PK6	Output	170
		Output enable	169
		Input	168
B9	PB7	Output	167
		Output enable	166
		Input	165

Table 40.5 Boundary Scan Register (320FBGA) (11 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
A8	PC0	Input	163
B8	PC1	Input	161
E10	PK7	Output	160
		Output enable	159
		Input	158
A7	PB0	Output	157
		Output enable	156
		Input	155
F10	PK5	Output	154
		Output enable	153
		Input	152
C8	PB1	Output	151
		Output enable	150
		Input	149
E9	PL0	Output	148
		Output enable	147
		Input	146
B7	PB2	Output	145
		Output enable	144
		Input	143
F9	PL1	Output	142
		Output enable	141
		Input	140
C7	PB3	Output	139
		Output enable	138
		Input	137
E8	PL2	Output	136
		Output enable	135
		Input	134
A6	PB4	Output	133
		Output enable	132
		Input	131
F8	PL3	Output	130
		Output enable	129
		Input	128
B6	PB5	Output	127
		Output enable	126
		Input	125
E7	PL4	Output	124
		Output enable	123
		Input	122
C6	PB6	Output	121
		Output enable	120
		Input	119
C5	PL5	Output	118
		Output enable	117
		Input	116

Table 40.5 Boundary Scan Register (320FBGA) (12 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
A5	PF7	Output	115
		Output enable	114
		Input	113
B5	PJ0	Output	112
		Output enable	111
		Input	110
A4	PJ1	Output	109
		Output enable	108
		Input	107
B4	PJ2	Output	106
		Output enable	105
		Input	104
A3	PJ3	Output	103
		Output enable	102
		Input	101
A2	PC2	Input	99
B2	PJ4	Output	98
		Output enable	97
		Input	96
E6	PL6	Output	95
		Output enable	94
		Input	93
B3	PC3	Input	91
C4	PL7	Output	90
		Output enable	89
		Input	88
B1	PJ5	Output	87
		Output enable	86
		Input	85
E5	PU0	Output	84
		Output enable	83
		Input	82
E3	PU1	Output	81
		Output enable	80
		Input	79
C3	PU2	Output	78
		Output enable	77
		Input	76
D3	PU3	Output	75
		Output enable	74
		Input	73
C2	PJ6	Output	72
		Output enable	71
		Input	70
C1	PJ7	Output	69
		Output enable	68
		Input	67

Table 40.5 Boundary Scan Register (320FBGA) (13 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
D2	P80	Output	66
		Output enable	65
		Input	64
E2	P82	Output	63
		Output enable	62
		Input	61
F5	PU4	Output	60
		Output enable	59
		Input	58
F3	P85	Output	57
		Output enable	56
		Input	55
D1	P81	Output	54
		Output enable	53
		Input	52
H5	ERROROUT#	Output	51
		Output enable	50
F2	P83	Output	48
		Output enable	47
		Input	46
H3	P35	Output	45
		Output enable	44
		Input	43
E1	P84	Output	42
		Output enable	41
		Input	40
G5	PU5	Output	39
		Output enable	38
		Input	37
G6	PM0	Output	36
		Output enable	35
		Input	34
F1	PC4	Input	32
G2	PC5	Input	30
G1	PU6	Output	29
		Output enable	28
		Input	27
H1	PU7	Output	26
		Output enable	25
		Input	24
H2	PM1	Output	23
		Output enable	22
		Input	21
J3	PM2	Output	20
		Output enable	19
		Input	18

Table 40.5 Boundary Scan Register (320FBGA) (14 / 14)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
J2	PM3	Output	17
		Output enable	16
		Input	15
J1	PM6	Output	14
		Output enable	13
		Input	12
K3	PM4	Output	11
		Output enable	10
		Input	9
K2	PM5	Output	8
		Output enable	7
		Input	6
K1	PM7	Output	5
		Output enable	4
		Input	3
N3	RSTOUT#	Output	2
		Output enable	1
To TDO			

Table 40.6 Boundary Scan Register (176HLFQFP) (1 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
40	P30	Input	643
41	P60	Output	630
		Output enable	629
		Input	628
42	P61	Output	624
		Output enable	623
		Input	622
44	P62	Output	621
		Output enable	620
		Input	619
46	P63	Output	615
		Output enable	614
		Input	613
47	P64	Output	609
		Output enable	608
		Input	607
48	P65	Output	606
		Output enable	605
		Input	604
51	P36	Output	584
		Output enable	583
		Input	582
52	P37	Output	578
		Output enable	577
		Input	576
53	PG0	Output	572
		Output enable	571
		Input	570
54	PG1	Output	569
		Output enable	568
		Input	567
56	PG2	Output	566
		Output enable	565
		Input	564
57	PG3	Output	560
		Output enable	559
		Input	558
58	PG4	Output	554
		Output enable	553
		Input	552
59	PG5	Output	551
		Output enable	550
		Input	549
60	PG6	Output	545
		Output enable	544
		Input	543

Table 40.6 Boundary Scan Register (176HLFQFP) (2 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
61	PG7	Output	539
		Output enable	538
		Input	537
62	PH0	Output	536
		Output enable	535
		Input	534
63	PH1	Output	533
		Output enable	532
		Input	531
64	PH2	Output	527
		Output enable	526
		Input	525
65	PH3	Output	521
		Output enable	520
		Input	519
68	PH4	Output	518
		Output enable	517
		Input	516
69	PH5	Output	512
		Output enable	511
		Input	510
70	PH6	Output	506
		Output enable	505
		Input	504
71	PH7	Output	503
		Output enable	502
		Input	501
72	P24	Output	500
		Output enable	499
		Input	498
73	P21	Output	497
		Output enable	496
		Input	495
74	P22	Output	491
		Output enable	490
		Input	489
75	P23	Output	485
		Output enable	484
		Input	483
76	P20	Output	482
		Output enable	481
		Input	480
77	P25	Output	479
		Output enable	478
		Input	477
78	P26	Output	473
		Output enable	472
		Input	471

Table 40.6 Boundary Scan Register (176HLFQFP) (3 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
79	P27	Output	467
		Output enable	466
		Input	465
82	P42	Output	455
		Output enable	454
		Input	453
83	P40	Output	449
		Output enable	448
		Input	447
84	P43	Output	446
		Output enable	445
		Input	444
85	P47	Output	431
		Output enable	430
		Input	429
87	P10	Output	428
		Output enable	427
		Input	426
89	P00	Output	425
		Output enable	424
		Input	423
90	P01	Output	419
		Output enable	418
		Input	417
91	P02	Output	413
		Output enable	412
		Input	411
93	P03	Output	410
		Output enable	409
		Input	408
94	P04	Output	404
		Output enable	403
		Input	402
95	P05	Output	401
		Output enable	400
		Input	399
96	P06	Output	395
		Output enable	394
		Input	393
97	P07	Output	389
		Output enable	388
		Input	387
98	PE0	Output	386
		Output enable	385
		Input	384
99	PE1	Output	380
		Output enable	379
		Input	378

Table 40.6 Boundary Scan Register (176HLFQFP) (4 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
101	PE2	Output	377
		Output enable	376
		Input	375
102	PE3	Output	371
		Output enable	370
		Input	369
103	PE4	Output	365
		Output enable	364
		Input	363
104	PE5	Output	362
		Output enable	361
		Input	360
105	PE6	Output	356
		Output enable	355
		Input	354
106	PE7	Output	353
		Output enable	352
		Input	351
109	P70	Output	350
		Output enable	349
		Input	348
110	P71	Output	344
		Output enable	343
		Input	342
111	P72	Output	338
		Output enable	337
		Input	336
112	P73	Output	335
		Output enable	334
		Input	333
113	P74	Output	332
		Output enable	331
		Input	330
114	P75	Output	329
		Output enable	328
		Input	327
115	P76	Output	323
		Output enable	322
		Input	321
116	P77	Output	317
		Output enable	316
		Input	315
117	PA0	Output	314
		Output enable	313
		Input	312
118	PA1	Output	308
		Output enable	307
		Input	306

Table 40.6 Boundary Scan Register (176HLFQFP) (5 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
121	PA2	Output	305
		Output enable	304
		Input	303
122	PA3	Output	299
		Output enable	298
		Input	297
123	PA4	Output	293
		Output enable	292
		Input	291
124	PA5	Output	284
		Output enable	283
		Input	282
125	PA6	Output	278
		Output enable	277
		Input	276
127	PA7	Output	272
		Output enable	271
		Input	270
130	P13	Output	245
		Output enable	244
		Input	243
131	P14	Output	239
		Output enable	238
		Input	237
132	P15	Output	233
		Output enable	232
		Input	231
133	P16	Output	230
		Output enable	229
		Input	228
134	P17	Output	224
		Output enable	223
		Input	222
150	P51	Output	212
		Output enable	211
		Input	210
151	P54	Output	203
		Output enable	202
		Input	201
152	P56	Output	197
		Output enable	196
		Input	195
153	PD5	Output	194
		Output enable	193
		Input	192
154	PD6	Output	191
		Output enable	190
		Input	189

Table 40.6 Boundary Scan Register (176HLFQFP) (6 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
155	PD7	Output	188
		Output enable	187
		Input	186
156	P86	Output	185
		Output enable	184
		Input	183
157	P87	Output	182
		Output enable	181
		Input	180
158	PF5	Output	179
		Output enable	178
		Input	177
162	PF6	Output	173
		Output enable	172
		Input	171
163	PB7	Output	167
		Output enable	166
		Input	165
164	PC0	Input	163
165	PC1	Input	161
166	PB0	Output	157
		Output enable	156
		Input	155
167	PB1	Output	151
		Output enable	150
		Input	149
168	PB2	Output	145
		Output enable	144
		Input	143
170	PB3	Output	139
		Output enable	138
		Input	137
171	PB4	Output	133
		Output enable	132
		Input	131
172	PB5	Output	127
		Output enable	126
		Input	125
175	PB6	Output	121
		Output enable	120
		Input	119
176	PC2	Input	99
1	PC3	Input	91
5	P82	Output	63
		Output enable	62
		Input	61

Table 40.6 Boundary Scan Register (176HLFQFP) (7 / 7)

From TDI			
Pin No	**Pin Name**	**Type**	**Bit Name**
6	P85	Output	57
		Output enable	56
		Input	55
7	ERROROUT#	Output	51
		Output enable	50
8	P35	Output	45
		Output enable	44
		Input	43
30	RSTOUT#	Output	2
		Output enable	1
To TDO			

40.3 Operation

The boundary scan function is valid when the RES# and BSCANP pins are driven high.

40.3.1 TAP Controller

Figure 40.2 shows the state transition diagram of the TAP controller. Table 40.7 describes each state.

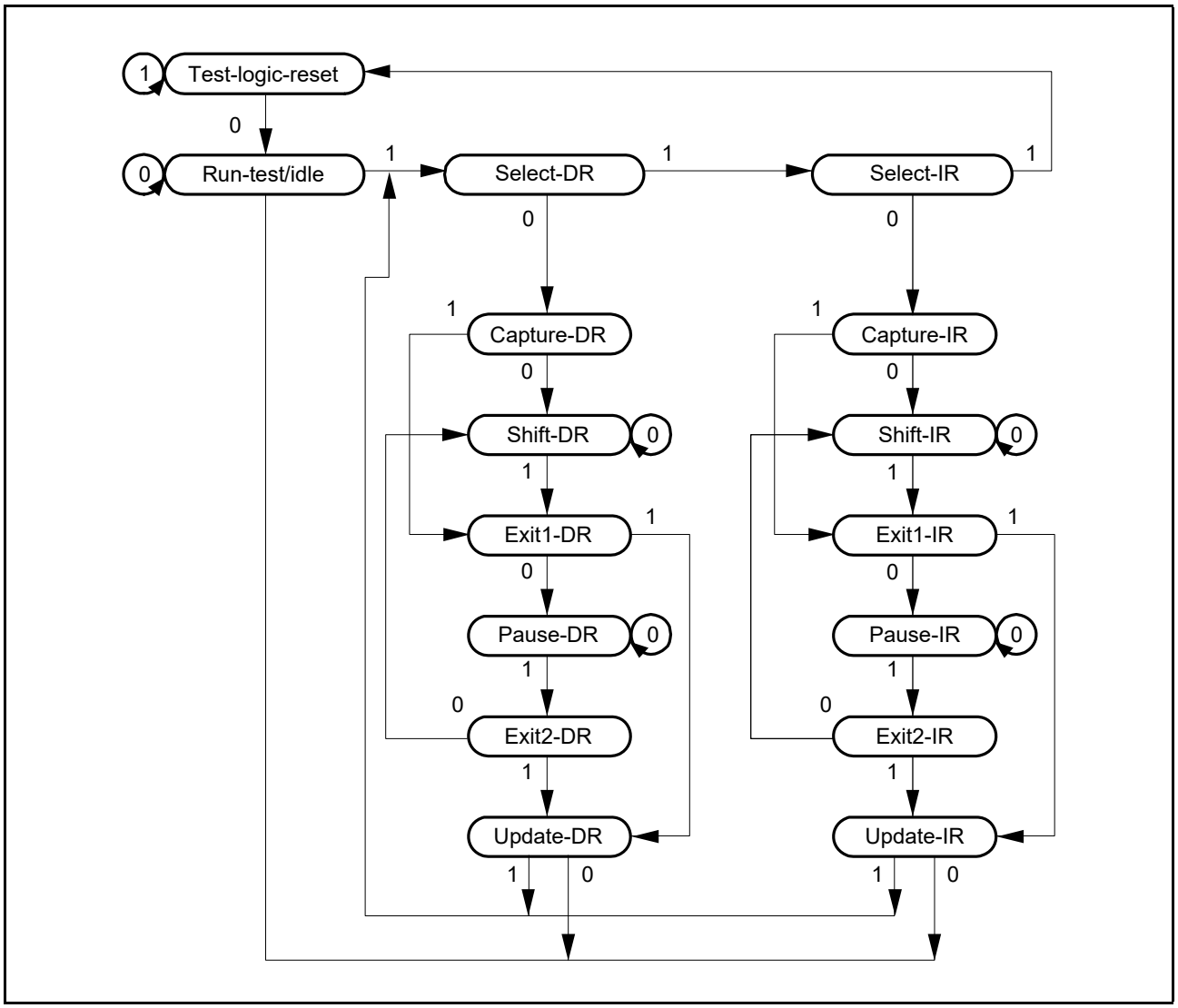


Figure 40.2 State Transition Diagram of TAP Controller

Table 40.7 Explanation of States

State	Explanation
Test Logic Reset	Reset state of the TAP controller. The LSI is in this state during normal operation.
Run Test/Idle	Test execution state
Select DR Scan	Temporary state used for selecting a data register.
Select IR Scan	Temporary state used for selecting an instruction register.
Capture DR	Data of the test data register corresponding to the current instruction is captured in parallel.
Shift DR	The test data register corresponding to the current instruction is connected between the TDI and TDO pins, and data is transferred serially.
Exit DR	Temporary state
Pause DR	Clocks are applied while the value input in the Shift DR state is retained.
Exit2 DR	Temporary state
Update DR	Output latches of the test data register corresponding to the current instruction are updated.
Capture IR	A fixed value is input to the instruction register.
Shift IR	The instruction register is connected between the TDI and TDO pins, and data is transferred serially.
Exit IR	Temporary state
Pause IR	Clocks are applied while the value input in the Shift IR state is retained.
Exit2 IR	Temporary state
Update IR	The current instruction is updated to the instruction input in the Shift IR state.

40.3.2 List of Commands

(1) BYPASS [Instruction Code: 1111 1111b]

The BYPASS instruction drives the bypass register. This instruction shortens the shift path, facilitating the transfer of serial data to other LSIs on a printed-circuit board at higher speeds. While this instruction is being executed, the test circuit does not affect the system circuit.
The bypass register is connected between the TDI and TDO pins. Bypass operation is initiated from shift-DR operation. The TDO is set to 0 in the first clock cycle in the Shift-DR state. In the subsequent clock cycles, the TDI signal is output on the TDO pin.

(2) EXTEST [Instruction Code: 0000 0000b]

The EXTEST instruction is used to test external circuits when this LSI is installed on the printed circuit board. If this instruction is executed, output pins are used to output test data (specified by the SAMPLE/PRELOAD instruction) from the boundary scan register to the print circuit board, and input pins are used to input test result to the boundary scan register from the print circuit board.

(3) SAMPLE/PRELOAD [Instruction Code: 0100 0000b]

The SAMPLE/PRELOAD instruction is used to input data from this LSI's internal circuits to the boundary scan register, output data from the scan path, and reload the data to the scan path. While this instruction is executed, input signals are directly input to this LSI and output signals are also directly output to the external circuits. The system circuit of this LSI is not affected by this instruction.
In SAMPLE operation, the boundary scan register latches the snap shot of data transferred from input pins to internal circuit or data transferred from internal circuit to output pins. The latched data is read from the scan path. The scan register latches the snap shot at the rising edge of the TCK in Capture-DR state. The scan register latches snap shots without affecting the LSI normal operation.
In PRELOAD operation, the value after reset is written from the scan path to the parallel output latch of the boundary scan register prior to the EXTEST instruction execution. If the EXTEST instruction is executed without executing this PRELOAD operation, undefined values are output over the period until the first scan sequence is completed (transfer to the output latch). (In the EXTEST instruction, output parallel latches are always output to the output pins.)

(4) IDCODE [Instruction Code: 0101 0101b]

When the IDCODE instruction is selected, the ID code register value is output from the TDO in LSB-first order in Shift-DR state of the TAP controller. While this instruction is being executed, the test circuit does not affect the system circuit. The instruction register is initialized by the IDCODE instruction in Test-Logic-Reset state of the TAP controller.

(5) CLAMP [Instruction Code: 1101 0000b]

When the CLAMP instruction is selected, output pins output the boundary scan register value which was specified by the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of the boundary scan register is maintained regardless of the TAP controller state.
The bypass register is connected between the TDI and TDO pins, leading to the same operation as when BYPASS mode has been selected

(6) HIGHZ [Instruction Code: 1000 0000b]

When the HIGHZ instruction is selected, all output pins enter high-impedance state. While the HIGHZ instruction is selected, the status of the boundary scan register is maintained regardless of the TAP controller state. The bypass register is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction has been selected.

40.4 Usage Notes

1. For serial transfer, data are input or output in LSB-first order. See Figure 40.3.

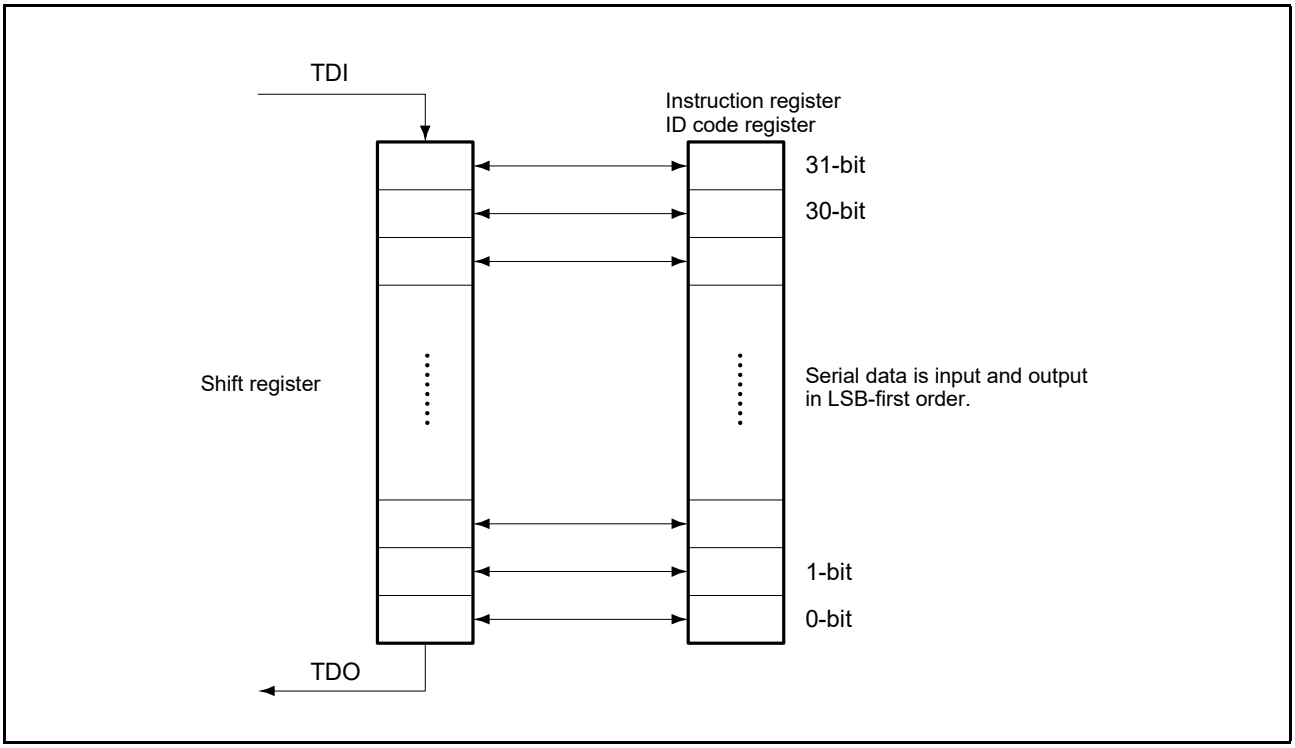


Figure 40.3 Serial Data Input/Output

2. Pins of the boundary scan (TDI, TMS, and TRST#) have to be pulled up by pull-up resistors. However, if an on-chip emulator is in use, handle the #TRST pin according to the manual for the given on-chip emulator.
3. Power supply pins (VDD, VSS, VCCQ33, PLLVDD0, PLLVSS0, PLLVDD1, PLLVSS1, VDD33_USB, VSS_USB, DVDD_USB, AVCC0, AVSS0, AVCC1, and AVSS1) cannot be boundary-scanned.
4. Analog reference pins (VREFH0, VREFL0, VREFH1, VREFL1, and USB_RREF) cannot be boundary-scanned.
5. Clock pins (EXTAL and XTAL) cannot be boundary-scanned.
6. The clock input mode select pin (OSCTH) cannot be boundary-scanned.
7. The reset pin (RES#) cannot be boundary-scanned.
8. The operating mode select input pins (MD0 to MD2) cannot be boundary-scanned.
9. USB dedicated pins (USB_DP and USB_DM) cannot be boundary-scanned.
10. The boundary-scan pin (BSCANP) cannot be boundary-scanned.
11. The boundary-scan pins (TCK, TMS, TRST#, TDI, and TDO) cannot be boundary-scanned.
12. Output registers of the I/O port C pins (PC0 to PC7) and pin P30 cannot be boundary-scanned.
13. The boundary scan function is not available when the chip is in the reset state.
14. For a pin that incorporates open-drain functionality and for which the open-drain function is enabled, if the boundary-scan function sets the corresponding bit in the output scan register and output enable register to 1, executing an EXTEST, CLAMP, or SAMPLE/PRELOAD instruction makes the pin output the high level rather than placing it in the high-impedance state.
15. Be sure to satisfy the standards for the boundary scan function when multiplex I/O is used. Figure 40.4, AD Pin Configuration shows the configuration of the multiplex I/O (P90 to P97, PD0 to PD7, and P86 and P87) in combination with the AD input. When the boundary scan function is used with the pins to be used as AD input pins, the conflict with the AD input or sneak current might be generated.
16. Analog input pins (AN000, AN001, AN002, AN003, AN004, AN005, AN006, and AN007) cannot be boundary-scanned.

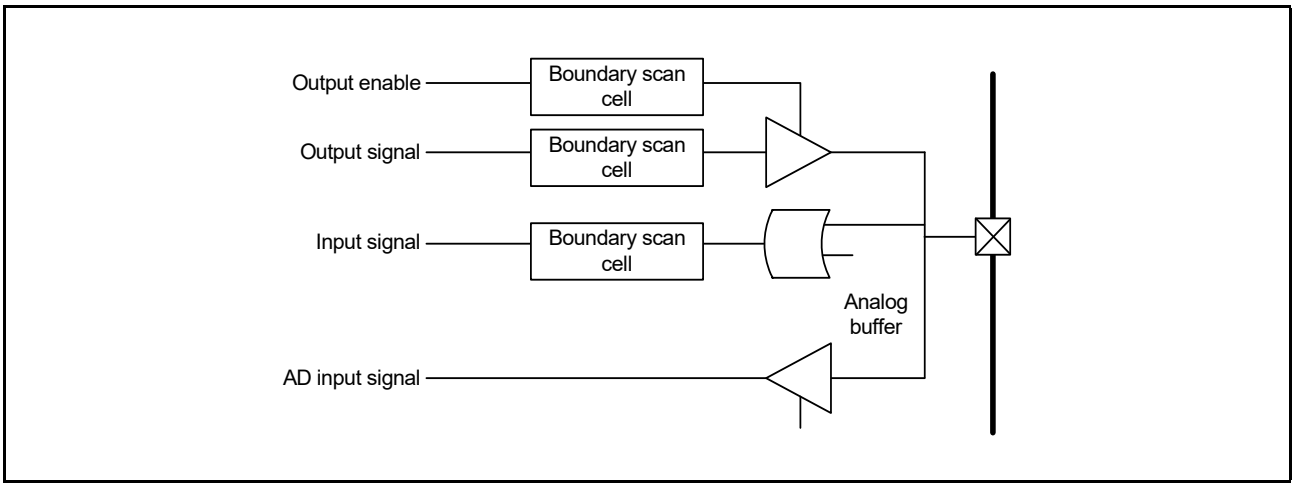


Figure 40.4 AD Pin Configuration

41. ΔΣ Interface (DSMIF)

This LSI has a total of four ΔΣ interfaces (DSMIFs), consisting of three interfaces (U, V, and W) in unit 0 and one interface (X) in unit 1. The DSMIF can be connected with up to four external ΔΣ modulators. It is capable of filtering delta-sigma modulated 1-bit digital input data and converting it into 16-bit digital data.

41.1 Overview

Table 41.1 lists the specifications of the DSMIF. Figure 41.1 is a block diagram of the DSMIF.

Table 41.1 DSMIF Specifications

Item	Description
Number of channels	Unit 0: channel 0 (U), channel 1 (V), and channel 2 (W) Unit 1: channel 3 (X)
Functions	• Capable of filtering 1-bit digital input data MDATAm (m = 0 to 2, 3) and converting them into 16-bit digital values. • The SINC filters are selectable as one-, two-, or three-stage. • MCLKm (m = 0 to 2, 3) can be output at up to 25 MHz in master operation (DSCLK0, DSCLK1) and input at up to 25 MHz in slave operation. • Crests and troughs can trigger capture, allowing capture of values for current with the same timing (only for channels 0 to 2 or channel 3).
Error source output	Error signals for the following reasons are output to the error control module (ECM). • Abnormal overcurrent detection (in units 0 and 1) • Short-circuit detection (in units 0 and 1) • Abnormal total current detection (in unit 0)
Low-power consumption function	The module-stop state can be set.

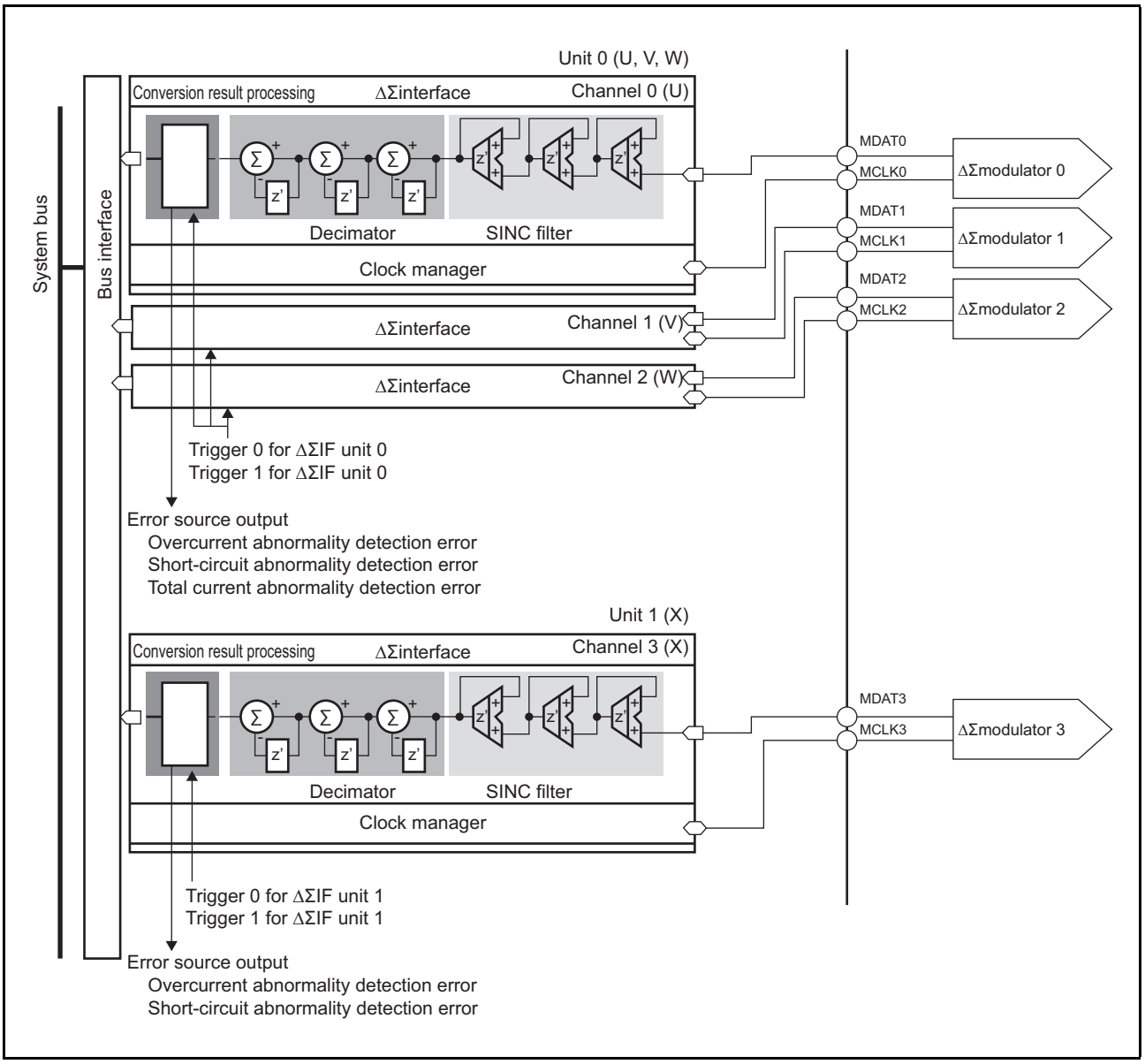


Figure 41.1 DSMIF Block Diagram

Table 41.2 lists the input/output pins of the DSMIF.

Table 41.2 Pin Configuration of DSMIF

Channel	Pin Name	I/O	Description
DSMIF0 (U)	MCLK0	I/O	Clock input/output pin
	MDAT0	Input	Data input pin
DSMIF1 (V)	MCLK1	I/O	Clock input/output pin
	MDAT1	Input	Data input pin
DSMIF2 (W)	MCLK2	I/O	Clock input/output pin
	MDAT2	Input	Data input pin
DSMIF3 (X)	MCLK3	I/O	Clock input/output pin
	MDAT3	Input	Data input pin

41.2 Register Descriptions

41.2.1 UVW Control Register (UVWCTL)

The UVWCTL register controls the settings for unit 0 (U, V, and W) of the DSMIF.
Writing to bits 1 to 31 during operations (i.e., while the UVWCTL.ENABLE bit = 1) is prohibited.

Address(es): DSMIF.UVWCTL A007 2000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BITSHIFT2[3:0]				—	WORD2GEN[2:0]			—	—	SINC2SEL[1:0]		BITSHIFT1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	WORD1GEN[2:0]			—	—	SINC1SEL[1:0]		—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ENABLE	Operation Enable	This bit enables operation of ΔΣ interfaces (unit 0, i.e. U, V, and W). 0: Filtering is stopped. 1: Filtering is started.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SINC1SEL [1:0]	Current Value Storage SINC Filter Select	These bits set the filters for the U1DATA, V1DATA, and W1DATA registers*1. 00: sinc3 (3-stage filter) 01: sinc1 (1-stage filter) 10: sinc2 (2-stage filter) Settings other than above are prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14 to b12	WORD1GEN [2:0]	Current Value Storage Decimation Clock Select	These bits set the decimation clock for the U1DATA, V1DATA, and W1DATA registers*1. 000: MCLKm/4 (m = 0 to 2) 010: MCLKm/8 (m = 0 to 2) 011: MCLKm/16 (m = 0 to 2) 100: MCLKm/32 (m = 0 to 2) 101: MCLKm/64 (m = 0 to 2) 110: MCLKm/128 (m = 0 to 2) 111: MCLKm/256 (m = 0 to 2) Settings other than above are prohibited.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b19 to b16	BITSHIFT1 [3:0]	Current Value Storage Bit Shift Select	These bits set the bit shift for the U1DATA, V1DATA, and W1DATA registers (i.e., these bits select the 16 bits to be used from the 24-bit results of decimation)*1. 0000: [23:8] 0001: [20:5] 0010: [17:2] 0011: [15:0] 0100: [14:0], 1'b0 0101: [13:0], 2'b00 0110: [11:0], 4'b0000 0111: [9:0], 6'b00_0000 1000: [8:0], 7'b000_0000 1001: [7:0], 8'b0000_0000 1010: [6:0], 9'b0_0000_0000 1011: [5:0], 10'b00_0000_0000 1100: [4:0], 11'b000_0000_0000 Settings other than above are prohibited. When BITSHIFT1[3:0] = 0100b to 1100b, the lower-order bits are padded with 0.	R/W
b21, b20	SINC2SEL [1:0]	Overcurrent Abnormality Detection SINC Filter Select	These bits set the filters for the U2DATA, V2DATA, and W2DATA registers*1. 00: sinc3 (3-stage filter) 01: sinc1 (1-stage filter) 10: sinc2 (2-stage filter) Settings other than above are prohibited.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	WORD2GEN [2:0]	Overcurrent Abnormality Detection Decimation Clock Select	These bits set the decimation clock for the U2DATA, V2DATA, and W2DATA registers*1. 000: MCLKm/4 (m = 0 to 2) 010: MCLKm/8 (m = 0 to 2) 011: MCLKm/16 (m = 0 to 2) 100: MCLKm/32 (m = 0 to 2) 101: MCLKm/64 (m = 0 to 2) 110: MCLKm/128 (m = 0 to 2) 111: MCLKm/256 (m = 0 to 2) Settings other than above are prohibited.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b28	BITSHIFT2 [3:0]	Overcurrent Abnormality Detection Bit Shift Select	These bits set the bit shift for the U2DATA, V2DATA, and W2DATA registers (i.e., these bits select the 16 bits to be used from the 24-bit results of decimation)*1. 0000: [23:8] 0001: [20:5] 0010: [17:2] 0011: [15:0] 0100: [14:0], 1'b0 0101: [13:0], 2'b00 0110: [11:0], 4'b0000 0111: [9:0], 6'b00_0000 1000: [8:0], 7'b000_0000 1001: [7:0], 8'b0000_0000 1010: [6:0], 9'b0_0000_0000 1011: [5:0], 10'b00_0000_0000 1100: [4:0], 11'b000_0000_0000 Settings other than above are prohibited. When BITSHIFT2[3:0] = 0100b to 1100b, the lower-order bits are padded with 0.	R/W

Note 1. For the relationship between the filter setting by the corresponding bits and values for current, see section 41.3.5, Settings for Filtering.

41.2.2 UVW Status Register (UVWSTA)

The UVWSTA register indicates the state of error detection in unit 0 (U, V, and W).

Address(es): DSMIF.UVWSTA A007 2004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERUVWIGND	—	ERWSC	ERVSC	ERUSC	—	ERWI	ERVI	ERUI
Value after reset:	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERUI	Channel 0 (U) Overcurrent Abnormality Detection Status	This bit indicates the detection of an overcurrent abnormality on channel 0 (U). 0: Overcurrent abnormality has not been found. 1: Overcurrent abnormality has been found. Setting condition: Overcurrent abnormality being detected from the values of data on current in the U2DATA register. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b1	ERVI	Channel 1 (V) Overcurrent Abnormality Detection Status	This bit indicates the detection of an overcurrent abnormality on channel 1 (V). 0: Overcurrent abnormality has not been found. 1: Overcurrent abnormality has been found. Setting condition: Overcurrent abnormality being detected from the values of data on current in the V2DATA register. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b2	ERWI	Channel 2 (W) Overcurrent Abnormality Detection Status	This bit indicates the detection of an overcurrent abnormality on channel 2 (W). 0: Overcurrent abnormality has not been found. 1: Overcurrent abnormality has been found. Setting condition: Overcurrent abnormality being detected from the values of data on current in the W2DATA register. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ERUSC	Channel 0 (U) Short-Circuit Abnormality Detection Status	This bit indicates the detection of a short-circuit abnormality on channel 0 (U). 0: Short-circuit abnormality has not been found. 1: Short-circuit abnormality has been found. Setting condition: Short-circuit abnormality being detected from 1-bit digital input data MDATA0. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b5	ERVSC	Channel 1 (V) Short-Circuit Abnormality Detection Status	This bit indicates the detection of a short-circuit abnormality on channel 1 (V). 0: Short-circuit abnormality has not been found. 1: Short-circuit abnormality has been found. Setting condition: Short-circuit abnormality being detected from 1-bit digital input data MDATA1. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W

Bit	Symbol	Bit Name	Description	R/W
b6	ERWSC	Channel 2 (W) Short-Circuit Abnormality Detection Status	This bit indicates the detection of a short-circuit abnormality on channel 2 (W). 0: Short-circuit abnormality has not been found. 1: Short-circuit abnormality has been found. Setting condition: Short-circuit abnormality being detected from 1-bit digital input data MDATA2. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	ERUVWIGND	Unit 0 (U, V, W) Total Current Abnormality Detection Status	This bit indicates the detection of total current abnormalities in unit 0 (U, V, and W). 0: Total current abnormality has not been found. 1: Total current abnormality has been found. Setting condition: Total current abnormality being detected from the sum of the data on current in the U1DATA, V1DATA, and W1DATA registers. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.3 UVW Overcurrent Abnormality Detection Lower Limit Setting Register (UVWIUNCMP)

The UVWIUNCMP register is used to set the lower limit for judging the detection of overcurrent abnormalities in unit 0 (U, V, or W).

If a value for current in the U2DATA, V2DATA, or W2DATA register falls below the value set in this register, the UVW overcurrent abnormality detection error signal is output.

Address(es): DSMIF.UVWIUNCMP A007 2008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPUVWIUNDER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPUVWIUNDER[15:0]	UVW Overcurrent Abnormality Detection Lower Limit Setting	When y2DATA < CMPUVWIUNDER[15:0], the corresponding UVWSTA.ERyI bit (y = U, V, or W) is set to 1. Also, the UVW overcurrent abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERyI bit.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.4 UVW Overcurrent Abnormality Detection Upper Limit Setting Register (UVWIOVCMP)

The UVWIOVCMP register is used to set the upper limit for judging the detection of overcurrent abnormalities in unit 0 (U, V, or W).

If a value for current in the U2DATA, V2DATA, or W2DATA register exceeds the value set in this register, the UVW overcurrent abnormality detection error signal is output.

Address(es): DSMIF.UVWIOVCMP A007 200Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPUVWIOVER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPUVWIOVER[15:0]	UVW Overcurrent Abnormality Detection Upper Limit Setting	When y2DATA > CMPUVWIOVER[15:0], the corresponding UVWSTA.ERyI bit (y = U, V, or W) is set to 1. Also, the UVW overcurrent abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERyI bit.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.5 UVW Short-Circuit Abnormality Detection 0 Data Input Threshold Setting Register (UVWSCUNCMP)

The UVWSCUNCMP register is used to set the threshold for the input of "0"-valued data for judging the detection of short-circuit abnormalities in unit 0 (U, V, or W).

The number of times 0 is consecutively input as 1-bit digital input data MDATAm (m = 0 to 2) is counted and the UVW short-circuit abnormality detection error signal is output if the number of times exceeds the value in this register.

Address(es): DSMIF.UVWSCUNCMP A007 2010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CMPUVWSCUNDER[12:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit NameBit Name	Description	R/W
b12 to b0	CMPUVWSCUNDER[12:0]	UVW Short-Circuit Abnormality Detection Lower Limit Setting	When the number of times 0 is consecutively input as MDATAm (m = 0 to 2) is greater than CMPUVWUNDER[12:0], the UVWSTA.ERySC bit (y = U, V, or W) is set to 1. Also, the UVW short-circuit abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERySC bit.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.6 UVW Short-Circuit Abnormality Detection 1 Data Input Threshold Setting Register (UVWSCOVCMP)

The UVWSCOVCMP register is used to set the threshold for the input of "1"-valued data for judging the detection of short-circuit abnormalities in unit 0 (U, V, or W).

The number of times 1 is consecutively input as 1-bit digital input data MDATAm (m = 0 to 2) is counted and the UVW short-circuit abnormality detection error signal is output if the number of times exceeds the value in this register.

Address(es): DSMIF.UVWSCOVCMP A007 2014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CMPUVWSCOVER[12:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	CMPUVWSCOVER[12:0]	UVW Short-Circuit Abnormality Detection Lower Limit Setting	When the number of times 0 is consecutively input as MDATAm (m = 0 to 2) is greater than CMPUVWSCOVER[12:0], the UVWSTA.ERySC bit (y = U, V, or W) is set to 1. Also, the UVW short-circuit abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERySC bit.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.7 UVW Total Current Abnormality Detection Lower Limit Setting Register (UVWIGUNCMP)

The UVWIGUNCMP register is used to set the lower limit for judging the detection of total current abnormalities in unit 0 (U, V, and W).

If the total of the values for current in channels 0 to 2 (U, V, or W) held in the U1DATA, V1DATA, and W1DATA registers falls below the value set in this register, the total current abnormality detection error signal is output.

Address(es): DSMIF.UVWIGUNCMP A007 2018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPUVWIGNDUNDER[17:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPUVWIGNDUNDER[17:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b17 to b0	CMPUVWIGNDUNDER[17:0]	UVW Total Current Abnormality Detection Lower Limit Setting	When U1DATA + V1DATA + W1DATA < CMPUVWIGNDUNDER[17:0], the UVWSTA.ERUVWIGND bit is set to 1. Also, the UVW total current abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERUVWIGND bit.	R/W
b31 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.8 UVW Total Current Abnormality Detection Upper Limit Setting Register (UVWIGOVCMP)

The UVWIGOVCMP register is used to set the upper limit for judging the detection of total current abnormalities in unit 0 (U, V, and W).
If the total of the values for current in channels 0 to 2 (U, V, and W) held in the U1DATA, V1DATA, and W1DATA registers exceeds the value set in this register, the total current abnormality detection error signal is output.

Address(es): DSMIF.UVWIGOVCMP A007 201Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPUVWIGNDOVER[17:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPUVWIGNDOVER[17:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b17 to b0	CMPUVWIGNDOVER[17:0]	UVW Total Current Abnormality Detection Upper Limit Setting	When U1DATA + V1DATA + W1DATA > CMPUVWIGNDOVER[17:0], the UVWSTA.ERUVWIGND bit is set to 1. Also, the UVW total current abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the UVWSTA.ERUVWIGND bit.	R/W
b31 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.9 Channel U Current Value Register 1 (U1DATA)

The U1DATA register indicates the value for current in channel 0 (U) of unit 0 (U, V, and W).
This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA0 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN, and UVWCTL.BITSHIFT1 bits.

Address(es): DSMIF.U1DATA A007 2020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	U1DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	U1DATA[15:0]	Channel 0 (U) Current Value 1	16-bit value for current obtained by filtering MDATA0 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN, and UVWCTL.BITSHIFT1 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.10 Channel U Current Value Crest Trigger Capture Register 1 (U1CDATA)

The U1CDATA register indicates the result of capturing the value held in the U1DATA register in response to trigger 0 for ΔΣ IF unit 0.

The value for current in the U1DATA register can be captured in response to a crest trigger by using the event link controller (ELC) to set the crest trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 0 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.U1CDATA A007 2024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	U1CDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	U1CDATA [15:0]	Channel 0 (U) Current Value Capture (Crest Trigger)	Value for current obtained by capturing U1DATA in response to trigger 0 for ΔΣ IF unit 0 (the crest trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.11 Channel U Current Value Trough Trigger Capture Register 1 (U1VDATA)

The U1VDATA register indicates the result of capturing the value held in the U1DATA register in response to trigger 1 for ΔΣ IF unit 0.

The value for current in the U1DATA register can be captured in response to a trough trigger by using the event link controller (ELC) to set the trough trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 1 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.U1VDATA A007 2028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	U1VDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	U1VDATA [15:0]	Channel 0 (U) Current Value Capture (Trough Trigger)	Value for current obtained by capturing U1DATA in response to trigger 1 for ΔΣ IF unit 0 (the trough trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.12 Channel U Current Value Register 2 (U2DATA)

The U2DATA register indicates the value for current in channel 0 (U) of unit 0 (U, V, and W).
This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA0 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN, and UVWCTL.BITSHIFT2 bits.
The value for current is used in the judgment of overcurrent abnormalities in accord with the settings in the UVWIUNCMP and UVWIOVCMP registers.

Address(es): DSMIF.U2DATA A007 202Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	U2DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	U2DATA [15:0]	Channel 0 (U) Current Value 2	16-bit value for current obtained by filtering MDATA0 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN and UVWCTL.BITSHIFT2 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.13 Channel V Current Value Register 1 (V1DATA)

The V1DATA register indicates the value for current in channel 1 (V) of unit 0 (U, V, and W).
The data is the result of filtering 1-bit digital input data MDATA1 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN, and UVWCTL.BITSHIFT1 bits.

Address(es): DSMIF.V1DATA A007 2030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	V1DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	V1DATA [15:0]	Channel 1 (V) Current Value 1	16-bit value for current obtained by filtering MDATA1 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN and UVWCTL.BITSHIFT1 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.14 Channel V Current Value Crest Trigger Capture Register 1 (V1CDATA)

The V1CDATA register indicates the result of capturing the value held in the V1DATA register in response to trigger 0 for ΔΣ IF unit 0.

The value for current in the V1DATA register can be captured in response to a crest trigger by using the event link controller (ELC) to set the crest trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 0 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.V1CDATA A007 2034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	V1CDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	V1CDATA [15:0]	Channel 1 (V) Current Value Capture (Crest Trigger)	Value for current obtained by capturing V1DATA in response to trigger 0 for ΔΣ IF unit 0 (the crest trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.15 Channel V Current Value Trough Trigger Capture Register 1 (V1VDATA)

The V1VDATA register indicates the result of capturing the value held in the V1DATA register in response to trigger 1 for ΔΣ IF unit 0.

The value for current in the V1DATA register can be captured in response to a trough trigger by using the event link controller (ELC) to set the trough trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 1 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.V1VDATA A007 2038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	V1VDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	V1VDATA [15:0]	Channel 1 (V) Current Value Capture (Trough Trigger)	Value for current obtained by capturing V1DATA in response to trigger 1 for ΔΣ IF unit 0 (the trough trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.16 Channel V Current Value Register 2 (V2DATA)

The V2DATA register indicates the value for current in channel 1 (V) of unit 0 (U, V, and W).
This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA1 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN, and UVWCTL.BITSHIFT2 bits.
The value for current is used in the judgment of overcurrent abnormalities in accord with the settings in the UVWIUNCMP and UVWIOVCMP registers.

Address(es): DSMIF.V2DATA A007 203Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	V2DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	V2DATA	Channel 1 (V) Current Value 2	16-bit value for current obtained by filtering MDATA1 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN and UVWCTL.BITSHIFT2 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.17 Channel W Current Value Register 1 (W1DATA)

The W1DATA register indicates the value for current in channel 2 (W) of unit 0 (U, V, and W).
This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA2 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN, and UVWCTL.BITSHIFT1 bits.

Address(es): DSMIF.W1DATA A007 2040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W1DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	W1DATA	Channel 2 (W) Current Value 1	16-bit value for current obtained by filtering MDATA2 according to the settings of the UVWCTL.SINC1SEL, UVWCTL.WORD1GEN and UVWCTL.BITSHIFT1 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.18 Channel W Current Value Crest Trigger Capture Register 1 (W1CDATA)

The W1CDATA register indicates the result of capturing the value held in the W1DATA register in response to trigger 0 for ΔΣ IF unit 0.

The value for current in the W1DATA register can be captured in response to a crest trigger by using the event link controller (ELC) to set the crest trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 0 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.W1CDATA A007 2044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W1CDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	W1CDATA	Channel 2 (W) Current Value Capture (Crest Trigger)	Value for current obtained by capturing W1DATA in response to trigger 0 for ΔΣ IF unit 0 (the crest trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.19 Channel W Current Value Trough Trigger Capture Register 1 (W1VDATA)

The W1VDATA register indicates the result of capturing the value held in the W1DATA register in response to trigger 1 for ΔΣ IF unit 0.

The value for current in the W1DATA register can be captured in response to a trough trigger by using the event link controller (ELC) to set the trough trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 1 for ΔΣ IF unit 0. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.W1VDATA A007 2048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W1VDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	W1VDATA	Channel 2 (W) Current Value Capture (Trough Trigger)	Value for current obtained by capturing W1DATA in response to trigger 1 for ΔΣ IF unit 0 (the trough trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.20 Channel W Current Value Register 2 (W2DATA)

The W2DATA register indicates the value for current in channel 2 (W) of unit 0 (U, V, and W).

This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA2 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN, and UVWCTL.BITSHIFT2 bits.

The value for current is used in the judgment of overcurrent abnormalities in accord with the settings in the UVWIUNCMP and UVWIOVCMP registers.

Address(es): DSMIF.W2DATA A007 204Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W2DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	W2DATA	Channel 2 (W) Current Value 2	16-bit value for current obtained by filtering MDATA2 according to the settings of the UVWCTL.SINC2SEL, UVWCTL.WORD2GEN and UVWCTL.BITSHIFT2 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.21 XYZ Control Register (XYZCTL)

The XYZCTL register controls the settings for unit 1 (X) of the DSMIF.
Writing to bits 1 to 31 during operations (i.e., while the XYZCTL.ENABLE bit = 1) is prohibited.

Address(es): DSMIF.XYZCTL A007 2080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BITSHIFT2[3:0]				—	WORD2GEN[2:0]			—	—	SINC2SEL[1:0]		BITSHIFT1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	WORD1GEN[2:0]			—	—	SINC1SEL[1:0]		—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ENABLE	Operation Enable	This bit enables operation of ΔΣ interfaces (unit 1 (X)). 0: Filtering is stopped. 1: Filtering is started.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SINC1SEL [1:0]	Current Value Storage SINC Filter Select	These bits set the filters for the X1DATA register*1. 00: sinc3 (3-stage filter) 01: sinc1 (1-stage filter) 10: sinc2 (2-stage filter) Settings other than above are prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14 to b12	WORD1GEN [2:0]	Current Value Storage Decimation Clock Select	These bits set the decimation clock for the X1DATA register*1. 000: MCLK3/4 010: MCLK3/8 011: MCLK3/16 100: MCLK3/32 101: MCLK3/64 110: MCLK3/128 111: MCLK3/256 Settings other than above are prohibited.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b19 to b16	BITSHIFT1 [3:0]	Current Value Storage Bit Shift Select	These bits set the bit shift for the X1DATA register (i.e., these bits select the 16 bits to be used from the 24-bit results of decimation)*1. 0000: [23:8] 0001: [20:5] 0010: [17:2] 0011: [15:0] 0100: [14:0], 1'b0 0101: [13:0], 2'b00 0110: [11:0], 4'b000 0111: [9:0], 6'b00_0000 1000: [8:0], 7'b000_0000 1001: [7:0], 8'b0000_0000 1010: [6:0], 9'b0_0000_0000 1011: [5:0], 10'b00_0000_0000 1100: [4:0], 11'b000_0000_0000 Settings other than above are prohibited. When BITSHIFT1[3:0] = 0100b to 1100b, the lower-order bits are padded with 0.	R/W

Bit	Symbol	Bit Name	Description	R/W
b21, b20	SINC2SEL [1:0]	Overcurrent Abnormality Detection SINC Filter Select	These bits set the filters for the X2DATA register*1. 00: sinc3 (3-stage filter) 01: sinc1 (1-stage filter) 10: sinc2 (2-stage filter) Settings other than above are prohibited.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	WORD2GEN [2:0]	Overcurrent Abnormality Detection Decimation Clock Select	These bits set the decimation clock for the X2DATA registers*1. 000: MCLK3/4 010: MCLK3/8 011: MCLK3/16 100: MCLK3/32 101: MCLK3/64 110: MCLK3/128 111: MCLK3/256 Settings other than above are prohibited.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b28	BITSHIFT2 [3:0]	Overcurrent Abnormality Detection Bit Shift Select	These bits set the bit shift for the X2DATA register (i.e., these bits select the 16 bits to be used from the 24-bit results of decimation)*1. 0000: [23:8] 0001: [20:5] 0010: [17:2] 0011: [15:0] 0100: [14:0], 1'b0 0101: [13:0], 2'b00 0110: [11:0], 4'b000 0111: [9:0], 6'b00_0000 1000: [8:0], 7'b000_0000 1001: [7:0], 8'b0000_0000 1010: [6:0], 9'b0_0000_0000 1011: [5:0], 10'b00_0000_0000 1100: [4:0], 11'b000_0000_0000 Settings other than above are prohibited. When BITSHIFT2[3:0] = 0100b to 1100b, the lower-order bits are padded with 0.	R/W

Note 1. For the relationship between the filter setting by the corresponding bits and values for current, see section 41.3.5, Settings for Filtering.

41.2.22 XYZ Status Register (XYZSTA)

The XYZSTA register indicates the state of error detection in unit 1 (X).

Address(es): DSMIF.XYZSTA A007 2084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERXI	—	—	—	ERXSC	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	ERXSC	Channel 3 (X) Short-Circuit Abnormality Detection Status	This bit indicates the detection of a short-circuit abnormality on channel 3 (X). 0: Short-circuit abnormality has not been found. 1: Short-circuit abnormality has been found. Setting condition: Short-circuit abnormality being detected from MDATA3. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1. However, reading this bit after writing 1 to it returns 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	ERXI	Channel 3 (X) Overcurrent Abnormality Detection Status	This bit indicates the detection of an overcurrent abnormality on channel 3 (X). 0: Overcurrent abnormality has not been found. 1: Overcurrent abnormality has been found. Setting condition: Overcurrent abnormality being detected from the values of data on current in the X2DATA register. Clearing condition: Writing 1 to this bit after it has been set to 1.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.23 XYZ Overcurrent Abnormality Detection Lower Limit Setting Register (XYZIUNCMP)

The XYZIUNCMP register is used to set the lower limit for judging the detection of overcurrent abnormalities in unit 1 (X).

If a value for current in the X2DATA register falls below the value set in this register, the X overcurrent abnormality detection error signal is output.

Address(es): DSMIF.XYZIUNCMP A007 2098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPXIUNDER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPXIUNDER[15:0]	X Overcurrent Abnormality Detection Lower Limit Setting	When X2DATA < CMPXIUNDER[15:0], the corresponding XYZSTA.ERXI bit is set to 1. Also, the X overcurrent abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the XYZSTA.ERXI bit.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.24 XYZ Overcurrent Abnormality Detection Upper Limit Setting Register (XYZIOVCMP)

The XYZIOVCMP register is used to set the upper limit for judging the detection of overcurrent abnormalities in unit 1 (X).

If a value for current in the X2DATA register exceeds the value set in this register, the X overcurrent abnormality detection error signal is output.

Address(es): DSMIF.XYZIOVCMP A007 209Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPXIOVER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPXIOVER [15:0]	X Overcurrent Abnormality Detection Upper Limit Setting	When X2DATA > CMPXIOVER[15:0], the corresponding XYZSTA.ERXI bit is set to 1. Also, the X overcurrent abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the XYZSTA.ERXI bit.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.25 XYZ Short-Circuit Abnormality Detection 0 Data Input Threshold Setting Register (XYZSCUNCMP)

The XYZSCUNCMP register is used to set the threshold for the input of “0”-valued data for judging the detection of short-circuit abnormalities in unit 1 (X).
The number of times 0 is consecutively input as 1-bit digital input data MDATA3 is counted and the X short-circuit abnormality detection error signal is output if the number of times exceeds the value in this register.

Address(es): DSMIF.XYZSCUNCMP A007 2090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CMPXSCUNDER[12:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	CMPXSCUNDER[12:0]	X Short-Circuit Abnormality Detection Lower Limit Setting	When the number of times 0 is consecutively input as MDATA3 is greater than CMPXSCUNDER[12:0], the XYZSTA.ERXSC bit is set to 1. Also, the X short-circuit abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the XYZSTA.ERXSC bit.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.26 XYZ Short-Circuit Abnormality Detection 1 Data Input Threshold Setting Register (XYZSCOVCMP)

The XYZSCOVCMP register is used to set the threshold for the input of “1”-valued data for judging the detection of short-circuit abnormalities in unit 1 (X).
The number of times 1 is consecutively input as 1-bit digital input data MDATA3 is counted and the X short-circuit abnormality detection error signal is output if the number of times exceeds the value in this register.

Address(es): DSMIF.XYZSCOVCMP A007 2094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CMPXSCOVER[12:0]												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	CMPXSCOVER[12:0]	X Short-Circuit Abnormality Detection Lower Limit Setting	When the number of times 1 is consecutively input as MDATA3 is greater than CMPXSCOVER[12:0], the XYZSTA.ERXSC bit is set to 1. Also, the X short-circuit abnormality detection error signal is output to the error control module (ECM) regardless of the setting of the XYZSTA.ERXSC bit.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

41.2.27 Channel X Current Value Register 1 (X1DATA)

The X1DATA register indicates the value for current in channel 3 (X) of unit 1 (X).
This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA3 according to the settings of the XYZCTL.SINC1SEL, XYZCTL.WORD1GEN, and XYZCTL.BITSHIFT1 bits.

Address(es): DSMIF.X1DATA A007 20A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	X1DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	X1DATA [15:0]	Channel 3 (X) Current Value 1	16-bit value for current obtained by filtering MDATA3 according to the settings of the XYZCTL.SINC1SEL, XYZCTL.WORD1GEN, and XYZCTL.BITSHIFT1 bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.28 Channel X Current Value Crest Trigger Capture Register 1 (X1CDATA)

The X1CDATA register indicates the result of capturing the value held in the X1DATA register in response to trigger 0 for ΔΣ IF unit 1.

The value for current in the X1DATA register can be captured in response to a crest trigger by using the event link controller (ELC) to set the crest trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 0 for ΔΣ IF unit 1. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.X1CDATA A007 20A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	X1CDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	X1CDATA [15:0]	Channel 3 (X) Current Value Capture (Crest Trigger)	Value for current obtained by capturing X1DATA in response to trigger 0 for ΔΣ IF unit 1 (the crest trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.29 Channel X Current Value Trough Trigger Capture Register 1 (X1VDATA)

The X1VDATA register indicates the result of capturing the value held in the X1DATA register in response to trigger 1 for ΔΣ IF unit 1.

The value for current in the X1DATA register can be captured in response to a trough trigger by using the event link controller (ELC) to set the trough trigger of the timers set to PWM mode (MTU3a, GPTa) as trigger 1 for ΔΣ IF unit 1. For details, see section 41.3.3.1, Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers.

Address(es): DSMIF.X1VDATA A007 20A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	X1VDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	X1VDATA [15:0]	Channel 3 (X) Current Value Capture (Trough Trigger)	Value for current obtained by capturing X1DATA in response to trigger 1 for ΔΣ IF unit 1 (the trough trigger from a PWM timer)	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.2.30 Channel X Current Value Register 2 (X2DATA)

The X2DATA register indicates the value for current in channel 3 (X) of unit 1 (X).

This register holds the 16-bit digital values produced by filtering 1-bit digital input data MDATA3 according to the settings of the XYZCTL.SINC2SEL, XYZCTL.WORD2GEN, and XYZCTL.BITSHIFT2 bits.

The value for current is used in the judgment of overcurrent abnormalities in accord with the settings in the XYZIUNCMP and XYZIOVCMP registers.

Address(es): DSMIF.X2DATA A007 20ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	X2DATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	X2DATA [15:0]	Channel 3 (X) Current Value 2	16-bit value for current obtained by filtering MDATA3 according to the settings of the UVWCTL.SINC2SEL and UVWCTL.WORD2GEN bits	R
b31 to b16	—	Reserved	These bits are read as 0.	R

41.3 Operation

The DSMIF consists of the SINC filter, decimator, and conversion result processing stages.
These stages filter 1-bit digital input data MDATAm (m = 0 to 2, 3) input to the DSMIF to produce 16-bit values for current per channel, and are also used in the detection of errors in the form of overcurrents, short-circuits, and abnormal total currents.
The decimator stage has two types of circuit: one for storage of values for current and one for detection of overcurrent abnormalities.
The conversion result processing stage handles the following four functions: conversion of values for current, capturing values in response to crest or trough triggers, overcurrent abnormality detection, short-circuit abnormality detection, and total current abnormality detection (only for channels 0 to 2).

41.3.1 SINC Filtering

Each DSMIF has three 24-bit adder stages to make up the SINC filter.
Filtering of 1-bit digital input data MDATAm for each channel m (m = 0 to 2 or 3) through the SINC filters is synchronized by the MCLKm clock.
Figure 41.2 shows the configuration of a SINC filter.

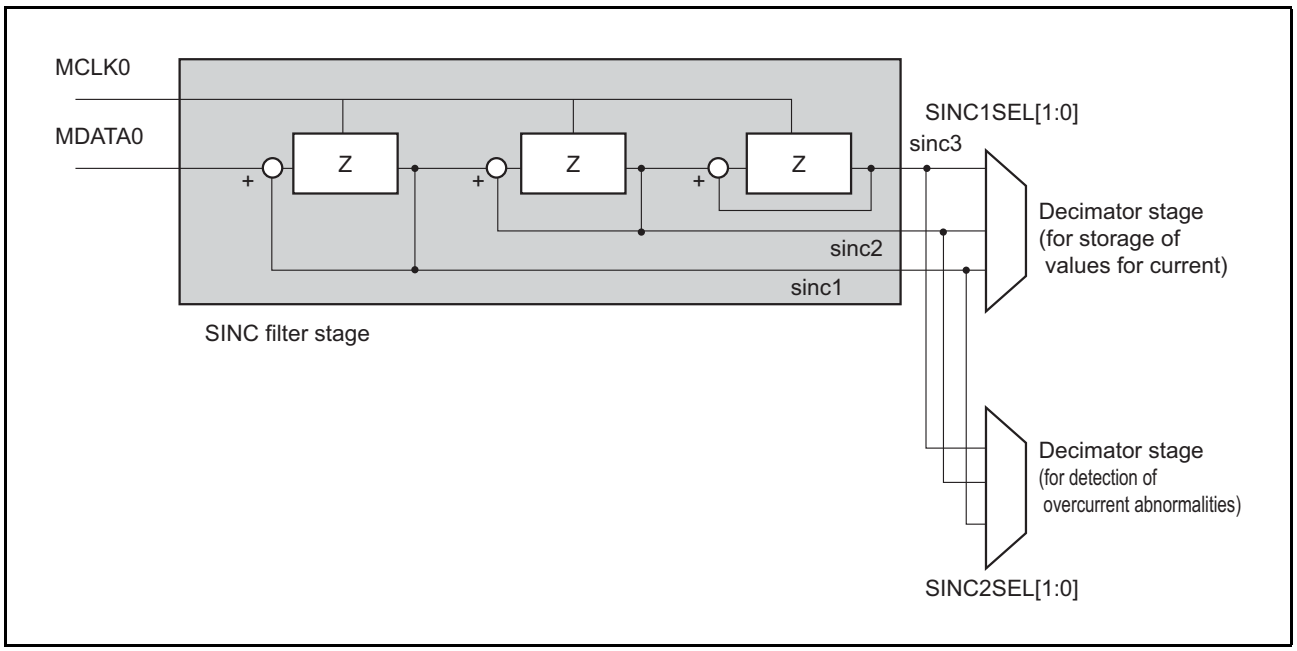


Figure 41.2 Configuration of a SINC Filter (Example of Channel 0 (U))

The orders of the filters (sinc3, sinc2, or sinc1) for storage of values for current and for the detection of abnormal overcurrents can be selected with the SINC1SEL[1:0] bits and the SINC2SEL[1:0] bits in the UVWCTL register (for unit 0) and XYZCTL register (for unit 1), respectively. Table 41.3 lists the SINC filter order settings.

Table 41.3 SINC Filter Order Settings

SINC1SEL[1:0] or SINC2SEL[1:0] Settings	SINC Filter Order
00b	3 (sinc3)
01b	1 (sinc1)
10b	2 (sinc2)

41.3.2 Decimation

Each DSMIF has three 24-bit divider stages which handle decimation.
The SINC filter output on each channel m (m = 0 to 2 or 3) is filtered by the decimation clock divided by a value from 4 to 256.
Figure 41.3 shows the configuration of the decimator.

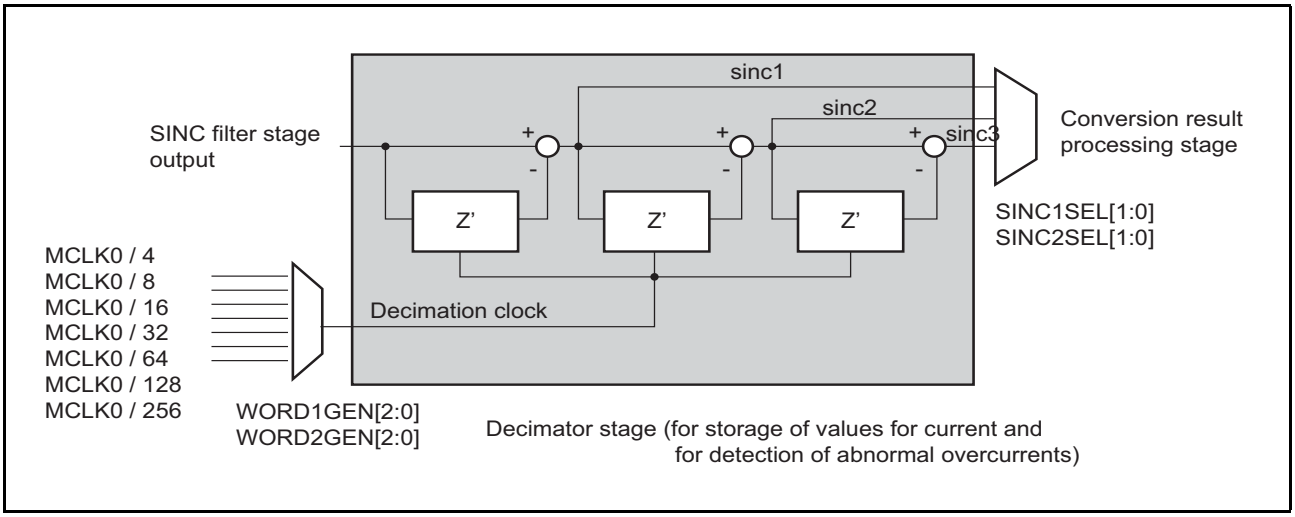


Figure 41.3 Configuration of the Decimator (Example of Channel 0 (U))

The division ratio of the decimation clocks for detection of abnormal overcurrents and for the storage of values for current are selected with the WORD1GEN[2:0] and WORD2GEN[2:0] bits in the UVWCTL register (for unit 0) and XYZCTL register (for unit 1), respectively.
Table 41.4 lists the decimation clock settings and resolutions.

Table 41.4 Decimation Clock Settings and Resolutions

WORD1GEN[2:0] or WORD2GEN[2:0] Settings	Division Ratio (m = 0 to 2, 3)	Resolution
000b	MCLKm/4	6 bits
010b	MCLKm/8	9 bits
011b	MCLKm/16	12 bits
100b	MCLKm/32	15 bits
101b	MCLKm/64	16 bits
110b	MCLKm/128	16 bits
111b	MCLKm/256	16 bits

Furthermore, the orders of the filters (sinc3, sinc2, or sinc1) for storage of values for current and for the detection of abnormal overcurrents can be selected with the SINC1SEL[1: 0] bits and the SINC2SEL[1:0] bits in the UVWCTL register (for unit 0) and XYZCTL register (for unit 1), respectively. For the SINC filter order settings, see Table 41.3, SINC Filter Order Settings.

41.3.3 Processing of Conversion Results

41.3.3.1 Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers

As facilities for current conversion, each DSMIF has current value registers 1 (U1DATA, V1DATA, W1DATA, and X1DATA) for storing the results of conversion on the corresponding channels, current value crest trigger capture registers (U1CDATA, V1CDATA, W1CDATA, and X1CDATA) and current value trough trigger capture registers (U1VDATA, V1VDATA, W1VDATA, and X1VDATA). The capture registers hold values for current captured in response to the crest and trough triggers from the PWM timer selected for input by using the event link controller (ELC). Figure 41.4 the configuration for the conversion of values for current.

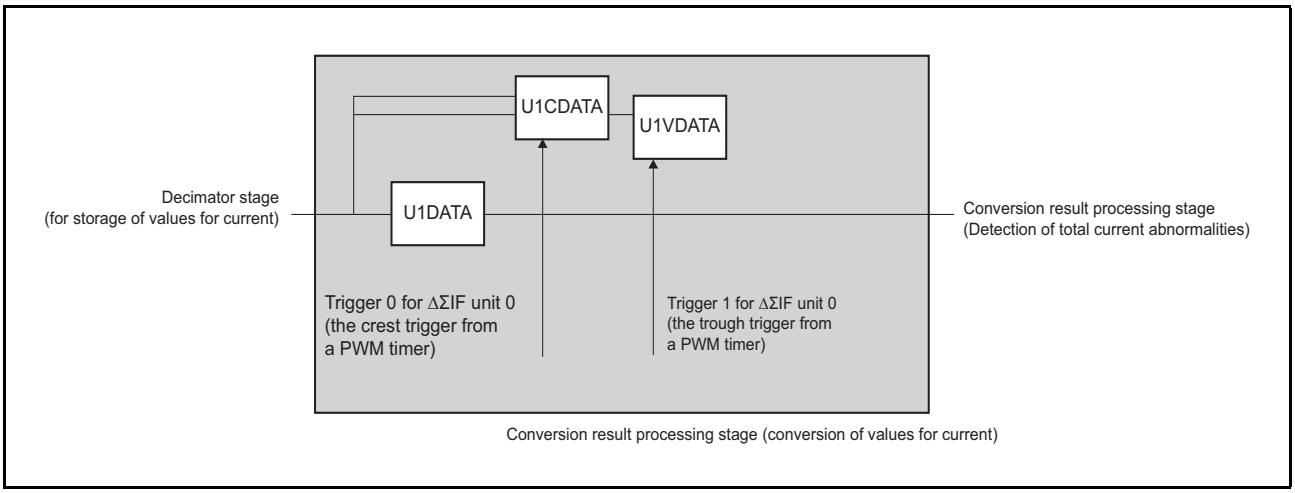


Figure 41.4 Configuration for the Conversion of Values for Current and Capture of Values in Response to Crest and Trough Triggers (Example of Channel 0 (U))

Also, as the results of conversion of values for current, 24-bit values for current from the decimator stage are filtered in accord with the bit shift setting of the BITSHIFT1[3:0] bits in the UVWCTL register (for unit 0) or the XYZCTL register (for unit 1) and stored as 16-bit values for current.

Table 41.5 Correspondence between BITSHIFT1[3:0] Settings and 16-Bit Values for Current

BITSHIFT1[3:0] Settings	16-Bit Values Selected from 24-Bit Values Output by the Decimator*1
0000b	[23:8]
0001b	[20:5]
0010b	[17:2]
0011b	[15:0]
0100b	[14:0], 0b
0101b	[13:0], 00b
0110b	[11:0], 0000b
0111b	[9:0], 00 0000b
1000b	[8:0], 000 0000b
1001b	[7:0], 0000 0000b
1010b	[6:0], 0 0000 0000b
1011b	[5:0], 00 0000 0000b
1100b	[4:0], 000 0000 0000b

Note 1. When BITSHIFT1[3:0] = 0100b to 1100b, the lower-order bits are padded with 0. For details, see Figure 41.8, Relationship between the Settings for Filtering and the Format of Values for Current.

Crest and trough trigger capturing allows capturing of values for current at the time of crest and trough triggers by setting the crest trigger (or trough trigger) from a timer (MTU3a, GPTa) set to PWM mode as trigger 0 for ΔΣ IF unit n (or trigger 1 for ΔΣ IF unit n) by using the event link controller (ELC).
Table 41.6 lists the crest and trough trigger settings. For details of the ELC, see section 16, Event Link Controller (ELC).

Table 41.6 Crest and Trough Trigger Settings

Unit	Crest and Trough Triggers
0 (U, V, W)	Crest trigger: trigger 0 for ΔΣ IF unit 0
	Trough trigger: trigger 1 for ΔΣ IF unit 0
1 (X)	Crest trigger: trigger 0 for ΔΣ IF unit 1
	Trough trigger: trigger 1 for ΔΣ IF unit 1

41.3.3.2 Detection of Overcurrent Abnormalities

For the detection of overcurrent abnormalities, 24-bit values for current from the decimator stage are filtered according to the bit shift setting of the BITSHIFT2[3:0] bits in the UVWCTL register (for unit 0) or the XYZCTL register (for unit 1), and the 16-bit values thus obtained are stored as the results of conversion of values for current.

Table 41.7 Correspondence between BITSHIFT2[3:0] Settings and 16-Bit Values for Current

BITSHIFT2[3:0] Settings	16-Bit Values Selected from 24-Bit Values Output by the Decimator*1
0000b	[23:8]
0001b	[20:5]
0010b	[17:2]
0011b	[15:0]
0100b	[14:0], 0b
0101b	[13:0], 00b
0110b	[11:0], 0000b
0111b	[9:0], 00 0000b
1000b	[8:0], 000 0000b
1001b	[7:0], 0000 0000b
1010b	[6:0], 0 0000 0000b
1011b	[5:0], 00 0000 0000b
1100b	[4:0], 000 0000 0000b

Note 1. When BITSHIFT1[3:0] = 0100b to 1100b, the lower-order bits are padded with 0. For details, see Figure 41.8, Relationship between the Settings for Filtering and the Format of Values for Current.

If a 16-bit value for current is not in the range defined by the upper and lower limits set by the UVWIUNCMP and UVWIOVCMP registers (for unit 0) and the XYZIUNCMP or XYZIOVCMP registers (for unit 1), the overcurrent abnormality detection error signal is generated. For details of the output of error sources, see section 41.4, Error Sources. Figure 41.5 shows the configuration for the detection of overcurrent abnormalities.

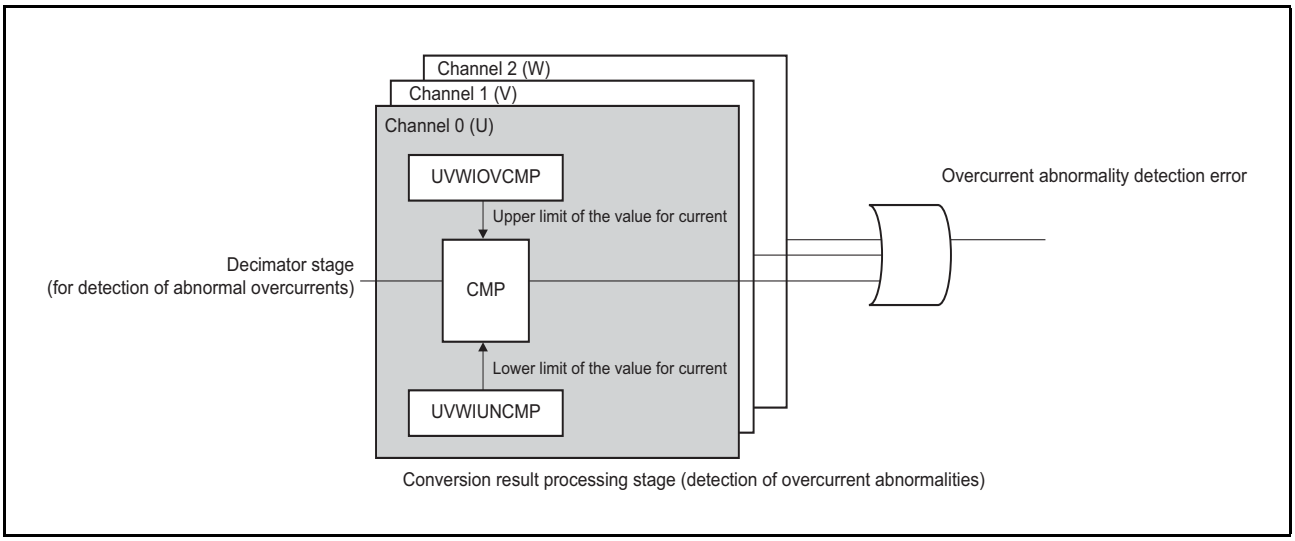


Figure 41.5 Detection of Overcurrent Abnormalities (Example of Unit 0 (U, V, and W))

41.3.3.3 Detection of Short-Circuit Abnormalities

For the detection of short-circuit abnormalities, a dedicated 13-bit counter counts the number of times 0 or 1 is consecutively input as 1-bit digital input data MDATAm (m = 0 to 2, 3). When the number of consecutive times exceeds the threshold for “0”- or “1”-valued data set in the UVWSCUNCMP and UVWSCOVCMP registers (for unit 0) or the XYZSCUNCMP and XYZSCOVCMP registers (for unit 1), the short-circuit abnormality detection error signal is generated. For details of the output of error sources, see section 41.4, Error Sources.
Figure 41.6 shows the configuration for the detection of short-circuit abnormalities.

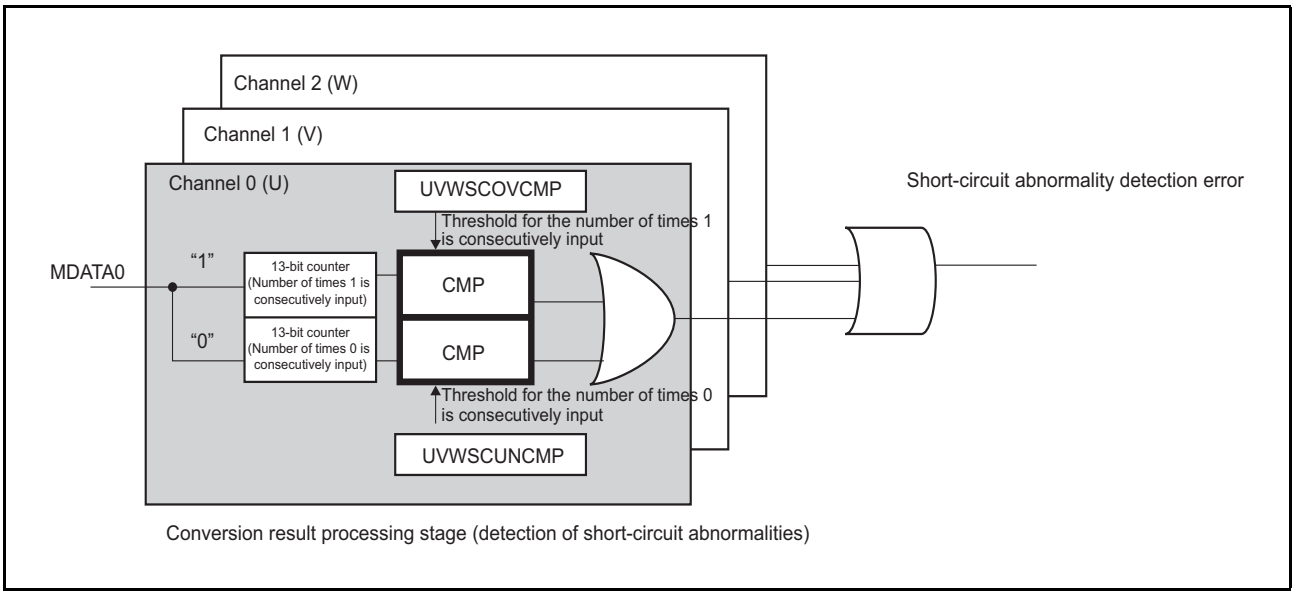


Figure 41.6 Detection of Short-Circuit Abnormalities (Example of Unit 0 (U, V, and W))

41.3.3.4 Detection of Total Current Abnormalities (only for unit 0 (U, W, and W))

In total current abnormality detection, a total current abnormality detection error signal is generated when the sum of the values for current after conversion on each channel of unit 0 is not in the range specified by the lower and upper limit settings in the UVWIGUNCMP and UVWIGOVCMP registers. For details of the output of error sources, see section 41.4, Error Sources.
Figure 41.7 shows the configuration for the detection of total current abnormalities.

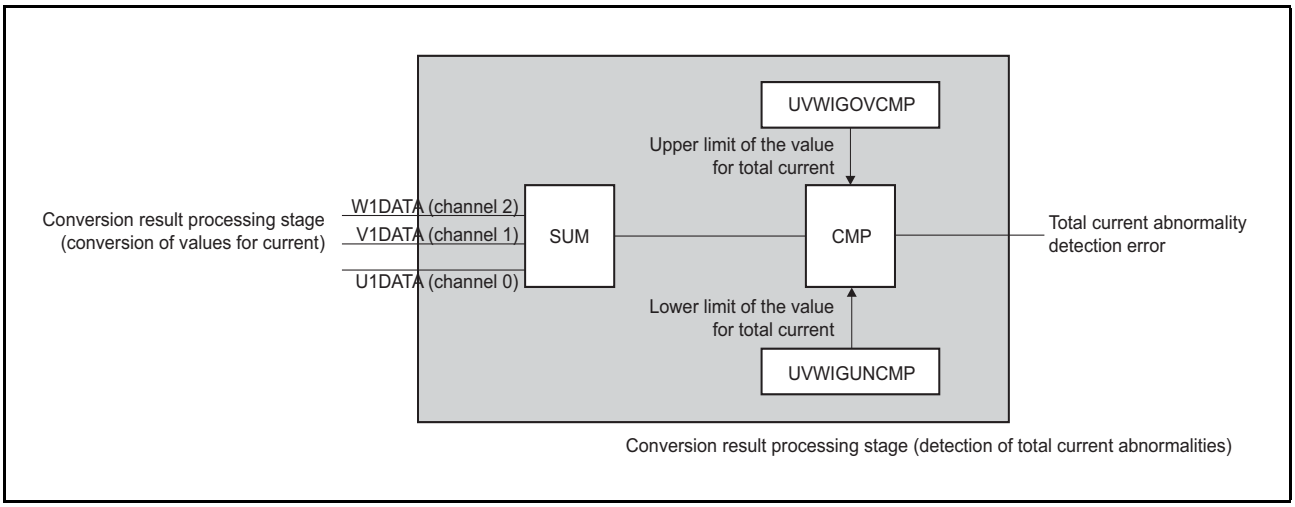


Figure 41.7 Detection of Total Current Abnormalities (Example of Unit 0 (U, V, and W)

41.3.4 Settings for Operating Clock Signals

In the DSMIF, the DSCR register is used to select whether the operating clock MCLKm (m = 0 to 2, 3) is to be supplied by a ΔΣ modulator external to the LSI (slave operation) or from the clock generator (master operation).
In master operation, the frequency of the DSCLKm clock is selectable as 6.25 MHz, 9.375 MHz, 12.5 MHz, 18.75 MHz, or 25 MHz. The active sense of the clock signal is selectable in both master and slave operation. For details of the DSCR register, see section 7, Clock Generation Circuit.

41.3.5 Settings for Filtering

Table 41.8 lists the settings for filtering by the individual registers and Figure 41.8 shows the relationship between the settings for filtering and the format of values for current.

Table 41.8 Settings for Filtering (The Only Allowed Combinations of the Register Values)

SINC Filter Order	WORD1GEN[2:0] or WORD2GEN[2:0] Settings	MSB	BITSHIFT1[3:0] or BITSHIFT2[3:0] Settings	Resolution
3 (sinc3)	010b	Bit 8	1000b	9 bits
	011b	Bit 11	0110b	12 bits
	100b	Bit 14	0100b	15 bits
	101b	Bit 17	0010b	16 bits
	110b	Bit 20	0001b	16 bits
	111b	Bit 23	0000b	16 bits
2 (sinc2)	011b	Bit 7	1001b	8 bits
	100b	Bit 9	0111b	10 bits
	101b	Bit 11	0110b	12 bits
	110b	Bit 13	0101b	14 bits
	111b	Bit 15	0011b	16 bits
1 (sinc1)	100b	Bit 4	1100b	5 bits
	101b	Bit 5	1011b	6 bits
	110b	Bit 6	1010b	7 bits
	111b	Bit 7	1001b	8 bits

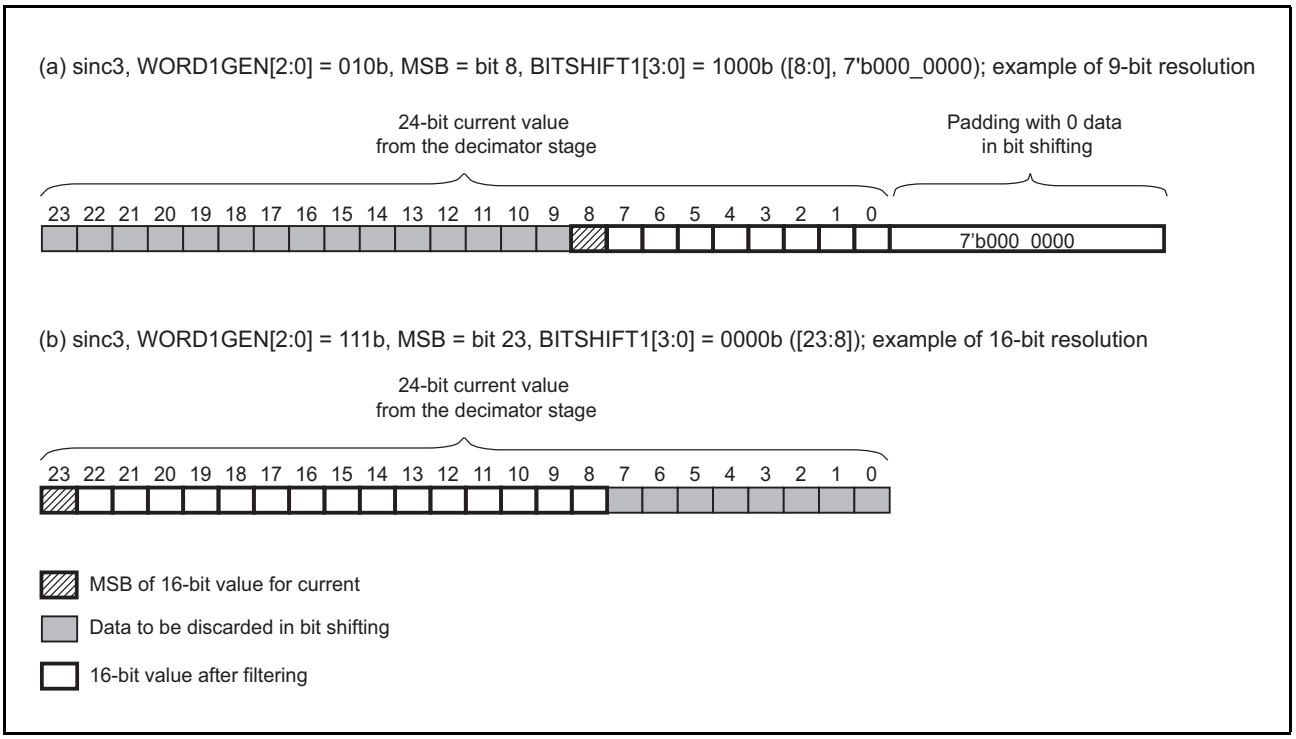
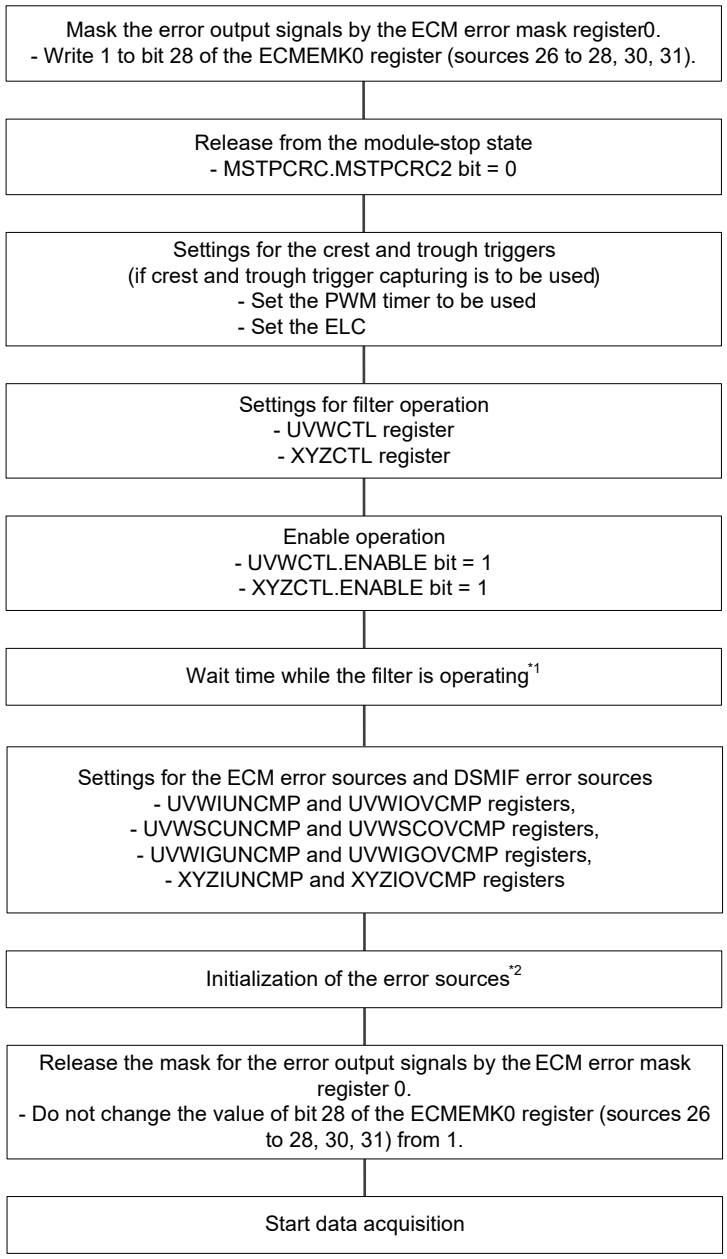


Figure 41.8 Relationship between the Settings for Filtering and the Format of Values for Current

41.3.6 Setting Examples

Figure 41.9 shows the setting procedure.



Note 1. The wait time while the filter is operating is obtained as follows:
[Period of MCLK] × [Number of SINC stages (1 to 3)] + [Period of decimation clock (max.)] × (6 + [Number of SINC stages (1 to 3)]) + [5 µs]
Use the period of decimation clock with its maximum allowable value.

Note 2. After release from the module-stop state, be sure to make initial settings for error sources in the error control module (ECM). For details, see section 41.5, Usage Notes.

Figure 41.9 Setting Example of the Error Control Module

41.3.7 Filtering

Figure 41.10 and Figure 41.11 show the timing for sampling in SINC3 filtering and decimation by the ΔΣ interfaces. Settings (1), (2), and (3) below can be made for filter clocks (MCLKn (n = 0 to 3) input to the ΔΣ interfaces by using the DSCR register. For the DSCR register, see section 7, Clock Generation Circuit.

(1) Select the source of the signal for input to MCLKn as being generated within (in master operation) or outside (in slave operation) the RZ/T1.
(2) If the clock is to be generated within the RZ/T1, select one of the five available frequencies.
(3) Select inversion or non-inversion for MCLKn.

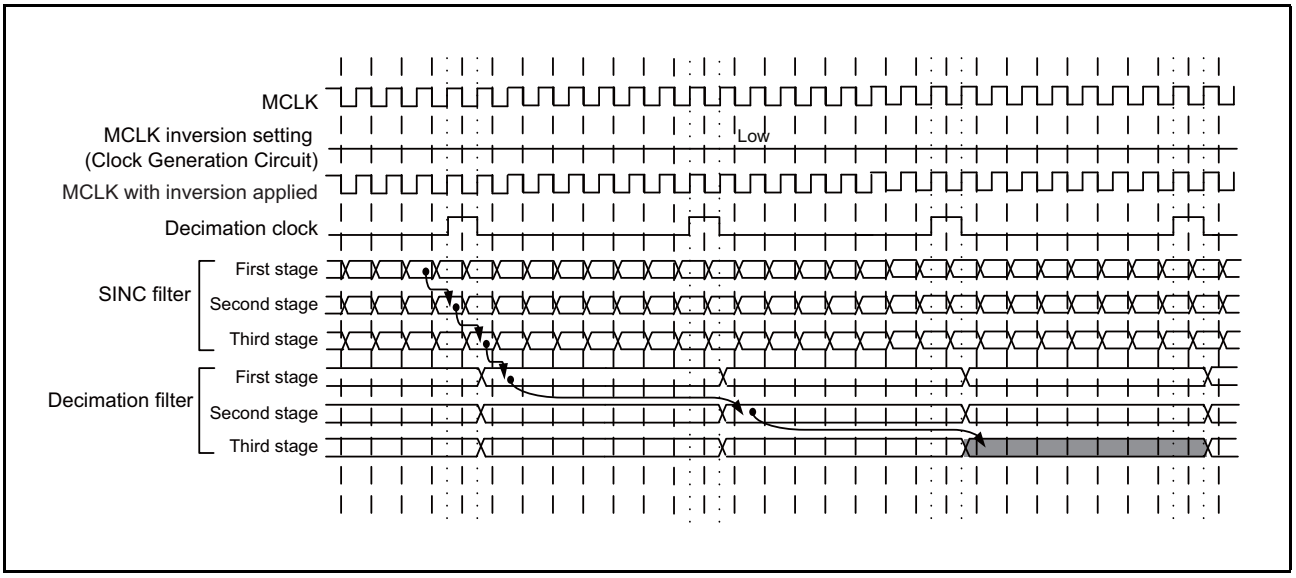


Figure 41.10 Operation when MCLKn is not Inverted

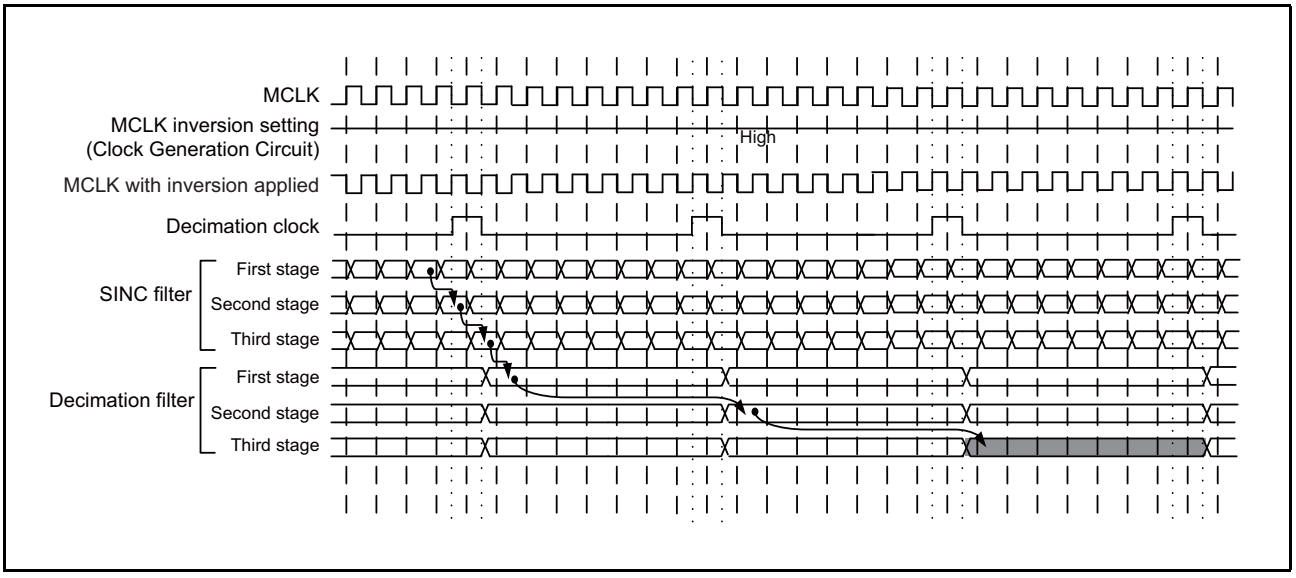


Figure 41.11 Operation when MCLKn is Inverted

41.4 Error Sources

The DSMIF can output the following three error signals to the error control module (ECM).

- Overcurrent abnormality detection error signal (in units 0 and 1)
- Short-circuit abnormality detection error signal (in units 0 and 1)
- Total current abnormality detection error signal (in unit 0)

For details of the error control module (ECM), see section 42, Error Control Module (ECM).

41.5 Usage Notes

41.5.1 Initial Settings for Error Sources after Release from the Module-Stop State

The DSMIF always outputs a short-circuit abnormality detection error signal after release from the module-stop state. Clear the error flag once before enabling error handling by the ECM.

(1) Mask the error output signals by the ECM error mask register 0 (sources 26 to 28, 30, 31). Do not change bit 28 from 1.
(2) Enable filter operation.
(3) Wait while the filter is operating.
(4) Clear the error status register of the DSMIF.*1
(5) Clear the error state of the ECM DSMIF error numbers (No. 26 to 28, 30 and 31) of the ECM error source status clear trigger register 0.
(6) Enable the ECM DSMIF error numbers (No. 26 to 28, 30 and 31).
(7) Release the mask for the error output signals by the ECM error mask register 0 (sources 26 to 28, 30, 31). Do not change bit 28 from 1.
(8) If a short-circuit abnormality detection error occurs, read the UVWSTA and XYZSTA registers to check if the error occurred in one of channels 0 to 3 (U, V, W, and X).*2

For details, see section 41.3.6, Setting Examples.

Note 1. Performing step (4) after step (5) does not create any problem.
Note 2. If the ECM is reset by an ECM error, the UVWSTA and XYZSTA registers are initialized, so read the flags retained in the corresponding error source status register of the ECM. However, if this is the case, you cannot judge in which of channels 0 to 2 (U, V, and W) of unit 0 the error occurred.

For details of the error control module (ECM), see section 42, Error Control Module (ECM).

41.5.2 Current Value on Detection of an Overcurrent

If a value for current increases and an overflow occurs on the related current value register, the read value of the current value register is not FFFFh but 0000h. For this reason, for the detection of overcurrent abnormalities, generate an error by using the overcurrent abnormality detection function and do not refer to the value of the current value register.

42. Error Control Module (ECM)

This section describes an error control module (ECM).

42.1 Overview

The error control module (ECM) collects error output signals coming from individual peripheral modules. It also outputs error signals from the error output pin (ERROROUT#) and generates error interrupts and internal reset signals. Table 42.1 describes the ECM specifications and Figure 42.1 shows the block diagram of ECM.

Table 42.1 Specifications of ECM

Item	Description
Safety processing	ECM can handle the following processing in response to error signal inputs from individual modules. • Error flag set ECM has flags that indicate the state of error occurrence for individual error sources. • ECM maskable interrupt generation Maskable interrupt generation can be controlled (enabled or disabled) for individual error sources. • ECM non-maskable interrupt generation Non-maskable interrupt generation can be controlled (enabled or disabled) for individual error sources. • ECM reset (Internal reset) Internal reset generation can be controlled (enabled or disabled) for individual error sources. • Error signal output from the ERROROUT# pin Error signal output and mask control (enable or disable) are possible for individual error sources. Output can be toggled in response to a CMTW timer input or made at a fixed level.
Error status	ECM incorporates error status registers, whose error flag values can be used to check whether the corresponding error sources have been generated.
Debug, self-diagnosis	• Pseudo errors can be generated for debug and self-diagnosis. The operation during injection of pseudo errors is identical to that for the occurrence of real errors. All configurations for the mask to the error pin output, interrupt, or internal reset apply in the same way. In addition, extended pseudo errors can be used for error detection for functional safely. • ECM incorporates a loop-back function of the error pin output that is used to diagnose the path to the error output pin. The status of the error output pin is reflected to an internal register and can be confirmed by reading the register.
Delay timer timeout	ECM has a function of outputting an error signal or resetting ECM when the delay timer starts at the same time with generation of an ECM maskable interrupt or an ECM non-maskable interrupt and a delay timer overflow occurs because the delay timer cannot be stopped during the interrupt processing.
Others	ECM has a duplexed structure (master and checker) for redundancy.

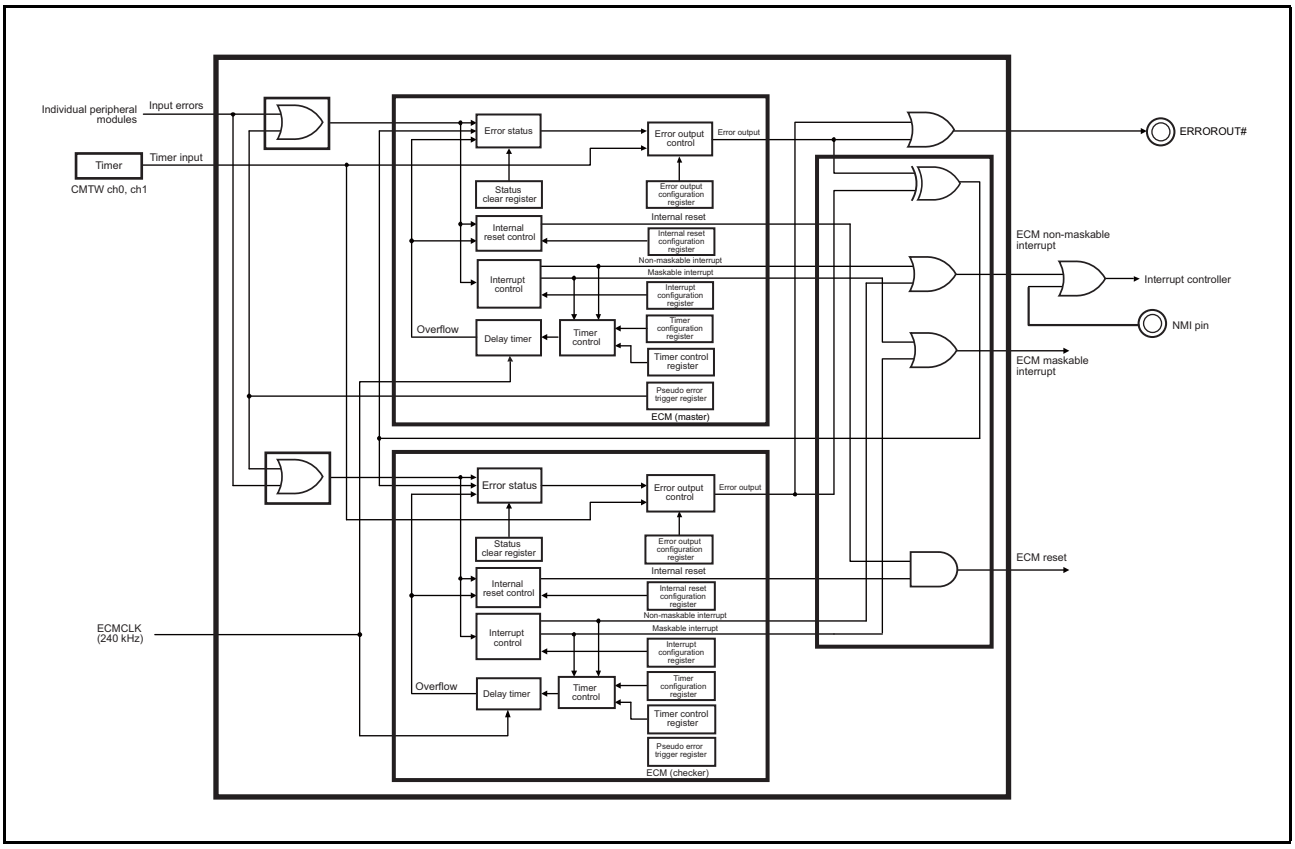


Figure 42.1 Block Diagram of ECM

Table 42.2 shows the error input to ECM.

Table 42.2 ECM Error Input (1 / 2)

Error Source Number	Module	Function
1	WDTA	WDTA underflow/refresh error (for Cortex-R4)
2	WDTA	WDTA underflow/refresh error (for Cortex-M3) (for products incorporating an R-IN engine)
3	IWDTa	IWDTa underflow/refresh error
4	—	Reserved
5	Cortex-R4 cache	1-bit or 2-bit ECC error in the instruction cache (Tag RAM)
6		1-bit or 2-bit ECC error in the instruction cache (Data RAM)
7		1-bit ECC error in the data cache (Tag/Dirty RAM)
8		2-bit ECC error in the data cache (Tag/Dirty RAM)
9		1-bit ECC error in the data cache (Data RAM)
10		2-bit ECC error in the data cache (Data RAM)
11	Cortex-R4 RAM	1-bit ECC error in the ATCM
12		2-bit ECC error in the ATCM
13		1-bit ECC error in the BTCM
14		2-bit ECC error in the BTCM
15	Extended internal SRAM	1-bit ECC error in the IRAM or DRAM
16		2-bit ECC error in the IRAM or DRAM
17	RSCAN	1-bit ECC error in the RSCAN RAM
18		2-bit ECC error in the RSCAN RAM
19		RSCAN overflow error
20	Clock monitor circuit (CLMA)	Main clock oscillation stop detection
21		CLMA0 oscillation stop detection (PLL0)
22		CLMA1 oscillation stop detection (PLL1)
23		CLMA2 oscillation stop detection (LOCO)
24	12-bit A/D converter (S12ADCa)	Unit 0 overwrite interrupt
25		Unit 1 overwrite interrupt
26	ΔΣ interface	UVW overcurrent abnormality detection error
27		UVW total current abnormality detection error
28		UVW short circuit abnormality detection error
29		Reserved
30		X overcurrent abnormality detection error
31		X short circuit abnormality detection error
32	Data operation circuit (DOC)	DOC operation error
33	Internal bus	Bus error
34	Bus state controller (BSC)	Detection of a timeout caused by the external WAIT pin
35	—	Extended pseudo error 35*1
36	—	Extended pseudo error 36*1
37	—	Extended pseudo error 37*1
38	—	Extended pseudo error 38*1
39	—	Extended pseudo error 39*1
40	—	Extended pseudo error 40*1
41	—	Extended pseudo error 41*1
42 to 92	—	Reserved

Table 42.2 ECM Error Input (2 / 2)

Error Source Number	Module	Function
93	Error control module (ECM)	Compare error
94		Delay timer overflow error
95		Error set by the ECMmESET register
96		Loopback error

Note 1. A pseudo error can be generated if the corresponding bit in the ECM pseudo error trigger register (ECMPEn) is set by software. For details, see section 42.3.3, Pseudo Error Generation.

42.2 Registers

42.2.1 ECM Master/Checker Error Set Trigger Register (ECMmESET (m = M or C))

The ECMmSET (m = M or C) register controls the output of the ERROROUT# pin. Setting the ECMmEST bit to 1 can set the output of the ERROROUT# pin to the active level (low level). The ERROROUT# pin output cannot be masked. Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers. This register is always read as 00h.

Address(es): ECMMESET: A007 D000h
ECMCESET: A007 D040h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMmEST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMmEST	Error Set Trigger	0: Writing 0 is invalid. 1: Sets the output level of the ERROROUT# pin to the active level (low level).	W
b7 to b1	—	Reserved	The write value should be 0.	W

Note 1. Setting the ECMmESET register will set the ECMmSSE228 bit of the ECMmESSTR2 register (ECM compare error). Therefore, to use the ECMmESET register to control the ERROROUT# pin, follow the procedure below.
1. Set the ECMEMK228 bit of the ECMEMK2 register to “masked”.
2. Prevent the generation of interrupts by setting the ECMMIE228 bit of the ECMMICFG2 register to “prohibited” and the ECMNMIE228 bit of the ECMNMICFG2 register to “prohibited”.
3. Prevent generation of an internal reset by setting the ECMIRE228 bit of the ECMIRCFG2 register to “prohibited”.
4. Set the error output bit in the ECMmESET register.
5. Clear error flags by setting the ECMCLSSE228 bit of the ECMESSTC2 register.
6. Make the following settings, as necessary, to change back the ECM compare error settings.
   - To enable the error output from the ERROROUT# pin, set the ECMEMK228 bit in the ECMEMK2 register to “not masked”.
   - To enable an error interrupt, set the ECMMIE228 bit in the ECMMICFG2 register or the ECMNMIE228 bit in the ECMNMICFG2 register to “enabled”.
   - To enable an ECM reset, set the ECMIRE228 bit in the ECMIRCFG2 register to “enabled”.

Note 2. When the error output is set by the ECMmESET register, an error state is retained even after all error sources that have not been masked in the ECMESSTCn register are cleared, and the low level is output from the ERROROUT# pin while the pin stays active. To clear an error state, perform clear processing on the ECMmECLR register.

42.2.2 ECM Master/Checker Error Clear Trigger Register (ECMmECLR (m = M or C))

The ECMmECLR (m = M or C) register controls the output from the ERROROUT# pin. When the ECMmECT bit is set to 1, the output of the ERROROUT# pin can be set to the inactive level (high level) if there is no other error sources that set the ERROROUT# pin to the active level (low level).
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers. This register is always read as 00h.

Address(es): ECMMECLR: A007 D004h
ECMCECLR: A007 D044h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMmECT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMmECT	Error Clear Trigger	0: Writing 0 has no effect. 1: Sets the output level of the ERROROUT# pin to the inactive level (high level). Note that, however, this bit cannot be used to clear an error while ECM error output clear is disabled. For details, see section 42.3.6, Setting of Disabling Error Output Clear.	W
b7 to b1	—	Reserved	The write value should be 0.	W

Note: Clearing the output of the error pin is only possible if all error sources, not masked by ECMEMK0, ECMEMK1, or ECMEMK2, are cleared beforehand. Setting the ECMmECT bit in this register will set the output of the ERROROUT# pin to the inactive level (high level).
If an error state is generated due to the error output set by ECMmESET, use this register to clear the error state.
Follow the procedure below to “clear” error states.

1. Set all bits corresponding to an error in the ECMESSTC0, ECMESSTC1, and ECMESSTC2 registers to clear the error state indicator.
2. To mask the output of error signals due to any error sources, set all bits corresponding to an error in the ECMEMK0, ECMEMK1, and ECMEMK2 registers to “masked”.
3. To prevent unintended processing in response to an ECM comparison error (error source 93), set the ECMMIE228, ECMNMIE228, and ECMIRE228 bits in the ECMMICFG2, ECMNMICFG2, and ECMIRCFG2 registers to “prohibited”.
4. Clear the output on the ERROROUT# pin by using the ECMMECT and ECMCECT bits in the ECMMECLR and ECMCECLR registers. At this time, an ECM comparison error will be generated.
5. Use software to set up the following interval of waiting until generation of the ECM compare error is reflected in the ECMESSTR2 register.
   (3 × ECMCLK) + (5 × PCLKD)
   In this product, the waiting time is about 12.6 µs because ECMCLK = 240 kHz and PCLKD = 75 MHz.
6. Use the ECMCLSSE228 bit in the ECMESSTC2 register to “clear” the ECM comparison error.
7. As required, restore the settings of the ECMEMK0, ECMEMK1, and ECMEMK2 registers which were changed in step 2 above.
8. As required, restore the settings of the ECMMICFG2, ECMNMICFG2, and ECMIRCFG2 registers which were changed in step 3 above.

42.2.3 ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0 (m = M or C))

The ECMmESSTR0 (m = M or C) register is a flag register that indicates whether individual error sources occurred. This register is cleared with the corresponding bits in the ECM error source status clear trigger register 0 (ECMESSTC0) set, or with the RES# pin reset. This register is not cleared by occurrence of other reset sources.

Address(es): ECMMESSTR0: A007 D008h
ECMCESSTR0: A007 D048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMm SSE031	ECMm SSE030	ECMm SSE029	—	ECMm SSE027	ECMm SSE026	ECMm SSE025	ECMm SSE024	ECMm SSE023	ECMm SSE022	ECMm SSE021	ECMm SSE020	ECMm SSE019	ECMm SSE018	ECMm SSE017	ECMm SSE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMm SSE015	ECMm SSE014	ECMm SSE013	ECMm SSE012	ECMm SSE011	ECMm SSE010	ECMm SSE009	ECMm SSE008	ECMm SSE007	ECMm SSE006	ECMm SSE005	ECMm SSE004	—	ECMm SSE002	ECMm SSE001	ECMm SSE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMmSSE000	Error Source Status 1	Indicates occurrence of a WDTA underflow/refresh error (for Cortex-R4) (error source 1). 0: Error not occurred 1: Error occurred	R
b1	ECMmSSE001	Error Source Status 2	Indicates occurrence of a WDTA underflow/refresh error (for Cortex-M3) (error source 2).*1 0: Error not occurred 1: Error occurred	R
b2	ECMmSSE002	Error Source Status 3	Indicates occurrence of an IWDTa underflow/refresh error (error source 3). 0: Error not occurred 1: Error occurred	R
b3	—	Reserved	This bit is read as 0.	R
b4	ECMmSSE004	Error Source Status 5	Indicates occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Error not occurred 1: Error occurred	R
b5	ECMmSSE005	Error Source Status 6	Indicates occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Error not occurred 1: Error occurred	R
b6	ECMmSSE006	Error Source Status 7	Indicates occurrence of a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Error not occurred 1: Error occurred	R
b7	ECMmSSE007	Error Source Status 8	Indicates occurrence of a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Error not occurred 1: Error occurred	R
b8	ECMmSSE008	Error Source Status 9	Indicates occurrence of a 1-bit ECC error in the data cache (Data RAM) (error source 9) 0: Error not occurred 1: Error occurred	R
b9	ECMmSSE009	Error Source Status 10	Indicates occurrence of a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Error not occurred 1: Error occurred	R

Bit	Symbol	Bit Name	Description	R/W
b10	ECMmSSE010	Error Source Status 11	Indicates occurrence of a 1-bit ECC error in the ATCM (error source 11). 0: Error not occurred 1: Error occurred	R
b11	ECMmSSE011	Error Source Status 12	Indicates occurrence of a 2-bit ECC error in the ATCM (error source 12). 0: Error not occurred 1: Error occurred	R
b12	ECMmSSE012	Error Source Status 13	Indicates occurrence of a 1-bit ECC error in the BTCM (error source 13). 0: Error not occurred 1: Error occurred	R
b13	ECMmSSE013	Error Source Status 14	Indicates occurrence of a 2-bit ECC error in the BTCM (error source 14). 0: Error not occurred 1: Error occurred	R
b14	ECMmSSE014	Error Source Status 15	Indicates occurrence of a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Error not occurred 1: Error occurred	R
b15	ECMmSSE015	Error Source Status 16	Indicates occurrence of a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Error not occurred 1: Error occurred	R
b16	ECMmSSE016	Error Source Status 17	Indicates occurrence of a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Error not occurred 1: Error occurred	R
b17	ECMmSSE017	Error Source Status 18	Indicates occurrence of a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Error not occurred 1: Error occurred	R
b18	ECMmSSE018	Error Source Status 19	Indicates occurrence of an RSCAN overflow error (error source 19). 0: Error not occurred 1: Error occurred	R
b19	ECMmSSE019	Error Source Status 20	Indicates occurrence of an error of main clock oscillation stop detection (error source 20). 0: Error not occurred 1: Error occurred	R
b20	ECMmSSE020	Error Source Status 21	Indicates occurrence of an error of CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Error not occurred 1: Error occurred	R
b21	ECMmSSE021	Error Source Status 22	Indicates occurrence of an error of CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Error not occurred 1: Error occurred	R
b22	ECMmSSE022	Error Source Status 23	Indicates occurrence of an error of CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Error not occurred 1: Error occurred	R
b23	ECMmSSE023	Error Source Status 24	Indicates occurrence of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Error not occurred 1: Error occurred	R
b24	ECMmSSE024	Error Source Status 25	Indicates occurrence of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Error not occurred 1: Error occurred	R

Bit	Symbol	Bit Name	Description	R/W
b25	ECMmSSE025	Error Source Status 26	Indicates occurrence of a UVW overcurrent abnormality detection error (error source 26). 0: Error not occurred 1: Error occurred	R
b26	ECMmSSE026	Error Source Status 27	Indicates occurrence of a UVW total current abnormality detection error (error source 27). 0: Error not occurred 1: Error occurred	R
b27	ECMmSSE027	Error Source Status 28	Indicates occurrence of a UVW short circuit abnormality detection error (error source 28). 0: Error not occurred 1: Error occurred	R
b28	—	Reserved	The read value is undefined.	R
b29	ECMmSSE029	Error Source Status 30	Indicates occurrence of an X overcurrent abnormality detection error (error source 30). 0: Error not occurred 1: Error occurred	R
b30	ECMmSSE030	Error Source Status 31	Indicates occurrence of an X short circuit abnormality detection error (error source 31). 0: Error not occurred 1: Error occurred	R
b31	ECMmSSE031	Error Source Status 32	Indicates occurrence of a DOC operation error (error source 32). 0: Error not occurred 1: Error occurred	R

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, this bit is read as 0.

42.2.4 ECM Master/Checker Error Source Status Register 1 (ECMmESSTR1 (m = M or C))

The ECMmESSTR1 (m = M or C) register is a flag register that indicates whether individual error sources occurred. This register is cleared with the corresponding bits in the ECM error source status clear trigger register 1 (ECMESSTC1) set, or with the RES# pin reset. This register is not cleared by occurrence of other reset sources.

Address(es): ECMMESSTR1: A007 D00Ch
ECMCESSTR1: A007 D04Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMm SSE108	ECMm SSE107	ECMm SSE106	ECMm SSE105	ECMm SSE104	ECMm SSE103	ECMm SSE102	ECMm SSE101	ECMm SSE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMmSSE100	Error Source Status 33	Indicates occurrence of a bus error (error source 33). 0: Error not occurred 1: Error occurred	R
b1	ECMmSSE101	Error Source Status 34	Indicates occurrence of a timeout error caused by the external WAIT pin (error source 34). 0: Error not occurred 1: Error occurred	R
b2	ECMmSSE102	Error Source Status 35	Indicates occurrence of extended pseudo error 35 (error source 35)*1. 0: Error not occurred 1: Error occurred	R
b3	ECMmSSE103	Error Source Status 36	Indicates occurrence of extended pseudo error 36 (error source 36)*1. 0: Error not occurred 1: Error occurred	R
b4	ECMmSSE104	Error Source Status 37	Indicates occurrence of extended pseudo error 37 (error source 37)*1. 0: Error not occurred 1: Error occurred	R
b5	ECMmSSE105	Error Source Status 38	Indicates occurrence of extended pseudo error 38 (error source 38)*1. 0: Error not occurred 1: Error occurred	R
b6	ECMmSSE106	Error Source Status 39	Indicates occurrence of extended pseudo error 39 (error source 39)*1. 0: Error not occurred 1: Error occurred	R
b7	ECMmSSE107	Error Source Status 40	Indicates occurrence of extended pseudo error 40 (error source 40)*1. 0: Error not occurred 1: Error occurred	R
b8	ECMmSSE108	Error Source Status 41	Indicates occurrence of extended pseudo error 41 (error source 41)*1. 0: Error not occurred 1: Error occurred	R
b31 to b9	—	Reserved	These bits are read as 0.	R

Note 1. An error occurs when the ECMPE1.ECMPE102 to ECMPE1.ECMPE108 bit is set by software.

42.2.5 ECM Master/Checker Error Source Status Register 2 (ECMmESSTR2 (m = M or C))

The ECMmESSTR2 (m = M or C) register is a flag register that indicates whether individual error sources occurred. Bits 30 to 28 of this register are cleared with the corresponding bits in the ECM error source status clear trigger register 2 (ECMESSTC2) set, or with the RES# pin reset. This register is not cleared by occurrence of other reset sources. Note that bit 31 of this register is not reset.

Address(es): ECMMESSTR2: A007 D010h
ECMCESSTR2: A007 D050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMm SSE231	ECMm SSE230	ECMm SSE229	ECMm SSE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0.	R
b28	ECMmSSE228	Error Source Status 93	Indicates occurrence of an ECM compare error (error source 93). 0: ECM compare error not occurred 1: ECM compare error occurred	R
b29	ECMmSSE229	Error Source Status 94	Indicates occurrence of a delay timer overflow (error source 94). 0: Delay timer overflow not occurred 1: Delay timer overflow occurred	R
b30	ECMmSSE230	Error Source Status 95	Indicates the status written in the ECMmESET register (error source 95). 0: Error not occurred 1: An error was set by the ECMmEST bit in the ECMmESET register.	R
b31	ECMmSSE231	Error Source Status 96	Indicates occurrence of a loopback error (error source 96). This bit is not initialized by reset. 0: Error output (master/checker) is the low level. 1: Error output (master/checker) is the high level.	R

42.2.6 ECM Master/Checker Protection Command Register (ECMmPCMD0 (m = M or C))

The ECMmPCMD0 (m = M or C) register controls writing to the protected registers. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): ECMMPCMD0: A007 D014h
ECMCPCMD0: A007 D054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	Undefined															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ECMm0REG[7:0]							
Value after reset:	Undefined															

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ECMm0REG7 to ECMm0REG0	Specific Instruction Sequence Write	Writes the specific instruction sequence to enable writing to the ECMm register (m = M or C).	W
b31 to b8	—	Reserved	The write value should be 0.	W

42.2.7 ECM Error Pulse Configuration Register (ECMEPCFG)

The ECMEPCFG register controls output to the ERROROUT# pin. For details, see section 42.3.1, Operations for Error Output.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D080h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMSL 0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMSL0	ERROROUT# Pin Operation Set	Sets the operation on the ERROROUT# pin for outputting an error. 0: Non-dynamic mode 1: Dynamic mode	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.8 ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0)

The ECMMICFG0 register controls generation of ECM maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMMIE031	ECMMIE030	ECMMIE029	—	ECMMIE027	ECMMIE026	ECMMIE025	ECMMIE024	ECMMIE023	ECMMIE022	ECMMIE021	ECMMIE020	ECMMIE019	ECMMIE018	ECMMIE017	ECMMIE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMMIE015	ECMMIE014	ECMMIE013	ECMMIE012	ECMMIE011	ECMMIE010	ECMMIE009	ECMMIE008	ECMMIE007	ECMMIE006	ECMMIE005	ECMMIE004	—	ECMMIE002	ECMMIE001	ECMMIE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMMIE000	ECM Maskable Interrupt Generation Control 1	Enables or disables a maskable interrupt due to occurrence of a WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b1	ECMMIE001	ECM Maskable Interrupt Generation Control 2	Enables or disables a maskable interrupt due to occurrence of a WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b2	ECMMIE002	ECM Maskable Interrupt Generation Control 3	Enables or disables a maskable interrupt due to occurrence of an IWDTa overflow/refresh error (error source 3). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMMIE004	ECM Maskable Interrupt Generation Control 5	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b5	ECMMIE005	ECM Maskable Interrupt Generation Control 6	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	ECMMIE006	ECM Maskable Interrupt Generation Control 7	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b7	ECMMIE007	ECM Maskable Interrupt Generation Control 8	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMMIE008	ECM Maskable Interrupt Generation Control 9	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b9	ECMMIE009	ECM Maskable Interrupt Generation Control 10	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b10	ECMMIE010	ECM Maskable Interrupt Generation Control 11	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the ATCM (error source 11). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b11	ECMMIE011	ECM Maskable Interrupt Generation Control 12	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the ATCM (error source 12). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b12	ECMMIE012	ECM Maskable Interrupt Generation Control 13	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the BTCM (error source 13). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b13	ECMMIE013	ECM Maskable Interrupt Generation Control 14	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the BTCM (error source 14). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b14	ECMMIE014	ECM Maskable Interrupt Generation Control 15	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b15	ECMMIE015	ECM Maskable Interrupt Generation Control 16	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b16	ECMMIE016	ECM Maskable Interrupt Generation Control 17	Enables or disables a maskable interrupt due to occurrence of a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b17	ECMMIE017	ECM Maskable Interrupt Generation Control 18	Enables or disables a maskable interrupt due to occurrence of a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b18	ECMMIE018	ECM Maskable Interrupt Generation Control 19	Enables or disables a maskable interrupt due to occurrence of an RSCAN overflow error (error source 19). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b19	ECMMIE019	ECM Maskable Interrupt Generation Control 20	Enables or disables a maskable interrupt due to occurrence of an error of main clock oscillation stop detection (error source 20). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMMIE020	ECM Maskable Interrupt Generation Control 21	Enables or disables a maskable interrupt due to occurrence of an error of CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b21	ECMMIE021	ECM Maskable Interrupt Generation Control 22	Enables or disables a maskable interrupt due to occurrence of an error of CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b22	ECMMIE022	ECM Maskable Interrupt Generation Control 23	Enables or disables a maskable interrupt due to occurrence of an error of CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b23	ECMMIE023	ECM Maskable Interrupt Generation Control 24	Enables or disables a maskable interrupt due to occurrence of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b24	ECMMIE024	ECM Maskable Interrupt Generation Control 25	Enables or disables a maskable interrupt due to occurrence of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b25	ECMMIE025	ECM Maskable Interrupt Generation Control 26	Enables or disables a maskable interrupt due to occurrence of a UVW overcurrent abnormality detection error (error source 26). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b26	ECMMIE026	ECM Maskable Interrupt Generation Control 27	Enables or disables a maskable interrupt due to occurrence of a UVW total current abnormality detection error (error source 27). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b27	ECMMIE027	ECM Maskable Interrupt Generation Control 28	Enables or disables a maskable interrupt due to occurrence of a UVW short circuit abnormality detection error (error source 28). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b28	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29	ECMMIE029	ECM Maskable Interrupt Generation Control 30	Enables or disables a maskable interrupt due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b30	ECMMIE030	ECM Maskable Interrupt Generation Control 31	Enables or disables a maskable interrupt due to occurrence of an X short circuit abnormality detection error (error source 31). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b31	ECMMIE031	ECM Maskable Interrupt Generation Control 32	Enables or disables a maskable interrupt due to occurrence of a DOC operation error (error source 32). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.9 ECM Maskable Interrupt Configuration Register 1 (ECMMICFG1)

The ECMMICFG1 register controls generation of ECM maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D088h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMMIE108	ECMMIE107	ECMMIE106	ECMMIE105	ECMMIE104	ECMMIE103	ECMMIE102	ECMMIE101	ECMMIE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMMIE100	ECM Maskable Interrupt Generation Control 33	Enables or disables a maskable interrupt due to occurrence of a bus error (error source 33). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b1	ECMMIE101	ECM Maskable Interrupt Generation Control 34	Enables or disables a maskable interrupt due to occurrence of a timeout error caused by the external WAIT pin (error source 34). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b2	ECMMIE102	ECM Maskable Interrupt Generation Control 35	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 35 (error source 35). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b3	ECMMIE103	ECM Maskable Interrupt Generation Control 36	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 36 (error source 36). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b4	ECMMIE104	ECM Maskable Interrupt Generation Control 37	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 37 (error source 37). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b5	ECMMIE105	ECM Maskable Interrupt Generation Control 38	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 38 (error source 38). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	ECMMIE106	ECM Maskable Interrupt Generation Control 39	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 39 (error source 39). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b7	ECMMIE107	ECM Maskable Interrupt Generation Control 40	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 40 (error source 40). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b8	ECMMIE108	ECM Maskable Interrupt Generation Control 41	Enables or disables a maskable interrupt due to occurrence of extended pseudo error 41 (error source 41). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.10 ECM Maskable Interrupt Configuration Register 2 (ECMMICFG2)

The ECMMICFG2 register controls generation of ECM maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D08Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ECMMIE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ECMMIE228	ECM Maskable Interrupt Generation Control 93	Enables or disables a maskable interrupt due to occurrence of an ECM compare error (error source 93). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.11 ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0)

The ECMNMICFG0 register controls generation of ECM non-maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMNMIE031	ECMNMIE030	ECMNMIE029	—	ECMNMIE027	ECMNMIE026	ECMNMIE025	ECMNMIE024	ECMNMIE023	ECMNMIE022	ECMNMIE021	ECMNMIE020	ECMNMIE019	ECMNMIE018	ECMNMIE017	ECMNMIE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMNMIE015	ECMNMIE014	ECMNMIE013	ECMNMIE012	ECMNMIE011	ECMNMIE010	ECMNMIE009	ECMNMIE008	ECMNMIE007	ECMNMIE006	ECMNMIE005	ECMNMIE004	—	ECMNMIE002	ECMNMIE001	ECMNMIE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMNMIE000	ECM Non-maskable Interrupt Generation Control 1	Enables or disables a non-maskable interrupt due to occurrence of a WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b1	ECMMIE001	ECM Non-maskable Interrupt Generation Control 2	Enables or disables a non-maskable interrupt due to occurrence of a WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b2	ECMNMIE002	ECM Non-maskable Interrupt Generation Control 3	Enables or disables a non-maskable interrupt due to occurrence of an IWDTa overflow/refresh error (error source 3). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMNMIE004	ECM Non-maskable Interrupt Generation Control 5	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error (with correction) and 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b5	ECMNMIE005	ECM Non-maskable Interrupt Generation Control 6	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error (with correction) and 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	ECMNMIE006	ECM Non-maskable Interrupt Generation Control 7	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b7	ECMNMIE007	ECM Non-maskable Interrupt Generation Control 8	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMNMIE008	ECM Non-maskable Interrupt Generation Control 9	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b9	ECMNMIE009	ECM Non-maskable Interrupt Generation Control 10	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b10	ECMNMIE010	ECM Non-maskable Interrupt Generation Control 11	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the ATCM (error source 11). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b11	ECMNMIE011	ECM Non-maskable Interrupt Generation Control 12	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the ATCM (error source 12). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b12	ECMNMIE012	ECM Non-maskable Interrupt Generation Control 13	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the BTCM (error source 13). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b13	ECMNMIE013	ECM Non-maskable Interrupt Generation Control 14	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the BTCM (error source 14). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b14	ECMNMIE014	ECM Non-maskable Interrupt Generation Control 15	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b15	ECMNMIE015	ECM Non-maskable Interrupt Generation Control 16	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b16	ECMNMIE016	ECM Non-maskable Interrupt Generation Control 17	Enables or disables a non-maskable interrupt due to occurrence of a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b17	ECMNMIE017	ECM Non-maskable Interrupt Generation Control 18	Enables or disables a non-maskable interrupt due to occurrence of a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b18	ECMNMIE018	ECM Non-maskable Interrupt Generation Control 19	Enables or disables a non-maskable interrupt due to occurrence of an RSCAN overflow error (error source 19). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b19	ECMNMIE019	ECM Non-maskable Interrupt Generation Control 20	Enables or disables a non-maskable interrupt due to occurrence of an error of main clock oscillation stop detection (error source 20). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMNMIE020	ECM Non-maskable Interrupt Generation Control 21	Enables or disables a non-maskable interrupt due to occurrence of an error of CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b21	ECMNMIE021	ECM Non-maskable Interrupt Generation Control 22	Enables or disables a non-maskable interrupt due to occurrence of an error of CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b22	ECMNMIE022	ECM Non-maskable Interrupt Generation Control 23	Enables or disables a non-maskable interrupt due to occurrence of an error of CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b23	ECMNMIE023	ECM Non-maskable Interrupt Generation Control 24	Enables or disables a non-maskable interrupt due to occurrence of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b24	ECMNMIE024	ECM Non-maskable Interrupt Generation Control 25	Enables or disables a non-maskable interrupt due to occurrence of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b25	ECMNMIE025	ECM Non-maskable Interrupt Generation Control 26	Enables or disables a non-maskable interrupt due to occurrence of a UVW overcurrent abnormality detection error (error source 26). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b26	ECMNMIE026	ECM Non-maskable Interrupt Generation Control 27	Enables or disables a non-maskable interrupt due to occurrence of a UVW total current abnormality detection error (error source 27). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b27	ECMNMIE027	ECM Non-maskable Interrupt Generation Control 28	Enables or disables a non-maskable interrupt due to occurrence of a UVW short circuit abnormality detection error (error source 28). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b28	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29	ECMNMIE029	ECM Non-maskable Interrupt Generation Control 30	Enables or disables a non-maskable interrupt due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b30	ECMNMIE030	ECM Non-maskable Interrupt Generation Control 31	Enables or disables a non-maskable interrupt due to occurrence of an X short circuit abnormality detection error (error source 31). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b31	ECMNMIE031	ECM Non-maskable Interrupt Generation Control 32	Enables or disables a non-maskable interrupt due to occurrence of a DOC operation error (error source 32). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.12 ECM Non-maskable Interrupt Configuration Register 1 (ECMNMICFG1)

The ECMNMICFG1 register controls generation of ECM non-maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMNMIE108	ECMNMIE107	ECMNMIE106	ECMNMIE105	ECMNMIE104	ECMNMIE103	ECMNMIE102	ECMNMIE101	ECMNMIE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMNMIE100	ECM Non-maskable Interrupt Generation Control 33	Enables or disables a non-maskable interrupt due to occurrence of a bus error (error source 33). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b1	ECMNMIE101	ECM Non-maskable Interrupt Generation Control 34	Enables or disables a non-maskable interrupt due to occurrence of a timeout error caused by the external WAIT pin (error source 34). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b2	ECMNMIE102	ECM Non-maskable Interrupt Generation Control 35	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 35 (error source 35). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b3	ECMNMIE103	ECM Non-maskable Interrupt Generation Control 36	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 36 (error source 36). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b4	ECMNMIE104	ECM Non-maskable Interrupt Generation Control 37	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 37 (error source 37). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b5	ECMNMIE105	ECM Non-maskable Interrupt Generation Control 38	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 38 (error source 38). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	ECMNMIE106	ECM Non-maskable Interrupt Generation Control 39	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 39 (error source 39). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b7	ECMNMIE107	ECM Non-maskable Interrupt Generation Control 40	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 40 (error source 40). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b8	ECMNMIE108	ECM Non-maskable Interrupt Generation Control 41	Enables or disables a non-maskable interrupt due to occurrence of extended pseudo error 41 (error source 41). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.13 ECM Non-maskable Interrupt Configuration Register 2 (ECMNMICFG2)

The ECMNMICFG2 register controls generation of ECM non-maskable interrupts due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ECMNMIE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ECMNMIE228	ECM Non-maskable Interrupt Generation Control 93	Enables or disables a non-maskable interrupt due to occurrence of an ECM compare error (error source 93). 0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.14 ECM Internal Reset Configuration Register 0 (ECMIRCFG0)

The ECMIRCFG0 register controls generation of internal resets (ECM resets) due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D09Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMIRE031	ECMIRE030	ECMIRE029	—	ECMIRE027	ECMIRE026	ECMIRE025	ECMIRE024	ECMIRE023	ECMIRE022	ECMIRE021	ECMIRE020	ECMIRE019	ECMIRE018	ECMIRE017	ECMIRE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMIRE015	ECMIRE014	ECMIRE013	ECMIRE012	ECMIRE011	ECMIRE010	ECMIRE009	ECMIRE008	ECMIRE007	ECMIRE006	ECMIRE005	ECMIRE004	—	ECMIRE002	ECMIRE001	ECMIRE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Description	R/W
b0	ECMIRE000	ECM Internal Reset Generation Control 1	Enables or disables generation of an ECM reset due to occurrence of a WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b1	ECMIRE001	ECM Internal Reset Generation Control 2	Enables or disables generation of an ECM reset due to occurrence of a WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b2	ECMIRE002	ECM Internal Reset Generation Control 3	Enables or disables generation of an ECM reset due to occurrence of an IWDTa overflow/refresh error (error source 3). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMIRE004	ECM Internal Reset Generation Control 5	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b5	ECMIRE005	ECM Internal Reset Generation Control 6	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b6	ECMIRE006	ECM Internal Reset Generation Control 7	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b7	ECMIRE007	ECM Internal Reset Generation Control 8	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMIRE008	ECM Internal Reset Generation Control 9	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b9	ECMIRE009	ECM Internal Reset Generation Control 10	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b10	ECMIRE010	ECM Internal Reset Generation Control 11	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the ATCM (error source 11). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b11	ECMIRE011	ECM Internal Reset Generation Control 12	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the ATCM (error source 12). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b12	ECMIRE012	ECM Internal Reset Generation Control 13	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the BTCM (error source 13). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b13	ECMIRE013	ECM Internal Reset Generation Control 14	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the BTCM (error source 14). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b14	ECMIRE014	ECM Internal Reset Generation Control 15	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b15	ECMIRE015	ECM Internal Reset Generation Control 16	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b16	ECMIRE016	ECM Internal Reset Generation Control 17	Enables or disables generation of an ECM reset due to occurrence of a 1-bit ECC error in the RSCAN RAM (error source 17). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b17	ECMIRE017	ECM Internal Reset Generation Control 18	Enables or disables generation of an ECM reset due to occurrence of a 2-bit ECC error in the RSCAN RAM (error source 18). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b18	ECMIRE018	ECM Internal Reset Generation Control 19	Enables or disables generation of an ECM reset due to occurrence of an RSCAN overflow error (error source 19). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b19	ECMIRE019	ECM Internal Reset Generation Control 20	Enables or disables generation of an ECM reset due to occurrence of an error of main clock oscillation stop detection (error source 20). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMIRE020	ECM Internal Reset Generation Control 21	Enables or disables generation of an ECM reset due to occurrence of an error of CLMA0 oscillation stop detection (PLL0) (error source 21). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b21	ECMIRE021	ECM Internal Reset Generation Control 22	Enables or disables generation of an ECM reset due to occurrence of an error of CLMA1 oscillation stop detection (PLL1) (error source 22). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b22	ECMIRE022	ECM Internal Reset Generation Control 23	Enables or disables generation of an ECM reset due to occurrence of an error of CLMA2 oscillation stop detection (LOCO) (error source 23). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b23	ECMIRE023	ECM Internal Reset Generation Control 24	Enables or disables generation of an ECM reset due to occurrence of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b24	ECMIRE024	ECM Internal Reset Generation Control 25	Enables or disables generation of an ECM reset due to occurrence of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b25	ECMIRE025	ECM Internal Reset Generation Control 26	Enables or disables generation of an ECM reset due to occurrence of a UVW overcurrent abnormality detection error (error source 26). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b26	ECMIRE026	ECM Internal Reset Generation Control 27	Enables or disables generation of an ECM reset due to occurrence of a UVW total current abnormality detection error (error source 27). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b27	ECMIRE027	ECM Internal Reset Generation Control 28	Enables or disables generation of an ECM reset due to occurrence of a UVW short circuit abnormality detection error (error source 28). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b28	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29	ECMIRE029	ECM Internal Reset Generation Control 30	Enables or disables generation of an ECM reset due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b30	ECMIRE030	ECM Internal Reset Generation Control 31	Enables or disables generation of an ECM reset due to occurrence of an X short circuit abnormality detection error (error source 31). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b31	ECMIRE031	ECM Internal Reset Generation Control 32	Enables or disables generation of an ECM reset due to occurrence of a DOC operation error (error source 32). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.15 ECM Internal Reset Configuration Register 1 (ECMIRCFG1)

The ECMIRCFG1 register controls generation of internal resets (ECM resets) due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMIRE108	ECMIRE107	ECMIRE106	ECMIRE105	ECMIRE104	ECMIRE103	ECMIRE102	ECMIRE101	ECMIRE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMIRE100	ECM Internal Reset Generation Control 33	Enables or disables generation of an ECM reset due to occurrence of a bus error (error source 33). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b1	ECMIRE101	ECM Internal Reset Generation Control 34	Enables or disables generation of an ECM reset due to occurrence of a timeout error caused by the external WAIT pin (error source 34). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b2	ECMIRE102	ECM Internal Reset Generation Control 35	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 35 (error source 35). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b3	ECMIRE103	ECM Internal Reset Generation Control 36	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 36 (error source 36). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b4	ECMIRE104	ECM Internal Reset Generation Control 37	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 37 (error source 37). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b5	ECMIRE105	ECM Internal Reset Generation Control 38	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 38 (error source 38). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b6	ECMIRE106	ECM Internal Reset Generation Control 39	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 39 (error source 39). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b7	ECMIRE107	ECM Internal Reset Generation Control 40	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 40 (error source 40). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b8	ECMIRE108	ECM Internal Reset Generation Control 41	Enables or disables generation of an ECM reset due to occurrence of extended pseudo error 41 (error source 41). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.16 ECM Internal Reset Configuration Register 2 (ECMIRCFG2)

The ECMIRCFG2 register controls generation of internal resets (ECM resets) due to occurrence of individual error sources.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	ECMIRE229	ECMIRE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ECMIRE228	ECM Internal Reset Generation Control 93	Enables or disables generation of an ECM reset due to occurrence of an ECM compare error (error source 93). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b29	ECMIRE229	ECM Internal Reset Generation Control 94	Enables or disables generation of an ECM reset due to occurrence of a delay timer overflow (error source 94). 0: ECM reset generation disabled 1: ECM reset generation enabled	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.17 ECM Error Mask Register 0 (ECMEMK0)

The ECMEMK0 register controls mask settings for error output signals due to occurrence of individual error sources. If an unmasked error output signal is generated, the output of the ERROROUT# pin is set to the active level (low level). This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMEMK031	ECMEMK030	ECMEMK029	ECMEMK028	ECMEMK027	ECMEMK026	ECMEMK025	ECMEMK024	ECMEMK023	ECMEMK022	ECMEMK021	ECMEMK020	ECMEMK019	ECMEMK018	ECMEMK017	ECMEMK016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMEMK015	ECMEMK014	ECMEMK013	ECMEMK012	ECMEMK011	ECMEMK010	ECMEMK009	ECMEMK008	ECMEMK007	ECMEMK006	ECMEMK005	ECMEMK004	—	ECMEMK002	ECMEMK001	ECMEMK000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMEMK000	ECM Error Output Signal Mask Control 1	Controls whether to mask an error output signal due to occurrence of a WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: Error signal output not masked 1: Error signal output masked	R/W
b1	ECMEMK001	ECM Error Output Signal Mask Control 2	Controls whether to mask an error output signal due to occurrence of a WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: Error signal output not masked 1: Error signal output masked	R/W
b2	ECMEMK002	ECM Error Output Signal Mask Control 3	Controls whether to mask an error output signal due to occurrence of an IWDTa overflow/refresh error (error source 3). 0: Error signal output not masked 1: Error signal output masked	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMEMK004	ECM Error Output Signal Mask Control 5	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Error signal output not masked 1: Error signal output masked	R/W
b5	ECMEMK005	ECM Error Output Signal Mask Control 6	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Error signal output not masked 1: Error signal output masked	R/W
b6	ECMEMK006	ECM Error Output Signal Mask Control 7	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Error signal output not masked 1: Error signal output masked	R/W
b7	ECMEMK007	ECM Error Output Signal Mask Control 8	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Error signal output not masked 1: Error signal output masked	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMEMK008	ECM Error Output Signal Mask Control 9	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Error signal output not masked 1: Error signal output masked	R/W
b9	ECMEMK009	ECM Error Output Signal Mask Control 10	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Error signal output not masked 1: Error signal output masked	R/W
b10	ECMEMK010	ECM Error Output Signal Mask Control 11	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the ATCM (error source 11). 0: Error signal output not masked 1: Error signal output masked	R/W
b11	ECMEMK011	ECM Error Output Signal Mask Control 12	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the ATCM (error source 12). 0: Error signal output not masked 1: Error signal output masked	R/W
b12	ECMEMK012	ECM Error Output Signal Mask Control 13	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the BTCM (error source 13). 0: Error signal output not masked 1: Error signal output masked	R/W
b13	ECMEMK013	ECM Error Output Signal Mask Control 14	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the BTCM (error source 14). 0: Error signal output not masked 1: Error signal output masked	R/W
b14	ECMEMK014	ECM Error Output Signal Mask Control 15	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Error signal output not masked 1: Error signal output masked	R/W
b15	ECMEMK015	ECM Error Output Signal Mask Control 16	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Error signal output not masked 1: Error signal output masked	R/W
b16	ECMEMK016	ECM Error Output Signal Mask Control 17	Controls whether to mask an error output signal due to occurrence of a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Error signal output not masked 1: Error signal output masked	R/W
b17	ECMEMK017	ECM Error Output Signal Mask Control 18	Controls whether to mask an error output signal due to occurrence of a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Error signal output not masked 1: Error signal output masked	R/W
b18	ECMEMK018	ECM Error Output Signal Mask Control 19	Controls whether to mask an error output signal due to occurrence of an RSCAN overflow error (error source 19). 0: Error signal output not masked 1: Error signal output masked	R/W
b19	ECMEMK019	ECM Error Output Signal Mask Control 20	Controls whether to mask an error output signal due to occurrence of an error of main clock oscillation stop detection (error source 20). 0: Error signal output not masked 1: Error signal output masked	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMEMK020	ECM Error Output Signal Mask Control 21	Controls whether to mask an error output signal due to occurrence of an error of CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Error signal output not masked 1: Error signal output masked	R/W
b21	ECMEMK021	ECM Error Output Signal Mask Control 22	Controls whether to mask an error output signal due to occurrence of an error of CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Error signal output not masked 1: Error signal output masked	R/W
b22	ECMEMK022	ECM Error Output Signal Mask Control 23	Controls whether to mask an error output signal due to occurrence of an error of CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Error signal output not masked 1: Error signal output masked	R/W
b23	ECMEMK023	ECM Error Output Signal Mask Control 24	Controls whether to mask an error output signal due to occurrence of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Error signal output not masked 1: Error signal output masked	R/W
b24	ECMEMK024	ECM Error Output Signal Mask Control 25	Controls whether to mask an error output signal due to occurrence of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Error signal output not masked 1: Error signal output masked	R/W
b25	ECMEMK025	ECM Error Output Signal Mask Control 26	Controls whether to mask an error output signal due to occurrence of a UVW overcurrent abnormality detection error (error source 26). 0: Error signal output not masked 1: Error signal output masked	R/W
b26	ECMEMK026	ECM Error Output Signal Mask Control 27	Controls whether to mask an error output signal due to occurrence of a UVW total current abnormality detection error (error source 27). 0: Error signal output not masked 1: Error signal output masked	R/W
b27	ECMEMK027	ECM Error Output Signal Mask Control 28	Controls whether to mask an error output signal due to occurrence of a UVW short circuit abnormality detection error (error source 28). 0: Error signal output not masked 1: Error signal output masked	R/W
b28	ECMEMK028	ECM Error Output Signal Mask Control 29	Always write 1.	R/W
b29	ECMEMK029	ECM Error Output Signal Mask Control 30	Controls whether to mask an error output signal due to occurrence of an X overcurrent abnormality detection error (error source 30). 0: Error signal output not masked 1: Error signal output masked	R/W
b30	ECMEMK030	ECM Error Output Signal Mask Control 31	Controls whether to mask an error output signal due to occurrence of an X short circuit abnormality detection error (error source 31). 0: Error signal output not masked 1: Error signal output masked	R/W
b31	ECMEMK031	ECM Error Output Signal Mask Control 32	Controls whether to mask an error output signal due to occurrence of a DOC operation error (error source 32). 0: Error signal output not masked 1: Error signal output masked	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.18 ECM Error Mask Register 1 (ECMEMK1)

The ECMEMK1 register controls mask settings for error output signals due to occurrence of individual error sources. If an unmasked error output signal is generated, the output of the ERROROUT# pin is set to the active level (low level). This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMEMK108	ECMEMK107	ECMEMK106	ECMEMK105	ECMEMK104	ECMEMK103	ECMEMK102	ECMEMK101	ECMEMK100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMEMK100	ECM Error Output Signal Mask Control 33	Controls whether to mask an error output signal due to occurrence of a bus error (error source 33). 0: Error signal output not masked 1: Error signal output masked	R/W
b1	ECMEMK101	ECM Error Output Signal Mask Control 34	Controls whether to mask an error output signal due to occurrence of a timeout error caused by the external WAIT pin (error source 34). 0: Error signal output not masked 1: Error signal output masked	R/W
b2	ECMEMK102	ECM Error Output Signal Mask Control 35	Controls whether to mask an error output signal due to occurrence of extended pseudo error 35 (error source 35). 0: Error signal output not masked 1: Error signal output masked	R/W
b3	ECMEMK103	ECM Error Output Signal Mask Control 36	Controls whether to mask an error output signal due to occurrence of extended pseudo error 36 (error source 36). 0: Error signal output not masked 1: Error signal output masked	R/W
b4	ECMEMK104	ECM Error Output Signal Mask Control 37	Controls whether to mask an error output signal due to occurrence of extended pseudo error 37 (error source 37). 0: Error signal output not masked 1: Error signal output masked	R/W
b5	ECMEMK105	ECM Error Output Signal Mask Control 38	Controls whether to mask an error output signal due to occurrence of extended pseudo error 38 (error source 38). 0: Error signal output not masked 1: Error signal output masked	R/W
b6	ECMEMK106	ECM Error Output Signal Mask Control 39	Controls whether to mask an error output signal due to occurrence of extended pseudo error 39 (error source 39). 0: Error signal output not masked 1: Error signal output masked	R/W
b7	ECMEMK107	ECM Error Output Signal Mask Control 40	Controls whether to mask an error output signal due to occurrence of extended pseudo error 40 (error source 40). 0: Error signal output not masked 1: Error signal output masked	R/W
b8	ECMEMK108	ECM Error Output Signal Mask Control 41	Controls whether to mask an error output signal due to occurrence of extended pseudo error 41 (error source 41). 0: Error signal output not masked 1: Error signal output masked	R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.19 ECM Error Mask Register 2 (ECMEMK2)

The ECMEMK2 register controls mask settings for error output signals due to occurrence of individual error sources. If an unmasked error output signal is generated, the output of the ERROROUT# pin is set to the active level (low level). This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	ECMEMK229	ECMEMK228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0.	R
b28	ECMEMK228	ECM Internal Reset Generation Control 93	ECM Error Output Signal Mask Control Controls whether to mask an error output signal due to occurrence of an ECM compare error (error source 93). 0: Error signal output not masked 1: Error signal output masked	R/W
b29	ECMEMK229	ECM Internal Reset Generation Control 94	ECM Error Output Signal Mask Control Controls whether to mask an error output signal due to occurrence of a delay timer overflow (error source 94). 0: Error signal output not masked 1: Error signal output masked	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.20 ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0)

The ECMESSTC0 register controls clearing of individual error statuses. Setting individual bits in this register to 1 can clear the corresponding error statuses held in the ECMmESSTR0 (m = M or C) register.

This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.

Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMCLSSE031	ECMCLSSE030	ECMCLSSE029	—	ECMCLSSE027	ECMCLSSE026	ECMCLSSE025	ECMCLSSE024	ECMCLSSE023	ECMCLSSE022	ECMCLSSE021	ECMCLSSE020	ECMCLSSE019	ECMCLSSE018	ECMCLSSE017	ECMCLSSE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMCLSSE015	ECMCLSSE014	ECMCLSSE013	ECMCLSSE012	ECMCLSSE011	ECMCLSSE010	ECMCLSSE009	ECMCLSSE008	ECMCLSSE007	ECMCLSSE006	ECMCLSSE005	ECMCLSSE004	—	ECMCLSSE002	ECMCLSSE001	ECMCLSSE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMCLSSE000	ECM Error Status Clear 1	Clears the error status of WDT overflow/refresh error (for Cortex-R4) (error source 1) and the ECMmESSTR0.ECMmSSE000 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b1	ECMCLSSE001	ECM Error Status Clear 2	Clears the error status of WDT overflow/refresh error (for Cortex-M3) (error source 2) and the ECMmESSTR0.ECMmSSE001 bit.*1 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b2	ECMCLSSE002	ECM Error Status Clear 3	Clears the error status of IWDTa overflow/refresh error (error source 3) and the ECMmESSTR0.ECMmSSE002 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b3	—	Reserved	The write value should be 0.	W
b4	ECMCLSSE004	ECM Error Status Clear 5	Clears the error status of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5) and the ECMmESSTR0.ECMmSSE004 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b5	ECMCLSSE005	ECM Error Status Clear 6	Clears the error status of a 1-bit ECC error (with correction) or a 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6) and the ECMmESSTR0.ECMmSSE005 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b6	ECMCLSSE006	ECM Error Status Clear 7	Clears the error status of 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7) and the ECMmESSTR0.ECMmSSE006 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b7	ECMCLSSE007	ECM Error Status Clear 8	Clears the error status of 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8) and the ECMmESSTR0.ECMmSSE007 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMCLSSE008	ECM Error Status Clear 9	Clears the error status of 1-bit ECC error in the data cache (Data RAM) (error source 9) and the ECMmESSTR0.ECMmSSE008 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b9	ECMCLSSE009	ECM Error Status Clear 10	Clears the error status of 2-bit ECC error in the data cache (Data RAM) (error source 10) and the ECMmESSTR0.ECMmSSE009 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b10	ECMCLSSE010	ECM Error Status Clear 11	Clears the error status of 1-bit ECC error in the ATCM (error source 11) and the ECMmESSTR0.ECMmSSE010 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b11	ECMCLSSE011	ECM Error Status Clear 12	Clears the error status of 2-bit ECC error in the ATCM (error source 12) and the ECMmESSTR0.ECMmSSE011 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b12	ECMCLSSE012	ECM Error Status Clear 13	Clears the error status of 1-bit ECC error in the BTCM (error source 13) and the ECMmESSTR0.ECMmSSE012 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b13	ECMCLSSE013	ECM Error Status Clear 14	Clears the error status of 2-bit ECC error in the BTCM (error source 14) and the ECMmESSTR0.ECMmSSE013 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b14	ECMCLSSE014	ECM Error Status Clear 15	Clears the error status of 1-bit ECC error in the IRAM or DRAM (error source 15) and the ECMmESSTR0.ECMmSSE014 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b15	ECMCLSSE015	ECM Error Status Clear 16	Clears the error status of 2-bit ECC error in the IRAM or DRAM (error source 16) and the ECMmESSTR0.ECMmSSE015 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b16	ECMCLSSE016	ECM Error Status Clear 17	Clears the error status of 1-bit ECC error in the RSCAN RAM (error source 17) and the ECMmESSTR0.ECMmSSE016 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b17	ECMCLSSE017	ECM Error Status Clear 18	Clears the error status of 2-bit ECC error in the RSCAN RAM (error source 18) and the ECMmESSTR0.ECMmSSE017 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b18	ECMCLSSE018	ECM Error Status Clear 19	Clears the error status of RSCAN overflow error (error source 19) and the ECMmESSTR0.ECMmSSE018 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b19	ECMCLSSE019	ECM Error Status Clear 20	Clears the error status of main clock oscillation stop detection (error source 20) and the ECMmESSTR0.ECMmSSE019 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMCLSSE020	ECM Error Status Clear 21	Clears the error status of CLMA0 oscillation stop detection (PLL0) (error source 21) and the ECMmESSTR0.ECMmSSE020 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b21	ECMCLSSE021	ECM Error Status Clear 22	Clears the error status of CLMA1 oscillation stop detection (PLL1) (error source 22) and the ECMmESSTR0.ECMmSSE021 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b22	ECMCLSSE022	ECM Error Status Clear 23	Clears the error status of CLMA2 oscillation stop detection (LOCO) (error source 23) and the ECMmESSTR0.ECMmSSE022 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b23	ECMCLSSE023	ECM Error Status Clear 24	Clears the error status of a 12-bit A/D converter unit 0 overwrite interrupt (error source 24) and the ECMmESSTR0.ECMmSSE023 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b24	ECMCLSSE024	ECM Error Status Clear 25	Clears the error status of a 12-bit A/D converter unit 1 overwrite interrupt (error source 25) and the ECMmESSTR0.ECMmSSE024 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b25	ECMCLSSE025	ECM Error Status Clear 26	Clears the error status of UVW overcurrent abnormality detection error (error source 26) and the ECMmESSTR0.ECMmSSE025 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b26	ECMCLSSE026	ECM Error Status Clear 27	Clears the error status of UVW total current abnormality detection error (error source 27) and the ECMmESSTR0.ECMmSSE026 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b27	ECMCLSSE027	ECM Error Status Clear 28	Clears the error status of UVW short circuit abnormality detection error (error source 28) and the ECMmESSTR0.ECMmSSE027 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b28	—	Reserved	The write value should be 0.	W
b29	ECMCLSSE029	ECM Error Status Clear 30	Clears the error status of X overcurrent abnormality detection error (error source 30) and the ECMmESSTR0.ECMmSSE029 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b30	ECMCLSSE030	ECM Error Status Clear 31	Clears the error status of X short circuit abnormality detection error (error source 31) and the ECMmESSTR0.ECMmSSE030 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b31	ECMCLSSE031	ECM Error Status Clear 32	Clears the error status of DOC operation error (error source 32) and the ECMmESSTR0.ECMmSSE031 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.21 ECM Error Source Status Clear Trigger Register 1 (ECMESSTC1)

The ECMESSTC1 register controls clearing of individual error statuses. Setting individual bits in this register to 1 can clear the corresponding error statuses held in the ECMmESSTR1 (m = M or C) register.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMCL SSE108	ECMCL SSE107	ECMCL SSE106	ECMCL SSE105	ECMCL SSE104	ECMCL SSE103	ECMCL SSE102	ECMCL SSE101	ECMCL SSE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMCLSSE100	ECM Error Status Clear 33	Clears the error status of bus error (error source 33) and the ECMmESSTR1.ECMmSSE100 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b1	ECMCLSSE101	ECM Error Status Clear 34	Clears the error status of a timeout error caused by the external WAIT pin (error source 34) and the ECMmESSTR1.ECMmSSE101 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b2	ECMCLSSE102	ECM Error Status Clear 35	Clears the error status of extended pseudo error 35 (error source 35) and the ECMmESSTR1.ECMmSSE102 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b3	ECMCLSSE103	ECM Error Status Clear 36	Clears the error status of extended pseudo error 36 (error source 36) and the ECMmESSTR1.ECMmSSE103 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b4	ECMCLSSE104	ECM Error Status Clear 37	Clears the error status of extended pseudo error 37 (error source 37) and the ECMmESSTR1.ECMmSSE104 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b5	ECMCLSSE105	ECM Error Status Clear 38	Clears the error status of extended pseudo error 38 (error source 38) and the ECMmESSTR1.ECMmSSE105 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b6	ECMCLSSE106	ECM Error Status Clear 39	Clears the error status of extended pseudo error 39 (error source 39) and the ECMmESSTR1.ECMmSSE106 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b7	ECMCLSSE107	ECM Error Status Clear 40	Clears the error status of extended pseudo error 40 (error source 40) and the ECMmESSTR1.ECMmSSE107 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b8	ECMCLSSE108	ECM Error Status Clear 41	Clears the error status of extended pseudo error 41 (error source 41) and the ECMmESSTR1.ECMmSSE108 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W

Bit	Symbol	Bit Name	Description	R/W
b31 to b9	—	Reserved	The write value should be 0.	W

42.2.22 ECM Error Source Status Clear Trigger Register 2 (ECMESSTC2)

The ECMESSTC2 register controls clearing of individual error statuses. Setting individual bits in this register to 1 can clear the corresponding error statuses held in the ECMmESSTR2 (m = M or C) register.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0BCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	ECMCLSSE230	ECMCLSSE229	ECMCLSSE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	The write value should be 0.	W
b28	ECMCLSSE228	ECM Error Status Clear 93	Clears the error status of ECM compare error (error source 93) and the ECMmESSTR2.ECMmSSE228 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b29	ECMCLSSE229	ECM Error Status Clear 94	Clears the error status of a delay timer overflow (error source 94) and the ECMmESSTR2.ECMmSSE229 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b30	ECMCLSSE230	ECM Error Status Clear 95	Clears the error status due to writing to ECMmESET (error source 95) and the ECMmESSTR2.ECMmSSE230 bit. 0: Corresponding error status unchanged 1: Corresponding error status cleared	W
b31	—	Reserved	The write value should be 0.	W

42.2.23 ECM Protection Command Register (ECMPCMD1)

The ECMPCMD1 register controls writing to protected common registers. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	Undefined															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ECM1REG[7:0]							
Value after reset:	Undefined															

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	ECM1REG[7:0]	Specific Instruction Sequence Write	Write the specific instruction sequence to enable writing to common registers.	W
b31 to b8	—	Reserved	The write value should be 0.	W

42.2.24 ECM Protection Status Register (ECMPS)

The ECMPS register indicates the status of whether writing to the protected register has been correctly done. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMPRERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMPRERR	ECM Protection Status	Indicates whether writing to the write protected register has been correctly done. 0: Writing was successful. 1: Writing failed.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

42.2.25 ECM Pseudo Error Trigger Register 0 (ECMPE0)

The ECMPE0 register is a control register that issues a pseudo error for self-diagnosis. When a pseudo error is issued, an interrupt set by ECM or an ECM reset occurs in the same way as when an actual error source occurs.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMPE031	ECMPE030	ECMPE029	—	ECMPE027	ECMPE026	ECMPE025	ECMPE024	ECMPE023	ECMPE022	ECMPE021	ECMPE020	ECMPE019	ECMPE018	ECMPE017	ECMPE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMPE015	ECMPE014	ECMPE013	ECMPE012	ECMPE011	ECMPE010	ECMPE009	ECMPE008	ECMPE007	ECMPE006	ECMPE005	ECMPE004	—	ECMPE002	ECMPE001	ECMPE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMPE000	ECM Pseudo Error Trigger 1	Generates a pseudo WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b1	ECMPE001	ECM Pseudo Error Trigger 2	Generates a pseudo WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b2	ECMPE002	ECM Pseudo Error Trigger 3	Generates a pseudo IWDTa overflow/refresh error (error source 3). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b3	—	Reserved	The write value should be 0.	W
b4	ECMPE004	ECM Pseudo Error Trigger 5	Generates a pseudo 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b5	ECMPE005	ECM Pseudo Error Trigger 6	Generates a pseudo 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b6	ECMPE006	ECM Pseudo Error Trigger 7	Generates a pseudo 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b7	ECMPE007	ECM Pseudo Error Trigger 8	Generates a pseudo 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b8	ECMPE008	ECM Pseudo Error Trigger 9	Generates a pseudo 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W

Bit	Symbol	Bit Name	Description	R/W
b9	ECMPE009	ECM Pseudo Error Trigger 10	Generates a pseudo 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b10	ECMPE010	ECM Pseudo Error Trigger 11	Generates a pseudo 1-bit ECC error in the ATCM (error source 11). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b11	ECMPE011	ECM Pseudo Error Trigger 12	Generates a pseudo 2-bit ECC error in the ATCM (error source 12). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b12	ECMPE012	ECM Pseudo Error Trigger 13	Generates a pseudo 1-bit ECC error in the BTCM (error source 13). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b13	ECMPE013	ECM Pseudo Error Trigger 14	Generates a pseudo 2-bit ECC error in the BTCM (error source 14). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b14	ECMPE014	ECM Pseudo Error Trigger 15	Generates a pseudo 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b15	ECMPE015	ECM Pseudo Error Trigger 16	Generates a pseudo 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b16	ECMPE016	ECM Pseudo Error Trigger 17	Generates a pseudo 1-bit ECC error in the RSCAN RAM (error source 17). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b17	ECMPE017	ECM Pseudo Error Trigger 18	Generates a pseudo 2-bit ECC error in the RSCAN RAM (error source 18). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b18	ECMPE018	ECM Pseudo Error Trigger 19	Generates a pseudo RSCAN overflow error (error source 19). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b19	ECMPE019	ECM Pseudo Error Trigger 20	Generates pseudo detection of main clock oscillation stoppage (error source 20). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b20	ECMPE020	ECM Pseudo Error Trigger 21	Generates pseudo detection of CLMA0 oscillation stoppage (PLL0) (error source 21). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b21	ECMPE021	ECM Pseudo Error Trigger 22	Generates pseudo detection of CLMA1 oscillation stoppage (PLL1) (error source 22). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b22	ECMPE022	ECM Pseudo Error Trigger 23	Generates pseudo detection of CLMA2 oscillation stoppage (LOCO) (error source 23). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b23	ECMPE023	ECM Pseudo Error Trigger 24	Generates a pseudo 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W

Bit	Symbol	Bit Name	Description	R/W
b24	ECMPE024	ECM Pseudo Error Trigger 25	Generates a pseudo 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b25	ECMPE025	ECM Pseudo Error Trigger 26	Generates a pseudo UVW overcurrent abnormality detection error (error source 26). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b26	ECMPE026	ECM Pseudo Error Trigger 27	Generates a pseudo UVW total current abnormality detection error (error source 27). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b27	ECMPE027	ECM Pseudo Error Trigger 28	Generates a pseudo UVW short circuit abnormality detection error (error source 28). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b28	—	Reserved	The write value should be 0.	W
b29	ECMPE029	ECM Pseudo Error Trigger 30	Generates a pseudo X overcurrent abnormality detection error (error source 30). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b30	ECMPE030	ECM Pseudo Error Trigger 31	Generates a pseudo X short circuit abnormality detection error (error source 31). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b31	ECMPE031	ECM Pseudo Error Trigger 32	Generates a pseudo DOC operation error (error source 32). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.26 ECM Pseudo Error Trigger Register 1 (ECMPE1)

The ECMPE1 register is a control register that issues a pseudo error for self-diagnosis. When a pseudo error is issued, an interrupt set by ECM or an ECM reset occurs in the same way as when an actual error source occurs.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.
Bits 2 to 8 are trigger bits for extended pseudo errors. For details, see section 42.3.3, Pseudo Error Generation.

Address(es): A007 D0CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMPE108	ECMPE107	ECMPE106	ECMPE105	ECMPE104	ECMPE103	ECMPE102	ECMPE101	ECMPE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMPE100	ECM Pseudo Error Trigger 33	Generates a pseudo bus error (error source 33). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b1	ECMPE101	ECM Pseudo Error Trigger 34	Generates a pseudo timeout error caused by the external WAIT pin (error source 34). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b2	ECMPE102	ECM Pseudo Error Trigger 35	Generates a pseudo “extended pseudo error 35” (error source 35). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b3	ECMPE103	ECM Pseudo Error Trigger 36	Generates a pseudo “extended pseudo error 36” (error source 36). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b4	ECMPE104	ECM Pseudo Error Trigger 37	Generates a pseudo “extended pseudo error 37” (error source 37). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b5	ECMPE105	ECM Pseudo Error Trigger 38	Generates a pseudo “extended pseudo error 38” (error source 38). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b6	ECMPE106	ECM Pseudo Error Trigger 39	Generates a pseudo “extended pseudo error 39” (error source 39). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b7	ECMPE107	ECM Pseudo Error Trigger 40	Generates a pseudo “extended pseudo error 40” (error source 40). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b8	ECMPE108	ECM Pseudo Error Trigger 41	Generates a pseudo “extended pseudo error 41” (error source 41). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b31 to b9	—	Reserved	The write value should be 0.	W

42.2.27 ECM Pseudo Error Trigger Register 2 (ECMPE2)

The ECMPE2 register is a control register that issues a pseudo error for self-diagnosis. When a pseudo error is issued, an interrupt set by ECM or an ECM reset occurs in the same way as when an actual error source occurs.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	ECMPE229	ECMPE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	The write value should be 0.	W
b28	ECMPE228	ECM Pseudo Error Trigger 93	Generates a pseudo EMC error (error source 93). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b29	ECMPE229	ECM Pseudo Error Trigger 94	Generates a pseudo delay timer overflow (error source 94). 0: Pseudo error not generated 1: Generates corresponding pseudo error	W
b31, b30	—	Reserved	The write value should be 0.	W

42.2.28 ECM Delay Timer Control Register (ECMDTMCTL)

The ECMDTMCTL register controls the delay timer.
This register is a common register. Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTMSTACNTCLK	—	—	DTMSTP	DTMSTA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DTMSTA	Delay Timer Start	Sets the operation of the delay timer. 0: Delay timer operation disabled 1: Delay timer operation enabled	R/W
b1	DTMSTP	Delay Timer Stop	Writing 1 to this bit initializes the delay timer counter, causing the delay timer to stop. Simultaneously, the DTMSTA bit is set to 0.	W
b3, b2	—	Reserved	These bits are read as 0.	R
b4	DTMSTACNTCLK	Delay Timer Status	The value of the DTMSTA bit is applied to the operating status of the delay timer. If the DTMSTA bit is modified once, modifying the DTMSTA bit is disabled until the setting value of the DTMSTACNTCLK bit.	R
b7 to b5	—	Reserved	These bits are read as 0.	R

42.2.29 ECM Delay Timer Register (ECMDTMR)

The ECMDTMR register is a 16-bit counter register for the delay timer. The 16-bit counter counts up using ECMCLK (240 kHz). Changing the DTMSTA bit in the ECM delay timer control register from 1 (delay timer operation enabled) to 0 (delay timer operation disabled) initializes the 16-bit counter. This register can only be read.

Address(es): A007 D0D8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMTDMR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

42.2.30 ECM Delay Timer Compare Register (ECMDTMCMP)

The ECMDTMCMP register is a compare register used to set the overflow cycle of the delay timer. A delay timer overflow signal is generated to set the ECMmSSE229 bit when the value of this register matches with the value of the delay timer counter. Writing data to this register has to be conducted while the delay timer is stopped.
This register is a common register. Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.
Write this register after confirming that the read value of the CMPW bit is 0.

Address(es): A007 D0DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPW
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMDTMCMP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ECMDTMCMP [15:0]	Delay Timer Compare	Sets the overflow cycle of the delay timer. (overflow cycle) = (N + 1) × (ECMCLK cycle (240 kHz)) N: Set value For details, see section 42.3.5, Timeout Function for Interrupt Processing by Using the Delay Timer.	R/W
b16	CMPW	Compare Write	Indicates whether writing to the delay timer compare bit is enabled. Writing the compare value is possible when this bit is 0. 0: Writing to ECMDTMCMP[15:0] enabled 1: Writing to ECMDTMCMP[15:0] disabled	R
b31 to b17	—	Reserved	These bits are read as 0.	R

42.2.31 ECM Delay Timer Configuration Register 0 (ECMDTMCFG0)

The ECMDTMCFG0 register controls delay timer operation in response to an ECM maskable interrupt. Whether to enable delay timer operation when an ECM maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMTE031	ECMTE030	ECMTE029	—	ECMTE027	ECMTE026	ECMTE025	ECMTE024	ECMTE023	ECMTE022	ECMTE021	ECMTE020	ECMTE019	ECMTE018	ECMTE017	ECMTE016
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMTE015	ECMTE014	ECMTE013	ECMTE012	ECMTE011	ECMTE010	ECMTE009	ECMTE008	ECMTE007	ECMTE006	ECMTE005	ECMTE004	—	ECMTE002	ECMTE001	ECMTE000
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMTE000	ECM Delay Timer Start Control 1	Enables delay timer operation in response to an ECM maskable interrupt caused by a WDT overflow/refresh error (for Cortex-R4) (error source 1). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b1	ECMTE001	ECM Delay Timer Start Control 2	Enables delay timer operation in response to an ECM maskable interrupt caused by a WDT overflow/refresh error (for Cortex-M3) (error source 2).*1 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b2	ECMTE002	ECM Delay Timer Start Control 3	Enables delay timer operation in response to an ECM maskable interrupt caused by an IWDTa overflow/refresh error (error source 3). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMTE004	ECM Delay Timer Start Control 5	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b5	ECMTE005	ECM Delay Timer Start Control 6	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b6	ECMTE006	ECM Delay Timer Start Control 7	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b7	ECMTE007	ECM Delay Timer Start Control 8	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMTE008	ECM Delay Timer Start Control 9	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b9	ECMTE009	ECM Delay Timer Start Control 10	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b10	ECMTE010	ECM Delay Timer Start Control 11	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the ATCM (error source 11). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b11	ECMTE011	ECM Delay Timer Start Control 12	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the ATCM (error source 12). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b12	ECMTE012	ECM Delay Timer Start Control 13	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the BTCM (error source 13). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b13	ECMTE013	ECM Delay Timer Start Control 14	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the BTCM (error source 14). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b14	ECMTE014	ECM Delay Timer Start Control 15	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b15	ECMTE015	ECM Delay Timer Start Control 16	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b16	ECMTE016	ECM Delay Timer Start Control 17	Enables delay timer operation in response to an ECM maskable interrupt caused by a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b17	ECMTE017	ECM Delay Timer Start Control 18	Enables delay timer operation in response to an ECM maskable interrupt caused by a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b18	ECMTE018	ECM Delay Timer Start Control 19	Enables delay timer operation in response to an ECM maskable interrupt caused by an RSCAN overflow error (error source 19). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b19	ECMTE019	ECM Delay Timer Start Control 20	Enables delay timer operation in response to an ECM maskable interrupt caused by main clock oscillation stop detection (error source 20). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMTE020	ECM Delay Timer Start Control 21	Enables delay timer operation in response to an ECM maskable interrupt caused by CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b21	ECMTE021	ECM Delay Timer Start Control 22	Enables delay timer operation in response to an ECM maskable interrupt caused by CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b22	ECMTE022	ECM Delay Timer Start Control 23	Enables delay timer operation in response to an ECM maskable interrupt caused by CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b23	ECMTE023	ECM Delay Timer Start Control 24	Enables delay timer operation in response to an ECM maskable interrupt caused by a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b24	ECMTE024	ECM Delay Timer Start Control 25	Enables delay timer operation in response to an ECM maskable interrupt caused by a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b25	ECMTE025	ECM Delay Timer Start Control 26	Enables delay timer operation in response to an ECM maskable interrupt caused by a UVW overcurrent abnormality detection error (error source 26). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b26	ECMTE026	ECM Delay Timer Start Control 27	Enables delay timer operation in response to an ECM maskable interrupt caused by a UVW total current abnormality detection error (error source 27). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b27	ECMTE027	ECM Delay Timer Start Control 28	Enables delay timer operation in response to an ECM maskable interrupt caused by a UVW short circuit abnormality detection error (error source 28). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b28	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29	ECMTE029	ECM Delay Timer Start Control 30	Enables delay timer operation in response to an ECM maskable interrupt caused by an X overcurrent abnormality detection error (error source 30). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b30	ECMTE030	ECM Delay Timer Start Control 31	Enables delay timer operation in response to an ECM maskable interrupt caused by an X short circuit abnormality detection error (error source 31). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31	ECMTE031	ECM Delay Timer Start Control 32	Enables delay timer operation in response to an ECM maskable interrupt caused by a DOC operation error (error source 32). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.32 ECM Delay Timer Configuration Register 1 (ECMDTMCFG1)

The ECMDTMCFG1 register controls delay timer operation in response to an ECM maskable interrupt. Whether to enable delay timer operation when an ECM maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMTE108	ECMTE107	ECMTE106	ECMTE105	ECMTE104	ECMTE103	ECMTE102	ECMTE101	ECMTE100
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMTE100	ECM Delay Timer Start Control 33	Enables delay timer operation in response to an ECM maskable interrupt caused by a bus error (error source 33). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b1	ECMTE101	ECM Delay Timer Start Control 34	Enables delay timer operation in response to an ECM maskable interrupt caused by a timeout error caused by the external WAIT pin (error source 34). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b2	ECMTE102	ECM Delay Timer Start Control 35	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 35 (error source 35). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b3	ECMTE103	ECM Delay Timer Start Control 36	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 36 (error source 36). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b4	ECMTE104	ECM Delay Timer Start Control 37	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 37 (error source 37). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b5	ECMTE105	ECM Delay Timer Start Control 38	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 38 (error source 38). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b6	ECMTE106	ECM Delay Timer Start Control 39	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 39 (error source 39). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b7	ECMTE107	ECM Delay Timer Start Control 40	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 40 (error source 40). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b8	ECMTE108	ECM Delay Timer Start Control 41	Enables delay timer operation in response to an ECM maskable interrupt caused by extended pseudo error 41 (error source 41). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.33 ECM Delay Timer Configuration Register 2 (ECMDTMCFG2)

The ECMDTMCFG2 register controls delay timer operation in response to an ECM maskable interrupt. Whether to enable delay timer operation when an ECM maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ECMTE228	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ECMTE228	ECM Delay Timer Start Control 93	Enables delay timer operation in response to an ECM maskable interrupt caused by an ECM compare error (error source 93). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.34 ECM Delay Timer Configuration Register 3 (ECMDTMCFG3)

The ECMDTMCFG3 register controls delay timer operation in response to an ECM non-maskable interrupt. Whether to enable delay timer operation when an ECM non-maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ECMTE331	ECMTE330	ECMTE329	—	ECMTE327	ECMTE326	ECMTE325	ECMTE324	ECMTE323	ECMTE322	ECMTE321	ECMTE320	ECMTE319	ECMTE318	ECMTE317	ECMTE316
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMTE315	ECMTE314	ECMTE313	ECMTE312	ECMTE311	ECMTE310	ECMTE309	ECMTE308	ECMTE307	ECMTE306	ECMTE305	ECMTE304	—	ECMTE302	ECMTE301	ECMTE300
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMTE300	ECM Delay Timer Start Control 1	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a WDT overflow/ refresh error (for Cortex-R4) (error source 1). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b1	ECMTE301	ECM Delay Timer Start Control 2	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a WDT overflow/ refresh error (for Cortex-M3) (error source 2).*1 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b2	ECMTE302	ECM Delay Timer Start Control 3	Enables delay timer operation in response to an ECM non-maskable interrupt caused by an IWDTa overflow/ refresh error (error source 3). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ECMTE304	ECM Delay Timer Start Control 5	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Tag RAM) (error source 5). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b5	ECMTE305	ECM Delay Timer Start Control 6	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error (with correction) or 2-bit ECC error (without correction) in the instruction cache (Data RAM) (error source 6). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b6	ECMTE306	ECM Delay Timer Start Control 7	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the data cache (Tag/Dirty RAM) (error source 7). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b7	ECMTE307	ECM Delay Timer Start Control 8	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the data cache (Tag/Dirty RAM) (error source 8). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b8	ECMTE308	ECM Delay Timer Start Control 9	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the data cache (Data RAM) (error source 9). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b9	ECMTE309	ECM Delay Timer Start Control 10	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the data cache (Data RAM) (error source 10). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b10	ECMTE310	ECM Delay Timer Start Control 11	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the ATCM (error source 11). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b11	ECMTE311	ECM Delay Timer Start Control 12	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the ATCM (error source 12). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b12	ECMTE312	ECM Delay Timer Start Control 13	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the BTCM (error source 13). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b13	ECMTE313	ECM Delay Timer Start Control 14	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the BTCM (error source 14). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b14	ECMTE314	ECM Delay Timer Start Control 15	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the IRAM or DRAM (error source 15). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b15	ECMTE315	ECM Delay Timer Start Control 16	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the IRAM or DRAM (error source 16). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b16	ECMTE316	ECM Delay Timer Start Control 17	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 1-bit ECC error in the RSCAN RAM (error source 17). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b17	ECMTE317	ECM Delay Timer Start Control 18	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 2-bit ECC error in the RSCAN RAM (error source 18). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b18	ECMTE318	ECM Delay Timer Start Control 19	Enables delay timer operation in response to an ECM non-maskable interrupt caused by an RSCAN overflow error (error source 19). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b19	ECMTE319	ECM Delay Timer Start Control 20	Enables delay timer operation in response to an ECM non-maskable interrupt caused by main clock oscillation stop detection (error source 20). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b20	ECMTE320	ECM Delay Timer Start Control 21	Enables delay timer operation in response to an ECM non-maskable interrupt caused by CLMA0 oscillation stop detection (PLL0) (error source 21). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b21	ECMTE321	ECM Delay Timer Start Control 22	Enables delay timer operation in response to an ECM non-maskable interrupt caused by CLMA1 oscillation stop detection (PLL1) (error source 22). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b22	ECMTE322	ECM Delay Timer Start Control 23	Enables delay timer operation in response to an ECM non-maskable interrupt caused by CLMA2 oscillation stop detection (LOCO) (error source 23). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b23	ECMTE323	ECM Delay Timer Start Control 24	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 12-bit A/D converter unit 0 overwrite interrupt (error source 24). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b24	ECMTE324	ECM Delay Timer Start Control 25	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a 12-bit A/D converter unit 1 overwrite interrupt (error source 25). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b25	ECMTE325	ECM Delay Timer Start Control 26	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a UVW overcurrent abnormality detection error (error source 26). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b26	ECMTE326	ECM Delay Timer Start Control 27	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a UVW total current abnormality detection error (error source 27). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b27	ECMTE327	ECM Delay Timer Start Control 28	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a UVW short circuit abnormality detection error (error source 28). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b28	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29	ECMTE329	ECM Delay Timer Start Control 30	Enables delay timer operation in response to an ECM non-maskable interrupt caused by an X overcurrent abnormality detection error (error source 30). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b30	ECMTE330	ECM Delay Timer Start Control 31	Enables delay timer operation in response to an ECM non-maskable interrupt caused by an X short circuit abnormality detection error (error source 31). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31	ECMTE331	ECM Delay Timer Start Control 32	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a DOC operation error (error source 32). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Note 1. This bit is only supported in products incorporating an R-IN engine.
For products other than those incorporating an R-IN engine, do not change the value from the value after a reset.

42.2.35 ECM Delay Timer Configuration Register 4 (ECMDTMCFG4)

The ECMDTMCFG4 register controls delay timer operation in response to an ECM non-maskable interrupt. Whether to enable delay timer operation when an ECM non-maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECMTE408	ECMTE407	ECMTE406	ECMTE405	ECMTE404	ECMTE403	ECMTE402	ECMTE401	ECMTE400
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECMTE400	ECM Delay Timer Start Control 33	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a bus error (error source 33). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b1	ECMTE401	ECM Delay Timer Start Control 34	Enables delay timer operation in response to an ECM non-maskable interrupt caused by a timeout error caused by the external WAIT pin (error source 34). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b2	ECMTE402	ECM Delay Timer Start Control 35	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 35 (error source 35). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b3	ECMTE403	ECM Delay Timer Start Control 36	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 36 (error source 36). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b4	ECMTE404	ECM Delay Timer Start Control 37	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 37 (error source 37). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b5	ECMTE405	ECM Delay Timer Start Control 38	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 38 (error source 38). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b6	ECMTE406	ECM Delay Timer Start Control 39	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 39 (error source 39). 0: Delay timer start disabled 1: Delay timer start enabled	R/W

Bit	Symbol	Bit Name	Description	R/W
b7	ECMTE407	ECM Delay Timer Start Control 40	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 40 (error source 40). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b8	ECMTE408	ECM Delay Timer Start Control 41	Enables delay timer operation in response to an ECM non-maskable interrupt caused by extended pseudo error 41 (error source 41). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.36 ECM Delay Timer Configuration Register 5 (ECMDTMCFG5)

The ECMDTMCFG5 register controls delay timer operation in response to an ECM non-maskable interrupt. Whether to enable delay timer operation when an ECM non-maskable interrupt is generated can be set.
This register is a common register. Settings for both ECM master and ECM checker can be performed by writing to this register.
Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.

Address(es): A007 D0F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ECMTE528	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ECMTE528	ECM Delay Timer Start Control 93	Enables delay timer operation in response to an ECM non-maskable interrupt caused by an ECM compare error (error source 93). 0: Delay timer start disabled 1: Delay timer start enabled	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.2.37 ECM Error Output Clear Disable Configuration Register (ECMEOCCFG)

The ECMEOCCFG register controls the setting to disable clearing of an error output signal.
Clearing an error output signal by the ECMmECLR register (m = M or C) can be disabled until the value of the error output clear disable counter exceeds the value set in this register.
Setting to this register is possible only when no error source occurs.
This register is reset by the RES# pin reset only, and is not reset by other reset sources.
This register is a common register. Writing to this register is protected by the specific instruction sequence. For details, see section 42.3.4, Writing to Protected Registers.
Write this register after confirming that the read value from the CMPW bit is 1.

Address(es): A007 D0F8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPW
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ECMEOUTCLRT[15:0]															
Value after reset:	000h															

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ECMEOUTCLRT[15:0]	Error Output Signal Clear Disabled Period Setting	Sets the clear disabled period for an error output signal. (clear disabled period) = (N + 1) × (ECMCLK cycle (240 kHz)) N: Set value For details, see section 42.3.6, Setting of Disabling Error Output Clear.	R/W
b16	CMPW	Compare Write	Indicates that ECM is waiting for the operation of the control circuit for clearing an ECM error output to be stable after reset is released. Write this register after confirming that the read value is 0. 0: Operating stably 1: Waiting for stable operation	R
b31 to b17	—	Reserved	These bits are read as 0.	R

42.2.38 ECM Mask Control Register (ECMMCNT)

The ECMMCNT register is used for mask control for ECM compare errors (error source 93).

Address(es): A00B 0A80h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSKM	MSKC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	MSKC	ECM Compare Error Mask for Checker	Masks the ECM compare error source (error source 93) on the ECM checker. 0: ECM compare error not masked 1: ECM compare error masked	R/W
b1	MSKM	ECM Compare Error Mask for Master	Masks the ECM compare error source (error source 93) on the ECM master. 0: ECM compare error not masked 1: ECM compare error masked	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

42.3 Operations

42.3.1 Operations for Error Output

There are two output modes (non-dynamic and dynamic) for the ERROROUT# pin when an error source occurs.
In non-dynamic mode, the ERROROUT# pin outputs the high level when an error is not detected.
In dynamic mode, the ERROROUT# pin can output a toggle waveform according to the compare match timer W (CMTW) when an error is not detected.
In both modes, the ERROROUT# pin outputs the low level when an error is detected.

Operating Mode	Error Status	ERROROUT# Pin Output Level
Non-dynamic (ECMEPCFG.ECMSL0 bit = 0)	No error*1	High
	Error	Low
Dynamic (ECMEPCFG.ECMSL0 bit = 1)	No error*1	Toggles (according to CMTW input)
	Error	Low

Note 1. After reset is released, the ERROROUT# pin outputs the low level (error status).
Use this pin after clearing the error status according to the procedure described in the note in section 42.2.2.

42.3.1.1 Dynamic Mode Enable

1. Initialize the compare match timer W (CMTW) for the input signal for toggle output. The output compare signal for toggle output can be selected by the ECDMESLR register.
   For details on the CMTW setting, see section 25, Compare Match Timer W (CMTW).
2. Set the output of the ERROROUT# pin to the high level (no error) by setting the ECMmECT bit (m = M or C) of the ECM master/checker error clear trigger register to 1.
3. Set the ECMSL0 bit in the ECM error pulse configuration register (ECMPCFG) to 1 to specify dynamic mode.
4. Start up the CMTW.

42.3.1.2 Dynamic Mode Disable

1. Set the output of the ERROROUT# pin to the low level by setting the ECMmEST bit (m = M or C) in the ECM master/checker error set trigger register to 1.
2. Stop the CMTW operation.
3. Clear the ECMSL0 bit in the ECM error pulse configuration register (ECMPCFG) to 0 to specify non-dynamic mode.

42.3.2 Loop-Back Function

ECM incorporates a loop-back function that is used to check the path for an error output signal from the ECM module to the ERROROUT# pin. The output level of the ERROROUT# pin can be checked with the ECMmSSE231 bit (m = M or C) in the ECM master/checker error source status register 1.

42.3.3 Pseudo Error Generation

ECM can generate individual pseudo error sources for self-diagnosis. ECM generates a pseudo error when the corresponding bit in the ECM pseudo error trigger register (ECMPEn) is set to 1. When a pseudo error is generated, ECM operates in the same way as when a real error occurs, and the settings for error source mask, ECM interrupt, ECM reset, and delay timer all apply in the same way.
Error sources 35 to 41 can be used as extended pseudo errors to detect errors for functional safety as shown below. When software detects an error, it can set a bit in the ECMPEn register to generate a corresponding pseudo error to use a function such as ECM interrupt, ECM reset, or delay timer.

Table 42.3 Example Assignment of Errors for Functional Safety to Error Sources

Error Source Number	Example Functions to be Assigned to Extended Pseudo Errors 35 to 41
35	Access violation to the Cortex-R4 protected area
36	Access violation to the Cortex-M3 protected area (only for products incorporating an R-IN engine)
37	PWM cycle/Duty error
38	ADC unit 0 range over error
39	ADC unit 1 range over error
40	ADC unit 0 pin-level self-diagnosis error
41	ADC unit 1 pin-level self-diagnosis error

42.3.4 Writing to Protected Registers

Write protected registers are protected from incorrect write access due to erroneous program execution, etc.

42.3.4.1 Protection Unlock Sequence

Write access to a write protected register is only possible within the following sequence.

1. Write the fixed value 0000 00A5h to the ECM protection command register (ECMPCMD1) or the ECM master/checker protection command register (ECMmPCMD0) (m = M or C). If the register to be written is the common register, write the fixed value to the ECM protection command register (ECMPCMD1). If the register to be written is not the common register, write the fixed value to the ECM master/checker protection command register (ECMmPCMD0). See descriptions of each register in section 42.2, Registers, to find out whether the target register is a common one or not.
2. Write the desired setting value to the protected, of the ECM common, ECM master, and ECM checker according to the following sequence:
   - Write the desired setting value.
   - Write the inversed value of the desired setting value.
   - Write the desired setting value again.
3. Check the desired setting value has been successfully written to the protected register by checking that the ECMPRERR bit of the ECM protection status register (ECMPS) is 0.

In case of any access to another register between step 1 to step 3 of the above sequence, the protection mechanism behaves as follows.

- If that register belongs to the ECM, the write to the protected register fails (the ECMPRERR bit of the ECM protection status register becomes 1). The sequence has to be reexecuted from step 1.
- If that register does not belong to the ECM, the sequence is not disrupted and the write to the protected register is conducted successfully.

In case the protection unlock sequence is interrupted, the protection mechanism behaves as follows.

- Interrupts during protection sequence
  If an interrupt is acknowledged within the protection sequence and the interrupt process does not access any ECM register, the protection sequence is not disrupted and the write to the protected register can be successfully completed after returning from the interrupt process.

In case a break occurs in the protection unlock sequence, the protection mechanism behaves as follows.

- Breaks during protection sequence
  If the CPU goes into the break state during the protection sequence and any ECM register is not accessed, the protection sequence is not disrupted and the write to the protected register can be successfully completed after returning from the break.
  If the CPU goes into the break state during the protection sequence and any ECM register is accessed, the protection sequence is disrupted and the write to the protected register is not performed after returning from the break. Therefore, be careful not to let the CPU go into the break state during the protection sequence.

42.3.5 Timeout Function for Interrupt Processing by Using the Delay Timer

ECM can start the delay timer at the same time as an ECM maskable or non-maskable interrupt request due to occurrence of an error source is issued, to manage timeout of the interrupt processing time. If ECM cannot stop the delay timer (by setting the ECMDTMCTL.DTMSTP bit to 1) during interrupt processing and the count value of the delay timer matches with the value of the delay timer compare register, ECM can generate a delay timer overflow (error source 94), and an error signal output on the ERROROUT# pin or ECM reset. Specify the settings of the error signal output and ECM reset when the delay timer overflow (error source 94) occurs in the ECMEMK2 and ECMIRCFG2 registers, respectively.
The delay timer always starts counting up from 0 by using ECMCLK (240 kHz).
Specify the setting of the overflow cycle of the delay timer in the ECMDTMCMP register.

(Overflow cycle) = (Value set in ECMDTMCMP. ECMDTMCMP[15:0] + 1) × ECMCLK cycle (240 kHz)

Note: The delay timer continues count operation even when a break occurs.

42.3.6 Setting of Disabling Error Output Clear

ECM has a function that disables clearing (by the ECMmECLR register (m = M or C)) of an error signal output from the ERROROUT# pin when an error occurs. An error output signal is disabled during the specified period. This period can be specified in the ECMEOCCFG register.
When an error source occurs, the error output clear disable counter starts counting up by using the ECMCLK clock (240 kHz). Clear processing by the ECMmECLR register for an error output is disabled until the counter value matches with the value set in ECMEOCCFG.ECMEOUTCLRT[15:0]. After the counter value exceeds the set value, clearing of an error output is possible.

(Error output clear disabled period) = (ECMEOUTCLRT[15:0] + 1) × ECMCLK cycle (240 kHz)

If another error source occurs while the error output clear disable counter is in count operation, the counter is cleared and restarts counting up. If the same error source occurs again, the counter is not cleared and continues counting up.

Note: The error output disable counter continues count operation even when a break occurs.

42.4 Usage Notes

42.4.1 Notes Regarding ECMCLK

Counting by the delay timer and by the counter to disable clearing of the error output is of cycles of ECMCKL, a signal generated by the low-speed on-chip oscillator.
After release from the reset state, counting does not proceed or the error output is not cleared if the delay timer is started while the low-speed on-chip oscillator is stopped.
To enable the delay timer function and error output, enable the low-speed on-chip oscillator beforehand and wait for the LOCO oscillation stabilization time.
For details on the low-speed on-chip oscillator, see section 7.2.6, Low-Speed On-Chip Oscillator Control Register (LOCOCR).

43. 12-Bit A/D Converter (S12ADCa)

43.1 Overview

This LSI incorporates two units of a 12-bit successive approximation A/D converter. In unit 0, up to eight analog input channels and temperature sensor output are selectable. In unit 1, up to 16 analog input channels and extended analog input are selectable.

The 12-bit A/D converter converts a maximum of 8 analog input channels and temperature sensor output (unit 0) and a maximum of 16 analog input channels (unit 1), which have been selected, into a 12-bit digital value through successive approximation.

The A/D converter has three operating modes: single scan mode in which the analog inputs of up to 8 (unit 0) and 16 (unit 1) channels arbitrarily selected are converted for only once in ascending channel order; continuous scan mode in which the analog inputs of up to 8 (unit 0) and 16 (unit 1) channels arbitrarily selected are continuously converted in ascending channel order; and group scan mode in which up to 8 (unit 0) and 16 (unit 1) channels of the analog inputs are arbitrarily divided into two groups (group A and group B) and converted in ascending channel order in each group.

In group scan mode, the conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. When group A priority control is selected along with operation as described above, if a request to start scanning for group A is received during A/D conversion for group B, the conversion operation for group B is discontinued and the conversion for group A starts, which is given priority.

In double trigger mode, one analog input channel arbitrarily selected is converted in single scan mode or group scan mode (group A), and the resulting data of A/D conversion started by the first and second synchronous triggers are stored into different registers (duplication of A/D conversion data).

The temperature sensor output can be selected at the same time as the analog input of channels. A/D conversion of the analog input of channels and the temperature sensor output is performed in that order.

A/D conversion of the extended analog input is independently performed.

Self-diagnosis, pin-level self-diagnosis, detection of guidewire malfunction, overwrite checking of data registers, and automatic clearing of data registers are provided as security functions.

Table 43.1 lists the specifications of the 12-bit A/D converter and Table 43.2 indicates the functions of the 12-bit A/D converter. Figure 43.1 shows a block diagram of the 12-bit A/D converter (unit 0) and Figure 43.2 shows a block diagram of the 12-bit A/D converter (unit 1).

Table 43.1 Specifications of 12-Bit A/D Converter (1 / 2)

Item	Specifications
Number of units	Two units
Input channels	Unit 0: Up to 8 channels Unit 1: Up to 16 channels + one extended*1
Extended analog function	Temperature sensor output, extended input
A/D conversion method	Successive approximation method
Resolution	12 bits
Conversion time	Unit 0: 0.483 µs per channel (when A/D conversion clock ADCLK = 60 MHz) Unit 1: 0.833 µs per channel*1 (when A/D conversion clock ADCLK = 60 MHz)
A/D conversion clock	Peripheral module clock PCLKH and A/D conversion clock ADCLK (PCLKF or PCLKG)*2 can be set so that the frequency division ratio should be one of the following. PCLKH to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8 ADCLK is set using the clock generation circuit.
Data registers	• 24 registers for analog input (8 for unit 0 and 16 for unit 1), 1 for A/D-converted data duplication in double trigger mode in each unit, and 2 for A/D-converted data duplication during extended operation in double trigger mode in each unit • One register for temperature sensor output (in unit 0 only) • One register for self-diagnosis (per unit) • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes*3	• Single scan mode: A/D conversion is performed only once on the analog inputs of up to 8 (unit 0) and 16 (unit 1) channels arbitrarily selected and on the temperature sensor output (in unit 0 only). A/D conversion is performed only once on the extended analog input (in unit 1 only). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 8 (unit 0) and 16 (unit 1) channels arbitrarily selected and on the temperature sensor output (in unit 0 only). A/D conversion is performed repeatedly on the extended analog input (in unit 1 only). • Group scan mode: Analog inputs of up to 8 (unit 0) and 16 (unit 1) channels arbitrarily selected and the temperature sensor output (in unit 0 only) are divided into group A and group B, and A/D conversion of the selected analog input is performed only once on a group basis. The conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. Restarting (rescanning) for A/D conversion on group B after completion of A/D conversion on group A can only be set when the ratio between the frequency division settings for PCLKH and ADCLK = 1:1.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU3a), the general-purpose PWM timer (GPTa), the event link controller (ELC), and 16-bit timer pulse unit (TPUa). • Asynchronous trigger A/D conversion can be triggered by the external trigger pins, ADTRG0 (unit 0) and ADTRG1 (unit 1).

Table 43.1 Specifications of 12-Bit A/D Converter (2 / 2)

Item	Specifications
Function	• Sample-and-hold function • Channel-dedicated sample-and-hold function (4ch: in unit 0 only) • Variable sampling state count (which can be set for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (Precharge function/discharge function) • Double trigger mode (duplication of A/D conversion data) • Switching function of 8-, 10-, and 12-bit conversion*4 • Automatic clear function of A/D data registers • Extended analog input function*3 • Compare Function (which compares the compare register and data register) • Pin-level self-diagnosis function • Overwrite checking function of the A/D data register
Interrupt source	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt (S12ADI) request can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt (S12ADI) request can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt (S12ADI) request can be generated on completion of group A scan, whereas an A/D scan end interrupt for group B (S12GBADI) request can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt (S12ADI) request can be generated on completion of double scan of group A, whereas A/D scan end interrupt specially for group B (S12GBADI) request can be generated on completion of group B scan. • A compare interrupt (S12CMPI) can be generated in response to the results of detection using compare function. • An AD error interrupt request (S12ADE) can be generated by an error in overwrite checking for data register. • The S12ADI or S12GBADI interrupt can activate the DMA controller (DMAC).
Event link (ELC) function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • Scan can be started by a trigger output by ELC.
Low-power consumption function	• Module-stop state can be specified.*5

Note 1. One unit for 176-pin devices (only unit 0 is provided)
Note 2. Peripheral module clock PCLKH is fixed to 60 MHz. A/D conversion clock ADCLK is set according to the setting of the SCKCR.PCKF[1:0] bits and the SCKCR.PCKG[1:0] bits in unit 0 and unit 1, respectively.
Note 3. When the extended analog input is selected, do not use group scan mode.
Note 4. When A/D conversion accuracy is modified, A/D conversion time is also changed. See section 43.3.7 Analog Input Sampling and Scan Conversion Time, for details.
Note 5. See section 9, Low-Power Consumption Function, for details.

Table 43.2 Functions of 12-Bit A/D Converter (1 / 2)

Item			Unit 0 (S12ADC0)	Unit 1 (S12ADC1)
Analog input channel			AN000 to AN007 Temperature sensor output	AN100 to AN115 Extended input
Conditions for A/D conversion start	Software	Software trigger	Enabled	Enabled
	External trigger	Trigger input pin	ADTRG0	ADTRG1
	Synchronous trigger (trigger from MTU3a)	Compare match with or input capture to MTU0.TGRA	TRGA0N	TRGA0N
		Compare match with or input capture to MTU1.TGRA	TRGA1N	TRGA1N
		Compare match with or input capture to MTU2.TGRA	TRGA2N	TRGA2N
		Compare match with or input capture to MTU3.TGRA	TRGA3N	TRGA3N
		Compare match with or input capture to MTU4.TGRA or underflow (trough) of MTU4.TCNT in complementary PWM mode	TRGA4N	TRGA4N
		Compare match with or input capture to MTU6.TGRA	TRGA6N	TRGA6N
		Compare match with or input capture to MTU7.TGRA or underflow (trough) of MTU7.TCNT in complementary PWM mode	TRGA7N	TRGA7N
		Compare match with MTU0.TGRE	TRG0N	TRG0N
		Compare match between MTU4.TADCORA and MTU4.TCNT	TRG4AN	TRG4AN
		Compare match between MTU4.TADCORB and MTU4.TCNT	TRG4BN	TRG4BN
		Compare match between MTU4.TADCORA and MTU4.TCNT or compare match between MTU4.TADCORB and MTU4.TCNT	TRG4AN or TRG4BN	TRG4AN or TRG4BN
		Compare match between MTU4.TADCORA and MTU4.TCNT and compare match between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is used)	TRG4ABN	TRG4ABN
		Compare match between MTU7.TADCORA and MTU7.TCNT	TRG7AN	TRG7AN
		Compare match between MTU7.TADCORB and MTU7.TCNT	TRG7BN	TRG7BN
		Compare match between MTU7.TADCORA and MTU7.TCNT or compare match between MTU7.TADCORB and MTU7.TCNT	TRG7AN or TRG7BN	TRG7AN or TRG7BN
		Compare match between MTU7.TADCORA and MTU7.TCNT and compare match between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is used)	TRG7ABN	TRG7ABN
	Synchronous trigger (trigger from GPTa)	Compare match with GTP0.GTADTRA	GTADTRA0N	GTADTRA0N
		Compare match with GPT0.GTADTRB	GTADTRB0N	GTADTRB0N
		Compare match with GPT1.GTADTRA	GTADTRA1N	GTADTRA1N
		Compare match with GPT1.GTADTRB	GTADTRB1N	GTADTRB1N
		Compare match with GPT2.GTADTRA	GTADTRA2N	GTADTRA2N
		Compare match with GPT2.GTADTRB	GTADTRB2N	GTADTRB2N
		Compare match with GPT3.GTADTRA	GTADTRA3N	GTADTRA3N
		Compare match with GPT3.GTADTRB	GTADTRB3N	GTADTRB3N
		Compare match with GTP0.GTADTRA or compare match with GTP0.GTADTRB	GTADTRA0N or GTADTRB0N	GTADTRA0N or GTADTRB0N
		Compare match with GTP1.GTADTRA or compare match with GTP1.GTADTRB	GTADTRA1N or GTADTRB1N	GTADTRA1N or GTADTRB1N
		Compare match with GTP2.GTADTRA or compare match with GTP2.GTADTRB	GTADTRA2N or GTADTRB2N	GTADTRA2N or GTADTRB2N
		Compare match with GTP3.GTADTRA or compare match with GTP3.GTADTRB	GTADTRA3N or GTADTRB3N	GTADTRA3N or GTADTRB3N

Table 43.2 Functions of 12-Bit A/D Converter (2 / 2)

Item			Unit 0 (S12ADC0)	Unit 1 (S12ADC1)
Conditions for A/D conversion start	Synchronous trigger (trigger from TPUa)*1	Compare match with or input capture to TPU0.TGRA, compare match with or input capture to TPU1.TGRA, compare match with or input capture to TPU2.TGRA, compare match with or input capture to TPU3.TGRA, or compare match with or input capture to TPU4.TGRA.	TPTRGAN_0	TPTRGAN_0
		Compare match with or input capture to TPU0.TGRA	TPTRG0AN_0	TPTRG0AN_0
		Compare match with or input capture to TPU6.TGRA, compare match with or input capture to TPU7.TGRA, compare match with or input capture to TPU8.TGRA, compare match with or input capture to TPU9.TGRA, or compare match with or input capture to TPU10.TGRA.	TPTRGAN_1	TPTRGAN_1
		Compare match with or input capture to TPU6.TGRA	TPTRG6AN_1	TPTRG6AN_1
	Synchronous trigger (trigger from ELC)	ELC trigger	ELCTRG0	ELCTRG1
Channel-dedicated sample-and-hold function	Target channel		AN000 to AN003	—
Interrupt	Interrupt request to the CPU		S12ADI0 S12GBADI0 S12CMPI0 S12ADE0	S12ADI1 S12GBADI1 S12CMPI1 S12ADE1
	Start request to DMAC		S12ADI0 S12GBADI0	S12ADI1 S12GBADI1
	Event output to ELC		S12ADI0	S12ADI1
Setting of module stop function*2, *3			MSTPCRC.MSTPCRC5 bit	MSTPCRC.MSTPCRC4 bit

Note 1. “0” and “1” added to synchronous triggers indicate the number of unit. For the settings to output synchronous triggers, see the sections related to A/D converter startup of the responding modules.
Note 2. See section 9, Low-Power Consumption Function for details.
Note 3. Wait for 1 µs or longer to start A/D conversion after release from the module-stop state.

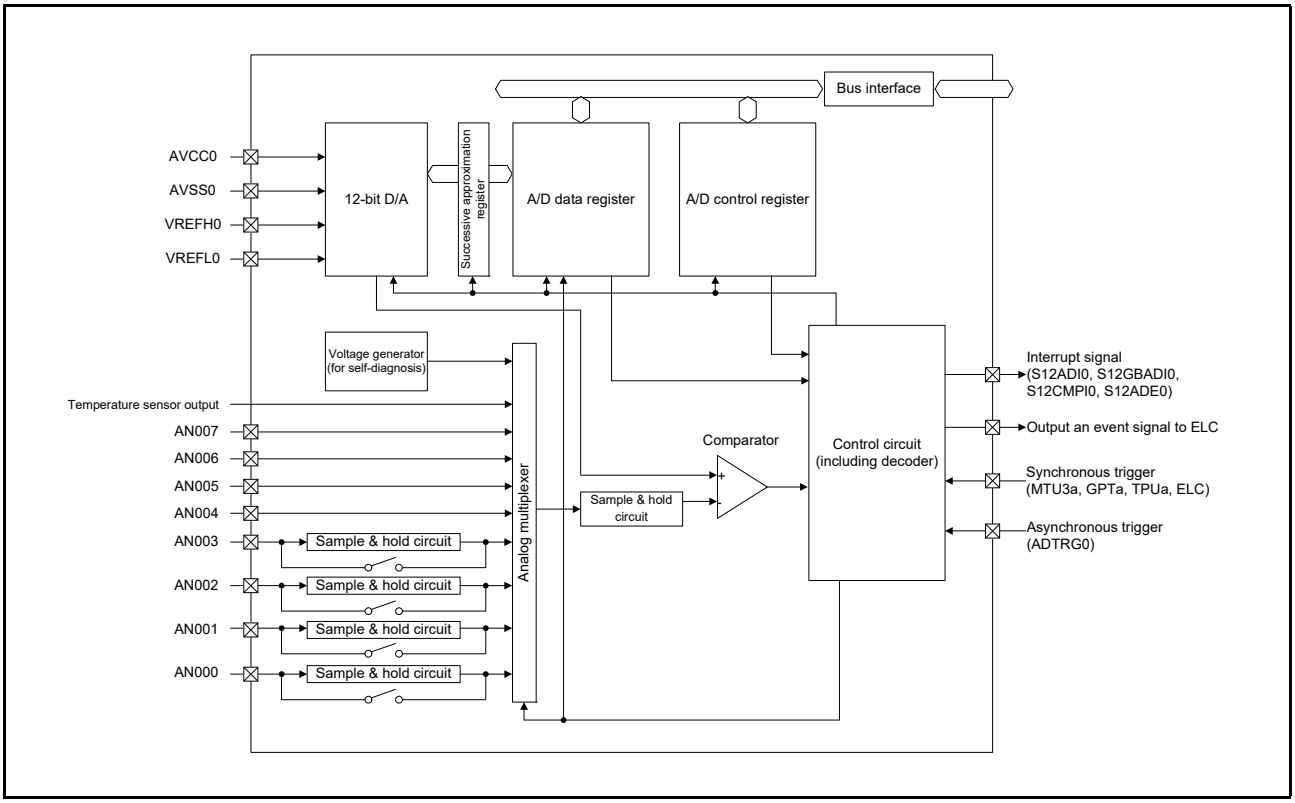


Figure 43.1 Block Diagram of 12-Bit A/D Converter (Unit 0)

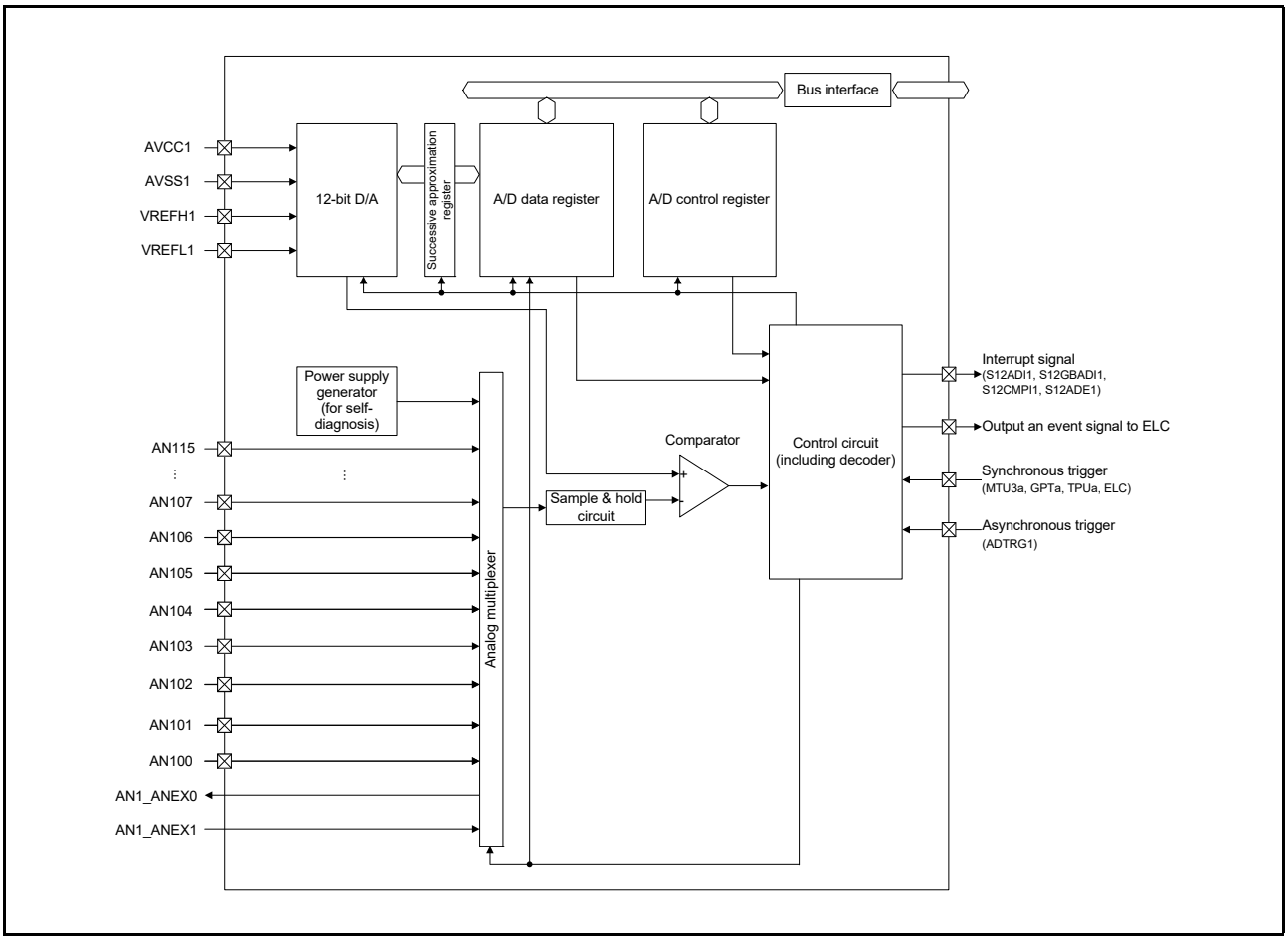


Figure 43.2 Block Diagram of 12-Bit A/D Converter (Unit 1)

Table 43.3 lists the I/O pins of the 12-bit A/D converter.

Table 43.3 I/O Pins of 12-Bit A/D Converter

Unit	Pin Name	I/O	Function
Unit 0	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	AN000 to AN007	Input	Analog input pins 0 to 7
	ADTRG0	Input	External trigger input pin for starting A/D conversion
Unit 1	AVCC1	Input	Analog block power supply pin
	AVSS1	Input	Analog block ground pin
	VREFH1	Input	Analog block power supply pin
	VREFL1	Input	Analog block ground pin
	AN100 to AN115	Input	Analog input pins 8 to 23
	AN1_ANEX0	Output	Extended analog output pin
	AN1_ANEX1	Input	Extended analog input pin
	ADTRG1	Input	External trigger input pin for starting A/D conversion

43.2 Register Descriptions

43.2.1 A/D Data Registers y (ADDRy), A/D Data Duplication Register (ADDBLDR), A/D Data Duplication Register A (ADDBLDRA), A/D Data Duplication Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR)

The ADDRy registers (y = 0 to 7 in unit 0; y = 0 to 15 in unit 1) are 16-bit read-only registers for storing the result of A/D conversion. Register ADDBLDR is a 16-bit read-only register for storing the result of A/D conversion in response to the second trigger in double trigger mode. Registers ADDBLDRA and ADDBLDRB are 16-bit read-only registers for storing the result of A/D conversion during extended operation in double trigger mode. Register ADTSDR is a 16-bit read-only register for storing the A/D conversion result of temperature sensor output.
The formats for data in the ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, and ADTSDR registers vary according to the following conditions.

- The setting of the A/D data register format select bit (ADCER.ADRFT) (determining whether the data are flush-left or flush-right in the registers)
- The setting of the A/D conversion-accuracy selection bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit is selectable.)
- The setting of the addition frequency select bits (ADADC.ADC[1:0]) (once, twice, three times, or four times is selectable.)
- The setting of the average mode enable bit (ADADC.AVEE) (Addition or average is selectable.)

The data formats for each given condition are shown below.

(1) When A/D-converted value addition/average mode is not selected

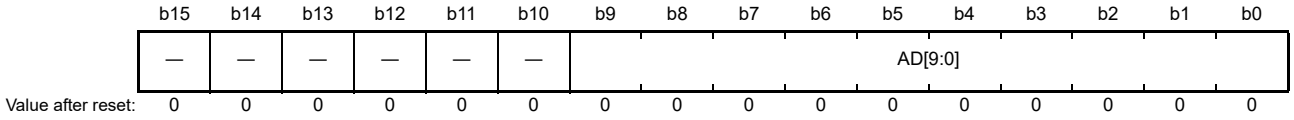
- The settings for flush-right data with 12-bit accuracy

Address(es): S12ADC0.ADDBLDR A008 C018h, S12ADC0.ADTSDR A008 C01Ah, S12ADC0.ADDR0 A008 C020h, S12ADC0.ADDR1 A008 C022h, S12ADC0.ADDR2 A008 C024h, S12ADC0.ADDR3 A008 C026h, S12ADC0.ADDR4 A008 C028h, S12ADC0.ADDR5 A008 C02Ah, S12ADC0.ADDR6 A008 C02Ch, S12ADC0.ADDR7 A008 C02Eh, S12ADC0.ADDBLDRA A008 C084h, S12ADC0.ADDBLDRB A008 C086h S12ADC1.ADDBLDR A008 C418h, S12ADC1.ADDR0 A008 C420h, S12ADC1.ADDR1 A008 C422h, S12ADC1.ADDR2 A008 C424h, S12ADC1.ADDR3 A008 C426h, S12ADC1.ADDR4 A008 C428h, S12ADC1.ADDR5 A008 C42Ah, S12ADC1.ADDR6 A008 C42Ch, S12ADC1.ADDR7 A008 C42Eh, S12ADC1.ADDR8 A008 C430h, S12ADC1.ADDR9 A008 C432h, S12ADC1.ADDR10 A008 C434h, S12ADC1.ADDR11 A008 C436h, S12ADC1.ADDR12 A008 C438h, S12ADC1.ADDR13 A008 C43Ah, S12ADC1.ADDR14 A008 C43Ch, S12ADC1.ADDR15 A008 C43Eh, S12ADC1.ADDBLDRA A008 C484h, S12ADC1.ADDBLDRB A008 C486h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

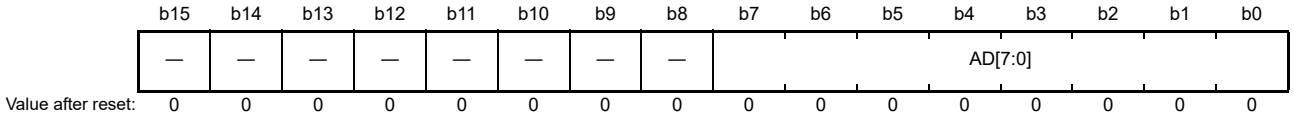
Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b15 to b12	—	Reserved	These bits are read as 0.	R

- The settings for flush-right data with 10-bit accuracy



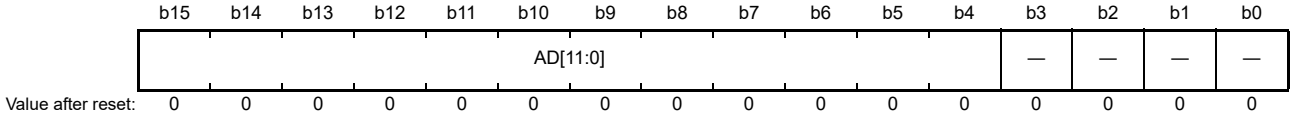
Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R
b15 to b10	—	Reserved	These bits are read as 0.	R

- The settings for flush-right data with 8-bit accuracy



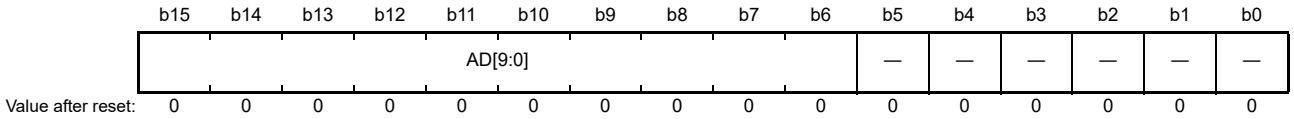
Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R
b15 to b8	—	Reserved	These bits are read as 0.	R

- The settings for flush-left data with 12-bit accuracy



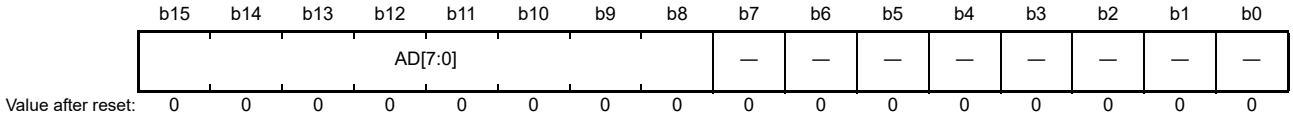
Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

- The settings for flush-left data with 10-bit accuracy



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R

- The settings for flush-left data with 8-bit accuracy



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0.	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R

(2) When A/D-converted value average mode is selected

When A/D-converted value average mode is selected, the AD[11:0] bits indicate the mean of A/D-converted values on a specific channel. Even if A/D-converted value average mode is selected, the value is stored in the A/D data register according to the settings of the A/D data register format select bit in the same way as normal A/D conversion.

(3) When A/D-converted value addition mode is selected

When A/D-converted value addition mode is selected, the AD[13:0] bits indicate the value that is obtained by adding up A/D-converted values on a specific channel. In A/D-converted value addition mode, the value obtained by adding up of A/D conversion results is retained in the A/D data register as a 2-bit-extended value of the conversion accuracy specified. Even if A/D-converted value addition mode is selected, the value is stored in the A/D data register according to the settings of the A/D data register format select bits.
The data formats for each given condition are shown below.

- The settings for flush-right data with 12-bit accuracy (when A/D-converted value addition mode is selected)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AD[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b13 to b0	AD[13:0]	Added Value 13 to 0	14-bit value obtained by adding up of A/D conversion results	R
b15, b14	—	Reserved	These bits are read as 0.	R

- The settings for flush-right data with 10-bit accuracy (when A/D-converted value addition mode is selected)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	Added Value 11 to 0	12-bit value obtained by adding up of A/D conversion results	R
b15 to b12	—	Reserved	These bits are read as 0.	R

- The settings for flush-right data with 8-bit accuracy (when A/D-converted value addition mode is selected)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

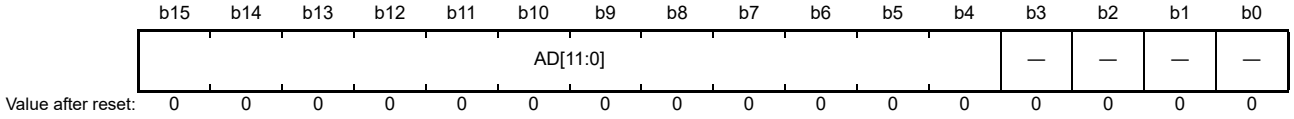
Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[9:0]	Added Value 9 to 0	10-bit value obtained by adding up of A/D conversion results	R
b15 to b10	—	Reserved	These bits are read as 0.	R

- The settings for flush-left data with 12-bit accuracy (when A/D-converted value addition mode is selected)



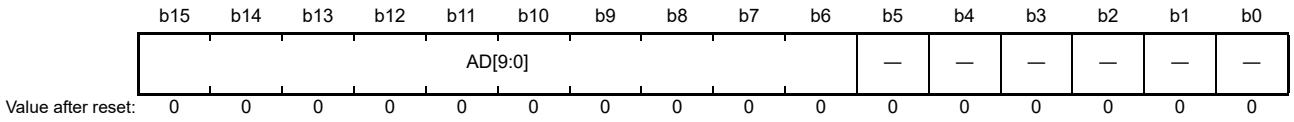
Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0.	R
b15 to b2	AD[13:0]	Added Value 13 to 0	14-bit value obtained by adding up of A/D conversion results	R

- The settings for flush-left data with 10-bit accuracy (when A/D-converted value addition mode is selected)



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Added Value 11 to 0	12-bit value obtained by adding up of A/D conversion results	R

- The settings for flush-left data with 8-bit accuracy (when A/D-converted value addition mode is selected)



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Added Value 9 to 0	10-bit value obtained by adding up of A/D conversion results	R

43.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the 12-bit A/D converter's self-diagnosis. In addition to the AD bit indicating A/D-converted value, the self-diagnosis status bit (DIAGST) is included in. In the ADRD register, the following different formats are used depending on the conditions below.

- The setting of the A/D data register format select bit (ADCER.ADRFT) (determining whether the data are flush-left or flush-right in the registers)
- The setting of the A/D conversion-accuracy selection bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit is selectable.)

The A/D-converted value addition mode and A/D-converted value average mode cannot be applied to the A/D self-diagnosis function. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER). The data formats for each given condition are shown below.

- The settings for flush-right data with 12-bit accuracy

Address(es): S12ADC0.ADRD A008 C01Eh, S12ADC1.ADRD A008 C41Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R
b13, b12	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R

Note 1. "Reference voltage" refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

- The settings for flush-right data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R
b13 to b10	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

- The settings for flush-right data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	—	—	—	—	AD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R
b13 to b8	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

- The settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

- The settings for flush-left data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R
b5 to b2	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value	R

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

- The settings for flush-left data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis has never been executed since power-on. 0 1: Self-diagnosis using the voltage of 0 V has been executed. 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 has been executed. 1 1: Self-diagnosis using the voltage of reference power supply*1 has been executed. For details of self-diagnosis, see section 43.2.8 A/D Control Extended Register (ADCER).	R
b7 to b2	—	Reserved	These bits are read as 0.	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

43.2.3 A/D Control Register (ADCSR)

ADCSR sets double trigger mode, A/D conversion start trigger; enables or disables scan end interrupt; selects the scan mode; and starts or stops A/D conversion.

Address(es): S12ADC0.ADCSR A008 C000h, S12ADC1.ADCSR A008 C400h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]		ADIE	—	—	TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double triggered operation. The setting is only effective while double trigger mode is selected.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt Enable	0: Disables S12GBADI interrupt generation upon group B scan completion. 1: Enables S12GBADI interrupt generation upon group B scan completion.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselects double trigger mode. 1: Selects double trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: A/D conversion is started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC). 1: A/D conversion is started by the asynchronous trigger (ADTRG0 in unit 0; ADTRG1 in unit 1).	R/W
b9	TRGE	Trigger Start Enable	0: Disables A/D conversion to be started by the synchronous or asynchronous trigger. 1: Enables A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ADIE	Scan End Interrupt Enable	0: Disables S12ADI interrupt generation upon scan completion. 1: Enables S12ADI interrupt generation upon scan completion.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited	R/W
b15	ADST	A/D Conversion Start	0: Stops A/D conversion process. 1: Starts A/D conversion process.	R/W

Note 1. Starting A/D conversion using an external pin (asynchronous trigger)
After a low-level signal is input to the external pin (ADTRG0 in unit 0; ADTRG1 in unit 1), write 1 to both the TRGE and EXTRG bits in ADCSR and change the signals of ADTRG0 in unit 0 and ADTRG1 in unit 1 to the high level. Thus the rising edge of ADTRG0 in unit 0 and ADTRG1 in unit 1 are detected and the scan conversion process is started. In this case, the pulse width of the high-level input must be at least 1.5 clock cycles of PCLK.

DBLANS[4:0] Bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double trigger mode. The A/D conversion results of the analog input of the channel selected by the DBLANS[4:0] bits are stored into the A/D data register y when conversion is started by the first trigger in double trigger mode, and into the A/D data duplication register when started by the second trigger. Table 43.4 shows selection of the channel for double triggered operation.
When double trigger mode is selected, the channels selected by the ADANSA register are invalid, and the channel selected by the DBLANS[4:0] bits is subjected to A/D conversion instead.
When double trigger mode is used, do not select A/D conversion for the temperature sensor output and extended analog input. The DBLANS[4:0] bits should be set while the ADST bit is 0. (They should not be set simultaneously when 1 is written to the ADST bit.)
To use A/D-converted value addition/average mode while double trigger mode is set, the channel selected by the DBLANS[4:0] bits should be selected in the ADANSA register.

Table 43.4 Relationship between DBLANS Bit Settings and Double Trigger Enabled Channels

Unit 0		Unit 1			
DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
00000	AN000	00000	AN100	01000	AN108
00001	AN001	00001	AN101	01001	AN109
00010	AN002	00010	AN102	01010	AN110
00011	AN003	00011	AN103	01011	AN111
00100	AN004	00100	AN104	01100	AN112
00101	AN005	00101	AN105	01101	AN113
00110	AN006	00110	AN106	01110	AN114
00111	AN007	00111	AN107	01111	AN115

Note: Settings other than above are prohibited.

GBADIE Bit (Group B Scan End Interrupt Enable)

The GBADIE bit sets whether to enable or disable group B scan end interrupt (S12GBADI) in group scan mode.

DBLE Bit (Double Trigger Mode Select)

Double trigger mode has a function to store the resulting data of A/D conversion started by the first and second synchronous triggers into separate registers.
When double trigger mode is selected, the channels specified in the ADANS register are invalid and the channel selected by the DBLANS[4:0] bits is effective instead. Double trigger mode is only operated by the synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the ADSTRGR.TRSA[5:0] bits. Neither asynchronous trigger nor software trigger can be operated in double trigger mode. The A/D conversion results started by the first trigger are stored into the A/D data register y and those started by the second trigger are stored into the A/D data duplication register. In this case, if the ADIE bit is set to 1, the interrupt is output not upon completion of the first scan but upon completion of the second scan.
In continuous scan mode, double trigger mode should not be selected. Also do not select double trigger mode for conversion of temperature sensor output.
The DBLE bit should be set after the ADST bit has been set to 0.

EXTRG Bit (Trigger Select)

The EXTRG bit selects the synchronous trigger or the asynchronous trigger as the trigger for starting A/D conversion.

TRGE Bit (Trigger Start Enable)

The TRGE bit sets whether to enable or disable starting of A/D conversion by the synchronous trigger and the asynchronous trigger.

This bit should be set to 1 in group scan mode.

ADIE Bit (Scan End Interrupt Enable)

The ADIE bit sets whether to enable or disable generation of the A/D scan end interrupt (S12ADI) in group scan mode (except for group B scan).
With double trigger mode deselected, the S12ADI interrupt is generated after the first scan is completed if the ADIE bit is set to 1.
With the extended analog input selected, the S12ADI interrupt is generated after A/D conversion is completed if the ADIE bit is set to 1.
With double trigger mode selected, the S12ADI interrupt is generated after the second scan is completed if the ADIE bit is set to 1 as long as the scan is started by the synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the ADSTRGR.TRSA[5:0] bits.

ADCS[1:0] Bits (Scan Mode Select)

The ADCS bit select the scan mode.
In single scan mode, A/D conversion is performed for the analog inputs of a maximum of eight channels in unit 0 and 16 channels in unit 1 selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, the scan conversion is stopped.*1
In continuous scan mode, while the ADST bit in ADCSR is 1, A/D conversion is performed for the analog inputs of a maximum of eight channels in unit 0 and 16 channels in unit 1 selected with the ADANSA register in the ascending order of the channel number, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is repeated from the first channel. If the ADST bit in ADCSR is set to 0 during continuous scan, A/D conversion is stopped even if scanning is in progress.*1
In group scan mode, A/D conversion is performed for the analog inputs (group A) of a maximum of eight channels in unit 0 and 16 channels in unit 1 selected with the ADANSA register in the ascending order of the channel number after scanning is started by the synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the TRSA[5:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. A/D conversion is also performed for the analog inputs (group B) of a maximum of eight channels in unit 0 and 16 channels in unit 1 selected with the ADANSB register in the ascending order of the channel number after scanning is started by the synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the TRSB[5:0] bits in ADSTRGR, and when one cycle of A/D conversion is completed for all the selected channels, A/D conversion is stopped. If the conversion processes in group A and B occur at the same time, ADC cannot control those conversion separately. In this case, set the group A priority control setting bit (ADGSPCR.PGS) in the A/D group scan priority control register (ADGSPCR) to 1 in order to assign a priority to conversion of group A.*1
In group scan mode, different channels and triggers should be selected for group A and group B.
When the extended analog input is selected, single scan mode or continuous scan mode should be selected.
The ADCS[1:0] bits should be set while the ADST bit is 0 (it should not be set simultaneously when 1 is written to the ADST bit.)

Note 1. When the temperature sensor output is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output.

Table 43.5 shows the selectable targets for A/D conversion depending on the settings of scan mode and double trigger mode.

Table 43.5 Selectable Targets for A/D Conversion Depending on the Settings of Scan Mode and Double Trigger Mode

		Targets for A/D Conversion				
Scan Mode Setting	Double Trigger Mode Setting	Self-Diagnosis	Analog Input (Including Group A)	Analog Input (Group B)	Temperature Sensor Output	Extended Analog Input
Single scan	DBLE = 0	√	√	×	√	√
	DBLE = 1	√	√ (1ch only)	×	×	×
Continuous scan	DBLE = 0	√	√	×	√	√
	DBLE = 1	×	×	×	×	×
Group scan	DBLE = 0	√	√	√	√	×
	DBLE = 1	×	√ (1ch only)	√	×	×

Note: √: Selectable; ×: Not selectable
Note: When the extended analog input is selected as a target for A/D conversion, other A/D conversion targets should not be selected.

ADST Bit (A/D Conversion Start)

The ADST bit starts or stops A/D conversion process.
Before the ADST bit is set to 1, set the A/D conversion clock, the conversion mode, and conversion target analog input.
[Setting conditions]
The ADST bit is set to 1 if one of the following conditions is satisfied:

- 1 is written by software.
- The synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the ADSTRGR.TRSA[5:0] bits is detected with ADCSR.EXTRG and ADCSR.TRGE bits being set to 0 and 1, respectively.
- The synchronous trigger (MTU3a, GPTa, TPUa, ELC) selected by the ADSTRGR.TRSB[5:0] bits is detected with the ADCSR.TRGE bit being set to 1 in group scan mode.
- The asynchronous trigger is detected with the ADCSR.TRGE and ADCSR.EXTRG bits being set to 1 and the ADSTRGR.TRSA[5:0] bits being set to 000000b.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), a group B trigger is detected and A/D conversion of group B is started.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1 and A/D conversion of group B is restarted.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1 and A/D conversion of group B is started.

[Clearing conditions]

The ADST bit is cleared to 0 if one of the following conditions is satisfied:

- 0 is written by software.
- The A/D conversion of all the selected channels or the temperature sensor output is completed in single scan mode.
- The A/D conversion of the extended analog input is completed in single scan mode.
- Group A scan is completed in group scan mode.
- Group B scan is completed in group scan mode.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), a group A trigger is detected during group B A/D conversion and the scanning of group B is stopped.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1 and the scanning of group B started by a resumption trigger is completed.
- With group-A priority control operation mode enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRSCN bit is set to 1 and the scanning of group B by a trigger is completed.

Note: When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.

Note: When group-A priority control operation mode has been enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1) and ADGSPCR.GBRP = 1, do not set the ADST bit to 0. When forcibly terminating A/D conversion, follow the procedure for clearing the ADST bit.

43.2.4 A/D Channel Select Register A (ADANSA)

ADANSA selects analog input channels for A/D conversion among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). In group scan mode, this register selects group A channels.

Address(es): S12ADC0.ADANSA A008 C004h, S12ADC1.ADANSA A008 C404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ANSA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ANSA[15:0]	A/D Conversion Channel Select	0: AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) are not subjected to conversion. 1: AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) are subjected to conversion.	R/W

ANSA[15:0] Bits (A/D Conversion Channel Select)

The ANSA[15:0] bits select analog input channels for A/D conversion among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). The channels to be selected and the number of channels can be arbitrarily set. In unit 0, the ANSA[0] bit corresponds to AN000 and the ANSA[7] bit corresponds to AN007. In unit 1, the ANSA[0] bit corresponds to AN100 and the ANSA[15] bit corresponds to AN115.

When double trigger mode is selected, the channel selected by the ANSA[15:0] bits is invalid, and the channel selected by the ADCSR.DBLANS[4:0] bits is selected in group A instead.

When group scan mode is selected, do not select the channels specified in the A/D channel select register B (ADANSB).

The ANSA[15:0] bits should be set while the ADCSR.ADST bit is 0.

43.2.5 A/D Channel Select Register B (ADANSB)

ADANSB selects analog input channels for A/D conversion among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) in group B when group scan mode is selected. The ADANSB register is not used in any scan mode other than group scan mode.

Address(es): S12ADC0.ADANSB A008 C014h, S12ADC1.ADANSB A008 C414h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ANSB[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ANSB[15:0]	A/D Conversion Channel Select	0: AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) are not subjected to conversion. 1: AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) are subjected to conversion.	R/W

ANSB[15:0] Bits (A/D Conversion Channel Select)

The ANSB[15:0] bits select analog input channels for A/D conversion among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) in group B when group scan mode is selected. The ADANSB register is used for group scan mode only; not used for any other modes. The channels specified in group A (the channels corresponding to group A, selected with the ADANSA register and the ADCSR.DBLANS[4:0] bits in double trigger mode) should be excluded as the channels to be selected and the number of channels to be set.

In unit 0, the ANSB[0] bit corresponds to AN000 and the ANSB[7] bit corresponds to AN007. In unit 1, the ANSB[0] bit corresponds to AN100 and the ANSB[15] bit corresponds to AN115.

The ANSB[15:0] bits should be set while the ADCSR.ADST bit is 0.

43.2.6 A/D-Converted Value Addition/Average Mode Select Register (ADADS)

ADADS selects the channels AN000 to AN007 and AN100 to AN115 on which A/D conversion is performed successively 2 to 4 times and then converted values are added (integrated) or averaged.

Address(es): S12ADC0.ADADS A008 C008h, S12ADC1.ADADS A008 C408h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	ADS[15:0]	A/D-Converted Value Addition/ Average Channel Select	0: A/D-converted value addition/average mode for AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) is not selected. 1: A/D-converted value addition/average mode for AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) is selected.	R/W

ADS[15:0] Bits (A/D-Converted Value Addition/Average Channel Select)

When the ADS[n] bit of the number that is the same as that of A/D-converted channel selected by the ANSA[n] bits (n = 0 to 7 in unit 0, or n = 0 to 15 in unit 1) in ADANSA or DBLANS[4:0] bits in ADCSR and ANSB[n] bits (n = 0 to 7 in unit 0, or n = 0 to 15 in unit 1) in ADANSB is set to 1, A/D conversion of analog input of the selected channels is performed successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register. As for the channel on which the A/D conversion is performed and addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored to the A/D data register.

The ADS[15:0] bits should be set while the ADCSR.ADST bit is 0.

Figure 43.3 shows the scan sequence when ADS[2] and ADS[6] are set to 1.

It is assumed that the scan is operated in continuous scan mode (ADCS = 10b in ADCSR), addition mode is selected (ADADC.AVEE = 0), the number of additions is set to 3 (conversion is performed four times) (ADADC.ADC[1:0] = 11b), and AN000 to AN007 is selected (ADANSA.ANSA[15:0] = 00FFh). Conversion is started from AN000. Conversion for AN002 is performed four times, and the value obtained by addition (integration) is stored in the A/D data register 2. Then, conversion for AN003 is started. Conversion for AN006 is performed four times successively, and the value obtained by addition (integration) is stored in the A/D data register 6. After conversion of AN007 is completed, the same sequence repeats from AN000.

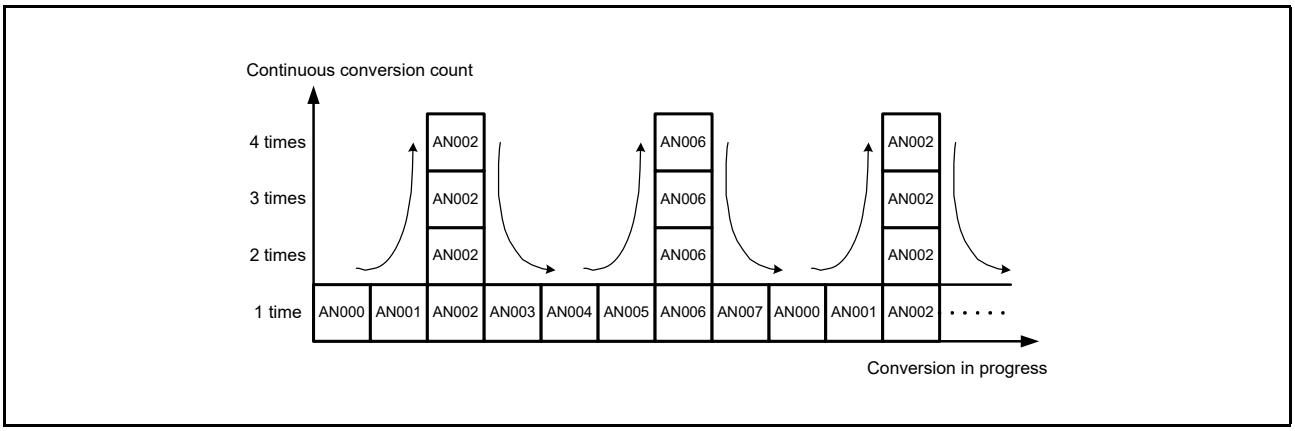


Figure 43.3 Scan Conversion Sequence with ADADC.ADC[1:0] = 11b, ADADC.AVEE = 0, ADS[2] = 1, and ADS[6] = 1

43.2.7 A/D-Converted Value Addition/Average Count Select Register (ADADC)

ADADC sets the addition count and average count for A/D conversion of the channel for which A/D-converted value addition/average mode is selected and for A/D conversion of temperature sensor output, and selects either addition or average mode.

Address(es): S12ADC0.ADADC A008 C00Ch, S12ADC1.ADADC A008 C40Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	—	ADC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	ADC[1:0]	Addition Count Select	b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition once) 1 0: 3-time conversion (addition twice)*1 1 1: 4-time conversion (addition three times)	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Addition mode is selected. 1: Average mode is selected.	R/W

Note 1. When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to three times (ADADC.ADC[1:0] = 10b)

ADC[1:0] Bits (Addition Count Select)

The ADC[1:0] bits set the addition count common to the channels for which A/D conversion and A/D-converted value addition/average mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits), and to A/D conversion of temperature sensor output.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to three times (ADADC.ADC[1:0] = 10b).

The ADC[1:0] bits should be set while the ADCSR.ADST bit is 0. When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[1:0] bits to any value other than 00b.

AVEE Bit (Average Mode Enable)

The AVEE bit selects addition or average mode for A/D conversion of the channel for which A/D conversion and A/D-converted value addition/average mode is selected, including the channels selected in double trigger mode (by ADCSR.DBLANS[4:0] bits) and temperature sensor output.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to three times (ADADC.ADC[1:0] = 10b).

The AVEE bits should be set while the ADCSR.ADST bit is 0.

43.2.8 A/D Control Extended Register (ADCER)

ADCER sets self-diagnosis mode, format of the A/D data registers y (ADDRy), and automatic clearing of A/D data registers.

Address(es): S12ADC0.ADCER A008 C00Eh, S12ADC1.ADCER A008 C40Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D Conversion Accuracy Specify	b2 b1 0 0: A/D conversion is performed with 12-bit accuracy. 0 1: A/D conversion is performed with 10-bit accuracy. 1 0: A/D conversion is performed with 8-bit accuracy. 1 1: Setting is prohibited.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Disables automatic clearing. 1: Enables automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: Uses the voltage of 0 V for self-diagnosis. 1 0: Uses the voltage of reference power supply*1 × 1/2 for self-diagnosis. 1 1: Uses the voltage of reference power supply*1 for self-diagnosis.	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Rotation mode for self-diagnosis voltage 1: Fixed mode for self-diagnosis voltage	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disables self-diagnosis of 12-bit A/D converter. 1: Enables self-diagnosis of 12-bit A/D converter.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Right-alignment is selected for the A/D data register format. 1: Left-alignment is selected for the A/D data register format.	R/W

Note 1. “Reference voltage” refers to VREFH0 for unit 0 and to VREFH1 for unit 1.

ADPRC[1:0] Bits (A/D Conversion Accuracy Specify)

These bits select the A/D conversion accuracy among 8-, 10-, or 12-bit accuracy. When the A/D conversion accuracy is changed, the bit width of effective data stored in the result register and A/D conversion time are also changed.
See section 43.3.7 Analog Input Sampling and Scan Conversion Time for details.

ACE Bit (A/D Data Register Automatic Clearing Enable)

The ACE bit selects enabling or disabling of automatic clearing (all “0”) of the A/D data register (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, or ADTSDR) when reading any of these registers by the CPU or DMACA. Automatic clearing of the A/D data register enables a failure which has not been updated in the A/D data register to be detected.

DIAGVAL[1:0] Bits (Self-Diagnosis Conversion Voltage Select)

These bits select the voltage value used in self-diagnosis voltage fixed mode. For details, refer to the descriptions of the ADCER.DIAGLD bit.

Self-diagnosis should not be executed by setting the ADCER.DIAGLD bit to 1 when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD Bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or the fixed voltage is used in self-diagnosis. Setting this bit (ADCER.DIAGLD) to 0 allows conversion of the voltages in rotation mode where 0, the reference power supply × 1/2, and the reference power supply are converted in this order. If the self-diagnosis voltage rotation mode is selected after a reset, rotation starts at 0 V. The fixed voltage specified by the ADCER.DIAGVAL[1:0] bits is converted when self-diagnosis voltage fixed mode is selected. In self-diagnosis voltage rotation mode, the self-diagnosis voltage value does not return to 0 when scan conversion is completed. When scan conversion is restarted, therefore, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

The DIAGLD bit should be set while the ADCSR.ADST bit is 0.

DIAGM Bit (Self-Diagnosis Enable)

The DIAGM bit selects execution of self-diagnosis.

Self-diagnosis is used to detect a failure of the 12-bit A/D converter. Specifically, it is used to convert the voltage value selected from the internally generated voltage values 0, the reference power supply × 1/2, and the reference power supply. When conversion is completed, information on the converted voltage and the conversion result is stored into the self-diagnosis data register (ADRD). ADRD can then be read out by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. The execution time of self-diagnosis differs from the A/D conversion time of one channel.

When self-diagnosis is selected in double trigger mode, self-diagnosis is executed only for the first scan conversion by a synchronous trigger (MTU3a, GPTa, TPUa, ELC), not executed in the second scan. When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed in group A and B.

The DIAGM bit should be set while the ADCSR.ADST bit is 0.

Self-diagnosis cannot be performed when extended analog input is used.

ADRFMT Bit (A/D Data Register Format Select)

The ADRFMT bit specifies right-alignment or left-alignment for the data to be stored in ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADRD, or ADCMPDRy.

For details on the format of each data register, see section 43.2.1 A/D Data Registers y (ADDRy), A/D Data Duplication Register (ADDBLDR), A/D Data Duplication Register A (ADDBLDRA), A/D Data Duplication Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), section 43.2.2 A/D Self-Diagnosis Data Register (ADRD), and section 43.2.21 A/D Compare Data Register y (ADCMPDRy) (y = 0, 1).

43.2.9 A/D Start Trigger Select Register (ADSTRGR)

ADSTRGR selects the A/D conversion start trigger.

Address(es): S12ADC0.ADSTRGR A008 C010h, S12ADC1.ADSTRGR A008 C410h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	Select the A/D conversion start trigger for group B in group scan mode.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	Select the A/D conversion start trigger in single scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] Bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in group B. The TRSB[5:0] bits require to be set only in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for group B, setting a software trigger or an asynchronous trigger is prohibited. Therefore, the TRSB[5:0] bits should be set to the value other than 000000b and the ADCSR.TRGE bit should be set to 1 in group scan mode.

When group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh.

Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger may have no effect.

Because an A/D conversion start trigger requires synchronization processing, a delay of the period for synchronization processing occurs. See section 43.3.7 Analog Input Sampling and Scan Conversion Time for details.

Table 43.6 lists the A/D conversion startup sources selected by the TRSB[5:0] bits.

TRSA[5:0] Bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in group A is selected. When scanning is executed in group scan mode or double trigger mode, a software trigger and an asynchronous trigger cannot be used at the same time.

- When using the A/D conversion startup source of a synchronous trigger (MTU3a, GPTa, TPUa, ELC), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 0.
- When using the asynchronous trigger (ADTRGn), set the TRGE bit in ADCSR to 1 and set the EXTRG bit in ADCSR to 1.
- Software trigger (ADCSR.ADST) is enabled regardless of the settings of the ADCSR.TRGE bit, the ADCSR.EXTRG bit, and the TRSA[5:0] bits.

Note that the issuance period of trigger for A/D conversion must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by a trigger may have no effect. Because an A/D conversion start trigger requires synchronization processing, a delay of the period for synchronization processing occurs. See section 43.3.7 Analog Input Sampling and Scan Conversion Time for details.

Table 43.7 lists the selection of A/D activation sources selected by the TRSA[5:0] bits.

Table 43.6 Selection of A/D Activation Sources by the TRSB[5:0] Bits (for Group B only) (1 / 2)

Module	Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source de-selection state			1	1	1	1	1	1
MTU3a	TRGA0N	Compare match with or input capture to MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match with or input capture to MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match with or input capture to MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match with or input capture to MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match with or input capture to MTU4.TGRA, or an underflow of MTU4.TCNT (in the trough) in complementary PWM mode	0	0	0	1	0	1
	TRGA6N	Compare match with or input capture to MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match with or input capture to MTU7.TGRA, or an underflow of MTU7.TCNT (in the trough) in complementary PWM mode	0	0	0	1	1	1
	TRG0N	Compare match with MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT, or between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT, and between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT, or between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT, and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	0	1	0	0	0	0
GPTa	GTADTRA0N	Compare match with GPT0.GTADTRA	0	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	0	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	0	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	0	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	0	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	0	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	0	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	0	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	0	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	0	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	0	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	0	1	1	1	0	0
TPUa	TPTRGAN_0	Compare match with or input capture to TPUn.TGRA (n = 0 to 4)	0	1	1	1	1	1
	TPTRG0AN_0	Compare match with or input capture to TPU0.TGRA	1	0	0	0	0	0
	TPTRGAN_1	Compare match with or input capture to TPUn.TGRA (n = 6 to 10)	1	0	0	0	0	1
	TPTRG6AN_1	Compare match with or input capture to TPU6.TGRA	1	0	0	0	1	0

Table 43.6 Selection of A/D Activation Sources by the TRSB[5:0] Bits (for Group B only) (2 / 2)

Module	Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
ELC	ELCTRG0/ ELCTRG1	Event signals from the respective peripheral modules	1	1	0	0	0	0

Table 43.7 Selection of A/D Activation Sources by the TRSA[5:0] Bits (1 / 2)

Module	Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source de-selection state			1	1	1	1	1	1
External	ADTRG0 ADTRG1	Input pin for the trigger	0	0	0	0	0	0
MTU3a	TRGA0N	Compare match with or input capture to MTU0.TGRA	0	0	0	0	0	1
	TRGA1N	Compare match with or input capture to MTU1.TGRA	0	0	0	0	1	0
	TRGA2N	Compare match with or input capture to MTU2.TGRA	0	0	0	0	1	1
	TRGA3N	Compare match with or input capture to MTU3.TGRA	0	0	0	1	0	0
	TRGA4N	Compare match with or input capture to MTU4.TGRA or, in complementary PWM mode, an underflow of MTU4.TCNT (in the trough)	0	0	0	1	0	1
	TRGA6N	Compare match with or input capture to MTU6.TGRA	0	0	0	1	1	0
	TRGA7N	Compare match with or input capture to MTU7.TGRA or, in complementary PWM mode, an underflow of MTU7.TCNT (in the trough)	0	0	0	1	1	1
	TRG0N	Compare match with MTU0.TGRE	0	0	1	0	0	0
	TRG4AN	Compare match between MTU4.TADCORA and MTU4.TCNT	0	0	1	0	0	1
	TRG4BN	Compare match between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	0
	TRG4AN or TRG4BN	Compare match between MTU4.TADCORA and MTU4.TCNT, or between MTU4.TADCORB and MTU4.TCNT	0	0	1	0	1	1
	TRG4ABN	Compare match between MTU4.TADCORA and MTU4.TCNT, and between MTU4.TADCORB and MTU4.TCNT (when interrupt skipping function 2 is in use)	0	0	1	1	0	0
	TRG7AN	Compare match between MTU7.TADCORA and MTU7.TCNT	0	0	1	1	0	1
	TRG7BN	Compare match between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	0
	TRG7AN or TRG7BN	Compare match between MTU7.TADCORA and MTU7.TCNT, or between MTU7.TADCORB and MTU7.TCNT	0	0	1	1	1	1
	TRG7ABN	Compare match between MTU7.TADCORA and MTU7.TCNT, and between MTU7.TADCORB and MTU7.TCNT (when interrupt skipping function 2 is in use)	0	1	0	0	0	0
GPTa	GTADTRA0N	Compare match with GPT0.GTADTRA	0	1	0	0	0	1
	GTADTRB0N	Compare match with GPT0.GTADTRB	0	1	0	0	1	0
	GTADTRA1N	Compare match with GPT1.GTADTRA	0	1	0	0	1	1
	GTADTRB1N	Compare match with GPT1.GTADTRB	0	1	0	1	0	0
	GTADTRA2N	Compare match with GPT2.GTADTRA	0	1	0	1	0	1
	GTADTRB2N	Compare match with GPT2.GTADTRB	0	1	0	1	1	0
	GTADTRA3N	Compare match with GPT3.GTADTRA	0	1	0	1	1	1
	GTADTRB3N	Compare match with GPT3.GTADTRB	0	1	1	0	0	0
	GTADTRA0N or GTADTRB0N	Compare match with GPT0.GTADTRA or with GPT0.GTADTRB	0	1	1	0	0	1
	GTADTRA1N or GTADTRB1N	Compare match with GPT1.GTADTRA or with GPT1.GTADTRB	0	1	1	0	1	0
	GTADTRA2N or GTADTRB2N	Compare match with GPT2.GTADTRA or with GPT2.GTADTRB	0	1	1	0	1	1
	GTADTRA3N or GTADTRB3N	Compare match with GPT3.GTADTRA or with GPT3.GTADTRB	0	1	1	1	0	0

Table 43.7 Selection of A/D Activation Sources by the TRSA[5:0] Bits (2 / 2)

Module	Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
TPUa	TPTRGAN_0	Compare match with or input capture to TPUn.TGRA (n = 0 to 4)	0	1	1	1	1	1
	TPTRG0AN_0	Compare match with or input capture to TPU0.TGRA	1	0	0	0	0	0
	TPTRGAN_1	Compare match with or input capture to TPUn.TGRA (n = 6 to 10)	1	0	0	0	0	1
	TPTRG6AN_1	Compare match with or input capture to TPU6.TGRA	1	0	0	0	1	0
ELC	ELCTRG0/ ELCTRG1	Event signals from the respective peripheral modules	1	1	0	0	0	0

43.2.10 A/D Conversion Extended Input Control Register (ADEXICR) Unit0 (with Temperature Sensor and without Extended Analog Input)

ADEXICR controls temperature sensor output and extended analog input and output.

Address(es): S12ADC0.ADEXICR A008 C012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSSB	—	TSSA	—	—	—	—	—	—	—	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select	0: Temperature sensor output A/D-converted value addition/average mode is not selected. 1: Temperature sensor output A/D-converted value addition/average mode is selected.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TSSA	Temperature Sensor Output A/D Conversion Select	0: A/D conversion of temperature sensor output is disabled. 1: A/D conversion of temperature sensor output is enabled.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	TSSB	Temperature Sensor Output A/D Conversion Select	0: A/D conversion of temperature sensor output is disabled. 1: A/D conversion of temperature sensor output is enabled.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSSAD Bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

This bit selects A/D conversion of the temperature sensor output. When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively 2 to 4 times that is set with the ADC[1:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D temperature sensor data register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.
The TSSAD bit should be set while the ADCSR.ADST bit is 0.

TSSA Bit (Temperature Sensor Output A/D Conversion Select)

This bit selects A/D conversion of the temperature sensor output for group A in single scan mode, continuous scan mode or group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.
The TSSA bit should be set while the ADCSR.ADST bit is 0.

TSSB Bit (Temperature Sensor Output A/D Conversion Select)

This bit selects A/D conversion of the temperature sensor output for group B in group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.
The TSSB bit should be set while the ADCSR.ADST bit is 0. Do not set the TSSB bit to 1 while the TSSA bit is 1.

43.2.11 A/D Conversion Extended Input Control Register (ADEXICR) Unit1 (without Temperature Sensor and with Extended Analog Input)

ADEXICR controls temperature sensor output and extended analog input and output.

Address(es): S12ADC1.ADEXICR A008 C412h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EXOEN	EXSEL[1:0]		—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b12 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	EXSEL[1:0]	Extended Analog Input Select	b14 b13 0 0: Analog input channel (ANn pin) 0 1: AN1_ANEX1 pin 1 0: Setting is prohibited. 1 1: Setting is prohibited.	R/W
b15	EXOEN	Extended Analog Output Control	0: Output is disabled. 1: Output is enabled.	R/W

EXSEL[1:0] Bits (Extended Analog Input Select)

These bits select the extended analog input pin (AN1_ANEX1) instead of the analog input channels (ANn).
When the AN1_ANEX1 pin is selected, AN1_ANEX0 pin output should be input to the AN1_ANEX1 pin via the external operational amplifier. In this case, only select AN100 to AN107; do not select AN108 to AN115. For details, see section 43.3.5.1 Usage of AN1_ANEX1.
When the AN1_ANEX1 pin is selected, self-diagnosis function cannot be used.

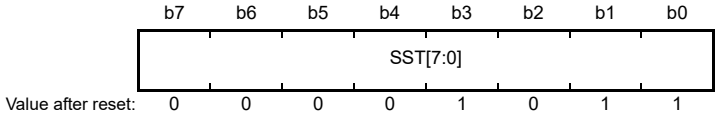
EXOEN Bit (Extended Analog Output Control)

This bit controls the extended analog output (AN1_ANEX0). When the output is enabled, the multiplexed value of AN100 to AN107 among analog input channels in unit 1 is output to the AN1_ANEX0 pin. Do not enable an output when the EXSEL[1:0] bits are 00b.

43.2.12 A/D Sampling State Register n (ADSSTRn) (n = 0 to 7, L, T)

The ADSSTRn register sets the sampling time for analog input.
If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 11 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted by the value of SST[7:0] bits. The SST[7:0] bits should be set while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 5 states or more and is 255 or less.
Table 43.8 shows the relationship between the A/D sampling state register and the relevant channels.
For details, refer to section 43.3.7 Analog Input Sampling and Scan Conversion Time.

Address(es): S12ADC0.ADSSTR0 A008 C060h, S12ADC0.ADSSTRT A008 C070h, S12ADC0.ADSSTR1 A008 C073h, S12ADC0.ADSSTR2 A008 C074h, S12ADC0.ADSSTR3 A008 C075h, S12ADC0.ADSSTR4 A008 C076h, S12ADC0.ADSSTR5 A008 C077h, S12ADC0.ADSSTR6 A008 C078h, S12ADC0.ADSSTR7 A008 C079h
S12ADC1.ADSSTR0 A008 C460h, S12ADC1.ADSSTRL A008 C461h, S12ADC1.ADSSTR1 A008 C473h, S12ADC1.ADSSTR2 A008 C474h, S12ADC1.ADSSTR3 A008 C475h, S12ADC1.ADSSTR4 A008 C476h, S12ADC1.ADSSTR5 A008 C477h, S12ADC1.ADSSTR6 A008 C478h, S12ADC1.ADSSTR7 A008 C479h



Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 5 to 255 states.	R/W

Table 43.8 Relationship between A/D Sampling State Register and Relevant Channels

	Corresponding Channels	
Bit Name	**Unit 0**	**Unit 1**
ADSSTR0.SST[7:0] bits*1	AN000	AN100
ADSSTR1.SST[7:0] bits	AN001	AN101
ADSSTR2.SST[7:0] bits	AN002	AN102
ADSSTR3.SST[7:0] bits	AN003	AN103
ADSSTR4.SST[7:0] bits	AN004	AN104
ADSSTR5.SST[7:0] bits	AN005	AN105
ADSSTR6.SST[7:0] bits	AN006	AN106
ADSSTR7.SST[7:0] bits	AN007	AN107
ADSSTRL.SST[7:0] bits	—	AN108 to AN115
ADSSTRT.SST[7:0] bits	Temperature sensor output (in unit 0 only)	—

Note 1. When self-diagnosis function is selected, the sampling time set by the ADSSTR0.SST[7:0] bits is applied to it.

43.2.13 A/D Sample and Hold Circuit Control Register (ADSHCR)

ADSHCR sets the parameters related to channel-dedicated sample-and-hold circuits.

Address(es): S12ADC0.ADSHCR A008 C066h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SHANS[3:0]				SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting	Set the sampling time (4 to 255 states).	R/W
b11 to b8	SHANS[3:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or not use (bypass) AN000 to AN003 channel-dedicated sample-and-hold circuits. 0: Bypass the channel-dedicated sample-and-hold circuits. 1: Use the channel-dedicated sample-and-hold circuits.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSTSH[7:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. If one state is one ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 24 states. If the impedance of analog input signal source is too high to secure sufficient sampling time or if the ADCLK clock is slow, the sampling time can be adjusted. The SSTSH[7:0] bits should be set while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 4 states or more and is 255 or less. Also, the sampling time must be 0.4 µs or more.

SHANS[3:0] Bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

The SHANS[3:0] bits select whether to use or not use (bypass) AN000 to AN003 channel-dedicated sample-and-hold circuits. The SHANS[0] bit selects AN000, SHANS[1] bit selects AN001, SHANS[2] bit selects AN002, and SHANS[3] bit selects AN003. The SHANS[3:0] bits should be set while the ADST bit in ADCSR is 0.

If any channel from among AN000 to AN003 is selected for group B while operation is in group scan mode under group A priority control, make the setting to bypass the channel's dedicated sample-and-hold circuit.

The channels in unit 1 do not include channel-dedicated sample-and-hold circuits.

43.2.14 A/D Disconnection Detection Control Register (ADDISCR)

ADDISCR sets the disconnection detection assist function.

Address(es): S12ADC0.ADDISCR A008 C07Ah, S12ADC1.ADDISCR A008 C47Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ADNDIS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	ADNDIS[4:0]	Disconnection Detection Assist Setting	Disconnection detection assist function is set.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADNDIS[4:0] Bits (Disconnection Detection Assist Setting)

These bits selects either precharge or discharge and the period of precharge/discharge for the A/D disconnection detection assist function. Setting the ADNDIS[4] bit = 1 allows to select precharge and setting the ADNDIS[4] bit = 0 allows to select discharge. The period of precharge/discharge can be set with the ADNDIS[3:0] bits. When the ADNDIS[3:0] bits = 0000b, the disconnection detection assist function is not effective. Setting of the ADNDIS[3:0] bits to 0001b is prohibited. Except for the case of ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge/discharge. When the temperature sensor output is converted or self-diagnosis is used, the disconnection detection assistance cannot be used. In that case, the ADNDIS[3:0] bits should be set to 0000b. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, and the disconnection detection assistance is enabled, the disconnection detection assistance for the channel-dedicated sample-and-hold circuit is also enabled. Note that if ADEXICR.EXSEL[1:0] and ADEXICR.EXOEN are set to any values other than ADEXICR.EXSEL[1:0] = 00b and ADEXICR.EXOEN = 0b, and the disconnection detection assistance is enabled, A/D conversion cannot be executed correctly. In such a case, disable the disconnection detection assistance function. Also, disable this function when pin-level self-diagnosis is executed.

43.2.15 A/D Group Scan Priority Control Register (ADGSPCR)

ADGSPCR is used to make settings for priority control of A/D conversion for group A in group scan mode.

Address(es): S12ADC0.ADGSPCR A008 C080h, S12ADC1.ADGSPCR A008 C480h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PGS	Group-A Priority Control Setting*1	0: Operation is without group A priority control 1: Operation is with group A priority control	R/W
b1	GBRSCN	Group B Restart Setting	(Enabled only when PGS = 1. Set 0 when PGS = 0.) 0: Scanning for group B is not restarted when priority control is performed for group A. 1: Scanning for group B is restarted when priority control is performed for group A.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*2	(Enabled only when PGS = 1. Set 0 when PGS = 0.) 0: Single scan for group B is not continuously activated. 1: Single scan for group B is continuously activated.	R/W

Note 1. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, proper operation cannot be guaranteed.
Note 2. When the GBRP bit has been set to 1, single scan is performed continuously for group B regardless of the setting of the GBRSCN bit.

PGS Bit (Group A Priority Control Setting)

This bit sets the priority of operation on group A. Set this bit to 1 when giving priority to operation on group A.
When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, proper operation cannot be guaranteed.
When the PGS bit has been set to 0, A/D conversion must be stopped according to section 43.5.2 Notes on Stopping A/D Conversion. When the PGS bit has been set to 1, make register settings according to section 43.3.4.3 Operation under Group-A Priority Control.

GBRSCN Bit (Group B Restart Setting)

This bit controls the restarting of scan operation on group B when operation on group A is given priority.
If a scan operation on group B has been stopped by a group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of the A/D conversion on group A. Also, if a group B trigger is input during A/D conversion on group A, the scan operation on group B is restarted on completion of the A/D conversion on group A. However, when this function is to be used, set the ratio between the frequency divisors for PCLKH and ADCLK to 1:1. This function cannot be used if the frequency division settings are not in accord with this.
If the GBRSCN bit has been set to 0, triggers that are input during A/D conversion are ignored. Also, the ADCSR.ADST bit must be 0 when the GBRSCN bit is to be set.
The setting of the GBRSCN bit has an effect when the PGS bit is set to 1.

GBRP Bit (Group B Single Scan Continuous Start)

This bit is set when a single scan operation is to be performed continuously on group B.
Setting the GBRP bit to 1 starts a single scan on group B. On completion of the scan, another single scan on group B is automatically started. If an A/D conversion on group B has been stopped due to an operation on group A that takes priority, single scan on group B is automatically restarted on completion of the A/D conversion on group A.
Disable group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting of the GBRSCN bit. The ADCSR.ADST bit must be 0 when the GBRP bit is to be set.
The setting of the GBRP bit is valid when the PGS bit is 1.

43.2.16 A/D Compare Control Register (ADCMPCR)

ADCMPCR is used to set compare function.

Address(es): S12ADC0.ADCMPCR A008 C090h, S12ADC1.ADCMPCR A008 C490h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPIE	WCMPE	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WCMPE	Window Function	0: Window function disabled 1: Window function enabled	R/W
b7	CMPIE	Compare Interrupt Enable	0: Generation of an S12CMPI interrupt in response to matches with a condition for comparison is disabled. 1: Generation of an S12CMPI interrupt in response to matches with a condition for comparison is enabled.	R/W

WCMPE Bit (Window Function)

Set enable/disable of Window function.
For details about Window function, see section 43.2.19 A/D Compare Level Register (ADCMPLR).

CMPIE Bit (Compare Interrupt Enable)

This bit selects whether to enable or disable generation of a compare interrupt (S12CMPI) in response to a match.

43.2.17 A/D Compare Channel Select Register (ADCMPANSR)

ADCMPANSR is used to select analog input channels for comparison from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1).

Address(es): S12ADC0.ADCMPANSR A008 C094h, S12ADC1.ADCMPANSR A008 C494h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPS[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPS[15:0]	Compare Channel Select	0: The corresponding channel from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) is not a target for comparison. 1: The corresponding channel from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1) is a target for comparison.	R/W

CMPS[15:0] Bits (Compare Channel Select)

Setting the CMPS[n] bit which has the same number as the A/D channel selected by the ADANSA.ANSA[n] (n = 0 to 7 for unit 0, n = 0 to 15 for unit 1) or ADANSB.ANSB[n] (n = 0 to 7 for unit 0, n = 0 to 15 for unit 1) bit to 1 enables comparison with that channel.

Set the CMPS0[15:0] bits while ADCSR.ADST bit is 0.

The CMPS[15:8] bits of the unit 0 are reserved bits. Reading to these bits returns 0. Writing value should be 0.

43.2.18 A/D Compare Channel Select Extended Register (ADCMPANSER)

ADCMPANSER sets whether to use the temperature sensor output for comparison.

Address(es): S12ADC0.ADCMPANSER A008 C092h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPSTS	Temperature Sensor Output Compare Select	0: Temperature sensor output is not a target for comparison. 1: Temperature sensor output is a target for comparison.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTS Bit (Temperature Sensor Output Compare Select)

Setting the CMPSTS bit to 1 while ADEXICR.TSSA or ADEXICR.TSSB = 1 enables comparison.

43.2.19 A/D Compare Level Register (ADCMPLR)

The ADCMPLR register sets the condition for use in comparing the values of the ADCMPDR0 and ADCMPDR1 registers with results of A/D conversion.
Set the ADCMPLR register while ADCSR.ADST is 0.

Address(es): S12ADC0.ADCMPLR A008 C098h, S12ADC1.ADCMPLR A008 C498h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPL[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPL[15:0]	Compare Level Select	Set the condition for comparison with the selected channels from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). When Window function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 register value > A/D-converted value 1: ADCMPDR0 register value < A/D-converted value When Window function is enabled (ADCMPCR.WCMPE bit = 1): 0: AD-converted value < ADCMPDR0 register value or A/D-converted value > ADCMPDR1 register value 1: ADCMPDR0 register value < A/D-converted value < ADCMPDR1 register value	R/W

CMPL[15:0] Bits (Compare Level Select)

The CMPL0[15:0] bits set the condition for use in comparison with the selected channel from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). A condition can be set for individual comparison of each analog input.
The CMPL[0] bit is used for AN000 (unit 0) and AN100 (unit 1), the CMPL[7] bit is used for AN007 (unit 0) and AN107 (unit 1), and the CMPL[15] bit is used for AN115 (unit 1).
When the result of comparison matches the set condition, ADCMPSR.CMPFn is set to 1 and a compare interrupt (S12CMPI) is generated.
The CMPL[15:8] bits of the unit 0 are reserved. Reading to these bits returns 0. Writing value should be 0.

43.2.20 A/D Compare Level Extended Register (ADCMPLER)

The ADCMPLER register sets the condition for use in comparing the values of ADCMPDR0 and ADCMPDR1 registers with results of A/D conversion.

Set the ADCMPLER register while ADCSR.ADST is 0.

Address(es): S12ADC0.ADCMPLER A008 C093h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPLTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPLTS	Temperature Sensor Output Compare Select	When Window function is disabled (ADCMPCR.WCMPE bit = 0): 0: ADCMPDR0 register value > A/D-converted value 1: ADCMPDR0 register value < A/D-converted value When Window function is enabled (ADCMPCR.WCMPE bit = 1): 0: AD-converted value < ADCMPDR0 register value or A/D-converted value > ADCMPDR1 register value 1: ADCMPDR0 register value < A/D-converted value < ADCMPDR1 register value	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLTS Bit (Temperature Sensor Output Compare Level Select)

This bit sets the condition for use in comparison with temperature sensor output.

When the result of comparison matches the set condition, ADCMPSER.CMPFTS is set to 1 and a compare interrupt (S12CMPI) is generated.

43.2.21 A/D Compare Data Register y (ADCMPDRy) (y = 0, 1)

Set the reference data for comparison with the selected channels.
This register is accessible even during A/D conversion which allows dynamic changing of the reference data. The ADCMPDR1 register is not used when the Window function is disabled.
The ADCMPDRy register use different formats depending on the following conditions.

- The value of A/D data register format select bit (flush-right or flush-left)
- The value of A/D-conversion accuracy specification bit (12 bits, 10 bits, 8 bits)
- The value of A/D-converted value addition/average mode select register (A/D-converted value addition mode selected and not selected)

(1) When A/D-Converted Value Addition Mode is Not Selected

- The settings for flush-right data with 12-bit accuracy

Address(es): S12ADC0.ADCMPDR0 A008 C09Ch, S12ADC0.ADCMPDR1 A008 C09Eh, S12ADC1.ADCMPDR0 A008 C49Ch, S12ADC1.ADCMPDR1 A008 C49Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMPD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b11 to b0	CMPD[11:0]	—	12-bit reference value	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-right data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b9 to b0	CMPD[9:0]	—	10-bit reference value	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-right data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	CMPD[7:0]	—	8-bit reference value	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b4	CMPD[11:0]	—	12-bit reference value	R/W

- The settings for flush-left data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPD[9:0]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b6	CMPD[9:0]	—	10-bit reference value	R/W

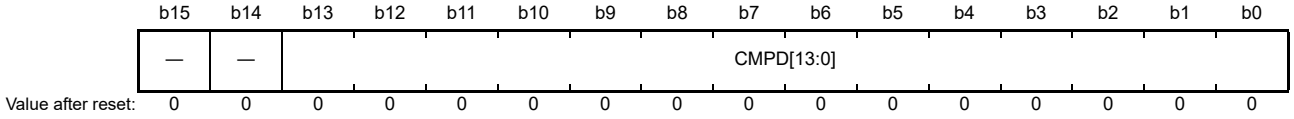
- The settings for flush-left data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPD[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	CMPD[7:0]	—	8-bit reference value	R/W

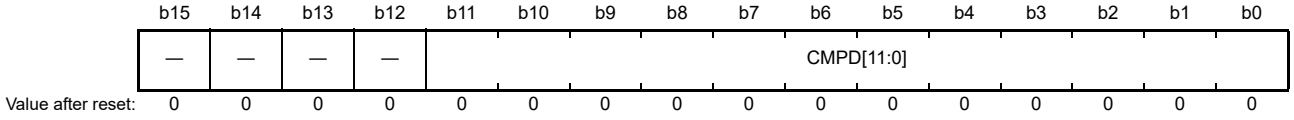
(2) When A/D-Converted Value Addition Mode is Selected

- The settings for flush-right data with 12-bit accuracy (when A/D-converted value addition mode is selected)



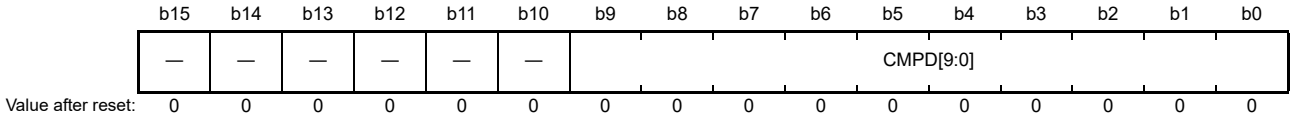
Bit	Symbol	Bit Name	Description	R/W
b13 to b0	CMPD[13:0]	—	14-bit reference value	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-right data with 10-bit accuracy (when A/D-converted value addition mode is selected)



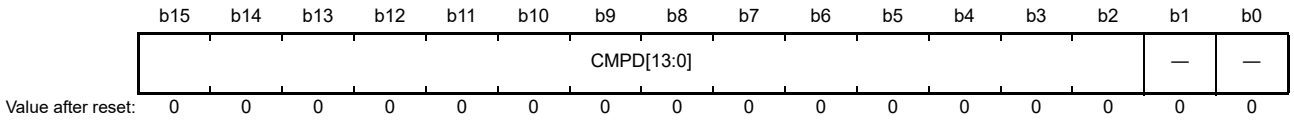
Bit	Symbol	Bit Name	Description	R/W
b11 to b0	CMPD[11:0]	—	12-bit reference value	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-right data with 8-bit accuracy (when A/D-converted value addition mode is selected)



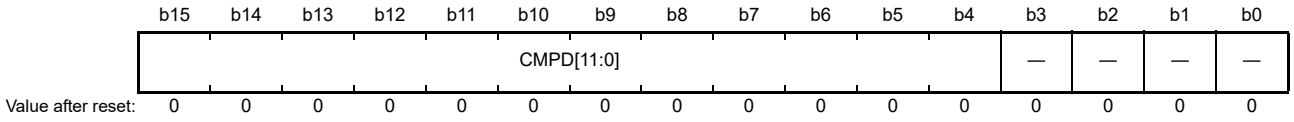
Bit	Symbol	Bit Name	Description	R/W
b9 to b0	CMPD[9:0]	—	10-bit reference value	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

- The settings for flush-left data with 12-bit accuracy (when A/D-converted value addition mode is selected)



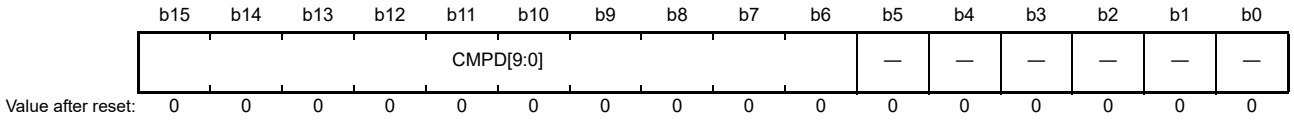
Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b2	CMPD[13:0]	—	14-bit reference value	R/W

- The settings for flush-left data with 10-bit accuracy (when A/D-converted value addition mode is selected)



Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b4	CMPD[11:0]	—	12-bit reference value	R/W

- The settings for flush-left data with 8-bit accuracy (when A/D-converted value addition mode is selected)



Bit	Symbol	Bit Name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b6	CMPD[9:0]	—	10-bit reference value	R/W

43.2.22 A/D Compare Status Register (ADCMPSR)

The ADCMPSR register stores the compare results of compare function.

Address(es): S12ADC0.ADCMPSR A008 C0A0h, S12ADC1.ADCMPSR A008 C4A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	CMPF[15:0]	Compare Flag	Indicates compare results of AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). 0: Condition for comparison was not met. 1: Condition for comparison was met.	R/W

CMPF[15:0] Bits (Compare Flag)

These bits are status flags to indicate the results of comparison with the selected analog inputs from among AN000 to AN007 (unit 0) and AN100 to AN115 (unit 1). When the result of comparison on completion of A/D conversion matches the condition set in ADCMPLR.CMPLn, the corresponding flags are set to 1.

When the ADCMPCR.CMPIE bit is 1, a compare interrupt (S12CMPI) request is generated when the setting of the flag becomes 1.

The CMPF[0] bit is used for AN000 (unit 0)/AN100 (unit 1), the CMPF[7] bit is used for AN007 (unit 0)/AN107 (unit 1), and the CMPF[15] bit is used for AN115 (unit 1).

The value 1 cannot be written to the CMPFn bit.

The CMPF[15:8] bits of the unit 0 are reserved. Reading to these bits returns 0. Writing value should be 0.

[Setting condition]

- The condition set in ADCMPLR.CMPLn is met.

[Clearing condition]

- 0 is written after reading 1.

43.2.23 A/D Compare Status Extended Register (ADCMPSER)

The ADCMPSER register is a status register that indicates the compare results of temperature sensor output.

Address(es): S12ADC0.ADCMPSER A008 C0A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPFTS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CMPFTS	Temperature Sensor Output Compare Flag	0: Condition for comparison was not met. 1: Condition for comparison was met.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPFTS Bit (Temperature Sensor Output Compare Flag)

This bit is a status flag to indicate the result of comparison with temperature sensor output. When the result of comparison on completion of A/D conversion matches the condition set in ADCMPLER.CMPLTS, this flag is set to 1. When the ADCMPCR.CMPIE bit is 1, a compare interrupt (S12CMPI) request is generated when the setting of the flag becomes 1.

The value 1 cannot be written to the CMPFTS bit.

[Setting condition]

- The condition set in ADCMPLER.CMPLTS is met.

[Clearing condition]

- 0 is written after reading 1.

43.2.24 A/D Pin-Level Self-Diagnosis Control Register (ADTDCR)

ADTDCR controls pin-level self-diagnosis function. For details about this function, see section 43.3.13 Pin-Level Self-Diagnosis Function.

Address(es): S12ADC0.ADTDCR A008 C0C8h, S12ADC1.ADTDCR A008 C4C8h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDE	—	—	—	—	—	TDLV[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	TDLV[1:0]	Pin-level Self-diagnosis Level Select	b1 b0 0 0: Input channels with even numbers are discharged to AVSS, and input channels with odd numbers are charged to AVCC. 0 1: Input channels with even numbers are charged to AVCC, and input channels with odd numbers are discharged to AVSS. 1 0: Input channels with even numbers are discharged to AVSS, and input channels with odd numbers are charged to AVCC × 1/2. 1 1: Input channels with even numbers are charged to AVCC × 1/2, and input channels with odd numbers are discharged to AVSS.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TDE	Pin-level Self-diagnosis Enable	0: Disables pin-level self-diagnosis. 1: Enables pin-level self-diagnosis.	R/W

TDLV[1:0] Bits (Pin-level Self-diagnosis Level Select)

These bits select the pin level for pin-level self-diagnosis.
Set the TDLV[1:0] bits while ADCSR.ADST bit is 0.

TDE Bit (Pin-level Self-diagnosis Enable)

This bit selects whether to perform pin-level self-diagnosis.
Set the TDE bit while ADCSR.ADST bit is 0.

43.2.25 A/D Error Control Register (ADERCR)

ADERCR controls error detection function. For details about errors, see section 43.3.14 Error Detection Function.

Address(es): S12ADC0.ADERCR A008 C0CAh, S12ADC1.ADERCR A008 C4CAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OWEIE	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	OWEIE	Overwrite Error Interrupt Enable	0: Disables interrupt generation when an overwrite error is detected. 1: Enables interrupt generation when an overwrite error is detected.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

OWEIE Bit (Overwrite Error Interrupt Enable)

This bit sets whether to enable or disable generation of an error interrupt request (S12ADE) when an overwrite error is detected.

Set the OWEIE bit while ADCSR.ADST bit is 0.

43.2.26 A/D Error Clear Register (ADERCLR)

The A/D error clear register is a write-only register for clearing errors.

Address(es): S12ADC0.ADERCLR A008 C0CBh, S12ADC1.ADERCLR A008 C4CBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OWEC	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	The write value should be 0.	W
b2	OWEC	Overwrite Error Clear	Writing 0: Disables clearing overwrite errors. Writing 1: Enables clearing overwrite errors.	W
b7 to b3	—	Reserved	The write value should be 0.	W

43.2.27 A/D Overwrite Error Register (ADOWER)

The ADOWER register is a status register that indicates that the results of A/D conversion in the ADDRy register were not read and an overwrite occurred.

Address(es): S12ADC0.ADOWER A008 C0D2h, S12ADC1.ADOWER A008 C4D2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OWE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b15 to b0	OWE[15:0]	Overwrite Error	0: No overwrite error occurred in S12ADC0.ADDR0 to S12ADC0.ADDR7 (unit 0) and S12ADC1.ADDR0 to S12ADC1.ADDR15 (unit 1). 1: An overwrite error occurred in S12ADC0.ADDR0 to S12ADC0.ADDR7 (unit 0) and S12ADC1.ADDR0 to S12ADC1.ADDR15 (unit 1).	R

OWE[15:0] Bits (Overwrite Error 0)

The OWE[15:0] bits are set to 1 when the results of the next A/D conversion are stored in the ADDRy register after the A/D conversion finishes without the results of A/D conversion in the ADDRy register being read.

The OWE[15:0] bits are cleared to 0 when 1 is written to the ADERCLR.OWEC register. The OWE[15:0] bits cannot be written to 1.

The OWE[0] bit corresponds to S12ADC0.ADDR0 and the OWE[7] bit corresponds to S12ADC0.ADDR7 for unit 0.

The OWE[0] bit corresponds to S12ADC1.ADDR0 and the OWE[15] bit corresponds to S12ADC1.ADDR15 for unit 1.

43.2.28 A/D Overwrite Error Extended Register (ADOWEER)

The ADOWEER register is a status register that indicates that the results of A/D conversion in the ADDBLDRB, ADDBLDRA, ADDBLDR, ADRD, ADTSDR registers were not read and an overwrite occurred.

Address(es): S12ADC0.ADOWEER A008 C0D6h, S12ADC1.ADOWEER A008 C4D6h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	TSOWE	DIAGOWE	DOWE	DAOWE	DBOWE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBOWE	A/D Data Duplication Register B Overwrite Error	0: No overwrite error occurred in ADDBLDRB. 1: An overwrite error occurred in ADDBLDRB.	R
b1	DAOWE	A/D Data Duplication Register A Overwrite Error	0: No overwrite error occurred in ADDBLDRA. 1: An overwrite error occurred in ADDBLDRA.	R
b2	DOWE	A/D Data Duplication Register Overwrite Error	0: No overwrite error occurred in ADDBLDR. 1: An overwrite error occurred in ADDBLDR.	R
b3	DIAGOWE	A/D Self-diagnosis Data Register Overwrite Error	0: No overwrite error occurred in ADRD. 1: An overwrite error occurred in ADRD.	R
b4	TSOWE	A/D Temperature Sensor Data Register Overwrite Error	0: No overwrite error occurred in ADTSDR. 1: An overwrite error occurred in ADTSDR.	R
b15 to b5	—	Reserved	These bits are read as 0.	R

DBOWE Bit (A/D Data Duplication Register B Overwrite Error)

DBOWE bit is set to 1 when the results of the next A/D conversion are stored in the ADDBLDRB register after the A/D conversion finishes without the results of A/D conversion in the ADDBLDRB register being read.
DBOWE bit is cleared to 0 when 1 is written to the ADERCLR.OWEC register. DBOWE bit cannot be written to 1.

DAOWE Bit (A/D Data Duplication Register A Overwrite Error)

DAOWE bit is set to 1 when the results of the next A/D conversion are stored in the ADDBLDRA register after the A/D conversion finishes without the results of A/D conversion in the ADDBLDRA register being read.
DAOWE bit is cleared to 0 when 1 is written to the ADERCLR.OWEC register. DAOWE bit cannot be written to 1.

DOWE Bit (A/D Data Duplication Register Overwrite Error)

DOWE bit is set to 1 when the results of the next A/D conversion are stored in the ADDBLDR register after the A/D conversion finishes without the results of A/D conversion in the ADDBLDR register being read.
DOWE bit is cleared to 0 when 1 is written to the ADERCLR.OWEC register. DOWE bit cannot be written to 1.

DIAGOWE Bit (A/D Self-diagnosis Data Register Overwrite Error)

DIAGOWE bit is set to 1 when the results of the next A/D conversion are stored in the ADRD register after the A/D conversion finishes without the results of A/D conversion in the ADRD register being read.
DIAGOWE bit is cleared to 0 when 1 is written to the ADERCLR.OWEC register. DIAGOWE bit cannot be written to 1.

TSOWE Bit (A/D Temperature Sensor Data Register Overwrite Error)

TSOWE bit is set to 1 when the results of the next A/D conversion are stored in the ADTSDR register after the A/D conversion finishes without the results of A/D conversion in the ADTSDR register being read.
TSOWE bit is cleared to 0 when 1 is written to the ADERCLR.OWEC register. TSOWE bit cannot be written to 1.

43.3 Operation

43.3.1 Scanning Operation

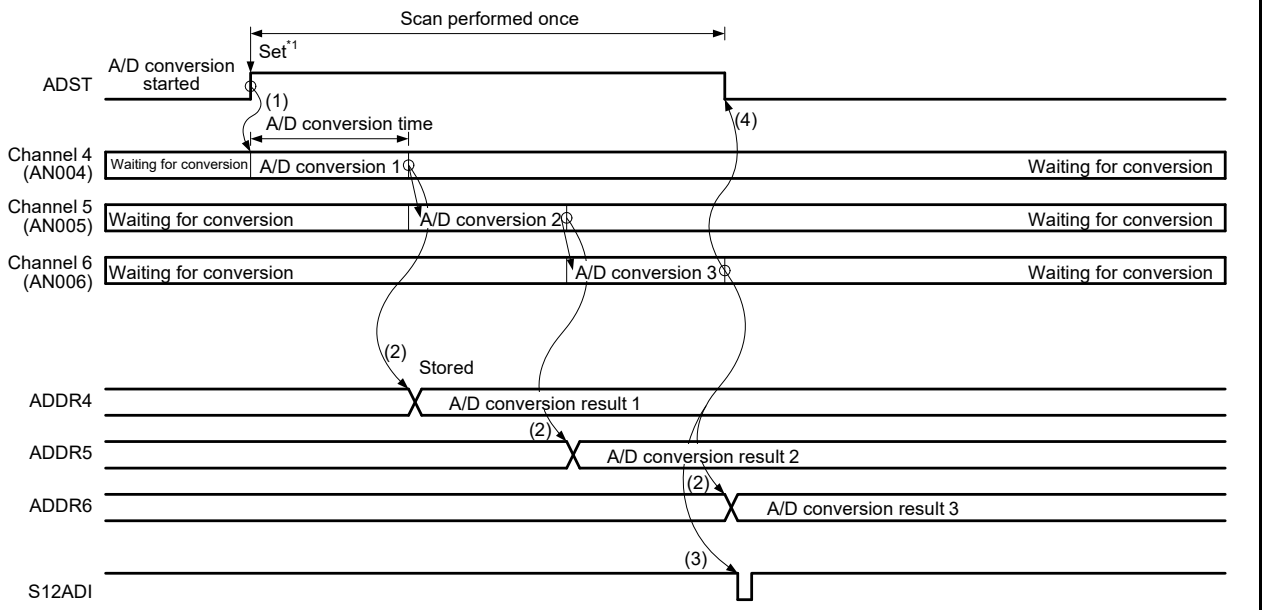
In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.
There are three operating modes: single scan mode, continuous scan mode, and group scan mode. In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADST bit in ADCSR is cleared to 0 from 1. In group scan mode, the selected channels of group A and the selected channels of group B are scanned once after starting to be scanned according to the respective synchronous triggers (MTU3a, GPTa, TPUa, ELC).
In single scan mode and continuous scan mode, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the pin with the smallest number n. In group scan mode, A/D conversion is performed for ANn pins selected by the ADANSA register for group A, and performed for ANn pins selected by the ADANSB register for group B, respectively, starting from the pin with the smallest number n.
When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three voltages internally generated in the 12-bit A/D converter is converted.
The temperature sensor output can be scanned at the same time as the analog input of channels, and A/D conversion of the analog input of channels and the temperature sensor output is performed in that order.
When the extended analog input is selected, A/D conversion should be performed in single scan mode or continuous scan mode.
Double trigger mode is to be used with single scan mode or group scan mode. With double trigger mode being enabled, A/D conversion data of a channel selected by the DBLANS[4:0] bits in ADCSR is duplicated only if the conversion is started by any of the synchronous triggers (MTU3a, GPTa, TPUa, ELC) selected by the TRSA[5:0] bits in ADSTRGR.
To enable double trigger extended mode, select double trigger mode, and then select the synchronous trigger TRGnAN or TRGnBN (n = 4, 7), or GTADTRAmN or GTADTRBmN (m = 0 to 3) as the trigger for starting A/D conversion. In double trigger extended mode, in addition to the usual double trigger mode operation, the A/D conversion data is stored in the A/D data duplication register A (ADDBLDRA) or A/D data duplication register B (ADDBLDRB), depending on the selected trigger.
If two types of trigger sources (TRGnAN and TRGnBN (n = 4, 7), or GTADTRAmN and GTADTRBmN (m = 0 to 3)) occur at the same time, the A/D conversion data is stored in the data duplication register B (ADDBLDRB), instead of the data being sorted by the trigger source. If a new trigger is input during A/D conversion caused by another trigger, the former new trigger is ignored.
When any of AN000 to AN003 channels is set for a channel-dedicated sample-and-hold circuit by the SHANS[3:0] bits in ADSHCR, the target analog input specified is sampled and held before the first A/D conversion of each scan.

43.3.2 Single Scan Mode

43.3.2.1 Basic Operation (without Channel-Dedicated Sample-and-Hold Circuits)

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as below.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the pin with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion is enabled).
(4) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



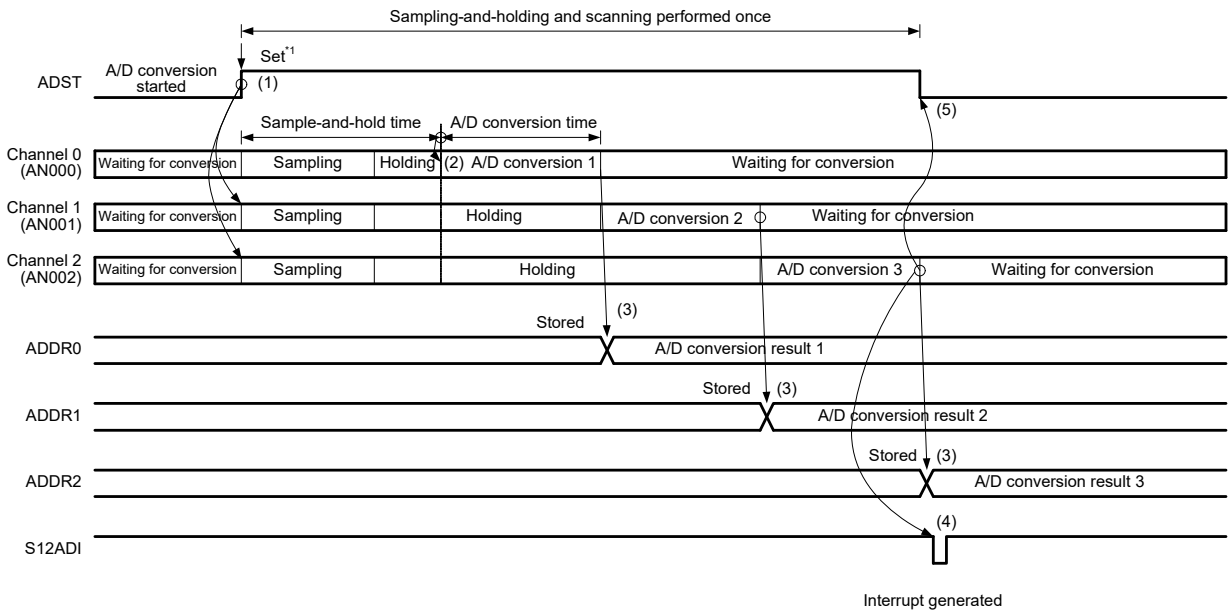
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.4 Example of Operation in Single Scan Mode (Basic Operation: AN004 to AN006 Selected)

43.3.2.2 Basic Operation (with Channel-Dedicated Sample-and-Hold Circuits)

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the selected channels as below. The channels whose channel-dedicated sample-and-hold circuit is to be used can be selected by the SHANS[3:0] bits in ADSHCR.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion is enabled).
(5) The ADST bit in ADCSR remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



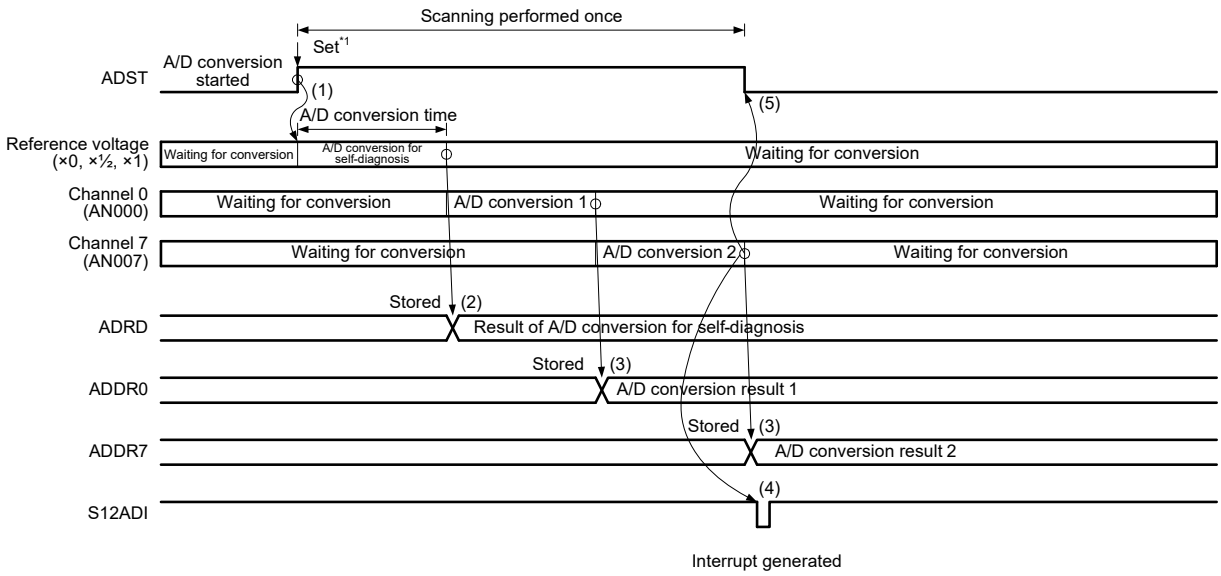
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.5 Example of Operation in Single Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used: AN000 to AN002 Selected)

43.3.2.3 Channel Selection and Self-Diagnosis (without Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH1 (unit 1) (reference voltage ×0, ×1/2, or ×1) supplied to the A/D converter, and then A/D conversion is performed once on the analog input of the selected channels as below.

(1) A/D conversion for self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).
(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



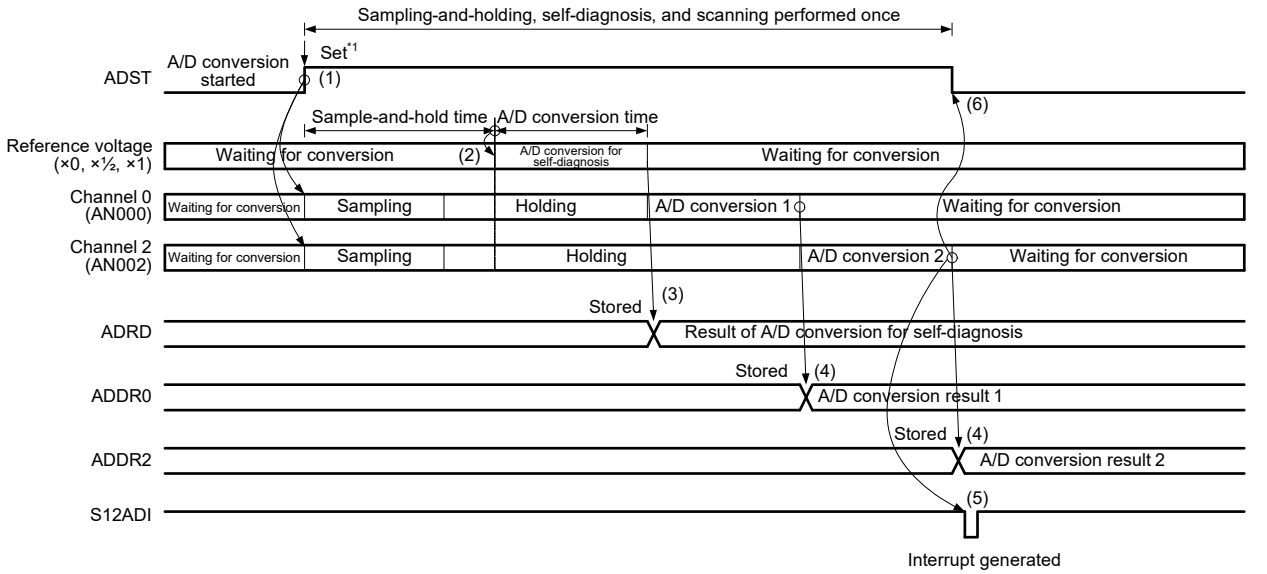
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.6 Example of Operation in Single Scan Mode (Basic Operation: AN000 and AN007 Selected + Self-Diagnosis)

43.3.2.4 Channel Selection and Self-Diagnosis (with Channel-Dedicated Sample-and-Hold Circuits)

When the channel-dedicated sample-and-hold circuit is used and channels and self-diagnosis are selected, sample-and-hold operation is first performed, and then A/D conversion is performed once for the reference voltage VREFH0 (unit 0) or VREFH1 (unit 1) (reference voltage ×0, ×1/2, or ×1) supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed only once on the analog input of the selected channels. The ADSHCR.SHANS[3:0] bits are used to select the channels for which the channel-dedicated sample-and-hold circuit is used.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is started by self-diagnosis.
(3) When A/D conversion due to self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(5) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled).
(6) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



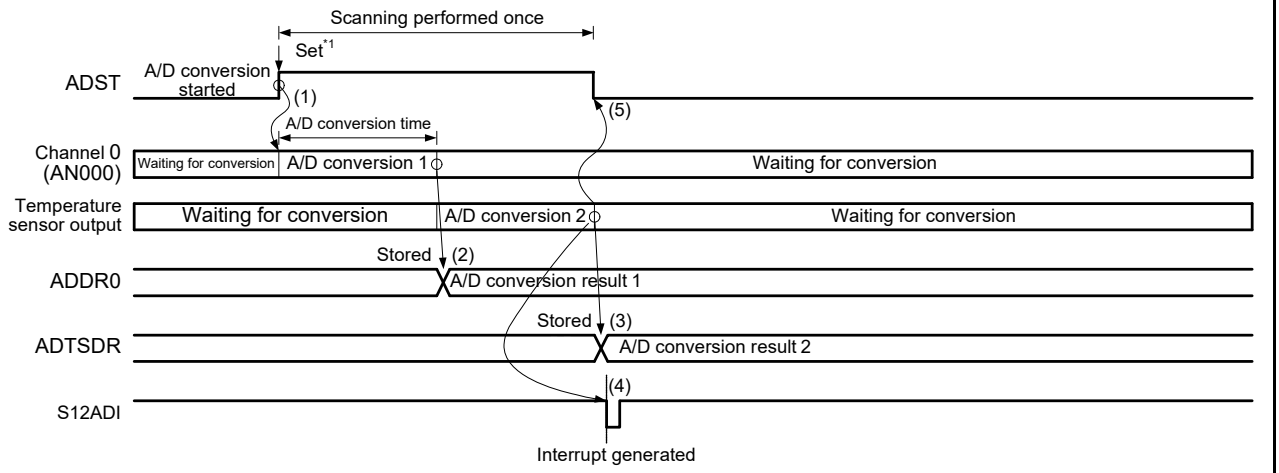
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.7 Example of Operation in Single Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used; AN000 and AN002 Selected + Self-Diagnosis)

43.3.2.5 A/D Conversion of Temperature Sensor Output

When the channels and temperature sensor output are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion is performed once on the temperature sensor output as below.
With the channels deselected, selecting only the temperature sensor output is also possible.

(1) When software, synchronous trigger (MTU3a, GPTa, TPUa, ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn pins selected in the ADANSA register starts in order from the channel with the lowest number n.
(2) On completion of A/D conversion on the channel, the result is stored in the corresponding A/D data register (ADDRy), and then A/D conversion of temperature sensor output starts.
(3) On completion of A/D conversion of temperature sensor output, the result is stored in the corresponding A/D temperature sensor data register (ADTRDR).
(4) If the ADCSR.ADIE bit is set to 1 (enabling S12ADI0 interrupt generation upon scan conversion completion), an S12ADI interrupt is generated.
(5) The ADCSR.ADST bit remains 1 (starting A/D conversion) during A/D conversion, and is automatically cleared to 0 upon completion of A/D conversion. Then the 12-bit A/D converter enters a waiting state.



Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.8 Example of Operation in Single Scan Mode (Basic Operation: AN000 and Temperature Sensor Output Selected)

43.3.2.6 A/D Conversion in Double Trigger Mode

When double trigger mode is selected in single scan mode, A/D conversion is performed for two rounds of single scan operation started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC) as a sequence as shown below.
The temperature sensor output A/D conversion select bits (ADEXICR.TSSA and ADEXICR.TSSB) should be set to 0.
Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1. When the DBLE bit in ADCSR is set to 1, channel selection using the ADANSA register is invalid. In double trigger mode, a synchronous trigger (MTU3a, GPTa, TPUa, ELC) should be selected using the TRSA[5:0] bits in ADSTRGR; the EXTRG bit and TRGE bit in ADCSR should be set to 0 and 1, respectively. Software trigger should not be used.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), A/D conversion is started on the single channel selected by the DBLANS[4:0] bits in ADCSR.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) The ADST bit in ADCSR is automatically cleared to 0 and the 12-bit A/D converter enters a waiting state. Here, an S12ADI interrupt request is not generated irrespective of the ADIE (S12ADI interrupt upon scanning completion enabled) bit setting in ADCSR.
(4) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by the second synchronous trigger input, A/D conversion is started on the single channel selected by the DBLANS[4:0] bits in ADCSR.
(5) When A/D conversion is completed, the A/D conversion result is stored into the A/D data duplication register (ADDBLDR), which is exclusively used in double trigger mode.
(6) If the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion enabled), an S12ADI interrupt is generated.
(7) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion is completed. Then the 12-bit A/D converter enters a waiting state.

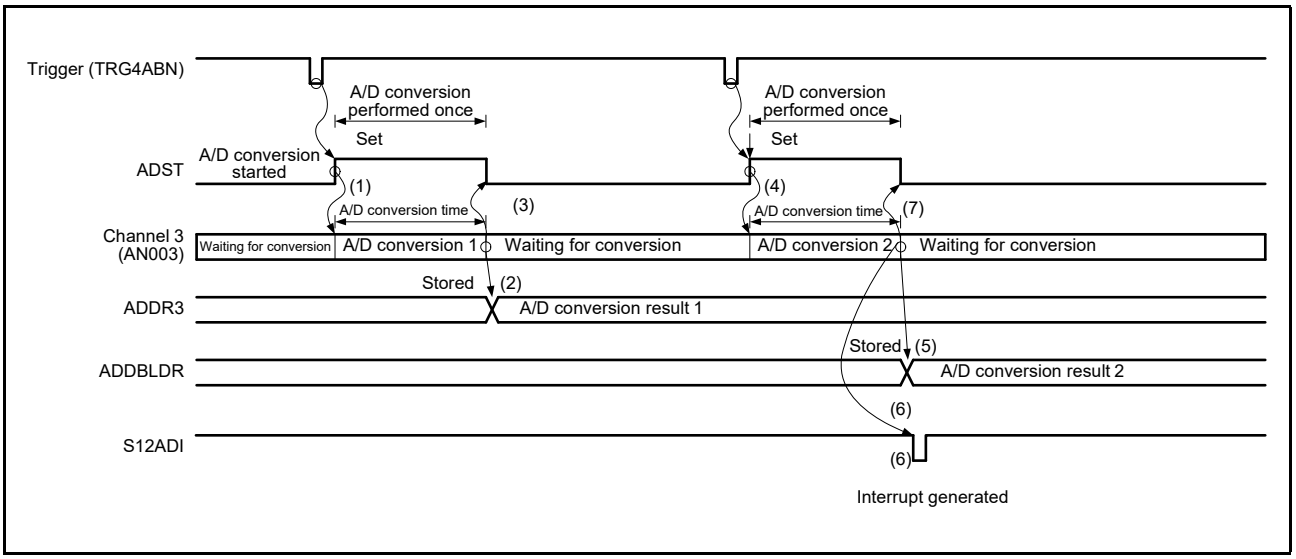


Figure 43.9 Example of Operation in Single Scan Mode (Double Trigger Mode Selected: AN003 Duplicated; TRG4ABN Selected as Trigger; Self-Diagnosis Deselected)

43.3.2.7 Extended Operations When Double Trigger Mode is Selected

When double trigger mode is selected in single scan mode, and a synchronous trigger TRGnAN or TRGnBN (n = 4, 7) is selected as the trigger for the start of A/D conversion (the ADSTRGR.TRSA[5:0] bits are set to 0Bh or 0Fh), or GTADTRAmN or GTADTRBmN (m = 0 to 3) is selected (the ADSTRGR.TRSA[5:0] bits are set to 19h, 1Ah, 1Bh, or 1Ch), the following operations are included with the operations described when double trigger mode is selected.
When A/D conversion is started by a synchronous trigger A (TRGnAN; n = 4, 7, or GTADTRAmN; m = 0 to 3), the results of A/D conversion are stored in A/D data duplication register A (ADDBLDRA). Furthermore, when A/D conversion is started by a synchronous trigger B (TRGnBN; n = 4, 7) or GTADTRBmN (m = 0 to 3), the results of A/D conversion are stored in A/D data duplication register B (ADDBLDRB). With the correspondence between synchronous trigger sources and registers for data storage determined in this way, the target register for storing the results of A/D conversion does not depend on the order of trigger input. Results of A/D conversion are also stored in the A/D data register (ADDRy) and the A/D data duplication register (ADDBLDR) at the same time, and this depends on the order of trigger input.
In extended double trigger mode, if two types of triggers have occurred simultaneously with TRGnAN or TRGnBN (n = 4, 7) or GTADTRAmN or GTADTRBmN (m = 0 to 3) selected, results are not sorted by the trigger sources and are stored in A/D data duplication register B (ADDBLDRB).
Note that if a new trigger source is input during A/D conversion caused by another trigger source, the former new trigger source is ignored and sorting is performed by the latter trigger source.

The extended operations in double trigger mode when the first trigger is TRG4AN with the synchronous trigger TRG4AN or TRG4BN selected as the trigger for the start of A/D conversion are performed as follows.

(1) A/D conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts when the TRG4AN input sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(2) The result is stored in A/D data-duplication register A (ADDBLDRA) and in the corresponding A/D data register (ADDRy) on completion of the A/D conversion for the channel.
(3) The ADST bit is automatically cleared and the A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) When the TRG4BN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(5) The result is stored in A/D data-duplication register B (ADDBLDRB) and in the A/D data-duplication register (ADDBLDR) on completion of A/D conversion.
(6) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled).
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters the waiting state.

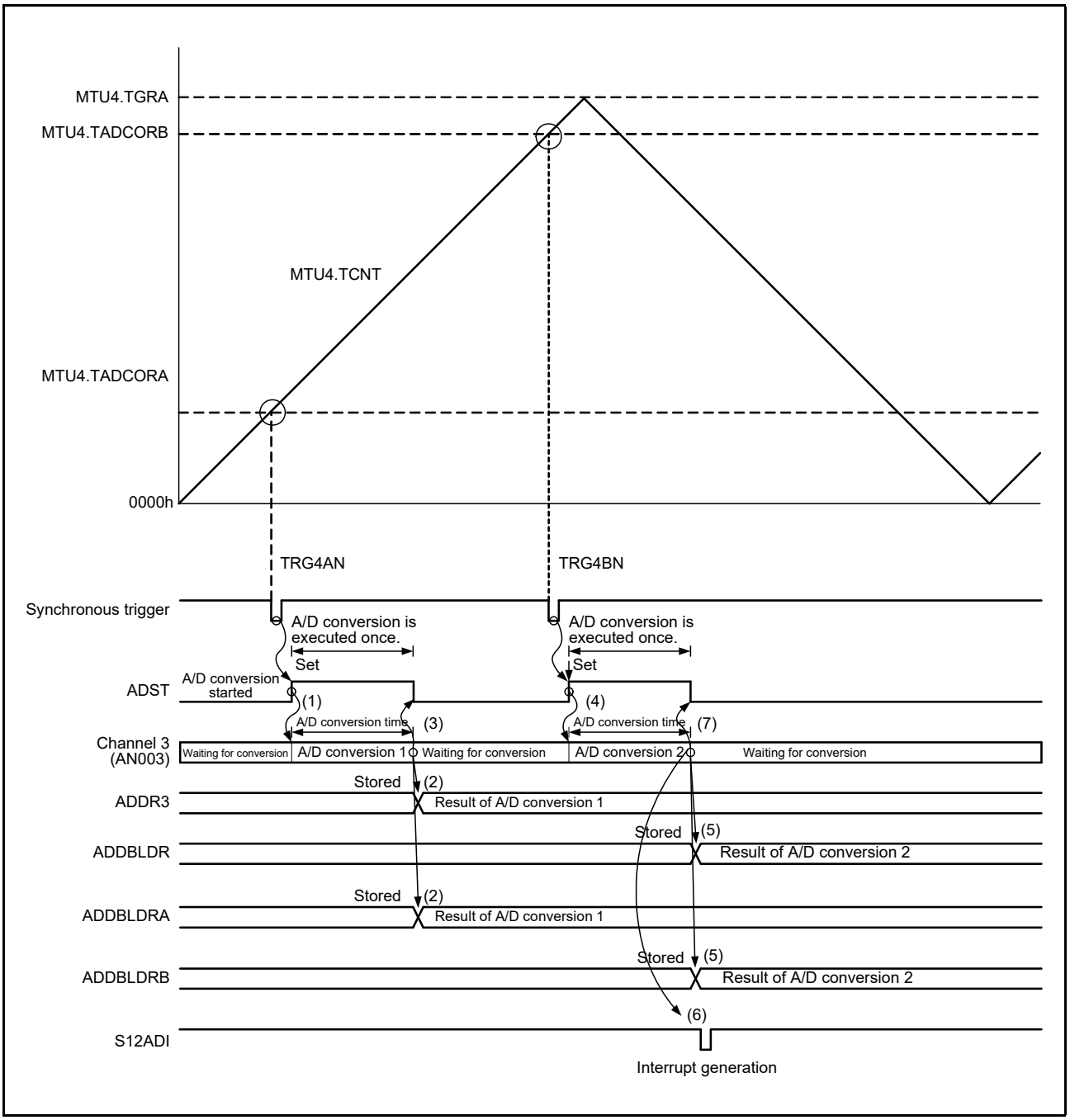


Figure 43.10 Example of Extended Operation in Double Trigger Mode (1)
(Duplication Selected for AN003, TRG4AN or TRG4BN Selected, First Trigger is TRG4AN)

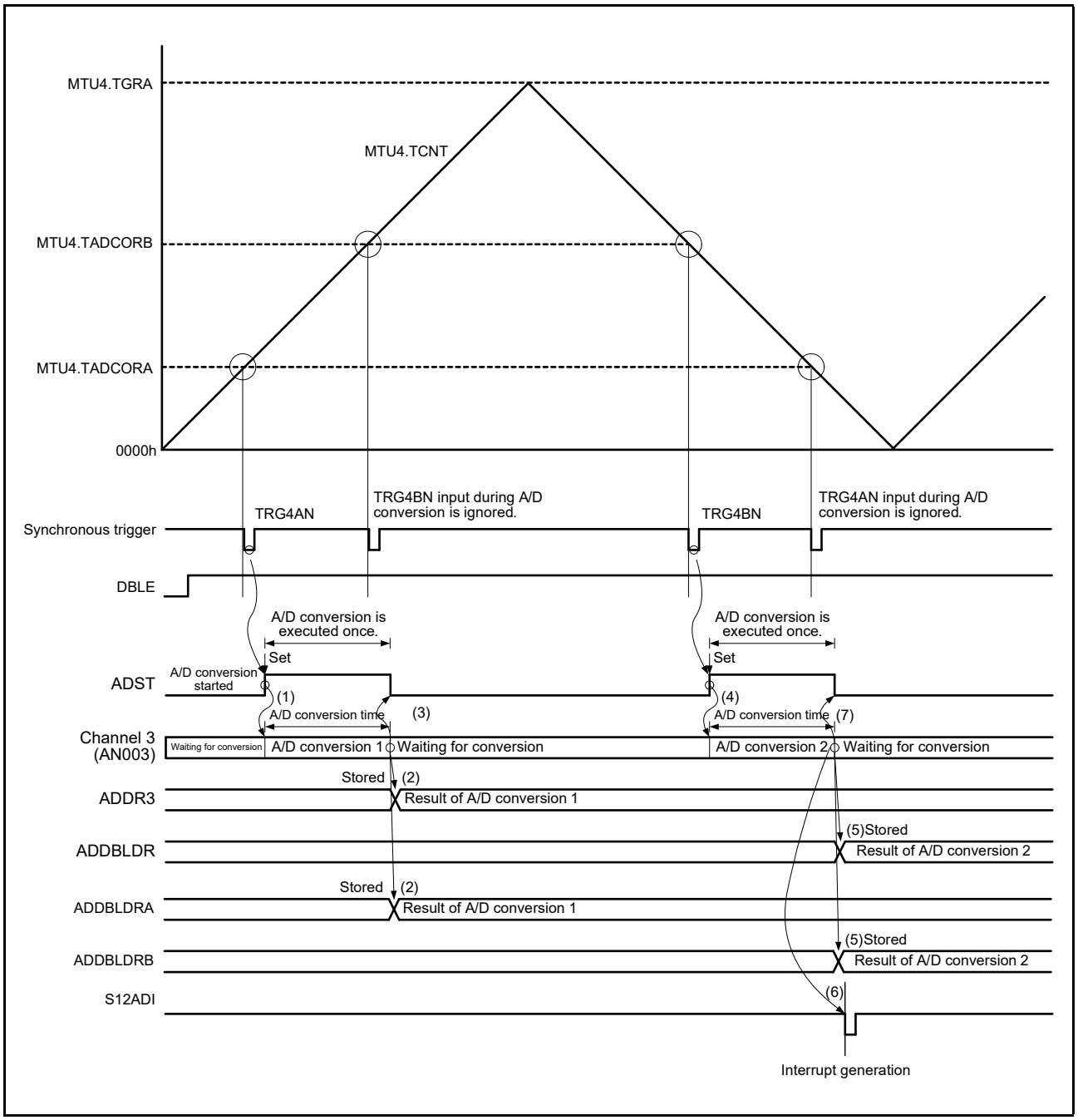


Figure 43.11 Example of Extended Operation in Double Trigger Mode (2)
(Duplication Selected for AN003, TRG4AN and TRG4BN Selected, First Trigger is TRG4AN)

The following describes the extended operations in double trigger mode in response to TRG4BN as the first trigger, again in the case where TRG4AN or TRG4BN is selected as the synchronous trigger for the start of A/D conversion.

(1) When the TRG4BN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(2) On completion of A/D conversion, the result is stored in A/D data duplication register B (ADDBLDRB) and in the corresponding A/D data register (ADDRy).
(3) ADST is automatically cleared and the 12-bit A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) When the TRG4AN input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the single channel selected by the ADCSR.DBLANS[4:0] bits starts.
(5) On completion of A/D conversion, the result is stored in A/D data duplication register A (ADDBLDRA) and in the A/D data duplication register (ADDBLDR).
(6) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the 12-bit A/D converter enters the waiting state.

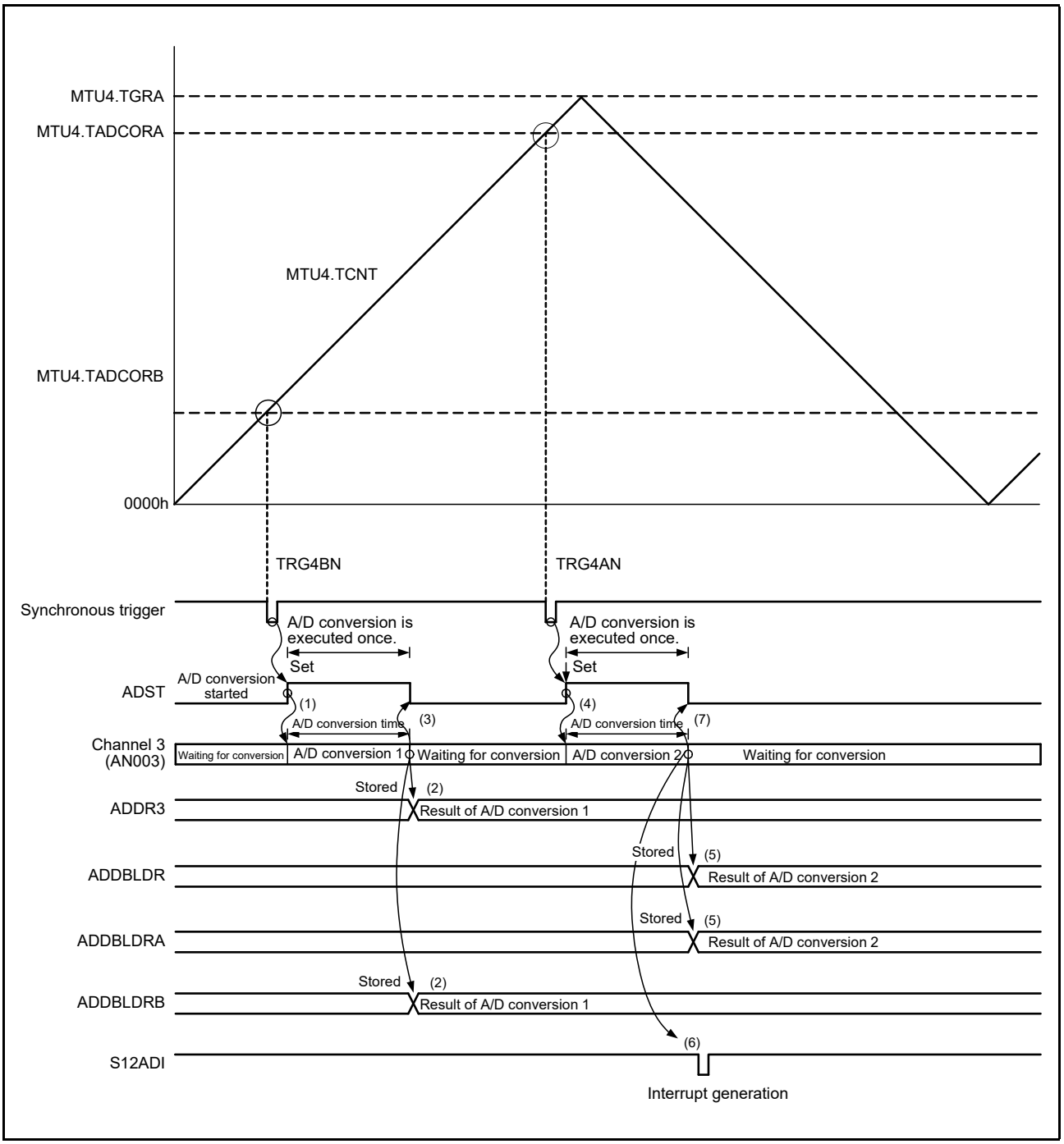


Figure 43.12 Example of Extended Operation in Double Trigger Mode (3)
(Duplication Selected for AN003, TRG4AN and TRG4BN Selected, First Trigger is TRG4BN)

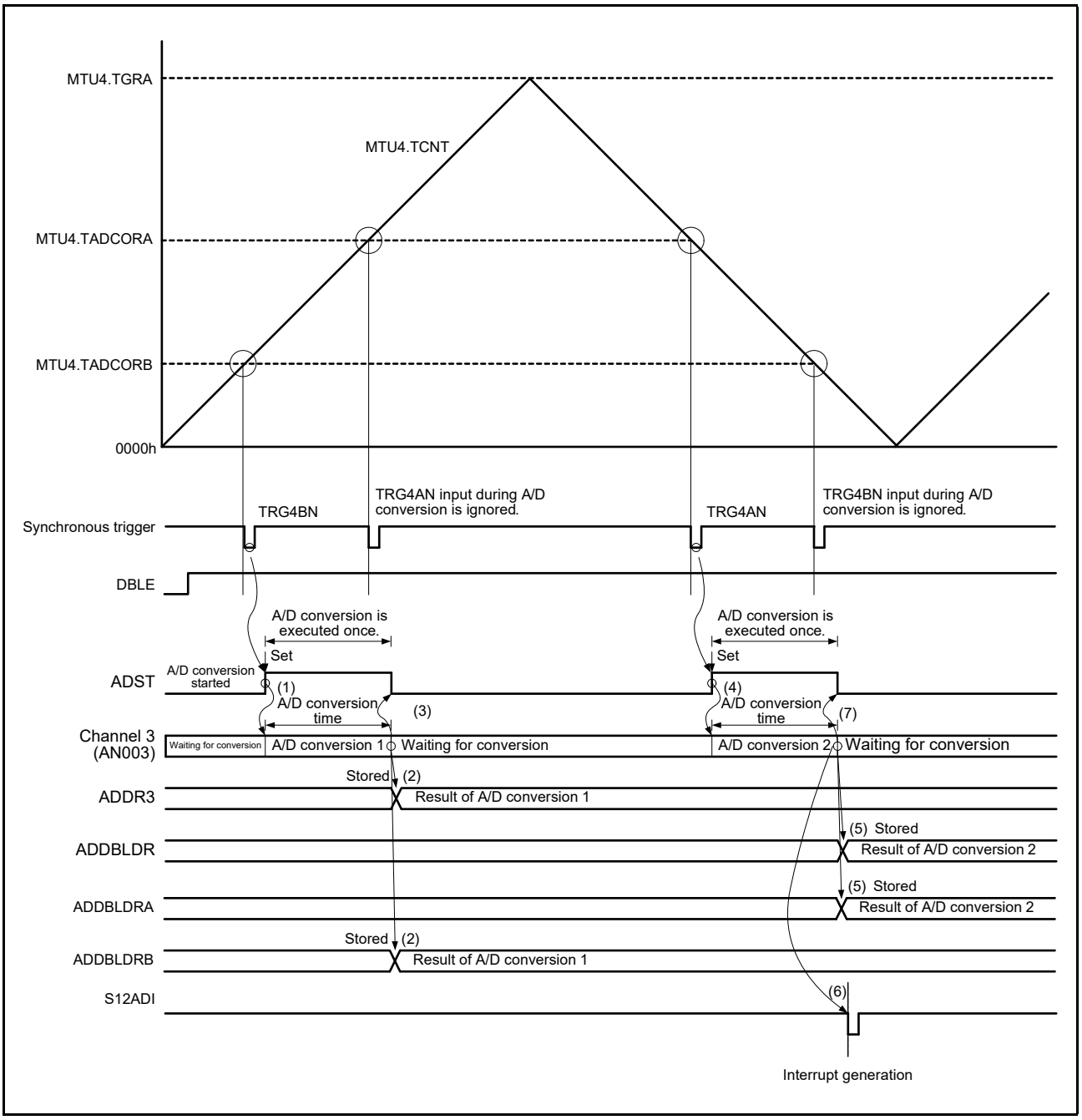


Figure 43.13 Example of Extended Operation in Double Trigger Mode (4)
(Duplication Selected for AN003, TRG4AN and TRG4BN Selected, First Trigger is TRG4BN)

The followings are the extended operations in double trigger mode performed when two types of trigger sources simultaneously occur with the synchronous trigger GTADTRA0N or GTADTRB0N selected as an A/D conversion start trigger.

(1) The first A/D conversion on the single channel selected by the ADCSR.DBLANS[4:0] bits starts when the first simultaneous input of the two trigger sources GTADTRA0N and GTADTRB0N sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(2) The result is stored in A/D data duplication register B (ADDBLDRB) and in the corresponding A/D data register (ADDRy) on completion of the A/D conversion on the channel.
(3) The ADST bit is automatically cleared and the 12-bit A/D converter enters the waiting state. An S12ADI interrupt is not generated at this time, regardless of the setting of the ADCSR.ADIE bit (i.e. whether or not this is set to enable S12ADI interrupts in response to scan completion).
(4) The second A/D conversion on the single channel selected by the ADCSR.DBLANS[4:0] bits starts when the second simultaneous input of the two trigger sources GTADTRA0N and GTADTRB0N sets the ADCSR.ADST bit to 1 (starting A/D conversion).
(5) The result is stored in A/D data duplication register B (ADDBLDRB) and in A/D data duplication register (ADDBLDR) on completion of the A/D conversion.
(6) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (enabling S12ADI interrupt due to completion of the scan).
(7) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the 12-bit A/D converter enters the waiting state.

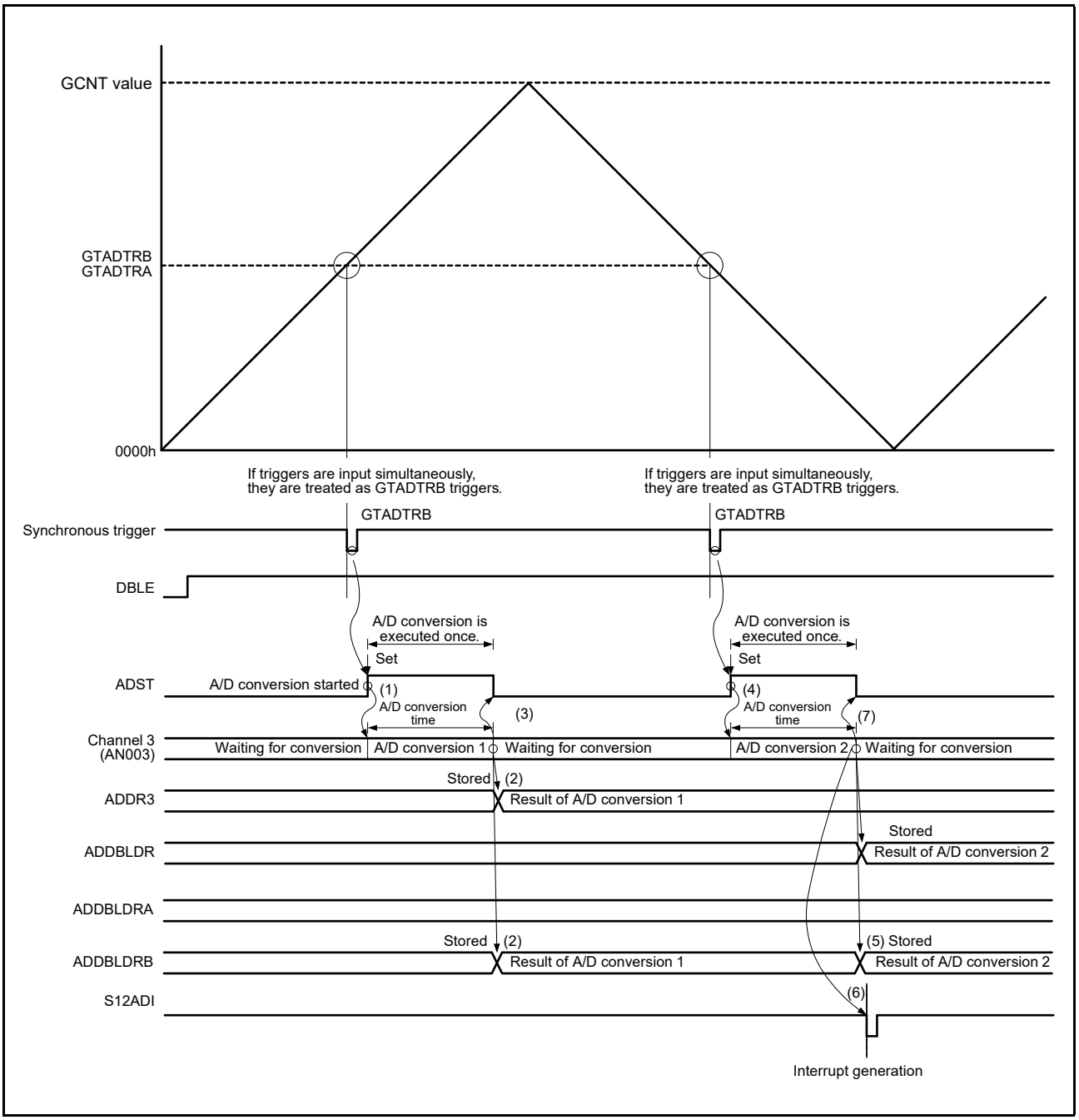


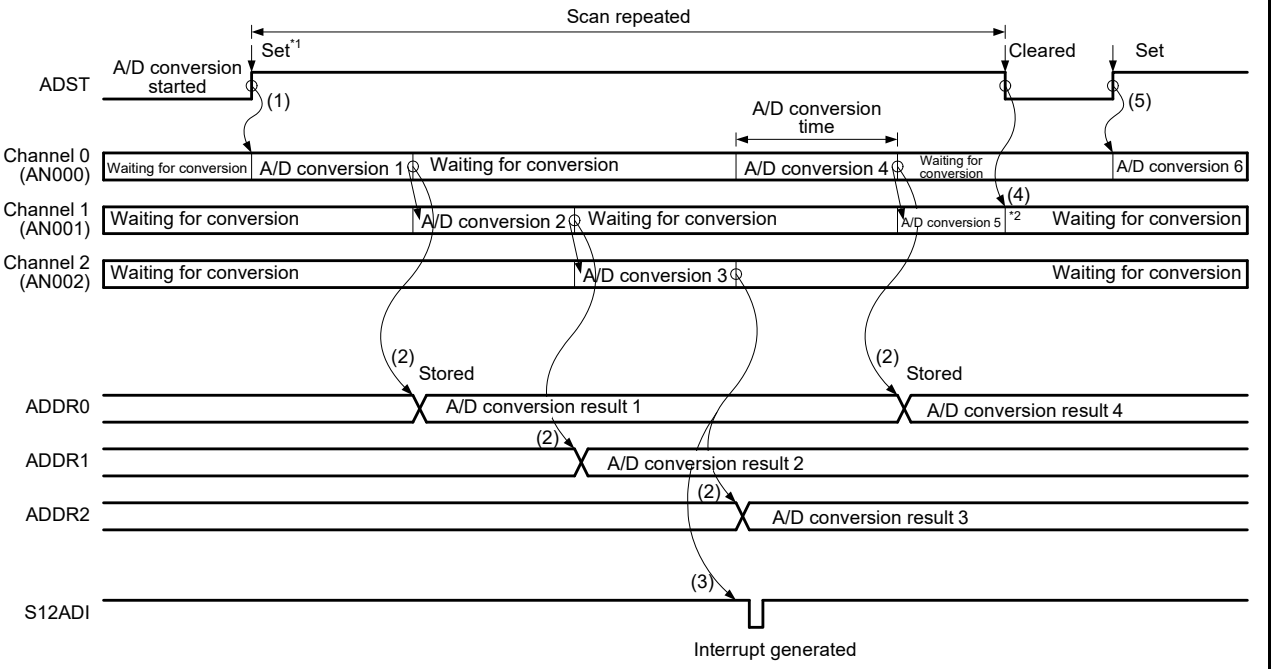
Figure 43.14 Example of Extended Operation in Double Trigger Mode (5) (Duplication Selected for AN003, GTADTRA0N and GTADTRB0N Selected, Two Trigger Sources Simultaneously Occurred)

43.3.3 Continuous Scan Mode

43.3.3.1 Basic Operation (without Channel-Dedicated Sample-and-Hold Circuits)

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the channels selected by the ADANSA register as below.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled).
The 12-bit A/D converter sequentially starts A/D conversion for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(4) The ADST bit in ADCSR is not automatically cleared and steps 2 and 3 are repeated as long as the bit remains 1 (A/ D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a waiting state.
(5) When the ADST bit is later set to 1 (A/D conversion start), A/D conversion is started again for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.



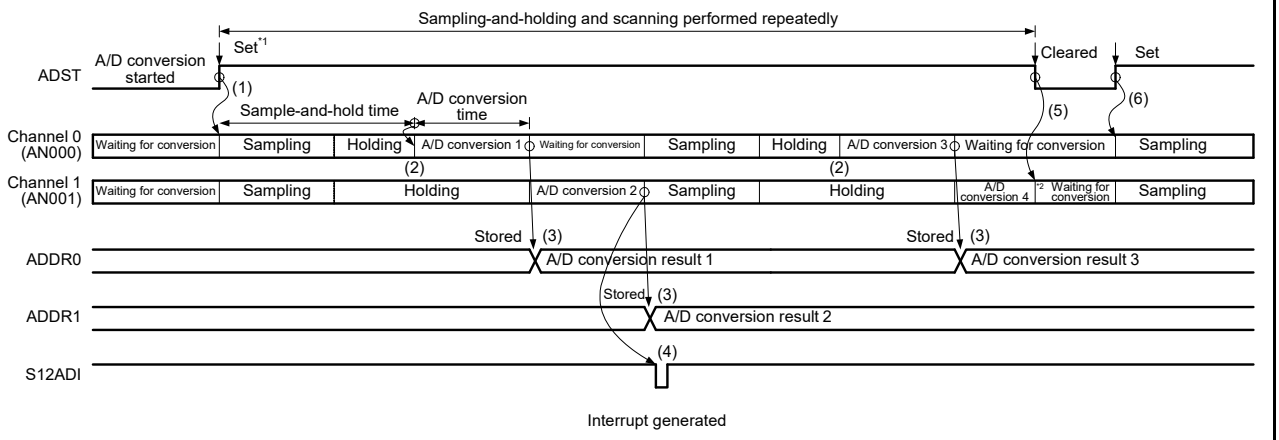
Note 1. The arrows in this figure indicate instruction execution by software.
Note 2. Data for A/D conversion 5 is ignored.

Figure 43.15 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 to AN002 Selected)

43.3.3.2 Basic Operation (with Channel-Dedicated Sample-and-Hold Circuits)

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is repeated on the analog input of all the selected channels as below. The channels whose channel-dedicated sample-and-hold circuit is to be used can be selected by the SHANS[3:0] bits in ADSHCR.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled). At the same time, analog input sampling is started for all the channels whose channel-dedicated sample-and-hold circuit is to be used.
(5) The ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a waiting state.
(6) When the ADST bit is then set to 1 (A/D conversion start), analog input sampling is started again for all the channels whose channel-dedicated sample-and-hold circuit is to be used.



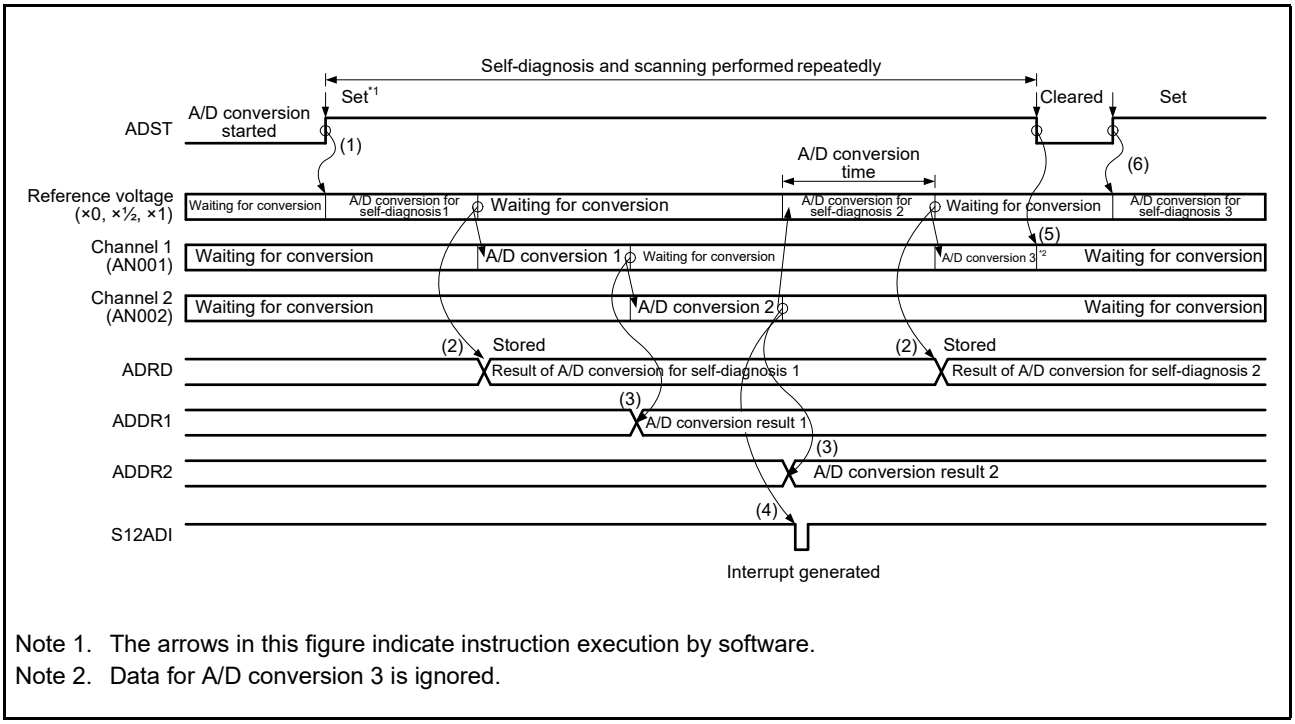
Note 1. The arrows in this figure indicate instruction execution by software.
Note 2. Data for A/D conversion 4 is ignored.

Figure 43.16 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used; AN000 and AN001 Selected)

43.3.3.3 Channel Selection and Self-Diagnosis (without Channel-Dedicated Sample-and-Hold Circuits)

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH1 (unit 1) (reference voltage ×0, ×1/2, or ×1) supplied to the 12-bit A/D converter, and then A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below.

(1) A/D conversion due to self-diagnosis is first started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) When A/D conversion due to self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled). At the same time, the 12-bit A/D converter starts A/D conversion due to self-diagnosis and then starts A/D conversion on ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(5) The ADST bit in ADCSR is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit in ADCSR is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a waiting state.
(6) When the ADST bit is later set to 1 (A/D conversion start), conversion is started again from the A/D conversion due to self-diagnosis.



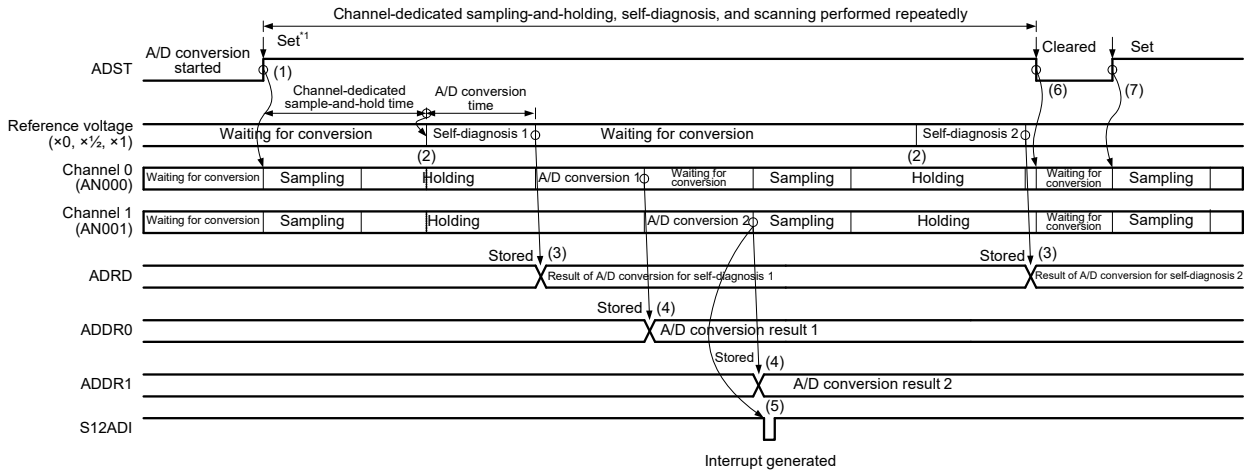
Note 1. The arrows in this figure indicate instruction execution by software.
Note 2. Data for A/D conversion 3 is ignored.

Figure 43.17 Example of Operation in Continuous Scan Mode (Basic Operation; AN001 and AN002 Selected + Self-Diagnosis)

43.3.3.4 Channel Selection and Self-Diagnosis (with Channel-Dedicated Sample-and-Hold Circuits)

When the channel-dedicated sample-and-hold circuit is used and channels and self-diagnosis are selected, sample-and-hold operation is first performed, and then A/D conversion is performed for the reference voltage VREFH0 (unit 0) or VREFH1 (unit 1) (reference voltage ×0, ×1/2, or ×1) supplied to the 12-bit A/D converter, and A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below. The ADSHCR.SHANS[3:0] bits are used to select the channels for which the channel-dedicated sample-and-hold circuit is used.

(1) Analog input sampling of all the channels whose channel-dedicated sample-and-hold circuit is to be used is started when the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input.
(2) After sample-and-hold operation, A/D conversion is started by self-diagnosis.
(3) When A/D conversion due to self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(4) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(5) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion enabled). At the same time, analog input sampling is started for all the channels whose channel-dedicated sample-and-hold circuit is to be used.
(6) The ADST bit is not automatically cleared and steps 2 to 5 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a waiting state.
(7) When the ADST bit is then set to 1 (A/D conversion start), analog input sampling is started again for all the channels whose channel-dedicated sample-and-hold circuit is to be used.



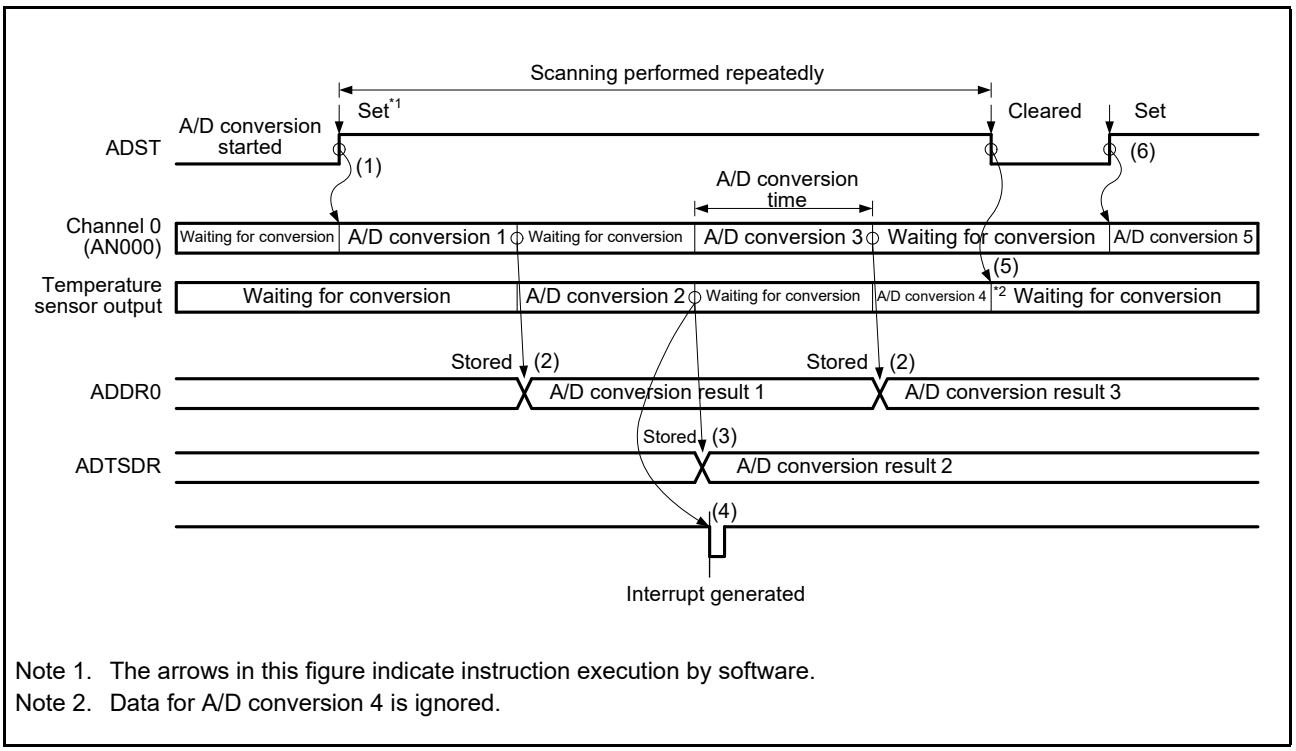
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.18 Example of Operation in Continuous Scan Mode (Channel-Dedicated Sample-and-Hold Circuits Used; AN000 and AN001 Selected + Self-Diagnosis)

43.3.3.5 A/D Conversion of Temperature Sensor Output

When the channels and temperature sensor output are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion of the temperature sensor output is repeated as below. With the channels to be subjected to A/D conversion deselected, selecting only the temperature sensor output is also possible.

(1) When software, synchronous trigger (MTU3a, GPTa, TPUa, ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn pins selected in the ADANSA register starts in order from the channel with the lowest number n.
(2) On completion of A/D conversion on the selected channel, the result is stored in the corresponding A/D data register (ADDRy), and then A/D conversion of temperature sensor output starts.
(3) On completion of A/D conversion of temperature sensor output, the result is stored in the corresponding A/D temperature sensor data register (ADTRDR).
(4) If the ADCSR.ADIE bit is set to 1 (enabling S12ADI interrupt generation upon scan conversion completion), an S12ADI interrupt is generated. Furthermore, the 12-bit A/D converter continuously starts A/D conversion for the ANn pins selected in the ADANSA register in order from the channel with the lowest number n.
(5) The ADCSR.ADST bit is not cleared automatically, and steps 2 to 4 are repeated as long as this bit remains set to 1. When the ADCSR.ADST bit is set to 0 (stopping A/D conversion), A/D conversion stops and the 12-bit A/D converter enters a waiting state.
(6) If the ADCSR.ADST bit is later set to 1 (starting A/D conversion), A/D conversion starts again for ANn pins selected by the ADANSA register in order from the channel with the lowest number n.



Note 1. The arrows in this figure indicate instruction execution by software.
Note 2. Data for A/D conversion 4 is ignored.

Figure 43.19 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 and Temperature Sensor Output or Internal Reference Voltage Selected)

43.3.4 Group Scan Mode

43.3.4.1 Basic Operation

In basic operation of group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A and group B after scanning is started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC) as below. Scan operation of each group is similar to the scan operation in single scan mode.
The synchronous triggers of group A and B can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be set for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger should not be used.
The ADANSA register and the TSSA bit in the ADEXICR register are used to select the channels subject to A/D conversion for group A. The ADANSB register and the TSSB bit in the ADEXICR register are used to select the channels subject to A/D conversion for group B. Group A and group B cannot use the same channels.
When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.
The following describes operation in group scan mode using a trigger of the MTU3a. Specifically, the TRG4AN and TRG4BN triggers of the MTU3a are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group A is started by the TRG4AN trigger of the MTU3a.
(2) When group A scanning is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion is enabled).
(3) Scanning of group B is started by the TRG4BN trigger of the MTU3a.
(4) When group B scanning is completed, an S12GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (S12GBADI interrupt upon scanning completion is enabled).

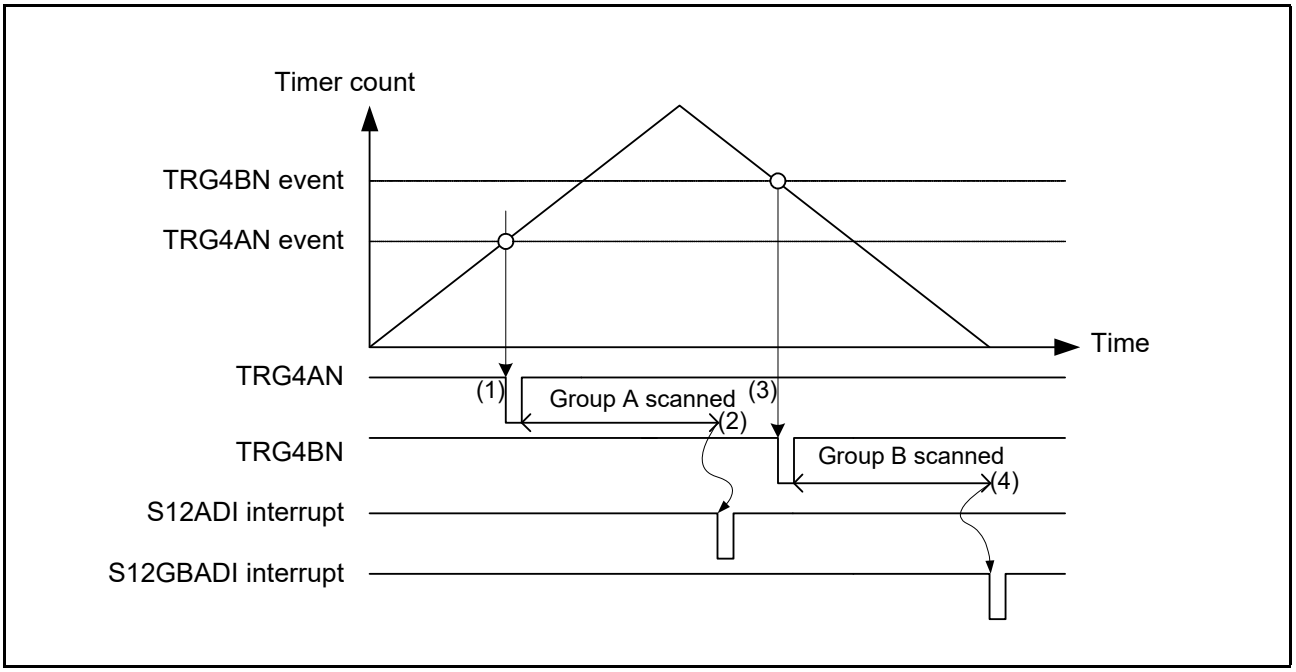


Figure 43.20 Example of Operation in Group Scan Mode (Basic Operation: Triggers from MTU3a Used)

43.3.4.2 A/D Conversion in Double Trigger Mode

When double trigger mode is selected in group scan mode, A/D conversion is performed for two rounds of single scan operation started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC) as a sequence for group A. For group B, single scan operation started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC) is performed once.

In group scan mode, the synchronous triggers of group A and B can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be selected for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger, or asynchronous trigger (ADTRGn) should not be used.

When a synchronous trigger TRGnAN or TRGnBN (n = 4, 7) is selected as the trigger for the start of A/D conversion (the ADSTRGR.TRSA[5:0] bits are set to 0Bh or 0Fh), or GTADTRAmN or GTADTRBmN (m = 0 to 3) is selected (the ADSTRGR.TRSA[5:0] bits are set to 19h, 1Ah, 1Bh, or 1Ch), operation proceeds in extended double trigger mode.

The DBLANS[4:0] bits in the ADCSR register are used to select the channels subject to A/D conversion for group A. The ADANSB register is used to select the channels subject to A/D conversion for group B. The same channels cannot be selected for both groups.

When double trigger mode is selected in group scan mode, the temperature sensor output A/D conversion select bits (ADEXICR.TSSA and ADEXICR.TSSB) should be set to 0 (deselected).

When double trigger mode is selected in group scan mode, self-diagnosis cannot be selected.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the DBLANS[4:0] bits in ADCSR and setting the DBLE bit in ADCSR to 1.

The following describes operation in group scan mode with double trigger mode using a trigger of the MTU3a. Specifically, the TRG4ABN and TRG0AN triggers of the MTU3a are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group B is started by the TRG0AN trigger of the MTU3a.
(2) When group B scanning is completed, an S12GBADI interrupt is generated if the GBADIE bit in ADCSR is 1 (S12GBADI interrupt upon scanning completion is enabled).
(3) The first scanning of group A is started by the first TRG4ABN trigger of the MTU3a.
(4) When the first scanning of group A is completed, the conversion result is stored into the corresponding A/D data register (ADDRy); an S12ADI interrupt is not generated irrespective of the ADIE bit setting in ADCSR.
(5) The second scanning of group A is started by the second TRG4ABN trigger of the MTU3a.
(6) When the second scanning of group A is completed, the conversion result is stored into the ADDBLDR register. An S12ADI interrupt is generated if the ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).

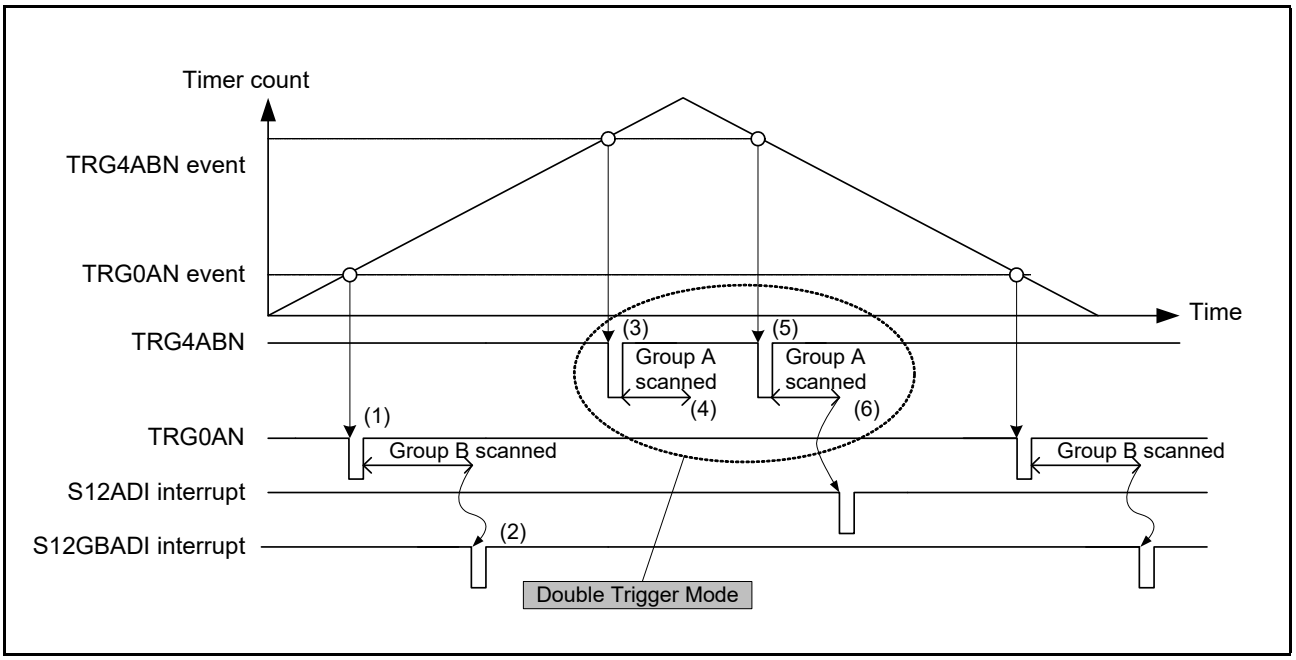


Figure 43.21 Example of Operation in Group Scan Mode with Double Trigger Mode (Basic Operation: Triggers from MTU3a Used)

43.3.4.3 Operation under Group-A Priority Control

Setting the ADGSPCR.PGS bit to 1 in group scan mode makes operation proceed under group-A priority control. When setting the PGS bit in the ADPGSCR register to 1, follow the procedure in Figure 43.22 to set the relevant registers. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.
In operation in basic group scan mode, input of the trigger for the other group during A/D conversion in group A or group B is ignored. Under group-A priority control, if a group-A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the setting of the ADGSPCR.GBRSCN bit is 0, the converter enters the waiting state on completion of the A/D conversion for group A, without restarting the A/D conversion for group B (that was discontinued by the group-A trigger). If the setting of the ADGSPCR.GBRSCN bit is 1, the converter automatically restarts scanning for group B from the head of the group after completion of the A/D conversion for group A. Table 43.9 summarizes operations in response to the input of a trigger during A/D conversion with the settings of the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single scan mode. Furthermore, single scanning for group B continues to proceed if the ADGSPCR.GBRP bit is set to 1.

In group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits and select a synchronous trigger different from that of group A for group B using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1. Furthermore, as targets for A/D conversion, select channels for group A using the ADANSA register and the ADEXICR.TSSA bit, and for group B, select channels different from those for group A using the ADANSB register and the ADEXICR.TSSB bit.

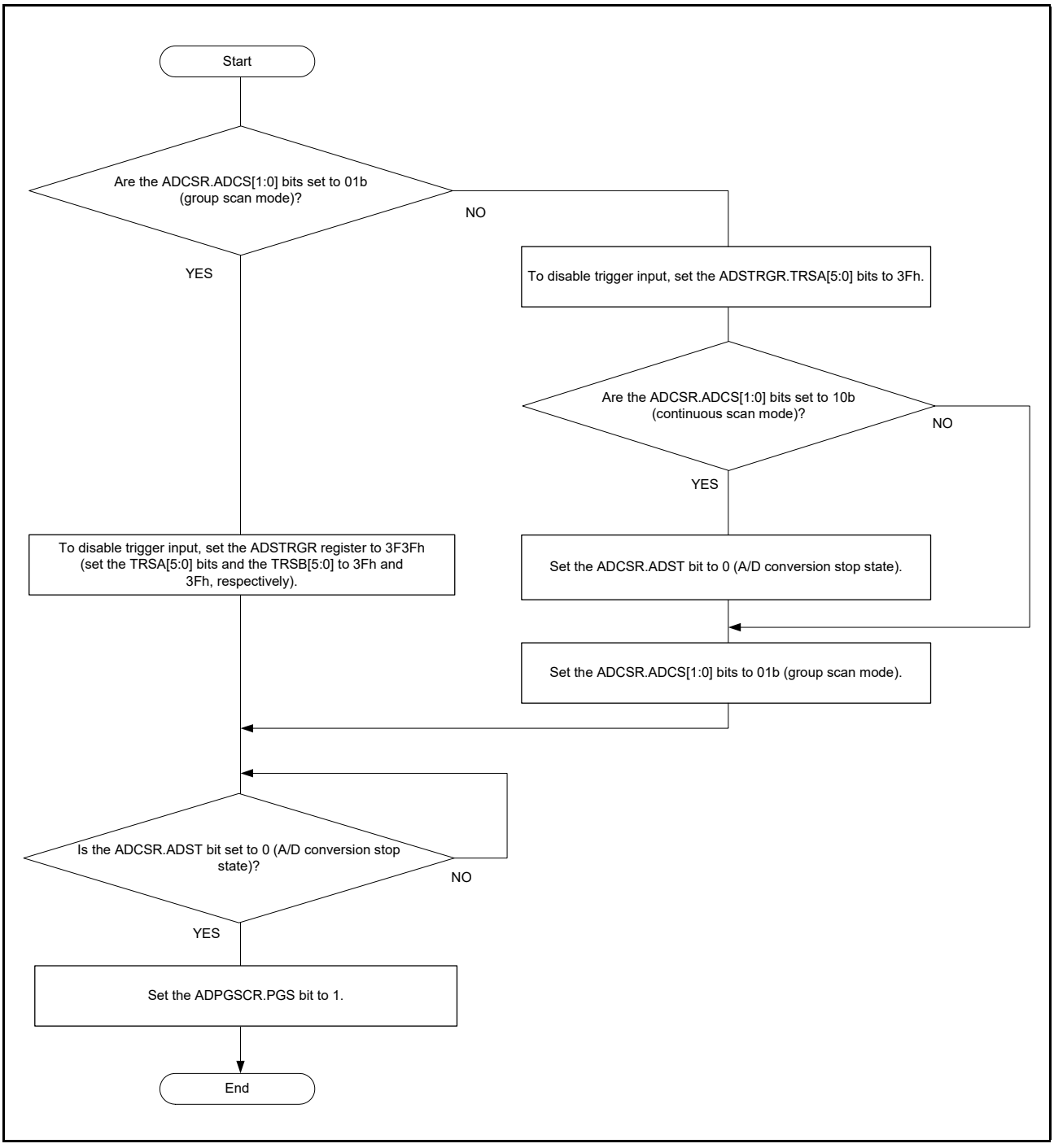


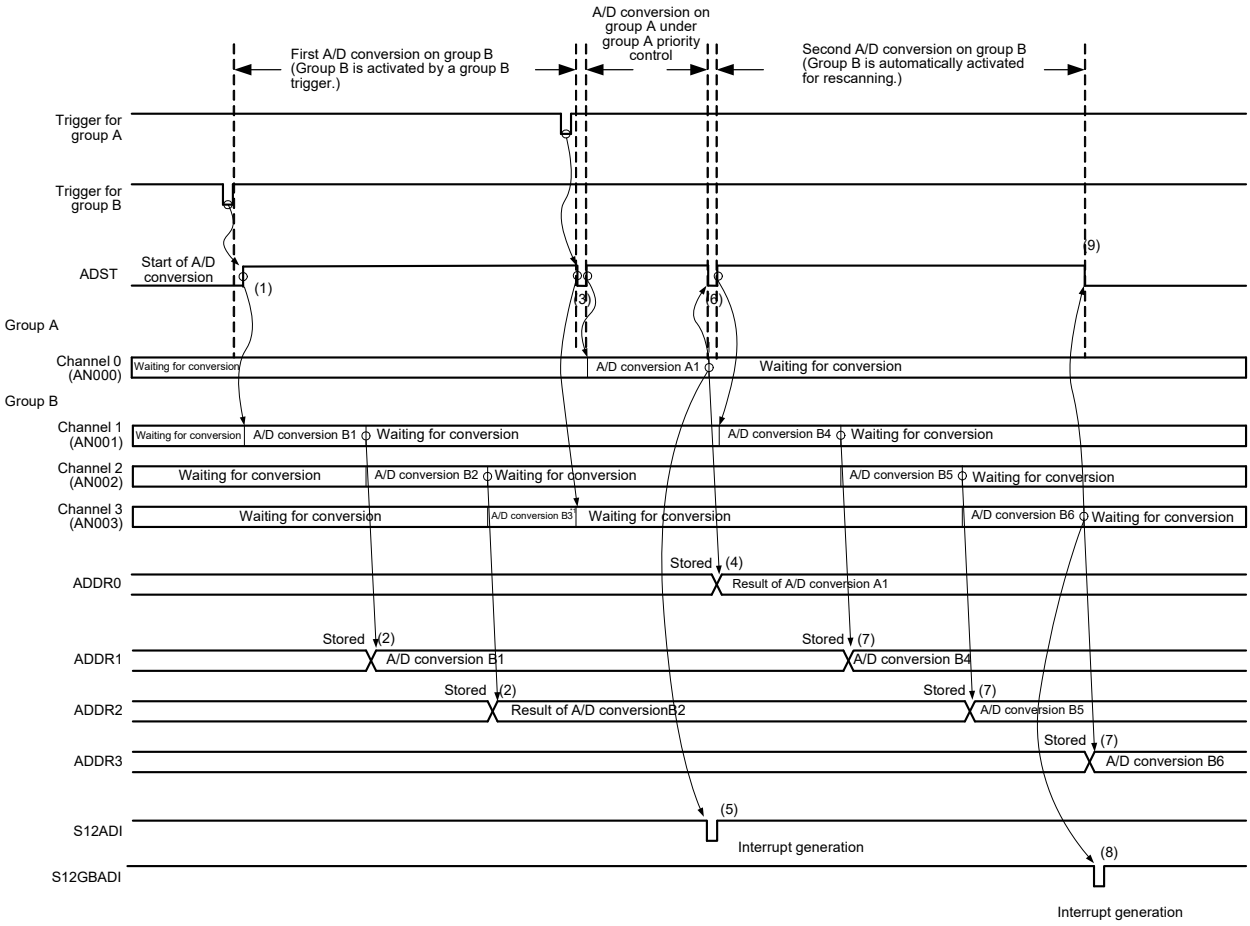
Figure 43.22 Flow of Setting the ADPGSCR.PGS Bit

Table 43.9 Control of A/D Conversion Operations According to the Settings of the ADGSPCR.GBRSCN Bit

A/D Conversion Operation	Trigger Input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion is performed on group B after A/D conversion on group A is completed.
When A/D conversion for group B is in progress	Input of trigger for group A	Conversion for group B that is in progress is discontinued and conversion for group A starts.	• Conversion in progress for group B is discontinued and conversion for group A starts. • Conversion for group B starts after conversion for group A is completed.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

The following describes the operations in group scan mode under group-A priority control (i.e. ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channel pins selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion for a channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is cleared on the input of a trigger for group A while A/D conversion in group B is in progress, and the latter is discontinued. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion), and conversion for the ANn channel pins selected in the ADANSA register starts in order from the channel with the lowest number.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(6) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (starting A/D conversion) and conversion for the ANn channel pins of group B selected in the ADANSB register starts in order from the channel with the lowest number.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) An S12GBADI interrupt is generated if the setting of the ADCSR.GBADIE bit is 1 (S12GBADI interrupt upon group B scanning completion enabled).
(9) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters the waiting state.

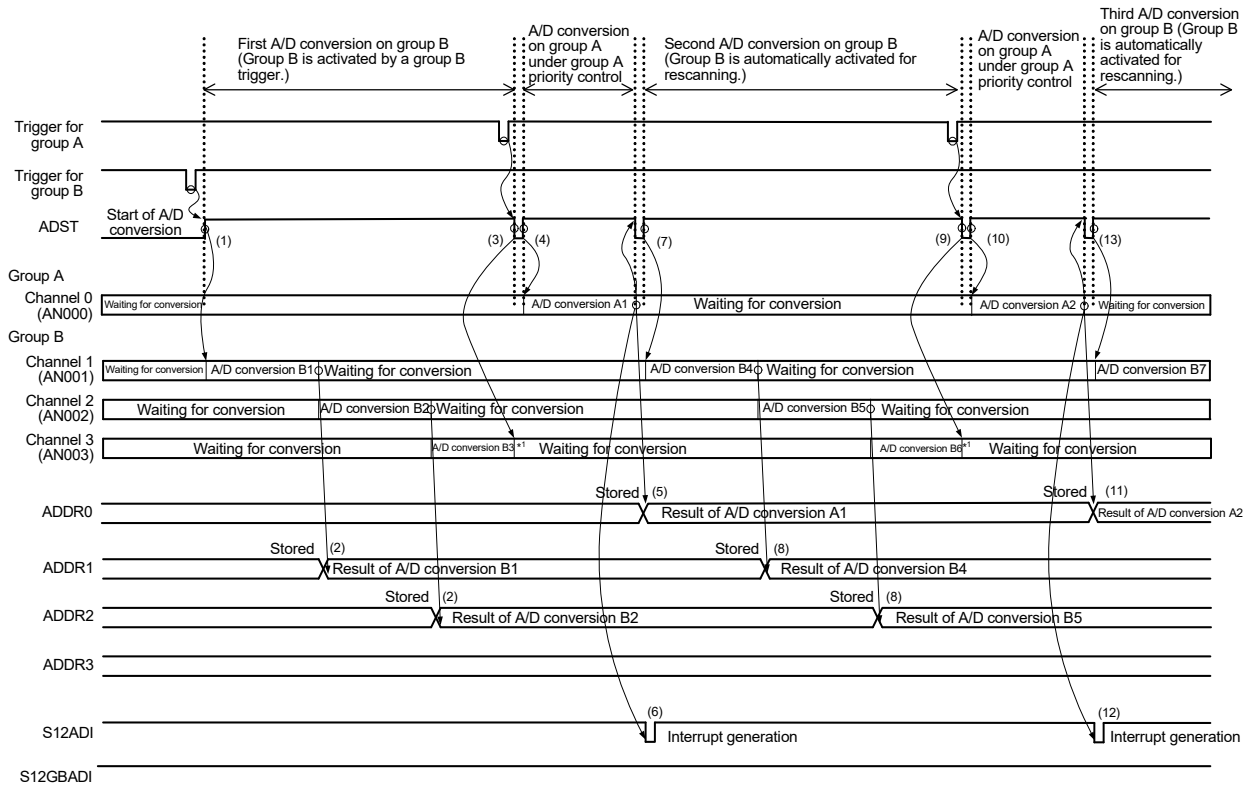


Note 1. Converted data from A/D conversion B3 are ignored.

Figure 43.23 Example of Operations under Group-A Priority Control (1) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example when a group A trigger is input again during rescanning operation on group B. In this example, channel 0 is selected for group A and channels 1 to 3 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When a group B trigger input sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channel pins of group B selected in the ADANSB register starts in order from the channel with the lowest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is cleared to 0 (stopping A/D conversion) on the input of a trigger for group A while A/D conversion in group B is in progress, and the latter is discontinued.
(4) After that, the ADCSR.ADST bit is set to 1 automatically and A/D conversion for the ANn group A channel pins selected in the ADANSA register starts in order from the channel with the lowest number n.
(5) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(6) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(7) On completion of A/D conversion on the group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning operation). After that, A/D conversion for the ANn group B channel pins selected in the ADANSB register starts again in order from the channel with the lowest number n.
(8) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(9) If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit is cleared to 0 (stopping A/D conversion) and the ongoing A/D conversion on group B is stopped.
(10) After that, the ADCSR.ADST bit is set to 1 automatically and A/D conversion for the ANn group A channel pins selected in the ADANSA register starts in order from the channel with the lowest number n.
(11) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(12) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(13) On completion of A/D conversion on group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the setting of the ADGSPCR.GBRSCN bit is 1 (enabling rescanning operation). After that, A/D conversion for the ANn group B channel pins selected in the ADANSB register starts again in order from the channel with the lowest number n.
(14) If a group A trigger is input during A/D conversion on group B for rescanning, steps 9 to 13 are repeated. If a group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on group B and the 12-bit A/D converter enters a waiting state.



Note 1. Conversion data from A/D conversion B3 and B6 are ignored.

Figure 43.24 Example of Operations under Group-A Priority Control (2) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 1 to 3 are selected for group A and channel 0 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When input of a trigger for group A sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channel pins of group A selected in the ADANSA register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group B trigger is input during A/D conversion on group A, A/D conversion on group B can be performed after the A/D conversion on group A is completed. (However, if group A triggers are input continuously, the scan operation on group B is cancelled by conversion on group A and is not performed.)
(4) On completion of the A/D conversion on the group A, an S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(5) On completion of the A/D conversion on the group A, activation of group B for rescanning sets the ADCSR.ADST bit to 1 automatically.
After that, conversion for the ANn channel pins of group B selected in the ADANSB register starts again in order from the channel with the lowest number.
(6) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(7) On completion of the rescanning operation on the group B, an S12GBADI interrupt is generated if the setting of the ADCSR.GBADIE bit is 1 (S12GBADI interrupt upon scanning completion is enabled).
(8) The ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters a waiting state.

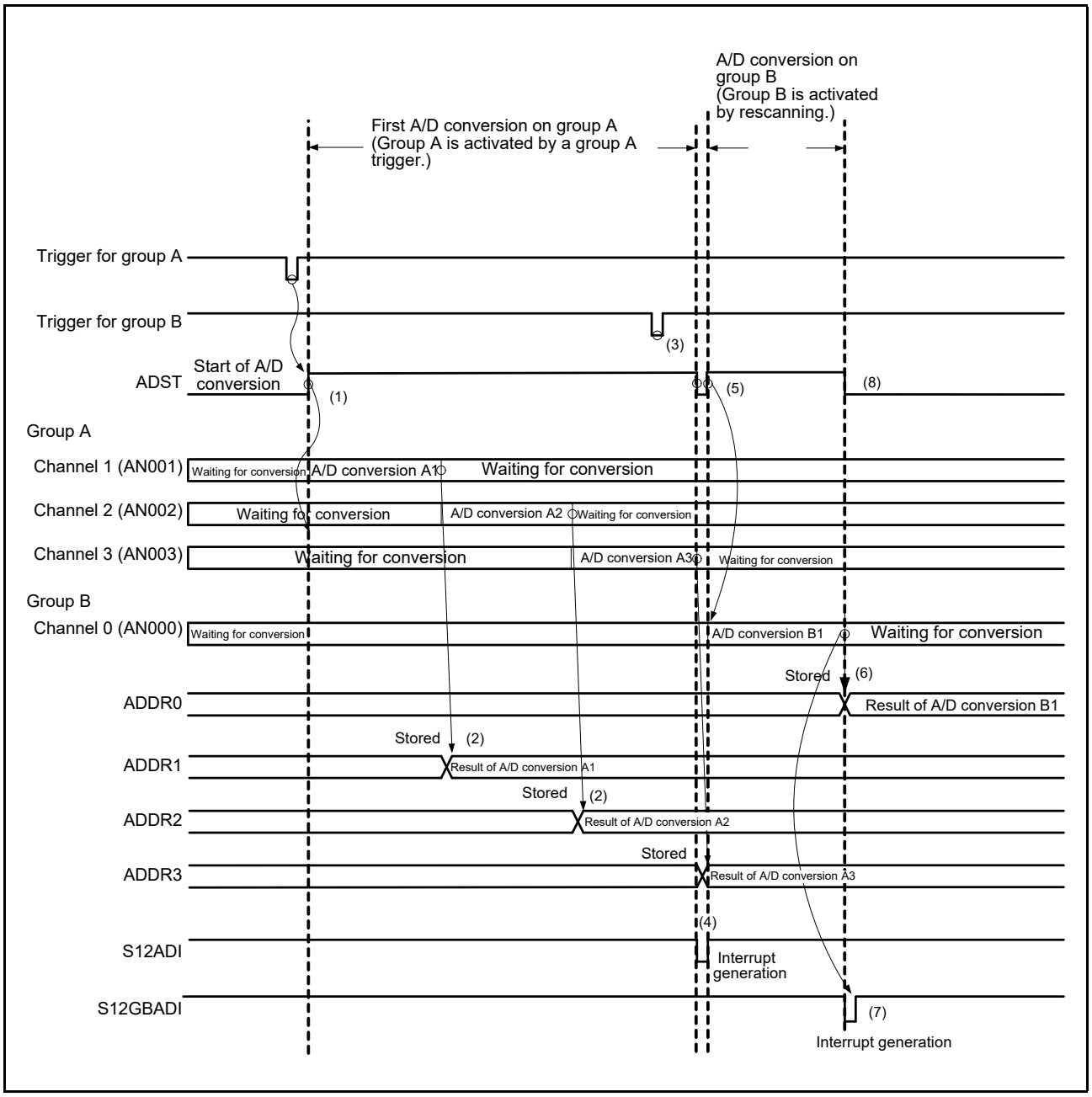
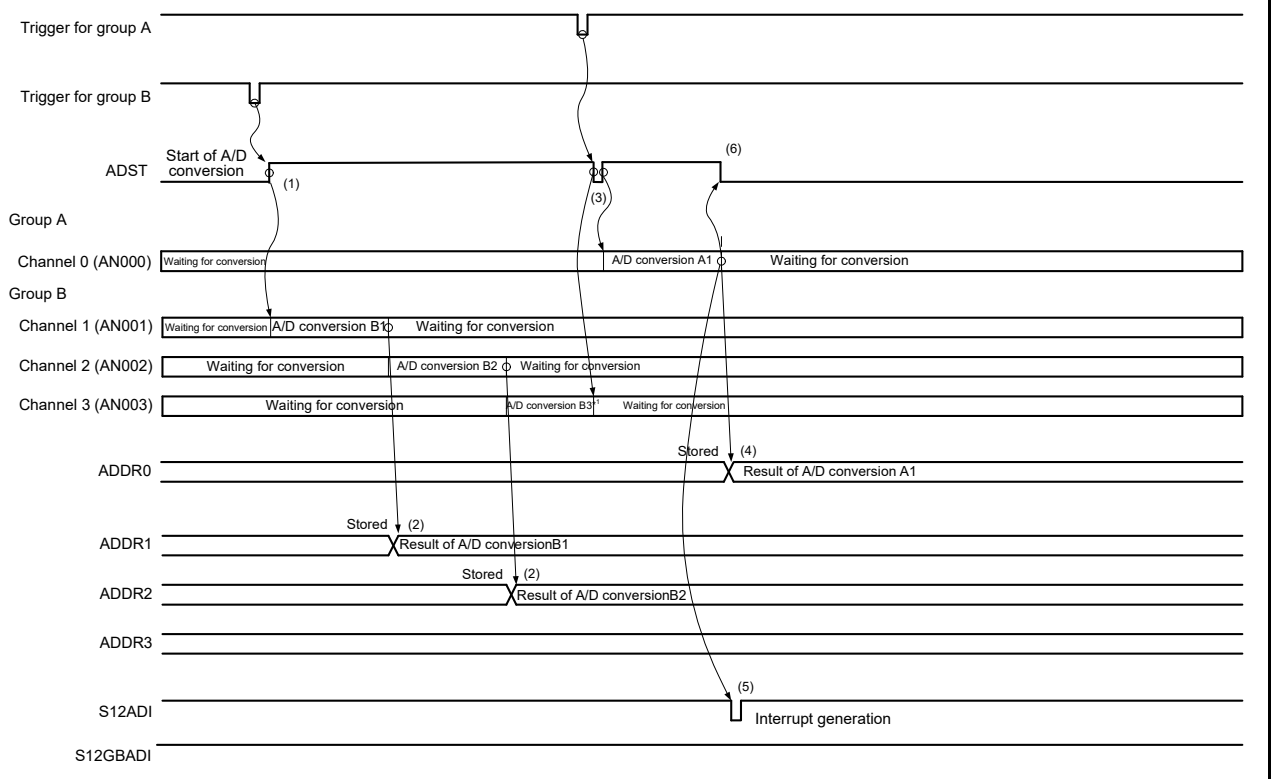


Figure 43.25 Example of Operations under Group-A Priority Control (3) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example of operation under group-A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSCR.GBRSCN = 0, ADGSCR.GBRP = 0).

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (starting A/D conversion), conversion for the ANn channel pins selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and conversion for the ANn channel pins selected in the ADANSA register starts in order from the channel with the lowest number.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(6) The ADCSR.ADST bit retains the value 1 (starting A/D conversion) during A/D conversion and is cleared on completion of conversion, after which the A/D converter enters the waiting state.

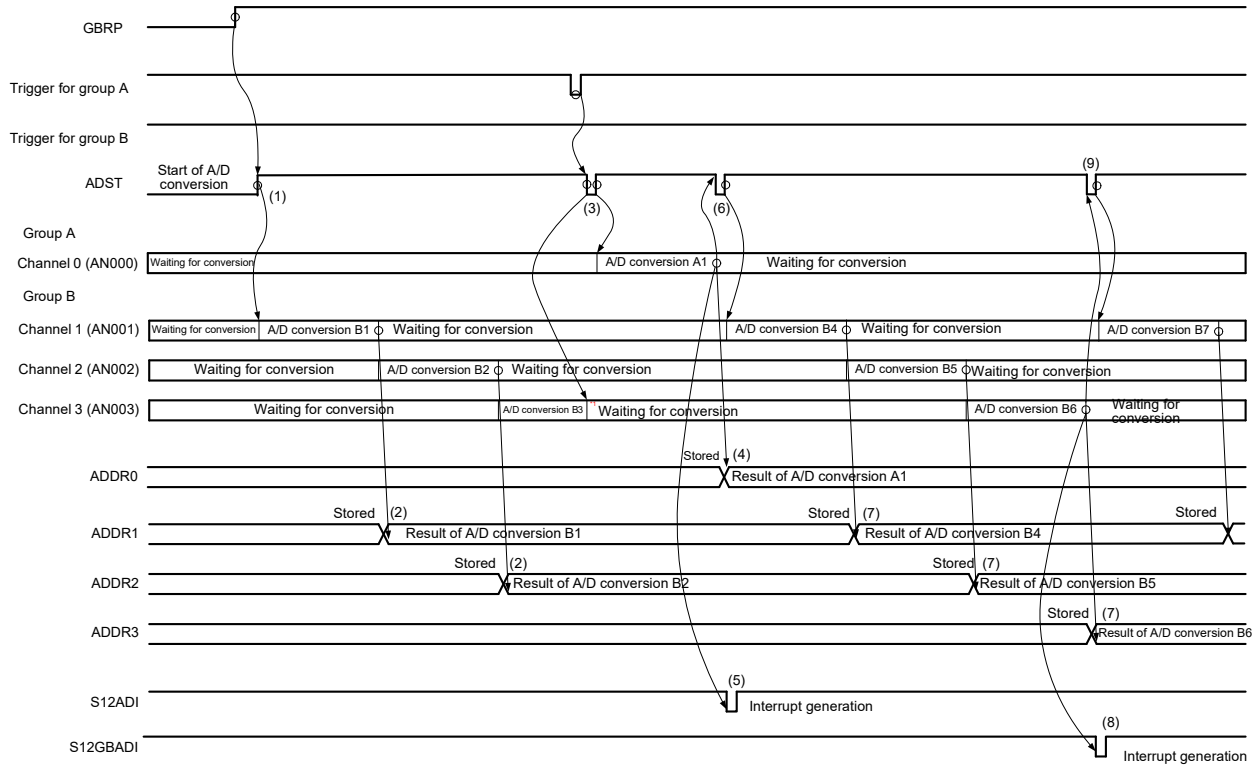


Note 1. The converted data of A/D conversion B3 is ignored.

Figure 43.26 Example of Operation under Group-A Priority Control (4) (when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0)

The following is an example of operation under group A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSCR.GBRP = 1).

(1) The ADCSR.ADST bit is set to 1 (starting A/D conversion) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channel pins selected in the ADANSB register starts in order from the channel with the lowest number.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (starting A/D conversion) and conversion for the ANn channel pins selected in the ADANSA register starts in order from the channel with the lowest number.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI interrupt is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI interrupt upon scanning completion is enabled).
(6) After the ADST bit is automatically cleared and then is automatically set to 1 (starting A/D conversion) again, conversion for the ANn channel pins selected in the ADANSB register starts again in order from the channel with the lowest number.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) An S12GBADI interrupt is generated if the setting of the ADCSR. GBADIE bit is 1 (S12GBADI interrupt upon completion of scanning for group B is enabled).
(9) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (starting A/D conversion), and then conversion for the ANn channel pins selected in the ADANSB register starts again in order from the channel with the lowest number. Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1.
Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 43.40, if you wish to forcibly stop A/D conversion while ADGSPCR.GBRP = 1.



Note 1. Converted data from A/D conversion B3 are ignored.

Figure 43.27 Example of Operation under Group-A Priority Control (5) (when ADGSPCR.GBRP = 1)

43.3.5 Extended Analog Input (Unit 1)

The extended analog input AN1_ANEX1 is used when an external operational amplifier is connected to this LSI to perform
A/D conversion for the multiple analog values. When the extended analog input is selected, AN100 to AN107 can only be selected. Do not select AN108 to AN115, and self-diagnosis function. Also, the disconnection detection assist function cannot be used. Furthermore, when the extended analog input is selected, if the pin-level self-diagnosis function is enabled, the diagnosis is performed for the extended analog input (AN1_ANEX1) and not for AN100 to AN107 and AN1_ANEX0 even if AN100 to AN107 are selected as the targets.

43.3.5.1 Usage of AN1_ANEX1

To perform A/D conversion of the multiple analog values via the operational amplifier, input the analog signal to the analog input channels (AN100 to AN107). Then take out the time-divided analog values from the extended analog output pin (AN1_ANEX0), and connect the operational amplifier between the AN1_ANEX0 pin and AN1_ANEX1 pin.
To select AN1_ANEX1, set the ADEXICR.EXSEL[1:0] bits to 01b. To enable AN1_ANEX0 output, set the ADEXICR.EXOEN bit to 1. Also select single scan mode or continuous scan mode. Do not select group scan mode.
Figure 43.28 shows an example of the extended analog input circuit configuration with AN1_ANEX1 used. Figure 43.29 shows the operation when three channels (AN100, AN101, and AN102) and single scan mode are selected.

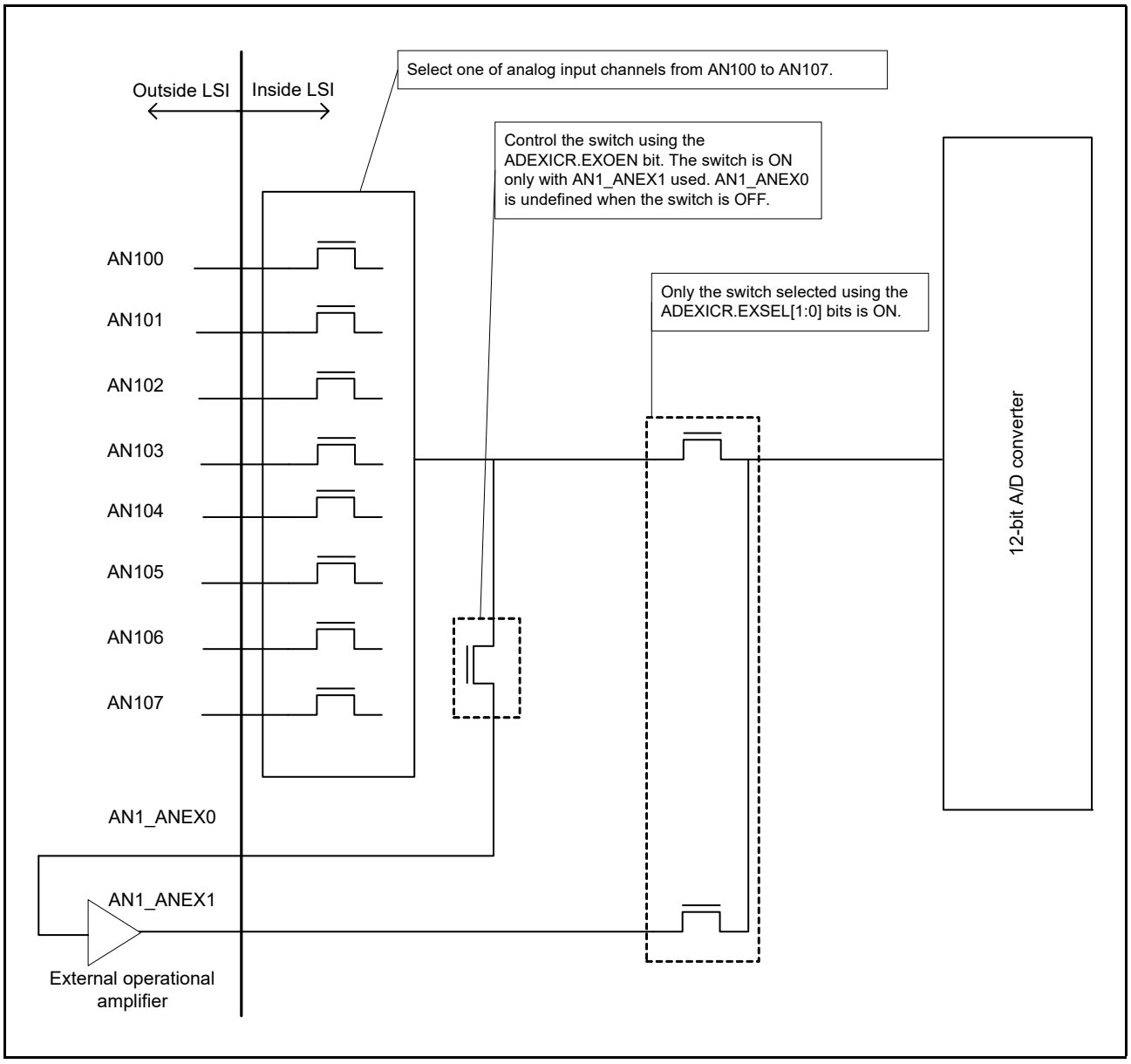


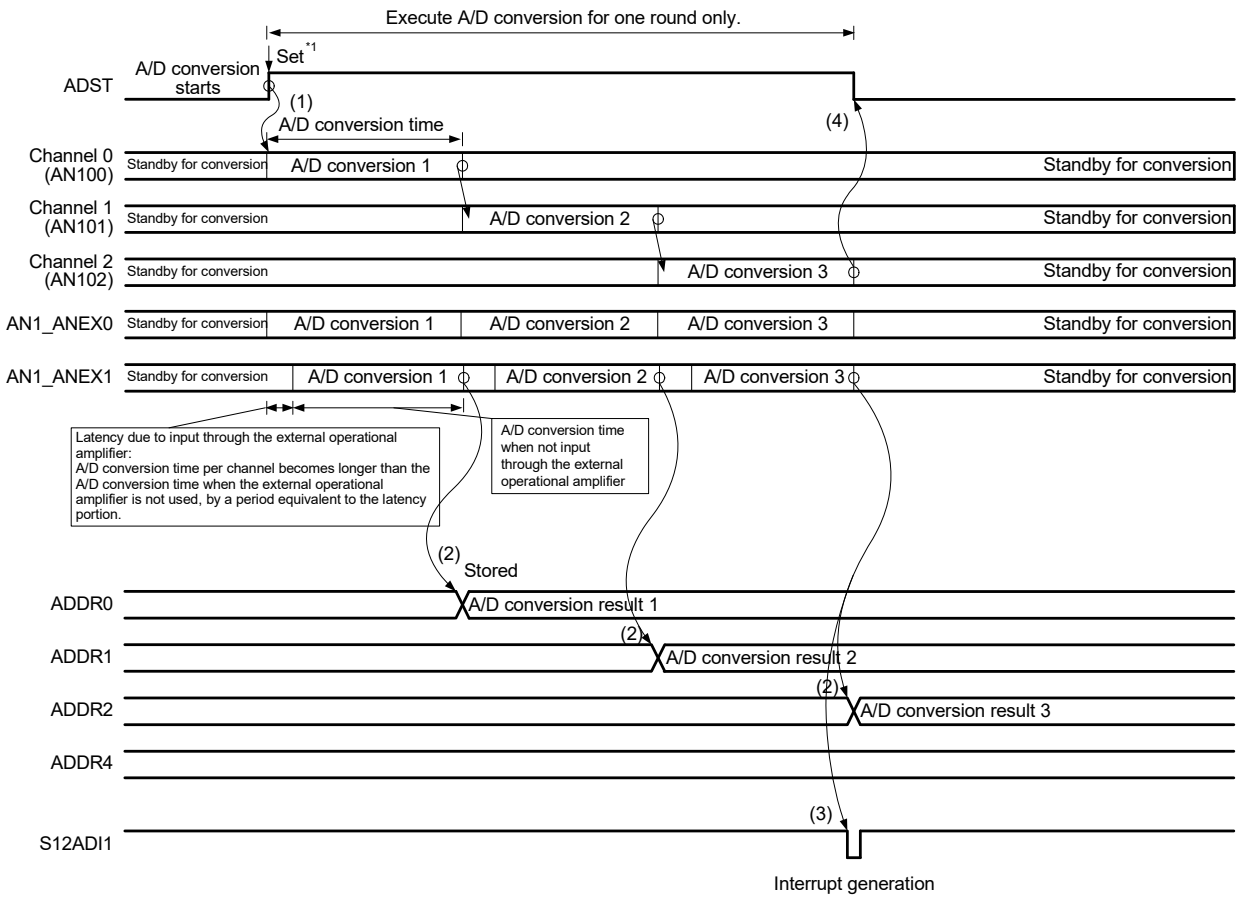
Figure 43.28 Configuration Example of Extended Analog Input Circuit with AN1_ANEX1 Used

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input, A/D conversion is performed for the selected channels, starting from the channel with the smallest number.

(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon scanning completion is enabled).

(4) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.29 AN1_ANEX1 Input Operation Example (Single Scan Mode)

When the extended analog input is selected, each A/D conversion time becomes longer due to the latency of the operational amplifier, compared to the A/D conversion that is directly performed for the analog input channels.

43.3.6 Comparison

Comparison is of a reference value set in a register with the result of A/D conversion on selected channels. Self-diagnosis function and double-triggered mode are not available while comparison is in use.

Operation using comparison in combination with continuous scan mode is described below.

(1) A/D conversion is started in the order of the selected channels and the temperature sensor output when ADCSR.ADST is set to 1 (to start A/D conversion) by software, or in response to a synchronous trigger (MTU3a, GPTa, TPUa, ELC) or asynchronous trigger.

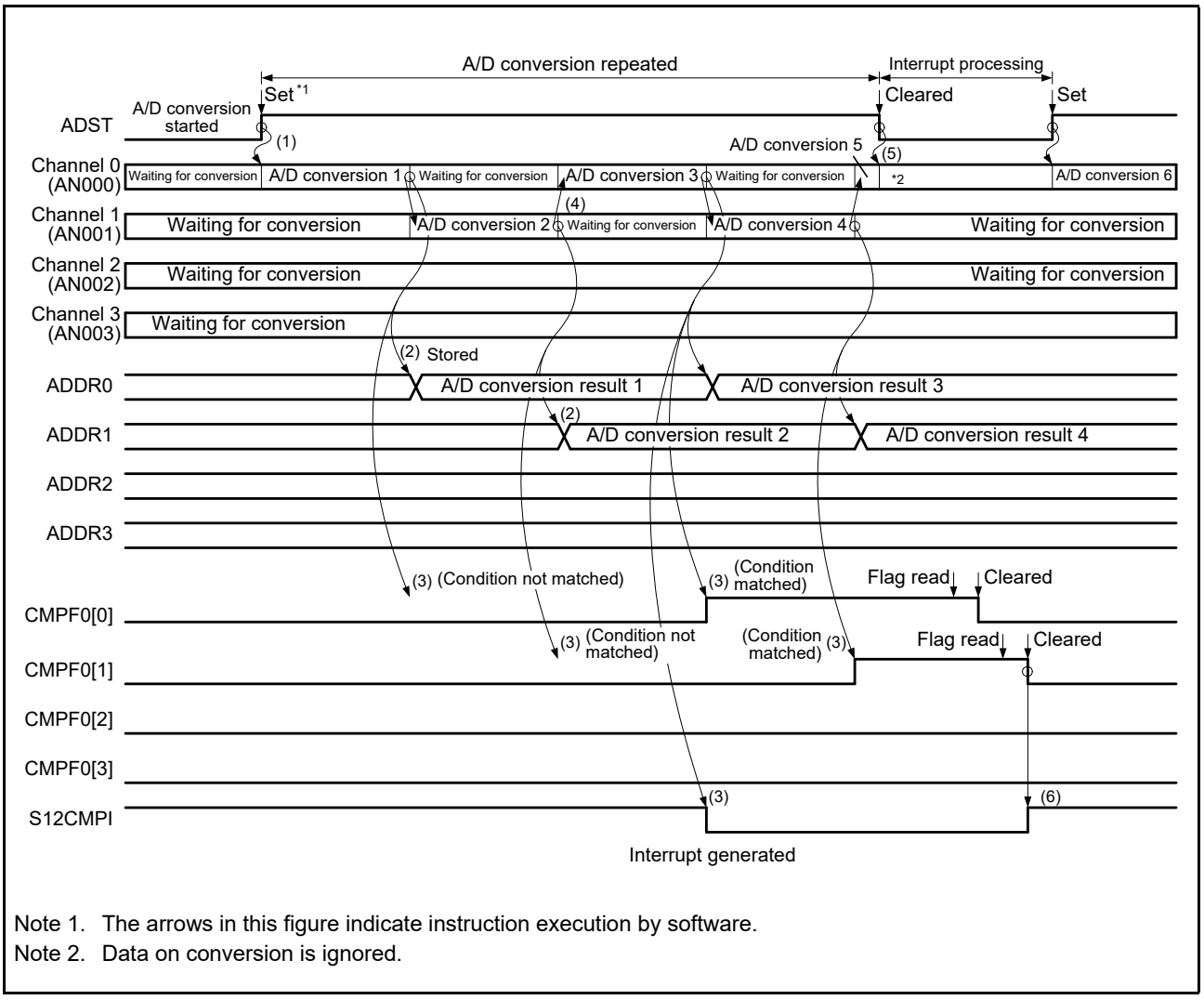
(2) When A/D conversion is completed, the result is stored in the A/D self-diagnosis data register (ADDRy, ADTSDR). If the register is selected for comparison by the settings of the ADCMPANSR and ADCMPANSER registers, its value is then compared with that of the ADCMPDR0/1 registers.

(3) If the result of comparison meets the condition set in the ADCMPCR.WCMPE bit, the ADCMPLR register, and the ADCMPLER register, the bits ADCMPSR.CMPFn and ADCMPSER.CMPFTS are set to 1. If the setting of the ADCMPCR.CMPIE bit is 1 at this time, an S12CMPI interrupt is also generated.

(4) When A/D conversion is completed for all selected channels, A/D conversion is started again.

(5) If the setting of the ADCSR.ADST bit is 0 (A/D conversion stop) after the S12CMPI interrupt is accepted, the interrupt processing proceeds for channels that have the compare flag.

(6) The S12CMPI interrupt signal is deasserted when all of the compare flags have been cleared. To start further comparison, start A/D conversion again.



Note 1. The arrows in this figure indicate instruction execution by software.
Note 2. Data on conversion is ignored.

Figure 43.30 Example of Operation Using Compare Function (AN000, AN001, AN002, and AN003 Selected for Comparison)

43.3.7 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated either by a software trigger; a synchronous trigger (MTU3a, GPTa, TPUa, ELC); or an asynchronous trigger (ADTRGn). After the start-of-scanning-delay time (t_D) has elapsed, processing by the channel-dedicated sample-and-hold circuits, processing for disconnection detection assistance, and processing of conversion for self-diagnosis proceed, and this is followed by A/D conversion.

Figure 43.31 shows the scan conversion timing in single scan mode, in which scan conversion is activated by a software trigger or a synchronous trigger (MTU3a, GPTa, TPUa, ELC). Figure 43.32 shows the scan conversion timing in single scan mode, in which scan conversion is activated by an asynchronous trigger ADTRGn. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), channel-dedicated sample-and-hold circuit processing time (t_{SPLSH})*1, disconnection detection assistance processing time (t_{DIS})*2, self-diagnosis A/D conversion processing time (t_{DIAG})*3, A/D conversion processing time (t_{CONV}), channel-dedicated sample-and-hold circuit end time (t_{SHED})*4, and end-of-scanning-delay time (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.

The time for conversion by successive approximation (t_{SAM}) is at 13 ADCLK states with 12-bit accuracy selected, 11 ADCLK states with 10-bit accuracy selected, and 9 ADCLK states with 8-bit accuracy selected. Table 43.11 shows the scan conversion time.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} plus t_{SHED}. The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed to $t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{SHED}$.

Note 1. When no channel-dedicated sample-and-hold circuits are used, $t_{SH} = 0$.
Note 2. When disconnection detection assistance is not selected, $t_{DIS} = 0$.
Note 3. When the self-diagnosis function is not used, $t_{DIAG} = 0$.
Note 4. When no channel-dedicated sample-and-hold circuits are used, $t_{SHED} = 0$. Here, continuous scan mode is assumed. In single scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay time (t_{ED}).

Table 43.10 Example of Setting the ADSSTR Register

Use	Setting Range	Sampling Time*1
Standard (initial value)	0Bh	0.18 µs (For ADCLK = 60 MHz)
Use this range if there is not sufficient sampling time due to the high impedance of an analog input signal source.	0Ch to FFh	Example: FFh 4.3 µs (For ADCLK = 60 MHz)
Use this range if ADCLK is less than 60 MHz and the sampling time needs to be less than the initial value.	05h to 0Ah	Example: 0Ah 0.67 µs (For ADCLK = 15 MHz)

Note 1. The sampling time is determined by the following formula.

$$\text{Sampling time (µs)} = \frac{\text{ADSSTR register setting}}{\text{ADCLK (MHz)}}$$

Table 43.11 Times for Conversion during Scanning (in Numbers of Cycles of the ADCLK and PCLKH)

Item			Symbol		Type/Conditions: Synchronous Trigger MTUa, GPTa	Synchronous Trigger TPUa, ELC	Asynchronous Trigger	Software Trigger	Unit
Scan start processing time*1, *2	A/D conversion on group A under group A priority control.	Group B is to be stopped. (Group A is activated after group B is stopped due to an A/D conversion source of group A.)	t_D		4 PCLKH + 6 ADCLK	3 PCLKH + 6 ADCLK	—	—	Cycle
		Group B is not to be stopped. (Activation by an A/D conversion source of group A.)			3 PCLKH + 4 ADCLK	2 PCLKH + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started.			3 PCLKH + 6 ADCLK	2 PCLKH + 6 ADCLK	4 PCLKH + 6 ADCLK	6 ADCLK	
		Normal A/D conversion is to be started after completion of self-diagnosis conversion.			2 ADCLK	2 ADCLK	2 ADCLK	2 ADCLK	
		A/D conversion for self-diagnosis is to be started after completion of conversion for continuous scan on the last channel specified.			2 ADCLK	2 ADCLK	2 ADCLK	2 ADCLK	
	Other than above				3 PCLKH + 4 ADCLK	2 PCLKH + 4 ADCLK	4 PCLKH + 4 ADCLK	4 ADCLK	
Channel-dedicated sample-and-hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	The setting of ADSHCR.SSTSH[7:0] (initial value = 18h) × ADCLK				
	Wait time between sampling and A/D Conversion			t_W	12 ADCLK				
Disconnection detection assistance processing time			t_{DIS}		The setting of ADNDIS[3:0] (initial value = 00h) × ADCLK				
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTR0 (initial value = 0Bh) × ADCLK				
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	15 ADCLK				
		10-bit conversion accuracy			13 ADCLK				
		8-bit conversion accuracy			11 ADCLK				
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn (n = 0 to 7, L, T) (initial value = 0Bh) × ADCLK				
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	13 ADCLK				
		10-bit conversion accuracy			11 ADCLK				
		8-bit conversion accuracy			9 ADCLK				
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK				
Scan end processing time*1			t_{ED}		1 PCLKH + 3 ADCLK				

Note 1. Refer to Figure 43.31 and Figure 43.32 for illustration of times t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. Set tSPLSH + tCONV to satisfy the conversion time conditions listed in the A/D conversion characteristics of section 47, Electrical Characteristics.

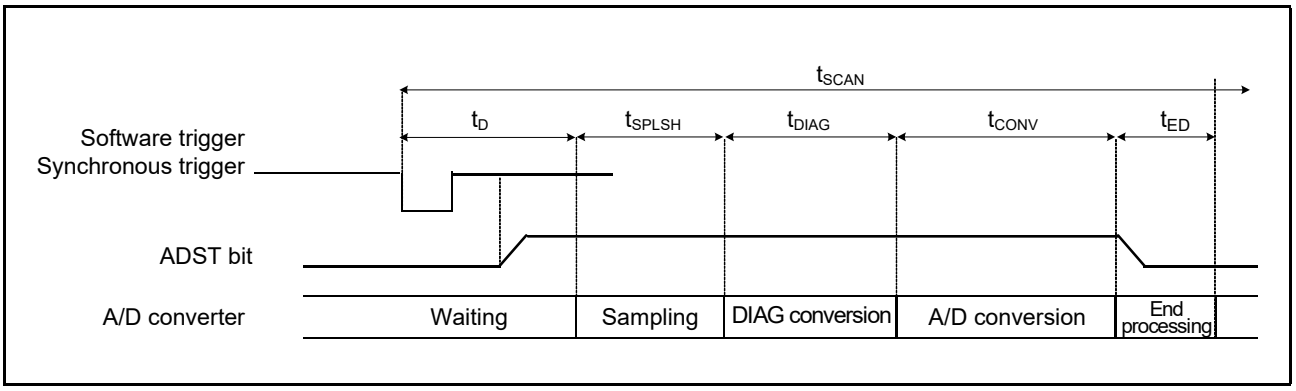


Figure 43.31 Scan Conversion Timing (Activated by Software or Synchronous Trigger Input (MTU3a, GPTa, TPUa, ELC))

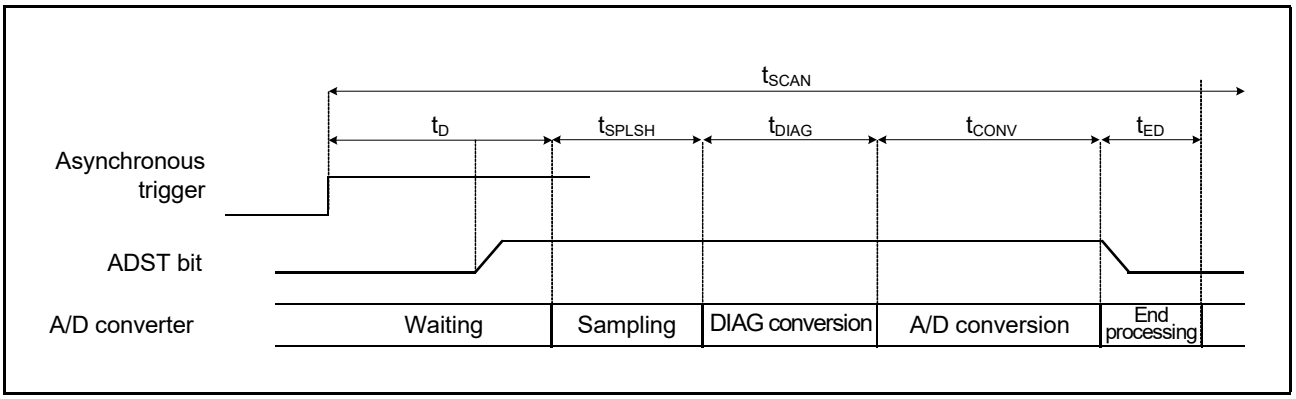


Figure 43.32 Scan Conversion Timing (Activated by Asynchronous Trigger Input (ADTRGn))

43.3.8 Usage Example of A/D Data Register Automatic Clearing Function

In A/D-converted value addition/average mode, the A/D data register automatic clearing function can be used when A/D conversion of the analog input of the selected channels or A/D conversion of the temperature sensor output is selected. Setting the ACE bit in ADCER to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR) to 0000h when the A/D data registers are read by the CPU or DMAC.
This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR). The following describes the examples in which the function to automatically clear the ADDRy register is enabled and disabled.
In a case where the ACE bit in ADCER is 0 (automatic clearing is disabled), if the A/D conversion result (0222h) is not written to the ADDRy register for some reason, the old data (0111h) will be the ADDRy value. Furthermore, if this ADDRy value is read into a general register using an A/D scan end interrupt, the old data (0111h) can be saved in the general register. When checking whether there is an update failure, it is necessary to frequently save the old data in the RAM or a general register.
In a case where the ACE bit in ADCER is 1 (automatic clearing is enabled), when ADDRy = 0111h is read by the CPU or DMAC, ADDRy is automatically cleared to 0000h. After that, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general register using an A/D scan end interrupt at this point, 0000h will be saved in the general register. Occurrence of an ADDRy update failure can be determined by simply checking that the read data value is 0000h.

43.3.9 A/D-Converted Value Addition/Average Mode

In A/D-converted value addition mode, the same channel is A/D-converted two to four consecutive times and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted two to four consecutive times and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that affect A/D conversion. This function, however, cannot always guarantee an improvement in A/D conversion accuracy. The A/D-converted value addition/average mode can be specified when A/D conversion of the channel select analog input or temperature sensor output is selected.

43.3.10 Disconnection Detection Assist Function

This converter incorporates the function to fix the charge for sampling capacitance to the specified state (VREFH0 or VREFL0 for unit 0; VREFH1 or VREFL1 for unit 1) before start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

Figure 43.33 illustrates the A/D conversion operation when the disconnection detection assist function is used. Figure 43.34 shows an example of disconnection detection when precharge is selected. Figure 43.35 shows an example of disconnection detection when discharge is selected.

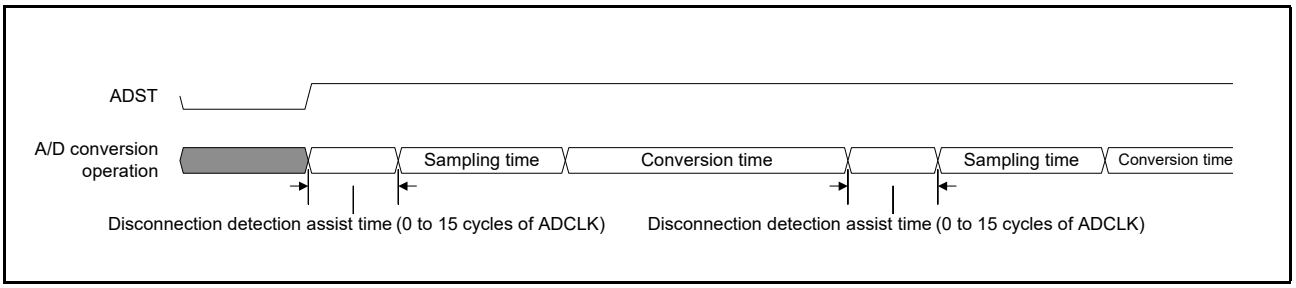
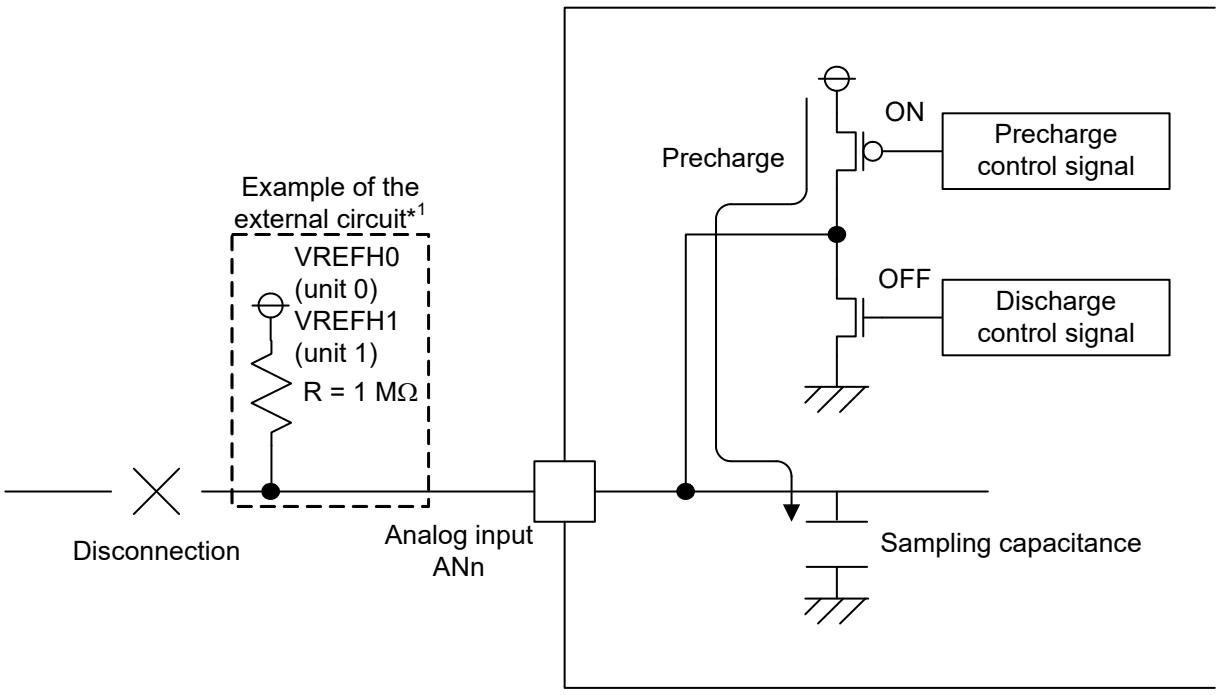
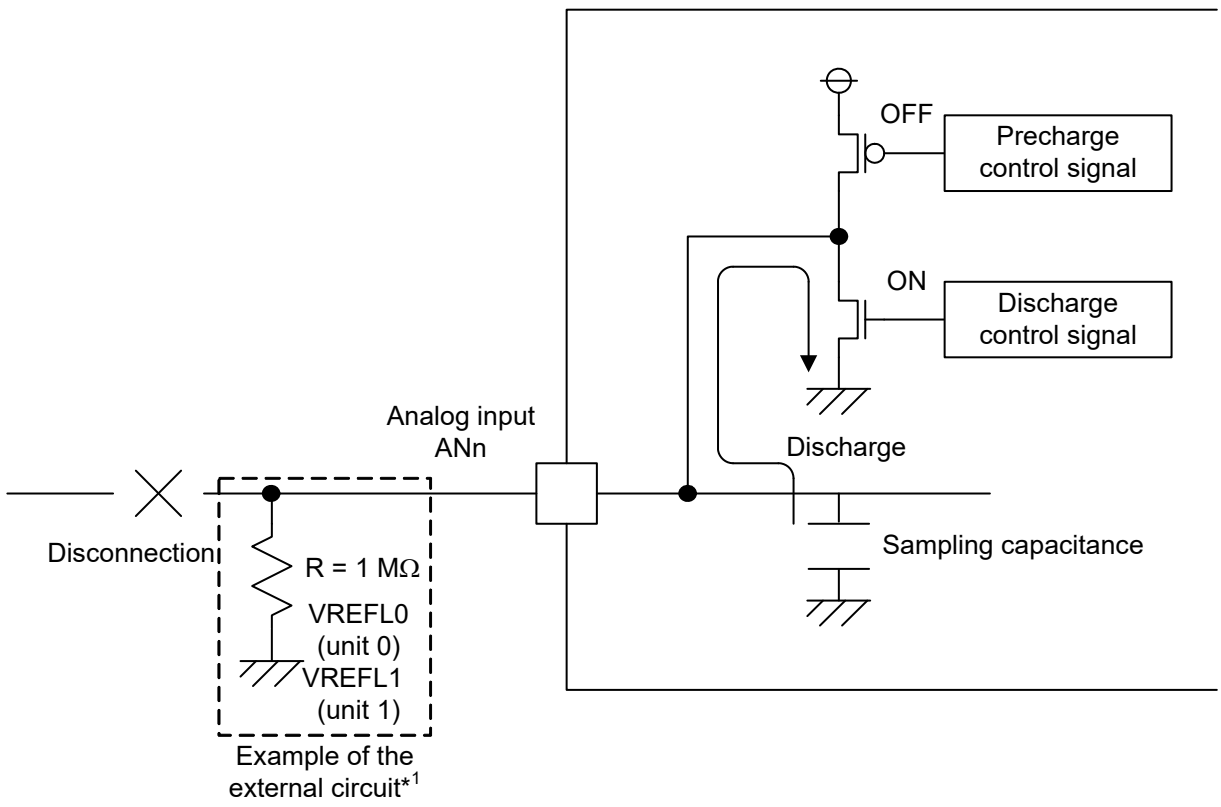


Figure 43.33 Operation of A/D Conversion when the Disconnection Detection Assist Function is Used



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 43.34 Example of Disconnection Detection when Precharge is Selected



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 43.35 Example of Disconnection Detection when Discharge is Selected

43.3.11 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRSA[5:0]) should be set to 000000b and a low-level signal should be input to the asynchronous trigger (ADTRGn pin). Both the ADCSR.TRGE and ADCSR.EXTRG bits then should be set to 1. Figure 43.36 shows a timing of the asynchronous trigger input.
For the time between setting the ADST bit to 1 and starting A/D conversion, refer to section 43.5.3 A/D Conversion Restarting Timing and Termination Timing.

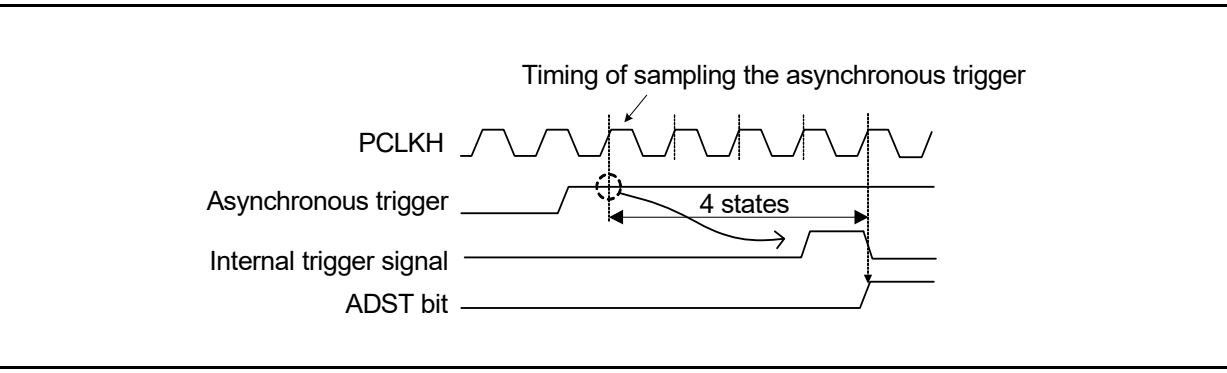


Figure 43.36 Asynchronous Trigger Input Timing

43.3.12 Starting A/D Conversion with Synchronous Trigger from Peripheral Module

The A/D conversion can be started by a synchronous trigger (MTU3a, GPTa, TPUa, ELC). To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant sources should be selected by the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

43.3.13 Pin-Level Self-Diagnosis Function

The pin-level self-diagnosis function performs A/D conversion using different voltage levels for input channels with odd numbers and for input channels with even numbers, respectively, to diagnose abnormality of routes from the ANn pins. Different voltage levels can be set in the ADTDCR register, with a combination of AVSS, AVCC, and 1/2 × AVCC. Users can select any physical channels to be tested in the pin-level self-diagnosis function. Furthermore, pin-level self-diagnosis can be performed for all scan operations.

43.3.13.1 Pin-Level Self-Diagnosis in Single Scan Mode (without Channel-Dedicated Sample-and-Hold Circuits)

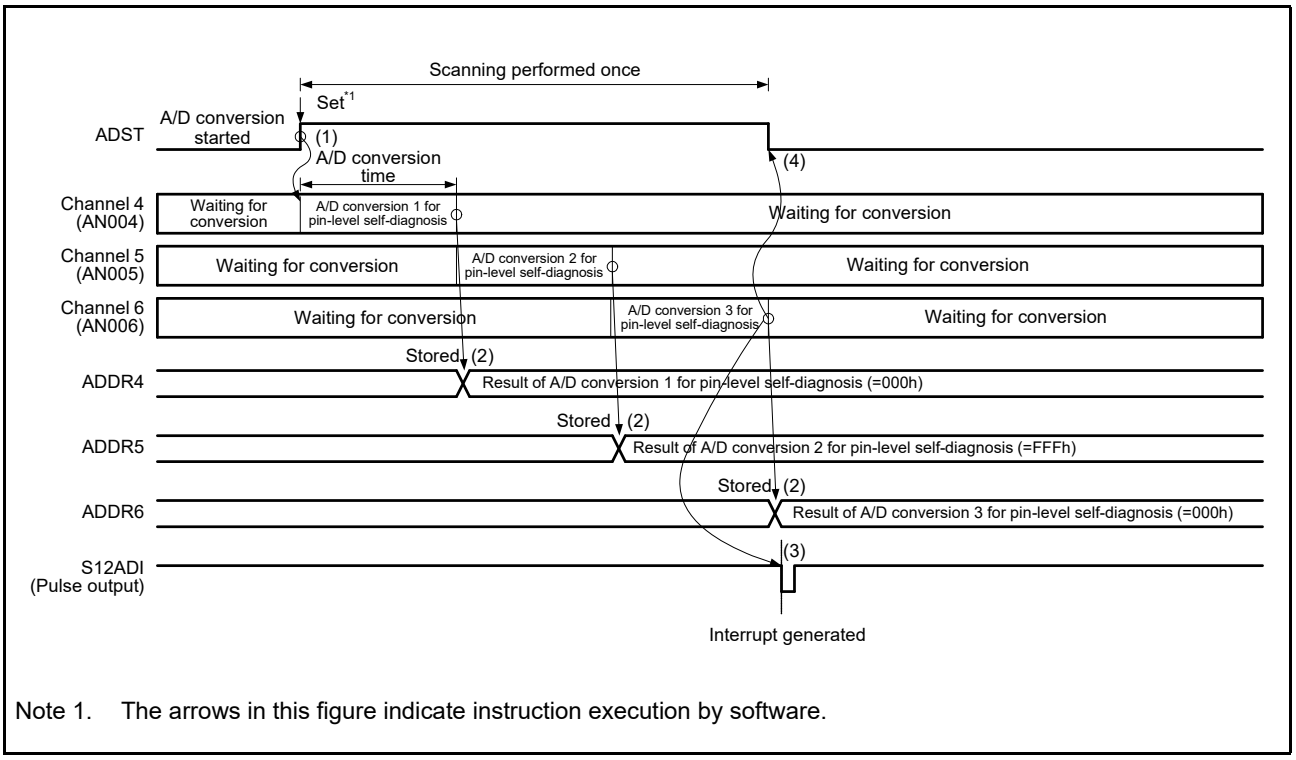
During pin-level self-diagnosis in single scan mode, A/D conversion of the analog input on the specified channel is performed for one cycle only as follows:

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the pin with the smallest number n.

(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).

(3) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon completion of scanning is enabled).

(4) The ADST bit in ADCSR remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



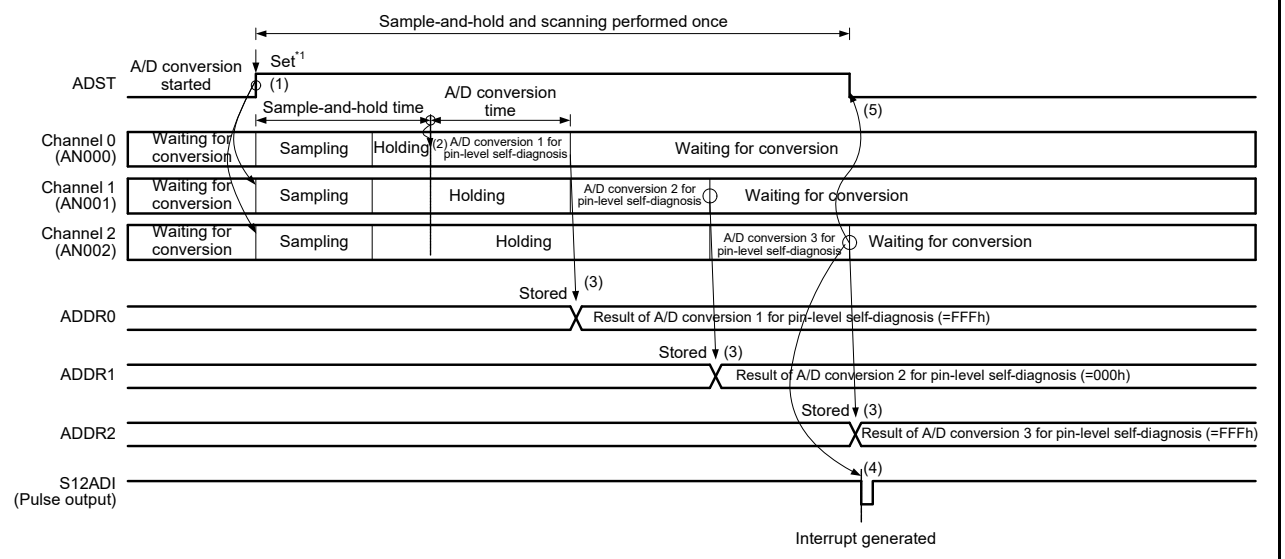
Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.37 Example Operation of Pin-Level Self-Diagnosis in Single Scan Mode (Basic Operation: AN004 to AN006 Selected/ADTDCR.TDLV[1:0] = 00b)

43.3.13.2 Pin-Level Self-Diagnosis in Single Scan Mode (with Channel-Dedicated Sample-and-Hold Circuits)

When pin-level self-diagnosis is performed with the channel-dedicated sample-and-hold circuit used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the selected channels as below. The channels whose channel-dedicated sample-and-hold circuit is to be used can be selected by the SHANS[3:0] bits in ADSHCR.

(1) When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger, a synchronous trigger input (MTU3a, GPTa, TPUa, ELC), or an asynchronous trigger input, sampling is started for analog input of all the channels that use channel-dedicated sample-and-hold circuit.
(2) After sample-and-hold operation, A/D conversion is performed for ANn pins selected by the ADANSA register, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI interrupt is generated if the ADIE bit in ADCSR is 1 (S12ADI interrupt upon completion of scanning is enabled).
(5) The ADST bit in ADCSR remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a waiting state.



Note 1. The arrows in this figure indicate instruction execution by software.

Figure 43.38 Example Operation of Pin-Level Self-Diagnosis in Single Scan Mode (with Channel-Dedicated Sample-and-Hold Circuits: AN000 to AN002 Selected/ADTDCR.TDLV[1:0] = 01b)

43.3.14 Error Detection Function

The overwrite error detection function detects update of the A/D conversion results held in various A/D data registers, without a need of reading those results. The 12-bit A/D converter can generate S12ADOWEI interrupt, which is an overwrite error interrupt request to the error control module (ECM).

Setting the OWEIE bit in the ADERCR register to 1 enables generation of S12ADOWEI interrupt, and clearing the bit to 0 disables generation of S12ADOWEI interrupt. Reading the ADOWER 0/1 and ADOWEER registers can determine the A/D data register in which the overwrite error occurred. Writing 1 to the OWEC bit in the ADERCLR register clears all the overwrite error flags held in the ADOWER 0/1 and ADOWEER registers.

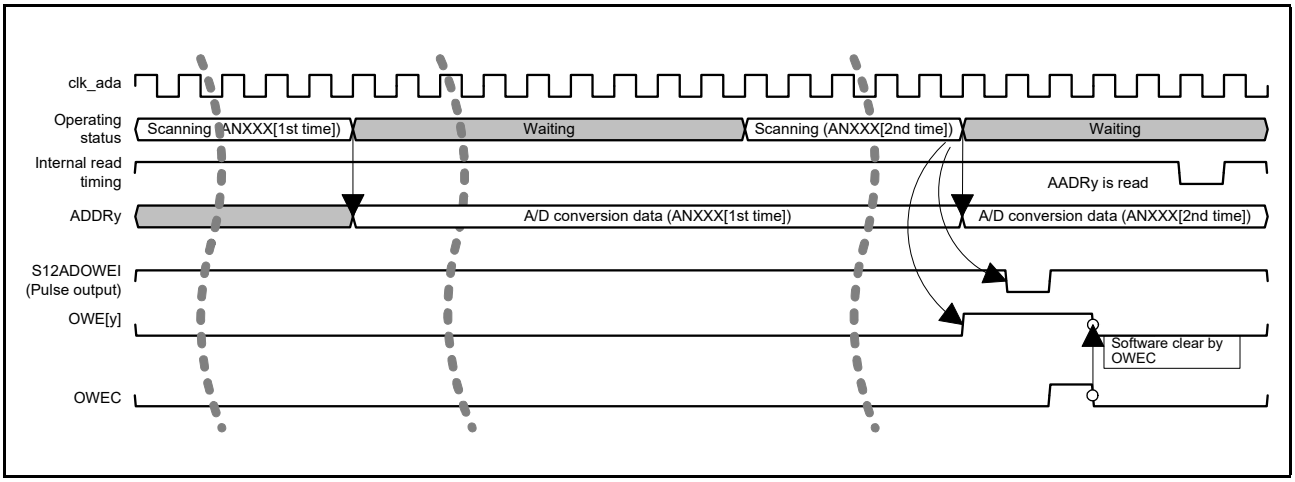


Figure 43.39 Example of Generation of AD Overwrite Error Interrupt

43.4 Interrupt Sources and DMAC Transfer Requests

43.4.1 Interrupt Requests

The 12-bit A/D converter can generate scan end interrupt requests S12ADI and S12GBADI. The module also generates the S12CMPI interrupt in response to matches with a condition for comparison.
Setting the ADCSR.ADIE bit to 1 and 0 enables and disables generation of an S12ADI interrupt, respectively; similarly, setting the ADCSR.GBADIE bit to 1 and 0 enables and disables generation of an S12GBADI interrupt, respectively.
Setting the ADCMPCR.CMPIE bit to 1 and 0 enables and disables generation of an S12CMPI interrupt, respectively.
In addition, the DMAC can be started up when an S12ADI or an S12GBADI interrupt is generated. Using an S12ADI or an S12GBADI interrupt to allow the DMAC to read the converted data enables continuous A/D conversion without burden on software.
For details on DMAC settings, see section 15, DMA Controller (DMACAa).
The S12ADI and S12GBADI interrupts are output according to the settings of scan mode and double trigger mode as shown in Table 43.12.

Table 43.12 Relationship between Mode Setting and S12ADI Interrupt Output

Scan Mode	Double Trigger Mode (DBLE)	Trigger	S12ADI Interrupt (ADIE = 1)	S12GBADI Interrupt (GBADIE = 1)
Single scan mode	DBLE = 0	Software trigger	Output on completion of each scan	Not output (group B scan is disabled)
		Synchronous trigger	Output on completion of each scan	Not output (group B scan is disabled)
		Asynchronous trigger	Output on completion of each scan	Not output (group B scan is disabled)
	DBLE = 1	Software trigger (setting prohibited)*1	—	—
		Synchronous trigger	Output on completion of each even-order scan	Not output (group B scan is disabled)
		Asynchronous trigger (setting prohibited)*1	—	—
Continuous scan mode	Setting prohibited	Software trigger	Output on completion of each scan	Not output (group B scan is disabled)
		Synchronous trigger	Output on completion of each scan	Not output (group B scan is disabled)
		Asynchronous trigger	Output on completion of each scan	Not output (group B scan is disabled)
Group scan mode	DBLE = 0	Software trigger (setting prohibited)*1	—	—
		Synchronous trigger	Output on completion of each scan for group A	Output on completion of each scan for group B
		Asynchronous trigger (setting prohibited)*1	—	—
	DBLE = 1	Software trigger (setting prohibited)*1	—	—
		Synchronous trigger	Output on completion of each even-order scan for group A	Output on completion of each scan for group B
		Asynchronous trigger (setting prohibited)*1	—	—

Note 1. Setting a software trigger and asynchronous trigger in double trigger mode is prohibited.
Setting a software trigger and asynchronous trigger in group scan mode is also prohibited.

43.4.2 Scan End Event Output to ELC

The event link controller (ELC) enables a link operation with the modules specified in advance using S12ADI interrupt request signal as an event signal. The S12GBADI and S12CMPI interrupt request signals cannot be used as an event signal. An event signal can be output regardless of the settings of the corresponding interrupt request enable bits. The 12-bit A/D converter outputs an A/D conversion end event.

43.5 Usage Notes

43.5.1 Notes on Reading Data Registers

The A/D data registers, A/D data duplication registers, A/D data duplication register A, A/D data duplication register B, A/D temperature sensor data register, and A/D self-diagnosis data register must be read in word units. If a register is read twice in byte units, that is, the upper byte and lower byte are separately read, the A/D-converted value having been read first may disagree with the A/D-converted value having been read for the second time.

43.5.2 Notes on Stopping A/D Conversion

To select an asynchronous trigger or a synchronous trigger as the condition for starting A/D conversion and stop A/D conversion, follow the procedure in Figure 43.40.

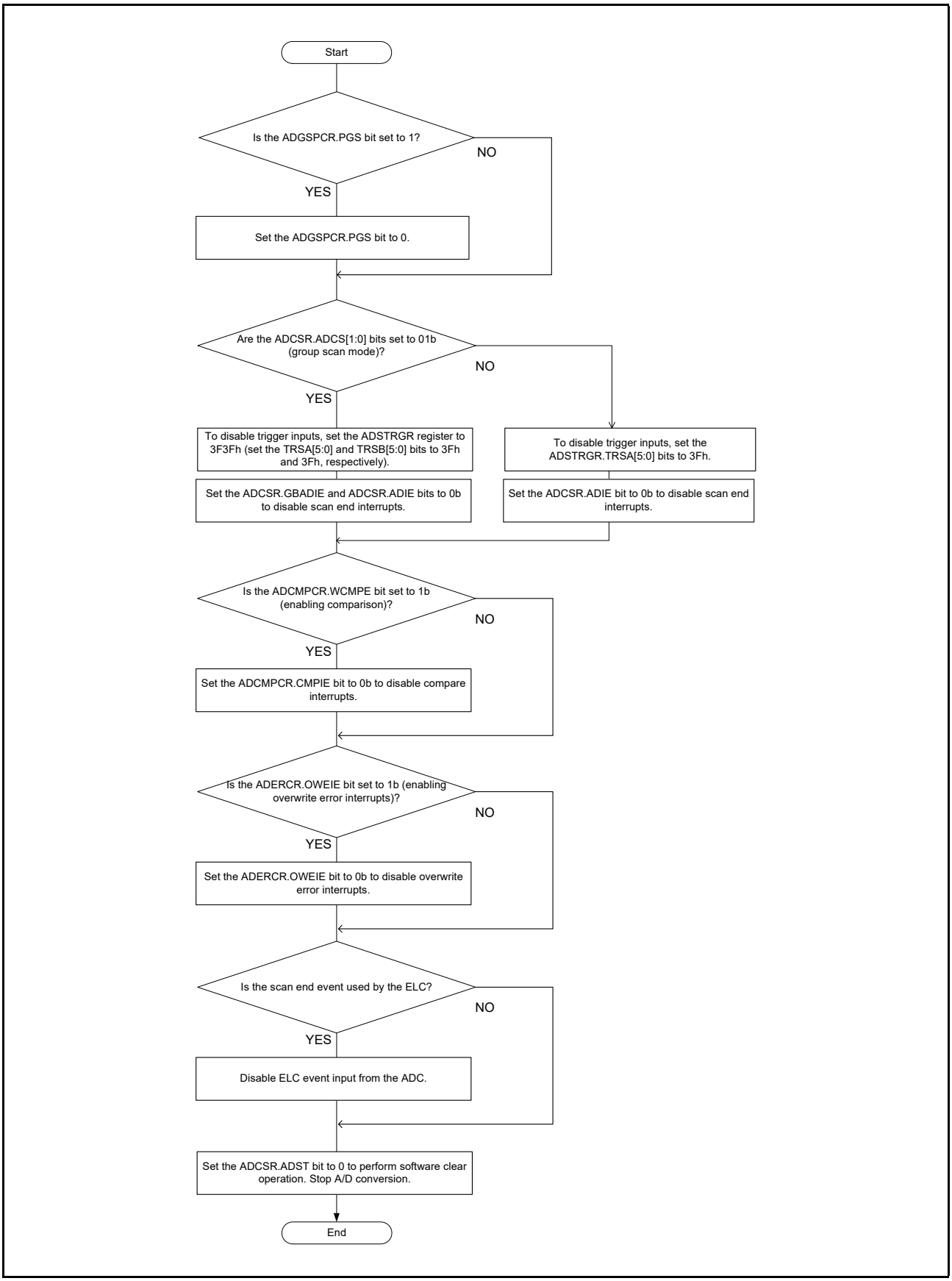


Figure 43.40 Procedures for Clear Operation by Software through the ADCSR.ADST Bit

43.5.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of six ADCLK cycles until the idle analog unit of the 12-bit A/D converter is restarted after the ADST bit in ADCSR is set to 1. It takes a maximum of two ADCLK cycles until the operating analog unit of the 12-bit A/D converter is terminated if the ADST bit in ADCSR is set to 0.

43.5.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, if the CPU does not complete reading out the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated, the first A/D-converted data is overwritten with the second A/D-converted data and an overwrite error occurs.

43.5.5 Module Stop Function Setting

Operation of the 12-bit A/D converter can be disabled or enabled using the module stop control register C (MSTPCRC). The initial setting is for operation of the 12-bit A/D converter to be halted. Releasing the module-stop state enables access to the registers. After release from the module-stop state, wait for at least 1µs before starting A/D conversion. For details, see section 9, Low-Power Consumption Function.

43.5.6 Notes on Entering Low-Power Consumption States

Before the transition to the module-stop state or software standby mode, make sure to stop A/D conversion. Here, set the ADST bit in ADCSR to 0, and secure certain period of time until the analog unit of the 12-bit A/D converter is stopped. Follow the procedure given below to secure this time.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 43.40. Then, after two clock cycles of ADCLK pass, place the 12-bit A/D converter in the module-stop state or software standby mode.
To place the 12-bit A/D converter in standby mode, set the MSTPCRC.MSTPCRC4 bit (unit 1) or the MSTPCRC.MSTPCRC5 bit (unit 0) to 1.

43.5.7 Caution When Using an External Bus

A/D conversion at the same time as access to an external bus may produce poor results.
Perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

43.5.8 Error in Absolute Accuracy When Disconnection Detection Assistance is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the A/D converter. This is because an error voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula. Only use disconnection detection assistance after thorough evaluation.

Maximum error in absolute accuracy (LSB) = 4095 × Rs / Rp

43.5.9 Caution When Using Disconnection Detection Assistance

If ADEXICR.EXSEL[1:0] and ADEXICR.EXOEN are set to any values other than ADEXICR.EXSEL[1:0] = 00b and ADEXICR.EXOEN = 0b, and disconnection detection assistance is enabled, A/D conversion cannot be executed correctly. Be sure to set ADEXICR.EXSEL[1:0] = 00b and ADEXICR.EXOEN = 0b when using disconnection detection assistance. Disable this function when pin-level self-diagnosis is executed.

43.5.10 Caution When Using Self-Diagnosis

If ADEXICR.EXSEL[1:0] and ADEXICR.EXOEN are set to any values other than ADEXICR.EXSEL[1:0] = 00b and ADEXICR.EXOEN = 0b, and self-diagnosis is enabled, A/D conversion cannot be executed correctly. Be sure to set ADEXICR.EXSEL[1:0] = 00b and ADEXICR.EXOEN = 0b when using self-diagnosis
When the channel-dedicated sample-and-hold circuit is to be used for simultaneous sampling of four channels (AN000 to AN003) and self-diagnosis is to be enabled, set the sampling time tSPL to 0.4 µs by using ADSSTR0.SST[7:0] to satisfy the holding characteristics of sample-and-hold circuits, 3.2 µs (max.).

43.5.11 Setting to Restart Conversion by Group B in Group Scan Mode (when Group A is Given Priority)

To enable setting for restarting group B (i.e., PGS = 1 and GBRSCN = 1) in group scan mode (when group A is given priority), set the ratio between the frequency divisors for PCLKH and ADCLK to 1:1. Conversion by group B cannot be restarted in group scan mode (when group A is given priority) unless the frequency division settings are in accord with this.

43.5.12 Allowable Signal Source Impedance

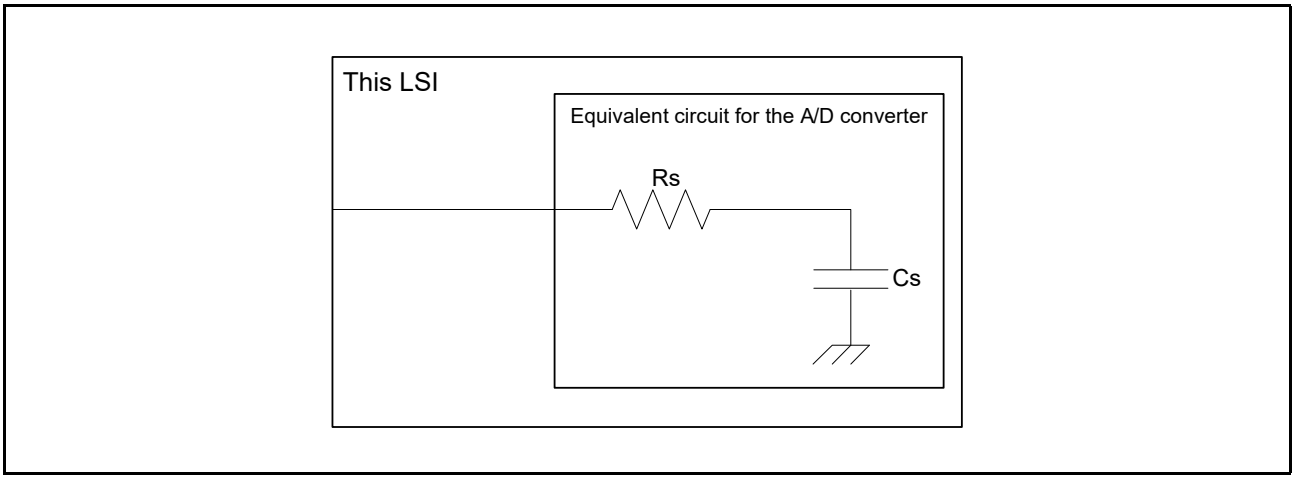


Figure 43.41 Internal Equivalent Circuit for Analog Input Pin

Table 43.13 Analog Pin Specifications

Item		Min.	Typ.	Max.	Unit
Equivalent circuit in ADC unit 0	Rs	—	1.5	—	kΩ
	Cs	—	8	—	pF
Equivalent circuit in ADC unit 1	Rs	—	3.0	—	kΩ
	Cs	—	16	—	pF

Note: As the capacitance estimated from the pin of the product, the pin capacitance listed in section 47, Electrical Characteristics, is included in the internal equivalent circuit.

44. Temperature Sensor

44.1 Overview

This LSI includes a temperature sensor. The temperature sensor outputs a voltage which varies with the temperature. The 12-bit A/D converter (unit 0) can convert the voltage from the sensor into a digital value. The user can then obtain the temperature around this LSI by converting the value into the temperature.
Table 44.1 lists the specifications of the temperature sensor, and Figure 44.1 shows a block diagram of the temperature sensor.

Table 44.1 Specifications of Temperature Sensor

Item	Description
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D converter (unit 0).
Low-power consumption function	The module-stop state is selectable.

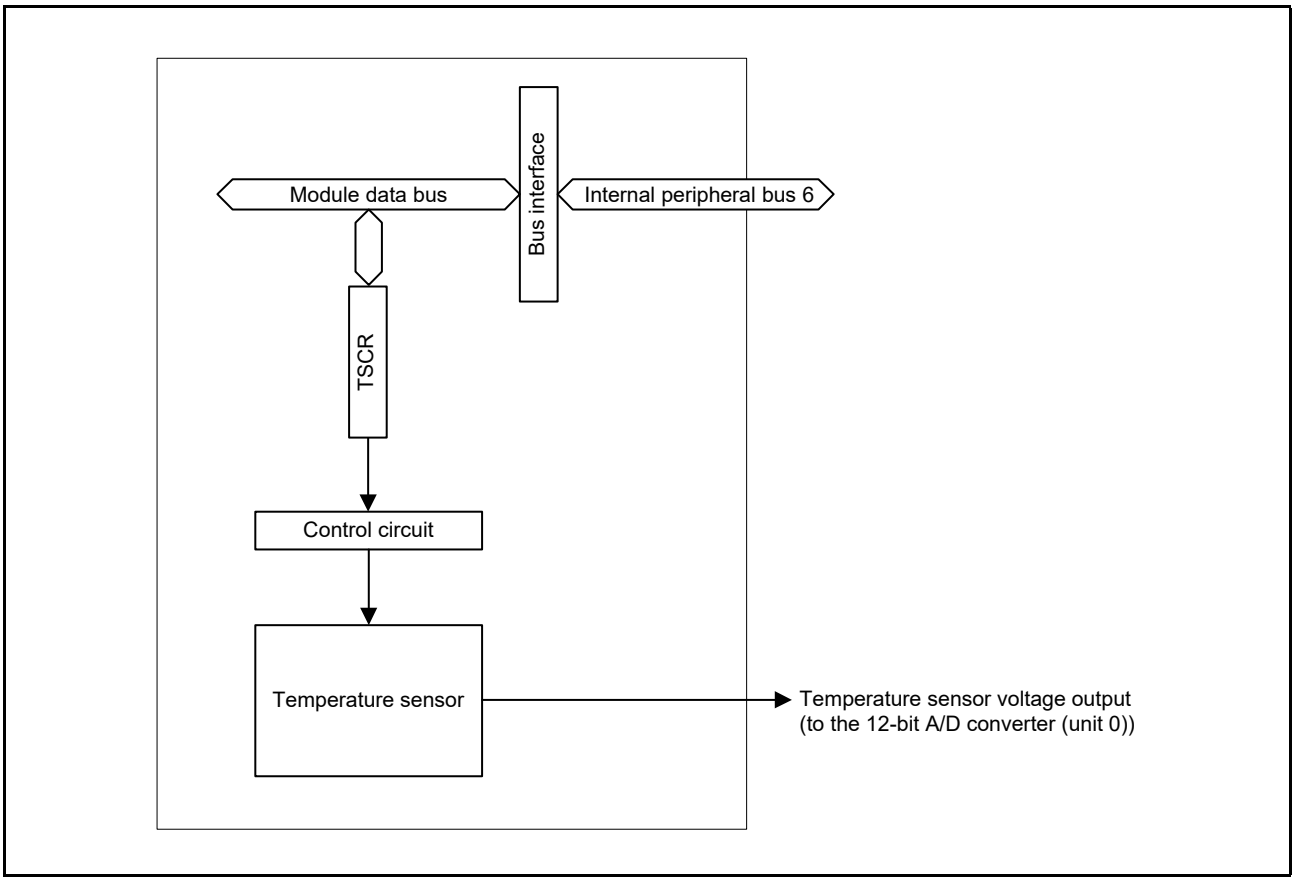


Figure 44.1 Block Diagram of Temperature Sensor

44.2 Register Descriptions

44.2.1 Temperature Sensor Control Register (TSCR)

Address(es): A008 0A00h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TSOE	Temperature Sensor Output Enable	0: Disables output from the temperature sensor to the 12-bit A/D converter (unit 0). 1: Enables output from the temperature sensor to the 12-bit A/D converter (unit 0).	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TSEN	Temperature Sensor Enable	0: Stops the temperature sensor. 1: Starts the temperature sensor.	R/W

The settings of TSCR register have the timing restrictions shown in Figure 44.3.

44.3 Using the Temperature Sensor

The temperature sensor outputs a voltage which varies with the temperature.
This voltage is converted to a digital value by the 12-bit A/D converter (unit 0). The user can then obtain the temperature around this LSI by converting the value into the temperature.

44.3.1 Preparation for Using the Temperature Sensor

The voltage output by the temperature sensor is proportional to temperature, which can be calculated according to the following formula.

Formula for the temperature characteristic:
T = (Vs – V1)/Slope + T1

T: Measured temperature (°C)
Vs: Voltage output by the temperature sensor at the time of temperature measurement (V)
T1: Temperature experimentally measured at one point (°C)
V1: Voltage output by the temperature sensor at the time of measurement of T1 (V)
T2: Temperature at the experimental measurement of another point (°C)
V2: Voltage output by the temperature sensor at the time of measurement of T2 (V)
Slope: Temperature gradient by the temperature sensor (V/°C); slope = (V2 – V1)/(T2 – T1)

Characteristics vary from sensor to sensor. Therefore, the following experimental measurement at two different temperatures is recommended.
Use the 12-bit A/D converter (unit 0) to measure the voltage V1 output by the temperature sensor at temperature T1. Again, using the 12-bit A/D converter (unit 0), measure the voltage V2 output by the temperature sensor at a different temperature T2. Obtain the temperature gradient (slope = (V2 – V1)/(T2 – T1)) from these results.
Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs – V1)/slope + T1).

If you are using the temperature gradient given in section 47.7, Temperature Sensor Characteristics, use the 12-bit A/D converter (unit 0) to measure the voltage V1 output by the temperature sensor at temperature T1, and then calculate the temperature characteristic by using the formula below.
However, this method gives less accurate temperatures than measurement at two points.

T = (Vs – V1)/Slope + T1

T: Measured temperature (°C)
Vs: Voltage output by the temperature sensor at the time of temperature measurement (V)
T1: Temperature experimentally measured at one point (°C)
V1: Voltage output by the temperature sensor at the time of measurement of T1 (V)
Slope: Temperature gradient (V/°C) given in section 47.7, Temperature Sensor Characteristics.

- Calculation of the voltage output by the temperature sensor (when AD-converted value addition mode is not selected)
  The voltage output by the temperature sensor (V) can be calculated from the following formula.

$$\text{Output voltage (V)} = \text{AVREFH0 voltage (V)} \times \frac{\text{ADTSDR register value}}{2^n}$$

n: The precision of the AD conversion that is specified by the ADCER.ADPRC[1:0] bits (n = 8, 10, 12).

Remark: When the AD-converted value addition mode is selected, a value corresponding to the number of additions specified by the ADADC register is stored in the ADTSDR register. This requires another calculation of the value calculated from the above formula, i.e., dividing it the specified number of additions.

44.3.2 Setting of 12-Bit A/D Converter (Unit 0)

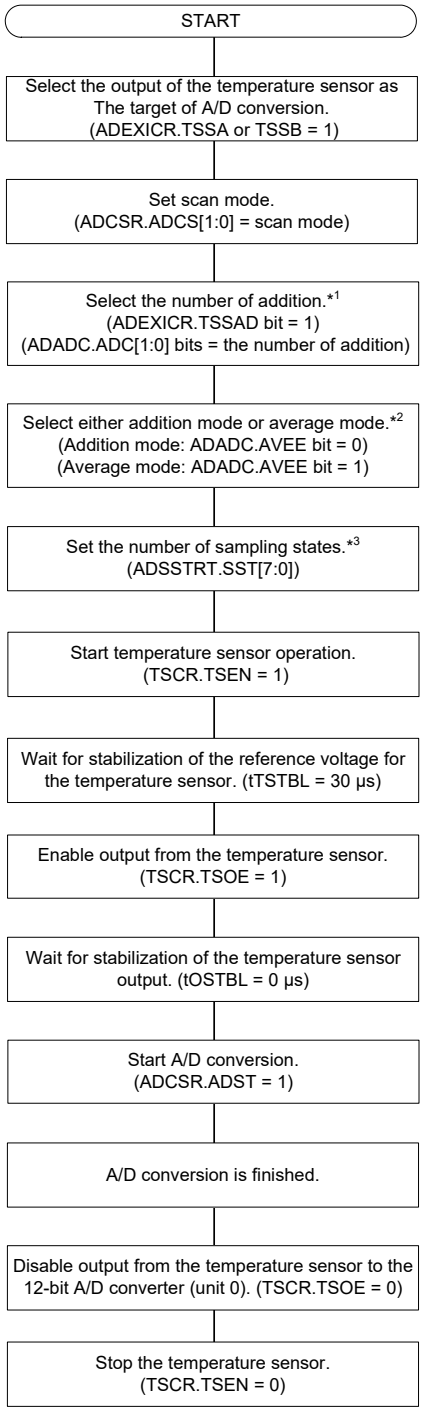
For A/D conversion of temperature sensor output voltages, 12-bit A/D converter (unit 0) registers should be set as follows.

- Setting the Temperature Sensor Voltage as an A/D Conversion Target
  Select A/D conversion of the voltage from the temperature sensor by setting the temperature sensor output A/D conversion select bit in the A/D conversion extended input control register (ADEXICR.TSSA or TSSB) to 1.
- Setting Scan Mode
  Select scan mode by setting the scan mode select bits in the A/D control register (ADCSR.ADCS[1:0]).
- Setting Addition/Average Mode
  For A/D conversion of the temperature sensor output, additional or average mode is selectable. To use either additional or average mode, set the temperature sensor output A/D converted value addition mode select bit in the A/D conversion extended input control register (ADEXICR.TSSAD) to 1, and the addition count select bits in the A/D converted value addition count select register (ADADC.ADC[1:0]) to the desired number of addition. Furthermore, clear the AVEE bit in ADADC to 0 to select addition mode; set the AVEE bit in ADADC to 1 to select average mode. In average mode, however, the ADC[1:0] bits in ADADC should not be set to 10b.
- Setting the Number of Sampling States of the 12-bit A/D converter (unit 0)
  The number of states for sampling of the output of the temperature sensor for A/D conversion is selectable. The initial setting is 11 states. To change the number of states for sampling from 11 states, set the sampling time setting bits in A/D sampling state register T (ADSSTRT.SST[7:0]), when the ADST bit in ADCSR is 0.

Setting the A/D conversion start bit in the A/D control register (ADCSR.ADST) to 1 starts A/D conversion, and the result is stored in the A/D temperature sensor data register (ADTSDR). If you will be using A/D conversion of the output from the temperature sensor, do so in accord with section 44.3.3, Procedure for Using the Temperature Sensor.

44.3.3 Procedure for Using the Temperature Sensor

Figure 44.2 shows the procedure for using the temperature sensor.



Note 1. Unless addition/average mode is set, this setting is not required. To select average mode, do not set the ADC[1:0] bits to 10b.
Note 2. Unless addition/average mode is set, this setting is not required.
Note 3. The initial value for the number of states over which sampling proceeds is 11. If the number of states is not to be changed, this setting is not required.

Figure 44.2 Procedure for Using the Temperature Sensor

44.3.4 Timing of A/D Conversion of Temperature Sensor Output

Figure 44.3 shows the timing from the start of temperature-sensor operation until the completion of A/D conversion when only the output from the temperature sensor is to be A/D converted and conversion is in single-scan mode. The times shown in the figure are described in Table 44.2.

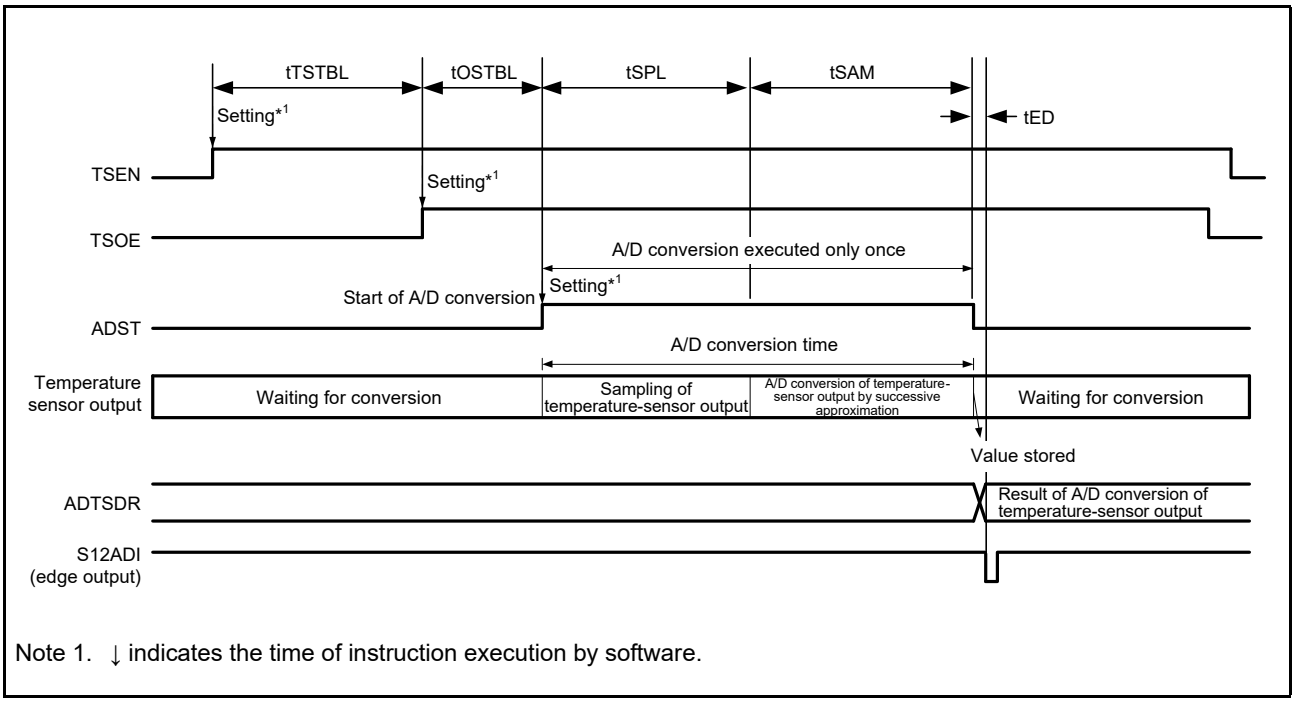


Figure 44.3 Timing from the Start of Temperature-Sensor Operation until Completion of A/D Conversion

Table 44.2 Time until Completion of A/D Conversion after the Start of Temperature-Sensor Operation

Item	Symbol	Time
Waiting time for temperature-sensor reference-voltage stabilization	tTSTBL	30 µs (min)
Waiting time for temperature-sensor output stabilization	tOSTBL	0 µs (min)
12-bit A/D converter (unit 0) input sampling time	tSPL	4.25 µs min. ADSSTRT setting × ADCLK cycles
Time for A/D conversion by successive approximation	tSAM	12-bit conversion accuracy: 13 ADCLK 10-bit conversion accuracy: 11 ADCLK 8-bit conversion accuracy: 9 ADCLK
Scan conversion end delay time	tED	1 PCLKH + 3 ADCLK

44.4 Usage Note

44.4.1 Module-Stop Function Setting

The corresponding bit in module stop control register C (MSTPCRC) can be used to enable and disable the temperature sensor. The initial setting is for the temperature sensor to be stopped. The register becomes accessible on release from the module-stop state. For details, see section 9, Low-Power Consumption Function.

45. Data Operation Circuit (DOC)

45.1 Overview

The data operation circuit (DOC) is used to compare, add, and subtract 16-bit data.
Table 45.1 lists the data operation circuit specifications and Figure 45.1 shows a block diagram of the data operation circuit.

- 16-bit data is compared and an interrupt can be generated when a selected condition applies.
- 16-bit data can be added.
- 16-bit data can be subtracted.

Table 45.1 DOC Specifications

Item	Description
Data operation function	16-bit data comparison, addition, and subtraction
Lower power consumption function	Module-stop state can be set.
Interrupts	An interrupt occurs at the following timings: • The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h
Event link function (event signal output)	An interrupt occurs at the following timings: • The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h

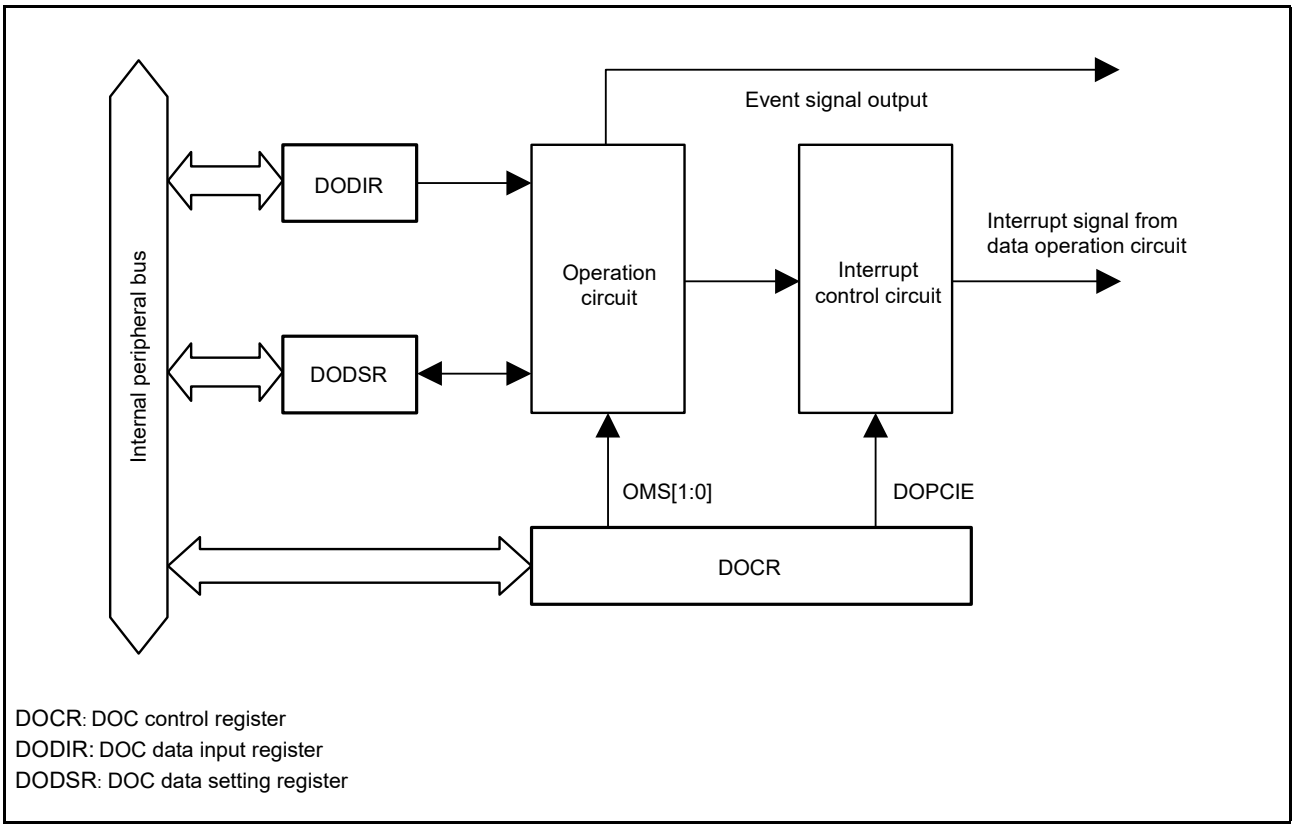


Figure 45.1 Block Diagram of Data Operation Circuit (DOC)

45.2 Register Descriptions

45.2.1 DOC Control Register (DOCR)

The DOCR register controls the DOC.

Address(es): A008 1200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	DOPCIE	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	Selects an operating mode of the data operation circuit. b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
b2	DCSEL	Detection Condition Select	Selects a condition for detecting data comparison result. 0: Data mismatch is detected. 1: Data match is detected. Note: Valid only in the data comparison mode.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DOPCIE	Data Operation Circuit Interrupt Enable	Specifies whether to enable or disable data operation circuit interrupt requests. 0: Disables interrupts from the data operation circuit. 1: Enables interrupts from the data operation circuit.	R/W
b5	DOPCF	Data Operation Circuit Flag	[Setting conditions] When any of the following is met: • The condition selected by the DCSEL bit is met. • A result of data addition is greater than FFFFh. • A result of data subtraction is less than 0000h. [Clearing condition] Writing 1 to the DOPCFCL bit	R
b6	DOPCFCL	DOPCF Clear	Setting this bit to 1 clears the DOPCF flag of this register. This bit is always read as 0. Writing 0 to this bit has no effect. Only 1 can be written to it.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

45.2.2 DOC Data Input Register (DODIR)

The DODIR register is a 16-bit readable/writable register in which 16-bit data for use in operations are stored.

Address(es): A008 1202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

45.2.3 DOC Data Setting Register (DODSR)

The DODSR register is a 16-bit readable/writable register. This register stores 16-bit data for use as a reference in data comparison mode. This register also stores the results of operations in data addition and data subtraction modes.

Address(es): A008 1204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

45.3 Operation

45.3.1 Data Comparison Mode

Figure 45.2 shows an example of the steps involved in data comparison mode operation by the data operation circuit. The following is an example of operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison).

(1) Writing 00b to the DOCR.OMS[1:0] bits selects data comparison mode.
(2) The 16-bit reference data is set in DODSR.
(3) 16-bit data for comparison is written to DODIR.
(4) Writing of 16-bit data continues until all data for comparison have been written to DODIR.
(5) If a value written to DODIR does not match that in DODSR, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note: When the DODIR register has the value after reset (0000h), the DOCR.DOPCF flag does not change to 1 if a value other than 0000h is set in the DODSR register. To perform data comparison, set the DODSR register and write a value to the DODIR register. If the DODSR register is set again after data comparison, the value remaining in the DODIR register will not be compared again with the value set in the DODSR register. That is, comparison proceeds in response to writing to the DODIR register but not in response to writing to the DODSR register.

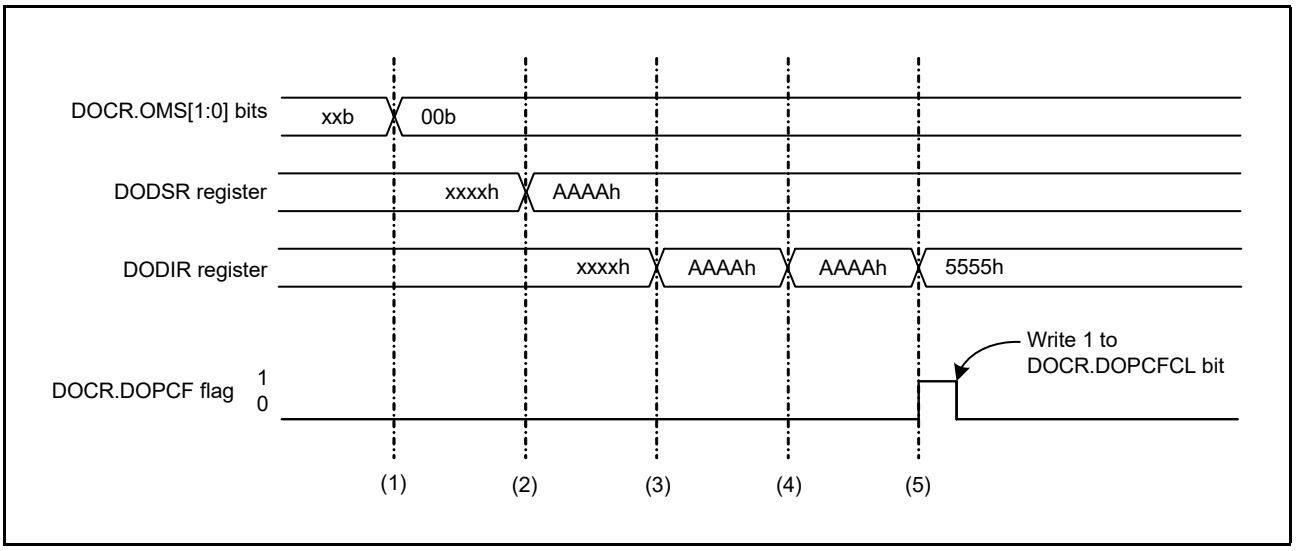


Figure 45.2 Example of Operation in Data Comparison Mode

45.3.2 Data Addition Mode

Figure 45.3 shows an example of the steps involved in data addition mode operation by the data operation circuit.

(1) Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
(2) 16-bit data is set in the DODSR register as the value after reset.
(3) 16-bit data to be added is written to DODIR. The result of the operation is stored in DODSR.
(4) Writing of 16-bit data continues until all data for addition have been written to DODIR.
(5) If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note: When the DODIR register has the value after reset (0000h), data addition is not performed if a value other than 0000h is set in the DODSR register. To perform data addition, set the DODSR register and write a value to be added into the DODIR register. If the DODSR register is set again after data addition, the value remaining in the DODIR register will not be added again to the value set in the DODSR register. That is, addition proceeds in response to writing to the DODIR register but not in response to writing to the DODSR register.

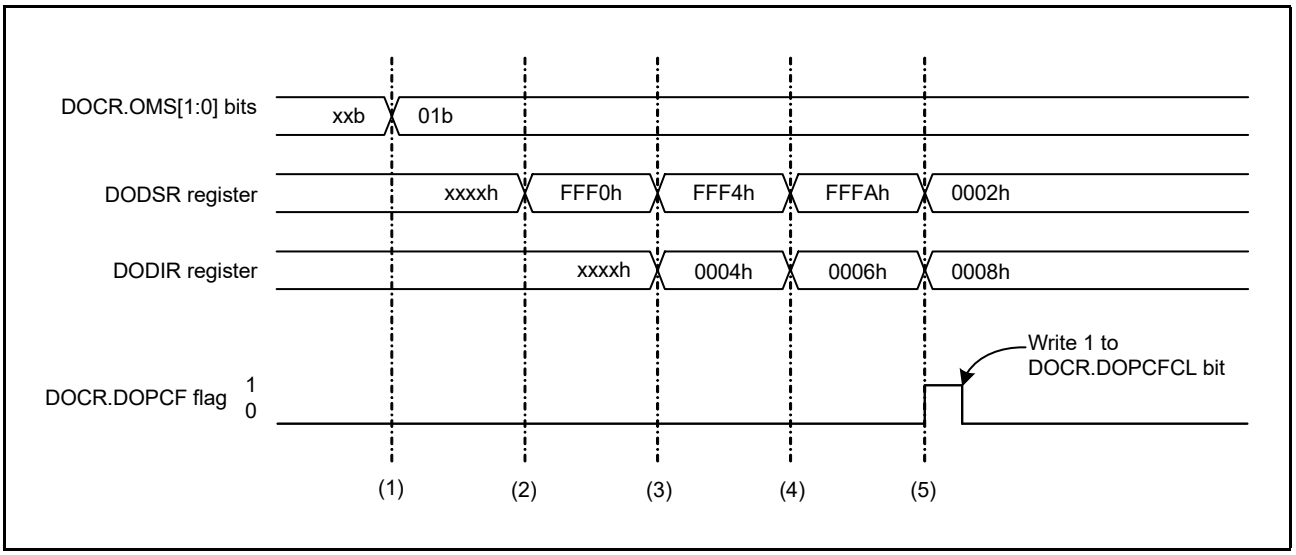


Figure 45.3 Example of Operation in Data Addition Mode

45.3.3 Data Subtraction Mode

Figure 45.4 shows an example of the steps involved in data subtraction mode operation by the data operation circuit.

(1) Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
(2) 16-bit data is set in the DODSR register as the value after reset.
(3) 16-bit data to be subtracted is written to DODIR. The result of the operation is stored in DODSR.
(4) Writing of 16-bit data continues until all data for subtraction have been written to DODIR.
(5) If the result of an operation is less than 0000h, the DOCR.DOPCF flag is set to 1. When the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also generated.

Note: When the DODIR register has the value after reset (0000h), data subtraction is not performed if a value other than 0000h is set in the DODSR register. To perform data subtraction, set the DODSR register and write a value to be subtracted into the DODIR register. If the DODSR register is set again after data subtraction, the value remaining in the DODIR register will not be subtracted again from the value set in the DODSR register. That is, subtraction proceeds in response to writing to the DODIR register but not in response to writing to the DODSR register.

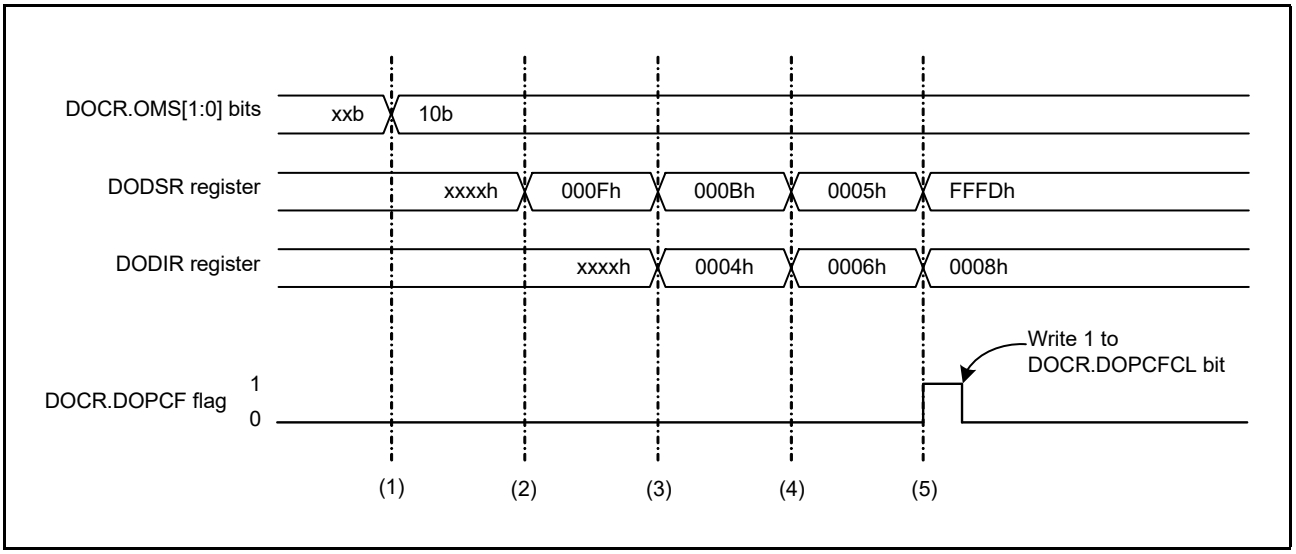


Figure 45.4 Example of Operation in Data Subtraction Mode

45.4 Interrupt Requests

The data operation circuit generates the data operation circuit interrupt as an interrupt request. When an interrupt source is generated, the data operation circuit flag (DOCR.DOPCF) corresponding to the interrupt is set to 1. Table 45.2 describes the interrupt request.

Table 45.2 Interrupt Request from Data Operation Circuit

Interrupt Request	Data Operation Circuit Flag	Interrupt Generation Timing
Data operation circuit interrupt	DOPCF	• The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h • The compared values either match or mismatch

Note: The data operation circuit interrupt is not conveyed to the interrupt controller, but it is conveyed to the error control module (ECM) as a DOC operation error.

45.5 Event Link Output

The DOC outputs event signals for the event link controller (ELC) under the following conditions, and these can be used to initiate operations by other modules selected in advance.

- The compared values either match or mismatch
- The result of data addition is greater than FFFFh
- The result of data subtraction is less than 0000h

45.5.1 Interrupt Handling and Event Linking

The data operation circuit (DOC) has a bit (DOCR.DOPCIE) to enable or disable interrupts. An interrupt request signal is output for the CPU when an interrupt source is generated while the corresponding enable bit is enabled.
In contrast, an event link output signal is sent to other modules as an event signal via the ELC when an interrupt source is generated, regardless of the setting of the corresponding interrupt enable bit.

45.6 Usage Note

45.6.1 Module Stop Function Setting

Operation of the data operation circuit can be disabled or enabled using module stop control register C (MSTPCRC). The value after reset indicates that the data operation circuit is in the stop state. Register access is enabled by canceling the module-stop state. For details, see section 9, Low-Power Consumption Function.

46. RAM (Product Option)

This LSI has on-chip high-speed RAM (with ECC error correction). The RAM, whose capacity is 1 Mbyte (512 Kbytes × 2), is installed.

46.1 Overview

Table 46.1 lists the specifications of the RAM.

Table 46.1 Specifications of RAM

Item	Description
RAM capacity	1 Mbyte
RAM addresses (for access from the Cortex-R4)	On-chip extended SRAM (area 1) 0400 0000h to 0407 FFFFh 2400 0000h to 2407 FFFFh (mirror) On-chip extended SRAM (area 2) 2000 0000h to 2007 FFFFh 2200 0000h to 2207 FFFFh (mirror)
RAM addresses (for products incorporating an R-IN engine) (for access from the Cortex-M3)	Instruction RAM 0000 0000h to 0007 FFFFh 0400 0000h to 0407 FFFFh (mirror) Data RAM 2000 0000h to 2007 FFFFh
Low-power consumption function	Operate only during access
Error checking	1-bit error correction, 2-bit error detection: The ECC decoder must be enabled to use these functions.
Initializing function	All areas of RAM are initialized to zero by a reset.

Note: The RAM is reset by the sources from the RES# pin input, the ECM, and software.

46.2 Register Descriptions

46.2.1 Protect Command Register (RAMPCMD)

The RAMPCMD register is used to provide write protection for registers that might seriously affect the system in order to prevent the application system from inadvertently stopping due to, for example, runaway of a program. Writing to the protected registers is disabled unless the PROTREL bit is set to 1.

Address(es): A00F 3000h
For access from the Cortex-M3
400F 3000h (for products incorporating an R-IN engine)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PROTREL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PROTREL	Enable Write Access to Protected Registers	1: Write access is enabled. 0: Write access is disabled (protected status).	R/W

To set the PROTREL bit of the RAMPCMD register to 1, the sequence shown below must be used. No special sequence is required to clear this bit to 0 or to read the register.

1. Write 0000 00A5h to the RAMPCMD register as a specific value.
2. Write 0000 0001h to the RAMPCMD register.
3. Write 0000 FFFEh to the RAMPCMD register.
4. Write 0000 0001h to the RAMPCMD register.

Note 1. In steps 1, 2, and 3, nothing is written to the register.
Note 2. Be sure to clear the PROTREL bit to 0 after writing to target registers is completed.

Table 46.2 Write-Protection Target Registers

Register Name	Symbol	R/W
Protect command register	RAMPCMD	R/W
ECC decoder configuration register	RAMEDC	R/W
ECC encoder configuration register	RAMEEC	R/W

46.2.2 ECC Decoder Configuration Register (RAMEDC)

Note: For products incorporating an R-IN engine, see section 46.2.3, ECC Decoder Configuration Register (RAMEDC) (for Products Incorporating an R-IN Engine).

The RAMEDC register controls the ECC decoders for the on-chip extended SRAM (areas 1 and 2).

Address(es): A00F 3100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECC_ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECC_ENABLE	ECC Decoder Enable	0: ECC decoder is disabled. 1: ECC decoder is enabled.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

When the RAMEDC.ECC_ENABLE bit is set to 1, ECC decoder logic for the on-chip extended SRAM (areas 1 and 2) is enabled, and the following functions are enabled, and this is conveyed to the error control module (ECM).

- 1-bit ECC error: Corrects the read data and conveys the error to the error control module (ECM).
- 2-bit ECC error: Conveys the error to the error control module (ECM).

When the RAMEDC.ECC_ENABLE bit is set to 0 (the “disabled” setting), even if an ECC error occurs, read data is not corrected or the error signal is not conveyed to the ECM. Therefore, retention of the status in the RAMDBEST register, capturing an error address in the RAMDBEAD register, and error count in the RAMDBECNT register are disabled.

Note 1. Switch this register while no masters are accessing the RAM.

Note 2. Writing to this register is disabled unless the write-protection is canceled by the RAMPCMD register.

46.2.3 ECC Decoder Configuration Register (RAMEDC) (for Products Incorporating an R-IN Engine)

The RAMEDC register controls the ECC decoders for instruction RAM and data RAM.

Address(es): 400F 3100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECC_ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ECC_ENABLE	ECC Decoder Enable	0: ECC decoder is disabled. 1: ECC decoder is enabled.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

When the RAMEDC.ECC_ENABLE bit is set to 1, ECC decoder logic for instruction RAM and data RAM are enabled, and the following functions are enabled, and this is conveyed to the error control module (ECM).

- For 1-bit ECC error: Correct the read data, and generate a 1-bit ECC error interrupt from the on-chip extended SRAM, and convey the interrupt signal to the error control module (ECM).
- For 2-bit ECC error: Generate a 2-bit ECC error interrupt from the on-chip extended SRAM and convey the interrupt signal to the error control module (ECM).

When the RAMEDC.ECC_ENABLE bit is set to 0 (the “disabled” setting), even if an ECC error occurs, read data is not corrected or the error signal is not conveyed to the ECM. Therefore, retention of the status in the RAMDBEST register, capturing an error address in the RAMDBEAD register, and error count in the RAMDBECNT register are disabled.

Note 1. Switch this register while no masters are accessing the RAM.

Note 2. Writing to this register is disabled unless the write-protection is canceled by the RAMPCMD register.

46.2.4 ECC Encoder Configuration Register (RAMEEC)

Note: For products incorporating an R-IN engine, see section 46.2.5, ECC Encoder Configuration Register (RAMEEC) (for Products Incorporating an R-IN Engine).

The RAMEEC register controls the self-test for the ECC circuit of the on-chip extended SRAM (areas 1 and 2).

If the RAMEEC.DBE_DISTn (n = 0 to 15) bit is set to 1, the Syndrome value (ECC redundancy bit data) is latched when the RAM corresponding to each bit is accessed. Then, when the RAM is accessed the next time, the latched Syndrome value is written to the RAM to inject an ECC error.

If the RAMEEC.DBE_DISTn (n = 0 to 15) bit is set to 0, the normal Syndrome value is always written to the RAM corresponding to each bit.

Address(es): A00F 3104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DBE_DIST15	DBE_DIST14	DBE_DIST13	DBE_DIST12	DBE_DIST11	DBE_DIST10	DBE_DIST9	DBE_DIST8	DBE_DIST7	DBE_DIST6	DBE_DIST5	DBE_DIST4	DBE_DIST3	DBE_DIST2	DBE_DIST1	DBE_DIST0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBE_DIST0	On-Chip Extended SRAM (area 1) BANK0 Way0 Syndrome Error Injection Enable	0: Normal Syndrome value is always written to the RAM. 1: The Syndrome value for the previous access is written to the RAM.	R/W
b1	DBE_DIST1	On-Chip Extended SRAM (area 1) BANK0 Way1 Syndrome Error Injection Enable		R/W
b2	DBE_DIST2	On-Chip Extended SRAM (area 1) BANK0 Way2 Syndrome Error Injection Enable		R/W
b3	DBE_DIST3	On-Chip Extended SRAM (area 1) BANK0 Way3 Syndrome Error Injection Enable		R/W
b4	DBE_DIST4	On-Chip Extended SRAM (area 1) BANK1 Way0 Syndrome Error Injection Enable		R/W
b5	DBE_DIST5	On-Chip Extended SRAM (area 1) BANK1 Way1 Syndrome Error Injection Enable		R/W
b6	DBE_DIST6	On-Chip Extended SRAM (area 1) BANK1 Way2 Syndrome Error Injection Enable		R/W
b7	DBE_DIST7	On-Chip Extended SRAM (area 1) BANK1 Way3 Syndrome Error Injection Enable		R/W
b8	DBE_DIST8	On-Chip Extended SRAM (area 2) BANK0 Way0 Syndrome Error Injection Enable		R/W
b9	DBE_DIST9	On-Chip Extended SRAM (area 2) BANK0 Way1 Syndrome Error Injection Enable		R/W
b10	DBE_DIST10	On-Chip Extended SRAM (area 2) BANK0 Way2 Syndrome Error Injection Enable		R/W
b11	DBE_DIST11	On-Chip Extended SRAM (area 2) BANK0 Way3 Syndrome Error Injection Enable		R/W
b12	DBE_DIST12	On-Chip Extended SRAM (area 2) BANK1 Way0 Syndrome Error Injection Enable		R/W
b13	DBE_DIST13	On-Chip Extended SRAM (area 2) BANK1 Way1 Syndrome Error Injection Enable		R/W
b14	DBE_DIST14	On-Chip Extended SRAM (area 2) BANK1 Way2 Syndrome Error Injection Enable		R/W
b15	DBE_DIST15	On-Chip Extended SRAM (area 2) BANK1 Way3 Syndrome Error Injection Enable		R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Switch this register while no masters are accessing the RAM.
Note 2. Writing to this register is disabled unless the write-protection is canceled by the RAMPCMD register.

46.2.5 ECC Encoder Configuration Register (RAMEEC) (for Products Incorporating an R-IN Engine)

The RAMEEC register controls the self-test for the ECC circuit of the instruction RAM and data RAM.
If the RAMEEC.DBE_DISTn (n = 0 to 15) bit is set to 1, the Syndrome value (ECC redundancy bit data) is latched when the RAM corresponding to each bit is accessed. Then, when the RAM is accessed the next time, the latched Syndrome value is written to the RAM to inject an ECC error.
If the RAMEEC.DBE_DISTn (n = 0 to 15) bit is set to 0, the normal Syndrome value is always written to the RAM corresponding to each bit.

Address(es): 400F 3104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DBE_DIST15	DBE_DIST14	DBE_DIST13	DBE_DIST12	DBE_DIST11	DBE_DIST10	DBE_DIST9	DBE_DIST8	DBE_DIST7	DBE_DIST6	DBE_DIST5	DBE_DIST4	DBE_DIST3	DBE_DIST2	DBE_DIST1	DBE_DIST0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBE_DIST0	Instruction RAM BANK0 Way0 Syndrome Error Injection Enable	0: Normal Syndrome value is always written to the RAM. 1: The Syndrome value for the previous access is written to the RAM.	R/W
b1	DBE_DIST1	Instruction RAM BANK0 Way1 Syndrome Error Injection Enable		R/W
b2	DBE_DIST2	Instruction RAM BANK0 Way2 Syndrome Error Injection Enable		R/W
b3	DBE_DIST3	Instruction RAM BANK0 Way3 Syndrome Error Injection Enable		R/W
b4	DBE_DIST4	Instruction RAM BANK1 Way0 Syndrome Error Injection Enable		R/W
b5	DBE_DIST5	Instruction RAM BANK1 Way1 Syndrome Error Injection Enable		R/W
b6	DBE_DIST6	Instruction RAM BANK1 Way2 Syndrome Error Injection Enable		R/W
b7	DBE_DIST7	Instruction RAM BANK1 Way3 Syndrome Error Injection Enable		R/W
b8	DBE_DIST8	Data RAM BANK0 Way0 Syndrome Error Injection Enable		R/W
b9	DBE_DIST9	Data RAM BANK0 Way1 Syndrome Error Injection Enable		R/W
b10	DBE_DIST10	Data RAM BANK0 Way2 Syndrome Error Injection Enable		R/W
b11	DBE_DIST11	Data RAM BANK0 Way3 Syndrome Error Injection Enable		R/W
b12	DBE_DIST12	Data RAM BANK1 Way0 Syndrome Error Injection Enable		R/W
b13	DBE_DIST13	Data RAM BANK1 Way1 Syndrome Error Injection Enable		R/W
b14	DBE_DIST14	Data RAM BANK1 Way2 Syndrome Error Injection Enable		R/W
b15	DBE_DIST15	Data RAM BANK1 Way3 Syndrome Error Injection Enable		R/W

Bit	Symbol	Bit Name	Description	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Switch this register while no masters are accessing the RAM.
Note 2. Writing to this register is disabled unless the write-protection is canceled by the RAMPCMD register.

46.2.6 2-Bit ECC Error Status Register (RAMDBEST)

Note: For products incorporating an R-IN engine, see section 46.2.7, 2-Bit ECC Error Status Register (RAMDBEST) (for Products Incorporating an R-IN Engine).

The RAMDBEST register indicates the 2-bit ECC error status for the on-chip extended SRAM (areas 1 and 2). After the error signal is conveyed to the error control module (ECM), read this register to identify the BANK and WAY in which a 2-bit ECC error occurred.

Address(es): A00F 3108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DBE_RAM15	DBE_RAM14	DBE_RAM13	DBE_RAM12	DBE_RAM11	DBE_RAM10	DBE_RAM9	DBE_RAM8	DBE_RAM7	DBE_RAM6	DBE_RAM5	DBE_RAM4	DBE_RAM3	DBE_RAM2	DBE_RAM1	DBE_RAM0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBE_RAM0	On-Chip Extended SRAM (area 1) Bank0 Way0 2-Bit ECC Error Detection	0: No error 1: Error occurred.	R
b1	DBE_RAM1	On-Chip Extended SRAM (area 1) Bank0 Way1 2-Bit ECC Error Detection		R
b2	DBE_RAM2	On-Chip Extended SRAM (area 1) Bank0 Way2 2-Bit ECC Error Detection		R
b3	DBE_RAM3	On-Chip Extended SRAM (area 1) Bank0 Way3 2-Bit ECC Error Detection		R
b4	DBE_RAM4	On-Chip Extended SRAM (area 1) Bank1 Way0 2-Bit ECC Error Detection		R
b5	DBE_RAM5	On-Chip Extended SRAM (area 1) Bank1 Way1 2-Bit ECC Error Detection		R
b6	DBE_RAM6	On-Chip Extended SRAM (area 1) Bank1 Way2 2-Bit ECC Error Detection		R
b7	DBE_RAM7	On-Chip Extended SRAM (area 1) Bank1 Way3 2-Bit ECC Error Detection		R
b8	DBE_RAM8	On-Chip Extended SRAM (area 2) Bank0 Way0 2-Bit ECC Error Detection		R
b9	DBE_RAM9	On-Chip Extended SRAM (area 2) Bank0 Way1 2-Bit ECC Error Detection		R
b10	DBE_RAM10	On-Chip Extended SRAM (area 2) Bank0 Way2 2-Bit ECC Error Detection		R
b11	DBE_RAM11	On-Chip Extended SRAM (area 2) Bank0 Way3 2-Bit ECC Error Detection		R
b12	DBE_RAM12	On-Chip Extended SRAM (area 2) Bank1 Way0 2-Bit ECC Error Detection		R
b13	DBE_RAM13	On-Chip Extended SRAM (area 2) Bank1 Way1 2-Bit ECC Error Detection		R
b14	DBE_RAM14	On-Chip Extended SRAM (area 2) Bank1 Way2 2-Bit ECC Error Detection		R
b15	DBE_RAM15	On-Chip Extended SRAM (area 2) Bank1 Way3 2-Bit ECC Error Detection		R
b31 to b16	—	Reserved	These bits are read as 0.	R

Note 1. Reading this register clears the ECC error source.

46.2.7 2-Bit ECC Error Status Register (RAMDBEST) (for Products Incorporating an R-IN Engine)

The RAMDBEST register indicates the 2-bit ECC error status for the instruction RAM and data RAM.
After a 2-bit ECC error interrupt is generated from the on-chip extended SRAM or the error signal is conveyed to the error control module (ECM), read this register to identify the BANK and WAY in which a 2-bit ECC error occurred.

Address(es): 400F 3108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DBE_RAM15	DBE_RAM14	DBE_RAM13	DBE_RAM12	DBE_RAM11	DBE_RAM10	DBE_RAM9	DBE_RAM8	DBE_RAM7	DBE_RAM6	DBE_RAM5	DBE_RAM4	DBE_RAM3	DBE_RAM2	DBE_RAM1	DBE_RAM0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DBE_RAM0	Instruction RAM Bank0 Way0 2-Bit ECC Error Detection Flag	0: No error 1: Error occurred.	R
b1	DBE_RAM1	Instruction RAM Bank0 Way1 2-Bit ECC Error Detection Flag		R
b2	DBE_RAM2	Instruction RAM Bank0 Way2 2-Bit ECC Error Detection Flag		R
b3	DBE_RAM3	Instruction RAM Bank0 Way3 2-Bit ECC Error Detection Flag		R
b4	DBE_RAM4	Instruction RAM Bank1 Way0 2-Bit ECC Error Detection Flag		R
b5	DBE_RAM5	Instruction RAM Bank1 Way1 2-Bit ECC Error Detection Flag		R
b6	DBE_RAM6	Instruction RAM Bank1 Way2 2-Bit ECC Error Detection Flag		R
b7	DBE_RAM7	Instruction RAM Bank1 Way3 2-Bit ECC Error Detection Flag		R
b8	DBE_RAM8	Data RAM Bank0 Way0 2-Bit ECC Error Detection Flag		R
b9	DBE_RAM9	Data RAM Bank0 Way1 2-Bit ECC Error Detection Flag		R
b10	DBE_RAM10	Data RAM Bank0 Way2 2-Bit ECC Error Detection Flag		R
b11	DBE_RAM11	Data RAM Bank0 Way3 2-Bit ECC Error Detection Flag		R
b12	DBE_RAM12	Data RAM Bank1 Way0 2-Bit ECC Error Detection Flag		R
b13	DBE_RAM13	Data RAM Bank1 Way1 2-Bit ECC Error Detection Flag		R
b14	DBE_RAM14	Data RAM Bank1 Way2 2-Bit ECC Error Detection Flag		R
b15	DBE_RAM15	Data RAM Bank1 Way3 2-Bit ECC Error Detection Flag		R
b31 to b16	—	Reserved	These bits are read as 0.	R

Note 1. Reading this register clears the ECC error source.

46.2.8 2-Bit ECC Error Address Register (RAMDBEAD)

Note: For products incorporating an R-IN engine, see section 46.2.9, 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine).

The RAMDBEAD register is a read-only register that holds the address where a 2-bit ECC error was found.

When a 2-bit ECC error is detected, the ECC error generation address is captured with the detection signal as a trigger, and then is stored in the ADDRESS[15:0] bits.

The register in which an ECC error generation address has been captured cannot retain the next ECC error generation address unless the LOCK bit of the register is enabled and the register is read. Therefore, if you want to capture a new ECC error generation address, you must first read this register.

Address(es): A00F 310Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	BANK[1:0]		ADDRESS[15:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDRESS[15:0]														—	LOCK
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LOCK	Lock Enable	0: Register unlocked (2-bit ECC error generation address can be captured.) 1: Register locked (2-bit ECC error generation address cannot be captured.) Read this register to unlock the registers.	R
b1	—	Reserved	This bit is read as 0.	R
b17 to b2	ADDRESS [15:0]	2-Bit ECC Error Generation Address	The 2-bit ECC error generation address is retained.	R
b19, b18	BANK[1:0]	2-Bit ECC Error Generation BANK	These bits indicate the number of the bank where a 2-bit ECC error was encountered. 0: On-chip extended SRAM (area 1) BANK0 1: On-chip extended SRAM (area 1) BANK1 2: On-chip extended SRAM (area 2) BANK0 3: On-chip extended SRAM (area 2) BANK1	R
b31 to b20	—	Reserved	These bits are read as 0.	R

Note: If 2-bit ECC errors occur at the same time in different WAYs, the priority of captured addresses is as follows:
On-chip extended SRAM (area 1) BANK0 WAY0 > On-chip extended SRAM (area 1) BANK0 WAY1 >
On-chip extended SRAM (area 1) BANK0 WAY2 > On-chip extended SRAM (area 1) BANK0 WAY3 >
On-chip extended SRAM (area 1) BANK1 WAY0 > On-chip extended SRAM (area 1) BANK1 WAY1 >
On-chip extended SRAM (area 1) BANK1 WAY2 > On-chip extended SRAM (area 1) BANK1 WAY3 >
On-chip extended SRAM (area 2) BANK0 WAY0 > On-chip extended SRAM (area 2) BANK0 WAY1 >
On-chip extended SRAM (area 2) BANK0 WAY2 > On-chip extended SRAM (area 2) BANK0 WAY3 >
On-chip extended SRAM (area 2) BANK1 WAY0 > On-chip extended SRAM (area 2) BANK1 WAY1 >
On-chip extended SRAM (area 2) BANK1 WAY2 > On-chip extended SRAM (area 2) BANK1 WAY3

46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine)

The RAMDBEAD register is a read-only register that holds the address where a 2-bit ECC error was found.
When a 2-bit ECC error is detected, the ECC error generation address is captured with the detection signal as a trigger, and then is stored in the ADDRESS[15:0] bits.
The register in which an ECC error generation address has been captured cannot retain the next ECC error generation address unless the LOCK bit of the register is enabled and the register is read. Therefore, if you want to capture a new ECC error generation address, you must first read this register.

Address(es): 400F 310Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	BANK[1:0]		ADDRESS[15:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADDRESS[15:0]														—	LOCK
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	LOCK	Lock Enable	0: Register unlocked (2-bit ECC error generation address can be captured.) 1: Register locked (2-bit ECC error generation address cannot be captured.) Read this register to unlock the registers.	R
b1	—	Reserved	This bit is read as 0.	R
b17 to b2	ADDRESS [15:0]	2-Bit ECC Error Generation Address	The 2-bit ECC error generation address is retained.	R
b19, b18	BANK[1:0]	2-Bit ECC Error Generation BANK	These bits indicate the number of the bank where a 2-bit ECC error was encountered. 0: Instruction RAM BANK0 1: Instruction RAM BANK1 2: Data RAM BANK0 3: Data RAM BANK1	R
b31 to b20	—	Reserved	These bits are read as 0.	R

Note: If 2-bit ECC errors occur at the same time in different WAYs, the priority of captured addresses is as follows:
Instruction RAM BANK0 WAY0 > Instruction RAM BANK0 WAY1 >
Instruction RAM BANK0 WAY2 > Instruction RAM BANK0 WAY3 >
Instruction RAM BANK1 WAY0 > Instruction RAM BANK1 WAY1 >
Instruction RAM BANK1 WAY2 > Instruction RAM BANK1 WAY3 >
Data RAM BANK0 WAY0 > Data RAM BANK0 WAY1 >
Data RAM BANK0 WAY2 > Data RAM BANK0 WAY3 >
Data RAM BANK1 WAY0 > Data RAM BANK1 WAY1 >
Data RAM BANK1 WAY2 > Data RAM BANK1 WAY3

46.2.10 2-Bit ECC Error Counter Register (RAMDBECNT)

The RAMDBECNT register is a read-only register that retains the 2-bit ECC error count.
If a 2-bit ECC error is detected, the error counter is incremented with the detection signal as a trigger.
If the counter value exceeds the maximum (Fh), it is cleared to 0h.

Address(es): A00F 3110h
For access from the Cortex-M3
400F 3110h (for products incorporating an R-IN engine)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	ERRCOUNT[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	ERRCOUNT [3:0]	2-Bit ECC Error Counter	The 2-bit ECC error count is retained.	R
b31 to b4	—	Reserved	These bits are read as 0.	R

Note: Even if 2-bit ECC errors occur at the same time in different WAYs, the count-up value is 1.

46.3 Description of Operation

46.3.1 Configuration of Memory Map

The instruction RAM and data RAM areas are separate 512-Kbyte RAMs, each having a two-bank four-way configuration.

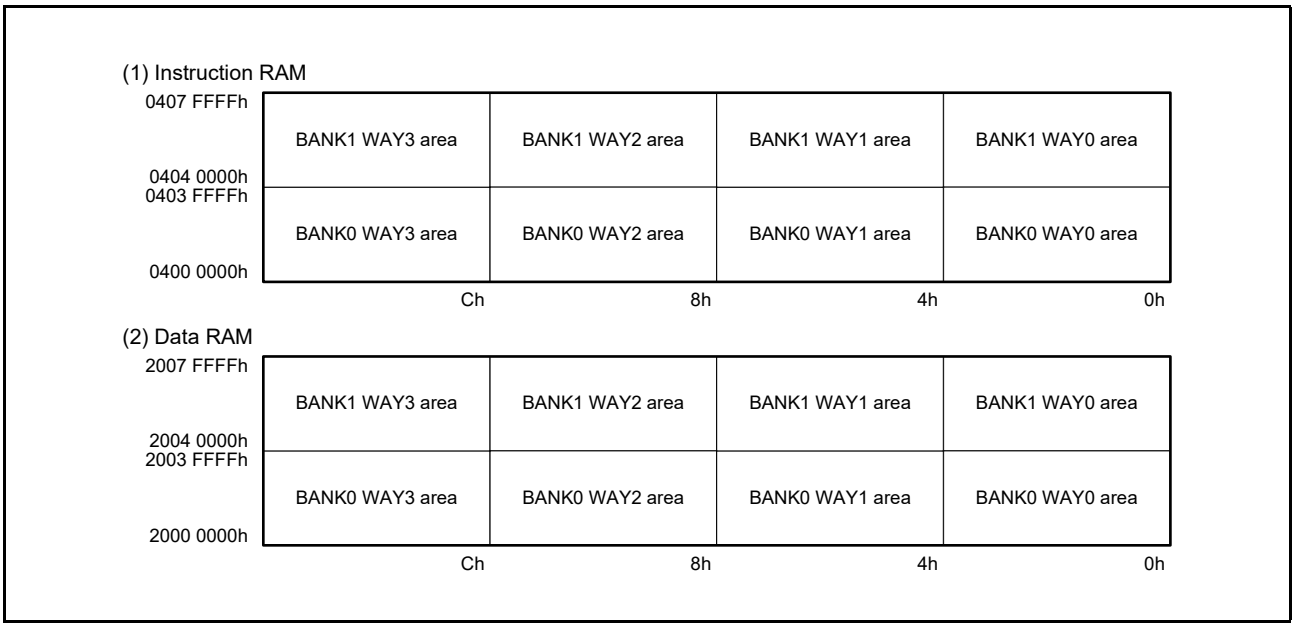


Figure 46.1 Configuration of Memory

46.3.2 ECC Error Correction Function

The RAMEDC register enables or disables ECC error correction in the 1-Mbyte space. ECCs can be used to correct 1-bit errors and detect 2-bit errors. The error control module (ECM) detects the sources of 2-bit errors, and the RAMDBEST register is used to check the way in which an error was found. Moreover, the RAMDBEAD register can be used to identify the address where a 2-bit error was found, and the RAMDBECNT indicates the number of 2-bit errors that have been encountered.

46.3.3 Self-Testing of the ECC Circuit

Self-testing of the ECC circuit proceeds in way units. The RAMEEC register sets the target area for each way. The following shows an example of the procedure for self-testing of the ECC circuit.

(1) Example of ECC error-injection setting procedure

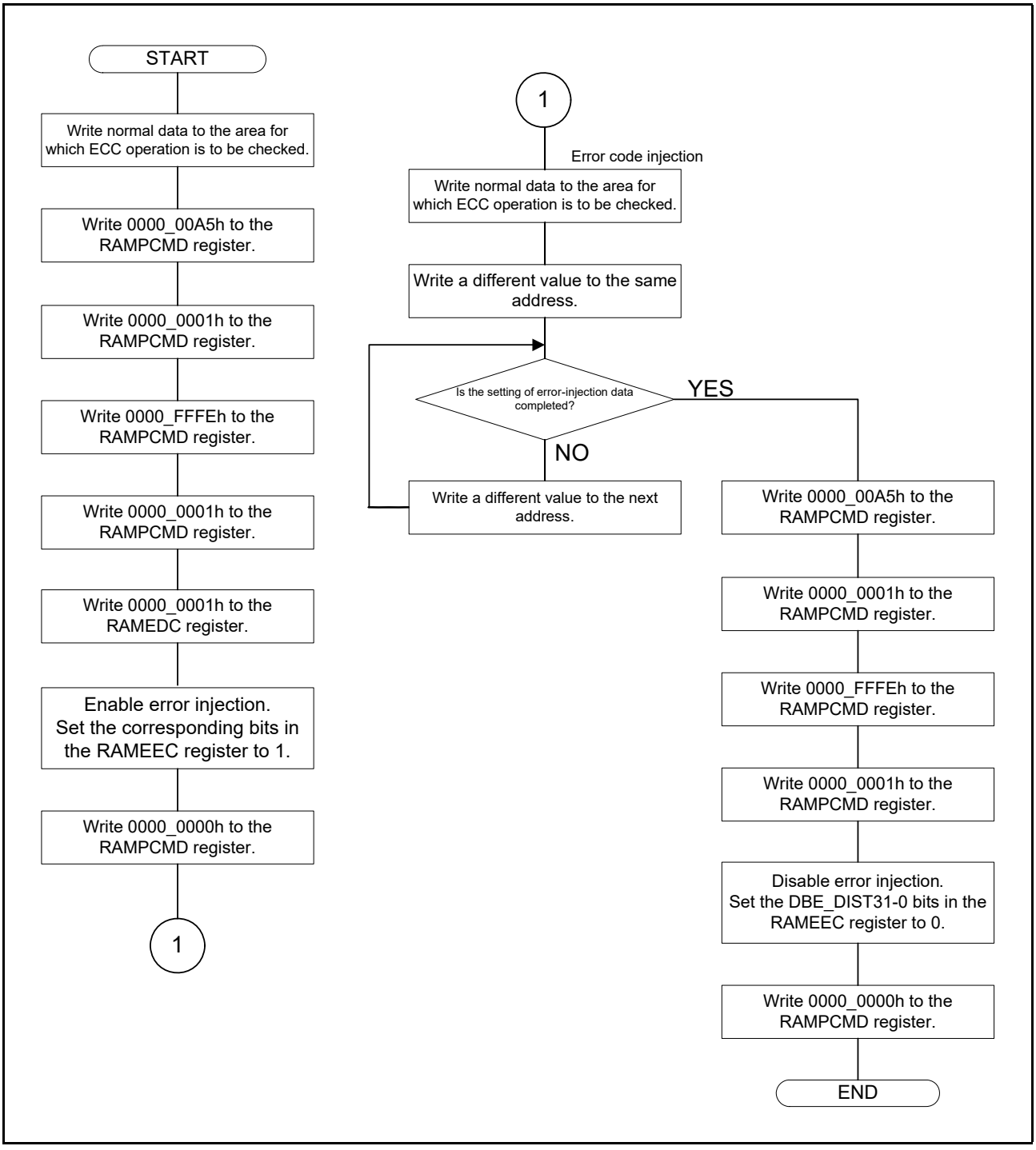
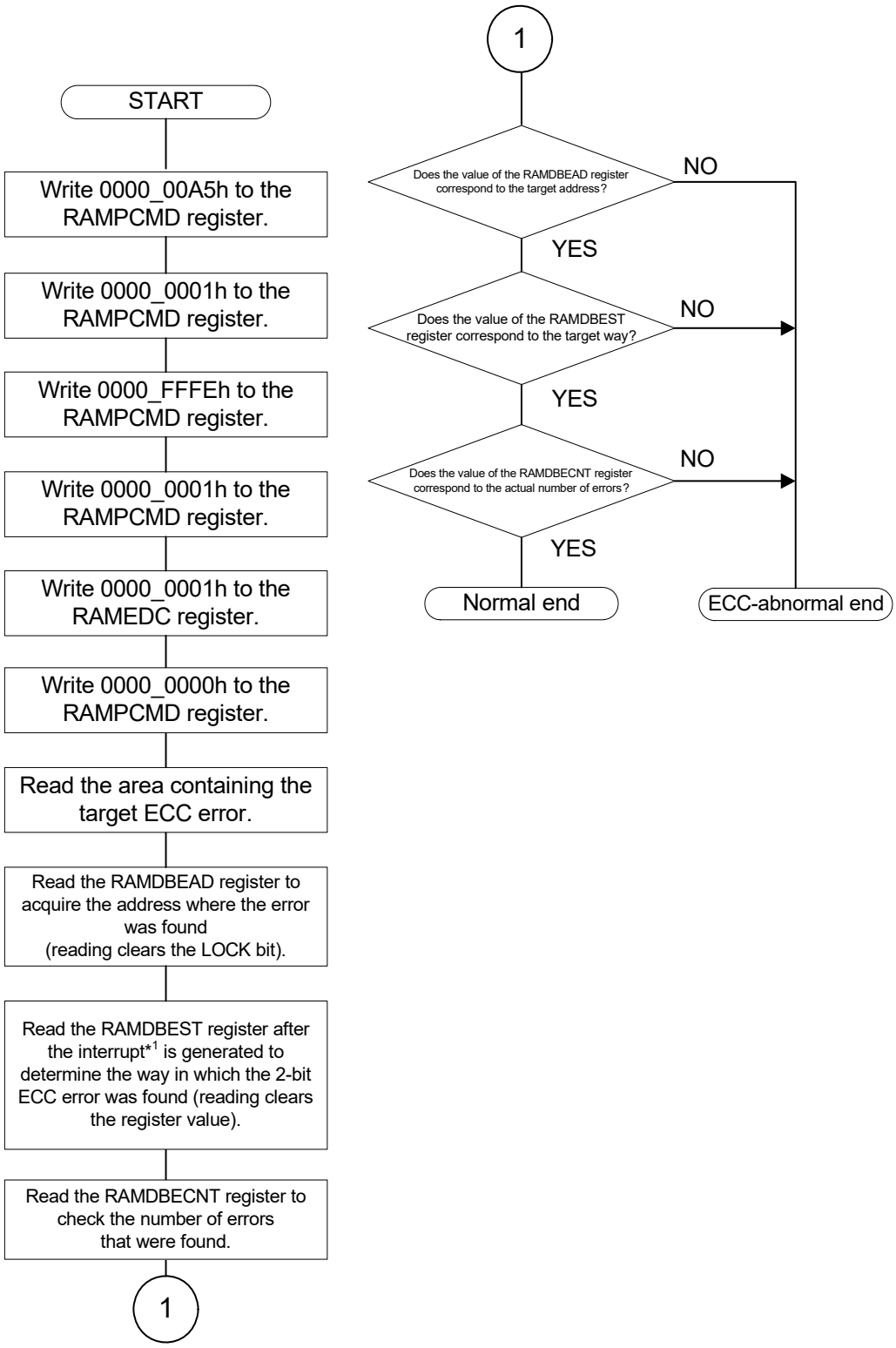


Figure 46.2 Example of ECC Error-Injection Setting Procedure

(2) Procedure for Checking ECC Operation



Note 1. For the Cortex-M3, ETHRSE2 interrupt is used to connect the error signal to the NVIC. For the Cortex-R4, the ERRD interrupt via the ECM is used.

Figure 46.3 Procedure of Checking ECC Operation

47. Electrical Characteristics

47.1 Absolute Maximum Ratings

Table 47.1 Absolute Maximum Rating

Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V

Item	Symbol	Value	Unit
Power supply voltage (I/O)	VCCQ33	-0.3 to +4.2	V
Power supply voltage (internal)	VDD	-0.3 to +1.6	V
PLL power supply voltage	PLLVDD0, PLLVDD1	-0.3 to +1.6	V
Input voltage (except for ports for 5-V tolerant*1)	V_{in1}	-0.3 to VCCQ33 + 0.3*5	V
Input voltage (ports for 5-V tolerant*1)	V_{in2}	-0.3 to +5.5*3	V
Analog power supply voltage	AVCC0, AVCC1*2	-0.3 to +4.2	V
Reference power supply voltage	VREFH0, VREFH1	-0.3 to (AVCC0, AVCC1) + 0.3*5	V
USB digital power supply voltage	DVDD_USB	-0.3 to +1.6	V
USB power supply voltage	VDD33_USB*2	-0.3 to +4.2	V
Analog input voltage	V_{AN}	-0.3 to (AVCC0, AVCC1) + 0.3*5	V
Operating temperature (junction temperature)	Tj*4	-40 to +125	°C
Storage temperature	T_{stg}	-55 to +125	°C

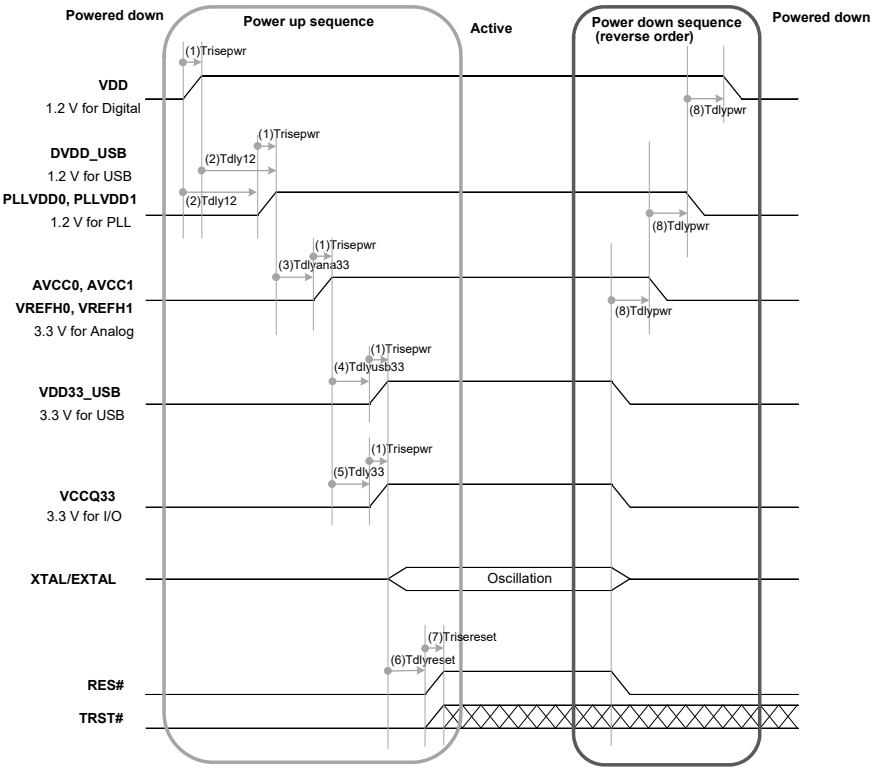
[Usage Notes]

1. Do not directly connect output pins (I/O pins in output state) of IC products to other output pins (including I/O pins in output state) , power pins, or GND pins. However, output pins are directly connectable in an external circuit where timing design is provided to avoid conflict of outputs of high-impedance pins such as I/O pins.
2. If even a single item exceeds the absolute maximum rating for even a moment, it may degrade the product's quality. In other words, the absolute maximum rating is a rated value that potentially causes physical damage to products. Use products with a margin of the absolute maximum rating.
   Specified values and conditions shown in DC characteristics and AC characteristics are the range of normal operation and quality assurance of products.

Note 1. Ports PC0 to PC7 and P30 are 5-V tolerant.
Note 2. When the A/D converter unit 0 is not to be used, connect the AVCC0 and VREFH0 pins to VCCQ33 and the AVSS0 and VREFL0 pins to VSS, respectively. Do not leave these pins open. In the same way, when the A/D converter unit 1 is not to be used, connect the AVCC1 and VREFH1 pins to VCCQ33 and the AVSS1 and VREFL1 pins to VSS, respectively. Do not leave these pins open. When the USB is not to be used, connect the VDD33_USB pin to VCCQ33, the VSS_USB pin to VSS, and the DVDD_USB pin to VDD, respectively. Do not leave these pins open.
Note 3. When VCCQ33 is less than 3.0 V, the rated value of ports for 5-V tolerant is 3.6 V.
Note 4. For operations at the temperatures over 110 °C (junction temperature), refer to the RZ/T1 Group Application Note: Precautions for High-Temperature Operations (R01AN3116).
Note 5. Do not exceed the absolute maximum rating, 4.2 V.

47.2 Power On/Off Sequence

Turn on and off each power supply voltage according to the procedure shown in the figure below.
When turning on the power, be sure to fix TRST# pins and RES# pins to the low level. Otherwise, initialization is not performed successfully.



Timing

		Value		
No.	Item	min	typ	max
(1)	Trisepwr	100 µs	—	50 ms
(2)	Tdly12	0 ms	—	100 ms
(3)	Tdlyana33	0 ms	—	100 ms
(4)	Tdlyusb33	0 ms	—	100 ms
(5)	Tdly33	0 ms	—	100 ms
(6)	Tdlyreset	10 ms	—	—
(7)	Trisereset	—	—	150 µs
(8)	Tdlypwr	0 ms	—	—

Note 1. Turn on all power supply voltages and reset signals with a monotonic increase and turn off with a monotonic decrease.
Note 2. Do not apply a negative voltage to power supply voltages.
Note 3. Before turning on the power, be sure to make reset pins (TRST# and RES#) active (low). Otherwise, inputs and outputs on the pins may be unstable. If this may also be a problem when turning off the power, make reset pins (TRST# and RES#) active (low.)

Note: If the power on/off sequence is not met (out of operation guarantee range), the pin input state and output state may be undefined.

Figure 47.1 Power On/Off Sequence

47.3 DC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = -40 to 125°C

Note: The 176-pin HLFQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 47.2 DC Characteristics (1)

Item	Symbol	min	typ	max	Unit	Test Conditions
Power supply voltage (I/O)	VCCQ33	3.0	3.3	3.6	V	
Power supply voltage (internal)	VDD	1.14	1.2	1.26	V	
PLL power supply voltage	PLLVDD0, PLLVDD1	1.14	1.2	1.26	V	
USB digital power supply voltage	DVDD_USB	1.14	1.2	1.26	V	
Analog power supply voltage	AVCC0, AVCC1	3.0	3.3	3.6	V	
USB power supply voltage	VDD33_USB	3.0	3.3	3.6	V	

Table 47.3 DC Characteristics (2) [Power Supply] (1 / 2)

Item	Type		Symbol	typ	max	Unit	Test Conditions
Normal operation	VDD	600MHz	Vlcc	330	820	mA	Tj = -40 to 125 °C (R7S910018CBG, R7S910118CBG)
				273	752	mA	Tj = -40 to 125 °C (R7S910017CBG, R7S910117CBG)
				265	740	mA	Tj = -40 to 125 °C (R7S910028CBG, R7S910128CBG)
				258	731	mA	Tj = -40 to 125 °C (R7S910013CBG, R7S910113CBG)
				209	673	mA	Tj = -40 to 125 °C (R7S910027CBG, R7S910127CBG)
				201	663	mA	Tj = -40 to 125 °C (R7S910007CBG, R7S910107CBG)
		450MHz		310	798	mA	Tj = -40 to 125 °C (R7S910016CBG, R7S910116CBG)
				253	730	mA	Tj = -40 to 125 °C (R7S910015CBG, R7S910115CBG)
				245	718	mA	Tj = -40 to 125 °C (R7S910026CBG, R7S910126CBG)
				238	709	mA	Tj = -40 to 125 °C (R7S910011CBG, R7S910111CBG)
				189	651	mA	Tj = -40 to 125 °C (R7S910025CBG, R7S910125CBG)
				181	641	mA	Tj = -40 to 125 °C (R7S910002CBG, R7S910006CBG, R7S910102CBG, R7S910106CBG)
				180	640	mA	Tj = -40 to 125 °C (R7S910001CFP, R7S910101CFP)
		300MHz		225	696	mA	Tj = -40 to 125 °C (R7S910036CBG, R7S910136CBG)
				169	629	mA	Tj = -40 to 125 °C (R7S910035CBG, R7S910135CBG)
	PLLVDD0 + PLLVDD1		PLLIcc	3.2	5	mA	
	VCCQ33		V33Icc	19*1, *2	—	mA	
	AVCC0		AV0Icc	2	5	mA	A/D conversion (unit 0)
	AVCC1		AV1Icc	0.7	1.5	mA	A/D conversion (unit 1)

Table 47.3 DC Characteristics (2) [Power Supply] (2 / 2)

Item	Type	Symbol	typ	max	Unit	Test Conditions
Normal operation	VREFH0	VRF0Icc	0.07	0.2	mA	A/D conversion (unit 0)
	VREFH1	VRF1Icc	0.07	0.2	mA	A/D conversion (unit 1)
	DVDD_USB	V12UIcc	5.1	9	mA	USB high-speed communication
			3.5	9	mA	USB full-speed communication
	VDD33_USB	V33UIcc	15*1	—	mA	USB high-speed communication
			10*1	—	mA	USB full-speed communication
Standby mode with all modules being inactive (reference value)	VDD	VIcc	41	—	mA	
	PLLVDD0 + PLLVDD1	PLLIcc	3.2	—	mA	
	VCCQ33	V33Icc	0.35*1, *2	—	mA	
	AVCC0	AV0Icc	0.64	—	µA	
	AVCC1	AV1Icc	0.32	—	µA	
	VREFH0	VRF0Icc	0.24	—	µA	
	VREFH1	VRF1Icc	0.24	—	µA	
	DVDD_USB	V12UIcc	3.5	—	mA	UTMI suspend mode
	VDD33_USB	V33UIcc	9.6*1	—	mA	UTMI suspend mode

Note 1. These values are reference values. The actual operating current greatly depends on the system (such as unsharpened waveforms due to I/O load and toggle frequency). Be sure to measure these current values in the system.

Note 2. V33Icc must be 80 mA or less. (ΣI_{OH} in Table 47.9)

Table 47.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins]

Item		Symbol	min	typ	max	Unit	Test Conditions
Schmitt trigger Input voltage	Other than 5-V tolerant pins	V_{IH1}	2.4	—	VCCQ33 + 0.3	V	
		V_{IL1}	–0.3	—	0.8	V	
		ΔV_{T1}	VCCQ33 × 0.05	—	—	V	
	5-V tolerant pins*1	V_{IH2}	VCCQ33 × 0.7	—	5.3*2	V	
		V_{IL2}	–0.3	—	VCCQ33 × 0.3	V	
		ΔV_{T2}	VCCQ33 × 0.05	—	—	V	
Input high level voltage (except for schmitt trigger input pins)		V_{IH3}	2.4	—	VCCQ33 + 0.3	V	
Input low level voltage (except for schmitt trigger input pins)		V_{IL3}	–0.3	—	0.8	V	
Output high level voltage	Other than 5-V tolerant pins	V_{OH}	VCCQ33 – 0.5	—	—	V	I_{OH} = -2 mA
Output low level voltage	Other than 5-V tolerant pins	V_{OL1}	—	—	0.4	V	I_{OL1} = 2 mA
	5-V tolerant pins*1	V_{OL2}	—	—	0.4	V	I_{OL2} = 3 mA
			—	—	0.6	V	I_{OL2} = 6 mA
Input leakage current		$\lvert I_{in} \rvert$	—	—	1.0	µA	$V_{in1} = V_{in2}$ = 0 V $V_{in1} = V_{in2}$ = VCCQ33
Three-state leakage current (off state)	Input/output and output pins excluding 5-V tolerant pins	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in1} = 0 V V_{in1} = VCCQ33
	5-V tolerant pins*1		—	—	5.0	µA	V_{in2} = 0 V V_{in2} = VCCQ33
Input pull-up MOS current and resistance	Ports P50 to P56, P86 to P87, P90 to P97, PD0 to PD7	I_{pu1}	–300	—	–30	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu1}	10	—	120	kΩ	
	Pins other than the above*3	I_{pu2}	–120	—	–7	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = 0 V
		R_{pu2}	25	—	515	kΩ	
Input pull-down MOS current and resistance	Ports P50 to P56, P86 to P87, P90 to P97, PD0 to PD7	I_{pd1}	30	—	300	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd1}	10	—	120	kΩ	
	Pins other than the above*3	I_{pd2}	7	—	120	µA	VCCQ33 = 3.0 to 3.6 V $V_{in1} = V_{in2}$ = VCCQ33
		R_{pd2}	25	—	515	kΩ	
Pin capacity	All input/output and input pins	C_{in}	—	—	10	pF	

Note 1. Ports PC0 to PC7 and P30 are 5-V tolerant.
Note 2. When VCCQ33 is less than 3.00 V, do not apply voltage of 3.6 V or higher to 5-V tolerant pins.
Note 3. 5-V tolerant pins are not included.

Table 47.5 DC Characteristics (4) [USB2.0 USB_RREF Pin]

Item	Symbol	min	typ	max	Unit	Test Conditions
Reference resistor	R_{REF}	200 ±1%			Ω	

Table 47.6 DC Characteristics (5) [USB2.0 Host/Function-Related Pins (Items for Both Full Speed and High Speed)*1]

Item	Symbol	min	typ	max	Unit	Test Conditions
DP pull-up resistor (when the function controller operation is selected)	R_{PU}	0.900	—	1.575	kΩ	Idle
		1.425	—	3.090	kΩ	Transmission/ reception
DP/DM pull-down resistors (when the host function is selected)	R_{PD}	14.25	—	24.80	kΩ	

Note 1. USB_DP and USB_DM pins

Table 47.7 DC Characteristics (6) [USB2.0 Host/Function-Related Pins (Full Speed)*1]

Item	Symbol	min	typ	max	Unit	Measuring Condition
Input high level voltage	V_{FSIH}	2.0	—	—	V	
Input low level voltage	V_{FSIL}	—	—	0.8	V	
Differential input sensitivity	V_{FSDI}	0.2	—	—	V	| (USB_DP) – (USB_DM) |
Differential common mode range	V_{FSCM}	0.8	—	2.5	V	
Output high level voltage	V_{FSOH}	2.8	—	3.6	V	I_{FSOH} = -200 µA
Output low level voltage	V_{FSOL}	0.0	—	0.3	V	I_{FSOL} = 2 mA
Output signal crossover voltage	V_{FSCRS}	1.3	—	2.0	V	CL = 50 pF (full-speed)

Note 1. USB_DP and USB_DM pins

Table 47.8 DC Characteristics (7) [USB2.0 Host/Function-Related Pins (High Speed)*1]

Item	Symbol	min	typ	max	Unit	Test Conditions
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	100	—	150	mV	
Common mode voltage range	V_{HSCM}	-50	—	500	mV	
Idle state	V_{HSOI}	-10.0	—	10.0	mV	
Output high level voltage	V_{HSOH}	360	—	440	mV	
Output low level voltage	V_{HSOL}	-10.0	—	10.0	mV	
Chirp J output voltage (differential)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K output voltage (differential)	V_{CHIRPK}	-900	—	-500	mV	

Note 1. USB_DP and USB_DM pins

Table 47.9 Permissible Output Currents

Item		Symbol	min	typ	max	Unit
Permissible output low current (average value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	2.0	mA
	5-V tolerant pins	I_{OL2}	—	—	3.0	mA
Permissible output low current (maximum value per pin)	Other than 5-V tolerant pins	I_{OL1}	—	—	4.0	mA
	5-V tolerant pins	I_{OL2}	—	—	6.0	mA
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins	I_{OH}	—	—	-2.0	mA
Permissible output high current (maximum value per pin)	All output pins	I_{OH}	—	—	-4.0	mA
Permissible output high current (total)	Total of all output pins	ΣI_{OH}	—	—	-80	mA

[Usage Note] All output current values shall be within the values in Table 47.9 to ensure the reliability of this LSI.

47.4 AC Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = -40 to 125°C

Note: The 176-pin HLFQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 47.10 Operating Frequency

Item			Symbol	min	max	Unit
Operating frequency	CPU clock (CPUCLK)	*1	f	150	600	MHz
		*2		150	450	
		*3		150	300	
	System clock (ICLK)			150		
	Peripheral module clock (PCLKA)			150		
	Peripheral module clock (PCLKB)			75		
	Peripheral module clock (PCLKC)			150		
	Peripheral module clock (PCLKD)			75		
	Peripheral module clock (PCLKE)			18.75	75	
	Peripheral module clock (PCLKF)			7.5	60	
	Peripheral module clock (PCLKG)			7.5	60	
	Peripheral module clock (PCLKH)			60		
	High-speed serial clock (SERICLK)			120	150	
	ΔΣ interface clock output (DSCLK0, DSCLK1)			6.25	25	
	External bus clock output (CKIO)			18.75	75	
	External clock output for Ethernet PHY (CLKOUT25M)			25	50	

Note 1. For R7S910007CBG, R7S910107CBG, R7S910013CBG, R7S910113CBG, R7S910017CBG, R7S910117CBG, R7S910018CBG, R7S910118CBG, R7S910027CBG, R7S910127CBG, R7S910028CBG, and R7S910128CBG only.
Note 2. For R7S910001CFP, R7S910101CFP, R7S910002CBG, R7S910102CBG, R7S910006CBG, R7S910106CBG, R7S910011CBG, R7S910111CBG, R7S910015CBG, R7S910115CBG, R7S910016CBG, R7S910116CBG, R7S910025CBG, R7S910125CBG, R7S910026CBG, and R7S910126CBG only.
Note 3. For R7S910035CBG, R7S910135CBG, R7S910036CBG, and R7S910136CBG only.

47.4.1 Clock Timing

Table 47.11 CKIO Pin Output Timing

Output load condition: C = 30 pF

Item	Symbol	min	typ	max	Unit	Test Conditions
CKIO pin output cycle time	t_{CKcyc}	13.3	—	53.4	ns	Figure 47.2
CKIO pin output high level pulse width	t_{CKH}	$t_{CKcyc}/2 - t_{CKr}$	—	—	ns	
CKIO pin output low level pulse width	t_{CKL}	$t_{CKcyc}/2 - t_{CKf}$	—	—	ns	
CKIO pin output rising time 1	t_{CKr}	—	—	5	ns	CKIO: High drive output setting*1 V_{OH} = VCCQ33 – 0.5 V V_{OL1} = 0.4 V
CKIO pin output falling time 1	t_{CKf}	—	—	5	ns	
CKIO pin output rising time 2	t_{CKr}	—	—	9	ns	CKIO: Normal output setting V_{OH} = VCCQ33 – 0.5 V V_{OL1} = 0.4 V
CKIO pin output falling time 2	t_{CKf}	—	—	9	ns	
CKIO pin output rising time 3	t_{CKr}	—	—	2.5	ns	CKIO: High drive output setting*1 V_{OH} = 2.0 V V_{OL1} = 0.8 V
CKIO pin output falling time 3	t_{CKf}	—	—	2.5	ns	
CKIO pin output rising time 4	t_{CKr}	—	—	4.5	ns	CKIO: Normal output setting V_{OH} = 2.0 V V_{OL1} = 0.8 V
CKIO pin output falling time 4	t_{CKf}	—	—	4.5	ns	

Note 1. When connecting SDRAM, be sure to set the B0 bit in the drive capacity control register (DSCR) to 1 to be a high drive output.

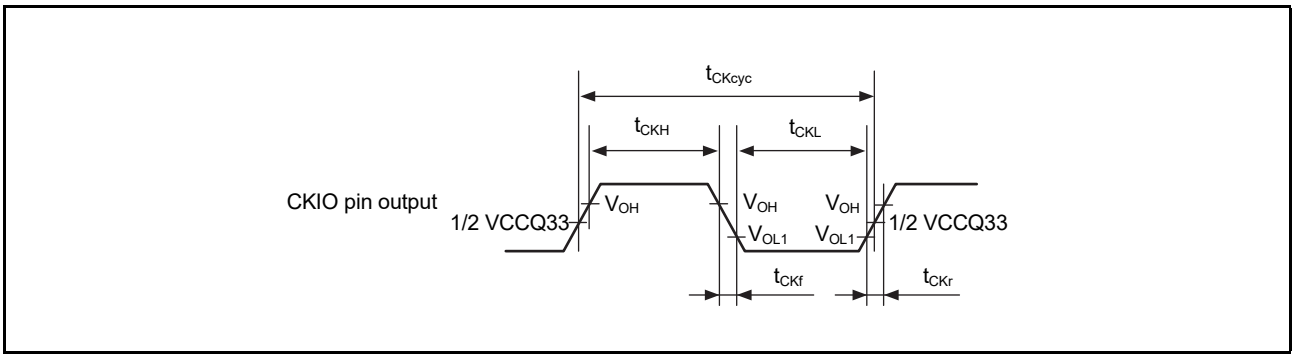


Figure 47.2 CKIO Pin Output Timing

Table 47.12 CLKOUT25Mn Timing

Output load conditions: V_{OH} = 2.0 V, V_{OL1} = 0.8 Vn, C = 25 pF (RMII)
V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V, C = 30 pF (MII)

Item		Symbol	min	max	Unit	Test Conditions
CLKOUT25Mn (RMII)	CLKOUT25Mn cycle time	T_{ck1}	20	—	ns	Figure 47.3
	CLKOUT25Mn frequency Typ. 50 MHz	—	50 ± 50 ppm		MHz	
	CLKOUT25Mn duty	—	35	65	%	
	CLKOUT25Mn output low pulse width 1	T_{ckl1}	$T_{ck1}/2 - T_{ckf1}$	$T_{ck1}/2 + T_{ckf1}$	ns	
	CLKOUT25Mn output high pulse width 1	T_{ckh1}	$T_{ck1}/2 - T_{ckr1}$	$T_{ck1}/2 + T_{ckr1}$	ns	
	CLKOUT25Mn rising/falling time 1	$T_{ckr1/ckf1}$	0.5	4	ns	
CLKOUT25Mn (MII)	CLKOUT25Mn cycle time	T_{ck2}	40	—	ns	Figure 47.4
	CLKOUT25Mn frequency Typ. 25 MHz	—	25 ± 50 ppm		MHz	
	CLKOUT25Mn duty	—	35	65	%	
	CLKOUT25Mn output low pulse width 2	T_{ckl2}	$T_{ck2}/2 - T_{ckf2}$	$T_{ck2}/2 + T_{ckf2}$	ns	
	CLKOUT25Mn output high pulse width 2	T_{ckh2}	$T_{ck2}/2 - T_{ckr2}$	$T_{ck2}/2 + T_{ckr2}$	ns	
	CLKOUT25Mn rising/falling time 2	$T_{ckr2/ckf2}$	0.5	9	ns	

n = 0 to 2

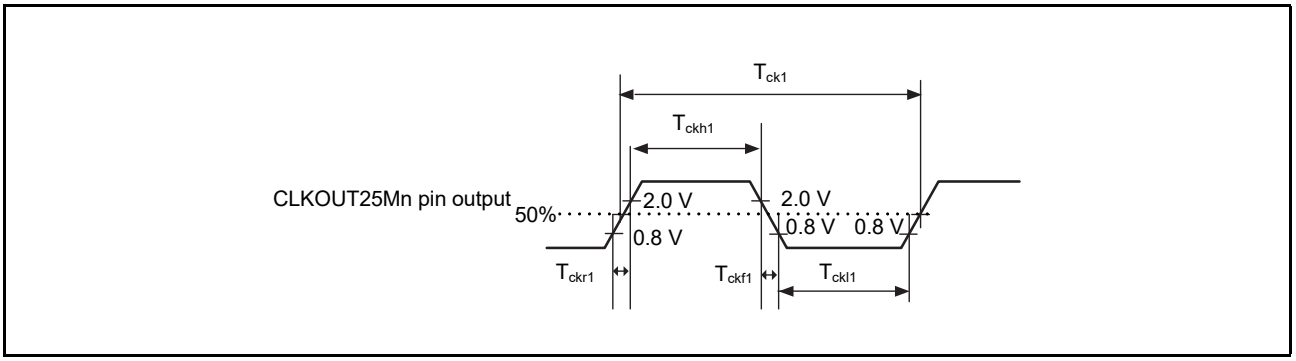


Figure 47.3 CLKOUT25Mn Pin Output Timing 1

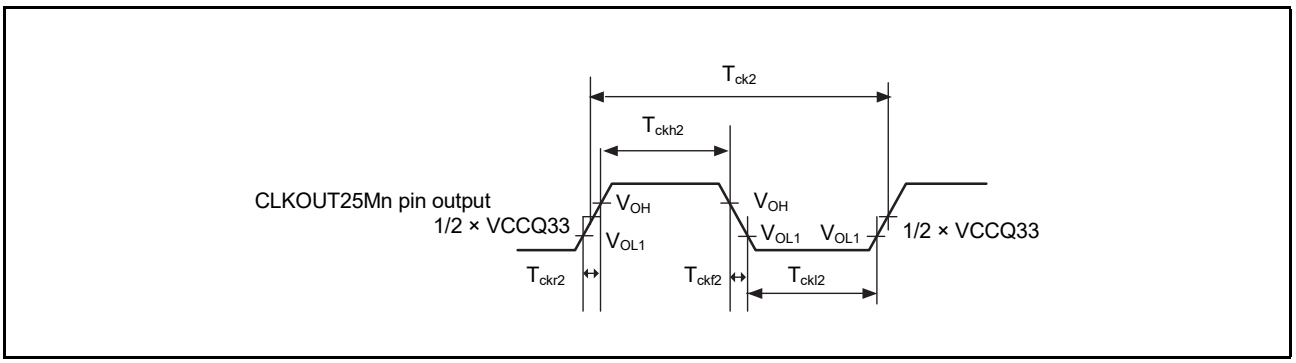


Figure 47.4 CLKOUT25Mn Pin Output Timing 2

Table 47.13 EXTAL Clock Timing

Item	Symbol	min	typ	max	Unit
EXTAL external clock input cycle time	t_{EXcyc}	40.00 ± 50 ppm			ns
		25.00 ± 25ppm*1			MHz

Note 1. When EtherCAT is in use.

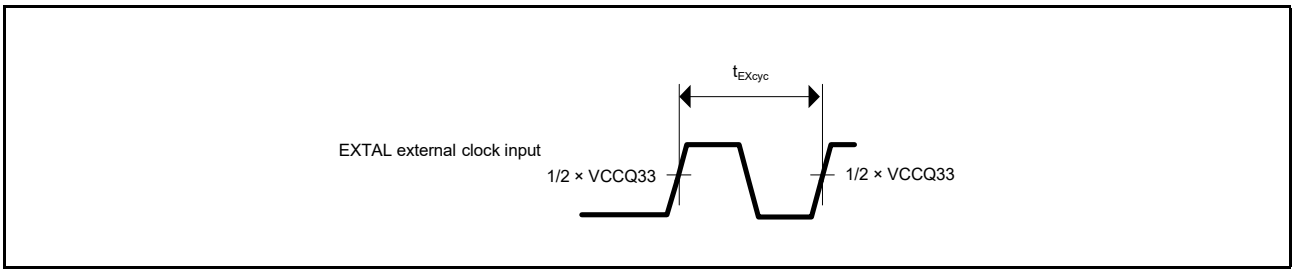


Figure 47.5 EXTAL External Clock Input Timing

Table 47.14 XTAL Clock Timing

Item	Symbol	min	typ	max	Unit
XTAL clock oscillator output cycle*1	$t_{XTALcyc}$		40.00 ± 50 ppm*2		ns

Note 1. When using the XTAL clock, ask the oscillator manufacturer to evaluate oscillation of the oscillator. For the oscillation stabilization time, see the evaluation result provided by the oscillator manufacturer.
Note 2. When using the EtherCAT, make sure that the clock timing satisfies 25.00 MHz ± 25 ppm.

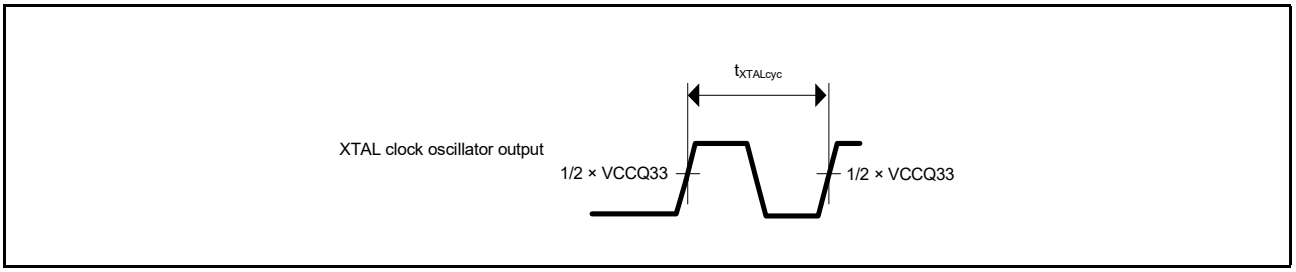


Figure 47.6 XTAL Clock Oscillator Output Timing

Table 47.15 LOCO Clock Timing

Item	Symbol	min	typ	max	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	4.62	4.17	3.79	µs	
LOCO clock oscillation frequency	f_{LOCO}	216	240	264	kHz	
LOCO clock oscillation stabilization wait time	t_{LOCOWT}	—	—	40	µs	Figure 47.7

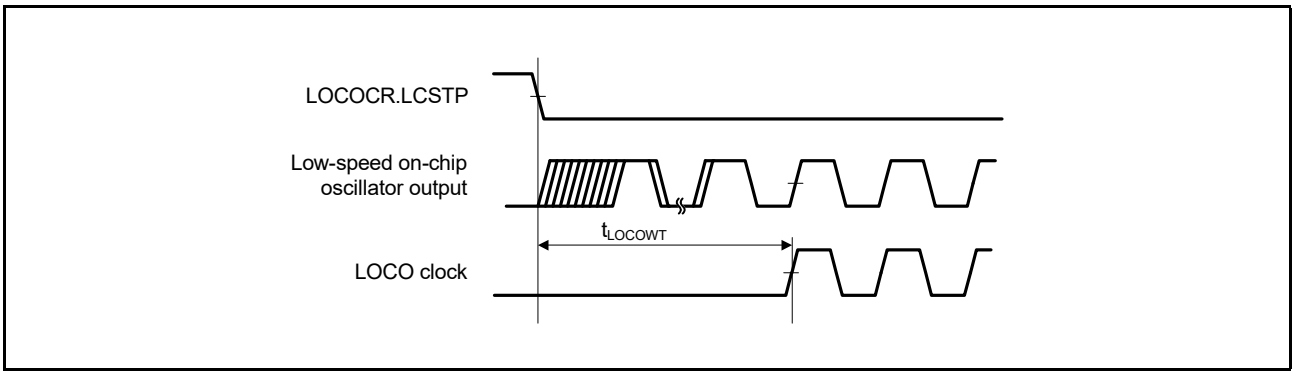


Figure 47.7 LOCO Clock Oscillation Start Timing

47.4.2 Reset Timing and Interrupt Timing

Table 47.16 Reset Timing and Interrupt Timing

Item		Symbol	Min*1	typ	max	Unit	Test Conditions
RES# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	Figure 47.8
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
RES# rising time		$T_{risereset}$	—	—	150	µs	
TRST# pulse width	At power on	$T_{dlyreset}$	10	—	—	ms	
	Other than above	$T_{dlyreset2}$	1	—	—	ms	
TRST# rising time		$T_{risereset}$	—	—	150	µs	
NMI pulse width		t_{NMIW}	t_{Icyc} × 2	—	—	ns	Figure 47.9
IRQ pulse width		t_{IRQW}	t_{Icyc} × 2	—	—	ns	Figure 47.10
ETH_INT pulse width		t_{EINTW}	t_{Icyc} × 2	—	—	ns	Figure 47.11

Note 1. t_{Icyc}: ICLK cycle

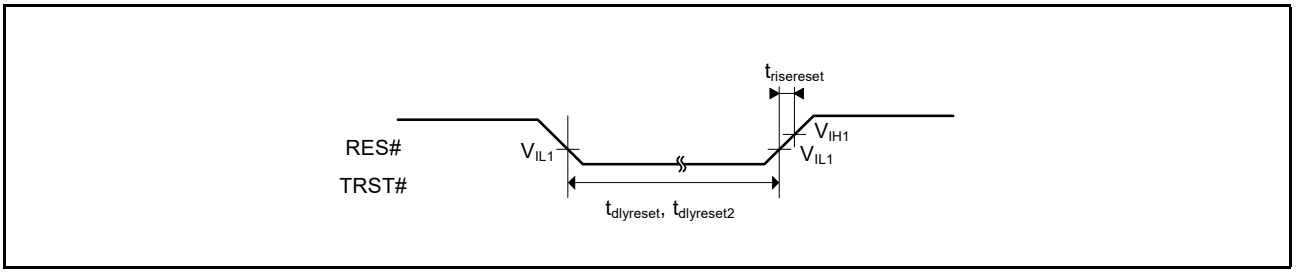


Figure 47.8 Reset Input Timing

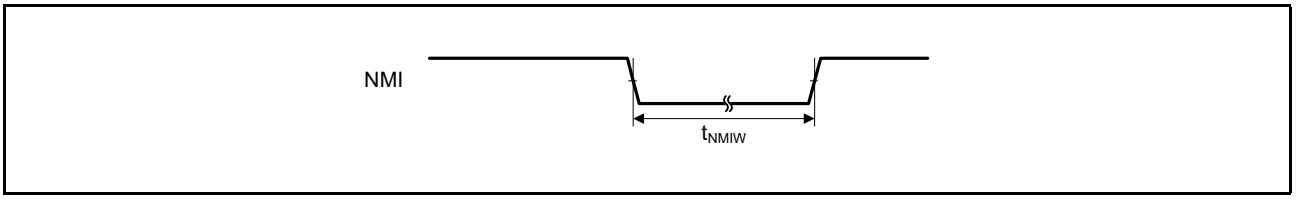


Figure 47.9 NMI Interrupt Input Timing

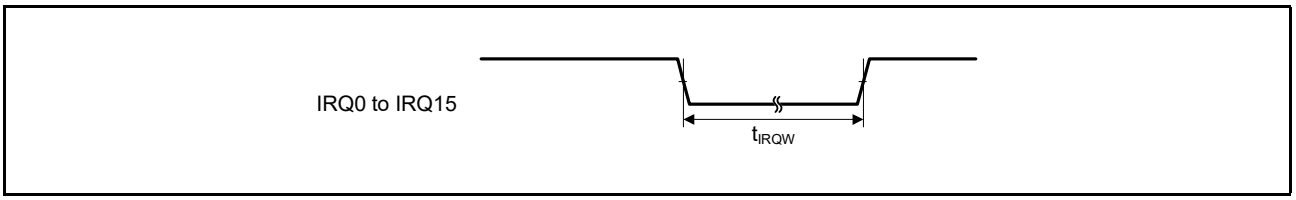


Figure 47.10 IRQ Interrupt Input Timing

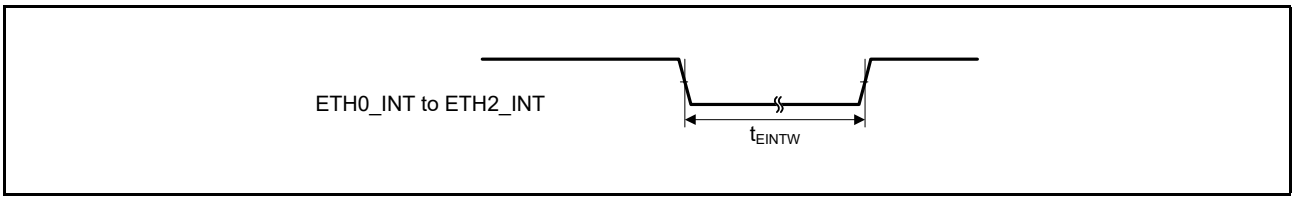


Figure 47.11 ETH_INT Interrupt Input Timing

47.4.3 Bus Timing

Table 47.17 Bus Timing (1 / 2)

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	CKIO = $1/t_{CKcyc}$*1 Min.	CKIO = $1/t_{CKcyc}$*1 Max.	Unit	Reference Figure
Address delay time 1	SDRAM*3	t_{AD1}	2	10	ns	Figure 47.12 to Figure 47.36
	Other than the above		0	10	ns	
Address delay time 2		t_{AD2}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 47.19
Address setup time		t_{AS}	0	—	ns	Figure 47.12 to Figure 47.15, Figure 47.19
Chip enable setup time		t_{cs}	0	—	ns	Figure 47.12 to Figure 47.15, Figure 47.19
Address hold time		t_{AH}	0	—	ns	Figure 47.12 to Figure 47.15
BS# delay time		t_{BSD}	—	10	ns	Figure 47.12 to Figure 47.33
CS# delay time 1	SDRAM*3	t_{CSD1}	2	10	ns	Figure 47.12 to Figure 47.36
	Other than the above		0	10	ns	
Read/write delay time 1	SDRAM*3	t_{RWD1}	2	10	ns	Figure 47.12 to Figure 47.36
	Other than the above		0	10	ns	
Read strobe delay time		t_{RSD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 47.12 to Figure 47.19
Read data setup time 1*4	High-drive output	t_{RDS1}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 47.12 to Figure 47.18
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data setup time 2*4	High-drive output	t_{RDS2}	6.6	—	ns	Figure 47.20 to Figure 47.23, Figure 47.28 to Figure 47.30
	Normal output		10	—	ns	
Read data setup time 3*4	High-drive output	t_{RDS3}	$1/2t_{CKcyc}$ + 4	—	ns	Figure 47.19
	Normal output		$1/2t_{CKcyc}$ + 7	—	ns	
Read data hold time 1		t_{RDH1}	0	—	ns	Figure 47.12 to Figure 47.18
Read data hold time 2		t_{RDH2}	2	—	ns	Figure 47.20 to Figure 47.23, Figure 47.28 to Figure 47.30
Read data hold time 3		t_{RDH3}	0	—	ns	Figure 47.19
Write enable delay time 1		t_{WED1}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 47.12 to Figure 47.17
Write enable delay time 2		t_{WED2}	—	10	ns	Figure 47.18
Write data delay time 1		t_{WDD1}	—	10	ns	Figure 47.12 to Figure 47.18
Write data delay time 2		t_{WDD2}	—	10	ns	Figure 47.24 to Figure 47.27, Figure 47.31 to Figure 47.33
Write data hold time 1		t_{WDH1}	1	—	ns	Figure 47.12 to Figure 47.18

Table 47.17 Bus Timing (2 / 2)

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

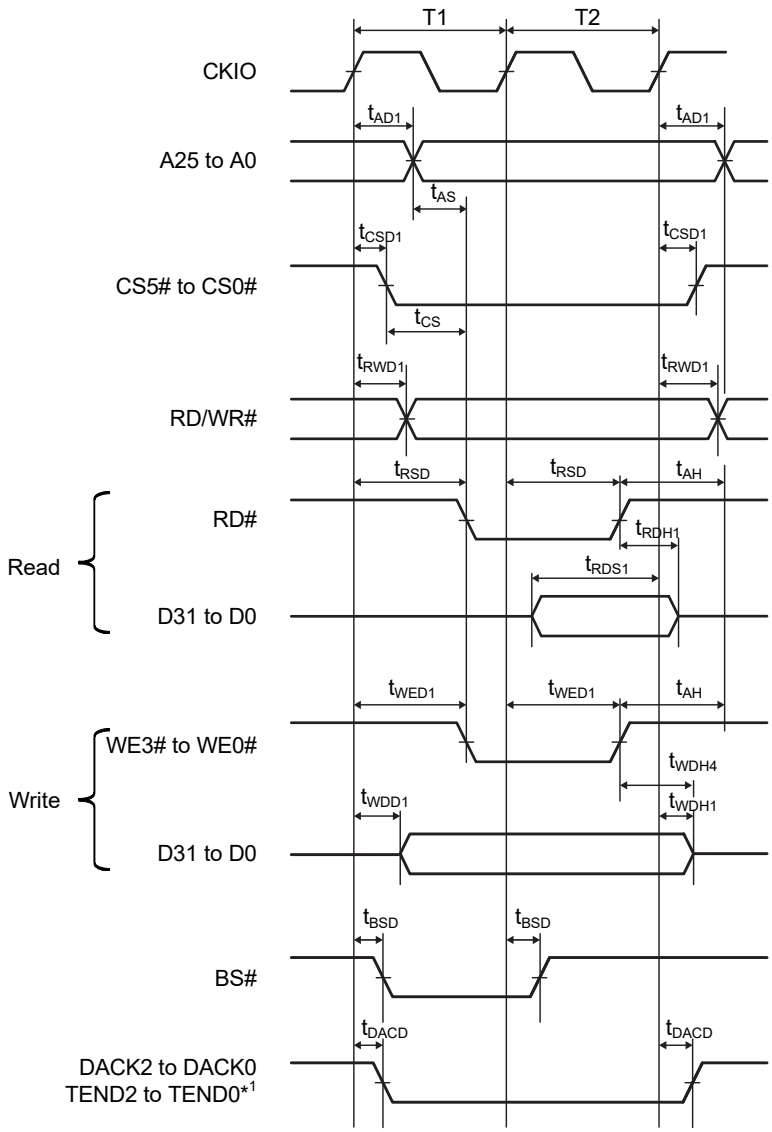
Item		Symbol	CKIO = $1/t_{CKcyc}$*1 Min.	CKIO = $1/t_{CKcyc}$*1 Max.	Unit	Reference Figure
Write data hold time 2		t_{WDH2}	2	—	ns	Figure 47.24 to Figure 47.27, Figure 47.31 to Figure 47.33
Write data hold time 4		t_{WDH4}	0	—	ns	Figure 47.12 to Figure 47.16
WAIT# setup time*4	High-drive output	t_{WTS}	$1/2t_{CKcyc}$ + 4.5	—	ns	Figure 47.13 to Figure 47.19
	Normal output		$1/2t_{CKcyc}$ + 8	—	ns	
WAIT# hold time		t_{WTH}	$1/2t_{CKcyc}$ + 3.5	—	ns	Figure 47.13 to Figure 47.19
RAS# delay time 1		t_{RASD1}	2	10	ns	Figure 47.20 to Figure 47.36
CAS# delay time 1		t_{CASD1}	2	10	ns	Figure 47.20 to Figure 47.36
DQM delay time 1		t_{DQMD1}	2	10	ns	Figure 47.20 to Figure 47.33
CKE delay time 1		t_{CKED1}	2	10	ns	Figure 47.35
AH# delay time		t_{AHD}	$1/2t_{CKcyc}$	$1/2t_{CKcyc}$ + 10	ns	Figure 47.16
Multiplex address delay time		t_{MAD}	—	10	ns	Figure 47.16
Multiplex address hold time		t_{MAH}	1	—	ns	Figure 47.16
Address setup time to AH#		t_{AVVH}	$1/2t_{CKcyc}$ – 2	—	ns	Figure 47.16
DACK/TEND delay time		t_{DACD}	See DMAC timing	See DMAC timing	ns	Figure 47.12 to Figure 47.33

Note 1. Take the number of cycles of waiting that suits the system configuration into consideration with regard to the fmax value for CKIO (the external bus clock). When CKIO is running at 50 MHz or a higher frequency, set the B0 bit of the driving ability control register (DSCR) to 1 to select high-drive output. When CKIO is running at less than 50 MHz, normal output of CKIO can be used (DSCR.B0 bit = 0).

Note 2. Notation of $1/2t_{CKcyc}$ in the delay time, setup time, and hold time shows 1/2 cycles from the clock rising edge, that is, the reference of clock falling.

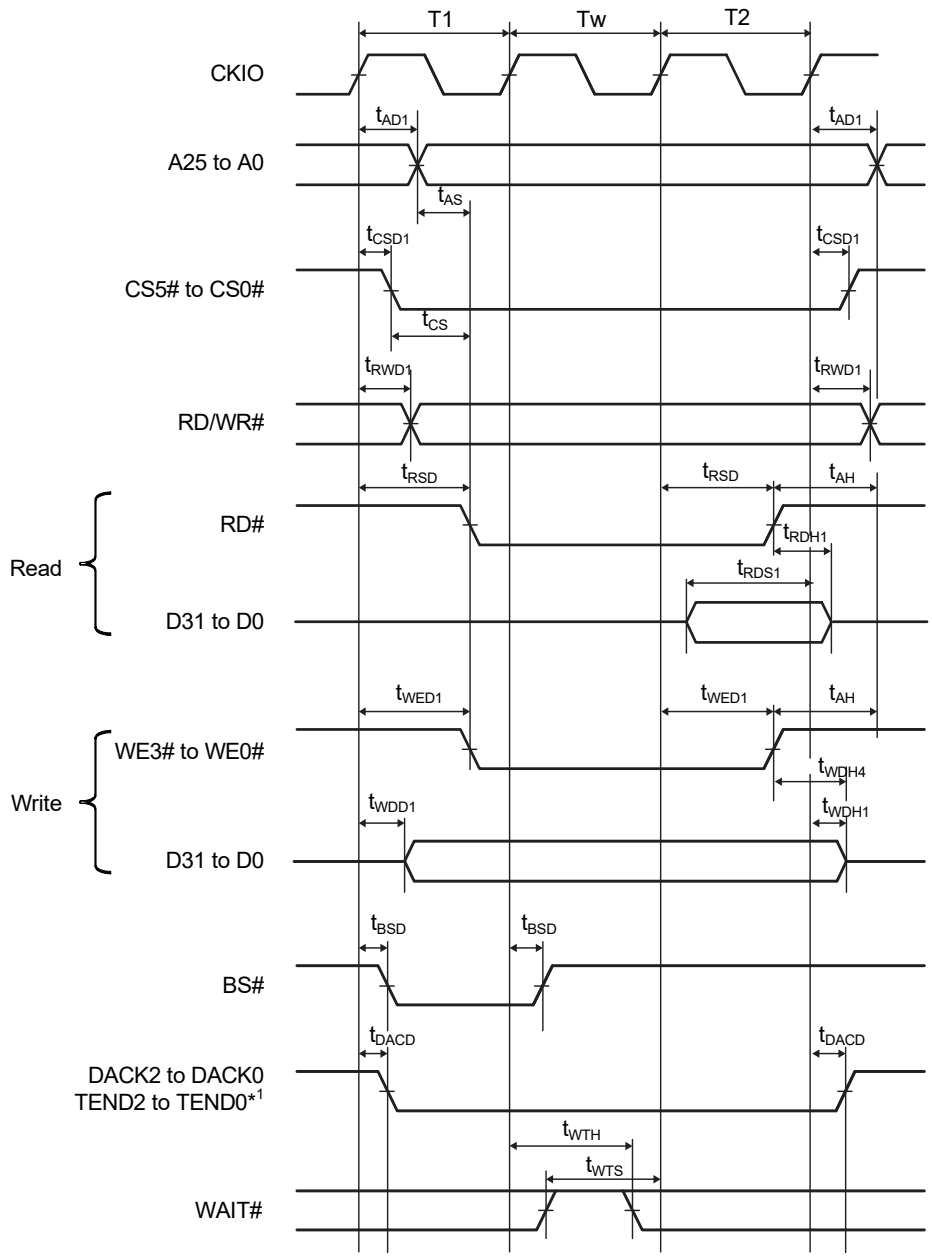
Note 3. These are values when SDRAM (TYPE[2:0] bits = 100b) is selected in the CSn space bus control register (CSnBCR) and high-drive output (B0 bit = 1) is selected in the driving ability control register (DSCR) for CKIO.

Note 4. These are values when high-drive output (B0 bit = 1) and normal output (B0 bit = 0) are respectively selected in the driving ability control register (DSCR) for CKIO.



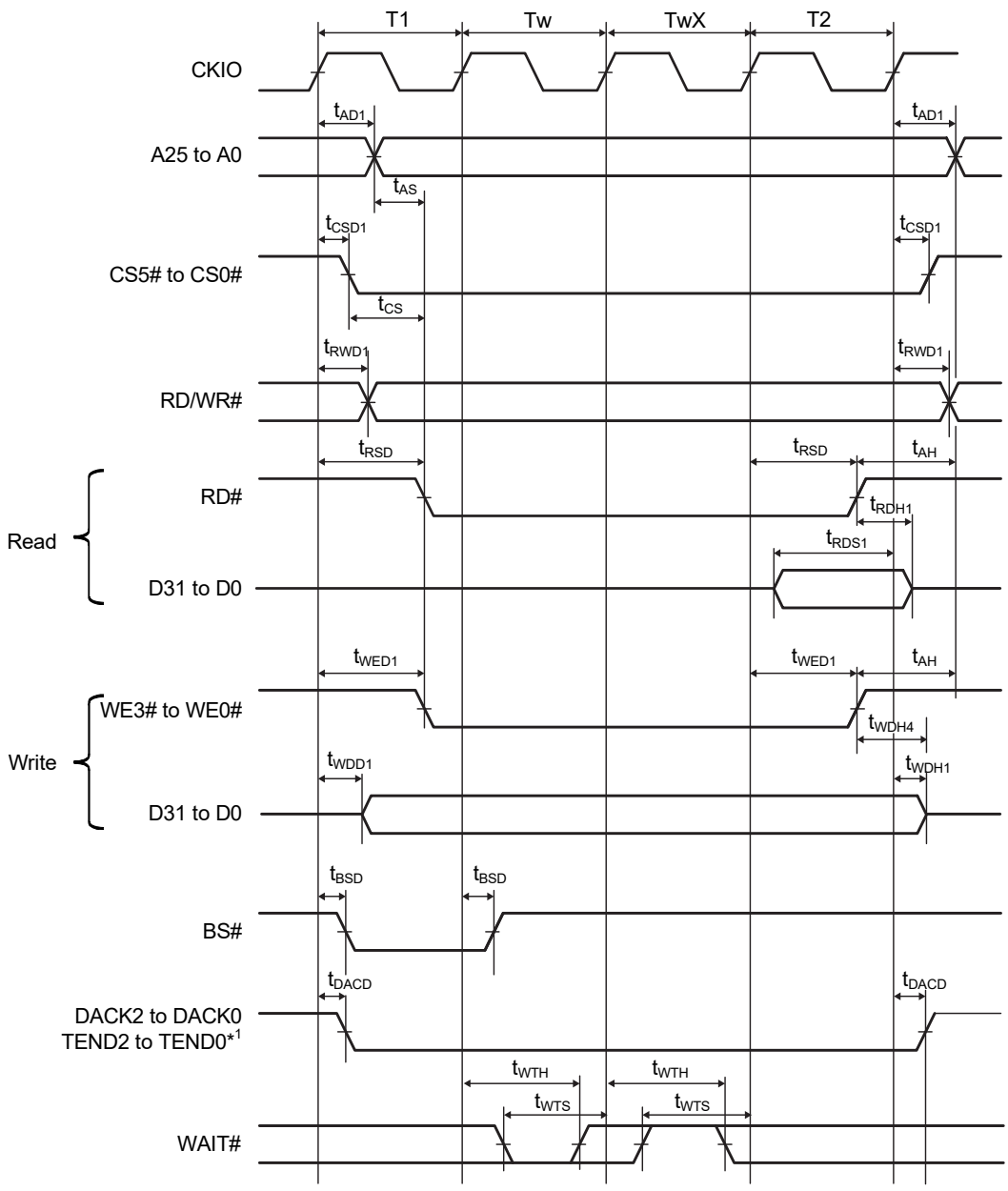
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.12 SRAM Interface Basic Bus Cycle (No Wait)



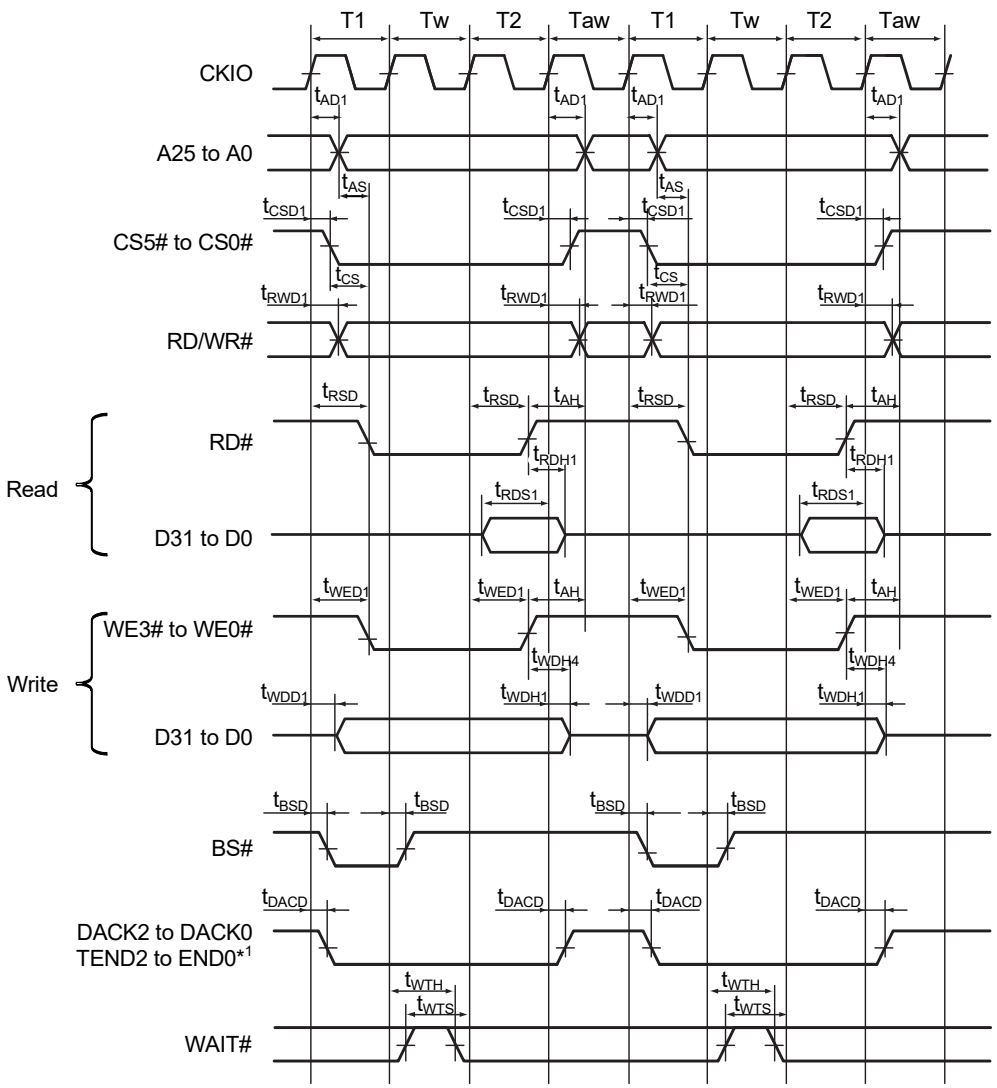
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.13 SRAM Interface Basic Bus Cycle (Software Wait 1)



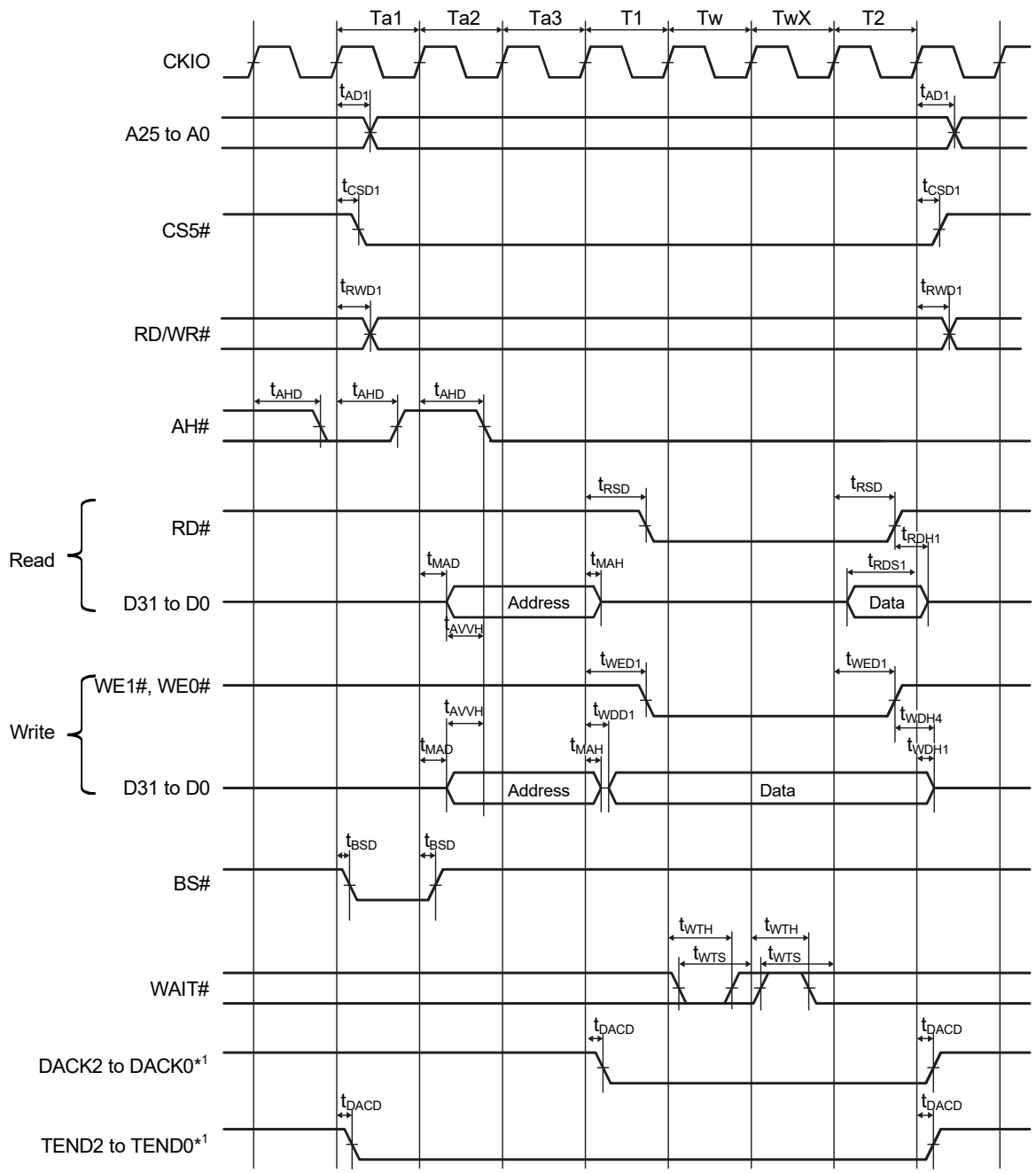
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.14 SRAM Interface Basic Bus Cycle (Software Wait 1, External Wait 1 Inserted)



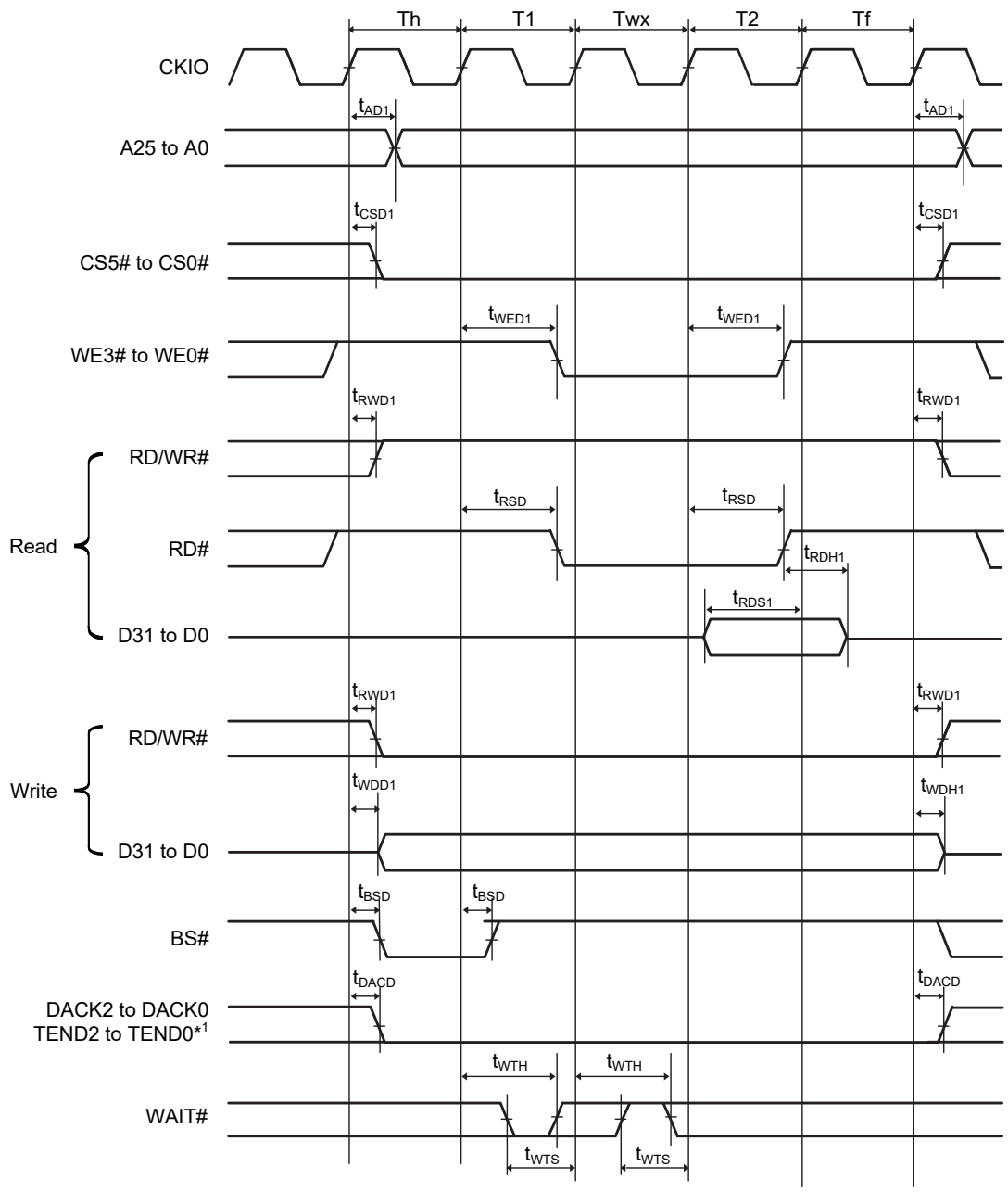
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.15 SRAM Interface Basic Bus Cycle (Software Wait 1, External wait Enabled (WM Bit = 0), No Idle Cycle)



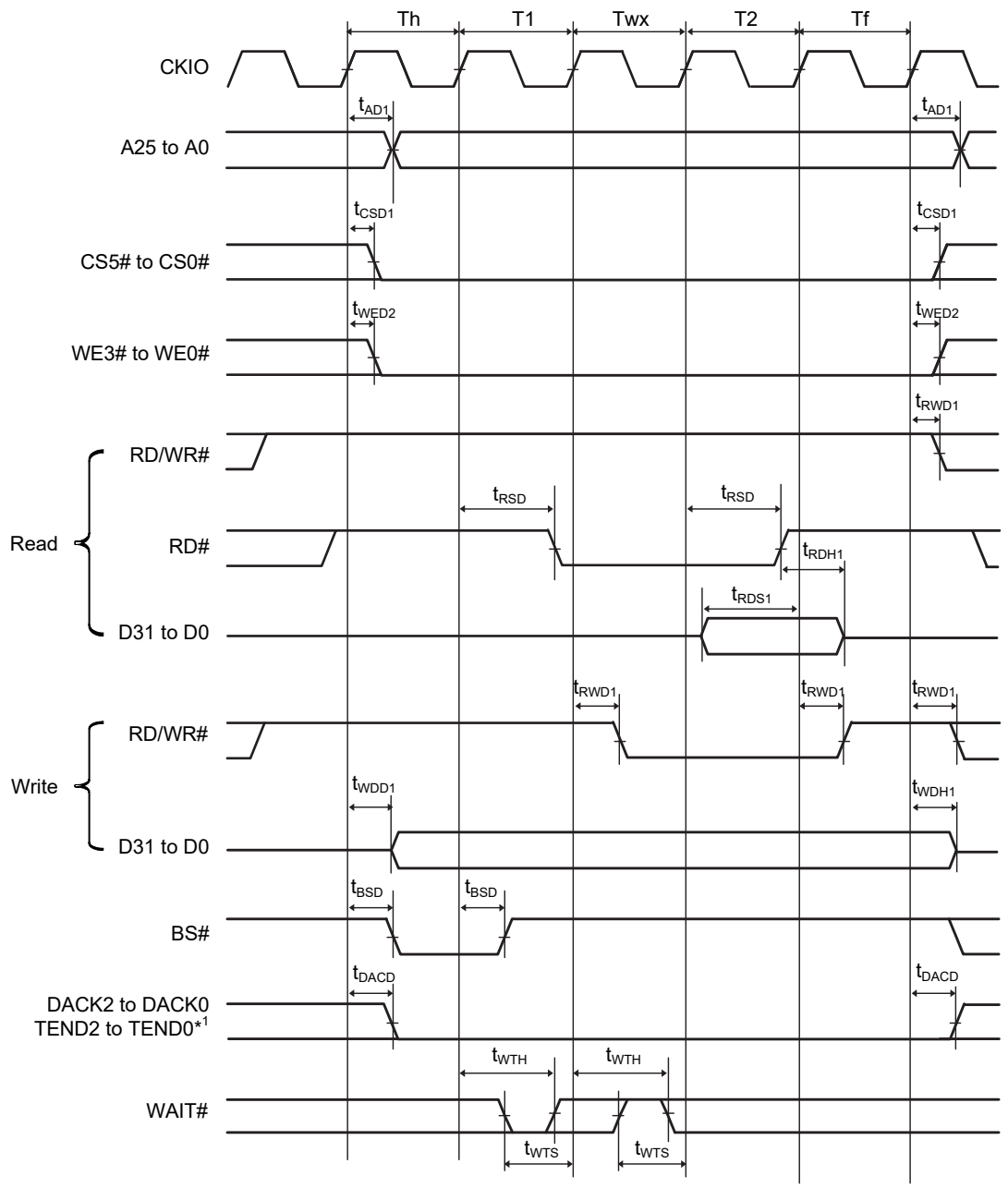
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.16 MPX-I/O Interface Bus Cycle (Address Cycle 3, Software Wait 1, External Wait 1 Inserted)



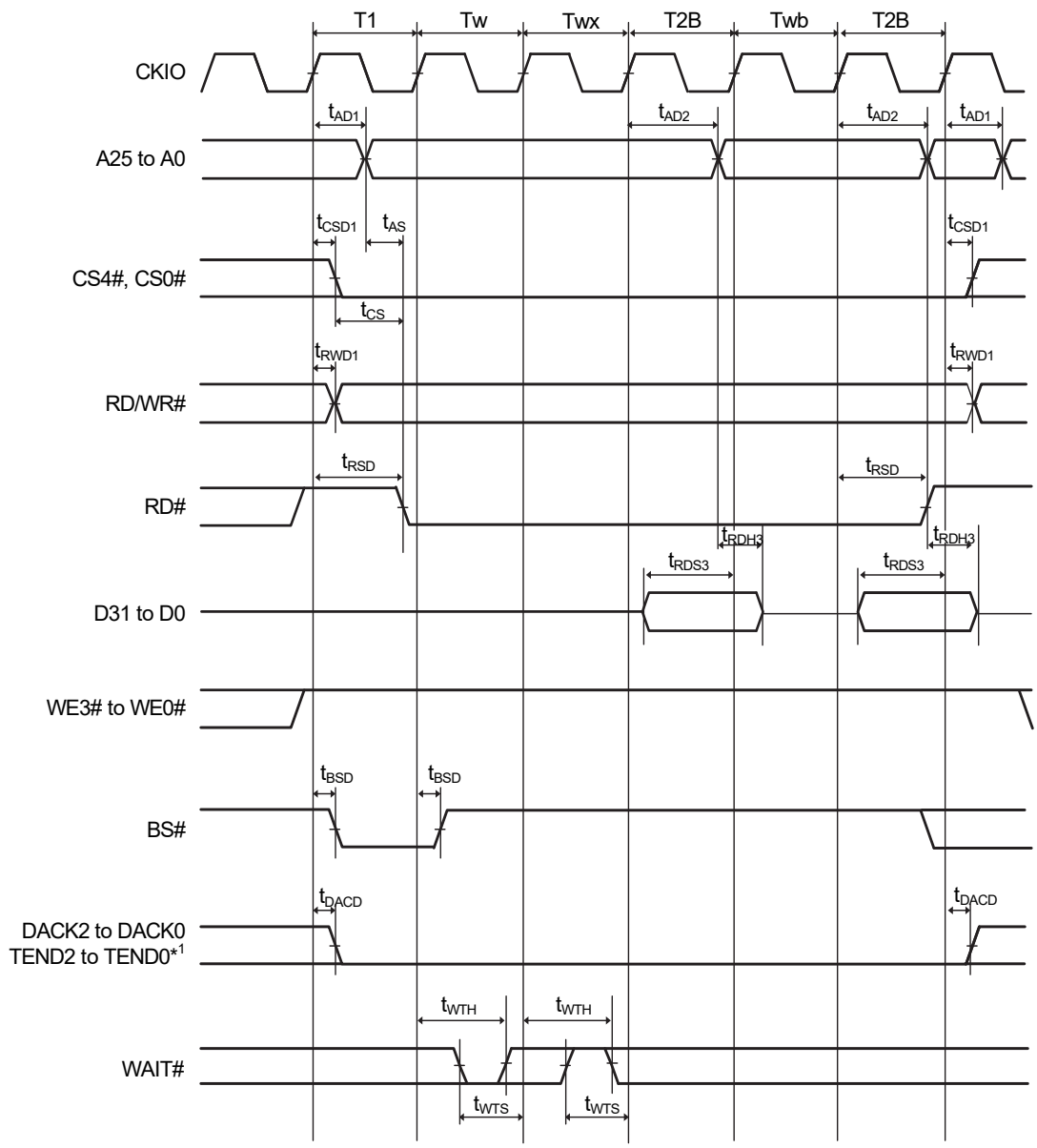
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.17 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Inserted, BAS = 0 (Write Cycle UB#/LB# Control))



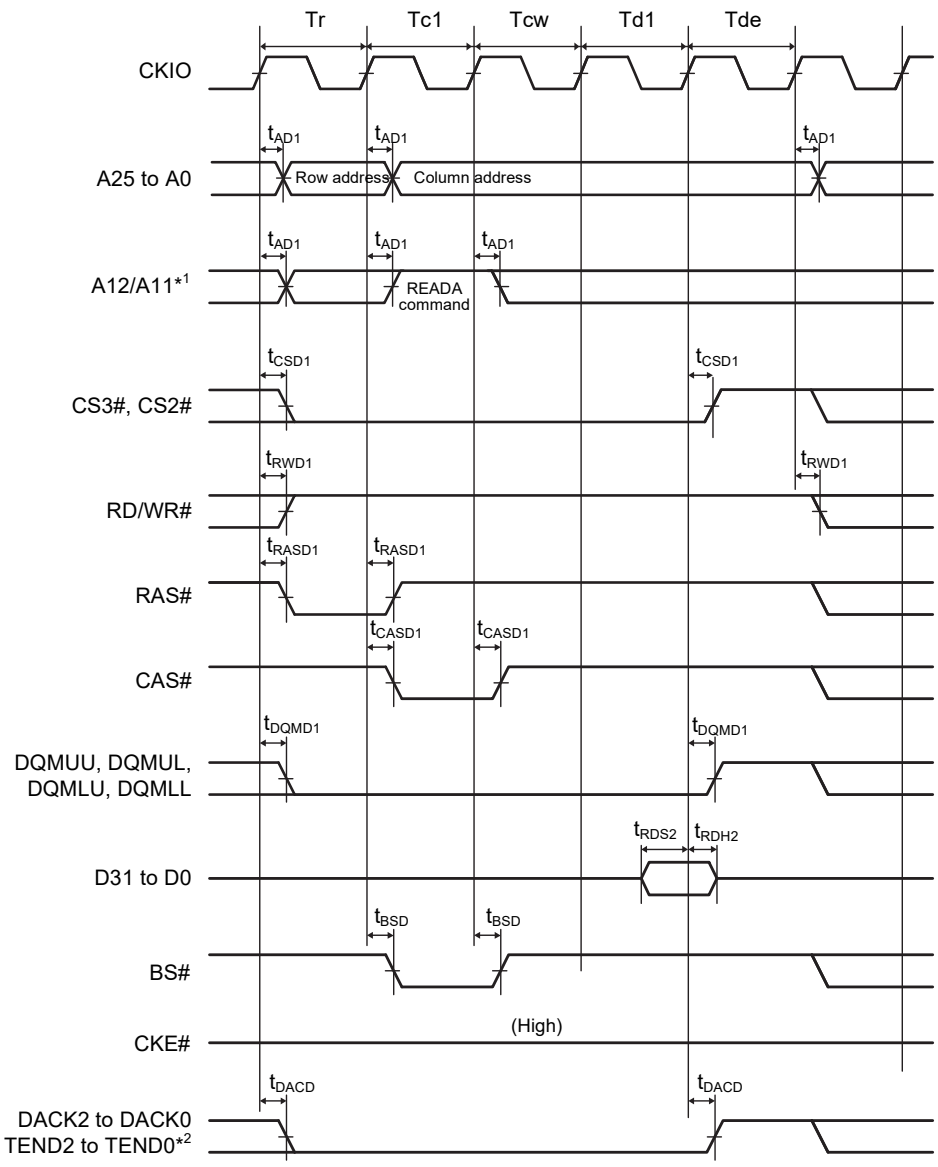
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.18 SRAM Bus Cycle with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, Asynchronous External Wait 1 Inserted, BAS = 1 (Write Cycle WE# Control))



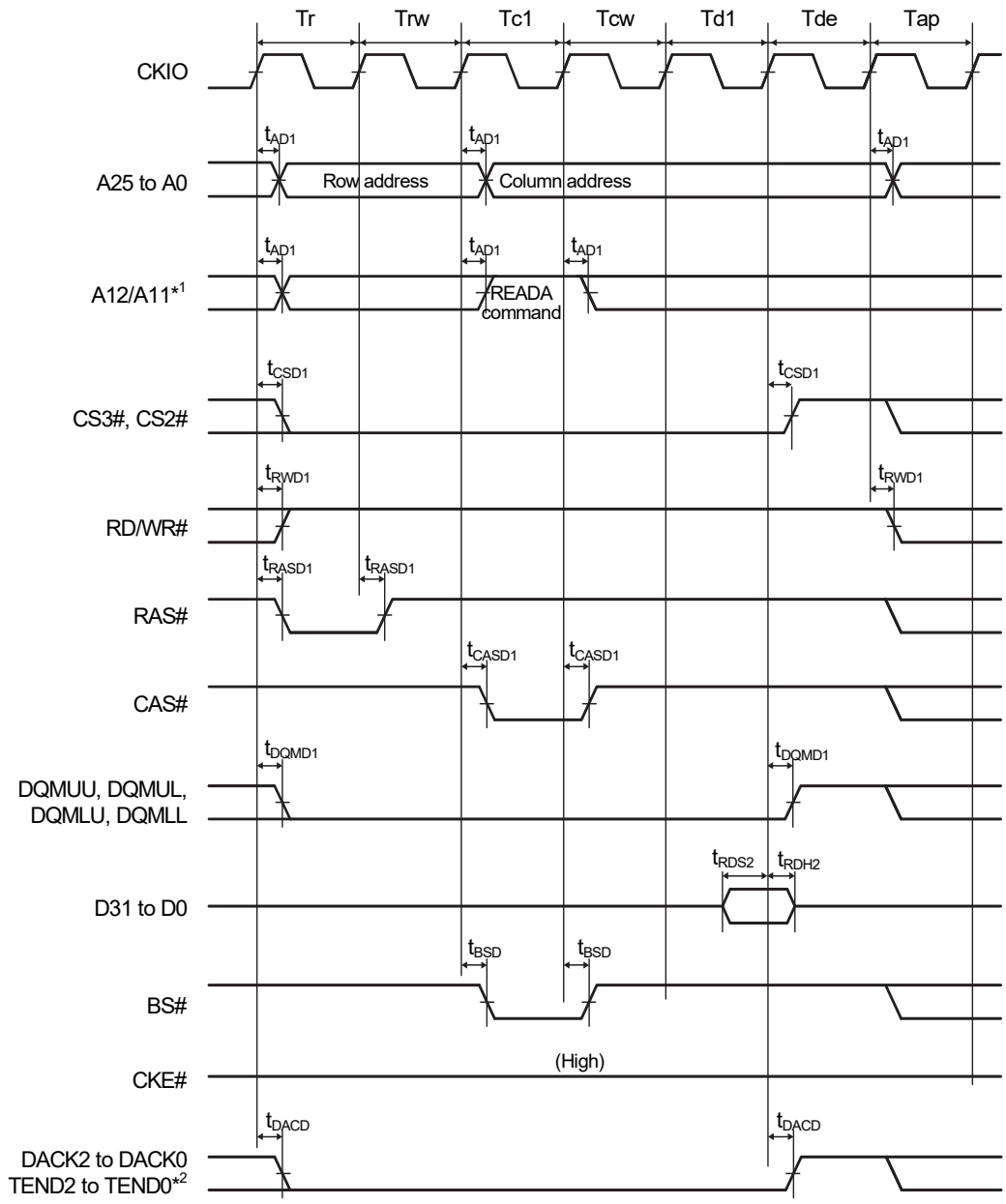
Note 1. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.19 Burst ROM Read Cycle (Software Wait 1, Asynchronous External Wait 1 Inserted, Burst Wait 1, 2)



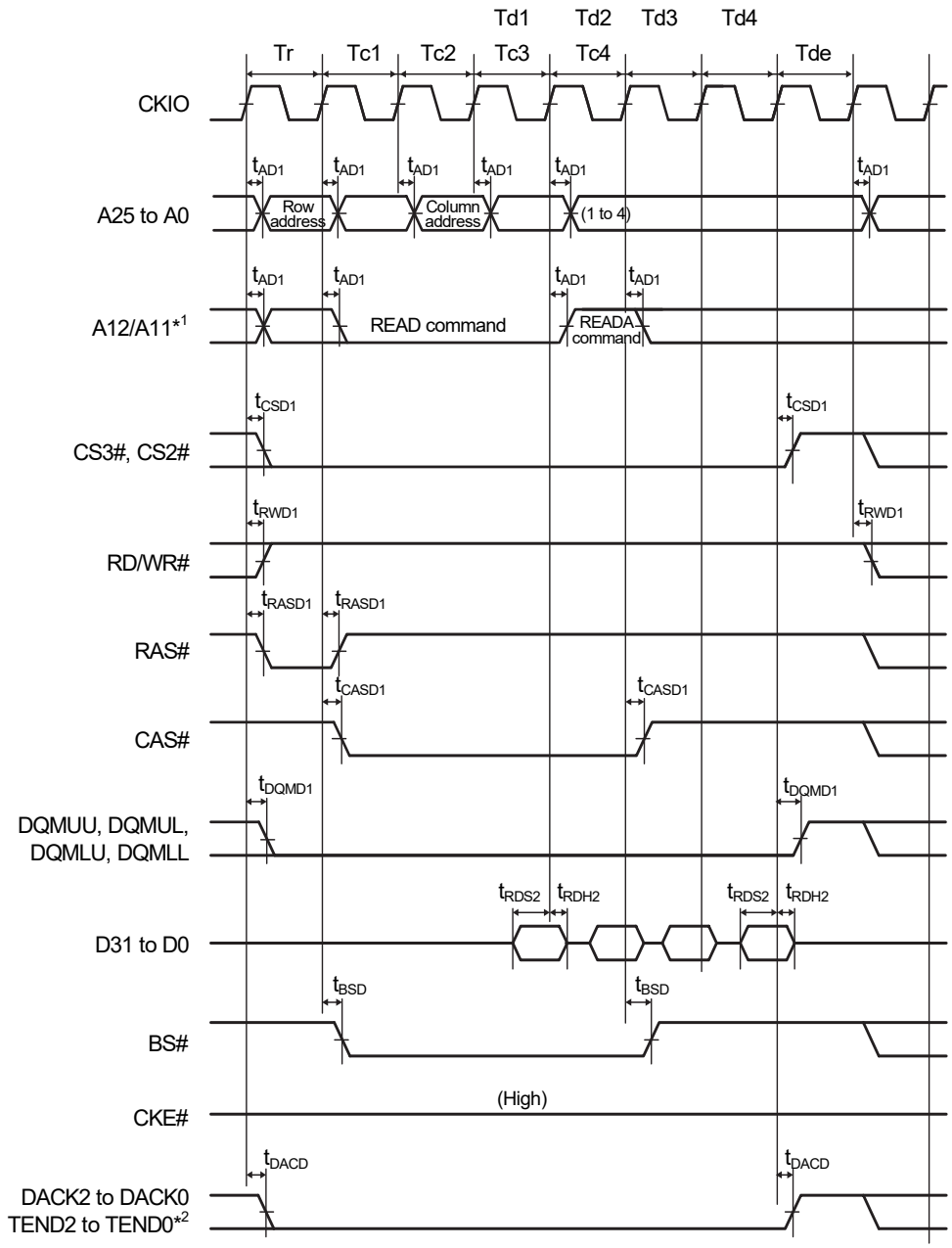
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.20 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 0 Cycles, WTRP = 0 Cycles)



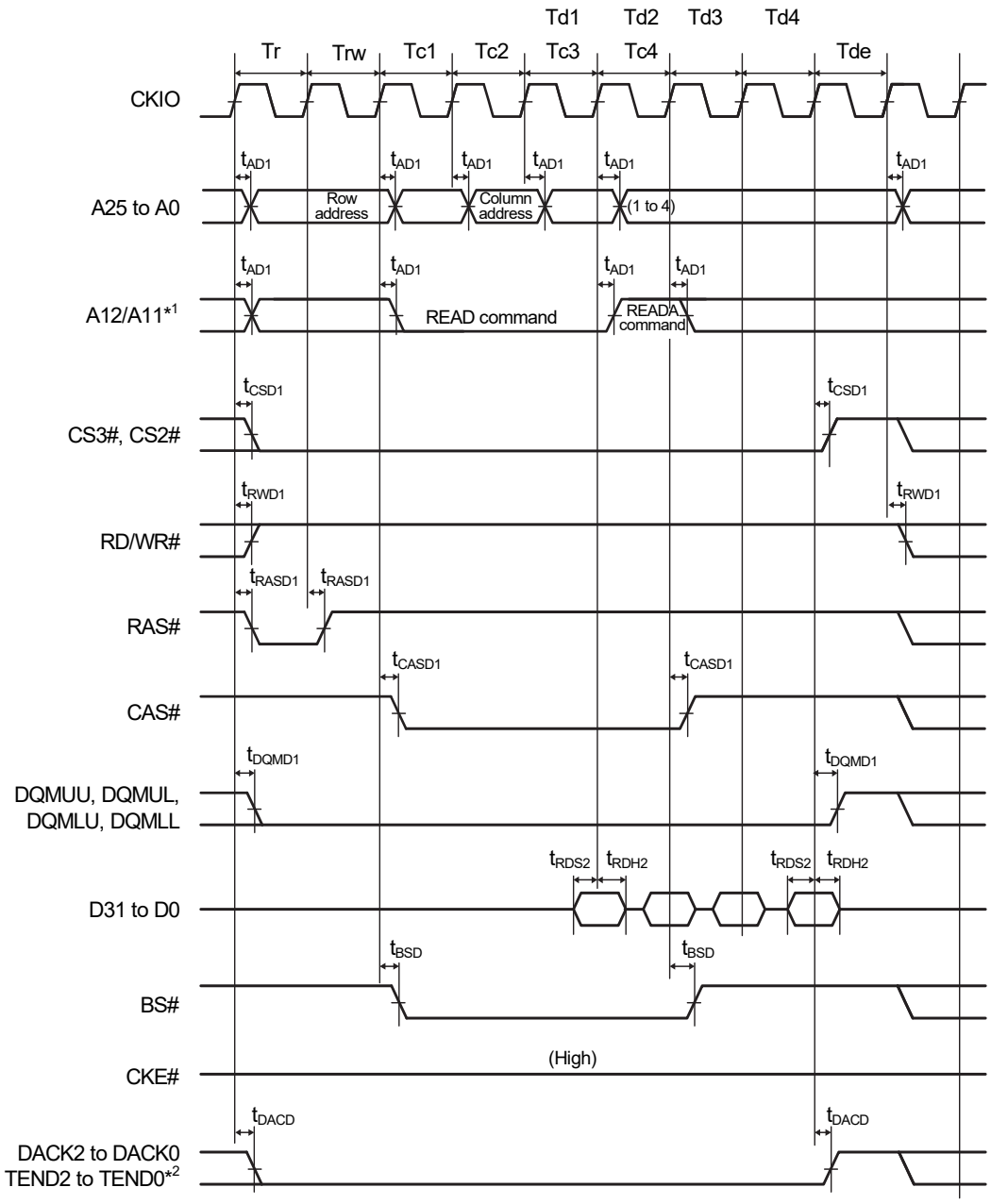
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.21 Synchronous DRAM Single-Read Bus Cycle (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



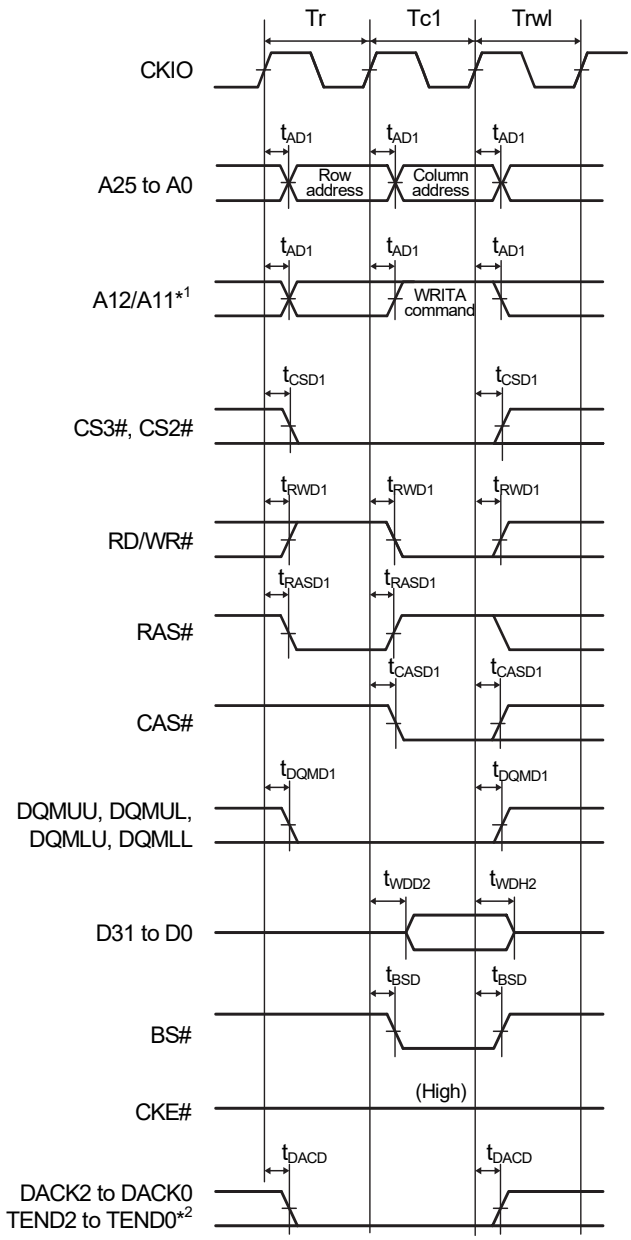
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.22 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (with Auto Precharge, CAS Latency 2, WTRCD = 0 Cycles, WTRP = 1 Cycle)



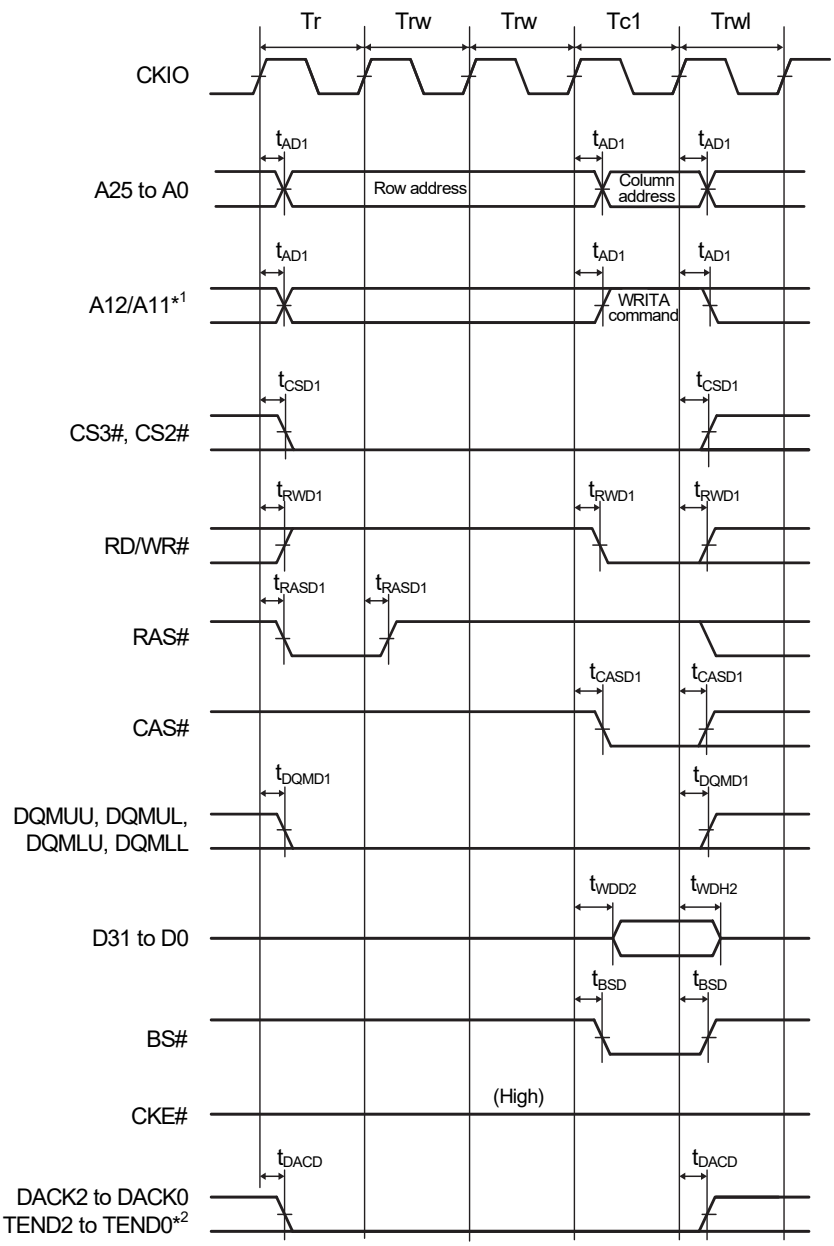
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.23 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (with Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 0 Cycles)



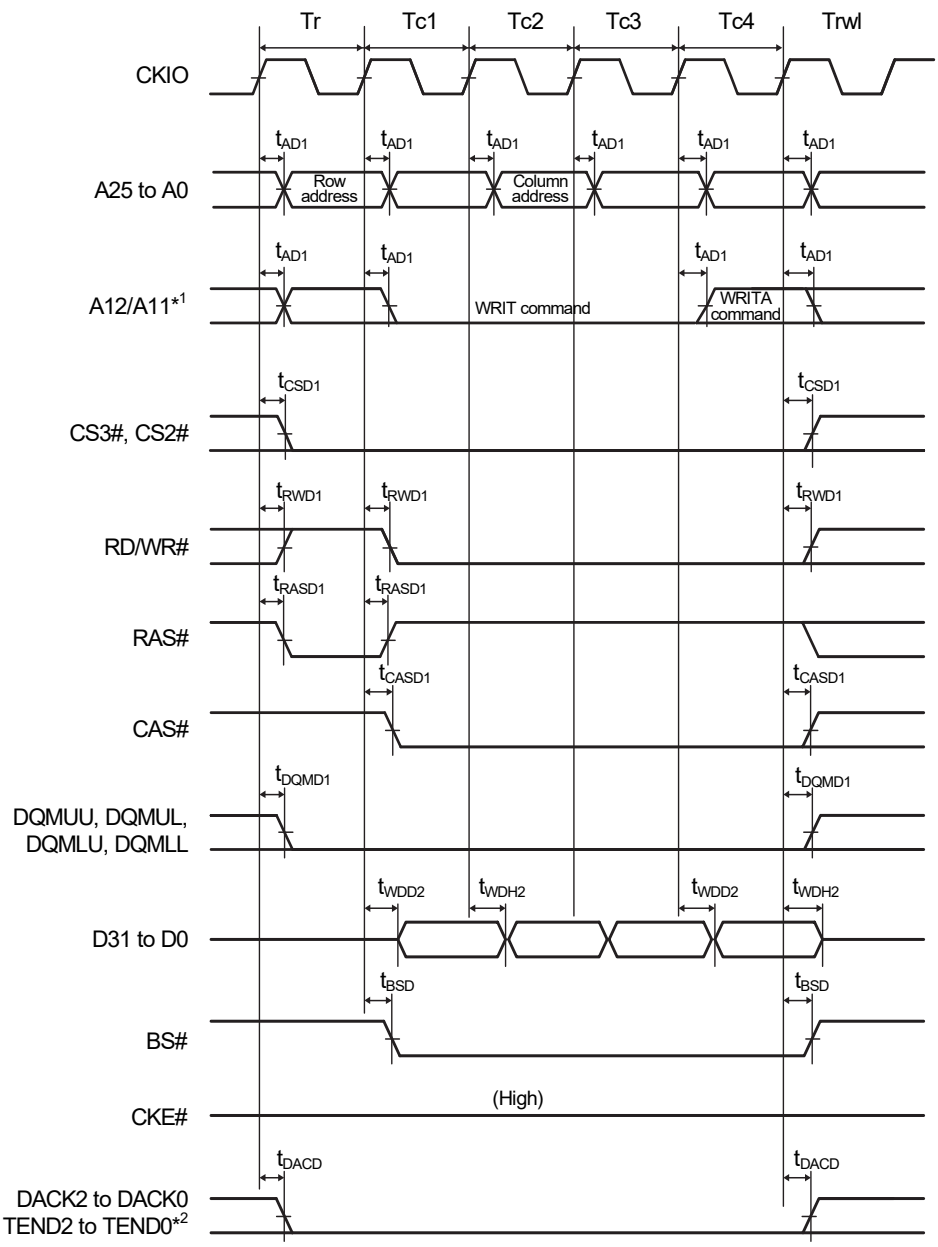
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.24 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, TRWL = 1 Cycle)



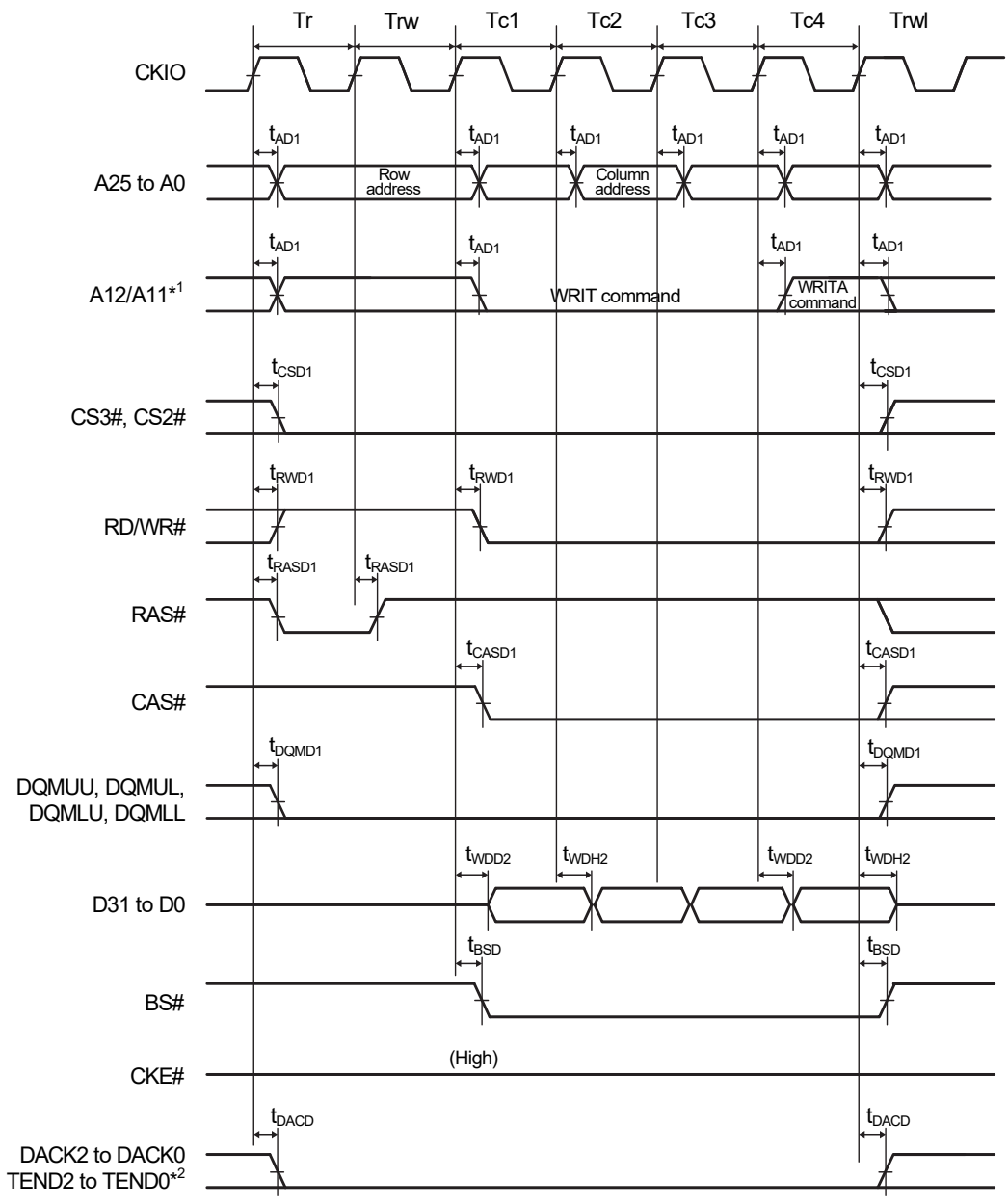
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.25 Synchronous DRAM Single-Write Bus Cycle (with Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)



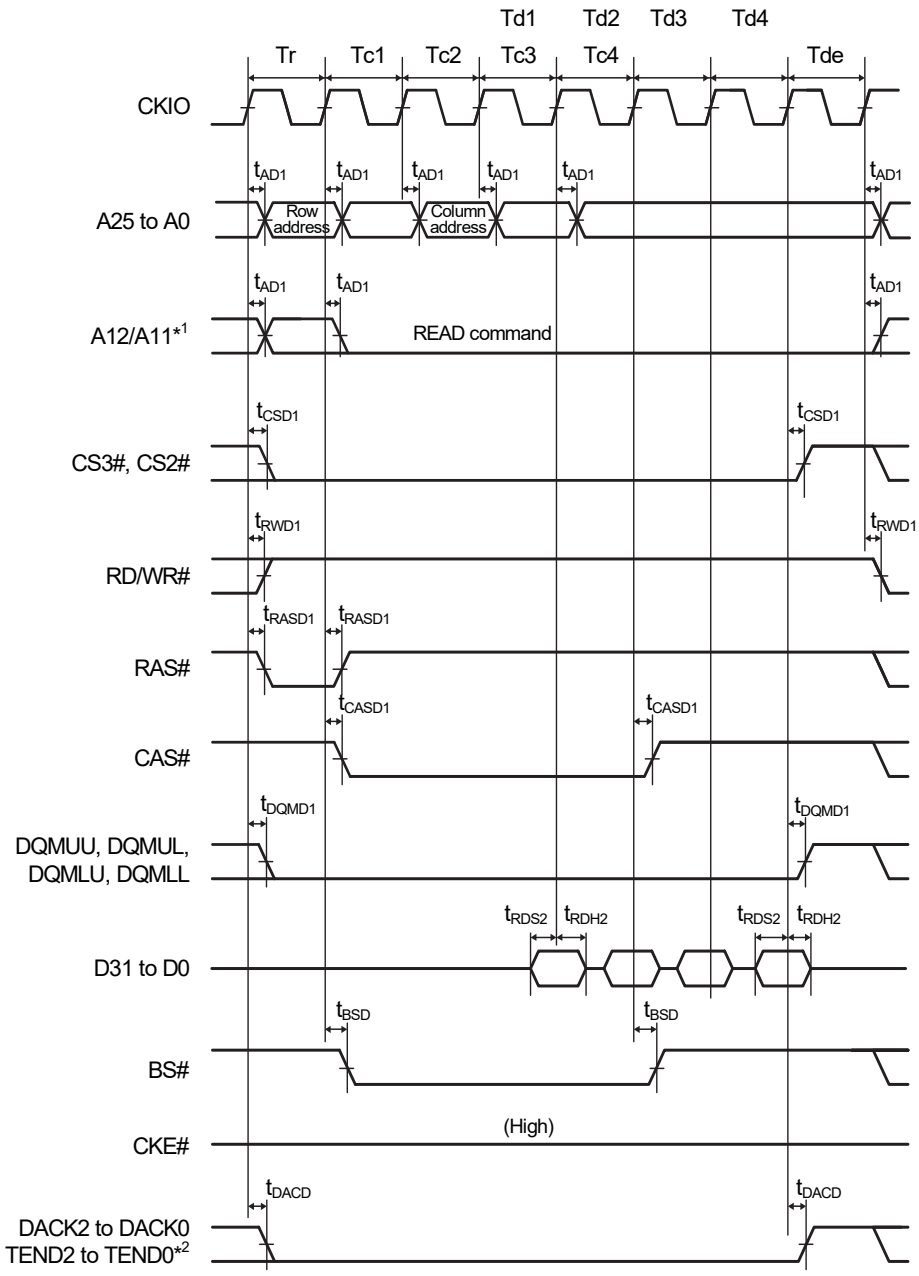
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.26 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (with Auto Precharge, WTRCD = 0 Cycles, TRWL = 1 Cycle)



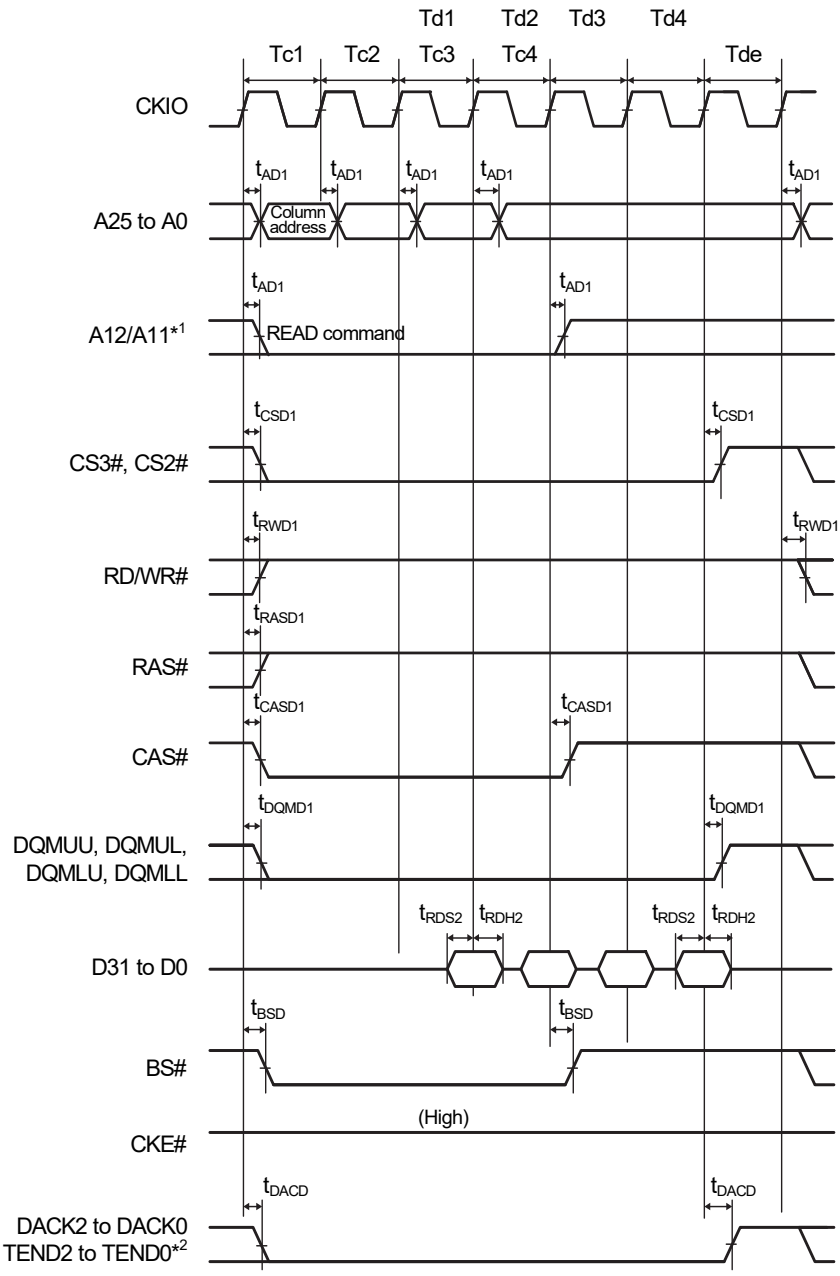
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.27 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (with Auto Precharge, WTRCD = 1 Cycle, TRWL = 1 Cycle)



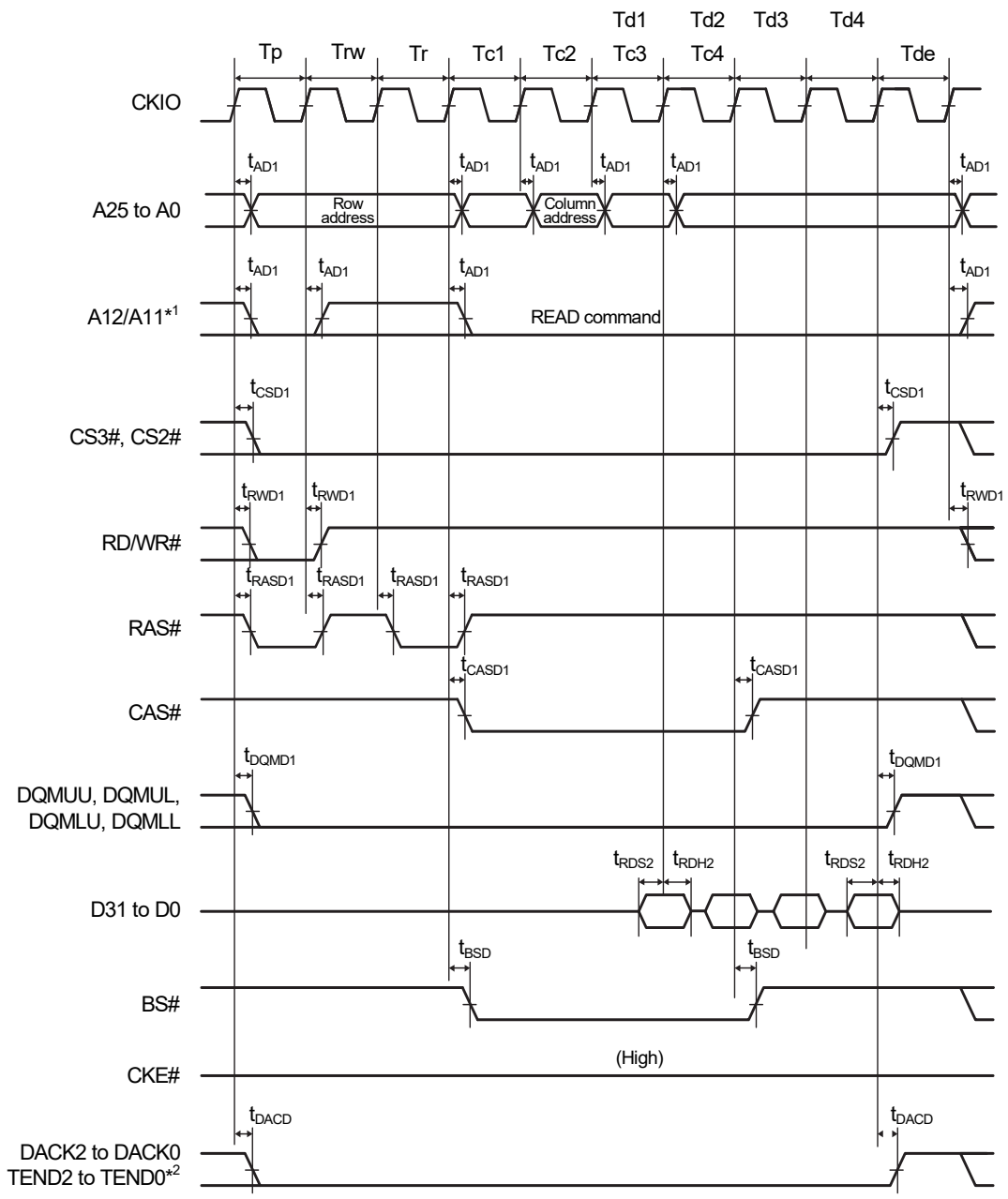
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.28 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: ACT + READ Command, CAS Latency 2, WTRCD = 0 Cycles)



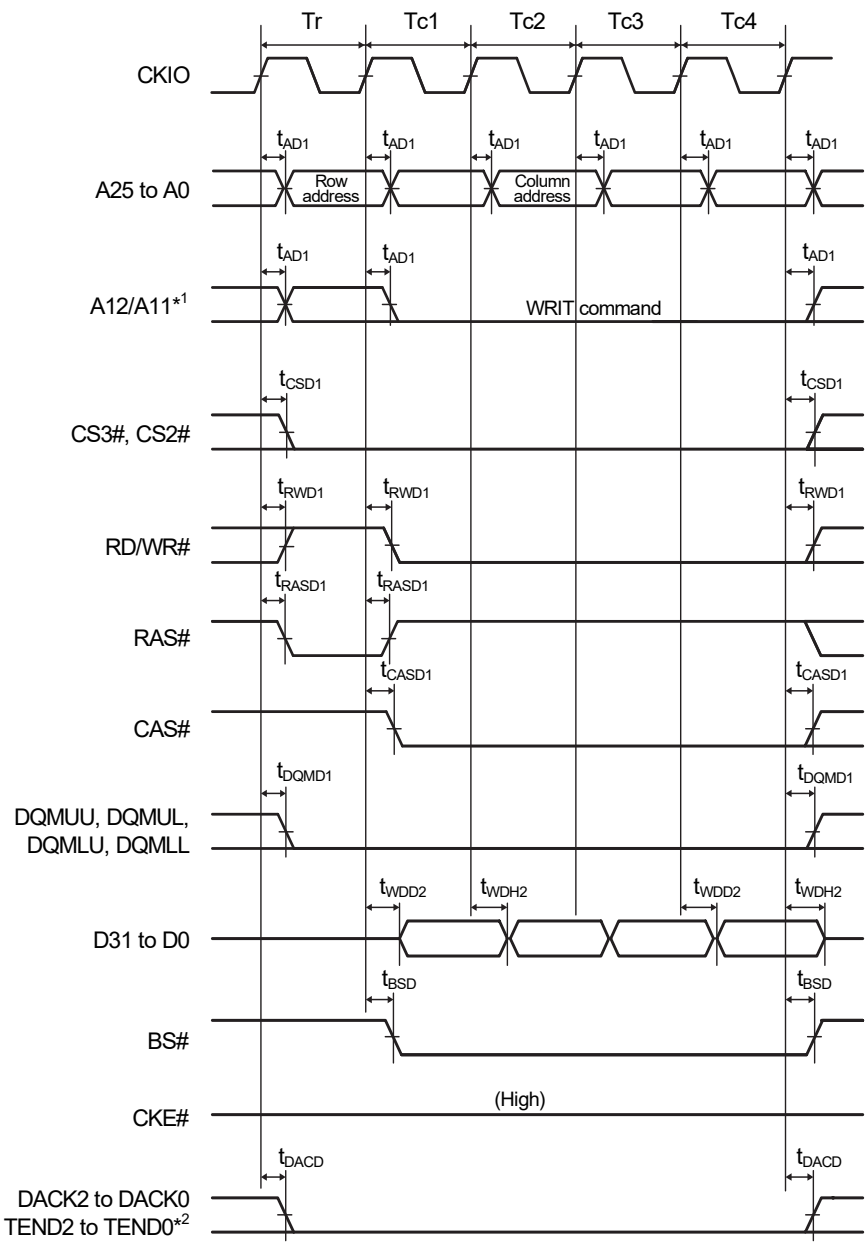
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.29 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycles)



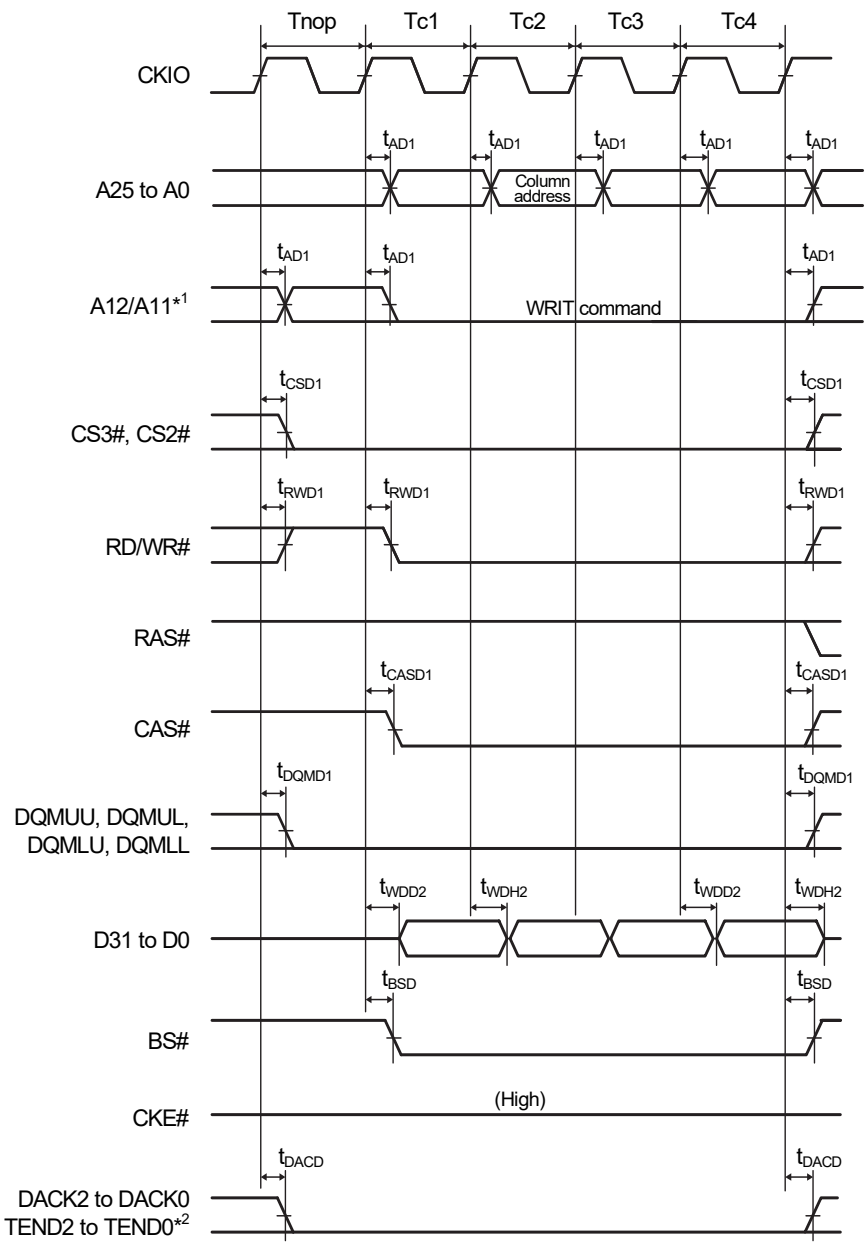
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.30 Synchronous DRAM Burst-Read Bus Cycle (Read for 4 Cycles) (Bank Active Mode: PRE + ACT + READ Command, Different Row Address, CAS Latency 2, WTRCD = 0 Cycles)



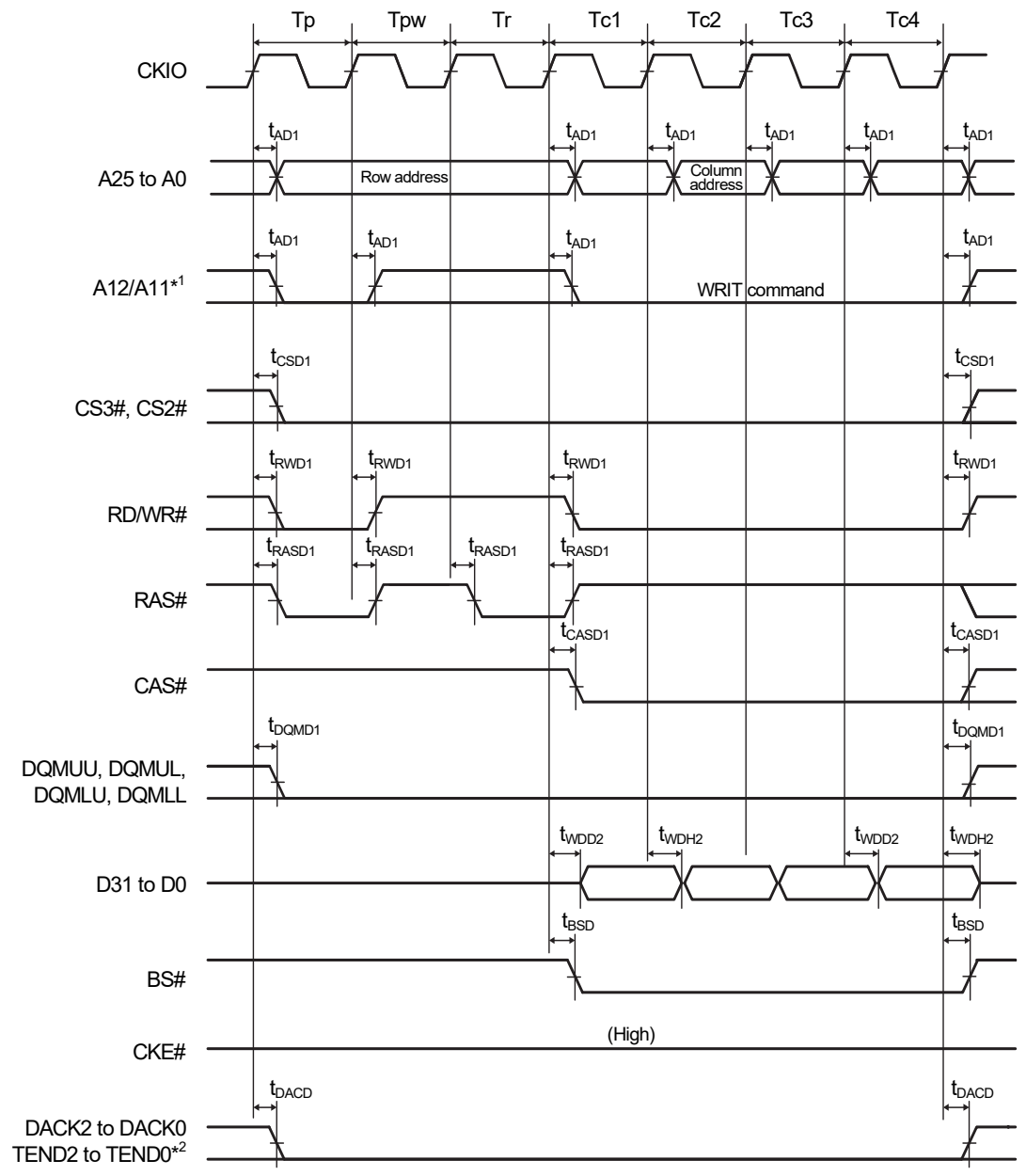
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.31 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (Bank Active Mode: ACT + WRITE Command, WTRCD = 0 Cycles, TRWL = 0 Cycles)



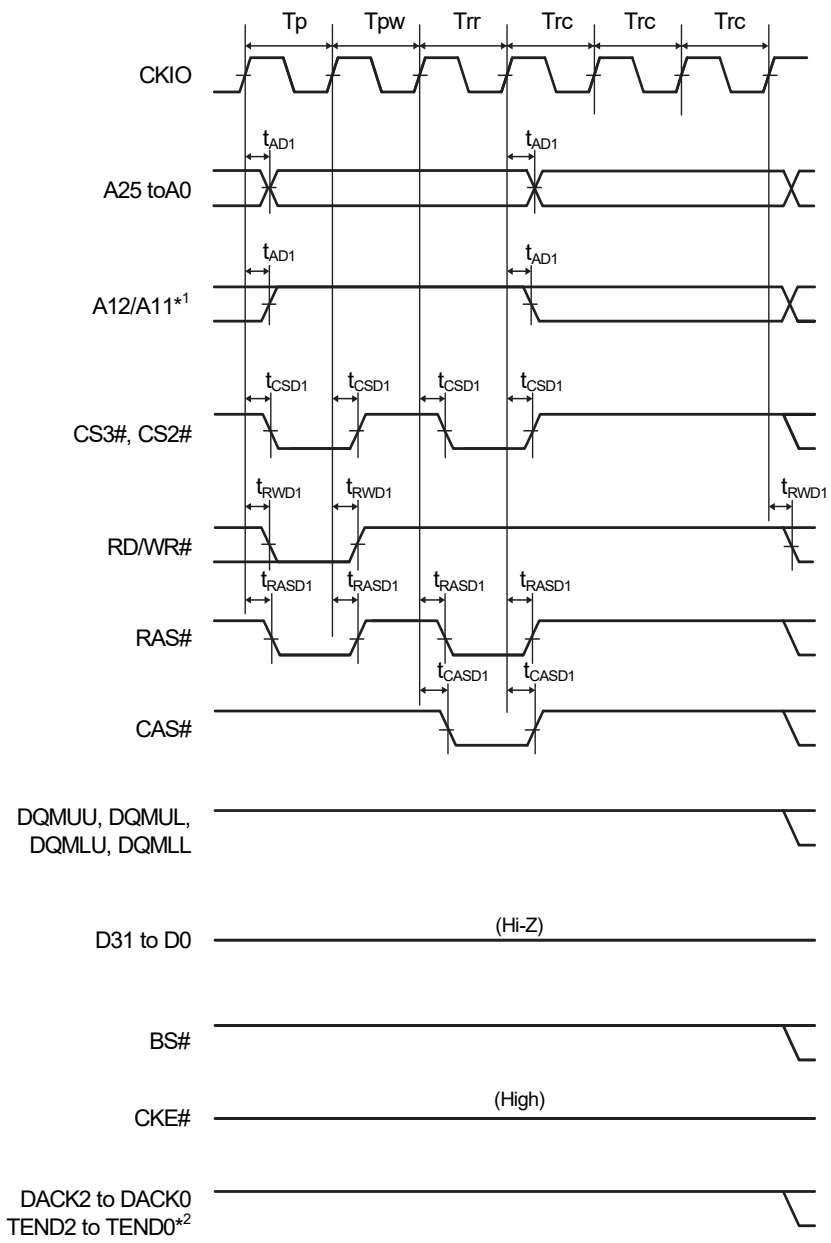
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.32 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (Bank Active Mode: WRITE Command, Same Row Address, WTRCD = 0 Cycles, TRWL = 0 Cycles)



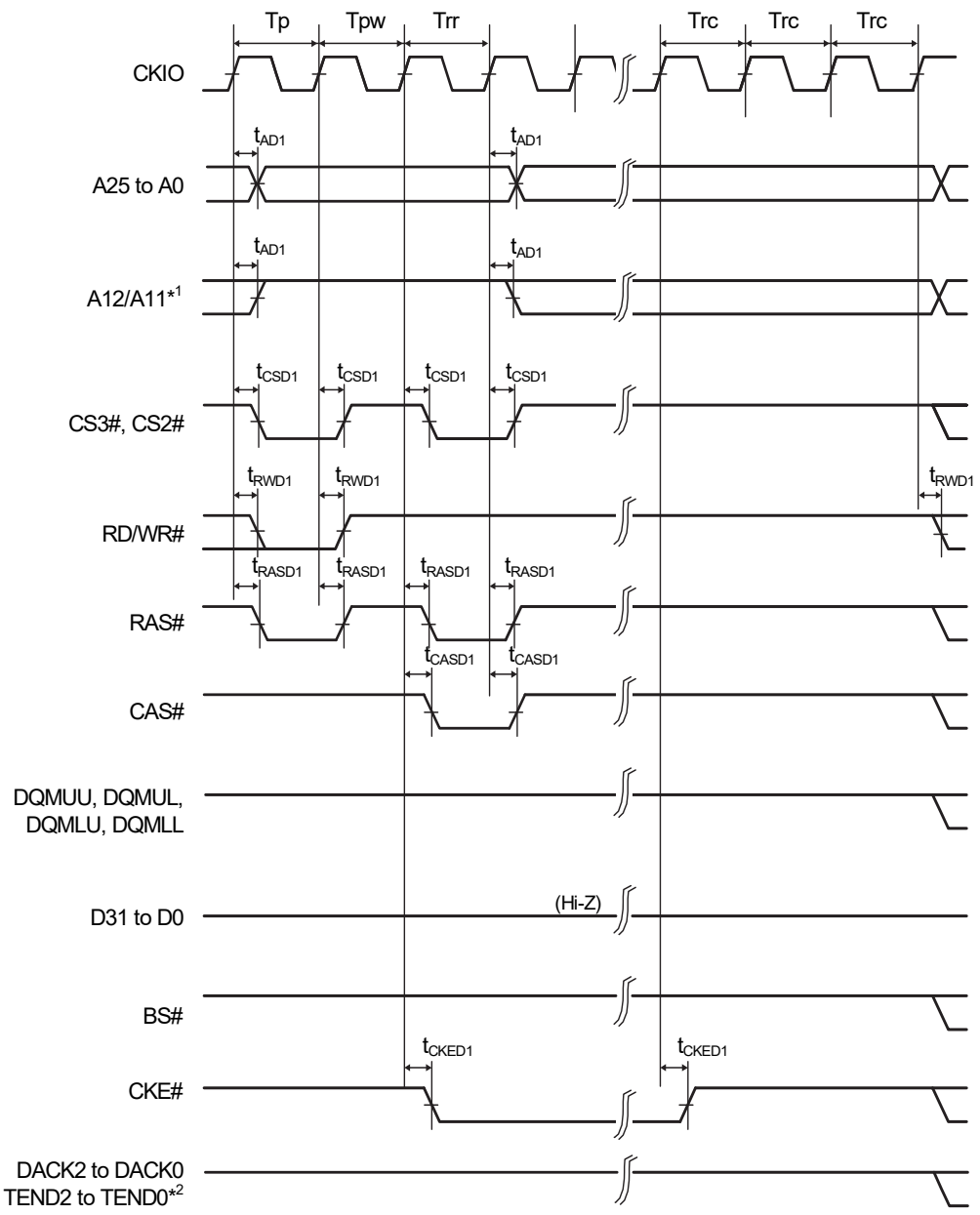
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.33 Synchronous DRAM Burst-Write Bus Cycle (Write for 4 Cycles) (Bank Active Mode: PRE + ACT + WRITE Command, Different Row Address, WTRCD = 0 Cycles, TRWL = 0 Cycles)



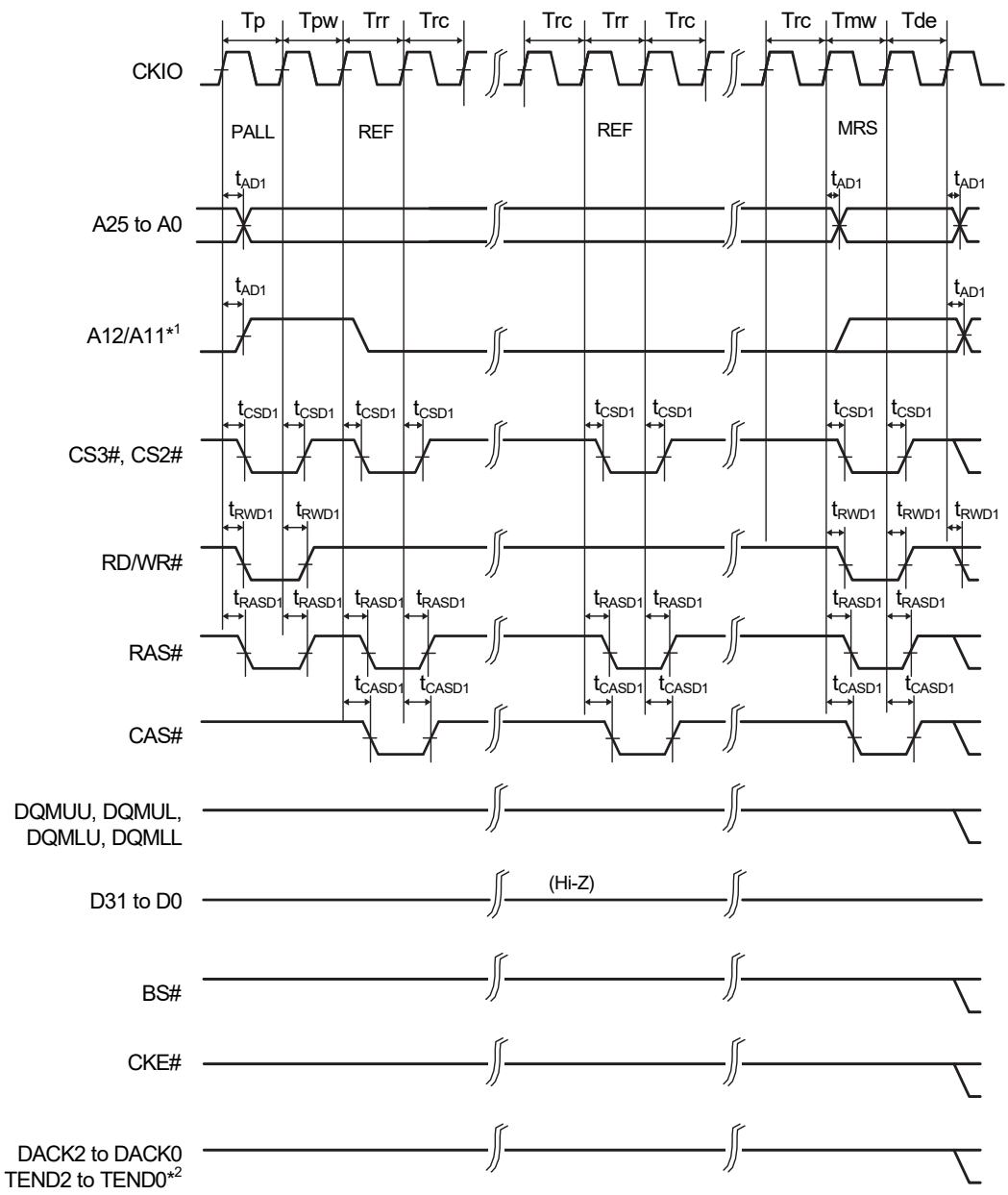
Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.34 Synchronous DRAM Auto-Refresh Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.35 Synchronous DRAM Self-Refresh Timing (WTRP = 1 Cycle)



Note 1. Address pin to be connected to A10 of SDRAM
Note 2. DACKn and TENDn are waveforms when “active low” is specified.

Figure 47.36 Synchronous DRAM Mode Register Write Timing (WTRP = 1 Cycle)

47.4.4 DMAC Timing

Table 47.18 DMAC Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min*1	max	Unit	Test Conditions
DMAC	DREQ pulse width	t_{DRQW}	t_{PBcyc} × 2	—	ns	Figure 47.37
	DACK and TEND delay time	t_{DACD}	0	10	ns	Figure 47.38

Note 1. t_{PBcyc}: PCLKB cycle

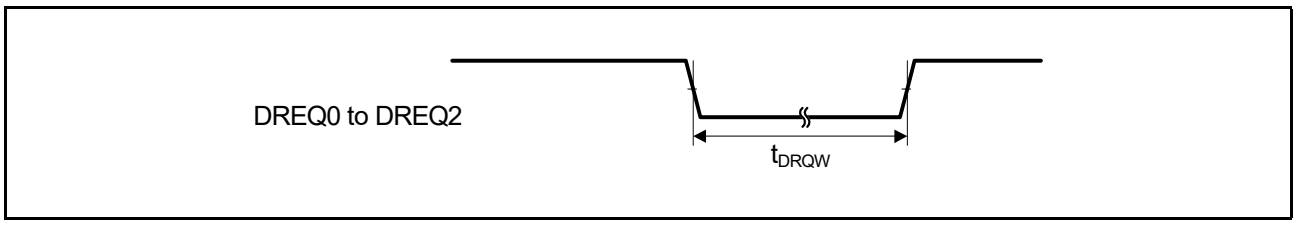


Figure 47.37 DREQ Input Timing

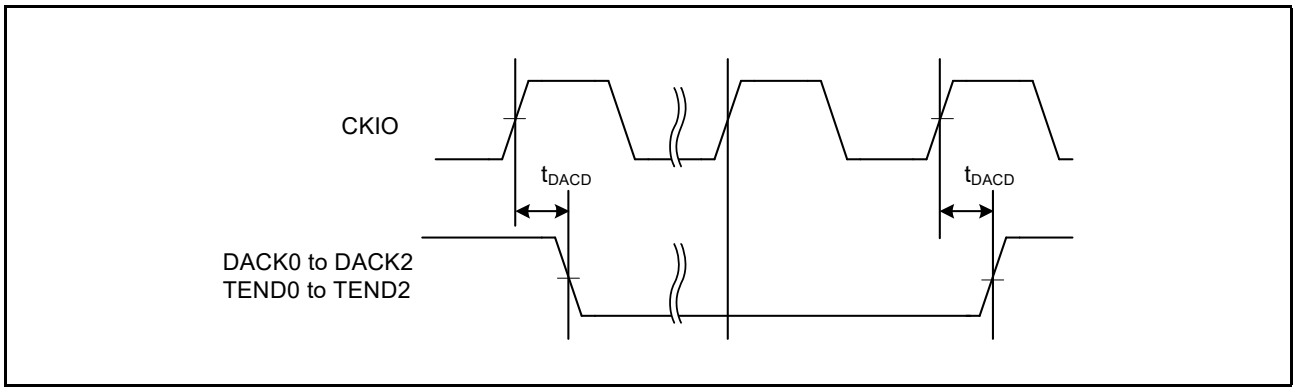


Figure 47.38 DACK and TEND Output Timing

47.4.5 On-Chip Peripheral Module Timing

47.4.5.1 I/O Port Timing

Table 47.19 I/O Port Timing

Item		Symbol	min	max	Unit*1	Test Conditions
I/O port	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 47.39

Note 1. t_{PBcyc}: PCLKB cycle

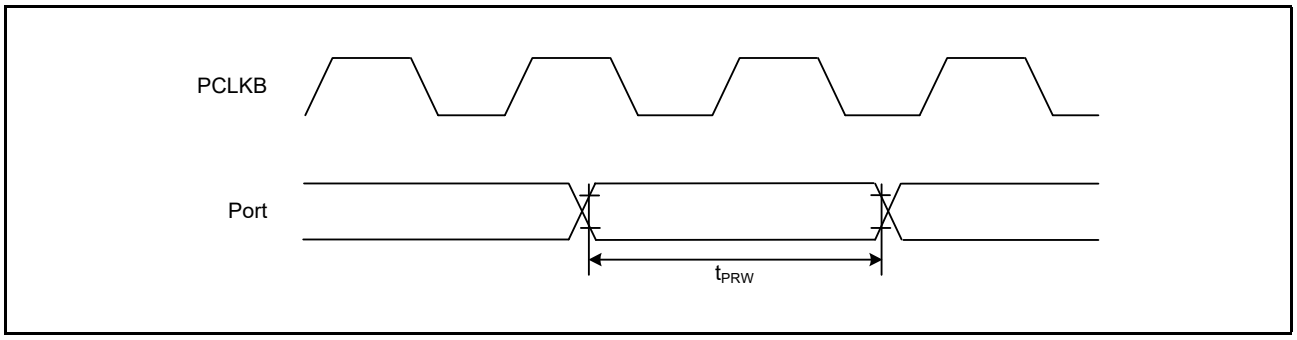


Figure 47.39 I/O Port Input Timing

47.4.5.2 TPUa Timing

Table 47.20 TPUa Timing

Item			Symbol	min	max	Unit*1	Test Conditions
TPUa	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PDcyc}	Figure 47.40
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PDcyc}	Figure 47.41
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

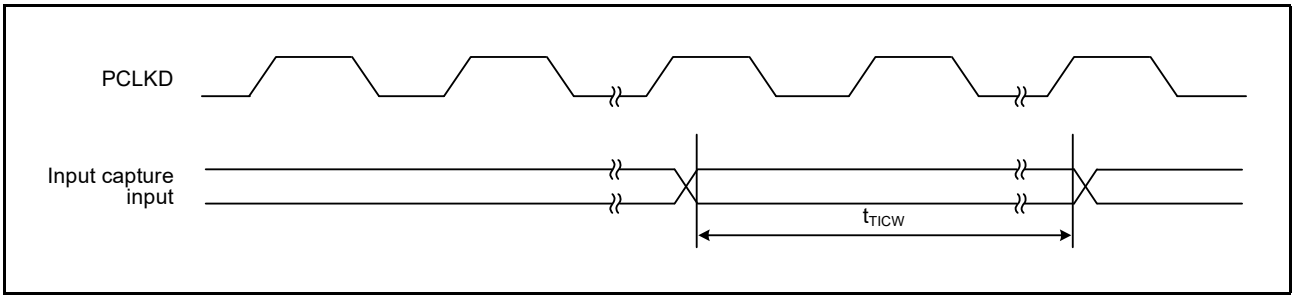


Figure 47.40 TPUa Input Capture Input Timing

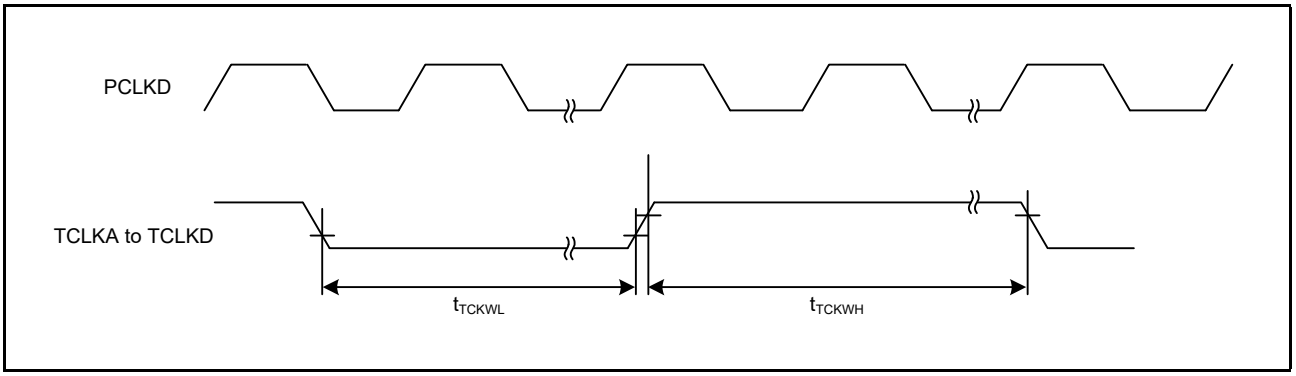


Figure 47.41 TPUa Clock Input Timing

47.4.5.3 CMTW Timing

Table 47.21 CMTW Timing

Item			Symbol	min	max	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWICW}$	1.5	—	t_{PDcyc}	Figure 47.42
		Both-edge setting		2.5	—		

Note 1. t_{PDcyc}: PCLKD cycle

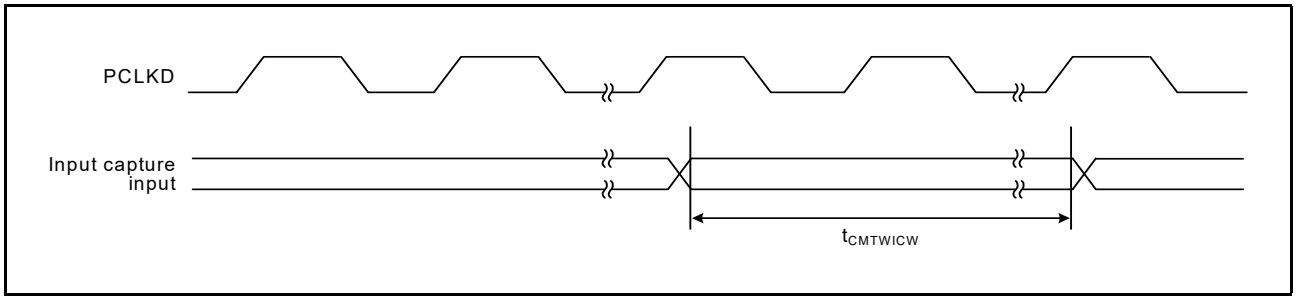


Figure 47.42 CMTW Input Capture Input Timing

47.4.5.4 MTU3a Timing

Table 47.22 MTU3a Timing

Item			Symbol	min	max	Unit*1	Test Conditions
MTU3a	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PCcyc}	Figure 47.43
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PCcyc}	Figure 47.44
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

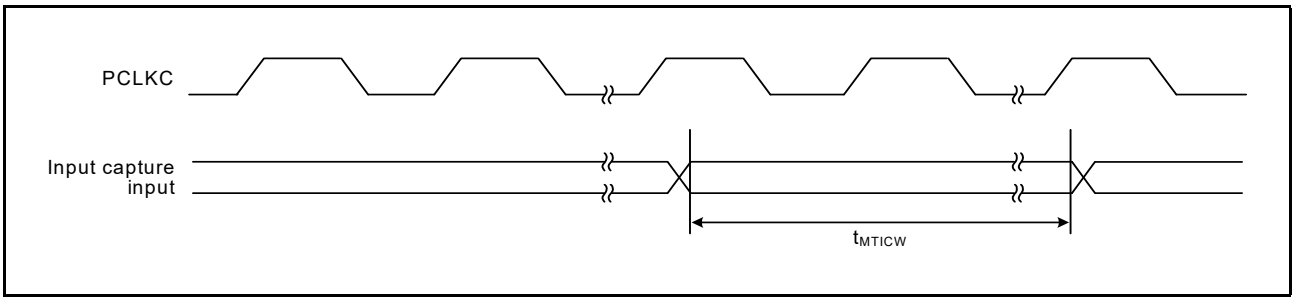


Figure 47.43 MTU3a Input Capture Input Timing

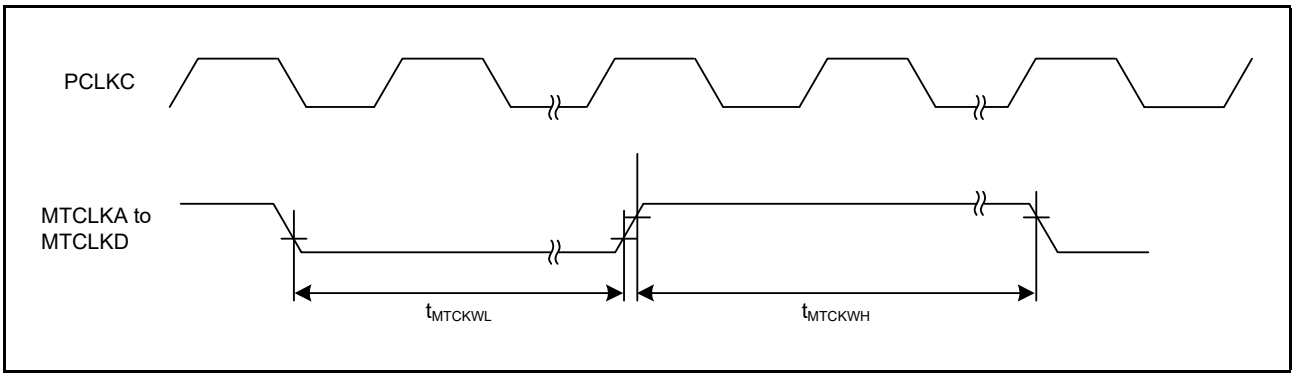


Figure 47.44 MTU3a Clock Input Timing

47.4.5.5 POE3 Timing

Table 47.23 POE3 Timing

Item		Symbol	min	max	Unit*1	Test Conditions
POE3	POEn# input pulse width	t_{POEW}	1.5	—	t_{PDcyc}	Figure 47.45

Note 1. t_{PDcyc}: PCLKD cycle

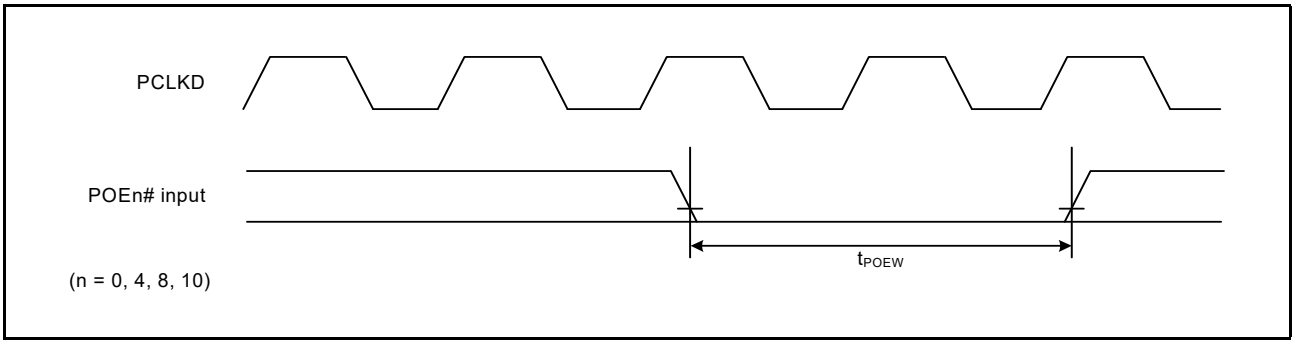


Figure 47.45 POEn# Input Pulse Timing

47.4.5.6 GPTa Timing

Table 47.24 GPTa Timing

Item			Symbol	min	max	Unit*1	Test Conditions
GPTa	Input capture input pulse width	Single-edge setting	t_{GTICW}	3	—	t_{PCcyc}	Figure 47.46
		Both-edge setting		5	—		
	External trigger input pulse width	Single-edge setting	t_{GTEW}	1.5	—	t_{PCcyc}	Figure 47.47
		Both-edge setting		2.5	—		

Note 1. t_{PCcyc}: PCLKC cycle

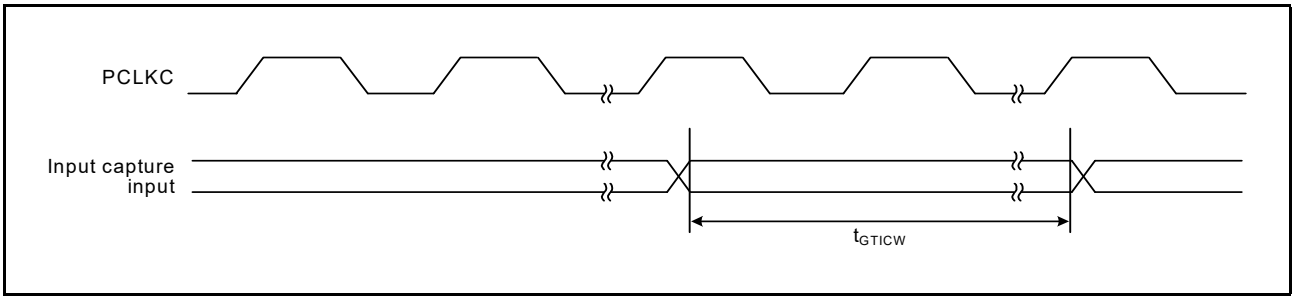


Figure 47.46 GPTa Input Capture Input Timing

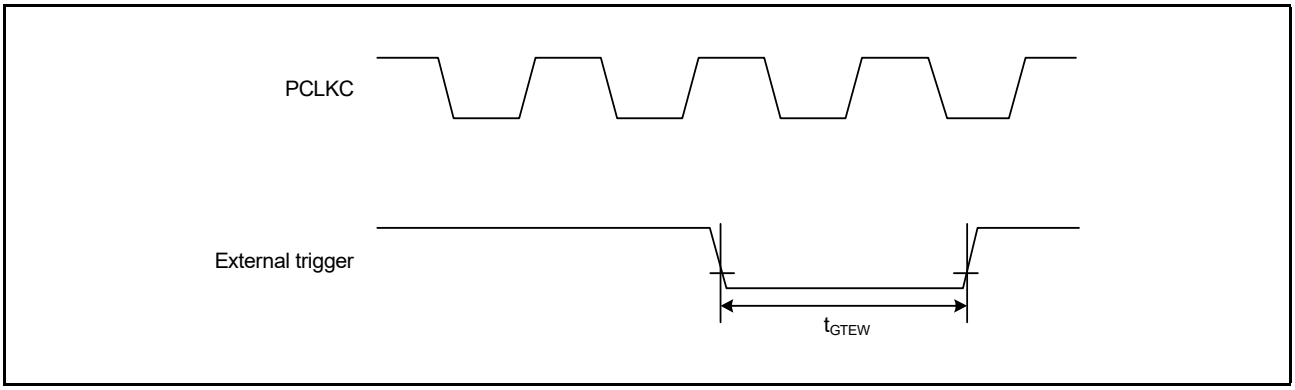


Figure 47.47 GPTa External Trigger Input Timing

47.4.5.7 A/D Converter Trigger Timing

Table 47.25 A/D Converter Trigger Timing

Item			Symbol	min	max	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	ADTRG0	t_{TRGW}	1.5	—	t_{PFcyc}	Figure 47.48
		ADTRG1		1.5		t_{PGcyc}	Figure 47.49

Note 1. t_{PFcyc}: PCLKF cycle, t_{PGcyc}: PCLKG cycle

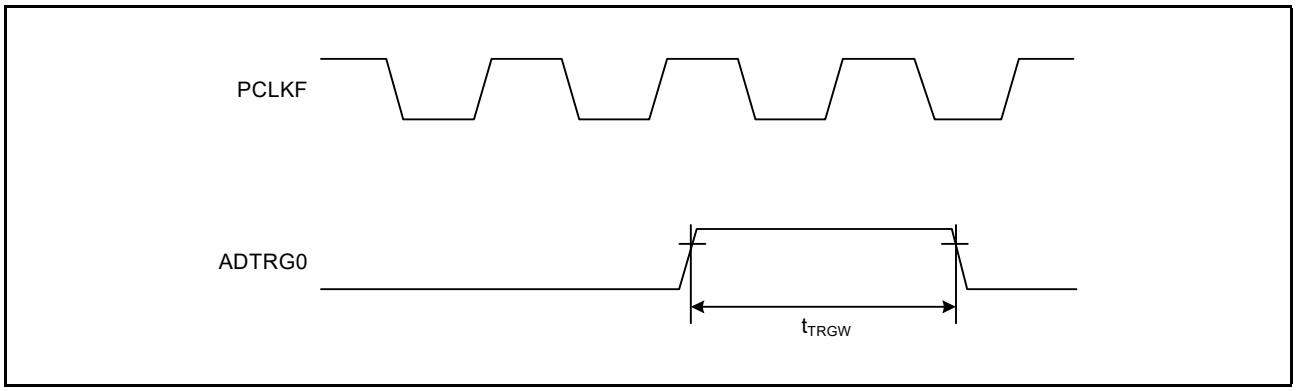


Figure 47.48 A/D Converter Trigger Input Timing (ADTRG0)

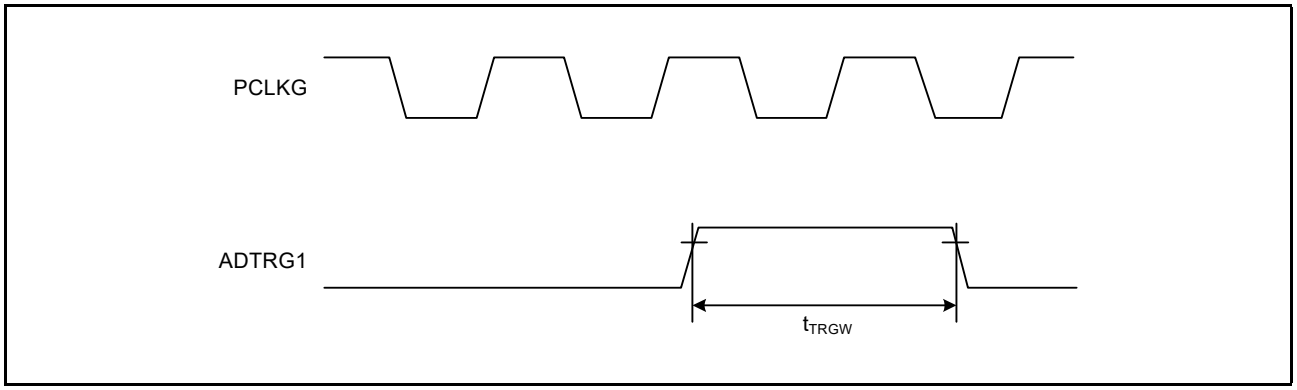


Figure 47.49 A/D Converter Trigger Input Timing (ADTRG1)

47.4.5.8 SCIFA Timing

Table 47.26 SCIFA Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min*1	max*1	Unit*1	Test Conditions
SCIFA	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{SEcyc}	Figure 47.50
		Clock synchronous		12	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rising time		t_{SCKr}	—	5	ns	
	Input clock falling time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous*2	t_{Scyc}	8	—	t_{SEcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rising time		t_{SCKr}	—	9	ns	
	Output clock falling time		t_{SCKf}	—	9	ns	
	Transmit data delay time	Internal clock	t_{TXD}	-10	10	ns	Figure 47.51
		External clock		3 × t_{SEcyc}	4 × t_{SEcyc} + 20		
	Receive data setup time	Internal clock	t_{RXS}	3 × t_{SEcyc} + 20	—	ns	
		External clock		t_{SEcyc} + 10	—		
	Receive data hold time	Internal clock	t_{RXH}	-3 × t_{SEcyc}	—	ns	
		External clock		2 × t_{SEcyc} + 10	—		

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. When the SEMR.ABCS0 bit = 1 and the SEMR.BGDM bit = 1

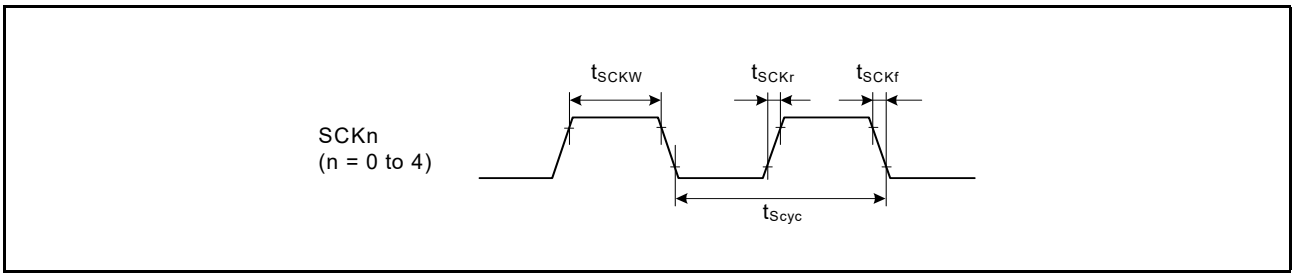


Figure 47.50 SCK Clock Input Timing

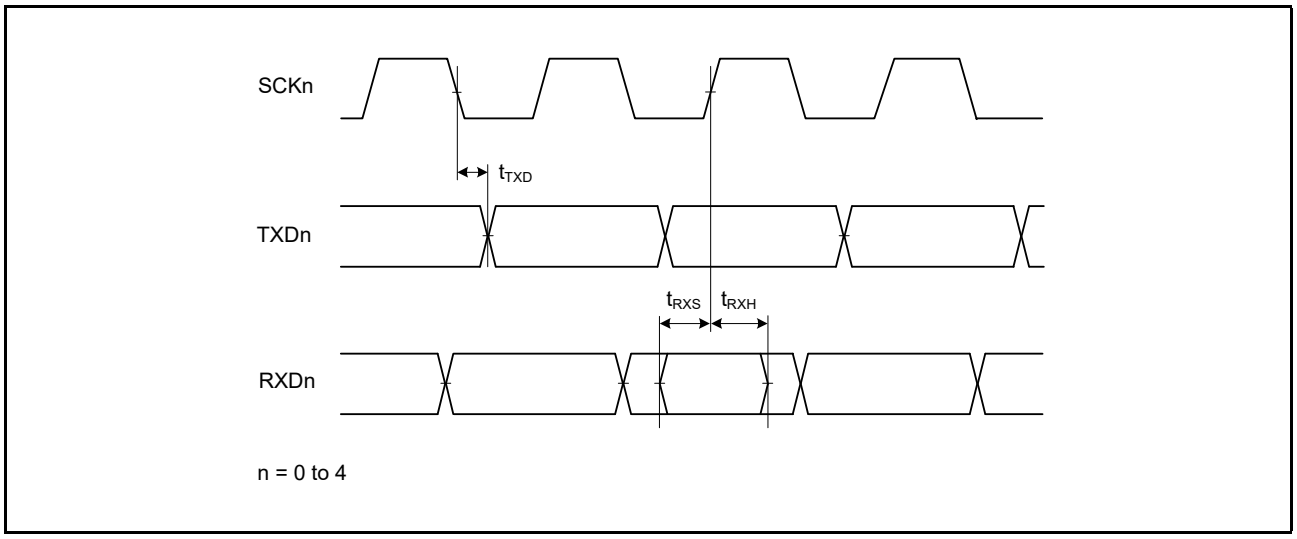


Figure 47.51 SCIFA Input/Output Timing/Clock Synchronous Mode

47.4.5.9 RSPIa Timing

Table 47.27 RSPIa Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol*1	Min*1	Max*1	Unit*1	Test Conditions
RSPIa	RSPCK clock cycle	Master	t_{SPcyc}	4	4096	t_{SEcyc}	Figure 47.52
		Slave*4		8	4096		
	RSPCK clock high level pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock low level pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	—	ns	
		Slave		0.4	—	t_{SPcyc}	
	RSPCK clock rising/falling time	Output	t_{SPCKr}, t_{SPCKf}	—	9	ns	
		Input		—	10	ns	
	Data input setup time	Master	t_{SU}	6	—	ns	Figure 47.53 to Figure 47.56
		Slave		$8 - t_{SEcyc}$	—		
	Data input hold time	Master	t_H	t_{SEcyc}	—	ns	
		Slave		$8 + 2 \times t_{SEcyc}$	—		
	SSL setup time	Master	t_{LEAD}	$N \times t_{Spcyc} - 3$*2	$N \times t_{Spcyc} + 3$*2	ns	
		Slave		4	—	t_{SEcyc}	
	SSL hold time	Master	t_{LAG}	$N \times t_{Spcyc} - 3$*3	$N \times t_{Spcyc} + 3$*3	ns	
		Slave		4	—	t_{SEcyc}	
	Data output delay time	Master	t_{OD}	—	6	ns	
		Slave		—	$3 \times t_{SEcyc} + 20$ *4		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Continuous transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{SEcyc}$	$8 \times t_{SPcyc} + 2 \times t_{SEcyc}$	ns	
		Slave		$4 \times t_{SEcyc}$	—		
	MOSI, MISO rising/falling time	Output	t_{Dr}, t_{Df}	—	9	ns	
		Input		—	10	ns	
	SSL rising/falling time	Output	t_{SSLr}, t_{SSLf}	—	9	ns	
		Input		—	10	ns	
	Slave access time		t_{SA}	—	4	t_{SEcyc}	Figure 47.55 to Figure 47.56
	Slave output release time		t_{REL}	—	3	t_{SEcyc}	

Note 1. t_{SEcyc}: SERICLK cycle
Note 2. N = SPCKD set value + 1 (1 to 8)
Note 3. N = SSLND set value + 1 (1 to 8)
Note 4. The data output delay time may become longer than half a cycle of the RSPCK clock depending on the bit rate setting. Be sure to satisfy the conditions required for the electrical characteristics of the master device.

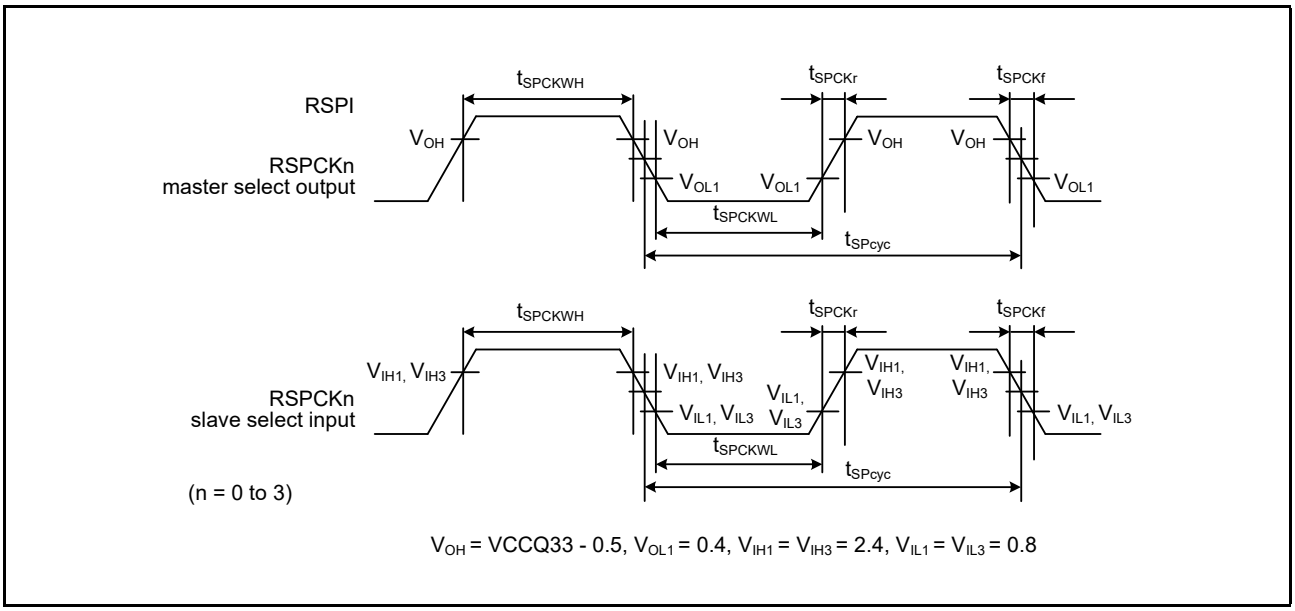


Figure 47.52 RSPIa Clock Timing

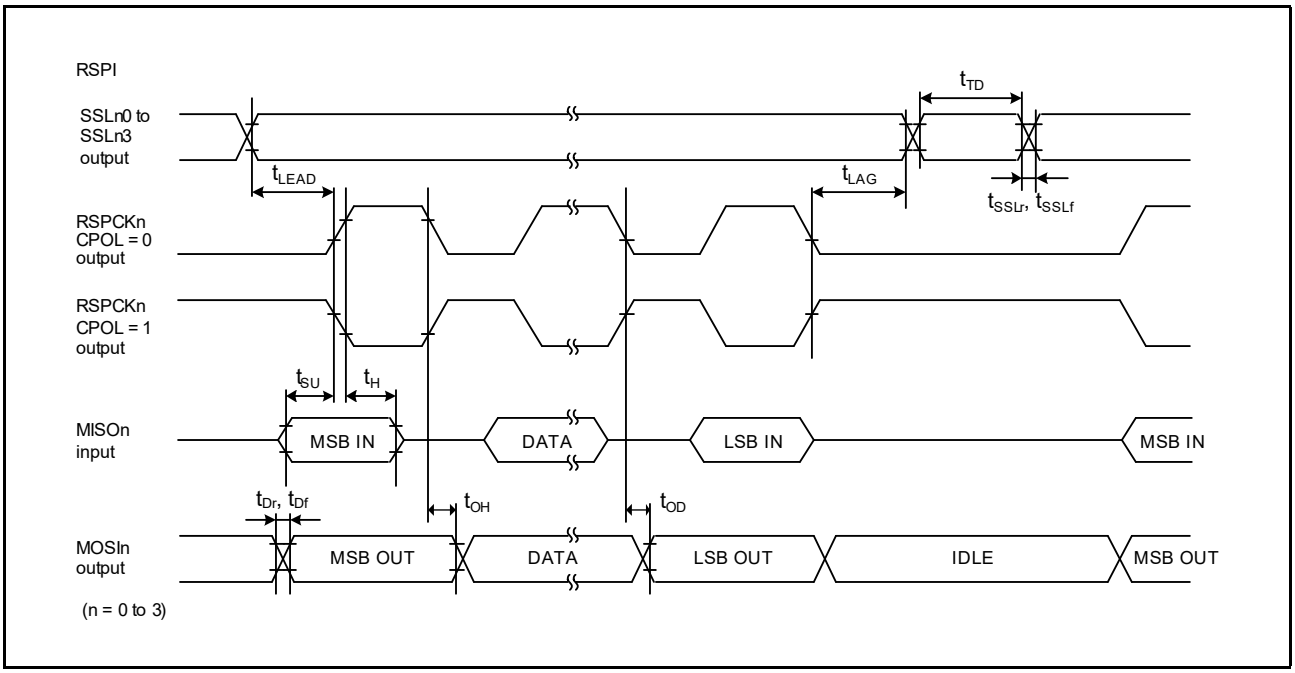


Figure 47.53 RSPIa Timing (Master, CPHA = 0)

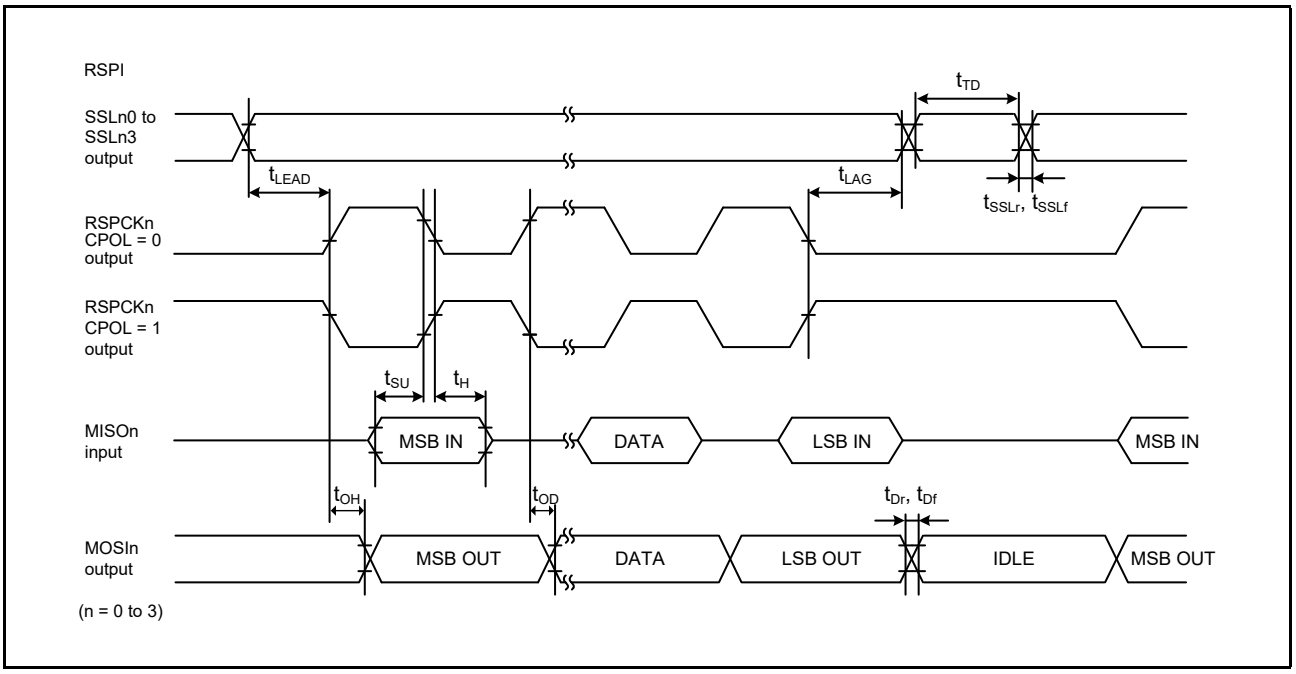


Figure 47.54 RSPIa Timing (Master, CPHA = 1)

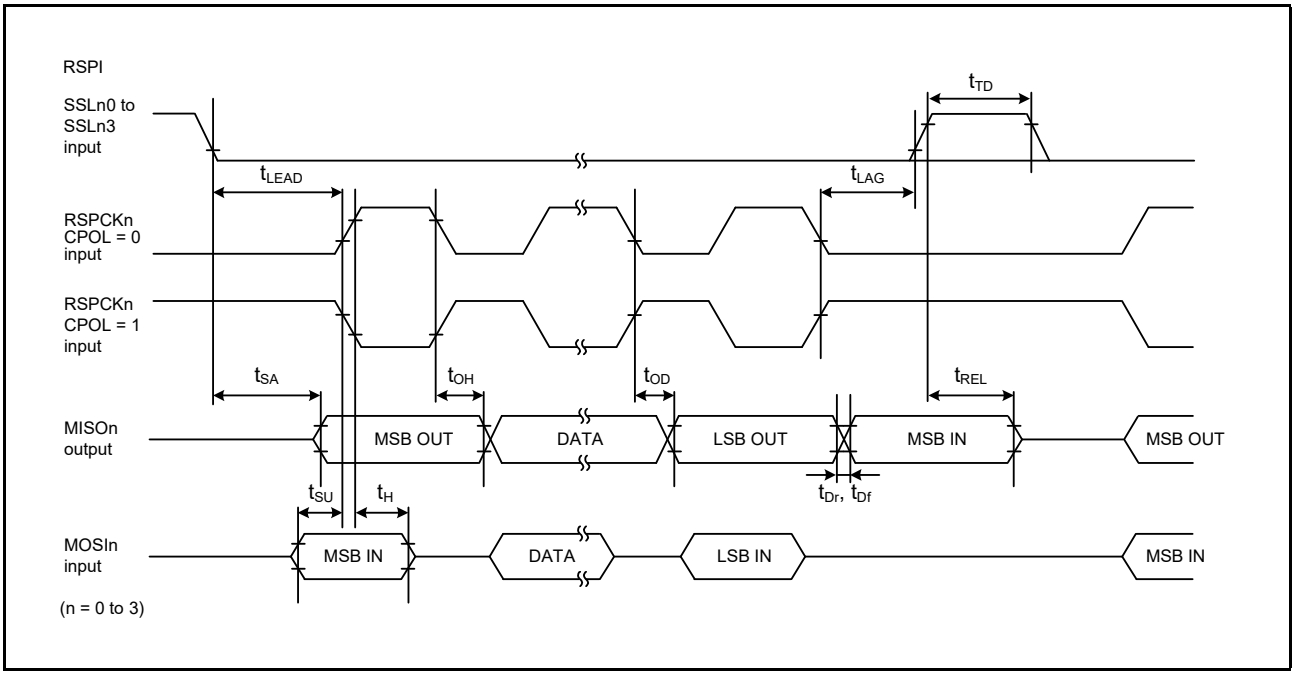


Figure 47.55 RSPI Timing (Slave, CPHA = 0)

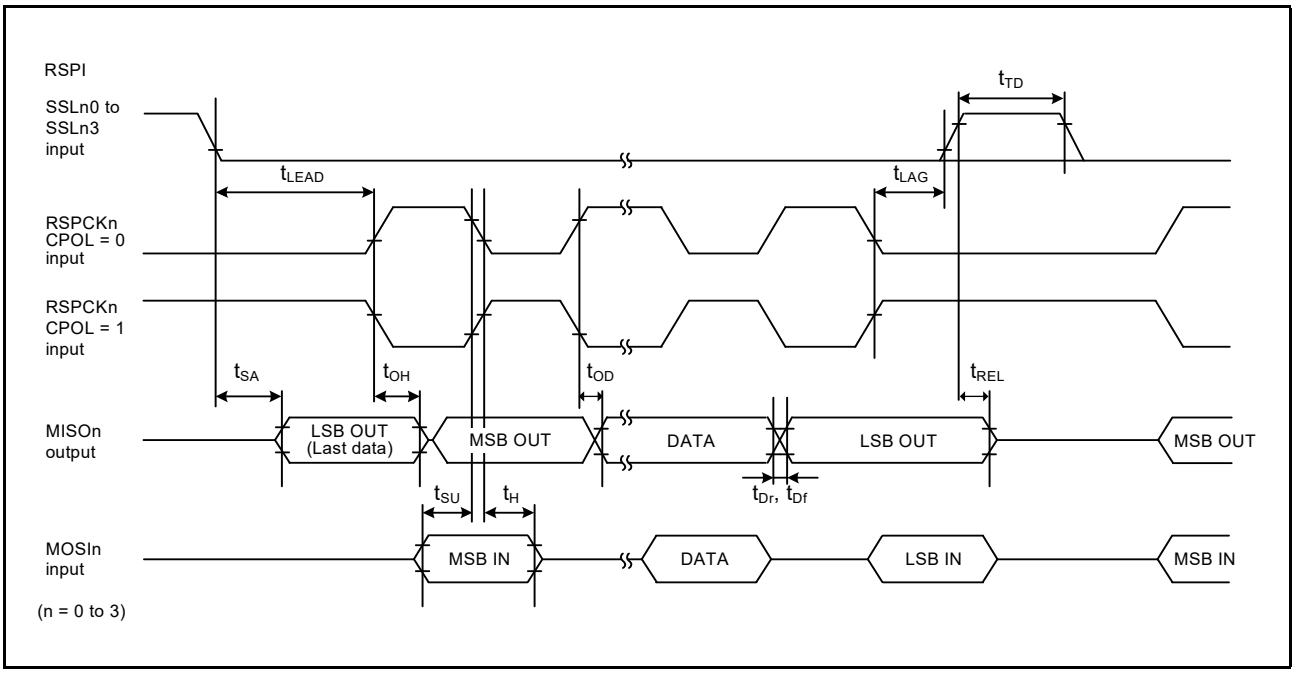


Figure 47.56 RSPI Timing (Slave, CPHA = 1)

47.4.5.10 SPIBSC Timing

Table 47.28 SPIBSC Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit*1	Test Conditions
SPIBSC	SPBCLK clock cycle	t_{SPBcyc}	2	4080	t_{PAcyc}	Figure 47.57
	SPBCLK high level pulse width	t_{SPBWH}	0.45	0.55	t_{SPBcyc}	
	SPBCLK low level pulse width	t_{SPBWL}	0.45	0.55	t_{SPBcyc}	
	Data input setup time	t_{SU}	3.5	—	ns	Figure 47.58, Figure 47.59, Figure 47.60
	Data input hold time	t_{H}	0.5	—	ns	
	SSL setup time	t_{LEAD}	1 × t_{SPBcyc} – 3	8 × t_{SPBcyc}	ns	
	SSL hold time	t_{LAG}	1.5 × t_{SPBcyc}	8.5 × t_{SPBcyc} + 3	ns	
	Continuous transfer delay time	t_{TD}	1	8	t_{SPBcyc}	
	Data output delay time	t_{OD}	—	3.6	ns	
	Data output hold time	t_{OH}	-1	—	ns	
	Data output buffer on time	t_{BON}	—	3.6	ns	Figure 47.61, Figure 47.62, Figure 47.63
	Data output buffer off time	t_{BOFF}	-7	0	ns	

Note 1. t_{PAcyc}: PCLKA cycle

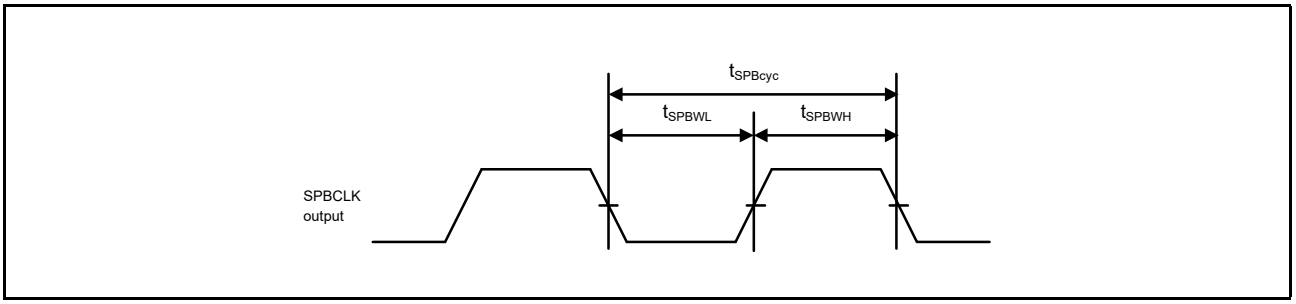


Figure 47.57 SPIBSC Clock Timing

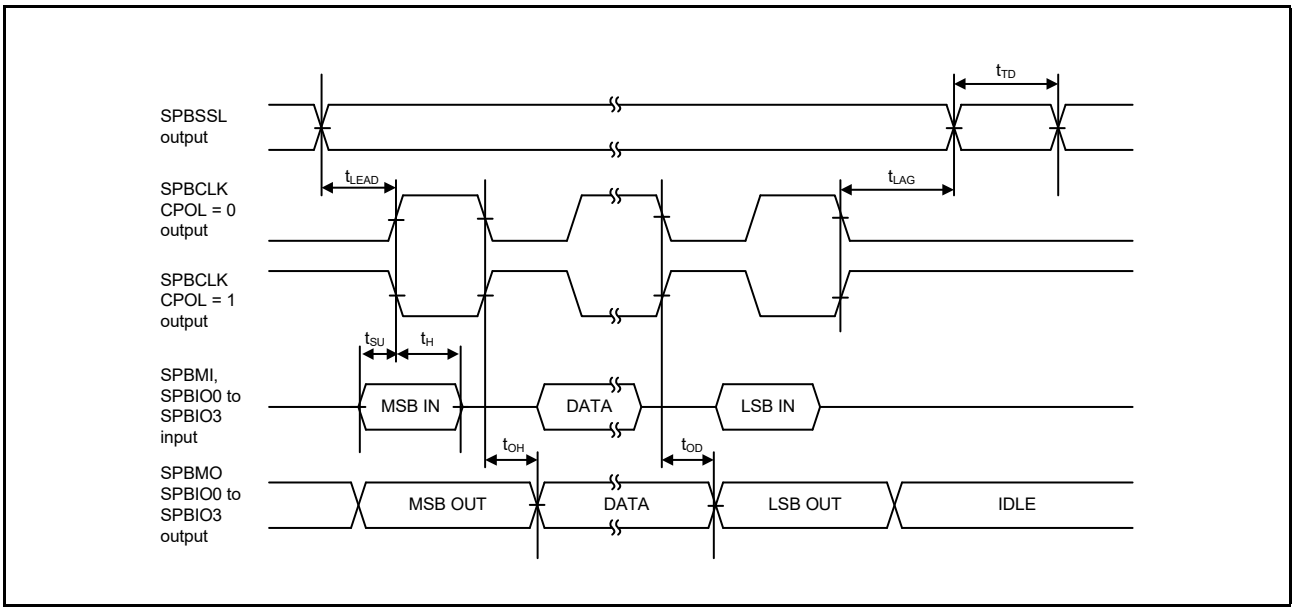


Figure 47.58 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 0)

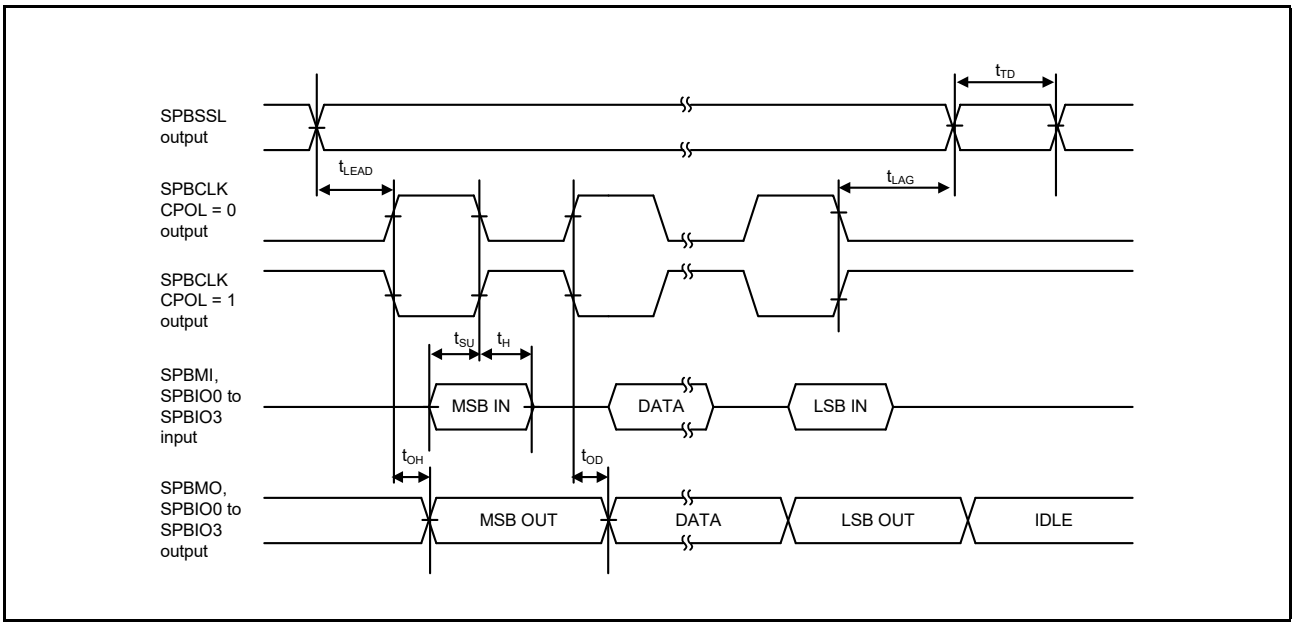


Figure 47.59 SPIBSC Transmit/Receive Timing (CPHAT = 1, CPHAR = 1)

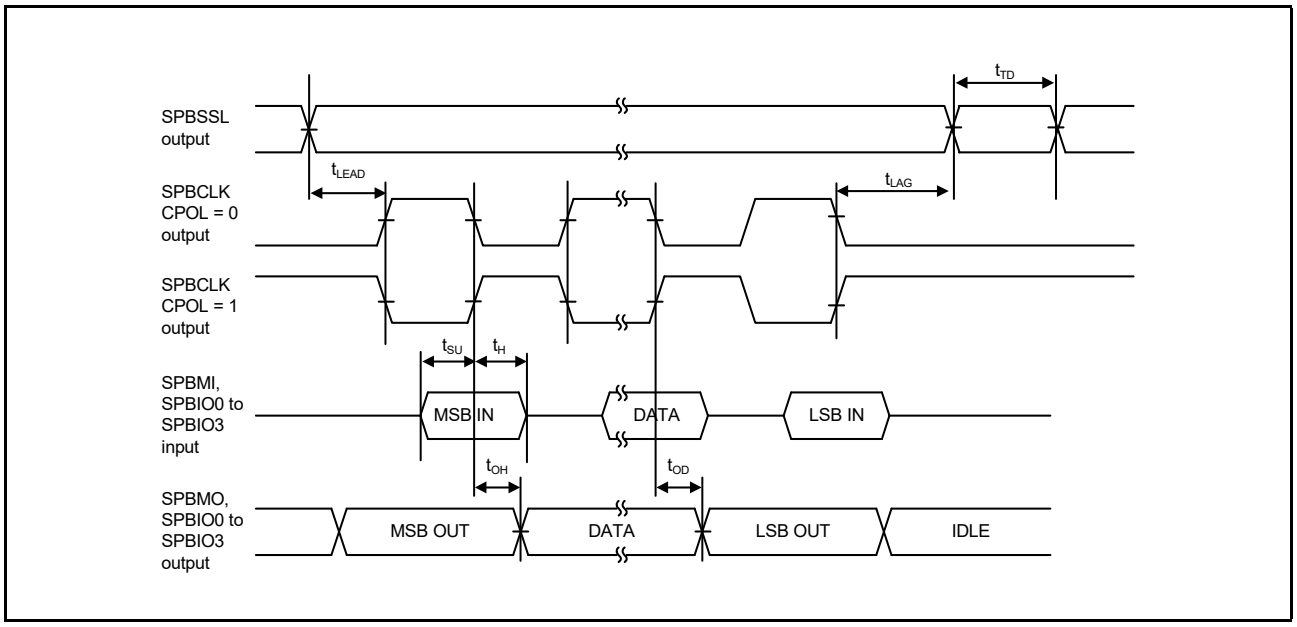


Figure 47.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1)

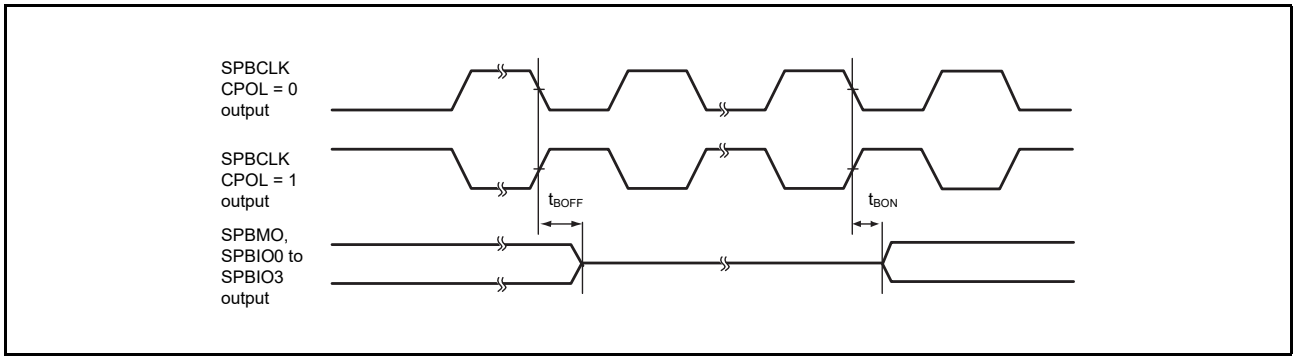


Figure 47.61 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 0)

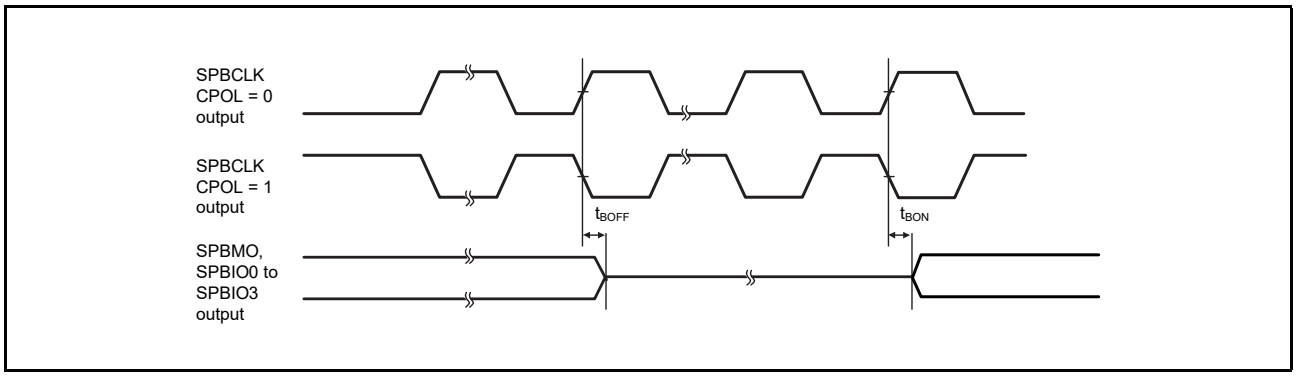


Figure 47.62 SPIBSC Buffer On/Off Timing (CPHAT = 1, CPHAR = 1)

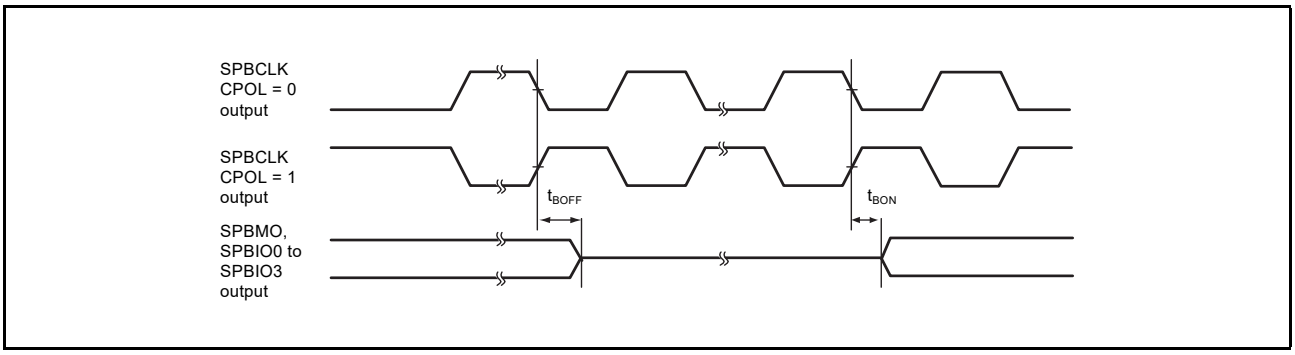


Figure 47.63 SPIBSC Buffer On/Off Timing (CPHAT = 0, CPHAR = 1)

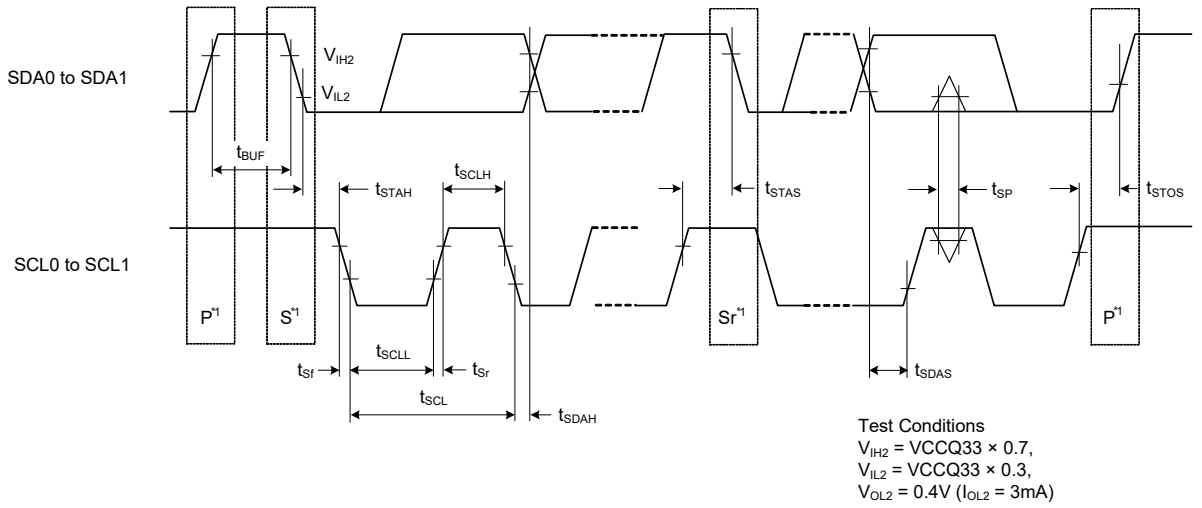
47.4.5.11 RIICa Timing

Table 47.29 RIICa Timing

Output load conditions: V_{OL2} = 0.4 V, I_{OL2} = 3 mA

Item		symbol	min*2	max*2	Unit*1	Test Conditions
RIICa (Standard-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 47.64
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—	1000	ns	
	SCL, SDA input falling time	t_{sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIICa (Fast-mode)	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rising time	t_{sr}	—*4	300	ns	
	SCL, SDA input falling time	t_{sf}	—*4	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load*3	C_b	—	400	pF	

Note 1. t_{IICcyc}: RIIC internal reference clock (IICϕ) cycle
Note 2. The value out of parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 00b while the digital filter is enabled by setting ICFER.NFE = 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by setting ICFER.NFE = 1.
Note 3. C_b is the total capacitance of the bus lines.
Note 4. The minimum values are not specified for tsr and tsf in Fast-mode.



Note 1. S, P, and Sr indicate the following conditions.
S: Start condition
P: Stop condition
Sr: Restart condition

Figure 47.64 RIICa Bus Interface Input/Output Timing

47.4.5.12 Serial Sound Interface Timing

Table 47.30 Serial Sound Interface Timing

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	Min.	Max.	Unit	Test Conditions
SSI	AUDIO_CLK input frequency	t_{AUDIO}	1	50	MHz	
	Output clock cycle	t_O	150	64000	ns	Figure 47.65
	Input clock cycle	t_I	150	64000	ns	
	Clock high level	t_{HC}	60	—	ns	
	Clock low level	t_{LC}	60	—	ns	
	Clock rising time	t_{RC}	—	25	ns	
	Data delay time	t_{DTR}	-5	25	ns	Figure 47.66, Figure 47.67
	Setup time	t_{SR}	25	—	ns	
	Hold time	t_{HTR}	25	—	ns	
	WS change edge SSITXD0 output delay	T_{DTRW}	—	25	ns	Figure 47.68

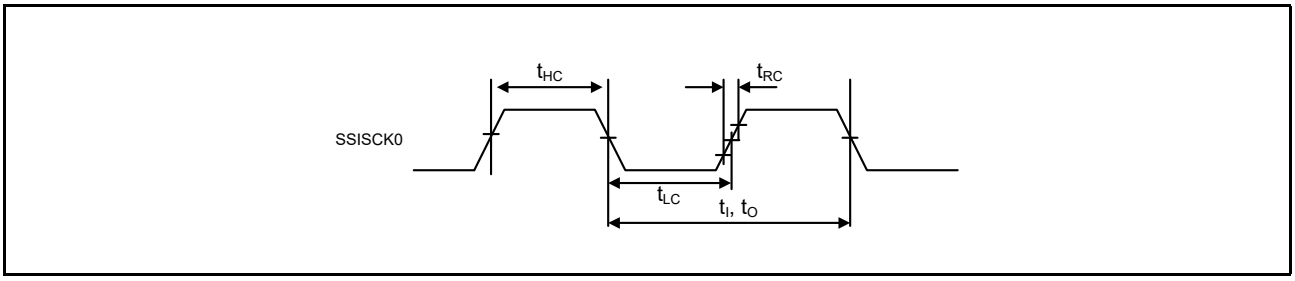


Figure 47.65 Clock Input/Output Timing

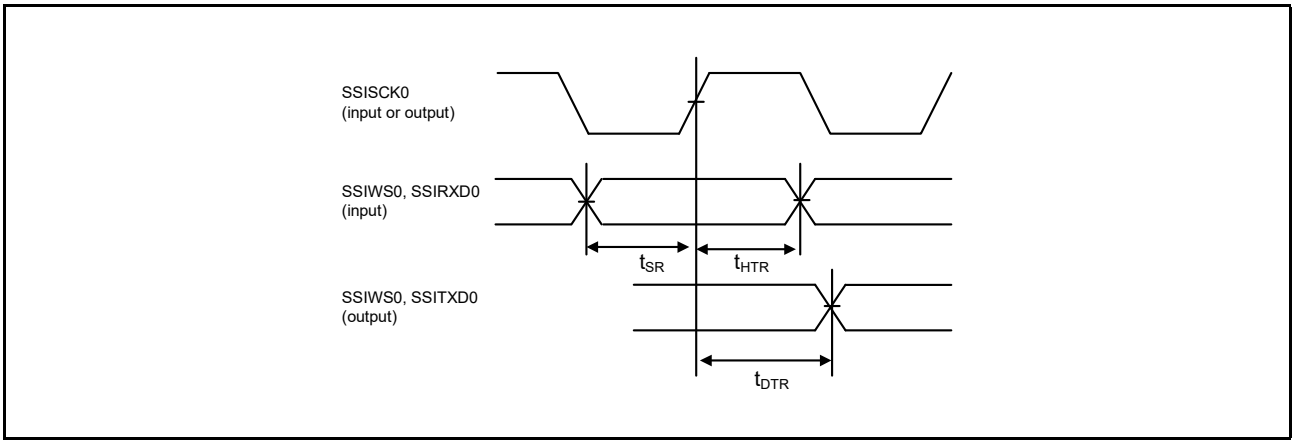


Figure 47.66 Transmit/Receive Timing (SSISCK0 Rising Synchronous)

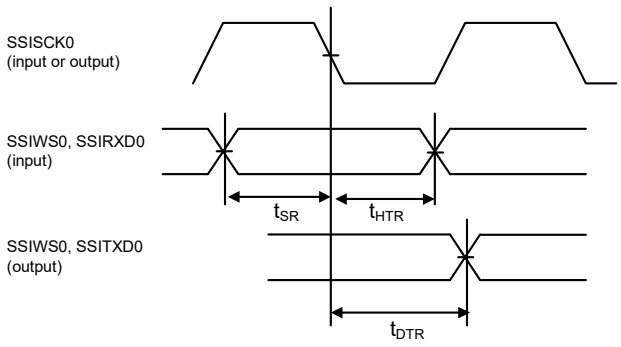
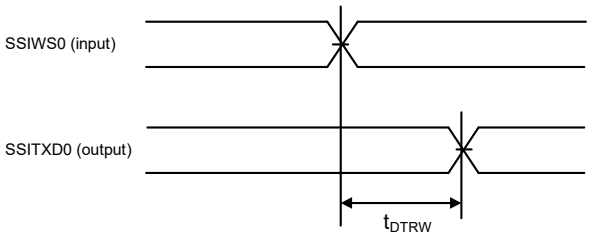


Figure 47.67 Transmit/Receive Timing (SSISCK0 Falling Synchronous)



MSB bit output timing in slave transmission from SSIWS0 with the settings of DEL = 1, SDTA = 0, or DEL = 1, SDTA = 1, SWL[2:0] = DWL[2:0]

Figure 47.68 SSITXD0 Output Delay from SSIWS0 Change Edge

47.4.5.13 CAN Interface Timing

Table 47.31 CAN Interface Timing

Item	Symbol	min	max	Unit	Test Conditions
Internal delay time	tnode	—	100	ns	Figure 47.69
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transmission delay time (toutput) + Internal reception delay time (tinput)

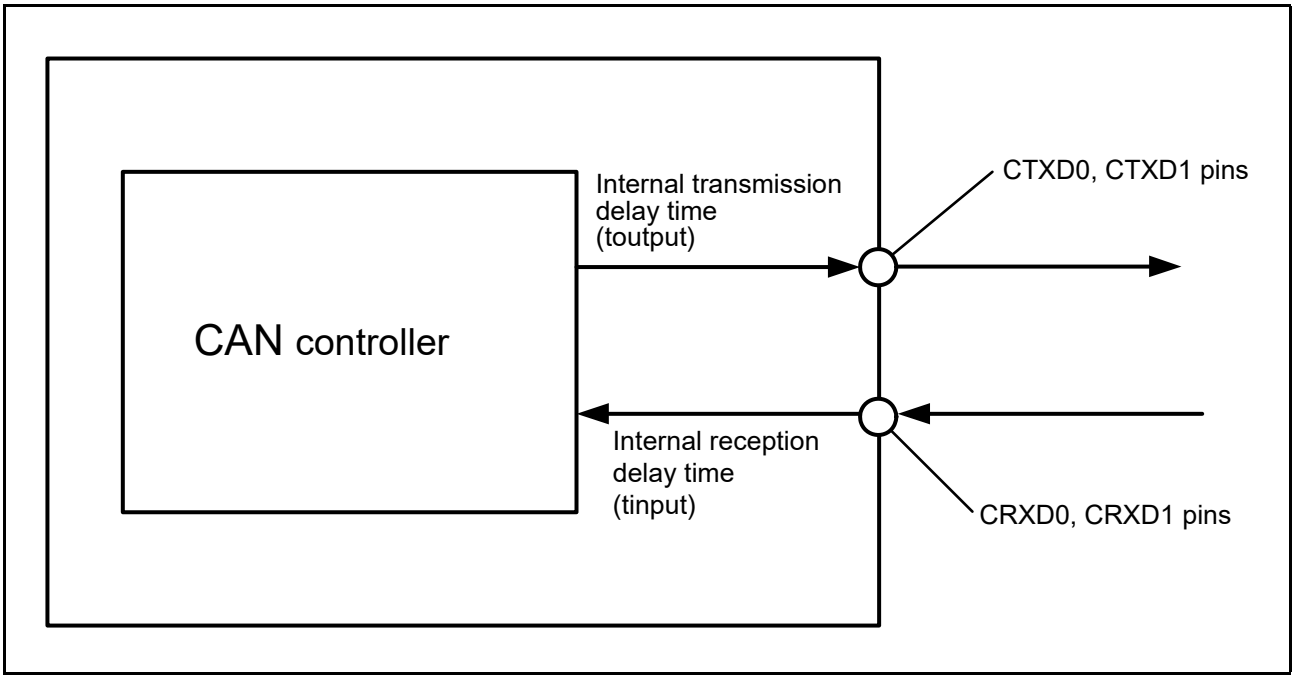


Figure 47.69 CAN Interface Conditions

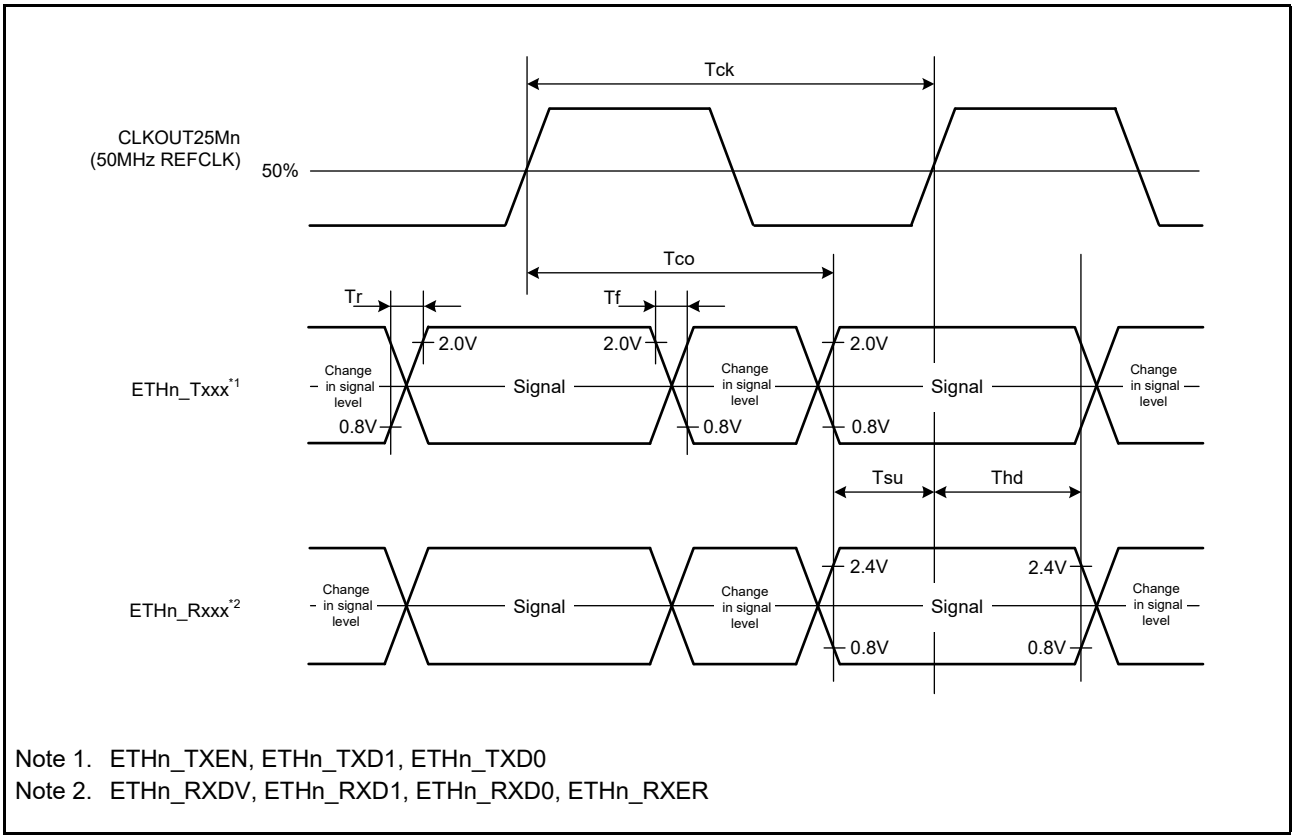
47.4.5.14 ETHERC Timing

Table 47.32 ETHERC Timing

Output load conditions: V_{OH} = 2.0 V, V_{OL1} = 0.8 V, C = 25 pF (RMII)
V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF (MII)

Item		Symbol	min	max	Unit	Test Conditions
ETHERC (RMII)	CLKOUT25Mn cycle time	T_{ck}	20	—	ns	Figure 47.70 to Figure 47.73
	ETHn_Txxx*1 output delay time	Tco	2	16	ns	
	ETHn_Rxxx*2 setup time	T_{su}	4	—	ns	
	ETHn_Rxxx*2 hold time	T_{hd}	2	—	ns	
	ETHn_xxxx*1, *2 rising/falling time	T_r, T_f	0.5	5	ns	
ETHERC (MII)	ETHn_TXC cycle time	t_{Tcyc}	40	—	ns	—
	ETHn_TXEN output delay time	t_{TENd}	0	25	ns	Figure 47.74
	ETHn_TXD0 to ETHn_TXD3 output delay time	t_{MTDd}	0	25	ns	
	ETHn_TXER output delay time	t_{TERd}	—	25	ns	Figure 47.75
	ETHn_RXC cycle time	t_{TRcyc}	40	—	ns	—
	ETHn_RXDV setup time	t_{RDVs}	10	—	ns	Figure 47.76
	ETHn_RXDV hold time	t_{RDVh}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 setup time	t_{MRDs}	10	—	ns	
	ETHn_RXD0 to ETHn_RXD3 hold time	t_{MRDh}	10	—	ns	
	ETHn_RXER setup time	t_{RERs}	10	—	ns	Figure 47.77
	ETHn_RXER hold time	t_{RERh}	10	—	ns	

Note 1. ETHn_TXEN, ETHn_TXD1, ETHn_TXD0
Note 2. ETHn_RXDV, ETHn_RXD1, ETHn_RXD0, ETHn_RXER
n = 0 to 2



Note 1. ETHn_TXEN, ETHn_TXD1, ETHn_TXD0
Note 2. ETHn_RXDV, ETHn_RXD1, ETHn_RXD0, ETHn_RXER

Figure 47.70 Timing with the CLKOUT25Mn and RMII Signals

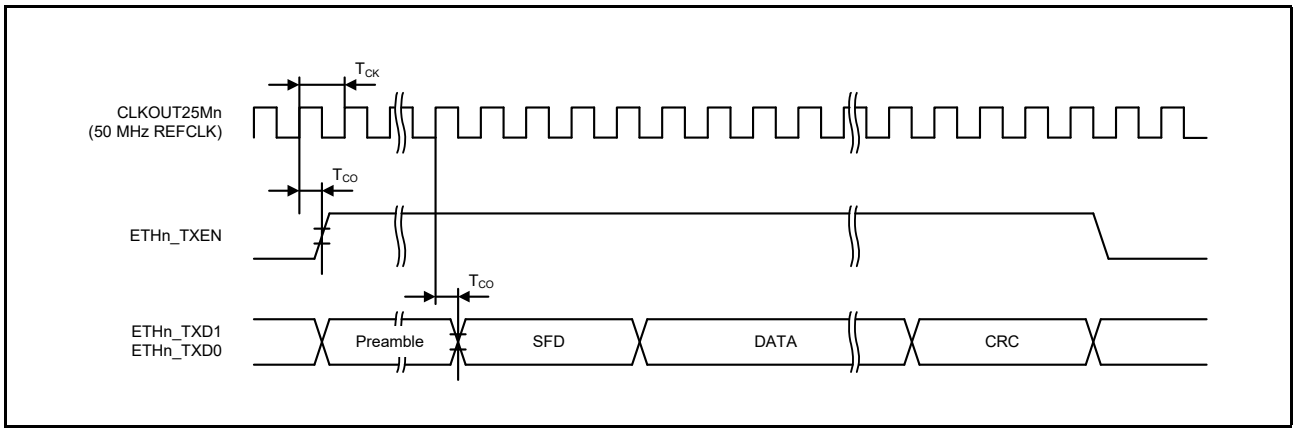


Figure 47.71 RMII Transmission Timing

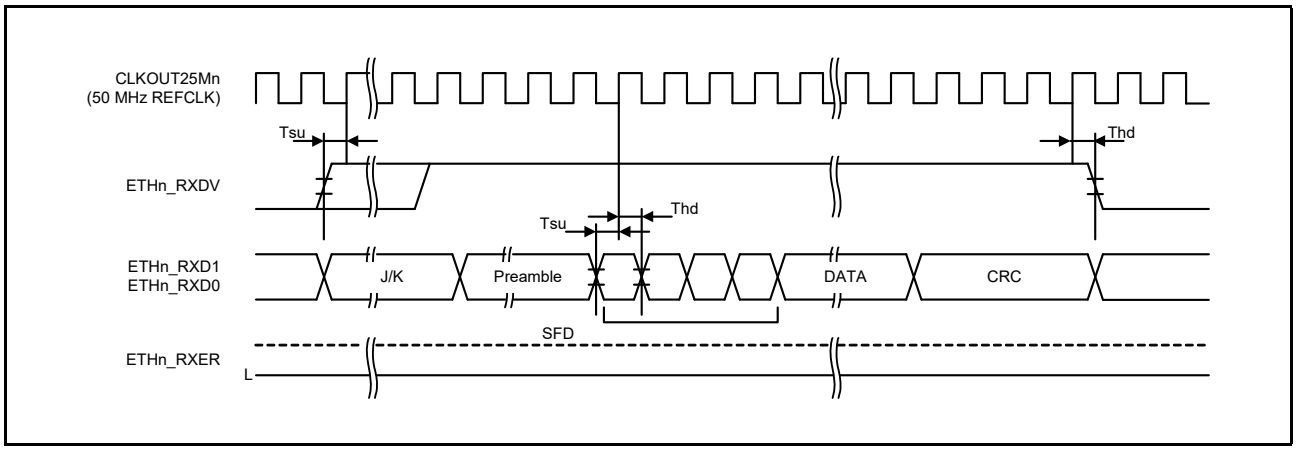


Figure 47.72 RMII Reception Timing (Normal Operation)

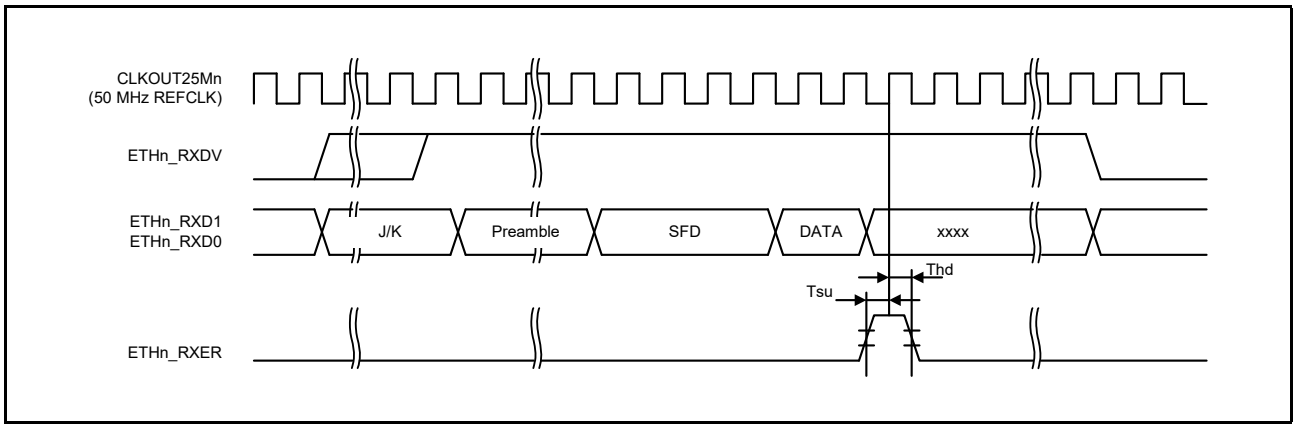


Figure 47.73 RMII Reception Timing (Error Occurrence)

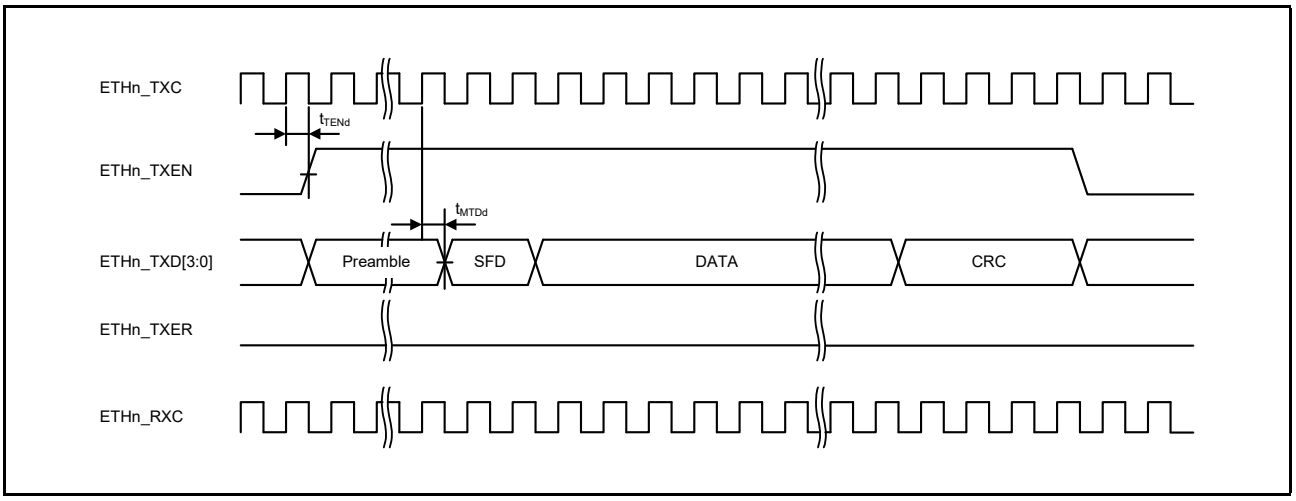


Figure 47.74 MII Transmission Timing

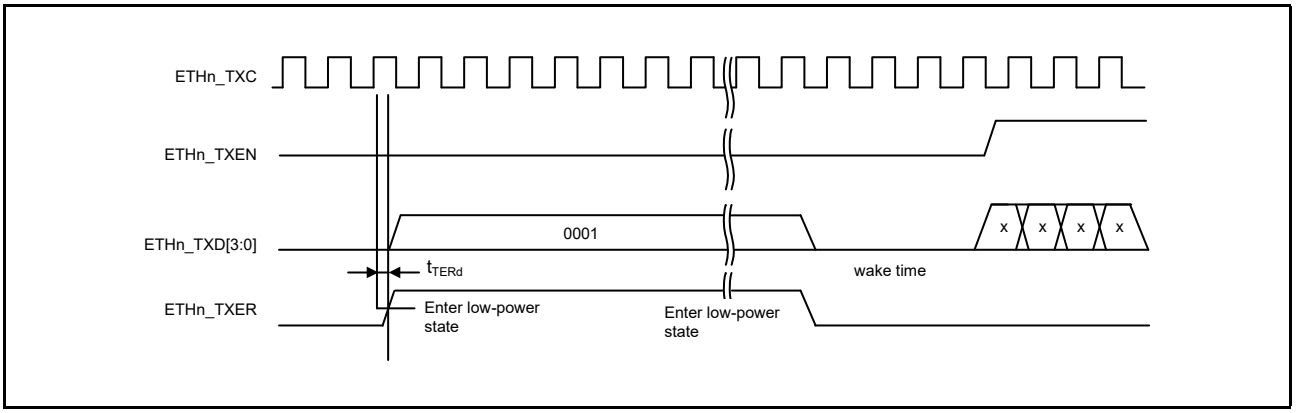


Figure 47.75 MII Transmission Timing

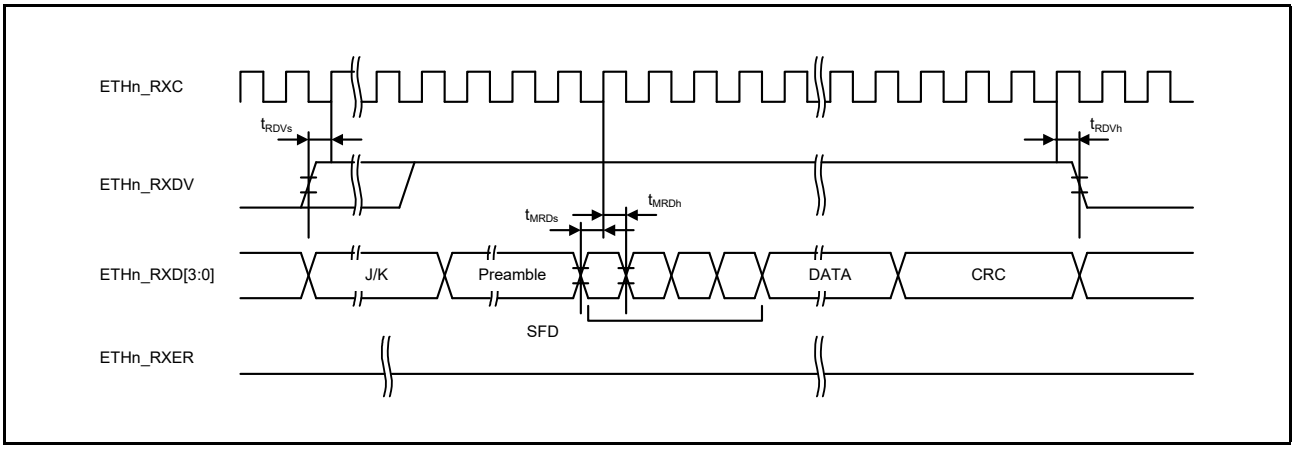


Figure 47.76 MII Reception Timing (Normal Operation)

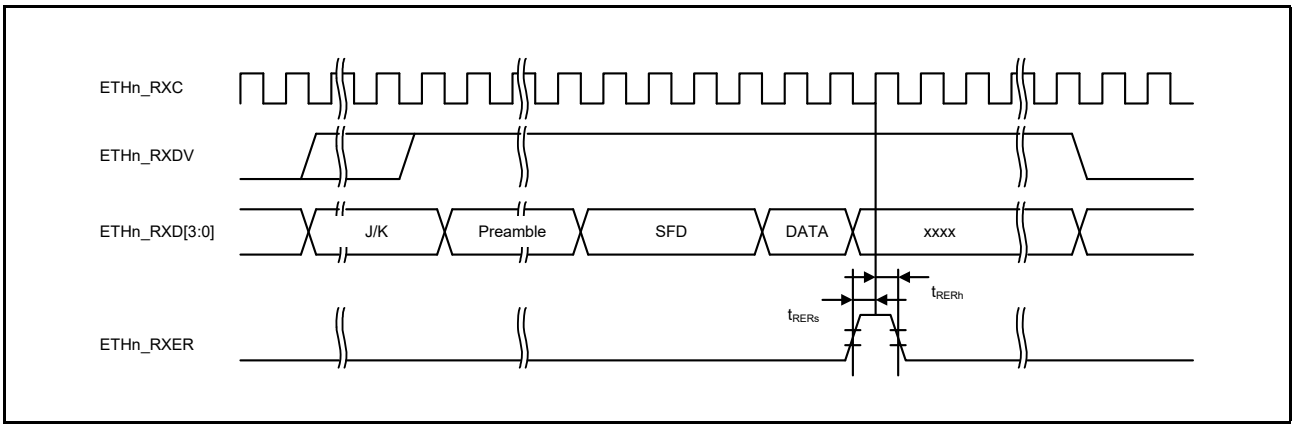


Figure 47.77 MII Reception Timing (Error Occurrence)

47.4.5.15 Serial Management Interface Timing

Table 47.33 Serial Management Interface

Output load conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item		Symbol	min	max	Unit	Test Conditions
MDIO	ETH_MDC output cycle	t_{MDC}	80	—	ns	Figure 47.78
	ETH_MDIO input setting time (to ETH_MDC↑)	t_{SMDIO}	10	—	ns	
	ETH_MDIO input hold time (to ETH_MDC↑)	t_{HMDIO}	0	—	ns	
	ETH_MDIO output delay time (to ETH_MDC↓)	t_{DMDIO}	—	20	ns	

Note: MII2_MDC is the same as for ETH_MDC and the MII2_MDIO is the same as for ETH_MDIO.

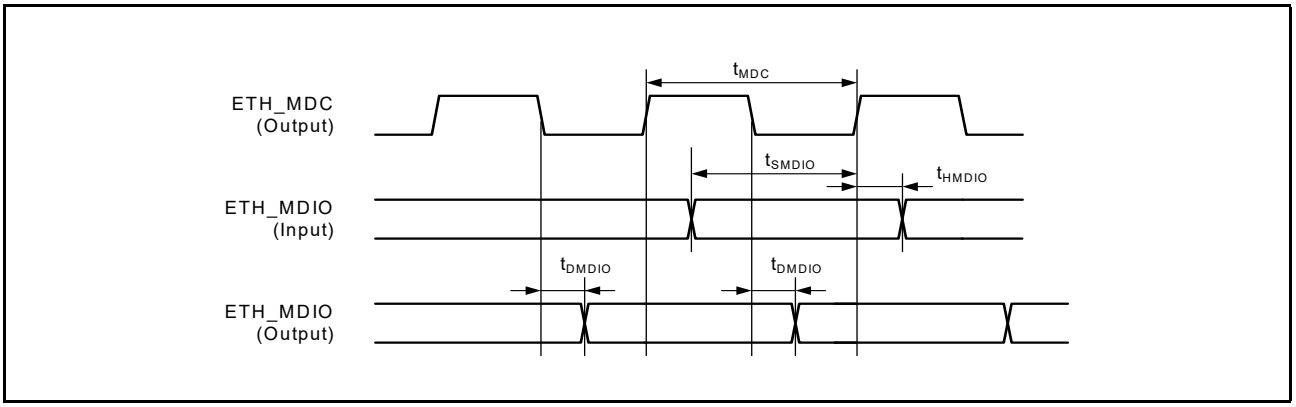


Figure 47.78 Serial Management Access Timing

47.4.5.16 Delta-Sigma Interface Timing

Table 47.34 ΔΣ Interface Timing

Conditions: V_{OH} = VCCQ33 × 0.5, V_{OL1} = VCCQ33 × 0.5, C = 30 pF

Item			Symbol	min	max	Unit	Test Conditions
DSMIF	Clock cycle	Master	t_{DScyc}	1	1	t_{DCcyc}	Figure 47.79
		Slave		40	200	ns	
	Clock high level	Master	t_{DSCKWH}	16	—	ns	
		Slave		16	—	ns	
	Clock low level	Master	t_{DSCKWL}	16	—	ns	
		Slave		16	—	ns	
	Setup time	Master	t_{SU}	15	—	ns	Figure 47.80, Figure 47.81
		Slave		10	—	ns	
	Hold time	Master	t_H	0	—	ns	
		Slave		10	—	ns	

Note: t_{DCcyc}: One cycle time of the ΔΣ interface clock (DSCLK0, DSCLK1)

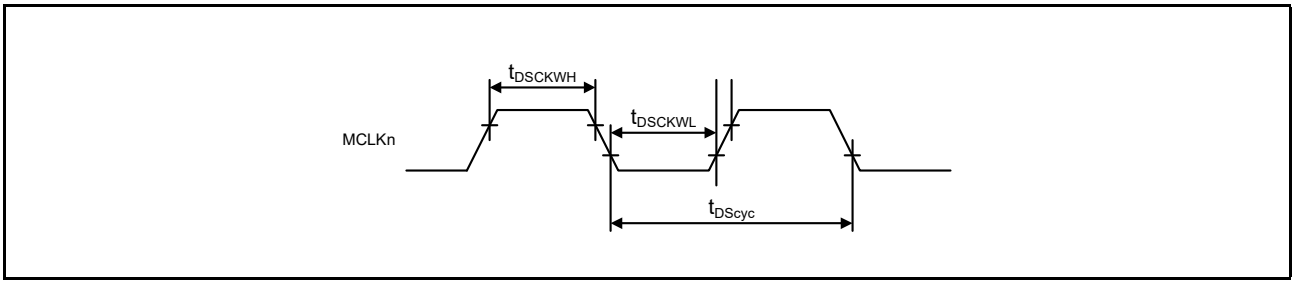


Figure 47.79 Clock Input/Output Timing

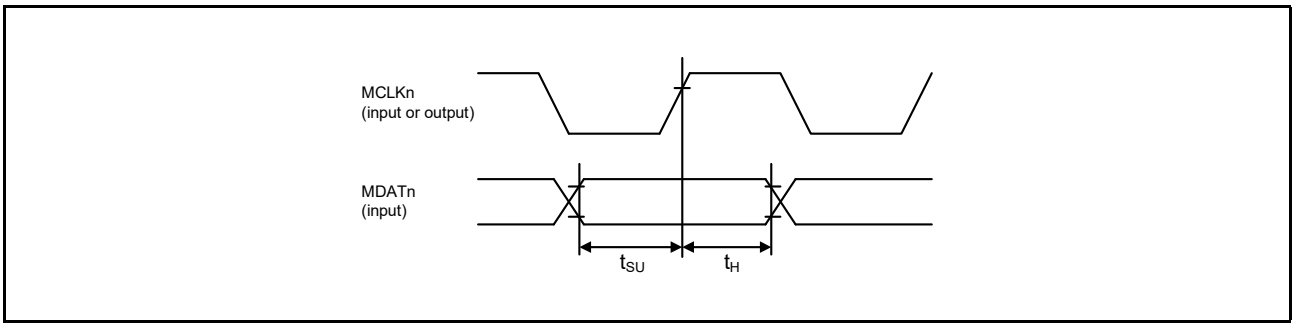


Figure 47.80 Reception Timing (MCLKn Rising Synchronous)

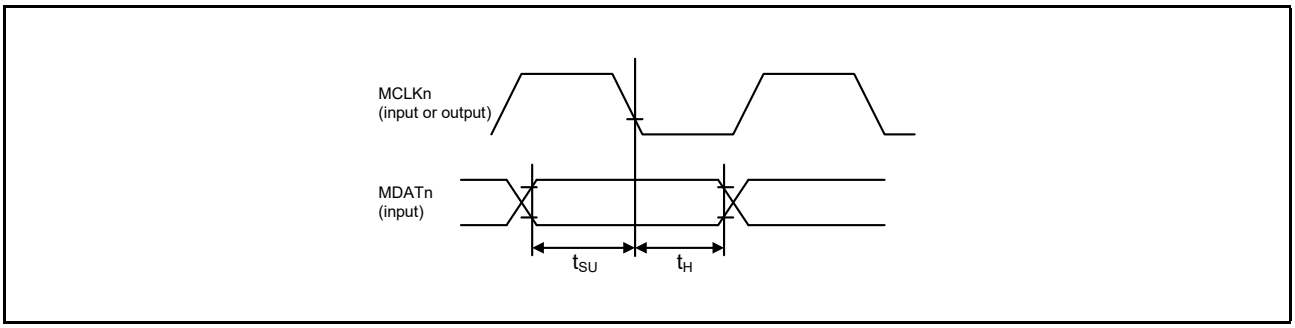


Figure 47.81 Reception Timing (MCLKn Falling Synchronous)

47.5 USB Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = -40 to 125 °C

Note: The 176-pin HLFQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 47.35 On-chip USB Full-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)

Item	Symbol	min	typ	max	Unit	Test Conditions
Rising time	t_{FR}	4	—	20	ns	Figure 47.82
Falling time	t_{FF}	4	—	20	ns	
Rising/falling time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR} / t_{FF}

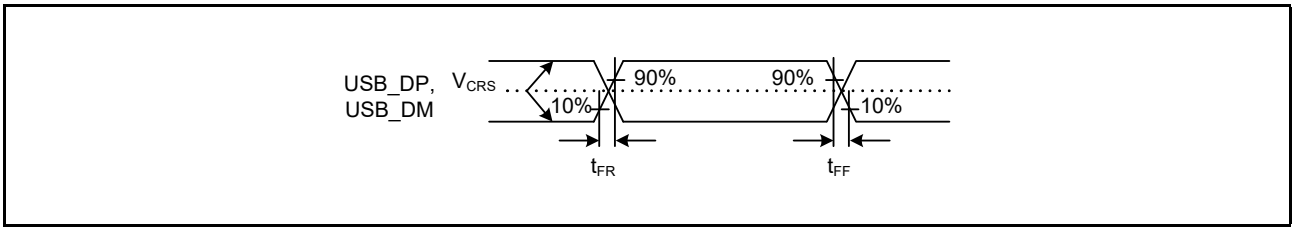


Figure 47.82 USB_DP, USB_DM Output Timing (Full Speed)

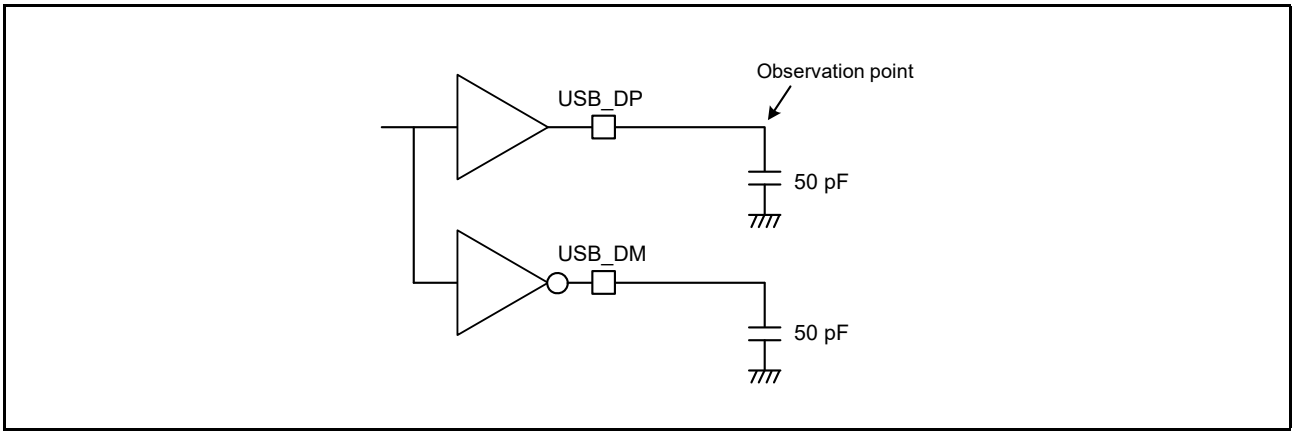


Figure 47.83 Measurement Circuit (Full Speed)

Table 47.36 On-chip USB High-Speed Characteristics (USB_DP, USB_DM Pin Characteristics)

Item		Symbol	min	typ	max	Unit	Test Conditions
AC characteristics	Rising time	t_{HSR}	500	—	—	ps	Figure 47.84
	Falling time	t_{HSF}	500	—	—	ps	
	Output resistance	Z_{HSDRV}	40.5	—	49.5	Ω	

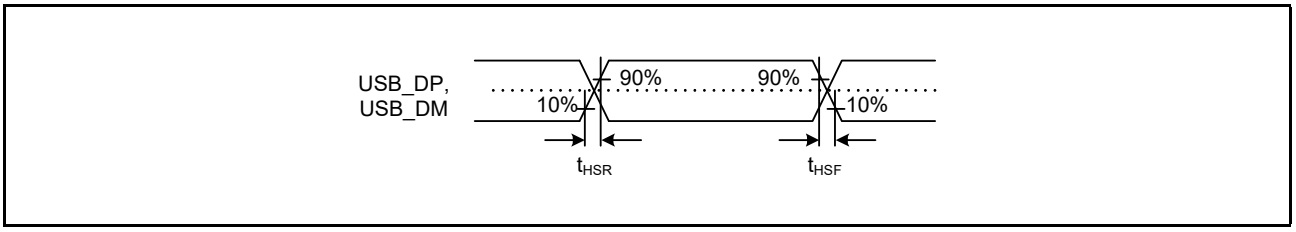


Figure 47.84 USB_DP, USB_DM Output Timing (High Speed)

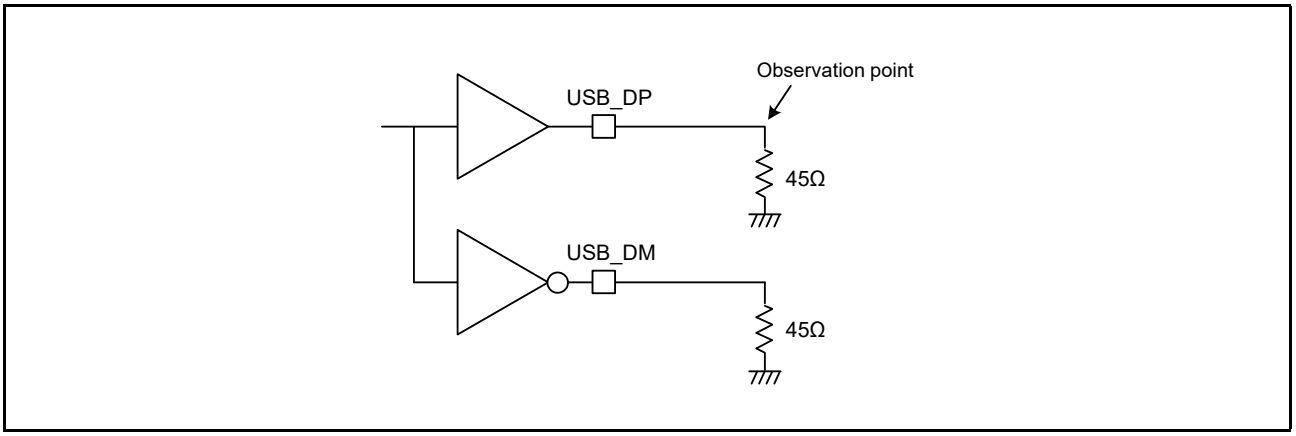


Figure 47.85 Measurement Circuit (High Speed)

47.6 A/D Conversion Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = -40 to 125°C

Note: The 176-pin HLFQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 47.37 12-Bit A/D (Unit 0) Conversion Characteristics

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Analog input capacitance		—	—	30	pF	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is in use	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	1.2 (0.4 + 0.4) *2	—	3.6	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±7.5	LSB	
	Full-scale error	—	—	±7.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±7.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits in use (AN000 to AN003) When disconnection detection assistance is not in use	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	1.2 (0.4 + 0.4) *2	—	3.6	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 24 states
	Offset error	—	—	±6.5	LSB	
	Full-scale error	—	—	±6.5	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.5	LSB	
	DNL differential nonlinearity error	—	—	±3.0	LSB	
	INL integral nonlinearity error	—	—	±4.0	LSB	
	Holding characteristics of sample-and-hold circuits	—	—	3.2	µs	Self-diagnosis + 4-channel simultaneous sampling
	Dynamic range	0.25	—	VREFH0 – 0.25	V	
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN007)	Conversion time*1 (Operation at PCLKF = 60 MHz) Permissible signal source impedance Max. = 1.0 kΩ	0.483 (0.267)*2	—	—	µs	Sampling in 16 states
	Offset error	—	—	±5.0	LSB	
	Full-scale error	—	—	±5.0	LSB	
	Quantization error	—	±0.5	—	LSB	
	Absolute accuracy	—	—	±6.0	LSB	
	DNL differential nonlinearity error	—	—	±2.5	LSB	
	INL integral nonlinearity error	—	—	±3.0	LSB	

Note: The above specified values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 43.31 and Figure 43.32 in section 43, 12-Bit A/D Converter (S12ADCa)). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

Table 47.38 12-Bit A/D (Unit 1) Conversion Characteristics

Item		min	typ	max	Unit	Test Conditions
Resolution		8	—	12	Bit	
Conversion time*1 (Operation at PCLKF = 60 MHz)	Permissible signal source impedance Max. = 1.0 kΩ	0.883 (0.667)*2	—	—	µs	Sampling in 40 states
Analog input capacitance		—	—	30	pF	
Offset error		—	—	±6.0	LSB	
Full-scale error		—	—	±6.0	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	—	±6.0	LSB	
DNL differential nonlinearity error		—	—	±3.0	LSB	
INL integral nonlinearity error		—	—	±4.0	LSB	

Note: The above specified values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time is the total of the sampling time and the comparison time (t_{SPLSH} + t_{CONV} in Figure 43.31 and Figure 43.32 in section 43, 12-Bit A/D Converter (S12ADCa)). The number of sampling states is indicated for each item in Test Conditions.
Note 2. The value in parentheses indicates the sampling time.

47.7 Temperature Sensor Characteristics

- Conditions: VDD = PLLVDD0 = PLLVDD1 = DVDD_USB = 1.14 to 1.26 V,
  VCCQ33 = AVCC0 = AVCC1 = VREFH0 = VREFH1 = VDD33_USB = 3.0 to 3.6 V
  VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V,
  Tj = -40 to 125°C

Note: The 176-pin HLFQFP does not have pins AVCC1, AVSS1, VREFH1, and VREFL1.

Table 47.39 Temperature Sensor Characteristics

Item	min	typ	max	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (at 25°C)	—	1.21	—	V	
Temperature sensor start time	—	—	30	µs	
Sampling time	4.25	—	—	µs	ADSSTRT.SST[7:0] = 255 states (when PCLKF [ADC (unit0) sampling CLK] = 60 MHz)

47.8 Oscillation Stop Detection Timing

Table 47.40 Oscillation Stop Detection Circuit Characteristics

Item	Symbol	min	typ	max	Unit	Test Conditions
Clock switching time	t_{dr}	—	—	1	ms	Figure 47.86

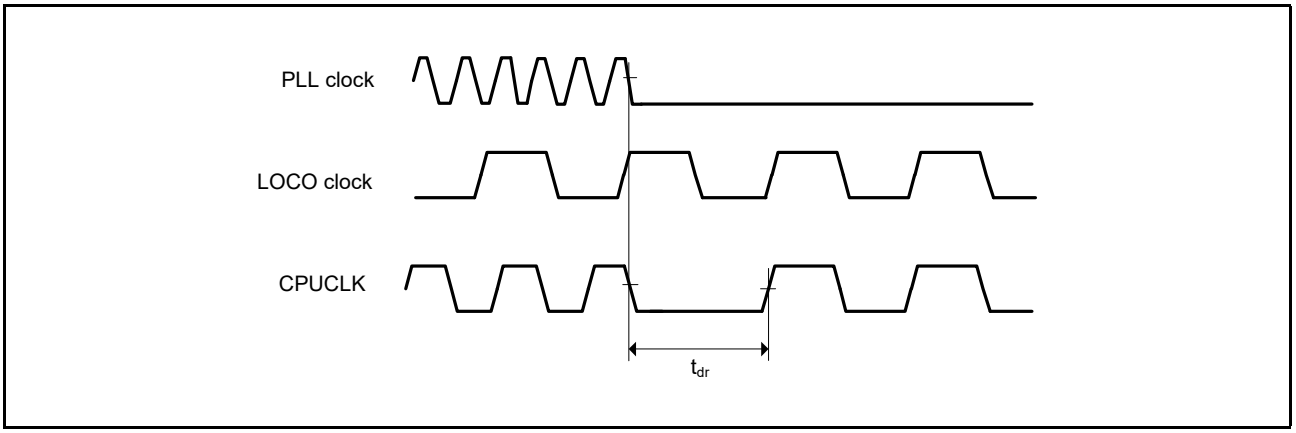


Figure 47.86 Oscillation Stop Detection Timing

47.9 Debug Interface Timing

Table 47.41 Debug Interface Timing

Output load conditions: V_{OH} = VCCQ33 – 0.5 V, V_{OL1} = 0.4 V

Item	Symbol	Min.	Max.	Unit	Reference Figure
TCK cycle time	t_{TCKcyc}	30	—	ns	Figure 47.87
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	5	—	ns	Figure 47.88 Output load: 30 pF
TDI hold time	t_{TDIH}	5	—	ns	
TMS/SWDIO setup time	t_{TMSS}	5	—	ns	
TMS/SWDIO hold time	t_{TMSH}	5	—	ns	
SWDIO delay time	t_{SWDO}	—	15	ns	
TDO delay time	t_{TDOD}	—	15	ns	
Capture register setup time	t_{CAPTS}	5	—	ns	Figure 47.89
Capture register hold time	t_{CAPTH}	5	—	ns	
Update register delay time	$t_{UPDATED}$	—	15	ns	
Trace clock cycle	t_{TCYC}	26.6	—	ns	Figure 47.90 Output load: 15 pF
Trace data delay time	t_{TDT}	0.25 × t_{TCYC} – 2	0.25 × t_{TCYC} + 2	ns	

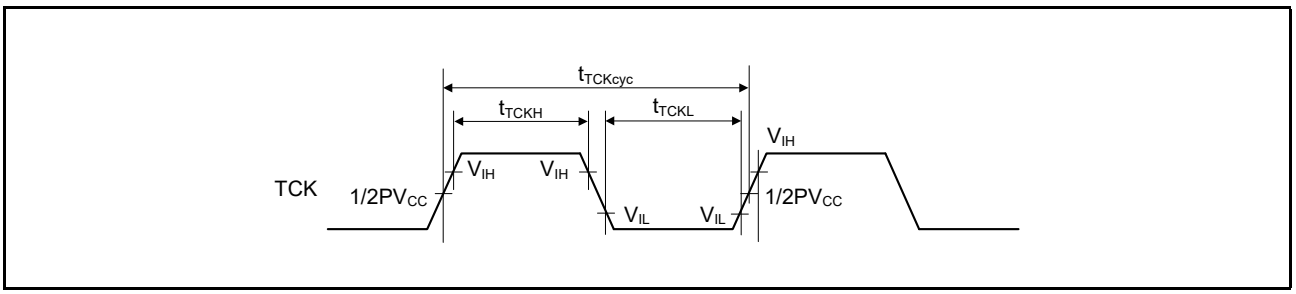


Figure 47.87 TCK Input Timing

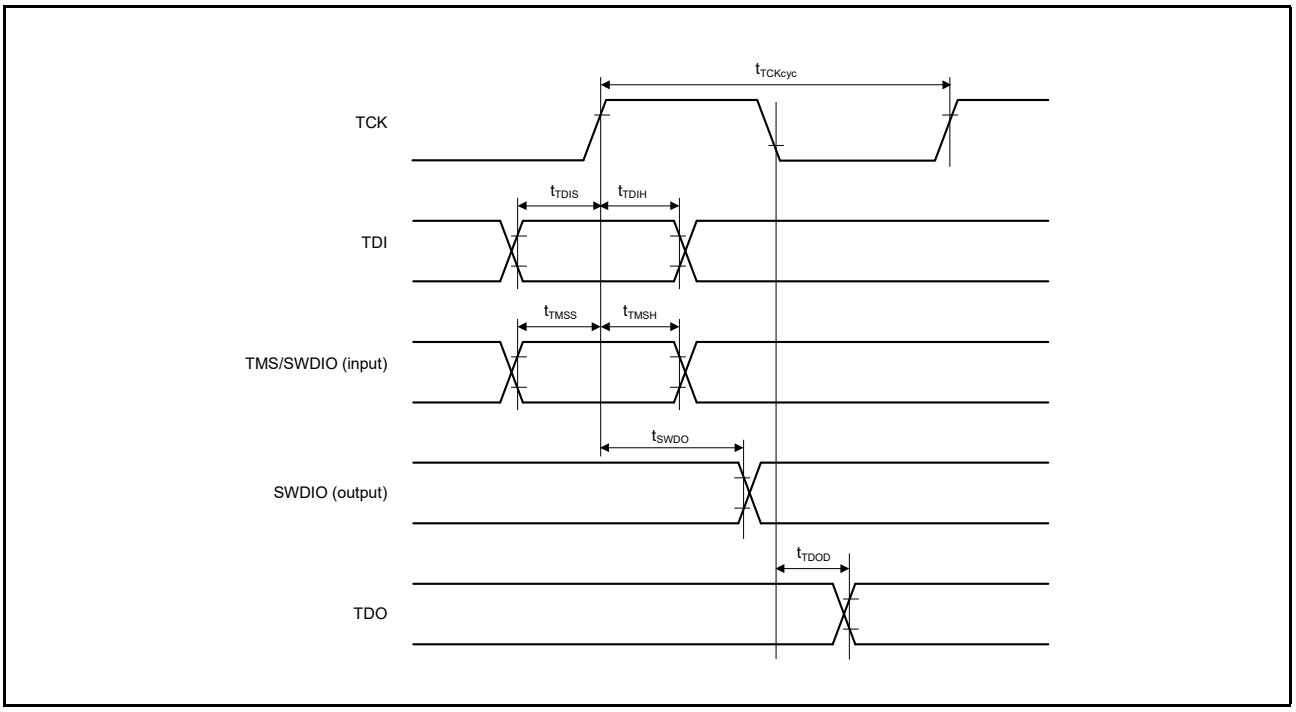


Figure 47.88 Data Transfer Timing

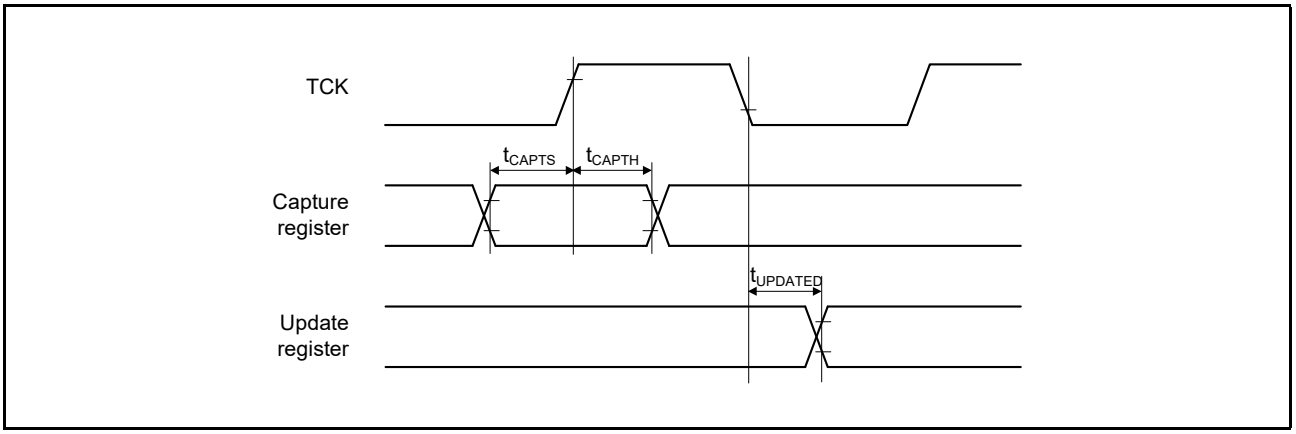


Figure 47.89 Boundary Scan Input/Output Timing

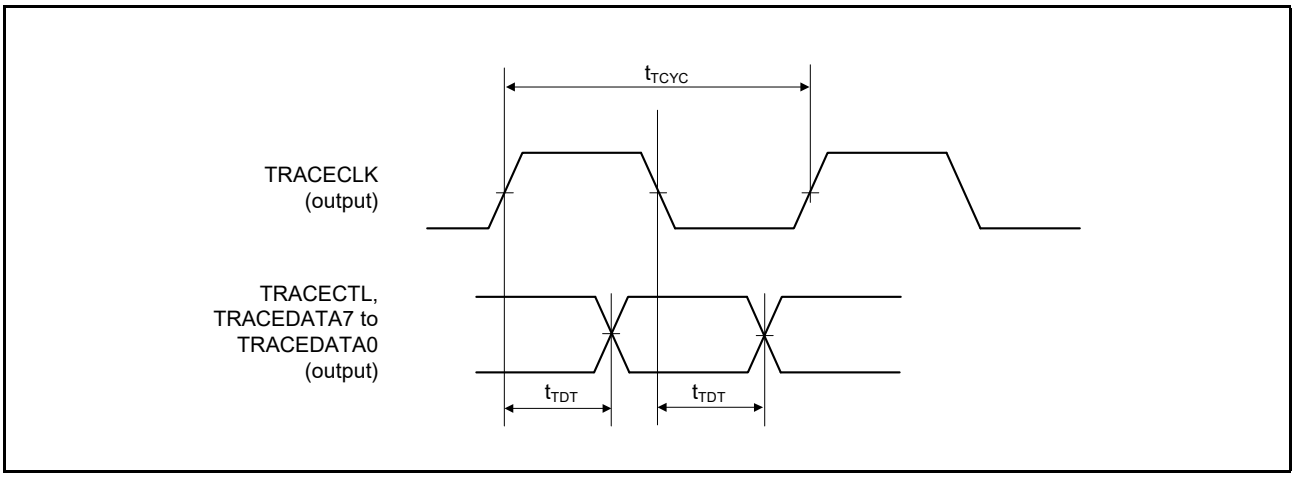
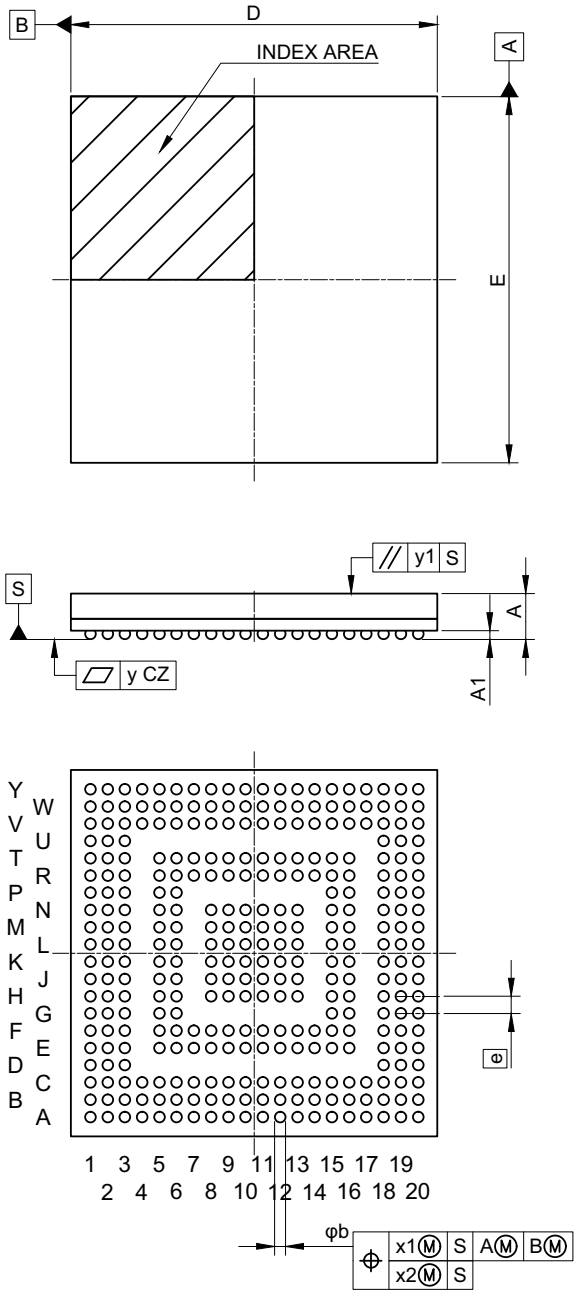


Figure 47.90 Trace Interface Timing

Appendix 1. Outer Dimensions Diagram

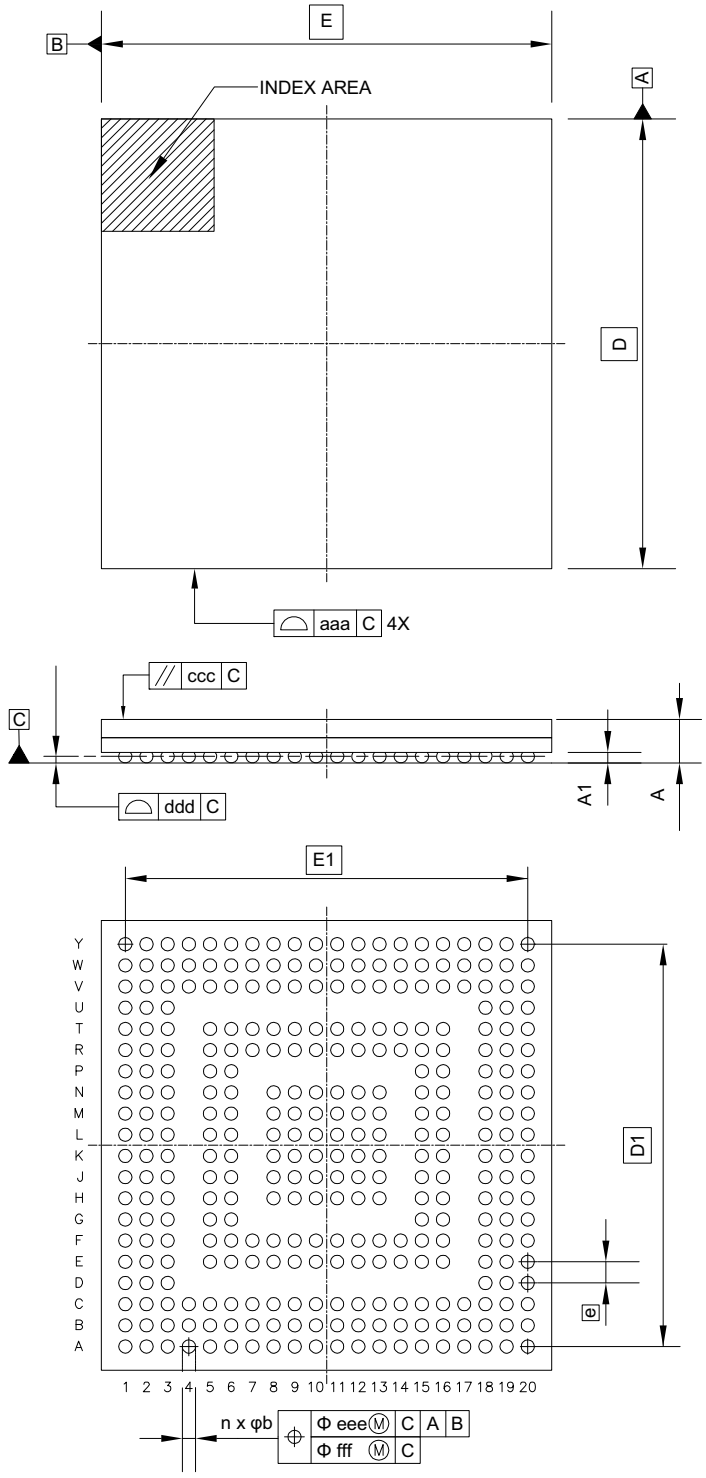
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA320-17x17-0.80	PRBG0320GA-A	-	1.16



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	16.80	17.00	17.20
E	16.80	17.00	17.20
A	—	—	2.30
A1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x1	—	—	0.20
x2	—	—	0.08
y	—	—	0.10
y1	—	—	0.20

Figure A 320-Pin FBGA (PRBG0320GA-A)

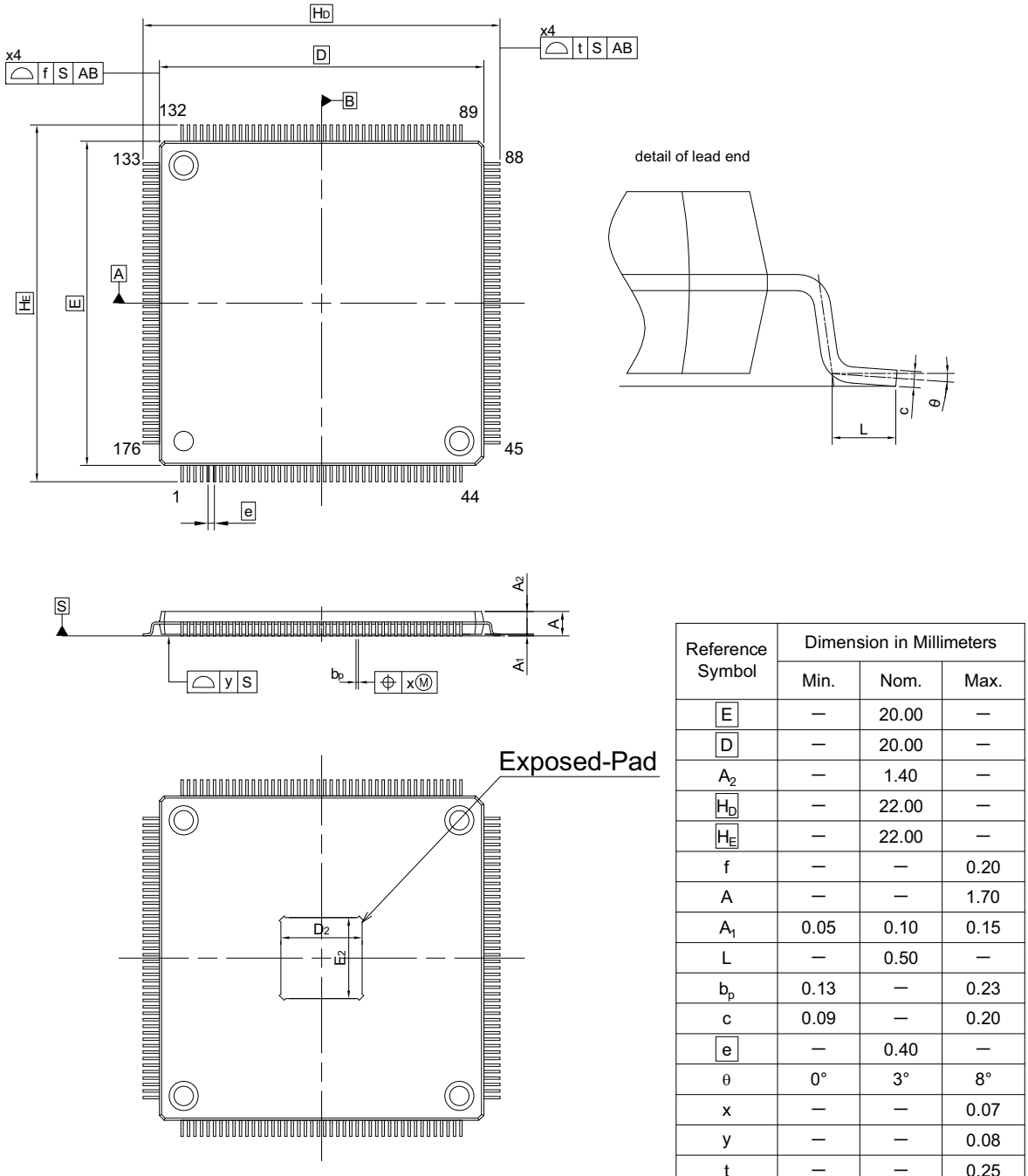
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFBGA320-17x17-0.80	PRBG0320GB-A	0.92



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	17.00	—
E	—	17.00	—
D1	—	15.20	—
E1	—	15.20	—
A	—	—	1.75
A1	0.35	—	—
b	0.45	0.50	0.55
e	—	0.80	—
aaa	—	—	0.20
ccc	—	—	0.20
ddd	—	—	0.12
eee	—	—	0.20
fff	—	—	0.08
n	—	320	—

Figure B 320-Pin FBGA (RBG0320GB-A)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HLFQFP176-20x20-0.40	PLQP0176LD-A	1.32



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
E	—	20.00	—
D	—	20.00	—
A_2	—	1.40	—
H_D	—	22.00	—
H_E	—	22.00	—
f	—	—	0.20
A	—	—	1.70
A_1	0.05	0.10	0.15
L	—	0.50	—
b_p	0.13	—	0.23
c	0.09	—	0.20
e	—	0.40	—
θ	0°	3°	8°
x	—	—	0.07
y	—	—	0.08
t	—	—	0.25
D_2	—	5.00	—
E_2	—	5.00	—

Figure C 176-Pin HLFQFP (PLQP0176LD-A)

REVISION HISTORY — RZ/T1 Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.60	Nov. 14, 2014	—	First edition, issued
0.70	Dec. 25, 2014	Features	
		53	■ Operating temperature range: Heading title and description corrected
		Section 1 Overview	
		63	Table 1.3 List of Products (2 / 2): Note corrected
		73	Figure 1.3 Pin Arrangement (176-pin HLQFP): The names of pins 33, 34, 38, 39, and 91, corrected
		78	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): The names of pins M20 and P19, corrected
		79	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): The names of pins R14, R19, R20, T9, V7, and V8, corrected
		81	Table 1.5 Pin Assignments (320-Pin FBGA) (8 / 8): The names of pins Y16 and Y17, corrected
		82	Table 1.6 Pin Assignments (176-Pin HLQFP) (1 / 4): The names of pins 33, 34, 38, and 39, corrected
		83	Table 1.6 Pin Assignments (176-Pin HLQFP) (2 / 4): The names of pins 58, 59, 60, 79, 82, and 83, corrected
		84	Table 1.6 Pin Assignments (176-Pin HLQFP) (3 / 4): The names of pins 91 and 110, corrected
		85	Table 1.6 Pin Assignments (176-Pin HLQFP) (4 / 4): The names of pins 136, 153, 154, 155, 156, and 157, corrected
		91	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (6 / 10): The name of pin M20, corrected
		92	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): The names of pins P19, R8, and R14, corrected
		93	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): The names of pins R19, R20, T9, V7, and V8, corrected
		94	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): The names of pins Y16 and Y17, corrected
		Section 4 Address Space	
		122	4.1 Address Space: Description corrected
		123	Figure 4.1 Memory Map: The description of the figure and Note 1, corrected
		Section 5 I/O Registers	
		199	Table 5.1 List of I/O Registers (Address Order) (73 / 86): The addresses and module symbols of ADCMPANSER and ADCMPLER, corrected. The ADCMPANSER and ADCMPLER lines, moved next to the ADCMPCR line.
		Section 7 Clock Generation Circuit	
		220	Table 7.1 Specifications of Clock Generation Circuit: Description of Frequency multiplication ratio at PLL0 circuit, corrected
		221	Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (1 / 2): The frequency of USB clock M (USBMCLK), corrected
		226, 227	7.2.1 System Clock Control Register (SCKCR): In the bit chart and the table of bits, bit 17 corrected to reserved
		Section 10 Debugging Interface	
		264	Figure 10.1 CoreSight Configuration Diagram, corrected

Rev.	Date	Description	
		Page	Summary
0.70	Dec. 25, 2014	265	Figure 10.2 CoreSight Configuration Diagram (in Products Incorporating an R-IN Engine), corrected
		Section 12 Interrupt Controller (ICUA)	
		286	12.2.4 Non-maskable Interrupt Status Register (NMISR): In the bit chart, the name of bit 0 corrected
		355	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (2 / 9): The source of vector number 63, corrected
		358	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (5 / 9): The source of vector number 169, corrected
		361	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (8 / 9): Vector Number 253 corrected to reserved
		Section 14 Bus State Controller	
		410	14.4.4 Refresh Timer Control/Status Register (RTCSR): In the table of bits, the symbol of bit 7 corrected
		Section 15 DMA Controller (DMACAa)	
		475	Table 15.1 Specifications of DMAC: Description of Interrupt request, corrected
		507	15.3.22 Descriptor Interval Register n (DSCITVL_X (X = A or B)): Functional description of the DITVL bit, corrected
		532	15.4.3.2 Round-Robin Mode: Description corrected
		534	Table 15.20 Method of Detecting DMA Transfer Request Signals: Description of Edge detection, corrected
		564	Table 15.29 DMA Transfer Setting Example 4 (Descriptor 1): Table header corrected (Item → Description)
		565	Table 15.30 DMA Transfer Setting Example 4 (Descriptor 2): Data size, corrected (64 bits → 256 bits)
		566	Table 15.32 Descriptor Settings: Descriptor 1, Descriptor 2, and Descriptor 3 of CFG (Configuration) corrected
		Section 17 I/O Ports	
		609	17.3.1 Port Direction Register (PDR): The erroneous description on the address, corrected
		Section 19 Multi-Function Timer Pulse Unit (MTU3a)	
		693	Table 19.6 TPSC[2:0] and TPSC2[2:0] (MTU0), corrected
		871	Table 19.78 MTU Interrupt Sources: TCIV4 and TCIV7 interrupt sources, corrected
		Section 20. Port Output Enable 3 (POE3)	
		959	20.2.20 MTU3 Pin Select Register (M3SELR): In the table of bits, the names of bits M3BSEL[3:0] and M3DSEL[3:0], corrected
		960	20.2.21 MTU4 Pin Select Register 1 (M4SELR1): In the table of bits, the names of bits M4ASEL[3:0] and M4CSEL[3:0], corrected
		961	20.2.22 MTU4 Pin Select Register 2 (M4SELR2): In the table of bits, the names of bits M4BSEL[3:0] and M4DSEL[3:0], corrected
		Section 22 16-Bit Timer Pulse Unit (TPUa)	
		1113	22.2.2 Timer Mode Register (TMDR): Note 3 and Note 4 corrected
		1153	Table 22.25 PWM Output Registers and Output Pins Register: Description in the Register column, corrected

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		Page	Summary
0.70	Dec. 25, 2014	Section 28 Ethernet MAC (ETHERC)	
		1310	Table 28.3 MAC Function Selection Method (for Products Incorporating an R-IN Engine): Media I/F Port 2 at MAC[2:0] = 001 or 101, corrected
		1310	Table 28.4 MAC Function Selection Method: Media I/F Port 1 at MAC[2:0] = 011, corrected
		1331	28.2.2.17 LPI CLIENT Timing Control Register (GMAC_LPI_TIMING): In the bit chart, the value after reset for bits 13, 11, 6, 5, 3, and 2, corrected
		Section 29 Ethernet Switch	
		1354	29.2.1.3 Ethernet Switch Operating Mode Setting Register (ETHSWMD): Note deleted. In the bit chart, bits 2 and 0 corrected to reserved
		1395	29.2.5.8 Generate Timer Periodic Event Register (ATIME_EVT_PERIOD): In the bit chart, the value after reset for bits 29, 28, 27, 25, 24, 23, 20, 19, 17, 15, 14, 11, and 9, corrected
		Section 30 EtherCAT Slave Controller (Only for Products Incorporating an R-IN Engine)	
		1464	30.4.2 Revision Register (REVISION): In the bit chart, the value after reset for bits 1 and 0, corrected
		Section 31 USB2.0HS Host Module (USBh)	
		1637	31.5.1 Externally Supplied Clocks: Description corrected
		1638	Figure 31.6 Clock Distribution Diagram, corrected (HOST clock, HCLK_ROOT, PHYDCLK48, and PHYDCLK60, deleted)
		1642	31.6.3 Time Required to Clear Interrupt Signals, (1) Host Logic: Description corrected
		Section 33 Serial Communications Interface with FIFO (SCIFA)	
		1766	33.3.10 FIFO Control Register (FCR): register contents table, Functional description of RFRST and TFRST, corrected
		Section 34 I^2C Bus Interface (RIIC)	
		1829	34.2.14 I^2C Bus Bit Rate High-Level Register (ICBRH): Note 1 corrected
		1830	Table 34.5 Examples of ICBRH/ICBRL Settings for Transfer Rate: Contents of the table corrected. The erroneous description on the Note, corrected.
		Section 42 Error Control Module (ECM)	
		2250	Table 42.2 ECM Error Input (1 / 2): Module and Function for Error Source Numbers 1 to 3, corrected
		2254	42.2.3 ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0 (m = M or C)): Functional description of ECMmSSE000, ECMmSSE001, and ECMmSSE002 corrected
		2285	42.2.23 ECM Protection Command Register (ECMPCMD1): The table of bits, corrected (Symbol, Bit Name, and Description of bits 7 to 0 and bits 31 to 8, exchanged)
		2308	42.3.4.1 Protection Unlock Sequence: The description of procedure 3, corrected
		Section 43 12-Bit A/D Converter (S12ADCa)	
		2348	43.2.18 A/D Compare Channel Select Extended Register (ADCMPANSER): Address corrected
		2350	43.2.20 A/D Compare Level Extended Register (ADCMPLER): Address corrected
		Section 46 RAM (Product Option)	
		2427	Table 46.1 Specifications of RAM: The description of the “Item” column, corrected
		2428	46.2.1 Protect Command Register (RAMPCMD): Address corrected
		2430	46.2.3 ECC Decoder Configuration Register (RAMEDC) (for Products Incorporating an R-IN Engine): Address corrected
		2433	46.2.5 ECC Encoder Configuration Register (RAMEEC) (for Products Incorporating an R-IN Engine): Address corrected

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		Page	Summary
0.70	Dec. 25, 2014	2437	46.2.7 2-Bit ECC Error Status Register (RAMDBEST) (for Products Incorporating an RIN Engine): Address corrected
		2439	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine): Address corrected
		2440	46.2.10 2-Bit ECC Error Counter Register (RAMDBECNT): Address corrected
		2441 to 2443	46.3 Description of Operation, added
		Section 47 Electrical Characteristics (Target)	
		2444	Table 47.1 Absolute Maximum Rating Conditions: VSS = PLLVSS0 = PLLVSS1 = AVSS0 = AVSS1 = VREFL0 = VREFL1 = VSS_USB = 0 V, corrected (Operating temperature (Junction temperature))
		2504	Table 47.32 ETHERC Timing Output load conditions: VOH = 2.0 V, VOL1 = 0.8 V, C = 25 pF (RMII), VOH = VCCQ33 × 0.5, VOL1 = VCCQ33 × 0.5, C = 30 pF (MII), corrected. The lines of ETHn_CRS setup time, ETHn_CRS hold time, ETHn_COL setup time, and ETHn_COL hold time, deleted.
		2506	Figure 47.72 MII Transmission Timing (Normal Operation), corrected (t_{CRSc} and t_{CRSh} deleted)
		2506	Figure 47.73 MII Transmission Timing (Conflict Occurrence), corrected (t_{COLs} and t_{COLh} deleted)
0.80	Apr. 21, 2015	All	Module name modified: ICU-M → ICUMB
		All	Configuration of the input/output pins unified
		Section 1 Overview	
		66 to 72	1.4 Pin Functions, pin name: PHYLINK2, deleted
		74	Figure 1.3 Pin Arrangement (176-pin HLQFP), pin name: ERROROUT corrected to ERROROUT#
		75 to 82	Table 1.5 Pin Assignments (320-Pin FBGA), pin names changed (MOSIn_BLUE → MOSIn, MOSIn_RED → MOSIn)
		77	Table 1.5 Pin Assignments (320-Pin FBGA), pin number H5: pin name ERROROUT corrected to ERROROUT#
		77	Table 1.5 Pin Assignments (320-Pin FBGA), pin number H18: pin name MDAT2 added
		80	Table 1.5 Pin Assignments (320-Pin FBGA), pin number R8: pin names WE0# and DQMLL deleted
		80	Table 1.5 Pin Assignments (320-Pin FBGA), pin number T8: pin name A1 deleted
		83 to 86	Table 1.6 Pin Assignments (176-Pin HLQFP), pin names changed (MOSIn_BLUE → MOSIn, MOSIn_RED → MOSIn)
		83	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 1: pin name CATI2CCLK deleted
		83	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 7: pin name ERROROUT corrected to ERROROUT#
		84	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 56: pin names WE0# and DQMLL deleted
		84	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 57, pin name A1 deleted
		84	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 89: pin name ADTRG1 deleted
		85	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 121, pin name MDAT2 added
		86	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 168: pin names CATSYNC1 and CATLATCH1 deleted
		86	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 171: pin names CATSYNC0 and CATLATCH0 deleted
		86	Table 1.6 Pin Assignments (176-Pin HLQFP), pin number 176, pin name CATI2CDATA deleted
		87 to 96	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin names changed (MOSIn_BLUE → MOSIn, MOSIn_RED → MOSIn)
		87	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin number A12, Power Supply Clock System Control: VSS added
		90	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin number F7, Power Supply Clock System Control: VCCQ33 added

Rev.	Date	Description	
		Page	Summary
0.80	Apr. 21, 2015	90	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin number H5, Power Supply Clock System Control: ERROROUT corrected to ERROROUT#
		94	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin number T2, Power Supply Clock System Control: VDD33_USB added
		97 to 102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin names changed (MOSIn_BLUE → MOSIn, MOSIn_RED → MOSIn)
		97	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), ECATC deleted from the header of Communication
		97	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 1, CATI2CCLK in the Communication column deleted
		97	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 7, Power Supply Clock System Control: ERROROUT corrected to ERROROUT#
		98	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 56, WE0# and DQMLL in the Bus column deleted
		98	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 57, A1 in the Bus column deleted
		98	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 58, D1 in the Bus column deleted
		98	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 59, D2 in the Bus column deleted
		98	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 60, D3 in the Bus column deleted
		99	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 79, D4 in the Bus column deleted
		99	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 82, D5 in the Bus column deleted
		99	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 83, D6 in the Bus column deleted
		99	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 89, ADTRG1 in the S12ADC column deleted
		100	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 110, D7 in the Bus column deleted
		102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 168, CATSYNC1 and CATLATCH1 in the Communication column deleted
		102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 171, PHYRESETOUT#, CATSYNC0, and CATLATCH0 in the Communication column deleted
		102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), pin number 176, CATI2CDATA in the Communication column deleted
		102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP), Note 1 deleted
		Section 4 Address Space	
		124	Figure 4.1 Memory Map: Note 8. added to the peripheral I/O register (1 MB) of the Cortex-M3 (in products incorporating an R-IN Engine)
		124	Figure 4.1 Memory Map: Note 8. and Note 9. added
		125	Figure 4.2 Memory Map: Note 5. added
		126	Figure 4.3 Memory Map: Note 6. added
		Section 5 I/O Registers	
		127	(1) I/O register addresses (address order): Description on the number of access cycles, deleted
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0000h, Register Name: PCI Configuration Registers for OHCI Register Symbol: VID_DID was changed to VID_DID_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0000h, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: VID_DID was changed to VID_DID_A.

Rev.	Date	Description	
		Page	Summary
0.80	Apr. 21, 2015	151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0004h, Register Name, PCI Configuration Registers for OHCI Register Symbol: CMND_STS was changed to CMND_STS_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0004h, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: CMND_STS was changed to CMND_STS_A.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0008h, Register Name: PCI Configuration Registers for OHCI Register Symbol: REVID_CC was changed to REVID_CC_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0008h, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: REVID_CC was changed to REVID_CC_A.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 000Ch, Register Name: PCI Configuration Registers for OHCI Register Symbol: CLS_LT_HT_BIST was changed to CLS_LT_HT_BIST_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 000Ch, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: CLS_LT_HT_BIST was changed to CLS_LT_HT_BIST_A.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0010h, Register Name: PCI Configuration Registers for OHCI Register Symbol: BASEAD was changed to BASEAD_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0010h, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: BASEAD was changed to BASEAD_A.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 0018h, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: WIN2_BASEAD, deleted
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 002Ch, Register Name: PCI Configuration Registers for OHCI Register Symbol: SVID_SSID was changed to SVID_SSID_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 002Ch, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol: SVID_SSID was changed to SVID_SSID_A.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 003Ch, Register Name: PCI Configuration Registers for OHCI Register Symbol: INTR_LINE_PIN was changed to INTR_LINE_PIN_0.
		151	Table 5.1 List of I/O Registers (Address Order) Address: A005 003Ch, Register Name: PCI Configuration Registers for AHB-PCI Bridge Register Symbol, INTR_LINE_PIN was changed to INTR_LINE_PIN_A.
		152	Table 5.1 List of I/O Registers (Address Order) Address: A005 0804h, Register Name: PCIAHB_WIN2_CTR Register Symbol: PCIAHB_WIN2_CTR, deleted
		Section 6 Reset	
		217	6.2.2 Software Reset Register (SWRR1), bit chart: SWRR1 corrected
		218	6.2.3 Software Reset Register 2 (SWRR2) (for products incorporating an R-IN engine), bit chart: SWRR2 corrected
		Section 7 Clock Generation Circuit	
		229	7.2.2 System Clock Control Register 2 (SCKCR2): Value after reset of b4 in the bit chart, changed
		230	7.2.3 Delta-Sigma Interface Clock Control Register (DSCR): Value after reset of b16 and b4 in the bit chart, changed
		241	7.8.8 High-Speed Serial Clock (SERICLK): Description changed

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0.80	Apr. 21, 2015	Section 8 Clock Monitor Circuit (CLMA)	
		245	Table 8.1 Specifications of CLMAn (n = 2 to 0): Table title changed
		246	Figure 8.1 Block Diagram of CLMAn (n = 2 to 0): Description was added to the top of the figure.
		246	Figure 8.1 Block Diagram of CLMAn (n = 2 to 0): Figure title changed
		Section 9 Low-Power Consumption Function	
		257	9.2.2 Module Stop Control Register B (MSTPCRB): Bit name and functional description of b18 in table of bits, changed
		Section 10 Debugging Interface	
		264	10.1 Overview: Description changed
		264	Table 10.1 CoreSight Specifications: Table title changed
		265	Figure 10.1 Block Diagram of CoreSight: Figure title changed
		266	Figure 10.2 Block Diagram of CoreSight (for products incorporating an R-IN engine): Figure title changed
		269	Table 10.8 Configuration of Pins for the Debugging Interface: Description on the top was changed.
		269	Table 10.8 Configuration of Pins for the Debugging Interface: Table title changed
		270	10.2.1 Debugging Interface Control Register (DBGIFCNT) Symbol: SWVSEL was changed in the bit chart.
		276	10.3.5.2 Example Connection of the emulator That Can Drive the nTRST Output to High: Description changed
		276	Figure 10.8 Example of Connection Circuit of an emulator That Can Drive the nTRST Output to High: Figure number changed
		Section 12 Interrupt Controller (ICUA)	
		281	12.1 Overview: Description changed
		281	Table 12.1 Specifications of Interrupt Controller: Table title changed
		282	Figure 12.1 Block Diagram of Interrupt Controller: Figure title changed
		282	Figure 12.2 Block Diagram of Interrupt Controller (for products incorporating an R-IN engine): Figure title changed
		282	Figure 12.2 Block Diagram of Interrupt Controller (for products incorporating an R-IN engine): Interrupt sources, changed
		339	12.4.2.13 Interrupt Address Register (HVA0) Symbol: HVA in the bit chart, changed
		354	12.4.3.1 Interrupt Vector Table: Description changed
		354	12.4.3.1 Interrupt Vector Table, Cortex-R4F/DMAC interrupt vector table: Description of the detection type, changed
		355-364	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table: Note 3. added
		372	Figure 12.10 Concept of Multiple Interrupts (2/2): Note 1. changed to Note 2. in interrupt request u (level 2)
		376	12.5.2.1 Interrupt Vector Table for CM3: Description changed
		Section 13 Internal Buses	
		381	Table 13.1 Specifications of Internal Buses: Buses for Ethernet in the internal bus type column, changed
		381	Table 13.1 Specifications of Internal Buses: Note added
		382	Figure 13.1 Bus Configuration: “AHB2DMA” deleted
		382	Figure 13.1 Bus Configuration: “RAM1” changed to “RAM2”, “RAM2” changed to “RAM1”
		382	Figure 13.1 Bus Configuration: Note added to “RAM”1 and “RAM2”
		383	Figure 13.2 Bus Configuration (for products incorporating an R-IN engine): “AHB2DMA” deleted
		383	Figure 13.2 Bus Configuration (for products incorporating an R-IN engine): Note added to “I-RAM” and “D-RAM”

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0.80	Apr. 21, 2015	383	Figure 13.2 Bus Configuration (for products incorporating an R-IN engine): Note added to “I-RAM” and “D-RAM”
		Section14 Bus State Controller	
		385	Table 14.1 Bus State Controller Specifications, External WAIT pin corrected to External WAIT# pin
		386	Figure 14.1 Block Diagram of Bus State Controller, description above the figure corrected
		—	14.2 Input/Output Pins, deleted
		387	Table 14.2 Input/Output Pins of the Bus State Controller, title corrected
		400	14.4.2(1) • CS5WCR: CS5WCR bit table, functional description of b1, 0 and b12, 11, corrected
		420	Table 14.6 16-Bit External Device Access and Data Alignment in Little Endian, entries in the Operation column corrected
		430	14.4.5 MPX-I/O Interface, description corrected
		430	Figure 14.11 Access Timing for MPX Space (1) (Address Cycle No Wait, 1.5 Assertion Delay States, Data Cycle No Wait, 1.5 Delay States), title corrected
		431	Figure 14.12 Access Timing for MPX Space (2) (Address Cycle No Wait, 1.5 Assertion Delay States, Data Cycle No Wait, 1.5 Delay States), added
		432	Figure 14.13 MPX Access Timing for MPX Space (3) (Address Cycle Access Wait 1, Data Cycle No Wait), title corrected
		433	Figure 14.14 MPX Access Timing for MPX Space (4) (Address Cycle Access Wait 1, Data Cycle Wait 1, External Wait 1), title corrected
		450	14.5.6(4) Single Read, description corrected
		452	14.5.6(6) Single Write, description corrected
		476	Table 14.24 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types, the number of cycles in the table corrected
		476	Table 14.24 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types, Note 1 added
		Section 15 DMA Controller (DMACAa)	
		—	Heading title: 15.2 Input/Output Pins, deleted
		479	Table 15.2 Pin Configuration of the DMAC: Description was added to the top of the table.
		479	Table 15.2 Pin Configuration of the DMAC: Table title changed
		480	15.2.1 • For N0SA_n_N and N1SA_n_N (normal mode) Symbol: SA in the bit chart, changed
		481	15.2.1 • For N0SA_n_W and N1SA_n_W (write-only mode) Symbol: WD in the bit chart, changed
		482	15.2.2 Next Destination Address Register n (N0DA_n and N1DA_n) Symbol: DA in the bit chart, changed
		483	15.2.3 Next Transaction Byte Register n (N0TB_n and N1TB_n) Symbol: TB in the bit chart, changed
		484	15.2.4 Current Source Address Register (CRSA_n) Symbol: CRSA in the bit chart, changed
		485	15.2.5 Current Destination Address Register (CRDA_n) Symbol: CRDA in the bit chart, changed
		486	15.2.6 Current Transaction Byte Register (CRTB_n) Symbol: CRTB in the bit chart, changed
		494	15.2.11 Common Control Register (CMNCR): Value after reset of b3 in the bit chart, changed
		494	15.2.11 Common Control Register (CMNCR): Functional description of b3 in the bit chart, changed
		497	15.2.13 Channel Configuration Register n (CHCFG_n): Description changed
		501	15.2.15 Next Link Address Register n (NXLA_n) Symbol: NXLA in the bit chart, changed

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0.80	Apr. 21, 2015	502	15.2.16 Current Link Address Register n (CRLA_n) Symbol: CRLA in the bit chart, changed
		503	15.2.17 Source Continuous Register n (SCNT_n) Symbol: SCNT in the bit chart, changed
		504	15.2.18 Source Skip Register n (SSKP_n) Symbol: SSKP in the bit chart, changed
		506	15.2.19 Destination Continuous Register n (DCNT_n) Symbol: DCNT in the bit chart, changed
		507	15.2.20 Destination Skip Register n (DSKP_n) Symbol: DSKP in the bit chart, changed
		528	Figure 15.10 header Area: Description changed
		532	15.3.2.1 Single Transfer Mode: Description changed
		532	15.3.2.2 Block Transfer Mode: Description changed
		537	15.3.4 DMA Transfer Request: Description changed
		538 to 543	Table 15.21 DMA Transfer Request Detection Operation Setting Table: Note 2. added to the table heading, AM[2:0]
		538 to 543	Table 15.21 DMA Transfer Request Detection Operation Setting Table: DNA transfer source of DMA transfer request source: MTU3a, changed
		538 to 543	Table 15.21 DMA Transfer Request Detection Operation Setting Table: Note 3. added to CHCHG_n AM[2:0] of DMA transfer source: USB
		538 to 543	Table 15.21 DMA Transfer Request Detection Operation Setting Table: Note 2. and Note 3. added
		544	Figure 15.16 Edge Detection Timing (Rising Edge (HIEN = 1), DACK Output is Active during Reading (REQD = 0)): Figure title changed
		544	Figure 15.17 Edge Detection Timing (Rising Edge (HIEN = 1), DACK Output is Active during Writing (REQD = 1)): Figure title changed
		545	Figure 15.18 Level Detection Timing (High-Level Detection (HIEN = 1), DACK Output is Active during Reading (REQD = 0)): Figure title changed
		545	Figure 15.19 Level Detection Timing (High-Level Detection (HIEN = 1), DACK Output is Active during Writing (REQD = 1)): Figure title changed
		558	15.4.2 DMA Transfer Completion Interrupts: Description changed
		558	15.4.2 DMA Transfer Completion Interrupts: Caution added
		562	Table 15.26 DMA Transfer Setting Example 2: Setting Example 2 at the bottom, changed
		563	Figure 15.38 Setting Example 2: Flow changed
		568	Table 15.32 Descriptor Settings: Descriptor 1, Descriptor 2, and Descriptor 3 values of CFG (Configuration), changed
		Section 18 Multi-Function Pin Controller (MPC)	
		618 to 638	Table 18.1 List of Multiplexed Pin Configurations, RD (output) in the Pin Function column for External bus controller corrected to RD# (output)
		640	18.2.2 P0n Pin Function Control Register (P0nPFS) (n = 0 to 7), description corrected
		641	18.2.3 P1n Pin Function Control Register (P1nPFS) (n = 0 to 7), description corrected
		643	18.2.4 P2n Pin Function Control Register (P2nPFS) (n = 0 to 7), description corrected
		644	18.2.5 P3n Pin Function Control Register (P3nPFS) (n = 0 to 7), description corrected
		646	18.2.6 P4n Pin Function Control Register (P4nPFS) (n = 0 to 7), description corrected
		648	18.2.7 P5n Pin Function Control Register (P5nPFS) (n = 0 to 6), description corrected
		649	18.2.8 P6n Pin Function Control Register (P6nPFS) (n = 0 to 7), description corrected
		651	18.2.9 P7n Pin Function Control Register (P7nPFS) (n = 0 to 7), description corrected
		652	18.2.10 P8n Pin Function Control Register (P8nPFS) (n = 0 to 7), description corrected
		654	18.2.11 P9n Pin Function Control Register (P9nPFS) (n = 0 to 7), description corrected
		655	18.2.12 PAn Pin Function Control Register (PAnPFS) (n = 0 to 7), description corrected
		656	18.2.13 PBn Pin Function Control Register (PBnPFS) (n = 0 to 7), description corrected

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0.80	Apr. 21, 2015	658	18.2.14 PCn Pin Function Control Register (PCnPFS) (n = 0 to 7), description corrected
		660	18.2.15 PDn Pin Function Control Register (PDnPFS) (n = 0 to 7), description corrected
		662	18.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 7), description corrected
		663	18.2.17 PFn Pin Function Control Register (PFnPFS) (n = 5 to 7), description corrected
		665	18.2.18 PGn Pin Function Control Register (PGnPFS) (n = 0 to 7), description corrected
		666	18.2.19 PHn Pin Function Control Register (PHnPFS) (n = 0 to 7), description corrected
		667	18.2.20 PJn Pin Function Control Register (PJnPFS) (n = 0 to 7), description corrected
		668	18.2.21 PKn Pin Function Control Register (PKnPFS) (n = 0 to 7), description corrected
		669	18.2.22 PLn Pin Function Control Register (PLnPFS) (n = 0 to 7), description corrected
		670	18.2.23 PMn Pin Function Control Register (PMnPFS) (n = 0 to 7), description corrected
		671	18.2.24 PNn Pin Function Control Register (PNnPFS) (n = 0 to 7), description corrected
		672	18.2.25 PPn Pin Function Control Register (PPnPFS) (n = 0 to 7), description corrected
		673	18.2.26 PRn Pin Function Control Register (PRnPFS) (n = 0 to 7), description corrected
		674	18.2.27 PSn Pin Function Control Register (PSnPFS) (n = 0 to 7), description corrected
		675	18.2.28 PTn Pin Function Control Register (PTnPFS) (n = 0 to 7), description corrected
		676	18.2.29 PUn Pin Function Control Register (PUnPFS) (n = 0 to 7), description corrected
		678	Table 18.39 Register Settings, Note 1 corrected
		Section 19 Multi-Function Timer Pulse Unit (MTU3a)	
		693	19.2.2 Timer Control Register 2 (TCR2), description corrected
		702	19.2.6 Timer I/O Control Register (TIOR), description corrected
		732	19.2.16 Timer Longword General Register n (TGRnLW) (n = A, B), description corrected
		735	19.2.18 Timer Synchronous Register (TSYR), description corrected
		737	19.2.19 Timer Counter Synchronous Start Register (TCSYSTR), address corrected
		755	19.2.33 Noise Filter Control Register n (NFCRn) (n = 0 to 4, 6, 7, 8, C), • NFCRC, address corrected
		Section 22 16-Bit Timer Pulse Unit (TPUa)	
		1127	22.2.4 Timer Interrupt Enable Register (TIER), bit table: Note 1 corrected
		Section 23 Programmable Pulse Generator (PPG)	
		1199	Table 23.2 List of Functions of the PPG, title corrected
		1201	Table 23.3 Pin Configuration of the PPG, title corrected
		Section 26 Watchdog Timer (WDTA)	
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		1273	Figure 26.1 WDT Block Diagram: Description on the top was changed.
		1273	Figure 26.1 WDT Block Diagram, changed
		1274	26.2.1 WDT Refresh Register (WDTRR): Note added to the value after reset
		1275	26.2.2 WDT Control Register (WDTCR): Note added to the value after reset
		1279	26.2.3 WDT Status Register (WDTSR): Note added to the value after reset
		1280	26.2.4 WDT Reset Control Register (WDTRCR): Note added to the value after reset
		—	26.5.1 Clock Division Ratio Setting, deleted
		Section 27 Independent Watchdog Timer (IWDTa)	
		—	Heading title: 27.1.1 Block Diagram, deleted
		1288	27.1.1 Block Diagram: Description changed
		1289	Figure 27.1 IWDT Block Diagram, changed
		Section 28 Ethernet MAC (ETHERC)	
		1308	Figure 28.1 Block Diagram of the ETHERC, description above the figure corrected
		1308	Figure 28.1 Block Diagram of the ETHERC, title corrected

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0.80	Apr. 21, 2015	1308	Figure 28.2 Block Diagram of the ETHERC (for Products Incorporating an R-IN Engine), title corrected
		1309	Table 28.2 Input/Output Pins of the ETHERC, description above the table corrected
		1309	Table 28.2 Input/Output Pins of the ETHERC, title corrected
		1309	Table 28.2 Input/Output Pins of the ETHERC, pin name: PHYLINK2 deleted
		1313	28.2.1.4 MAC Select Register (MACSEL), description corrected
		1313	Table 28.3 MAC Function Selection Method (for Products Incorporating an R-IN Engine), description in the Media I/F Port 1 column for 011 corrected
		1314	28.2.1.5 MII Control Register (MII_CTRLn) (n = 0 to 2), bit chart: RMII_RX_ER_EN deleted
		1314	28.2.1.5 MII Control Register (MII_CTRLn) (n = 0 to 2), bit table: symbol, bit name, and functional description of b9 corrected
		1316	28.2.2.1 MIIM Register (GMAC_MIIM), description corrected
		1317	28.2.2.2 TX ID Register (GMAC_TXID), bit chart: TXID corrected
		1325	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: PPDATA1 corrected
		1325	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: ETHERC.GMAC_PAUSE1, PPDATA1 corrected
		1325	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: ETHERC.GMAC_PAUSE2, PPDATA2 corrected
		1326	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: ETHERC.GMAC_PAUSE3, PPDATA3 corrected
		1326	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: ETHERC.GMAC_PAUSE4, PPDATA4 corrected
		1326	28.2.2.8 PAUSE Packet Data Register (GMAC_PAUSEn) (n = 1 to 5), bit chart: ETHERC.GMAC_PAUSE5, PPDATA5 corrected
		1328	28.2.2.11 MAC Address Registers (GMAC_ADRnA and GMAC_ADRnB) (n = 0 to 15), o GMAC_ADRnB: bit table corrected
		1336	28.2.3.1 Hardware Function System Call Register (SYSC), title corrected
		1336	28.2.3.1 Hardware Function System Call Register (SYSC), bit table: b15 to b0 corrected
		1337	28.2.3.2 Hardware Function Argument Register (Rn) (n = 4 to 7), • R4, bit chart: R4B corrected
		1337	28.2.3.2 Hardware Function Argument Register (Rn) (n = 4 to 7), • R5, bit chart: R5B corrected
		1338	28.2.3.2 Hardware Function Argument Register (Rn) (n = 4 to 7), • R6, bit chart: R6B corrected
		1338	28.2.3.2 Hardware Function Argument Register (Rn) (n = 4 to 7), • R7, bit chart: R7B corrected
		1339	28.2.3.3 Hardware Function Command Register(CMD), added
		1340	28.2.3.4 Hardware Function Return Value Register (R0, R1), • R0, bit chart: R0B corrected
		1340	28.2.3.4 Hardware Function Return Value Register (R0, R1), • R1, bit chart: R1B corrected
		1341	28.2.3.5 Hardware Function Type Register (C0TYPE), added
		1341	28.2.3.6 Hardware Function State Register (C0STAT), added
		1342	28.3.1 Hardware Functions, added
		1366	28.3.2 Interrupts, added
		1369	28.3.3.1 Initial Settings, description corrected
		1376	28.3.4.6 (1) Receive frame information, table listing the fields of the receive frame information: entries in the Explanation column for MARSTAT[2:0] corrected
		Section 29 Ethernet Switch	
		1382	Figure 29.1 Block Diagram of the Ethernet Interface, description corrected
		1382	Figure 29.1 Block Diagram of the Ethernet Interface, title corrected
		1382	Figure 29.2 Block Diagram of the Ethernet Interface (for Products Incorporating an R-IN Engine), title corrected

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		1399	29.2.2.13 Internal Queue Interface Status Register (QMGR_IFACE_STAT), bit chart, b31 to b19, b15 to b3: value after reset corrected
		1410	29.2.3.2 Learning Record B Register (LRN_REC_B), bit chart, b31 to b28: value after reset corrected
		1410	29.2.3.3 Learning Data Status Register (LRN_STATUS), bit chart, b31 to b1: value after reset corrected
		1415	29.2.4.4 MAC Status Register n (MAC_STATUSn) (Shared) (n = 0, 1), bit chart, b31 to b15, b13, b11, b9, b7 to b0: value after reset corrected
		1418	29.2.4.6 (2) MAC TX Statistic Counters, description for the address 0C 81A8h + 2000h*n in the table corrected
		1433	29.2.5.18 Timer Pulse Width Register (SWTMWTH), Note 2 deleted
		1436	29.2.6.2 DLR Status Register (DLR_STATUS), bit chart, b23 to 18, b7: value after reset corrected
		1443	29.2.6.9 DLR Supervisor MAC Address High Register (SUPR_MAChi), bit chart, b31 to b24: value after reset corrected
		1444	29.2.6.10 DLR Ring Status/VLAN Register (STATE_VLAN), bit chart, b15 to b9: value after reset corrected
		1446	29.2.6.14 DLR Sub Type/Protocol Version Register (ETH_STYP _VER), bit chart, b31 to b24: value after reset corrected
		1481	29.4.2 Switch Initialization, description corrected
		1482	Table 29.22 Examples of Initial Settings of Switch Engine, register at address A00B F118h added
		Section 30 EtherCAT Slave Controller (Only for Products Incorporating an R-IN Engine)	
		1489	Figure 30.1 Block Diagram of the EtherCAT Slave Controller, description above the figure corrected
		1489	Figure 30.1 Block Diagram of the EtherCAT Slave Controller, title corrected
		1489	Table 30.2 Input/Output Pins of the EtherCAT Slave Controller (excluding PHY MII pins), description above the figure corrected
		1489	Table 30.2 Input/Output Pins of the EtherCAT Slave Controller (excluding PHY MII pins), title corrected
		1493	30.3.1 EtherCAT PHY Offset Address Setting Register (CATOFFADD), bit chart, b31 to b5: value after reset corrected
		1493	30.3.1 EtherCAT PHY Offset Address Setting Register (CATOFFADD), bit table: b31 to b5 added
		1494	30.3.2 EtherCAT Operation Mode Setting Register (CATEMMD), bit chart, b31 to b1: value after reset corrected
		1494	30.3.2 EtherCAT Operation Mode Setting Register (CATEMMD), bit table: b31 to b1 added
		1495	30.3.3 EtherCAT TXC Shift Setting Register (CATTXCSFT), description corrected
		1495	30.3.3 EtherCAT TXC Shift Setting Register (CATTXCSFT), bit chart, b31 to b4: value after reset corrected
		1495	30.3.3 EtherCAT TXC Shift Setting Register (CATTXCSFT), bit table: b31 to b4 added
		1499	30.4.8 ESC Features Supported Register (FEATURE), bit chart, b15 to b12, b5 to b4, b1: value after reset corrected
		1499	30.4.8 ESC Features Supported Register (FEATURE), bit table: b15 to b12, b5, b4, b1 added
		1500	30.5.2 Configured Station Alias Register (STATION_ALIAS), bit table: entries in the PDI and ECT columns for b15 to b0 corrected
		1501	30.6.1 Write Register Enable Register (WR_REG_ENABLE), bit chart, b7 to b1: value after reset corrected
		1501	30.6.1 Write Register Enable Register (WR_REG_ENABLE), bit table: b7 to b1 added
		1501	30.6.2 Write Register Protection Register (WR_REG_PROTECT), bit chart, b7 to b1: value after reset corrected
		1501	30.6.2 Write Register Protection Register (WR_REG_PROTECT), bit table: b7 to b1 added

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		1502	30.6.3 ESC Write Enable Register (ESC_WR_ENABLE), bit table: b7 to b1 added
		1502	30.6.4 ESC Write Protection Register (ESC_WR_PROTECT), bit chart, b7 to b1: value after reset corrected
		1502	30.6.4 ESC Write Protection Register (ESC_WR_PROTECT), bit table: b7 to b1 added
		1503	30.7.1 ESC Reset ECAT Register (ESC_RESET_ECAT), When read: ESC_RESET_ECAT_R, bit chart, b7 to b2: value after reset corrected
		1503	30.7.1 ESC Reset ECAT Register (ESC_RESET_ECAT), When read: ESC_RESET_ECAT_R, bit table: b7 to b2 added
		1504	30.7.2 ESC Reset PDI Register (ESC_RESET_PDI), When read: ESC_RESET_PDI_R, bit chart: b7 to b2: value after reset corrected
		1504	30.7.2 ESC Reset PDI Register (ESC_RESET_PDI), When read: ESC_RESET_PDI_R, bit table: b7 to b2 added
		1505	30.7.3 ESC DL Control Register (ESC_DL_CONTROL), bit chart, b31 to b25, b23 to b19, b7 to b2: value after reset corrected
		1505	30.7.3 ESC DL Control Register (ESC_DL_CONTROL), bit table: b31 to b25, b23 to b19, b7 to b2 added
		1507	30.7.5 ESC DL Status Register (ESC_DL_STATUS), bit chart, b3: value after reset corrected
		1507	30.7.5 ESC DL Status Register (ESC_DL_STATUS), bit table: b3 added
		1509	30.8.1 AL Control Register (AL_CONTROL), bit chart, b15 to b5: value after reset corrected
		1509	30.8.1 AL Control Register (AL_CONTROL), bit table: b15 to b5 added
		1510	30.8.2 AL Status Register (AL_STATUS), bit chart, b15 to b5: value after reset corrected
		1510	30.8.2 AL Status Register (AL_STATUS), bit table: b15 to b5 added
		1511	30.8.4 RUN LED Override Register (RUN_LED_OVERRIDE), bit chart, b7 to b5: value after reset corrected
		1511	30.8.4 RUN LED Override Register (RUN_LED_OVERRIDE), bit table: b7 to b5 added
		1512	30.8.5 ERR LED Override Register (ERR_LED_OVERRIDE), bit chart, b7 to b5: value after reset corrected
		1512	30.8.5 ERR LED Override Register (ERR_LED_OVERRIDE), bit table: b7 to b5 added
		1516	30.9.5 Extended PDI Configuration Register (EXT_PDI_CONFIG), bit chart, b15 to b1: value after reset corrected
		1516	30.9.5 Extended PDI Configuration Register (EXT_PDI_CONFIG), bit table: b15 to b1 added
		1518	30.10.3 ECAT Event Request Register (ECAT_EVENT_REQ), bit chart, b15 to b12, b1: value after reset corrected
		1518	30.10.3 ECAT Event Request Register (ECAT_EVENT_REQ), bit table: b15 to b12, b1 added
		1519	30.10.4 AL Event Request Register (AL_EVENT_REQ), bit chart, b31 to b16, b7, b5: value after reset corrected
		1519	30.10.4 AL Event Request Register (AL_EVENT_REQ), bit chart, b14, symbol corrected
		1519	30.10.4 AL Event Request Register (AL_EVENT_REQ), bit table: b31 to b16, b7, b5 added
		1525	30.12.4 Watchdog Status Process Data Register (WDS_DATA), bit chart, b15 to b2: value after reset corrected
		1525	30.12.4 Watchdog Status Process Data Register (WDS_DATA), bit table: b15 to b2 added
		1527	30.13.1 EEPROM Configuration Register (EEP_CONF), bit chart, b7 to b2: value after reset corrected
		1527	30.13.1 EEPROM Configuration Register (EEP_CONF), bit table: b7 to b2 added
		1527	30.13.2 EEPROM PDI Access State Register (EEP_STATE), bit chart, b7 to b1: value after reset corrected
		1527	30.13.2 EEPROM PDI Access State Register (EEP_STATE), bit table: b7 to b1 added
		1528	30.13.3 EEPROM Control/Status Register (EEP_CONT_STAT), bit chart, b5 to b1: value after reset corrected

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		1530	30.14.1 MII Management Control/Status Register (MII_CONT_STAT), bit chart, b12 to b10: value after reset corrected
		1530	30.14.1 MII Management Control/Status Register (MII_CONT_STAT), bit table: b12 to b10 added
		1531	30.14.2 PHY Address Register (PHY_ADR), bit chart, b7 to b5: value after reset corrected
		1531	30.14.2 PHY Address Register (PHY_ADR), bit table: b7 to b5 added
		1531	30.14.3 PHY Register Address Register (PHY_REG_ADR), bit chart, b7 to b5: value after reset corrected
		1531	30.14.3 PHY Register Address Register (PHY_REG_ADR), bit table: b7 to b5 added
		1532	30.14.5 MII Management ECAT Access State Register (MII_ECAT_ACS_STAT), bit chart, b7 to b1: value after reset corrected
		1532	30.14.5 MII Management ECAT Access State Register (MII_ECAT_ACS_STAT), bit table: b7 to b1 added
		1533	30.14.6 MII Management PDI Access State Register (MII_PDI_ACS_STAT), bit chart, b7 to b2: value after reset corrected
		1533	30.14.6 MII Management PDI Access State Register (MII_PDI_ACS_STAT), bit table: b7 to b2 added
		1534	30.14.7 PHY Port Status n Register (PHY_STATUSn), bit chart, b7, b6: value after reset corrected
		1534	30.14.7 PHY Port Status n Register (PHY_STATUSn), bit table: b7, b6 added
		1535	30.15.1 FMMU Logical Start Address m Register (FMMUm_L_START_ADR), address corrected
		1535	30.15.2 FMMU Length m Register (FMMUm_LEN), address corrected
		1536	30.15.3 FMMU Logical Start Bit m Register (FMMUm_L_START_BIT), address corrected
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		1536	30.15.4 FMMU Logical Stop Bit m Register (FMMUm_L_STOP_BIT), address corrected
		1536	30.15.4 FMMU Logical Stop Bit m Register (FMMUm_L_STOP_BIT), bit chart, b7 to b3: value after reset corrected
		1536	30.15.4 FMMU Logical Stop Bit m Register (FMMUm_L_STOP_BIT), bit table: b7 to b3 added
		1537	30.15.5 FMMU Physical Start Address m Register (FMMUm_P_START_ADR), address corrected
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		1537	30.15.6 FMMU Physical Start Bit m Register (FMMUm_P_START_BIT), bit chart, b7 to b3: value after reset corrected
		1537	30.15.6 FMMU Physical Start Bit m Register (FMMUm_P_START_BIT), bit table: b7 to b3 added
		1538	30.15.7 FMMU Type m Register (FMMUm_TYPE), address corrected
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		1538	30.15.7 FMMU Type m Register (FMMUm_TYPE), bit table: b7 to b2 added
		1538	30.15.8 FMMU Activate m Register (FMMUm_ACT), address corrected
		1538	30.15.8 FMMU Activate m Register (FMMUm_ACT), bit chart, b7 to b1: value after reset corrected
		1538	30.15.8 FMMU Activate m Register (FMMUm_ACT), bit table: b7 to b1 added
		1539	30.16.1 SyncManager Physical Start Address m Register (SMm_P_START_ADR), address corrected
		1539	30.16.2 SyncManager Length m Register (SMm_LEN), address corrected
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		1540	30.16.3 SyncManager Control m Register (SMm_CONTROL), bit chart, b7: value after reset corrected
		1540	30.16.3 SyncManager Control m Register (SMm_CONTROL), bit table: b7 added
		1541	30.16.4 SyncManager Status m Register (SMm_STATUS), address corrected

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		1541	30.16.4 SyncManager Status m Register (SMm_STATUS), bit table: b2 added
		1542	30.16.5 SyncManager Activate m Register (SMm_ACT), address corrected
		1542	30.16.5 SyncManager Activate m Register (SMm_ACT), bit chart, b5 to b2: value after reset corrected
		1542	30.16.5 SyncManager Activate m Register (SMm_ACT), bit table: b5 to b2 added
		1543	30.16.6 SyncManager PDI Control m Register (SMm_PDI_CONT), address corrected
		1543	30.16.6 SyncManager PDI Control m Register (SMm_PDI_CONT), bit chart, b7 to b2: value after reset corrected
		1543	30.16.6 SyncManager PDI Control m Register (SMm_PDI_CONT), bit table: b7 to b2 added
		1544	30.17.1.1 Receive Time Port 0 Register (DC_RCV_TIME_PORT0), bit chart, b31 to b0: value after reset added
		1544	30.17.1.2 Receive Time Port 1 Register (DC_RCV_TIME_PORT1), bit chart, b31 to b0: value after reset added
		1550	30.17.2.6 Speed Counter Start Register (DC_SPEED_COUNT_START), bit chart, b15: value after reset corrected
		1550	30.17.2.6 Speed Counter Start Register (DC_SPEED_COUNT_START), bit table: b15 added
		1551	30.17.2.8 System Time Difference Filter Depth Register (DC_SYS_TIME_DIFF_FIL_DEPTH), bit chart, b7 to b4: value after reset corrected
		1551	30.17.2.8 System Time Difference Filter Depth Register (DC_SYS_TIME_DIFF_FIL_DEPTH), bit table: b7 to b4 added
		1551	30.17.2.9 Speed Counter Filter Depth Register (DC_SPEED_COUNT_FIL_DEPTH), bit chart, b7 to b4: value after reset corrected
		1551	30.17.2.9 Speed Counter Filter Depth Register (DC_SPEED_COUNT_FIL_DEPTH), bit table: b7 to b4 added
		1552	30.17.3.1 Cyclic Unit Control Register (DC_CYC_CONT), bit chart, b7, b3 to b1: value after reset corrected
		1552	30.17.3.1 Cyclic Unit Control Register (DC_CYC_CONT), bit table: b7, b3 to b1 added
		1554	30.17.4.2 SYNC Signal Pulse Length Register (DC_PULSE_LEN), bit chart, b13, b10 to b8, b4: value after reset corrected
		1554	30.17.4.3 Activation Status Register (DC_ACT_STAT), bit chart, b7 to b3: value after reset corrected
		1554	30.17.4.3 Activation Status Register (DC_ACT_STAT), bit table: b7 to b3 added
		1555	30.17.4.4 SYNC0 Status Register (DC_SYNC0_STAT), bit chart, b7 to b1: value after reset corrected
		1555	30.17.4.4 SYNC0 Status Register (DC_SYNC0_STAT), bit table: b7 to b1 added
		1555	30.17.4.5 SYNC1 Status Register (DC_SYNC1_STAT), bit chart, b7 to b1: value after reset corrected
		1555	30.17.4.5 SYNC1 Status Register (DC_SYNC1_STAT), bit table: b7 to b1 added
		1559	30.17.5.1 Latch 0 Control Register (DC_LATCH0_CONT), bit chart, b7 to b1: value after reset corrected
		1559	30.17.5.2 Latch 1 Control Register (DC_LATCH1_CONT), bit chart, b7 to b1: value after reset corrected
		1559	30.17.5.2 Latch 1 Control Register (DC_LATCH1_CONT), bit table: b7 to b1 added
		1560	30.17.5.3 Latch 0 Status Register (DC_LATCH0_STAT), bit chart, b7 to b3: value after reset corrected
		1560	30.17.5.3 Latch 0 Status Register (DC_LATCH0_STAT), bit table: b7 to b3 added
		1560	30.17.5.4 Latch 1 Status Register (DC_LATCH1_STAT), bit chart, b7 to b3: value after reset corrected
		1560	30.17.5.4 Latch 1 Status Register (DC_LATCH1_STAT), bit table: b7 to b3 added

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0.80	Apr. 21, 2015	1568	30.18.2 Vendor ID Register (VENDOR_ID), bit chart, b63 to b32: value after reset corrected
		1568	30.18.2 Vendor ID Register (VENDOR_ID), bit table: b63 to b32 added
		Section 31 USB2.0HS Host Module (USBh)	
		1571	31.1.1 Overview, description corrected
		—	31.1.2 Features, section title corrected
		—	31.1.3 Overview of Blocks, section title deleted
		1572	Figure 31.1 Schematic Block Diagram, title corrected
		1575 to 1576	Table 31.1 Register Mapping List, address A005 0804h: register name and symbol corrected
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 000h: VID_DID corrected to VID_DID_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 004h: CMND_STS corrected to CMND_STS_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 008h: REVID_CC corrected to REVID_CC_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 00Ch: CLS_LT_HT_BIST corrected to CLS_LT_HT_BIST_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 010h: BASEAD corrected to BASEAD_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, offset 018h deleted
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 02Ch: SSVID_SSID corrected to SSVID_SSID_A
		1576	Table 31.2 PCI Configuration Space For AHB-PCI Bridge, symbol of offset 03Ch: INTR_LINE_PIN corrected to INTR_LINE_PIN_A
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 000h: VID_DID corrected to VID_DID_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 004h: CMND_STS corrected to CMND_STS_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 008h: REVID_CC corrected to REVID_CC_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 00Ch: CLS_LT_HT_BIST corrected to CLS_LT_HT_BIST_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 010h: BASEAD corrected to BASEAD_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 02Ch: SSVID_SSID corrected to SSVID_SSID_O
		1577	Table 31.3 PCI Configuration Space for OHCI, symbol of offset 03Ch: INTR_LINE_PIN corrected to INTR_LINE_PIN_O
		1577	Table 31.3 PCI Configuration Space for OHCI, offset 0F0h: description and symbol corrected
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		1578	Table 31.4 PCI Configuration Space for EHCI, offset 1F0h: description and symbol corrected
		1578	Table 31.4 PCI Configuration Space for EHCI, offset 1F4h: description and symbol corrected
		1589	31.3.1.7 HcHCCA Register, bit chart: symbol HcHCCA corrected
		1589	31.3.1.7 HcHCCA Register, bit table, symbol of b31 to b8: HcHCCA corrected
		1589	31.3.1.8 HcPeriodicCurrentED Register, bit chart: symbol PeriodicCurrentED corrected
		1589	31.3.1.8 HcPeriodicCurrentED Register, bit table, symbol of b31 to b4: PeriodicCurrentED corrected
		1590	31.3.1.9 HcControlHeadED Register, bit chart: symbol ControlHeadED corrected
		1590	31.3.1.9 HcControlHeadED Register, bit table, symbol of b31 to b4: ControlHeadED corrected
		1590	31.3.1.10 HcControlCurrentED Register, bit chart: symbol ControlCurrentED corrected

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0.80	Apr. 21, 2015	1590	31.3.1.10 HcControlCurrentED Register, bit table, symbol of b31 to b4: ControlCurrentED corrected
		1591	31.3.1.11 HcBulkHeadED Register, bit chart: symbol BulkHeadED corrected
		1591	31.3.1.11 HcBulkHeadED Register, bit table, symbol of b31 to b4: BulkHeadED corrected
		1591	31.3.1.12 HcBulkCurrentED Register, bit chart: symbol BulkCurrentED corrected
		1591	31.3.1.12 HcBulkCurrentED Register, bit table, symbol of b31 to b4: BulkCurrentED corrected
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		1592	31.3.1.13 HcDoneHead Register, bit table, symbol of b31 to b4: DoneHead corrected
		1608	31.3.2.4 HCSP_PORTROUTE Register, bit chart: symbol Companion Port Route corrected
		1615	31.3.2.9 CTRLDSSEGMENT Register, bit chart: symbol CTRLDSSEGMENT corrected
		1615	31.3.2.10 PERIODICLISTBASE Register, bit chart: symbol BaseAddress (Low) corrected
		1615	31.3.2.10 PERIODICLISTBASE Register, bit table, symbol of b31 to b12: BaseAddress (Low) corrected
		1616	31.3.2.11 ASYNCLISTADDR Register, bit chart: symbol LPL corrected
		1616	31.3.2.11 ASYNCLISTADDR Register, bit table, symbol of b31 to b5: LPL corrected
		1625	31.3.3.4 Offset 0Ch Register (Cache Line Size, Latency Timer, Header Type, BIST), address corrected
		1626	31.3.3.5 Offset 10h Register (OHCI Base Address), bit chart: symbol OHCI Base Address corrected
		1626	31.3.3.5 Offset 10h Register (OHCI Base Address), bit table, symbol of b31 to b12: OHCI Base Address corrected
		1638	31.3.4.5 Offset 10h Register (EHCI Base Address), bit chart: symbol EHCI Base Address corrected
		1638	31.3.4.5 Offset 10h Register (EHCI Base Address), bit table, symbol of b31 to b4: EHCI Base Address corrected
		—	31.3.4.15 Offset F0h Register (Transceiver characteristic), deleted
		—	31.3.4.16 Offset F4h Register (UTMI + Operation Mode Control), deleted
		1648	31.3.5.5 Offset 10h Register (AHB-PCI Bridge Base Address), bit chart: symbol PCICOM_BASEADR corrected
		1648	31.3.5.5 Offset 10h Register (AHB-PCI Bridge Base Address), bit table, symbol of b31 to b10: PCICOM_BASEADR corrected
		1649	31.3.5.6 Offset 14h Register (PCI-AHB WIN1 Base Address), bit chart: symbol PCI_WIN1_BASEADR corrected
		1649	31.3.5.6 Offset 14h Register (PCI-AHB WIN1 Base Address), bit table, symbol of b31 to b28, PCI_WIN1_BASEADR: functional description corrected
		—	31.3.5.7 Offset 18h Register (PCI-AHB WIN2 Base Address), deleted
		1651	31.3.6.1 PCIAHB_WIN1_CTR Register, bit chart: symbol AHB_BASEADR corrected
		1651	31.3.6.1 PCIAHB_WIN1_CTR Register, bit table, symbol of b31 to b2: AHB_BASEADR corrected
		1652	31.3.6.2 AHBPCI_WIN1_CTR Register, bit chart: symbol PCIWIN1_BASEADR corrected
		1652	31.3.6.2 AHBPCI_WIN1_CTR Register, bit table, symbol of b31 to b11: PCIWIN1_BASEADR corrected
		1653	31.3.6.3 AHBPCI_WIN2_CTR Register, address corrected
		1653	31.3.6.3 AHBPCI_WIN2_CTR Register, bit chart: symbol PCIWIN2_BASEADR corrected
		1653	31.3.6.3 AHBPCI_WIN2_CTR Register, bit table, symbol of b31 to b16: PCIWIN2_BASEADR corrected
		1656	31.3.6.5 PCI_INT_STATUS Register, address corrected
		1659	31.3.6.7 USBCTR Register, bit table: functional description of b9 corrected
		1679	Figure 31.13 Initial Setting Sequence, Release write protection: (BOWI): MPC.PWPR[7] = 0: bit name corrected

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0.80	Apr. 21, 2015	1679	Figure 31.13 Initial Setting Sequence, Release write protection: (PFSWE): MPC.PWPR[6] = 1: bit name corrected
		1679	Figure 31.13 Initial Setting Sequence, PCIAHB_WIN1_CTR Register: Setting of endian for PCI transfer deleted
		1679	Figure 31.13 Initial Setting Sequence, PCIAHB_WIN1_CTR Register: setting of 16 beats max. for prefetch corrected
		Section 32 USB 2.0 HS Function Module (USBf)	
		1682	32.1 Overview, description corrected
		1682 to 1683	Table 32.1 Specifications of the USB Module, title corrected
		1683	32.1.1 Block Diagram, deleted
		1683	Figure 32.1 Block Diagram of the USB Module, title corrected
		1688	32.2.1.2 System Configuration Control Register 1 (SYSCFG1), bit chart, b11 to b8: value after hardware reset corrected
		1689	32.2.1.3 System Configuration Status Register (SYSSTS0), description of Line Status Monitor Bits (LNST) below the bit table corrected
		1694	32.2.5.1 CFIFO Port Register (CFIFO) D0FIFO Port Register (D0FIFO) D1FIFO Port Register (D1FIFO) bit chart: symbol FIFOPORT corrected
		1727	32.2.12.2 DCP Control Register (DCPCTR), bit table, b14 to b13, b11: functional description corrected
		1730	32.2.13.1 Pipe Window Select Register (PIPESEL), bit chart, Note 1 deleted
		1742	32.2.14.1 PIPE1 Control Register (PIPE1CTR) PIPE2 Control Register (PIPE2CTR) PIPE3 Control Register (PIPE3CTR) PIPE4 Control Register (PIPE4CTR) PIPE5 Control Register (PIPE5CTR) bit table, b13: functional description corrected
		1748	32.2.14.2 PIPE6 Control Register (PIPE6CTR) PIPE7 Control Register (PIPE7CTR) PIPE8 Control Register (PIPE8CTR) PIPE9 Control Register (PIPE9CTR) bit table, b13: functional description corrected
		1754	Table 32.18 List of Registers that can be Written by Software when SUSPM = 0 Register name for address A006 0002h corrected Address A006 0032h deleted Register name for address A006 0102h corrected Note 1 deleted
		1755	32.2.17.1 D0FIFO Continuous Transfer Port Register n (D0FIFOBn) (n = 0 to 7) D1FIFO Continuous Transfer Port Register n (D1FIFOBn) (n = 0 to 7) bit chart: symbol FIFOPORT corrected
		1757	Figure 32.4 Startup Sequence, bit name corrected
		1759	Table 32.22 Operations for USBf Interrupt Output, description above the table corrected
		1761	Figure 32.6 Interrupt Configuration Diagram, corrected
		1775	32.11.1 Isochronous Transfer Error Detection, (3) Maximum packet size over, title corrected
		Section 33 Serial Communications Interface with FIFO (SCIFA)	
		1782	Heading title: 33.2 Input/Output Pins, deleted
		1791	33.2.8 Bit Rate Register (BRR): Note deleted
		1794	Table 33.9 Maximum Bit Rates with External Clock Input (in Clock Synchronous Mode), totally changed
		1800	33.3.12 Serial Port Register (SPTR): Description changed
		1800	33.3.12 Serial Port Register (SPTR) Values after reset of symbols: RTS2DT, CTS2DT, SCKDT, and SPB2DT in the bit chart, changed

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0.80	Apr. 21, 2015	Section 34 I2C Bus Interface (RIIC)	
		1835	Table 34.2Pin Configuration: Description on the top was changed.
		1845	34.2.5 I2C Bus Mode Register 3 (ICMR3) Symbol of b7 was changed in the bit chart.
		1862	Table 34.5 Examples of ICBRH/ICBRL Settings for Transfer Rate: Note changed
		1905	Table 34.6 Interrupt Sources: Table heading, Priority, deleted
		Section 35 CAN Interface (RSCAN)	
		1909	35.1.1 Functional Overview, description corrected
		1909, 1910	Table 35.1 RSCAN Module Specifications, title corrected
		—	35.1.2 Block Diagram, section title deleted
		1911	Figure 35.1 RSCAN Module Block Diagram, title corrected
		1936	35.2.13 Reception Rule ID Register (RSCAN0GAFLIDj) (j = 0 to 15), bit chart: symbol GAFLID corrected
		1937	35.2.14 Reception Rule Mask Registers (RSCAN0GAFLMj) (j = 0 to 15), bit chart: symbol GAFLIDM corrected
		1940	35.2.16 Reception Rule Pointer 1 Registers (RSCAN0GAFLP1j) (j = 0 to 15), bit chart: symbol GAFLFDP corrected
		1940	35.2.16 Reception Rule Pointer 1 Registers (RSCAN0GAFLP1j) (j = 0 to 15), bit table: symbol of b25 to b8 corrected
		1943	35.2.19 Receive Buffer ID Registers (RSCAN0RMIDq) (q = 0 to 31), bit chart: symbol RMID corrected
		1952	35.2.26 Receive FIFO Buffer Access ID Registers (RSCAN0RFIDx) (x = 0 to 7), bit chart: symbol RFID corrected
		1964	35.2.33 Transmit/Receive FIFO Buffer Access ID Registers (RSCAN0CFIDk) (k = 0 to 5), bit chart: symbol CFID corrected
		1970	35.2.37 FIFO Empty Status Register (RSCAN0FESTS), bit chart, b25 to b17: value after hardware reset corrected
		1970	35.2.37 FIFO Empty Status Register (RSCAN0FESTS), bit table: symbol of b25 to b17 corrected
		1985	35.2.50 Transmit Buffer ID Registers (RSCAN0TMIDp) (p = 0 to 31), bit chart: symbol TMID corrected
		1991	35.2.55 Transmit Queue Status Registers (RSCAN0TXQSTSm) (m = 0, 1), bit chart, b12 to b8: value after reset corrected
		2002	35.2.64 RAM Test Page Access Registers (RSCAN0RPGACCr) (r = 0 to 63), bit chart: symbol RDTA corrected
		Section 37 SPI Multi I/O Bus Controller (SPIBSC)	
		2143	Table 37.1 SPIBSC Specifications: Description of Figure 37.1, Block Diagram of SPIBSC, at the bottom, changed
		—	Heading title: 37.2 Block Diagram, deleted
		—	Heading title: 37.3 Input/Output Pins, deleted
		2144	Table 37.2 Pin Configuration of the SPIBSC: Table title changed
		2145	37.4.1 Common Control Register (CMNCR) Functional description of b6 in the bit chart, changed
		2160	37.4.11 SPI Mode Address Setting Register (SMADR) Symbol: ADR was changed in the bit chart.
		2163	37.4.14 SPI Mode Read Data Register 0 (SMRDR0) Symbol: RDATA0 was changed in the bit chart.
		2163	37.4.14 SPI Mode Read Data Register 0 (SMRDR0) Value after reset was changed in the bit chart.
		2163	37.4.15 SPI Mode Write Data Register 0 (SMWDR0) Symbol: WDATA0 was changed in the bit chart.

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0.80	Apr. 21, 2015	Section 38 CRC Operation Units (CRC)	
		2188	38.2.1 CRC Data Input Register (CRCDIR), bit chart: symbol CRCDIR corrected
		2189	38.2.2 CRC Data Output Register (CRCDOR), bit chart: symbol CRCDOR corrected
		Section 41 ΔΣ Interface (DSMIF)	
		2244	41.2.2 UVW Status Register (UVWSTA), bit chart, symbols ERWSC, ERVSC, ERUSC: value after reset corrected
		2250	41.2.7 UVW Total Current Abnormality Detection Lower Limit Setting Register (UVWIGUNCMP), bit chart: symbol CMPUVWIGNDUNDER corrected
		2251	41.2.8 UVW Total Current Abnormality Detection Upper Limit Setting Register (UVWIGOVCMP), bit chart: symbol CMPUVWIGNDOVER corrected
		2261	41.2.22 XYZ Status Register (XYZSTA), bit chart, b6, b5: value after reset corrected
		2261	41.2.22 XYZ Status Register (XYZSTA), bit chart, symbol ERXSC: value after reset corrected
		2261	41.2.22 XYZ Status Register (XYZSTA), bit table, b6, b5: description corrected
		Section 42 Error Control Module (ECM)	
		2279	Table 42.1 Specifications of ECM: Table title changed
		2291	42.2.8 ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0) Functional description of b2, b1, and b0 in the bit chart, changed
		2296	42.2.11 ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0) Functional description of b2, b1, and b0 in the bit chart, changed
		2301	42.2.14 ECM Internal Reset Configuration Register 0 (ECMIRCFG0) Functional description of b2, b1, and b0 in the bit chart, changed
		2306	42.2.17 ECM Error Mask Register 0 (ECMEMK0) Functional description of b2, b1, and b0 in the bit chart, changed
		2311	42.2.20 ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0) Functional description of b2, b1, and b0 in the bit chart, changed
		2317	42.2.25 ECM Pseudo Error Trigger Register 0 (ECMPE0) Functional description of b2, b1, and b0 in the bit chart, changed
		2322	42.2.29 ECM Delay Timer Register (ECMDTMR): Description changed
		2324	42.2.31 ECM Delay Timer Configuration Register 0 (ECMDTMCFG0) Functional description of b2, b1, and b0 in the bit chart, changed
		2330	42.2.34 ECM Delay Timer Configuration Register 3 (ECMDTMCFG3) Functional description of b2, b1, and b0 in the bit chart, changed
		2341	42.4.1 Notes Regarding ECMCLK: Description changed
		Section 43 12-Bit A/D Converter (S12ADCa)	
		2343 to 2344	Table 43.1 Specifications of 12-Bit A/D Converter, Input channels and A/D conversion clock: Note 1 corrected to Note 3
		2375	43.2.13 A/D Sample and Hold Circuit Control Register (ADSHCR), address corrected
		2442	Figure 43.40 Procedures for Clear Operation by Software through the ADCSR.ADST Bit, “Is data transfer to EMU2 used?” deleted from the flow
		2442	Figure 43.40 Procedures for Clear Operation by Software through the ADCSR.ADST Bit, “Disable data transfer from the ADC to EMU2.” deleted from the flow
		Section 44 Temperature Sensor	
		2451	44.4.1 Module-Stop Function Setting, description deleted
		Section 45 Data Operation Circuit (DOC)	
		2452	Figure 45.1 Block Diagram of Data Operation Circuit (DOC): Figure title changed
		Section 46 RAM (Product Option)	
		2459	Table 46.1 Specifications of RAM: Description on RAM addresses (for products incorporating an R-IN engine) (for access from the Cortex-M3), changed
		2459	Table 46.1 Specifications of RAM: Caution added
		2470	46.2.8 2-Bit ECC Error Address Register (RAMDBEAD): Description changed

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0.80	Apr. 21, 2015	2470	46.2.8 2-Bit ECC Error Address Register (RAMDBEAD) Symbol: ADDRESS of b31 to b20 in the bit chart was changed to “—”
		2470	46.2.8 2 2-Bit ECC Error Address Register (RAMDBEAD) Symbol: ADDRESS of b19 and b18 in the bit chart was changed to “BANK”
		2470	46.2.8 2-Bit ECC Error Address Register (RAMDBEAD) Symbol: ADDRESS of b31 to b20 in the table of bits was changed to “Reserved”
		2470	46.2.8 2-Bit ECC Error Address Register (RAMDBEAD) Symbol: ADDRESS of b19 and b18 in the table of bits was changed to “BANK”
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine): Description changed
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine) Symbol: ADDRESS of b31 to b20 in the bit chart was changed to “—”
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine) Symbol: ADDRESS of b19 and b18 in the bit chart was changed to “BANK”
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine) Symbol: ADDRESS of b31 to b20 in the table of bits was changed to “Reserved”
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine) Symbol: ADDRESS of b19 and b18 in the table of bits was changed to “BANK”
		2471	46.2.9 2-Bit ECC Error Address Register (RAMDBEAD) (for Products Incorporating an R-IN Engine): Note changed
		2474	46.3.3 (1) Example of ECC error-injection setting procedure Flow procedure “Enable error injection”, changed
		2475	46.3.3 (2) Procedure for Checking ECC Operation After the flow procedure “Write 0000_0001h to the RAMEDC register”, add the procedure “Write 0000_0000h to the RAMPCMD register”.
		2475	46.3.3 (2) Procedure for Checking ECC Operation The flow procedure “Read the RAMDBEAD register to acquire the address where the error was found”, changed
		2475	46.3.3 (2) Procedure for Checking ECC Operation The flow procedure “Read the RAMDBECNT register to check the number of errors that were found”, changed
		2475	46.3.3 (2) Procedure for Checking ECC Operation The flow procedure “Write 0000_0000h to the RAMPCMD register”, deleted
		Section 47 Electrical Characteristics (Target)	
		2477	Figure 47.1 Power On/Off Sequence: Period of (2) Tdly12, corrected
		2485	Table 47.13 EXTAL Clock Timing, 25.00 ± 25 ppm: Note 1, added
		2485	Table 47.14 XTAL Clock Timing: Note 2, added
		2491	Figure 47.12 SRAM Interface Basic Bus Cycle (No Wait): Figure title changed
		2492	Figure 47.13 SRAM Interface Basic Bus Cycle (Software Wait 1): Figure title changed
		2493	Figure 47.14 SRAM Interface Basic Bus Cycle (Software Wait 1, External Wait 1 Inserted): Figure title changed
		2494	Figure 47.15 SRAM Interface Basic Bus Cycle (Software Wait 1, External wait Enabled (WM Bit = 0), No Idle Cycle): Figure title changed
		2517	Heading title: 47.4.5.1 I/O Port Timing, added
		2518	Heading title: 47.4.5.2 TPUa Timing, added
		2519	Heading title: 47.4.5.3 CMTW Timing, added
		2520	Heading title: 47.4.5.4 MTU3a Timing, added
		2521	Heading title: 47.4.5.5 POE3 Timing, added
		2522	Heading title: 47.4.5.6 GPTA Timing, added

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0.80	Apr. 21, 2015	2523	Heading title: 47.4.5.7 A/D Converter Trigger Timing, added
		2524	Heading title: 47.4.5.8 SCIFA Timing, added
		2526	Heading title: 47.4.5.9 RSPIa Timing, added
		2530	Heading title: 47.4.5.10 SPIBSC Timing, added
		2533	Figure 47.63 SPIBSC Buffer On/Off Timing (CPHAT = 0, SPHAR = 1), added
		2534	Heading title: 47.4.5.11 RIICa Timing, added
		2534	Table 47.29 RIICa Timing: Symbol of SCL, SDA input rising time for RIICa (Standard-mode), changed
		2534	Table 47.29 RIICa Timing: Symbol of SCL, SDA input falling time for RIICa (Standard-mode), changed
		2534	Table 47.29 RIICa Timing: Symbol of SCL, SDA input rising time for RIICa (Fast-mode), changed
		2534	Table 47.29 RIICa Timing: Symbol of SCL, SDA input falling time for RIICa (Fast-mode), changed
		2536	Heading title: 47.4.5.12 Serial Sound Interface Timing, added
		2538	Heading title: 47.4.5.13 CAN Interface Timing, added
		2539	Heading title: 47.4.5.14 ETHERC Timing, added
		2539	Table 47.32 ETHERC Timing: ETHn_TXD0 to ETHn_TXD3 output delay time for ETHERC (MII), changed
		2539	Table 47.32 ETHERC Timing: ETHn_RXD0 to ETHn_RXD3 setup time for ETHERC (MII), changed
		2539	Table 47.32 ETHERC Timing: ETHn_RXD0 to ETHn_RXD3 hold time for ETHERC (MII), changed
		2543	Heading title: 47.4.5.15 Serial Management Interface, added
		2544	Heading title: 47.4.5.16 Delta-Sigma Interface Timing, added
		2547	Figure 47.83 Measurement Circuit (High Speed): Resistor symbol, deleted
		2548	Table 47.37 12-Bit A/D (Unit 0) Conversion Characteristics Description on “Channel-dedicated sample-and-hold circuits in use (AN000 to AN003), When disconnection detection assistance is in use”, changed
		2548	Table 47.37 12-Bit A/D (Unit 0) Conversion Characteristics Description on “Channel-dedicated sample-and-hold circuits in use (AN000 to AN003), When disconnection detection assistance is not in use”, added
		2550	Table 47.39 Temperature Sensor Characteristics: Typ. of output voltage, changed
0.90	Sep. 07, 2015	1. Overview	
		62	Table 1.2 Comparison of Functions for Different Packages, encoder interfaces, description changed
		64	Table 1.3 List of Products, products added
		71	Table 1.4 Pin Functions, USB_RREF, description partly changed (AVSS33USB → VSS_USB)
		72	Table 1.4 Pin Functions, the category Encoder I/F added
		75 to 82	Table 1.5 Pin Assignments (320-Pin FBGA), pin names ENCIF00 to ENCIF07 added
		87 to 96	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), Others, Encoder I/F added
		87 to 96	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), pin names ENCIF00 to ENCIF07 added
		94	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA), Bus for pin number T8, pin names changed
		3. Operating Modes	
		112	Figure 3.2 Memory Assignment of the Loader Program and Parameters for the Loader, note 4, changed
		118	Table 3.7 Status of the ARM CP15 Registers at the Time the Boot Finishes, System control auxiliary register: Setting Value at the Time the Boot Processing Finishes, changed
		4 Address Space	
		124	Figure 4.1 Memory Map, erroneous description corrected (DMA0 ' DMAC0), note 6 in the map replaced with the statement “mirror area of xxx”

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0.90	Sep. 07, 2015	125	Figure 4.2 Memory Map (1-Mbyte Extended Internal SRAM), note 4 in the map replaced with the statement “mirror area of xxx”
		7. Clock Generation Circuit	
		241	7.8.9 USB Clock M (USBMCLK), description changed
		241	7.8.14 ECM Clock (ECMCLK), description changed
		14. Bus State Controller	
		434	14.4.6 SDRAM Interface, (1) SDRAM Direct Connection, description changed
		15. DMA Controller (DMACAa)	
		495	15.2.12 Channel Control Register n (CHCTRL_n), description for b0 (SETEN), a note added
		497 to 500	15.2.13 Channel Configuration Register n (CHCFG_n), description changed, description for b30 (REN) changed
		562	15.5.2 Setting Example 2 (Register Mode Software Request), Setting Example 2, Setting of CHCFG changed
		17. I/O ports	
		617	Table 17.3 Handling of Unused Pins, erroneous description corrected (ERROROUT → ERROROUT#)
		18. Multi-Function Pin Controller (MPC)	
		639	Table 18.1 List of Multiplexed Pin Configurations, Module/Function, Encoder I/F added
		645	18.2.5 P3n Pin Function Control Register (P3nPFS), Value after reset changed, Table 18.6 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, value after reset changed
		646	18.2.5 P3n Pin Function Control Register (P3nPFS), Table 18.7 Register Settings for the Input/Output Function in the 176-Pin QFP Pin, PSEL[5:0] Setting, value after reset changed
		650	18.2.8 P6n Pin Function Control Register (P6nPFS) Table 18.12 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 011110b, setting for the P67 pin, changed
		652	18.2.9 P7n Pin Function Control Register (P7nPFS) (n = 0 to 7) Table 18.14 Register Settings for the Input/Output Function in the 320-Pin BGA and 176-Pin QFP Pins, PSEL[5:0] Setting, 101011b added
		655	18.2.11 P9n Pin Function Control Register (P9nPFS) Table 18.17 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 01011b added
		656	18.2.12 PAn Pin Function Control Register (PAnPFS) (n = 0 to 7) Table 18.18 Register Settings for the Input/Output Function in the 320-Pin BGA and 176-Pin QFP Pins, PSEL[5:0] Setting, 101011b added
		673	18.2.25 PPn Pin Function Control Register (PPnPFS) Table 18.34 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 01011b added
		674	18.2.26 PRn Pin Function Control Register (PRnPFS) Table 18.35 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 101011b added
		675	18.2.27 PSn Pin Function Control Register (PSnPFS) Table 18.36 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 101011b added
		676	18.2.28 PTn Pin Function Control Register (PTnPFS) Table 18.37 Register Settings for the Input/Output Function in the 320-Pin BGA Pin, PSEL[5:0] Setting, 101011b added
		20. Port Output Enable 3 (POE3)	
		All	Erroneous descriptions corrected (GTP → GPT)
		28. Ethernet MAC (ETHERC)	
		1337	28.2.3 Hardware Function Call Register, reference destination changed
		1344	28.3.3.1 Initial Settings, relocated from section 28.3.1.1, descriptions changed, Procedure for setting up the hardware functions, changed

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0.90	Sep. 07, 2015	1348	Table 28.6 HWFNC_LongBuffer_Get, Return value register R0[1:0] (Result), description changed
		1369	28.3.3 Ethernet Frame Transmission Function, sequence 1, reference destination changed
		1369	28.3.3.1 Obtaining a transmit buffer, R0, value changed
		1374	28.3.4.1 Initial setup, description changed
		—	28.3.4.7 Hardware Function Call Issuance Flowchart, deleted
		29. Ethernet Switch	
		1435	29.2.6.2 DLR Status Register (DLR_STATUS), b16 and b17, value after reset changed, note 1 added
		1439	29.2.6.5 DLR Interrupt Status/ACK Register (DLR_IRQ_STAT_ACK), b7 and b8, value after reset changed
		30. EtherCAT Slave Controller (Only for Products Incorporating an R-IN Engine)	
		1499	30.5.1 Configured Station Address Register (STATION_ADR), PDI and ECAT, R/W attributes changed
		1499	30.5.2 Configured Station Alias Register (STATION_ALIAS), PDI and ECAT, R/W attributes changed
		31. USB2.0HS Host Module (USBh)	
		1570	31.1 Overview, USB2.0 Host Controller Operation, changed, AHB Bus Interface, deleted
		1572	31.1.1.1 General Precautions, (3) and (4) added (relocated from 31.1.1.4 System Implementation)
		—	31.1.1.4 System Implementation, deleted
		1578	31.3.1 OHCI Operational Registers, description added
		1604	31.3.2 EHCI Operational Registers, description added
		32. USB 2.0 HS Function Module (USBf)	
		1681	Table 32.1 Specifications of the USB Module, For High-Speed USB, description changed
		1683	32.1.1.2 Bus interface, description changed
		1684	32.1.1.4 USB Data Transfer, description changed
		All	32.2 Register Descriptions, common through the section, itemized sentences “When function controller operation is selected” deleted
		1686	32.2.1.1 System Configuration Control Register 0 (SYSCFG0), b5 (DRPD), description changed, USB Block Operation Enable (USBE), Function, a bit symbol changed (SuspendM → SUSPM)
		1688	32.2.1.3 System Configuration Status Register (SYSSTS0), Line Status Monitor Bits (LNST), description changed
		1688	Table 32.4 States of USB Data Bus Line, the column “Low-Speed Operations (only when Host Controller Operation is Selected)”, deleted
		1696	32.2.5.2 CFIFO Port Select Register (CFIFOSEL), FIFO Port Access Pipe Specification (CURPIPE) and CFIFO Port Access Bit Width Bits (MBW), descriptions changed
		1699	32.2.5.3 D0FIFO Port Select Register (D0FIFOSEL)/D1FIFO Port Select Register (D1FIFOSEL), DxFIFO Port Byte Endian Control Bit (BIGEND), description changed
		1711	32.2.8.2 BRDY Interrupt Status Register (BRDYSTS), BRDY Interrupt Status for (PIPEBRDY), description changed
		1714	32.2.8.3 NRDY Interrupt Status Register (NRDYSTS), NRDY Interrupt Status for Each Pipe (PIPENRDY), description changed
		1716	32.2.8.4 BEMP Interrupt Status Register (BEMPSTS), BEMP Interrupt Status for Each Pipe (PIPEBEMP), description changed
		1722	32.2.11.2 USB Request Value Register (USBVAL), Value (wValue), Function, description changed
		1723	32.2.11.3 USB Request Index Register (USBINDX), Index (wIndex), Function, description changed
		1724	32.2.11.4 USB Request Length Register (USBLENG), Length (wLength), Function, description changed

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0.90	Sep. 07, 2015	1734	32.2.13.3 Pipe Buffer Specification Register (PIPEBUF), b7 to b0 (BUFNMB[7:0]), Function, description changed (4h-87h) → (4h-80h), Buffer number (BUFNMB), Function, description changed (0 [00h] to 8640 [87h] for 8.5-Kbyte memory) → (0 [00h] to 8192 [0x80] for 8-Kbyte memory)
		1757	32.3.3 USB Data Bus Resistor Controller, description changed
		1757	32.3.5 Notes on Stopping Clocks, description changed (6.5 ms → 5.5 ms)
		1764	Table 32.23 Pipe Settings, PIPEBUF.BUFNMB bit, Remark, area range changed (8 to 87 hex → 8 to 80 hex)
		1776	32.11.3.2 Interval Counter Initialization, section title changed
		33. Serial Communications Interface with FIFO (SCIFA)	
		1792	Table 33.4 Bit Rates and BRR Register Settings in Asynchronous Mode, Bit Rate, 110 bps deleted, 115200 bps and 500000 bps, settings for SERICLK changed (to blank), note changed
		1793	Table 33.6 Maximum Bit Rates for Various Frequencies with Baud Rate Generator (in Asynchronous Mode), Maximum Bit Rate, values changed, note changed
		1793	Table 33.8 Maximum Bit Rates with External Clock Input (in Asynchronous Mode), Maximum Bit Rate, values changed, note changed
		1794	Table 33.10 Bit Rates and BRR and MDDR Registers Settings in Asynchronous Mode, added
		1830	33.8.4 Break Signal Transmission, erroneous descriptions of bit name corrected (SPB2DT → SPB2IO)
		37. SPI Multi I/O Bus Controller (SPIBSC)	
		2145	37.2.1 Common Control Register (CMNCR), b24 (SFDE), value after reset changed
		41. ΔΣ Interface (DSMIF)	
		2275	Table 41.8, title name, “example” deleted and a complement “The Only Allowed Combinations of the Register Values” added
		2278	41.5.2 Current Value on Detection of an Overcurrent, added
		42. Error Control Module (ECM)	
		2338	42.3.1 Operations for Error Output, description changed, ERROROUT# Pin Output Level for Dynamic-mode in the table, changed
		46. RAM (Product Option)	
		2459	Table 46.1 Specifications of RAM, the item “Data retention function” deleted
		47. Electrical Characteristics (Target)	
		2478	Table 47.3 DC Characteristics (2) [Power Supply], Normal Operation, “TBD” cells filled with values, VDD type, values changed
		2530	Table 47.28 SPIBSC Timing, minimum values for tSU and tH changed
		2532	Figure 47.60, bit name included in the title changed (SPHAR → CPHAR)
		2533	Figure 47.63, bit name included in the title changed (SPHAR → CPHAR)
		2534	Table 47.29 RIICa Timing, symbols changed (tr → tsr, tf → tsf), note 4 added
		2539	Table 47.32 ETHERC Timing, expression of a symbol changed (Tr/Tf → Tr, Tf)
		2539	Figure 47.70 Timing with the CLKOUT25Mn and RMII Signals, changed
		2541	Figure 47.74 MII Transmission Timing (Normal Operation), changed (ETHn_CRS and ETHn_COL deleted)
		2541	Figure 47.75 MII Transmission Timing (Conflict Occurrence), changed (ETHn_CRS and ETHn_COL deleted)
		2543	Table 47.33 Serial Management Interface, ETHn_MDIO output delay time (to ETHn_MDC↑), the arrow direction changed from up to down, the minimum and maximum values for tDMDIO changed
		2543	Figure 47.78 Serial Management Access Timing, changed
		2548	Table 47.37 12-Bit A/D (Unit 0) Conversion Characteristics, “TBD” cells filled with values
		2549	Table 47.38 12-Bit A/D (Unit 1) Conversion Characteristics, “TBD” cells filled with values

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0.90	Sep. 07, 2015	Appendix 1. Outer Dimensions Diagram	
		2554, 2555	Newly added
1.00	Feb. 15, 2016	All	Products incorporating an R-IN Engine → Products incorporating an R-IN Engine (optional), EtherCAT slave controller (optional), EtherCAT (optional), products incorporating an EtherCAT (optional)
		All	Module symbol changed (S12ADC → S12ADCa)
		All	Module symbol changed (GPTA → GPTa)
		Features	
		54	Note 4 added
		1. Overview	
		60	Table 1.1 Outline of Specifications, 12-bit A/D converter, conversion times are changed
		61	Table 1.1 Outline of Specifications, note 5 added
		62	Table 1.2 Comparison of Functions for Different Packages, description of EtherCAT slave controller (ECATC) changed
		65	Figure 1.1 Block Diagram, module name corrected (GPTA → GPTa)
		70	Table 1.4 Pin Functions, ETH2_RXD0 to 3 pins added, description for the PHYLINK0 and PHYLINK1 pins changed, descriptions for the PHYRESETOUT# and PHYRESETOUT2# pins changed, the CATRESTOUT pin deleted
		72	Table 1.4 Pin Functions, note 1 added
		73	Figure 1.2 Pin Arrangement (320-pin FBGA), name of A10 pin corrected
		5. I/O Register	
		179	Table 5.1 List of I/O Registers, address corrected (A007 20BCh → A007 20ACh)
		204	Table 5.1 List of I/O Registers, register symbol of the input learning blocking register corrected
		213	Table 5.1 List of I/O Registers, register name of BUFID changed (receive FIFO information register → receive buffer information register), Ether Switch 10-Mbps/half-duplex mode setting register (ETHSW10HDEN) added
		9. Low-Power Consumption Function	
		258	Bit name of b18 (MSTPCRB18), note 3 added
		261	9.2.5 Module Stop Control Register E (MSTPCRE), descriptions of b1 to b3 (reserved bits) changed
		10. Debugging Interface	
		277	Table 10.10 Available Trace Functions, module names are changed
		12. Interrupt Controller (ICUA)	
		289	12.2.6 NMI Pin Interrupt Control Register (NMICR), description for the register changed
		339	12.4.2.13 Interrupt Address Register (HVA0), description for the register changed
		365	Figure 12.6 Initializing Registers of VIC, content changed and a note added
		369	Figure 12.8 IRQ Interrupt Operation (Level Operations), register name changed (HVA → HVA0)
		370	Figure 12.9 IRQ Interrupt Operation (Edge Interrupt), register name changed (HVA → HVA0),
		372	Figure 12.10 Concept of Multiple Interrupts (1 / 2), descriptions changed
		373	Figure 12.10 Concept of Multiple Interrupts (2 / 2), descriptions added
		375	12.4.6.3 Notes on Selecting Level Detection, descriptions changed, an example program added
		14. Bus State Controller	
		476	Table 14.19 Number of Idle Cycles Inserted between Access Cycles to Different Memory Types, note 1, bit symbol corrected (HM → HW)
		15. DMA Controller (DMACAa)	
		479	Table 15.2 Pin Configuration of the DMAC, note, a section for reference added
		498	15.2.13 Channel Configuration Register n (CHCFG_n), bit table, b10 to b8, AM[2:0], description, a note added

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1.00	Feb. 15, 2016	503	15.2.17 Source Continuous Register n (SCNT_n), description of the register changed (0000h → 0000 0000h)
		506	15.2.19 Destination Continuous Register n (DCNT_n), description of the register changed (0000h → 0000 0000h)
		509	15.2.21 DMA Control Register (DCTRL_X (X = A or B)), bit table, b31-b1 (reserved bits) changed
		533	Figure 15.13 Block Transfer Mode (REQD = 0, SDS = DDS), changed to internal signals, a note added
		546	15.3.5 DMA Acknowledge Output/DMA Transaction Completion Output Function, descriptions added
		547	Table 15.22 DACKn/TENDn Pin Output Settings, description of applications for the mask mode partially changed (low → inactive)
		561	Table 15.25 DMA Transfer Setting Example 1, the start address of transfer source changed, description of DAM transfer request changed, an item “selection of the side which makes a transfer requests” added
		561	15.5.1 Setting Example 1 (Register Hardware Request), Setting Example 1, values for N0SA and CHCFG, changed
		562	Figure 15.37 Setting Example 1, content changed
		16. Event Link Controller (ELC)	
		577	16.2.2 Event Link Setting Register n (ELSRn), n = 16 deleted
		579	Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers, descriptions of Ethernet controller changed (limitation for the product is deleted, signals are denoted as optional)
		18. Multi-Function Pin Controller (MPC)	
		All	Package names corrected (320-pin BGA → 320-pin BGA, 176-pin QFP → 176-pin HLQFP)
		646	18.2.5 P3n Pin Function Control Register (P3nPFS), bit map, values after reset are changed, notes 1 and 2 are added
		20. Port Output Enable 3 (POE3)	
		937	Table 20.1 POE3 Specifications, Conditions for the high-impedance state, descriptions of MTU complementary PWM output pins changed
		21. General PWM Timer (GPTa)	
		1104	Table 21.10 Output Pins for Channels 0 to 2, specified ports are changed
		28. Ethernet MAC (ETHERC)	
		All	Descriptions changed (receive FIFO → receive buffer)
		1311	Table 28.2 Input/Output Pins of the ETHERC, pins ETH2_RXD0 to ETH2_RXD3 are added, descriptions for PHYLINK0 and PHYLINK1 are changed, descriptions for PHYRESETOUT# and PHYRESETOUT2# are changed
		1315	Table 28.3 MAC Function Selection Method for Products Incorporating EtherCAT (an Optional Function), contents changed
		1315	Table 28.4 MAC Function Selection Method, contents changed
		1317	28.2.1.6 Ethernet Peripheral Reset Register (ETHSFTRST), bit table, b2 (PHYRST), descriptions changed
		1318	28.2.2.1 MIIM Register (GMAC_MIIM), bit table, b26 (RWDV), write or read attribute changed
		1324	28.2.2.6 TX MODE Register (GMAC_TXMODE), b26 changed (SFOP → reserved bit)
		1333	28.2.2.13 TX FIFO Status Register (GMAC_TXFIFO), b31 changed (TFULL → reserved bit)
		1337	28.2.2.18 Receive Buffer Information Register (BUFID), descriptions of the register changed, the bit name, description and the write or read attribute of b31 (NOEP) in the bit table changed
		1344	28.3.1 Hardware Functions, a note added
		1345	Figure 28.4 Flow of Processing for Issuing the Hardware Function Call, contents changed
		1349	(e) List of Hardware Function Calls, a note added
		1353	Figure 28.9 Outline of Processing by the Reception MACDMAC, a register name corrected (BUFFID → BUFID)

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1.00	Feb. 15, 2016	1376	28.3.4.6 Format of receive data, description of the register partially changed (a word boundary → a 64-bit boundary)
		1376	Figure 28.15, “for Frames without the TCP/IP and UDP/IP Packets” is added in the title name, the size of padding changed (0 to 3 → 0 to 7), a field name corrected (TOOSHOTR → TOOSHORT)
		1377	Figure 28.16 Format of Receive Data for Frames with the TPC/IP and UDP/IP Packets, newly added
		29. Ethernet Switch	
		All	Descriptions changed (receive FIFO → receive buffer)
		1385	29.2.1.1 Ethernet PHY LINK Mode Register (ETHPHYLNK), bit table, bit names of b0 (SWLINK0), b1 (SWLINK1), b2 (CATLINK0), and b3 (CATLINK1) are changed
		1388	29.2.1.4 Ether Switch 10-Mbps/Half-Duplex Mode Setting Register (ETHSW10HDEN), newly added
		1393	29.2.2.5 Input Learning Blocking Register, register symbol changed
		1416	29.2.4.3 FIFO BUffer Threshold Register n (Shared), descriptions for TX_SECTION_EMPTYn and TX_SECTION_FULLn partially corrected (receive FIFO → transmit FIFO)
		1447	29.2.6.12 DLR Beacon Interval Register (BEC_INTRVL), b31 to b0 (BECINTCAL), descriptions partially changed
		1449	29.2.6.15 DLR Beacon Timeout Timer Register (INV_TMOUT), b31 to b0 (INVBECTMOUT), descriptions partially changed
		30. EtherCAT Slave Controller (Only for Products Incorporating an R-IN Engine)	
		1503	30.6.1 Write Register Enable Register (WR_REG_ENABLE), b7 to b1 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1503	30.6.2 Write Register Protection Register (WR_REG_PROTECT), b7 to b1 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1504	30.6.3 ESC Write Enable Register (ESC_WR_ENABLE), b7 to b1 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1504	30.6.4 ESC Write Protection Register (ESC_WR_PROTECT), b7 to b1 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1506	30.7.2 ESC Reset PDI Register (ESC_RESET_PDI), b7 to b2 (reserved bits), descriptions partially deleted, write or read attribute for PDI changed
		1507, 1508	30.7.3 ESC DL Control Register (ESC_DL_CONTROL), b7 to b2 (reserved bits), b23 to b29, and b31 to b25, descriptions partially deleted, write or read attributes for ECAT changed
		1529	30.13.1 EEPROM Configuration Register (EEP_CONF), b7 to b2 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1530	30.13.3 EEPROM Control/Status Register (EEP_CONT_STAT), b6 (READBYTE) and b7 (PROMSIZE), write or read attributes for PDI and ECAT changed
		1533	30.14.2 PHY Address Register (PHY_ADR), b7 to b5 (reserved bits), write or read attributes for PDI and ECAT changed
		1533	30.14.3 PHY Register Address Register (PHY_REG_ADR), b7 to b5 (reserved bits), write or read attributes for PDI and ECAT changed
		1534	30.14.5 MII Management ECAT Access State Register (MII_ECAT_ACS_STAT), b7 to b1 (reserved bits), write or read attribute for ECAT changed
		1535	30.14.6 MII Management PDI Access State Register (MII_PDI_ACS_STAT), b7 to b2 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1538	30.15.3 FMMU Logical Start Bit m Register (FMMUm_L_START_BIT), b7 to b3 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1538	30.15.4 FMMU Logical Stop Bit m Register (FMMUm_L_STOP_BIT), b7 to b3 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1539	30.15.6 FMMU Physical Start Bit m Register (FMMUm_P_START_BIT), b7 to b3 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1540	30.15.7 FMMU Type m Register (FMMUm_TYPE), b7 to b2 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed

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1.00	Feb. 15, 2016	1540	30.15.8 FMMU Activate m Register (FMMUm_ACT), b7 to b1 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1542	30.16.3 SyncManager Control m Register (SMm_CONTROL), b7 (reserved bit), write or read attribute for ECAT changed
		1544	30.16.5 SyncManager Activate m Register (SMm_ACT), b5 to b2 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1545	30.16.6 SyncManager PDI Control m Register (SMm_PDI_CONT), b7 to b2 (reserved bits), descriptions partially deleted, write or read attribute for PDI changed
		1548	30.17.2.2 Receive Time ECAT Processing Unit Register (DC_RCV_TIME_UNIT), values after reset are added to each bit table
		1554	30.17.3.1 Cyclic Unit Control Register (DC_CYC_CONT), b3 to b1 (reserved bits) and b7, b6 (reserved bits), descriptions partially deleted, write or read attribute for ECAT changed
		1557	30.17.4.4 SYNC0 Status Register (DC_SYNC0_STAT), b7 to b1 (reserved bits), write or read attribute for PDI changed
		1557	30.17.4.5 SYNC1 Status Register (DC_SYNC1_STAT), b7 to b1 (reserved bits), write or read attribute for PDI changed
		1561	30.17.5.1 Latch 0 Control Register (DC_LATCH0_CONT), b7 to b2 (reserved bits), write or read attribute for ECAT changed
		1561	30.17.5.2 Latch 1 Control Register (DC_LATCH1_CONT), b7 to b2 (reserved bits), write or read attribute for ECAT changed
		31. USB2.0HS Host Module (USBh)	
		1611	31.3.2.5 USBCMD Register, b4 Periodic Schedule Enable, a note added
		1633	31.3.3.12 Offset E0h Register (EXT1), b12 changed (reserved → PSD),
		33. Serial Communications Interface with FIFO (SCIFA)	
		1802	33.2.12 Serial Port Register (SPTR), descriptions of the register partially deleted, a note added
		1814	Figure 33.4 Sample Flowchart for Transmitting Serial Data in Asynchronous Mode, a note added
		1832	33.8.4 Writing to the SPTR Register, newly added
		35. CAN Interface (RSCAN)	
		1912	Table 35.1 Specifications of the RSCAN, Tq in the item Communication speed changed
		1919	35.2.2 Channel Control Registers (RSCAN0CmCTR), the RTBO bit, descriptions partially changed (1 CAN bit time → One CANm bit time)
		1928	35.2.5 Global Configuration Register (RSCAN0GCFG), the DCS bit, descriptions partially changed, Table 35.4 Range of Operating Frequency Depending on the Transfer Rate and the Number of Channels in Use, deleted
		1943	35.2.17 Receive Buffer Number Register (RSCAN0RMNB), b7 to b0 (NRXMB[7:0]), descriptions partially changed
		2014	Table 35.14 Global Mode Transition Time, descriptions partially changed (CAN frame → CANm frame)
		2017	Table 35.15 Channel Mode Transition Time, descriptions partially changed (CANm frame → CANm frame (one message))
		2035	Figure 35.16 CAN Setting Procedure after the MCU is Reset, bit names are changed (GSLPR → GMDC, CSLPR → GHMDC), the register RSCAN0GAFLCFG1 deleted
		2037	Table 35.22 Example of Bit Timing Setting, 12 Tq, 24 Tq, and 25 Tq are added
		2038	Table 35.23 Example of Communication Speed Setting, frequencies changed (40 MHz, 16 MHz, and 8 MHz are deleted, 32 MHz was changed to 25 MHz)
		2041	Figure 35.21 Buffer Setting Procedure, the number of the receive buffers changed (0 to 31 → 0 to 32)
		36. Serial Peripheral Interface (RSPIa),	
		2074	36.2.5 RSPI Data Register (SPDR), bit map for the 16 higher-order bits added
		40. Boundary Scan	
		2230 to 2236	Table 40.5 Boundary Scan Register, package name corrected (320BGA → 320 FBGA)

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1.00	Feb. 15, 2016	41. ΔΣ Interface (DSMIF)	
		2270	41.2.30 Channel X Current Value Register 2 (X2DATA), the addresses are changed
		42. Error Control Module (ECM)	
		2286	42.2.2 ECM Master/Checker Error Clear Trigger Register (ECMmECLR (m = M or C)), the register symbol in the description corrected (ECMmEST → ECMmECT)
		43. 12-Bit A/D Converter (S12ADCa)	
		2345	Table 43.1 Specifications of 12-Bit A/D Converter, conversion time changed
		2346	Table 43.1 Specifications of 12-Bit A/D Converter, numbering of notes are changed
		2446	43.5.11 Allowable Signal Source Impedance, deleted
		46. RAM (Product Option)	
		2463	46.2.3 ECC Decoder Configuration Register (RAMEDC) (for Products Incorporating an R-IN Engine), descriptions partially changed (... for instruction RAM is enabled → ... for instruction RAM and data RAM are enabled)
		47. Electrical Characteristics	
		2477	Table 47.1 Absolute Maximum Rating, note 4 added
		2478	Figure 47.1 Power On/Off Sequence, notes 1 and 3 are changed
		2479	47.3 DC Characteristics, conditions are changed
		2479	Table 47.3 DC Characteristics (2) [Power Supply], Normal operation, values for VIcc changed, Standby mode with all modules inactive (reference value), units for the typical values of AV0Icc, AV1Icc, VRF0Icc, VRF1Ivcc are changed
		2483	47.4 AC Characteristics, conditions are changed
		2540	Table 47.32 ETHERC Timing, ETHERC (RMII), descriptions partially changed (ETHn_Txxx, ETHn_Rxxx, ETHn_Rxxx), values are added in T.B.D cells, ETHERC (MII), ETHn_TXER output delay time (tTERd) is added, note 1 changed
		2542	Figure 47.74 MII Transmission Timing, changed
		2542	Figure 47.75 MII Transmission Timing, changed
		2547	47.5 USB Characteristics, conditions are added
		2549	47.6 A/D Conversion Characteristics, conditions are added
		2551	47.7 Temperature Sensor Characteristics, conditions are added
		2554	Figure 47.90 Trace Interface Timing, changed
1.10	May 31, 2016	Feature	
		54	A feature added (maximum operating frequency of 300 MHz with 498 DMIPS)
		1. Overview	
		55	Table 1.1 Outline of Specifications, Cortex-R4F: Maximum operation frequency (320-pin FBGA) changed
		55	Table 1.1 Outline of Specifications, Clock generation circuit: CPU clock is modified
		56	Table 1.1 Outline of Specifications, VIC: Sources for peripheral function interrupts changed
		56	Table 1.1 Outline of Specifications, General-purpose I/O ports: Open-drain outputs for 320-pin FBGA and 176-pin HLQFP deleted
		57	Table 1.1 Outline of Specifications TPUa: Description for PWM output mode changed, Number of channels for cascaded-connected operation changed
		64	Table 1.3 List of Products: Four products are added
		66	Table 1.4 Pin Functions (1 / 7), Debug interface: Descriptions for TRST#, TMS, TDI, TDO, and TCK changed
		72	Table 1.4 Pin Functions (7 / 7), I/O ports (P30 to P37, PC0 to PC7): Input/output attribute and description changed
		73	Figure 1.2 Pin Arrangement (320-Pin FBGA) (Top View): Title changed
		74	Figure 1.3 Pin Arrangement (176-pin HLQFP), Pin numbers 35 and 37: Pin names changed
		83	Table 1.6 Pin Assignments (176-Pin HLQFP) (1 / 4), Pin numbers 35 and 37: Pin names changed

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1.10	May 31, 2016	90	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (4 / 10), F6: Newly added
		94	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10) T13, T15, T16, T18: Newly added
		95	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10) V14: Newly added
		4. Address Space	
		125	Figure 4.2 Memory Map (1-Mbyte Extended Internal SRAM): Note 1 added
		126	Figure 4.3 Memory Map (0-Kbyte Extended Internal SRAM): Note 4 deleted, statement “mirror area of” added
		126	Figure 4.3 Memory Map (0-Kbyte Extended Internal SRAM): Note 1 changed, Note 4 and 5 deleted (Note 6 moved up to Note 4)
		5. I/O Registers	
		179	Table 5.1 List of I/O Registers (Address Order) (52 / 86), XYZ overcurrent abnormality detection lower limit setting register (XYZIUNCMP) and XYZ overcurrent abnormality detection upper limit setting register (XYZIOVCMP): Addresses changed
		7. Clock Generation Circuit	
		227	7.2.1 System Clock Control Register (SCKCR), Bit table, b15, b14 (ETCKD[1:0]): Description for the value 11 changed
		232	7.2.4 PLL1 Control Register (PLL1CR), Bit table: Note 1 added (Previous note moved down to Note 2)
		9. Low-Power Consumption Function	
		254	Table 9.2 Stopping Peripheral Modules and Exiting Module-Stop State (2/ 2): Encoder interface added, Note 3 changed
		261	9.2.5 Module Stop Control Register E (MSTPCRE), Bit map and bit table: b0 (MSTPCRE0) added
		12. Interrupt Controller (ICUA)	
		375	12.4.6.2 Notes on Accessing HVA0 Register: Descriptions changed, program example and note added
		15. DMA Controller (DMACAa)	
		509	Figure 15.2 Relationship between DSKP and DCNT: Title changed
		552	Table 15.26 DMA Transfer Setting Example 2: Transfer source start address changed
		563	15.5.2 Setting Example 2 (Register Mode Software Request): N1SA transfer source address changed
		564	Figure 15.38 Setting Example 2: Addresses changed
		565	Table 15.27 DMA Transfer Setting Example 3: Transfer source start address changed
		565	15.5.3 Setting Example 3 (Register Mode Continuous Execution): Addresses of N0DA (transfer destination), N1SA (transfer source), and N1DA (transfer destination) changed
		566	Figure 15.39 Setting Example 3: Addresses changed
		568	Table 15.30 DMA Transfer Setting Example 4 (Descriptor 2): Transfer source start address changed
		568	Table 15.31 DMA Transfer Setting Example 4 (Descriptor 3): Transfer source/destination start addresses changed
		569	Table 15.32 Descriptor Settings, SA: Addresses for descriptor 1 and 3 changed, DA: Address for descriptor 3 changed
		17. I/O Ports	
		608	Figure 17.2 I/O Port Configuration (2), Note 1 changed
		609	Figure 17.2 I/O Port Configuration (3), Note 1 changed
		610	Figure 17.2 I/O Port Configuration (4), Note 1 changed
		611	Figure 17.2 I/O Port Configuration (5), Note 1 changed
		612	Table 17.3 Handling of Unused Pins: RES# and Port 33 (TDO) deleted
		18. Multi-Function Pin Controller (MPC)	
		646	18.2.5 P3n Pin Function Control Register (P3nPFS) (n = 0 to 7): Descriptions changed

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1.10	May 31, 2016	646	18.2.5 P3n Pin Function Control Register (P3nPFS) (n = 0 to 7): Description for ISEL changed
		19. Multi-Function Timer Pulse Unit (MTU3a)	
		905	Table 19.81 Output Pins for Channels 6 and 7, Note for Port group 1 changed, Note 3 changed
		20. Port Output Enable 3 (POE3)	
		969	Table 20.5 Correspondence between MTU and GPT Pins: Note 2 added
		28. Ethernet MAC (ETHERC)	
		1342	28.2.3.4 Hardware Function Return Value Register (R0, R1): Descriptions changed
		1342	28.2.3.4 Hardware Function Return Value Register (R0, R1), R0 bit table: b31 to b0 (R0B[31:0]), descriptions changed
		1342	28.2.3.4 Hardware Function Return Value Register (R0, R1), R1 bit table; b31 to b0 (R1B[31:0]), descriptions changed
		1346	Figure 28.4 Flow of Processing for Issuing the Hardware Function Call: Note 1 added
		29. Ethernet Switch	
		1386	29.2.1.1 Ethernet PHY LINK Mode Register (ETHPHYLNK), Bit table, b2 (CATLINK0) and b3 (CATLINK1): Erroneous description for value 1 corrected
		1389	29.2.1.4 Ether Switch 10-Mbps/Half-Duplex Mode Setting Register (ETHSW10HDEN), Bit map, b1 and b0: Value after reset changed
		1394	29.2.2.5 Input Learning Blocking Register (INPUT_LEARN_BLOCK): Erroneous register symbol corrected (LERAN → LEARN)
		31. USB2.0HS Host Module (USBh)	
		1683	Figure 31.13 Initial Setting Sequence: Terms changed (CPG → Clock)
		32. USB 2.0 HS Function Module (USBf)	
		1760	Figure 32.4 Startup Sequence: Terms changed (CPG → Clock)
		34. I2C Bus Interface (RIICa)	
		1837	Figure 34.1 RIIC Block Diagram, FMPE deleted
		1839	34.2.1 I2C Bus Control Register 1 (ICCR1): Index n added
		1879	34.3.5 Slave Transmit Operation: Steps (2) and (6) changed (ICSR1.HOA deleted)
		1882	34.3.6 Slave Receive Operation: Steps (2) and (5) changed (ICSR1.HOA deleted)
		35. CAN Interface (RSCAN)	
		1912	Table 35.1 Specifications of the RSCAN (1 / 2), Communication speed: Definition of Tq changed
		37. SPI Multi I/O Bus Controller (SPIBSC)	
		2148	37.2.1 Common Control Register (CMNCR), Bit table: Bit names of b17, b16 (MOIIO0[1:0]), b19, b18 (MOIIO1[1:0]), b21, b20 (MOIIO2[1:0]), and b23, b22 (MOIIO3[1:0]) changed
		2158	37.2.7 Data Read Option Setting Register (DROPR), Bit map: Bit symbol of b7 to b0 changed
		41. ΔΣ Interface (DSMIF)	
		2264	41.2.22 XYZ Status Register (XYZSTA), Bit map: b8 and b0 changed, Bit table: b0, b7, b8, and b9 changed
		2265	41.2.23 XYZ Overcurrent Abnormality Detection Lower Limit Setting Register (XYZIUNCMP): Address changed
		2266	41.2.24 XYZ Overcurrent Abnormality Detection Upper Limit Setting Register (XYZIOVCMP): Address changed
		2279	41.3.6 Setting Examples: Descriptions changed
		2279	Figure 41.9: Title changed, flows changed, Note 1 added
		2280	Figure 41.10 Operation when MCLKn is not Inverted: Terms changed (CPG → Clock generation circuit)
		2280	Figure 41.11 Operation when MCLKn is Inverted: Terms changed (CPG → Clock generation circuit)
		2281	41.5.1 Initial Settings for Error Sources after Release from the Module-Stop State: Descriptions changed, Note 1 changed

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1.10	May 31, 2016	42. Error Control Module (ECM)	
		2286	Table 42.2 ECM Error Input (1 / 2), Error source numbers 29 and 30: Functions changed
		2288	42.2.3 ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0 (m = M or C)), Bit map: b29 and b28 changed
		2288	42.2.3 ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0 (m = M or C)), Bit table: b28 and b29 changed
		2294	42.2.8 ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0), Bit map: b29 and b28 changed, Bit table: b28 and b29 changed, Bit names of b30 and b31 changed
		2299	42.2.11 ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0), Bit map: b29 and b28 changed
		2301	42.2.11 ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0), Bit table: b29 and b28 changed
		2304	42.2.14 ECM Internal Reset Configuration Register 0 (ECMIRCFG0), Bit map: b29 and b28 changed, Bit table: b28 and b29 changed, Bit name of b31 changed
		2309	42.2.17 ECM Error Mask Register 0 (ECMEMK0), Bit map: b29 changed
		2311	42.2.17 ECM Error Mask Register 0 (ECMEMK0), Bit table: b28 and b29 changed
		2314	42.2.20 ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0), Bit map: b29 and b28 changed
		2316	42.2.20 ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0), Bit table: b28 and b29 changed
		2319	42.2.24 ECM Protection Status Register (ECMPS), Bit table: R/W for b0 (ECMPRERR) changed, descriptions and R/W for b7 to b1 (reserved bits) changed
		2320	42.2.25 ECM Pseudo Error Trigger Register 0 (ECMPE0), Bit map: b29 and b28 changed
		2322	42.2.25 ECM Pseudo Error Trigger Register 0 (ECMPE0), Bit table: b28 and b29 changed
		2327	42.2.31 ECM Delay Timer Configuration Register 0 (ECMDTMCFG0), Bit map: b29 and b28 changed
		2329	42.2.31 ECM Delay Timer Configuration Register 0 (ECMDTMCFG0), Bit table: b28 and b29 changed
		2333	42.2.34 ECM Delay Timer Configuration Register 3 (ECMDTMCFG3), Bit map: b29 and b28 changed
		2335	42.2.34 ECM Delay Timer Configuration Register 3 (ECMDTMCFG3), Bit table: b28 and b29 changed
		2342	42.3.4.1 Protection Unlock Sequence, Description 1 changed
		43. 12-Bit A/D Converter (S12ADCa)	
		2346	Table 43.1 Specifications of 12-Bit A/D Converter (1 / 2): Descriptions changed (term CPG deleted)
		2446	43.5.12 Allowable Signal Source Impedance added
		44. Temperature Sensor	
		2451	Figure 44.2 Procedure for Using the Temperature Sensor: Content changed
		47. Electrical Characteristics	
		2477	Table 47.1 Absolute Maximum Rating: Note 5 added
		2480	Table 47.3 DC Characteristics (2) [Power Supply], Normal operation: VDD changed
		2485	Table 47.10 Operating Frequency, CPU clock (CPUCLK): Values for 320-pin FBGA changed, Note 1 added
		2556	Figure 47.90: Trance Interface Timing: Symbol corrected from RACECTR to TRACECTL
1.20	Mar. 02, 2017	1. Overview	
		62	Table 1.2 Comparison of Functions for Different Packages: Functions of ETHERC and ECATC, modified. Note 1 added.
		65	Figure 1.1 Block Diagram: Functional blocks of ECATC and ETHERC, modified. Note 1 modified.
		73	Figure 1.2 Pin Arrangement (320-Pin FBGA) (Top View): Pin ERROROUT#, modified

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1.20	Mar. 02, 2017	3. Operating Modes	
		113	Table 3.3 Parameter Information for the Loader in 16-bit or 32-bit Bus Boot Mode: Reference of Note 2, modified
		114	Table 3.4 Parameter Information for the Loader in SPI Boot Mode: Reference of Note 2, modified
		116	3.5.4.1 Operation Settings in SPI Boot Mode: Operation settings, added
		123	3.5.8.2 Serial Flash Memory in SPI Boot Mode, added
		9. Low-Power Consumption Function	
		259	9.2.2 Module Stop Control Register B (MSTPCRB): Notes 1 and 3 for the table of bits were modified.
		10. Debugging Interface	
		266	Figure 10.1 Block Diagram of CoreSight: Reference modified
		277	Figure 10.8 Example of Connection Circuit of an Emulator That Can Drive the nTRST Output to High: Waveforms when the emulator is not connected and when the emulator is connected, modified
		12. Interrupt Controller (ICUA)	
		288	12.2.4 Non-maskable Interrupt Status Register (NMISR), Description on the NMIST flag: [Setting condition] modified
		302	12.3.4 NMI Pin Interrupts: Description modified
		347	12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9), ISC1, Description on the ISCi bit: Suffix (n) modified
		348	12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9), ISC3, Description on the ISCi bit: Suffix (n) modified
		349	12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9), ISC5, Description on the ISCi bit: Suffix (n) modified
		350	12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9), ISC7, Description on the ISCi bit: Suffix (n) modified
		351	12.4.2.15 Interrupt Service Current Register n (ISCn) (n = 0 to 9), ISC9, Description on the ISCi bit: Suffix (n) modified
		352	12.4.2.16 Interrupt Address Store Register 0 (VADn) (n = 1 to 255) Interrupt Address Store Register 1 (VADn) (n = 256 to 300): Suffix modified (n → i)
		357	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (2 / 9): Vector number 50: Source of ETHPHYI2, modified
		365	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table: Note 4. added
		368	Figure 12.8 Register Rewrite Flow, modified
		377	12.4.6.5 Using Falling-Edge Detection with the NMI Pin, added
		16. Event Link Controller (ELC)	
		579	Table 16.2 Correspondence between the ELSRn Register and the Peripheral Functions: ELSR16, Encoder I/F trigger 0 (optional) and ELSR28, Encoder I/F trigger 1 (optional), added
		580	Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers (1 / 3): Encoder I/F, added
		597	Table 16.5 Operations of Modules When Event is Input: Encoder I/F, added
		17. I/O Ports	
		619	Table 17.3 Handling of Unused Pins: Handling of the TRST# and TCK pins, modified
		18. Multi-Function Pin Controller (MPC)	
		635	Table 18.1 List of Multiplexed Pin Configurations (16 / 21): PHYRESETOUT# was moved to the Ethernet controller (Ether0) section.
		20. Port Output Enable 3 (POE3)	
		937	Table 20.1 POE3 Specifications, Conditions for the high-impedance state: MTU complementary PWM output pins, modified
		971	Figure 20.4 Low-Level Detection Operation: PCLKB clocks, modified

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1.20	Mar. 02, 2017	21. General PWM Timer (GPTa)	
		1101	21.7.4 Output Protection Function for GTIOC Pin Output, (4) Restricted Specification of Output Protection Function: Description modified
		1103	21.9.2 Settings of GTCCRn during Compare Match Operation (n = A, B, C, D, E, F), (1) When automatic dead time setting has been made in triangle-wave PWM mode: Description modified
		24. Compare Match Timer (CMT)	
		1228	24.2.4 Compare Match Timer Control Register (CMCR): b7 (reserved bit) was added to the table of bits.
		28. Ethernet MAC (ETHERC)	
		1319	28.2.2.1 MIIM Register (GMAC_MIIM): Functional description on the RWDV bit, modified
		1320	28.2.2.3 TX RESULT Register (GMAC_TXRESULT): Description modified
		1322	28.2.2.5 RX MODE Register (GMAC_RXMODE): Register description modified. Functional description on the RX FIFO Read Trigger Threshold, Receive Almost Full Threshold, and Receive Almost Empty Threshold bits in the table of bits, modified.
		1325	28.2.2.6 TX MODE Register (GMAC_TXMODE): Register description modified. Functional description on the Transmit Almost Full Threshold and Transmit Almost Empty Threshold bits in the table of bits, modified. Note 1 added.
		1326	28.2.2.7 RESET Register (GMAC_RESET): Functional description modified
		1329	28.2.2.9 RX FLOW CONTROL Register (GMAC_FLWCTL): Register description modified
		1329	28.2.2.10 PAUSE Packet Register (GMAC_PAUSPKT): Register description modified
		1332	28.2.2.12 RX FIFO Status Register (GMAC_RXFIFO): Functional description on the RX FIFO Read Trigger bit in the table of bits, modified
		1333	28.2.2.13 TX FIFO Status Register (GMAC_TXFIFO): The TFULL bit was added to the bit chart and the table of bits.
		1334	28.2.2.14 TCPIPACC Register (GMAC_ACC): Functional description on the RX TCPIP accelerator enable bit in the table of bits, modified
		1335	28.2.2.16 LPI Mode Control Register (GMAC_LPI_MODE): Register description modified
		1337	28.2.2.18 Receive Buffer Information Register (BUFID): Register description modified
		1338	28.2.3.1 Hardware Function System Call Register (SYSC): Functional description on the SYSC[15:0] bits in the table of bits, modified. 5104h and 5114h, deleted.
		1344	Figure 28.3 Schematic Block Diagram of the Hardware Functions, modified
		1345	28.3.1.1 Initial Settings, Procedure for setting up the hardware functions: <3> modified, <4> added
		1347	28.3.1.3 Buffer Allocator, (1) Functional Overview: Description modified
		1350	28.3.1.3 Buffer Allocator, (2) Buffer Control Operation, (e) List of Hardware Function Calls: Description modified
		1354	Table 28.9 HWFNC_Buffer_Return: Function of R0[2:0] in return value registers, modified
		1354	28.3.1.4 MAC DMA Controller, (2) DMA for the reception MAC: Description modified
		1354	Figure 28.9 Outline of Processing by the Reception MACDMAC: Names of interrupts, modified
		1355	28.3.1.4 MAC DMA Controller, (2) DMA for the reception MAC, (a) Description of the individual functions of the MAC DMA controller: (2) description in 1-2) Full release of the buffer, modified
		1355	28.3.1.4 MAC DMA Controller, (2) DMA for the reception MAC, (a) Description of the individual functions of the MAC DMA controller: Description in 1-5) Judging whether a received frame is valid or invalid, modified
		1356	Figure 28.10 Conceptual Diagram of Judging Whether a Received Frame is Valid or Invalid, modified
		1360	Table 28.13 HWFNC_MACDMA_RX_Errstat: Function of R0[3:0] in return value registers, modified
		1363	Table 28.14 HWFNC_MACDMA_TX_Start: Functional description modified
		1364	28.3.1.5 Buffer RAM DMA Controller, (2) DMA transfer (a) Transfer between the buffer RAM and the data RAM: Description modified (b) Replacing data in the buffer RAM or data RAM: Description modified

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1.20	Mar. 02, 2017	—	28.3.1.5 Buffer RAM DMA Controller, (2) DMA transfer (c) Transfer from the buffer RAM to the buffer RAM, deleted
		—	Table 28.18 HWFNC_INTBUFF_DMA_Start, deleted
		—	Table 28.19 HWFNC_INTBUFF_DMA_Start (Descriptor), deleted
		1370	Figure 28.13 Format of Transmit Data: Modified, Note 2 deleted.
		1371	Figure 28.14 Transmission Frame Control Information, added
		1371	28.3.3.2 Creating transmit data, (1) Transmission frame control information: Description of ICRC in the table, modified. Contents description, modified.
		1372	28.3.3.2 Creating transmit data, (2) Ethernet frame Type/Length: Length added, description modified VLAN Tag, VLAN Info: Added
		1372	28.3.3.2 Creating transmit data, (2) Ethernet frame, (a) When the transmission TCPIP accelerator is enabled: Added
		1373	28.3.3.2 Creating transmit data, (2) Ethernet frame, (b) When the transmission TCPIP accelerator is disabled: Added
		1375	28.3.3.5 Completing transmission: Description modified
		1377	Figure 28.20 Format of Received Data, modified
		—	Figure 28.16 Format of Receive Data for Frames with the TPC/IP and UDP/IP Packets, deleted
		1378	Figure 28.21 Reception Frame Information, added
		1378	28.3.4.6 Format of receive data, (1) Reception frame information: FIFOFULL was modified to FIFOOVF in the table. Description on IPV6NG, OUT_OF_LIST, VTAG, and FIFOOVF was modified. Note 1, added.
		1380	28.3.4.6 Format of receive data, (2) Ethernet frame Type/Length: Length added, description modified VLAN Tag, VLAN Info: Added FCS: Description modified
		1380	Figure 28.22 Destination MAC Address Field when Insertion of Management Tags is Permitted, modified
		1380	28.3.4.6 Format of receive data, (2) Ethernet frame, (a) If insertion of management tags is permitted: Note added
		1381	28.3.4.6 Format of receive data, (2) Ethernet frame, (b) When the reception TCPIP accelerator is enabled and TCP/UDP packet data is not included: Added
		1382	28.3.4.6 Format of receive data, (2) Ethernet frame, (c) When the reception TCPIP accelerator is enabled and TCP/UDP packet data is included: Added
		1383	28.3.4.6 Format of receive data, (2) Ethernet frame, (d) When the reception TCPIP accelerator is disabled: Added
		1384	28.3.5 TCPIP Accelerator, added
		1384	28.3.5.1 Transmission with Use of the TCPIP Accelerator, added
		1385	28.3.5.2 Reception with Use of the TCPIP Accelerator, added
		1387	28.4.1 Padding added to the MAC header in the transmit frame: Description modified
		1387	28.4.2 Misjudgment of the Result of Checksum Calculation by Hardware in Reception, added
		1387	28.4.3 Setting of the Module Stop Function Description modified: MSTPCRB.MSTPCRB14 to MSTPCRB17 → MSTPCRB.MSTPCRB16 to MSTPCRB19
		29. Ethernet Switch	
		1396	29.2.2.2 Unicast Default Mask Register (UCAST_DEFAULT_MASK): Functional description on the P0UCASTDM, P1UCASTDM, and P2UCASTDM bits, modified
		1397	29.2.2.3 Broadcast Default Mask Register (BCAST_DEFAULT_MASK): Functional description on the P0BCASTDM, P1BCASTDM, and P2BCASTDM bits, modified
		1398	29.2.2.4 Multicast Default Mask Register (MCAST_DEFAULT_MASK): Functional description on the P0MCASTDM, P1MCASTDM, and P2MCASTDM bits, modified

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1.20	Mar. 02, 2017	1482	29.3.4.3 Adjustable Timer Module, (1) Overview: Description modified (nanosecond-timer reaches: 109 → 10^9)
		1495	29.4.4 Setting of Module Stop Function: Description modified
		30. EtherCAT Slave Controller (optional)	
		1578	30.18.5 Setting the Module-Stop Function: Description modified
		1578	30.19 Initial Settings, added
		33. Serial Communications Interface with FIFO (SCIFA)	
		1821	Figure 33.5 Example of Transmit Operation in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit when LSB-First Transfer is Selected), modified (ICU.IRn → ICU.RAISn)
		1824	Figure 33.9 Example of SCIFA Receive Operation in Asynchronous Mode (8-Bit Data with Parity and One Stop Bit when LSB-First Transfer is Selected), modified (ICU.IRn → ICU.RAISn)
		1829	Figure 33.14 Example of SCIFA Transmit Operation in Clock Synchronous Mode (when LSB-First Transfer is Selected), modified (ICU.IRn → ICU.RAISn)
		1831	Figure 33.16 Example of SCIFA Receive Operation (when LSB-First Transfer is Selected), modified (ICU.IRn → ICU.RAISn)
		34. I^2C Bus Interface (RIICa)	
		—	34.12.1 Buffer Operation for TXI and RXI Interrupts, deleted
		—	34.15.2 Notes on Starting Transfer, deleted
		36. Serial Peripheral Interface (RSPIa)	
		2080	36.2.5 RSPI Data Register (SPDR): Bit chart of the SPDR register when accessing in words (the SPLW bit is 0), modified (b31 to b16 → b15 to b0)
		37. SPI Multi I/O Bus Controller (SPIBSC)	
		2154, 2155	37.2.1 Common Control Register (CMNCR): Description on the IO0FV[1:0], IO2FV[1:0], IO3FV[1:0], MOIIO0[1:0], MOIIO1[1:0], MOIIO2[1:0], and MOIIO3[1:0] bits in the table of bits, modified
		2171	37.2.14 SPI Mode Read Data Register 0 (SMRDR0): Register description, modified
		2171	37.2.15 SPI Mode Write Data Register 0 (SMWDR0): Register description, modified
		2177	Figure 37.4 Data Alignment in External Address Space Read Mode, modified
		2177	Figure 37.5 Data Alignment in SPI Operating Mode, modified
		40. Boundary Scan	
		2235	40.2.4 Boundary Scan Register (JTBSR): Description modified
		2236 to 2242	Table 40.5 Boundary Scan Register (320FBGA), modified
		2243 to 2246	Table 40.6 Boundary Scan Register (176QFP), added
		2250	40.4 Usage Notes: Notes no. 6, 8, 12, and 16 were added
		42. Error Control Module (ECM)	
		2293	Table 42.2 ECM Error Input (1 / 2): Functions of error source numbers 5 and 6, modified
		2295	42.2.1 ECM Master/Checker Error Set Trigger Register (ECMmESET (m = M or C)): Error of bit names in Notes 2 and 6, modified (ECMIE228 bit →ECMMIE228 bit)
		2297	42.2.3 ECM Master/Checker Error Source Status Register 0 (ECMmESSTR0 (m = M or C)): Description of bits ECMmSSE004 and ECMmSSE005, modified
		2303	42.2.8 ECM Maskable Interrupt Configuration Register 0 (ECMMICFG0): Description of bits ECMMIE004 and ECMMIE005, modified
		2308	42.2.11 ECM Non-maskable Interrupt Configuration Register 0 (ECMNMICFG0): Description of bits ECMNMIE004 and ECMNMIE005, modified
		2313	42.2.14 ECM Internal Reset Configuration Register 0 (ECMIRCFG0): Description of bits ECMIRE004 and ECMIRE005, modified
		2318	42.2.17 ECM Error Mask Register 0 (ECMEMK0): Description of bits ECMEMK004 and ECMEMK005, modified

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1.20	Mar. 02, 2017	2323	42.2.20 ECM Error Source Status Clear Trigger Register 0 (ECMESSTC0): Description of bits ECMCLSSE004 and ECMCLSSE005, modified
		2328	42.2.23 ECM Protection Command Register (ECMPCMD1): Symbol of b7 to b0 in the table of bits, modified (ECM1REG7 to ECM1REG0 →ECM1REG[7:0])
		2329	42.2.25 ECM Pseudo Error Trigger Register 0 (ECMPE0): Description of bits ECMPE004 and ECMPE005, modified
		2336	42.2.31 ECM Delay Timer Configuration Register 0 (ECMDTMCFG0): Description of bits ECMTE004 and ECMTE005, modified
		2342	42.2.34 ECM Delay Timer Configuration Register 3 (ECMDTMCFG3): Description of bits ECMTE304 and ECMTE305, modified
		43. 12-Bit A/D Converter (S12ADCa)	
		2455	Table 43.13 Analog Pin Specifications: Note added
		46. RAM (Product Option)	
		2469	Table 46.1 Specifications of RAM: Description on the error checking, modified
		2470	46.2.1 Protect Command Register (RAMPCMD): Description on step 2, modified
		47. Electrical Characteristics	
		2490	Table 47.3 DC Characteristics (2) [Power Supply] Test conditions, modified: Product part no. added
		2491	Table 47.4 DC Characteristics (3) [Except for USB2.0 Host/Function-Related Pins] Item modified: "Input pull-up MOS current and resistance" and "Input pull-down MOS current and resistance" R_{pu1}, R_{pu2}, R_{pd1}, and R_{pd2} were added. Test conditions for "Input pull-down MOS current and resistance" were modified.
		2494	Table 47.10 Operating Frequency: Notes 1 to 3, added. The max. value of the CPU clock (CPUCLK), modified.
1.30	Apr. 25, 2017	1. Overview	
		102	Table 1.8 List of Pin and Pin Functions (176-Pin HLQFP) (6/6): The communication function of pin 171, modified
		3. Operating Modes	
		109	3.1 Overview: The description, modified
		5. I/O Registers	
		155	Table 5.1 List of I/O Registers (Address Order) (26/86): DCP configuration register (DCPCFG), deleted
		9. Low-Power Consumption Function	
		258	9.2.1 Module Stop Control Register A (MSTPCRA): The description, added
		259	9.2.2 Module Stop Control Register B (MSTPCRB): The description, added
		261	9.2.3 Module Stop Control Register C (MSTPCRC): The description, added
		262	9.2.4 Module Stop Control Register D (MSTPCRD): The description, added
		263	9.2.5 Module Stop Control Register E (MSTPCRE): The description, added
		263	9.2.6 Module Stop Control Register F (MSTPCRF): The description, added
		264, 265	9.3.1 Module-Stop Function: The description (procedure, description of procedures, table 9.3), added
		12. Interrupt Controller (ICUA)	
		365	Table 12.3 Cortex-R4F/DMAC Interrupt Vector Table (7/9): Vector Number 214 and 215, modified
		371	Figure 12.8 Register Rewrite Flow: The processing, modified
		13. Internal Buses	
		386	Table 13.1 Specifications of Internal Buses: The contents of external serial flash bus, modified (PCLKD → ICLK)
		387	Figure 13.1 Bus Configuration: Serial Flash (PCLKD) → Serial Flash, modified

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1.30	Apr. 25, 2017	388	Figure 13.2 Bus Configuration (for products incorporating an R-IN engine): Serial Flash (PCLKD) → Serial Flash, modified
		15. DMA Controller (DMACAa)	
		577	15.6 Usage Notes: The note, added
		19. Multi-Function Timer Pulse Unit (MTU3a)	
		696	19.2.1 Timer Control Register (TCR): The functional description of the TPSC[2:0] bits in the table of bits, modified (The reference, modified)
		812	19.3.6, (4) 32-bit Phase Counting Mode Application Example: The description, modified
		880	19.4.2, (1) DMAC Activation: The description, deleted
		20. Port Output Enable 3 (POE3)	
		978	20.6.1 Transition to Low Power Consumption Mode: Deleted
		28. Ethernet MAC (ETHERC)	
		1328	28.2.2.6 TX MODE Register (GMAC_TXMODE): The functional description of the TEMPTH[2:0] bits in the table of bits, modified
		32. USB 2.0 HS Function Module (USBf)	
		1777	Table 32.23 Pipe Settings: The DCPCFG register, deleted
		1779	32.5.3 Pipe Control Register Switching Procedures: The DCPCFG register, deleted
		37. SPI Multi I/O Bus Controller (SPIBSC)	
		2155	Table 37.1 SPIBSC Specifications: The contents of the bit rate, modified (PCLKA → ICLK)
		2156	Figure 37.1 Block Diagram of SPIBSC: PCLKA → ICLK, modified
		2162	37.2.3, (1) Bit Rate: PCLKA → ICLK, modified
		2162	Table 37.3 Relationship between SPBR[7:0] and BRDV[1:0] Settings: Bit Rate, PCLKA → ICLK, modified. Setting of bits SPBR[7:0] and BRDV[1:0]: 0,1, 0,2, and 0,3, added.
		47. Electrical Characteristics	
		2547	Figure 47.60 SPIBSC Transmit/Receive Timing (CPHAT = 0, CPHAR = 1): Modified
1.40	Jan. 19, 2018	All	Cortex-R4F changed to Cortex-R4
			Terms corrected (Ether Switch → Ethernet switch; Ether Mac → Ethernet Mac; Ether PHY → Ethernet PHY; Ether clock(s) → Ethernet clock(s); receive buffer(s) → reception buffer(s); transmit buffer(s) → transmission buffer(s); transmit/receive buffer(s) → transmission/reception buffer(s); transmit mode → transmission mode; receive mode → reception mode; compare match counter (CMCNT) → compare match timer counter (CMCNT); compare match constant register (CMCOR) → compare match timer constant register (CMCOR); low active → active low; high active → active high; valley → trough)
		Features	
		54	■ Encoder interfaces, changed ■ Various communications interfaces: Features of Ethernet changed
		1. Overview	
		55	1.1 Outline of Specifications: "Cortex®-R4F processor" changed to "Cortex®-R4 processor with FPU"
		55	Table 1.1 Outline of Specifications (1 / 7): Registered trademark symbol added to "Thumb"; description of "Clock" changed
		61	Table 1.1 Outline of Specifications (7 / 7): Description of the encoder interfaces changed
		69	Table 1.4 Pin Functions (4 / 7): CTS0# to CTS4#: I/O and functional description changed; RTS0# to RTS4#: Functional description changed
		72	Table 1.4 Pin Functions (7 / 7): ENCIF07 to ENCIF12 changed to ENCIF00 to ENCIF12
		75	Table 1.5 Pin Assignments (320-Pin FBGA) (1 / 8): ENCIF12 added to B19; ENCIF11 added to B20
		76	Table 1.5 Pin Assignments (320-Pin FBGA) (2 / 8): ENCIF10 added to C19; ENCIF09 added to D19; ENCIF08 added to E19
		77	Table 1.5 Pin Assignments (320-Pin FBGA) (3 / 8): ENCIF11 added to H19; ENCIF12 added to H20

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1.40	Jan. 19, 2018	78	Table 1.5 Pin Assignments (320-Pin FBGA) (4 / 8): ENCIF10 added to J19
		79	Table 1.5 Pin Assignments (320-Pin FBGA) (5 / 8): ENCIF09 added to N20; ENCIF08 added to P20
		80	Table 1.5 Pin Assignments (320-Pin FBGA) (6 / 8): ENCIF09 added to U3
		81	Table 1.5 Pin Assignments (320-Pin FBGA) (7 / 8): ENCIF10 added to W3; ENCIF11 added to W4; ENCIF08 added to W10; ENCIF12 added to Y4
		88	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (2 / 10): ENCIF12 added to B19 under "Others"; ENCIF11 added to B20 under "Others"
		89	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (3 / 10): ENCIF10 added to C19 under "Others"; ENCIF09 added to D19 under "Others"; ENCIF08 added to E19 under "Others"
		91	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (5 / 10); ENCIF11 added to H19 under "Others"; ENCIF12 added to H20 under "Others"; ENCIF10 added to J19 under "Others"
		93	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (7 / 10): ENCIF09 added to N20 under "Others"; ENCIF08 added to P20 under "Others"
		94	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (8 / 10): ENCIF09 added to U3 under "Others"
		95	Table 1.7 List of Pin and Pin Functions (320-Pin FBGA) (9 / 10): ENCIF10 added to W3 under "Others"; ENCIF11 added to W4 under "Others"; ENCIF08 added to W10 under "Others; ENCIF12 added to Y4
		3. Operating Modes	
		113	Table 3.3 Parameter Information for the Loader in 16-bit or 32-bit Bus Boot Mode: Offset address of DEST_ADDR_NML changed (0000 000Ch → 0000 001Ch)
		114	Table 3.4 Parameter Information for the Loader in SPI Boot Mode: Offset address of DEST_ADDR_NML changed (0000 000Ch → 0000 001Ch)
		115	3.5.3 Loader Program: Description modified
		115	Figure 3.3 Connection Diagram of This LSI with a Serial Flash Memory: Pins in serial flash memory changed (SI/SIO0 → SO/SIO1, SI/SIO1 → SI/SIO0)
		4. Address Space	
		125	Figure 4.1 Memory Map: Encoder I/F area (16 MB) added; Address 1000 0000h added to the USB; Note 2 changed; Note 9 added
		126	Figure 4.2 Memory Map (1-Mbyte Extended Internal SRAM): Encoder I/F area (16 MB) added; Address 1000 0000h added to the USB; Note 5 added
		127	Figure 4.3 Memory Map (0-Kbyte Extended Internal SRAM): Address 1000 0000h added to the USB
		5. I/O Registers	
		138	Table 5.1 List of I/O Registers (Address Order) (10 / 86): Interrupt level control register 8 (LVLC8) and interrupt level control register 9 (LVLC9) added
		152	Table 5.1 List of I/O Registers (Address Order) (24 / 86): Register name corrected (HcPeriodCurED register → HcPeriodicCurrentED register)
		153	Table 5.1 List of I/O Registers (Address Order) (25 / 86): Number of bits and access size of the CFIFO port register, D0FIFO port register, and D1FIFO port register changed
		180	Table 5.1 List of I/O Registers (Address Order) (52 / 86): XYZ short abnormality detection 0 data input threshold setting register and XYZ short abnormality detection 1 data input threshold setting register moved
		199	Table 5.1 List of I/O Registers (Address Order) (71 / 86): Event link setting register 16 (ELSR16) and event link setting register 28 (ELSR28) added
		210	Table 5.1 List of I/O Registers (Address Order) (82 / 86): Register symbol of the timer offset correction count register corrected (ATIME_CORR_OFFS → ATIME_OFFS_CORR)
		211	Table 5.1 List of I/O Registers (Address Order) (83 / 86): PHY Port Status n Register (PHY_STATUSn) deleted
		6. Reset	
		215	Table 6.2 Targets to Be Initialized for Each Reset Type: Reset sources for RSTOUT# pin output and ERROROUT# pin output changed

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1.40	Jan. 19, 2018	7. Clock Generation Circuit	
		244	7.9.1 Notes on Clock Generation Circuit (7): Description in (7) corrected ("channels 0 to 45" → "channels 0 to 4")
		9. Low-Power Consumption Function	
		261	9.2.5 Module Stop Control Register E (MSTPCRE): Note 1 added to the bit table (MSTPCRE0 bit)
		10. Debugging Interface	
		281	Table 10.10 Available Trace Functions: Module name corrected (Cortex-R4 → Cortex-R4 (CR4), Cortex-M3 → Cortex-M3 (CM3))
		12. Interrupt Controller (ICUA)	
		285	Table 12.1 Specifications of Interrupt Controller: Note 2 modified (CR4F → CR4)
		286	Figure 12.2 Block Diagram of Interrupt Controller (for products incorporating an R-IN engine): MTU3a ch6.7 source selection (ISEL) deleted
		291	12.2.4 Non-maskable Interrupt Status Register (NMISR): "NMI Error Status Flag" in the bit table corrected to "ECM Error Status Flag"
		294	12.2.8 NMI Pin Digital Noise Filter Setting Register (NMIFLTC): Bits "b7 to b2" in the bit table changed to "b31 to b2"
		355	12.4.2.16 Interrupt Address Store Register 0 (VADn), Interrupt Address Store Register 1 (VADn): Description of the VADi[31:0] bits corrected
		358, 359	12.4.2.19 Interrupt Level Control Register n (LVLCn), added
		361	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (1 / 10): Request source for vector numbers 1 to 3 modified (System (CR4F) → System (CR4))
		365	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (4 / 10): Vector numbers 129 to 144: Encoder I/F (ENCINT0 to ENCINT15) added
		371	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table: Notes 5 and 6 added
		372	Figure 12.6 Initializing Registers of VIC: Processing changed (LVLCr added)
		373	12.4.4.2 Procedure for Rewriting the PLS, LVLCr, PRLM, VAD, and PRL Registers: LVLC register added
		375	12.4.4.3, (1) Specifying Interrupt Detection Types, Description changed
		375	Table 12.4 VIC Settings by Interrupt Detection Type: Interrupt request types LVCx1 and LVCx0 added
		384	12.4.6.6 Notes on Vector Settings, added
		386 to 389	Table 12.6 CM3 Interrupt Vector Table: DMAC setting vector numbers changed, Note 4 added
		14. Bus State Controller	
		394	Table 14.1 Bus State Controller Specifications: Note 1 added
		397	Table 14.3 Address Map: Note 1 added
		399	14.3.1 CSn Space Bus Control Register (CSnBCR): R/W for b8 to b0 changed
		403	14.3.2 CSn Space Wait Control Register (CSnWCR), (3), CS3WCR_1: Note 1 added
		424	14.3.7 Timeout Cycle Constant Register (TOSCORn): Description of b15 to b0 in the bit table modified
		428	14.3.10 CKIO Control Register (CIOSET): The description, modified
		473	Table 14.16 Output Addresses when EMRS Command Is Issued: Entries for CS2 MRS and CS3 MRS under "EMRS Command Issue Address", modified
		15. DMA Controller (DMACAa)	
		523	15.2.26 DMA Status SUS Register (DST_SUS_X (X = A or B)): Addresses corrected
		531	Figure 15.7 Link Mode Overview: "Memory" changed to "External memory"
		548	Table 15.21 DMA Transfer Request Detection Operation Setting Table (3 / 6): DMA transfer source for MTU3a corrected (TCID6 → TGID6)
		551	Table 15.21 DMA Transfer Request Detection Operation Setting Table: Note 4 added

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1.40	Jan. 19, 2018	16. Event Link Controller (ELC)	
		585	16.2.2 Event Link Setting Register n (ELSRn): n = 16, 28 added
		587	Table 16.3 Correspondence between Event Signal Names Set in ELSRn.ELS[7:0] Bits and Signal Numbers (1 / 3): Event signals set in ELSRn of the Ethernet controller changed
		595	16.2.8 Port Group Control Register n (PGCn): Symbol PGCInl[1:0] corrected to PGCIn[1:0]
		601	16.2.14 Event Link Option Setting Register I (ELOPI): Symbol GPT2MD corrected to GPT0MD
		17. I/O Ports	
		622	17.3.3 Port Input Register (PIDR): Address corrected
		626	Table 17.3 Handling of Unused Pins: Handling of EXTAL changed; USB_RREF pin added; Note 1 added
		18. Multi-Function Pin Controller (MPC)	
		647	Table 18.1 List of Multiplexed Pin Configurations (21 / 22): ENCIF08 to ENCIF12 added to "Encoder I/F"
		651	Table 18.3 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: PSEL[5:0] = 101011b added
		654	18.2.5 P3n Pin Function Control Register (P3nPFS): ISEL Bit (Interrupt Input Function Select), description added
		664	Table 18.17 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: Pin functions added to P94 and P96 for 101011b
		678	Table 18.30 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: PSEL[5:0] = 101011b added
		681	Table 18.33 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: PSEL[5:0] = 101011b added
		683	Table 18.35 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: Pin function added to PR1 for 101011b
		685	Table 18.37 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: Pin functions added to PT1, PT3, and PT7 for 101011b
		19. Multi-Function Timer Pulse Unit (MTU3a)	
		694	Table 19.1 Specifications of the MTU: Description of available operations of [MTU1, MTU2] changed
		696	Table 19.2 Functions of the MTU (2 / 3): Entries added to MTU6 and MTU7 for event link function (input)
		885	Table 19.78 MTU Interrupt Sources: Note 2 added
		929 to 934	Figures 19.164 to 19.171: Step numbers corrected ((8), (9) → (7), (8))
		20. Port Output Enable 3 (POE3)	
		962	20.2.12 Port Output Enable Control Register 2 (POECR2): Address corrected
		967	20.2.15 Port Output Enable Control Register 5 (POECR5): Symbols of b1, b2 and b4 corrected
		21. General PWM Timer (GPTa)	
		990	21.2.2 Noise Filter Control Register (NFCR): Symbol of b7 corrected
		1006	21.2.14 General PWM Timer Control Register (GTCR): CCLR[1:0] Bits: Description added; "CCLR[1:0] Bits (Counter Clear)" corrected to "CCLR[1:0] Bits (Counter Clear Source Select)"
		1007	21.2.15 General PWM Timer Buffer Enable Register (GTBER): PR[1:0] Bits: Description added
		1013	21.2.21 General PWM Timer Cycle Setting Register (GTPR): Description added
		1032	21.3.2.1 GTPR Register Buffer Operation: Description added
		—	Figure 21.14 Example of GTPR Buffer Operation (Saw Waves in Down-Count Operation), deleted
		1091, 1092	Figures 21.71 and 21.73: GPTR changed to GTPR
		22. 16-Bit Timer Pulse Unit (TPUa)	
		1159	22.3.3, (2) Examples of Buffer Operation, (a) When TPUm.TGRy is an output compare register: Title corrected (TPUm.TCNT → TPUm.TGRy)
		1163	22.3.4 Cascaded Operation: Note 2 added

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1.40	Jan. 19, 2018	1164	22.3.4, (2) Examples of Cascaded Operation: Description added
		1164	Figure 22.20 Example of Cascaded Operation (1): Waveforms of TPU1.TCNT and TPU2.TCNT clock signals changed
		1166	Table 22.25 PWM Output Registers and Output Pins: Description of note modified
		1203	22.9.16 Input Capture Operation in Cascaded Operation, added
		24. Compare Match Timer (CMT)	
		1235	Table 24.1 CMT Specifications: Entries as the number of internal channels changed
		1235	Figure 24.1 Block Diagram of CMT (Units 0 to 2): Units 1 and 2 added
		1238	24.2.4 Compare Match Timer Control Register (CMCR): Addresses added; Description of CKS[1:0] and CMIE in the bit table modified
		1239	24.2.5 Compare Match Timer Counter (CMCNT): Addresses added
		1239	24.2.6 Compare Match Timer Constant Register (CMCOR): Note 1 added; addresses added
		1241	24.4.2 Timing of Compare Match Interrupt Generation: Description modified
		25. Compare Match Timer W (CMTW)	
		1258	25.2.5 Compare Match Constant Register (CMWCOR): Description added
		26. Watchdog Timer (WDTA)	
		1289	Table 26.3 Relationship between Timeout Period and Window Start/End Counter Values: b1 and b0 added under "TOPS[1:0] Bits"
		1292	26.2.4 WDT Reset Control Register (WDTRCR): R/W for b6 to b0 changed
		28. Ethernet MAC (ETHERC)	
		1322	Table 28.3 I/O Pin Functions for ETHERC, added
		1334	28.2.2.5 RX MODE Register (GMAC_RXMODE): Note 1 added to the bit table (AFILLTEREN bit)
		1361	Table 28.7 HWFNC_LongBuffer_Get: Descriptions of argument registers and return value registers changed
		1362	Table 28.8 HWFNC_ShortBuffer_Get: Descriptions of argument registers and return value registers changed
		1362	Table 28.9 HWFNC_Buffer_Release: Descriptions of argument registers and return value registers changed
		1363	Table 28.10 HWFNC_Buffer_Return: Descriptions of argument registers and return value registers changed
		1368	28.3.1.4, (2) DMA for the reception MAC, (b) Usage: Bit name corrected (LBID[6:0] → LLID[6:0])
		1369	Table 28.11 HWFNC_MACDMA_RX_Enable: Descriptions of argument registers and return value registers changed
		1370	Table 28.12 HWFNC_MACDMA_RX_Disable: Descriptions of argument registers and return value registers changed
		1371	Table 28.13 HWFNC_MACDMA_RX_Control: Descriptions of argument registers and return value registers changed
		1371	Table 28.14 HWFNC_MACDMA_RX_Errstat: Descriptions of argument registers and return value registers changed
		1374	Table 28.15 HWFNC_MACDMA_TX_Start: Descriptions of argument registers and return value registers changed
		1374	Table 28.16 HWFNC_MACDMA_TX_Errstat: Descriptions of argument registers and return value registers changed
		1376	Table 28.17 HWFNC_Direct_Memory_Transfer: Description of "Function" partially deleted; descriptions of argument registers and return value registers changed
		1377	Table 28.18 HWFNC_Direct_Memory_Replace: Description of "Function" modified; descriptions of argument registers and return value registers changed
		1378	Table 28.19 Interrupts related to Operations for Transmission: TX FIFO error interrupt (ETHTFIE): Description under "Conditions for Asserting and De-asserting Interrupts" changed
		1382	28.3.3.2, (1) Transmission frame control information: Entries in the table below Figure 28.14 changed (descriptions of TX_WORD[12:0] and APAD modified); Note 2 added

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1.40	Jan. 19, 2018	1383	28.3.3.2, (2) Ethernet frame: Description changed
		1383	Figure 28.16 Format for Transmission Data (TCPIP Accelerator Enabled, VLAN Tag Included): VLAN tag (2 bytes) corrected to VLAN info (2 bytes)
		—	28.3.3.3 Creating transmit descriptors: Description of the restrictions deleted
		1388	28.3.4.6 Format of received data: Misdescription corrected
		1389	28.3.4.6, (1) Received frame information: Note 2 added to the table below Figure 28.21
		1395	Table 28.22 GMAC_ACC Register Settings and Transmission TCPIP Accelerator Operation: Note 2 added
		1396	28.3.5.2 Reception with Use of the TCPIP Accelerator: Description added Table 28.23 GMAC_ACC Register Settings and Reception TCPIP Accelerator Operation: Note changed
		1398	28.4.4 Misjudgment of the Result of Checksum Calculation in Reception, added
		1399 to 1403	28.4.5 Incorrect Information on Received Frames when the Reception FIFO Overflows, added
		1404, 1405	28.4.6 Incorrect Information on Received Frames with Size, Inclusive of Padding, Exceeding 64 Bytes, added
		29. Ethernet Switch	
		1425	29.2.2.13 Internal Queue Interface Status Register (QMGR_IFACE_STAT): Symbols of b2 to b0 in the bit chart corrected
		1435	29.2.3.1 Learning Record A Register (LRN_REC_A): Symbols modified
		1439	29.2.4.2 Maximum Frame Length Register n (FRM_LENGTHn) (Shared): Title corrected
		1464	29.2.6.4 DLR Interrupt Control Register (DLR_IRQ_CTRL): Symbol of b9 in the bit chart corrected
		30. EtherCAT Slave Controller (optional)	
		1520	30.3.2 EtherCAT Operation Mode Setting Register (CATEMMD): Symbol of b0 in the bit chart corrected
		1535	30.8.1 AL Control Register (AL_CONTROL): b5 (DEVICEID bit) added
		1536	30.8.2 AL Status Register (AL_STATUS): b5 (DEVICEID bit) added
		1541	30.9.3 PDI Configuration Register (PDI_CONFIG): Functional description of b7 to b5 (ONCHIPBUS bits) in the bit table changed (100 → 010)
		—	30.14.7 PHY Port Status n Register (PHY_STATUSn), deleted
		1596	30.20 Configuration of the Reset Circuit, added
		31. USB2.0HS Host Module (USBh)	
		1602	Table 31.1 Register Mapping List (1 / 2): Name of the HcPeriodCurED register at A004 001Ch corrected (HcPeriodCurrentED → HcPeriodicCurrentED)
		1618	31.3.1.11 HcBulkHeadED Register: Bit numbers of BulkHeadED[27:0] corrected
		1625	31.3.1.21 HcRhStatus_A, HcRhStatus_B Register, (1) HcRhStatus_A Register and (2) HcRhStatus_B Register: Bit numbers of reserved bits corrected
		1633	31.3.2.2 HCSPARAMS Register: Symbol of b7 in the bit chart corrected
		1666	31.3.4.8 Offset 34h Register (Capability Pointer): Bit numbers of reserved bits corrected
		33. Serial Communications Interface with FIFO (SCIFA)	
		1818, 1819	33.2.8 Bit Rate Register (BRR): Register symbol corrected (SMER → SEMR)
		1822	33.2.9 Modulation Duty Register (MDDR): [Asynchronous mode] o When the baud rate generator is in double-speed mode (SEMR.BGDM = 1): Value in the formula under (When operating on the base clock with a frequency 16 times the bit rate (SEMR.ABCS0 = 0)) corrected (64 → 16)
		1846	33.3.3, (3) Transmitting and Receiving Data: Receiving Serial Data (in Clock Synchronous Mode): Description changed
		1858	33.8.6 Receive Data Sampling Timing and Receive Margin in Asynchronous Mode: Description partially deleted

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1.40	Jan. 19, 2018	35. CAN Interface (RSCAN)	
		1964	35.2.15 Reception Rule Pointer 0 Registers (RSCAN0GAFLP0j): Symbol of b15 in the bit chart corrected
		2006	Table 35.5 TMTRSTSp Bit Assignment: Transmission buffer numbers corrected
		2007	Table 35.6 TMTARSTSp Bit Assignment: Transmission buffer numbers corrected
		2008	Table 35.7 TMTCSTSp Bit Assignment: Transmission buffer numbers corrected
		2009	Table 35.8 TMTASTSp Bit Assignment: Transmission buffer numbers corrected
		2010	Table 35.9 TMIEp Bit Assignment: Transmission buffer numbers corrected
		2016	Table 35.10 Transmission Buffers p Allocated to the Transmission Queue of Each Channel, changed
		2044	Table 35.18 Registers Initialized Only in Global Reset Mode: Register name corrected (RSCAN0RMNDy register → RSCAN0RMND0 register)
		2064	Figure 35.20 Buffer Configuration, changed
		36. Serial Peripheral Interface (RSPIa)	
		2111	36.2.14 RSPI Command Registers 0 to 7 (SPCMD0 to SPCMD7): b6 to b4 (SSLy[2:0] bits) in the bit table: Description of 010 and 011 corrected; register symbol corrected (SSLA[2:0] → SSLy[2:0])
		2115	Table 36.7 MOSI Signal Value Determination during SSL Negation Period: Note added
		37. SPI Multi I/O Bus Controller (SPIBSC)	
		2171	37.2.1 Common Control Register (CMNCR): Description of the CPHAR bit changed
		2187	37.2.13 SPI Mode Enable Setting Register (SMENR): Notes added to the description of the DME bit
		2189	37.2.14 SPI Mode Read Data Register 0 (SMRDR0): Description added
		2189	37.2.15 SPI Mode Write Data Register 0 (SMWDR0): Description added
		2198	Figure 37.8 Burst Read Operation Timing (SSLE Bit = 0), changed
		40. Boundary Scan	
		2266	Table 40.7 Explanation of States: "Select IR Scan" under "State" corrected
		41. ΔΣ Interface (DSMIF)	
		2270	Table 41.1 DSMIF Specifications: Description of functions changed (m = 0 to 2 → m = 0 to 2, 3)
		2291	41.2.22 XYZ Status Register (XYZSTA): b7 in the bit table moved
		43. 12-Bit A/D Converter (S12ADCa)	
		2374	Table 43.1 Specifications of 12-Bit A/D Converter (1 / 2): Specifications of "Conversion time" modified
		2385	43.2.2 A/D Self-Diagnosis Data Register (ADRD): o The settings for flush-left data with 10-bit accuracy: Bit name corrected (Converted Value 11 to 0 → Converted Value 9 to 0)
		2385	43.2.2 A/D Self-Diagnosis Data Register (ADRD): o The settings for flush-left data with 8-bit accuracy: Bit numbers corrected (b15 to b4 → b15 to b8) and bit name corrected (Converted Value 11 to 0 → Converted Value 7 to 0)
		2405	43.2.12 A/D Sampling State Register n (ADSSTRn): Address and values after reset changed
		46. RAM (Product Option)	
		2503	46.3.1 Configuration of Memory Map: Description modified
		47. Electrical Characteristics	
		2509	Table 47.3 DC Characteristics (2) [Power Supply]: Entries added to the "300MHz" row of VDD
		2521, 2522	Table 47.17 Bus Timing: "CKIO = 75MHz" changed to "CKIO = 1/tCKcyc; "tcyc" changed to "tCKcyc"; entries for "Address delay time 1", "CS# delay time 1", "Read/write delay time 1", "Read data setup time 1 to 3" and "WAIT# setup time" changed; Notes 1, 3, and 4 changed
		2558	Table 47.27 RSPIa Timing: Note 2 changed (SSLND → SPCKD): Note 3 added
		2567	Figure 47.64 RIICa Bus Interface Input/Output Timing: SDA0 to SDA3 and SCL0 to SCL3 deleted

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1.50	Jan. 17, 2019	All	The company name, modified (ARM → Arm)
		Features	
		55	■ Encoder interfaces (optional): The descriptions and related note 4, added
		Section 1 Overview	
		56	Table 1.1 Outline of Specifications (1/7): Central processing unit (Cortex-M3): The architecture type, corrected (Arm v7-R architecture → Arm v7-M architecture)
		56	Table 1.1 Outline of Specifications (1/7): On-chip extended SRAM with ECC: The entry "Operating frequency", added
		56	Table 1.1 Outline of Specifications (1/7): Operating modes: The description, modified
		57	Table 1.1 Outline of Specifications (2/7): DMAC: Activation sources, modified
		57	Table 1.1 Outline of Specifications (2/7): ELC: The number of event signals, modified
		58	Table 1.1 Outline of Specifications (3/7): TPUa: The descriptions for pulse input/output, PWM mode, PPG output trigger, event linking, modified
		58	Table 1.1 Outline of Specifications (3/7): MTU3a: The number of counter-input clock signals, modified; the feature "automatic transfer of register data", deleted; the description of phase-counting mode, modified
		59	Table 1.1 Outline of Specifications (4/7): CMT: Event linking, modified
		59	Table 1.1 Outline of Specifications (4/7): POE3: Pin names, corrected
		60	Table 1.1 Outline of Specifications (5/7): ETHERC: The description in relation with "1 port", modified
		61	Table 1.1 Outline of Specifications (6/7): SSI: "programmable word clock", deleted from the clock to be generated
		61	Table 1.1 Outline of Specifications (6/7): DSMIF: The description in relation with channel, modified
		62	Table 1.1 Outline of Specifications (7/7): Encoder interfaces: The number of channels and note 6, added
		66	Figure 1.1 Block Diagram: The number of channels of MTU3a and DSMIF, modified
		68	Table 1.4 Pin Functions (2/7): Pin names, modified (A0 to A25 → A25 to A0, D0 to D31 → D31 to D0); the "Description" column for RAS# and CAS#, modified
		69	Table 1.4 Pin Functions (3/7): The "Description" column for MTIOC8A to MTIOC8D and for GPTa, modified
		70	Table 1.4 Pin Functions (4/7): The "Description" column for each TPUa pin, modified
		71	Table 1.4 Pin Functions (5/7): Ethernet controller (ETHERC): ETH0_RXC, ETH1_RXC, ETH2_RXC: The "I/O" and "Description" columns, modified (I/O → Input, Receive clock I/O pins → Receive clock input pins)
		72	Table 1.4 Pin Functions (6/7): The AUDIO_CLK pin, added
		2. CPU	
		106	2.4.1 ATCM Wait Control Register: Note 1 to the bit table, modified
		109	2.5.2 Handling of Semaphore Register n: The section, added
		3. Operating Modes	
		111	3.4.1 Mode Monitor Register: Bit map: Value after reset for b24, modified
		112	3.5.1 Boot Function: Step (3), modified
		112	Figure 3.1 Operating Overview of Boot Processing: Step (3), modified
		113	Figure 3.2 Memory Assignment of the Loader Program and Parameters for the Loader: Note 3, modified
		114	Table 3.3 Parameter Information for the Loader in 16-bit or 32-bit Bus Boot Mode: Note 3, modified
		115	Table 3.4 Parameter Information for the Loader in SPI Boot Mode: Note 3, added (former note 3 renumbered as note 4)
		116	3.5.3 Loader Program: The descriptions for external memory storage address: The address range in 16-/32-bit bus boot mode, modified; the address range in SPI boot mode, added

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1.50	Jan. 17, 2019	117	Table 3.5 Setting Values of the Individual Peripheral Modules and Registers at the Time SPI Boot Mode Finishes: The "Setting Value at the Time the Boot Processing Finishes" column for the MSTPCRC, PORT6.PMR, and MPC.PmnPFS registers, modified
		121	Table 3.8 Setting Values of the Individual Peripheral Modules and Registers at the Time 16-bit or 32-bit Bus Boot Mode Finishes: The "Setting Value at the Time the Boot Processing Finishes" column for the MSTPCRC, PORTn.PMR, and MPC.PmnPFS registers, modified
		4. Address Space	
		126	Figure 4.1 Memory Map: Cortex-M3: A bit width and size of BitBand Alias Area0, modified (2200 0000h to 2300 0000h (16 MB) → 2200 0000h to 2400 0000h (32 MB)); notes 6 and 7, deleted
		127	Figure 4.2 Memory Map (1-Mbyte Extended Internal SRAM): The maps for A000 0000h Cortex-R4 and DMAC0/DMAC1: Peripheral I/O register (1MB): Note 3, added
		128	Figure 4.3 Memory Map (0-Kbyte Extended Internal SRAM): The maps for Cortex-R4 and DMAC0/DMAC1: B000 0000h to B100 0000h Encoder I/F area (16 MB); added, note 5, added
		5. I/O Registers	
		132	Table 5.1 List of I/O Registers (Address Order) (3/86): Access size for the DSCR register, modified
		153	Table 5.1 List of I/O Registers (Address Order) (24/86): The HcLSThreshold register, deleted
		154	Table 5.1 List of I/O Registers (Address Order) (25/86): Register names of DVSTCTR0, TESTMODE, and SOFCFG, modified
		155	Table 5.1 List of I/O Registers (Address Order) (26/86): The register name of UFRMNUM, modified
		155	Table 5.1 List of I/O Registers (Address Order) (26/86): The LPCTRL and PHYFUNCTR registers, deleted
		180	Table 5.1 List of I/O Registers (Address Order) (51/86): Register names of V1CDATA, V1VDATA, W1CDATA, and W1VDATA, modified
		182	Table 5.1 List of I/O Registers (Address Order) (53/86): Regitser name of RSCAN0FMSTS, modified
		214	Table 5.1 List of I/O Registers (Address Order) (85/86): Register names of GMAC_FLWCTL, GMAC_PAUSPKT, and GMAC_MIIM, modified
		6. Reset	
		221	6.3.1 RES# Pin Reset: The description in relation to a waiting time for PLL0 oscillation stabilization (tPL0WT), deleted
		221	6.3.2 ECM Reset: The description in relation to a waiting time for PLL0 oscillation stablization (tPL0WT), deleted
		221	6.3.3 Software Reset: The description in relation to a waiting time for PLL0 oscillation stablization (tPL0WT), deleted
		223	6.4 Usage Note: 6.4.1 Connection of Reset Output Pin (RSTOUT#), added
		7. Clock Generation Circuit	
		225	Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (1/2): The frequency of PCLKE, modified
		226	Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (2/2): The frequencies of CLMAPLCLK1 and TCLK, modified; note 1, added
		227	Figure 7.1 Block Diagram of Clock Generation Circuit: Clock names, modified (ACLK → AUDIO_CLK, AUDIOCLK → ATCLK)
		228	Figure 7.2 Block Diagram of Clock Generation Circuit (for products incorporating an R-IN engine): Clock names, modified (ACLK → AUDIO_CLK, AUDIOCLK → ATCLK)
		230, 231	7.2.1 System Clock Control Register: Bit table, modified (b13 (reserved) → b11 (reserved), b13 (reserved), added); the "Description" column for b20 (TCLK), modified
		233, 234	7.2.3 Delta-Sigma Interface Clock Control Register: Bit table: The description of the MCLK pin, modified
		235	7.2.4 PLL1 Control Register: Bit table: Note 1, modified
		238	7.2.6 Low-Speed On-Chip Oscillator Control Register (LOCOCR): The register name, modified (the low-speed on-chip oscillator control register → the LOCOCR register)

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1.50	Jan. 17, 2019	239	7.2.7 Oscillation Stop Detection Control Register (OSTDCR): Bit table: Note 1, modified
		240	7.3 Selecting Input to Main Clock Oscillator: The reference destination (table), corrected
		242	7.4.1 Oscillation Stop Detection and Operation after Detection: A section for reference, added
		243	7.8 Internal Clock: (9), CLMA clocks, modified
		244	7.8.9 USB Clock M (USBMCLK): The description, added
		244	7.8.12 CLMA Clock (CLMAMCLKA, CLMAMCLKB, CLMALCLK, CLMAPLCLK0, and CLMAPLCLK1): The title and body, modified
		244	7.8.14 ECM Clock (ECMCLK): The description, added
		245	7.8.16 Delta-Sigma Interface Clock 0 (DSCLK0): The description partially modified, (clock generation circuit → clock generation circuit (PLL0))
		245	7.8.17 Delta-Sigma Interface Clock 1 (DSCLK1): The description partially modified, (clock generation circuit → clock generation circuit (PLL0))
		245	7.8.19 Trace Interface Clock (TCLK): The description, added
		246	7.9.1 Notes on Clock Generation Circuit: The descriptions on (3) to (7), modified
		9. Low-Power Consumption Function	
		258	Table 9.2 Stopping Peripheral Modules and Exiting Module-Stop State (2/2): Ethernet MAC/HW-RTOS (for products incorporating an R-IN engine), added
		259	9.2 Register Descriptions: The body, modified
		270	9.4.5 Low Power Consumption for Ethernet-Related Functions: The description partially modified (the MSTPCRB.MSTPCRB14 to MSTPCRB17 bits → the MSTPCRB.MSTPCRB14 to MSTPCRB19 bits)
		10. Debugging Interface	
		271	10.1 Overview: A figure for reference, added
		271	Table 10.1 CoreSight Specifications: The description for trace port interface, modified
		276	Table 10.8 Configuration of Pins for the Debugging Interface: Note 1, modified
		280	10.3.3 Trace Port Interface: The description for 75 MHz, deleted
		11. Register Write Protection Function	
		287	11.2.1 Protect Register: The values represented by the suffix "i" of the PRCi bit, modified
		12. Interrupt Controller	
		288	12.1 Overview: The body, modified
		288	Table 12.1 Specifications of Interrupt Controller: Note 3, added
		291	12.2.1 IRQ Control Register i: A note, added
		293	12.2.3 IRQ Pin Digital Noise Filter Setting Register: The description for the FCLKSELi[1:0] bits, modified
		298	12.2.9 EtherPHY Control Register i: Bit table, modified (b7 to b4 (reserved) → b31 to b4 (reserved))
		299	12.2.10 Ethernet PHY Interrupt Request Pin Digital Noise Filter Enable Register: Bit table, modified (b31 to b2 (reserved) → b31 to b3 (reserved))
		302	12.2.13 External DMA Request Pin Digital Noise Setting Register: Bit table, modified (b7, b6 (reserved) → b31 to b6 (reserved))
		304	12.3.1 Selecting Interrupt Request Destinations: The body, modified; a note, added
		304	Figure 12.3 DMAC as the Interrupt Request Destination: The title, modified; the description, added
		305	Figure 12.4 CPU (Interrupt Controller) as the Interrupt Request Destination: The title, modified; the description, added
		306	12.3.2 Digital Noise Filter: The description in relation with the sampling cycle, modified
		307	12.3.3 External Pin Interrupts: The body, modified
		309	12.4 Cortex-R4 Vector Interrupt Controller (VIC), 12.4.1 Overview: The body, modified
		314	12.4.2.1 IRQ Status Register n, IRQS9: Bit table, modified (b6 to b0 (IRQ[300:288]) → b12 to b0 (IRQ[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))

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1.50	Jan. 17, 2019	319	12.4.2.2 Interrupt Input Status Register n, RAIS9: Bit table, modified (b6 to b0 (RAI[300:288]) → b12 to b0 (RAI[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		324	12.4.2.3 Interrupt Enable Register 0, IEN9: Bit table, modified (b6 to b0 (IEN[300:288]) → b12 to b0 (IEN[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		329	12.4.2.4 Interrupt Enable Clear Register n, IEC9: Bit table, modified (b6 to b0 (IEC[300:288]) → b12 to b0 (IEC[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		332	12.4.2.5 Interrupt Detection Type Selection Register n, PLS5: Erroneous vector number in the description of the PLSi bit (Interrupt Input Detection Type Selection) (i = 128 to 191), corrected (28 → 128):
		334	12.4.2.5 Interrupt Detection Type Selection Register n, PLS9: Bit table, modified (b6 to b0 (PLS[300:288]) → b12 to b0 (PLS[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		339	12.4.2.6 Edge Detection Bit Clear Register n, PIC9: Bit table, modified (b6 to b0 (PIC[300:288]) → b12 to b0 (PIC[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		341	12.4.2.8 Interrupt Priority Level Mask Register 1: Bit table: b15 to b0 (PRLM[15: 0]), description for the value 1, modified; the description for the PRLMi bit, modified
		351	12.4.2.14 Interrupt Service Status Register n, ISS9: Bit table, modified (b6 to b0 (ISS[300:288]) → b12 to b0 (ISS[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		357	12.4.2.15 Interrupt Service Current Register n, ISC9: Bit table, modified (b6 to b0 (ISC[300:288]) → b12 to b0 (ISC[300:288]), b31 to b7 (reserved) → b31 to b13 (reserved))
		358	12.4.2.16 Interrupt Address Store Register 0, Interrupt Address Store Register 1: The description for the VADi bit, modified
		361	12.4.2.19 Interrupt Level Control Register n, LVLC8: Bit map: Value after reset, partially modified; bit table: b0, b1 (reserved), the description, modified
		362, 363	12.4.2.19 Interrupt Level Control Register n, LVLC9: Bit map: Value after reset, partially modified; bit table: the bit symbol for b1, b0, modified; the "Description" column for b2 to b31 (reserved), modified
		380	12.4.4.3, (2) IRQ Interrupt (Level interrupt): The suffix, modified (m → n)
		384	Figure 12.11 Concept of Multiple Interrupts (2 / 2): The routine starting from interrupt request o (level 3), modified ("interrupt request 1 (level 1)" added after the interrupt request p (level 2))
		387	12.4.6.5 Notes on Vector Settings: The description, modified (offset addresses → addresses)
		393	12.6 Usage Notes: 12.6.1 Using “Falling-Edge” or “Rising and Falling Edges” Detection with the external pin interrupts, added
		393	12.6.2 Using Falling-Edge Detection with the NMI Pin, relocated (12.4.6.5 → 12.6.2)
		13. Internal Buses	
		394	Table 13.1 Specifications of Internal Buses: The bus type, modified (Memory bus 1, Memory bus 2 → Memory buses 1 and 2 (only for products incorporating an R-IN engine))
		395	Figure 13.1 Bus Configuration: Peripheral bus 1 (PCLKA) and ECAT, added
		396	Figure 13.2 Bus Configuration (for products incorporating an R-IN engine): Peripheral bus 1 (PCLKA) and ECAT, added
		397	Table 13.3 Internal Main Bus 2: Connection between Bus Master and Bus Slave: "AHB2DMA" is deleted from "AHB2DMA (Buffer RAM)", accessesibility from the CPU for Instruction RAM, Data RAM, and Buffer RAM, modified
		14. Bus State Controller	
		All	A request name, modified (timeout detection interrupt request → timeout detection error request)
		399	Figure 14.1 Block Diagram of Bus State Controller: Pin names, modified (BS → BS#, DQMxx → DQMUU, DQMUL, DQMLU, DQMLL, AH → AH#); the register name of CSnWCR, modified; note 1, added
		403, 404	14.3.1 CSn Space Bus Control Register: Bit table: b10, b9 (BSZ[1: 0]), note 1 in the description column, modified; b14-b12 (TYPE[2: 0]), note 2 added to the description column
		407	14.3.2 CSn Space Wait Control Register: (1) Normal Space, SRAM with Byte Selection, and MPX-I/O, CS0WCR_0, Bit table: b17, b16, b21, modified to reserved bits; b21 (reserved), the description, modified
		423	14.3.3 SDRAM Control Register: Bit table: The bit name of b10 (RMODE), modified (Refresh Control → Refresh Mode)

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1.50	Jan. 17, 2019	425	14.3.4 Refresh Timer Control/Status Register: Bit map: Bit symbol of b2 to b0, modified
		427	14.3.6 Refresh Time Constant Register: The body, modified (interrupt request → interrupt request (BSCCMI)); erroneous description of b7 to b0, corrected (8-Bit Counter → 8-Bit Register)
		428	14.3.7 Timeout Cycle Constant Register: The body, modified
		440	Figure 14.8 Wait Timing for SRAM Interface Access (Software Wait Only): The description, added
		441	Figure 14.9 Wait Cycle Timing for SRAM Interface Access (Wait Cycle Insertion Using WAIT# Signal): The description, added; the signal name, modified (WAIT → WAIT#)
		442	Figure 14.10 Active Period Expansion for the CSn Signal: The description, added
		443	Figure 14.11 Access Timing for MPX Space (1): The description, added
		444	Figure 14.12 Access Timing for MPX Space (2): The description, added
		445	Figure 14.13 Access Timing for MPX Space (3): The description, added
		446	Figure 14.14 Access Timing for MPX Space (4): The description, added
		447	14.4.6, (1) SDRAM Direct Connection: The suffix "x", added
		480	14.4.7 Burst ROM (Clocked Asynchronous) Interface: The reference destination (table), corrected
		481	Table 14.17 Relationship between Bus Width, Access Size, and Number of Bursts: Note 1, modified
		484	Figure 14.37 Wait Timing for SRAM with Byte Selection (BAS = 1) (SW[1:0] = 01b, WR[3:0] = 0001b, HW[1:0] = 01b): The title, modified (the suffix "b" indicating a binary number, added)
		15. DMA Controller (DMACAa)	
		491	Table 15.1 Specifications of DMAC: Channel priority, DMA mode (register mode/link mode), skip function, modified
		498	15.2.5 Current Destination Address Register: Address(es): Register symbol, modified (CRDA_C → CRDA_8)
		503, 504	15.2.7 Channel Status Register n: Bit table: b10 (DER), b16 (INTM), the descriptions, modified
		505	15.2.8 DMAC Unit 0 Source Select Register i: The body, modified; address(es): Module symbols, modified (ICU.DMA0SELx → DMA0.DMA0SELx)
		505	15.2.9 DMAC Unit 1 Source Select Register i: The body, modified; address(es): Module symbols, modified (ICU.DMA1SELx → DMA1.DMA1SELx)
		506	15.2.10 DMAC Software Activation Register: Address(es): Module symbol, modified (ICU.DMASTG → DMAC.DMASTG)
		509	15.2.12 Channel Control Register n: Bit table: The "Symbol" and "Description" columns for b7 (CLRDE), modified; the "Description" column for b12 (SETREN), modified
		510 to 513	15.2.13 Channel Configuration Register n: Bit table: The "Description" column for b3 (REQD), b10 to b8 (AM[2:0]), b20 (SAD), b21 (DAD), modified; note 1, added
		520	15.2.20 Destination Skip Register n: Address(es): Address modified (DSKP_15: A006 36E8 → DSKP_15: A006 36ECh)
		523	15.2.22 Descriptor Interval Register n: Bit table, modified (b7 to b1 (reserved) → b7 to b0 (reserved))
		535	15.3.1.2 Link Mode: The body, modified (memory area → memory area outside the DMAC)
		535	Figure 15.7 Link Mode Overview: A notation, modified (External memory → Memory)
		538	Table 15.12 Descriptor Format: The "Channel Extension" column, deleted
		539	Table 15.13 Description of activation in Table 15.12 Descriptor Format: “Channel Extension”, deleted
		539	Table 15.14 Descriptor Placement Example: DSCFM 1h address +18h, modified ("Extension" → "—")
		539	Figure 15.9 Header Area: The description, modified
		541	Figure 15.10 Header Area: The descriptions, corrected ("External memory" → "Memory", "DMA transaction" → "DMA transfer")
		542	15.3.1.2 Link Mode, (3) Descriptor settings, The bullet item "Notes on descriptors": The body, modified (LV = 0 → LV = 1)
		543	Figure 15.11 Header Area: The description, modified ("External memory" → "Memory")

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1.50	Jan. 17, 2019	545	Figure 15.12 Single Transfer Mode (REQD = 1, SDS > DDS): The description, added
		546	Figure 15.13 Block Transfer Mode (REQD = 0, SDS = DDS): The description, added
		546	15.3.3.1 Fixed Priority Mode: The body, modified
		546	Figure 15.14 Priority Levels Immediately after a Reset and Transfer through DMA Channel 0, added
		547	Figure 15.15 Fixed Priority Mode (Number of Channels Is 4, and REQD = 1): The description, added; the explanation regarding DMA request, modified
		547	15.3.3.2 Round-Robin Mode: The body, modified
		547	Figure 15.16 Priority Levels Immediately after a Reset and Transfer through DMA Channel 2, added
		551	Table 15.21 DMA Transfer Request Detection Operation Setting Table (2/6): DMA Transfer Request Source/S12ADCa Unit 0, S12ADCa Unit 1, the "TM" column under CHCFG_n, modified
		562	Figure 15.26 Software Forced Ejection Timing: The description partially modified ("Sweep write" → "Forced ejection (write)")
		563	Figure 15.27 Interval Count (REQD = 0, SDS < DDS): DREQ[1], DACK[1], CHITVL1, CH1 DMA transfer, deleted; the description, added
		564	Figure 15.28 DMA Transfer Settings and Interval Counts: Cases of REQD = 0, REQD = 1, the description, added
		564	15.3.8.1 When the Transfer Data Size on the Transfer Source is Small: The body, modified
		571	Table 15.23 Interrupt Sources of DMAC: An interrupt source name, corrected ("Descriptor inbound" → "Descriptor invalid"); output condition, modified (DRRP bit → DRRP and DIM bits)
		573	Table 15.25 DMA Transfer Setting Example 1: The item "AHB setting", deleted
		575	Table 15.26 DMA Transfer Setting Example 2: The item "AHB setting", deleted
		577	Table 15.27 DMA Transfer Setting Example 3: The item "AHB setting", deleted
		585	15.6 Usage Notes: Notation, modified (SKIP transfer → skip transfer)
		16. Event Link Controller (ELC)	
		All	Throughout the section, the expressions related to restarting a counter, modified to those meaning clearing of a counter
		588	Table 16.1 ELC Specifications, Event link function: The number of event signals, modified
		589	16.2.2 Event Link Setting Register n: Address(es): The ELSR16, ELSR28 registers, added; note 1, added
		600	16.2.9 Port Buffer Register n: Bit table:The "Description" column, modified
		604	16.2.13 Event Link Option Setting Register H (ELOPH): Bit name, modified (CMTW Operation Select → CMTW0 Operation Select)
		607	Figure 16.2 Relation between Interrupt Handling and ELC (excluding the Ethernet MAC and EtherCAT): The title, modified; a block "Interrupt request (Event)", added
		608	16.3.2 Event Linkage: The body, modified
		608	Table 16.5 Operations of Modules When Event is Input: The modules MTU, CMT, CMTW, TPU, GPT: The "Operations When Event is Input" column, modified; the DSMIF module, added; I/O ports (output), I/O port (input), the "Operations When Event is Input" column, modified; note 1, added
		609	16.3.3, (2) Counting Clear Operation: The body, modified
		609	16.3.5, (1) Single ports and Port Groups: Register symbols, modified (PEL0 to PEL3 → PELn, PGCn → PGRn)
		610	16.3.5, (2) Single Input Port Operation upon Event Generation: The title and description, modified
		610	16.3.5, (3) Single Output Ports Operation upon Event Input: The description, modified
		610	Figure 16.3 Event Linkage Related to Single Ports (Port B), modified
		611	16.3.5, (4) Input Port Group Operation upon Event Generation: The title and description, modified
		611	16.3.5, (5) Input Port Group Operation upon Event Input: The entire paragraph added
		611	Figure 16.4 Input Port Group Operation upon Event Input (Port B), modified

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1.50	Jan. 17, 2019	—	16.3.5, (6) Operation of Port Buffer Registers, deleted
		612	16.3.5, (6) Output Port Group Operation upon Event Input: The title and description, modified
		612	Figure 16.5 Event Linkage Operation of Output Port Group (Port B), modified
		613	Figure 16.6 Bit-Rotating Operation of Output Port Groups (Port B), modified
		613	16.3.5, (7) Restrictions on Writing to PODR and PDBFn Registers by a CPU: The title and description, modified
		614	16.3.6 Example of Procedure for Linking Events: Step 2: Subheads, added
		615	16.4.1 Setting ELSR18 and ELSR19 Registers: The body, modified
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		618	Figure 17.1 I/O Port Configuration (1): Note 1, modified
		619	Figure 17.2 I/O Port Configuration (2): Note 1, modified
		620	Figure 17.3 I/O Port Configuration (3): Note 1, modified
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		622	Figure 17.5 I/O Port Configuration (5): Note 1, deleted
		623	17.3.1 Port Direction Register: The ports covered with the index m for 176-pin products, modified (ports K to N, R to U → ports 9, J to N, P, R to U)
		624	17.3.2 Port Output Data Register: The ports covered with the index m for 176-pin products, modified (ports K to N, R to U → ports 9, J to N, P, R to U)
		626	17.3.4 Port Mode Register: The ports covered with the index m for 176-pin products, modified (ports K to N, R to U → ports 9, J to N, P, R to U)
		628	17.3.6 Driving Ability Control Register: The body, modified
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		657	Table 18.6 Register Settings for the Input/Output Function in the 320-pin FBGA Pin: Note 1, note 2, added
		660	Table 18.9 Register Settings for the Input/Output Function in the 176-pin HLQFP Pin: Setting values 000011b and 001001b, deleted
		661	Table 18.11 Register Settings for the Input/Output Function in the 176-pin HLQFP Pin: Pins for the setting value 000000b, modified
		663	Table 18.13 Register Settings for the Input/Output Function in the 176-pin HLQFP Pin: Setting values 011001b and 011110b, deleted
		665	18.2.10 P8n Pin Function Control Register: ISEL bit: The description, added
		667	18.2.11 P9n Pin Function Control Register: ISEL bit: The description, added
		674	18.2.15 PDn Pin Function Control Register: The body, modified
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		19. Multi-Function Timer Pulse Unit (MTU3a)	
		698	Table 19.1 Specifications of the MTU: Operating frequency, modified, available operations [MTU1, MTU2], modified
		700	Table 19.2 Functions of the MTU (2/3): DMAC activation, modified
		701	Table 19.2 Functions of the MTU (3/3): Note 1, added (former note 1 renumbered as note 2)
		704	Table 19.3 Pin Configuration of the MTU: Function of the MTCLKA and MTCLKB pins, modified
		707	19.2.2 Timer Control Register 2: Register symbols, modified (TCRU/V/W → TCR2U/V/W)
		707	19.2.2 Timer Control Register 2: Bit table: b2 to b0 (TPSC2[2:0]): The "Description" column, modified (the reference destination table)
		710	Table 19.9 TPSC[2:0], TPSC2[2:0] (MTU3, MTU4, MTU6, MTU7, and MTU8): Note 1, deleted

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1.50	Jan. 17, 2019	714	Table 19.11 Operating Mode Setting by MD[3:0] Bits (MTU0 to MTU4, MTU6 to MTU8): The "Description" column for 0000b, modified
		715	19.2.5 Timer Mode Register 3: The description of the LWA and PHCKSEL bits, modified
		738	19.2.9 Timer Status Register: The body, corrected (MUT5 → MTU5); bit table: The "Description" column for b5 (TCFU), modified (description in relation with MTU8, deleted)
		740	19.2.9 Timer Status Register: TCFU Flag: the body, modified (description in relation with MTU8, deleted)
		744	19.2.13 Timer Counter: The body, modified; MTU8.TCNT: A note, added
		745	19.2.15 Timer General Register: Note to bit map for MTU8.TGRA, TGRB, TGRC, TGRD, added
		756	19.2.22 Timer Output Control Registers 1: The body, modified; bit table: b3 (TOCL): Note 4, added
		757	Figure 19.3 Example of Output in Complementary PWM Mode: Item names on Y axis, modified ("Positive phase output" → "Positive phase output (MTIOC4A)", "Negative phase output" → "Negative phase output (MTIOC4C)")
		762	19.2.25 Timer Gate Control Register A: Bit table: b0 (UF), b1 (VF), b2 (WF): The "Description" colum, modified (TGCR.FB → TGCRA.FB)
		788	Figure 19.7 Periodic Counter Operation: Item name on the chart, modified ("TCIV interrupt signal" → "TGI interrupt signal")
		789	19.3.1, (2) Waveform Output by Compare Match: The body, modified
		789	Figure 19.8 Example of Procedure for Setting Waveform Output by Compare Match: Step [3], modified
		791	19.3.1, (3) Input Capture Function: The body, modified (the MTIC5U, MTIC5V, and MTIC5W pins, added)
		793	19.3.2 Synchronous Operation: The description regarding MTU8, added
		800	19.3.4 Cascaded Operation: The body, modified ("when the MTU1.TMDR3.LWA bit is set to 0" → "when the MTU1.TMDR3.LWA bit is set to 1")
		809	Figure 19.29 Examples of PWM Mode Operation (PWM Waveform Output with 0% Duty and 100% Duty) (n = 0 to 4, 6, or 7): Case titles [1] to [3], added
		810	19.3.6 Phase Counting Mode: One of the registers in 32-bit phase counting mode, modified (TGR → TMDR1)
		810	Figure 19.30 Example of Phase Counting Mode Setting Procedure: Expression, modified ("A- or B-phase input signal" → "A- or B-phase input pin")
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		823	Figure 19.43 Procedure of Selecting 32-bit Phase Counting Mode: Throughout the steps, the letter "b"s for binary notation, added; Note, modified (TMDR → TMDR1)
		825	Figure 19.44 Procedure for Selecting Reset-Synchronized PWM Mode: Step [5], modified, box [9], modified
		835	Figure 19.50 Example of Operation in Complementary PWM Mode (MTU3 and MTU4): Items on the chart, modified ("Positive-phase output" → "Positive-phase output (MTIOC4A)", "Negative-phase output" → "Negative-phase output (MTIOC4C)")
		853, 854	Figure 19.68 to Figure 19.71: The title, modified ("TWCRB" deleted)
		859	Figure 19.78 Example of Counter Clearing Operation by MTU3.TGRA Compare Match: Items on the chart, modified ("Output waveform" → "Positive-phase output", "Output waveform#" → "Negative-phase output")
		873	Figure 19.93 Basic Example of A/D Converter Start Request Signal (TRG4AN) Operation: Legends MTU4.TADCORA and MTU4.TADCOBRA, relocated
		874	Figure 19.94 Example of A/D Converter Start Request Signal (TRG4AN) and Buffer Transfer Operation: Legends MTU4.TADCORA and MTU4.TADCOBRA, relocated
		908	19.6.12 Contention between MTU2.TCNT Write Operation and Overflow/Underflow in Cascaded Operation: Erroneous descriptions corrected (write cycle → writing)

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1.50	Jan. 17, 2019	913	19.6.20 Output Level in Complementary PWM Mode and Reset-Synchronized PWM Mode: Bit names, modified (TDER.TDER→TDERA.TDER (TDERB.TDER), TOCR1.OLSN → TOCR1A.OLSN (TOCR1B.OLSN), TOCR1.OLSP → TOCR1A.OLSP (TOCR1B.OLSP))
		915	19.6.25 Points for Caution to Prevent Malfunctions in Synchronous Clearing for Complementary PWM Mode: Erroneous description on the body, corrected
		949	19.8.2, (3) Clear Counting Operation: The title and body, modified
		20. Port Output Enable 3 (POE3)	
		953	20.2.1 Input Level Control/Status Register 1 (ICSR1): The body, modified (POE0# to POE3# pins → POE0# pin)
		954	20.2.2 Input Level Control/Status Register 2: The bit name for PIE2, modified
		957	20.2.5 Input Level Control/Status Register 5 (ICSR5): Note, modified; [Clearing condition] for the POE10F flag (POE10 flag), modified (POE11F → POE10F)
		958	20.2.6 Input Level Control/Status Register 6: OSTSTF flag, the body, modified
		962	20.2.9 Active Level Setting Register 1: OLSEN bit, the body, modified (the range covered by the index m, added)
		964	20.2.10 Software Port Output Enable Register: GPT3HIZ Bit, erroneous descriptions corrected (GPT23HIZ → GPT3HIZ)
		980	Table 20.4 Target Pins and Conditions for High-Impedance Control (2 / 2): Detailed conditions for the GPT3 pins, modified
		982	Table 20.5 Correspondence between MTU and GPT Pins: Note 2, modified
		21. General PWM Timer (GPTa)	
		All	The expressions related to restarting a counter, modified to those meaning clearing of a counter; representation of the letter n, modified (channel number → 0 to 3)
		988	Table 21.1 Specifications of GPT: Event counting, deleted; description in relation with transition to module-stop state, added
		990	Table 21.2 Functions of GPT (2 / 2): The item "Setting module-stop state", added
		991	Figure 21.1 Block Diagram of GPT: The register names of GTHPSR, GTCNT, GTDVU, GTDVD, GTDBU, GTDBD, modified
		1005, 1006	21.2.12 General PWM Timer I/O Control Register: OAHLD bit, OBHLD bit: The body, modified
		1023	21.2.29 General PWM Timer Dead Time Value Register m: Address(es): GPT1.GTDVU, modified
		1036	Figure 21.13 Example of GTPR Buffer Operation (Saw Waves in Up-Count Operation): Example operation of GTPBR, "dddd" added as a buffer content
		1038	Figure 21.15 Example for Setting GTPR Buffer Operation: Figure 21.14, deleted
		1100	21.6.2, (1) Start Counting: The title and description, modified
		1101	21.6.2, (3) Clear Counting: The title and description, modified
		1115	21.8.1 Pin Settings after Reset: The body, modified
		22. 16-Bit Timer Pulse Unit (TPUa)	
		All	The expressions related to restarting a counter, modified to those meaning clearing of a counter
		1118	Table 22.1 Specifications of TPU: Pulse input/output, settable operations, and interrupt source: "× 2 units", added
		1119	Table 22.2 TPU (Unit 0) Functions (1 / 2): DMAC activation: TGRB added as the target register
		1119, 1120	Table 22.2 TPU (Unit 0) Functions: Module-stop setting: Erroneous bit name, corrected; note 1, added (former notes 1 and 2 renumbered as notes 2 and 3)
		1120, 1121	Table 22.3 TPU (Unit 1) Functions: Module-stop setting: Erroneous bit name, corrected; note 1, added (former note 1 renumbered as note 2)
		1142	22.2.4 Timer Interrupt Enable Register: Bit table: Note 3, added
		1150	22.2.10 Noise Filter Control Register: Note 1, modified
		1152	22.2.11 PWM Feedback Select Register: Bit table: b4 to b2 (FBSL0[2:0]), R/W, added
		1153	Figure 22.3 PWM Feedback Setting and TPU Input Capture Configuration (Example of Unit 0): Interrupt source modules, corrected (GPU0 to GPU2 → GPT0 to GPT2)

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1.50	Jan. 17, 2019	1157	Figure 22.7 Example of Setting Procedure for Waveform Output by Compare Match: A suffix shown in the figure, modified (n → m)
		1167	22.3.4 Cascaded Operation: Erroneous suffix, corrected (TPUm.TCNT (n = 2, 5) → TPUn.TCNT (n = 2, 5); note 3, added
		1169	22.3.5 PWM Modes: The description, partially relocated; the paragraphs titled "1. PWM mode 1" and "2. PWM mode 2": The body, modified
		1173	Figure 22.25 Example of PWM Mode Operation (3): Case titels (a) to (c) and descriptions for each case, added
		1179	22.3.6.1 Phase Counting Mode Application Example: The body, modified
		1180	22.3.7 Noise Filters: The description in relation with the sampling condition, modified
		1181	22.3.8.1 Example Setting of PWM 1-Axis Measurement (TPU (Unit 0) is Set as the Internal PWM Feedback Input): The body, modified
		1182	Figure 22.33 Connection Diagram of Example Setting for PWM 1-Axis Measurement: Suffix m for TGRA and TGRB, deleted
		1183	22.3.8.2 Example Setting of PWM 2-Axes Measurement (TPU (Unit 0) is Set as the Internal PWM Feedback Input): The body, modified
		1184	Figure 22.34 Connection Diagram of Example Setting for PWM 2-Axes Measurement: Suffix m for TGRA and TGRB, deleted
		1185	22.3.8.3 Example Setting of PWM 1-Axis Measurement (TPU (Unit 0) Is Set as the Input Capture Function): The body, modified
		1186	Figure 22.35 Connection Diagram of Example Setting for PWM 1-Axis Measurement: Suffix m for TGRA and TGRB, deleted
		1187	22.3.8.4 Example Setting of PWM 2-Axes Measurement (TPU (Unit 0, Unit 1) Is Set as the Input Capture Function): The body, modified
		1188	Figure 22.36 Connection Diagram of Example Setting for PWM 2-Axes Measurement: Suffix m for TGRA and TGRB, deleted
		1191	22.4, (3) Underflow Interrupt: The number of interrupts, modified
		1191	22.5 DMAC Activation: The TPUm.TGRB register, added; the number of input capture/compare match interrupts, modified
		1193	Figure 22.40 Input Capture Signal Timing: The timing lines showing a rise on the input capture signal, modified
		1201	Figure 22.54 Conflict between Reading from the TPUm.TGRy Register and Input Capture: Notation in the figure, modified (buffer register → TPUm.TGRy register)
		1202	Figure 22.55 Conflict between Writing to the TPUm.TGRy Register and Input Capture: Notation in the figure, modified (TPUm.TCNT → TPUm.TGRy)
		1208	Table 22.32 Ability of Interrupt Sources to Serve as Event Signals for Transmission to the ELC: Channels 4 and 5, deleted; note 2, modified
		1208	22.10.2, (1) Start Counting: A sentence "by the ELOPF register of the ELC", added
		1209	22.10.2, (2) Clear Counting: The title and body, modified
		1209	Figure 22.63 Restart Counting on Reception of the Event Signal: Explanation added to the timing chart
		1210	22.10.2, (3) Input Capture Operation: The body, modified
		1211	22.10.3, (2) Clear Counting: The body, modified
		23. Programmable Pulse Generator (PPG)	
		1215	Table 23.2 Functions of the PPG: Symbols of the MTU3a and TPUa modules, modified
		1216	Figure 23.1 Block Diagram of PPG: Alternative group names added to each block for pulse output pins (groups 7 to 4)
		1220	23.2.3 Output Data Registers H (PODRH)/Output Data Registers L (PODRL): The body, modified
		1222	23.2.4 Next Data Registers H (NDRH), Next Data Registers L (NDRL): Address(es): Register symbols added
		1222, 1223	23.2.4, NDRH: (1), bullet items, modified; note 1, modified; (2), bullet items, modified

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		1225	23.2.5 PPG Output Control Register: The body, modified
		1227	23.2.6 PPG Output Mode Register: The body, modified
		1230	23.3 Operation: The body, modified
		1233	23.3.3 Example of Normal Pulse Output (Example of Five-Phase Pulse Output): The body, steps 1 to 4, modified
		1234	23.3.4 Non-Overlapping Pulse Output: The suffix for TGIA, modified (TGIAn → TGIAm (m = 0 to 3))
		1236, 1237	23.3.6 Example of Non-Overlapping Pulse Output (Example of Four-Phase Complementary Non-Overlapping Output): The body, steps 1 to 4, modified
		1239	23.3.8 Pulse Output Triggered by Input Capture: The body, modified
		24. Compare Match Timer (CMT)	
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		1240	Table 24.1 CMT Specifications: Event link function: The explanation supplemented ("only channel 1" → "only channel 1 of unit 0)
		1243	24.2.4 Compare Match Timer Control Register: b1, b0 (CKS[1:0]): The "Description" column, modified (CMCNTn counter → CMTn.CMCNT counter, CMSTR.STRn bit → CMSTRm.STRn bit); the description for suffix "m", added
		1244	24.2.5 Compare Match Timer Counter: Register symbol, modified (CMSTRn.STRm → CMSTRm.STRn); the description for suffixes "m" and "n", modified
		1245	24.3.1 Periodic Count Operation: Register symbol, modified (CMSTRn.STRm → CMSTRm.STRn)
		1247	24.5.1 Event Issuance to ELC: Register symbol, modified (CMCSRn.CMIE → CMT1.CMCR.CMIE)
		1248	24.5.2, (1) Count Start: Register-bit name, modified
		1248	Figure 24.6 Count Start Operation at Reception of an Event: Items on the chart, modified ("function select n" → "operation select", "Event input signal n" → " Event input signal", CMSTR.STRn → CMSTR0.STR1, CMCNTn → CMT1.CMCNT)
		1249	24.5.2, (2) Event Count: Register symbol and name, modified
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		1296	26.2.3 WDT Status Register: The body, modified
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		1304	Table 26.4 WDT Operation in Transition between Low-Power Consumption Modes <in Low-Power Consumption Mode Transition>: The column of VDD, deleted
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		1327	28.2.1.1 System Protect Command Register: Address(es): The address for access from the Cortex-M3, deleted
		1328	28.2.1.2 Ethernet MAC Reset Register: Address(es): The address for access from the Cortex-M3, deleted
		1331	28.2.1.5 MII Control Register: Bit table: Note 1, added
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		1341	28.2.2.7 RESET Register: Address(es): The address for access from the Cortex-M3, deleted, bit table: b14 (reserved bit), added
		1342, 1343	28.2.2.8 PAUSE Packet Data Register: Addresses of the GMAC_PAUSE1 to GMAC_PAUSE5 registers: The addresses for access from the Cortex-M3, deleted
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		1350	28.2.2.15 RX MAC ENABLE Register: Address(es): The address for access from the Cortex-M3, deleted
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		1353	28.2.3.1 Hardware Function System Call Register: The address for access from the Cortex-M3, deleted
		1354, 1355	28.2.3.2 Hardware Function Argument Register: Addresses of the R4 to R7 registers: The addresses for access from the Cortex-M3, deleted
		1357	28.2.3.4 Hardware Function Return Value Register: Addresses of the R0 and R1 registers: The addresses for access from the Cortex-M3, deleted
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		2484	43.4.1 Interrupt Requests: The body, modified (ADI and GBADI interrupts → S12ADI and S12GBADI interrupts)
		2484	Table 43.12 Relationship between Mode Setting and S12ADI Interrupt Output, modified (ADI interrupt → S12ADI interrupt, GBADI interrupt → S12GBADI interrupt)
		2488	43.5.6 Notes on Entering Low-Power Consumption States: The body, errorneous description corrected
		44. Temperature Sensor	
		2492	44.3.1 Preparation for Using the Temperature Sensor: The reference destination, modified
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		46. RAM (Product Option)	
		2503	46.1 Overview: Note, modified
		2505	46.2.2 ECC Decoder Configuration Register: The body, modified (the description for the cases of both 1-bit and 2-bit ECC errors, added)
		2511	46.2.6 2-Bit ECC Error Status Register: The body, modified
		2514	46.2.8 2-Bit ECC Error Address Register: Bit table: The erroneous description in the note, corrected; term unified (ECC 2-bit error → 2-bit ECC error)
		2515	46.2.9 2-Bit ECC Error Address Register: Bit table: The erroneous description in the note, corrected; term unified (ECC 2-bit error → 2-bit ECC error)
		2518	Figure 46.2 Example of ECC Error-Injection Setting Procedure: Figure title, added; the processing, modified
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		47. Electrical Characteristics	
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		2523	Table 47.3 DC Characteristics (2) [Power Supply] (1 / 2): VIcc when VDD is 300 MHz in normal operation, modified
		2526	Table 47.5 DC Characteristics (4) [USB2.0 USB_RREF Pin]: The "min" column, modified (200Ω ±1% → 200 ±1%); the "Ω" in the "Unit" column, added
		2530	Table 47.12 CLKOUT25Mn Timing, modified (CLKOUT25Mn (RMII): Tck → Tck1, CLKOUT25Mn (MII): Tck → Tck2)
		2530	Figure 47.3 CLKOUT25Mn Pin Output Timing 1: Symbols, modified
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		2531	Table 47.13 EXTAL Clock Timing: Time value, modified (40.00 + 50 ppm → 40.00 ± 50 ppm)
		2531	Table 47.14 XTAL Clock Timing: Time value, modified (40.00 + 50 ppm → 40.00 ± 50 ppm)
		2568	Table 47.24 GPTa Timing: The symbol, modified (T_{OTETW} → t_{GTEW})
		2572	Table 47.27 RSPIa Timing: Note 4, added
1.60	Nov. 30, 2020	All	Registered trademark symbol added (Arm → Arm®)
		All	Package name changed (HLQFP → HLFQFP)
		Features	
		55	Note 3 deleted (renumbering the subsequent note numbers: Note 4 → Note 3, Note 5 → Note 4)
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		57	Table 1.1 Outline of Specifications (2 / 7): VIC, NVIC: Peripheral function interrupts: Number of sources, modified
		58	Table 1.1 Outline of Specifications (3 / 7): TPUa: The footnote number for the number of units, modified
		59	Table 1.1 Outline of Specifications (4 / 7): IWDTa: The unit of frequency, modified

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		69	Table 1.4 Pin Functions (3 / 7): MTU3a: The function of pins MTIOC0m to MTIOC8m, modified
		69	Table 1.4 Pin Functions (3 / 7): GPTa: The function of pins GTIOC0A, GTIOC0B to GTIOC3A, and GTIOC3B, modified
		71	Table 1.4 Pin Functions (5 / 7): ETHERC: The function of pin ETHSWSECOUT, modified
		75	Figure 1.3 Pin Arrangement (176-pin HLFQFP): Note 2 added
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		114	Table 3.3 Parameter Information for the Loader in 16-bit or 32-bit Bus Boot Mode: Note 3 modified
		115	Table 3.4 Parameter Information for the Loader in SPI Boot Mode: 0000 0018h/LDR_SIZE_NML: The footnote number (*3) added; Note 3 modified
		116	3.5.3 Loader Program: The description of storage address in the external memory in SPI boot mode, modified
		4. Address Space	
		126	Figure 4.1 Memory Map: Cortex-M3: Text modified (BitBand Alias Area0 (32 MB) → BitBand Alias Area0 (16 MB))
		127	Figure 4.2 Memory Map: Cortex-R4: The description of "Mirror area of extended internal SRAM" modified
		5. I/O Registers	
		All	"EtherPHY" was modified to "Ethernet PHY"
		129	5. I/O Registers: The description modified
		205	Table 5.1 List of I/O Registers (Address Order) (76 / 86): Address A00B 0028h: The register name modified
		6. Reset	
		218	6.2.1 Reset Status Register 0 (RSTSR0): R/W in the table of bits, modified (R(/W) → R/(W))
		220	6.2.3 Software Reset Register 2 (SWRR2): Address(es) modified: (SWRR21 → SWRR2)
		221	6.3.4 Software Reset 2 (for products incorporating an R-IN engine): The register symbol modified (SWPR2 register → SWRR2 register)
		7. Clock Generation Circuit	
		224	7.1 Overview: The description modified
		227	Figure 7.1 Block Diagram of Clock Generation Circuit: Bus lines added
		228	Figure 7.2 Block Diagram of Clock Generation Circuit (for products incorporating an R-IN engine): Bus lines added
		229	Table 7.3 Pin Configuration of Clock Generation Circuit: The "Description" column, modified (EtherPHY → Ethernet PHY)
		237	7.2.5 PLL1 Control Register 2 (PLL1CR2): Table of bits: Note 1 modified
		239	7.2.7 Oscillation Stop Detection Control Register (OSTDCR): Table of bits: Note 1 modified
		242	7.4.1 Oscillation Stop Detection and Operation after Detection: The description modified
		243	7.8.2 System Clock (ICLK): The description modified
		243	7.8.3 High-Speed Peripheral Module Clock (PCLKA): The description modified
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		244	7.8.6 Low-Speed Peripheral Module Clocks (PCLKD, PCLKE, PCLKF, PCLKG, and PCLKH): The description modified
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		246	7.9.1 Notes on Clock Generation Circuit: The descriptions in (4), (6), (7), and (9), modified
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		256	8.3.2 Detecting Error Clock Frequency, (2) Method of calculating threshold values, CLMAnCMPL.CLMAnCMPL[11:0] and CLMAnCMPH.CLMAnCMPH[11:0], Example: For CLMA0: The upper-limit threshold, modified
		9. Low-Power Consumption Function	
		All	RIICa Unit → RIICa channel, SCIFA Unit → SCIFA channel, RSPIa Unit → RSPIa channel
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		12. Interrupt Controller (ICUA)	
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		304	12.3.1 Selecting Interrupt Request Destinations: The description modified
		307	12.3.3 External Pin Interrupts: The description modified
		308	12.3.4 NMI Pin Interrupts: The description modified
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		367	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (3 / 10): The request sources modified: RSPI unit 0 to RSPI unit 3, SCIFA unit 0 → RSPI ch0 to RSPI ch3, SCIFA ch0
		368	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (4 / 10): The request sources modified: SCIFA unit 1 to SCIFA unit 4, RIIC unit 0, RIIC unit 1 → SCIFA ch1 to SCIFA ch4, RIIC ch0, RIIC ch1
		372	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (8 / 10): The sources of vector numbers 242 and 243, modified
		373	Table 12.3 Cortex-R4/DMAC Interrupt Vector Table (9 / 10): The source of vector number 259, modified
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		391	Table 12.6 CM3 Interrupt Vector Table (3 / 4): The request sources modified: RSPI unit 0, RSPI unit 1 → RSPI ch0, RSPI ch1
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		396	Figure 13.2 Internal Bus Configuration (for products incorporating an R-IN engine): The title modified
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		408	14.3.2 CSn Space Wait Control Register (CSnWCR), (1) Normal Space, SRAM with Byte Selection, and MPX-I/O, CS1WCR: The bit names and functional descriptions of b1, b0 and b12, b11, modified (CSn# → CS1#)
		438	Figure 14.5 Example of 32-Bit Data-Width SRAM Connection: Text modified (OE → OE#)
		439	Figure 14.6 Example of 16-Bit Data-Width SRAM Connection: Text modified (OE → OE#)
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		442	14.4.4 CSn# Assert Period Expansion: Note added
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		447	14.4.6 SDRAM Interface, (12) Low-Power SDRAM: The description modified
		482	14.4.8 SRAM Interface with Byte Selection: The description modified (UB → UB#, LB → LB#)
		485	Figure 14.38 Example of Connection with 32-Bit Data-Width SRAM with Byte Selection: Text modified (OE → OE#, UB → UB#, LB → LB#)
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		487	14.4.10 Wait between Access Cycles: The description modified
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		All	"display" was modified to " indicate"
		491	15. DMA Controller (DMACAa): The description modified
		491	Table 15.1 Specifications of DMAC: The descriptions of "Channel priority" and "Transfer mode/ Block transfer", modified
		549	15.3.4.1 Specifying Detection Operation of DMA Transfer Requests for Each Source: The description modified
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		583	Figure 15.44 Setting Example of Next Register Continuous Execution: The title modified
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		608	Table 16.5 Operations of Modules When Event is Input: MTU, CMT, CMTW, TPU, GPT modules: The description under "Operations When Event is Input" modified
		609	16.3.3 Operation of Peripheral Timer Modules When Event is Input: The description modified
		610	Figure 16.3 Event Linkage Related to Single Ports (Port B): The titles of [1] and [2], modified
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		611	Figure 16.4 Input Port Group Operation upon Event Input (Port B): The direction of the text "Levels input on the pins", modified; text modified
		612	16.3.5 I/O Port Operation upon Event Input and Event Generation, (6) Output Port Group Operation upon Event Input: The description "while the PGCn.PGCOn bit being 1XXb", modified
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		All	"Hi-z" was modified to "Hi-Z"
		618	Figure 17.1 I/O Port Configuration (1): Note 1 modified
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		623	17.3.1 Port Direction Register (PDR): Address(es) modified: PORT0 PDR → PORT0.PDR
		625	17.3.3 Port Input Data Register (PIDR): The title modified
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		629	17.4 Handling of Unused Pins: The description modified
		18. Multi-Function Pin Controller (MPC)	
		All	18.2 Register Descriptions: The description in each subsection modified: "Modify the register after releasing the protection." → "Modifications to this register can only be made after releasing protection."
		662	18.2.8 P6n Pin Function Control Register (P6nPFS): The description modified
		667	18.2.11 P9n Pin Function Control Register (P9nPFS): The description of "ISEL Bit", modified
		676	18.2.16 PEn Pin Function Control Register (PEnPFS) (n = 0 to 7): The description of "ISEL Bit", modified
		685	18.2.24 PNn Pin Function Control Register (PNnPFS): The description modified
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		19. Multi-Function Timer Pulse Unit (MTU3a)	
		719	Table 19.15 TIOR (MTU1): The functional description of the MTIOC1B pin when IOB[3:0] = 111x, modified
		724	Table 19.25 TIORH (MTU8): The entries under IOB[3:0] modified: 1x00, 1x01, 1x1x, 11xx → 1000, 1001, 101x, 11xx
		810	19.3.6 Phase Counting Mode: The description in the case of 32-bit phase counting mode, modified
		830	Figure 19.46 Block Diagram of MTU3 and MTU4 in Complementary PWM Mode: External cutoff input: POE11#, deleted
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		988	Table 21.1 Specifications of GPT: The description of the module-stop state, modified
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		1149	22.2.9 Timer Synchronous Register (TSYRA, TSYRB): The description modified
		1150	22.2.10 Noise Filter Control Register (NFCR): Table of bits: Note 1 modified
		1157	Figure 22.7 Example of Setting Procedure for Waveform Output by Compare Match: The description in [1]: Index modified
		1159	22.3.1 Basic Functions, (3) Input Capture Function: Index modified
		1167	22.3.4 Cascaded Operation: Note 2 modified
		1169	22.3.5 PWM Modes: 1. PWM mode 1: The description modified; 2. PWM mode 2: The description modified
		1180	Figure 22.32 Timing Chart for the Noise Filter: Text modified (Input-capture input → Input-capture input pin)
		1182	Figure 22.33 Connection Diagram of Example Setting for PWM 1-Axis Measurement: Text modified
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		1188	Figure 22.36 Connection Diagram of Example Setting for PWM 2-Axes Measurement: Text modified
		1191	22.5 DMAC Activation: The description modified
		1209	22.10.2 Receiving an Event Signal from ELC, (2) Clear Counting: The description modified
		1210	22.10.2 Receiving an Event Signal from ELC, (3) Input Capture Operation: The description modified
		1212	Figure 22.67 Conflict between TGRy Read Cycle and Input Capture Operation: Text modified
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		1239	23.3.8 Pulse Output Triggered by Input Capture: The description modified
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		1247	Figure 24.5 Timing of Event Issuance: Text modified (CMCNTn → CMT1.CMCNT, CMCORn → CMT1.CMCOR)
		1248	24.5.2 CMT Operation When Receiving an Event from ELC, (1) Count Start: The bit symbol, modified
		1249	24.5.2 CMT Operation When Receiving an Event from ELC, (2) Event Count: The register name, modified
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