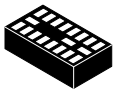
Audio Processor for Digital Hearing Aids

EZAIRO 7111 HYBRID



SIP19
CASE 127ES

Introduction

Ezairo® 7111 is an open−programmable DSP−based hybrid specifically designed for use in high−performance hearing aid and hearing implant devices. The Ezairo 7111 hybrid includes the Ezairo 7100 System−on−Chip (SoC), with its high−precision quad−core architecture that delivers 375 MIPS, without sacrificing power consumption.

The highly integrated Ezairo 7100 includes an optimized, dual−Harvard CFX Digital Signal Processor (DSP) core and HEAR Configurable Accelerator signal processing engine. It also features an Arm® Cortex®−M3 Processor Subsystem that supports various types of protocols for wireless communication. This block combines an open−programmable controller with hardware accelerators for audio coding and error correction support.

Ezairo 7100 also includes a programmable Filter Engine that enables time domain filtering and supports an ultra−low−delay audio path. When combined with non−volatile memory and wireless transceivers, Ezairo 7100 forms a complete hardware platform.

The Ezairo 7111 hybrid contains the Ezairo 7100 SoC, 2 Mb EEPROM storage and the necessary passive components to directly interface with the transducers required in a hearing aid.

Development Tools

Ezairo Preconfigured Suite (Pre Suite)*

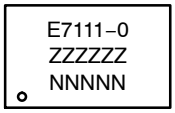
The Ezairo Pre Suite provides a complete framework to easily develop Ezairo−based hearing aids and fitting software. Included in the Ezairo Pre Suite is a firmware bundle, configuration software, and a cross−platform Software Development Kit (SDK) to develop your own fitting software.

Open−Programmable Evaluation and Development Kit (EDK)

To develop your own firmware on Ezairo 7111, the Ezairo 7100 Evaluation and Development Kit (EDK) includes optimized hardware, programming interface, and a comprehensive Integrated Development Environment (IDE).

Note: This datasheet describes all features of the Ezairo 7111 hybrid module. Not all of these features are available using the Ezairo Preconfigured Suite.

MARKING DIAGRAM



(Top View)

E7111−0 = Specific Device Code
ZZZZZZ = Assembly Lot Code
NNNNN = Serial Number

ORDERING INFORMATION

Device	Package	Shipping†
E7111−0-102A19-AG	SIP19 (RoHS Compliant)	250 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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KEY FEATURES

- **Programmable Flexibility**: the open−programmable DSP−based system can be customized to the specific signal processing needs of manufacturers. Algorithms and features can be modified or completely new concepts implemented without having to modify the chip.
- **Fully Integrated Hybrid**: includes the Ezairo 100 SoC, 2 Mbit EEPROM storage and the necessary passive components to directly interface with the transducers required in a hearing aid.
- **Quad−core Architecture**: includes a CFX DSP, a HEAR Configurable Accelerator, an Arm Cortex−M3 Processor Subsystem and a programmable Filter Engine. The system also includes an efficient input/output controller (IOC), system memories, input and output stages along with a full complement of peripherals and interfaces.
- **CFX DSP**: a highly cycle−efficient, programmable core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture.
- **HEAR Configurable Accelerator**: a highly optimized signal processing engine designed to perform common signal processing operations and complex standard filterbanks.
- **Arm Cortex−M3 Processor Subsystem**: a complete subsystem that supports efficient data transfer to and from a wireless transceiver. The subsystem includes hardwired CODECS (G.722, CVSD) and Error Correction support (Reed−Solomon, Hamming), as well as a fully programmable Arm Cortex−M3 processor and dedicated interfaces. It is compatible with various wireless technologies (NFMI, RF).
- **Programmable Filter Engine**: a filtering system that allows applying a various range of pre− or post−processing filtering, such as IIR, FIR and biquad filters.
- **Configurable System Clock Speeds**: 1.28 MHz, 1.92 MHz, 2.56 MHz, 3.84 MHz, 5.12 MHz, 6.4 MHz, 7.68 MHz, 8.96 MHz, 9.60 MHz, 10.24 MHz* (default clock calibration), 12.80 MHz and 15.36 MHz to optimize the computing performance versus power consumption ratio. The calibration for these 12 clock speeds are stored in the manufacturing area of the EEPROM.
- **Ultra−low Delay**: programmable Filter Engine supports an ultra−low−delay audio path of 0.044 ms (44 μs) for superior performance of features such as occlusion management.
- **Ultra−high Fidelity**: 85 dB system dynamic range with up to 110 dB input signal dynamic range, exceptionally−low system noise and low group delay.
- **Ultra−low Power Consumption**: <0.7 mA @ 10.24 MHz system clock (executing a tight MAC−loop in the CFX DSP core plus a typical hearing aid filterbank on the HEAR Configurable Accelerator).
- **High Output Level**: output levels of ~139 dB SPL possible with low impedance receiver (measured using IEC 711 coupler).
- **Diverse Memory Architecture**: a total of 40 kwords of program memory and 44 kwords of data memory, shared between the four cores included on the Ezairo 7100 chip.
- **Data Security**: sensitive program data can be encrypted for storage in EEPROM to prevent unauthorized parties from gaining access to proprietary algorithm intellectual property.
- **Signal Detection** Unit: ultra−low−power detection system for signals on any analog inputs.
- **High Throughput Communication Interface**: fast I^2C−based interface for quick download, debugging and general communication.
- **Highly Configurable Interfaces**: two PCM interfaces, two I^2C interfaces, two SPI interfaces, a UART interface as well as multiple GPIOs can be used to stream configuration, control or signal data into and out of the Ezairo 7111 hybrid.
- **On−chip PLL**: support for communication synchronization with wireless transceiver.
- **Glueless MMI**: link to various analog and digital user interfaces such as analog or digital volume control potentiometers, push buttons for program selection and microphone/telecoil switching.
- **Fitting Support**: support for Microcard, HI−PRO 2, HI−PRO USB, QuickCom, and NOAHlink, including NOAHlink's audio streaming feature.
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage		2	V
VBATOD	Output drivers power supply voltage		2	V
Vin	Voltage at any input pin	GNDC−0.3	VDDO + 0.3	V
GNDC, GNDA	Digital and Analog Grounds	0	–	V
T functional	Functional temperature range (Note 1)	−40	85	°C
T operational	Operational temperature range (Note 1)	0	50	°C
T storage	Storage temperature range	−40	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Electrical Specification may exceed listed tolerances when out of the temperature range 0°C to 50°C.

Electrical Performance Specifications

The tests were performed at 20°C with a 1.25 V supply voltage and 4.7 Ω series resistor to simulate a nominal hearing aid battery. The system clock (SYS_CLK) was set to 5.12 MHz and an audio input sampling frequency of 16 kHz was used.

Parameters marked as screened are tested on each chip.

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
OVERALL							
Supply Voltage	VBAT	Supply voltage measured at the VBAT pin	1.05	1.25	2.0	V	
Current consumption	I_{VBAT}	Filterbank: 30% load CFX: 100% load SYS_CLK: 10.24 MHz	–	700	–	μA	
		Ezairo Pre Suite firmware bundle running at 10.24 MHz, all algorithms active, no transducers connected.	–	1090	–	μA	
Stand by current	Istb	Using ON's macro		40	120	μA	
VREG							
Regulated voltage output	VREG	Trimmed bandgap I_{load} = 100 μA	0.96	0.97	0.98	V	√
Regulator PSRR	$VREG_{PSRR}$	1 kHz, VBAT = 1.25 V	76	80	–	dB	
Load current	I_{LOAD}		–	–	2	mA	
Load regulation	$LOAD_{REG}$	5 μA < I_{load} < 2 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	I_{load} = 1 mA	–	2	5	mV/V	
VDDA							
Output voltage trimming range	VDDA	Control register configured, typical values	1.8	2.0	2.1	V	√
Regulator PSRR	$VDDA_{PSRR}$	1 kHz, VBAT = 1.25 V	40	50	–	dB	
Load current	I_{LOAD}		–	–	1	mA	
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; 100 μA < I_{load} < 1 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	1.2 V < VBAT < 1.86 V; I_{load} = 100 μA	–	6	20	mV/V	

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
VDBL							
Output voltage trimming range	VDBL	Control register configured, typical values, unloaded	1.6	2.0	2.2	V	√
Regulator PSRR	$VDBL_{PSRR}$	1 kHz, VBAT = 1.25 V	30	40	–	dB	
Load current	I_{LOAD}	ITRIM (A_CP_VDBL_CTRL) = 0x7	–	–	15	mA	
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; 100 μA < I_{load} < 3 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	VBAT > 1.2 V; I_{load} = 100 μA	–	6	20	mV/V	
VDDC							
Digital supply output voltage trimming range	VDDC	Control register configured, typical values, unloaded	0.72	– (Note 2)	1.32	V	√
VDDC output level adjustment	$VDDC_{STEP}$		1.5	2.5	3	mV	√
Regulator PSRR	$VDDC_{PSRR}$	1 kHz, VBAT = 1.25 V	25	30	–	dB	
Load current	I_{LOAD}	Delivered by LDO	–	–	5	mA	
Load regulation	$LOAD_{REG}$		–	5	10	mV/mA	
Line regulation	$LINE_{REG}$		–	6	12	mV/V	

2. Recommended VDDC values depend on the system clock (SYS_CLK) frequency. Table 3 gives the recommended VDDC values for different system clocks.

VDDM							
Memory supply output voltage trimming range	VDDM	Control register configured, typical values, unloaded	0.82	– (Note 3)	1.32	V	√
VDDM output level adjustment	$VDDM_{STEP}$		1.5	2.5	3	mV	√
Regulator PSRR	$VDDM_{PSRR}$	1 kHz, VBAT = 1.25 V	25	30	–	dB	
Load current	I_{LOAD}	Delivered by LDO	–	–	5	mA	
Load regulation	$LOAD_{REG}$		–	5	10	mV/mA	
Line regulation	$LINE_{REG}$		–	6	12	mV/V	

3. The minimum VDDM value required for proper system functioning is 0.90 V.

POWER−ON−RESET							
POR startup voltage	$VBAT_{STARTUP}$		–	0.9	–	V	√ (Note 4)
POR shutdown voltage	$VBAT_{SHUTDOWN}$		–	0.88	–	V	√ (Note 5)

4. Pass fail test with 0.855 V and 0.945 V
5. Pass fail test with 0.835 V and 0.925 V

INPUT STAGE							
Analog input voltage range	V_{IN}		0	–	2	V	
Preamplifier gain	PAG	3 dB steps	0	–	36	dB	√
Preamplifier gain accuracy	PAG acc	1 kHz, PAG from 0 to 36 dB	−1.5	0	1.5	dB	√
Input impedance	R_{IN}	Non−0 dB preamplifier gains	370	500	725	kΩ	√

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
INPUT STAGE							
Input referred noise	IN_{IRN}	AIR connected to AGND Unweighted, 100 Hz to 10 kHz BW Preamplifier settings:				μVrms	
		0 dB		53	–		
		12 dB		13	–		
		15 dB		9	–		
		18 dB		6.6	10.6		√
		21 dB		4.9	–		
		24 dB		4.3	–		
		27 dB		3.7	–		
		30 dB		3.2	–		
		33 dB		3.2	–		
		36 dB		3.2	–		
Input Dynamic Range	IN_{DR}	AIR connected to AGND Unweighted, 100 Hz to 10 kHz BW Preamplifier settings:				dB	
		0 dB	–	86			
		12 dB	–	86			
		15 dB	–	86			
		18 dB	81	86			√
		21 dB	–	85			
		24 dB	–	82			
		27 dB	–	82			
		30 dB	–	80			
		33 dB	–	77			
		36 dB	–	74			
Input peak THD+N	IN_{THD+N}	Any preamplifier gain −10 dBFS signal at preamp output, 1kHz.	–	–	−68	dB	√
OUTPUT DRIVER							
Maximum peak current	I_{DO}	High Power mode	–	–	25	mA	
Output impedance	R_{DO}	Normal mode, I_{load} = 1 mA	–	4.5	5.5	Ω	
Output impedance	R_{DO}	High Power mode	–	2.5	4	Ω	
Output dynamic range	DO_{DR}	Normal mode, VBAT = 1.25 V	90	–	–	dB	
Output THD+N	DO_{THDN}	At 1 kHz, −6 dBFS, 8 kHz bandwidth, VBAT = 1.25 V, normal mode	–	−78	−76	dB	
10−BIT LOW−SPEED A/D							
Input voltage range	$LSAD_{RANGE}$	Peak input voltage	0	–	1.94	V	√
INL	$LSAD_{INL}$	From GND to 2*VREG	−4	–	+4	LSB	
DNL	$LSAD_{DNL}$	From GND to 2*VREG	−2	–	+2	LSB	
Sampling frequency	$LSAD_{SF}$	All channels sequentially	–	12.8	–	kHz	
Channel sampling frequency	$LSAD_{CH_SF}$		–	1.6	–	kHz	

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Unit	Screened
SIGNAL DETECTION UNIT							
Preamplifier gain	SDU_{PAG}	3dB steps	0	–	36	dB	√
Equivalent IRN	SDU_{IRN}	Non−weighted, 30 dB gain, 100 Hz – 10 kHz	–	–	20	μVrms	√
Input impedance	SDU_{R}		370	500	725	kΩ	√
Low Pass Filter Bandwidth	SDU_{LPF}			50		kHz	
ADC input signal range	SDU_{RANGE}	Referred to VREG	−1		+1	V	
ADC resolution	SDU_{RES}			12		bits	
ADC sampling frequency	SDU_{SF}	At slow_clock = 1.28 MHz	1		64	kHz	
DIGITAL							
Voltage level for high input	V_{IH}		V_{DDO} * 0.8	-	-	V	√
Voltage level for low input	V_{IL}		-	-	V_{DDO} * 0.2	V	√
Voltage level for high output	V_{OH}	2mA source current	V_{DDO} * 0.8	-		V	√
Voltage level for low output	V_{OL}	2mA sink current	-	-	V_{DDO} * 0.2	V	√
Oscillator frequency trimming precision	SYS_CLK		−1	–	+1	%	√
Oscillator frequency stability over temperature	SYS_CLK	Over temperature range of 0°C to 50°C	−1.5	–	+1.5	%	
Recommended working frequency	SYS_CLK	For recommended VDDC and VDDM	1.28	–	15.36	MHz	
Oscillator period jitter		RMS at System clock: 1.28 MHz, before multiplication	–	–	400	ps	
PLL lock time		For an input phase error <2%, input reference clock of 128 kHz, output clock of 2.56 MHz	–	–	10	ms	√
PLL tracking range			−2	–	2	%	
LOW DELAY PATH							
Group Delay		Using the low delay path of the Filter Engine	–	44	–	μs	
EEPROM							
EEPROM burn cycles		Per EA2M datasheet	1'000'000	–	–	Cycles	
Current consumption – writing to EEPROM	I_W	V_{DBL} = 1.6 V, SPI_CLK = 5 MHz		0.7		mA	
Current consumption – read from EEPROM	I_R	V_{DBL} = 1.6 V, SPI_CLK = 5 MHz		0.4		mA	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 3. RECOMMENDED MINIMUM VDDC LEVELS

Operating Frequency (MHz)	Minimum VDDC Voltage (V)
1.28 to 5.12	0.73
5.13 to 10.24	0.82 (Note 6)
10.25 to 12.80	0.85
12.81 to 15.36	0.88 (Note 7)

6. The default VDDC calibration entry, stored in the manufacturing area of the EEPROM at address 0x0064, should be used for operation at 0.82 V.
7. An alternate VDDC calibration entry, stored in the manufacturing area of the EEPROM at address 0x00E8, should be used for operation at 0.88 V.

PACKAGING AND MANUFACTURING

- Ultra−miniature form factor: suitable for all hearing aid styles including CIC, ITE, RITE, BTE, and mini−BTE.
- Can easily be soldered by hand.
- Re−flowable: the Ezairo 7111 hybrid is re−flowable onto FR4 and other substrates.
- Bump metallization: SAC305 (Sn96.5/Ag3.0/Cu0.5)
- RoHS compliant: the Ezairo 7111 hybrid complies with the RoHS directive.

SYSTEM DIAGRAM

Figure 1 is a simplified diagram of the hybrid system that shows the major internal functional blocks and possible external peripherals.

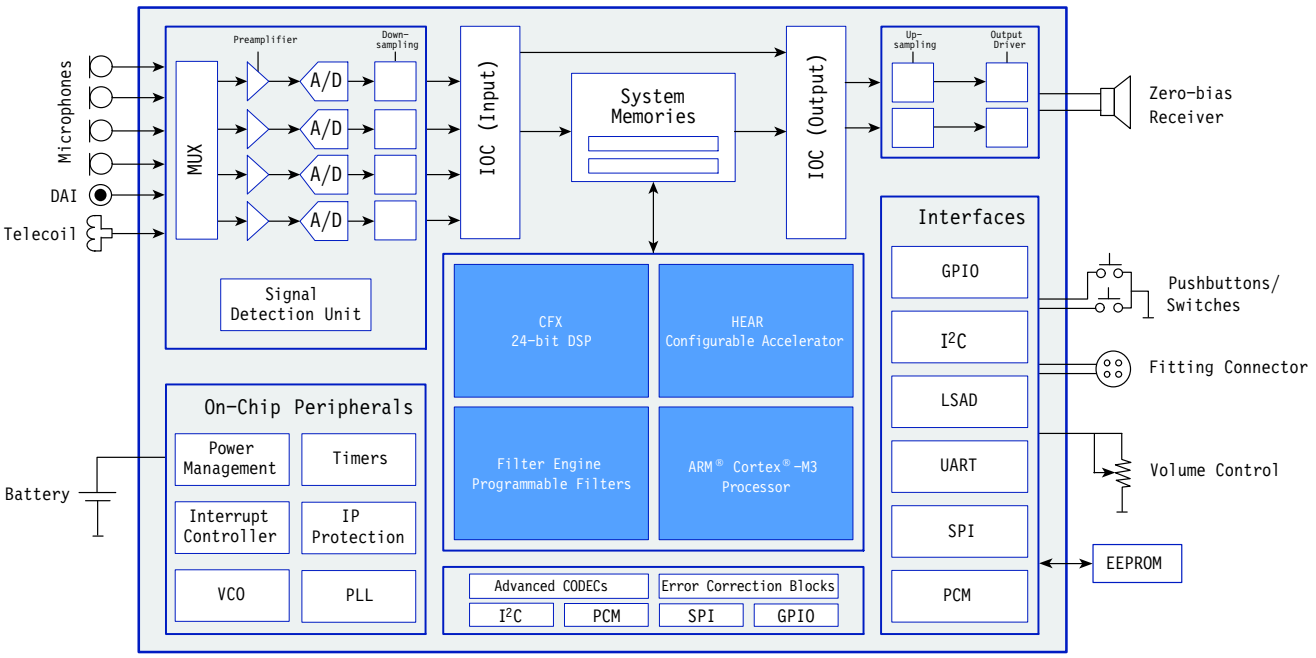


Figure 1. Ezairo 7111 Hybrid System Diagram

Ezairo 7111 HYBRID INTERFACE SPECIFICATIONS

A total of 19 pads are present on the Ezairo 7111 hybrid. These pads are the interfaces between the hybrid and the other components in the hearing aid. They are listed in Table 4 along with the internal connections.

Table 4. PAD DESCRIPTION

Ball Number	Hybrid Pad Name	Hybrid Pad Description
A1	AI0	Analog Input 0: Microphone or Telecoil Input
A2	MIC_VREG	Regulated voltage for microphone
A3	GND_MIC	Input Transducer Ground
A4	DIO24	Digital Input Output 24
A5	DIO23	Digital Input Output 23
A6	DIO22	Digital Input Output 22
A7	DIO21	Digital Input Output 21
A8	VBAT	Power Supply
B1	AI1	Analog Input 1: Microphone or Telecoil Input
B3	AI3	Analog Input 3: Direct Analog Input
B8	RCVR_BAT	Output Stage Power Supply
C1	AI2	Analog Input 2: Microphone or Telecoil Input
C2	VREG	Regulated voltage output
C3	GND	Ground
C4	DIO25	Digital Input Output 25
C5	RCVR0P	Receiver Output 0 Positive
C6	RCVR0N	Receiver Output 0 Negative
C7	SCL	Debug Port Clock
C8	SDA	Debug Port Data

Ezairo 7111 HYBRID SCHEMATICS

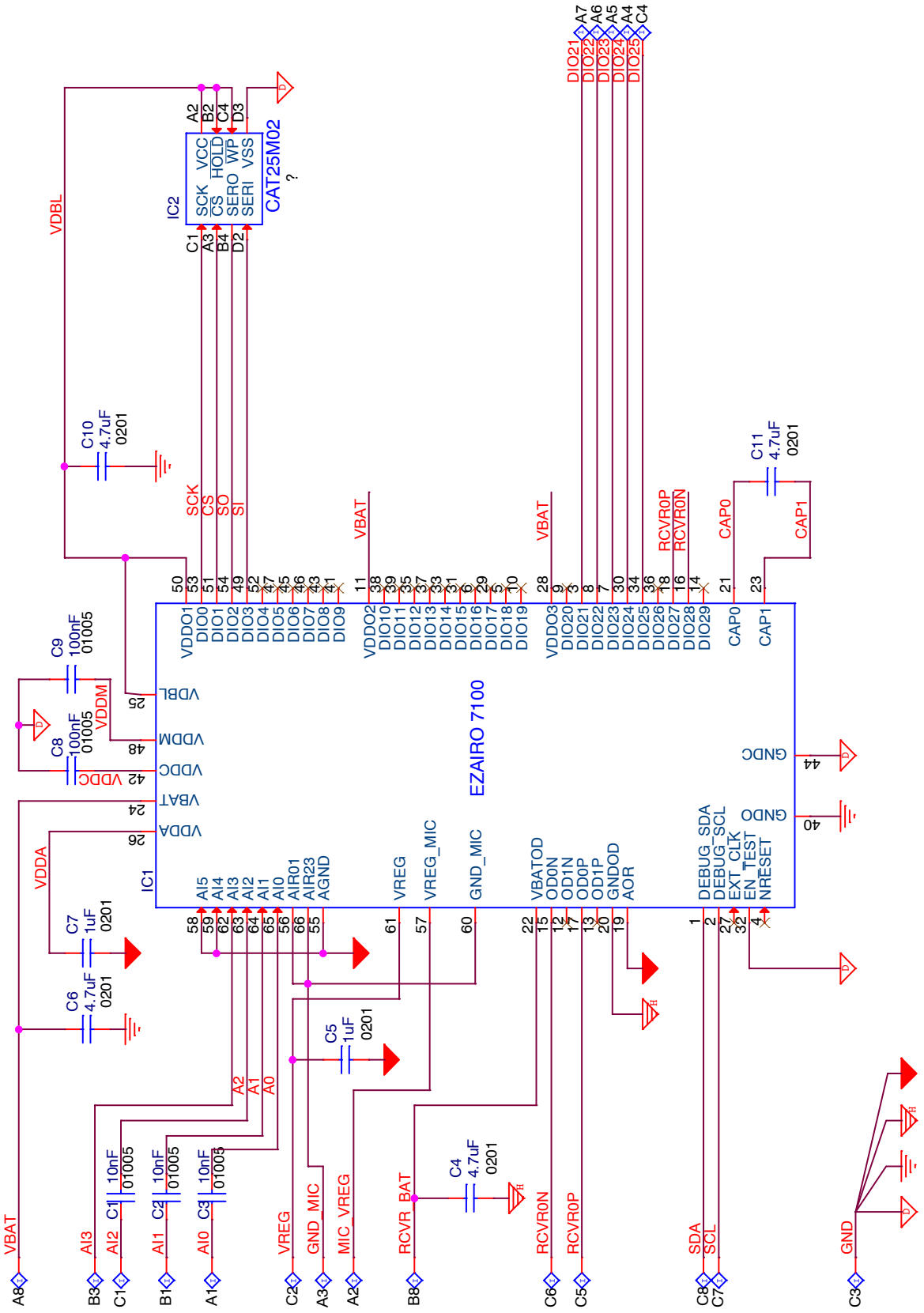


Figure 2. Ezairo 7111 Hybrid Schematics

CONNECTION DIAGRAM

The following connections are typical when Ezairo 7111 is used in a hearing aid application. For details on the connections required by the preconfigured firmware bundle refer to AND9677/D.

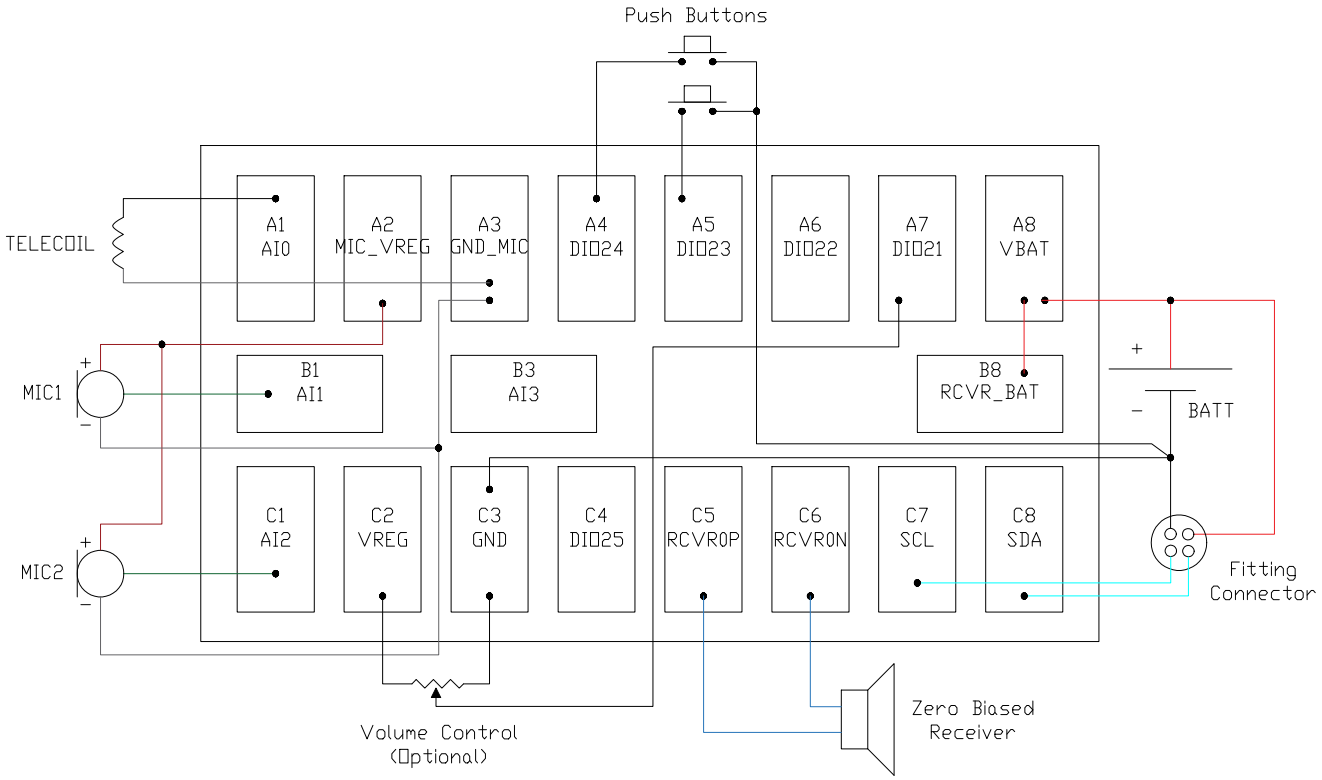


Figure 3. Connection Diagram (hybrid view: bottom view)

ARCHITECTURE OVERVIEW

The Ezairo 7100 system is an asymmetric quad−core architecture, mixed−signal system−on−chip designed specifically for audio processing. It centers around four processing cores: the CFX Digital Signal Processor (DSP), the HEAR Configurable Accelerator, the Arm Cortex−M3 Processor Subsystem, and the Filter Engine.

CFX DSP Core

The CFX DSP core is used to configure the system and the other cores, and it coordinates the flow of signal data progressing through the system. The CFX DSP can also be used for custom signal processing applications that can't be handled by the HEAR or the Filter Engine.

The CFX DSP is a user−programmable general−purpose DSP core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture. It is able to perform two MACs, two memory operations and two pointer updates per cycle, making it well−suited to computationally intensive algorithms.

The CFX features:

- Dual−MAC 24−bit load−store DSP core
- Four 56−bit accumulators
- Four 24−bit input registers
- Support for hardware loops nested up to four deep
- Combined XY memory space (48 bits wide)
- Dual address generator units
- A wide range of addressing modes:
  - Direct
  - Indirect with post−modification
  - Modulo addressing
  - Bit reverse

For further information on the usage of the CFX DSP, please refer to the *Hardware Reference Manual* and to the *CFX DSP Architecture Manual* available in the Ezairo 7100 Evaluation and Development Kit (EDK).

HEAR Configurable Accelerator

The HEAR coprocessor is designed to perform both common signal processing operations and complex standard filterbanks such as the WOLA filterbank, reducing the load on the CFX DSP core.

The HEAR Configurable Accelerator is a highly optimized signal processing engine that is configured through the CFX. It offers high speed, high flexibility and high performance, while maintaining low power consumption. For added computing precision, the HEAR supports block floating point processing. Configuration of the HEAR is performed using the HEAR configuration tool (HCT). For further information on the usage of the HEAR, please refer to the *HEAR Configurable Accelerator Reference Manual* available in the Ezairo 7100 EDK.

The HEAR is optimized for advanced hearing aid algorithms including but not limited to the following:

- Dynamic range compression
- Directional processing
- Feedback cancellation
- Noise reduction

To execute these and other algorithms efficiently, the HEAR excels at the following:

- Processing using a weighted overlap add (WOLA) filterbank
- Time domain filtering
- Subband filtering
- Attack/release filtering
- Vector addition/subtraction/multiplication
- Signal statistics (such as average, variance and correlation)

Arm Cortex−M3 Processor Subsystem

The Arm Cortex−M3 Processor Subsystem provides support for data transfer to and from the wireless transceiver. The subsystem includes hardwired CODECS (G.722, CVSD), Error Correction support (Reed−Solomon, Hamming), interfaces (SPI, I^2C, PCM, GPIOs), as well as an open−programmable Arm Cortex−M3 processor.

Arm Cortex−M3 Processor

The Arm Cortex−M3 processor is a low−power processor that features low gate count, low interrupt latency, and low−cost debugging. It is intended for deeply embedded applications that require fast interrupt response features.

GNU tools provide build and link support C programs that run on the Arm Cortex−M3 processor.

Filter Engine

The Filter Engine is a core that provides low−delay path and basic filtering capabilities for the Ezairo 7100 system. The Filter Engine can implement filters (either FIR or IIR) with a total of up to 160 coefficients. FIR filters are implemented using a direct−form structure. IIR filters are implemented with a cascade of second−order sections (biquads), each implemented as a direct−form I filter.

The Filter Engine is programmable, but does not include direct debugging access. The CFX can monitor the Filter Engine state through control and configuration registers on the program memory bus.

Digital Input/Output (DIO) Pads

A total of 5 DIOs are available on the Ezairo 7111 hybrid. These pads can all be configured for a variety of digital input and output modes or as LSADs. The user can configure DIOs signal to be, for example:

- CFX PCM interface
- CFX UART interface
- CFX SPI interface
- LSAD input
- GPIOs data for the CFX

- Arm Cortex−M3 processor PCM interface
- Arm Cortex−M3 processor SPI interface
- Arm Cortex−M3 processor I^2C interface
- Arm Cortex−M3 processor GPIOs

More details on the Ezairo 7111 external interfaces can be found in the *Ezairo 7100 Hardware Reference Manual* available in the Ezairo 7100 EDK.

The 5 DIOs are brought out of the Ezairo 7111 hybrid: DIO21, DIO22, DIO23, DIO24 and DIO25. The associated power domain is defined by VDDO3. VDDO3 is connected to Vbat inside the hybrid.

The SDA and SCL pads are on the VDDO3 power domain.

Debug Ports

The CFX's I^2C interfaces share the same I^2C bus within the Ezairo 7100 chip with two other I^2C interfaces:

CFX Debug Port I^2C

The CFX debug port I^2C interface is a hardware debugger for the Ezairo 7100 system that is always enabled regardless of the configuration of the general−purpose I^2C interface. The debug port implements the debug port protocol command set and is tightly coupled with the CFX DSP and the memory components attached to the CFX. The default address is 0x60.

Arm Cortex−M3 Processor Debug Port I^2C

The Arm Cortex−M3 processor debug port I^2C interface is a hardware debugger for the Ezairo 7100 system that is always enabled regardless of the configuration of the general−purpose I^2C interface. The debug port implements an

Arm Cortex−M3 processor debug port protocol command set that is tightly coupled with the Arm Cortex−M3 processor and the memory components attached to this core. The default address is 0x40.

PRE SUITE FIRMWARE BUNDLE

The Pre Suite Firmware Bundle of Ezairo 7111 comprises a real−time framework and suite of advanced sound processing algorithms ideal for high−end, full featured hearing aids (available under NDA). For additional details about the Pre Suite firmware bundle for Ezairo 7111 refer to Ezairo 7111 Firmware Bundle User's Guide.

DEFAULT APPLICATION ON EZAIRO 7111

The default application includes functionality that allows the application of the Ezairo 7111 to be updated to the latest Pre Suite version using Sound Designer/SDK. It leaves the debug port of Ezairo 7111 in Restricted Mode.

For customers using the Ezairo 7111 as an open−programmable device, it is possible to erase the default application and replace it with your own firmware image. This can be done using the Ezairo 7100 IDE or in a script using the Jump ROM functions "Wipe" and "Unlock" to place the device in Unrestricted Mode. Refer to the Communication Protocols Manual for Ezairo 7100 for more information.

FREQUENCY RESPONSE GRAPH

Conditions

SYS_CLK = 10.24 Mhz
Firmware: Simple FIFO copy application
Gain normalized to 0 dB at 1 kHz

Measurements taken electrically with a two−pole RC filter on the output with a cutoff frequency (−3 dB point) of 8 kHz. From 2 kHz to 8 kHz, the roll−off is due to the RC filter.

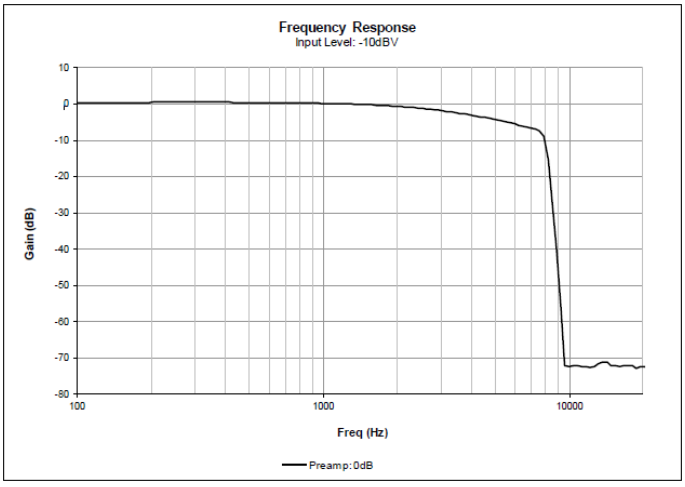


Figure 4. Frequency Response Graph

System Identification

System identification is used to identify different system components. This information can be retrieved using the Promira Serial Platform from TotalPhase, Inc. Or the Communications Accelerator Adaptor (CAA) and some protocol software provided by ON Semiconductor (see CAA instruction manual). For the Ezairo 7100 chip, the key identifier components and values are as follows:

- Chip Family: 0x06
- Chip Version:0x01
- Chip Revision: 0x0200

The hybrid ID can be found in the manufacturing area of the EEPROM at address 0x00F1 to 0x00F2 (2 bytes => 16 bits)

- Hybrid ID: 0x00B0

Solder Information

The Ezairo 7111 hybrid is constructed with all RoHS compliant material and should therefore be reflowed accordingly.

This hybrid device is Moisture Sensitive Class MSL3 and must be stored and handled accordingly. Re−flow according to IPC/JEDEC standard J−STD−020C, Joint Industry Standard: Moisture/Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

For soldering guidelines, please refer to the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D).

Electrostatic Discharge (ESD) Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

Development Tools

For more information on which development tools best suit your product development, contact your local sales representative or authorized distributor.

Company or Product Inquiries

For more information about ON Semiconductor products or services visit our web site at http://onsemi.com.

Technical Contact Information

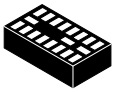
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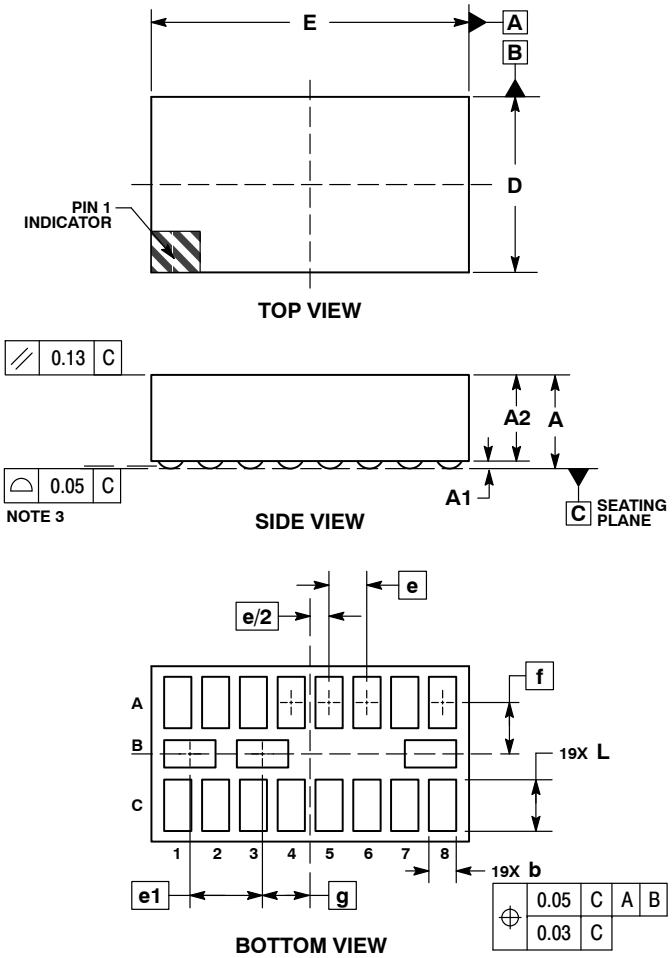
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SIP19 5.25x2.90
CASE 127ES
ISSUE C

DATE 10 MAR 2022



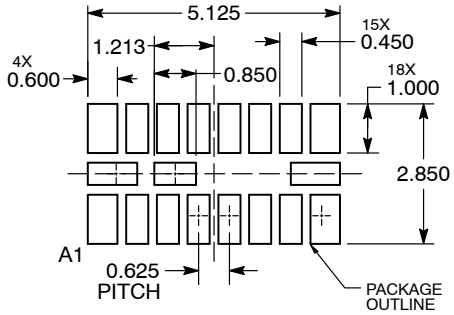
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BUMPS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.525
A1	0.060	0.125
A2	1.200	1.400
b	0.400	0.500
D	2.775	3.025
E	5.125	5.375
e	0.625 BSC	
e1	1.200 BSC	
f	0.850 BSC	
g	0.788 BSC	
L	0.800	0.900

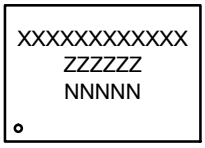
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
ZZZ = Assembly Lot Code
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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