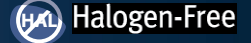


EPC2302 – Enhancement Mode Power Transistor

V_{DS} , 100 V

$R_{DS(on)}$, 1.8 mΩ max



General Description

The EPC2302 is a 1.8 mΩ max $R_{DS(on)}$, 100 V eGaN® power transistor in a low inductance 3 x 5 mm QFN package with exposed top for excellent thermal management. It is tailored to high frequency DC-DC applications to/from 40 V–60 V and 48 V BLDC motor drives.

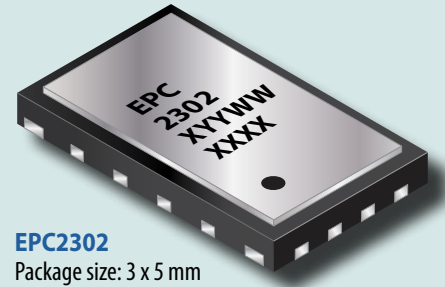
The thermal resistance to case top is ~0.2 °C/W, resulting in excellent thermal behavior and easy cooling. The device features an enhanced PQFN “Thermal-Max” package. The exposed top enhances top-side thermal management and the side-wettable flanks guarantee that the complete side-pad surface is wetted with solder during the reflow soldering process, which protects the copper and allows soldering to occur on this external flank area for easy optical inspection.

Compared to a Si MOSFET, the footprint of 15 mm² is less than half of the size of the best-in-class Si MOSFET with similar $R_{ds(on)}$ and voltage rating, Q_G and Q_{GD} are significantly smaller and Q_{RR} is 0. This results in lower switching losses and lower gate driver losses. Moreover, EPC2302 is very fast and can operate with deadtime less than 10 ns for higher efficiency and $Q_{RR} = 0$ is a big advantage for reliability and EMI. In summary, EPC2302 allows the highest power density due to enhanced efficiency, smaller size, and higher switching frequency for smaller inductor and fewer capacitors.

The EPC2302 enables designers to improve efficiency and save space. The excellent thermal behavior enables easier and lower cost cooling. The ultra-low capacitance and zero reverse recovery of the eGaN® FET enables efficient operation in many topologies. Performance is further enhanced due to the small, low inductance footprint.

Application notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source
- Questions: **Ask a GaN Expert** <https://epc-co.com/epc/Contact/AskGaNExpert.aspx>



EPC2302

Package size: 3 x 5 mm

Features

- 100 V
- 1.4 mΩ typical, 1.8 mΩ max $R_{DS(on)}$
- 3 x 5 mm QFN package
- Exposed top for top-side thermal management
- Moisture rating MSL2
- Enhanced Thermal-Max package

Applications

- AC-DC chargers, SMPS, adaptors, power supplies
- High Frequency DC-DC Conversion up to 80 V input (Buck, Boost, Buck-Boost and LLC)
- 24 V–60 V Motor Drives
- High Power Density DC-DC modules from 40 V– 60 V to 5 V–12 V
- Synchronous Rectification
- Solar MPPT

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint
- Excellent Thermal



Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	101	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	408	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.5	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	45	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90142 EVB)	21	

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.15\text{ mA}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		1	100	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.01	4	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		0.4	9	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.01	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 14\text{ mA}$	0.8	1.3	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 50\text{ A}$		1.4	1.8	m Ω
V_{SD}	Source-to-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.5		V

[#] Defined by design. Not subject to production test.

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		3200	4800	pF
C_{RSS}	Reverse Transfer Capacitance			7		
C_{OSS}	Output Capacitance			1000	1200	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		1300		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			1700		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 50\text{ A}$		23	29	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 50\text{ A}$		8.9		
Q_{GD}	Gate-to-Drain Charge			2.3		
$Q_{G(TH)}$	Gate Charge at Threshold			6.3		
Q_{OSS}	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		85	94	
Q_{RR}	Source-Drain Recovery Charge			0		

[#] Defined by design. Not subject to production test.

Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1: Typical Output Characteristics at 25°C

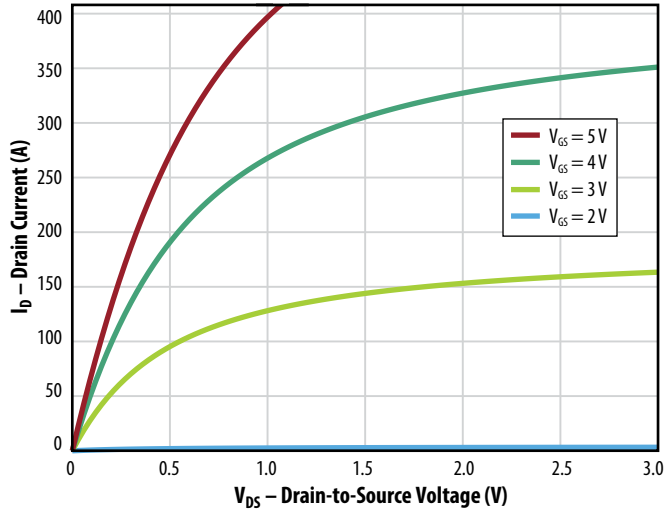


Figure 2: Typical Transfer Characteristics

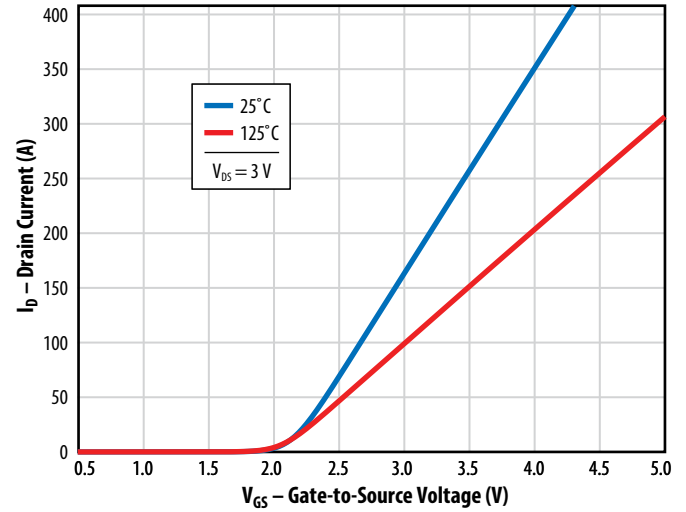
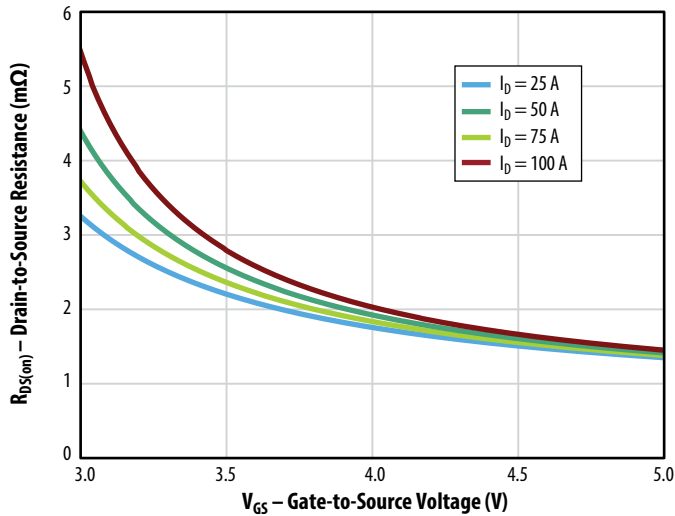
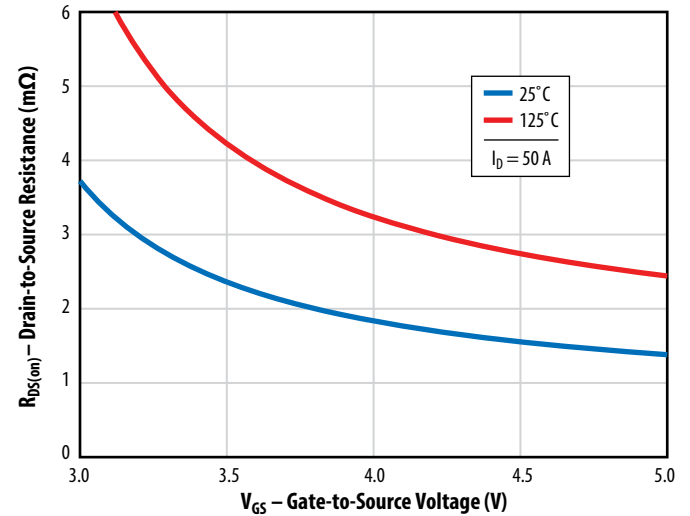
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

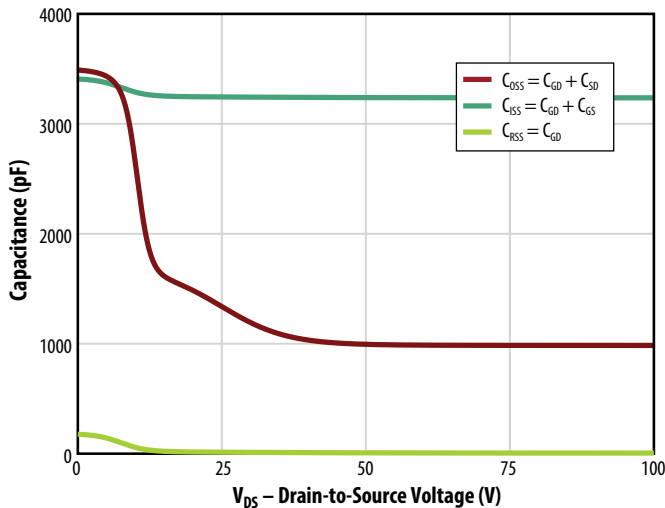


Figure 5b: Typical Capacitance (Log Scale)

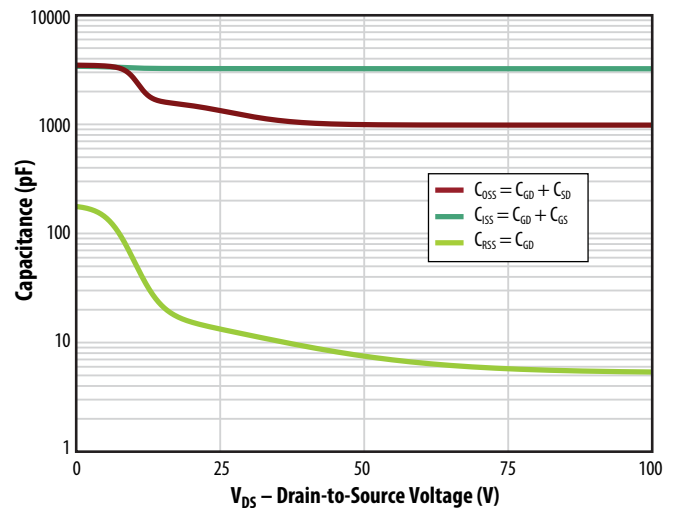


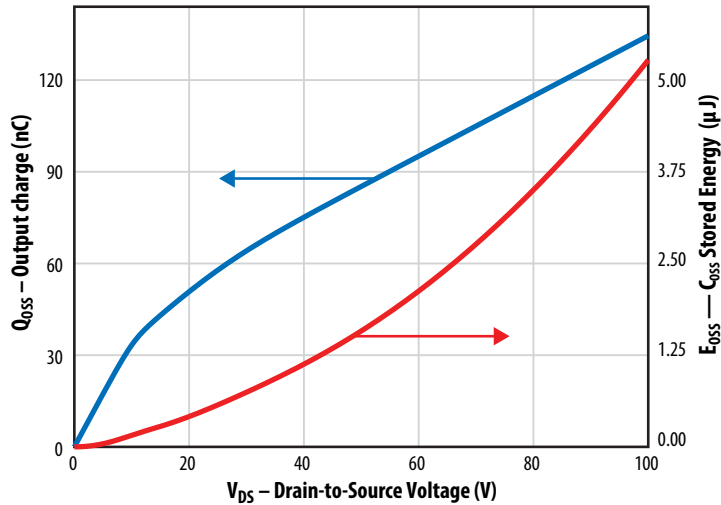
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

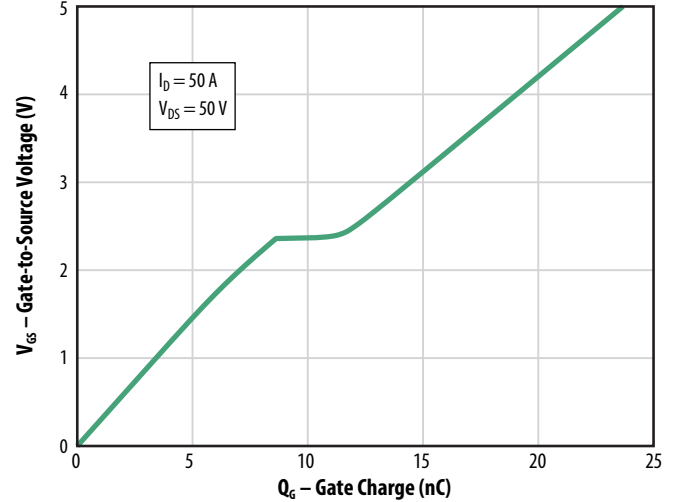


Figure 8: Typical Reverse Drain-Source Characteristics

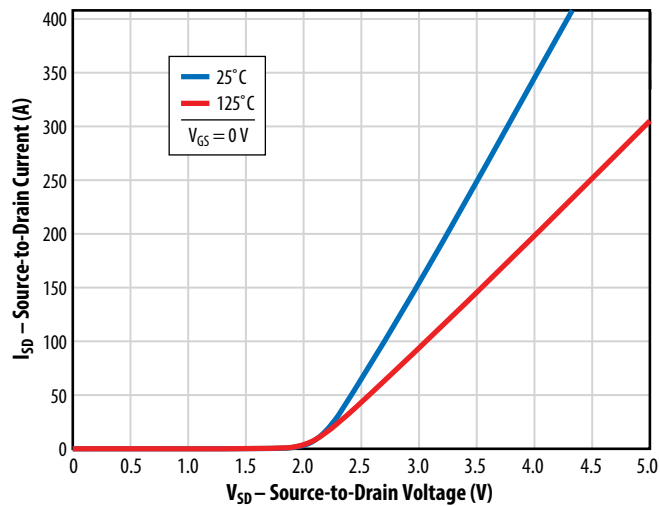


Figure 9: Typical Normalized On-State Resistance vs. Temp.

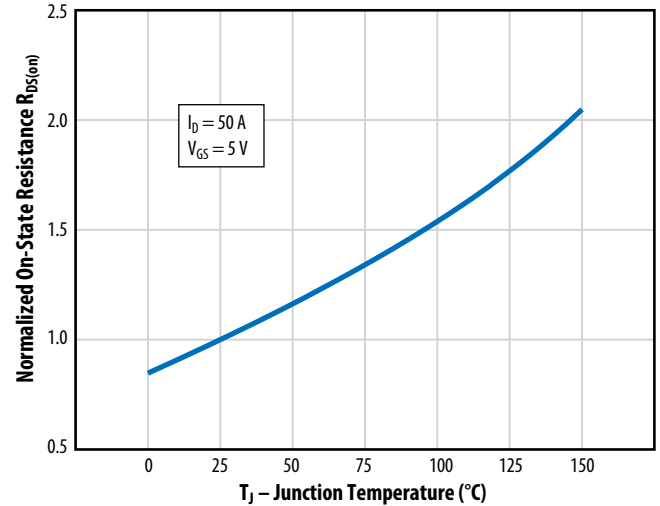


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

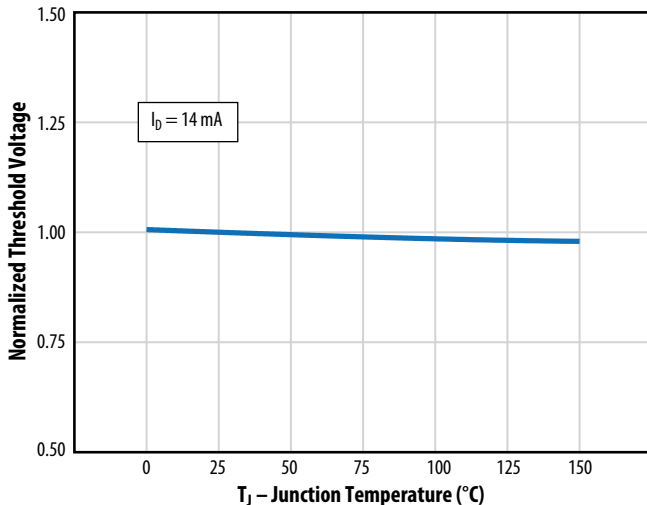


Figure 11: Safe Operating Area

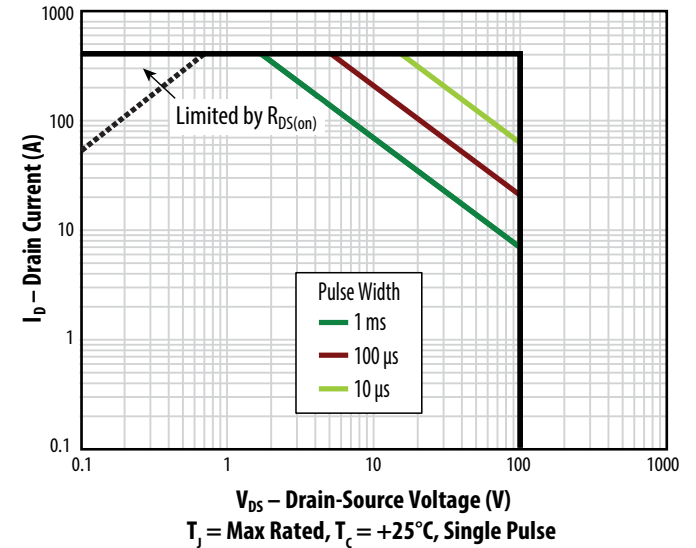
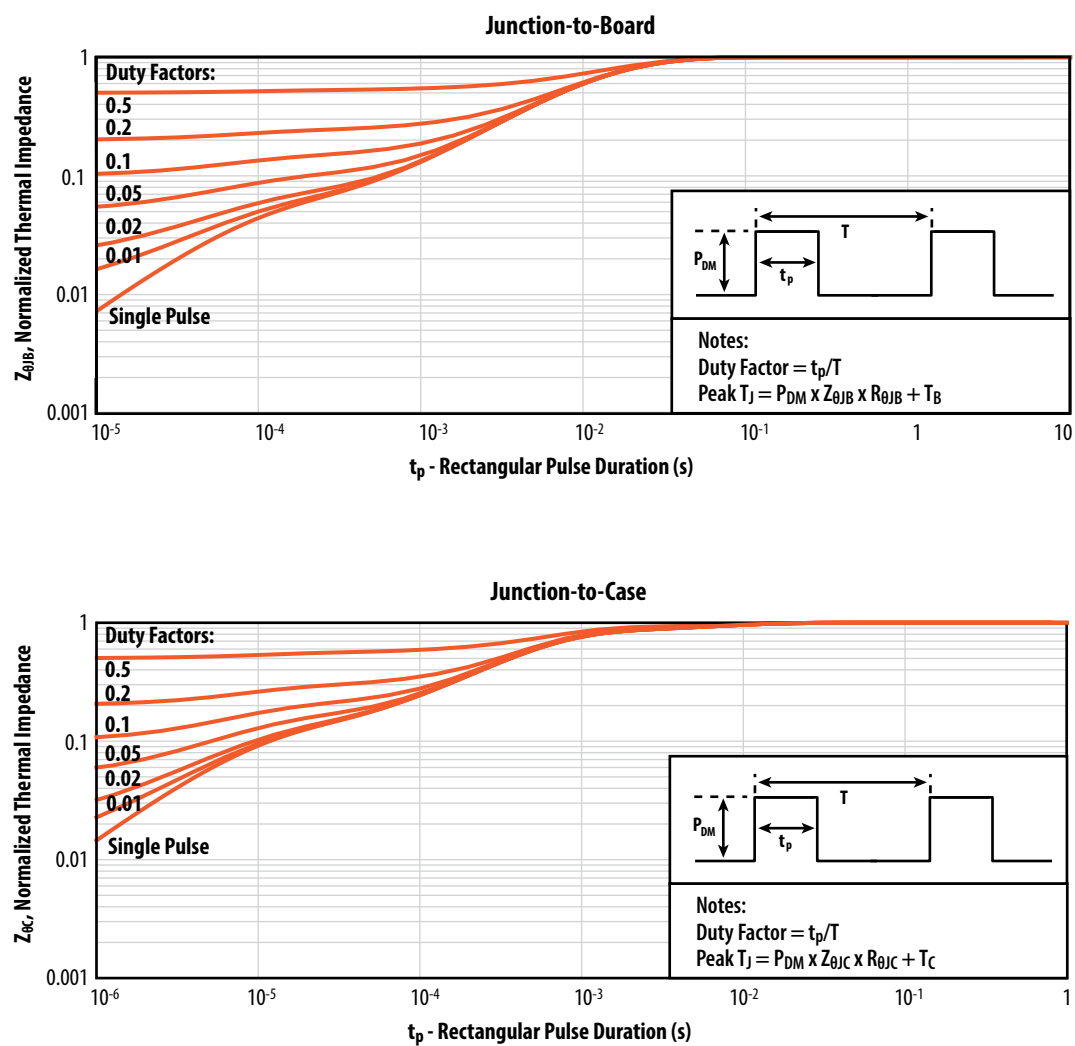
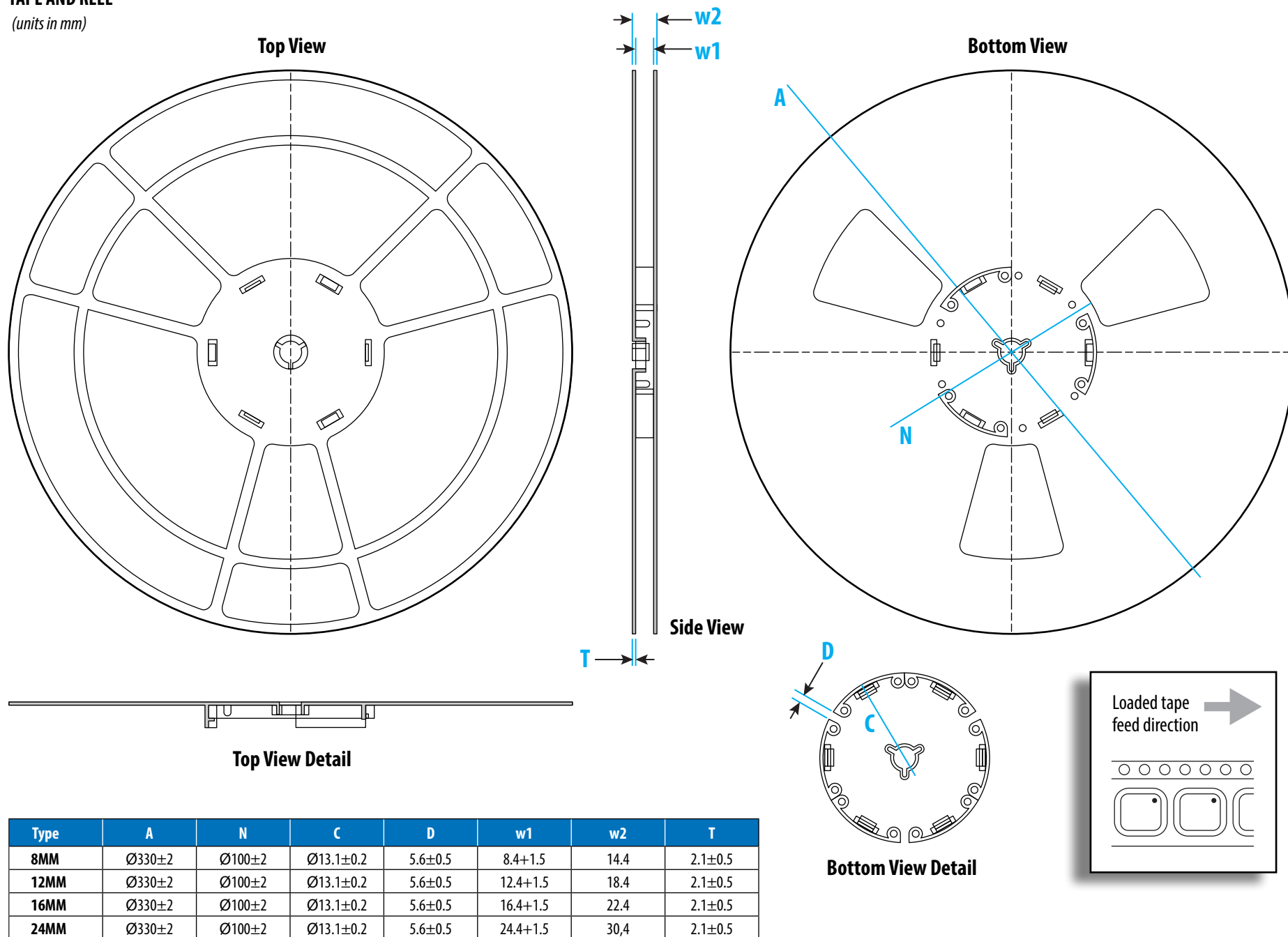


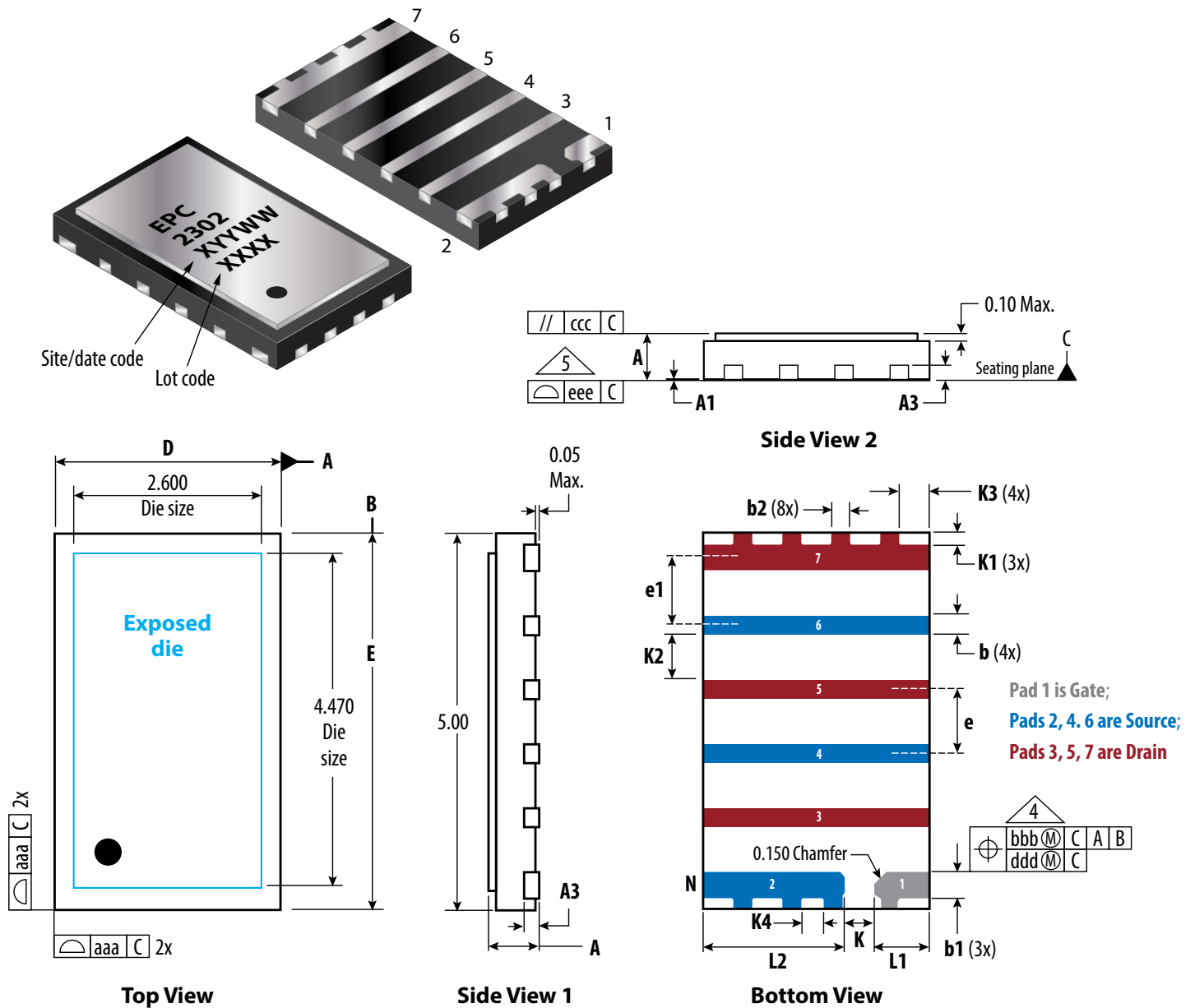
Figure 12: Transient Thermal Response Curves



TAPE AND REEL

(units in mm)



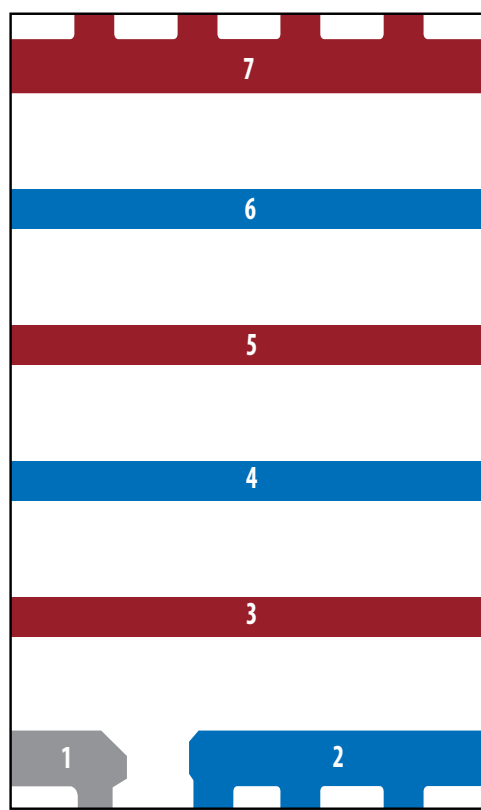


SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
b2	0.20	0.25	0.30	4
D		3.00 BSC		
E		5.00 BSC		
e		0.85 BSC		
e1		0.90 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K	0.35	0.40	0.45	
K1	0.10	0.15	0.20	
K2	0.55	0.60	0.65	
K3	0.35	0.40	0.45	
K4	0.25	0.30	0.35	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		15		3
NE		6		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

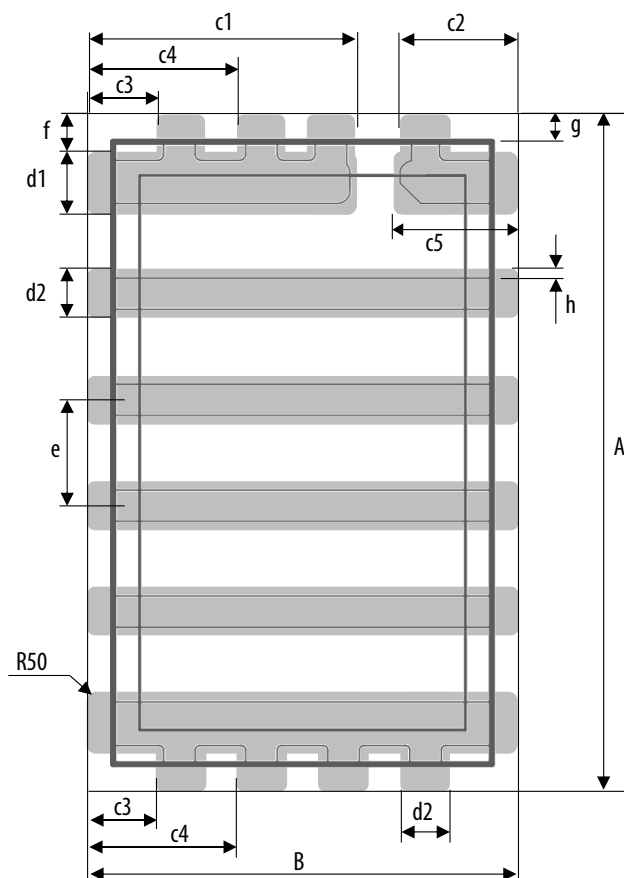
Transparent Top View

Additional Resources Available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

**RECOMMENDED
LAND PATTERN**

(units in mm)

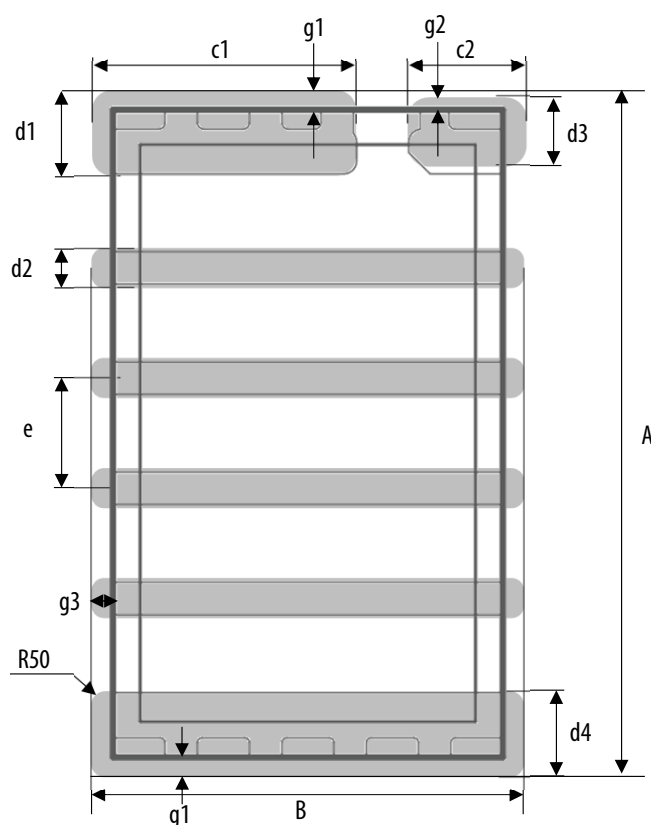


Land pattern is solder mask defined.
It is recommended to have on-Cu trace PCB vias.

DIM	Nominal
A	5.4
B	3.4
c1	2.1
c2	0.91
c3	0.54
c4	1.19
c5	0.985
d1	0.47
d2	0.37
e	0.85
f	0.29
g	0.2
h	0.06

**RECOMMENDED
STENCIL DRAWING**

(units in mm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

DIM	Nominal
A	5.22
B	3.32
c1	2
c2	0.875
d1	0.65
d2	0.28
d3	0.6
d4	0.61
e	0.85
g1	0.13
g2	0.11
g3	0.2

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