ESD Protection Diode
Micro−Packaged Diodes for ESD Protection

ESDM3032

The ESDM3032 is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium.

Features

- Low Clamping Voltage
- Small Body Outline Dimensions: 0.62 mm x 0.32 mm
- Low Body Height: 0.3 mm
- Stand−off Voltage: 3.3 V
- IEC61000−4−2 Level 4 ESD Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- μSD Card Protection
- Audio Line
- GPIO

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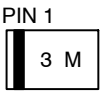
www.onsemi.com





X3DFN2
CASE 152AF

MARKING DIAGRAM



3 = Specific Device Code
M = Date Code

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±30 ±30	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C		P_D	250	mW
Thermal Resistance, Junction−to−Ambient		$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.

ORDERING INFORMATION

Device	Package	Shipping†
ESDM3032MXT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

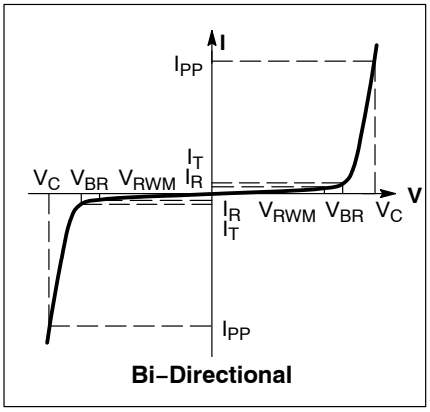
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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	4.1		5.7	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			100	nA
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±8 kV Air)		7.2		V
		I_{PP} = 16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±16 kV Air)		8.5		V
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8/20 μs)	7.5	8.5		A
Clamping Voltage (8/20 μs) (Note 3)	V_C	I_{PP} = 7.5 A		8.5	9.7	V
Dynamic Resistance	R_{DYN}	100 ns TLP Pulse		0.16		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		8.5	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 1 ns, averaging window; t_1 = 70 ns to t_2 = 90 ns.
3. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.

TYPICAL CHARACTERISTICS

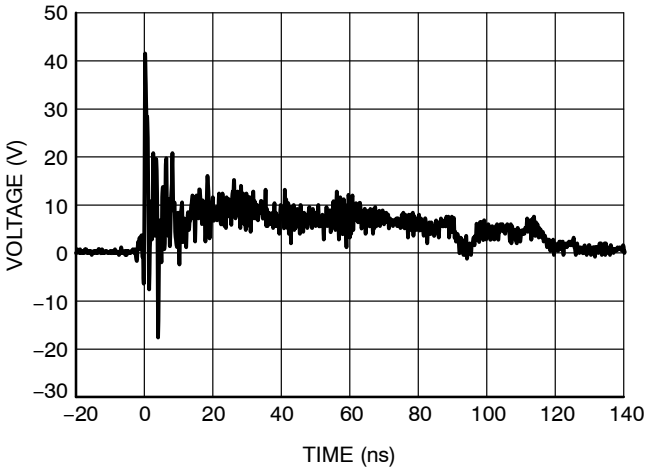


Figure 1. ESD Clamping Voltage − Pin 1 to Pin 2 8 kV Contact per IEC61000−4−2

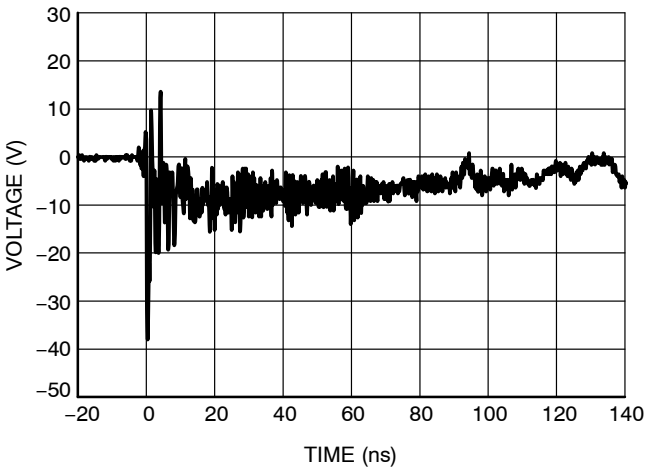


Figure 2. ESD Clamping Voltage − Pin 2 to Pin 1 8 kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

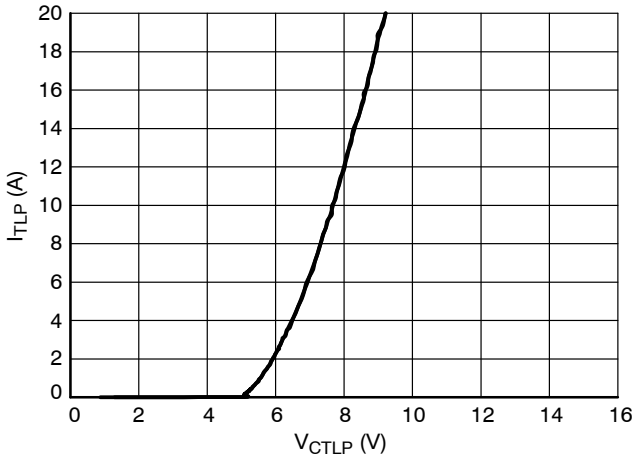


Figure 3. 100 ns TLP I–V Curve – Pin 1 to Pin 2

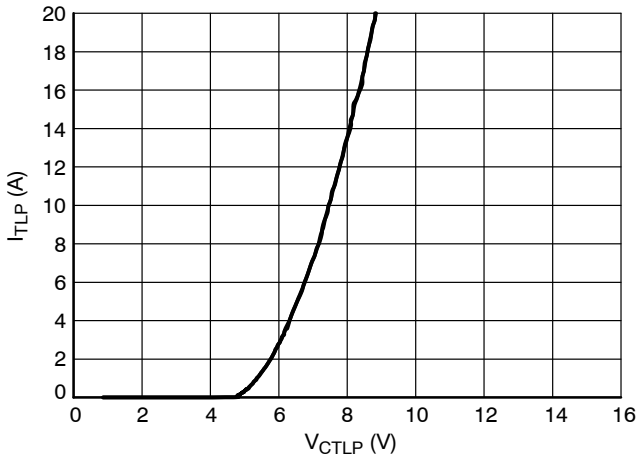


Figure 4. 100 ns TLP I–V Curve – Pin 2 to Pin 1

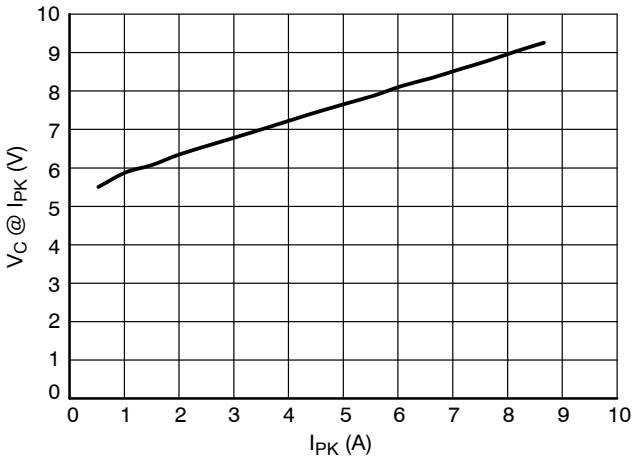


Figure 5. Clamping Voltage vs. Peak Pulse Current – Pin 1 to Pin 2 (t_p = 8/20 μs)

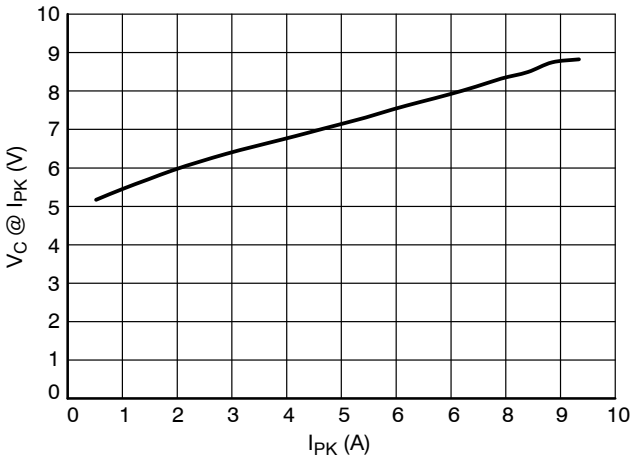


Figure 6. Clamping Voltage vs. Peak Pulse Current – Pin 2 to Pin 1 (t_p = 8/20 μs)

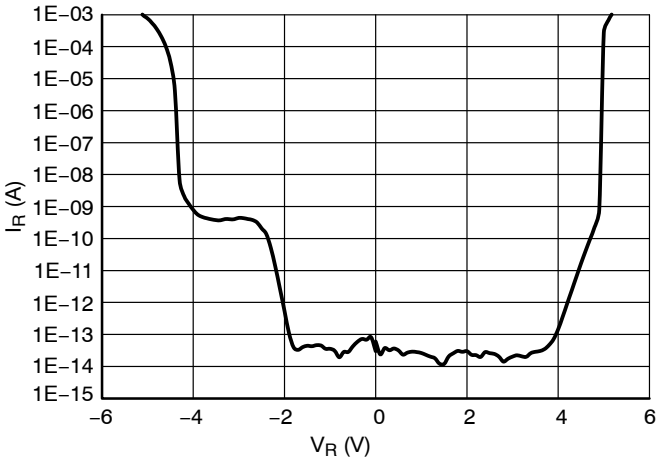


Figure 7. Reverse Leakage Current

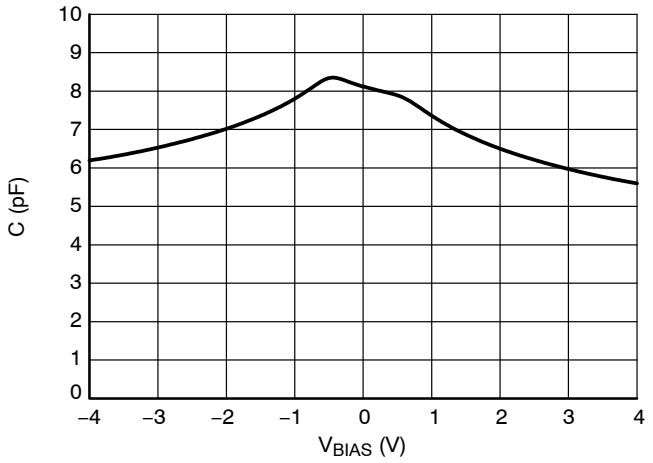


Figure 8. Line Capacitance, *f* = 1 MHz

TYPICAL CHARACTERISTICS

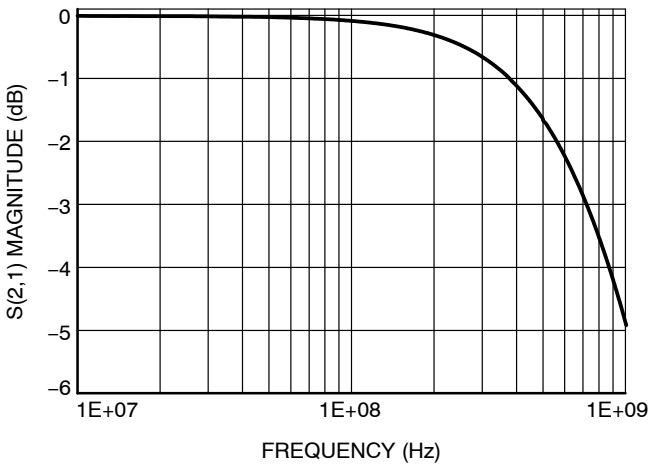


Figure 9. Insertion Loss

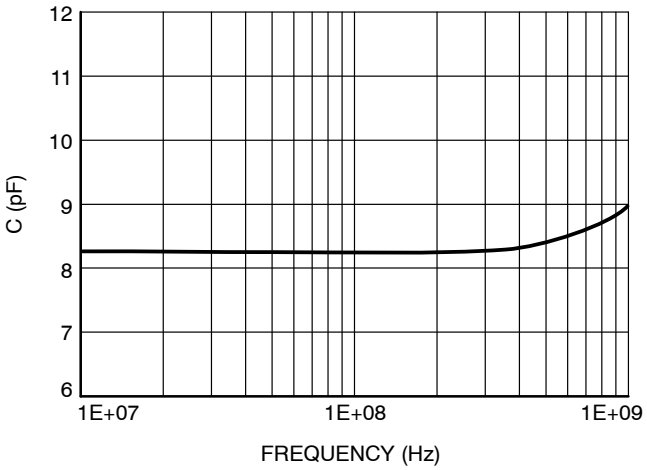


Figure 10. Capacitance Over Frequency

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

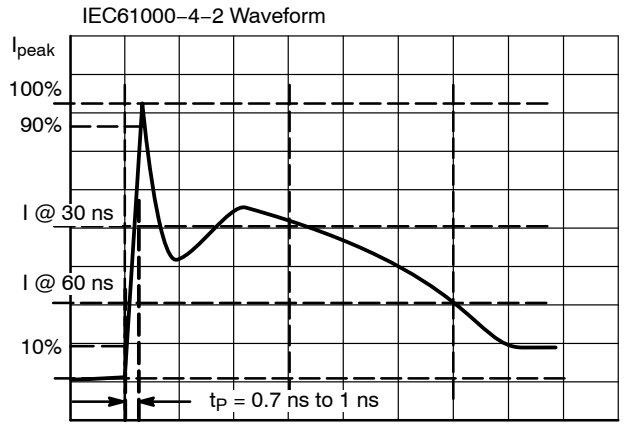


Figure 11. IEC61000−4−2 Spec

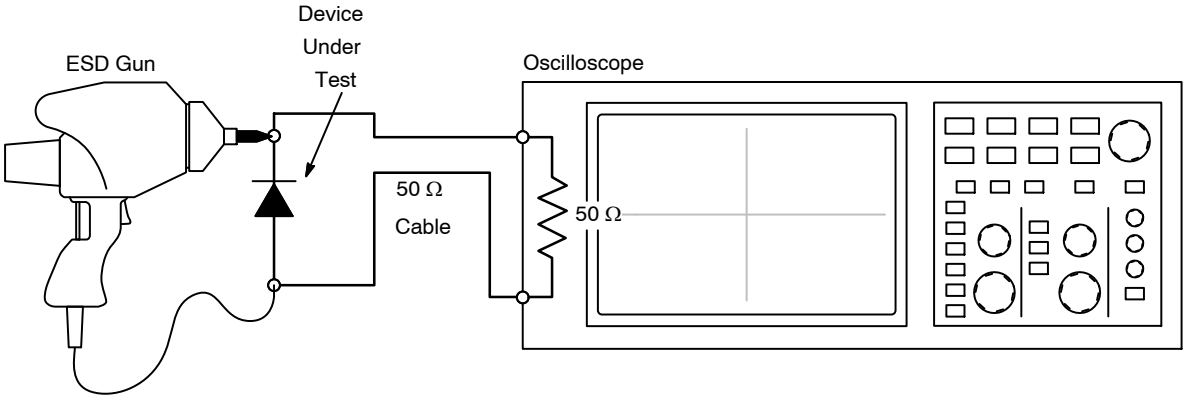


Figure 12. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

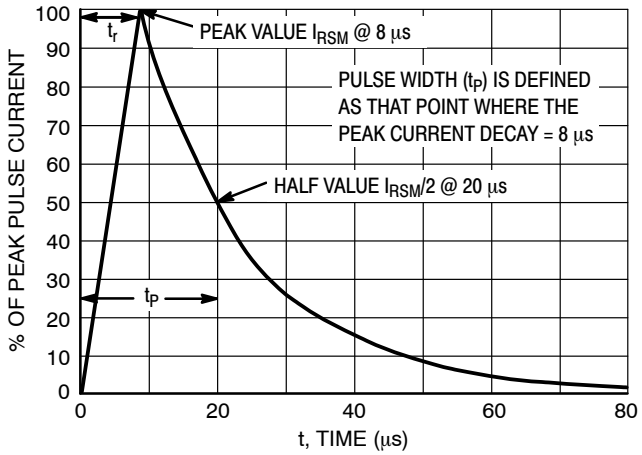


Figure 13. 8 x 20 μs Pulse Waveform

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 14. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 15 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

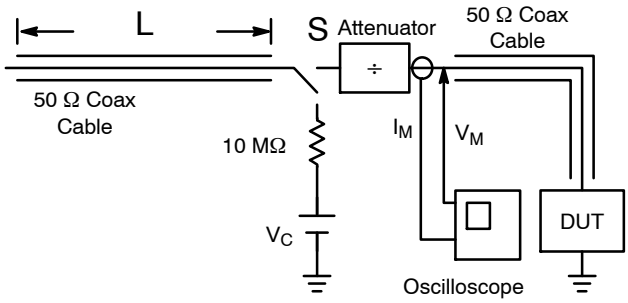


Figure 14. Simplified Schematic of a Typical TLP System

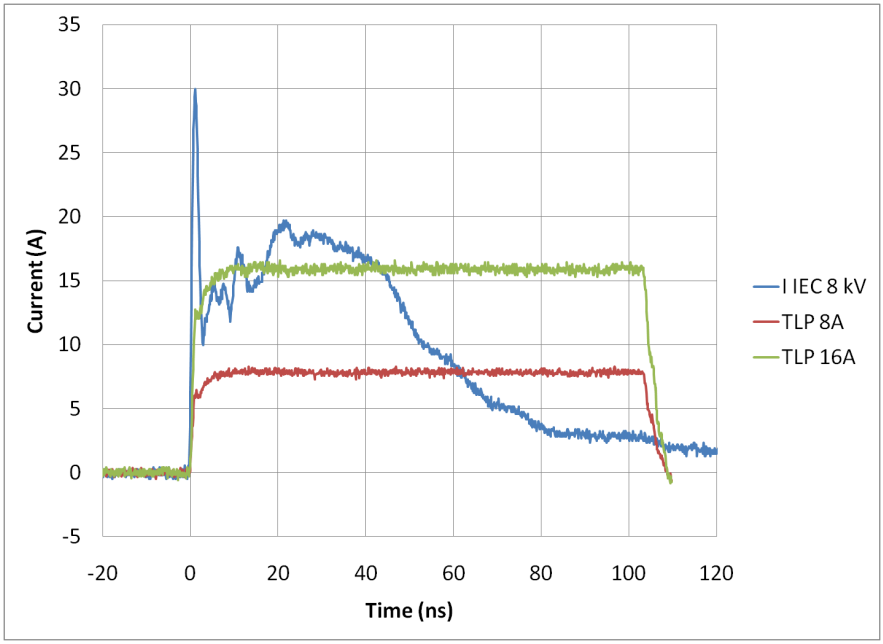


Figure 15. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

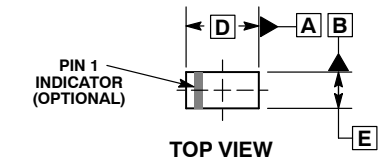
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

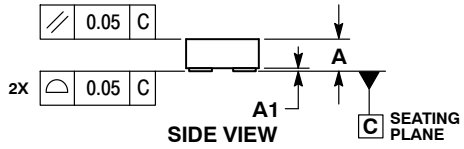
X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE A

SCALE 8:1

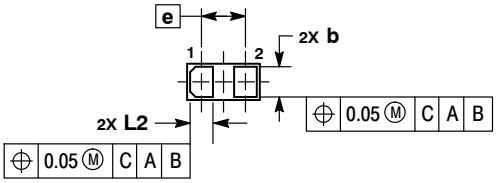
DATE 17 FEB 2015



TOP VIEW



SIDE VIEW

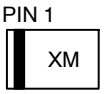


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

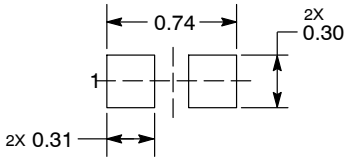
	MILLIMETERS	
DIM	MIN	MAX
A	0.25	0.33
A1	---	0.05
b	0.22	0.28
D	0.58	0.66
E	0.28	0.36
e	0.355 BSC	
L2	0.17	0.23

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**X3DFN2, 0.62X0.32, 0.355P, (0201)**		**PAGE 1 OF 1**

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