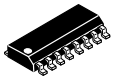
FAD6263

Product Preview

Half-Bridge Gate Driver, 600 V, 3 A

ON Semiconductor®

www.onsemi.com



SOIC−16
CASE 751B

Description

The FAD6263 is a high voltage half bridge gate driver IC providing 2 complementary outputs for driving power MOSFETs or IGBTs in a half−bridge configuration.

It uses the bootstrap technique to ensure a proper drive of the high−side power switch. The driver works with a single input.

Features

- Complementary High and Low Drive Outputs
- Shoot−Through Protection with adjustable Dead−Time
- High Voltage Range: Up to 600 V
- DV/dt Immunity ±50 V/ns
- Matched Propagation Delay 100 ns
- Gate Drive Supply Range from 10 V to 22 V
- Output Source / Sink Current Capability 3 A / 3 A
- 3.3 V and 5 V Input Logic Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to −10 V for Signal Propagation
- Under Voltage LockOut (UVLO) for Both Channels
- Shutdown Pin with Latched Fault State
- AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free, Halogen Free and is RoHS Compliant

Applications

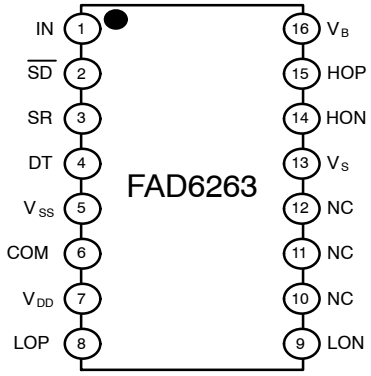
- Automotive
- Motor Control (fans, pumps, compressors)
- MOSFET and IGBT driver applications

MARKING DIAGRAM



FAD6263	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
FAD6263M1X	SOIC−16 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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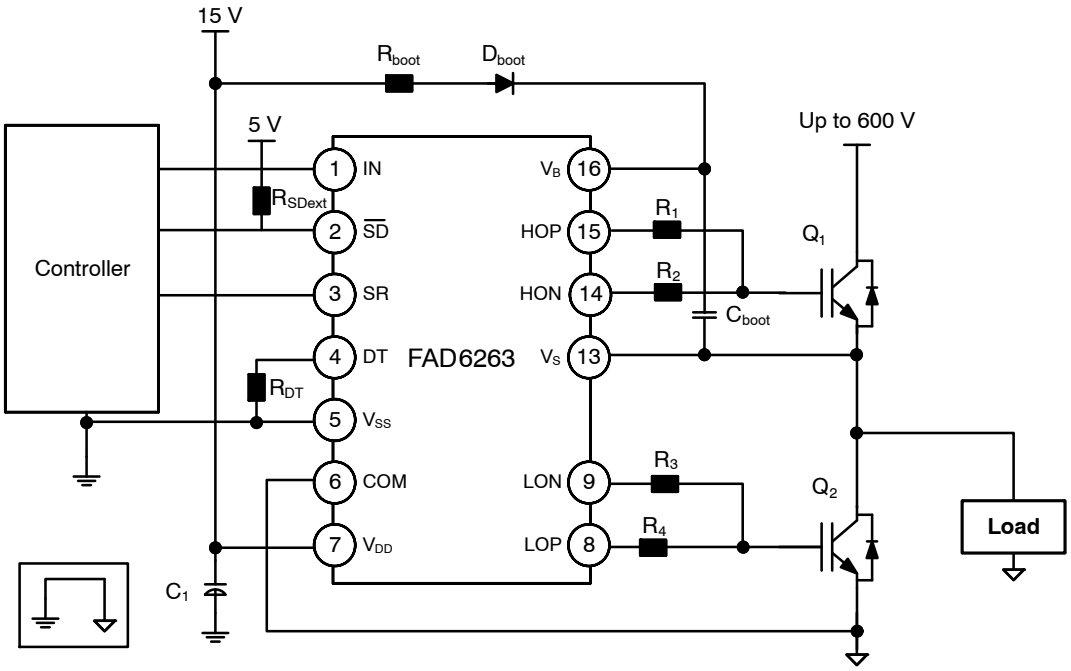


Figure 1. Application Schematic – SOIC16

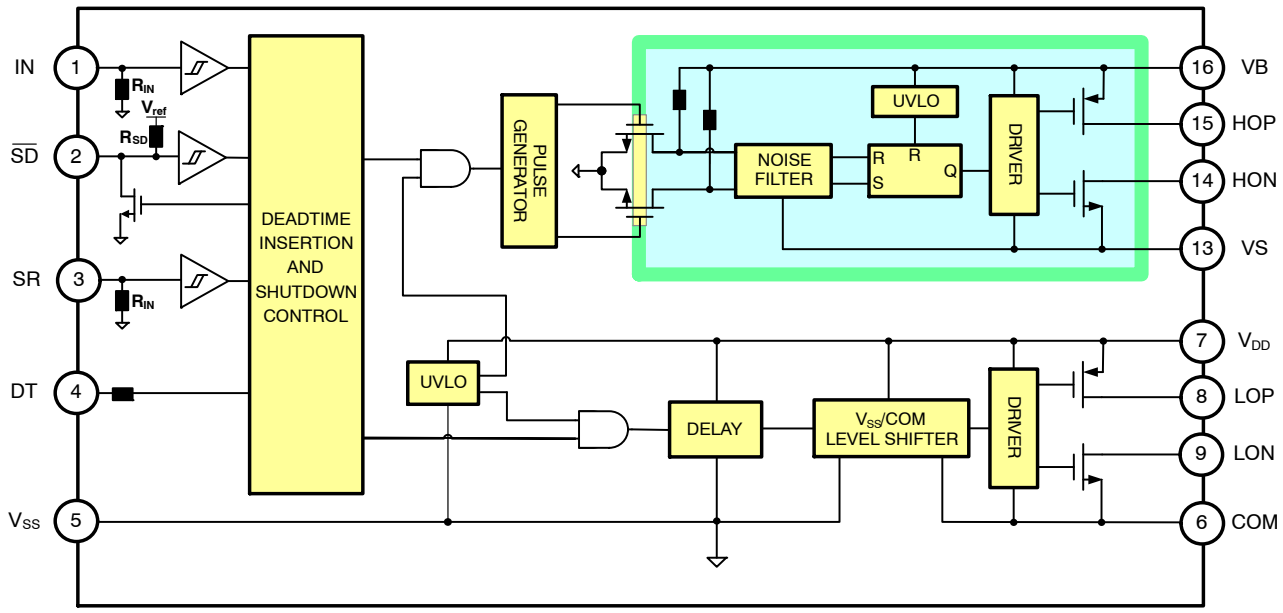


Figure 2. Simplified Block Diagram

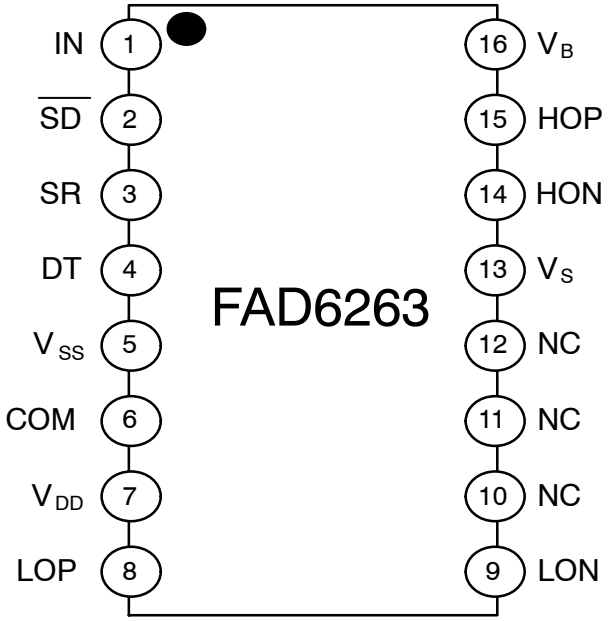


Figure 3. Pin Connection (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
1	IN	Logic Input for Complementary Outputs
2	$\overline{SD}$	Logic Input Shutdown (Active Low)
3	SR	Shutdown Reset
4	DT	Dead−Time Control with External Resistor (referenced to VSS)
5	VSS	Logic Ground
6	COM	Power Ground, Low−Side Driver Return
7	VDD	Low−Side and Logic Power Supply Voltage
8	LOP	Low−Side Driver Output (Pull Up)
9	LON	Low−Side Driver Output (Pull Down)
10	NC	No Electrical Connection (Note 1)
11	NC	No Electrical Connection (Note 1)
12	NC	No Electrical Connection (Note 1)
13	VS	High−Side Floating Supply Return
14	HON	High−Side Driver Output (Pull Down)
15	HOP	High−Side Driver Output (Pull Up)
16	VB	High−Side Floating Supply

1. The lead and the silicon die are not electrically connected. Printed circuit board traces are allowable.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High−Side Floating Supply Voltage	V_B	−0.3 to 625	V
High−Side Floating Offset Voltage	V_S	(V_B − 25) to (V_B + 0.3)	V
High−Side Floating Output Voltage	V_{HO}	(V_S − 0.3) to (V_B + 0.3)	V
Low−Side and Logic−Fixed Supply Voltage	V_{DD}	−0.3 to 25	V
Logic Input Voltage (IN, $\overline{SD}$, SR)	V_{IN}	−0.3 to (V_{DD} + 0.3)	V
Programmable Dead−Time Pin Voltage	DT	−0.3 to (V_{DD} + 0.3)	V
Low−Side Output Voltage	V_{LO}	(COM − 0.3) to (V_{DD} + 0.3)	V
Power Ground	COM	(V_{DD} − 25) to (V_{DD} + 0.3)	V
Allowable Offset Voltage Slew Rate	dV_S/dt	50	V/ns
Power Dissipation (Note 2)	P_D	0.86	W
Thermal Resistance, Junction−to−Ambient (Do not exceed PD under any circumstances Note 3)	θ_{JA}	145	°C/W
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	−55 to 150	°C
ESD Capability, Human Body Model (Note 4)	ESDHBM	2	kV
ESD Capability, Charged Device Model (Note 4)	ESDCDM	2	kV
Moisture Sensitivity Level	MSL	1	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 5)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Do not exceed P_D under any circumstances.
3. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions − natural convection
   JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per ANSI/ESDA/JEDEC JS−001−2012
   ESD Charged Device Model tested per JESD22−C101
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 3. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
High−Side V_s Floating Supply Offset Voltage (Note 6)	V_S	5 − V_{BS}	600	V
High−side V_{BS} Bootstrap Voltage	V_{BS}	V_{BSUV+}	22	V
High−Side Output Voltage	V_{HO}	V_S	V_B	V
Low−Side and Logic Supply Voltage	V_{DD}	V_{DDUV+}	22	V
Low−Side Output Voltage	V_{LO}	COM	V_{DD}	V
Logic Input Voltage (IN, $\overline{SD}$, SR)	V_{IN}	V_{SS}	V_{DD}	V
Programmable Dead−Time Pin Voltage	DT	V_{SS}	V_{DD}	V
Power Ground	COM	V_{DD} − 22	V_{DD}	V
Ambient Temperature (Note 7)	T_A	−40	125	°C
External Shutdown Input Pull−Up Resistance (Note 8)	R_{SDext}	3.1	12.4	kΩ

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Recommended based on min 5 V on VB, for proper operation of the level shifter circuit and ensure proper propagation of the signal from the input to the output.
7. Power and thermal impedance should be determined with case so T_J does not exceed 150°C.
8. Pulled up to 5 V.

Table 4. ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_{SS} = COM = 0 V, DT = V_{SS} and T_A = −40°C to 125°C unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
POWER SUPPLY SECTION (V_{DD} and V_{BS})						
V_{DD} and V_{BS} Supply Under−Voltage Positive−going Threshold		V_{DDUV+} V_{BSUV+}	7.3	8.3	9.3	V
V_{DD} and V_{BS} Supply Under−Voltage Negative−going Threshold		V_{DDUV-} V_{BSUV-}	6.7	7.8	8.6	
V_{DD} and V_{BS} Supply Under−Voltage Lockout Hysteresis Voltage		V_{DDUVH} V_{BSUVH}		0.5		
Offset Supply Leakage Current	V_B = V_S = 600 V	I_{LK}			50	μA
Quiescent V_{DD} Supply Current	V_{IN} = 0 V or 5 V	I_{QDD}		355	550	
Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V	I_{QBS}		45	110	
Operating V_{DD} Supply Current	V_{IN} = 0 V or 5V; f_{SW} = 20 kHz; C_L = 1 nF	I_{PDD}		1000	2000	
Operating V_{BS} Supply Current	V_{IN} = 0 V or 5 V; f_{SW} = 20 kHz; C_L = 1 nF	I_{PBS}		700	1400	
LOGIC INPUT SECTION						
Logic “1” Input Voltage for IN, $\overline{SD}$, SR Threshold (Note 9)		V_{IH}		2.1	2.5	V
Logic “0” Input Voltage for IN, $\overline{SD}$, SR Threshold (Note 9)		V_{IL}	0.8	1.6		
Logic Input High Bias Current	V_{IN} = 5 V	I_{IN+}		20	40	μA
Logic Input Low Bias Current	V_{IN} = 0 V	I_{IN-}			3	
$\overline{SD}$ High Bias Current	$\overline{SD}$ = 5 V	I_{SD+}	−11	−6		μA
$\overline{SD}$ Low Output Voltage (Note 10)	10 kΩ external pull up to 5 V	V_{SD-}			0.8	V
Logic Input Pull−Down/Up Resistance		R_{IN}	125	250		kΩ
Shutdown Input Pull−Up Resistance		R_{SD}	125	250		kΩ
Shutdown Reset Pull−Down Resistance		R_{SRES}	125	250		kΩ
GATE DRIVER OUTPUT SECTION						
High−Level Output Voltage (V_B − V_{OH}) for High Side and (V_{DD} − V_{OL}) for Low Side	V_{IN} = 5 V for High Side, V_{IN} = 0 V for Low Side, No Load (I_O = 0 A)	V_{OH}			10	mV
Low−Level Output Voltage (V_{OH}−V_S) for High Side and (V_{OL} − COM) for Low Side	V_{IN} = 0 V for High Side, V_{IN} = 5 V for Low Side, No Load (I_O = 0 A)	V_{OL}			10	mV
Source Peak Pulsed Current	V_{OH} = 0 V, Pulse Width ≤ 10 μs	I_{O+}	2	3.3		A
Sink Peak Pulsed Current	V_{OH} = 15 V, Pulse Width ≤ 10 μs	I_{O-}	2	3.3		
Allowable Negative V_S Pin Voltage, with signal Propagation capability from IN to HO	V_{BS} = 15 V	V_S	−10			V
Allowable Transient Negative V_S Pin Voltage, no signal propagation capability from IN to HO (Note 12)	V_{BS} = 15 V	V_S	−15			V
Allowable COM−V_{SS} Power/Signal Grounds Offset	V_{DD} = 15 V, V_{SS} = 0 V	COM−V_{SS}	−8			V

Table 4. ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_{SS} = COM = 0 V, DT = V_{SS} and T_A = −40°C to 125°C unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
DYNAMIC SECTION						
Turn−On Propagation Delay (Note 10)	V_S = 0 V, R_{DT} = 0 Ω, C_L = 1000 pF	t_{ON}		155	230	ns
Turn−Off Propagation Delay (Note 11)	V_S = 0 V, C_L = 1000 pF	t_{OFF}		55	90	ns
Delay Matching HO and LO Turn−On		Mt_{ON}			25	ns
Delay Matching HO and LO Turn−Off		Mt_{OFF}			20	ns
Turn−On Rise Time	V_S = 0 V, C_L = 1000 pF	t_R		10	23	ns
Turn−Off Fall Time		t_F		10	20	ns
Dead−Time: LO Turn−Off to HO Turn−On, HO Turn−Off to LO Turn−On	R_{DT} = 0 Ω	DT	85	120	160	ns
	R_{DT} = 200 kΩ		0.7	1	1.5	μs
Dead−Time Matching: $\lvert DT_{LO-HO} - DT_{HO-LO} \rvert$	R_{DT} = 0 Ω	MDT		10		ns
	R_{DT} = 200 kΩ			75		ns
Shutdown Minimum Pulse Width		t_{SDMIN}	270	310	450	ns
Shutdown Reset Minimum Pulse Width		t_{SRMIN}	1	1.6	2.4	μs
UVLO Response Time (Note 12)				15		μs
POR Settling Time after Vdd Ramp Up		t_{POR}		50		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. SR Logic Input Voltage guaranteed by design.
10. The turn−on propagation delay includes the dead time.
11. Turn−off propagation applies to $\overline{SD}$ pin. See Figure 37 for timing definitions.
12. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

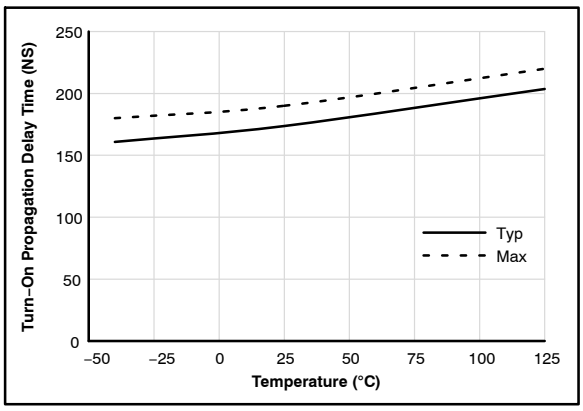


Figure 4. Turn−On Propagation Delay vs. Temperature

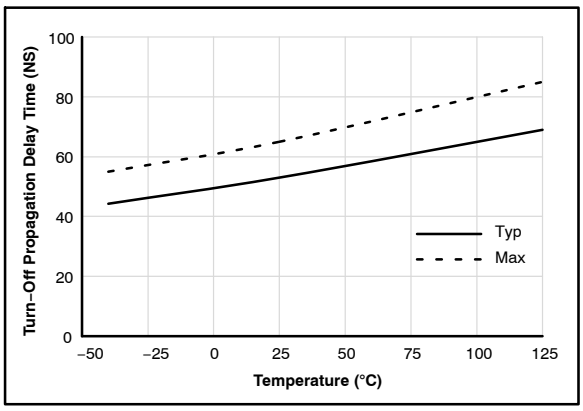


Figure 5. Turn−Off Propagation Delay vs. Temperature

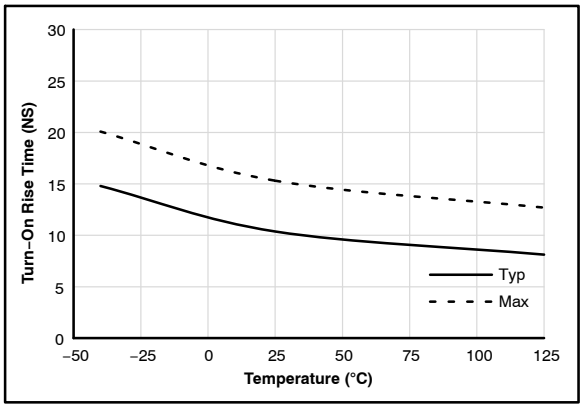


Figure 6. Turn−On Rise Time vs. Temperature

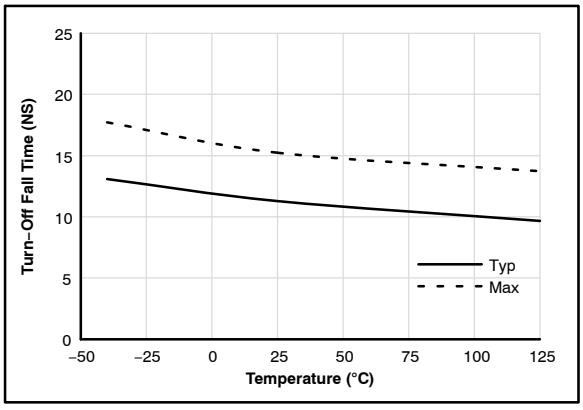


Figure 7. Turn−Off Fall Time vs. Temperature

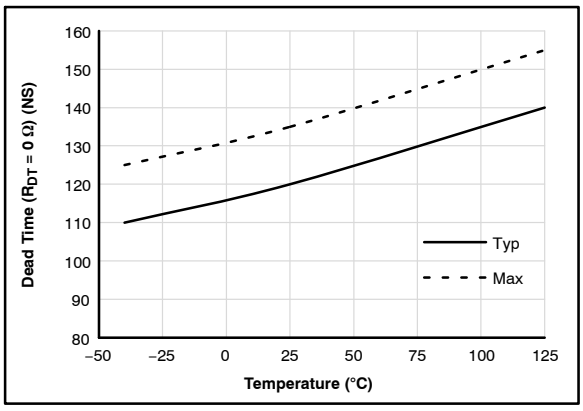


Figure 8. Dead Time (R_{DT} = 0 Ω) vs. Temperature

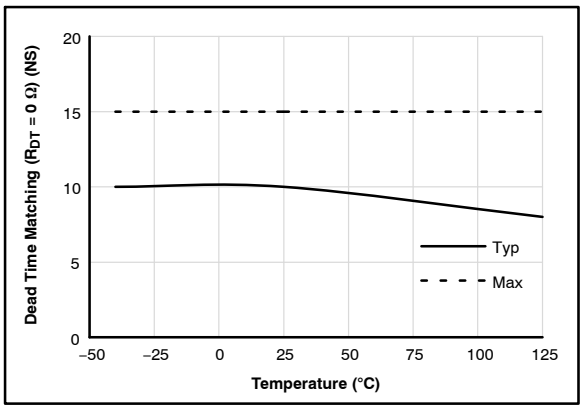


Figure 9. Dead Time Matching (R_{DT} = 0 Ω) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

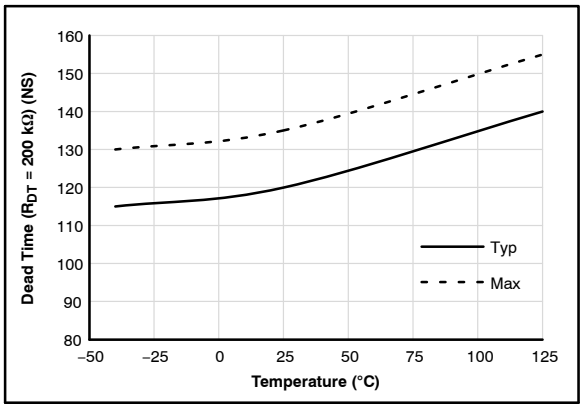


Figure 10. Dead Time (R_{DT} = 200 kΩ) vs. Temperature

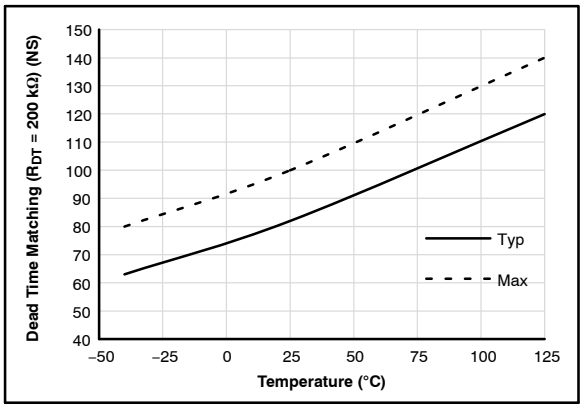


Figure 11. Dead Time Matching (R_{DT} = 200 kΩ) vs. Temperature

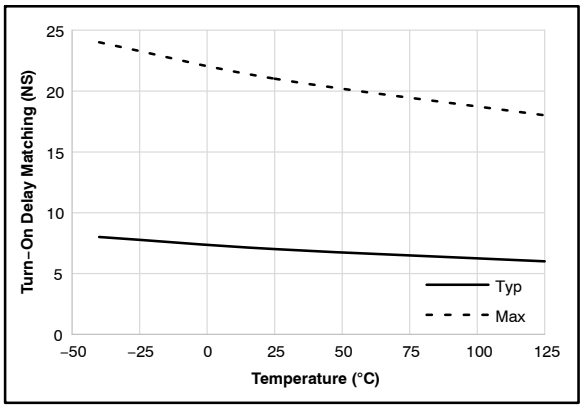


Figure 12. Turn−On Delay Matching vs. Temperature

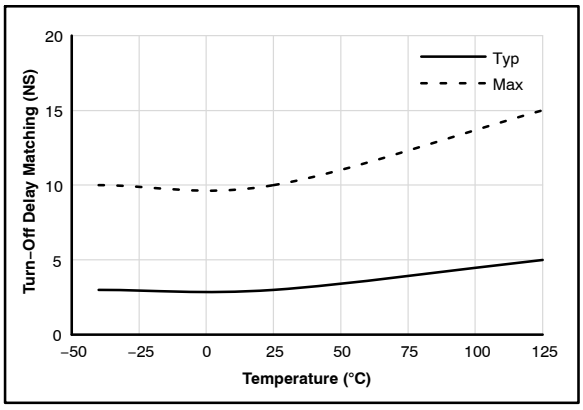


Figure 13. Turn−Off Delay Matching vs. Temperature

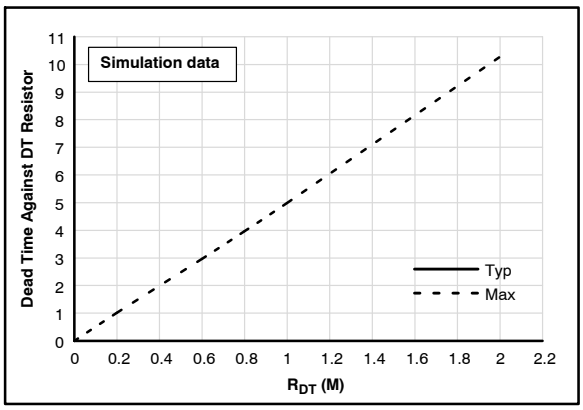


Figure 14. Dead Time vs. R_{DT}

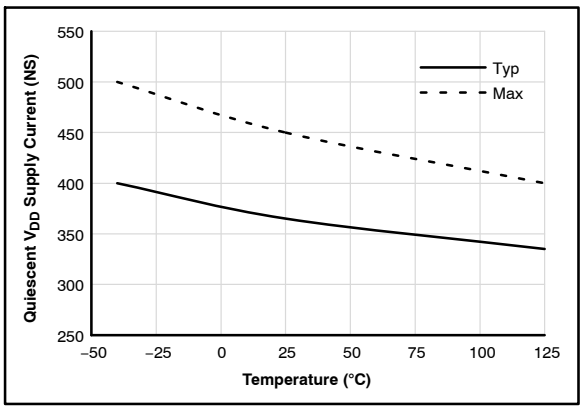


Figure 15. Quiescent V_{DD} Supply Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

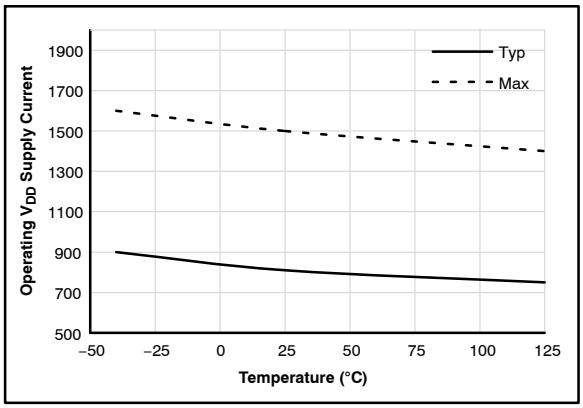


Figure 16. Operating V_{DD} Supply Current vs. Temperature

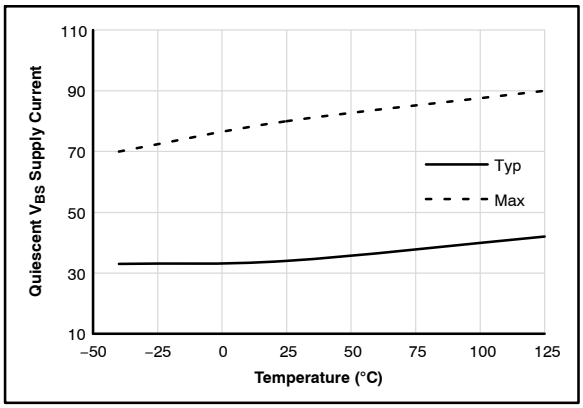


Figure 17. Quiescent V_{BS} Supply Current vs. Temperature

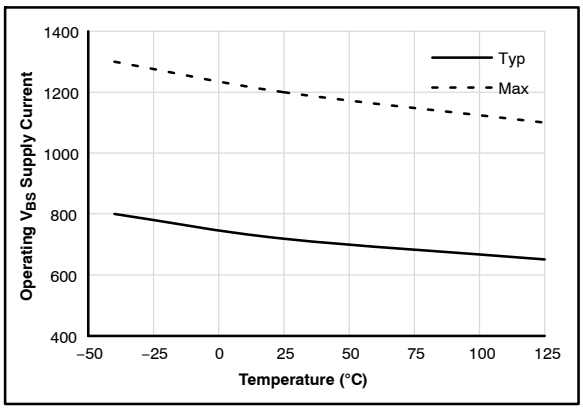


Figure 18. Operating V_{BS} Supply Current vs. Temperature

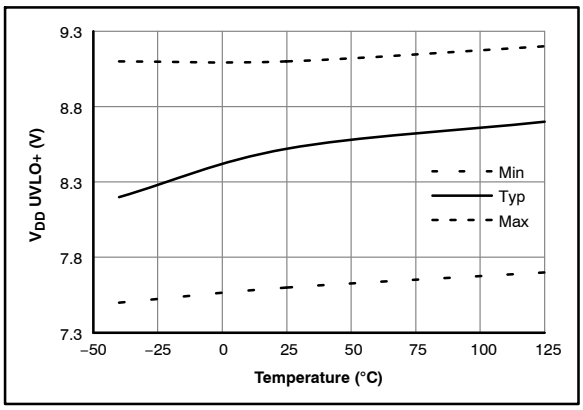


Figure 19. V_{DD} UVLO+ vs. Temperature

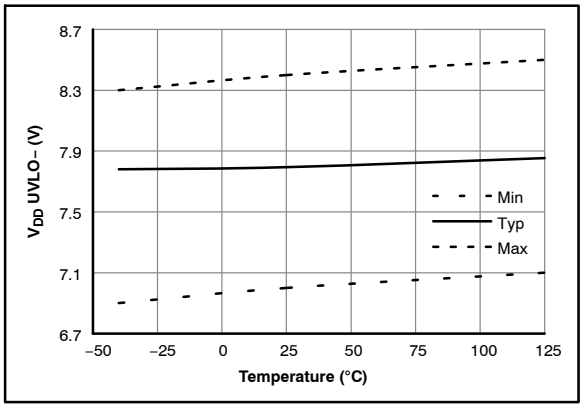


Figure 20. V_{DD} UVLO− vs. Temperature

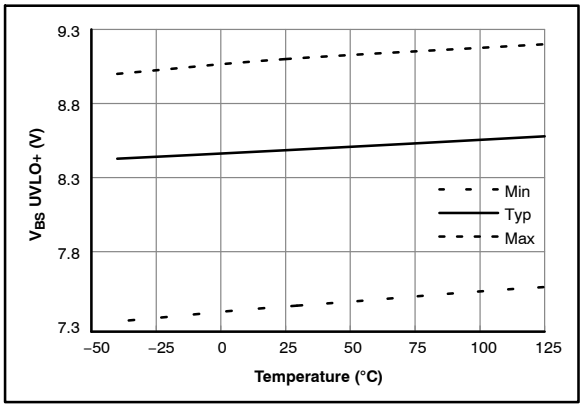


Figure 21. V_{BS} UVLO+ vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

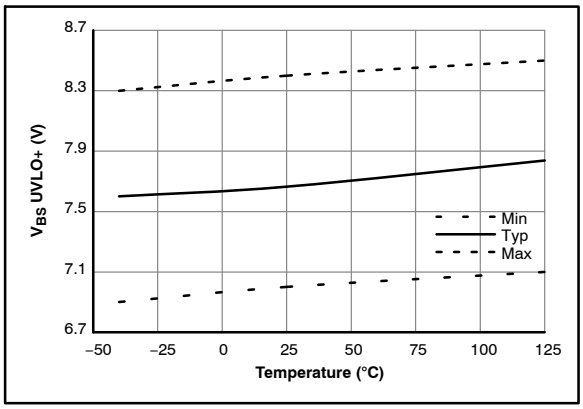


Figure 22. V_{BS} UVLO− vs. Temperature

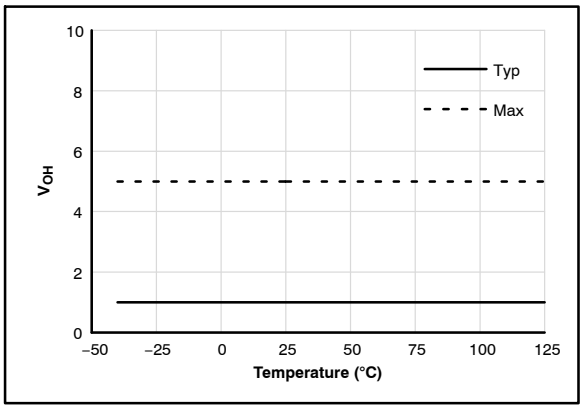


Figure 23. High−Level Output Voltage vs. Temperature

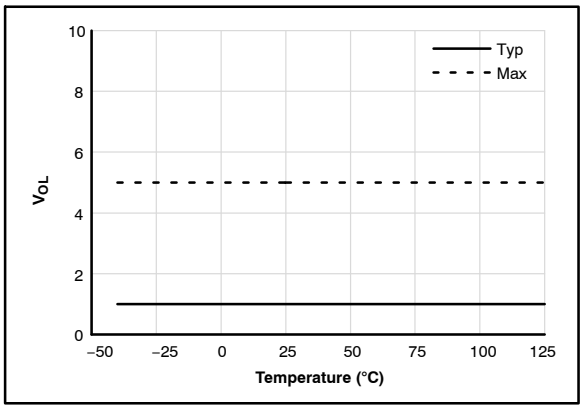


Figure 24. Low−Level Output Voltage vs. Temperature

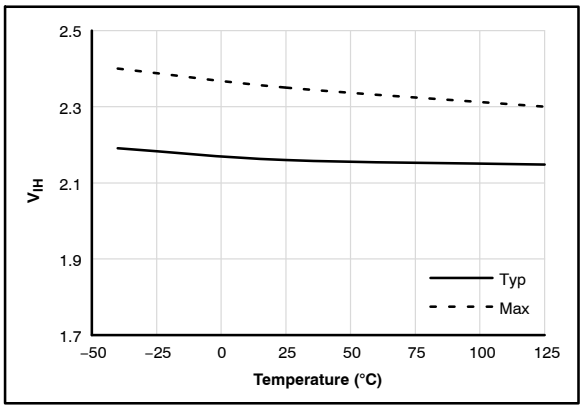


Figure 25. Logic HIGH Input Voltage vs. Temperature

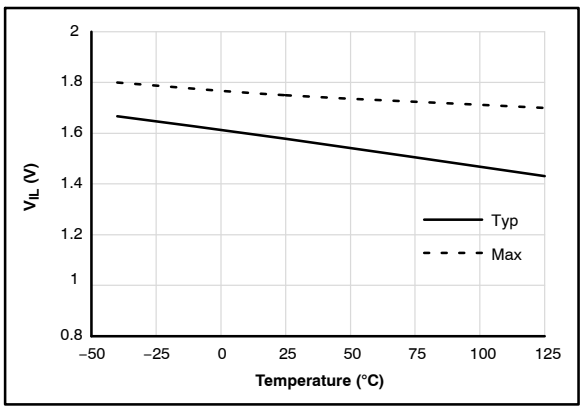


Figure 26. Logic LOW Input Voltage vs. Temperature

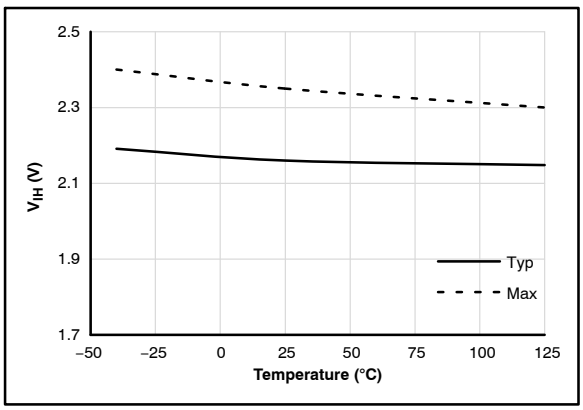


Figure 27. Logic Input HIGH Bias Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

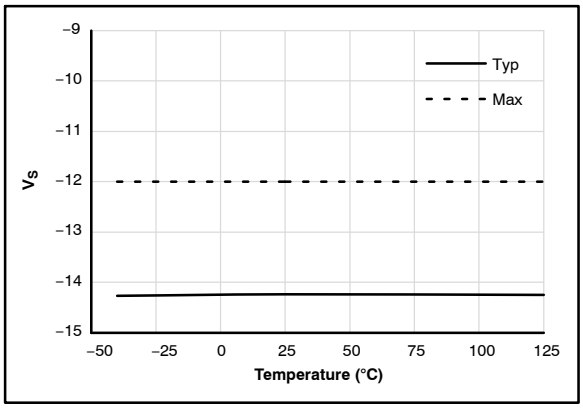


Figure 28. Allowable Negative V_S Voltage vs. Temperature

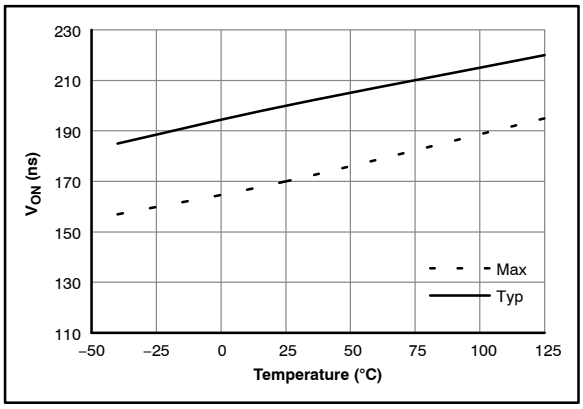


Figure 29. Turn−on Propagation Delay vs. Supply Voltage

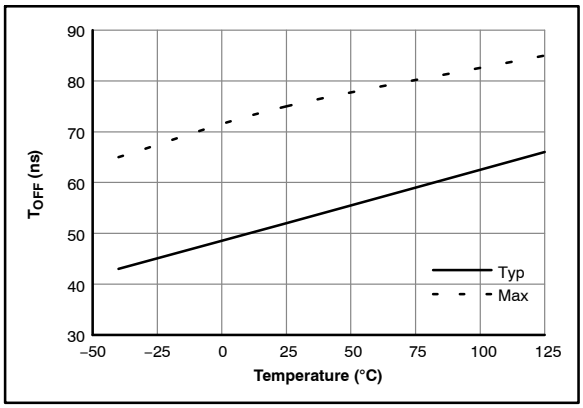
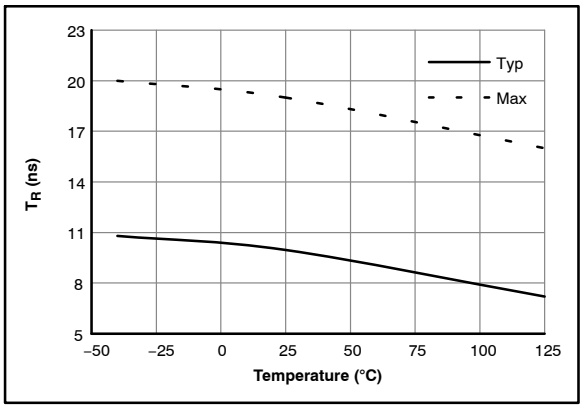


Figure 30. Turn−off Propagation Delay vs. Supply Voltage



TOFF (ns)

Figure 31. Turn−on Rise Time vs. Supply Voltage

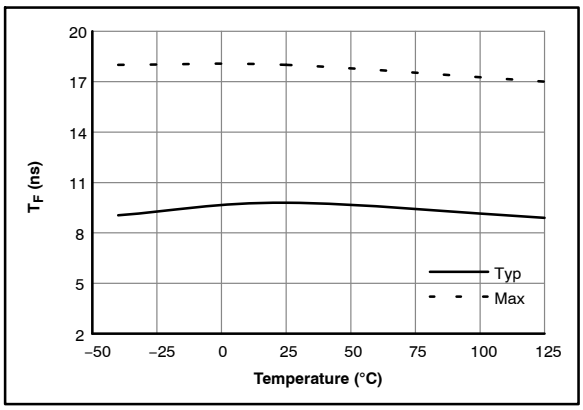


Figure 32. Turn−off Rise Time vs. Supply Voltage

SWITCHING TIME DEFINITIONS

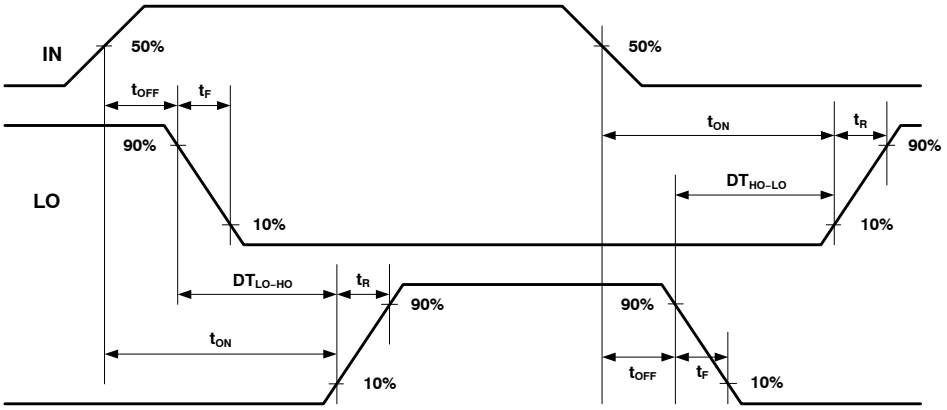


Figure 33. Switching Time and Dead−Time Waveform Definition

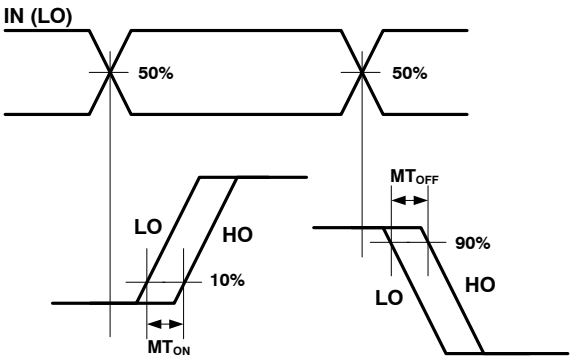


Figure 34. Delay Matching Waveform Definition

APPLICATIONS DESCRIPTION

Power On Reset (POR) Sequence

The purpose of the POR sequence is to ensure that the logic circuitry has reached a stable state after Vdd has ramped up before the gate driver can be operated:

1. Ramp up V_{DD} to the target operating voltage.
2. Wait during t_{POR} for the internal logic to settle.
3. Apply a SR pulse to ensure the LO output is activated.
4. Wait sufficient time for the bootstrap capacitor to charge.
5. Operate the device as intended.

It is recommended to keep IN low until the bootstrap capacitor is properly charged.

The POR sequence is illustrated in Figure 35.

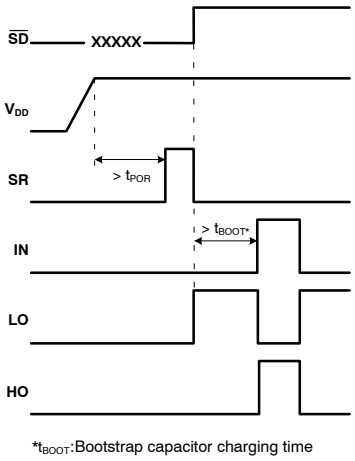


Figure 35. POR Sequence

Shut Down and Reset Signal

This section describes how to use the $\overline{SD}$ and the SR pins to shutdown the driver outputs, ie pull down all outputs independently from the input signal, and to reactivate them.

When the SR pin is pulled down, the $\overline{SD}$ pin is used to trigger a shutdown of the driver outputs and the SR pin is then used to reactivate the outputs.

The sequence with the SR pin pulled down:

- To shutdown the outputs, pull down the $\overline{SD}$ pin for a minimum duration of t_{SDMIN}.
- After being pulled down externally, the $\overline{SD}$ pin is kept low/latched by the internal pull down transistor. The equivalent Rdson resistance of the internal pull down transistor in latch mode is around 300 Ω.
- The output of the driver remains shutdown as long as the $\overline{SD}$ pin is kept pulled down.
- The $\overline{SD}$ pin is released and the outputs are reactivated by pulling up the SR pin for a duration of t_{SRMIN}.

Refer to Figure 36.

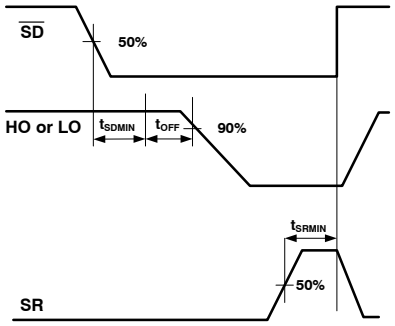


Figure 36. Shutdown with SR Pin Pulled Down – Timing Waveform Definition

Operating and Reset Signal

Important note: once pulled down, the pin should not be pulled up externally otherwise:

- The HO and LO will be reactivated for the duration that $\overline{SD}$ is forced high.
- Additional current drawn by the $\overline{SD}$ pin through its internal pull down circuit will add needlessly to the total power dissipation of the IC. With equivalent Rdson resistance of 300 Ω, the internal pull down transistor in latch mode can dissipate additional 83 mW if the $\overline{SD}$ pin is forced externally to 5 V.

To prevent this situation after $\overline{SD}$ is latch to low, it is recommended to not force externally any state to $\overline{SD}$ to avoid any conflict with the internal logic of the driver. The $\overline{SD}$ must have the possibility to be pulled up by the external pull up resistor Rsdext after a pulse is given on the SR pin.

To do so, the $\overline{SD}$ could be driven by a pull up open drain circuit.

Alternate Operating Mode with SR Pin Pulled Up and SD Pin Used as Enable

When the SR pin is kept pulled up, the pin operates similar to an Enable. With the SR pin pulled up:

- When the pin is pulled down, all outputs are pulled down independently from the input pin.
- When the pin is pulled up, the outputs are activated and respond to the input pin.

Note: as long as the SR pin is pulled up, the pin does not draw any current through its internal pull down transistor. The internal pull down transistor remains open with SR pin being pulled up.

Refer to Figure 37.

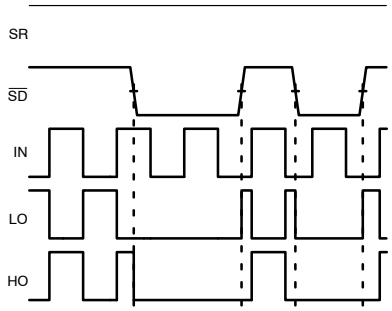


Figure 37. Shutdown with SR Pin Pulled Down SR Pin Pulled Up

Adjustable Dead time

The dead time between turn off and turn on of the opposite outputs can be adjusted with an external resistor. The relation between the resistor value and the dead time is defined in the Figure 14.

A floating DT pin would not allow any output to turn on. This pin must be connected to ground with a proper resistor.

UVLO

Two independent Under Voltage Lock Out circuitries monitor the Vbs voltage and the Vdd to Vss voltage.

- If the Vbs voltage drops below the negative going threshold voltage, then the output of the high side is pulled down.
- If the Vdd voltage drops below the negative going threshold voltage, then the output of the low side as well as the output of the high side is pulled down.

In both cases, the outputs will be reactivated at the next positive edge at the input after the Vbs/Vdd voltages reach again the positive going threshold voltage.

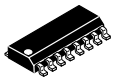
Note that an under voltage lockout event has no impact to the Shutdown functionality and it does not need a signal on the SR pin to reactivate the output.

Pull Up and Pull Down Outputs

The turn on and turn off speed can be defined separately without the need for a diode in the gate resistance path.

HOP and LOP are the pull up output stages that command the turn on of the power switch to drive. The value of R1 and R3 consequently impacts the turn on speed.

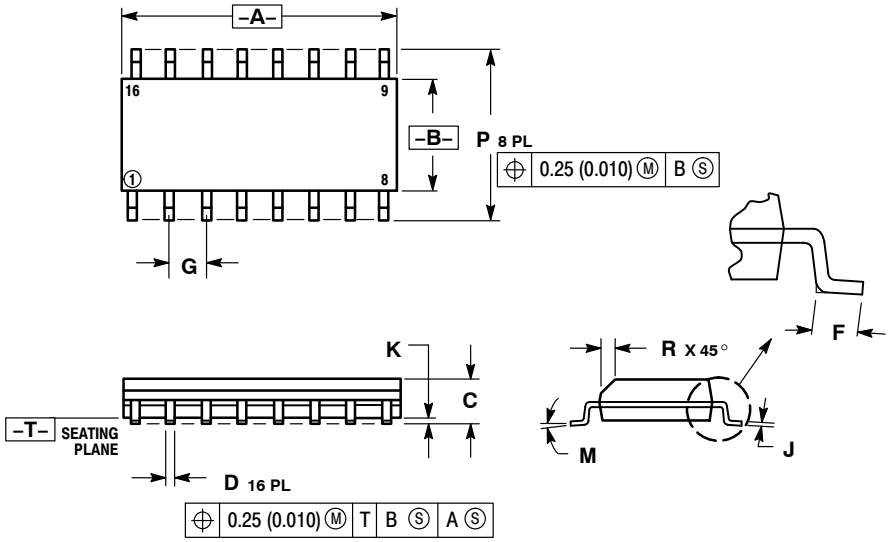
HON and LON are the pull down output stages that command the turn off of the power switch to drive. The value of R2 and R4 consequently impacts the turn off speed.



SCALE 1:1

SOIC–16
CASE 751B–05
ISSUE K

DATE 29 DEC 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

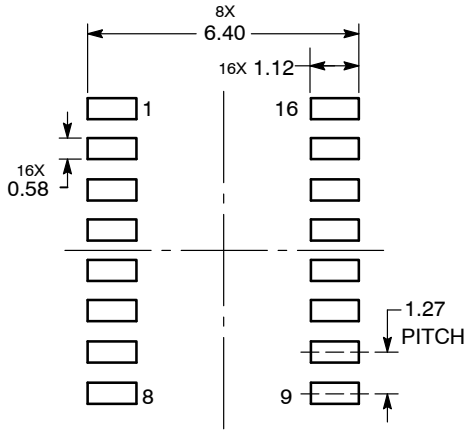
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT



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