Microphone Pre-Amplifier with Digital Output

FAN3852

Description

The FAN3852 integrates a pre−amplifier, LDO, and ADC that converts Electret Condenser Microphone (ECM) outputs to digital Pulse Density Modulation (PDM) data streams. The pre−amplifier accepts analog signals from the ECM and drives an over−sampled sigma delta Analog−to−Digital Converter (ADC) and outputs PDM data. The PDM digital audio has the advantage of noise rejection and easy interface to mobile handset processors.

The FAN3852 features an integrated LDO and is powered from the system supply rails up to 3.63 V, with low power consumption of only 0.85 mW and less than 20 μW in Power−Down Mode.

Features

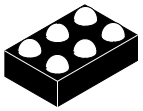
- Optimized for Mobile Handset and Notebook PC Microphone Applications
- Accepts Input from Electret Condenser Microphones (ECM)
- Pulse Density Modulation (PDM) Output
- Standard 5−Wire Digital Interface
- Low Input Capacitance, High PSR, 20 kHz Pre−Amplifier
- Low−Power 1.5 μA Sleep Mode
- Typical 420 μA Supply Current
- SNR of 62 dB (A) for 16 dB Gain
- Total Harmonic Distortion 0.02%
- Input Clock Frequency Range of 1−4 MHz
- Integrated Low Drop−Out Regulator (LDO)
- Small 1.242 mm × 0.842 mm 6−Ball, 0.400 mm pitch standard WLCSP Package
- 1.5 kV HBM ESD on MIC Input

Typical Applications

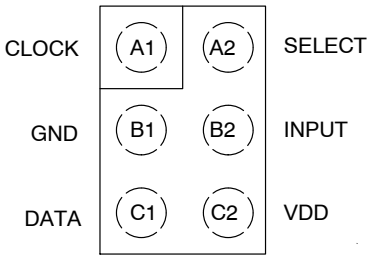
- Electret Condenser Microphones with Digital Output
- Mobile Handset
- Headset Accessories
- Personal Computer (PC)

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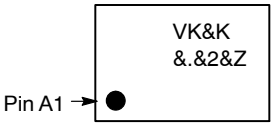
WLCSP−6
CASE 567TS



Top View

PIN CONFIGURATION

MARKING DIAGRAM



VK	= Device Identifier
K	= Lot Run Code
.	= Pin A1 Mark
2	= Date Code
Z	= Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method†
FAN3852UC16X	−40°C to 85°C	6 Ball, Wafer−Level Chip−Scale Package (WLCSP)	3000 Units/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

INTERNAL BLOCK DIAGRAM

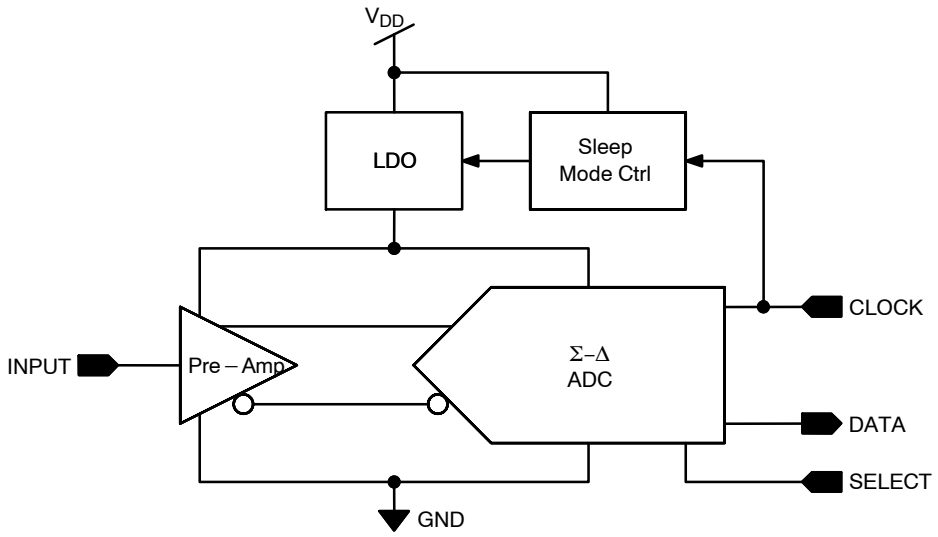


Figure 1. Block Diagram

Table 1. PIN DEFINITIONS

Pin #	Name	Type	Description
A1	CLOCK	Input	Clock Input
B1	GND	Input	Ground Pin
C1	DATA	Output	PDM Output − 1 Bit ADC
A2	SELECT	Input	Rising or Falling Clock Edge Select
B2	INPUT	Input	Microphone Input
C2	VDD	Input	Device Power Pin

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	−0.3	4.0	V
V_{IO}	Digital I/O	−0.3	V_{DD} + 0.3	V
	Microphone Input	−0.3	2.2	
ESD	Human Body Model, JESD22−A114, All Pins Except Microphone Input	±8		kV
	Human Body Model, JESD2−A114 − Microphone Input	±1.5		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device is fabricated using CMOS technology and is therefore susceptible to damage from electrostatic discharges. Appropriate precautions must be taken during handling and storage of this device to prevent exposure to ESD.

Table 3. RELIABILITY INFORMATION

Symbol	Rating	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	−65		+125	°C
T_{RFLW}	Peak Reflow Temperature			+260	°C
θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		90		°C/W

2. T_A = 25°C unless otherwise specified

Table 4. RECOMMENDED OPERATING CONDITIONS

Symbol	Rating	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	−40		+85	°C
V_{DD}	Supply Voltage Range	1.64	1.80	3.63	V
T_{RF-CLK}	Clock Rise and Fall Time			10	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. DEVICE SPECIFIC ELECTRICAL CHARACTERISTICS

Symbol	Value	FAN3852UC16X			Unit
		Min.	Typ.	Max.	
SNR	Signal−to−Noise Ratio f_{IN} = 1 kHz (1 Pa), A−Weighted		62		dB (A)
e_N	Total Input RMS Noise 20 Hz to 20 kHz, A−Weighted		5.74	6.80	μV_{RMS}
V_{IN}	Maximum Input Signal f_{IN} = 1 kHz, THD + N < 10%, Level = 0 V			448	mV_{PP}

3. Guaranteed by characterization and/or design. Not production tested.

Table 6. ELECTRICAL CHARACTERISTICS

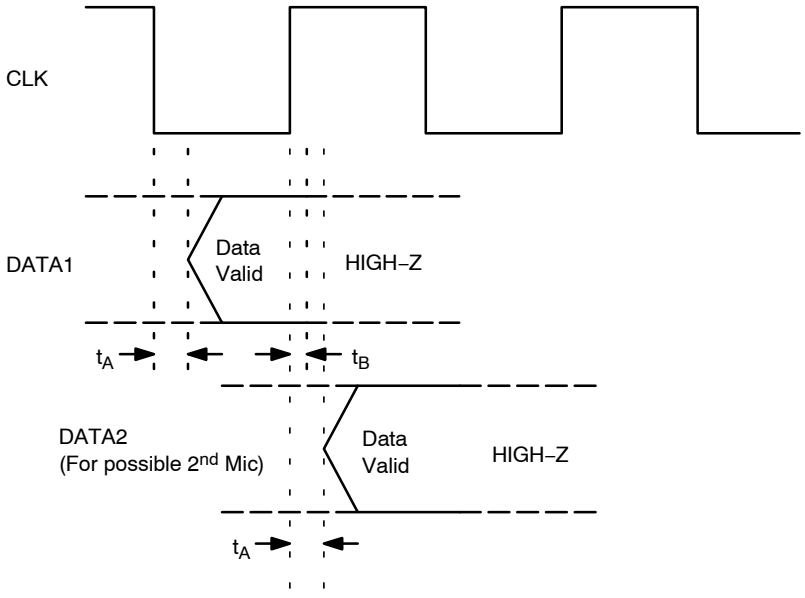
Unless otherwise specified, al limits are guaranteed for T_A = 25°C, V_{DD} = 1.8 V, V_{IN} = 94 dB (SPL) and f_{CLK} = 2.4 MHz. Duty Cycle = 50% and C_{MIC} = 15 pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage Range		1.64	1.80	3.63	V
I_{DD}	Supply Current	INPUT = AC Coupled to GND, CLOCK = On, No Load		420		μA
I_{SLEEP}	Sleep Mode Current	f_{CLK} = GND		1.50	8.0	μA
PSR	Power Supply Rejection (Note 5)	INPUT = AC Coupled to GND, Test Signal on V_{DD} = 217 Hz, Square Wave and Broadband Noise (Note 4), Both 100 mV_{P-P}		−74		dBFS
IN_{NOM}	Nominal Sensitivity (Note 6)	INPUT = 94 dBSPL (1 Pa)		−26		dBFS
THD	Total Harmonic Distortion (Note 7)	f_{IN} = 1 KHz, INPUT = −26 dBFS		0.02	0.20	%
THD+N	THD and Noise (Note 5)	50 Hz ≤ f_{IN} ≤ 1 kHz, INPUT = −20 dBFS		0.2	1.0	%
		f_{IN} = 1 KHz, INPUT = −5 dBFS		1.0	5.0	
		f_{IN} = 1 KHz, INPUT = 0 dBFS		5.0	10.0	
C_{IN}	Input Capacitance (Note 8)	INPUT		1.3		pF
R_{IN}	Input Resistance (Note 8)	INPUT	>10			GΩ
V_{IL}	CLOCK & SELECT Input Logic LOW Level				0.3	V

Table 6. ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified, al limits are guaranteed for T_A = 25°C, V_{DD} = 1.8 V, V_{IN} = 94 dB (SPL) and f_{CLK} = 2.4 MHz. Duty Cycle = 50% and C_{MIC} = 15 pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	CLOCK & SELECT Input Logic HIGH Level		1.5		V_{DD}+0.3	V
V_{OL}	Data Output Logic LOW Level				0.35*V_{DD}	V
V_{OH}	Data Output Logic HIGH Level		0.65*V_{DD}			V
V_{OUT}	Acoustic Overload Point (Note 8)	THD+N < 10%	120			dBSPL
t_A	Time from CLOCK Transition to Data becoming Valid	On Falling Edge of CLOCK, SELECT = GND, C_{LOAD} = 15 pF	18	43		ns
t_B	Time from CLOCK Transition to Data becoming HIGH−Z	On Rising Edge of CLOCK, SELECT = GND, C_{LOAD} = 15 pF	0	5	16	ns
t_A	Time from CLOCK Transition to Data becoming Valid	On Rising Edge of CLOCK, SELECT = V_{DD}, C_{LOAD} = 15 pF	18	58		ns
t_B	Time from CLOCK Transition to Data becoming HIGH−Z	On Falling Edge of CLOCK, SELECT = V_{DD}, C_{LOAD} = 15 pF	0	5	16	ns
f_{CLK}	Input CLOCK Frequency (Note 9)	Active Mode	1.0	2.4	4.0	MHz
CLK_{dc}	CLOCK Duty Cycle (Note 5)		40	50	60	%
t_{WAKEUP}	Wake−Up Time (Note 10)	f_{CLK} = 2.4 MHz		0.35	2.00	ms
$t_{FALLASLEAP}$	Fall−Asleep Time (Note 11)	f_{CLK} = 2.4 MHz	0	0.01	1.00	ms
C_{LOAD}	Load Capacitance on Data				100	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pseudo−random noise with triangular probability density function. Bandwidth up to 10 MHz.
5. Guaranteed by characterization. Not production tested.
6. Assuming that 120 dB (SPL) is mapped to 0 dBFS.
7. Assuming an input of −45 dBV.
8. Guaranteed by design. Not production tested.
9. All parameters are tested at 2.4 MHz. Frequency range guaranteed by characterization.
10. Device wakes up when $f_{CLK} \geq$ 300 kHz.
11. Device falls asleep when $f_{CLK} \leq$ 70 kHz.



t_A − Microphone delay from clock edge to data assertion.
t_B − Microphone delay from clock edge to high−impedance state.
$t_A > t_B$ to have interim HIGH−Z state in both signals.

Figure 2. Interface Timing

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{DD} = 1.8 V, V_{IN} = 94 dB (SPL), f_{CLK} = 2.4 MHz and duty Cycle = 50%.

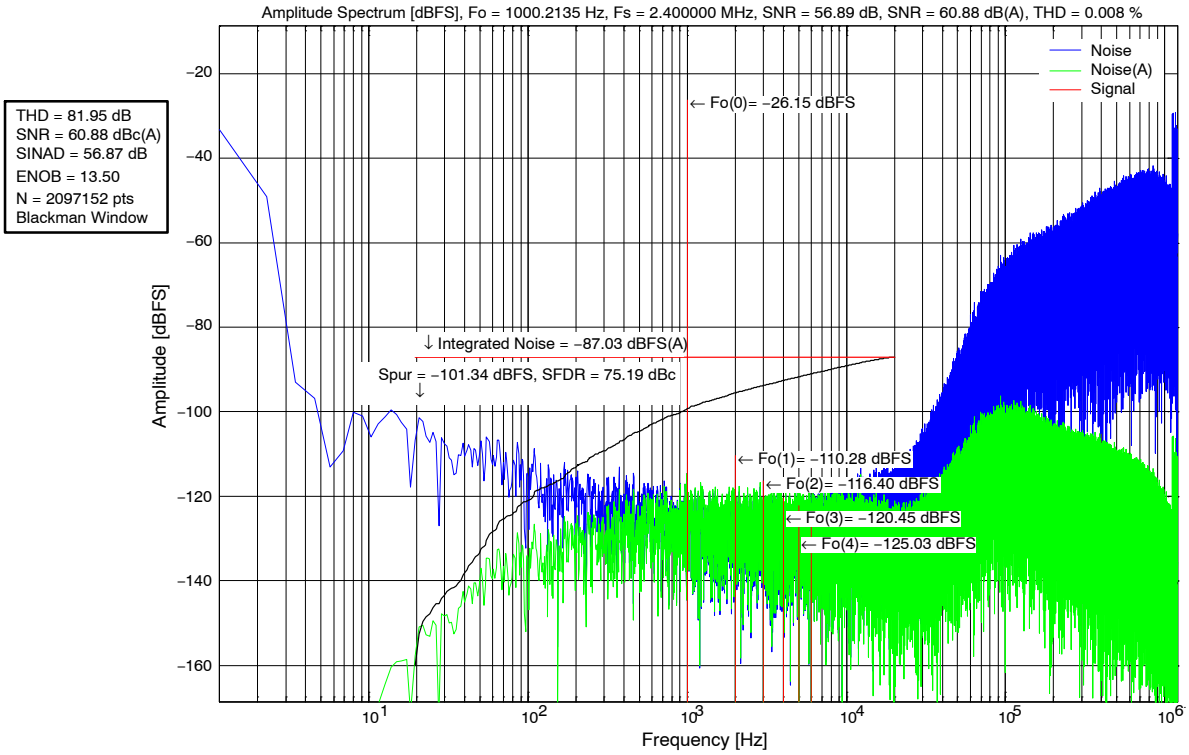


Figure 3. Noise vs. Frequency

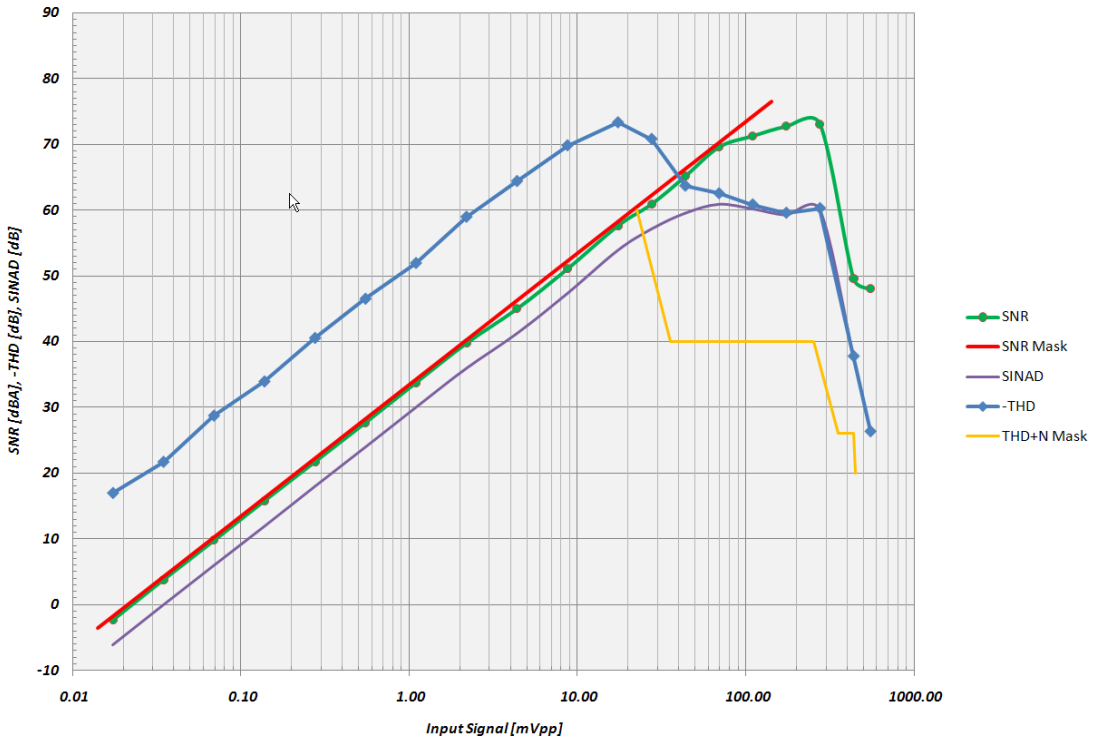


Figure 4. THD, SINDA, and SNR vs. Input Amplitude

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{DD} = 1.8 V, V_{IN} = 94 dB (SPL), f_{CLK} = 2.4 MHz and duty Cycle = 50%.

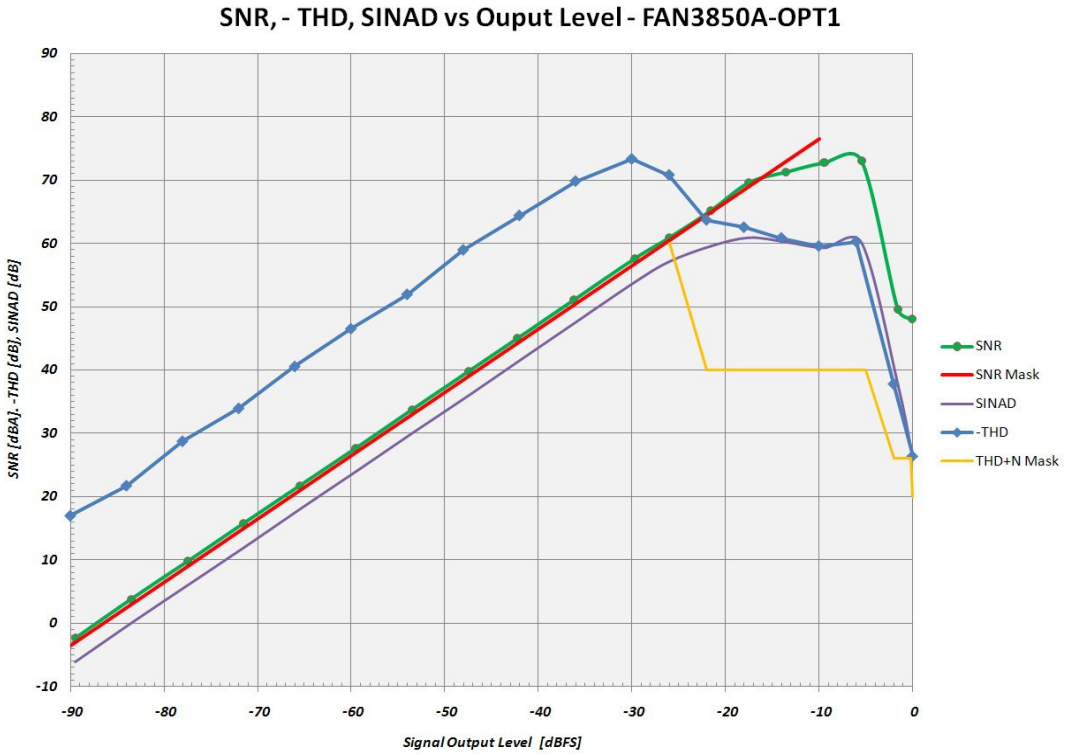


Figure 5. THD, SINAD and SNR vs. Output Level

Temp (°C)	Delta (dB)
−40	0.1971
−30	0.1644
−20	0.1260
−10	0.0954
0	0.0657
10	0.0359
20	0.0139
25	0.0000
30	−0.0097
40	−0.0344
50	−0.0514
60	−0.0739
70	−0.0998
80	−0.1183
85	−0.1271

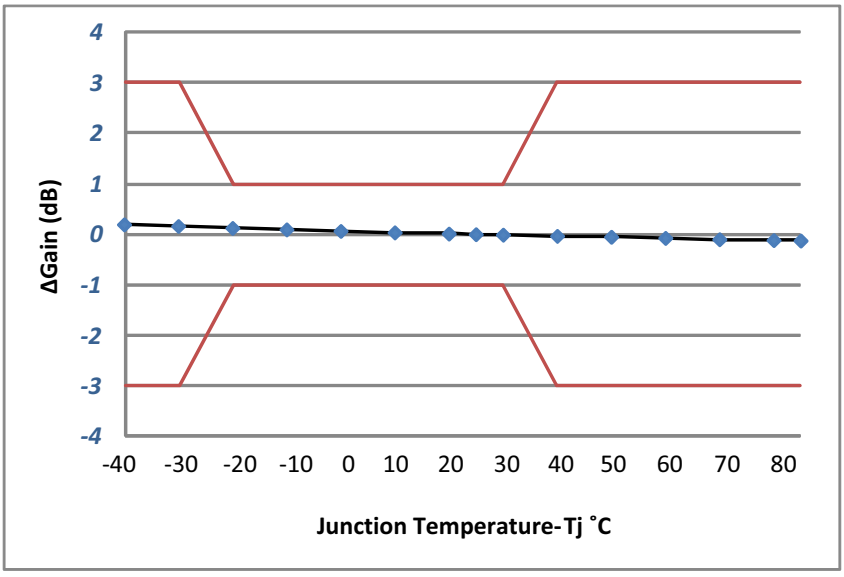


Figure 6. Δ Gain vs. Temperature (Nominal Temperature = 25°C)

APPLICATIONS INFORMATION

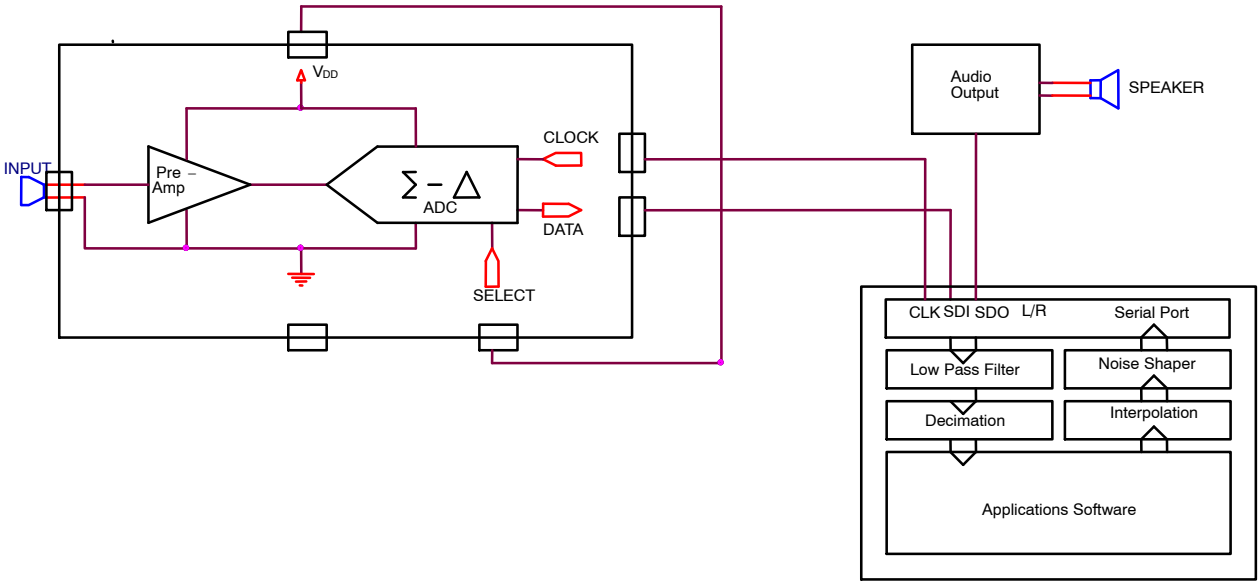


Figure 7. Mono Microphone Application Circuit

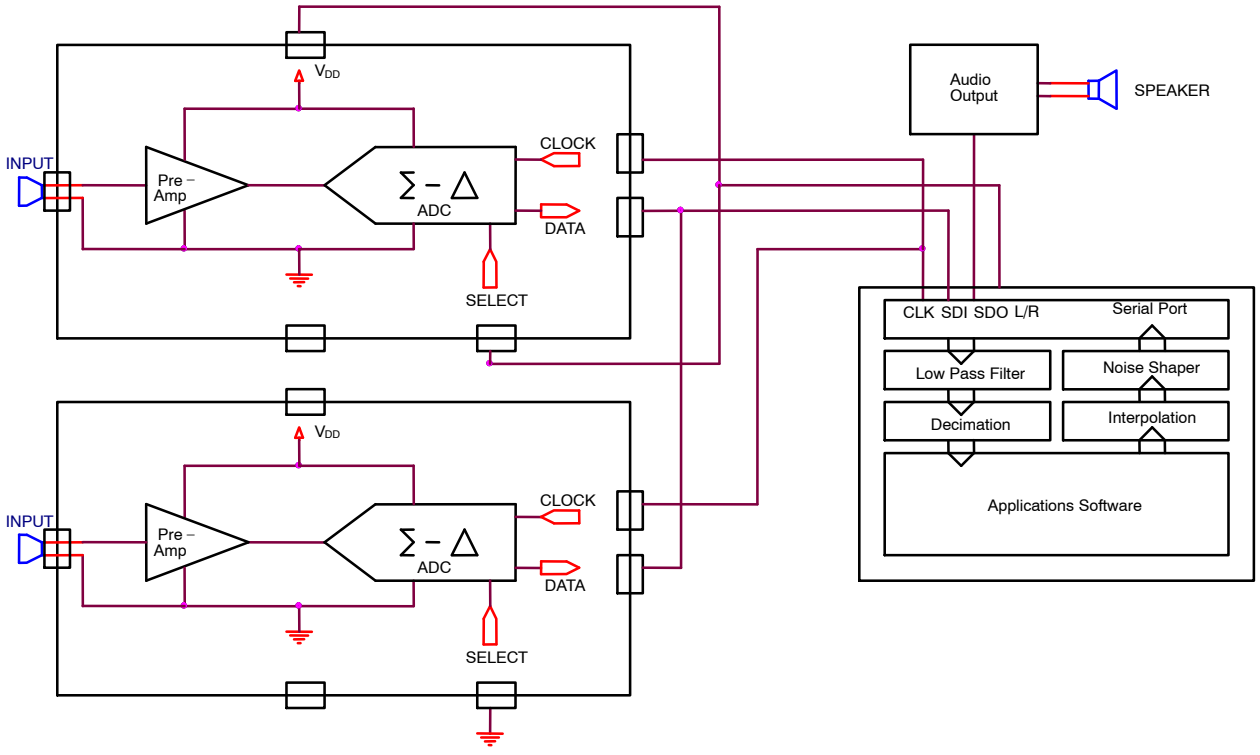


Figure 8. Stereo Microphone Application Circuit

APPLICATIONS INFORMATION (continued)

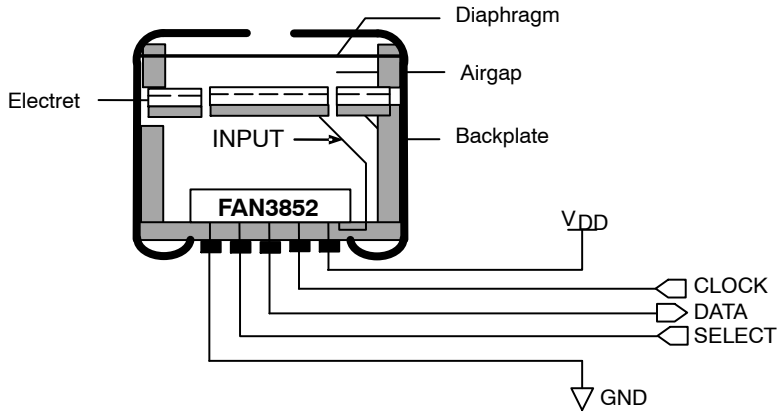


Figure 9. MIC Element Drawing

A 0.1 μF decoupling capacitor is required for VDD. It can be located inside the microphone or on the PCB very close to the VDD pin.

Due to high input impedance, care should be taken to remove all flux used during the reflow soldering process.

A 100 Ω resistance is recommended on the clock output of the device driving the FAN3852 to minimize ringing and improve signal integrity.

For optimal PSR, route a trace to the VDD pin. Do not place a VDD plane under the device.

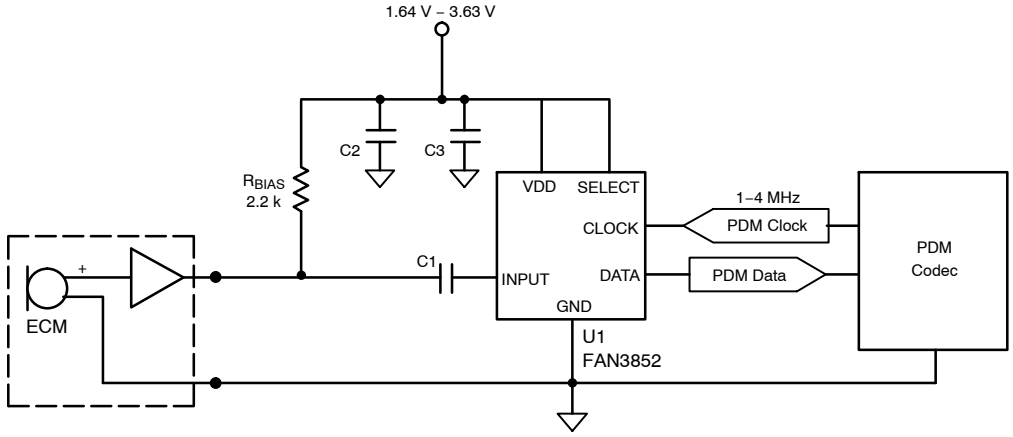


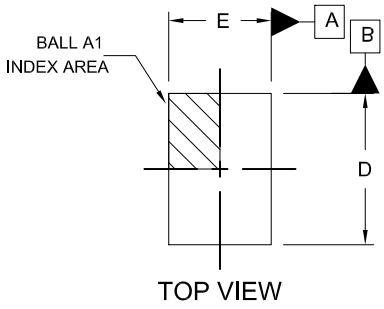
Figure 10. Example Hardware Implementation

Table 7. RECOMMENDED COMPONENTS

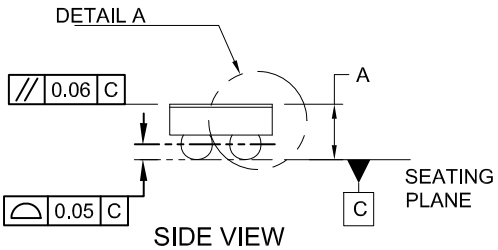
Ref Des	Qty	Description of Options	Package	Manufacturer	Mfg PIN
U1	1	FAN3852 Microphone Pre−Amplifier with Digital Output	WLCSP6	ON Semiconductor	FAN3852UC16X
C1	1	Input AC Coupling Capacitor; 1 nF/1000 pF, ≥ 6.3 V, low−leakage	0402	Johansen Dielectrics	500R07W102KV4T
			0402	Murata	GCM155R71H102KA37D
			0603	Taiyo Yuden	UMK107SD102KA−T
C2	1	Primary VDD Decoupling Capacitor; 0.1 μF, MLCC, ≥ 6.3 V	0402	Samsung	CL05B104KO5NNNC
			0402	Yageo	CC0402KRX7R7BB104
			0603	AVX	06033C104KAT4A
C3	1	Optional VDD Decoupling Capacitor; 0.01 μF, MLCC, ≥ 6.3 V	0402	Samsung	CL05B103KB5VPNC
			0402	Murata	GCM155R71H103KA55J
			0603	Yageo	CC0603KRX7R7BB103

WLCSP6 1.242x0.842x0.457
CASE 567TS
ISSUE A

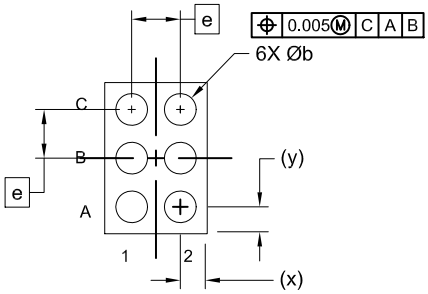
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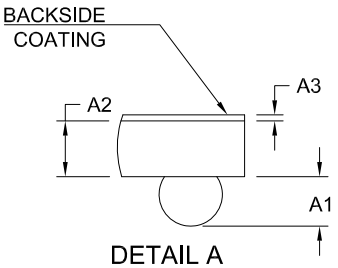
TOP VIEW



SIDE VIEW



BOTTOM VIEW

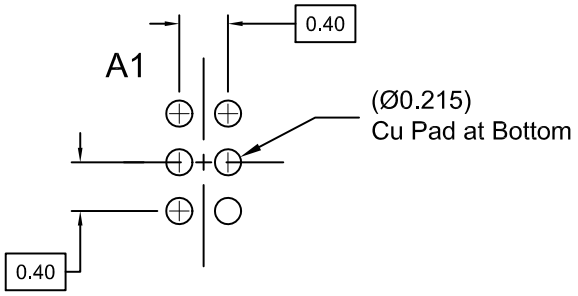


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.419	0.457	0.495
A1	0.183	0.203	0.223
A2	0.214	0.229	0.244
A3	0.022	0.025	0.028
b	0.24	0.26	0.28
D	1.212	1.242	1.272
E	0.812	0.842	0.872
e	0.40 BSC		
x	0.206	0.221	0.236
y	0.206	0.221	0.236



RECOMMENDED MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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