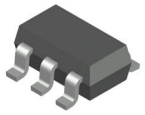
High Efficiency, High Current Serial LED Driver with 30 V Integrated Switch

FAN5333A, FAN5333B



SOT−23, LEAD−5
CASE 527AH

Description

The FAN5333A/FAN5333B is a general purpose LED driver that features fixed frequency mode operation and an integrated FET switch. The device's high output power makes it suitable to drive flash LEDs in serial connections. This device is designed to operate at high switching frequencies in order to minimize switching noise measured at the battery terminal of hand−held communications equipment. Quiescent current in both normal and shutdown mode is designed to be minimal in order to extend battery life. Normal or shutdown mode can be selected by a logic level shutdown circuitry.

The low ON−resistance of the internal N−channel switch ensures high efficiency and low power dissipation. A cycle−by−cycle current limit circuit keeps the peak current of the switch below a typical value of 1.5 A. The FAN5333A/FAN5333B is available in a 5−lead SOT23 package.

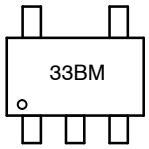
Features

- 1.5 MHz Switching Frequency
- Low Noise
- Adjustable Output Voltage
- Up to 1.5 A Peak Switch Current
- 1.5 W Output Power Capability
- Low Shutdown Current: <1 μA
- Cycle−by−Cycle Current Limit
- Low Feedback Voltage
- Over−Voltage Protection
- Fixed−Frequency PWM Operation
- Internal Compensation
- FAN5333A has 110 mV Feedback Voltage
- FAN5333B has 315 mV Feedback Voltage
- Thermal Shutdown
- 5−Lead SOT23 Package
- These Devices are Pb−Free and Halide Free

Applications

- Cell Phones
- PDAs
- Handheld Equipment
- Display Bias
- LED Bias
- Flash LED

MARKING DIAGRAM



33B = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FAN5333ASX	SOT−23−5 (Pb-Free/ Halide Free)	3000 / Tape & Reel
FAN5333BSX	SOT−23−5 (Pb-Free/ Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL APPLICATION

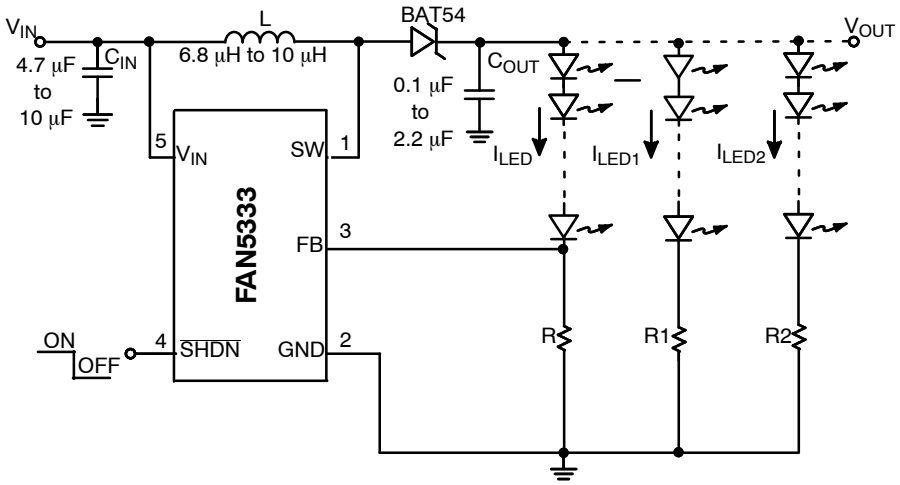


Figure 1. Typical Application Diagram

PIN ASSIGNMENT & DESCRIPTION

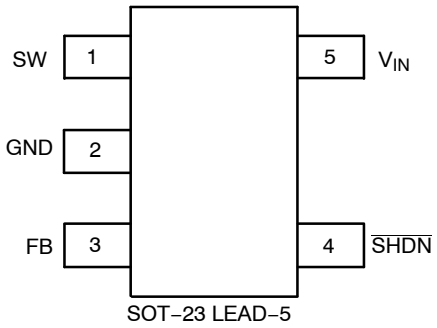


Figure 2. Pin Assignment

Table 1. PIN DESCRIPTION

Pin	Name	Description
1	SW	Switching Node
2	GND	Analog and Power Ground
3	FB	Feedback Pin. Feedback node that connects to an external current set resistor
4	$\overline{SHDN}$	Shutdown Control Pin. Logic HIGH enables, logic LOW disables the device
5	V_{IN}	Input Voltage Pin

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
V_{IN} to GND		6.0	V
FB, $\overline{SHDN}$ to GND	−0.3	V_{IN} + 0.3	V
SW to GND	−0.3	35	V
Lead Soldering Temperature (10 seconds)		300	°C
Junction Temperature		150	°C
Storage Temperature	−55	150	°C
Thermal Resistance (Θ_{JA})		210	°C/W
Electrostatic Discharge Protection (ESD) Level (Note 1) HBM CDM	 2 1		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Using EIA/JESD22A114B (Human Body Model) and EIA/JESD22C101−A (Charge Device Model).

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Type	Max	Unit
Input Voltage	1.8		5.5	V
Output Voltage	V_{IN}		30	V
Operating Ambient Temperature	−40	25	85	°C
Output Capacitance Rated at the Required Output (Note 2) for Maximum Load Current	0.47			μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. This load capacitance value is required for the loop stability. Tolerance, temperature variation, and voltage dependency of the capacitance must be considered. Typically a 1 μF ceramic capacitor is required to achieve specified value at V_{OUT} = 30 V.

Table 4. ELECTRICAL CHARACTERISTICS

Unless otherwise noted, V_{IN} = 3.6 V, V_{OUT} = 20 V, I_{LED} = 20 mA, T_A = −40°C to 85°C, Typical values are at T_A = 25°C, Test Circuit, Figure 3.

Parameter	Conditions	Min	Type	Max	Unit
Feedback Voltage	FAN5333A FAN5333B	99 299	110 315	121 331	mV
Switch Current Limit	V_{IN} = 3.2 V	1.1	1.5		A
Load Current Capability	$V_{OUT} \le$ 20 V, V_{IN} = 3.2 V	65			mA
Switch On−resistance	V_{IN} = 5 V V_{IN} = 3.6 V		0.6 0.7		Ω
Quiescent Current	$V_{\overline{SHDN}}$ = 3.6 V, No Switching		0.6		mA
OFF Mode Current	$V_{\overline{SHDN}}$ = 0 V		0.1	3	μA
Shutdown Threshold	Device ON Device OFF	1.5		 0.5	V
Shutdown Pin Bias Current	$V_{\overline{SHDN}}$ = 0 V or $V_{\overline{SHDN}}$ = 5.5 V		1	300	nA
Feedback Pin Bias Current			1	300	nA
Feedback Voltage Line Regulation	2.7 V < V_{IN} < 5.5 V, $V_{OUT} \le$ 20 V		0.3		%
Switching Frequency		1.2	1.5	1.8	MHz
Maximum Duty Cycle		87	93		%
Switch Leakage Current	No Switching, V_{IN} = 5.5 V			1	μA
OVP			15		%
Thermal Shutdown Temperature			150		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TEST CIRCUIT

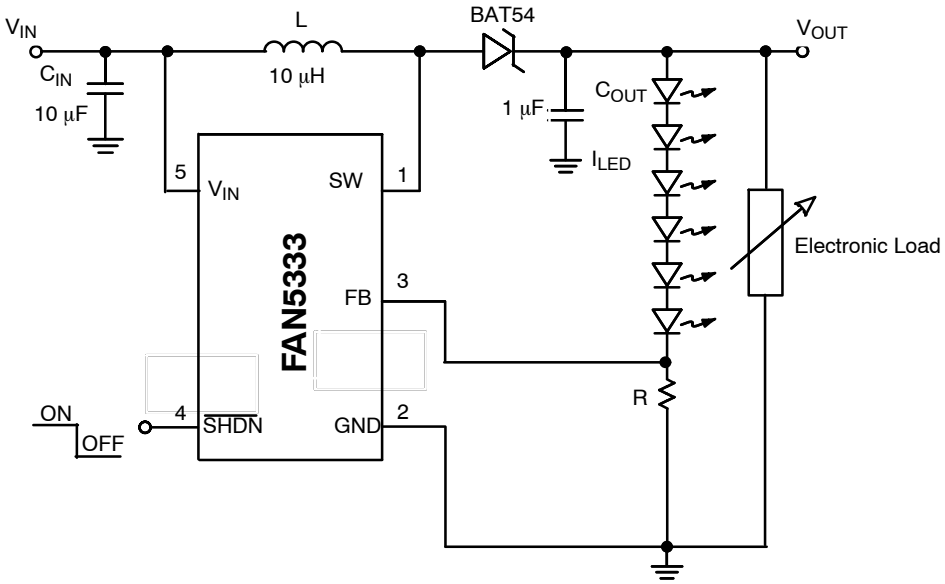


Figure 3. Test Circuit

TYPICAL CHARACTERISTICS

T_A = 25°C, C_{IN} = 4.7 μF, C_{OUT} = 0.47 μF, L = 10 μH, unless otherwise noted.

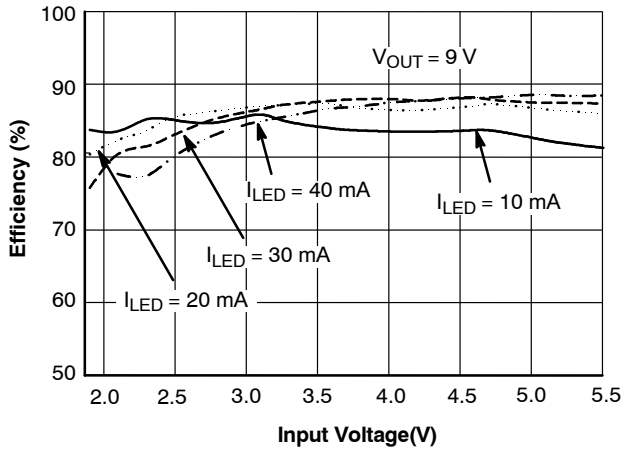


Figure 4. Efficiency vs. Input Voltage

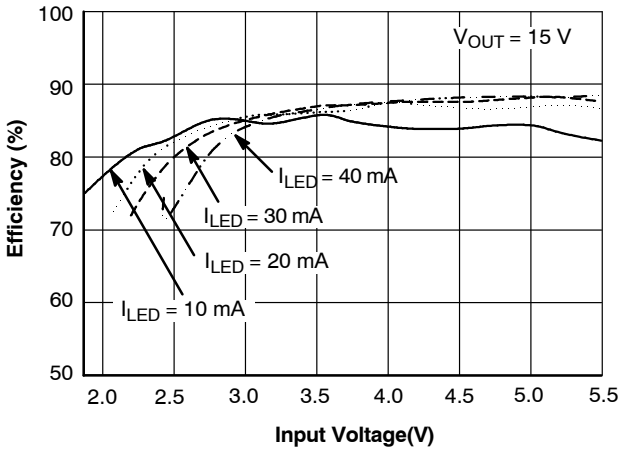


Figure 5. Efficiency vs. Input Voltage

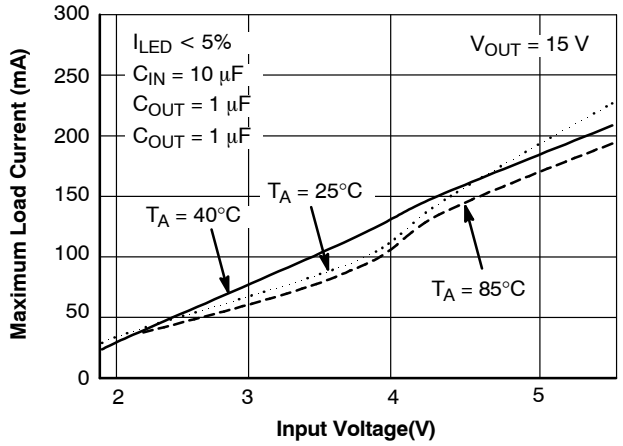


Figure 6. Maximum Load Current vs. Input Voltage

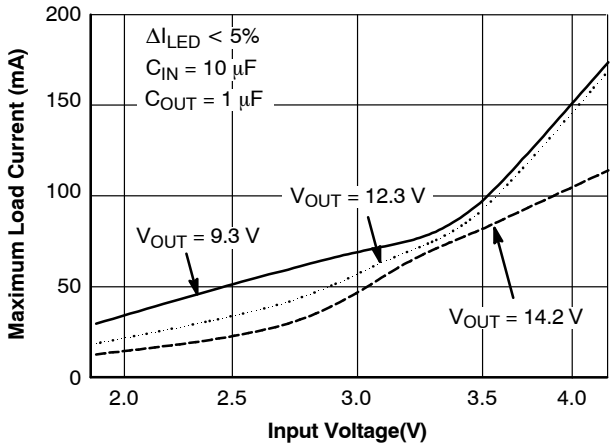


Figure 7. Maximum Load Current vs. Input Voltage

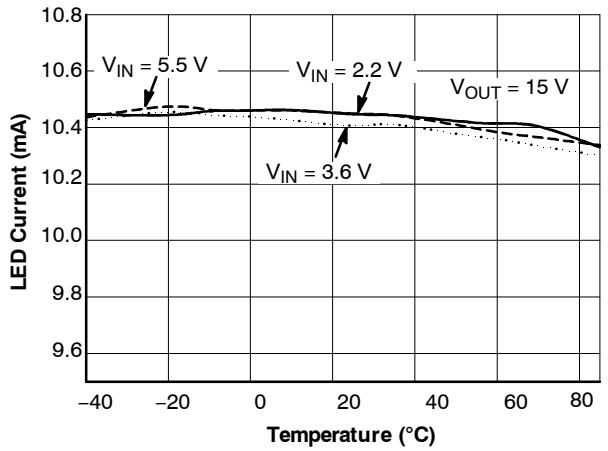


Figure 8. LED Current vs Temperature

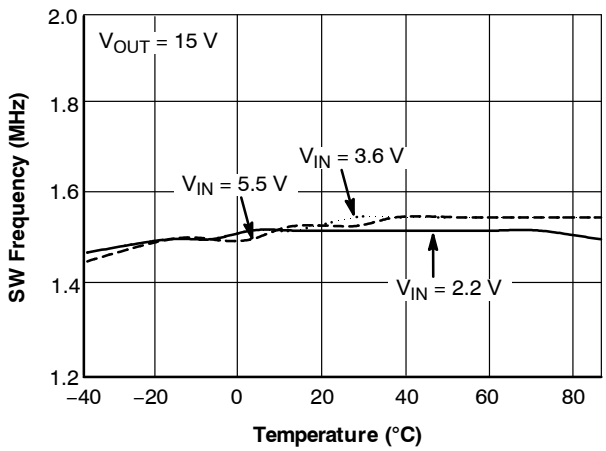


Figure 9. SW Frequency vs Temperature

TYPICAL CHARACTERISTICS (Continued)

T_A = 25°C, C_{IN} = 4.7 μF, C_{OUT} = 0.47 μF, L = 10 μH, unless otherwise noted.

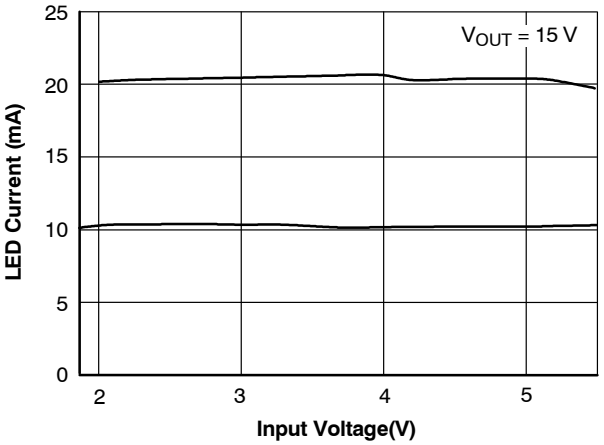


Figure 10. Load Current vs. Input Voltage

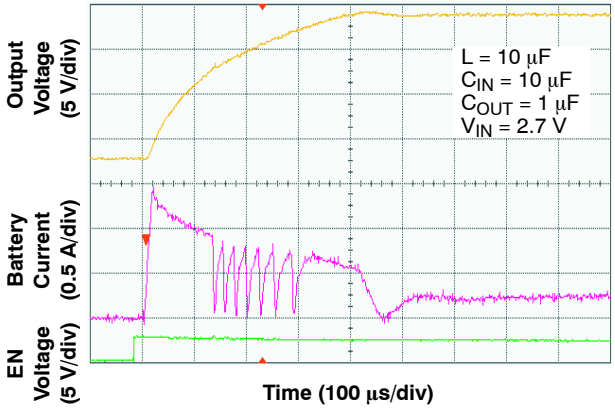


Figure 11. Start−Up Response

BLOCK DIAGRAM

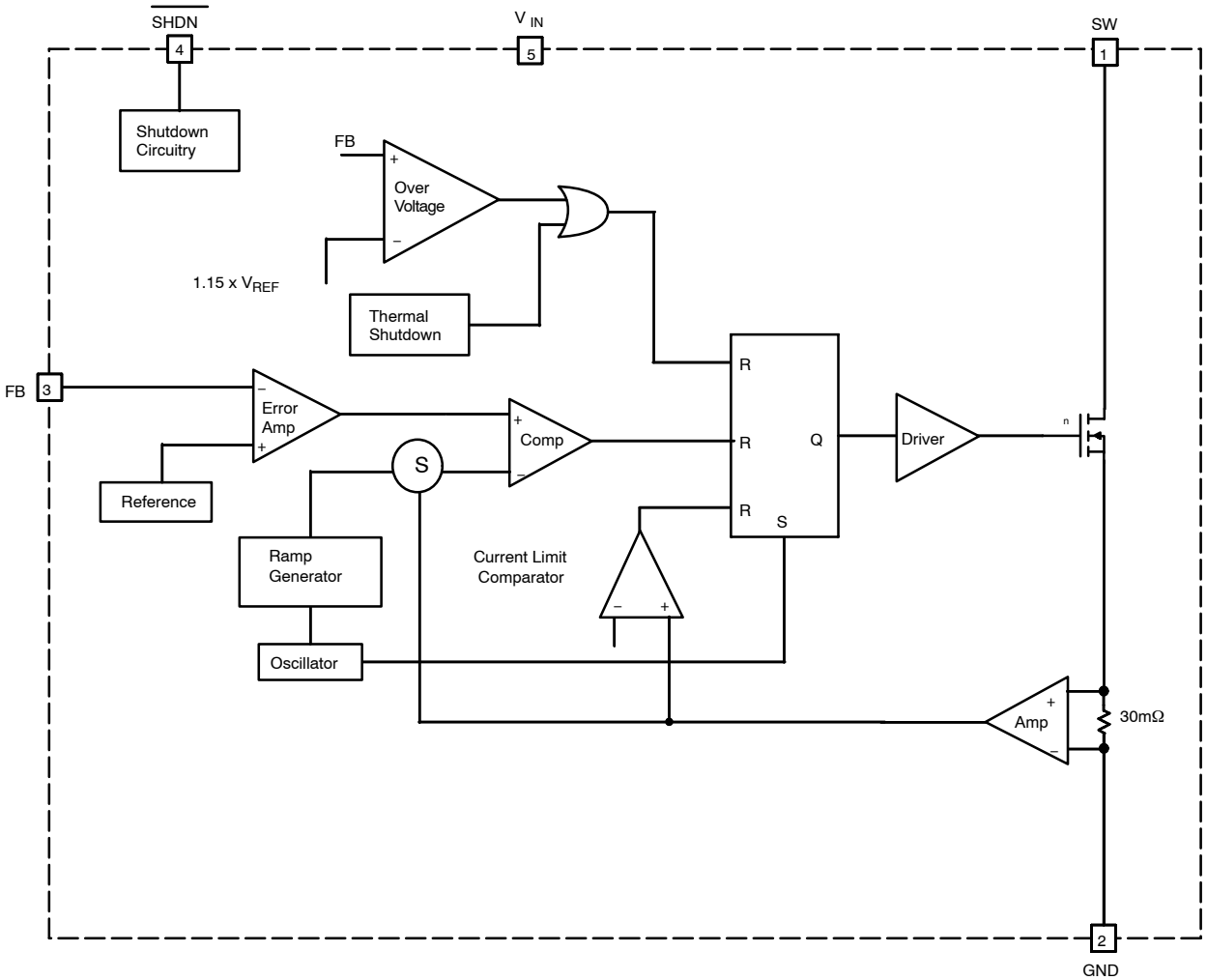


Figure 12. Block Diagram

CIRCUIT DESCRIPTION

The FAN5333A/FAN5333B is a pulse−width modulated (PWM) current−mode boost converter. The FAN5333A/ FAN5333B improves the performance of battery powered equipment by significantly minimizing the spectral distribution of noise at the input caused by the switching action of the regulator. In order to facilitate effective noise filtering, the switching frequency was chosen to be high, 1.5 MHz. The device architecture is that of a current mode controller with an internal sense resistor connected in series with the N−channel switch. The voltage at the feedback pin tracks the output voltage at the cathode of the external Schottky diode (shown in the test circuit). The error amplifier amplifies the difference between the feedback voltage and the internal band− gap reference. The amplified error voltage serves as a reference voltage to the PWM comparator. The inverting input of the PWM comparator consists of the sum of two components: the amplified control signal received from the 30 mΩ current sense resistor and the ramp generator voltage derived from the oscillator. The oscillator sets the latch, and the latch turns on the FET switch. Under normal operating conditions, the PWM comparator resets the latch and turns off the FET, thus terminating the pulse. Since the comparator input contains information about the output voltage and the control loop is arranged to form a negative feedback loop, the value of the peak inductor current will be adjusted to maintain regulation.

Every time the latch is reset, the FET is turned off and the current flow through the switch is terminated. The latch can be reset by other events as well. Over−current condition is monitored by the current limit comparator which resets the latch and turns off the switch instantaneously within each clock cycle.

Over−Voltage Protection

The voltage on the feedback pin is sensed by an OVP Comparator. When the feedback voltage is 15% higher than the nominal voltage, the OVP Comparator stops switching of the power transistor, thus preventing the output voltage from going higher.

OPEN−CIRCUIT PROTECTION

As in any current regulator, if the feedback loop is open, the output voltage increases until it is limited by some additional external circuitry. In the particular case of the FAN5333, the output voltage is limited by the switching transistor breakdown at around 45 V, typically (assuming that C_{OUT} and the Schottky diode rating voltage are higher). Since at such high output voltage the output current is inherently limited by the discontinuous conduction mode, in most cases, the switching transistor enters non−destructive breakdown and the IC survives.

However, to ensure 100% protection for LED disconnection, we recommend limiting V_{OUT} with an external Zener diode or stopping the boost switching with an external voltage supervisory circuit.

APPLICATIONS INFORMATION

Setting the Output Current

The internal reference (V_{REF}) is 110 mV (Typical) for FAN5333A and 315 mV (Typical) for FAN5333B. The output current is set by a resistor divider R connected between FB pin and ground. The output current is given by:

$$I_{LED} = \frac{V_{FB}}{R} \qquad \text{(eq. 1)}$$

Inductor Selection

The inductor parameters directly related to device performances are saturation current and dc resistance. The FAN5333A/ FAN5333B operates with a typical inductor value of 10 μH. The lower the dc resistance, the higher the efficiency. Usually a trade−off between inductor size, cost and overall efficiency is needed to make the optimum choice.

The inductor saturation current should be rated around 1 A, in an application having the LED current near the maximum current as indicated in “Typical Performance Characteristics”. The peak inductor current is limited to 1.5 A by the current sense loop. This limit is reached only during the start−up and with heavy load condition; when this event occurs the converter can shift over in discontinuous conduction mode due to the automatic turn−off of the switching transistor, resulting in higher ripple and reduced efficiency

Some recommended inductors are suggested in the table below:

Table 5. RECOMMENDED INDUCTORS

Inductor Value	Vendor	Part Number	Comment
10 μH	TDK	SLF6025&−100M1R0	
10 μH	MURATA	LQH66SN100M01C	Highest Efficiency
10 μH	COOPER	SD414−100	Small Size

Capacitors Selection

For best performance, low ESR input and output capacitors are required. Ceramic capacitors of C_{IN} = 10 μF and C_{OUT} = 1 μF placed as close to the IC pins, are required for the maximum load (65 mA). For the lighter load (≤20 mA) the capacitances may be reduced to C_{IN} = 4.7 μF and C_{OUT} = 0.47 μF or even to 0.1 μF, if higher ripple is acceptable. The output capacitor voltage rating should be according to the V_{OUT} setting. Some capacitors are suggested in the table below:

Table 6. RECOMMENDED CAPACITORS

Capacitor Value	Vendor	Part Number
0.47 μH	Panasonic	ECJ−3YB1E474K
1 μH	MURATA	GRM21BR61E105K
10 μH	MURATA	GRM21BR61A106K

Diode Selection

The external diode used for rectification is usually a Schottky diode. Its average forward current and reverse voltage maximum ratings should exceed the load current and the voltage at the output of the converter respectively. A barrier Schottky diode such as BAT54 is preferred, due to its lower reverse current over the temperature range. Care should be taken to avoid any short circuit of V_{OUT} to GND, even with the IC disabled, since the diode can be instantly damaged by the excessive current

BRIGHTNESS CONTROL

1. Dimming Using PWM Logic Signal

A PWM signal applied to $\overline{SHDN}$ (See Figure 14) can control the LED's brightness in direct dependence with the duty cycle. The maximum frequency should not exceed 1kHz to ensure a linear dependence of the LED's average current. The amplitude of the PWM signal should be suitable to turn the FAN5333 ON and OFF. Alternatively, a PWM logic signal can be used to switch a FET ON/OFF to change the resistance that sets the LED's current (See Figure 14). Adjusting the duty cycle from 0% to 100% results in varying the LED's current between I_{MIN} and I_{MAX}.

Where:

$$I_{MIN} = \frac{V_{FB}}{R_{MIN}} \text{ and } I_{MAX} = \frac{V_{FB}}{R_{MIN} \parallel R_{SET}} \quad \text{(eq. 2)}$$

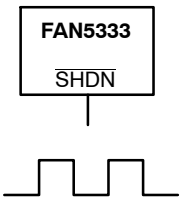


Figure 13. Dimming Using a PWM Signal

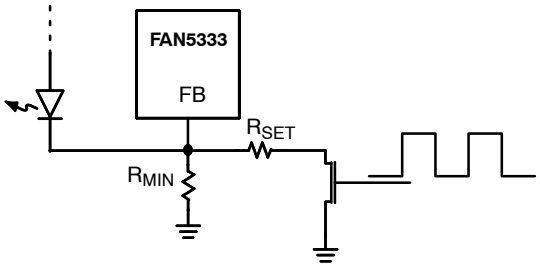


Figure 14. Dimming Using a PWM Logic Signal

2. Dimming Using DC Voltage

An external adjustable DC voltage (See Figure 15) between 0 V to 2 V can control the LED's current from 15 mA to 0 mA, respectively.

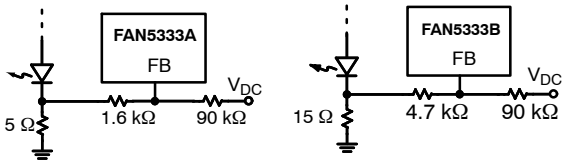


Figure 15. Dimming Using DC Voltage

3. Dimming Using Filtered PWM Signal

This method allows the use of a greater than 1 kHz PWM frequency signal with minimum impact on the battery ripple. The filtered PWM signal (See Figure 16) acts as an adjustable DC voltage as long as its frequency is significantly higher than the corner frequency of the RC low pass filter.

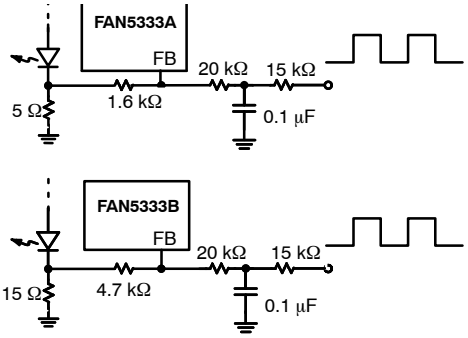


Figure 16. Dimming Using Filtered PWM Signal

THERMAL SHUTDOWN

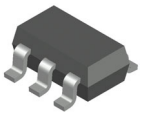
When the die temperature exceeds 150°C, a reset occurs and will remain in effect until the die cools to 130°C, at that time the circuit will be allowed to restart.

PCB LAYOUT RECOMMENDATIONS

The inherently high peak currents and switching frequency of power supplies require careful PCB layout design. Therefore, use wide traces for high current paths and place the input capacitor, the inductor, and the output capacitor as close as possible to the integrated circuit terminals. The FB pin connection should be routed away from the inductor proximity to prevent RF coupling. A PCB with at least one ground plane connected to pin 2 of the IC is recommended. This ground plane acts as an electromagnetic shield to reduce EMI and parasitic coupling between components.

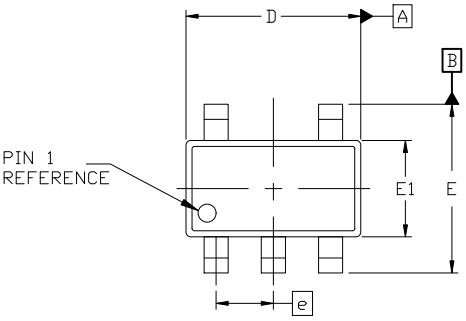
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

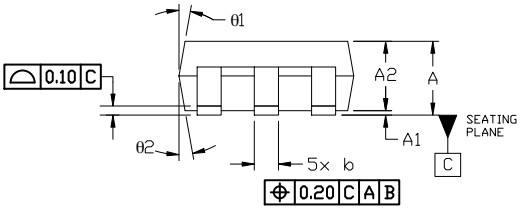


SOT−23, 5 Lead
CASE 527AH
ISSUE A

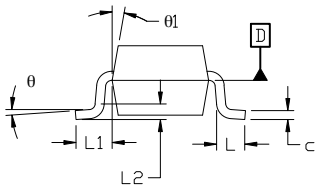
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TOP VIEW



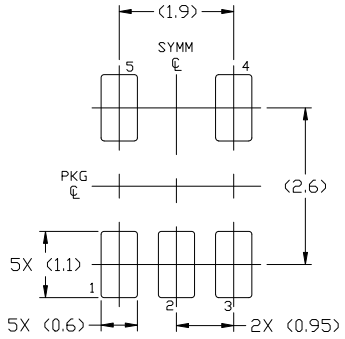
SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 19894
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM D.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL NOT BE LESS THAN 0.07mm.

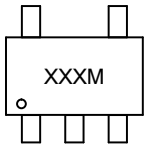
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	—	1.45
A1	0.00	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ	0°	4°	8°
θ1	0°	10°	15°
θ2	0°	10°	15°



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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