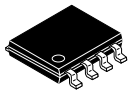
High- and Low-Side Gate Driver

FAN7842



SOIC8
(8−SOP)
CASE 751EG

Description

The FAN7842, a monolithic high and low side gate drive IC, which can drive MOSFETs and IGBTs that operate up to +200 V.

onsemi's high−voltage process and common−mode noise canceling technique provide stable operation of the high−side driver under high−dv/dt noise circumstances. An advanced level−shift circuit allows high−side gate driver operation up to V_S = −9.8 V (typical) for V_{BS} = 15 V. The input logic level is compatible with standard TTL−series logic gates.

The UVLO circuits for both channels prevent malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Output driver current (source/sink) is typically 350 mA/650 mA, respectively.

Features

- Floating Channels Designed for Bootstrap Operation to +200 V
- Typically 350 mA/650 mA Sourcing/Sinking Current Driving Capability for Both Channels
- Common−Mode dv/dt Noise Canceling Circuit
- Extended Allowable Negative V_S Swing to −9.8 V for Signal Propagation at V_{CC} = V_{BS} = 15 V
- V_{CC} & V_{BS} Supply Range from 10 V to 20 V
- UVLO Functions for Both Channels
- TTL Compatible Input Logic Threshold Levels
- Matched Propagation Delay Below 50 ns
- Output In−phase with Input Signal
- This Device is Pb−Free, Halide Free and is RoHS Compliant

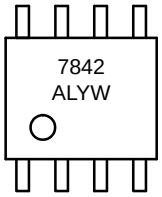
Applications

- Battery Based Motor Applications (E−bike, Power Tool)
- Telecom DC−DC Converter

Related Resources

- AN−6076 − Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC
- AN−9052 − Design Guide for Selection of Bootstrap Components
- AN−8102 − Recommendations to Avoid Short Pulse Width Issues in HVIC Gate Driver Applications

MARKING DIAGRAM



7842 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

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TYPICAL APPLICATION CIRCUIT

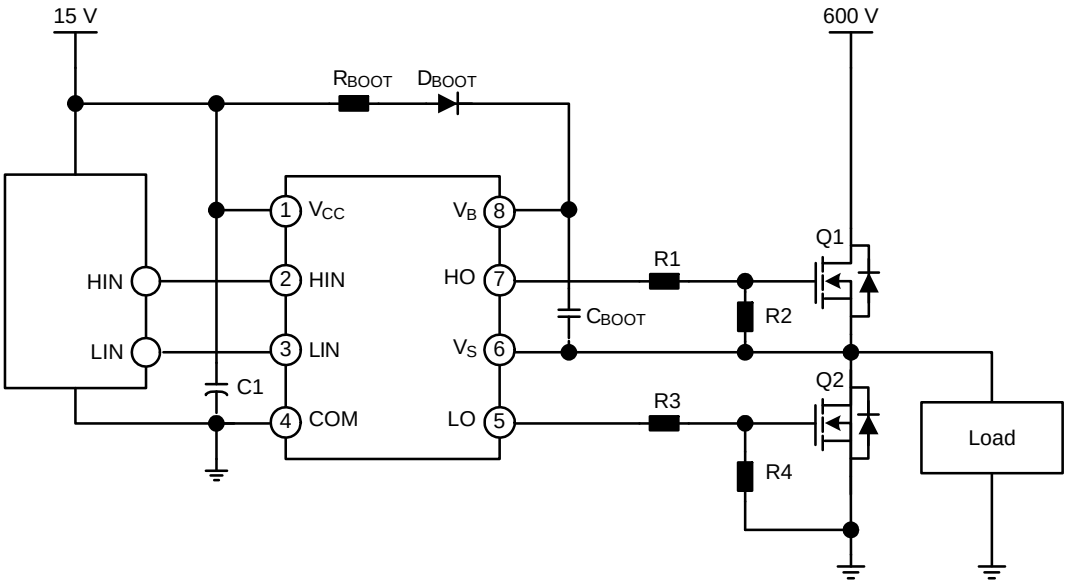


Figure 1. Application Circuit for Half−Bridge

INTERNAL BLOCK DIAGRAM

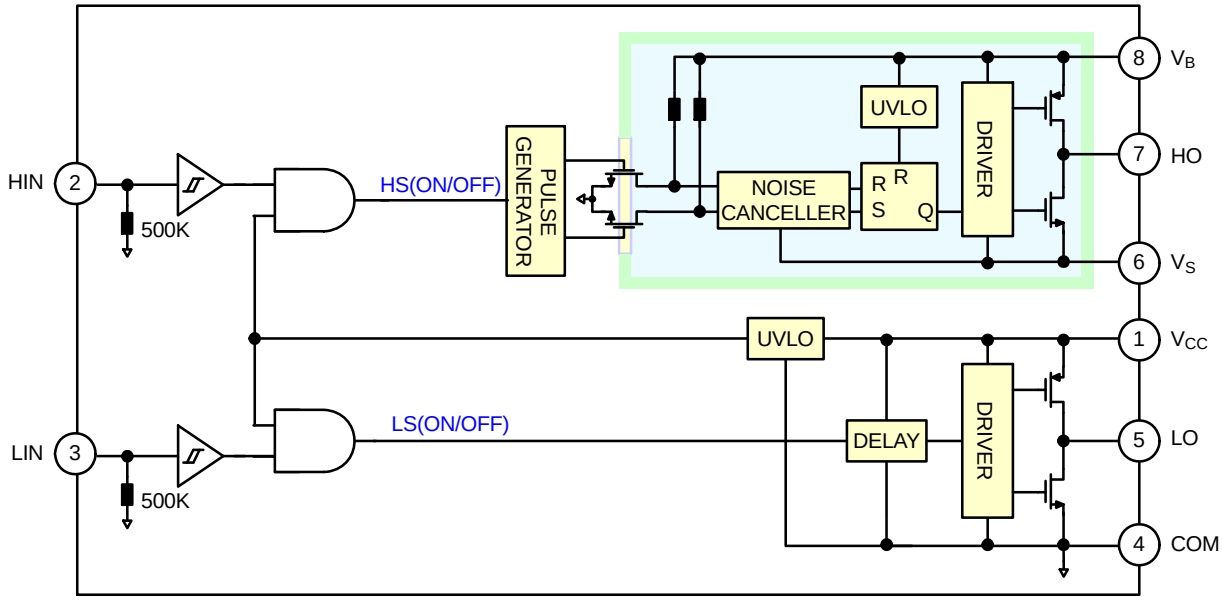


Figure 2. Functional Block Diagram

PIN ASSIGNMENTS

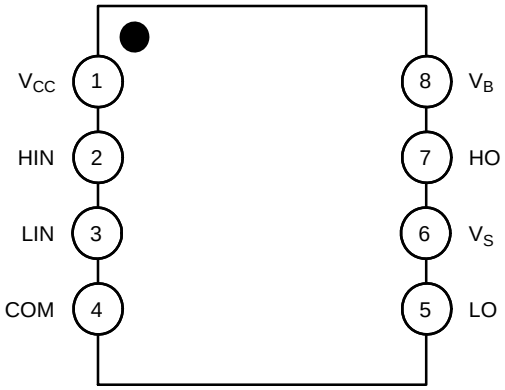


Figure 3. Pin Configuration (Top View)

PIN DEFINITIONS

Name	Description
V_{CC}	Low−Side Supply Voltage
HIN	Logic Input for High−Side Gate Driver Output
LIN	Logic Input for Low−Side Gate Driver Output
COM	Logic Ground and Low−Side Driver Return
LO	Low−Side Driver Output
V_S	High−Voltage Floating Supply Return
HO	High−Side Driver Output
V_B	High−Side Floating Supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_S	High−side Offset Voltage	V_B − 25	V_B + 0.3	V
V_B	High−side Floating Supply Voltage	−0.3	225	
V_{HO}	High−side Floating Output Voltage HO	V_S − 0.3	V_B + 0.3	
V_{CC}	Low−side and Logic Fixed Supply Voltage	−0.3	25	
V_{LO}	Low−side Output Voltage LO	−0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN)	−0.3	V_{CC} + 0.3	
COM	Logic Ground	V_{CC} − 25	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Voltage Slew Rate	−	50	V/ns
P_D (Note 1) (Note 2) (Note 3)	Power Dissipation	−	0.625	W
θ_{JA}	Thermal Resistance, Junction−to−ambient	−	200	°C/W
T_J	Junction Temperature	−	150	°C
T_{STG}	Storage Temperature	−	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).
2. Refer to the following standards:
   JESD51−2: Integral circuits thermal test method environmental conditions − natural convection
   JESD51−3: Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed P_D under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_B	High−side Floating Supply Voltage	V_S + 10	V_S + 20	V
V_S	High−side Floating Supply Offset Voltage	6 − V_{CC}	200	
V_{HO}	High−side (HO) Output Voltage	V_S	V_B	
V_{LO}	Low−side (LO) Output Voltage	COM	V_{CC}	
V_{IN}	Logic Input Voltage (HIN, LIN)	COM	V_{CC}	
V_{CC}	Low−side Supply Voltage	10	20	
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{CC}, V_{BS}) = 15.0 V, T_A = 25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} Supply Under−voltage Positive Going Threshold		8.2	9.2	10.0	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} Supply Under−voltage Negative Going Threshold		7.6	8.7	9.6	
V_{CCUVH} V_{BSUVH}	V_{CC} Supply Under−voltage Lockout Hysteresis		−	0.6	−	
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 200 V	−	−	50	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{IN} = 0 V or 5 V	−	45	120	
I_{QCC}	Quiescent V_{CC} Supply Current	V_{IN} = 0 V or 5 V	−	70	180	
I_{PBS}	Operating V_{BS} Supply Current	f_{IN} = 20 kHz, rms value	−	−	600	μA
I_{PCC}	Operating V_{CC} Supply Current	f_{IN} = 20 kHz, rms value	−	−	600	
V_{IH}	Logic “1” Input Voltage		2.9	−	−	V
V_{IL}	Logic “0” Input Voltage		−	−	0.8	
V_{OH}	High−level Output Voltage, V_{BIAS}−V_O	I_O = 20 mA	−	−	1.0	
V_{OL}	Low−level Output Voltage, V_O		−	−	0.6	
I_{IN+}	Logic “1” Input Bias Current	V_{IN} = 5 V	−	10	20	μA
I_{IN-}	Logic “0” Input Bias Current	V_{IN} = 0 V	−	1.0	2.0	
I_{O+}	Output High Short−circuit Pulsed Current	V_O = 0 V, V_{IN} = 5 V with PW < 10 μs	250	350	−	mA
I_{O-}	Output Low Short−circuit Pulsed Current	V_O = 15 V, V_{IN} = 0 V with PW < 10 μs	500	650	−	
V_S	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO		−	−9.8	−7.0	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC ELECTRICAL CHARACTERISTICS (V_{BIAS} (V_{CC}, V_{BS}) = 15.0 V, V_S = COM, C_L = 1000 pF and, T_A = 25°C, unless otherwise specified.)

Symbol	Characteristics	Test Condition	Min	Typ	Max	Unit
t_{on}	Turn−on Propagation Delay	V_S = 0 V	100	170	300	ns
t_{off}	Turn−off Propagation Delay	V_S = 0 V or 200 V (Note 4)	100	200	300	ns
t_r	Turn−on Rise Time		20	60	140	ns
t_f	Turn−off Fall Time		−	30	80	ns
MT	Delay Matching, HS & LS Turn−on/off		−	−	50	ns

4. This parameter guaranteed by design.

TYPICAL CHARACTERISTICS

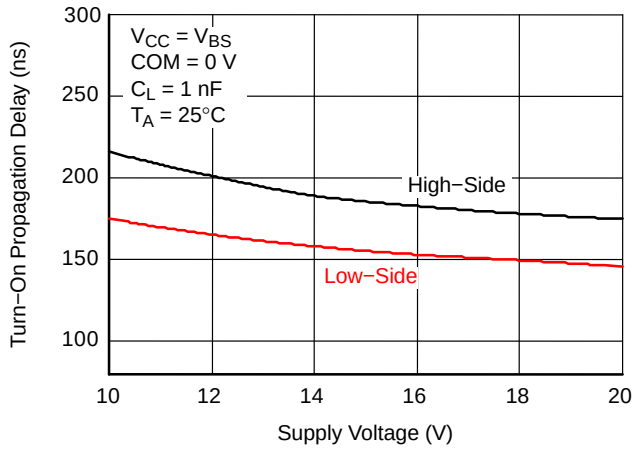


Figure 4. Turn−On Propagation Delay vs. Supply Voltage

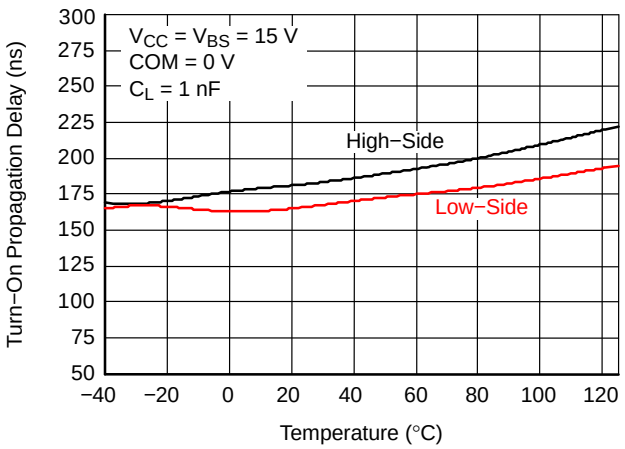


Figure 5. Turn−On Propagation Delay vs. Temperature

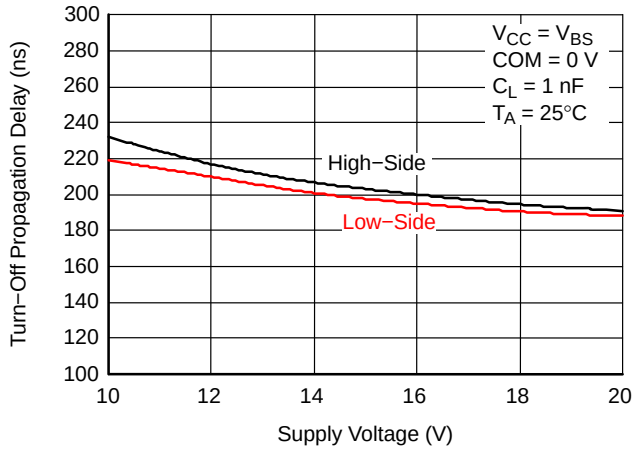


Figure 6. Turn−Off Propagation Delay vs. Supply Voltage

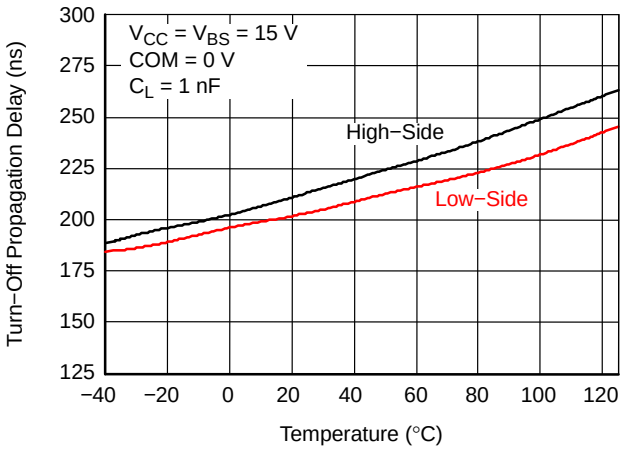


Figure 7. Turn−Off Propagation Delay vs. Temperature

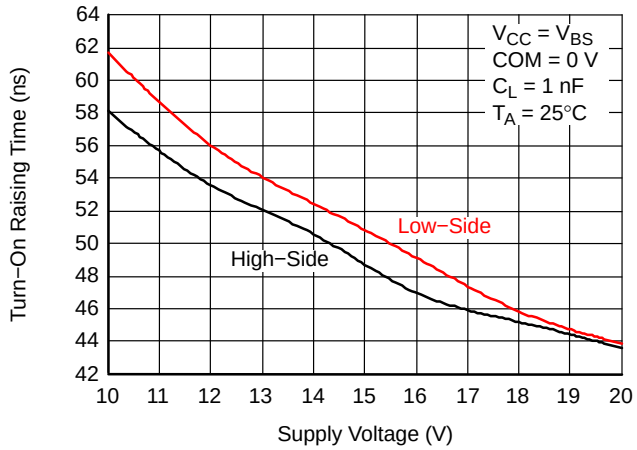


Figure 8. Turn−On Rising Time vs. Supply Voltage

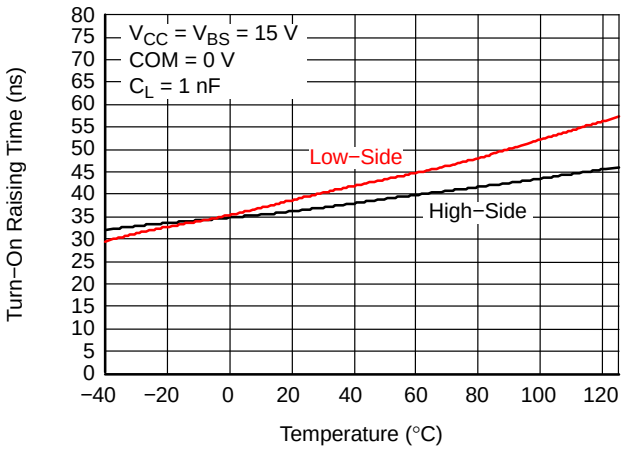


Figure 9. Turn−On Rising Time vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

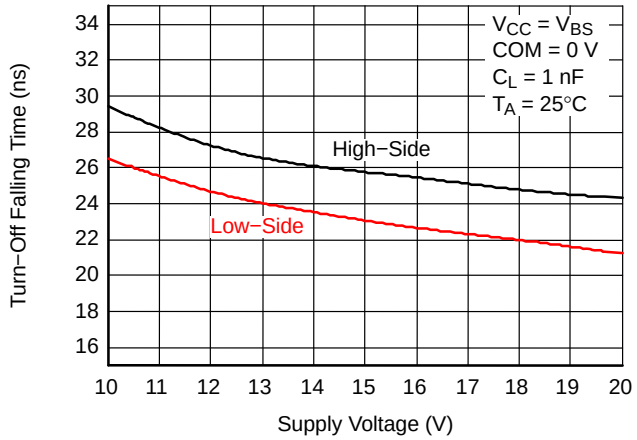


Figure 10. Turn−Off Falling Time vs. Supply Voltage

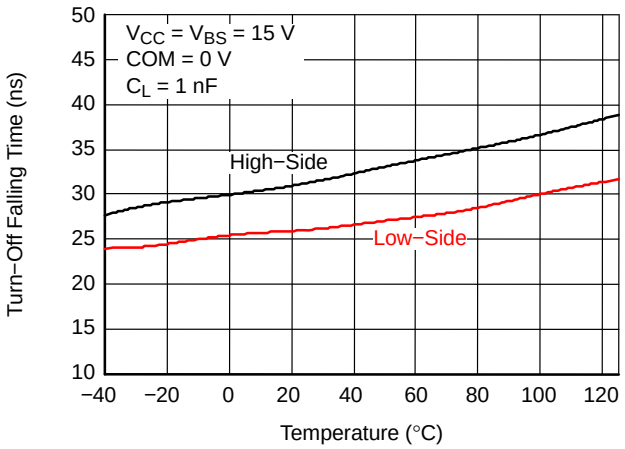


Figure 11. Turn−Off Falling Time vs. Temperature

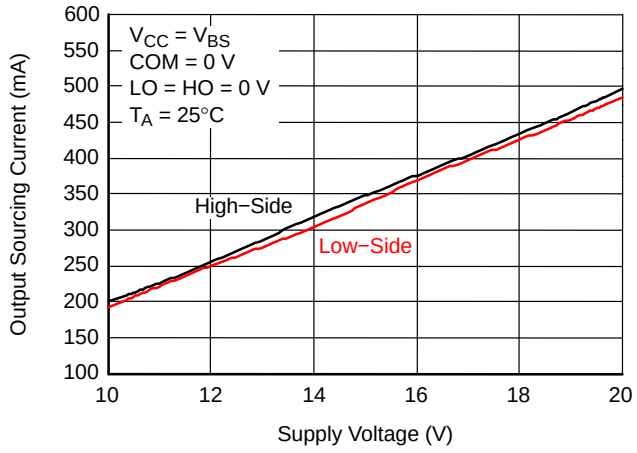


Figure 12. Output Sourcing Current vs. Supply Voltage

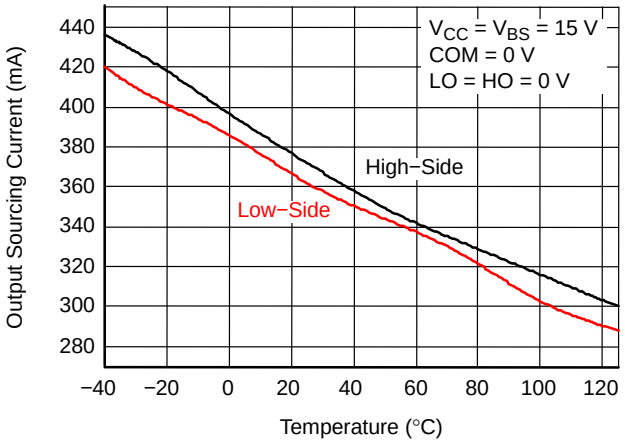


Figure 13. Output Sourcing Current vs. Temperature

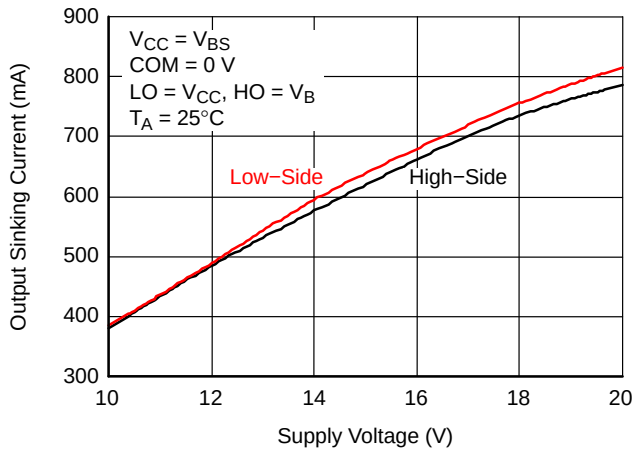


Figure 14. Output Sinking Current vs. Supply Voltage

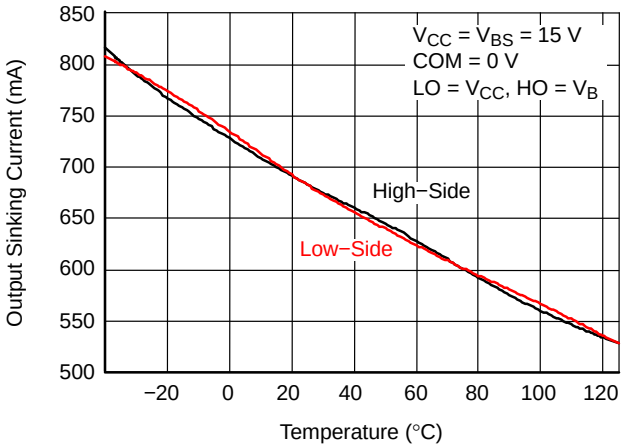


Figure 15. Output Sinking Current vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

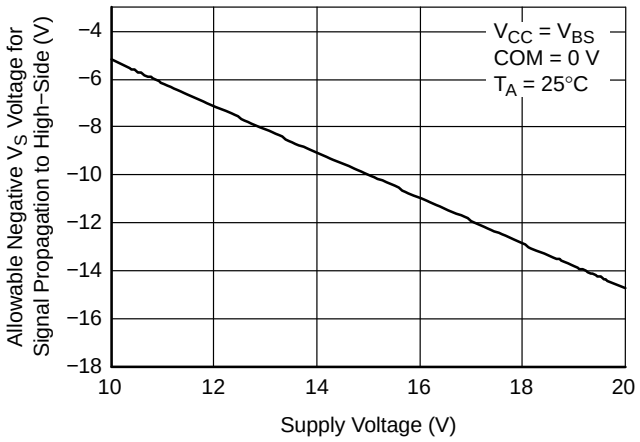


Figure 16. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Supply Voltage

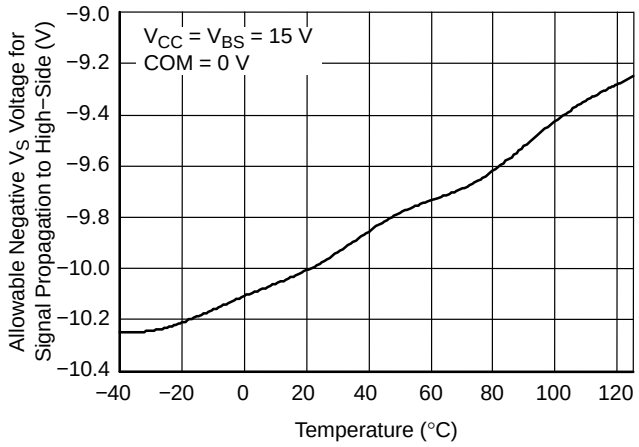


Figure 17. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temperature

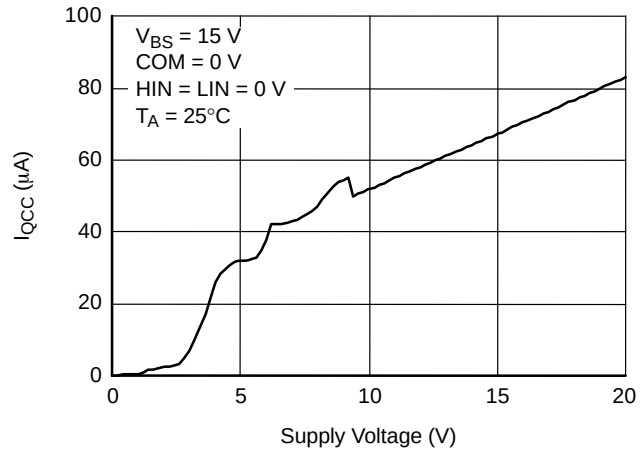


Figure 18. I_{QCC} vs. Supply Voltage

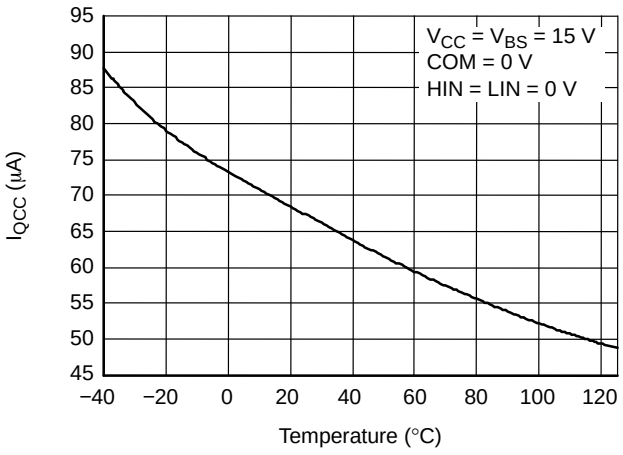


Figure 19. I_{QCC} vs. Temperature

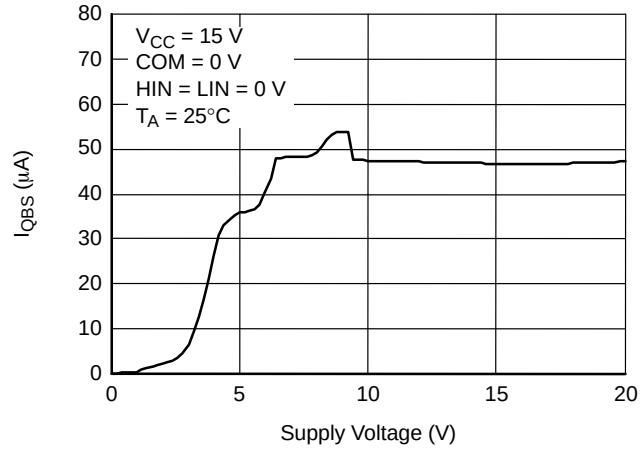


Figure 20. I_{QBS} vs. Supply Voltage

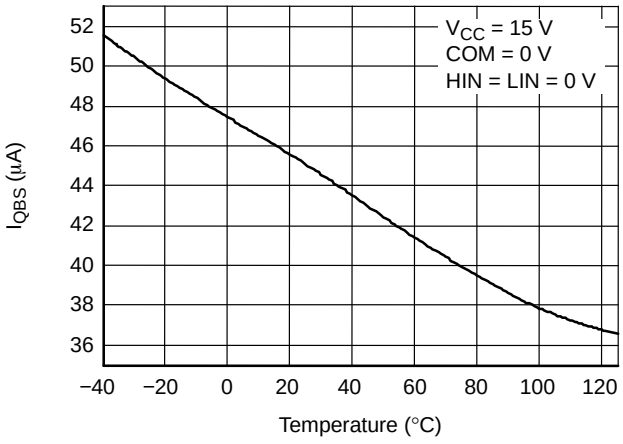


Figure 21. I_{QBS} vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

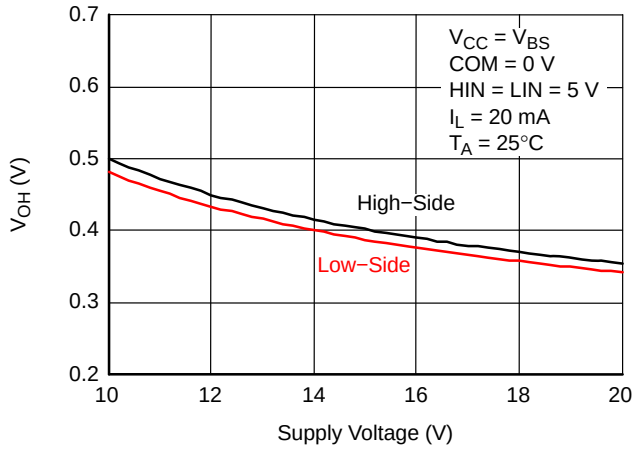


Figure 22. High−Level Output Voltage vs. Supply Voltage

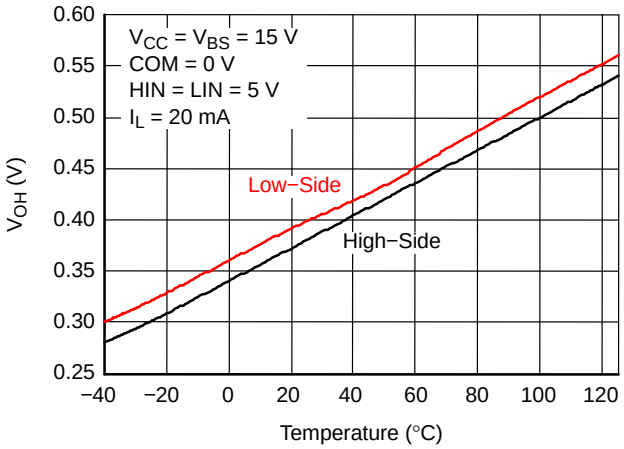


Figure 23. High−Level Output Voltage vs. Temperature

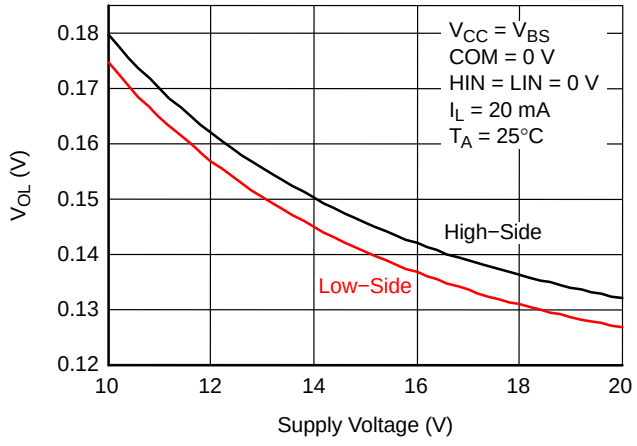


Figure 24. Low−Level Output Voltage vs. Supply Voltage

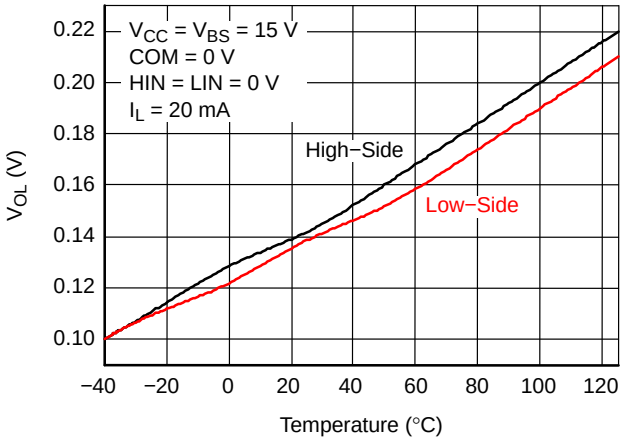


Figure 25. Low−Level Output Voltage vs. Temperature

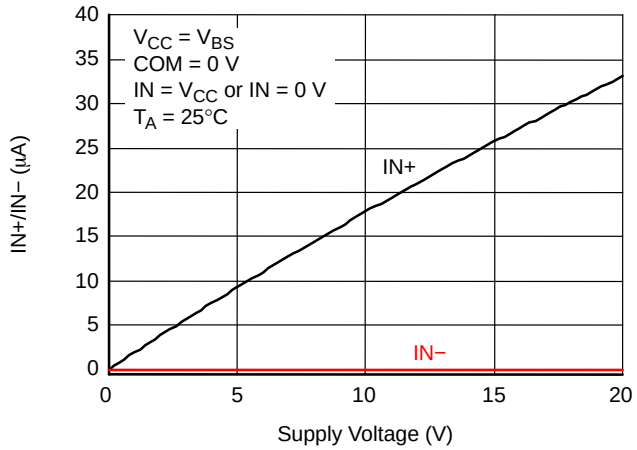


Figure 26. Input Bias Current vs. Supply Voltage

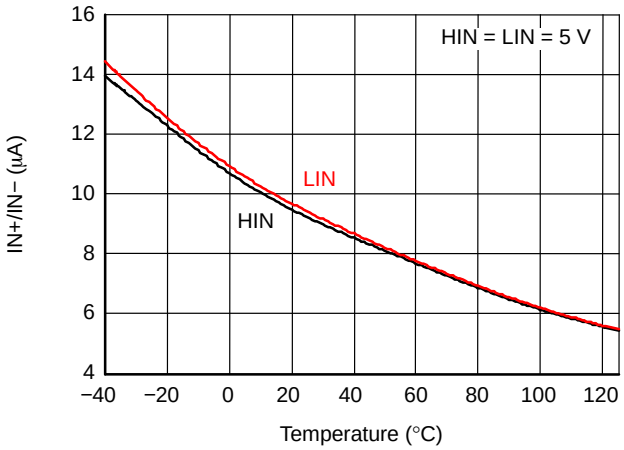


Figure 27. Input Bias Current vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

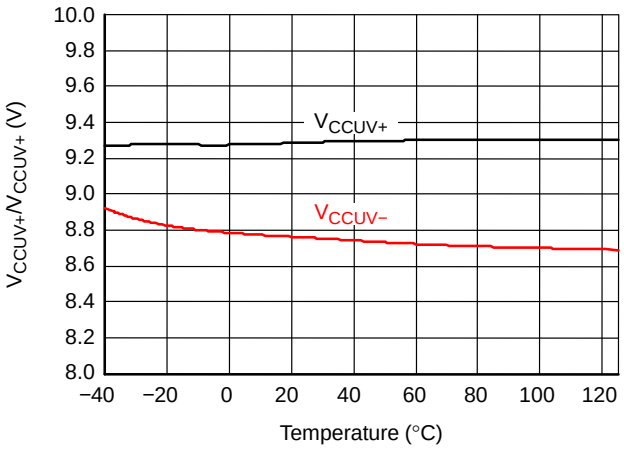


Figure 28. V_{CC} UVLO Threshold Voltage vs. Temperature

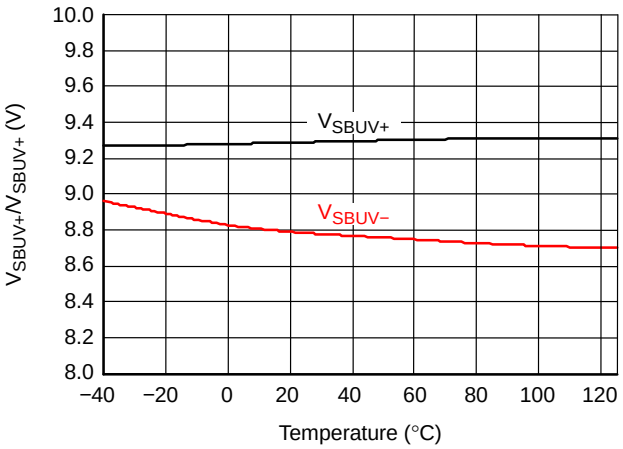


Figure 29. V_{BS} UVLO Threshold Voltage vs. Temperature

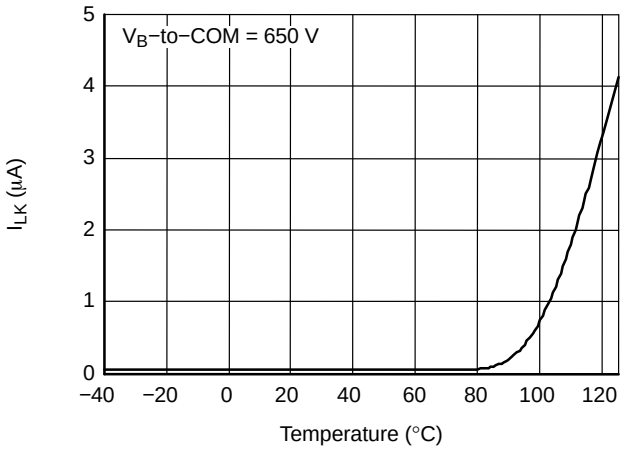


Figure 30. V_B to COM Leakage Current vs. Temperature

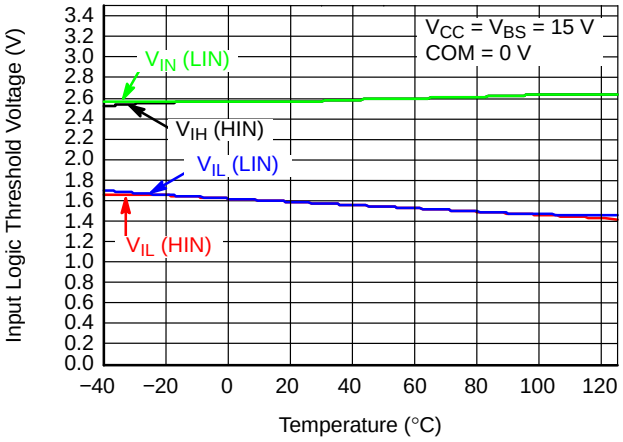


Figure 31. Input Logic Threshold Voltage vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

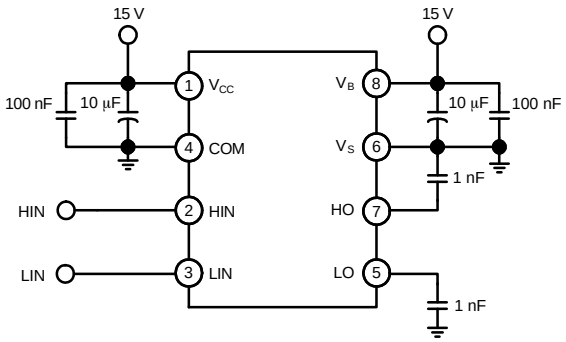


Figure 32. Switching Time Test Circuit

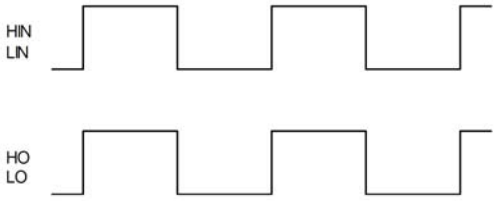


Figure 33. Input / Output Timing Diagram

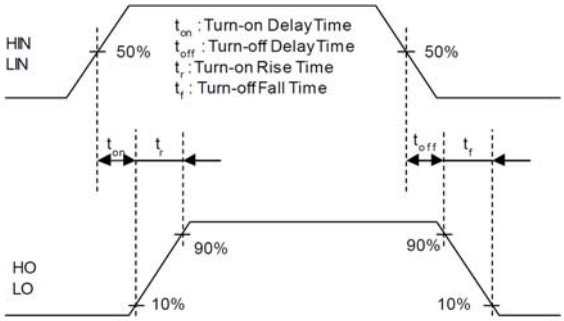


Figure 34. Switching Time Waveform Definition

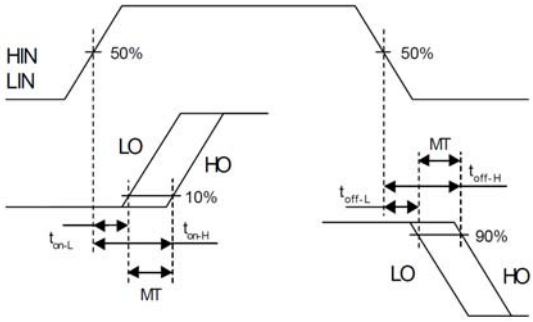


Figure 35. Delay Matching Waveform Definition

ORDERING INFORMATION

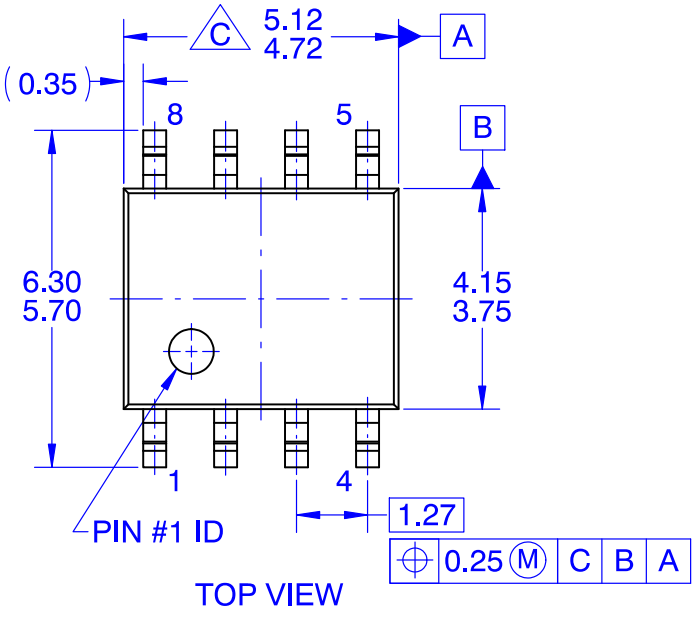
Part Number	Package	Operating Temperature Range	Shipping†
FAN7842MX (Note 5)	SOIC8 (8−SOP) (Pb−Free, Halide Free)	−40°C~125°C	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

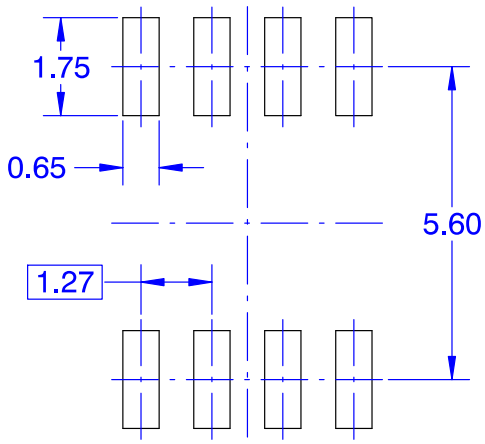
5. These devices passed wave soldering test by JESD22A−111.

SOIC8
CASE 751EG
ISSUE O

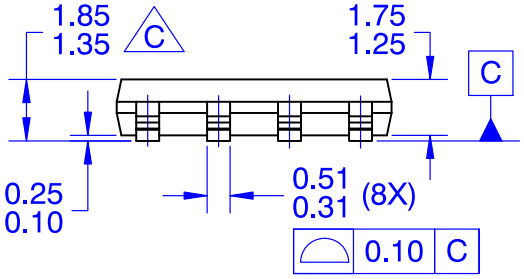
DATE 30 SEP 2016



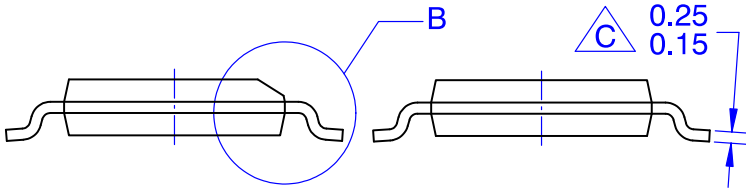
TOP VIEW



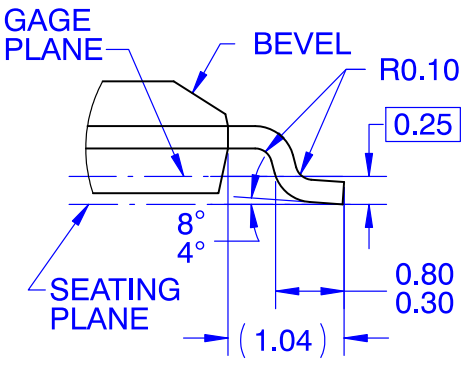
LAND PATTERN RECOMMENDATION



FRONT VIEW



SIDE VIEW



DETAIL "B"
SCALE 2:1

NOTES: UNLESS OTHERWISED SPECIFIED

A. THIS PACKAGE CONFORMS TO JEDEC MS–012 VARIATION A EXCEPT WHERE NOTED.
B. ALL DIMENSIONS ARE IN MILLIMETERS
C OUT OF JEDEC STANDARD VALUE
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
E. LAND PATTERN AS PER IPC SOIC127P600X175–8M

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DESCRIPTION:	**SOIC8**	**PAGE 1 OF 1**

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