

MOSFET - N-Channel Shielded Gate POWER trench® 80 V, 64 A, 6.8 mΩ

FDMC007N08LCDC

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 6.8 mΩ at V_{GS} = 10 V, I_D = 22 A
- Max $R_{DS(on)}$ = 11.1 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- 5 V Drive Capable
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous, T_C = 25°C (Note 5) Continuous, T_C = 100°C (Note 5) Continuous, T_A = 25°C (Note 1a) Pulsed (Note 4)	64 41 15 339	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	150	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	57 3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

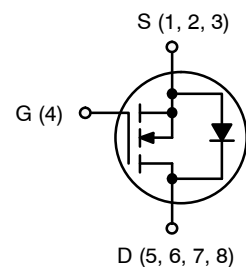
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



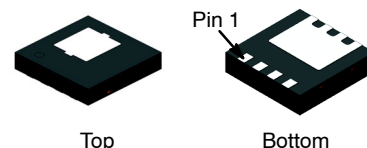
ON Semiconductor®

www.onsemi.com

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
80 V	6.8 mΩ @ 10 V 11.1 mΩ @ 4.5 V	22 A

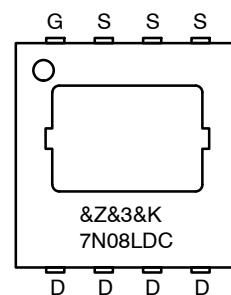


N-CHANNEL MOSFET



Dual Cool™ 33
(PQFN8)
CASE 483AY

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
7N08LDC = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	80			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		67		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 130\ \mu\text{A}$	1.0	1.5	2.5	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 130\ \mu\text{A}$, referenced to 25°C		-5.2		mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 22\ \text{A}$		5.1	6.8	m Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 18\ \text{A}$		7.3	11.1	
		$V_{GS} = 10\ \text{V}$, $I_D = 22\ \text{A}$, $T_J = 125^\circ\text{C}$		9.5	12.5	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 22\ \text{A}$		80		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		2195	3070	pF
C_{oss}	Output Capacitance			521	730	pF
C_{rss}	Reverse Transfer Capacitance			25	40	pF
R_g	Gate Resistance		0.1	0.5	0.9	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\ \text{V}$, $I_D = 22\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		11	21	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t_f	Fall Time			4	10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 22\ \text{A}$		31	44	nC
		$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$, $V_{DD} = 40\ \text{V}$, $I_D = 22\ \text{A}$		15	21	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 40\ \text{V}$, $I_D = 22\ \text{A}$		5		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = 40\ \text{V}$, $I_D = 22\ \text{A}$		4		nC
Q_{oss}	Output Charge	$V_{DD} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$		29		nC
Q_{sync}	Total Gate Charge Sync	$V_{DS} = 0\ \text{V}$, $I_D = 22\ \text{A}$		28		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.5\ \text{A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\ \text{V}$, $I_S = 22\ \text{A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 11\ \text{A}$, $di/dt = 300\ \text{A}/\mu\text{s}$		18	32	ns
Q_{rr}	Reverse Recovery Charge			24	38	nC

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
t_{rr}	Reverse Recovery Time	$I_F = 11\text{ A}$, $di/dt = 1000\text{ A}/\mu\text{s}$		15	26	ns
Q_{rr}	Reverse Recovery Charge			60	96	nC

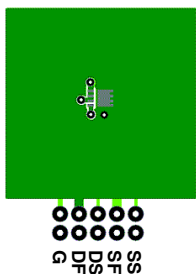
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	6.0	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Source)	2.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	29	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	19	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	23	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	30	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	79	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	16	$^\circ\text{C}/\text{W}$

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $42^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



- b) $105^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Still air, $20.9 \times 10.4 \times 12.7\text{ mm}$ Aluminum Heat Sink, 1 in^2 pad of 2 oz copper
 - Still air, $20.9 \times 10.4 \times 12.7\text{ mm}$ Aluminum Heat Sink, minimum pad of 2 oz copper
 - Still air, $45.2 \times 41.4 \times 11.7\text{ mm}$ Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper
 - Still air, $45.2 \times 41.4 \times 11.7\text{ mm}$ Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, 1 in^2 pad of 2 oz copper
 - 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, $20.9 \times 10.4 \times 12.7\text{ mm}$ Aluminum Heat Sink, 1 in^2 pad of 2 oz copper
 - 200FPM Airflow, $20.9 \times 10.4 \times 12.7\text{ mm}$ Aluminum Heat Sink, minimum pad of 2 oz copper
 - 200FPM Airflow, $45.2 \times 41.4 \times 11.7\text{ mm}$ Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper
 - 200FPM Airflow, $45.2 \times 41.4 \times 11.7\text{ mm}$ Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.
 - E_{AS} of 150 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 10\text{ A}$, $V_{DD} = 80\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 32\text{ A}$.
 - Pulsed I_d please refer to Figure 11 SOA graph for more details.
 - Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

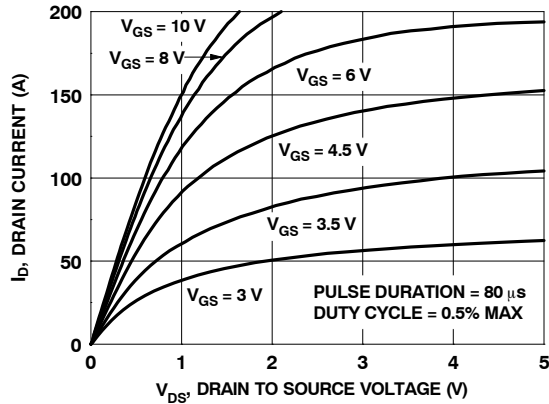
(T_J = 25°C unless otherwise noted)

Figure 1. On Region Characteristics

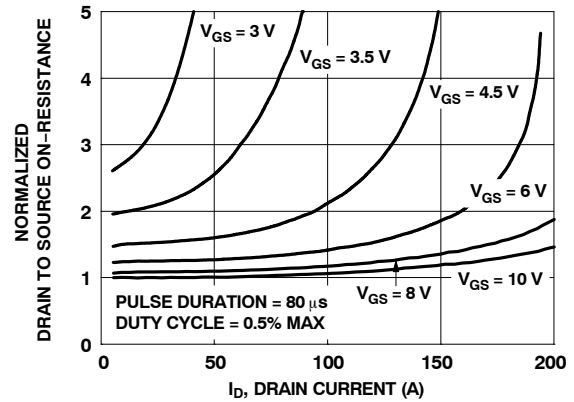


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

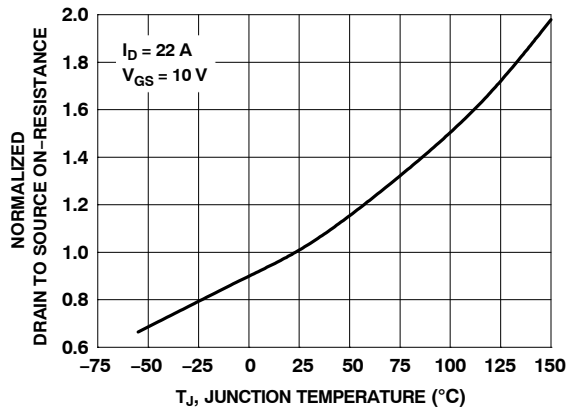


Figure 3. Normalized On-Resistance vs. Junction Temperature

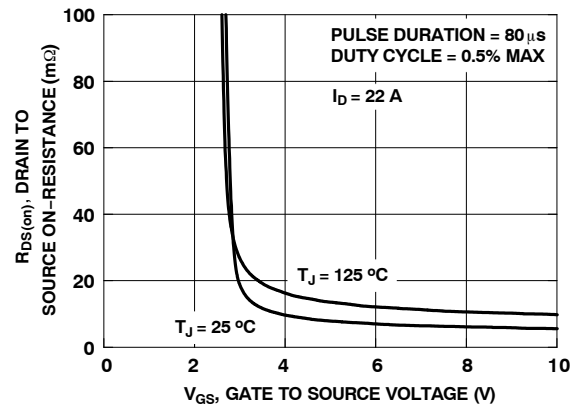


Figure 4. On-Resistance vs. Gate to Source Voltage

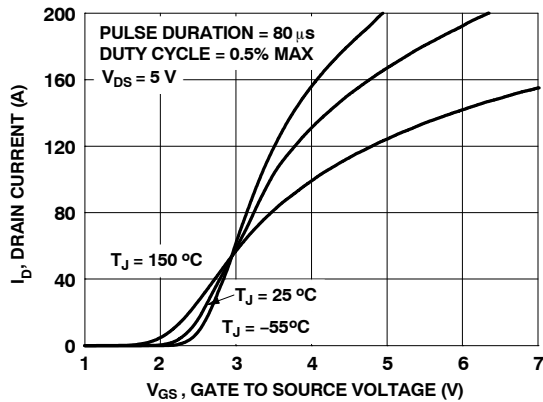


Figure 5. Transfer Characteristics

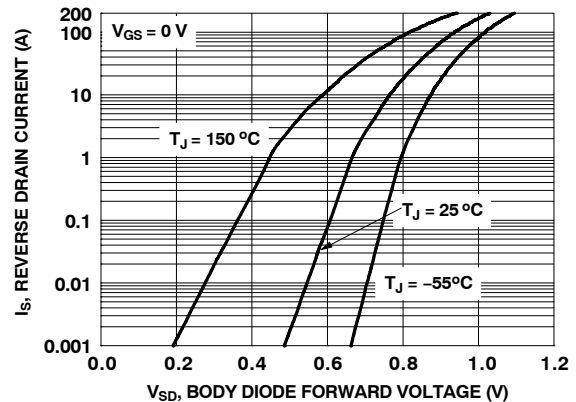


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

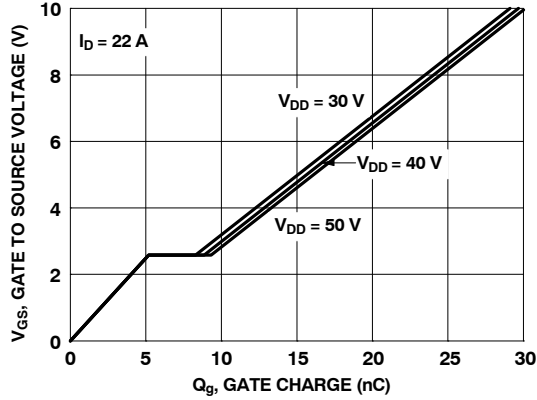


Figure 7. Gate Charge Characteristics

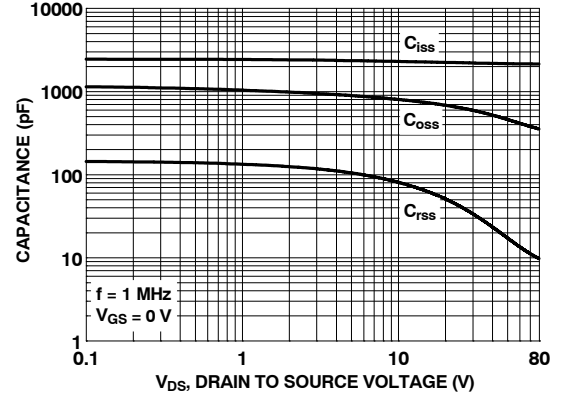


Figure 8. Capacitance vs. Drain to Source Voltage

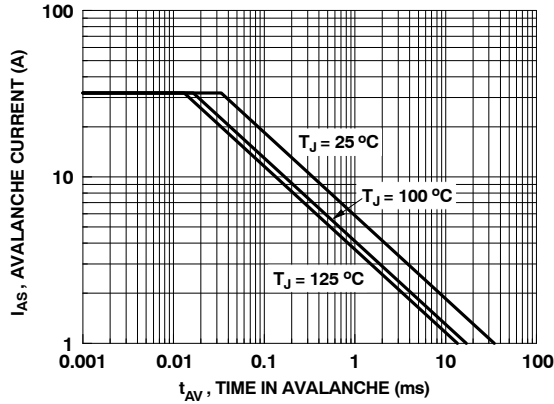


Figure 9. Unclamped Inductive Switching Capability

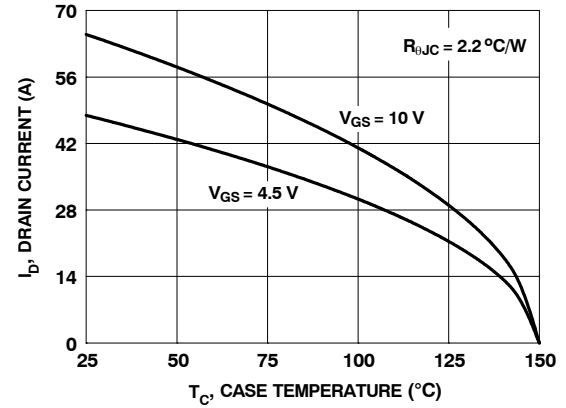


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

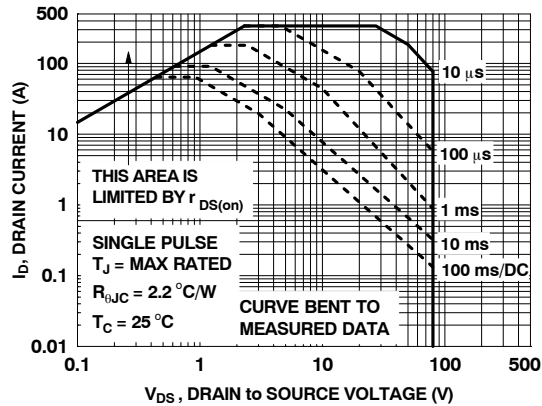


Figure 11. Forward Bias Safe Operating Area

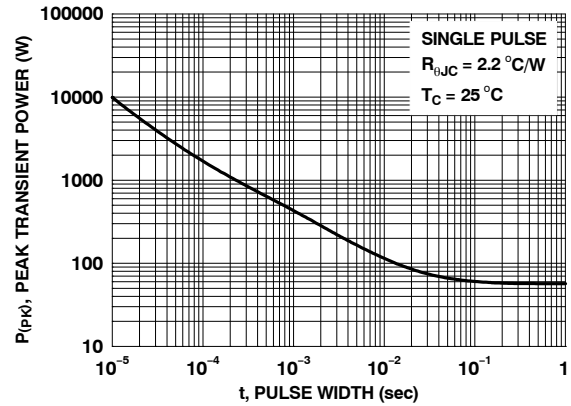


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

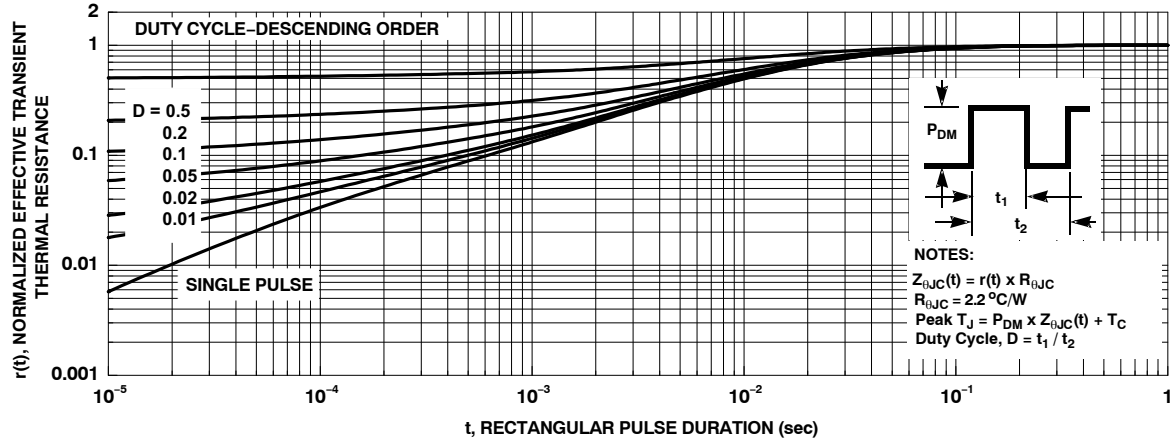
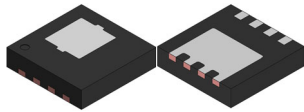


Figure 13. Junction-to-Case Transient Thermal Response Curve

ORDERING INFORMATION

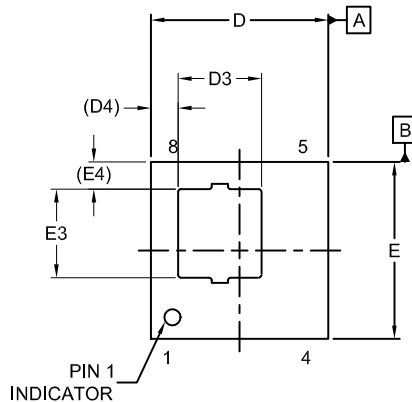
Device	Marking	Package	Reel Size	Tape Width	Quantity
FDMC007N08LCDC	7N08LDC	Dual Cool™ 33 (PQFN8) (Pb-Free / Halogen Free)	13"	12 mm	3000 Units

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

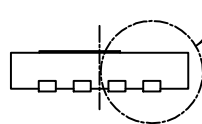


PQFN8 3.3X3.3, 0.65P
CASE 483AY
ISSUE A

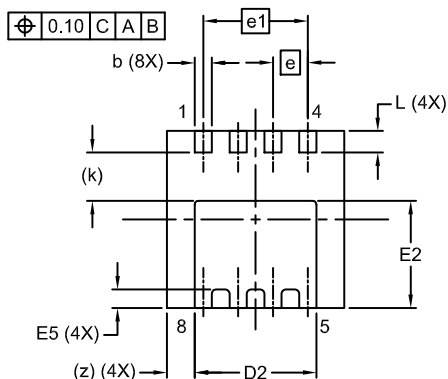
DATE 08 SEP 2021



TOP VIEW



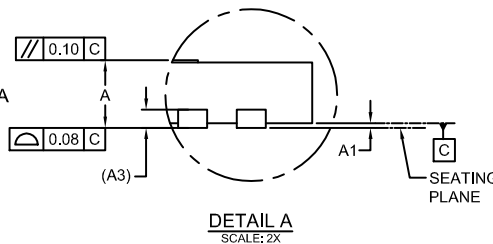
FRONT VIEW



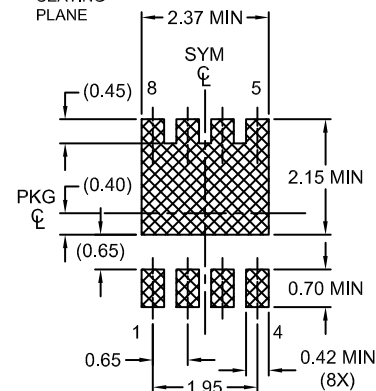
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	1.45	1.55	1.65
D4	0.51 REF		
E	3.20	3.30	3.40
E2	1.85	1.95	2.05
E3	1.55	1.65	1.75
E4	0.51 REF		
E5	0.24	0.34	0.44
e	0.65 BSC		
e1	1.95 BSC		
k	0.90 REF		
L	0.30	0.40	0.50
z	0.52 REF		



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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