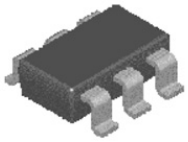
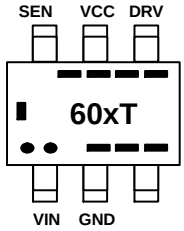
High-Side Sensing Constant Current Buck Controller for High Switching Frequency LED Driver

FL7760



SOT23−6LD
CASE 527AJ

MARKING DIAGRAM



(Top View)

60 : Production Identifier
x : Version (A or B)
T: Wafer Lot Code
▬▬ Week Code
▬▬▬ Year Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

The FL7760 is a constant current step−down CCM controller for wide output power LED lighting applications. The FL7760 adapts hysteretic reference architecture that accurately regulates LED current by sensing voltage across an external high side sense resistor. This control scheme can stabilize LED current against input voltage and output load transient condition and implement optimal PWM and analog dimming control. Time delay control method widens analog dimming range down to less than 5%.

FL7760 has low 200 mV reference voltage to maximize system efficiency and high frequency driving capability so that system profile can be minimized in wide scale power ranges.

The FL7760 implements PWM and analog dimming together through a DIM pin and provides thermal shutdown (TSD), and under−voltage lockout (UVLO) protections.

Features

- Wide Input Range (8 VDC~70 VDC)
- Continuous Conduction Mode Operation
- Hysteretic LED Current Control
- Wide analog dimming range down to 5%
- Wide PWM dimming duty range to 0.2% at 2 kHz PWM freq.
- High switching frequency up to 1 MHz
- High source / sink current of 1.5 A / 2.5 A
- Cycle−by−Cycle Peak Current Limit
- Low Operating Current (300 uA)
- Low Stand−by Current (240 uA)

Typical Applications

- LED Lighting System

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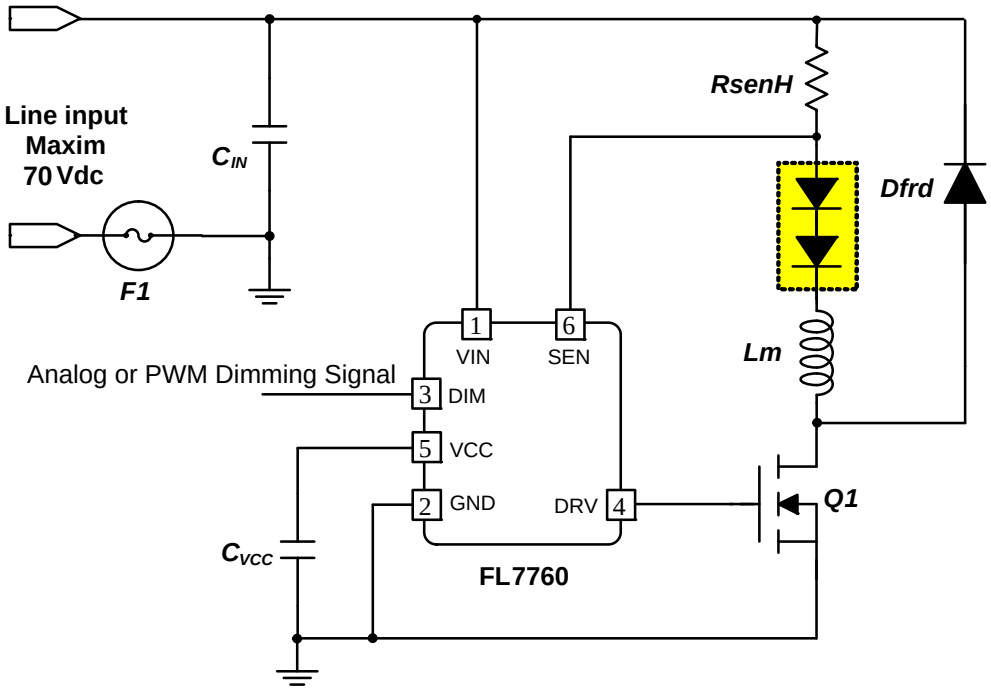
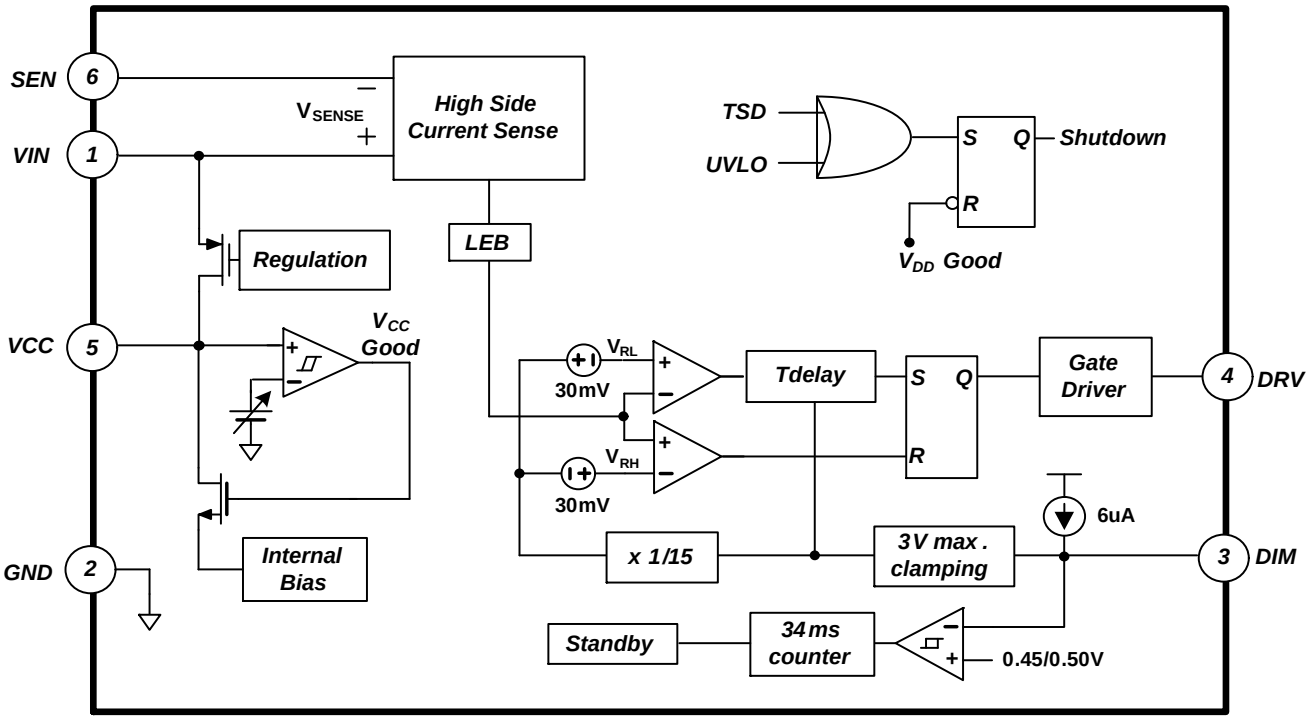


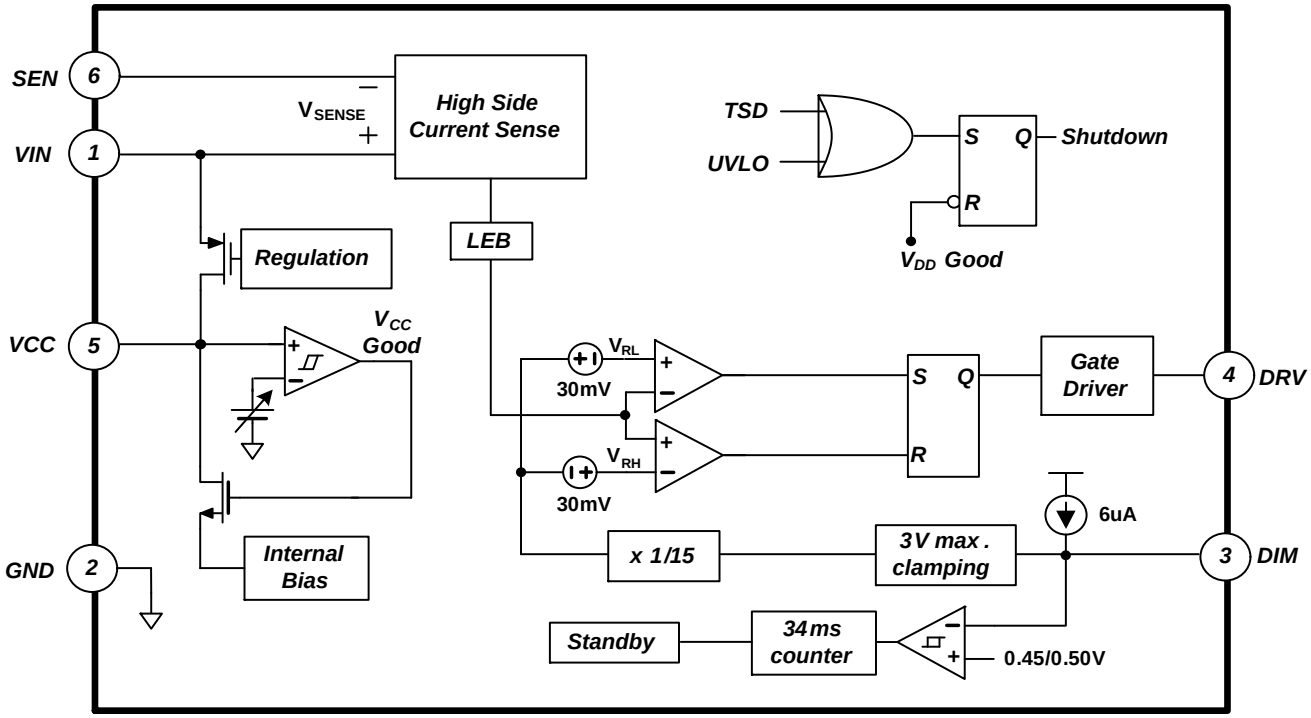
Figure 1. Application Schematic for Analog or PWM Dimming

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Function	Description
1	VIN	IC Input	Connect to the high voltage input line and supply current to the IC.
2	GND	Ground	Ground of IC.
3	DIM	Analog / PWM / Hybrid / Dimming	DIM voltage determines LED current regulation reference and switching is terminated when DIM voltage is 0 V. If dimming function is not used, it is recommended to add a 0.1 μF bypass capacitor between DIM and GND.
4	DRV	Driver Output	Connect to the MOSFET gate.
5	VCC	IC Supply	Supply pin for IC operation.
6	SEN	Current Sense	The SEN pin is used to set the output LED current regulation.



a) A Version (with Time Delay Control)



b) B Version (without Time Delay Control)

Figure 2. Block Diagram

Table 2. MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$VIN_{(MAX)}$	Maximum VIN Pin Voltage Range	−0.3 to 70	V
$SEN_{(MAX)}$	Maximum SEN Pin Voltage Range	−0.3 to 70	V
$VCC_{(MAX)}$	VCC Pin Voltage Range	−0.3 to 5.5	V
$VDIM_{(MAX)}$	DIM Pin Voltage Range	−0.3 to 5.5	V
$VDRV_{(MAX)}$	DRV Pin Voltage Range	−0.3 to 5.5	V
$VCC_{(PULSE)}$	Maximum VCC Pin Pulse Voltage at t_{PULSE} < 20 ns	8	V
$VDRV_{(PULSE)}$	Maximum DRV Pin Pulse Voltage at t_{PULSE} < 20 ns	8	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−65 to 150	°C
$R_{\theta JA}$	Junction−to−Ambient Thermal Impedance	263	°C/W
P_D	Power Dissipation	247	mW
ESD_{HBM}	ESD Capability, Human Body Model (Note 2)	1.2	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 2)	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
2. This device series incorporates ESD protection and is tested by the following methods
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

Table 3. ORDERING INFORMATION

Device	Package	Shipping†
FL7760AM6X	6LD,SOT23, JEDEC MO−178 VARIATION AB, 1.6MM WIDE	Tape & Reel
FL7760BM6X	6LD,SOT23, JEDEC MO−178 VARIATION AB, 1.6MM WIDE	Tape & Reel

Table 4. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Ambient Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
VIN SECTION						
Self BIAS Start Threshold Voltage	V_{CC} = 5 V	$V_{IN,ON}$	7.05	7.5	7.95	V
Self BIAS Stop Threshold Voltage	V_{CC} = 5 V	$V_{IN,OFF}$	6.55	7	7.45	V
Self BIAS Current for Startup (Note 3)		I_{ST}		2		mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This item is guaranteed by design.
4. This is only a recommended specification and there is no limit to the PWM Dimming frequency.
5. Drift after IC reliability test (JEDEC JESD22−A08) is not included.
6. This value indicates the change in internal reference voltage with temperature change and indicates the rate of change based on 25 °C ambient temperature. This item is guaranteed by design.

Table 5. ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 V, For typical values T_j = 25°C, for min/max values T_j = −40°C to +125°C, Max T_j = 150°C, unless otherwise noted)

Characteristics	Condition	Symbol	Min	Typ	Max	Unit
VCC SECTION						
VCC Regulator Output Voltage	V_{VIN} = 24 V_{DC}	V_{CC}	4.5	5	5.5	V
IC Start Threshold Voltage	V_{CC} Increasing	$V_{CC,ON}$	4.04	4.50	4.95	V
IC Stop Threshold Voltage	V_{CC} Decreasing	$V_{CC,OFF}$	3.03	3.50	3.96	V
UVLO Hysteresis		$V_{CC,HYS}$	0.505	1.000	1.485	V
Operation Current	No Switching	I_{CC}	51	300	495	uA
Stand−by Current (Note 3)	No Switching	I_{stby}	0.1	0.24	0.4	mA
GATE SECTION						
Gate High Voltage		$V_{GATE,H}$	4.5	5	5.5	V
Gate Low Voltage		$V_{GATE.L}$			0.5	V
Peak Pull−up Current (Note 3)	V_{CC} = 5 V	$I_{GATE,pullup}$		1.5		A
Peak Pull−down Current (Note 3)	V_{CC} = 5 V	$I_{GATE,pulldown}$		2.5		A
Recommended Maximum Operating Frequency (Note 4)		$F_{SW,MAX}$		1		MHz
CURRENT−SENSE AND REFERENCE SECTION						
Internal Reference Voltage	V_{DIM} = 3.5 V (T_J = 25°C)	$V_{FB,DC}$	192	200	208	mV
Internal Reference Voltage Drift (Note 5)	V_{DIM} = 3.5 V (T_J = 25°C)	$V_{FB,DC,R}$	196	200	204	mV
Variation of $V_{FB,DC}$ for Temperature (Note 6)	V_{DIM} = 3.5 V	$V_{FB,DC,T}$		±118.2		uV/°C
Feedback Reference Voltage Hysteresis	V_{DIM} = 3.5 V	$V_{FB,HYS}$		±30		mV
SWITCHING SECTION						
Minimum On−Time (Note 3)		$t_{ON,MIN}$		200		ns
Minimum Off−Time (Note 3)		$t_{OFF,MIN}$		200		ns
DIMMING SECTION						
Maximum Effective Dimming Voltage (Note 3)		$V_{DIM,MAX}$	2.7	3.0	3.3	V
Minimum Effective Dimming Voltage	V_{DIM}>$V_{DIM,R}$ then decreased	$V_{DIM,MIN}$	0.40	0.45	0.50	V
Dimming Recovery Voltage		$V_{DIM,R}$	0.45	0.50	0.55	V
Internal Sourcing Current Pull up to 3V		$I_{pull\ up,DIM}$	5	6	7	uA
Delay Time at 0.5 V_{DIM} (A version only, Note 3)	V_{DIM} = 0.5 V	$T_{Delay.max}$	5.00	5.35	5.70	us
Delay Time at 3 V_{DIM} (A version only, Note 3)	V_{DIM} = 3 V	$T_{Delay.min}$	28.5	30.0	31.5	ns
Blanking Time for Standby Mode (Note 3)	V_{DIM} = 0 V	$T_{Blank.stby}$	28	34	40	ms
THERMAL SHUT DOWN SECTION						
Thermal Shutdown Temperature (Note 3)			140	150		°C
Hysteresis Temperature of TSD (Note 3)				30		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. This item is guaranteed by design.
4. This is only a recommended specification and there is no limit to the PWM Dimming frequency.
5. Drift after IC reliability test (JEDEC JESD22−A08) is not included.
6. This value indicates the change in internal reference voltage with temperature change and indicates the rate of change based on 25 °C ambient temperature. This item is guaranteed by design.

TYPICAL CHARACTERISTICS

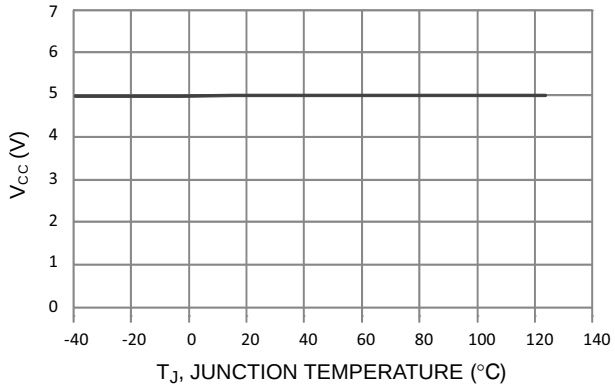


Figure 3. V_{CC} vs. Temperature

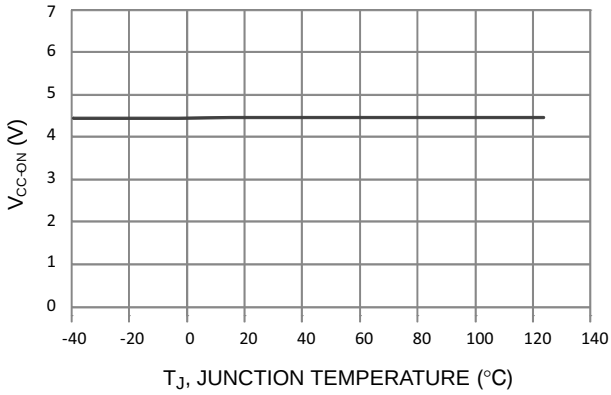


Figure 4. V_{CC-ON} vs. Temperature

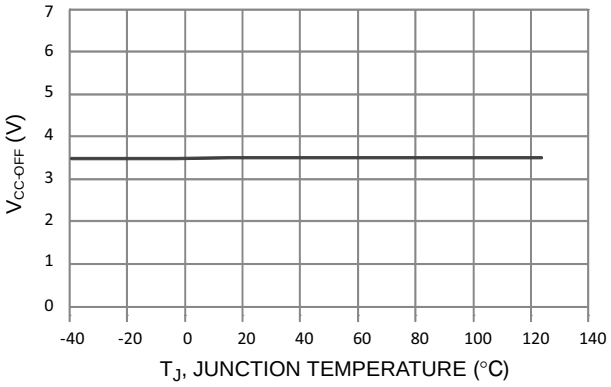


Figure 5. V_{CC-OFF} vs. Temperature

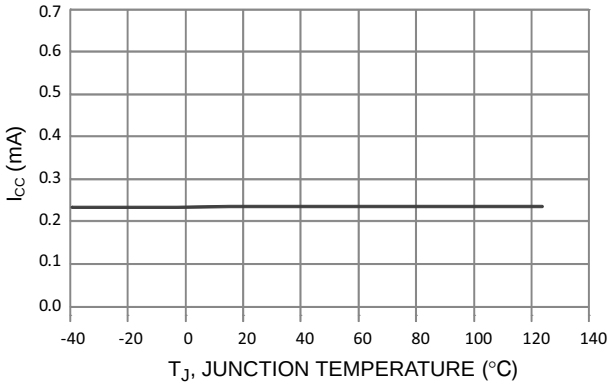


Figure 6. I_{CC} vs. Temperature

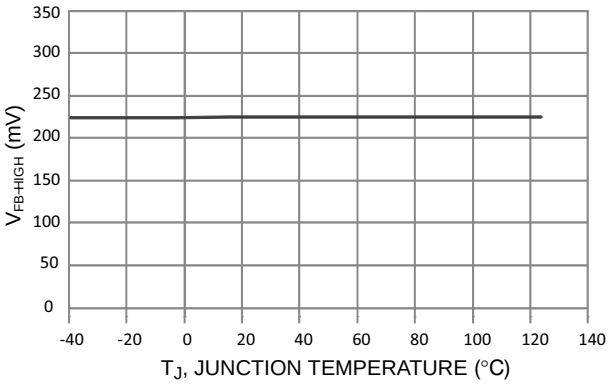


Figure 7. $V_{FB-HIGH}$ vs. Temperature

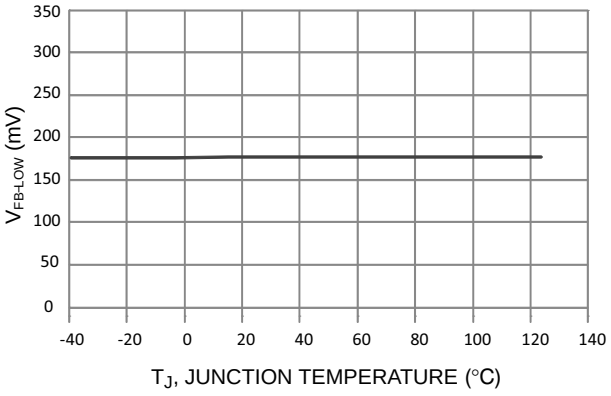


Figure 8. V_{FB-LOW} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

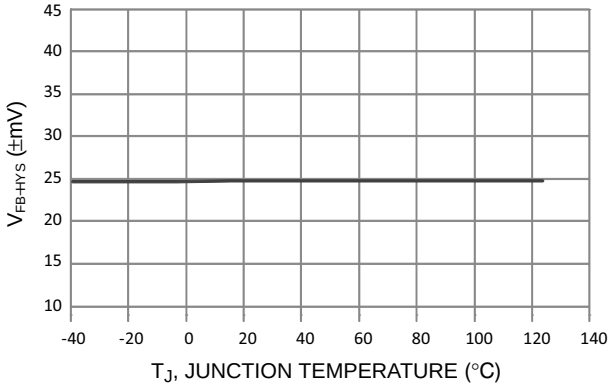


Figure 9. V_{FB-HYS} vs. Temperature

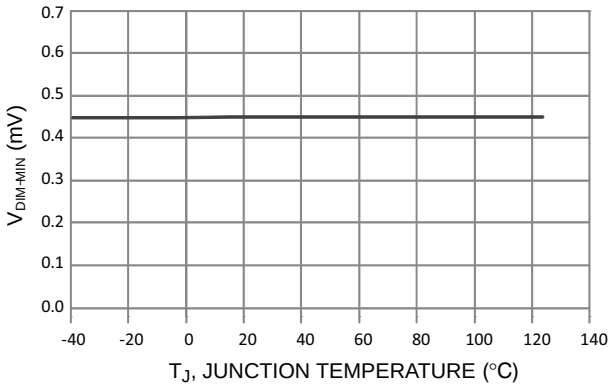


Figure 10. $V_{DIM-MIN}$ vs. Temperature

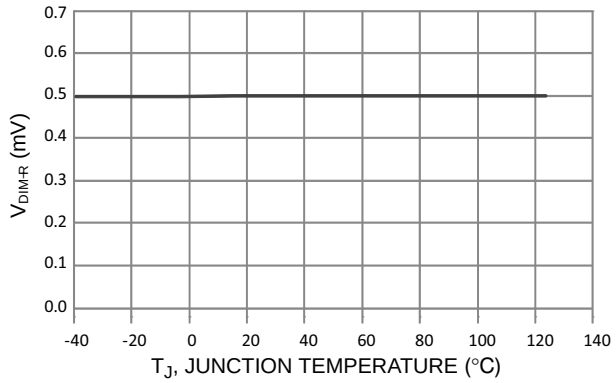


Figure 11. V_{DIM-R} vs. Temperature

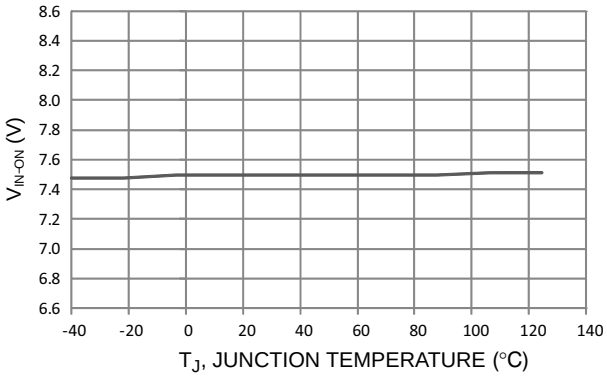


Figure 12. V_{IN-ON} vs. Temperature

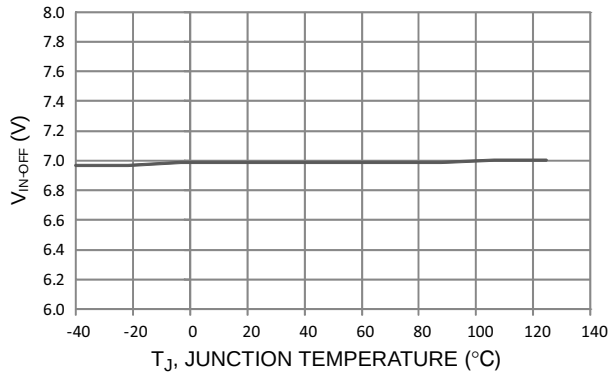


Figure 13. V_{IN-OFF} vs. Temperature

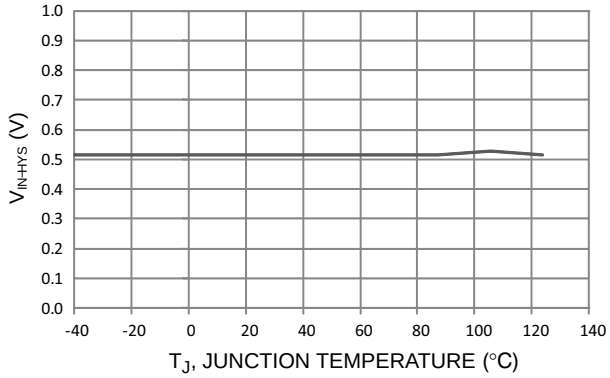


Figure 14. V_{IN-HYS} vs. Temperature

APPLICATION INFORMATION

General

The FL7760 is a step down hysteretic LED current controller that is easily configured in varies input voltage range from 8 V to 70 V. The converter employs a high side current sensing resistor to detect and regulate the LED current. Analog, PWM and hybrid dimming can be easily implemented with single DIM pin. In addition, the time delay control operation can realize analog dimming less than 5%.

Continuous Conduction Mode Regulation

The FL7760 employs hysteretic reference architecture that accurately regulates LED current by detecting an external high−side current−sense resistor voltage. The voltage across the current sensing resistor is kept measured and regulated in 200 mV±15% range. This control scheme performs stable LED current regulation at input voltage and load transient conditions..

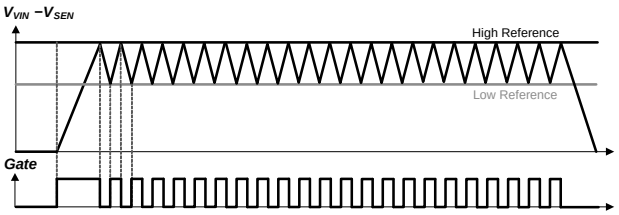


Figure 15. CCM Operation with Hysteresis

VIN biasing at startup

Internal VIN biasing circuit quickly charges external VCC capacitor to begin IC operation. During the initial start−up, the VCC pin voltage gradually increases, and when the voltage reaches 4.5 V, the IC starts operating by VCC good signal.

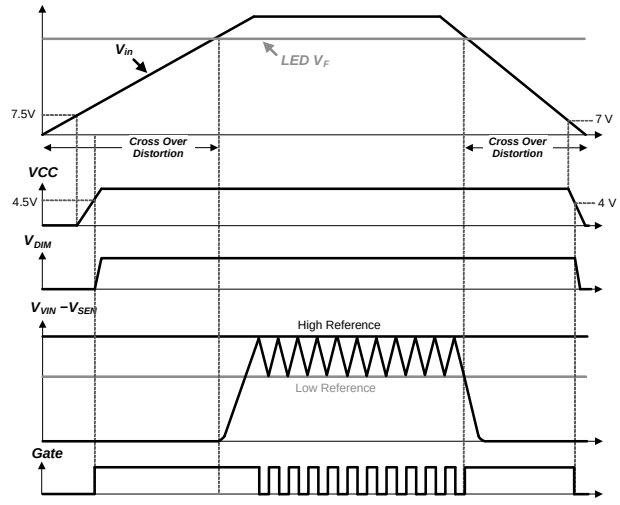


Figure 16. Start Up and Regulation

Thereafter, the internal current source in the DIM pin pulls up the DIM voltage and internal hysteresis reference is enabled with gate switching. Although the gate signal is generated and the MOSFET is turned on, the LED current is still close to zero in the crossover distortion area where the input voltage is lower than the LED forward voltage.

Soft Start

The hysteric reference voltage to regulate LED current is proportional to DIM voltage. Internal current source [6 uA] charges an external capacitor connected at DIM pin and soft start time can be programmable with capacitances. Soft start time can be calculated as below equation.

$$T_{SoftStart} = \frac{C_{DIM} \times 3V}{6uA} \qquad \text{(eq. 1)}$$

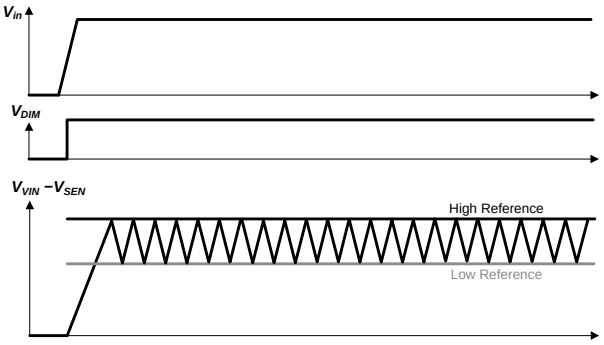


Figure 17. Soft Start with DIM pin Resistor

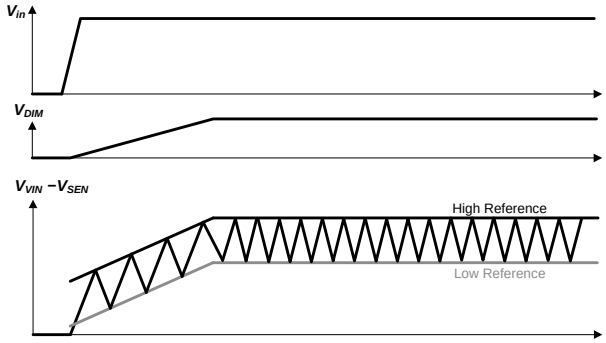


Figure 18. Soft Start with DIM pin Capacitor

Although soft start is not preferred, small filtering capacitor (~ hundreds pF) at DIM pin is recommended for noise immunity. PWM dimming signal delivered from an external PWM generator can be filtered by the capacitor, so the capacitor value needs to be carefully selected by considering an output impedance of PWM signal generator.

Analog Dimming

When DIM voltage is higher than 3 V, hysteretic reference voltage is set to 200 mV±30 mV. This hysteretic reference condition limits LED current ripple spec of ±15% without storage capacitor in parallel with the LED string.

The control range of the DIM pin in analog dimming is from 3 V to 0.5 V. As DIM voltage decreases, hysteretic

references are reduced accordingly with the fixed +/−30 mV hysteresis. To perform wide analog dimming range to less than 5%, the FL7760 has Time Delay Control (built in version A) with hysteresis control. In this delay control method, gate is not turned on during the delay time determined by DIM voltage once $V_{VIN} - V_{SEN}$ reaches to the low reference. Therefore, operating mode is entered into DCM (Discontinuous Current Mode) that makes non−linear dimming curve in low DIM voltage range.

Therefore, for analog dimming application with wide dimming requirement, version A is recommended and for PWM dimming application with linear dimming curve, version B is preferred.

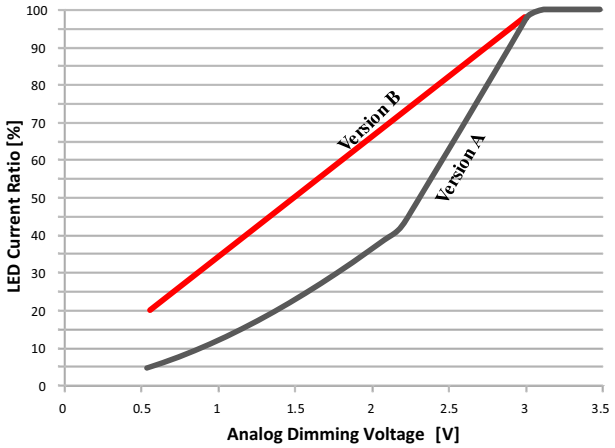


Figure 19. Analog Dimming Curve

PWM Dimming

If the DIM pin voltage is less than 0.45 V for 1 us blanking time, FL7760 stops switching. When the DIM voltage is up again over 0.5 V for the blanking time, switching begins. Based on the blanking time, the minimum duty ratio for PWM dimming can be calculated as 0.2% for a 2 kHz dimming signal.

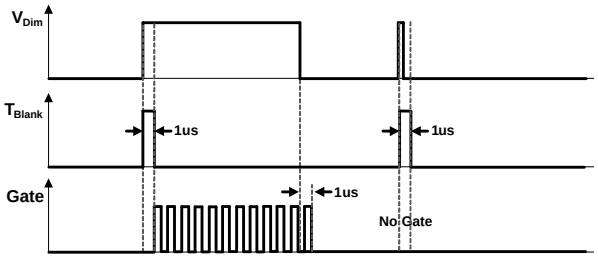


Figure 20. PWM Dimming

Hybrid Dimming

The FL7760 can implement hybrid dimming by adjusting amplitude and duty ratio of the single DIM signal provided at DIM pin. It provides wide dimming range with good dimming linearity.

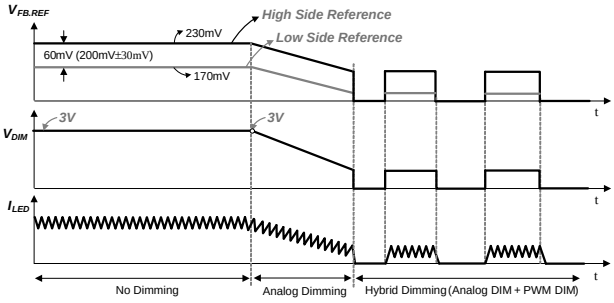


Figure 21. Hybrid Dimming

Standby Operation

When the voltage of the DIM pin falls below 0.45 V for 34 ms, standby mode is entered and the power consumption of the control circuitry is minimized. Standby mode is terminated once DIM voltage is over 0.5 V.

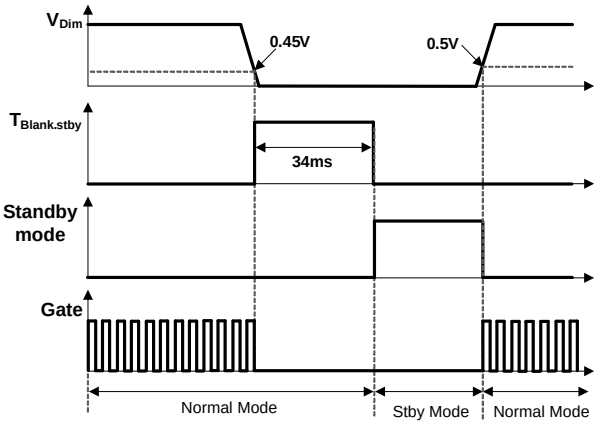


Figure 22. Standby Mode

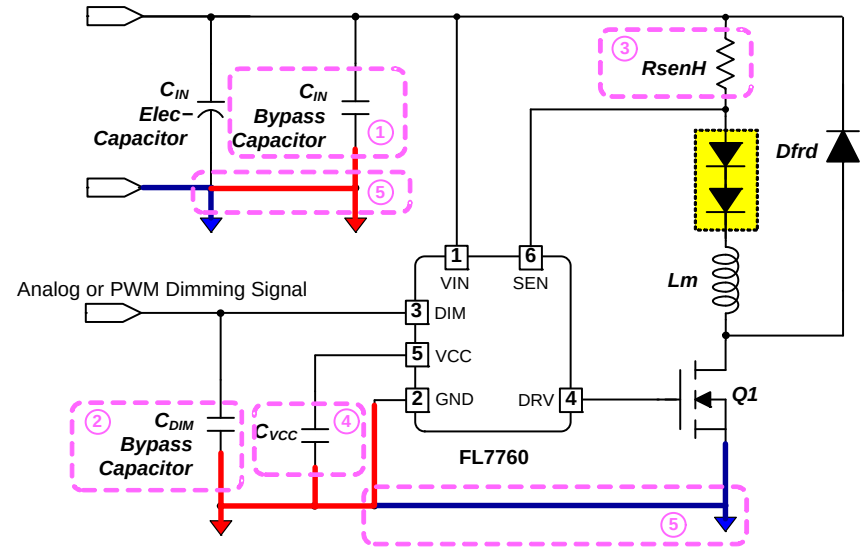
Thermal Shut Down

If internal junction temperature is higher than 150°C, TSD protection is triggered and released with 30°C hysteresis.

Selection the Input Capacitor

A low ESR input capacitor reduces the surge current and switching noise drawn from the front end power supply. Ceramic capacitors (100 ~ 120 nF) closely connected to VIN and GND pin can be effective in bypassing switching noise generated from front−end power stage and FL7760 buck converter stage.

Single layer PCB layout guidance



PG
(Power GND)

SG
(Signal GND)

① C_{IN} bypass capacitor is closely connected to VIN and GND pins .

② C_{DIM} bypass capacitor is closely connected to DIM and GND pins .

③ Sensing resistor is connected close at VIN and SEN pins .

④ VCC capacitor is connected close at VCC pin .

⑤ SG and PG are combined and connected close at GND pin .

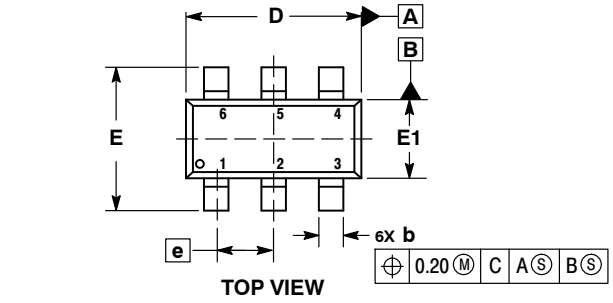
Figure 23. Single layer PCB layout guidance

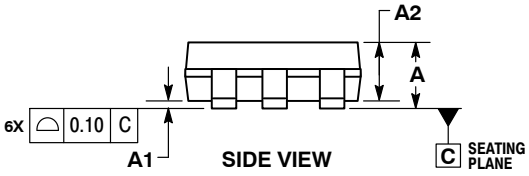
SOT−23, 6 Lead
CASE 527AJ
ISSUE B

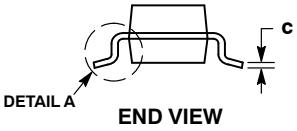
DATE 29 FEB 2012



SCALE 2:1



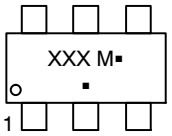




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

GENERIC MARKING DIAGRAM*

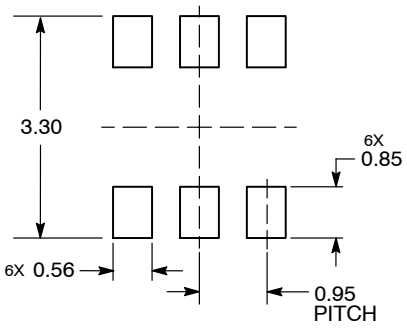


XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**SOT−23, 6 LEAD**	**PAGE 1 OF 1**

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