

MOSFET – P-Channel, QFET®

-200 V, -11.5 A, 470 mΩ

FQB12P20

General Description

These P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

Features

- -11.5 A, -200 V, $R_{DS(on)} = 0.47 \Omega @ V_{GS} = -10 V$
- Low Gate Charge (Typical 31 nC)
- Low C_{rss} (typical 30 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_C = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	FQB12P20	Unit
V_{DSS}	Drain-Source Voltage	-200	V
I_D	Drain Current – Continuous ($T_C = 25^\circ C$) – Continuous ($T_C = 100^\circ C$)	-11.5	A
		-7.27	A
I_{DM}	Drain Current – Pulsed (Note 1)	-46	A
V_{GSS}	Gate-Source Voltage	+30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	810	mJ
I_{AR}	Avalanche Current (Note 1)	-11.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	12	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.5	V/ns
	Power Dissipation ($T_A = 25^\circ C$) * Power Dissipation ($T_C = 25^\circ C$) – Derate above $25^\circ C$	3.13	W
		120	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*When mounted on the minimum pad size recommended (PCB Mount)

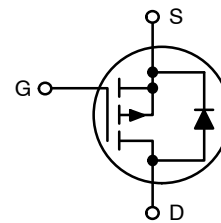
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 9.2 mH$, $I_{AS} = -11.5 A$, $V_{DD} = -50 V$, $R_G = 25 \Omega$, Starting $T_J = 25^\circ C$
3. $I_{SD} \leq -11.5 A$, $di/dt \leq 300 A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ C$



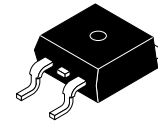
ON Semiconductor®

www.onsemi.com

V_{DSS}	$R_{DS(ON)} MAX$	$I_D MAX$
-200 V	$0.47 \Omega @ -10 V$	-11.5 A

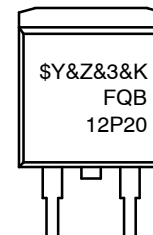


P-CHANNEL MOSFET



**D²PAK-3 (TO-263, 3-LEAD)
CASE 418AJ**

MARKING DIAGRAM



FQB12P20 = Specific Device Code
\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Digit Date Code
&K = Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FQB12P20

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	–	1.04	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	–	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	–	62.5	°C/W

*When mounted on the minimum pad size recommended (PCB Mount)

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-200	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	–	–	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -200\text{ V}, V_{GS} = 0\text{ V}$	–	–	-1	μA
		$V_{DS} = -160\text{ V}, T_C = 125^\circ\text{C}$	–	–	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	–	–	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	–	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -5.75\text{ A}$	–	0.36	0.47	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -5.75\text{ A}$ (Note 4)	–	6.4	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	–	920	1200	pF
C_{oss}	Output Capacitance		–	190	250	pF
C_{rss}	Reverse Transfer Capacitance		–	30	40	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -100\text{ V}, I_D = -11.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	–	20	50	ns
t_r	Turn-On Rise Time		–	195	400	ns
$t_{d(off)}$	Turn-Off Delay Time		–	40	90	ns
t_f	Turn-Off Fall Time		–	60	130	ns
Q_g	Total Gate Charge	$V_{DS} = -160\text{ V}, I_D = -11.5\text{ A},$ $V_{GS} = -10\text{ V}$ (Note 4, 5)	–	31	40	nC
Q_{gs}	Gate-Source Charge		–	8.1	–	nC
Q_{gd}	Gate-Drain Charge		–	16	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–11.5	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	–46	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –11.5 A	–	–	–5.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = –11.5 A, dI _F / dt = 100 A/μs (Note 4)	–	180	–	ns
Q _{rr}	Reverse Recovery Charge		–	1.44	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

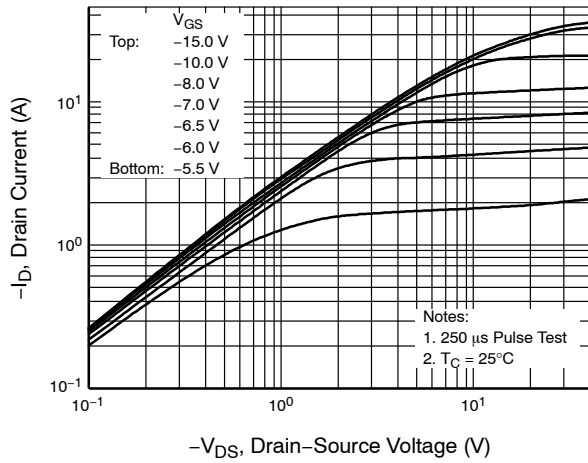


Figure 1. On Characteristics

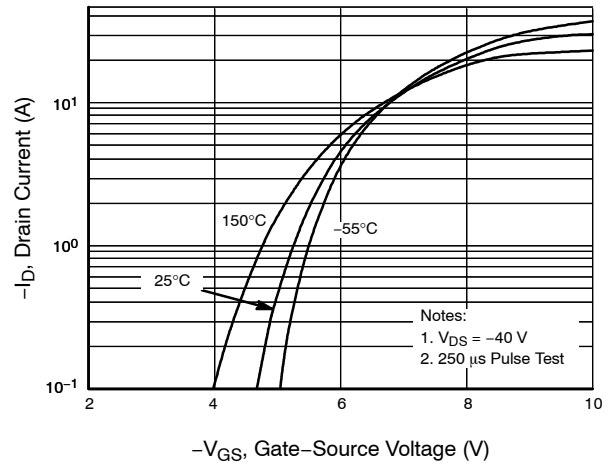


Figure 2. Transfer Characteristics

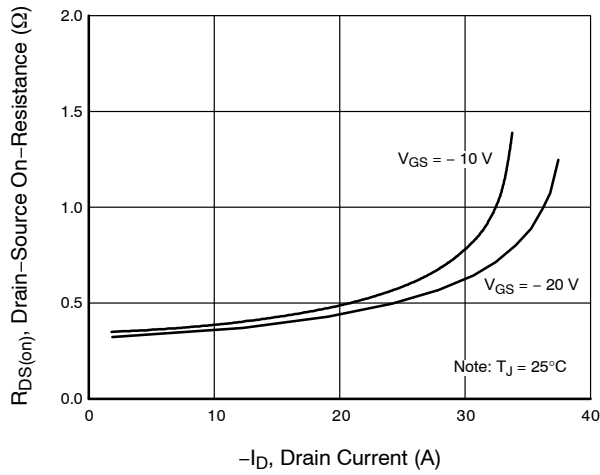


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

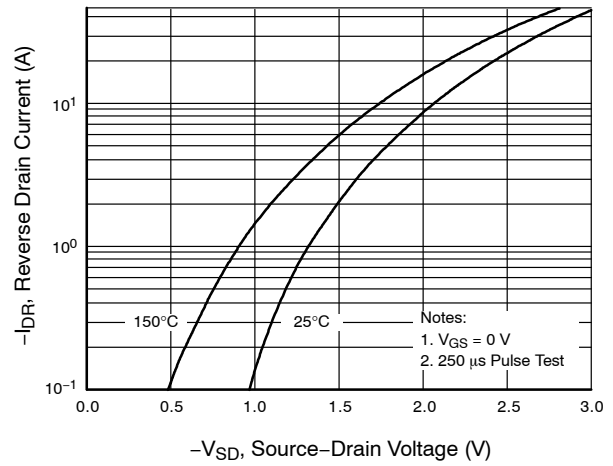


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

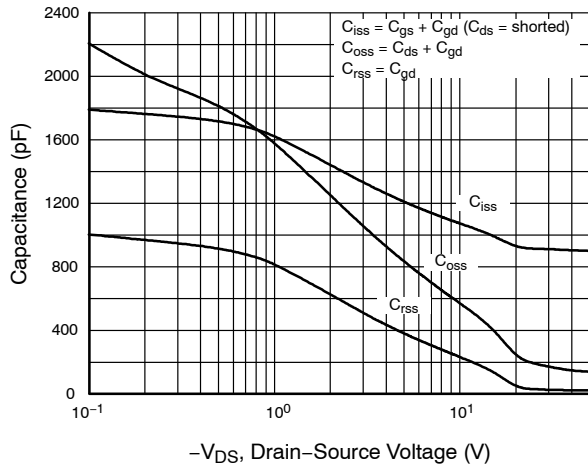


Figure 5. Capacitance Characteristics

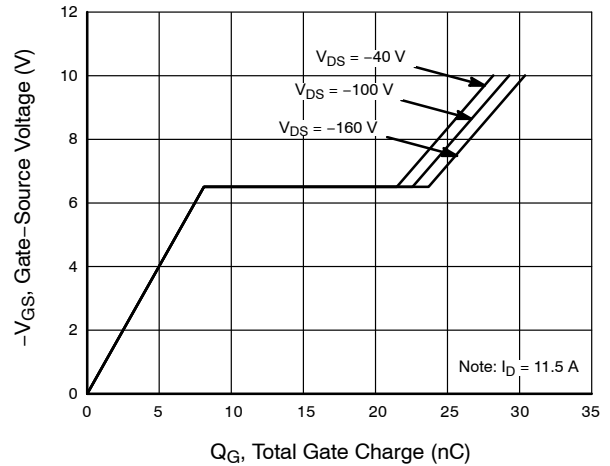


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

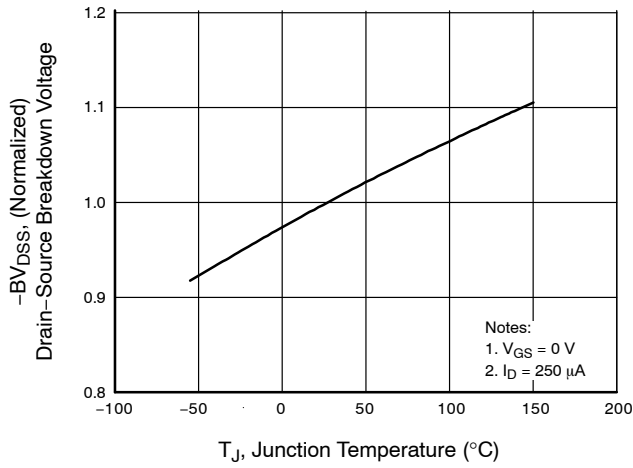


Figure 7. Breakdown Voltage Variation vs. Temperature

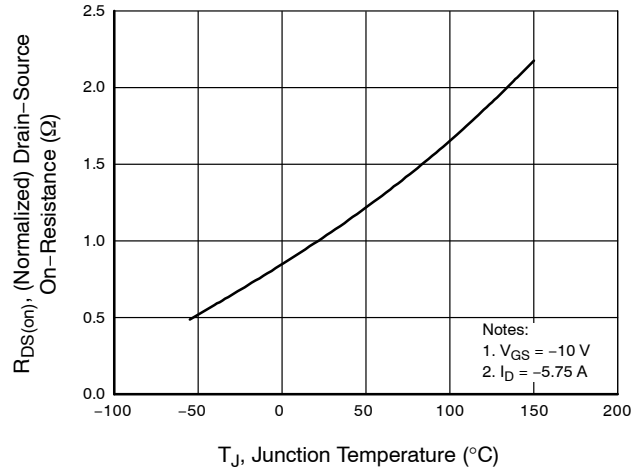


Figure 8. On-Resistance Variation vs. Temperature

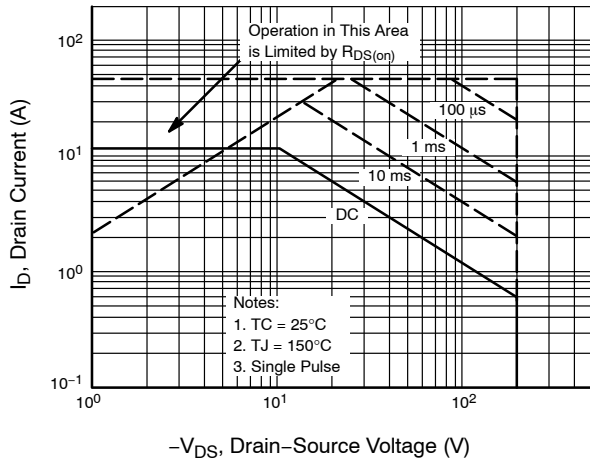


Figure 9. Maximum Safe Operating Area

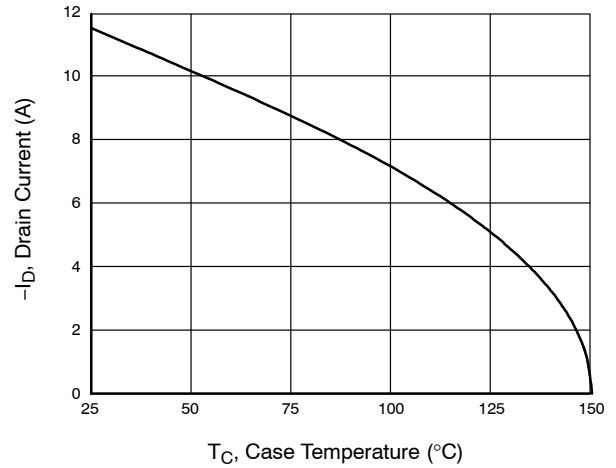


Figure 10. Maximum Drain Current vs. Case Temperature

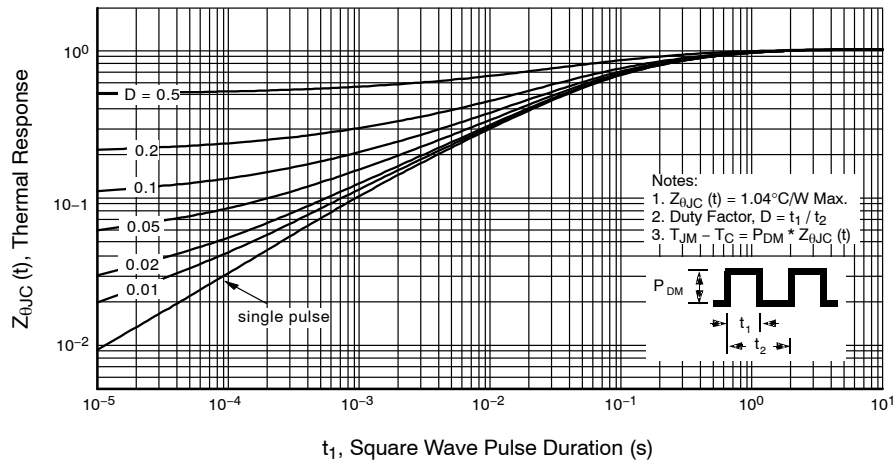


Figure 11. Capacitance Characteristics

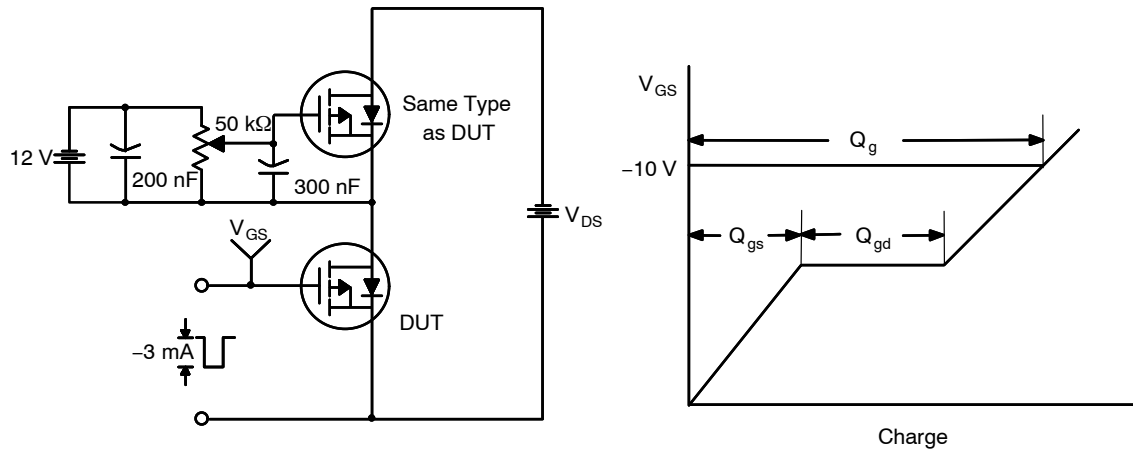


Figure 12. Gate Charge Test Circuit & Waveform

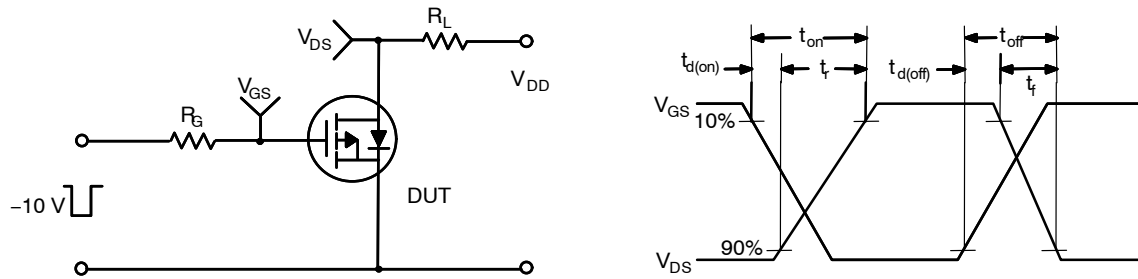


Figure 13. Resistive Switching Test Circuit & Waveforms

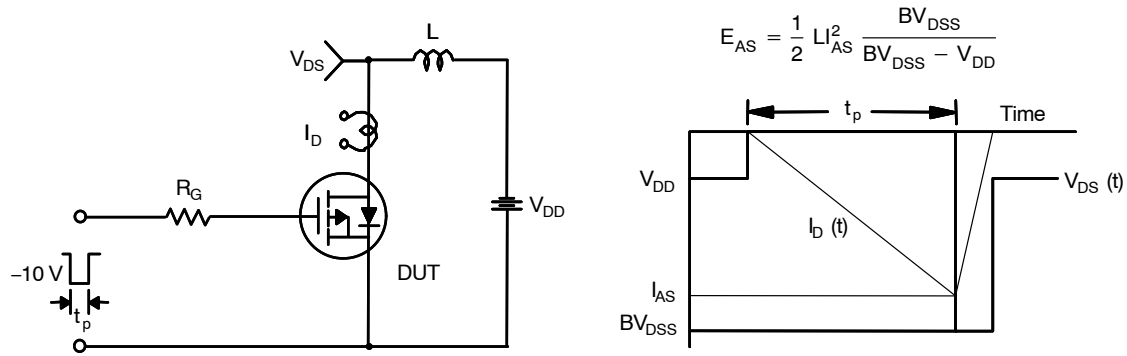


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

The top diagram shows a circuit for testing the body diode of a MOSFET. The DUT (Device Under Test) is an N-channel MOSFET with its source connected to ground and its drain connected to a load inductor L and a supply voltage V_{DD} . The drain-source voltage is V_{DS} and the drain-source current is I_{SD} . The gate of the DUT is driven by a "Driver" MOSFET (N-channel) whose source is connected to ground and its gate is driven by a pulse V_{GS} through a gate resistor R_G . The drain of the driver is connected to the gate of the DUT. The driver's drain-source voltage is V_{DS} and its drain-source current is I_{SD} . The driver's body diode is the "Compliment of DUT (N-Channel)".

The bottom part of the image shows three waveforms:

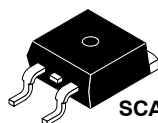
- V_{GS} (Driver):** A square wave pulse with a duty cycle $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$. The pulse height is 10 V .
- I_{SD} (DUT):** The drain-source current of the DUT. It shows a negative reverse current I_{RM} during the gate pulse, followed by a positive forward current I_{FM} during the recovery phase. The recovery phase is labeled "Body Diode Recovery dv/dt ".
- V_{DS} (DUT):** The drain-source voltage of the DUT. It shows a positive voltage V_{SD} during the gate pulse, followed by a negative voltage V_{DD} during the recovery phase. The recovery phase is labeled "Body Diode Forward Voltage Drop".

PACKAGE MARKING AND ORDERING INFORMATION

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

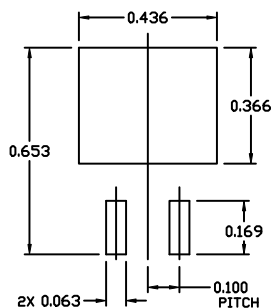
ON Semiconductor®



SCALE 1:1

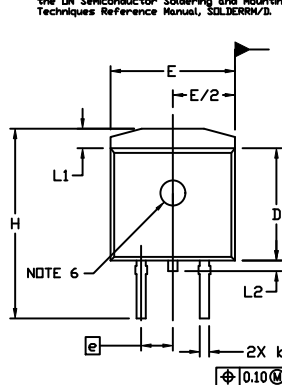
D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

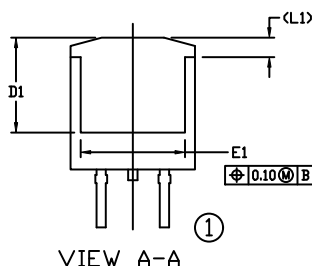
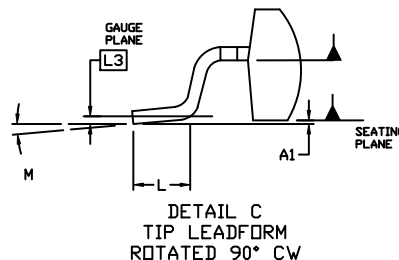
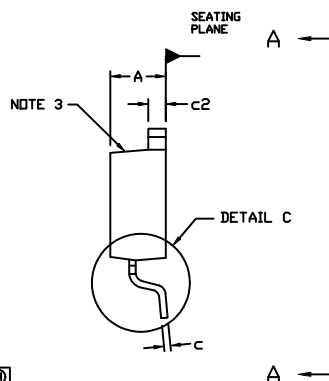
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/T.



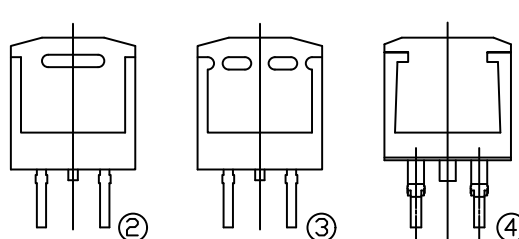
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

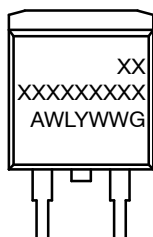


VIEW A-A

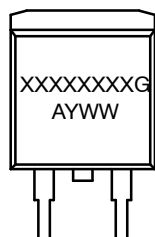


VIEW A-A
OPTIONAL CONSTRUCTIONS

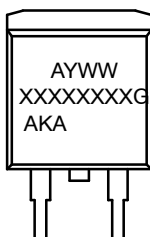
GENERIC MARKING DIAGRAMS*



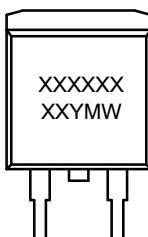
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON56370E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	D ² PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative