KA2807

Ground Fault Circuit Interrupter

Description

The KA2807 is an IC for ground fault circuit interrupters which are intended to provide an electrical shock hazard protection from line to ground fault currents on grounded circuits of 120 V supplies.

Features

- Full Advantage of the UL943
- Built−In Voltage Regulator
- Sense Coil Ratio – 1000:1
- GND/Neutral Coil Ratio – 200:1
- Trip Time in Normal Fault and Grounded Neutral Fault is 18 ms Typ
- Wide Operating Temperature Range
- Excellent ESD Characteristic
- 1 mA Output Current Pulse to Trigger SCR
- Available in 8 Pin SOIC and 8 Pin MSOP
- Pb−Free Device

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RELATED STANDARDS

UL943

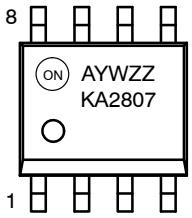


SOIC8
CASE 751EB

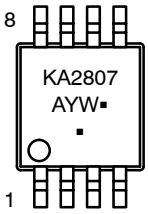


Micro8
CASE 846A

MARKING DIAGRAMS



SOIC8



Micro8

KA2807 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly LOT Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
KA2807DTF	SOIC (Pb−Free)	2,500 / Tape & Reel
KA2807MUX	Micro8 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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PIN ASSIGNMENT

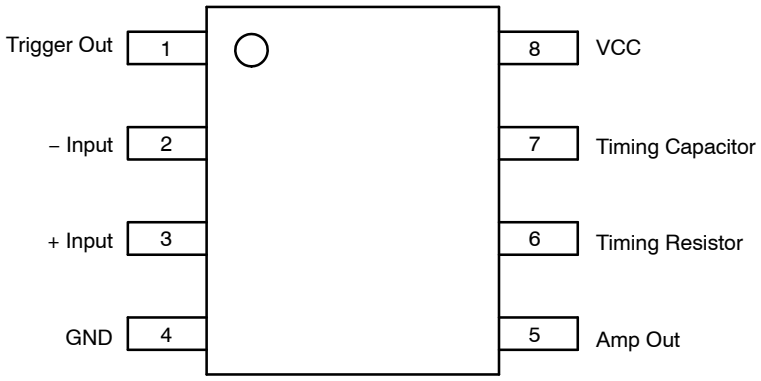


Figure 1. Pin Out KA2807 in 8−pin SOP or MSOP (Top View)

BLOCK DIAGRAM

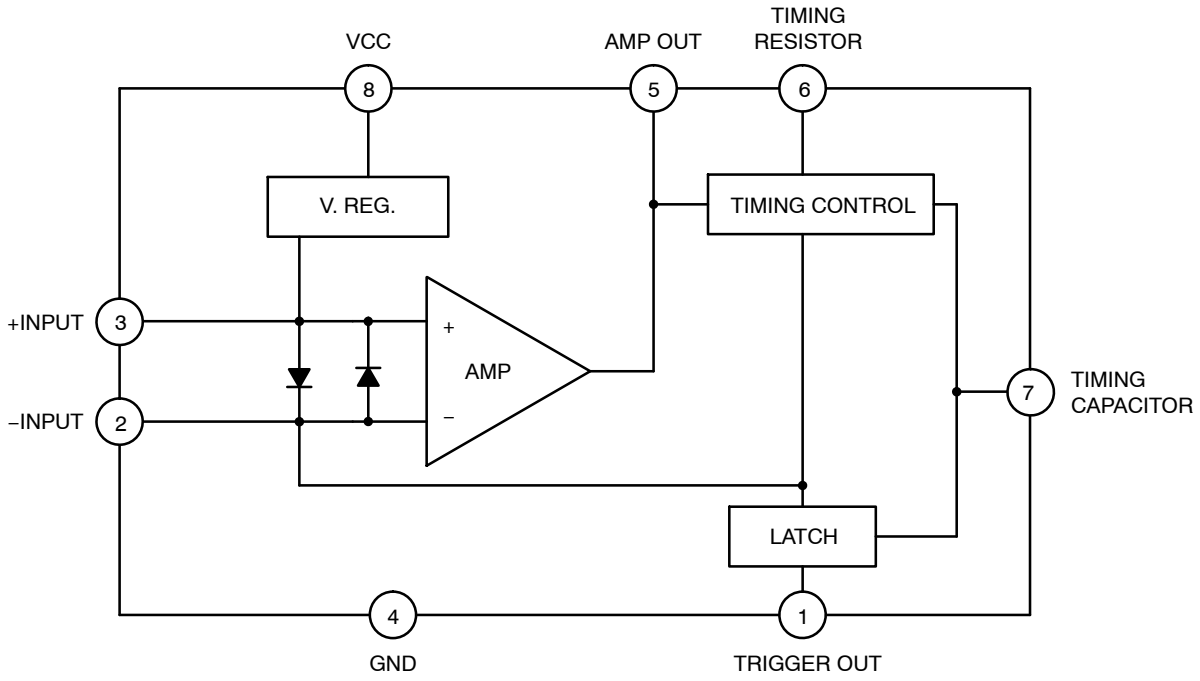


Figure 2. KA2807 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
I_{CC}	Supply Current	–	+19	mA
P_D	Power Dissipation SOIC−8 MSOP−8	 – –	 0.41 0.3	W
T_{OPR}	Operating Temperature Range	−40	+70	°C
T_{STG}	Storage Temperature Range	−55	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REG}	Shunt Regulator Voltage	Pin 8, S1: 2, S2: OFF	23	26	29	V
V_{REF}	Amplifier Reference Voltage	Pin 3, S1: 2, S2: OFF	9.5	10.5	11.5	V
V_{OH}	Amplifier High Output Voltage	Pin 5, S1: 3, S2: ON Sig: 800 Hz, 3.0 V_{P-P} Sinusoidal wave	17	19	21	V
V_{OL}	Amplifier Low Output Voltage	Pin 5, S1: 3, S2: ON Sig: 800 Hz, 3.0 V_{P-P} Sinusoidal wave	1.5	2.5	3.5	V
I_{SEN}	Amplifier Sensitivity Current	Pin 2, S1: 3, S2: ON Sig: 800 Hz, 1.0 V_{P-P} ~ 2.5 V_{P-P} Sinusoidal wave	3.5	5	6.5	μArms
$V_{ON(LATCH)}$	Latch On Voltage	Pin 7, S1: 3, S2: ON Sig: 800 Hz, 3.0 V_{P-P} Sinusoidal wave	16.5	17.5	19.5	V
I_{TR}	SCR Trigger Current	Pin 1, S1: 3, S2: ON Sig: 800 Hz, 3.0 V_{P-P} Sinusoidal wave	0.5	1	2.0	mA
V_S 1	Output Low Voltage	Pin 1, S1: 2, S2: OFF	–	100	240	mA
Z_O	Output Impedance	Pin 1, S1: 2, S2: OFF	–	100	250	Ω
I_{SINK}	Output Sink Current	Pin 1, S1: 2, S2: OFF	2.0	6.0	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TEST CIRCUIT

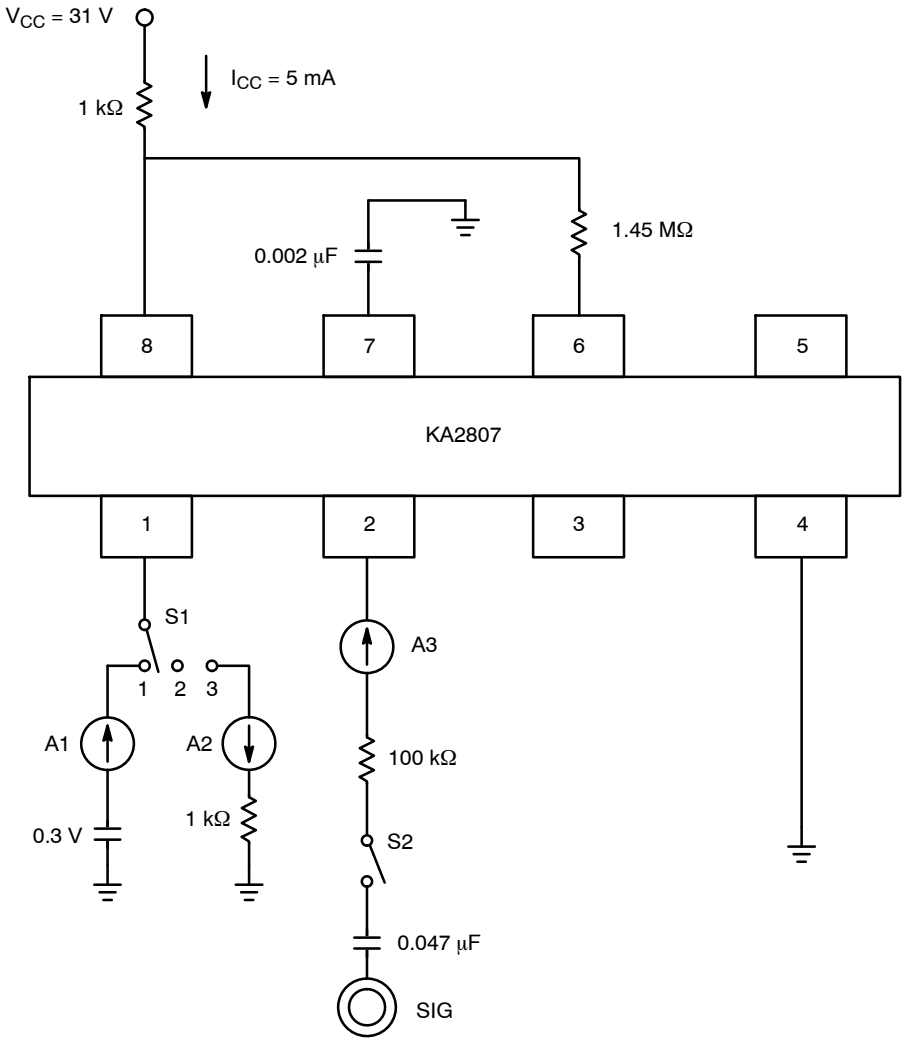
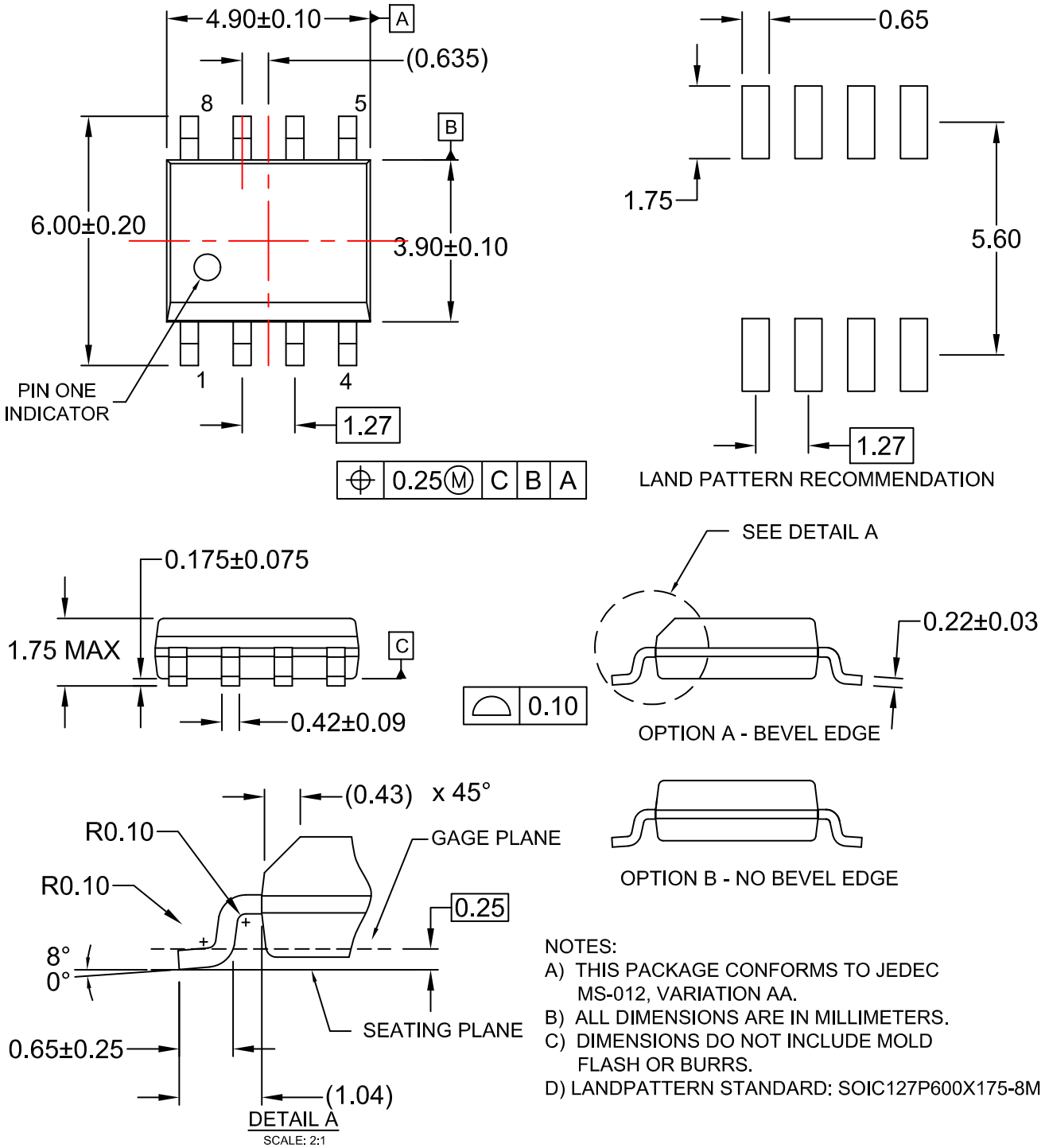


Figure 3. KA2807 Test Circuit

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

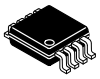
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

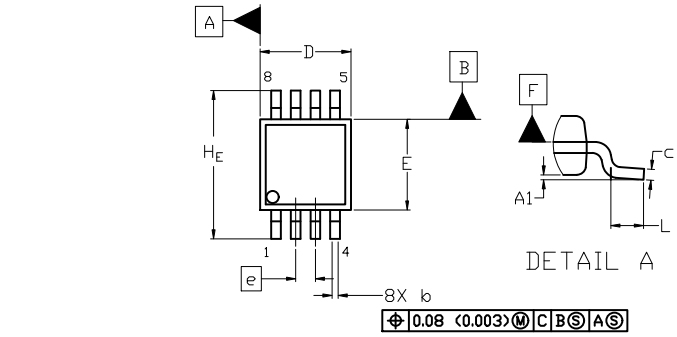
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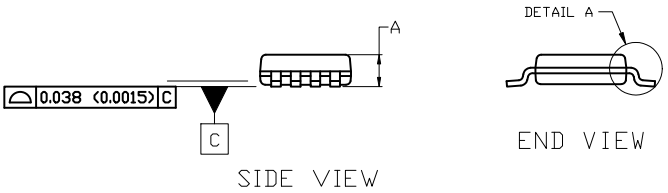


SCALE 2:1

Micro8
CASE 846A−02
ISSUE K

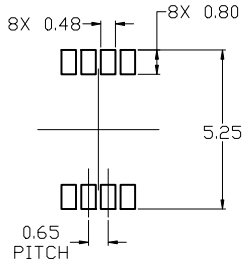
DATE 16 JUL 2020





NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

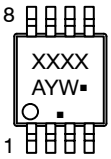


RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.05	0.08	0.15
b	0.25	0.33	0.40
c	0.13	0.18	0.23
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e	0.65 BSC		
H_E	4.75	4.90	5.05
L	0.40	0.55	0.70

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 3:
PIN 1. N-SOURCE
2. N-GATE
3. P-SOURCE
4. P-GATE
5. P-DRAIN
6. P-DRAIN
7. N-DRAIN
8. N-DRAIN

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