

5.0 V ECL 8-Bit Synchronous Binary Up Counter

MC10E016, MC100E016

Description

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10H™ family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC} = \text{LOW}$, thus functioning as a programmable counter. The Q_n outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

The 100 series contains temperature compensation.

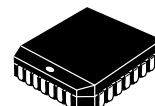
Features

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- PECL Mode Operating Range: $V_{CC} = 4.2 \text{ V}$ to 5.7 V with $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0 \text{ V}$ with $V_{EE} = -4.2 \text{ V}$ to -5.7 V
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



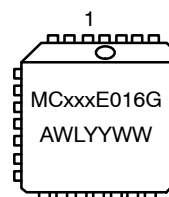
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PLCC-28
FN SUFFIX
CASE 776-02

MARKING DIAGRAM*



xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

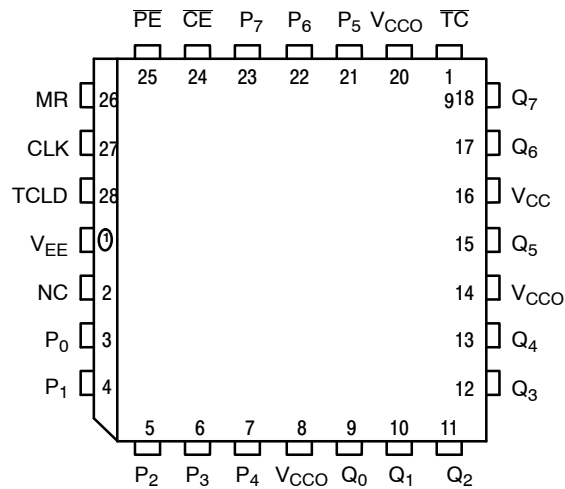
*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC10E016FNG	PLCC-28 (Pb-Free)	37 Units/Tube
MC10E016FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel
MC100E016FNR2G	PLCC-28 (Pb-Free)	500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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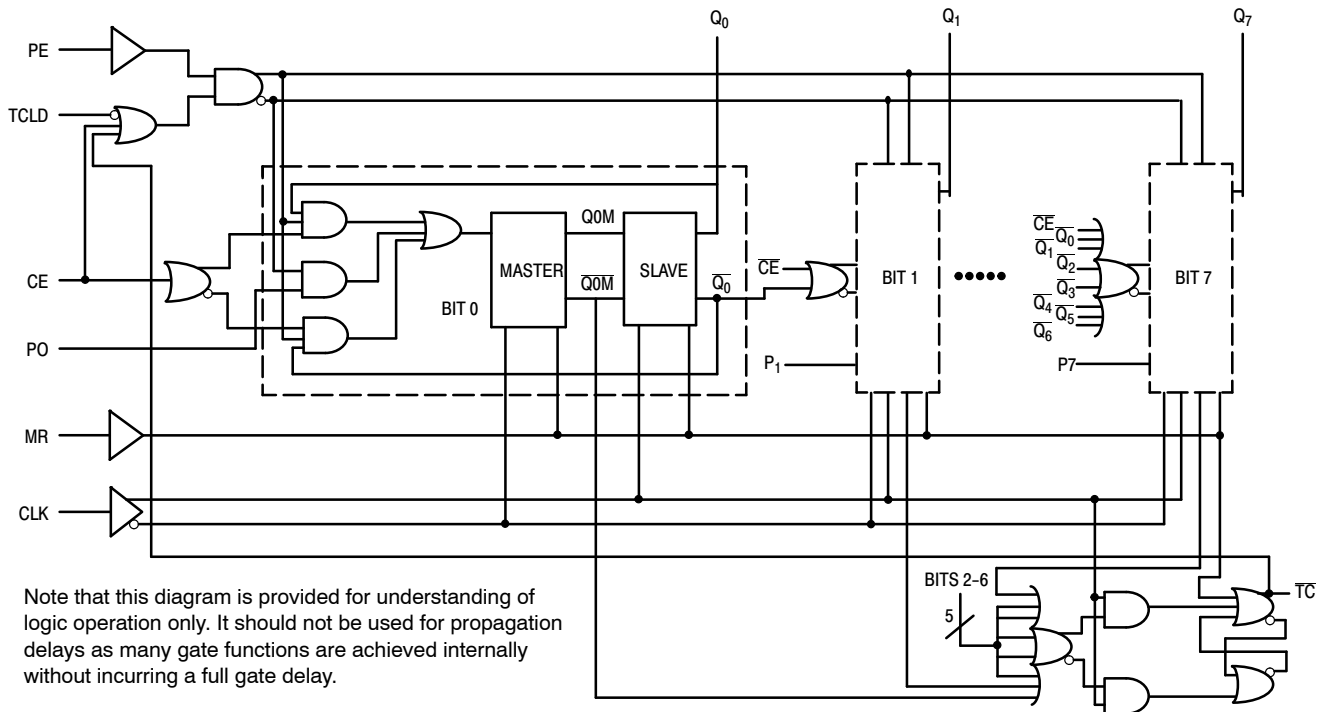


All V_{CC} and V_{CCO} pins are tied together on the die.
Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 28-Lead Pinout Assignment (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
$P_0 - P_7$	ECL Parallel Data (Preset) Inputs
$Q_0 - Q_7$	ECL Data Outputs
CE	ECL Count Enable Control Input
PE	ECL Parallel Load Enable Control Input
MR	ECL Master Reset
CLK	ECL Clock
TC	ECL Terminal Count Output
TCLD	ECL TC-Load Control Input
NC	No Connect
V_{CC} , V_{CCO}	Positive Supply
V_{EE}	Negative Supply



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

Figure 2. 8-Bit Binary Counter Logic Counter

Table 2. FUNCTION TABLE

FUNCTION	CE	PE	TCLD	MR	CLK
Load Parallel (P_n to Q_n)	X	L	X	L	Z
Continuous Count	L	H	L	L	Z
Count; Load Parallel on $TC = LOW$	L	H	H	L	Z
Hold	H	H	X	L	Z
Masters Respond, Slaves Hold	X	X	X	L	ZZ
Reset ($Q_n := LOW$, $TC := HIGH$)	X	X	X	H	X

Z = clock pulse (low to high);
ZZ = clock pulse (high to low)

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Table 3. EXPANDED FUNCTION TABLE

Function	PE	CE	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	TC
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

Table 4. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	50 kΩ
Internal Input Pullup Resistor	50 kΩ
ESD Protection Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) PLCC-28	Pb-Free Pkg Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	592 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V
I _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC-28 PLCC-28	63.5 43.5	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC-28	22 to 26	°C/W
T _{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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Table 6. 10E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

Table 7. 10E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1020	-930	-840	-980	-895	-810	-910	-815	-720	mV
V_{OL}	Output LOW Voltage (Note 2)	-1950	-1790	-1630	-1950	-1790	-1630	-1950	-1773	-1595	mV
V_{IH}	Input HIGH Voltage	-1170	-1005	-840	-1130	-970	-810	-1060	-890	-720	mV
V_{IL}	Input LOW Voltage	-1950	-1715	-1480	-1950	-1715	-1480	-1950	-1698	-1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

Table 8. 100E SERIES PECL DC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		174	208	mA
V_{OH}	Output HIGH Voltage (Note 2)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage	3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

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Table 9. 100E SERIES NECL DC CHARACTERISTICS ($V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		174	208	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1025	-950	-880	-1025	-950	-880	-1025	-950	-880	mV
V_{OL}	Output LOW Voltage (Note 2)	-1810	-1705	-1620	-1810	-1745	-1620	-1810	-1740	-1620	mV
V_{IH}	Input HIGH Voltage	-1165	-1025	-880	-1165	-1025	-880	-1165	-1025	-880	mV
V_{IL}	Input LOW Voltage	-1810	-1645	-1475	-1810	-1645	-1475	-1810	-1645	-1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
2. Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.

Table 10. AC CHARACTERISTICS ($V_{CCx} = 5.0\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CCx} = 0.0\text{ V}$; $V_{EE} = -5.0\text{ V}$ (Note 1))

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		700			700			700		MHz
f_{COUNT}	Maximum Count Frequency	700	900		700	900		700	900		MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output CLK to Q MR to Q CLK to $\overline{TC}$ MR to $\overline{TC}$	500 500 500 500	725 775 775 775	900	500 500 500 500	725 775 775 775	900	500 500 500 500	725 775 775 775	900	ps
t_s	Setup Time (to CLK +)										ps
t_s	Setup Time (to CLK +) Pn CE PE TCLD	150 600 600 500	-30 400 400 300		150 600 600 500	-30 400 400 300		150 600 600 500	-30 400 400 300		ps
t_h	Hold Time (to CLK +) Pn CE PE TCLD	350 400 0 100	100 200 200 -300		350 400 0 100	100 200 200 -300		350 400 0 100	100 200 200 -300		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width CLK, MR	400			400			400			ps
t_{JITTER}	Random Clock Jitter (RMS)		< 1			< 1			< 1		ps
t_r, t_f	Rise/Fall Times (20–80%)	200	510	700	200	510	700	200	510	700	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. 10 Series: V_{EE} can vary $-0.46\text{ V} / +0.06\text{ V}$.
100 Series: V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

Note that this assumes the trace delay between the $\overline{\text{TC}}$ outputs and the $\overline{\text{CE}}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.



APPLICATIONS INFORMATION (continued)

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 4 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

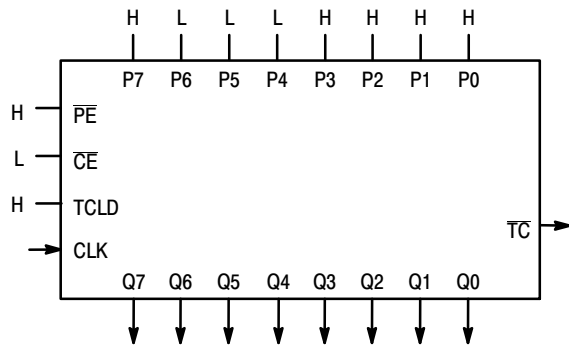


Figure 4. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

$$Pn's = 256 - 113 = 8F_{16} = 1000\ 1111$$

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 4 will result in the waveforms of Figure 5. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is

equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 11. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
w	w	•	•	•	•	•	•	•
w	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

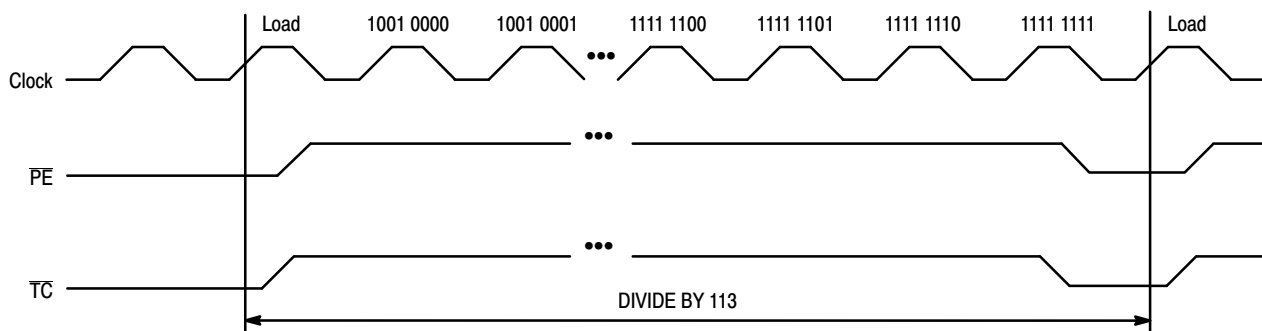


Figure 5. Divide by 113 E016 Programmable Divider Waveforms

APPLICATIONS INFORMATION (continued)

Maximizing E016 Count Frequency

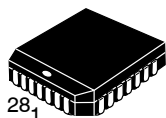
The diagram shows a differential signaling system. On the left, a dashed box labeled "Driver Device" contains two signal sources, Q and $\bar{Q}$. Each source is connected to a series resistor labeled $Z_0 = 50\ \Omega$. The output of the first resistor is connected to a node that branches to a load resistor D (part of the Receiver Device) and a common-mode feedback network. The output of the second resistor is connected to a node that branches to a load resistor $\bar{D}$ (part of the Receiver Device) and the same common-mode feedback network. The common-mode feedback network consists of two $50\ \Omega$ resistors connected in series between the two signal nodes, with a third $50\ \Omega$ resistor connected from the midpoint of this series combination to a common ground symbol. Below the ground symbol, the text V_{TT} and $V_{TT} = V_{CC} - 2.0\text{ V}$ is present.

8

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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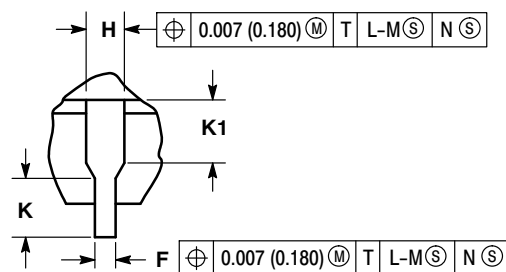
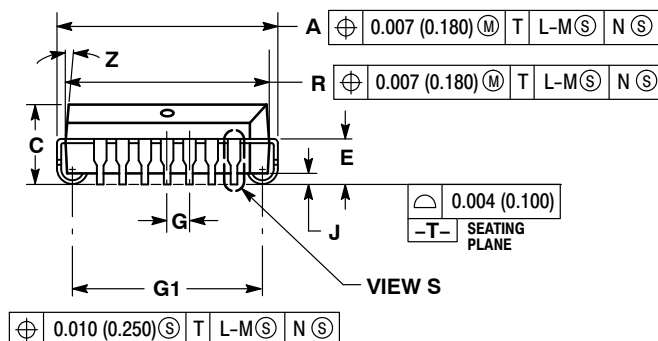
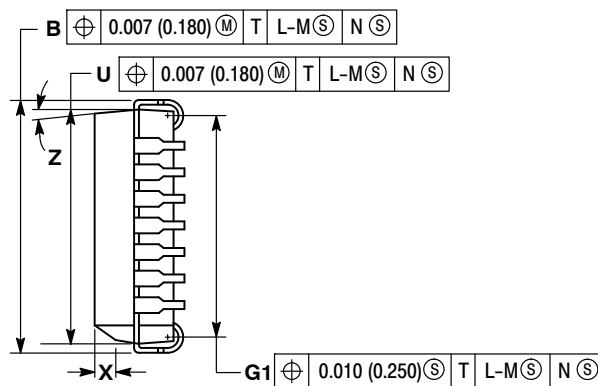
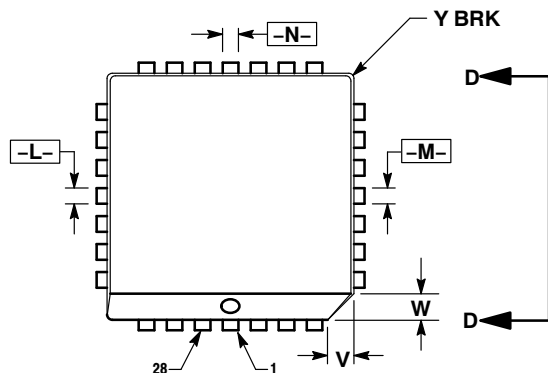
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SCALE 1:1

28 LEAD PLCC CASE 776-02 ISSUE G

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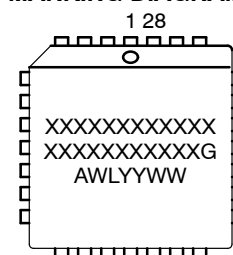


NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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