MC10E131, MC100E131

5 V ECL 4-Bit D Flip-Flop

Description

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

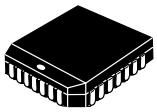
The 100 Series contains temperature compensation.

Features

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- PECL Mode Operating Range:
  - V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range:
  - V_{CC} = 0 V with V_{EE} = −4.2 V to −5.7 V
- Metastability Time Constant is 200 ps.
- Internal Input 50 kΩ Pulldown Resistors
- ESD Protection:
  - Human Body Model; > 2 kV
  - Machine Model; > 200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level: 3 (Pb-Free)
  - For Additional Information, see Application Note AND8003/D
- Flammability Rating:UL 94 V−0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 240 devices
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

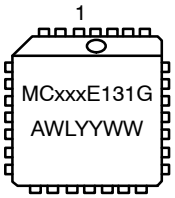
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PLCC−28
FN SUFFIX
CASE 776−02

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

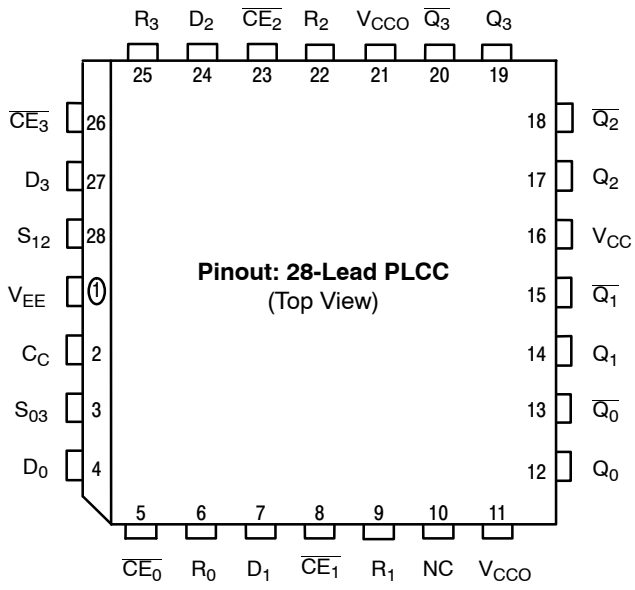
*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC10E131FNG	PLCC−28 (Pb-Free)	37 Units/Tube
MC10E131FNR2G	PLCC−28 (Pb-Free)	500/Tape & Reel
MC100E131FNG	PLCC−28 (Pb-Free)	37 Units/Tube
MC100E131FNR2G	PLCC−28 (Pb-Free)	500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. Pinout Diagram

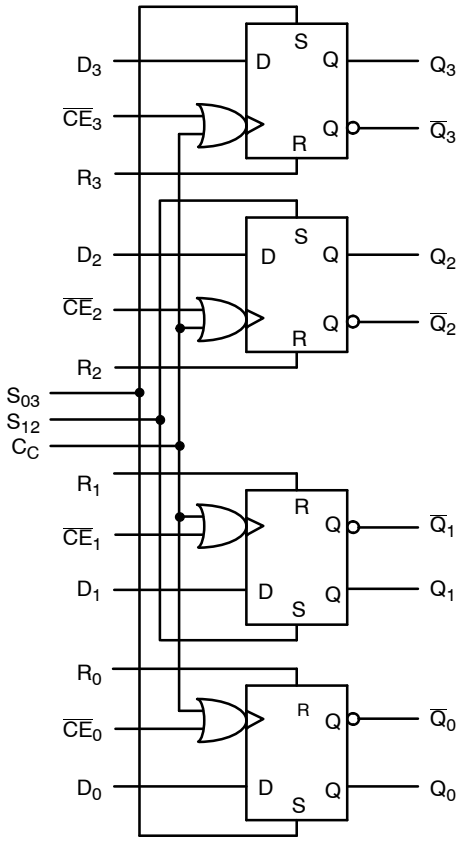


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D_0 – D_3	ECL Data Inputs
$\overline{CE}_0$ – $\overline{CE}_3$	ECL Clock Enables (Individual)
R_0 – R_3	ECL Resets
C_C	ECL Common Clock
S_{03}, S_{12}	ECL Sets (paired)
Q_0 – Q_3, $\overline{Q}_0$ – $\overline{Q}_3$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Table 2. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		−8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 −6	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	PLCC−28	63.5 43.5	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	PLCC−28	22 to 26	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. 10E SERIES PECL DC CHARACTERISTICS (V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1))

		−40°C			0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		58	70		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 2)				3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2)				3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage				3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage				3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			 350 450 300 150			 350 450 300 150			 350 450 300 150			 350 450 300 150	μA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 4. 10E SERIES NECL DC CHARACTERISTICS (V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 1))

		−40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		58	70		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 2)				−1020	−930	−840	−980	−895	−810	−910	−815	−720	mV
V_{OL}	Output LOW Voltage (Note 2)				−1950	−1790	−1630	−1950	−1790	−1630	−1950	−1773	−1595	mV
V_{IH}	Input HIGH Voltage				−1170	−1005	−840	−1130	−970	−810	−1060	−890	−720	mV
V_{IL}	Input LOW Voltage				−1950	−1715	−1480	−1950	−1715	−1480	−1950	−1698	−1445	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			 350 450 300 150			 350 450 300 150			 350 450 300 150			 350 450 300 150	μA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.06 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 5. 100E SERIES PECL DC CHARACTERISTICS (V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1))

		−40°C			0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		58	70		58	70		58	70		67	81	mA
V_{OH}	Output HIGH Voltage (Note 2)				3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2)				3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage		3975		3835	3975	4120	3835	3975	4120	3835	3975	4120	mV
V_{IL}	Input LOW Voltage		3355		3190	3355	3525	3190	3355	3525	3190	3355	3525	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			 350 450 300 150			 350 450 300 150			 350 450 300 150			 350 450 300 150	μA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 6. 100E SERIES NECL DC CHARACTERISTICS (V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 1))

Symbol	Characteristic	−40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		58	70		58	70		58	70		67	81	mA
V_{OH}	Output HIGH Voltage (Note 2)				−1025	−950	−880	−1025	−950	−880	−1025	−950	−880	mV
V_{OL}	Output LOW Voltage (Note 2)				−1810	−1705	−1620	−1810	−1745	−1620	−1810	−1740	−1620	mV
V_{IH}	Input HIGH Voltage		−1025		−1165	−1025	−880	−1165	−1025	−880	−1165	−1025	−880	mV
V_{IL}	Input LOW Voltage		−1645		−1810	−1645	−1475	−1810	−1645	−1475	−1810	−1645	−1475	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			 350 450 300 150			 350 450 300 150			 350 450 300 150			 350 450 300 150	μA
I_{IL}	Input LOW Current				0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary −0.46 V / +0.8 V.
2. Outputs are terminated through a 50 Ω resistor to V_{CC} − 2.0 V.

Table 7. AC CHARACTERISTICS (V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = −5.0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency	1100	1400		1100	1400		1100	1400		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output $\overline{CE}$ C_C R S	 310 275 400 300	 600 600 635 550	 750 725 875 775	 360 325 450 350	 500 500 640 550	 700 675 825 725	 360 325 450 350	 500 500 640 550	 700 675 825 725	ps
t_S	Setup Time (Note 2) D	200	20		150	20		150	20		ps
t_H	Hold Time (Note 2) D	225	−20		175	−20		175	−20		ps
t_{RR}	Reset Recovery Time	450	150		400	150		400	150		ps
t_{PW}	Minimum Pulse Width CLK R, S	 400 400			 400 400			 400 400			ps
t_{SKEW}	Within-Device Skew (Note 3)		60			60			60		ps
t_{JITTER}	Random Clock Jitter		< 1			< 1			< 1		ps
t_r/t_f	Rise/Fall Time (20−80%)	275	460	725	300	480		300	480	675	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. 10 Series: V_{EE} can vary −0.46 V / +0.06 V.
   100 Series: V_{EE} can vary −0.46 V / +0.8 V.
2. Setup/hold times guaranteed for both C_C and $\overline{CE}$.
3. Within-device skew is defined as identical transitions on similar paths through a device.

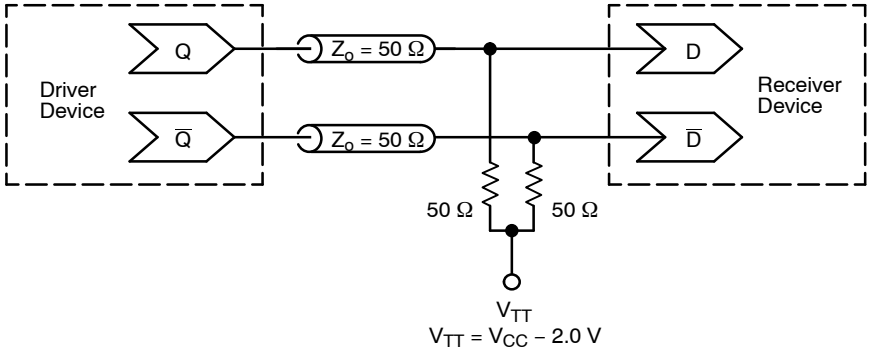


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

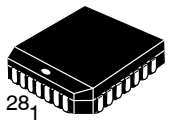
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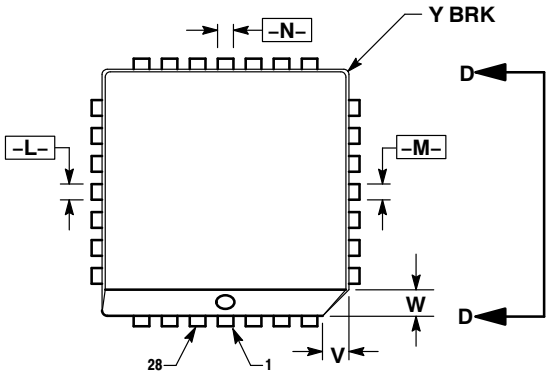
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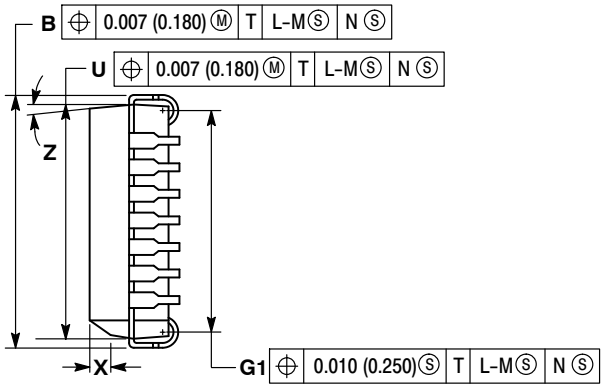
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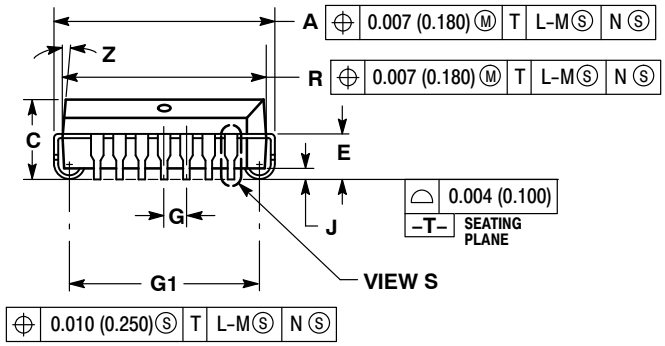


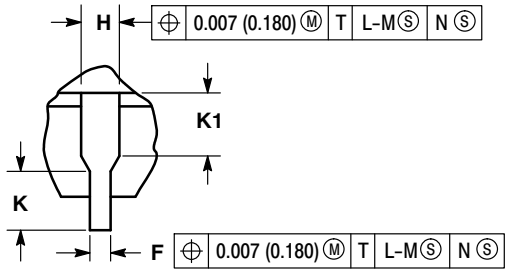
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VIEW D–D



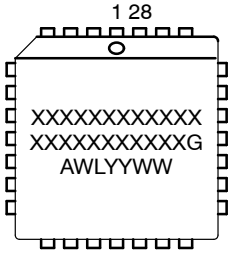


VIEW S

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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