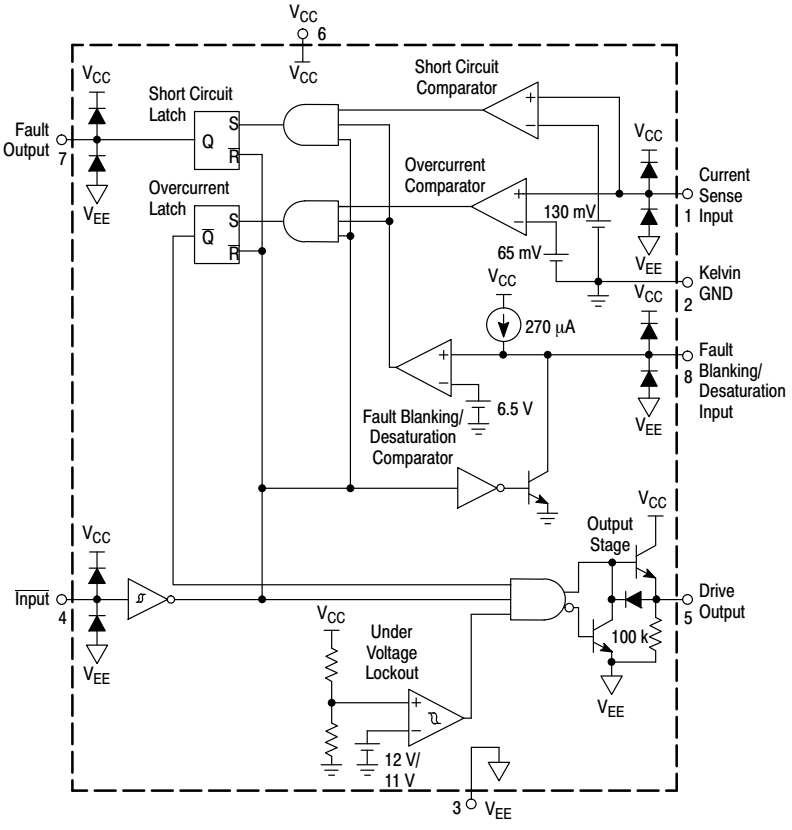
MC33153

Single IGBT Gate Driver

The MC33153 is specifically designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual−in−line and surface mount packages.

Features

- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors
- This is a Pb−Free and Halide−Free Device



This device contains 133 active transistors.

Figure 1. Representative Block Diagram

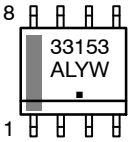
ON Semiconductor®

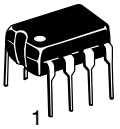
http://onsemi.com

MARKING DIAGRAMS

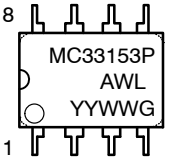


SOIC−8
D SUFFIX
CASE 751





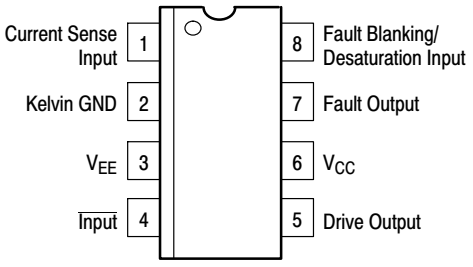
PDIP−8
P SUFFIX
CASE 626



A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
▪ or G	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC} to V_{EE} Kelvin Ground to V_{EE} (Note 1)	$V_{CC} - V_{EE}$ $KGND - V_{EE}$	20	V
Logic Input	V_{in}	V_{EE} −0.3 to V_{CC}	V
Current Sense Input	V_S	−0.3 to V_{CC}	V
Blanking/Desaturation Input	V_{BD}	−0.3 to V_{CC}	V
Gate Drive Output Source Current Sink Current Diode Clamp Current	I_O	 1.0 2.0 1.0	A
Fault Output Source Current Sink Current	I_{FO}	 25 10	mA
Power Dissipation and Thermal Characteristics D Suffix SO−8 Package, Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air P Suffix DIP−8 Package, Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−40 to +105	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Electrostatic Discharge Sensitivity (ESD) (Note 2) Human Body Model (HBM) Machine Model (MM) Charged Device Model (CDM)	ESD	 2500 250 1500	V

NOTE: ESD data available upon request.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. ESD protection per JEDEC Standard JESD22−A114−F for HBM
   per JEDEC Standard JESD22−A115−A for MM
   per JEDEC Standard JESD22−C101D for CDM.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT					
Input Threshold Voltage High State (Logic 1) Low State (Logic 0)	 V_{IH} V_{IL}	 − 1.2	 2.70 2.30	 3.2 −	V
Input Current High State (V_{IH} = 3.0 V) Low State (V_{IL} = 1.2 V)	 I_{IH} I_{IL}	 − −	 130 50	 500 100	μA
DRIVE OUTPUT					
Output Voltage Low State (I_{Sink} = 1.0 A) High State (I_{Source} = 500 mA)	 V_{OL} V_{OH}	 − 12	 2.0 13.9	 2.5 −	V
Output Pull−Down Resistor	R_{PD}	−	100	200	kΩ
FAULT OUTPUT					
Output Voltage Low State (I_{Sink} = 5.0 mA) High State (I_{Source} = 20 mA)	 V_{FL} V_{FH}	 − 12	 0.2 13.3	 1.0 −	V

3. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
   T_{low} = −40°C for MC33153 T_{high} = +105°C for MC33153

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin GND connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 1.0 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH(in/out)}$ $t_{PHL\ (in/out)}$	 – –	 80 120	 300 300	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	17	55	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	17	55	ns
Propagation Delay Current Sense Input to Drive Output Fault Blanking/Desaturation Input to Drive Output	$t_{P(OC)}$ $t_{P(FLT)}$	–	0.3	1.0	μs
UVLO					
Startup Voltage	$V_{CC\ start}$	11.3	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	11.7	V
COMPARATORS					
Overcurrent Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Circuit Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Fault Blanking/Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Current Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	μA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} = 0 V)	I_{chg}	–200	–270	–300	μA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 5.0 V)	I_{dschg}	1.0	2.5	–	mA
TOTAL DEVICE					
Power Supply Current Standby ($V_{Pin\ 4}$ = V_{CC}, Output Open) Operating (C_L = 1.0 nF, f = 20 kHz)	I_{CC}	 – –	 7.2 7.9	 14 20	mA

4. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
   T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

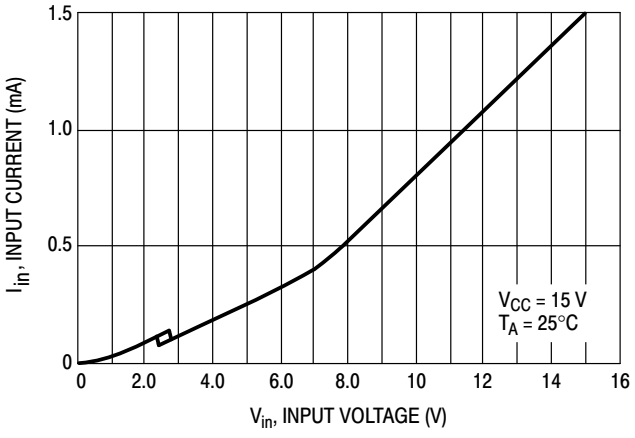


Figure 2. Input Current versus Input Voltage

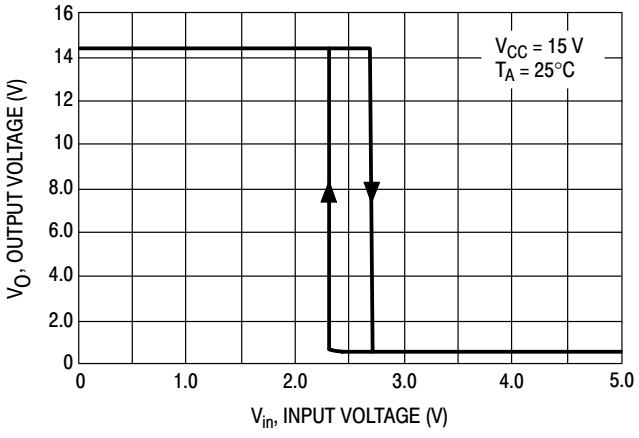


Figure 3. Output Voltage versus Input Voltage

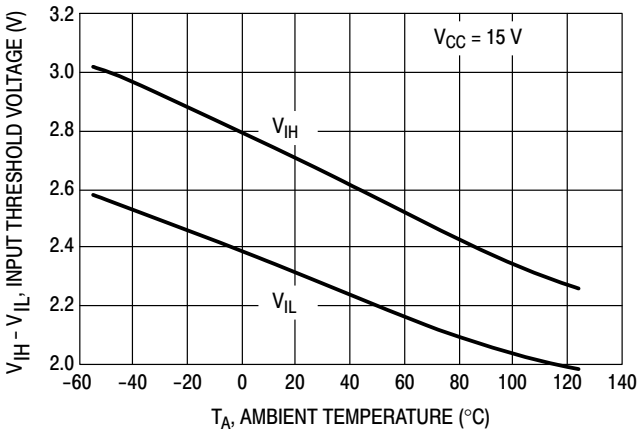


Figure 4. Input Threshold Voltage versus Temperature

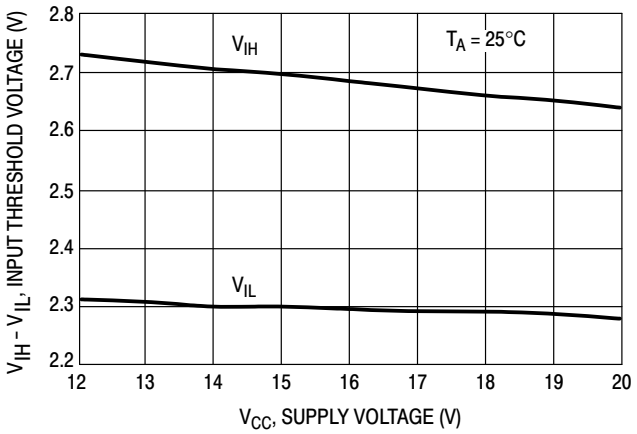


Figure 5. Input Threshold Voltage versus Supply Voltage

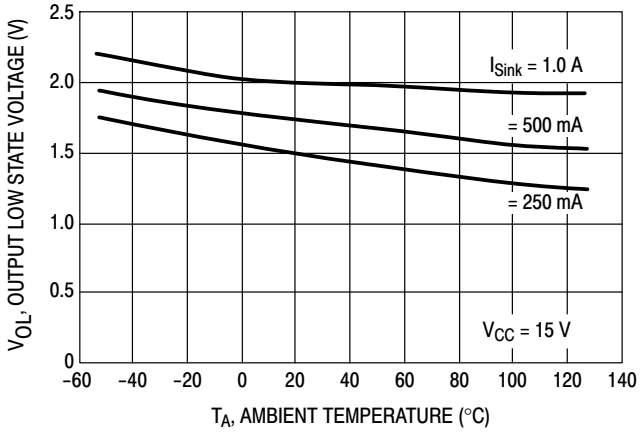


Figure 6. Drive Output Low State Voltage versus Temperature

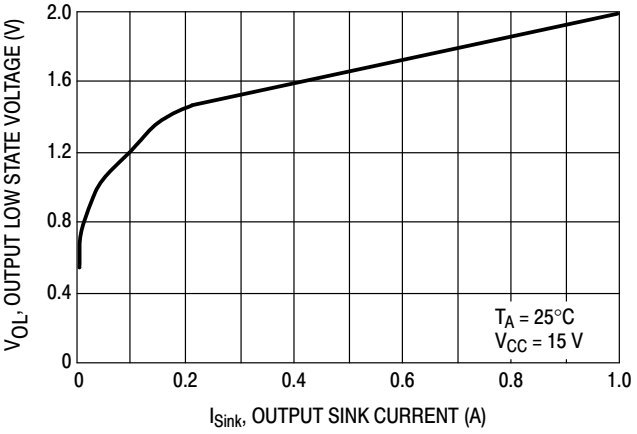


Figure 7. Drive Output Low State Voltage versus Sink Current

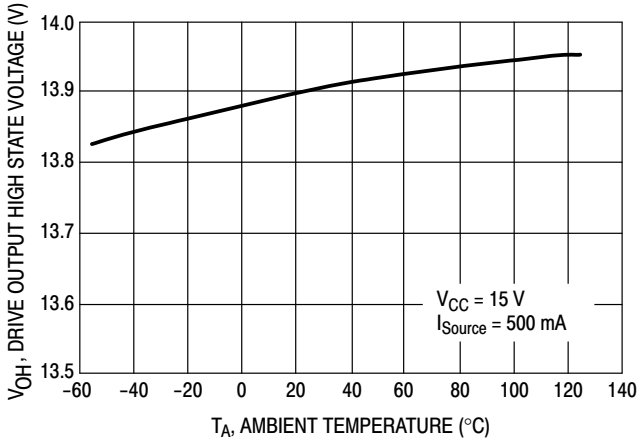


Figure 8. Drive Output High State Voltage versus Temperature

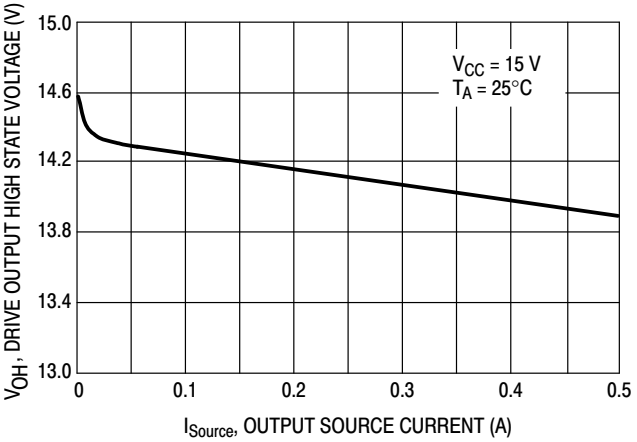


Figure 9. Drive Output High State Voltage versus Source Current

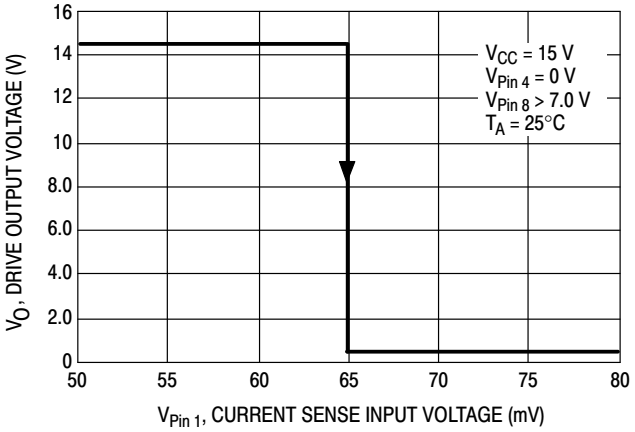


Figure 10. Drive Output Voltage versus Current Sense Input Voltage

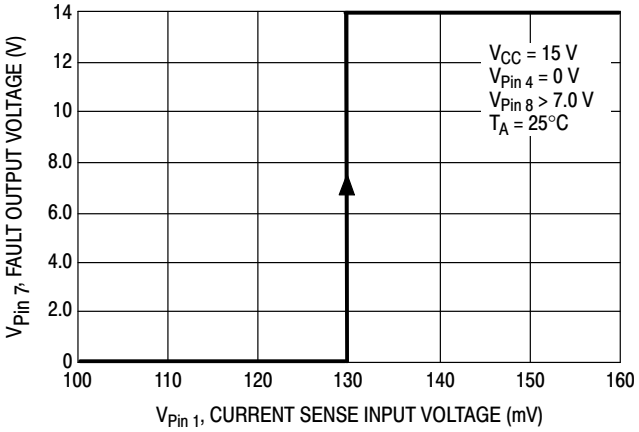


Figure 11. Fault Output Voltage versus Current Sense Input Voltage

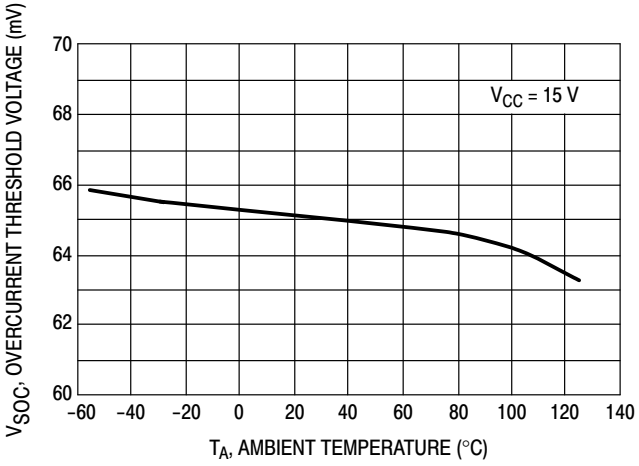


Figure 12. Overcurrent Protection Threshold Voltage versus Temperature

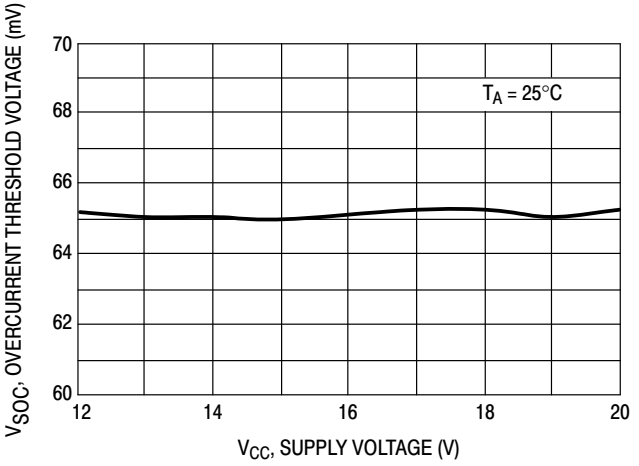


Figure 13. Overcurrent Protection Threshold Voltage versus Supply Voltage

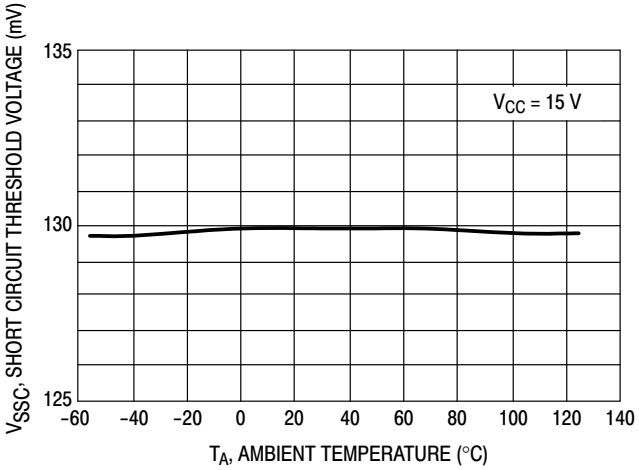


Figure 14. Short Circuit Comparator Threshold Voltage versus Temperature

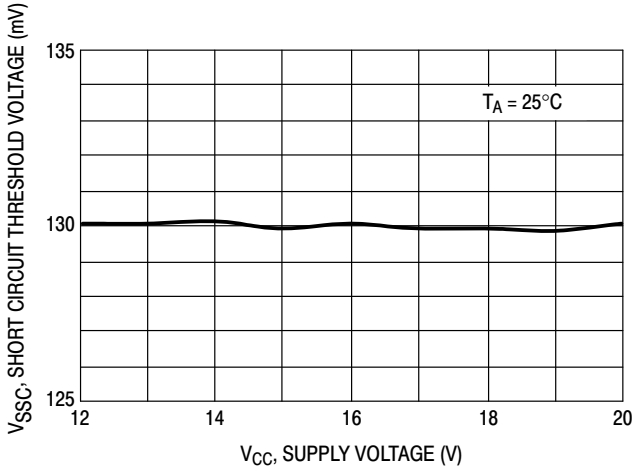


Figure 15. Short Circuit Comparator Threshold Voltage versus Supply Voltage

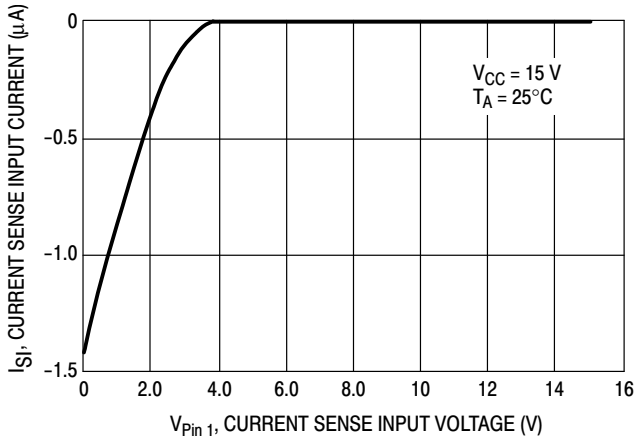


Figure 16. Current Sense Input Current versus Voltage

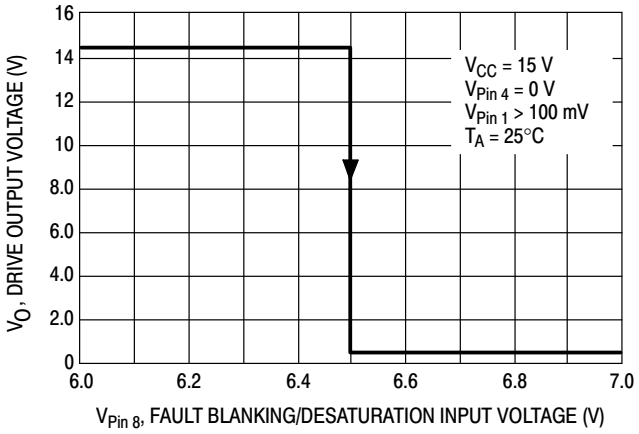


Figure 17. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage

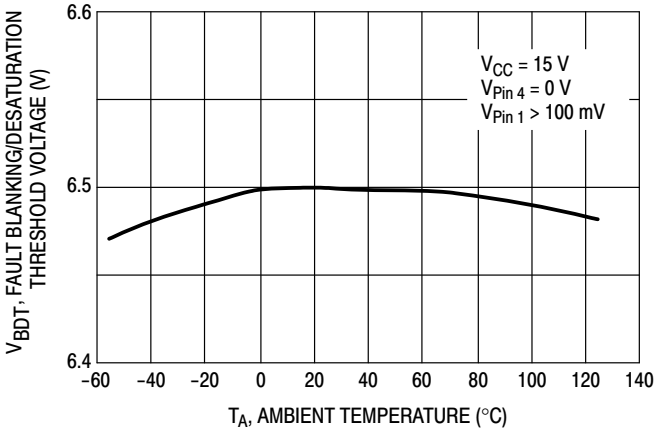


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature

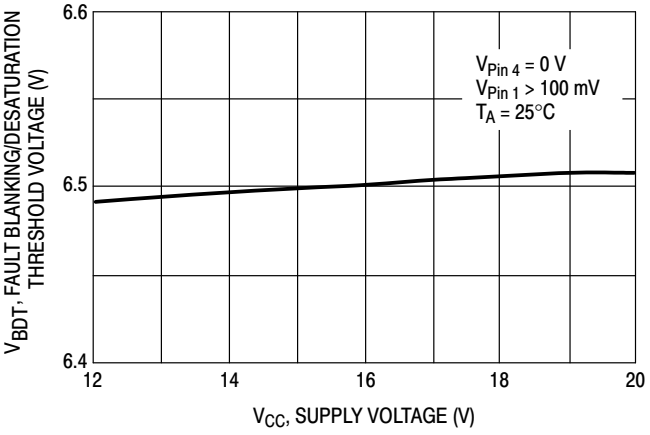


Figure 19. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage

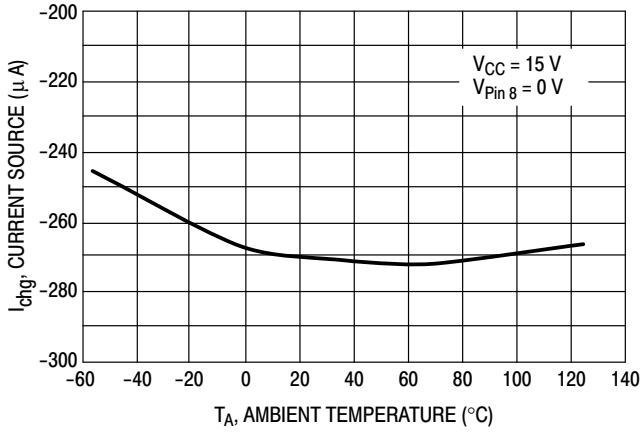


Figure 20. Fault Blanking/Desaturation Current Source versus Temperature

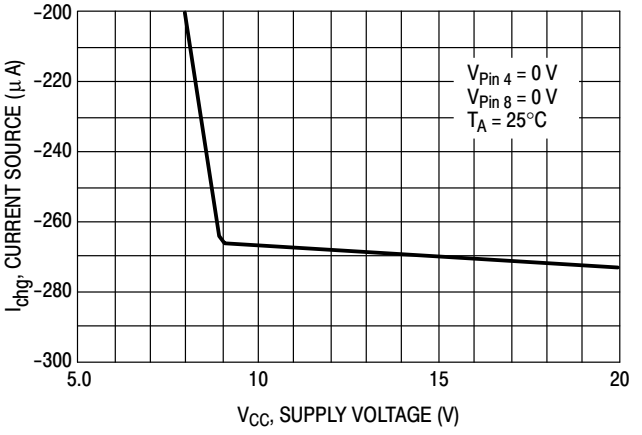


Figure 21. Fault Blanking/Desaturation Current Source versus Supply Voltage

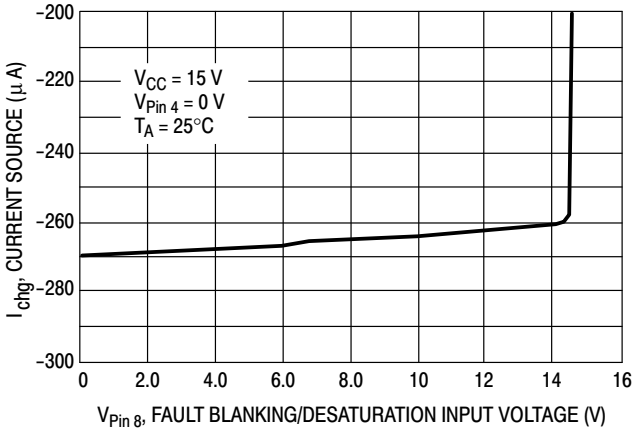


Figure 22. Fault Blanking/Desaturation Current Source versus Input Voltage

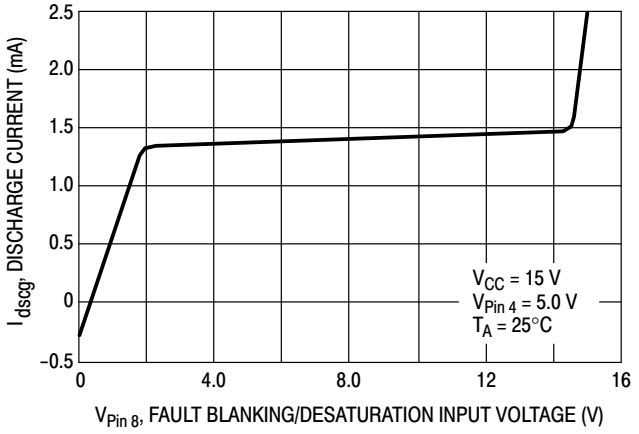


Figure 23. Fault Blanking/Desaturation Discharge Current versus Input Voltage

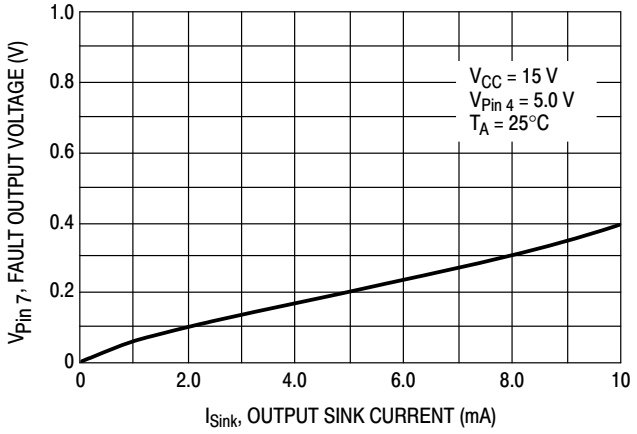


Figure 24. Fault Output Low State Voltage versus Sink Current

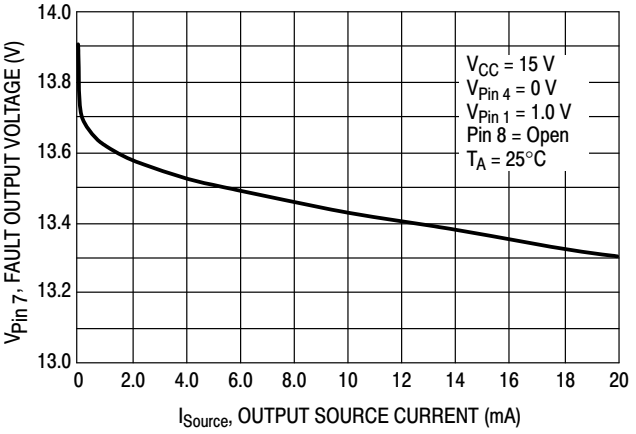


Figure 25. Fault Output High State Voltage versus Source Current

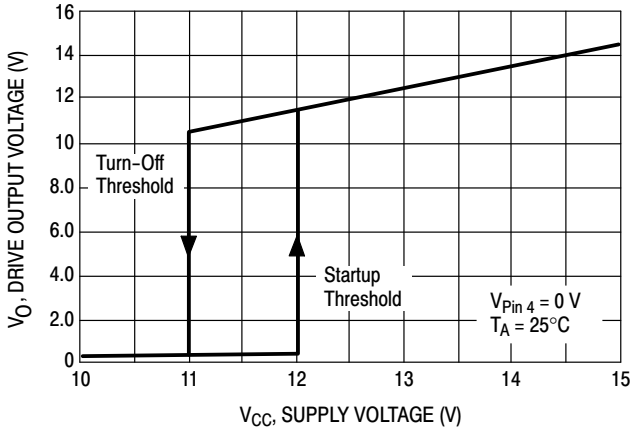


Figure 26. Drive Output Voltage versus Supply Voltage

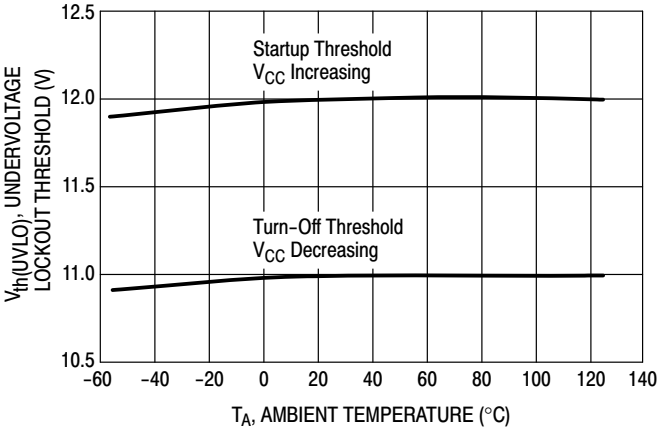


Figure 27. UVLO Thresholds versus Temperature

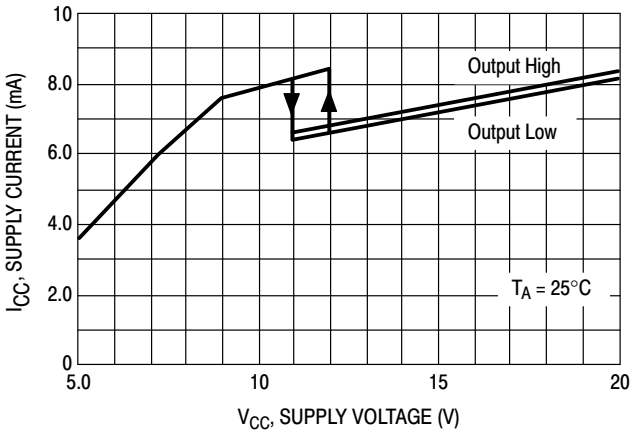


Figure 28. Supply Current versus Supply Voltage

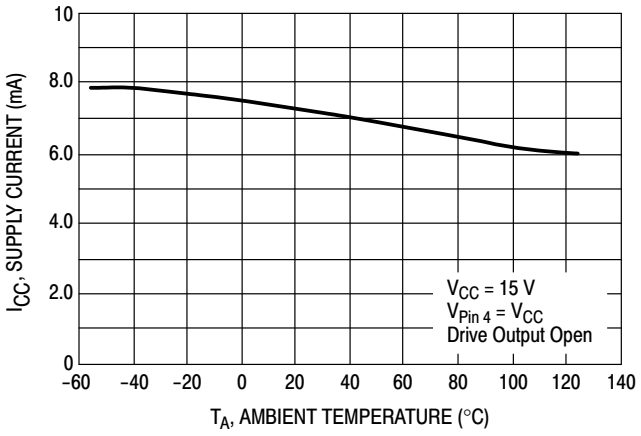


Figure 29. Supply Current versus Temperature

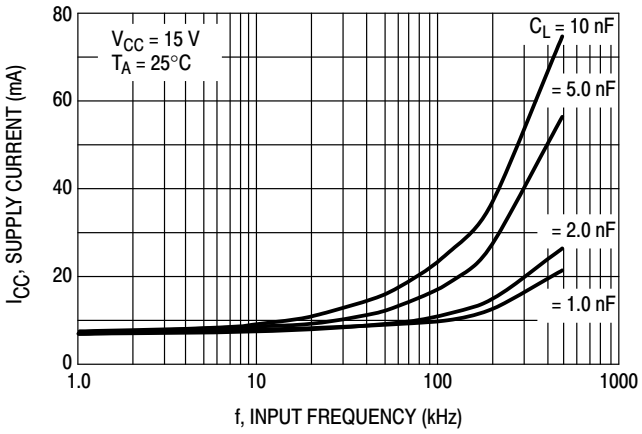


Figure 30. Supply Current versus Input Frequency

OPERATING DESCRIPTION

GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn−on, turn−off and off−state impedance. A single resistor may be used to control both turn−on and turn−off as shown in Figure 31. However, the resistor value selected must be a compromise in turn−on abruptness and turn−off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 32. This circuit allows turn−on and turn−off to be optimized separately. The turn−on resistor, R_{on}, provides control over the IGBT turn−on speed. In motor control circuits, the resistor sets the turn−on di/dt that controls how fast the free−wheel diode is cleared. The interaction of the IGBT and free−wheeling diode determines the turn−on dv/dt. Excessive turn−on dv/dt is a common problem in half−bridge circuits. The turn−off resistor, R_{off}, controls the turn−off speed and ensures that the IGBT remains off under commutation stresses. Turn−off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn−off losses. This is particularly true for fast IGBTs. It is also possible to turn−off an IGBT too fast. Excessive turn−off speed will result in large overshoot voltages. Normally, the turn−off resistor is a small fraction of the turn−on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient V_{CC} to the MC33153.

In a PWM inverter, IGBTs are used in a half−bridge configuration. Thus, at least one device is always off. While

the IGBT is in the off−state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn−on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot−through currents, it is necessary to provide a low sink impedance to the device that is in the off−state. In most applications the turn−off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn−off speeds.

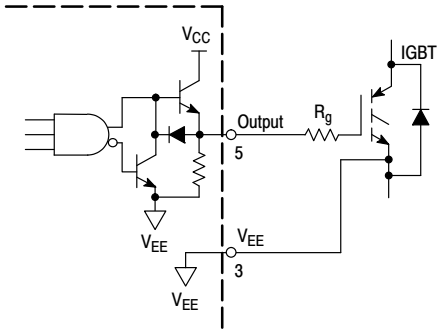


Figure 31. Using a Single Gate Resistor

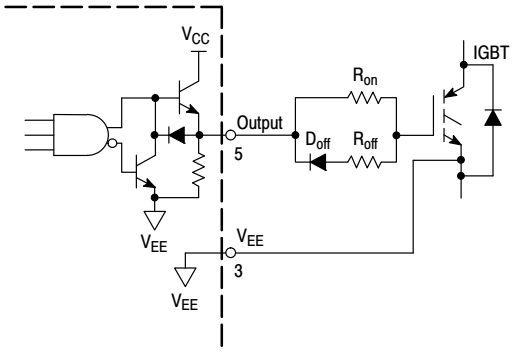


Figure 32. Using Separate Resistors for Turn−On and Turn−Off

A negative bias voltage can be used to drive the IGBT into the off−state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot−through. The MC33153 has separate pins for V_{EE} and Kelvin Ground. This permits operation using a +15/−5.0 V supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn−on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open−collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pullup resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 33.

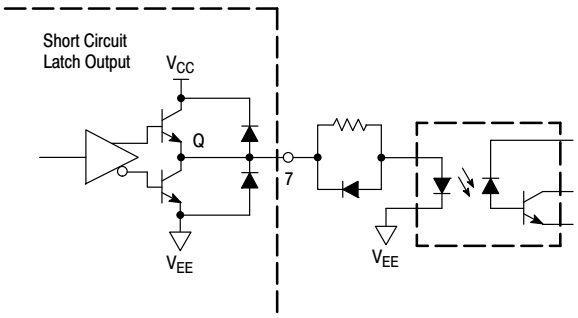


Figure 33. Output Fault Optoisolator

UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on−voltage. At gate voltages below 13 V, the on−voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V. The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11 V.

PROTECTION CIRCUITRY

Desaturation Protection

Bipolar Power circuits have commonly used what is known as "Desaturation Detection". This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in

saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain (h_{FE}) of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is “on” and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is “off”, the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V, allowing a maximum on−voltage of about 5.8 V.

A fault exists when the gate input is high and V_{CE} is greater than the maximum allowable $V_{CE(sat)}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn−off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to V_{CC}.

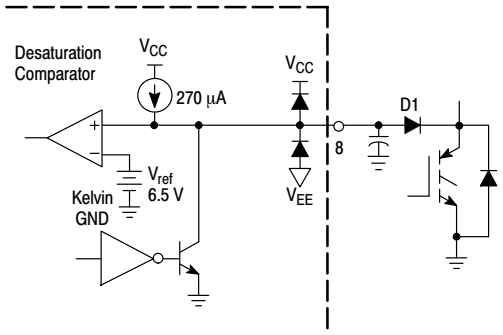


Figure 34. Desaturation Detection

The MC33153 also features a programmable fault blanking time. During turn−on, the IGBT must clear the opposing free−wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared, the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn−on, there is normally considerable ringing on the collector due to the C_{OSS} capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn “off”, allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on−voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on−resistance, sense IGBTs behave much like low−on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires fault blanking to prevent false tripping during turn−on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn−on and turn−off due to the collector to mirror capacitance. With non−sensing types of IGBTs, a low resistance current shunt (5.0 to 50 mΩ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on−time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned−off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

APPLICATION INFORMATION

Figure 35 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and V_{EE} pins should be connected together. Separate gate resistors are recommended to optimize the turn−on and turn−off drive.

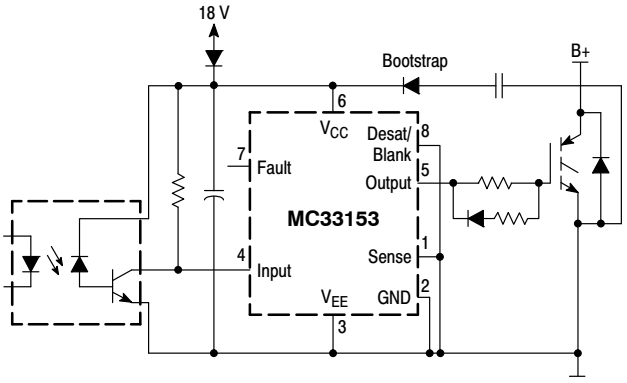


Figure 35. Basic Application

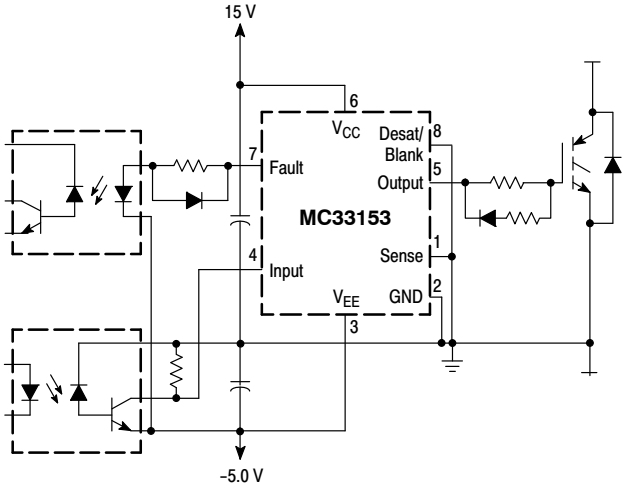


Figure 36. Dual Supply Application

When used in a dual supply application as in Figure 36, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to V_{EE}.

If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free−wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.

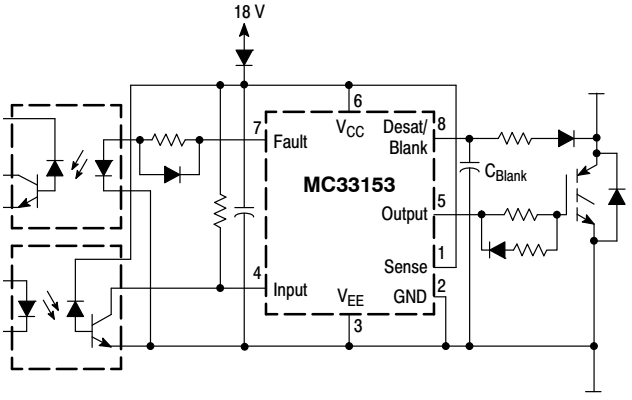


Figure 37. Desaturation Application

When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.

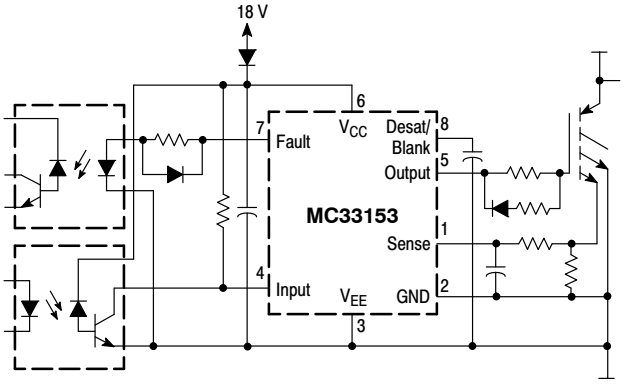


Figure 38. Sense IGBT Application

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
MC33153DG	T_A = −40° to +105°C	SOIC−8 (Pb−Free)	98 Units / Rail
MC33153DR2G		SOIC−8 (Pb−Free)	1000 / Tape & Reel
MC33153PG		PDIP−8 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

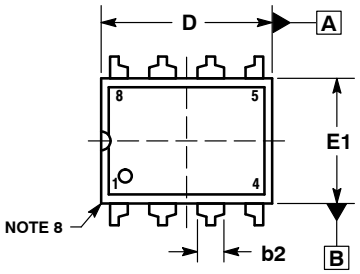
ON Semiconductor®



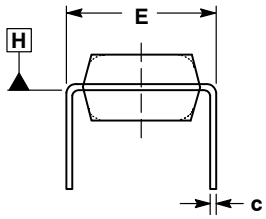
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

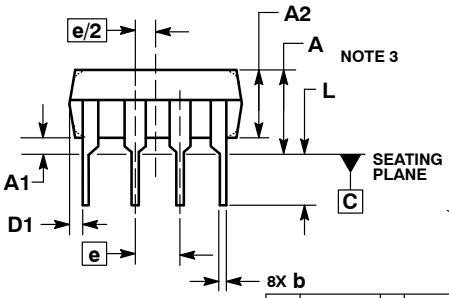
DATE 22 APR 2015



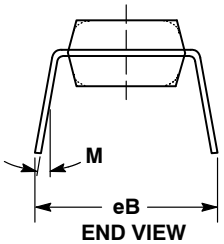
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



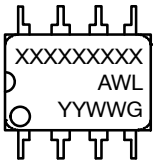
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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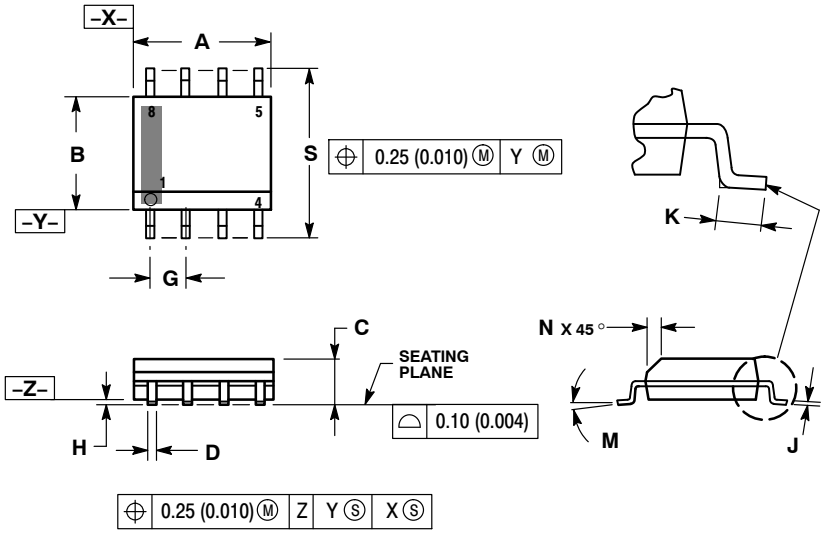
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

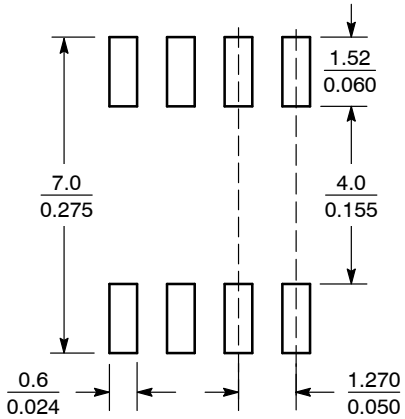
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

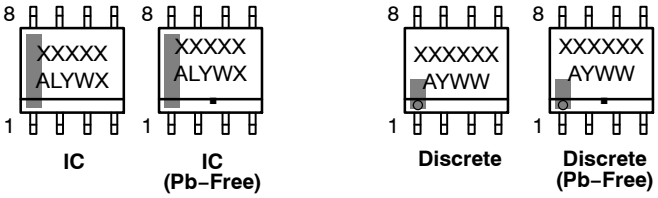
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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