# MC74AC259, MC74ACT259

## 8-Bit Addressable Latch

The MC74AC259/74ACT259 is a high−speed 8−bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1−of−8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the ALS259 8−bit addressable latch.

- Serial−to−Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear
- These are Pb−Free Devices

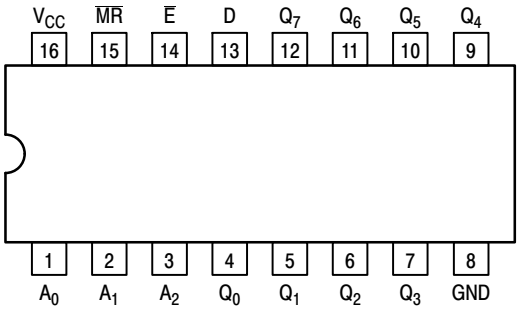



**Figure 1. Pinout: 16−Lead Packages Conductors**
(Top View)

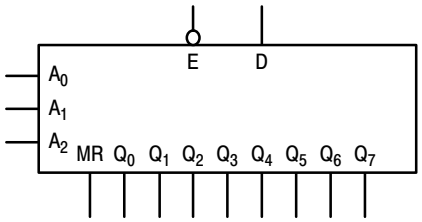



**Figure 2. Logic Symbol**

**MODE SELECT TABLE**

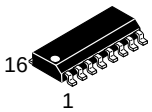
| $\overline{E}$ | $\overline{MR}$ | Mode |
|---|---|---|
| L | H | Addressable Latch |
| H | H | Memory |
| L | L | Active HIGH 8−Channel Demultiplexer |
| H | L | Clear |

H = HIGH Voltage Level
L = LOW Voltage Level

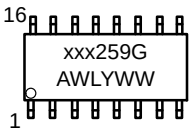
ON Semiconductor®

www.onsemi.com

**MARKING DIAGRAM**




**SOIC−16**
**D SUFFIX**
**CASE 751B**




| | |
|---|---|
| xxx | = AC or ACT |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

© Semiconductor Components Industries, LLC, 2015

**MODE SELECT−FUNCTION TABLE**

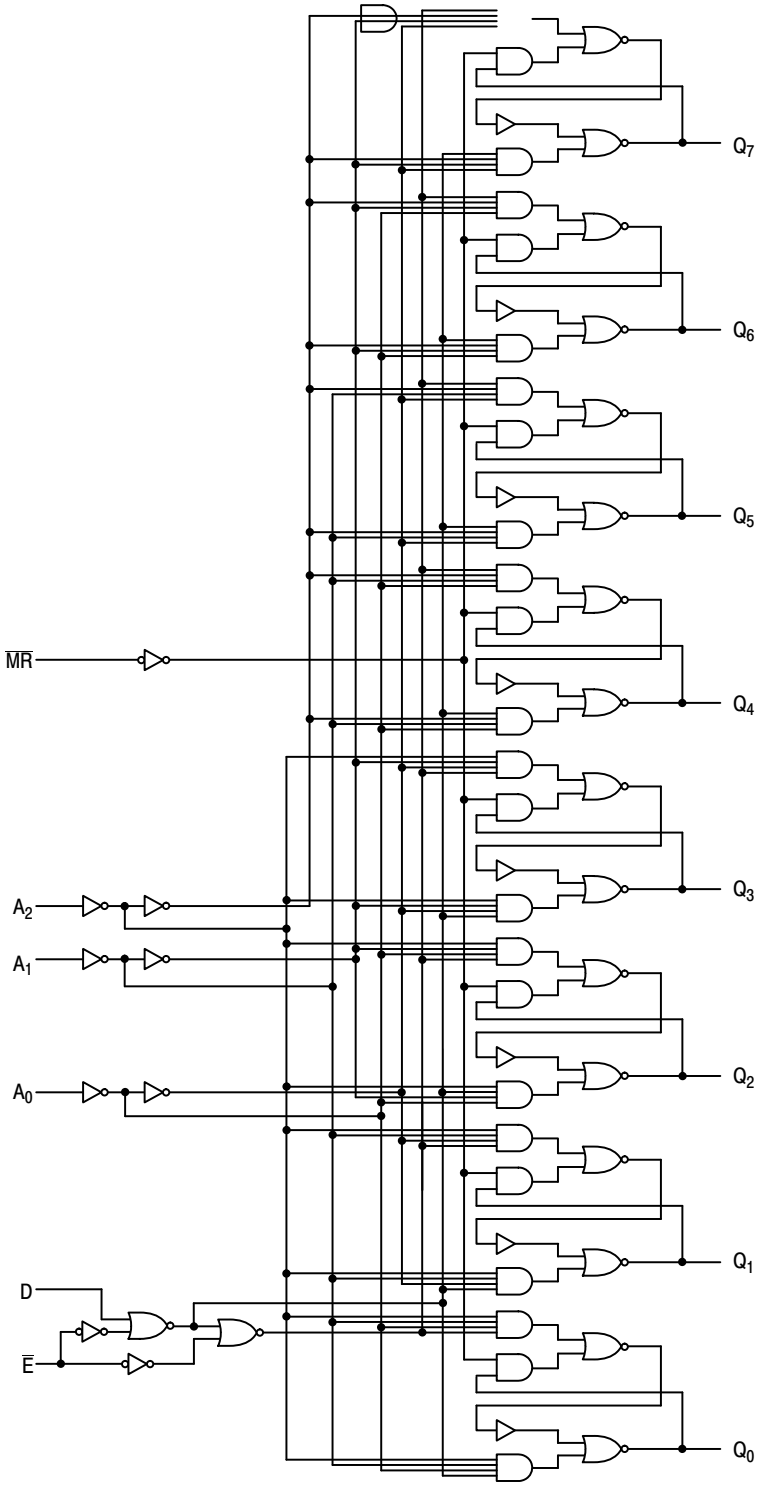
| Operating Mode | Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{E}$ | D | $A_0$ | $A_1$ | $A_2$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ |
| Master Reset | L | H | X | X | X | X | L | L | L | L | L | L | L | L |
| Demultiplex (Active HIGH Decoder when D = H) | L | L | d | L | L | L | Q = d | L | L | L | L | L | L | L |
| | L | L | d | H | L | L | L | Q = d | L | L | L | L | L | L |
| | L | L | d | L | H | L | L | L | Q = d | L | L | L | L | L |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | L | L | d | H | H | H | L | L | L | L | L | L | L | Q = d |
| Store (Do Nothing) | H | H | X | X | X | X | $q_0$ | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| Addressable Latch | H | L | d | L | L | L | Q = d | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | H | L | d | H | L | L | $q_0$ | Q = d | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | H | L | d | L | H | L | $q_0$ | $q_1$ | Q = d | $q_3$ | $q_4$ | $q_5$ | $q_6$ | $q_7$ |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | • | • | • | • | • | • | • | • | • | • | • | • | • | • |
| | H | L | d | H | H | H | $q_0$ | $q_1$ | $q_2$ | $q_3$ | $q_4$ | $q_5$ | $q_6$ | Q = d |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW−to−HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

## FUNCTIONAL DESCRIPTION

The MC74AC259/74ACT259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non−addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one−of−eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC74AC/ACT259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Mode Select Function Table summarizes the operations of the MC74AC/ACT259.




NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | −0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | $-0.5 \le V_{CC} +0.5$ | V |
| $V_O$ | DC Output Voltage (Note 1) | $-0.5 \le V_{CC} +0.5$ | V |
| $I_{IK}$ | DC Input Diode Current | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | ±50 | mA |
| $I_O$ | DC Output Sink/Source Current | ±50 | mA |
| $I_{CC}$ | DC Supply Current per Output Pin | ±50 | mA |
| $I_{GND}$ | DC Ground Current per Output Pin | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| $T_J$ | Junction temperature under Bias | +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | 69.1 | °C/W |
| $P_D$ | Power Dissipation in Still Air at 65°C (Note 3) | 500 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| $F_R$ | Flammability Rating Oxygen Index: 30% − 35% | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage Human Body Model (Note 4)<br>Machine Model (Note 5)<br>Charged Device Model (Note 6) | > 2000<br>> 200<br>> 1000 | V |
| $I_{Latch-Up}$ | Latch−Up Performance Above $V_{CC}$ and Below GND at 85°C (Note 7) | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_O$ absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD51−7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/ from 65°C to 85°C.
4. Tested to EIA/JESD22−A114−A.
5. Tested to EIA/JESD22−A115−A.
6. Tested to JESD22−C101−A.
7. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | ′AC | 2.0 | 5.0 | 6.0 | V |
| | | ′ACT | 4.5 | 5.0 | 5.5 | |
| $V_{IN}$, $V_{OUT}$ | DC Input Voltage, Output Voltage (Ref. to GND) | | 0 | − | $V_{CC}$ | V |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 1)<br>′AC Devices except Schmitt Inputs | $V_{CC}$ @ 3.0 V | − | 150 | − | ns/V |
| | | $V_{CC}$ @ 4.5 V | − | 40 | − | |
| | | $V_{CC}$ @ 5.5 V | − | 25 | − | |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 2)<br>′ACT Devices except Schmitt Inputs | $V_{CC}$ @ 4.5 V | − | 10 | − | ns/V |
| | | $V_{CC}$ @ 5.5 V | − | 8.0 | − | |
| $T_A$ | Operating Ambient Temperature Range | | −40 | 25 | 85 | °C |
| $I_{OH}$ | Output Current − High | | − | − | −24 | mA |
| $I_{OL}$ | Output Current − Low | | − | − | 24 | mA |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. $V_{IN}$ from 30% to 70% $V_{CC}$; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. $V_{IN}$ from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

## DC CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | 74AC $T_A$ = +25°C | 74AC $T_A$ = −40°C to +85°C | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75 | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ − 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75 | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ − 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49 | 2.9<br>4.4<br>5.4 | 2.9<br>4.4<br>5.4 | V | $I_{OUT}$ = −50 μA |
| | | 3.0<br>4.5<br>5.5 | −<br>−<br>− | 2.56<br>3.86<br>4.86 | 2.46<br>3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>−12 mA<br>$I_{OH}$ −24 mA<br>−24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0<br>4.5<br>5.5 | −<br>−<br>− | 0.36<br>0.36<br>0.36 | 0.44<br>0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>12 mA<br>$I_{OL}$ 24 mA<br>24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | − | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | − | − | 75 | mA | $V_{OLD}$ = 1.65 V Max |
| $I_{OHD}$ | | 5.5 | − | − | −75 | mA | $V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | − | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: $I_{IN}$ and $I_{CC}$ @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V $V_{CC}$.

**AC CHARACTERISTICS** (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C, $C_L$ = 50 pF | | | 74AC $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay<br>$D_n$ to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 9.0<br>6.5 | 14.5<br>10.0 | 1.5<br>1.5 | 17.0<br>11.5 | ns | 3−5 |
| $t_{PHL}$ | Propagation Delay<br>$D_n$ to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 9.0<br>6.0 | 13.5<br>9.5 | 1.5<br>1.5 | 16.0<br>11.0 | ns | 3−5 |
| $t_{PLH}$ | Propagation Delay<br>$\overline{E}$ to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 10.5<br>7.0 | 15.0<br>10.5 | 1.5<br>1.5 | 17.5<br>12.5 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay<br>$\overline{E}$ to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 8.0<br>7.5 | 12.5<br>9.0 | 1.5<br>1.5 | 15.0<br>11.0 | ns | 3−6 |
| $t_{PLH}$ | Propagation Delay<br>Address to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 12.0<br>8.0 | 19.0<br>13.0 | 1.5<br>1.5 | 22.5<br>15.5 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay<br>Address to $Q_n$ | 3.3<br>5.0 | 2.0<br>2.0 | 10.0<br>7.0 | 16.0<br>11.0 | 1.5<br>1.5 | 19.0<br>13.0 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to Q | 3.3<br>5.0 | 2.0<br>2.0 | 8.0<br>6.0 | 12.0<br>9.0 | 1.5<br>1.5 | 13.5<br>10.0 | ns | 3−7 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

**AC OPERATING REQUIREMENTS**

| Symbol | Parameter | $V_{CC}$* (V) | 74AC $T_A$ = +25°C, $C_L$ = 50 pF | | 74AC $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | |
| $t_s$ | Setup Time, HIGH or LOW<br>$D_n$ to $\overline{E}$ | 3.3<br>5.0 | −<br>− | 3.5<br>2.5 | 4.5<br>3.5 | ns | 3−9 |
| $t_h$ | Hold Time, HIGH or LOW<br>$D_n$ to $\overline{E}$ | 3.3<br>5.0 | −<br>− | 2.5<br>2.0 | 2.5<br>2.0 | ns | 3−9 |
| $t_s$ | Setup Time<br>Address to $\overline{E}$ | 3.3<br>5.0 | −<br>− | 7.0<br>4.0 | 9.0<br>6.0 | ns | 3−6 |
| $t_h$ | Hold Time<br>Address to $\overline{E}$ | 3.3<br>5.0 | −<br>− | 2.0<br>2.0 | 2.0<br>2.0 | ns | 3−6 |
| $t_w$ | Minimum Pulse<br>Width $\overline{M}$R | 3.3<br>5.0 | −<br>− | 6.0<br>5.5 | 6.5<br>6.0 | ns | 3−6 |
| $t_w$ | Minimum Pulse<br>Width $\overline{E}$ | 3.3<br>5.0 | −<br>− | 6.5<br>5.5 | 7.0<br>6.0 | ns | 3−6 |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## DC CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | 74ACT $T_A$ = +25°C | 74ACT $T_A$ = −40°C to +85°C | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ − 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V | $V_{OUT}$ = 0.1 V<br>or $V_{CC}$ − 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V | $I_{OUT}$ = −50 μA |
| | | 4.5<br>5.5 | −<br>− | 3.86<br>4.86 | 3.76<br>4.76 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OH}$ −24 mA<br>$I_{OH}$ −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V | $I_{OUT}$ = 50 μA |
| | | 4.5<br>5.5 | −<br>− | 0.36<br>0.36 | 0.44<br>0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$<br>$I_{OL}$ 24 mA<br>$I_{OL}$ 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | − | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $\Delta I_{CCT}$ | Additional Max. $I_{CC}$/Input | 5.5 | 0.6 | − | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1 V |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 5.5 | − | − | 75 | mA | $V_{OLD}$ = 1.65 V Max |
| $I_{OHD}$ | | 5.5 | − | − | −75 | mA | $V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | − | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS (For Figures and Waveforms − See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C, $C_L$ = 50 pF | | | 74ACT $T_A$ = −40°C to +85°C, $C_L$ = 50 pF | | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay $D_n$ to $Q_n$ | 5.0 | 2.0 | 6.5 | 11.0 | 1.5 | 12.5 | ns | 3−5 |
| $t_{PHL}$ | Propagation Delay $D_n$ or $Q_n$ | 5.0 | 2.0 | 7.0 | 10.5 | 1.5 | 12.0 | ns | 3−5 |
| $t_{PLH}$ | Propagation Delay $\overline{E}$ to $Q_n$ | 5.0 | 2.0 | 10.5 | 14.0 | 1.5 | 16.5 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay $\overline{E}$ or $Q_n$ | 5.0 | 2.0 | 9.0 | 12.0 | 1.5 | 14.0 | ns | 3−6 |
| $t_{PLH}$ | Propagation Delay Address to $Q_n$ | 5.0 | 2.0 | 8.0 | 11.5 | 1.5 | 13.5 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay Address to $Q_n$ | 5.0 | 2.0 | 6.0 | 10.0 | 1.5 | 12.0 | ns | 3−6 |
| $t_{PHL}$ | Propagation Delay $\overline{MR}$ to Q | 5.0 | 2.0 | | 10.0 | 1.5 | 11.0 | ns | 3−7 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## AC OPERATING REQUIREMENTS

| Symbol | Parameter | $V_{CC}$* (V) | 74ACT $T_A$ = +25°C $C_L$ = 50 pF | | 74ACT $T_A$ = −40°C to +85°C $C_L$ = 50 pF | Unit | Fig. No. |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Minimum | | | |
| $t_s$ | Setup Time, HIGH or LOW $D_n$ to $\overline{E}$ | 5.0 | − | 3.0 | 4.0 | ns | 3−9 |
| $t_h$ | Hold Time, HIGH or LOW $D_n$ to $\overline{E}$ | 5.0 | − | 2.5 | 2.5 | ns | 3−9 |
| $t_s$ | Setup Time Address to $\overline{E}$ | 5.0 | − | 4.5 | 6.5 | ns | 3−6 |
| $t_h$ | Hold Time Address to $\overline{E}$ | 5.0 | − | 2.5 | 2.5 | ns | 3−6 |
| $t_w$ | Minimum Pulse Width $\overline{MR}$ | 5.0 | − | 7.0 | 7.5 | ns | 3−6 |
| $t_w$ | Minimum Pulse Width $\overline{E}$ | 5.0 | − | 7.0 | 7.5 | ns | 3−6 |

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

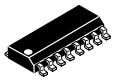
## CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 50.0 | pF | $V_{CC}$ = 5.0 V |

## ORDERING INFORMATION

| Part Number | Package | Shipping† |
|---|---|---|
| MC74AC259DG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74AC259DR2G | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |
| MC74ACT259DG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74ACT259DR2G | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |

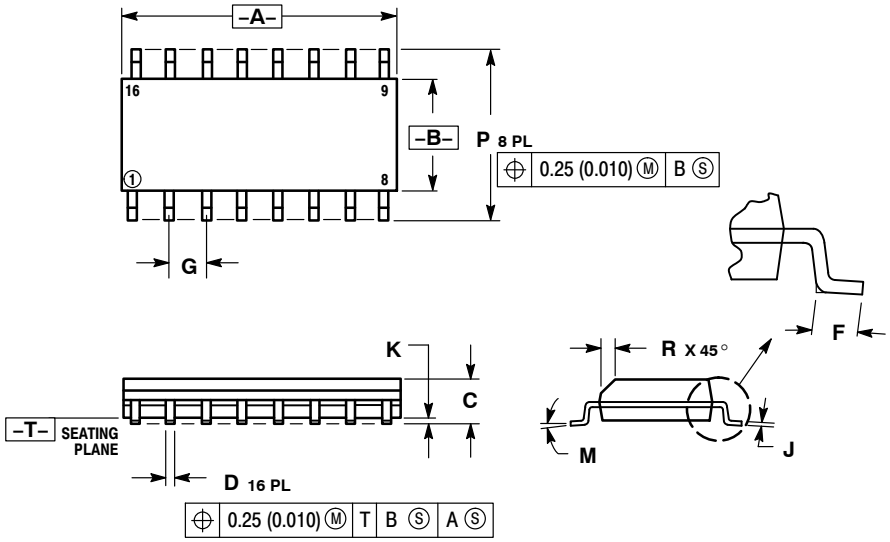
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

**SOIC–16**
CASE 751B–05
ISSUE K

DATE 29 DEC 2006




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

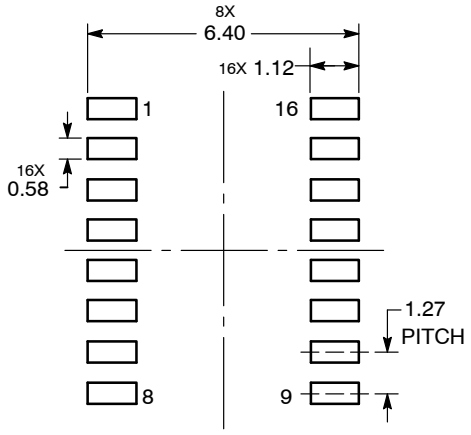
STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

**SOLDERING FOOTPRINT**




DIMENSIONS: MILLIMETERS

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC–16 | PAGE 1 OF 1 |


ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**onsemi**, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊