# MC74ACT564

# Octal D-Type Flip-Flop with 3-State Outputs

The MC74ACT564 is a high−speed, low power octal flip−flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$).

The information presented to the D inputs is stored in the flip−flops on the LOW−to−HIGH Clock (CP) transition.

The MC74ACT564 device is functionally indentical to the MC74ACT574, but with inverted outputs.

### Features

- Inputs and Outputs on the Opposite Sides of the Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessor
- Functionally Indentical to the MC74ACT574 but with Inverted Outputs
- 3−State Outputs for Bus−Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs
- These are Pb−Free Devices

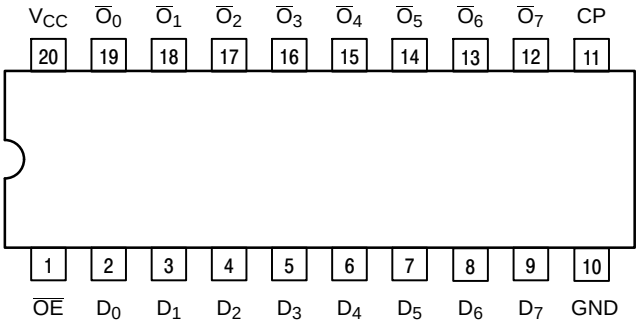


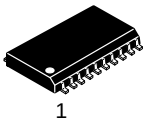

**Figure 1. Pinout: 20−Lead Packages Conductors**
(Top View)

**PIN ASSIGNMENT**

| PIN | FUNCTION |
|---|---|
| $D_0$−$D_7$ | Data Inputs |
| CP | Clock Pulse Input |
| $\overline{OE}$ | 3−State Output Enable Input |
| $\overline{O}_0$−$\overline{O}_7$ | 3−State Outputs |

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**SOIC−20W**
**DW SUFFIX**
**CASE 751D**

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 5 of this data sheet.

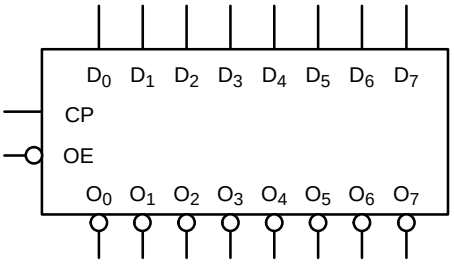
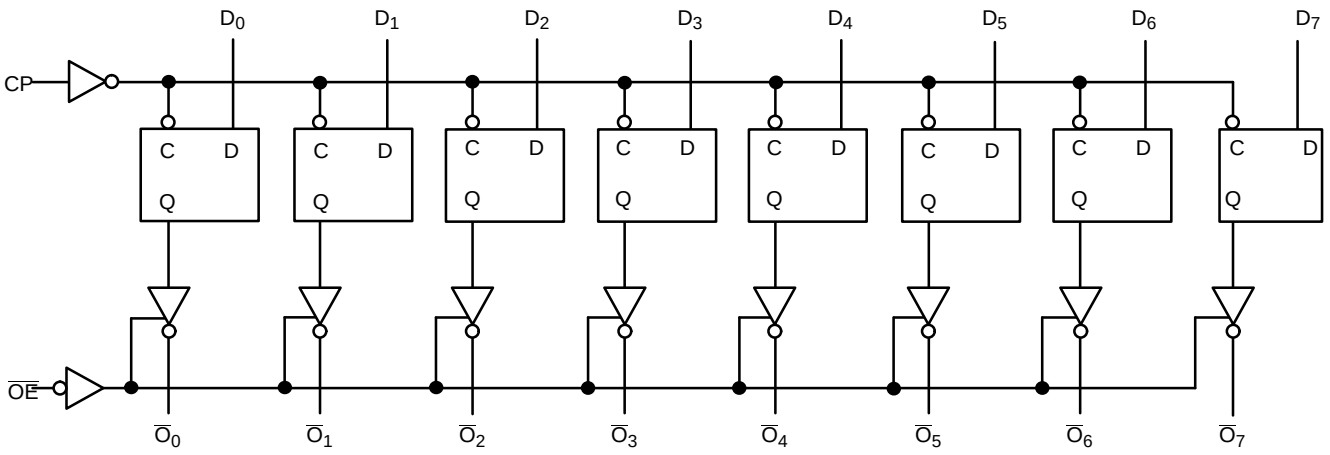



**Figure 2. Logic Symbol**

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Figure 3. Logic Diagram**

**FUNCTION TABLE**

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | CP | D | Q | O | |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | ⌐¬ | L | H | Z | Load |
| H | ⌐¬ | H | L | Z | Load |
| L | ⌐¬ | L | H | H | Data Available |
| L | ⌐¬ | H | L | L | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐¬ = LOW−to−HIGH Transition
NC = No Change

## FUNCTIONAL DESCRIPTION

The MC74ACT564 consists of eight edge−triggered flip−flops with individual D−type inputs and 3−state complementary outputs. The buffered clock and buffered Output Enable are common to all flip−flops. The eight flip−flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW−to−HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip−flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip−flops.

## MAXIMUM RATINGS

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage (Referenced to GND) | | −0.5 to $V_{CC}$ +0.5 | V |
| $V_{OUT}$ | DC Output Voltage (Referenced to GND) (Note 1) | | −0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | DC Input Diode Current | | ±20 | mA |
| $I_{OK}$ | DC Output Diode Current | | ±50 | mA |
| $I_{OUT}$ | DC Output Sink/Source Current | | ±50 | mA |
| $I_{CC}$ | DC Supply Current, per Output Pin | | ±50 | mA |
| $I_{GND}$ | DC Ground Current, per Output Pin | | ±100 | mA |
| $T_{STG}$ | Storage Temperature Range | | − 65 to + 150 | °C |
| $T_L$ | Lead temperature, 1 mm from Case for 10 Seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | 140 | °C |
| $\theta_{JA}$ | Thermal Resistance (Note 2) | | 65.8 | °C/W |
| MSL | Moisture Sensitivity | | Level 1 | |
| $F_R$ | Flammability Rating | Oxygen Index: 30% − 35% | UL 94 V−0 @ 0.125 in | |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 3)<br>Machine Model (Note 4)<br>Charged Device Model (Note 5) | > 2000<br>> 200<br>> 1000 | V |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 85°C (Note 6) | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. $I_{OUT}$ absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JESD 51−7.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | DC Input Voltage (Referenced to GND) | | 4.5 | | 5.5 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | | 0 | | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | | −40 | 25 | +85 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Note 8) | $V_{CC}$ = 4.5 V<br>$V_{CC}$ = 5.5 V | 0<br>0 | 10<br>8.0 | 10<br>8.0 | ns/V |
| $I_{OH}$ | Output Current − High | | | | −24 | mA |
| $I_{OL}$ | Output Current − Low | | | | 24 | mA |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. $V_{in}$ from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

## DC CHARACTERISTICS

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | | $T_A$ = −40°C to +85°C | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 2.0<br>2.0 | 2.0<br>2.0 | V<br>V | $V_{OUT}$ = 0.1 V<br>or<br>$V_{CC}$ − 0.1 V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 4.5<br>5.5 | 1.5<br>1.5 | 0.8<br>0.8 | 0.8<br>0.8 | V<br>V | $V_{OUT}$ = 0.1 V<br>or<br>$V_{CC}$ − 0.1 V |
| $V_{OH}$ | Minimum High Level Output Voltage | 4.5<br>5.5 | 4.49<br>5.49 | 4.4<br>5.4 | 4.4<br>5.4 | V<br>V | $I_{OUT}$ = −50 μA |
| | | 4.5<br>5.5 | | 3.86<br>4.86 | 3.76<br>4.76 | V<br>V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ −24 mA<br>$I_{OH}$ −24 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1 | 0.1<br>0.1 | V<br>V | $I_{OUT}$ = 50 μA |
| | | 4.5<br>5.5 | | 0.36<br>0.36 | 0.44<br>0.44 | V<br>V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ 24 mA<br>$I_{OL}$ 24 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |
| $\Delta I_{CCT}$ | Additional Max. $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I$ = $V_{CC}$ − 2.1 V |
| $I_{OZ}$ | Maximum 3−State Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I$ (OE) = $V_{IL}$, $V_{IH}$<br>$V_I$ = $V_{CC}$, GND<br>$V_O$ = $V_{CC}$, GND |
| $I_{OLD}$<br>$I_{OHD}$ | †Minimum Dynamic Output Current | 5.5<br>5.5 | | | 75<br>−75 | mA<br>mA | $V_{OLD}$ = 1.65 V Max<br>$V_{OHD}$ = 3.85 V Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80 | μA | $V_{IN}$ = $V_{CC}$ or GND |

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

## AC CHARACTERISTICS $t_r = t_f$ = 3.0 ns (For Figures and Waveforms, See Figures 4, 5, and 6.)

| Symbol | Parameter | $V_{CC}$* (V) | $T_A$ = +25°C<br>$C_L$ = 50 pF | | | $T_A$ = −40°C to +85°C<br>$C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $f_{max}$ | Maximum Clock Frequency | 5.0 | 85 | − | − | 75 | − | MHz |
| $t_{PLH}$ | Propagation Delay CP to $\overline{Q}_n$ | 5.0 | 2.0 | − | 10.5 | 1.5 | 11.5 | ns |
| $t_{PHL}$ | Propagation Delay CP to $\overline{Q}_n$ | 5.0 | 1.5 | − | 9.5 | 1.5 | 10.5 | ns |
| $t_{PZH}$ | Output Enable Time | 5.0 | 1.5 | − | 9.0 | 1.5 | 9.5 | ns |
| $t_{PZL}$ | Output Enable Time | 5.0 | 1.5 | − | 8.5 | 1.0 | 9.5 | ns |
| $t_{PHZ}$ | Output Disable Time | 5.0 | 1.5 | − | 10.5 | 1.5 | 11.5 | ns |
| $t_{PLZ}$ | Output Disable Time | 5.0 | 1.5 | − | 8.0 | 1.0 | 8.5 | ns |

*Voltage Range 5.0 V is 5.0 V ±0.5 V

## AC OPERATING REQUIREMENTS

| Symbol | Parameter | | $V_{CC}$* (V) | $T_A$ = +25°C $C_L$ = 50 pF | $T_A$ = −40°C to +85°C $C_L$ = 50 pF | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Minimum | | |
| $t_s$ | Setup Time, HIGH or LOW | $D_n$ to $C_P$ | 5.0 | − | 2.5 | 3.0 | ns |
| $t_h$ | Hold Time, HIGH or LOW | $D_n$ to $C_P$ | 5.0 | − | 1.0 | 1.0 | ns |
| $t_w$ | $C_P$ Pulse Width | HIGH or LOW | 5.0 | − | 3.0 | 3.5 | ns |

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

## CAPACITANCE

| Symbol | Parameter | Value Typ | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = 5.0 V |
| $C_{PD}$ | Power Dissipation Capacitance | 50 | pF | $V_{CC}$ = 5.0 V |

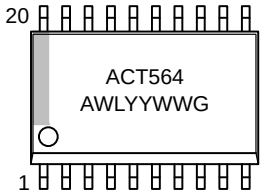
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74ACT564DWR2G | SOIC−20 (Pb−Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

**SOIC−20W**




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

## SWITCHING WAVEFORMS

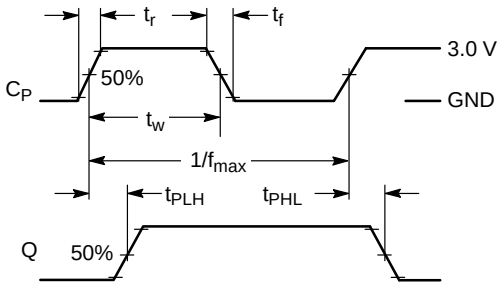



**Figure 4.**

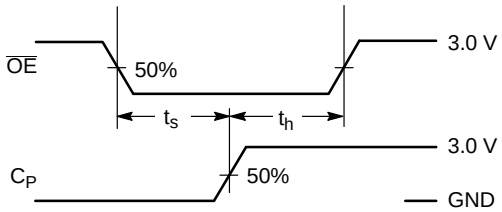



**Figure 5.**

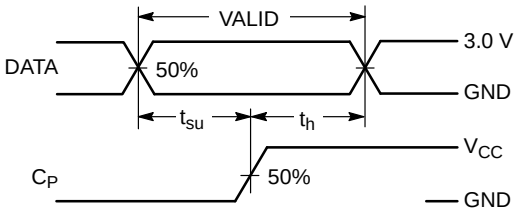
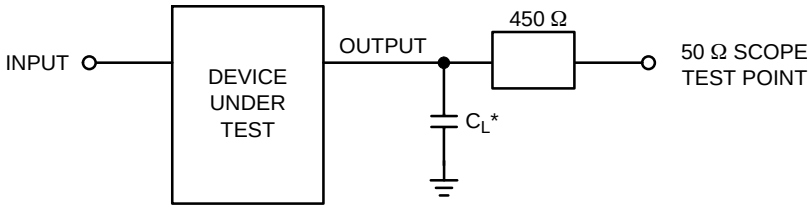



**Figure 6.**



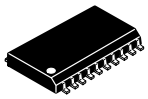

*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

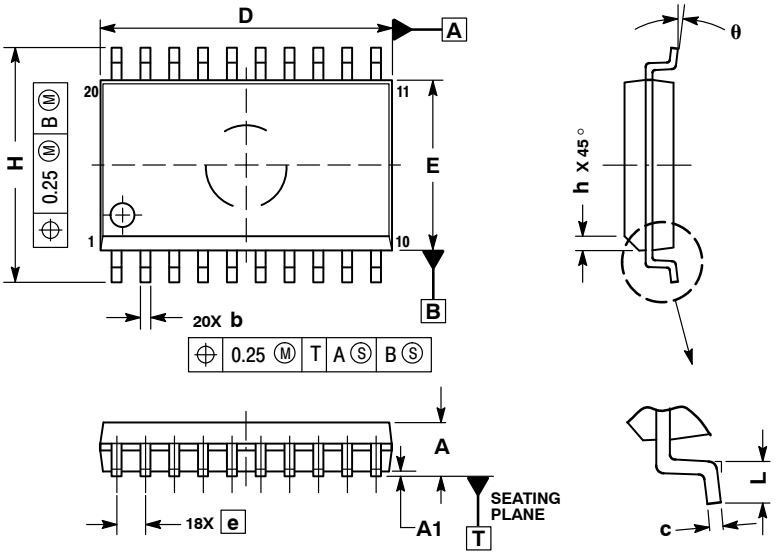
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SOIC−20 WB**
CASE 751D−05
ISSUE H

DATE 22 APR 2015



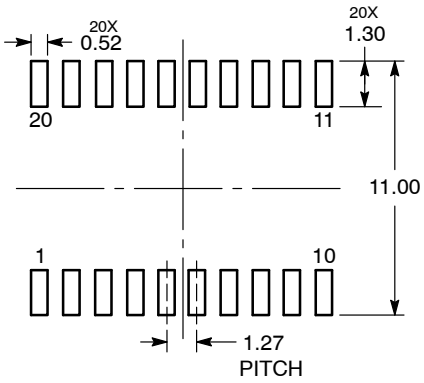
**SCALE 1:1**




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| b | 0.35 | 0.49 |
| c | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

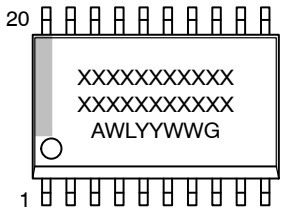
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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