MC74HC377A

Octal D Flip-Flop with Common Clock and Enable

High−Performance Silicon−Gate CMOS

The MC74HC377A is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of eight D flip−flops with common Clock and Enable ($\overline{E}$) inputs. Each flip−flop is loaded with a low−to−high transition of the Clock input. Enable ($\overline{E}$) is active low.

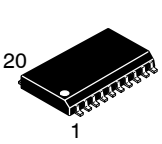
Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 264 FETs or 66 Equivalent Gates
- These are Pb−Free Devices

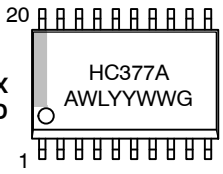
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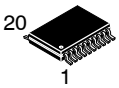
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MARKING DIAGRAMS

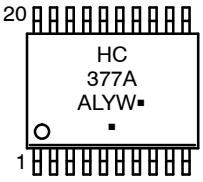


SOIC−20
DW SUFFIX
CASE 751D



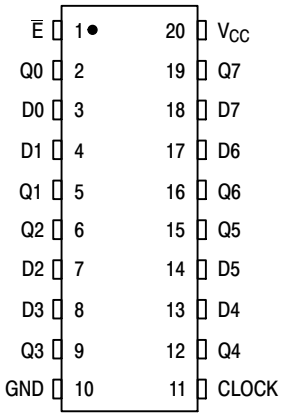


TSSOP−20
DT SUFFIX
CASE 948E



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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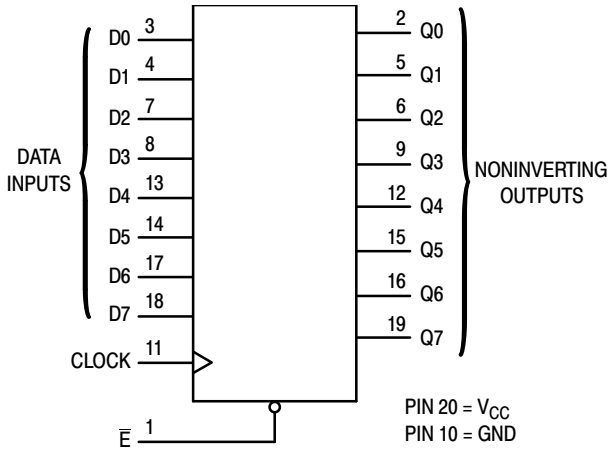


Figure 1. Logic Diagram

FUNCTION TABLE

Operating Modes	Inputs			Outputs
	Clock	$\overline{E}$	Dn	Qn
Load “1”	↑	l	h	H
Load “0”	↑	l	l	L
Hold (Do Nothing)	↑ X	h H	X X	No Change No Change

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW−to−HIGH CP transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW−to−HIGH CP transition
↑ = LOW−to−HIGH CP transition
X = Don’t Care

Design Criteria	Value	Units
Internal Gate Count*	66	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	pJ

*Equivalent to a two−input NAND gate.

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC377ADWG	SOIC−20 WIDE (Pb−Free)	38 Units / Rail
MC74HC377ADWR2G	SOIC−20 WIDE (Pb−Free)	1000 Tape & Reel
MC74HC377ADTG	TSSOP−20*	75 Units / Rail
MC74HC377ADTR2G	TSSOP−20*	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air SOIC Package†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	–65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating – SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figure 2)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	3.98 5.48	3.84 5.34	3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	4.5 6.0	0.26 0.26	0.33 0.33	0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

AC Electrical Characteristics (C_L = 50 pF, Input t_r, t_f = 6.0 ns)

Symbol	Parameter	Test Conditions	V_{CC} (V)	Guaranteed Limits			Unit
				−55°C to 25°	≤ 85°C	≤ 125°C	
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Qn	Figures 2, 4	2.0	160	200	240	ns
			4.5	32	40	48	
			6.0	27	34	41	
t_{THL}, t_{TLH}	Maximum Output Transition Time	Figures 2, 4	2.0	75	95	110	ns
			4.5	15	19	22	
			6.0	13	16	19	
t_W	Minimum Clock Pulse Width High or Low	Figure 2	2.0	80	100	120	ns
			4.5	16	20	24	
			6.0	4	17	20	
t_{su}	Minimum Set−up Time D_n to Clock	Figure 3	2.0	60	75	90	ns
			4.5	12	15	18	
			6.0	10	13	15	
t_{su}	Minimum Set−up Time Enable to Clock	Figure 3	2.0	60	75	90	ns
			4.5	12	15	18	
			6.0	10	13	15	
t_h	Minimum Hold Time D_n to Clock	Figure 3	2.0	3	3	3	ns
			4.5	3	3	3	
			6.0	3	3	3	
t_h	Minimum Hold Time Enable to Clock	Figure 3	2.0	4	4	4	ns
			4.5	4	4	4	
			6.0	4	4	4	
f_{max}	Maximum Clock Pulse Frequency (50% duty cycle)	Figures 2, 4	2.0	6	5	4	ns
			4.5	30	24	20	
			6.0	35	28	24	
C_{in}	Maximum Input Capacitance		−	10	10	10	pF

C_{PD} (Note 1)		Typical @ 25°C, V_{CC} = 5.0 V	pF
	Power Dissipation Capacitance	35	

1. C_{PD} is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from: I_{CC}(operating) ≈ C_{PD} x V_{CC} x f_{IN} x N_{SW} where N_{SW} = total number of outputs switching and f_{IN} = switching frequency.

SWITCHING WAVEFORMS

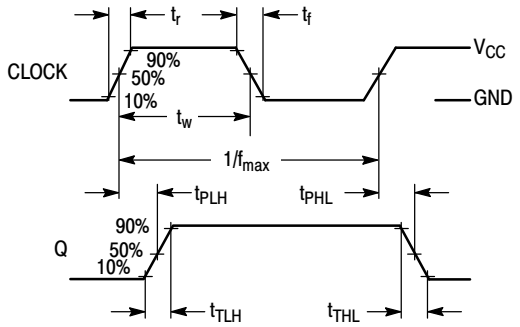


Figure 2.

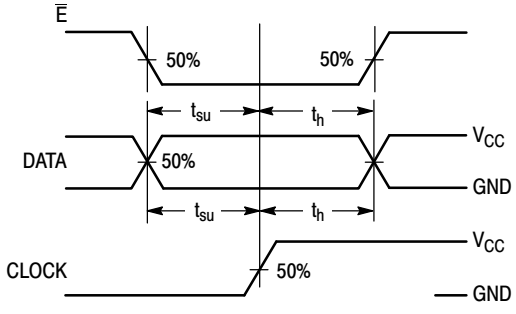
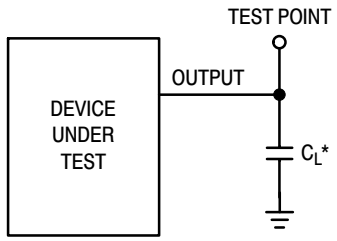


Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

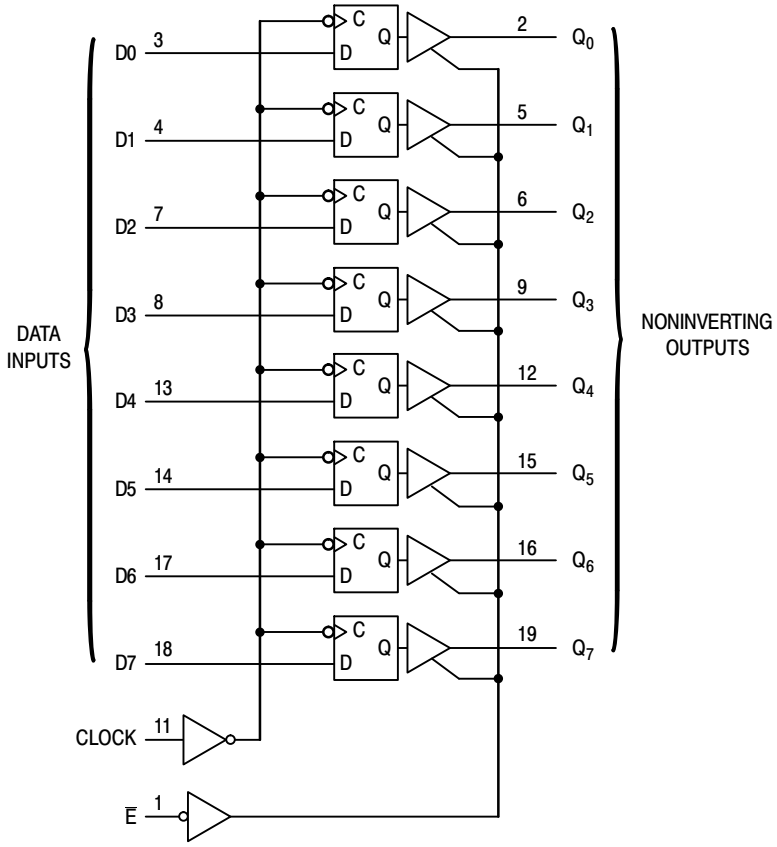
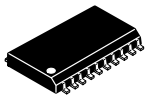


Figure 5. Expanded Logic Diagram

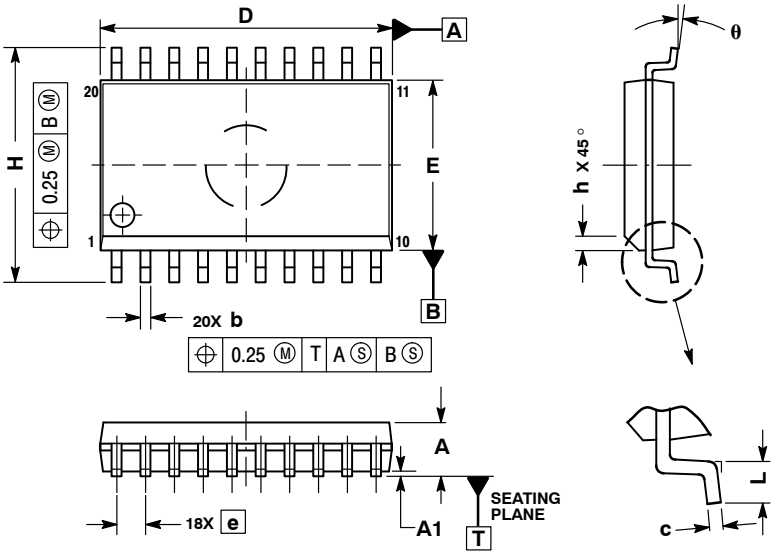
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



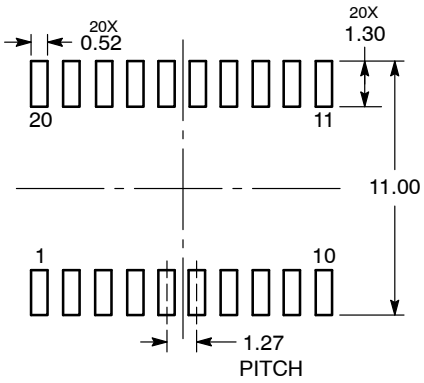
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

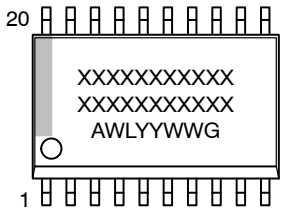
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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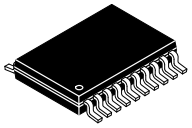
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

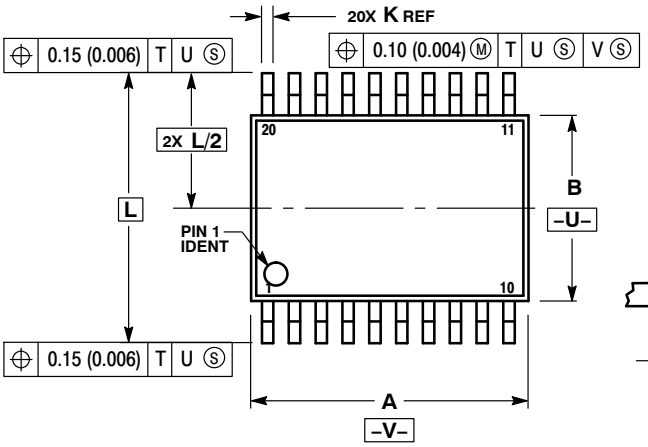
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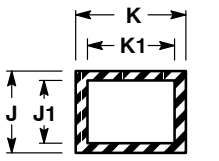
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

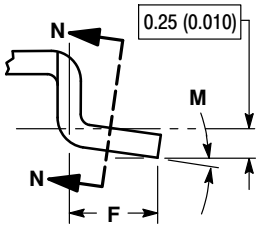


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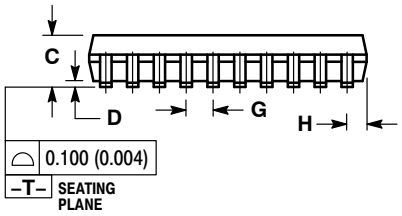


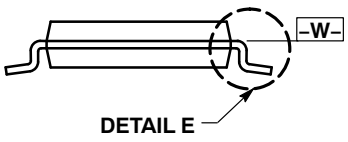


SECTION N−N



DETAIL E

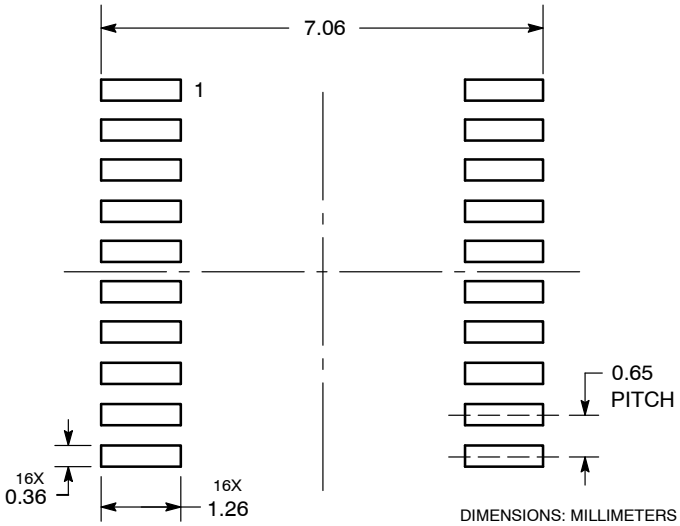




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

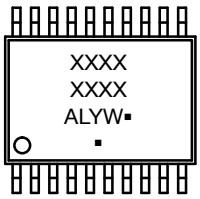
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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