MC74VHC1GT66

SPST (NO) Normally Open Analog Switch

The MC74VHC1GT66 is a Single Pole Single Throw (SPST) analog switch. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power−supply range (from V_{CC} to GND).

The MC74VHC1GT66 is compatible in function to a single gate of the High Speed CMOS MC74VHCT4066 and the metal−gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal−gate CMOS or High Speed CMOS analog switches.

The ON/OFF Control input is compatible with TTL−type input thresholds allowing the device to be used as a logic−level translator from 3 V CMOS logic to 5 V CMOS logic or from 1.8 V CMOS logic to 3 V CMOS logic while operating at the high−voltage power supply. The input protection circuitry on this device allows overvoltage tolerance on the input, which provides protection when voltages of up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT66 to be used to interface 5 V circuits to 3 V circuits.

Features

- High Speed: t_{PD} = 20 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 1.0 μA (Max) at T_A = 25°C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- On/Off Control Input Has OVT
- Chip Complexity: FETs = 11; Equivalent Gates = 3
- Pb−Free Packages are Available

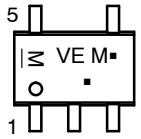
ON Semiconductor®

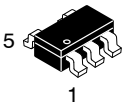
http://onsemi.com

MARKING DIAGRAMS

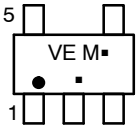


SC−88A
DF SUFFIX
CASE 419A





TSOP−5
DT SUFFIX
CASE 483



VE = Device Code
M = Date Code*
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT	
1	IN/OUT X_A
2	OUT/IN Y_A
3	GND
4	ON/OFF CONTROL
5	V_{CC}

FUNCTION TABLE

On/Off Control Input	State of Analog Switch
L	Off
H	On

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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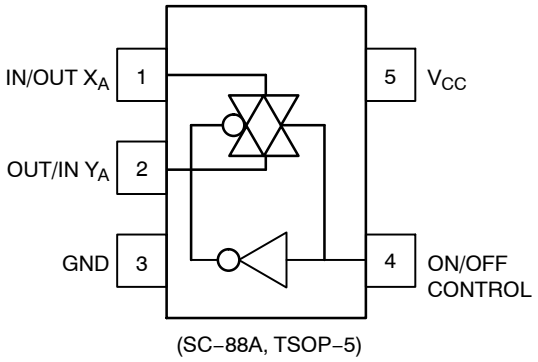


Figure 1. Pinout Diagram

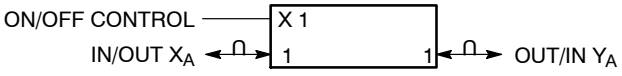


Figure 2. Logic Symbol

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{IS}	Analog Output Voltage		−0.5 to 7.0	V
I_{IK}	Input Diode Current		−20	mA
I_{CC}	DC Supply Current, V_{CC} and GND		+25	mA
T_{STG}	Storage Temperature Range		− 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+ 150	°C
θ_{JA}	Thermal Resistance	SC70−5 (Note 1) SOT23−5	350 230	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC70−5 SOT23−5	150 200	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 5)	± 500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	Digital Input Voltage		GND	5.5	V
V_{IS}	Analog Input Voltage		GND	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
t_r , t_f	Input Rise and Fall Time	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

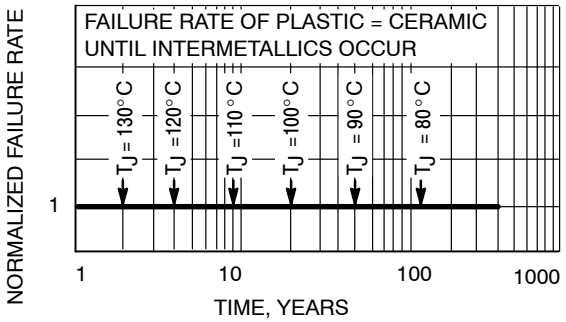


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C		$T_A \le$ 85°C		−55°C ≤ $T_A \le$ 125°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5	1.2 2.0 2.0		1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low−Level Input Voltage ON/OFF Control Input	R_{ON} = Per Spec	3.0 4.5 5.5		0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
I_{IN}	Maximum Input Leakage Current ON/OFF Control Input	V_{IN} = V_{CC} or GND	0 to 5.5		±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND V_{IO} = 0 V	5.5		1.0		20		40	μA
I_{CCT}	Quiescent Supply Current	ON/OFF Control at 3.4 V	5.5		1.35		1.5		1.65	mA
R_{ON}	Maximum "ON" Resistance	V_{IN} = V_{IH} V_{IS} = V_{CC} or GND $\|I_{IS}\| \le$ 10 mA (Figure 4)	3.0 4.5 5.5		60 45 40		70 50 45		100 60 55	Ω
I_{OFF}	Maximum Off−Channel Leakage Current	V_{IN} = V_{IL} V_{IS} = V_{CC} or GND Switch Off (Figure 5)	5.5		0.1		0.5		1.0	μA

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r/t_f = 3.0 ns

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \le$ 85°C		−55°C ≤ $T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input X to Y	Y_A = Open (Figures 7, 14)	2.0 3.0 4.5 5.5		1 0.6 0.6 0.6	5 2 1 1		6 3 1 1		7 4 2 1	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figures 8, 15)	2.0 3.0 4.5 5.5		32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, ON/OFF Control to Analog Output	R_L = 1000 Ω (Figures 8, 15)	2.0 3.0 4.5 5.5		32 28 24 20	40 35 30 25		45 40 35 30		50 45 40 35	ns
C_{IN}	Maximum Input Capacitance	ON/OFF Control Input	0.0		3	10		10		10	pF
		Control Input = GND Analog I/O Feedthrough	5.0		 4 4	 10 10		 10 10		 10 10	

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	18	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Symbol	Parameter	Test Conditions	V_{CC}	Limit 25°C	Unit
BW	Maximum On−Channel Bandwidth or Minimum Frequency Response (Figure 10)	f_{in} = 1 MHz Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase f_{in} = frequency until dB meter reads −3 dB R_L = 50 Ω	3.0 4.5 5.5	150 175 180	MHz
ISO_{off}	Off−Channel Feedthrough Isolation (Figure 11)	f_{in} = Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} f_{in} = 10 kHz, R_L = 600 Ω	3.0 4.5 5.5	−80 −80 −80	dB
$NOISE_{feed}$	Feedthrough Noise Control to Switch (Figure 12)	$V_{in} \le$ 1 MHz Square Wave ($t_r = t_f$ = 2ns) R_L = 600 Ω	3.0 4.5 5.5	45 60 130	mV_{PP}
THD	Total Harmonic Distortion (Figure 13)	f_{in} = 1 kHz, R_L = 10 kΩ THD = $THD_{Measured} - THD_{Source}$ V_{IS} = 3.0 V_{PP} sine wave V_{IS} = 5.0 V_{PP} sine wave	 3.3 5.5	 0.30 0.15	%

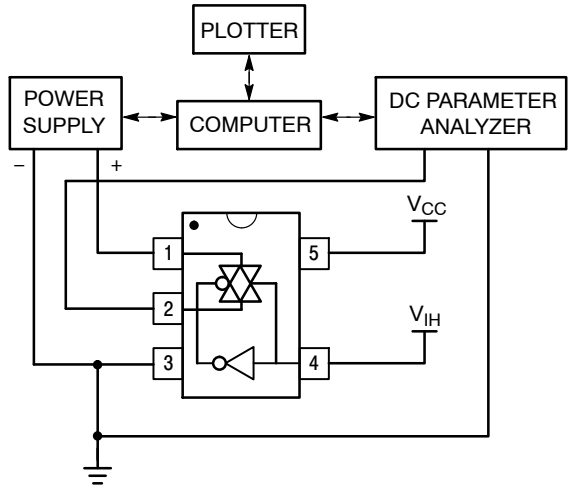


Figure 4. On Resistance Test Set−Up

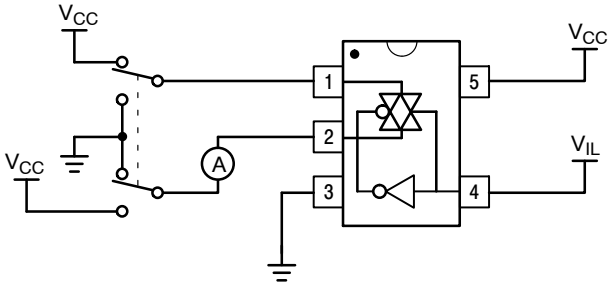


Figure 5. Maximum Off−Channel Leakage Current Test Set−Up

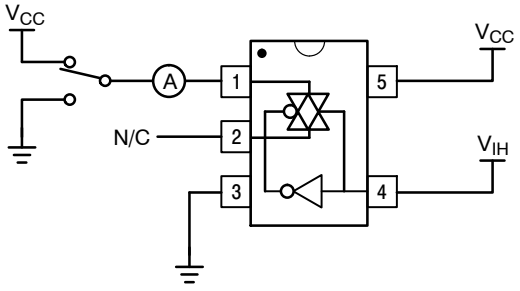


Figure 6. Maximum On−Channel Leakage Current Test Set−Up

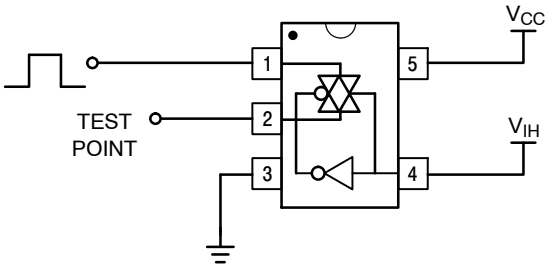


Figure 7. Propagation Delay Test Set−Up

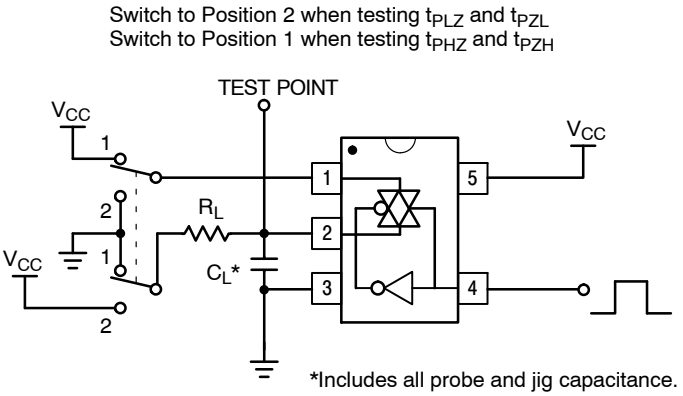


Figure 8. Propagation Delay Output Enable/Disable Test Set−Up

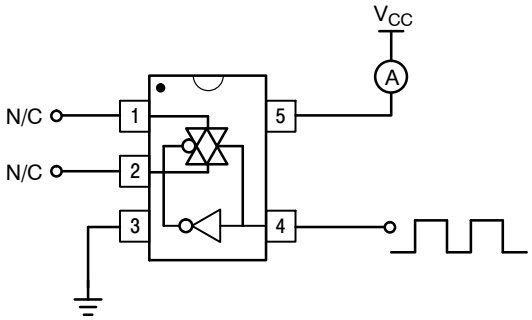


Figure 9. Power Dissipation Capacitance Test Set−Up

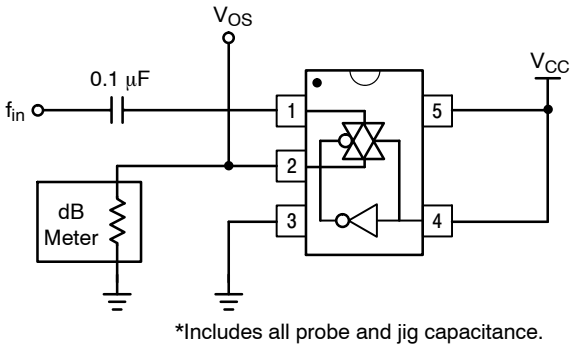


Figure 10. Maximum On−Channel Bandwidth Test Set−Up

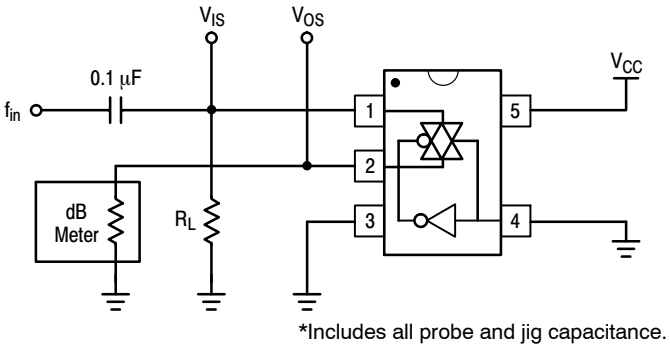


Figure 11. Off−Channel Feedthrough Isolation Test Set−Up

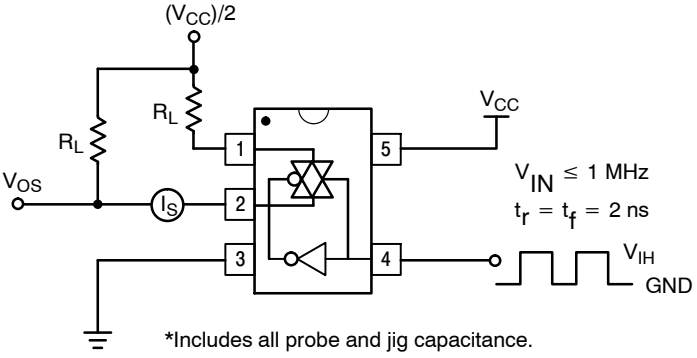


Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set−Up

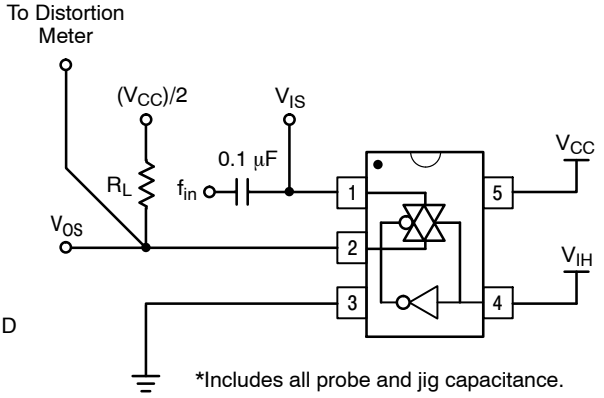


Figure 13. Total Harmonic Distortion Test Set−Up

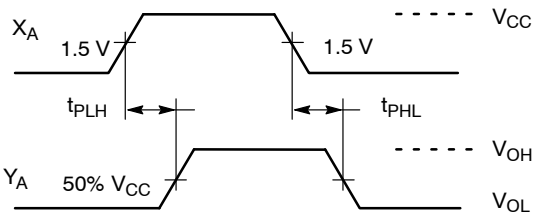


Figure 14. Propagation Delay, Analog In to Analog Out Waveforms

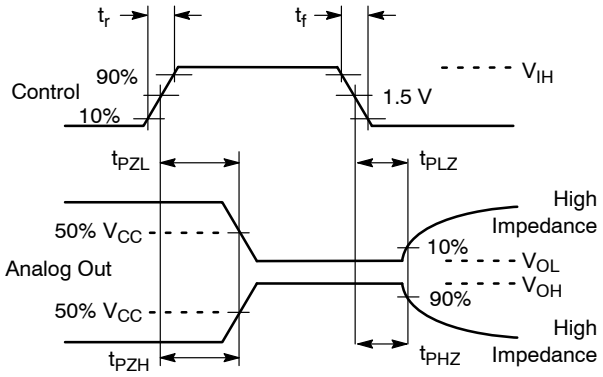


Figure 15. Propagation Delay, ON/OFF Control

ORDERING INFORMATION

Device	Package	Shipping†
M74VHC1GT66DFT1G	SC−88A (Pb−Free)	3000 / Tape & Reel
MC74VHC1GT66DFT2	SC−88A	
M74VHC1GT66DFT2G	SC−88A (Pb−Free)	
MC74VHC1GT66DTT1	TSOP−5	
M74VHC1GT66DTT1G	TSOP−5 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

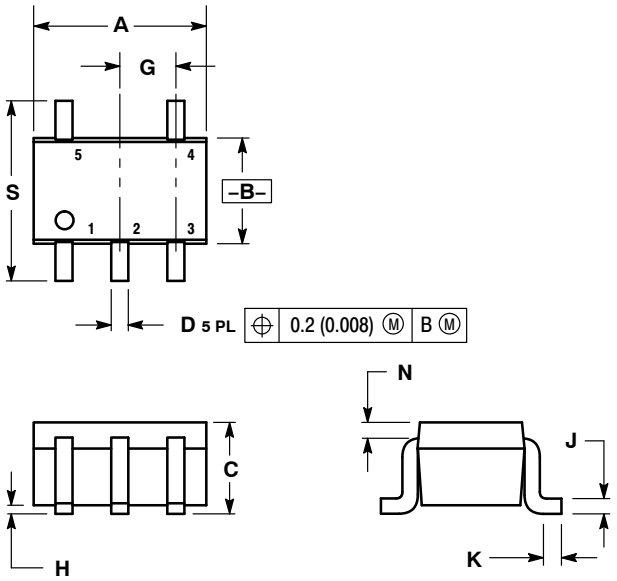
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE L

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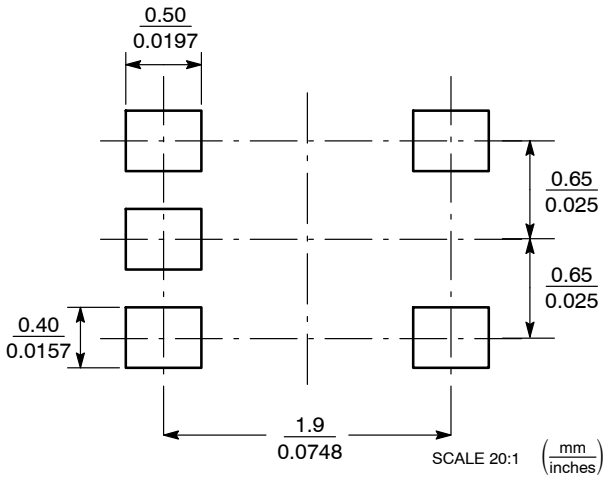
DATE 17 JAN 2013



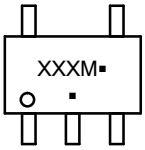
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

SOLDER FOOTPRINT



GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

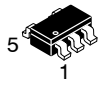
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DESCRIPTION:	SC−88A (SC−70−5/SOT−353)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

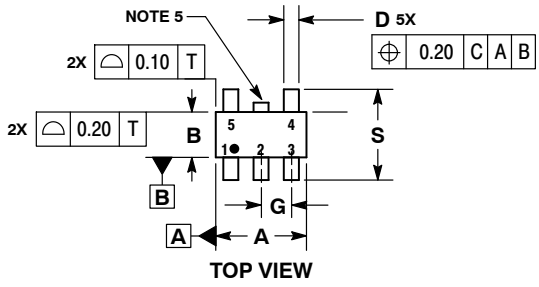
ON Semiconductor®



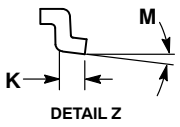
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TSOP−5
CASE 483
ISSUE N

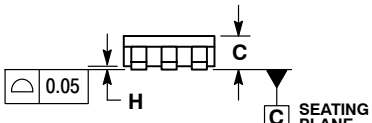
DATE 12 AUG 2020



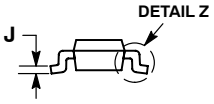
TOP VIEW



DETAIL Z



SIDE VIEW

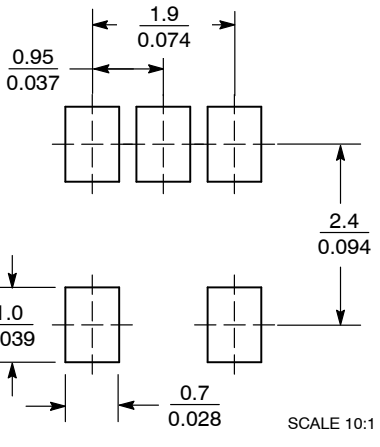


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

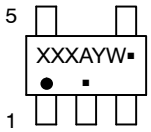
SOLDERING FOOTPRINT*



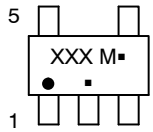
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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