MC74VHC373

Octal D-Type Latch with 3-State Output

The MC74VHC373 is an advanced high speed CMOS octal latch with 3−state output fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This 8−bit D−type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

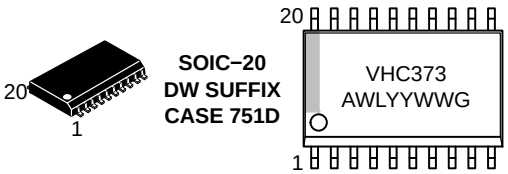
Features

- High Speed: t_{PD} = 5.0 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 4.0 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.9 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 186 FETs or 46.5 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

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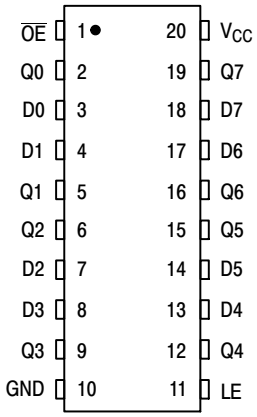
MARKING DIAGRAM



VHC373	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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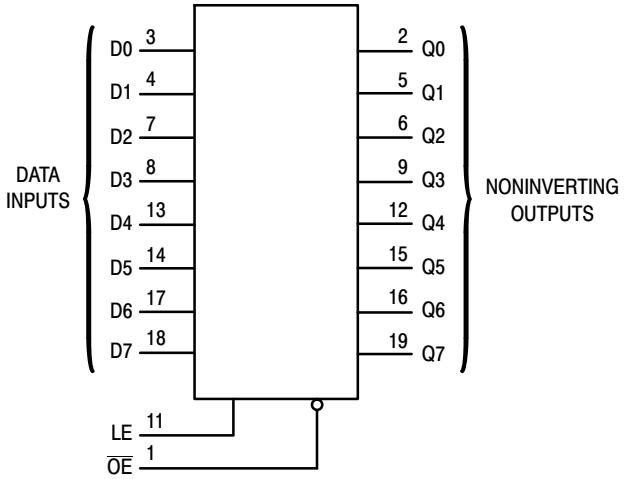


Figure 1. Logic Diagram

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating — SOIC Package: – 7 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		− 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3 V V_{CC} = 5.0 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = − 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = − 50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = − 4 mA I_{OH} = − 8 mA	 3.0 4.5	 2.58 3.94			 2.48 3.80		
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	 3.0 4.5			 0.36 0.36		 0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND	0 to 5.5			± 0.1		± 1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = − 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, D to Q	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		4.9 6.4	7.2 9.2	1.0 1.0	8.5 10.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, LE to Q	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF C_L = 50 pF		7.0 9.5	11.0 14.5	1.0 1.0	13.0 16.5	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF		5.0 6.5	7.2 9.2	1.0 1.0	8.5 10.5	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to Q	V_{CC} = 3.3 ± 0.3 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		7.3 9.8	11.4 14.9	1.0 1.0	13.5 17.0	ns
		V_{CC} = 5.0 ± 0.5 V C_L = 15 pF R_L = 1 kΩ C_L = 50 pF		5.5 7.0	8.1 10.1	1.0 1.0	9.5 11.5	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to Q	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF R_L = 1 kΩ		9.5	13.2	1.0	15.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50 pF R_L = 1 kΩ		6.5	9.2	1.0	10.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3 V C_L = 50 pF (Note 1)			1.5		1.5	ns
		V_{CC} = 5.5 ± 0.5 V C_L = 50 pF (Note 1)			1.0		1.0	ns

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
			Min	Typ	Max	Min	Max	
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)			6				pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 2)	27	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per latch). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$ pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.6	− 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = -40$ to $85°C$	Unit
			Typ	Limit	Limit	
$t_{w(h)}$	Minimum Pulse Width, LE	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	ns
t_{su}	Minimum Setup Time, D to LE	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		4.0 4.0	4.0 4.0	ns
t_h	Minimum Hold Time, D to LE	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		1.0 1.0	1.0 1.0	ns

ORDERING INFORMATION

Device	Package	Shipping†
MC74VHC373DWR2G	SOIC−20 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SWITCHING WAVEFORMS

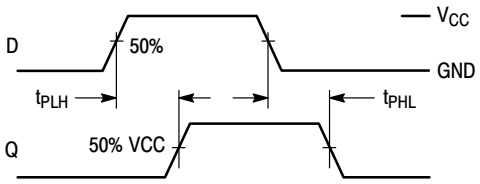


Figure 2.

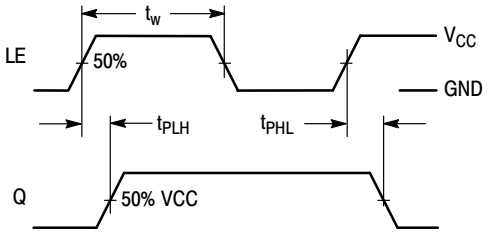


Figure 3.

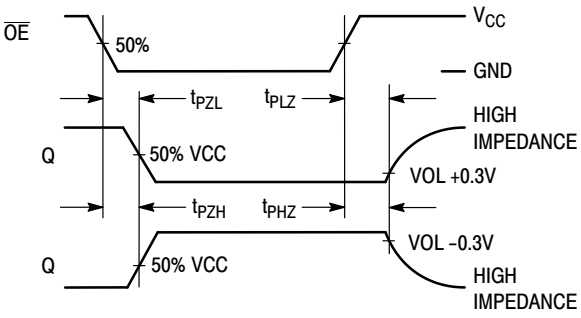


Figure 4.

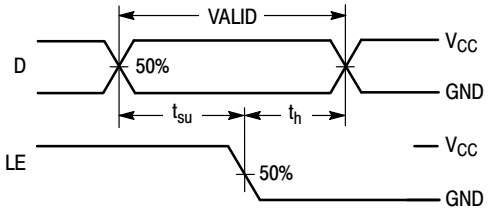
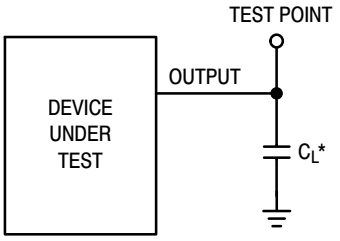


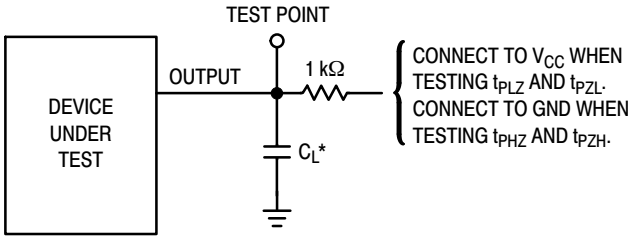
Figure 5.

TEST CIRCUITS



*Includes all probe and jig capacitance

Figure 6.



*Includes all probe and jig capacitance

Figure 7.

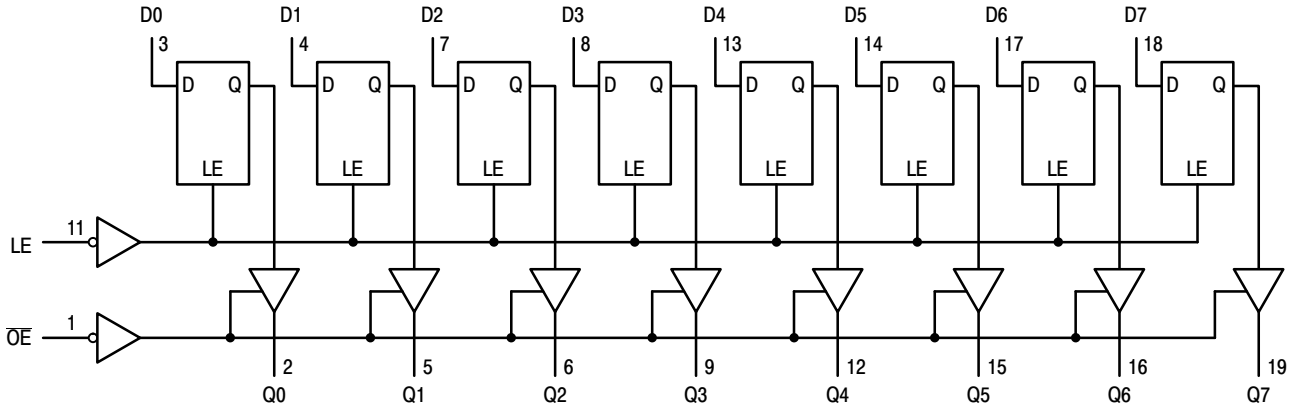


Figure 8. EXPANDED LOGIC DIAGRAM

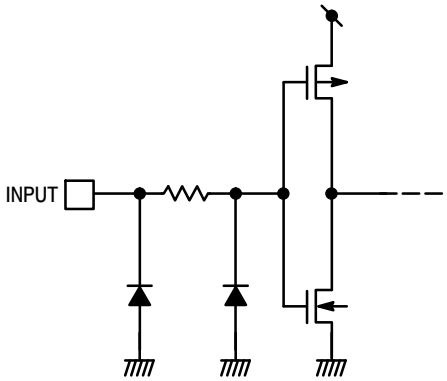
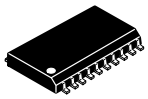


Figure 9. INPUT EQUIVALENT CIRCUIT

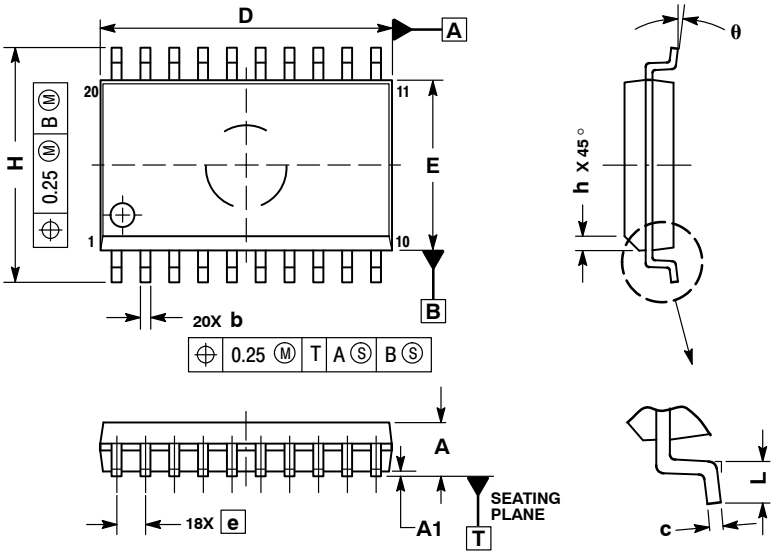
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



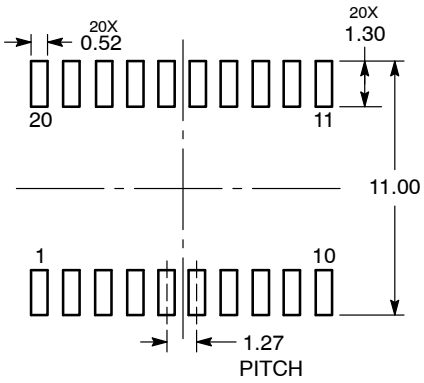
SCALE 1:1



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

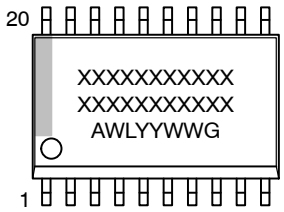
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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