MC74VHCT14A

Hex Schmitt Inverter

The MC74VHCT14A is an advanced high speed CMOS Schmitt inverter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHCT04A, but the inputs have hysteresis and, with its Schmitt trigger function, the VHCT14A can be used as a line receiver which will receive slow input signals.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT14A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when V_{CC} = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

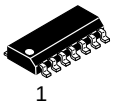
Features

- High Speed: t_{PD} = 5.5 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 2.0 μA (Max) at T_A = 25°C
- TTL−Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: 60 FETs or 15 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

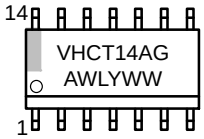
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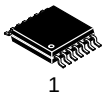
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MARKING DIAGRAMS

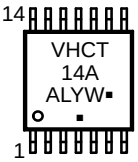


SOIC−14
D SUFFIX
CASE 751A





TSSOP−14
DT SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
Y, YY = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs	Outputs
A	**$\overline{Y}$**
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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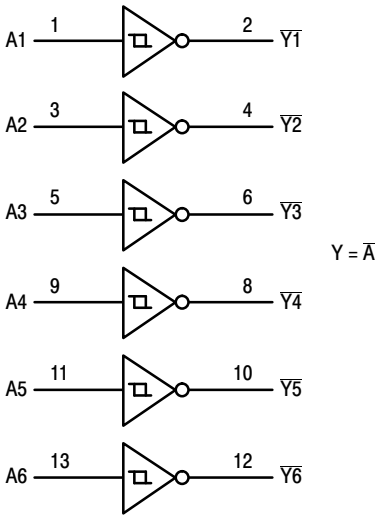
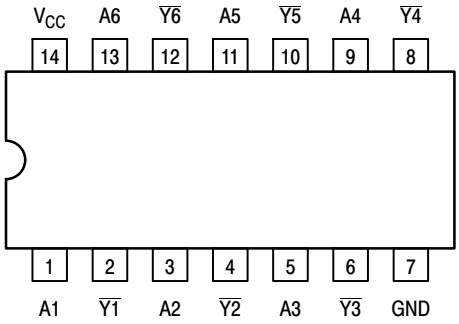


Figure 1. Logic Diagram



Pinout: 14−Lead Packages (Top View)

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	−0.5 to +7.0	V
DC Input Voltage		V_{IN}	−0.5 to +7.0	V
DC Output Voltage	Output in HIGH or LOW State (Note 1)	V_{OUT}	−0.5 to V_{CC} +0.5 V	V
V_{CC} = 0 V		V_{OUT}	−0.5 to 7.0	V
DC Input Diode Current		I_{IK}	−20	mA
DC Output Diode Current		I_{OK}	±20	mA
DC Output Source/Sink Current		I_O	±25	mA
DC Supply Current per Supply Pin		I_{CC}	±50	mA
DC Ground Current per Ground Pin		I_{GND}	±50	mA
Storage Temperature Range		T_{STG}	−65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds		T_L	260	°C
Junction Temperature under Bias		T_J	+150	°C
Thermal Resistance	SOIC TSSOP	θ_{JA}	125 170	°C/W
Power Dissipation in Still Air	SOIC TSSOP	P_D	500 450	mW
ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	V_{ESD}	>2000 >200 2000	V
Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 5)	$I_{Latchup}$	±300	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input Voltage	V_I	0	5.5	V
Output Voltage (Note 6)	V_O	0	V_{CC}	V
V_{CC} = 0 V	V_O	0	5.5	V
Operating Free−Air Temperature	T_A	−55	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. I_O absolute maximum rating must be observed.

DC ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	Symbol	V_{CC} V	T_A = 25°C			$T_A \le$ 85°C		$T_A \le$ 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
Positive Threshold Voltage		V_{T+}	4.5 5.5			1.9 2.1		1.9 2.1		1.9 2.1	V
Negative Threshold Voltage		V_{T-}	4.5 5.5	0.5 0.6			0.5 0.6		0.5 0.6		V
Hysteresis Voltage		V_H	4.5 5.5	0.40 0.40		1.40 1.50	0.40 0.40	1.40 1.50	0.40 0.40	1.40 1.50	V
Minimum High−Level Output Voltage I_{OH} = −50 μA	V_{IN} = V_{IH} or V_{IL} I_{OH} = −50 μA	V_{OH}	4.5	4.4	4.5		4.4		4.4		V
	I_{OH} = −8.0 mA		5.5	3.94			3.80		3.66		
Maximum Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	V_{OL}	4.5		0.0	0.1		0.1		0.1	V
	I_{OL} = 8.0 mA		5.5			0.36		0.44		0.52	
Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	I_{IN}	0 to 5.5			±0.1		±1.0		±1.0	μA
Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	I_{CC}	5.5			2.0		20		40	μA
Quiescent Supply Current	Input: V_{IN} = 3.4 V	I_{CCT}	5.5			1.35		1.50		1.65	mA
Output Leakage Current	V_{OUT} = 5.5 V	I_{OFF}	0.0			0.5		5.0		10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Parameter	Test Conditions	Symbol	T_A = 25°C			$T_A \le$ 85°C		$T_A \le$ 125°C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
Maximum Propagation Delay, A to $\overline{Y}$	V_{CC} = 5.0 ± 0.5 V C_L = 15 pF C_L = 50 pF	t_{PLH}, t_{PHL}		5.5 7.0	7.6 9.6	1.0 1.0	9.0 11.0	1.0 1.0	11.5 13.5	ns
Maximum Input Capacitance		C_{IN}		2.0	10		10		10	pF
Power Dissipation Capacitance (Note 7)			Typical @ 25°C, V_{CC} = 5.0 V							
		C_{PD}		11						pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/6$ (per buffer). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0 ns, C_L = 50 pF, V_{CC} = 5.0 V)

Characteristic	Symbol	T_A = 25°C		Unit
		Typ	Max	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	0.8	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	−0.8	−1.0	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		0.8	V

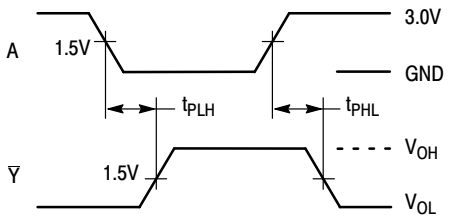
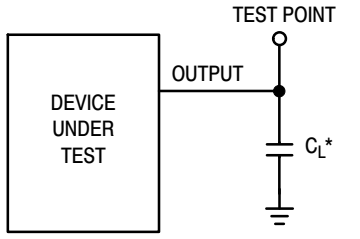


Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

(a) A Schmitt−Trigger Squares Up Inputs With Slow Rise and Fall Times

(b) A Schmitt−Trigger Offers Maximum Noise Immunity

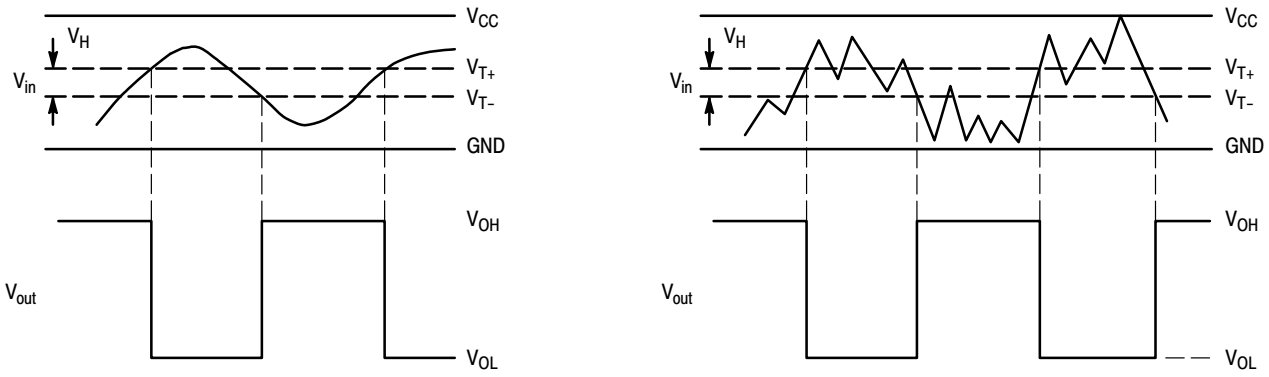


Figure 4. Typical Schmitt−Trigger Applications

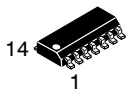
ORDERING INFORMATION

Device	Package	Shipping†
MC74VHCT14ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
NLV74VHCT14DR2G*		
MC74VHCT14ADTR2G	TSSOP−14 (Pb−Free)	
NLV74VHCT14ADTR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

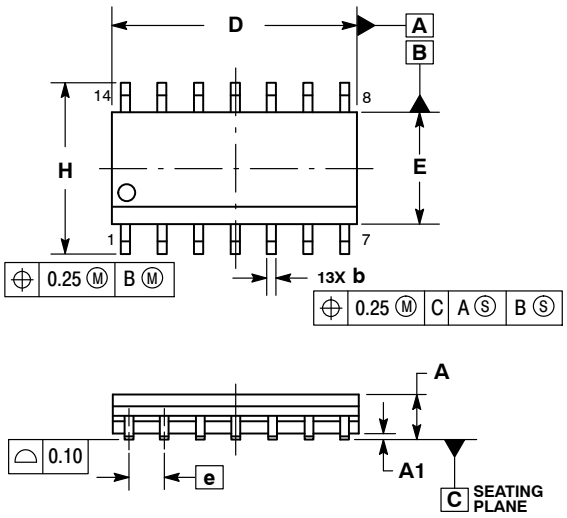
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

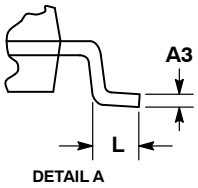


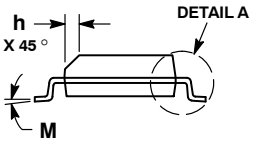
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SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



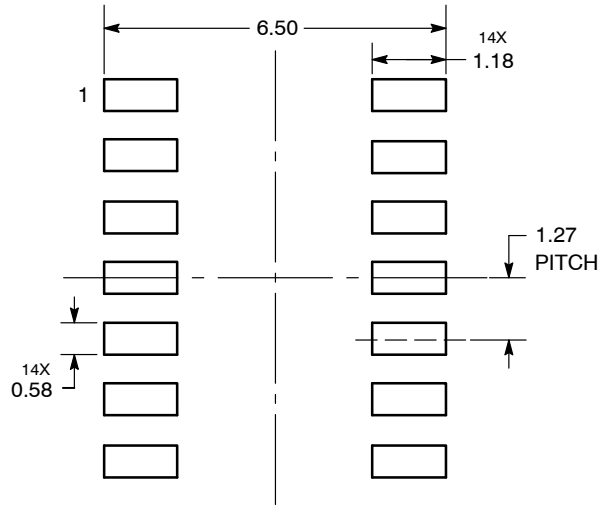




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

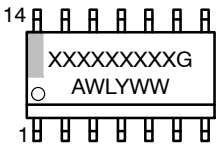
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
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5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
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7. ANODE
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11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
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8. CATHODE
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10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
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2. ANODE/CATHODE
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4. ANODE/CATHODE
5. ANODE/CATHODE
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7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
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12. ANODE
13. ANODE
14. ANODE

STYLE 7:
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9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
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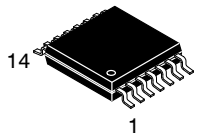
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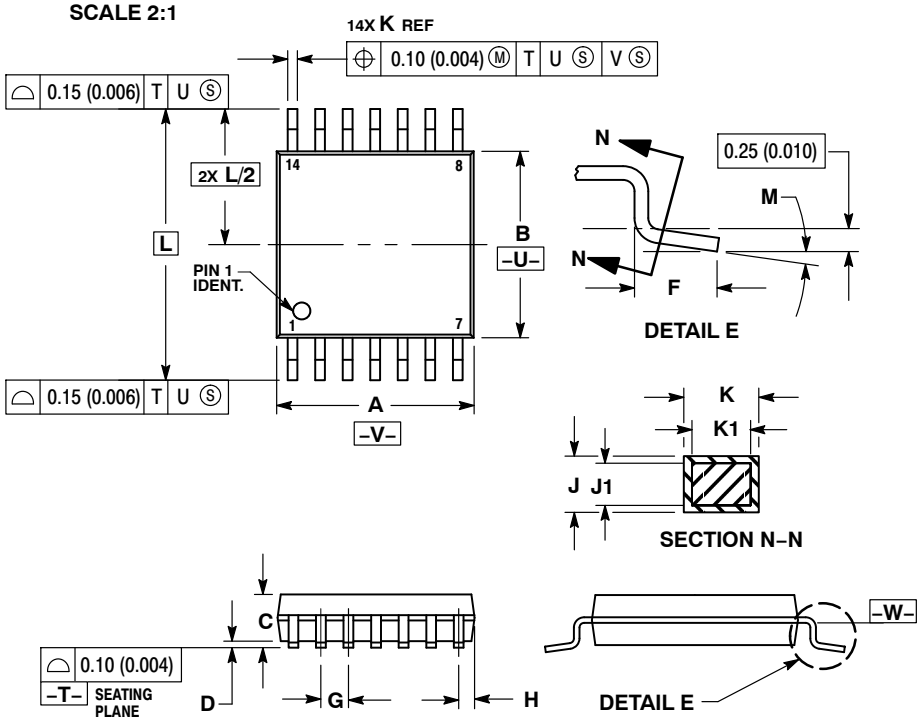
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PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



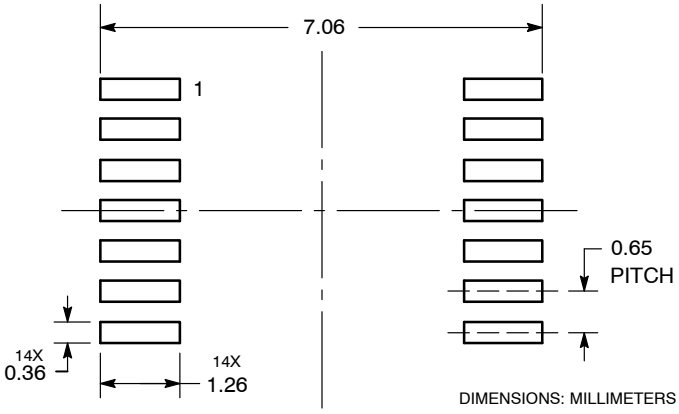
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NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

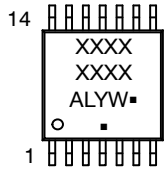
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C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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