# NB6N11S

# 3.3 V 1:2 AnyLevel™ Input to LVDS Fanout Buffer / Translator

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### Description

The NB6N11S is a differential 1:2 Clock or Data Receiver and will accept AnyLevel input signals: LVPECL, CML, LVCMOS, LVTTL, or LVDS. These signals will be translated to LVDS and two identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N11S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6N11S has a wide input common mode range from GND + 50 mV to $V_{CC}$ − 50 mV. Combined with the 50 Ω internal termination resistors at the inputs, the NB6N11S is ideal for translating a variety of differential or single−ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6N11S is functionally equivalent to the EP11, LVEP11, SG11 or 7L11M devices and is offered in a small, 3 mm X 3 mm, 16−QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB6N11S is a member of the ECLinPS MAX™ family of high performance products.

### Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Functionally Compatible with Existing 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb−Free Devices

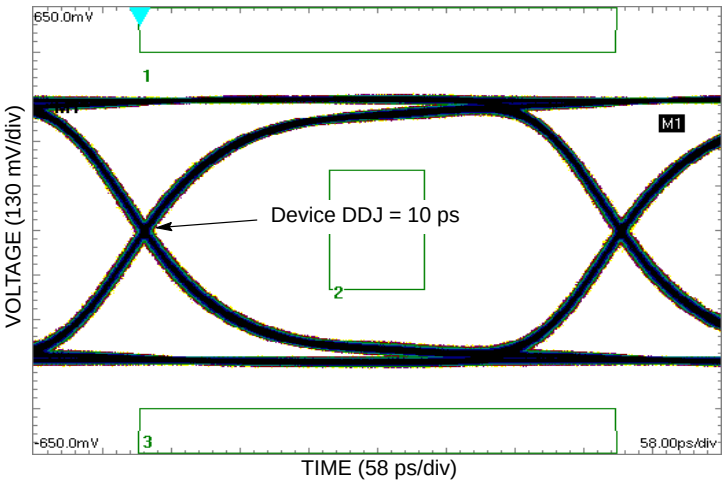
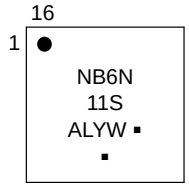



**Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23-1}$ ($V_{INPP}$ = 400 mV; Input Signal DDJ = 14 ps)**



**QFN−16**
**MN SUFFIX**
**CASE 485G**

**MARKING DIAGRAM***




A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

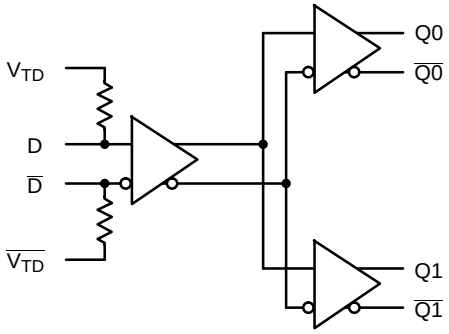



**Figure 1. Logic Diagram**

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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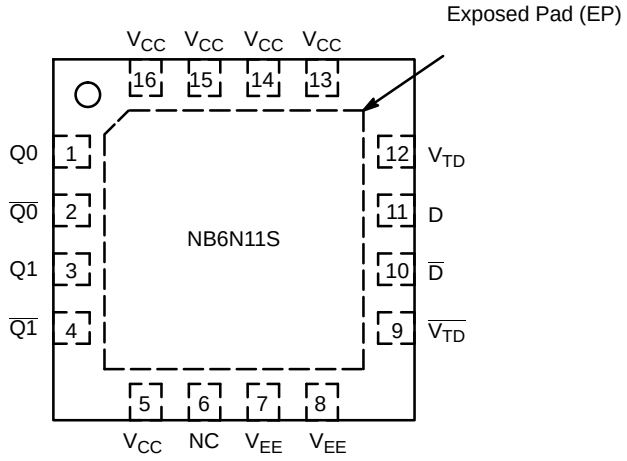



**Figure 3. NB6N11S Pinout, 16−pin QFN** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin | Name | I/O | Description |
|---|---|---|---|
| 1 | Q0 | LVDS Output | Non−inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair. |
| 2 | $\overline{Q0}$ | LVDS Output | Inverted D output. Typically loaded with 10 Ω receiver termination resistor across differential pair. |
| 3 | Q1 | LVDS Output | Non−inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair. |
| 4 | $\overline{Q1}$ | LVDS Output | Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair. |
| 5 | $V_{CC}$ | − | Positive Supply Voltage |
| 6 | NC | | No Connect |
| 7 | $V_{EE}$ | | Negative Supply Voltage |
| 8 | $V_{EE}$ | | Negative Supply Voltage |
| 9 | $\overline{V_{TD}}$ | − | Internal 50 Ω termination pin for $\overline{D}$ |
| 10 | $\overline{D}$ | LVPECL, CML, LVDS, LVCMOS, LVTTL | Inverted Differential Clock/Data Input (Note 1) |
| 11 | D | LVPECL, CML, LVDS, LVCMOS, LVTTL | Non−inverted Differential Clock/Data Input (Note 1) |
| 12 | $V_{TD}$ | − | Internal 50 Ω termination pin for $\overline{D}$ |
| 13 | $V_{CC}$ | − | Positive Supply Voltage |
| 14 | $V_{CC}$ | − | Positive Supply Voltage |
| 15 | $V_{CC}$ | − | Positive Supply Voltage |
| 16 | $V_{CC}$ | − | Positive Supply Voltage |
| EP | | | Exposed pad. The exposed pad (EP) on the package bottom must be attached to a heat−sinking conduit. The exposed pad may only be electrically connected to $V_{EE}$. |

1. In the differential configuration when the input termination pins (VTD/$\overline{VTD}$) are connected to a common termination voltage or left open, and if no signal is applied on D/$\overline{D}$ inputs, then the device will be susceptible to self oscillation.

**Table 2. ATTRIBUTES**

| Characteristics | | Value | |
|---|---|---|---|
| ESD Protection | Human Body Model<br>Machine Model<br>Charged Device Model | > 2 kV<br>> 200 V<br>> 1 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 2) | | Pb Pkg | Pb−Free Pkg |
| | QFN−16 | − | 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in | |
| Transistor Count | | 225 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

2. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive Power Supply | GND = 0 V | | 3.8 | V |
| $V_{IN}$ | Positive Input | GND = 0 V | $V_{IN} \le V_{CC}$ | 3.8 | V |
| $I_{IN}$ | Input Current Through $R_T$ (50 Ω Resistor) | Static<br>Surge | | 35<br>70 | mA<br>mA |
| $I_{OSC}$ | Output Short Circuit Current<br>Line−to−Line (Q to $\overline{Q}$)<br>Line−to−End (Q or $\overline{Q}$ to GND) | <br>Q or $\overline{Q}$<br>Q to $\overline{Q}$ to GND | <br>Continuous<br>Continuous | <br>12<br>24 | mA |
| $T_A$ | Operating Temperature Range | QFN−16 | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 3) | 0 lfpm<br>500 lfpm | QFN−16<br>QFN−16 | 41.6<br>35.2 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 1S2P (Note 3) | QFN−16 | 4.0 | °C/W |
| $T_{sol}$ | Wave Solder Pb<br>Pb−Free | | | 265<br>265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board − 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS** $V_{CC}$ = 3.0 V to 3.6 V, GND = 0 V, $T_A$ = −40°C to +85°C

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{CC}$ | Power Supply Current (Note 8) | | 35 | 50 | mA |
| **DIFFERENTIAL INPUTS DRIVEN SINGLE−ENDED** (Figures 15, 16, 20, and 22) | | | | | |
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 7) | GND +100 | | $V_{CC}$ − 100 | mV |
| $V_{IH}$ | Single−ended Input HIGH Voltage | $V_{th}$ + 100 | | $V_{CC}$ | mV |
| $V_{IL}$ | Single−ended Input LOW Voltage | GND | | $V_{th}$ − 100 | mV |
| **DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 11, 12, 13, 14, 21, and 23) | | | | | |
| $V_{IHD}$ | Differential Input HIGH Voltage | 100 | | $V_{CC}$ | mV |
| $V_{ILD}$ | Differential Input LOW Voltage | GND | | $V_{CC}$ − 100 | mV |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration) | GND + 50 | | $V_{CC}$ − 50 | mV |
| $V_{ID}$ | Differential Input Voltage ($V_{IHD}$ − $V_{ILD}$) | 100 | | $V_{CC}$ | mV |
| $R_{TIN}$ | Internal Input Termination Resistor | 40 | 50 | 60 | Ω |
| **LVDS OUTPUTS** (Note 4) | | | | | |
| $V_{OD}$ | Differential Output Voltage | 250 | | 450 | mV |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 9) | 0 | 1 | 25 | mV |
| $V_{OS}$ | Offset Voltage (Figure 19) | 1125 | | 1375 | mV |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 9) | 0 | 1 | 25 | mV |
| $V_{OH}$ | Output HIGH Voltage (Note 5) | | 1425 | 1600 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 6) | 900 | 1075 | | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 18.
5. $V_{OH}$max = $V_{OS}$max + ½ $V_{OD}$max.
6. $V_{OL}$max = $V_{OS}$min − ½ $V_{OD}$max.
7. $V_{th}$ is applied to the complementary input when operating in single−ended mode.
8. Input termination pins open, D/$\overline{D}$ at the DC level within $V_{CMR}$ and output pins loaded with $R_L$ = 100 Ω across differential.
9. Parameter guaranteed by design verification not tested in production.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 5. AC CHARACTERISTICS** $V_{CC}$ = 3.0 V to 3.6 V, GND = 0 V; (Note 10)

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OUTPP}$ | Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \le 1.0$ GHz<br>(Figure 4) $f_{in}$= 1.5 GHz<br>$f_{in}$= 2.0 GHz | 220<br>200<br>170 | 350<br>300<br>270 | | 250<br>200<br>170 | 350<br>300<br>270 | | 250<br>200<br>170 | 350<br>300<br>270 | | mV |
| $f_{DATA}$ | Maximum Operating Data Rate | 1.5 | 2.5 | | 1.5 | 2.5 | | 1.5 | 2.5 | | Gb/s |
| $t_{PLH}$, $t_{PHL}$ | Differential Input to Differential Output Propagation Delay | 270 | 370 | 470 | 270 | 370 | 470 | 270 | 370 | 470 | ps |
| $t_{SKEW}$ | Duty Cycle Skew (Note 11)<br>Within Device Skew (Note 16)<br>Device−to−Device Skew (Note 15) | | 8<br>5<br>30 | 45<br>25<br>100 | | 8<br>5<br>30 | 45<br>25<br>100 | | 8<br>5<br>30 | 45<br>25<br>100 | ps |
| $t_{JITTER}$ | RMS Random Clock Jitter (Note 13) $f_{in}$ = 1.0 GHz<br>$f_{in}$ = 1.5 GHz<br>Deterministic Jitter (Note 14) $f_{DATA}$ = 622 Mb/s<br>$f_{DATA}$ = 1.5 Gb/s<br>$f_{DATA}$ = 2.488 Gb/s | | 0.5<br>0.5<br>6<br>7<br>10 | 1<br>1<br><br>20<br>20 | | 0.5<br>0.5<br>6<br>7<br>10 | 1<br>1<br><br>20<br>20 | | 0.5<br>0.5<br>6<br>7<br>10 | 1<br>1<br><br>20<br>20 | ps |
| $V_{INPP}$ | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12) | 100 | | $V_{CC}$− GND | 100 | | $V_{CC}$− GND | 100 | | $V_{CC}$− GND | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times @ 250 MHz Q, $\overline{Q}$<br>(20% − 80%) | 70 | 120 | 170 | 70 | 120 | 170 | 70 | 120 | 170 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing $V_{INPPmin}$ with 50% duty cycle clock source and $V_{CC}$ − 1400 mV offset. All loading with an external $R_L$ = 100 Ω across "D" and "$\overline{D}$" of the receiver. Input edge rates 150 ps (20%−80%).
11. See Figure 17 differential measurement of $t_{skew} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform @ 250 MHz.
12. Input voltage swing is a single−ended measurement operating in differential mode.
13. RMS jitter with 50% Duty Cycle clock signal at 750 MHz.
14. Deterministic jitter with input NRZ data at PRBS $2^{23}$−1 and K28.5.
15. Skew is measured between outputs under identical transition @ 250 MHz.
16. The worst case condition between Q0/$\overline{Q0}$ and Q1/$\overline{Q1}$ from D, $\overline{D}$, when both outputs have the same transition.

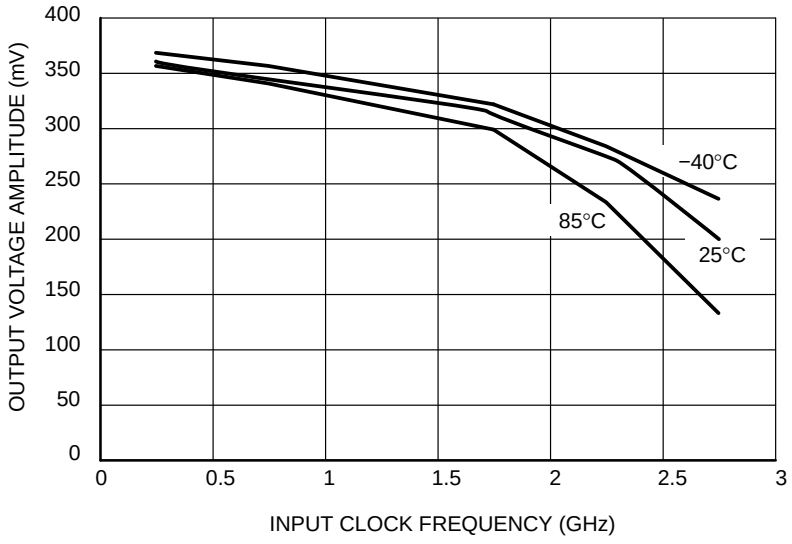



**Figure 4. Output Voltage Amplitude ($V_{OUTPP}$) versus Input Clock Frequency ($f_{in}$) and Temperature (@ $V_{CC}$ = 3.3 V)**

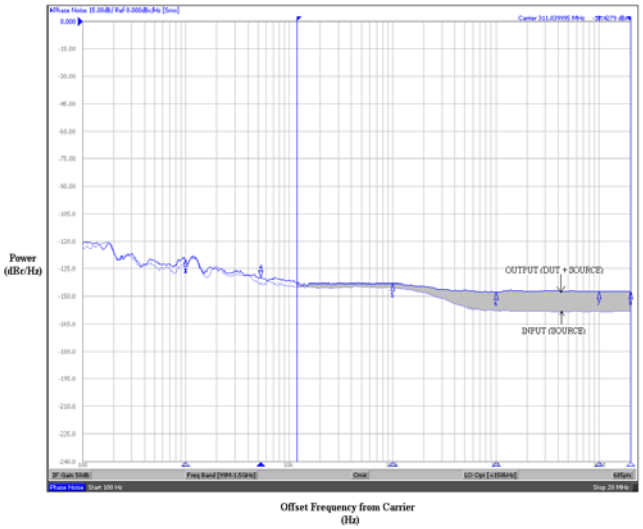



**Figure 5. Typical Phase Noise Plot at $f_{carrier}$ = 311.04 MHz**

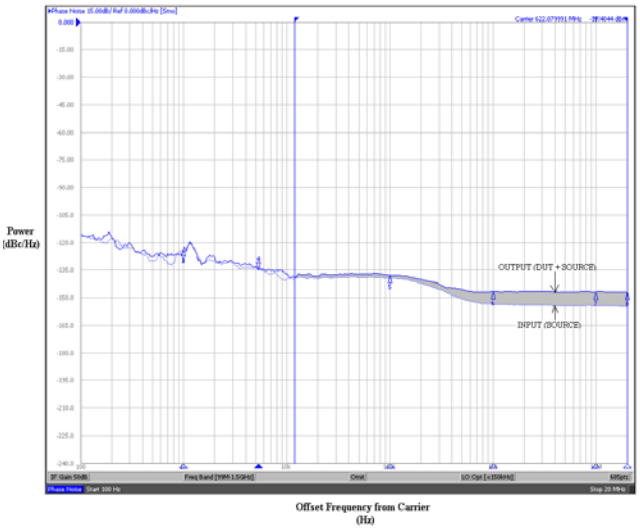



**Figure 6. Typical Phase Noise Plot at $f_{carrier}$ = 622.08 MHz**

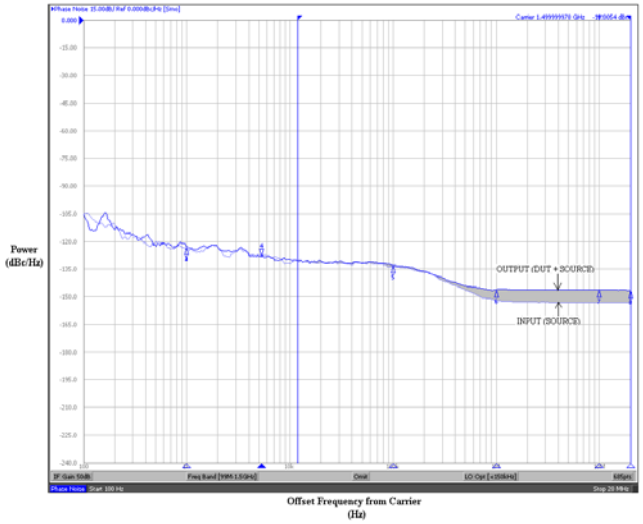



**Figure 7. Typical Phase Noise Plot at $f_{carrier}$ = 1.5 GHz**

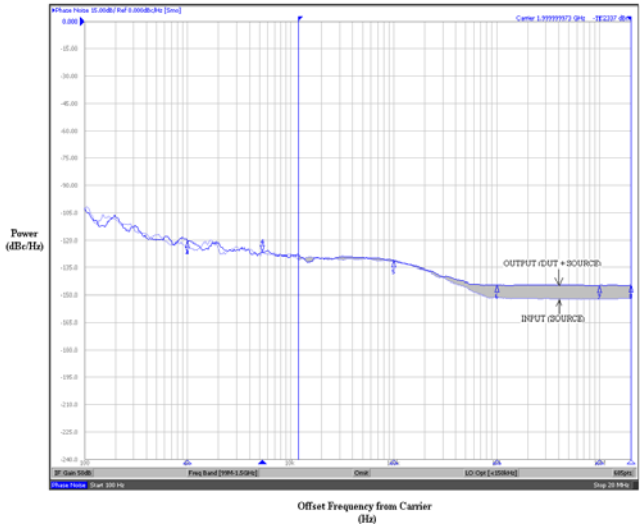



**Figure 8. Typical Phase Noise Plot at $f_{carrier}$ = 2 GHz**

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6N11S device at frequencies 311.04 MHz, 622.08 MHz, 1.5 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 96 fs, 40 fs, 15 fs and 14 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

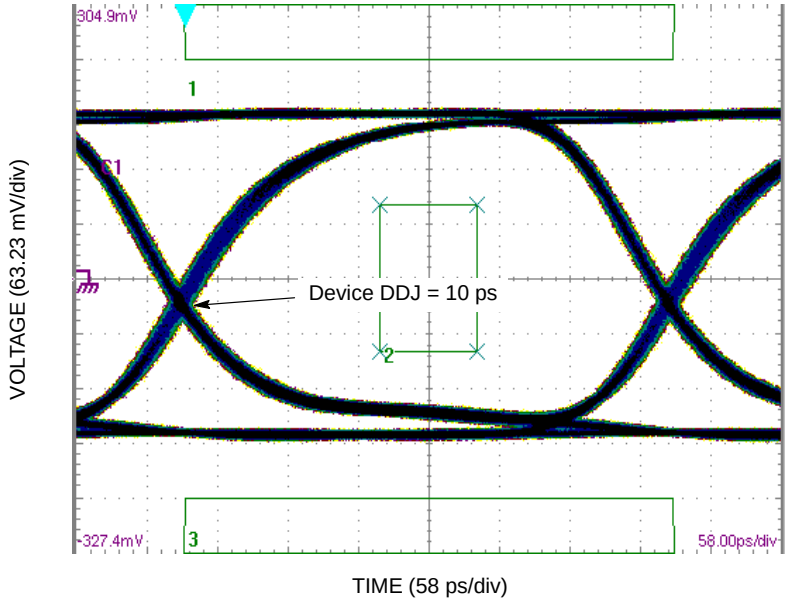



**Figure 9. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23-1}$ and OC48 mask ($V_{INPP}$ = 100 mV; Input Signal DDJ = 14 ps)**

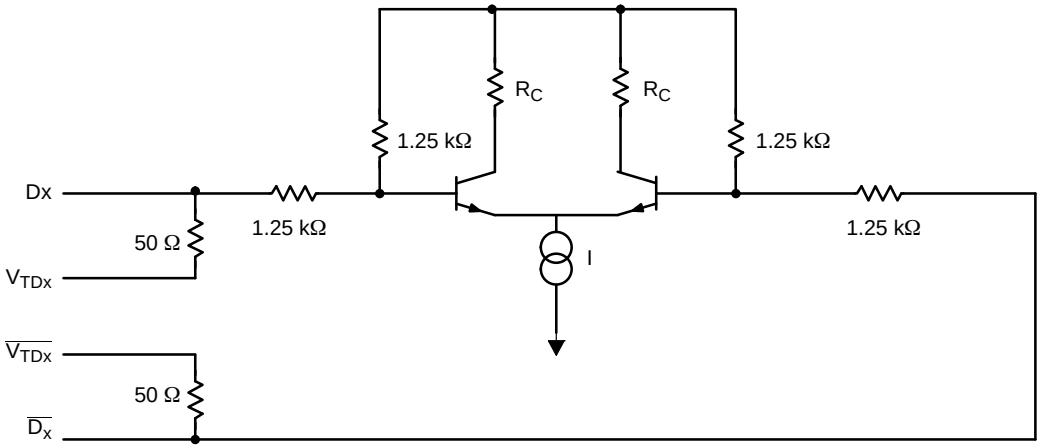



**Figure 10. Input Structure**

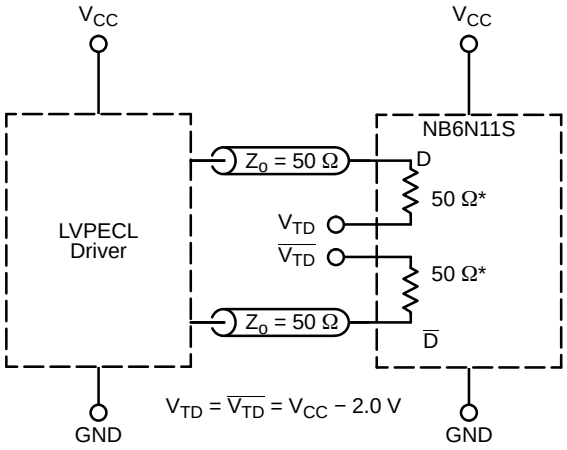



**Figure 11. LVPECL Interface**

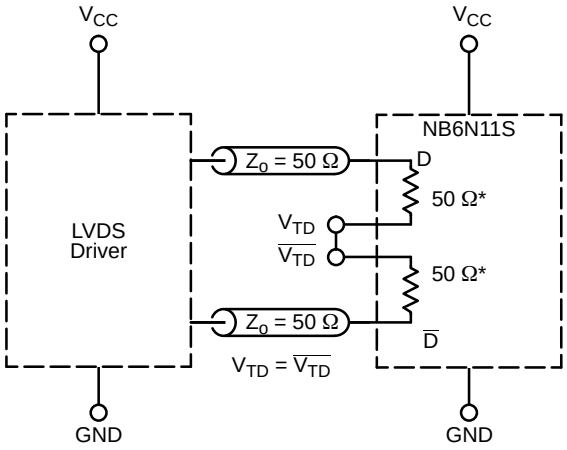



**Figure 12. LVDS Interface**

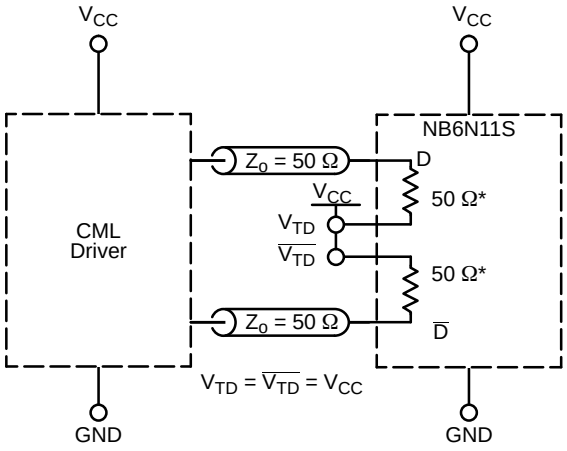



**Figure 13. Standard 50 Ω Load CML Interface**

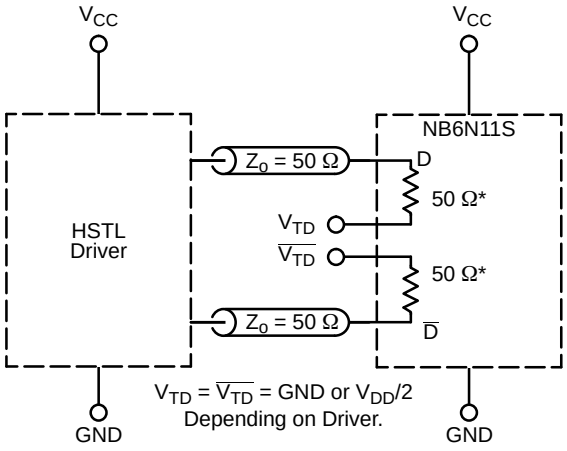



**Figure 14. HSTL Interface**

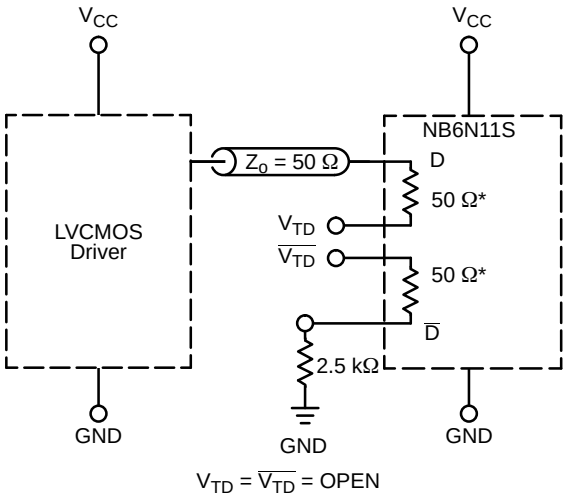



**Figure 15. LVCMOS Interface**

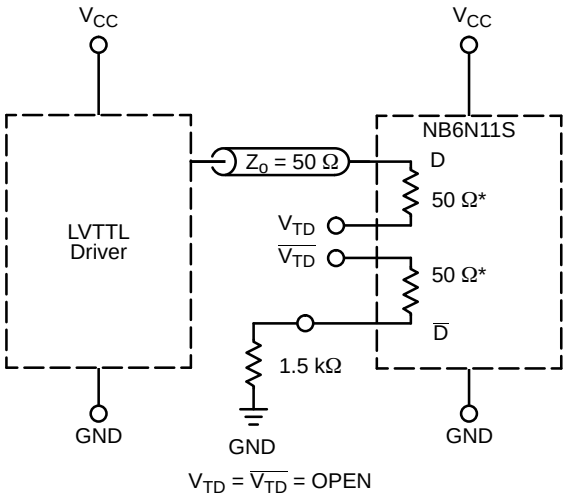



**Figure 16. LVTTL Interface**

*$R_{TIN}$, Internal Input Termination Resistor.

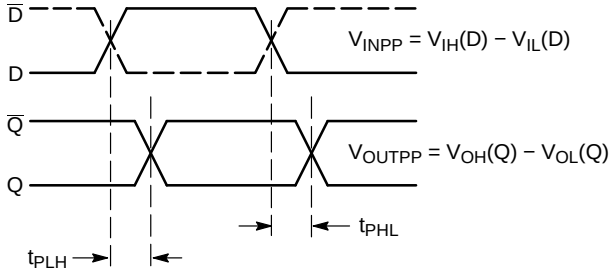



**Figure 17. AC Reference Measurement**

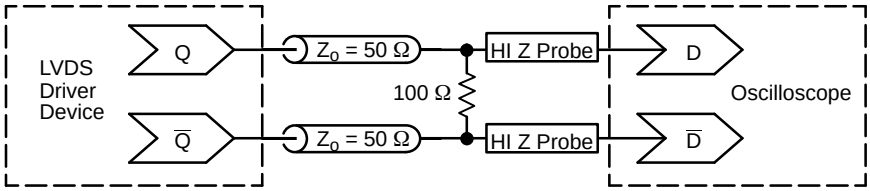



**Figure 18. Typical LVDS Termination for Output Driver and Device Evaluation**

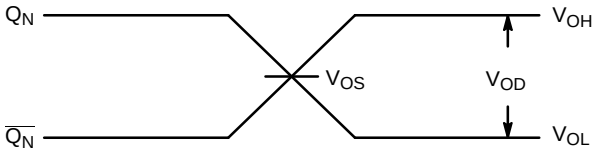



**Figure 19. LVDS Output**

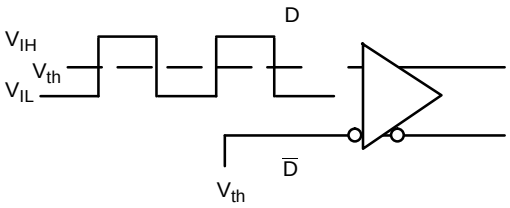



**Figure 20. Differential Input Driven Single−Ended**

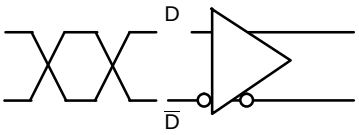



**Figure 21. Differential Inputs Driven Differentially**

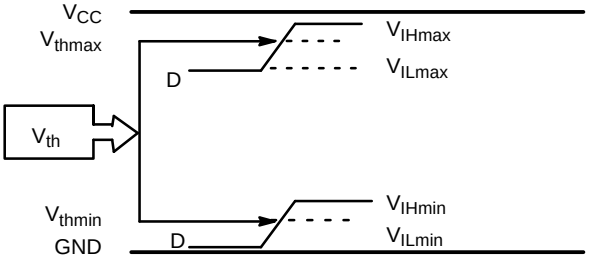



**Figure 22. $V_{th}$ Diagram**

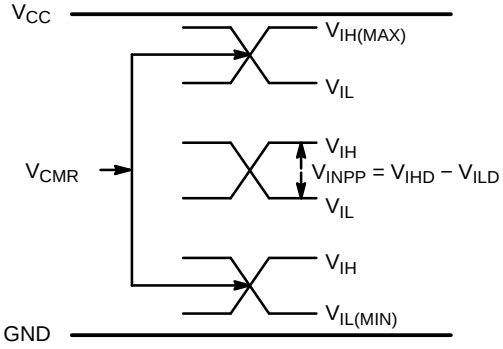



**Figure 23. $V_{CMR}$ Diagram**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB6N11SMNG | QFN−16, 3 X 3 mm (Pb−Free) | 123 Units / Rail |
| NB6N11SMNR2G | QFN−16, 3 X 3 mm (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

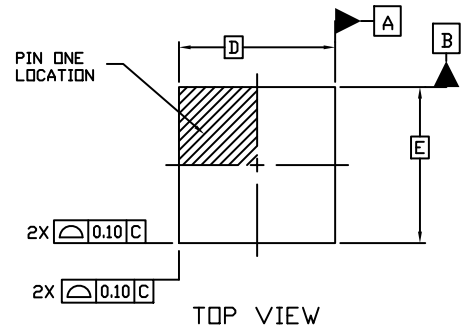
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# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

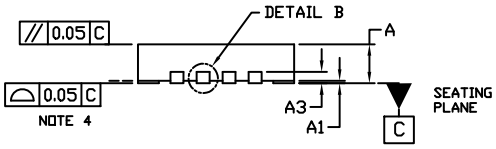
**QFN16 3x3, 0.5P**
CASE 485G
ISSUE G

DATE 08 OCT 2021

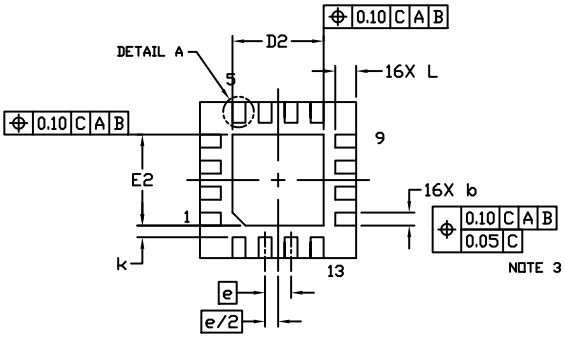
**SCALE 2:1**




TOP VIEW

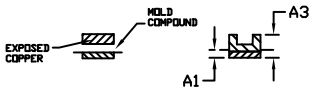



SIDE VIEW

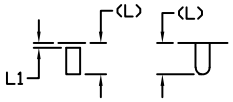



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



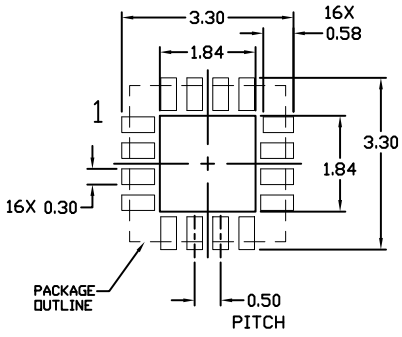

DETAIL B
ALTERNATE CONSTRUCTIONS




DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.03 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.18 | 0.24 | 0.30 |
| D | | 3.00 BSC | |
| D2 | 1.65 | 1.75 | 1.85 |
| E | | 3.00 BSC | |
| E2 | 1.65 | 1.75 | 1.85 |
| e | | 0.50 BSC | |
| k | | 0.18 TYP | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | 0.08 | 0.15 |

MOUNTING FOOTPRINT




### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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