

2.5 V/3.3 V 1:8 CML Fanout

Multi-Level Inputs w/ Internal Termination

NB7L1008M

Description

The NB7L1008M is a high performance differential 1:8 Clock/Data fanout buffer. The NB7L1008M produces eight identical output copies of Clock or Data operating up to 6 GHz or 10.7 Gb/s, respectively. As such, the NB7L1008M is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB7L1008M to accept various logic standards, such as LVPECL, CML, LVDS, LVC MOS or LVTTL logic levels. The V_{REFAC} reference output can be used to rebias capacitor-coupled differential or single-ended input signals. The 1:8 fanout design was optimized for low output skew applications. The NB7L1008M is a member of the GigaComm™ family of high performance clock products.

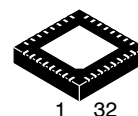
Features

- Input Data Rate > 12 Gb/s Typical
- Data Dependent Jitter < 20 ps
- Maximum Input Clock Frequency > 8 GHz Typical
- Random Clock Jitter < 0.8 ps RMS
- Low Skew 1:8 CML Outputs, < 25 ps max
- Multi-Level Inputs, accepts LVPECL, CML, LVDS
- 160 ps Typical Propagation Delay
- 45 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 2.375$ V to 3.6 V, GND = 0 V
- Internal Input Termination Resistors, 50 Ω
- V_{REFAC} Reference Output
- QFN-32 Package, 5 mm x 5 mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



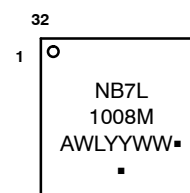
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QFN32
MN SUFFIX
CASE 488AM

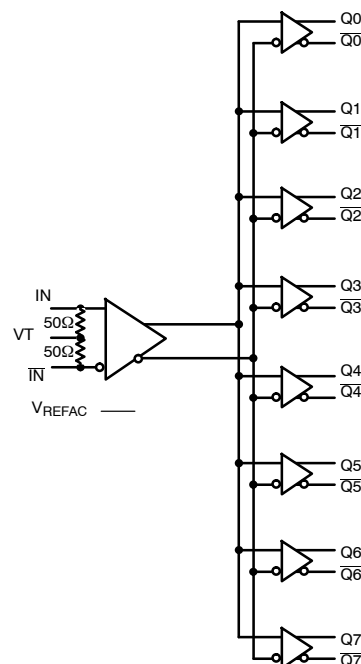
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
• = Pb-Free Package

(Note: Microdot may be in either location)

SIMPLIFIED LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NB7L1008M

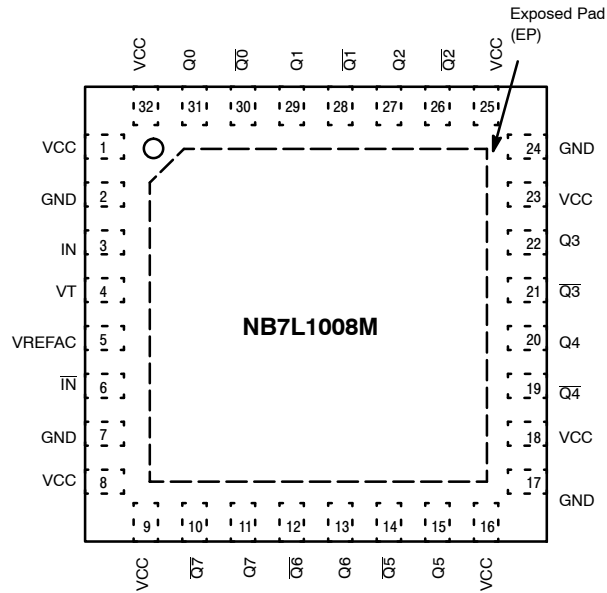


Figure 1. 32-Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
3, 6	IN, $\overline{\text{IN}}$	LVPECL, CML, LVDS Input	Non-inverted / Inverted Differential Clock/Data Input. Note 1
4	VT		Internal 50 Ω Termination Pin for IN and $\overline{\text{IN}}$
2, 7 17,24	GND		Negative Supply Voltage. (Note 2)
1, 8, 9, 16, 18, 23, 25, 32	V _{CC}		Positive Supply Voltage. (Note 2)
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, $\overline{\text{Q0}}$, Q1, $\overline{\text{Q1}}$, Q2, $\overline{\text{Q2}}$, Q3, $\overline{\text{Q3}}$, Q4, $\overline{\text{Q4}}$, Q5, $\overline{\text{Q5}}$, Q6, $\overline{\text{Q6}}$, Q7, $\overline{\text{Q7}}$	CML	Non-inverted / Inverted Differential Output. (Note 1)
5	VREFAC		Output Voltage Reference for Capacitor-Coupled Inputs, only
–	EP	–	The Exposed Pad (EP) on the QFN-24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to GND and is recommended to be electrically connected to GND on the PC board.

1. In the differential configuration when the input termination pin (V_T) is connected to a common termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$, then the device will be susceptible to self-oscillation. Q_n/ $\overline{\text{Qn}}$ outputs have internal 50 Ω source termination resistors.
2. All V_{CC} and GND pins must be externally connected to the same power supply voltage to guarantee proper device operation.

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Table 2. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity (Note 3) Indefinite Time of the Drypack QFN-32	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	263
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

3. For additional information, refer to Application Note [AND8003/D](#).

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{IN}	Input Voltage	GND = 0 V		-0.5 to V_{CC}	V
V_{INPP}	Differential Input Voltage $ I_N - \bar{I}_N $			1.89	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			± 40	mA
I_{out}	Output Current	Continuous Surge		34 40	mA
I_{VREFAC}	V_{REFAC} Sink/Source Current			± 1.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4) TGSD 51-6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-32	12	°C/W
T_{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS – CML OUTPUT $V_{CC} = 2.375 \text{ V to } 3.6 \text{ V}$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (Note 6)

Symbol	Characteristic	Min	Typ	Max	Unit
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POWER SUPPLY

V_{CC}	Power Supply Voltage	$V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$	3.0 2.375	3.3 2.5	3.6 2.625	V
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POWER SUPPLY CURRENT

I_{CC}	Power Supply Current, Inputs and Outputs Open		265	315		mA
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CML OUTPUTS (Note 5, Figures 10 and 11)

V_{OH}	Output HIGH Voltage	$V_{CC} = 3.3\text{V}$ $V_{CC} = 2.5\text{V}$	$V_{CC} - 30$ 3270 2470	$V_{CC} - 10$ 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage	$V_{CC} = 3.3\text{V}$ $V_{CC} = 2.5\text{V}$	$V_{CC} - 600$ 2700 1900	$V_{CC} - 400$ 2900 2100	$V_{CC} - 350$ 2950 2150	mV

DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Notes 7 and 8) (Figures 6 and 8)

V_{IH}	Single-Ended Input HIGH Voltage	$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-Ended Input LOW Voltage	GND		$V_{th} - 100$	mV
V_{th}	Input Threshold Reference Voltage Range	1100		$V_{CC} - 100$	mV
V_{ISE}	Single-Ended Input Voltage ($V_{IH} - V_{IL}$)	200		1200	mV

V_{REFAC}

V_{REFAC}	Output Reference Voltage @ 100 μA for Capacitor – Coupled Inputs, Only	$V_{CC} = 3.3 \text{ V}$ $V_{CC} = 2.5 \text{ V}$	$V_{CC} - 1375$ $V_{CC} - 1325$	$V_{CC} - 1200$ $V_{CC} - 1200$	$V_{CC} - 1100$ $V_{CC} - 1075$	mV
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DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (I_N , $\bar{I}_N$) (Note 9) (Figures 4 and 7)

V_{IHD}	Differential Input HIGH Voltage	1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{IHD} - 100$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	100		1200	mV
I_{IH}	Input HIGH Current	-150	40	+150	μA
I_{IL}	Input LOW Current	-150	5	+150	μA

TERMINATION RESISTORS

R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

5. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
6. Input and output parameters vary 1:1 with V_{CC} .
7. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
8. V_{th} is applied to the complementary input when operating in single-ended mode.
9. V_{IHD} , V_{ILD} , V_{ID} , and V_{CMR} parameters must be complied with simultaneously.

Table 5. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{DATA}	Maximum Operating Input Data Rate	10	12		Gb/s
f_{INCLK}	Maximum Input Clock Frequency, $V_{\text{OUTPP}} \geq 200\text{ mV}$	6	8		GHz
V_{OUTPP}	Output Voltage Amplitude (see Figures 2 and 5, Note 11) $f_{\text{in}} \leq 4\text{ GHz}$ $f_{\text{in}} \leq 6\text{ GHz}$	200 200	400 350		mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 12, Figure 9)	600		$V_{CC} - 50$	mV
$t_{\text{PLH}}, t_{\text{PHL}}$	Propagation Delay to Output Differential, $\text{IN}/\overline{\text{IN}}$ to $\text{Qn}/\overline{\text{Qn}}$	100	160	250	ps
$t_{\text{PLH TC}}$	Propagation Delay Temperature Coefficient $-40^\circ\text{C to }+85^\circ\text{C}$		35		fs/ $^\circ\text{C}$
t_{DC}	Output Clock Duty Cycle $f_{\text{in}} \leq 6\text{ GHz}$	45	49/51	55	%
t_{SKEW}	Duty Cycle Skew (Note 13) Within Device Skew (Note 14) Device to Device Skew (Note 15)		0.15 7 25	1 25 70	ps
t_{JITTER}	Clock Jitter RMS, 1000 Cycles (Note 16) $f_{\text{in}} \leq 6\text{ GHz}$ Data Dependent Jitter (DDJ) (Note 17) $\leq 10\text{ Gb/s}$		0.2 3	0.8 20	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 18) (Figure 5)	100		1200	mV
t_r, t_f	Output Rise/Fall Times (20% – 80%) $\text{Qn}, \overline{\text{Qn}}$	20	45	70	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

10. Measured using a 400 mV source, 50% duty cycle 1 GHz clock source. All outputs must be loaded with external $50\ \Omega$ to V_{CC} . Input edge rates 40 ps (20% – 80%).

11. Output voltage swing is a single-ended measurement operating in differential mode.

12. $V_{\text{IHD}_{\text{MIN}}} \geq 1100\text{ mV}$.

13. Duty cycle skew is measured between differential outputs using the deviations of the sum of $T_{\text{pw-}}$ and $T_{\text{pw+}}$ @ 1 GHz.

14. Within device skew compares coincident edges.

15. Device to device skew is measured between outputs under identical transition

16. Additive CLOCK jitter with 50% duty cycle clock signal.

17. Additive Peak-to-Peak jitter with input NRZ data at PRBS23.

18. Input voltage swing is a single-ended measurement operating in differential mode.

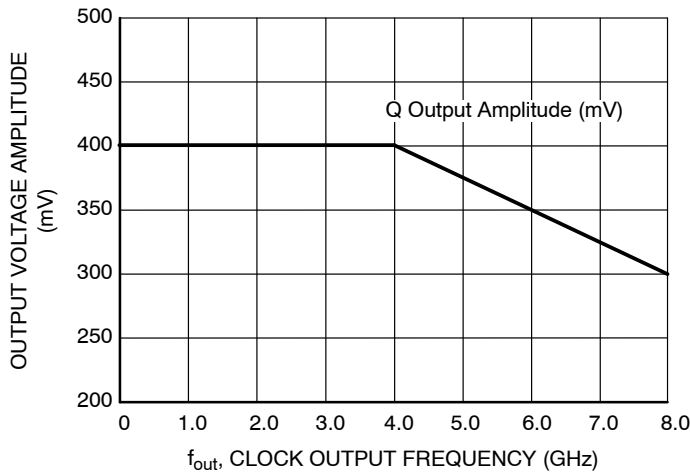


Figure 2. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)

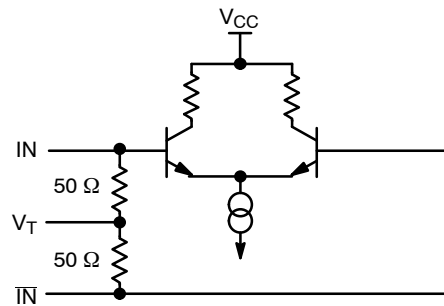


Figure 3. Input Structure

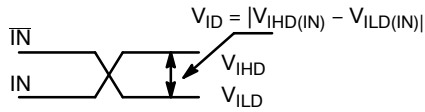


Figure 4. Differential Inputs Driven Differentially

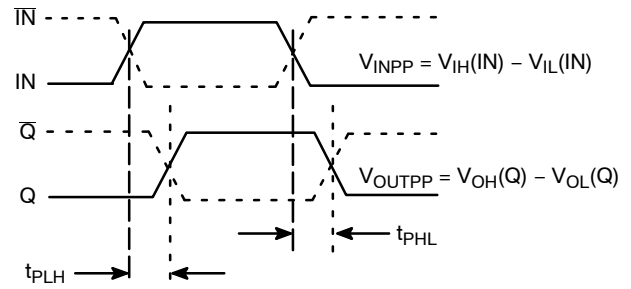


Figure 5. AC Reference Measurement

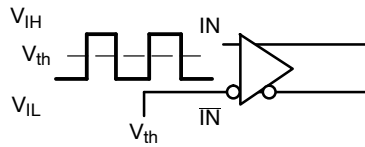


Figure 6. Differential Input Driven Single-Ended

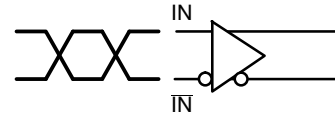


Figure 7. Differential Inputs Driven Differentially

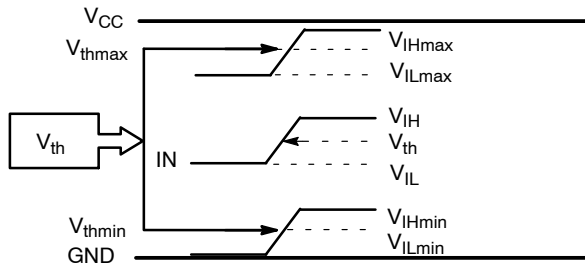


Figure 8. V_{th} Diagram

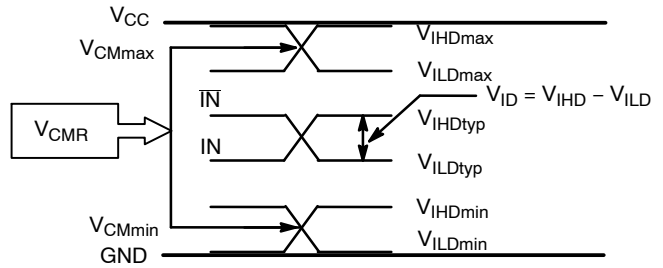


Figure 9. V_{CM} Diagram

NB7L1008M

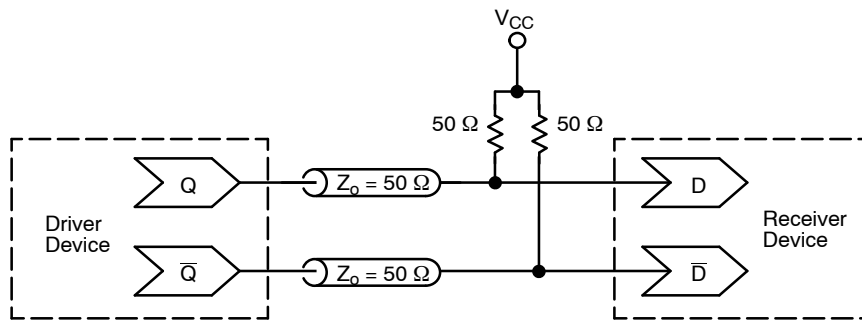


Figure 10. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8173/D](#))

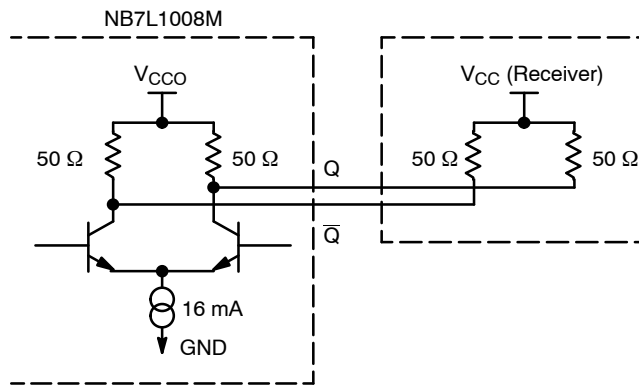


Figure 11. Typical CML Output Structure and Termination

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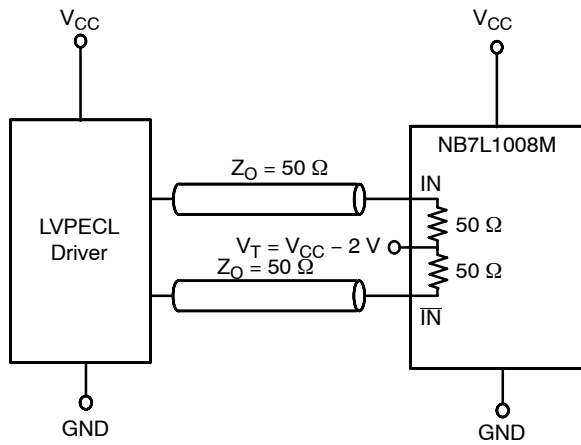


Figure 12. LVPECL Interface

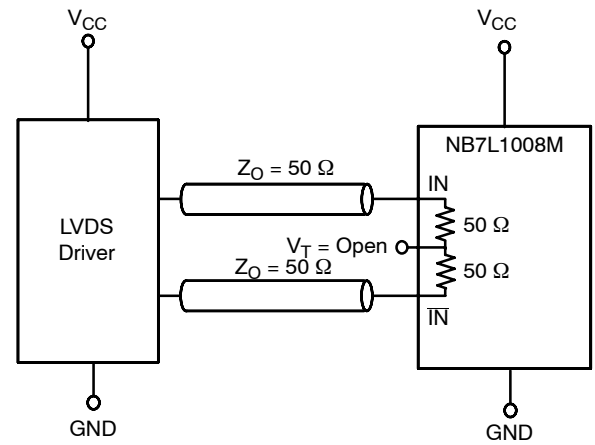


Figure 13. LVDS Interface

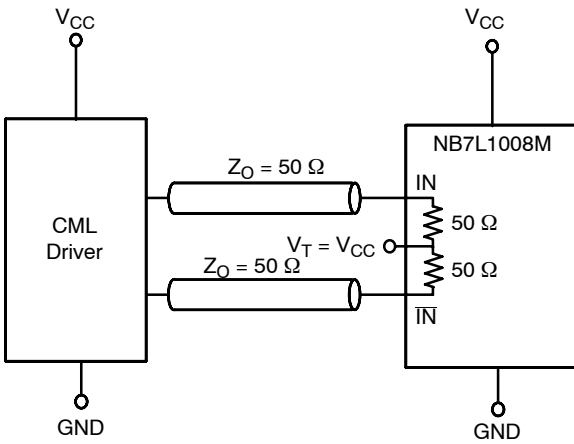


Figure 14. Standard 50 Ω Load CML Interface

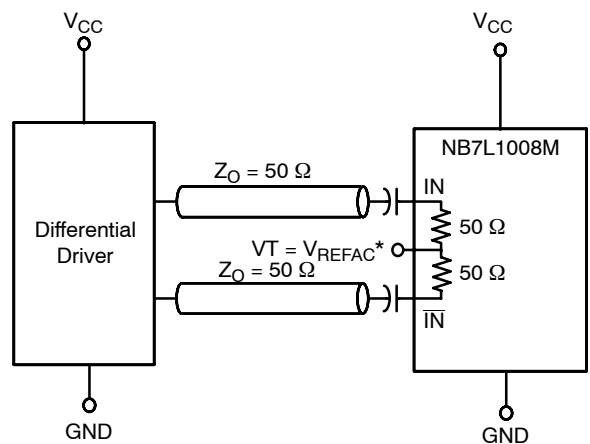


Figure 15. Capacitor-Coupled Differential Interface
(V_T Connected to V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μ F capacitor

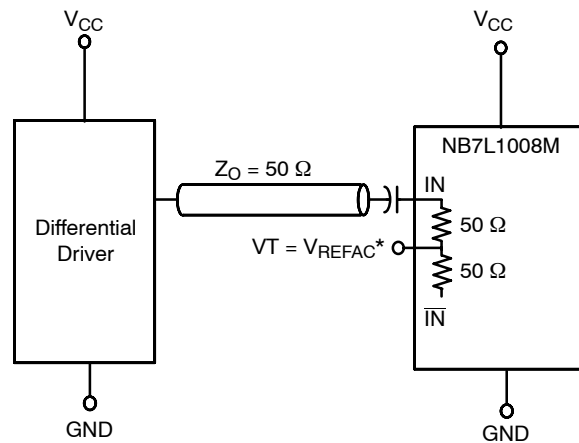


Figure 16. Capacitor-Coupled Single-Ended Interface
(V_T Connected to V_{REFAC})

NB7L1008M

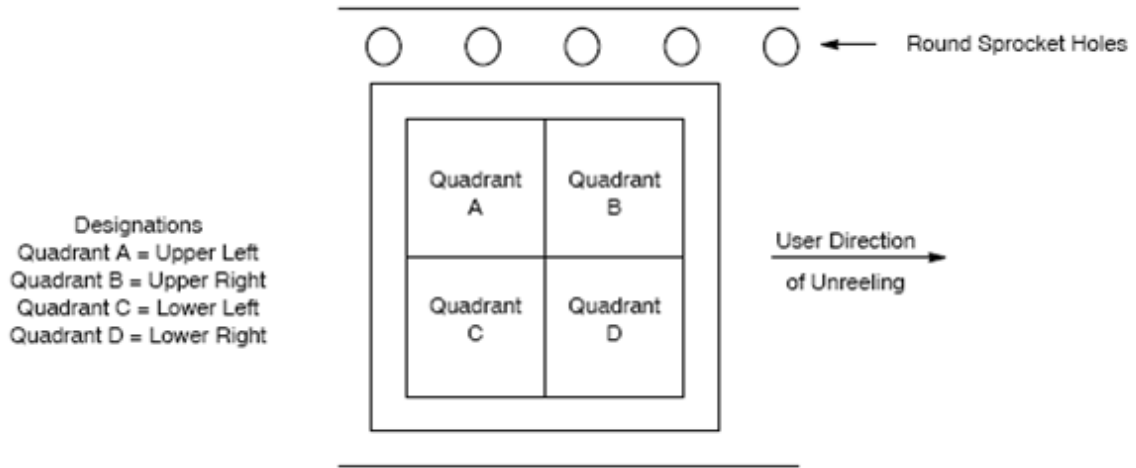
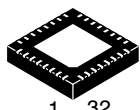


Figure 17. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

Device	Package	Shipping
NB7L1008MMNG	QFN32 (Pb-Free)	74 Units / Tube
NB7L1008MMNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 17)

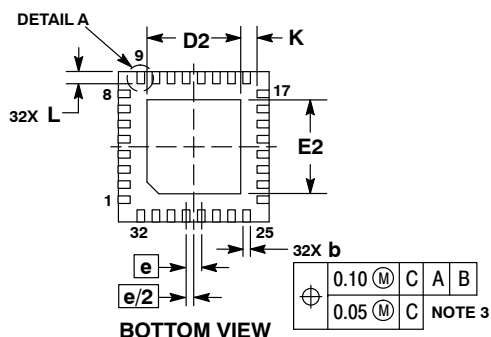
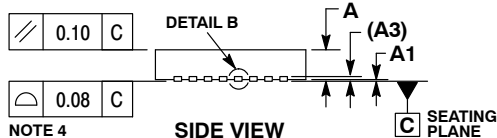
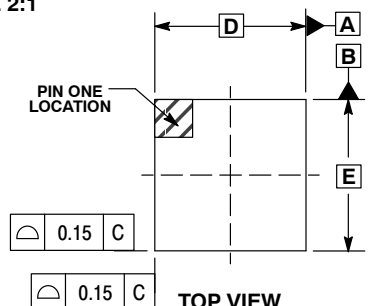
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



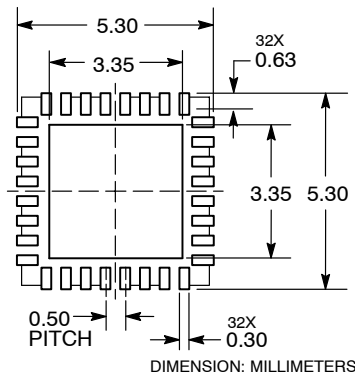
1 32
SCALE 2:1

QFN32 5x5, 0.5P CASE 488AM ISSUE A

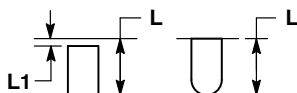
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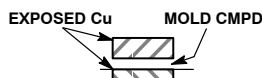
RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



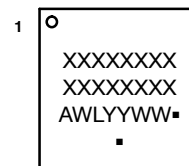
DETAIL B
ALTERNATE
CONSTRUCTION

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1		0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	
L	0.30	0.50
L1		0.15

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	QFN32 5x5 0.5P	PAGE 1 OF 1

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