NCL30073

Current-Mode PWM Controller for LED Application

The NCL30073 is a highly integrated PWM controller capable of delivering a rugged and high performance LED converter in a tiny TSOP−6 package. With a supply range up to 24 V, the controller hosts a 65 kHz switching circuitry operated in peak current mode control. When the voltage on FB pin decreases, the controller enters skip cycle while limiting the peak current.

Over Power Protection (OPP) is a difficult exercise especially when no−load standby requirements drive the converter specifications. The ON proprietary integrated OPP lets you harness the maximum delivered power without affecting your standby performance simply via two external resistors. An Over Voltage Protection is also combined on the same pin but also on the V_{CC} line. They offer an efficient protection in case of adverse open loop operation.

Finally, a timer−based short−circuit protection offers the best protection scheme, letting you precisely select the protection trip point without caring of a loose coupling between the auxiliary and the power windings.

Features

- Fixed−frequency 65 kHz Current−mode Control Operation
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Internal Ramp Compensation
- Internally Fixed 4 ms Soft−start
- 115 ms Timer−based Auto−recovery Short−circuit Protection
- Protection − Autorecovery
  - OVP by V_{CC}
  - OIP
  - OTP − Foldback
  - Short Circuit
- Up to 24 V V_{CC} Operation
- Extremely Low No−load Standby Power
- Isolated and Non−isolated Outputs
- Good Regulation – 5%
- High Power Factor > 0.9
- Single Winding Inductor
- Low Parts Count
- EPS 2.0 Compliant
- Pb−Free Devices
- +300 mA/ −500 mA Source/Sink Drive Capability

Typical Application

- Dimmable Retrofit and Low Power Fixture LED Applications
- Phase Cut Dimmer Compatible – LE or TE Types
- Multiple Topology Support
  - Buck
  - Buck Boost
  - Flyback

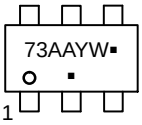
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TSOP−6
CASE 318G−02

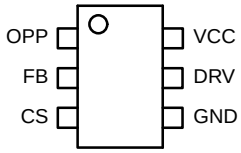
MARKING DIAGRAM



73A = Specific Device Code
A =Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



TSOP−6 (Top view)

ORDERING INFORMATION

Device	Package	Shipping†
NCL30073SN065T1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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TYPICAL APPLICATION SCHEMATIC

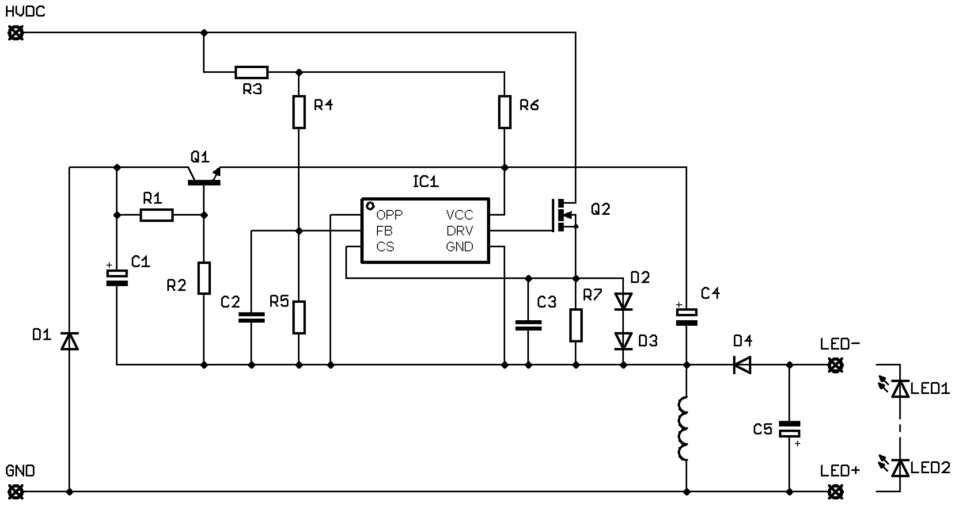


Figure 1. Typical Non−isolated (Buck−Boost) Application

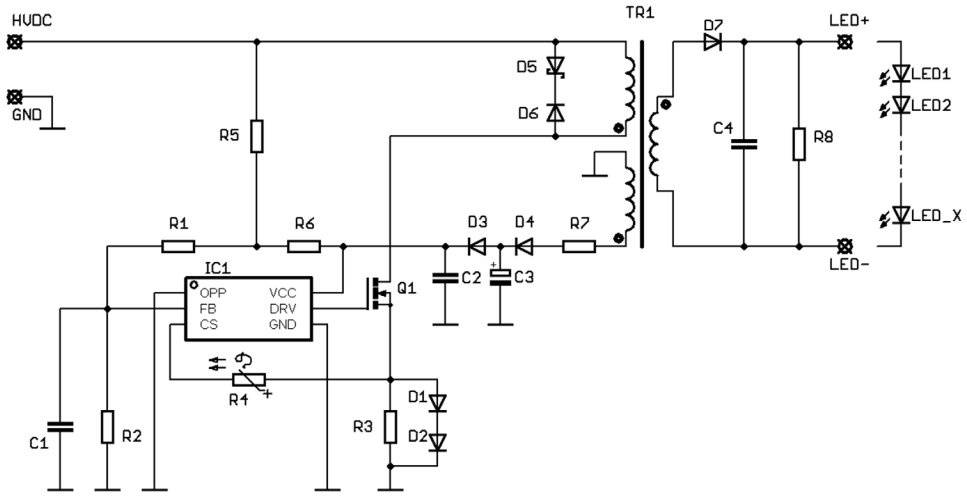


Figure 2. Typical Isolated (Flyback) Application Example

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	OPP	Adjust the Over Power Protection	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part enters auto−recovery mode.
2	FB	Feedback pin	A voltage variation on this pin will allow regulation.
3	CS	Current Sense + Slope Compensation	This pin monitors the primary peak current but also offers a means to introduce slope compensation.
4	GND		The controller ground.
5	DRV	Driver Output	The driver output to an external MOSFET gate.
6	V_{CC}	Supplies the Controller − Protects the IC	This pin is connected to an external auxiliary voltage. When the V_{CC} exceeds a certain level, the part enters an auto−recovery hiccup mode.

INTERNAL CIRCUIT ARCHITECTURE

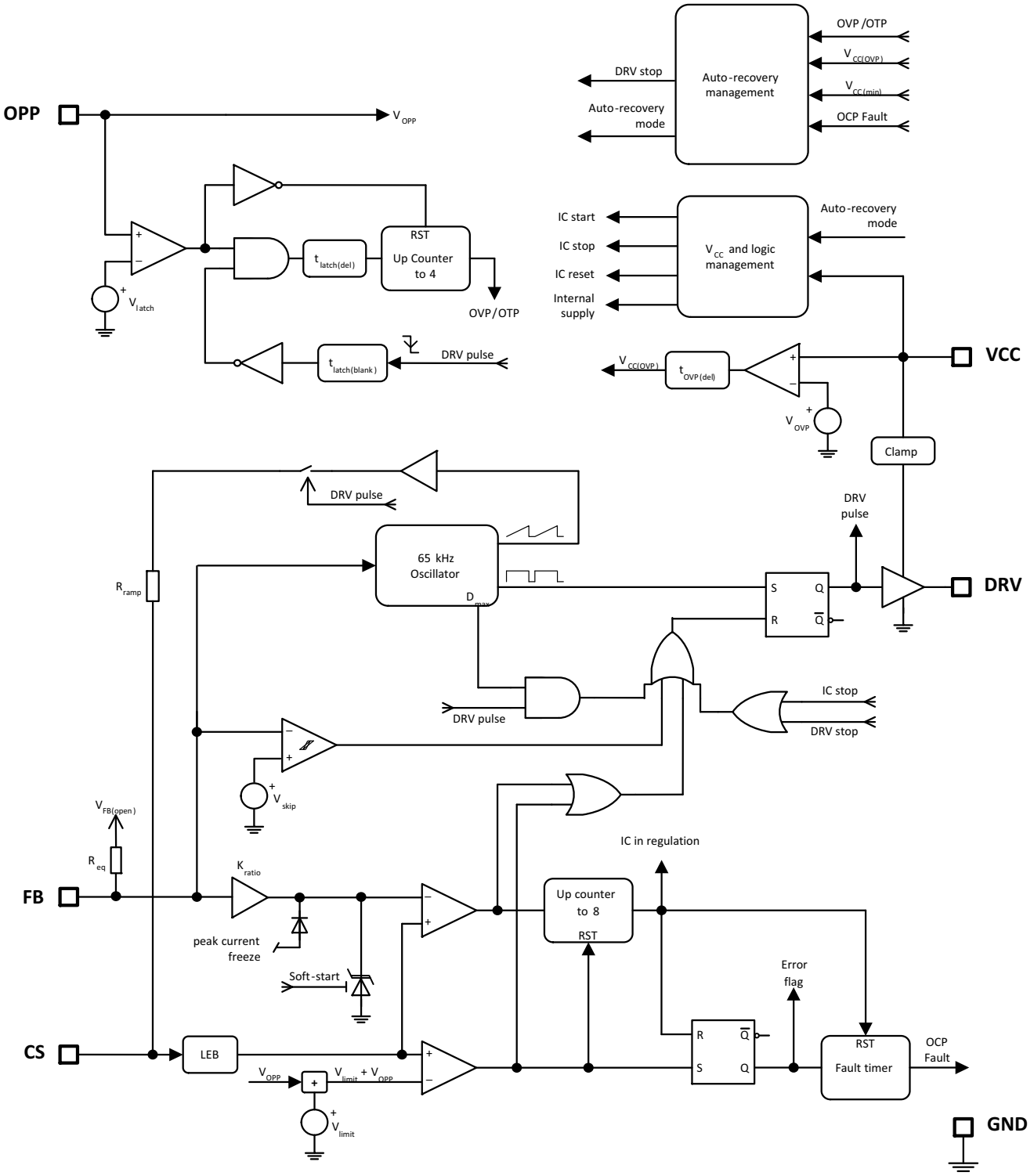


Figure 3. Internal Circuit Architecture

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Units
V_{CC}	Power Supply voltage, VCC pin, continuous voltage	−0.3 to 35	V
$V_{DRV(tran)}$	Maximum DRV pin voltage when DRV in H state, transient voltage (Note 1)	−0.3 to V_{CC} + 0.3	V
V_{CS}, V_{FB}, V_{OPP}	Maximum voltage on low power pins CS, FB and OPP (Note 2)	−0.3 to 5.5	V
$V_{OPP(tran)}$	Maximum negative transient voltage on OPP pin (Note 2)	−1	V
$I_{source,max}$	Maximum sourced current, pulsed width < 800 ns	0.6	A
$I_{sink,max}$	Maximum sinked current, pulse width < 800 ns	1.0	A
I_{OPP}	Maximum injected negative current into the OPP pin (pin 1)	−2	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	360	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−60 to +150	°C
HBM	Human Body Model ESD Capability per JEDEC JESD22−A114F (All pins)	4	kV
CDM	Charged−Device Model ESD Capability per JEDEC JESD22−C101E	750	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The transient voltage is a voltage spike injected to DRV pin being in high state. Maximum transient duration is 100 ns.
2. See the Figure 4 for detailed specification of transient voltage.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

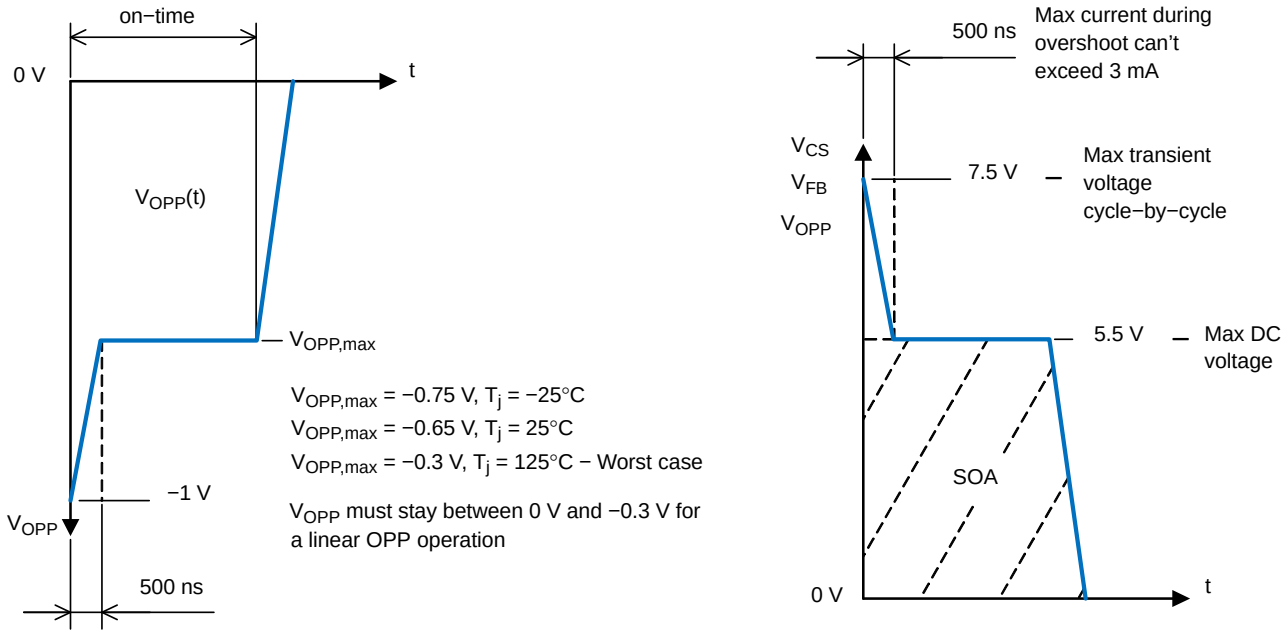


Figure 4. Negative Pulse for OPP Pin during On−time and Positive Pulse for all Low Power Pins

Table 3. ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.

Symbol	Rating	Pin	Min	Typ	Max	Units
SUPPLY SECTION						
$V_{CC(on)}$	V_{CC} increasing level at which driving pulses are authorized	6	16	18	20	V
$V_{CC(min)}$	V_{CC} decreasing level at which driving pulses are stopped	6	8.3	8.9	9.5	V
$V_{CC(hyst)}$	Hysteresis $V_{CC(on)} - V_{CC(min)}$	6	7.7	−	−	V
$V_{CC(reset)}$	Auto−recovery state reset voltage	6	−	8.6	−	V
$V_{CC(reset_hyst)}$	Defined hysteresis between minimum and reset voltage $V_{CC(min)} - V_{CC(reset)}$	6	0.15	0.30	0.45	V
I_{CC1}	Start−up current ($V_{CC(on)}$ − 100 mV)	6	−	6	10	μA
I_{CC2}	Internal IC consumption with V_{FB} = 3.2 V, f_{SW} = 65 kHz and C_L = 0 nF	6	−	1.0	1.4	mA
I_{CC3}	Internal IC consumption with V_{FB} = 3.2 V, f_{SW} = 65 kHz and C_L = 1 nF	6	−	1.8	2.7	mA
$I_{CC(no-load)}$	Internal consumption in skip mode – non switching, V_{FB} = 0 V	6	−	300	−	μA
$I_{CC(fault)}$	Internal consumption in fault mode – during going−down V_{CC} cycle, V_{FB} = 4 V	6	0.6	0.9	1.2	mA
$I_{CC(standby)}$	Internal IC consumption in skip mode for 65 kHz version (V_{CC} = 14 V, driving a typical 7 A / 600 V MOSFET, includes FB pin current) – (Note 5)	6	−	420	−	μA
DRIVE OUTPUT						
t_r	Output voltage rise−time @ C_L = 1 nF, 10−90% of output signal	5	−	25	−	ns
t_f	Output voltage fall−time @ C_L = 1 nF, 10−90% of output signal	5	−	30	−	ns
R_{OH}	Source resistance, V_{CC} = 12 V, I_{DRV} = 100 mA	5	−	28	−	Ω
R_{OL}	Sink resistance, V_{CC} = 12 V, I_{DRV} = 100 mA	5	−	7	−	Ω
I_{source}	Peak source current, V_{GS} = 0 V (Note 4)	5	−	300	−	mA
I_{sink}	Peak sink current, V_{GS} = 12 V (Note 4)	5	−	500	−	mA
$V_{DRV(low)}$	DRV pin level at V_{CC} = $V_{CC(min)}$ + 100 mV with a 33 kΩ resistor to GND	5	8	−	−	V
$V_{DRV(high)}$	DRV pin level at V_{CC} = V_{OVP} – 100 mV (DRV unloaded)	5	10	12	14	V
CURRENT COMPARATOR						
V_{limit}	Maximum internal current set point (pin 1 grounded) T_J = 25°C T_J = −40°C to 125°C	3	 0.744 0.720	 0.810 0.810	 0.856 0.880	V
$V_{CS(freeze)}$	Internal peak current setpoint freeze (≈31% of V_{limit})	3	−	260	−	mV
t_{DEL}	Propagation delay from CS pin to DRV output	3	−	35	80	ns
t_{LEB}	Leading Edge Blanking Duration	3	−	270	−	ns
t_{SS}	Internal soft−start duration activated upon startup or auto−recovery	3	−	4.1	−	ms
I_{OPPs}	Set point decrease for pin 1 grounded	1	−	0	−	%
I_{OPPo}	Set point decrease for pin 1 biased to −250 mV (Note 4)	1	−	31.3	−	%
I_{OOPv}	Voltage set point for pin 1 biased to −250 mV T_J = 25°C T_J = −40°C to 125°C	1	 0.51 0.50	 0.55 0.55	 0.60 0.62	V
INTERNAL OSCILLATOR						
$f_{OSC(nom)}$	Oscillation frequency T_J = 25°C T_J = −40°C to 125°C	−	 63.0 61.0	 65.5 65.5	 67.0 69.0	kHz
D_{max}	Maximum duty−ratio	−	76	80	84	%

Table 3. ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 12 V unless otherwise noted.

Symbol	Rating	Pin	Min	Typ	Max	Units
FEEDBACK SECTION						
R_{eq}	Internal equivalent feedback resistance	2	−	29	−	kΩ
K_{ratio}	FB pin to current set point division ratio	−	−	4	−	−
$V_{FB(freeze)}$	Feedback voltage below which the peak current is frozen	2	−	1	−	V
$V_{FB(limit)}$	Feedback voltage corresponding with maximum internal current set point	2	−	3.2	−	V
$V_{FB(open)}$	Internal pull−up voltage on FB pin	2	−	4	−	V
SKIP SECTION						
V_{skip}	Skip−cycle level voltage on the feedback pin	−	−	0.8	−	V
$V_{skip(hyst)}$	Hysteresis on the skip comparator (Note 4)	−	−	50	−	mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C (Note 6)	3	−	2.5	−	V
R_{ramp}	Internal ramp resistance to CS pin	3	−	20	−	kΩ
PROTECTIONS						
$V_{(latch)}$	Fault level input on OPP pin	1	2.85	3.0	3.15	V
$t_{latch\ (blank)}$	Blanking time after Drive output turn off	1	−	1	−	μs
$t_{latch\ (count)}$	Number of clock cycles before fault is confirmed	1	−	4	−	
$t_{latch\ (del)}$	OVP/OTP delay time constant before fault is confirmed	1	−	600	−	ns
t_{fault}	Internal auto−recovery fault timer duration	−	100	115	130	ms
V_{OVP}	Over voltage protection on the VCC pin	6	24.0	25.5	27.0	V
$t_{OVP(del)}$	Delay time constant before OVP on VCC is confirmed	6	−	20	−	μs

4. Guaranteed by design.
5. Application parameter for information only.
6. 1 MΩ resistor is connected from pin 3 to the ground for the measurement.

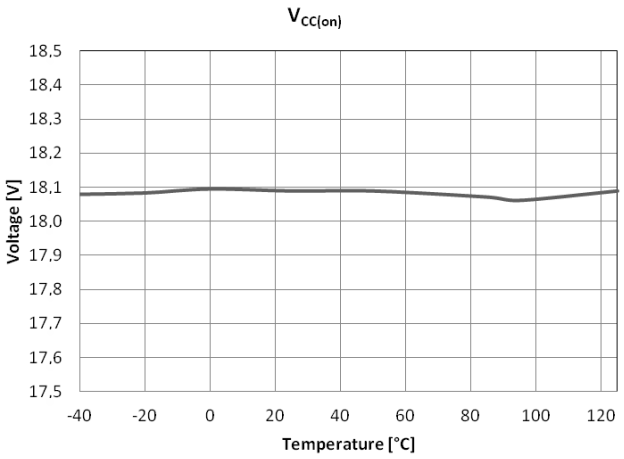


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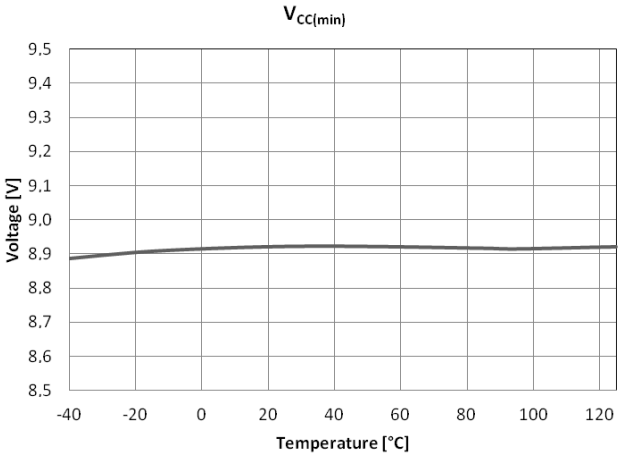


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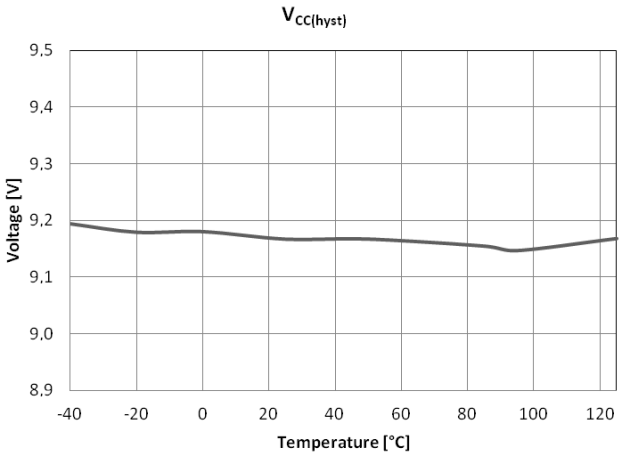


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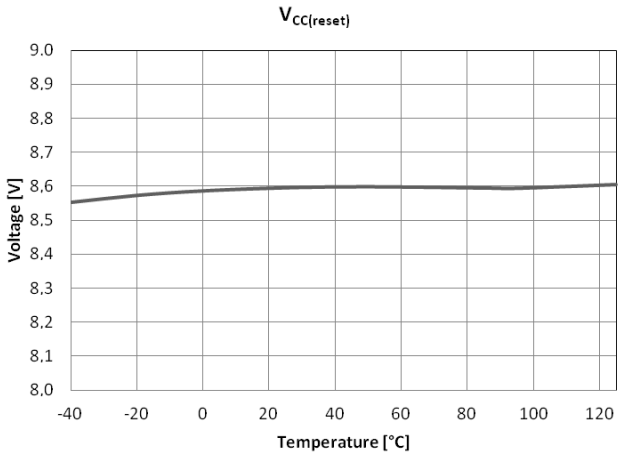


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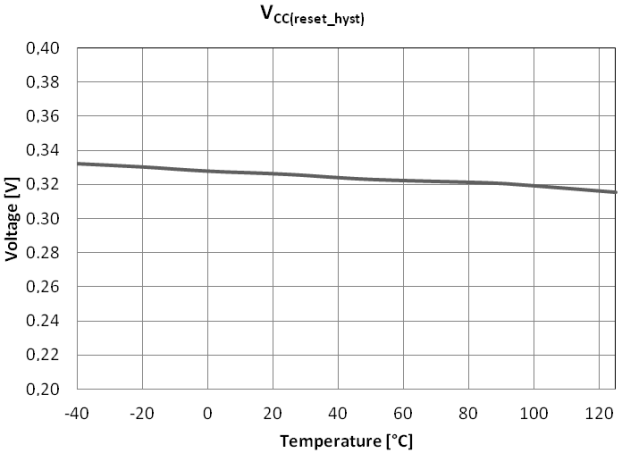


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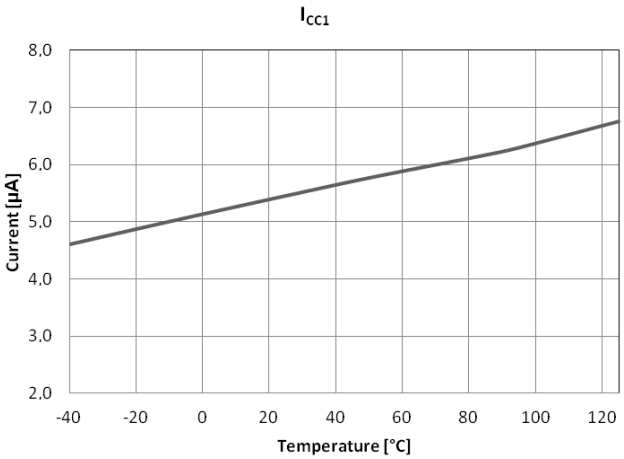


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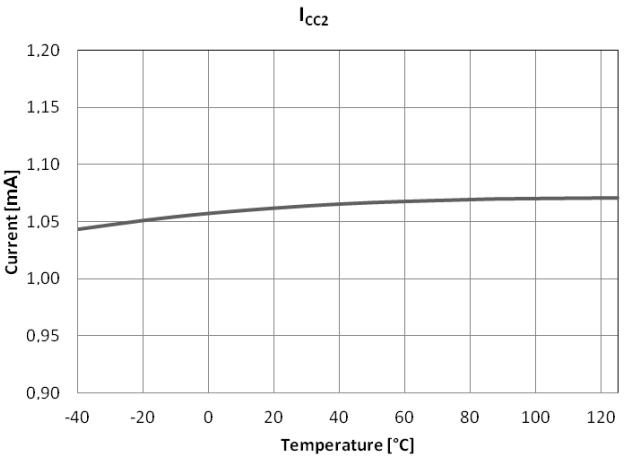


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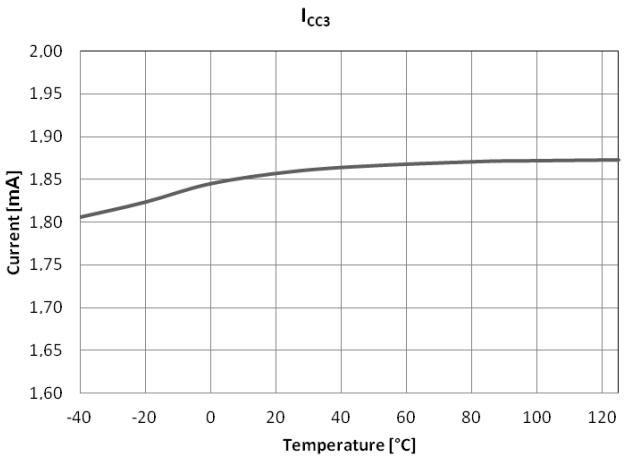


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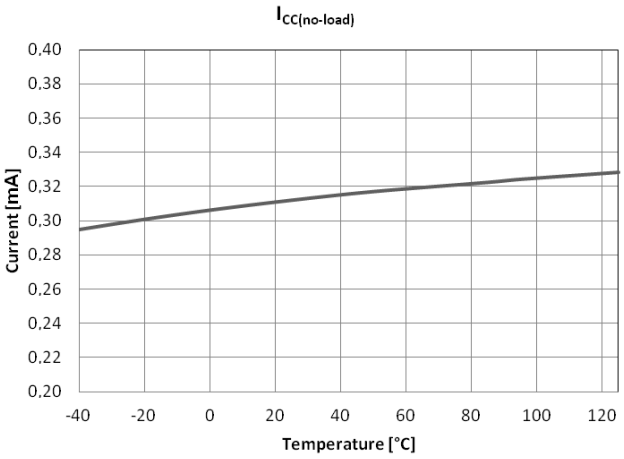


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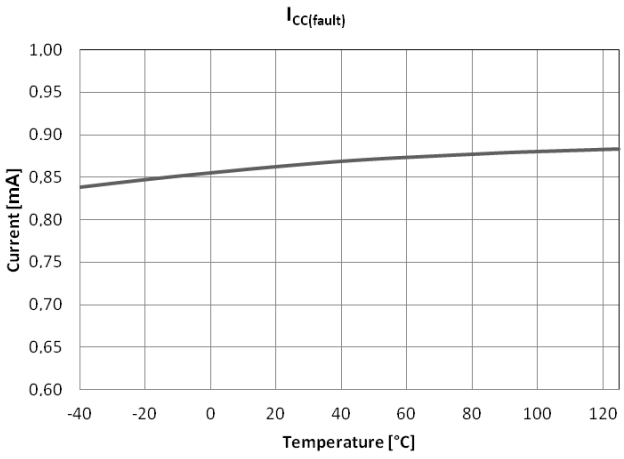


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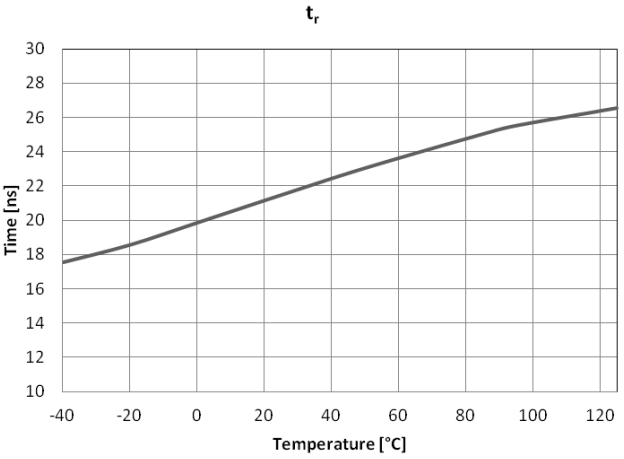


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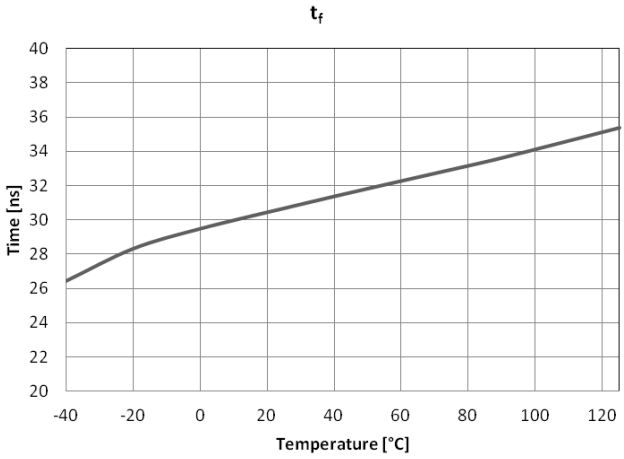


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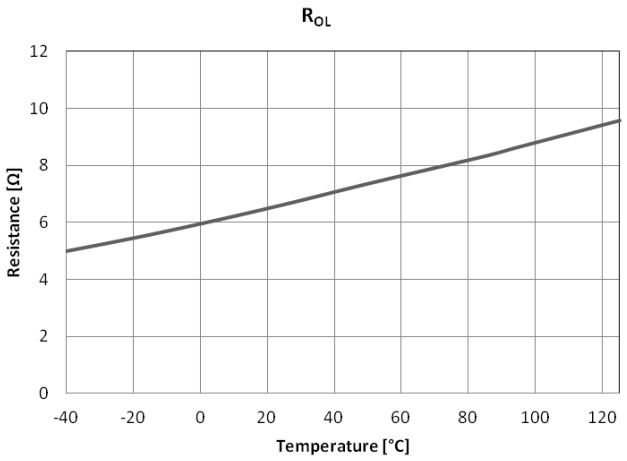


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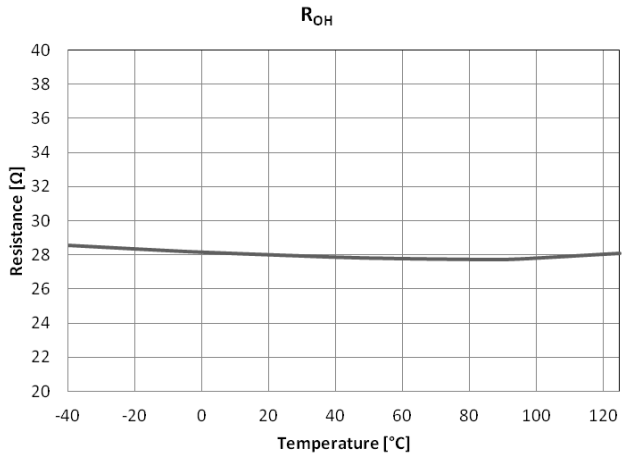


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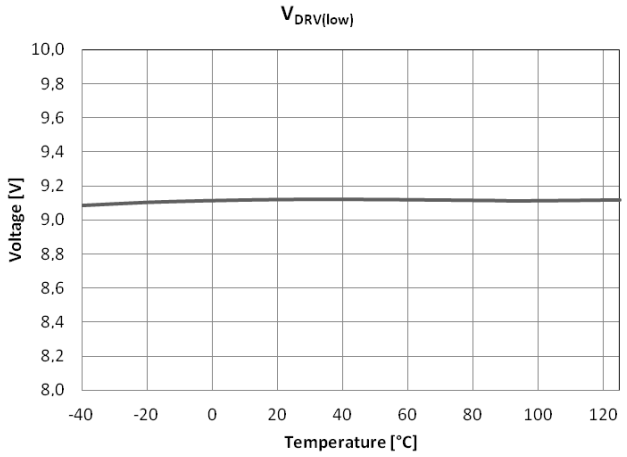


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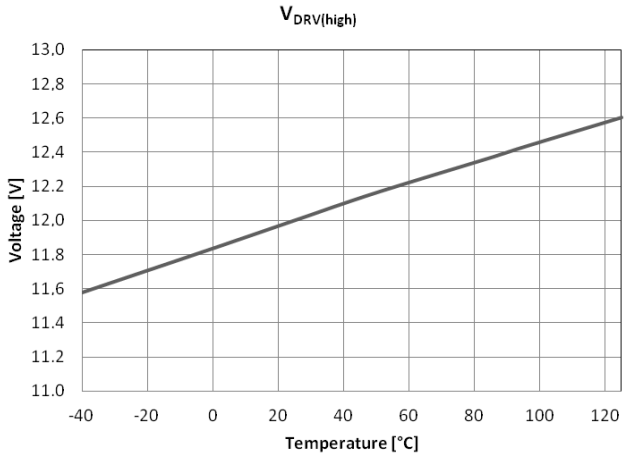


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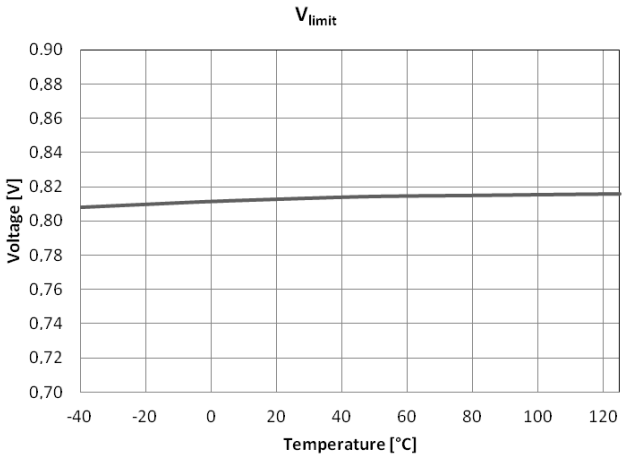


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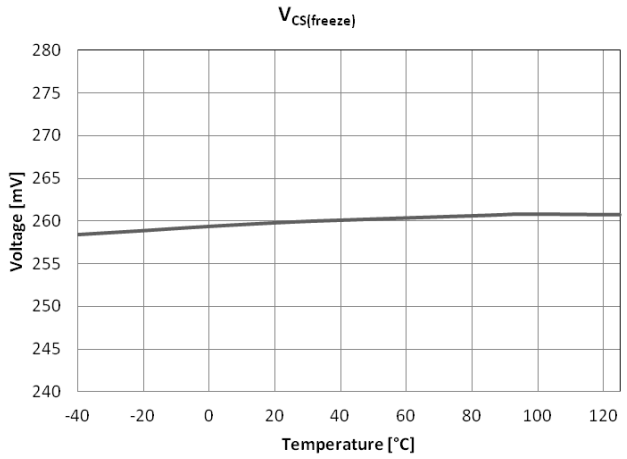


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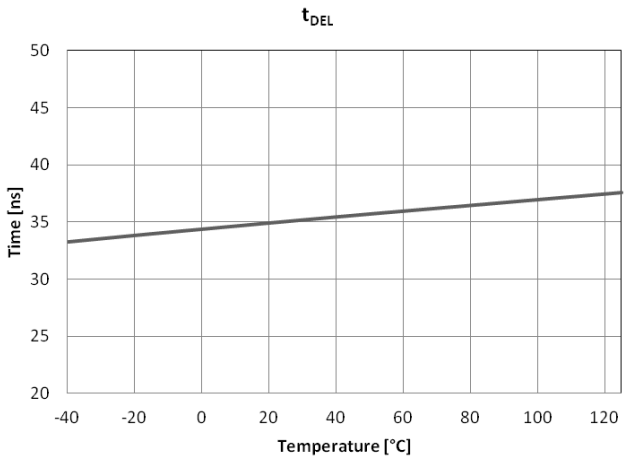


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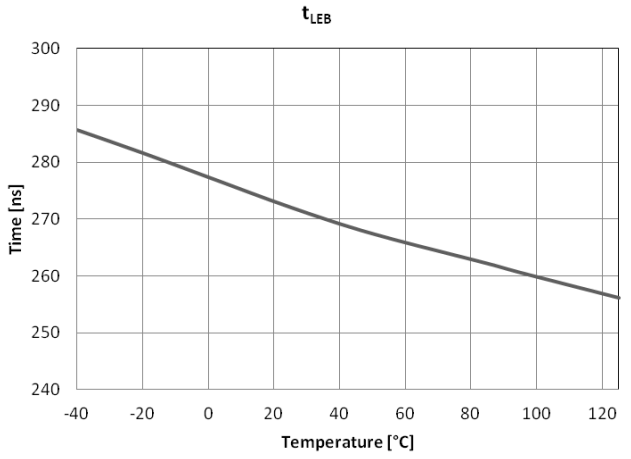


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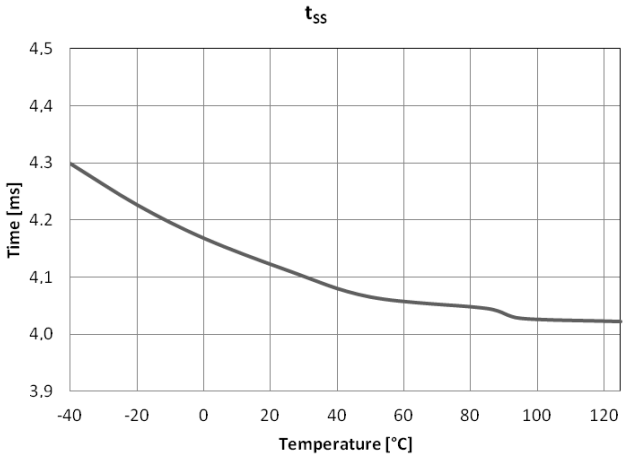


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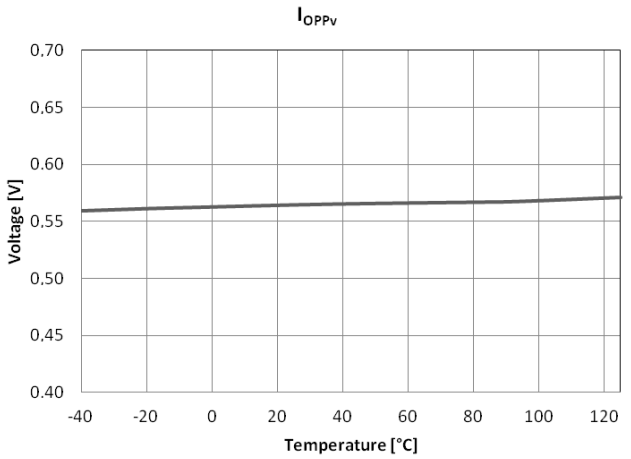


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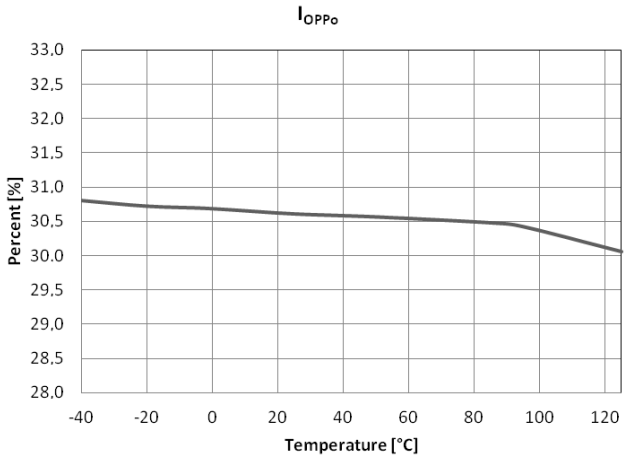


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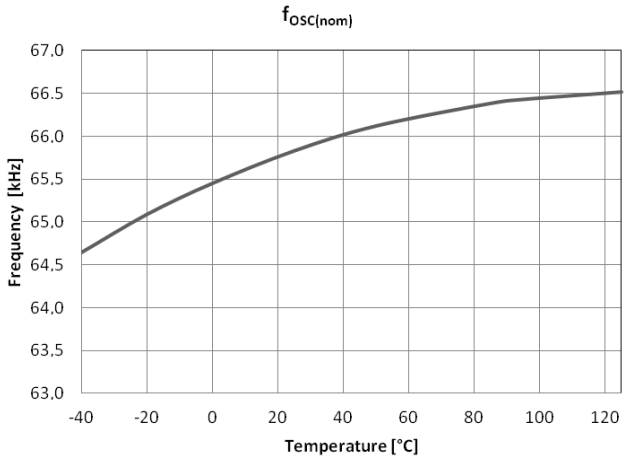


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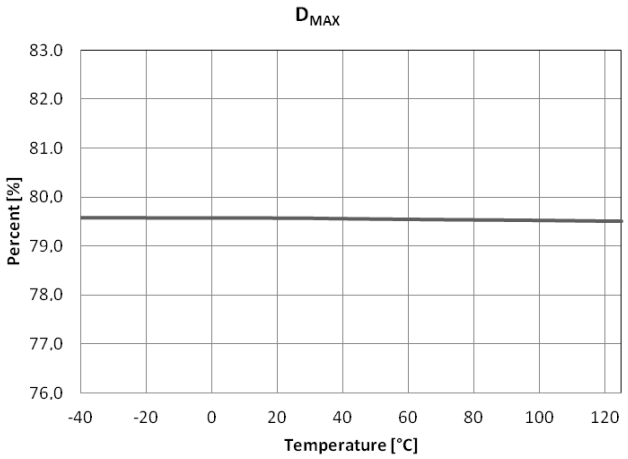


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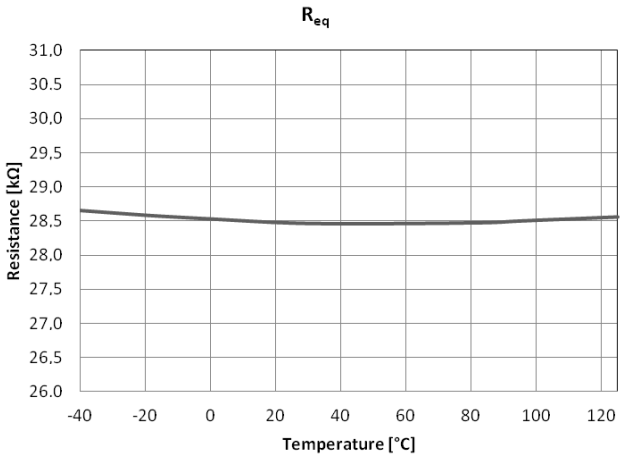


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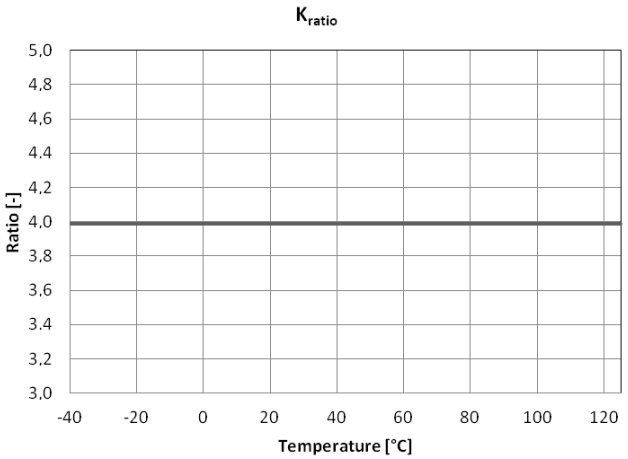


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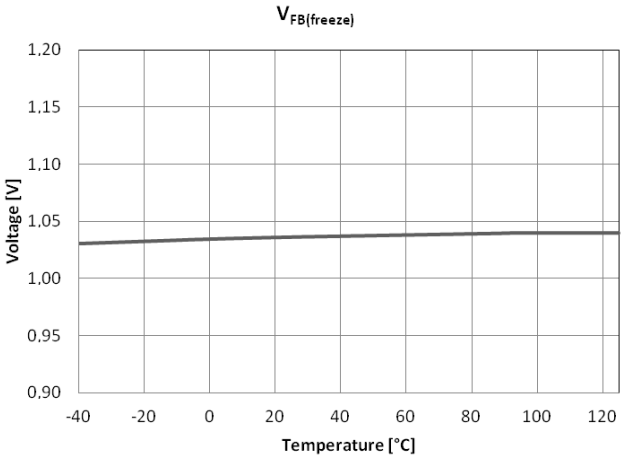


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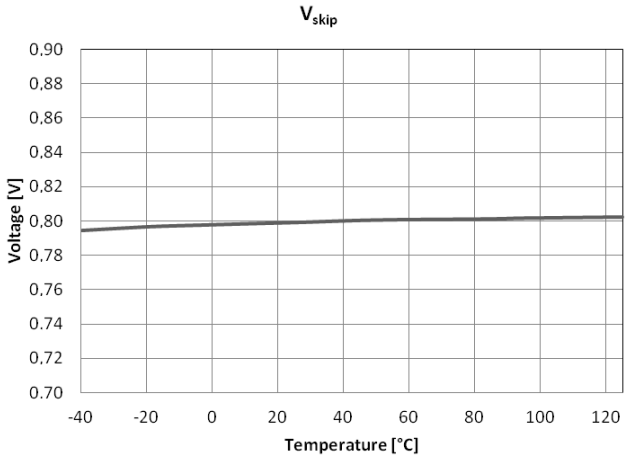


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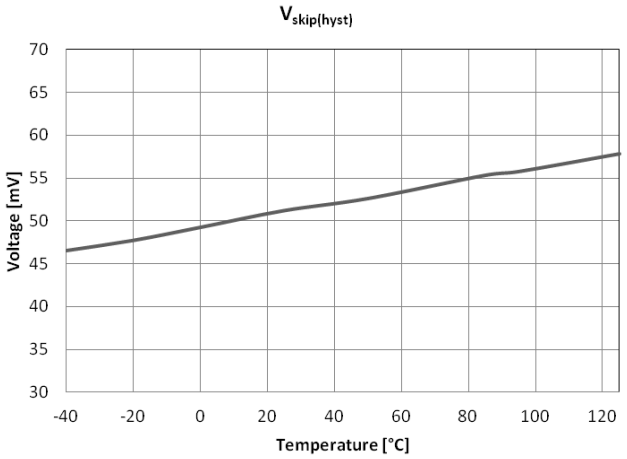


Figure 34.

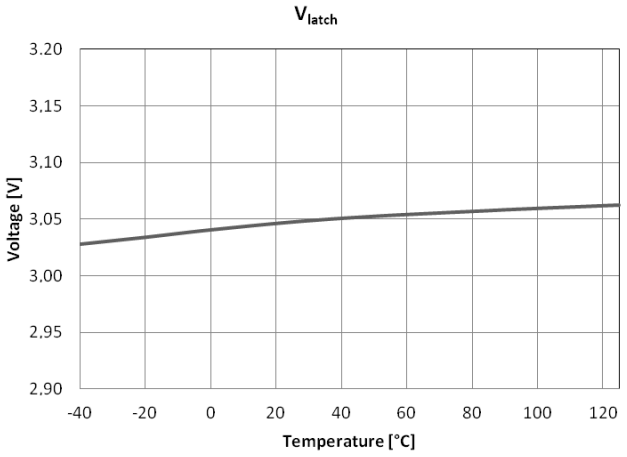


Figure 35.

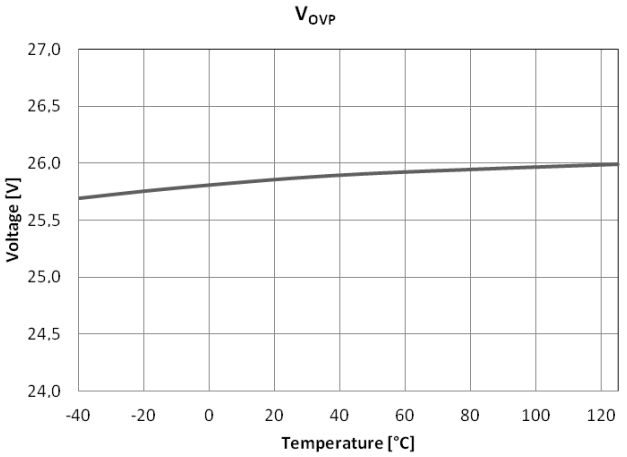


Figure 36.

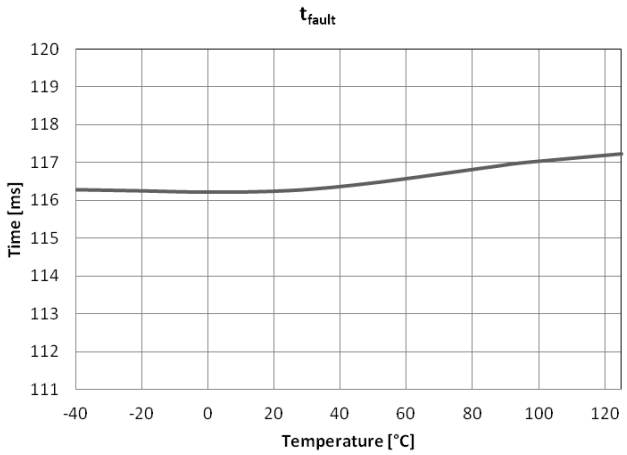


Figure 37.

APPLICATION INFORMATION

Introduction

NCL30073 implements a standard current mode architecture where the switch−off event is dictated by the peak current set point. This component represents the ideal candidate for LED applications. The NCL30073 packs all the necessary components normally needed in today modern LED converter designs, bringing several enhancements such as a non−dissipative OPP, OVP/OTP implementation, short−circuit protection, improved consumption, robustness and ESD capabilities.

- Current−mode Operation with Internal Slope Compensation:
  Implementing peak current mode control at a 65 kHz switching frequency, the NCL30073 offers an internal slope compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be fought via the inclusion of a simple resistor in series with the current−sense information.
- Internal OPP:
  By routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 1), the user has a simple and non−dissipative means to alter the maximum peak current set point as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage, then a peak current is reduced down.
- Low Startup and Standby Current:
  Reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during startup.
- Skip Capability:
  A continuous flow of pulses is not desired in all application. The controller monitors FB pin voltage and when it reaches a level of V_{skip}, the controller enters skip−cycle mode, to reduce number of switching periods
- Internal Soft−start:
  A soft−start precludes the main power switch from being stressed upon start−up. The soft−start duration is internally fixed for time t_{SS} and it is activated during new startup sequence or during recovering after auto−recovery hiccup mode.
- Auto−recovery Input:
  The controller includes an OPP input (pin 1) that can be used to sense an over voltage or an over temperature event on the converter. If this pin is brought higher than the internal reference voltage V_{latch} for four consecutive cycles, then the circuit enters into auto−recovery mode.
- Auto−recovery OVP on V_{CC}:
  An OVP protects the circuit against V_{CC} runaways. If the fault is present at least for time $t_{OVP(del)}$ then the OVP is validated and the controller enters hiccup mode. When the V_{CC} returns to a nominal level, the controller resumes operation.
- Short−circuit Protection:
  Short−circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). In this controller, every time the internal maximum peak current limit V_{limit} is activated (or less when OPP is used), an error flag is asserted and a time period starts thanks to an internal timer. When the timer has elapsed while a fault is still present, the controller enters an auto−recovery mode.

Start−up Sequence

The NCL30073 start−up voltage is made purposely high to permit large energy storage in a small V_{CC} capacitor value. This helps operate with a small start−up current which, together with a small V_{CC} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low, below 10 μA. The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage to further reduce the power dissipation.

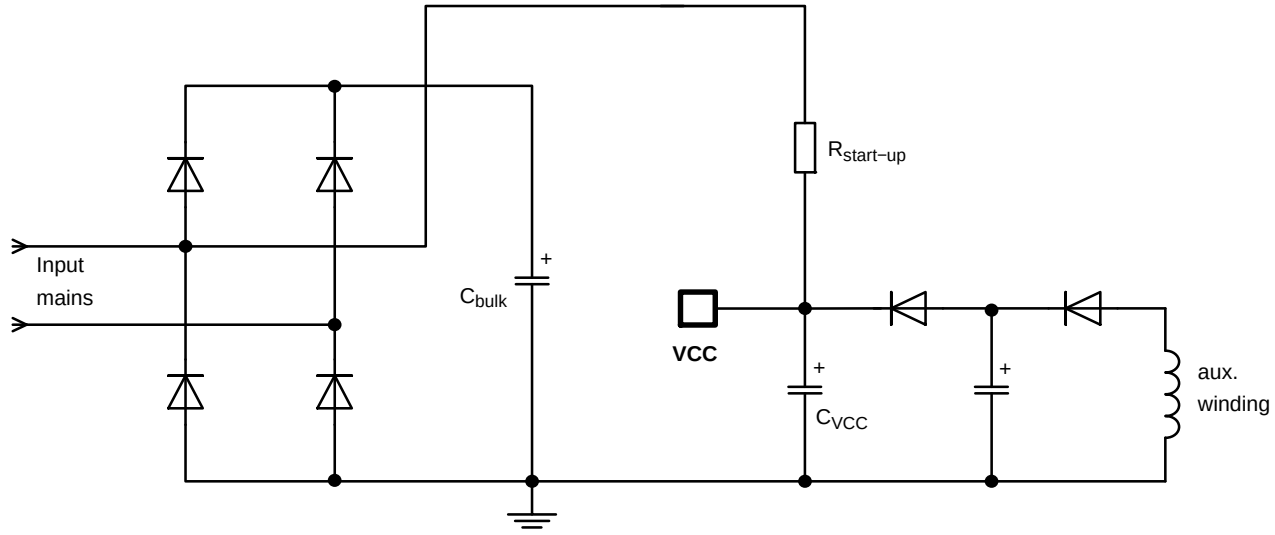


Figure 38. The Startup Resistor can be Connected to the Input Mains for further Power Dissipation Reduction

The first step starts with the calculation of the needed VCC capacitor which will supply the controller which it operates until the auxiliary winding takes it over. Experience shows that this time t_1 can be between 5 and 20 ms. If we consider we need at least an energy reservoir for a t_1 time of 10 ms, the VCC capacitor must be larger than:

$$C_{VCC} \geq \frac{I_{CC} \cdot t_1}{V_{CC(on)} - V_{CC(min)}} \geq \frac{1.6m \cdot 10m}{18 - 8.9} \geq 1.7\ \mu F \quad \text{(eq. 1)}$$

Let us select a 2.2 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for the time t_1. The VCC capacitor being known, we can now evaluate the charging current we need to bring the V_{CC} voltage from 0 V to the $V_{CC(on)}$ of the IC. This current has to be selected to ensure a start−up at the lowest mains (85 V_{rms}) to be less than 200 ms (acceptable time):

$$I_{charge} \geq \frac{V_{CC(on)} \cdot C_{VCC}}{t_{start-up}} \geq \frac{18 \cdot 2.2\ \mu}{0.1} \geq 198\ \mu A \quad \text{(eq. 2)}$$

If we account for the 10 μA (maximum) that will flow to the controller, then the total charging current delivered by the start−up resistor must be 208 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the $V_{CC(on)}$ of the controller:

$$I_{CVCC,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 346 μA, then, the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - V_{CC(on)}}{I_{CVCC(min)}} \leq \frac{\frac{85\sqrt{2}}{\pi} - 18}{208\ \mu} \leq 97\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the VCC capacitor. Thus, a decrease in charging current and an increase of the start−up resistor can be experimentally tested, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 92 kΩ resistor as suggested by Eq.4 , the dissipated power at high line amounts to:

$$P_{R_{start-up,max}} \approx \frac{V_{ac,peak}^{\ 2}}{4 \cdot R_{start-up}} \approx \frac{(230 \cdot \sqrt{2})^2}{4 \cdot 92k} \approx 287\ mW \quad \text{(eq. 5)}$$

Now that the first VCC capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the VCC capacitor. If this ripple is too large, chances exist to touch the $V_{CC(min)}$ and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 38 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the VCC pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without affecting the start−up time and standby power.

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage

swing present on the auxiliary diode anode. During the turn−on time, this point dips to $-N_2 V_{bulk}$, where N_2 being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 39 will have amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the internal voltage reference V_{limit} = 0.8 V. For instance, if the voltage swings down to −150 mV during the on−time, then the internal peak current set point will be fixed to the value 0.8 V – 0.150 V = 650 mV. The adopted principle appears in Figure 40 and shows how the final peak current set point is constructed.

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 0.8 \cdot V_{limit} - V_{limit} = 0.64 - 0.8 = -160\ mV \quad \text{(eq. 6)}$$

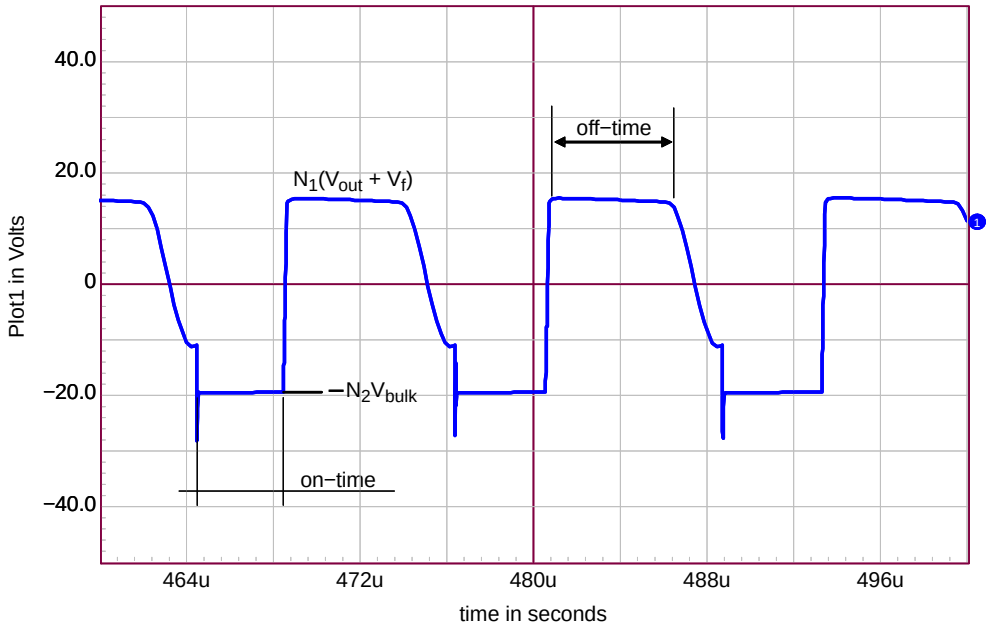


Figure 39. The Signal Obtained on the Auxiliary Winding Swings Negative During the On−time

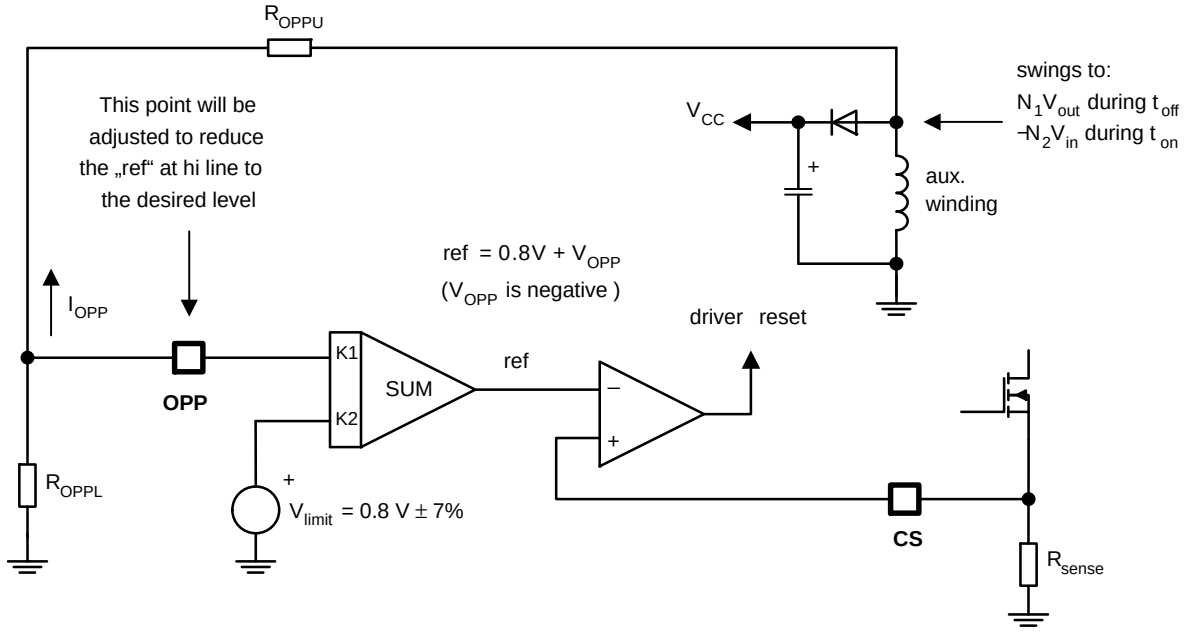


Figure 40. The OPP Circuitry Affects the Maximum Peak Current Set Point by Summing a Negative Voltage to the Internal Voltage Reference

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internal clamped slightly below –300 mV which means that if more current is injected before reaching the ESD forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal zener diode, then care must be taken to avoid injecting a current beyond –2 mA.

Finally, please note that another comparator internally fixes the maximum peak current set point to value V_{limit} even if the OPP pin is adversely biased above 0 V.

Short−Circuit Protection

In case of output short−circuit or if the LED converter experiences a severe overloading situation, an internal error flag is raised and the fault timer starts countdown. If the UVLO has come (see Figure 41 – Short−circuit case I.) or the error flag is asserted throughout the t_{fault} time (see Figure 41 – Short−circuit case II.) – i.e. the fault timer has elapsed, the driving pulses are stopped and the V_{CC} falls down as the auxiliary voltage are missing. When the supply voltage V_{CC} touches the $V_{CC(min)}$ level, the controller consumption is down to a few μA and the V_{CC} slowly builds up again thanks to the resistive startup network. When V_{CC} reaches $V_{CC(on)}$, the controller enter into start−up cycle. Please note that soft−start is activated upon every re−start attempt.

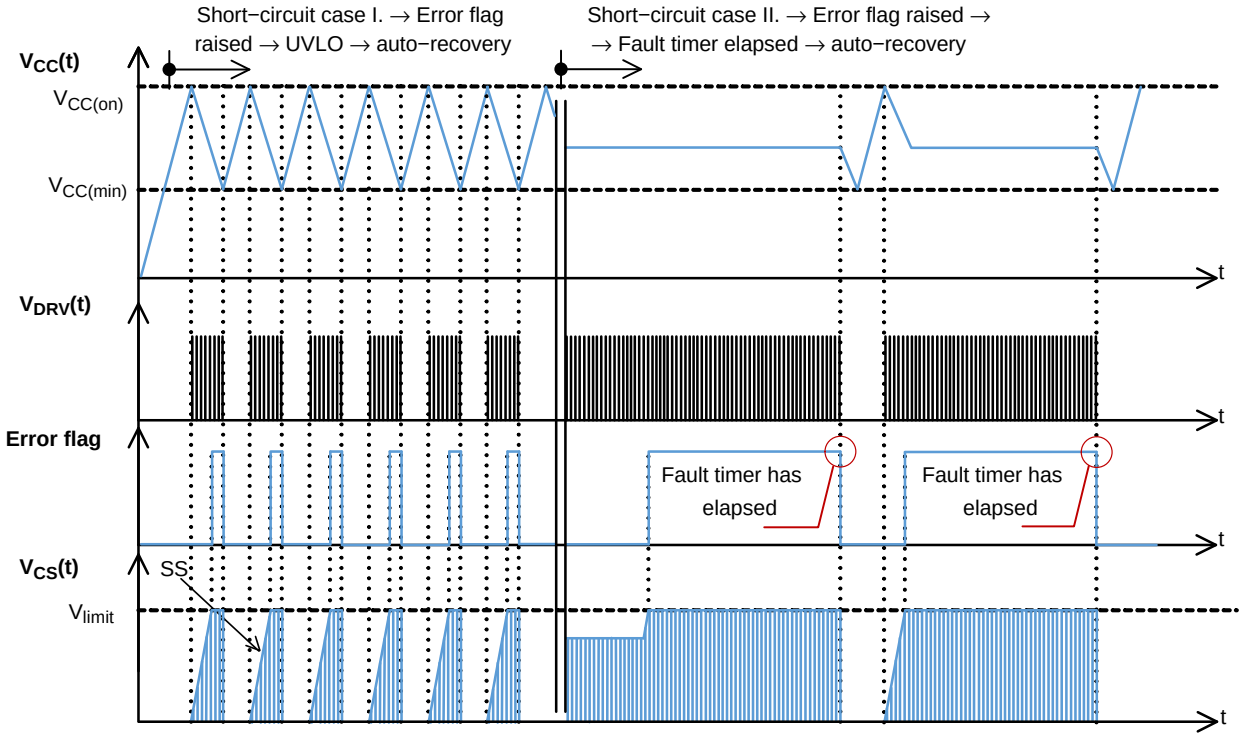


Figure 41. An Auto−recovery Description

Slope Compensation

The NCL30073 includes an internal slope compensation signal. This is the buffered oscillator clock delivered during the on−time only. Its amplitude is around 2.5 V at the maximum duty ratio. Slope compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty ratio greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the primary inductance downslope. Figure 42 depicts how the ramp is generated internally. Please note that the ramp signal will be disconnected from the CS pin during the off−time.

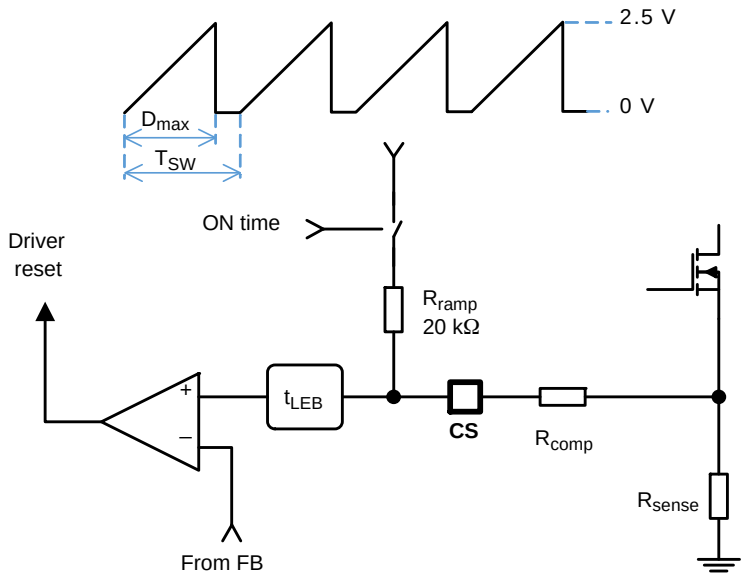


Figure 42. Inserting a Resistor in Series with the Current Sense Information Brings Slope Compensation and Stabilizes the Converter in CCM Operation

In the NCL30073 controller, the oscillator ramp features a 2.5 V swing. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max} \cdot T_{SW}} = \frac{2.5}{0.8 \cdot 15\mu} = 208\ mV/\mu s \quad \text{(eq. 7)}$$

In a flyback design, let's assume that our primary inductance L_p is 770 µH, and the SMPS delivers 19 V with a N_p:N_s ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_p = \frac{(V_{out} + V_f) \cdot \frac{N_s}{N_p}}{L_p} = \frac{(19 + 0.7) \cdot 4}{770\mu} = 102\ mA/\mu s \quad \text{(eq. 8)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p \cdot R_{sense} = 102m \cdot 0.33 = 34\ mV/\mu s \quad \text{(eq. 9)}$$

If we select 50% of the downslope as the required amount of slope compensation, then we shall inject a ramp whose slope is 17 mV/µs. Our internal compensation being of 208 mV/µs, the divider ratio (*divratio*) between R_{comp} and the internal R_{ramp} = 20 kΩ resistor is:

$$divratio = \frac{0.5 \cdot S_{sense}}{S_{ramp}} = 0.082 \quad \text{(eq. 10)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp} \cdot divratio = 20k \cdot 0.082 = 1.64\ k\Omega \quad \text{(eq. 11)}$$

A resistor of the calculated value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. Please make sure both components are located very close to the controller.

Protection Pin

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to enter the auto−recovery mode.

The auto−recovery detection is made by observing the OPP pin by a comparator featuring a V_{latch} reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a blanking delay $t_{latch-blank}$ is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high−state duration lasts for a minimum time $t_{latch-del}$. Below this value, the event is ignored. Then, a counter ensures that only 4 successive OVP events have occurred before actually auto−recovery mode is triggered. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on−time.

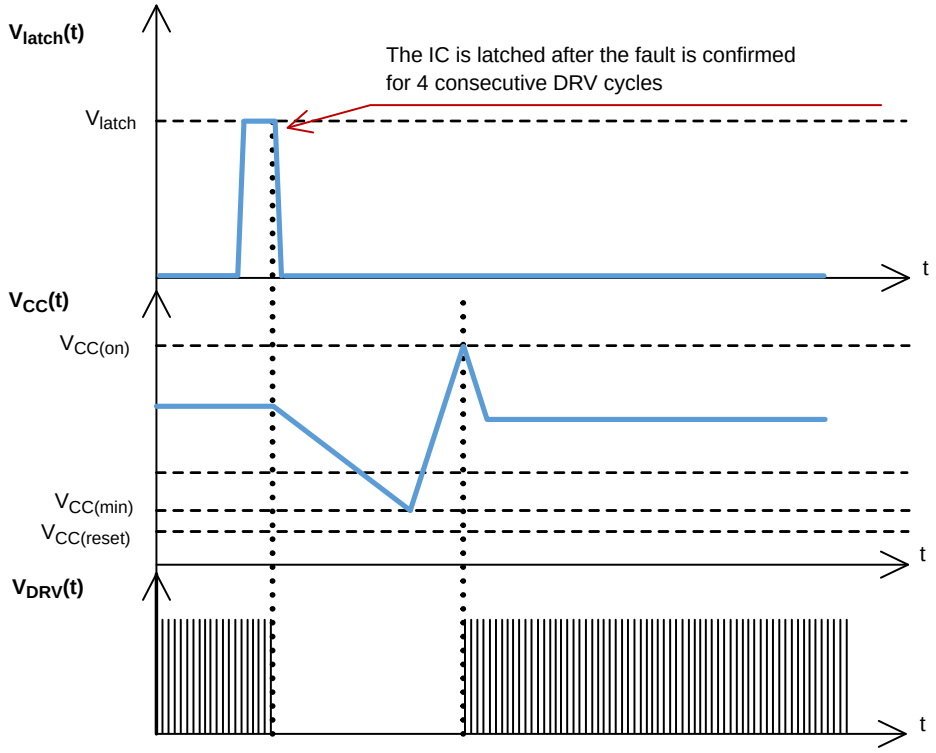


Figure 43. Auto−recovery of the Controller and Resuming Operation

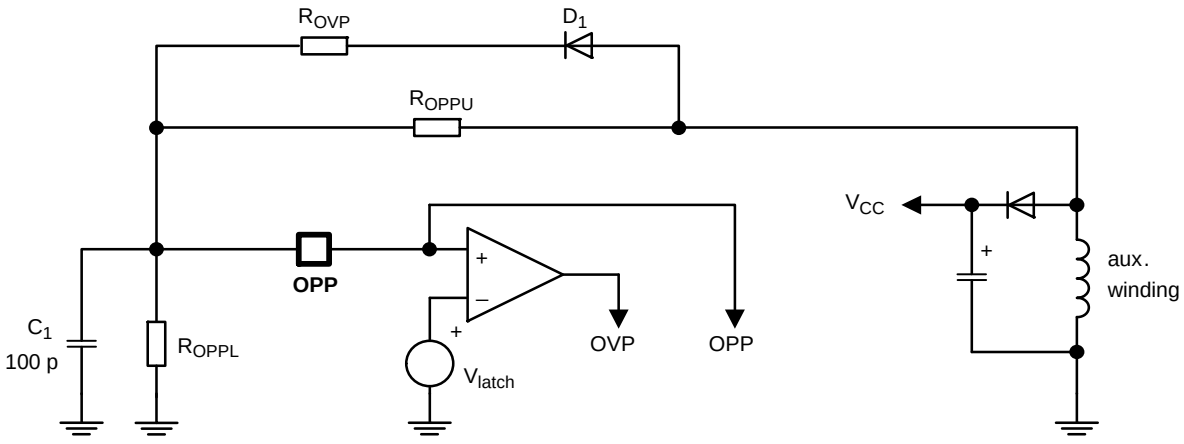


Figure 44. A Simple Resistive Divider Brings the OPP Pin above 3 V in case of a V_{CC} Voltage Runaway above 18 V

First, calculate the OPP network with the above equations. Then, suppose we want to trigger auto−recovery of our controller when V_{out} exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary winding. In case of voltage runaway for 19 V output, the plateau will go up to:

$$V_{aux,OVP} = V_{out} \cdot \frac{N_s}{N_{aux}} = 25 \cdot \frac{0.18}{0.25} = 18\ V \quad \text{(eq. 12)}$$

Since our OVP comparator trips at level V_{latch} = 3 V, across the 1 kΩ selected OPP pull−down resistor, it implies a 3 mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = V_{out} \cdot \frac{V_{aux,OVP} - V_{latch}}{\frac{V_{OVP}}{R_{OPPL}}} = \frac{18 - 3}{\frac{3}{1k}} = 5\ k\Omega \quad \text{(eq. 13)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide by 6 ratio, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV for the noise immunity. A 100 pF capacitor can be added to improve it and avoid erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

A second solution for the OVP detection alone is to use a Zener diode wired as recommended by Figure 45.

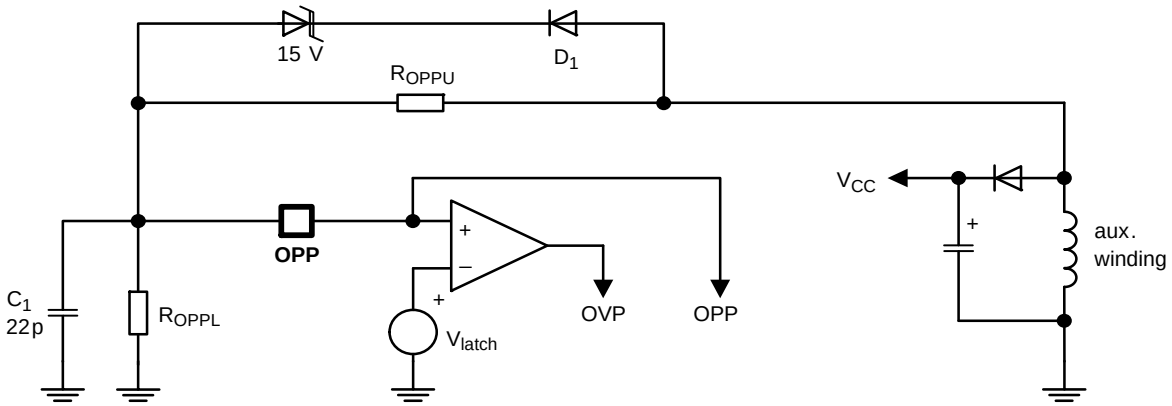


Figure 45. A Zener Diode in Series with a Diode Helps to Improve the Noise Immunity of the System

In this case, to still trip at 18 V level, we have selected a 15 V Zener diode. In nominal conditions, the voltage on the OPP pin is almost 0 V during the off−time as the Zener is fully blocked. This technique clearly improves the noise immunity of the system compared to that obtained from a resistive string as in Figure 44. Please note the reduction of the capacitor on the OPP pin to 10−22 pF. This is because of the potential spike going through the Zener parasitic capacitor and the possible auxiliary level shortly exceeding its breakdown voltage during the leakage inductance reset period (hence the internal blanking delay $t_{latch-blank}$ at turn off). This spike despite its very short time is energetic enough to charge the added capacitor C_1 and given the time constant, could make it discharge slower, potentially disturbing the blanking circuit. When implementing the Zener option, it is important to carefully observe the OPP pin voltage (short probe connections!) and check that enough margin exists to that respect.

Over Temperature Protection

In a lot of designs, the converter must be protected against thermal runaways, e.g. when the temperature inside the converter box increases a certain value. Figure 46 shows how to implement a simple OTP using an external NTC and a series diode. The principle remains the same: make sure the OPP network is not bothered by the additional NTC hence the presence of this diode.

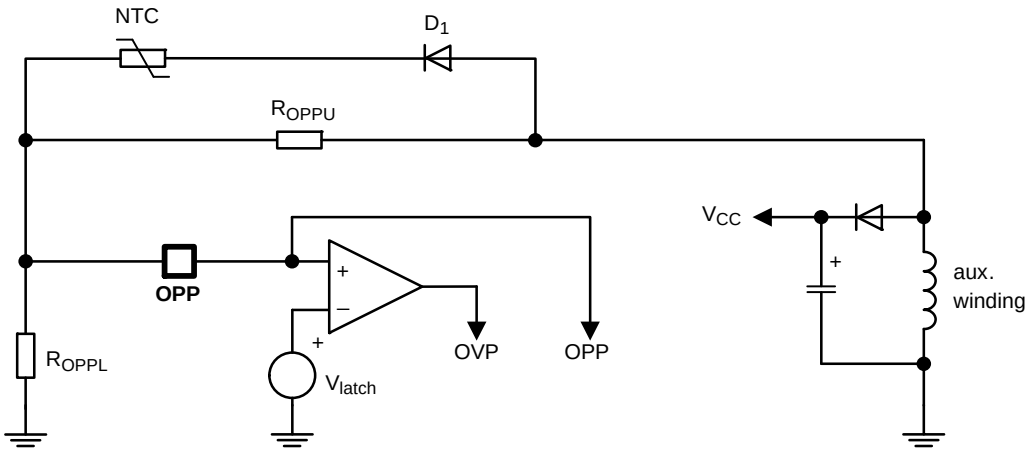


Figure 46. The Internal Circuitry Hooked to OPP Pin can be used to Implement Over Temperature Protection (OTP)

When the NTC resistor will diminish as the temperature increases, the voltage on the OPP pin during the off−time will slowly increase and, once it passes V_{latch} level for 4 consecutive clock cycles, the controller will enter auto−recovery mode.

We have found that the plateau voltage on the auxiliary diode was 14 V in nominal conditions. We have selected an NTC which offers a 470 kΩ resistance at 25°C and drops to 8.8 kΩ at 110°C. If our auxiliary winding plateau is 14 V and we consider a 0.7 V forward drop for the diode, then the voltage across the NTC in fault mode must be:

$$V_{NTC} = V_{aux} - V_{latch} - V_F = 14 - 3 - 0.7 = 10.3\ V \quad \text{(eq. 14)}$$

Based on the 8.8 kΩ NTC resistor at 110°C, the current inside the device must be:

$$I_{NTC} = \frac{V_{NTC}}{R_{NTC(110)}} = \frac{10.3}{8.8k} = 1.2\ mA \quad \text{(eq. 15)}$$

As such, the bottom resistor R_{OPPL}, can easily be calculated:

$$R_{OPPL} = \frac{V_{latch}}{I_{NTC}} = 2.5\ k\Omega \quad \text{(eq. 16)}$$

Now the pull down OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose we need a 200 mV decrease from the V_{limit} setpoint and the on−time swing on the auxiliary anode is −67.5 V, then we need to drop over R_{OPPU} a voltage of:

$$V_{R_{OPPU}} = V_{aux} - V_{OPP} = -67.5 + 0.2 = -67.3\ V \quad \text{(eq. 17)}$$

The current circulating the pull down resistor R_{OPPL} in this condition will be:

$$I_{R_{OPPL}} = \frac{V_{OPP}}{R_{OPPL}} = \frac{-0.2}{2.5k} = -80\ \mu A \quad \text{(eq. 18)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{V_{R_{OPPU}}}{I_{R_{OPPU}}} = \frac{-67.3}{-80\mu} \approx 841\ k\Omega \quad \text{(eq. 19)}$$

Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 47. In nominal V_{CC}/output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the protection in case of a fault. On the contrary, in nominal temperature conditions, if the loop is broken, the voltage runaway will be detected and acknowledged by the controller.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

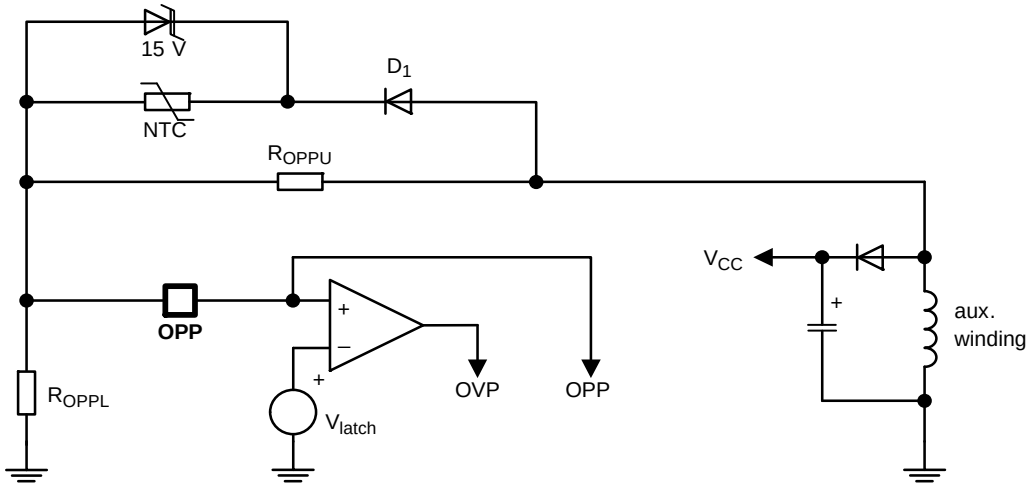


Figure 47. With the NTC Back in Place, the Circuit Nicely Combines OVP, OTP and OPP on the Same Pin

Filtering the Spikes

The auxiliary winding is the seat of spikes that can couple to the OPP pin via the parasitic capacitances exhibited by the Zener diode and the series diode. To prevent an adverse triggering of the Over Voltage Protection circuitry, we recommend the installation of a small *RC* filter before the detection network as illustrated by Figure 48. The values of resistance and capacitance must be selected to provide the adequate filtering function without degrading the stand−by power by an excessive current circulation.

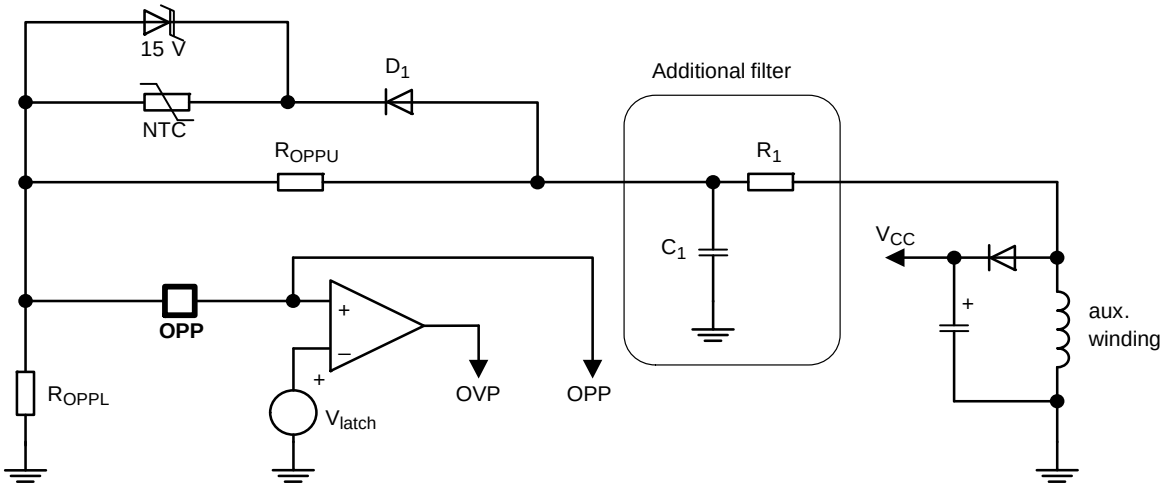


Figure 48. A Small *RC* Filter Prevents the Fast Rising Spikes from Reaching the Protection Pin OPP in Presence of Energetic Perturbations Superimposed on the Input Line

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

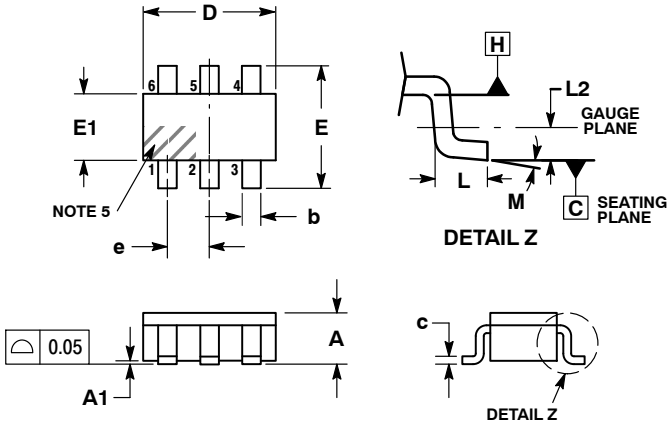
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SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

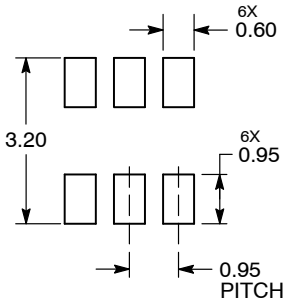
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

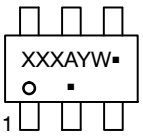
RECOMMENDED SOLDERING FOOTPRINT*



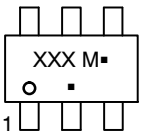
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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