NCL30081

Dimmable Quasi-Resonant Primary Side Current-Mode Controller for LED Lighting

The NCL30081 is a PWM current mode controller targeting isolated flyback and non−isolated constant current topologies. The controller operates in a quasi−resonant mode to provide high efficiency. Thanks to a novel control method, the device is able to precisely regulate a constant LED current from the primary side. This removes the need for secondary side feedback circuitry, biasing and an optocoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs. It supports step dimming by monitoring the AC line and detecting when the line has been toggled on−off−on by the user to reduce the light intensity in 5 steps down to 5% dimming.

Features

- Quasi−resonant Peak Current−mode Control Operation
- Primary Side Sensing (no optocoupler needed)
- Wide V_{CC} Range
- Precise LED Constant Current Regulation ±1% Typical
- Line Feed−forward for Enhanced Regulation Accuracy
- Low LED Current Ripple
- 250 mV ±2% Guaranteed Voltage Reference for Current Regulation
- ~ 0.9 Power Factor with Valley Fill Input Stage
- Low Start−up Current (10 μA typ.)
- Small Space Saving Low Profile Package
- 5 State Quasi−log Dimmable
- Wide Temperature Range of −40 to +125°C
- Pb−free, Halide−free MSL1 Product
- Robust Protection Features
  - Over Voltage / LED Open Circuit Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Shorted Current Sense Pin Fault Detection
  - Latched and Auto−recoverable Versions
  - Brown−out
  - V_{CC} Under Voltage Lockout
  - Thermal Shutdown

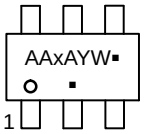
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TSOP−6
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CASE 318G

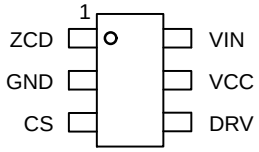
MARKING DIAGRAM



AAx = Specific Device Code
x = G or H
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

Typical Applications

- Integral LED Bulbs
- LED Power Driver Supplies
- LED Light Engines

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 30 of this data sheet.

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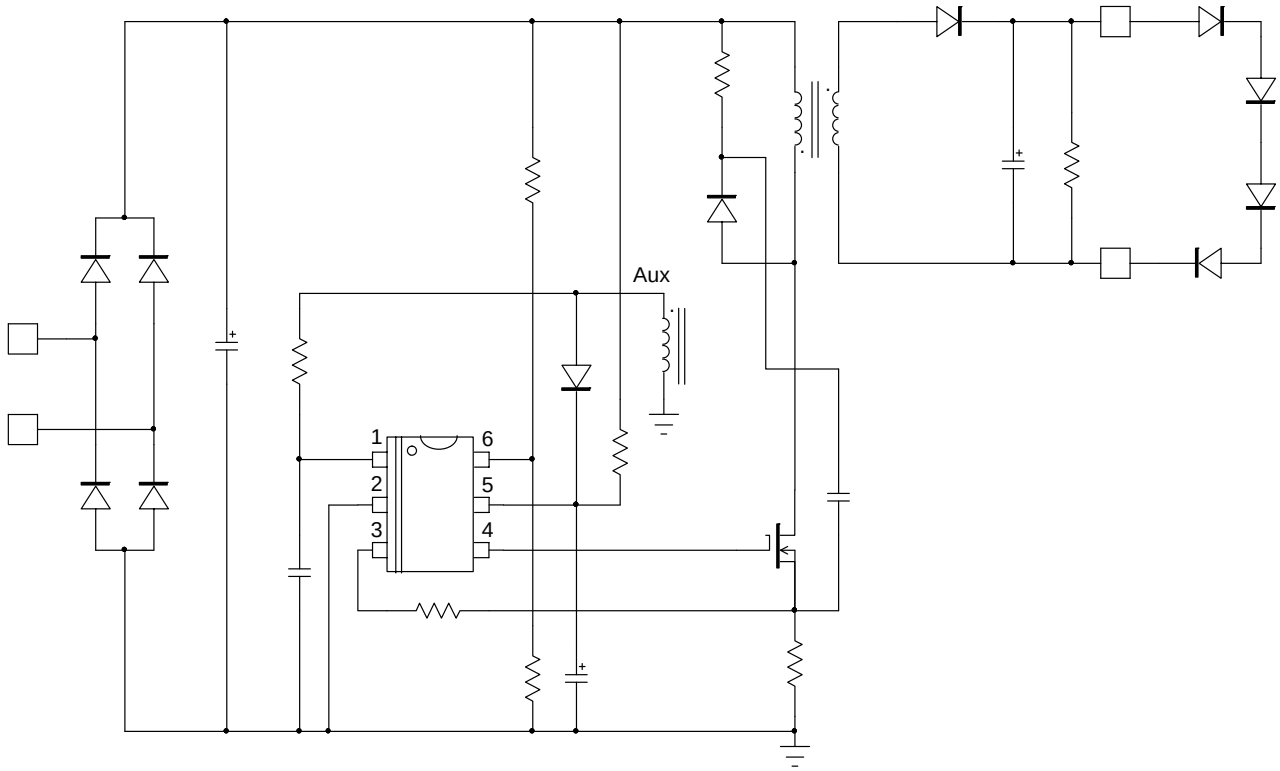


Figure 1. Typical Application Schematic for NCL30081

Table 1. PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	ZCD	Zero Crossing Detection	Connected to the auxiliary winding, this pin detects the core reset event.
2	GND	−	The controller ground
3	CS	Current sense	This pin monitors the primary peak current
4	DRV	Driver output	The current capability of the totem pole gate drive (+0.3/−0.5 A) makes it suitable to effectively drive a broad range of power MOSFETs.
5	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage.
6	VIN	Input voltage sensing Brown−Out	This pin observes the HV rail and is used in valley selection. This pin also monitors and protects for low mains conditions.

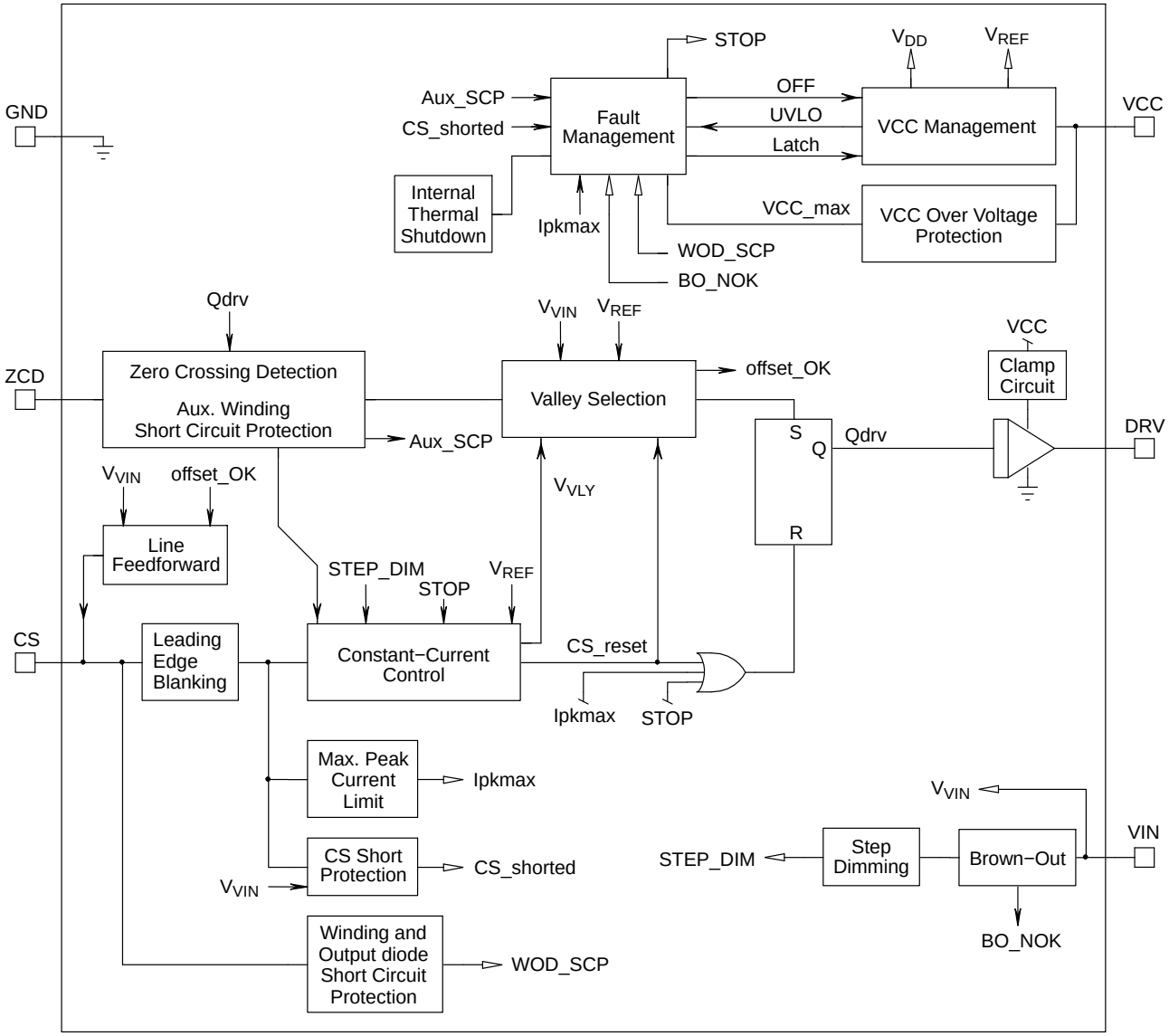


Figure 2. Internal Circuit Architecture

Table 2. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, VCC pin, continuous voltage Maximum current for VCC pin	−0.3, +35 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 1) −500, +800	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins DRV and VCC) Current range for low power pins (except pins ZCD, DRV and VCC)	−0.3, +5.5 −2, +5	V mA
$V_{ZCD(MAX)}$ $I_{ZCD(MAX)}$	Maximum voltage for ZCD pin Maximum current for ZCD pin	−0.3, +10 −2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance, Junction−to−Air	360	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−60 to +150	°C
	ESD Capability, HBM model (Note 2)	4	kV
	ESD Capability, MM model (Note 2)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} unless otherwise noted.
2. This device series contains ESD protection and exceeds the following tests: Human Body Model 4000 V per JEDEC JESD22−A114−F and Machine Model Method 200 V per JEDEC JESD22−A115−A.
3. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78 except for VIN pin which passes 60 mA.

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V; For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	16	18	20	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.2	8.8	9.4	
Hysteresis $V_{CC(on)} - V_{CC(off)}$	V_{CC} decreasing	$V_{CC(HYS)}$	8	–	–	
Internal logic reset		$V_{CC(reset)}$	3.5	4.5	5.5	
Over Voltage Protection VCC OVP threshold		$V_{CC(OVP)}$	26	28	30	V
$V_{CC(off)}$ noise filter		$t_{VCC(off)}$	–	5	–	μs
$V_{CC(reset)}$ noise filter−		$t_{VCC(reset)}$	–	20	–	
Startup current		$I_{CC(start)}$	–	13	30	μA
Startup current in fault mode		$I_{CC(sFault)}$	–	46	60	μA
Supply Current						mA
Device Disabled/Fault	$V_{CC} > V_{CC(off)}$	I_{CC1}	0.8	1.0	1.4	
Device Enabled/No output load on pin 5	F_{sw} = 65 kHz	I_{CC2}	–	2.15	4.0	
Device Switching (F_{sw} = 65 kHz)	C_{DRV} = 470 pF, F_{sw} = 65 kHz	I_{CC3}	–	2.6	5.0	
CURRENT SENSE						
Maximum Internal current limit		V_{ILIM}	0.95	1	1.05	V
Leading Edge Blanking Duration for V_{ILIM} (T_j = −25°C to 125°C)		t_{LEB}	250	300	350	ns
Leading Edge Blanking Duration for V_{ILIM} (T_j = −40°C to 125°C)		t_{LEB}	240	300	350	ns
Input Bias Current	DRV high	I_{bias}	–	0.02	–	μA
Propagation delay from current detection to gate off−state		t_{ILIM}	–	50	150	ns
Threshold for immediate fault protection activation		$V_{CS(stop)}$	1.35	1.5	1.65	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	120	–	ns
Blanking time for CS to GND short detection V_{pinVIN} = 1 V		$t_{CS(blank1)}$	8.0	–	14.0	μs
Blanking time for CS to GND short detection V_{pinVIN} = 3.3 V		$t_{CS(blank2)}$	2.6	–	4.6	μs
GATE DRIVE						
Drive Resistance						Ω
DRV Sink		R_{SNK}	–	13	–	
DRV Source		R_{SRC}	–	30	–	
Drive current capability						mA
DRV Sink (Note 4)		I_{SNK}	–	500	–	
DRV Source (Note 4)		I_{SRC}	–	300	–	
Rise Time (10% to 90%)	C_{DRV} = 470 pF	t_r	–	40	–	ns
Fall Time (90% to 10%)	C_{DRV} = 470 pF	t_f	–	30	–	ns
DRV Low Voltage	$V_{CC} = V_{CC(off)}$+0.2 V, C_{DRV} = 470 pF, R_{DRV} = 33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	V_{CC} = 30 V, C_{DRV} = 470 pF, R_{DRV} = 33 kΩ	$V_{DRV(high)}$	10	12	14	V

4. Guaranteed by design

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V; For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
ZERO VOLTAGE DETECTION CIRCUIT						
ZCD threshold voltage	V_{ZCD} increasing	$V_{ZCD(THI)}$	25	45	65	mV
ZCD threshold voltage (Note 4)	V_{ZCD} decreasing	$V_{ZCD(THD)}$	5	25	45	mV
ZCD hysteresis (Note 4)	V_{ZCD} increasing	$V_{ZCD(HYS)}$	10	–	–	mV
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.8	1	1.2	V
Short circuit detection Timer	$V_{ZCD} < V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery timer duration		$t_{recovery}$	3	4	5	s
Input clamp voltage High state Low state	 I_{pin1} = 3.0 mA I_{pin1} = −2.0 mA	 V_{CH} V_{CL}	 – −0.9	 9.5 −0.6	 – −0.3	V
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing	t_{DEM}	–	–	150	ns
Equivalent time constant for ZCD input (Note 4)		t_{PAR}	–	20	–	ns
Blanking delay after on−time		t_{BLANK}	2.25	3	3.75	μs
Timeout after last demag transition		t_{TIMO}	5	6.5	8	μs
CONSTANT CURRENT CONTROL						
Reference Voltage at T_j = 25°C		V_{REF}	245	250	255	mV
Reference Voltage T_j = −40°C to 125°C		V_{REF}	242.5	250	257.5	mV
70% reference voltage		V_{REF50}	–	175	–	mV
40% reference voltage		V_{REF50}	–	100	–	mV
25% reference voltage		V_{REF50}	–	62.5	–	mV
10% reference voltage		V_{REF50}	–	25	–	mV
5% reference voltage		V_{REF50}	–	12.5	–	mV
Current sense lower threshold for detection of the leakage inductance reset time		$V_{CS(low)}$	30	55	80	mV
LINE FEED−FORWARD						
V_{VIN} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	15	17	19	μA/V
Offset current maximum value	V_{pinVIN} = 4.5 V	$I_{offset(MAX)}$	67.5	76.5	85.5	μA
V_{REF} value below which the offset current source is turned off	V_{REF} decreases	$V_{REF(off)}$	–	15	–	mV
V_{REF} value above which the offset current source is turned on	V_{REF} increases	$V_{REF(on)}$	–	20	–	mV
VALLEY SELECTION						
Threshold for line range detection V_{in} increasing (1^{st} to 2^{nd} valley transition for V_{REF} > 0.75 V)	V_{VIN} increases	V_{HL}	2.28	2.4	2.52	V
Threshold for line range detection V_{in} decreasing (2^{nd} to 1^{st} valley transition for V_{REF} > 0.75 V)	V_{VIN} decreases	V_{LL}	2.18	2.3	2.42	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms

4. Guaranteed by design

Table 3. ELECTRICAL CHARACTERISTICS (Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V; For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
VALLEY SELECTION						
Valley thresholds						mV
1st to 2nd valley transition at LL and 2nd to 3rd valley HL	V_{REF} decreases	$V_{VLY1-2/2-3}$	177.5	187.5	197.5	
2nd to 1st valley transition at LL and 3rd to 2nd valley HL	V_{REF} increases	$V_{VLY2-1/3-2}$	185.0	195.0	205.0	
2nd to 4th valley transition at LL and 3rd to 5th valley HL	V_{REF} decreases	$V_{VLY2-4/3-5}$	117.5	125.0	132.5	
4th to 2nd valley transition at LL and 5th to 3rd valley HL	V_{REF} increases	$V_{VLY4-2/5-3}$	125.0	132.5	140.0	
4th to 7th valley transition at LL and 5th to 8th valley HL	V_{REF} decreases	$V_{VLY4-7/5-8}$	–	75.0	–	
7th to 4th valley transition at LL and 8th to 5th valley HL	V_{REF} increases	$V_{VLY7-4/8-5}$	–	82.5	–	
7th to 11th valley transition at LL and 8th to 12th valley HL	V_{REF} decreases	$V_{VLY7-11/8-12}$	–	37.5	–	
11th to 7th valley transition at LL and 12th to 8th valley HL	V_{REF} increases	$V_{VLY11-7/12-8}$	–	50.0	–	
11th to 13th valley transition at LL and 12th to 15th valley HL	V_{REF} decreases	$V_{VLY11-13/12-15}$	–	15.0	–	
13th to 11th valley transition at LL and 15th to 12th valley HL	V_{REF} increases	$V_{VLY13-11/15-12}$	–	20.0	–	
THERMAL SHUTDOWN						
Thermal Shutdown (Note 4)	Device switching (F_{SW} around 65 kHz)	T_{SHDN}	130	155	170	°C
Thermal Shutdown Hysteresis (Note 4)		$T_{SHDN(HYS)}$	–	55	–	°C
BROWN−OUT						
Brown−Out ON level (IC start pulsing)	V_{SD} increasing	$V_{BO(on)}$	0.90	1	1.10	V
Brown−Out OFF level (IC shuts down)	V_{SD} decreasing	$V_{BO(off)}$	0.85	0.9	0.95	V
BO comparators delay		$t_{BO(delay)}$	–	30	–	µs
Brown−Out blanking time		$t_{BO(blank)}$	35	50	65	ms
Brown−out pin bias current		$I_{BO(bias)}$	−250	–	250	nA

4. Guaranteed by design

TYPICAL CHARACTERISTICS

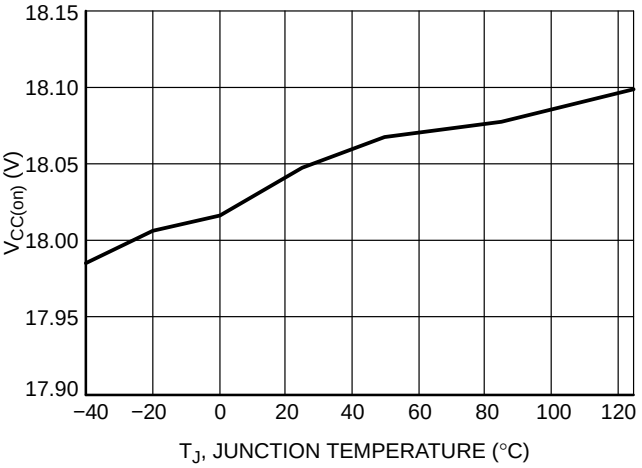


Figure 3. $V_{CC(on)}$ vs. Junction Temperature

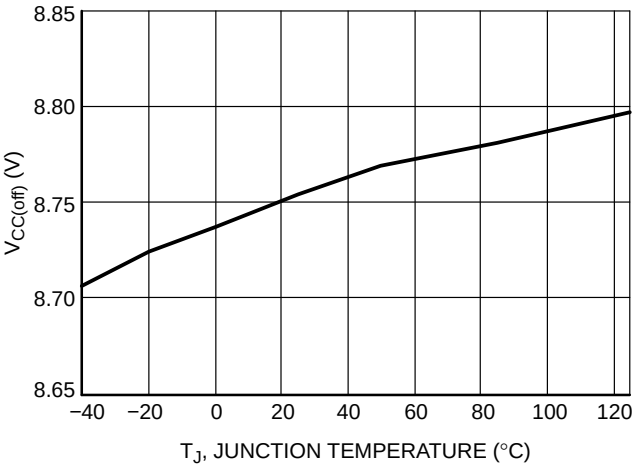


Figure 4. $V_{CC(off)}$ vs. Junction Temperature

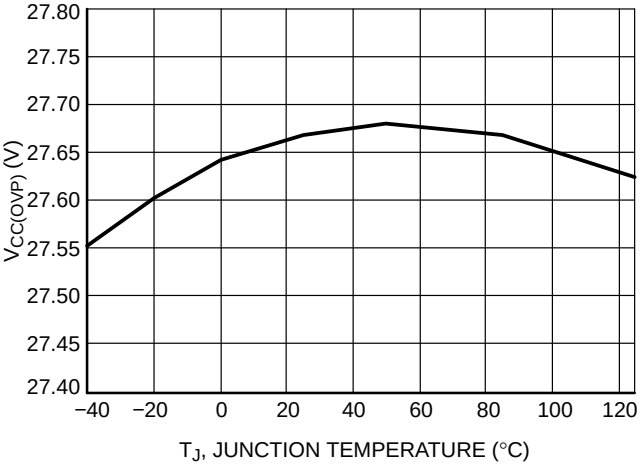


Figure 5. $V_{CC(OVP)}$ vs. Junction Temperature

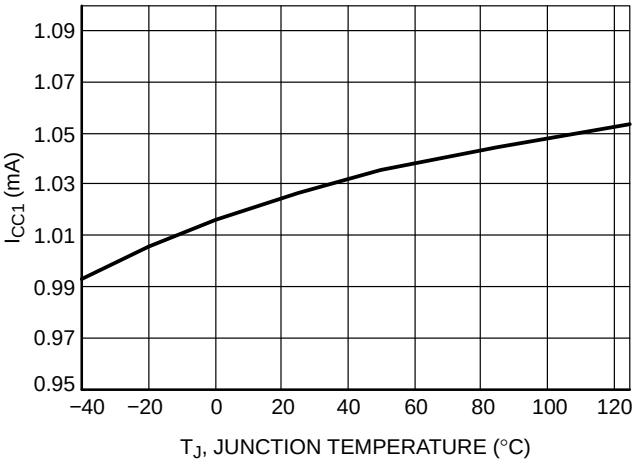


Figure 6. I_{CC1} vs. Junction Temperature

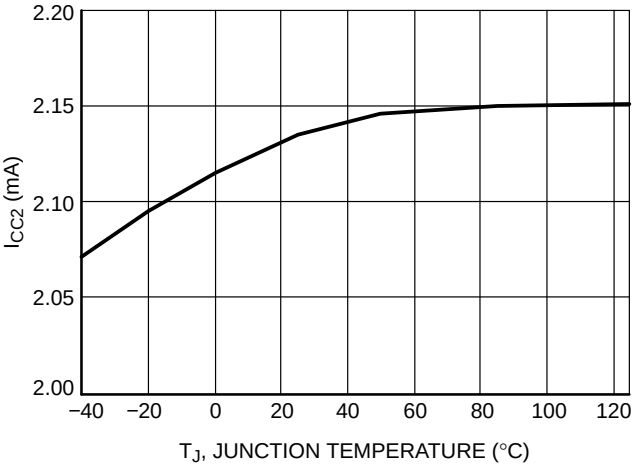


Figure 7. I_{CC2} vs. Junction Temperature

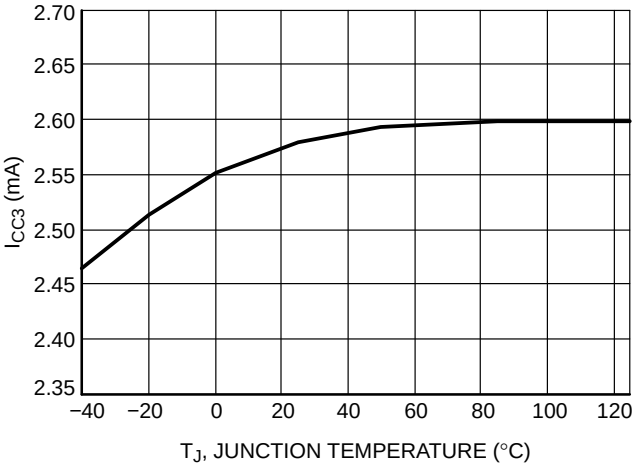


Figure 8. I_{CC3} vs. Junction Temperature

TYPICAL CHARACTERISTICS

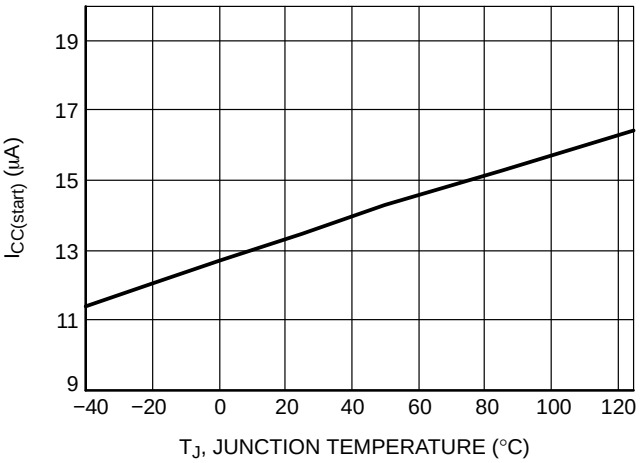


Figure 9. $I_{CC(start)}$ vs. Junction Temperature

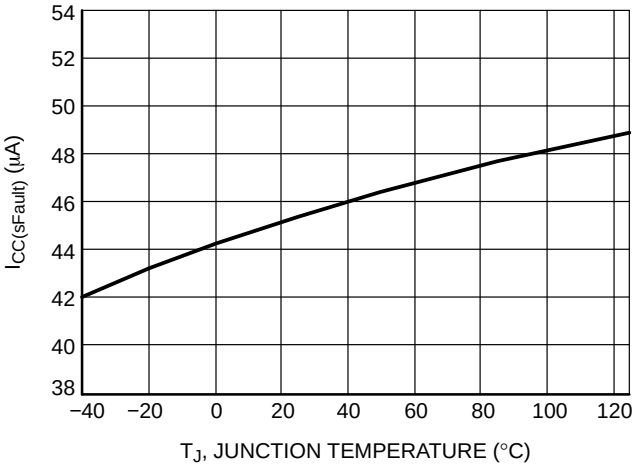


Figure 10. $I_{CC(sFault)}$ vs. Junction Temperature

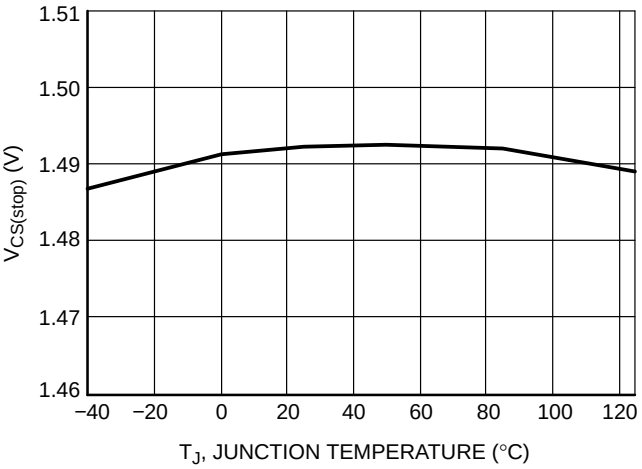


Figure 11. $V_{CS(stop)}$ vs. Junction Temperature

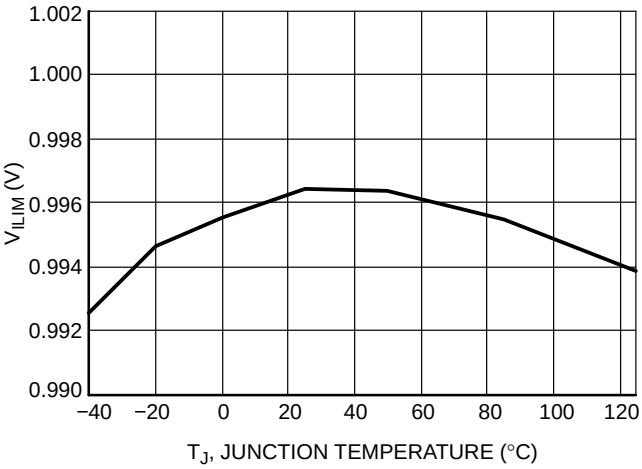


Figure 12. V_{ILIM} vs. Junction Temperature

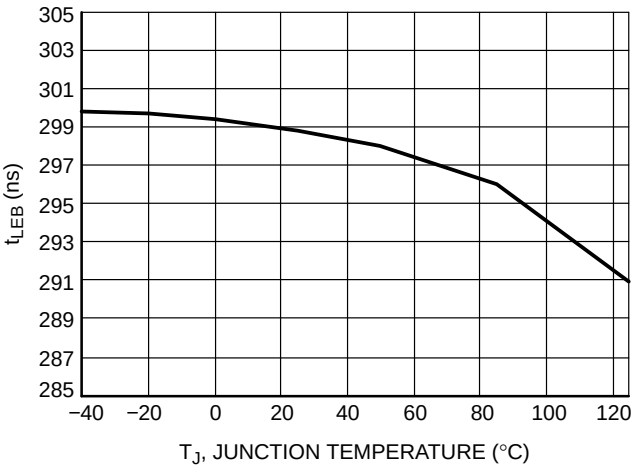


Figure 13. t_{LEB} vs. Junction Temperature

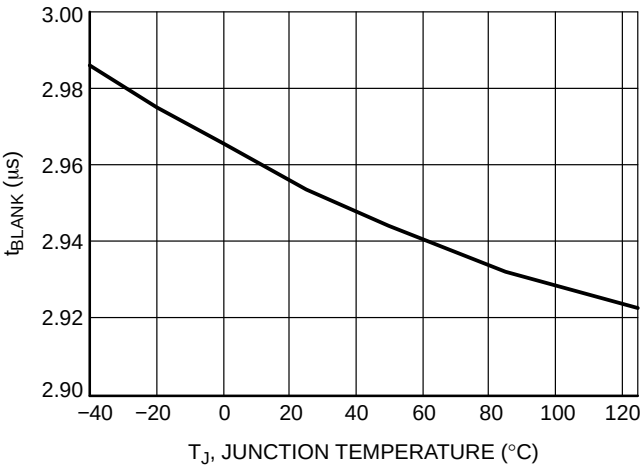


Figure 14. t_{BLANK} vs. Junction Temperature

TYPICAL CHARACTERISTICS

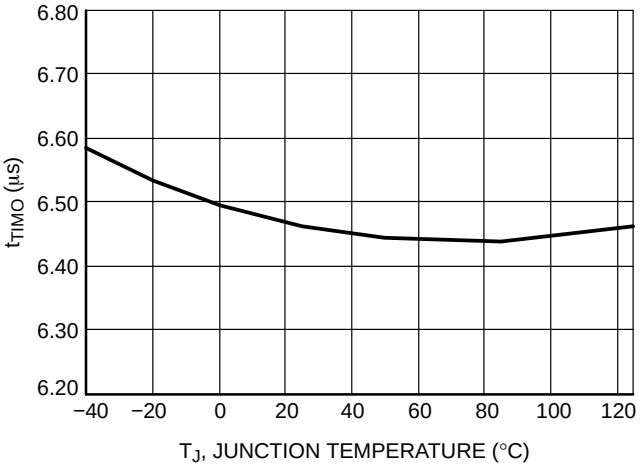


Figure 15. t_{TIMO} vs. Junction Temperature

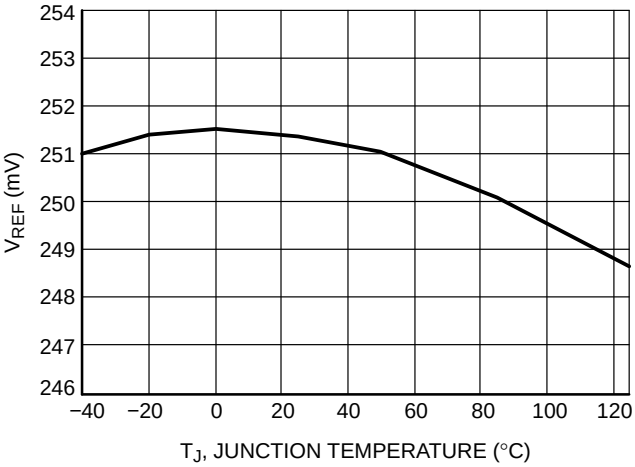


Figure 16. V_{REF} vs. Junction Temperature

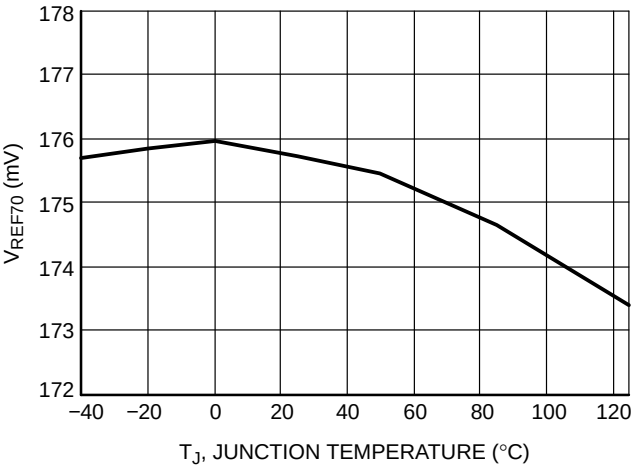


Figure 17. V_{REF70} vs. Junction Temperature

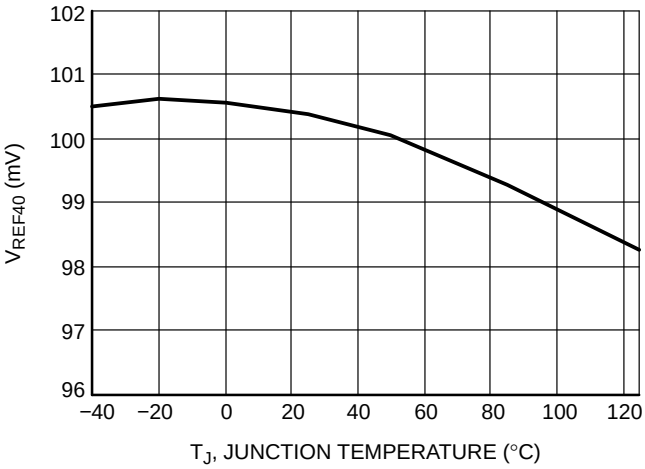


Figure 18. V_{REF40} vs. Junction Temperature

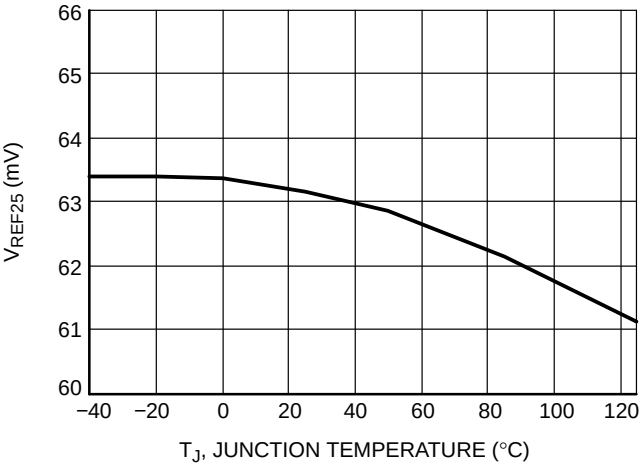


Figure 19. V_{REF25} vs. Junction Temperature

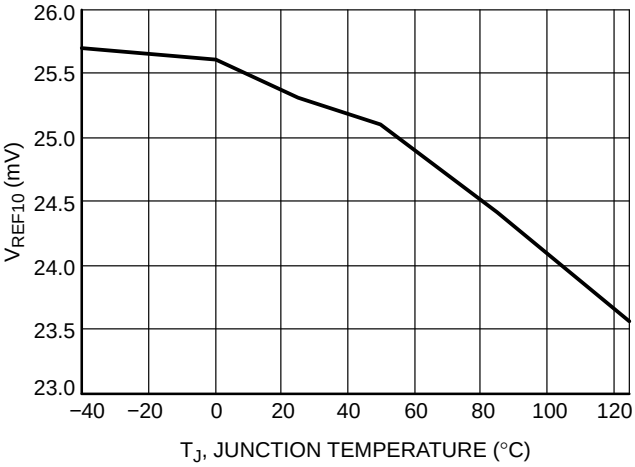


Figure 20. V_{REF10} vs. Junction Temperature

TYPICAL CHARACTERISTICS

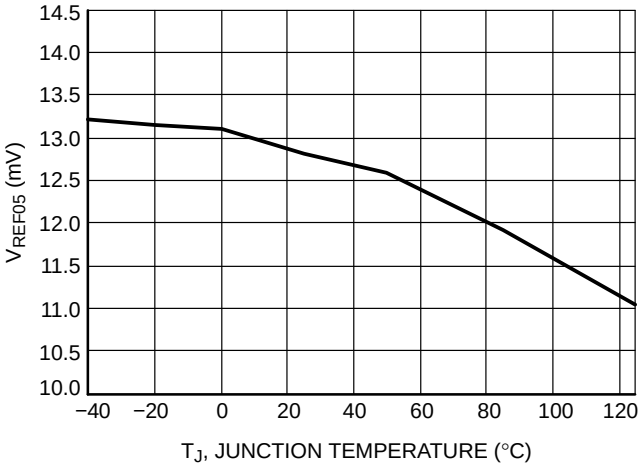


Figure 21. V_{REF05} vs. Junction Temperature

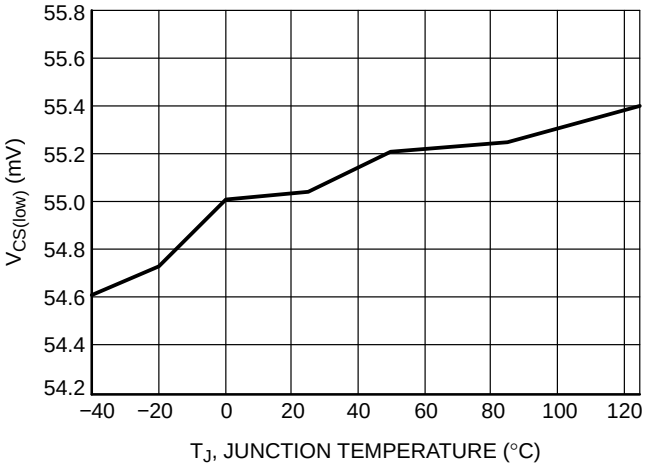


Figure 22. $V_{CS(low)}$ vs. Junction Temperature

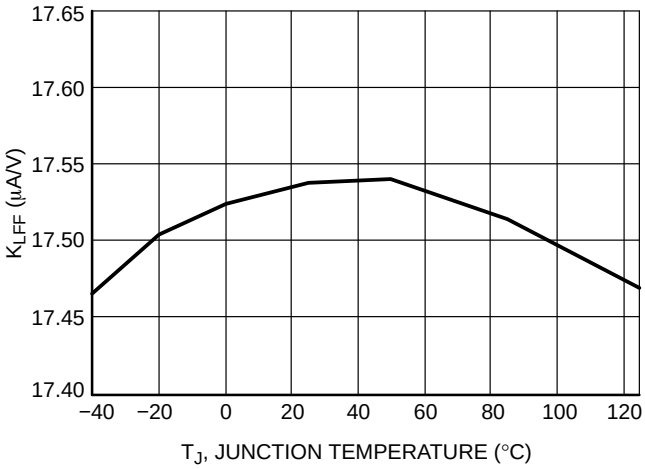


Figure 23. K_{LFF} vs. Junction Temperature

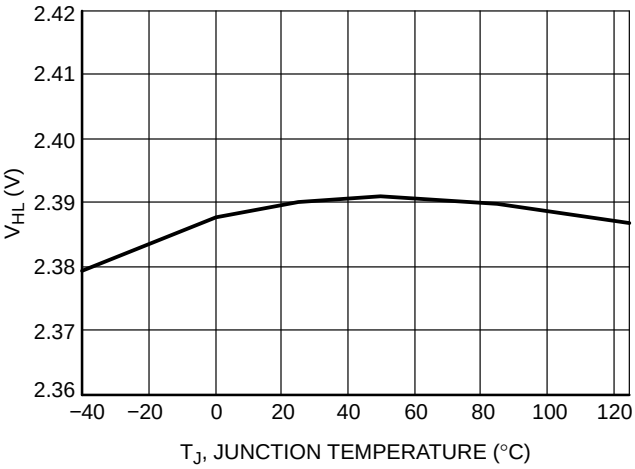


Figure 24. V_{HL} vs. Junction Temperature

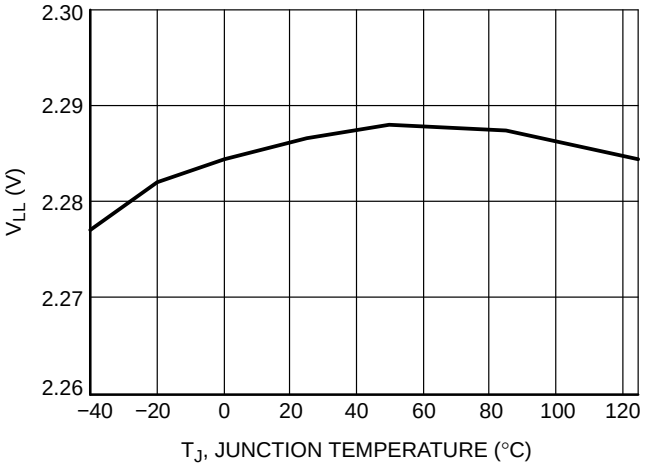


Figure 25. V_{LL} vs. Junction Temperature

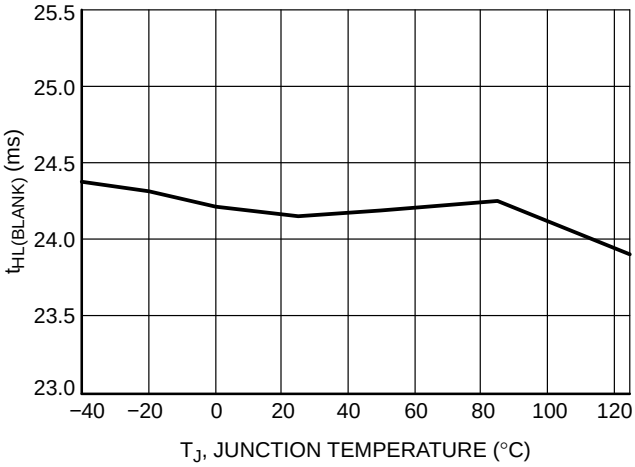


Figure 26. $t_{HL(BLANK)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

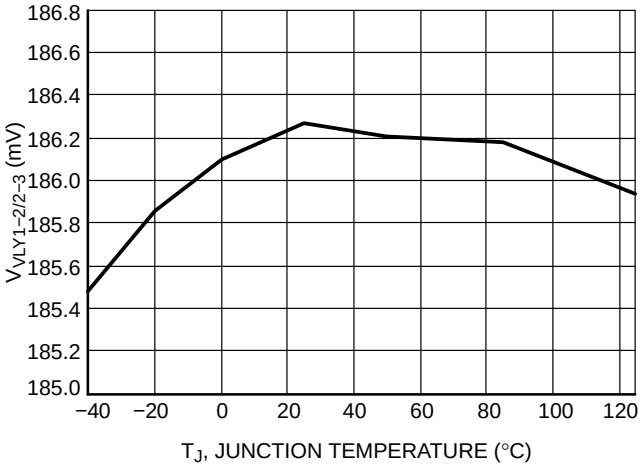


Figure 27. $V_{VLY1-2/2-3}$ vs. Junction Temperature

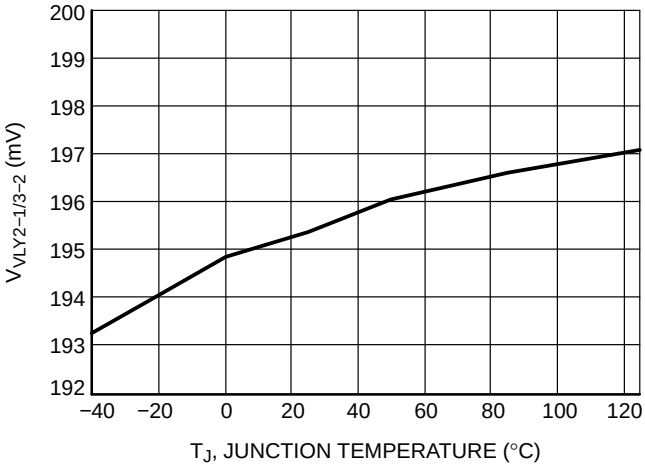


Figure 28. $V_{VLY2-1/3-2}$ vs. Junction Temperature

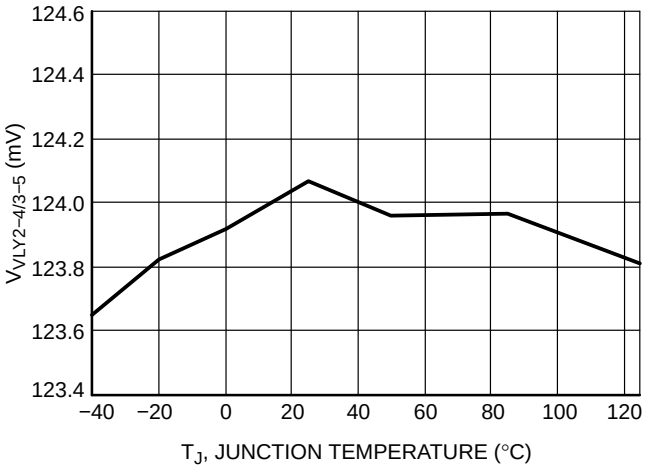


Figure 29. $V_{VLY2-4/3-5}$ vs. Junction Temperature

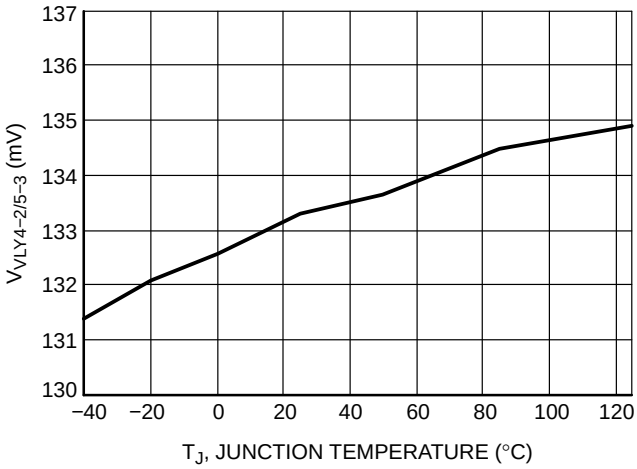


Figure 30. $V_{VLY4-2/5-3}$ vs. Junction Temperature

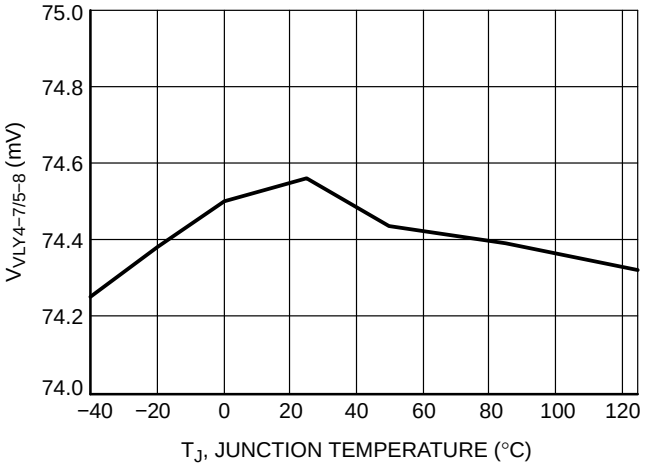


Figure 31. $V_{VLY4-7/5-8}$ vs. Junction Temperature

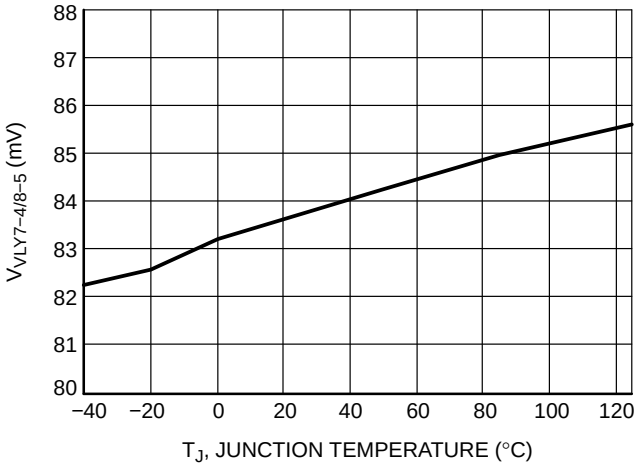


Figure 32. $V_{VLY7-4/8-5}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

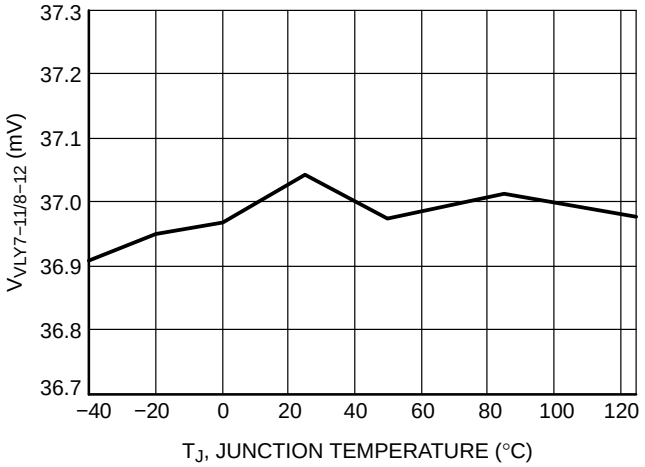


Figure 33. $V_{VLY7–11/8–12}$ vs. Junction Temperature

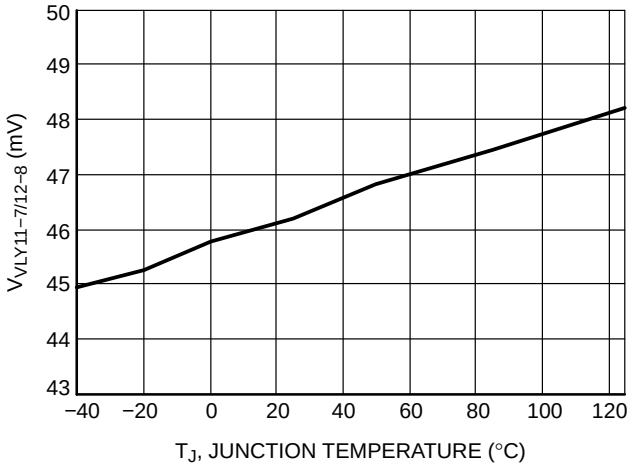


Figure 34. $V_{VLY11–7/12–8}$ vs. Junction Temperature

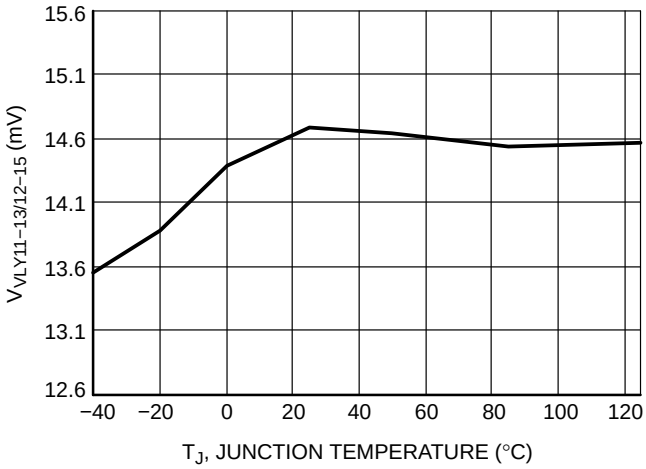


Figure 35. $V_{VLY11–13/12–15}$ vs. Junction Temperature

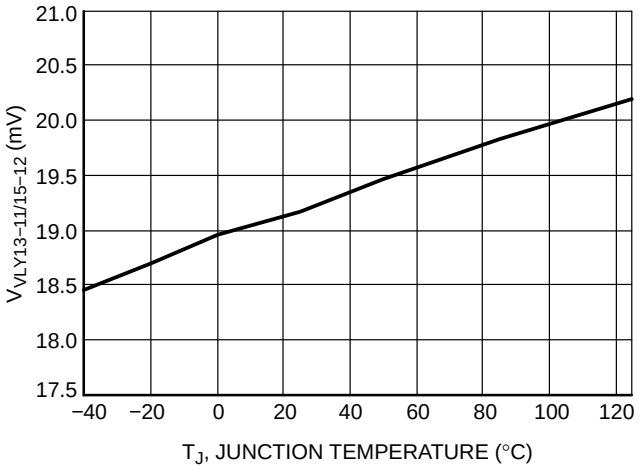


Figure 36. $V_{VLY13–11/15–12}$ vs. Junction Temperature

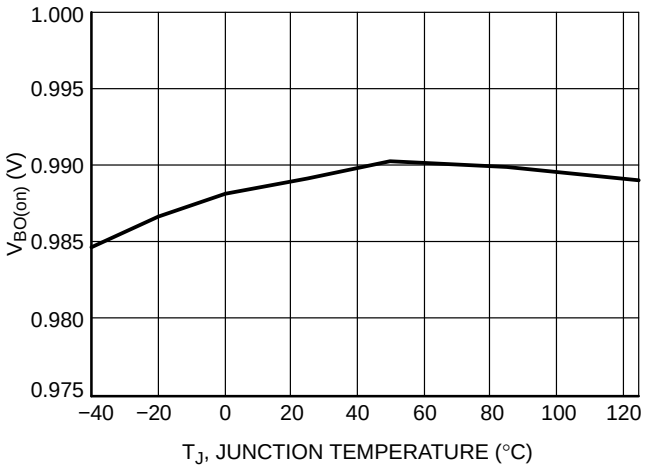


Figure 37. $V_{BO(on)}$ vs. Junction Temperature

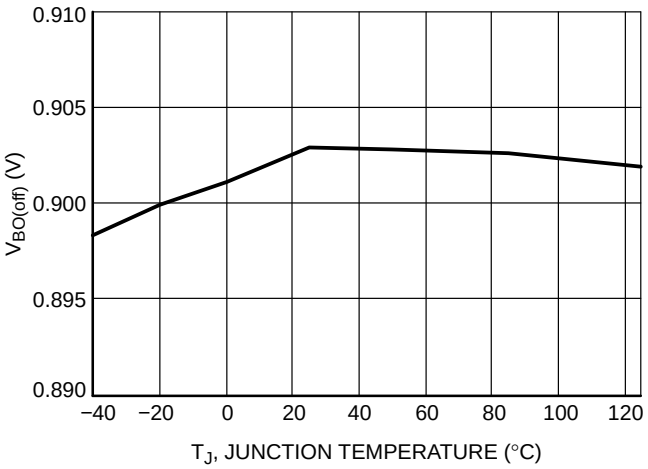


Figure 38. $V_{BO(off)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

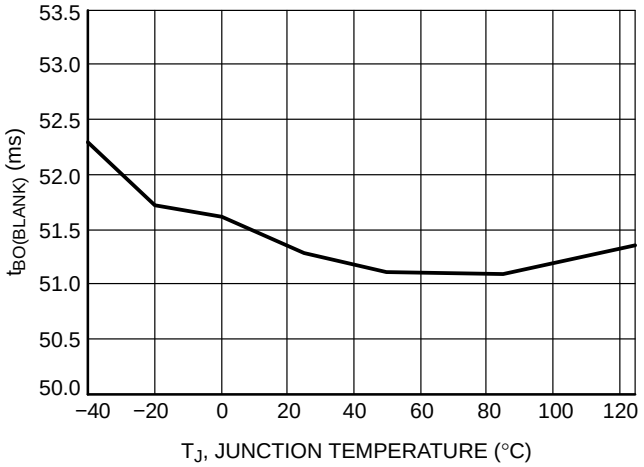


Figure 39. $t_{BO(BLANK)}$ vs. Junction Temperature

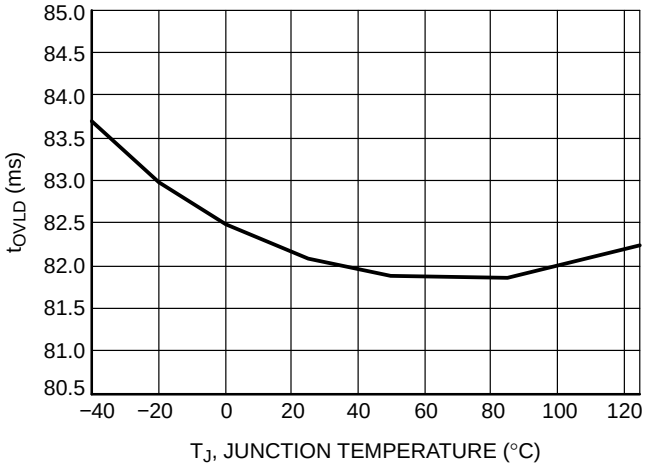


Figure 40. t_{OVLD} vs. Junction Temperature

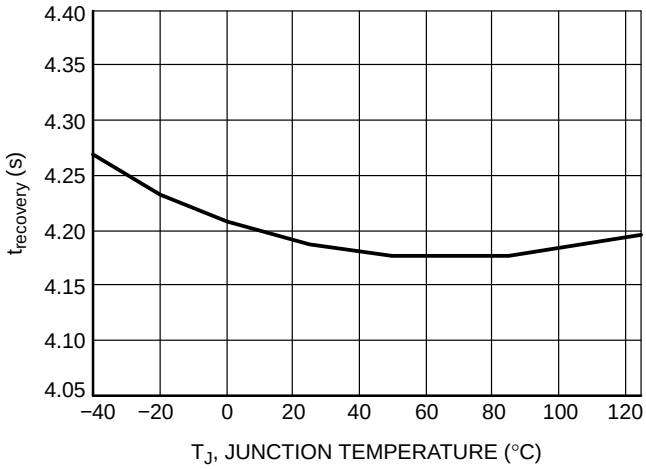


Figure 41. $t_{recovery}$ vs. Junction Temperature

Application Information

The **NCL30081** implements a current−mode architecture operating in quasi−resonant mode. Thanks to proprietary circuitry, the controller is able to accurately regulate the secondary side current of the flyback converter without using any opto−coupler or measuring directly the secondary side current.

- **Quasi−Resonance Current−Mode Operation:** implementing quasi−resonance operation in peak current−mode control, the NCL30081 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Thanks to a smart control algorithm, the controller locks−out in a selected valley and remains locked until the input voltage or the output current set point significantly changes.
- **Primary Side Constant Current Control:** thanks to a proprietary circuit, the controller is able to compensate for the leakage inductance of the transformer and allow accurate control of the secondary side current.
- **Line Feed−forward:** compensation for possible variation of the output current caused by system slew rate variation.
- **Open LED protection:** if the voltage on the VCC pin exceeds an internal limit, the controller shuts down and waits 4 seconds before restarting switching.
- **Brown−Out:** the controller includes a brown−out circuit with a validation timer which safely stops the controller in the event that the input voltage is too low. The device will automatically restart if the line recovers.
- **Cycle−by−cycle peak current limit:** when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- **Winding Short−Circuit Protection:** an additional comparator with a short LEB filter (t_{BCS}) senses the CS signal and stops the controller if V_{CS} reaches 1.5 x V_{ILIM}. For noise immunity reasons, this comparator is enabled only during the main LEB duration t_{LEB}.
- **Output Short−circuit protection:** If a very low voltage is applied on ZCD pin for 90 ms (nominal), the controllers assume that the output or the ZCD pin is shorted to ground and enters shutdown. The auto−restart version (B suffix) waits 4 seconds, then the controller restarts switching. In the latched version (A suffix), the controller is latched as long as V_{CC} stays above the $V_{CC(reset)}$ threshold.
- **Step dimming:** Each time the IC detects a brown−out condition, the output current is decreased by discrete steps.

Constant Current Control

Figure 43 portrays the primary and secondary current of a flyback converter in discontinuous conduction mode (DCM). Figure 42 shows the basic circuit of a flyback converter.

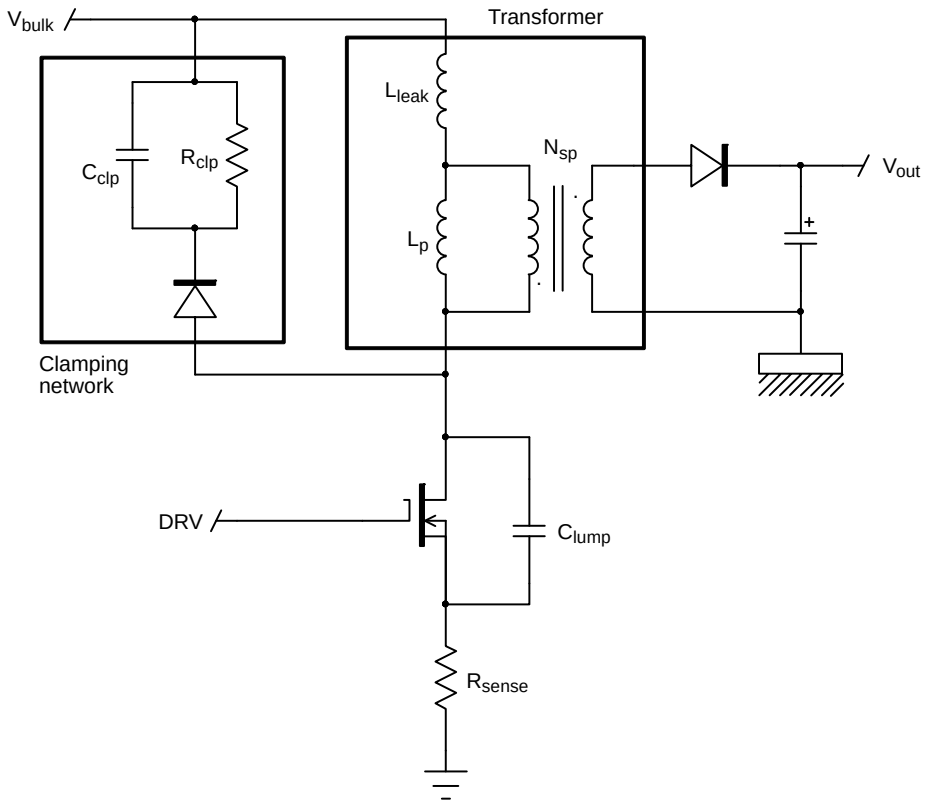


Figure 42. Basic Flyback Converter Schematic

During the on−time of the MOSFET, the bulk voltage V_{bulk} is applied to the magnetizing and leakage inductors L_p and L_{leak} and the current ramps up.

When the MOSFET is turned−off, the inductor current first charges C_{lump}. The output diode is off until the voltage across L_p reverses and reaches:

$$N_{sp}\left(V_{out} + V_f\right) \quad \text{(eq. 1)}$$

The output diode current increase is limited by the leakage inductor. As a consequence, the secondary peak current is reduced:

$$I_{D,pk} < \frac{I_{L,pk}}{N_{sp}} \quad \text{(eq. 2)}$$

The diode current reaches its peak when the leakage inductor is reset. Thus, in order to accurately regulate the output current, we need to take into account the leakage inductor current. This is accomplished by sensing the clamping network current. Practically, a node of the clamp capacitor is connected to R_{sense} instead of the bulk voltage V_{bulk}. Then, by reading the voltage on the CS pin, we have an image of the primary current (red curve in Figure 43).

When the diode conducts, the secondary current decreases linearly from $I_{D,pk}$ to zero. When the diode current has turned off, the drain voltage begins to oscillate because of the resonating network formed by the inductors (L_p+L_{leak}) and the lump capacitor. This voltage is reflected on the auxiliary winding wired in flyback mode. Thus, by looking at the auxiliary winding voltage, we can detect the end of the conduction time of secondary diode. The constant current control block picks up the leakage inductor current, the end of conduction of the output rectifier and controls the drain current to maintain the output current constant.

We have:

$$I_{out} = \frac{V_{REF}}{2N_{sp}R_{sense}} \quad \text{(eq. 3)}$$

The output current value is set by choosing the sense resistor:

$$R_{sense} = \frac{V_{ref}}{2N_{sp}I_{out}} \quad \text{(eq. 4)}$$

From Equation 3, the first key point is that the output current is independent of the inductor value. Moreover, the leakage inductance does not influence the output current value as the reset time is taken into account by the controller.

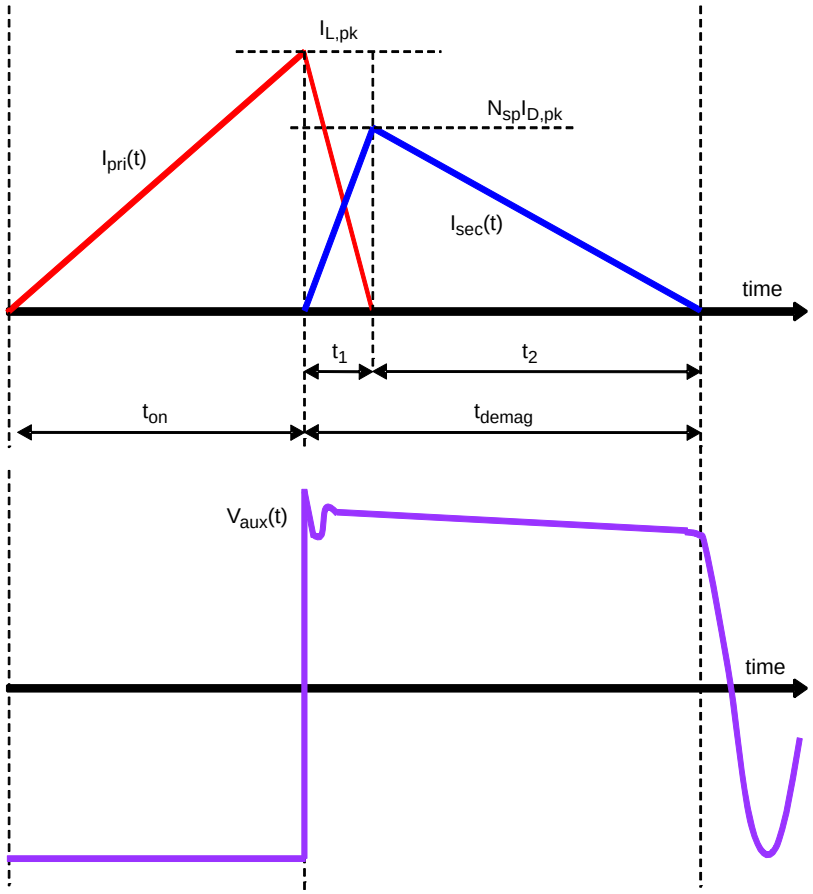


Figure 43. Flyback Currents and Auxiliary Winding Voltage in DCM

Internal Soft−Start

At startup or after recovering from a fault, there is a small internal soft−start of 40 μs.

In addition, during startup, as the output voltage is zero volts, the demagnetization time is long and the constant current control block will slowly increase the peak current towards its nominal value as the output voltage grows. Figure 44 shows a soft−start simulation example for a 9 W LED power supply.

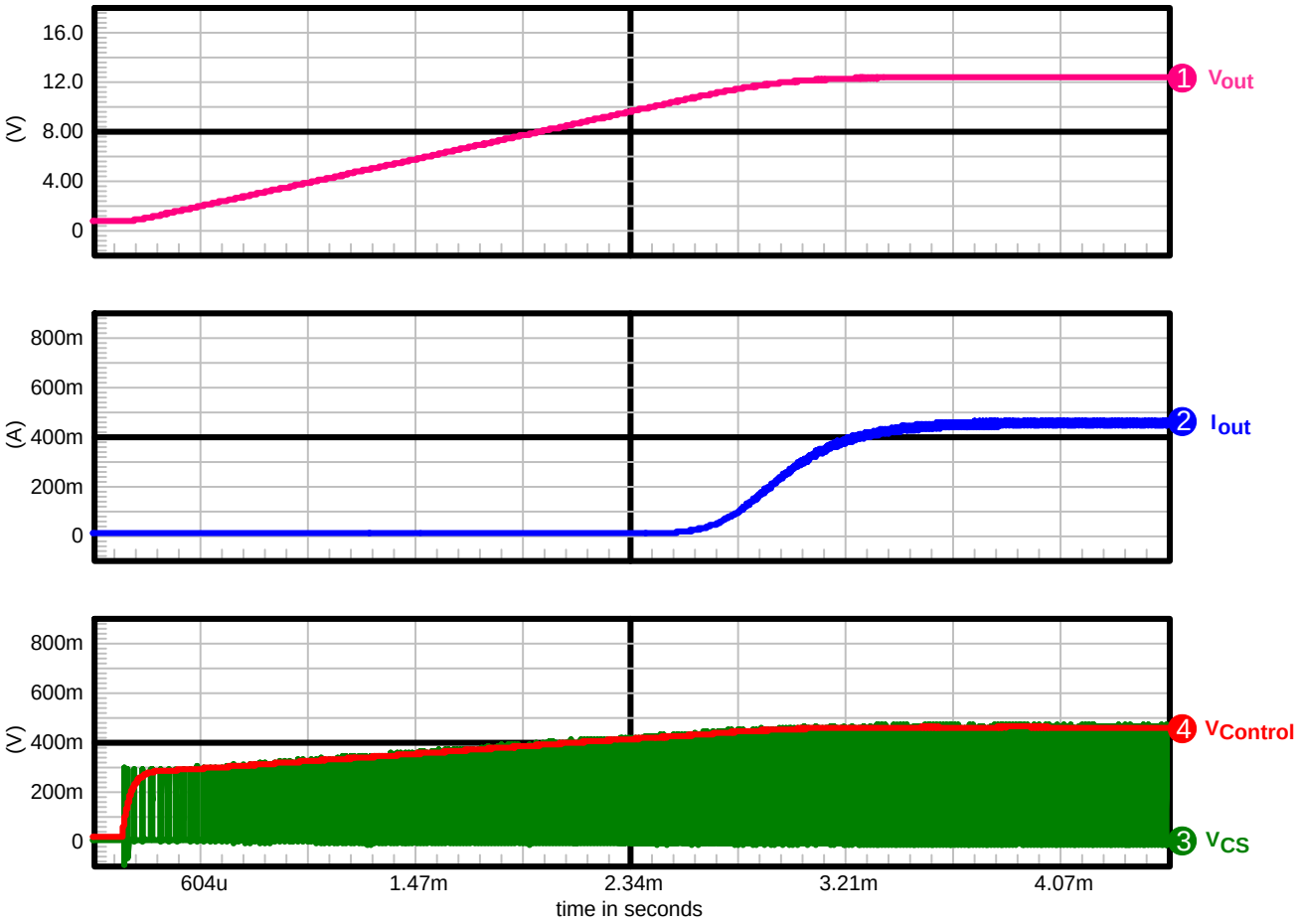


Figure 44. Startup Simulation Showing the Natural Soft−start

Cycle−by−Cycle Current Limit

When the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle (Figure 45).

Winding and Output Diode Short−Circuit Protection

In parallel with the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a higher threshold (1.5 V typical) is able to sense winding short−circuit and immediately stops the DRV pulses. The controller goes into auto−recovery mode in version B.

In version A, the controller is latched. In latch mode, the DRV pulses stop and VCC ramps up and down. The circuit un−latches when VCC pin voltage drops below $V_{CC(reset)}$ threshold.

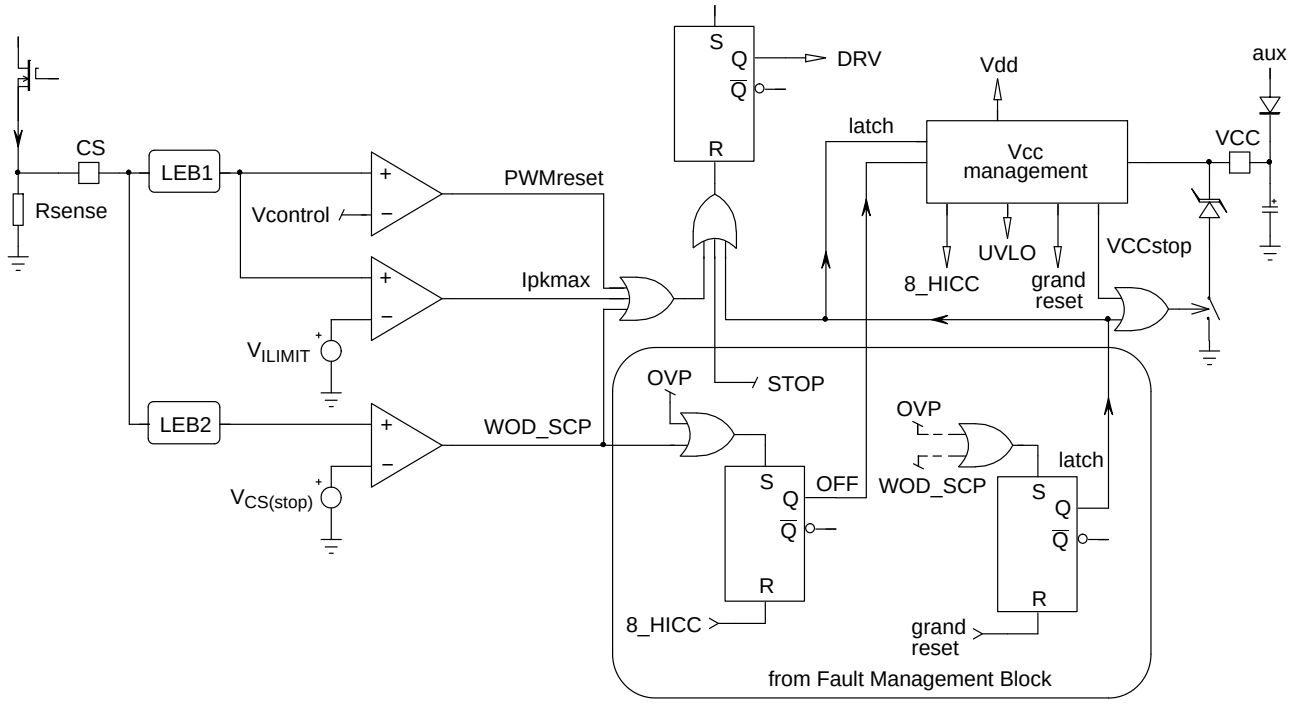


Figure 45. Winding Short Circuit Protection, Max. Peak Current Limit Circuits

Step Dimming

The step dimming function decreases the output current from 100% to 5% of its nominal value in discrete steps. There are 5 steps in total. Table 4 shows the different steps value and the corresponding output current set−point. Each time a brown−out is detected, the output current is decreased by decreasing the reference voltage V_{REF} setting the output current value.

When the 5% dimming step is reached, if a brown−out event occurs, the controller restarts at 100% of the output current.

Table 4. DIMMING STEPS

Dimming Step	I_{out}	Perceived Light
ON	100%	100%
1	70%	84%
2	40%	63%
3	25%	50%
4	10%	32%
5	5%	17%

Note:

The power supply designer must ensure that V_{CC} stays high enough when the light is turned−off to let the controller memorize the dimming step state.

The power supply designer should use a split V_{CC} circuit for step dimming with a capacitor allowing providing enough V_{CC} for 1 s (47 μF to 100 μF capacitor).

The step dimming state is memorized by the controller until V_{CC} crosses $V_{CC(reset)}$.

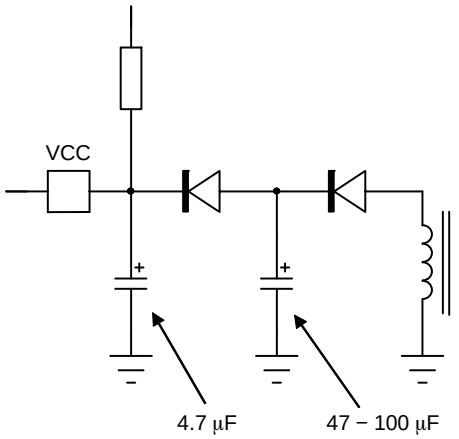


Figure 46. Split VCC Supply

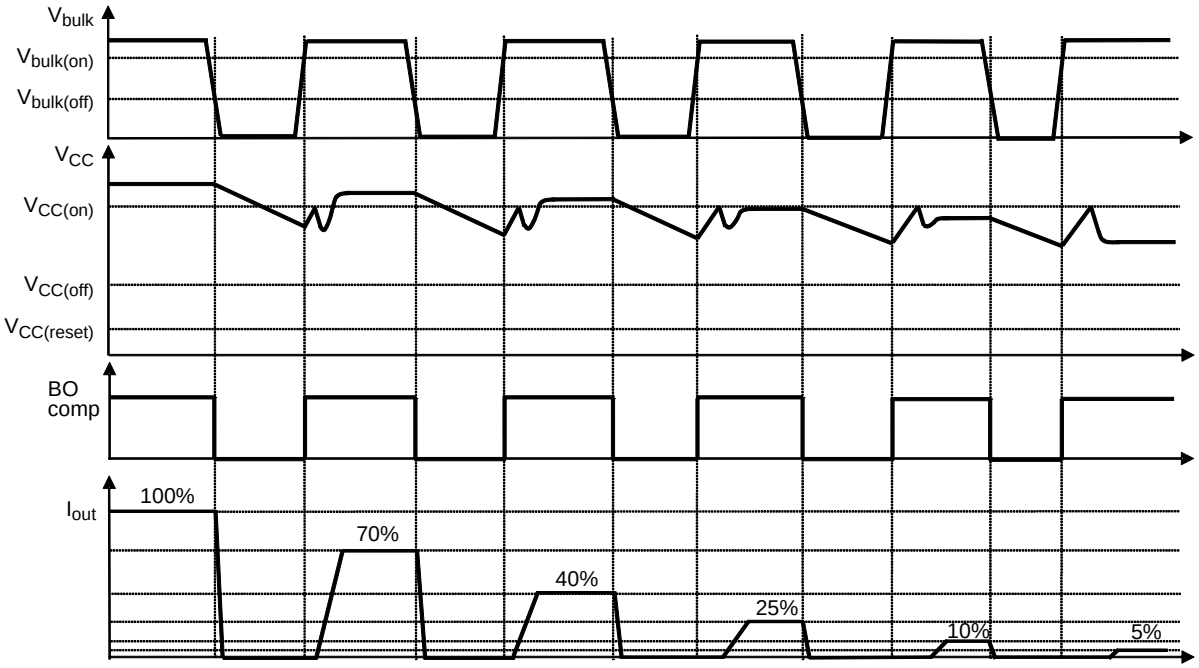


Figure 47. Step Dimming Chronograms

V_{CC} Over Voltage Protection (Open LED Protection)

If no output load is connected to the LED power supply, the controller must be able to safely limit the output voltage excursion.

In the NCL30081, when the V_{CC} voltage reaches the $V_{CC(OVP)}$ threshold, the controller stops the DRV pulses and the 4−s timer starts counting. The IC re−start switching after the 4−s timer has elapsed as long as $V_{CC} \geq V_{CC(on)}$. This is illustrated in Figure 48.

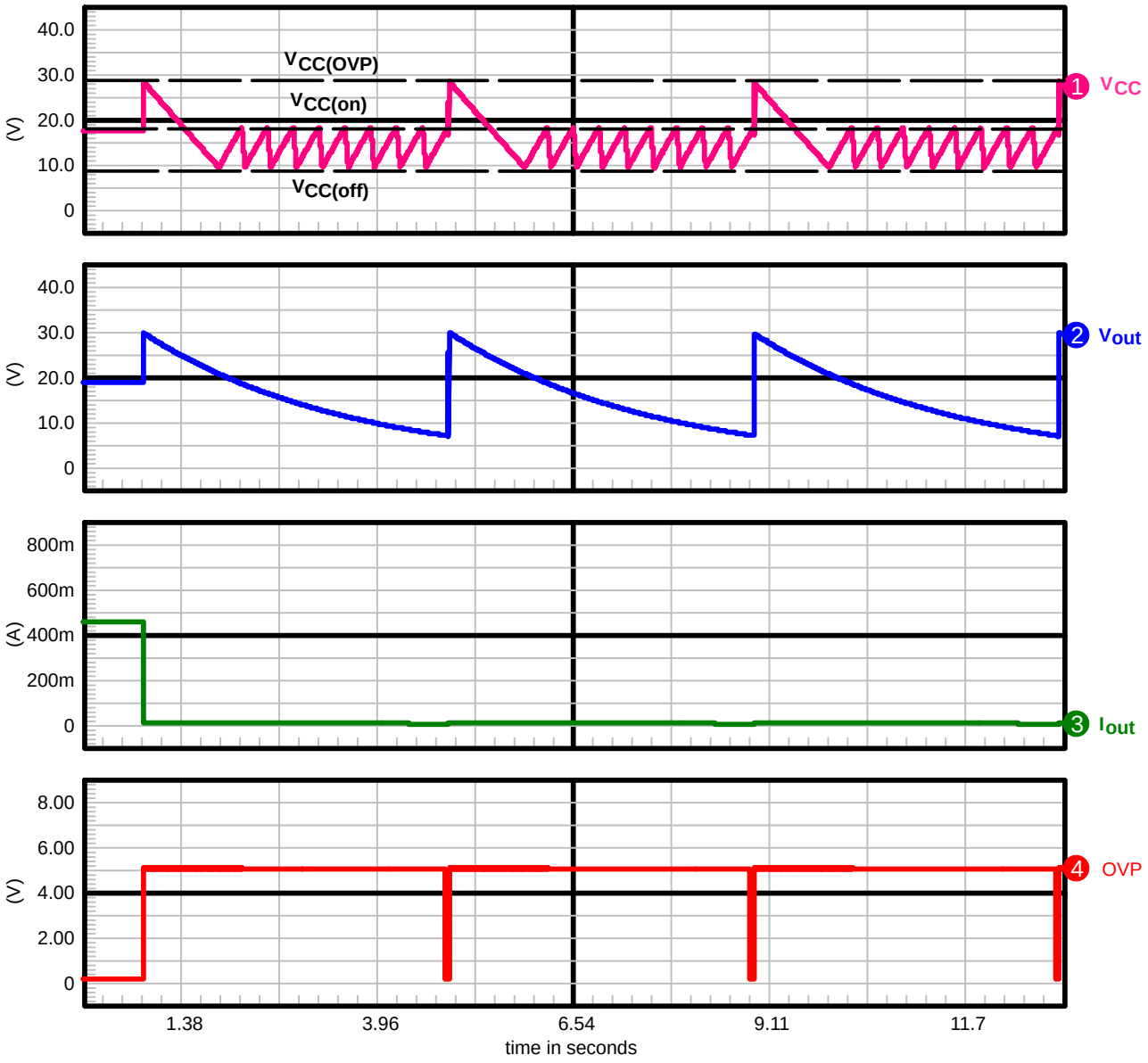


Figure 48. Open LED Protection Chronograms

Valley Lockout

Quasi−Square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

The NCL30081 changes valley as the input voltage increases and as the output current set−point is varied (thermal fold−back and step dimming). This limits the switching frequency excursion. Once a valley is selected, the controller stays locked in the valley until the input voltage or the output current set−point varies significantly. This avoids valley jumping and the inherent noise caused by this phenomenon.

The input voltage is sensed by the VIN pin. The internal logic selects the operating valley according to VIN pin voltage (Figure 49) and the dimming state imposed by the Step Dimming feature.

By default, when the output current is not dimmed, the controller operates in the first valley at low line and in the second valley at high line.

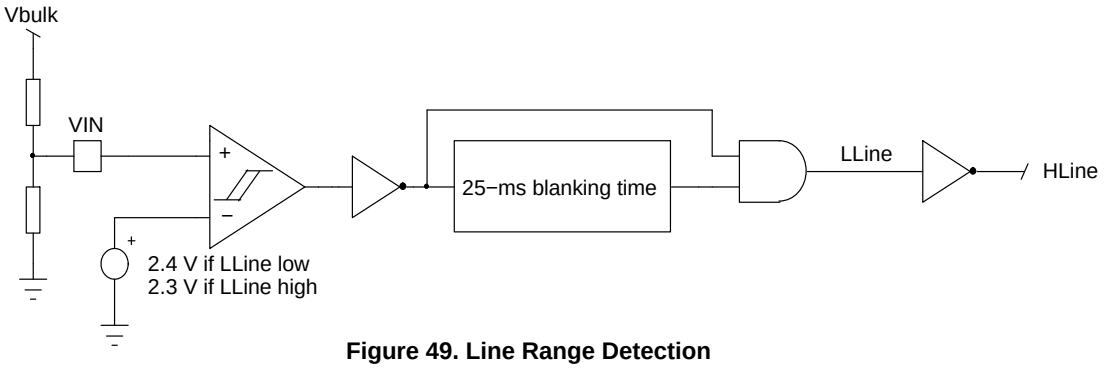


Figure 49. Line Range Detection

Table 5. VALLEY SELECTION

I_{out} value at which the controller changes valley (I_{out} decreasing)	VIN pin voltage for valley change					I_{out} value at which the controller changes valley (I_{out} increasing)
	V_{VIN} decreases ←					
	0	−LL−	2.3 V	−HL−	5 V	
100%		1st		2nd		100%
75%		2nd		3rd		78%
50%		4th		5th		53%
30%		7th		8th		33%
15%		11th		12th		20%
6%		13th		15th		8%
0%						0%
I_{out} decreases ↓						I_{out} increases ↑
	0	−LL−	2.4 V	−HL−	5 V	
	V_{VIN} increases →					
	VIN pin voltage for valley change					

Zero Crossing Detection Block

The ZCD pin allows detecting when the drain−source voltage of the power MOSFET reaches a valley.

A valley is detected when the voltage on pin 1 crosses below the $V_{ZCD(THD)}$ internal threshold.

At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, the NCL30081 features a Time−Out circuit that generates pulses if the voltage on ZCD pin stays below the $V_{ZCD(THD)}$ threshold for 6.5 μs.

The time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case of too damped free oscillations.

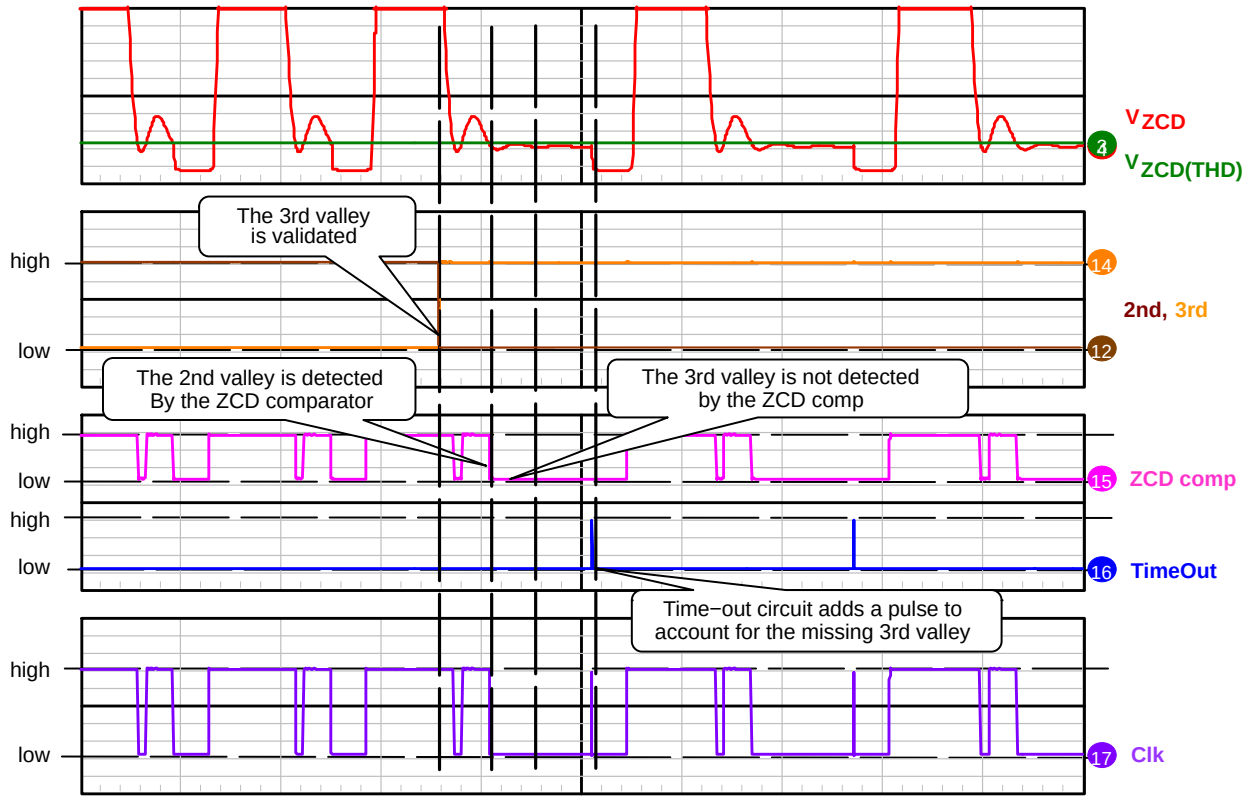


Figure 50. Time−out Chronograms

Normally with this type of time−out function, in the event the ZCD pin or the auxiliary winding is shorted, the controller could continue switching leading to improper regulation of the LED current. Moreover during an output short circuit, the controller will strive to maintain constant current operation.

To avoid these scenarios, a protection circuit consisting of a comparator and secondary timer starts counting when the ZCD voltage is below the $V_{ZCD(short)}$ threshold. If this timer reaches 90 ms, the controller detects a fault and shutdown. The auto−restart version (B suffix) waits 4 seconds, then the controller restarts switching. In the latched version (A suffix), the controller is latched as long as V_{CC} stays above the $V_{CC(reset)}$ threshold.

Line Feed−forward

Because of internal and external propagation delays, the MOSFET is not turned−off immediately when the current set−point is reached. As a result, the primary peak current is slightly higher than expected resulting in a small output current error which can be compensated for during component selection.

Normally this error would increase if the input line voltage increased because the slew rate through the primary inductance would increase. To compensate the peak current increase brought by the variation, a positive voltage proportional to the line voltage is added to the current sense signal. The amount of offset voltage can be adjusted using the R_{LFF} resistor as shown in Figure 51. The offset voltage is applied only during the MOSFET on−time and when I_{out} is above 6% of the nominal output current.

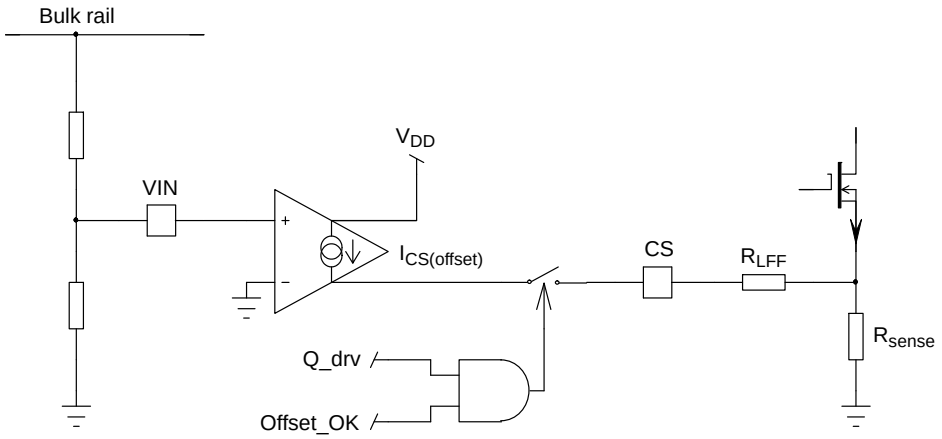


Figure 51. Line Feed−forward Schematic

Brown−out

In order to protect the supply against a very low input voltage, the NCL30081 features a brown−out circuit with a fixed ON/OFF threshold. The controller is allowed to start if a voltage higher than 1 V is applied to the VIN pin and shuts−down if the VIN pin voltage decreases and stays below 0.9 V for 50 ms nominal. Exiting a brown−out condition overrides the hiccup on V_{CC} (V_{CC} does not wait to reach $V_{CC(off)}$) and the IC immediately goes into startup mode ($I_{CC} = I_{CC(start)}$).

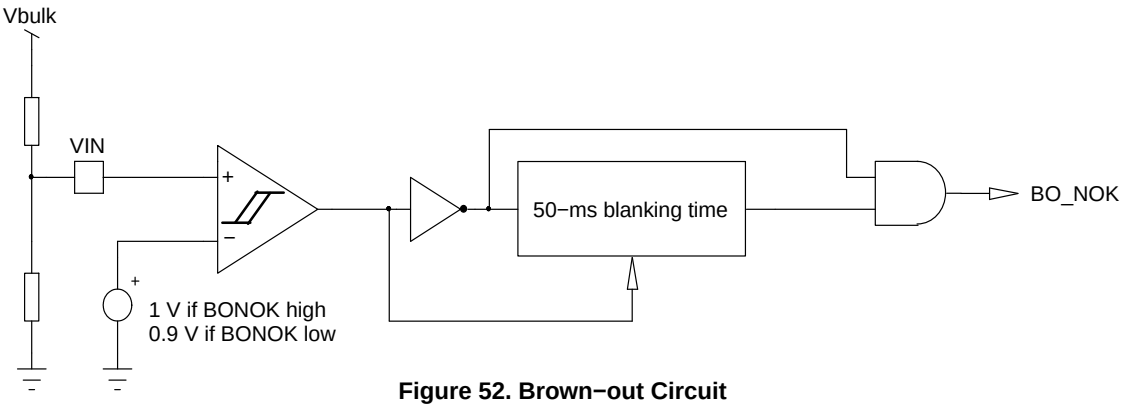


Figure 52. Brown−out Circuit

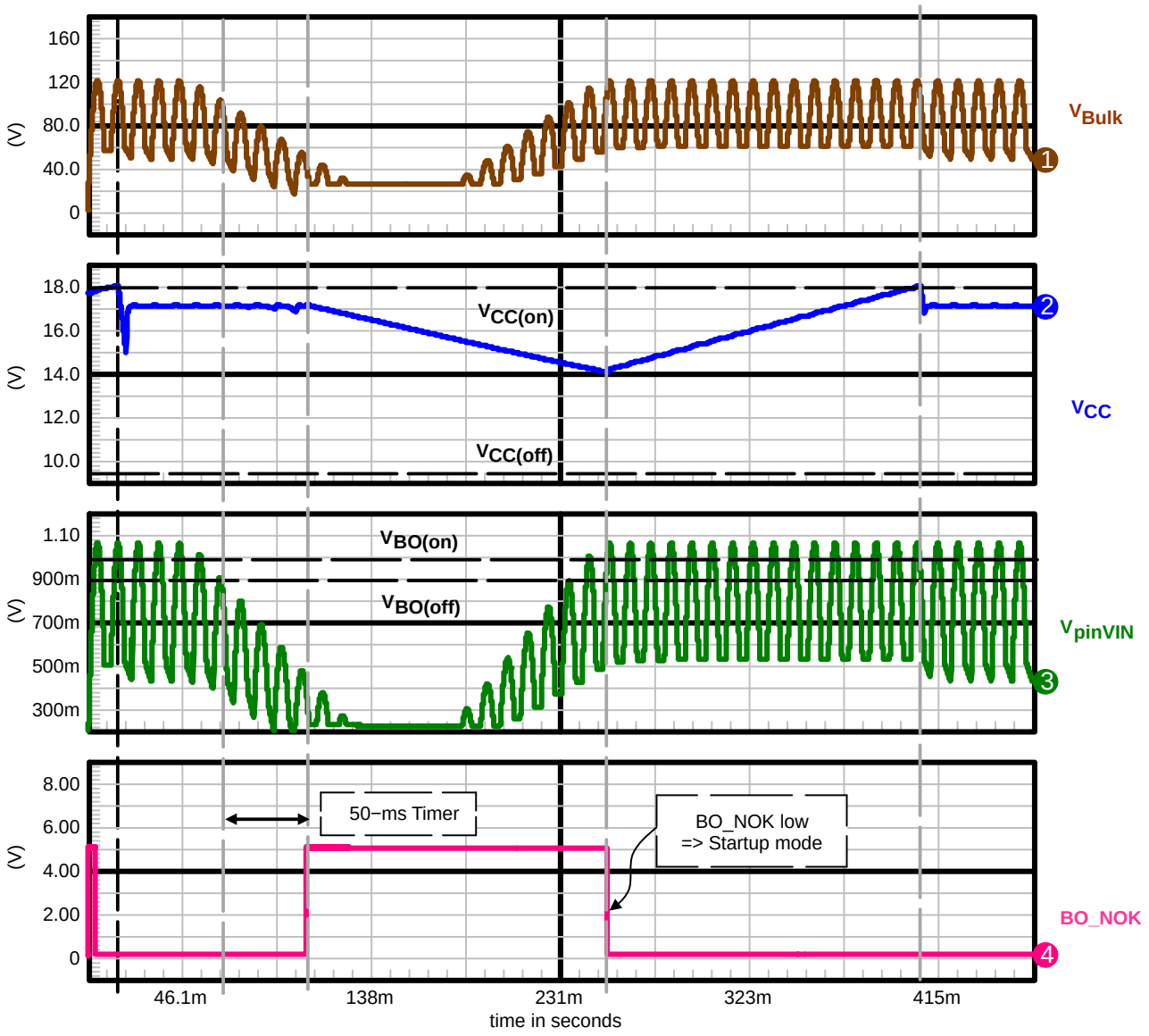


Figure 53. Brown−Out Chronograms (Valley Fill circuit is used)

CS Pin Short Circuit Protection

Normally, if the CS pin or the sense resistor is shorted to ground, the Driver will not be able to turn off, leading to potential damage of the power supply. To avoid this, the NCL30081 features a circuit to protect the power supply against a short circuit of the CS pin. When the MOSFET is on, if the CS voltage stays below $V_{CS(low)}$ after the adaptive blanking timer has elapsed, the controller shuts down and will attempt to restart on the next V_{CC} hiccup.

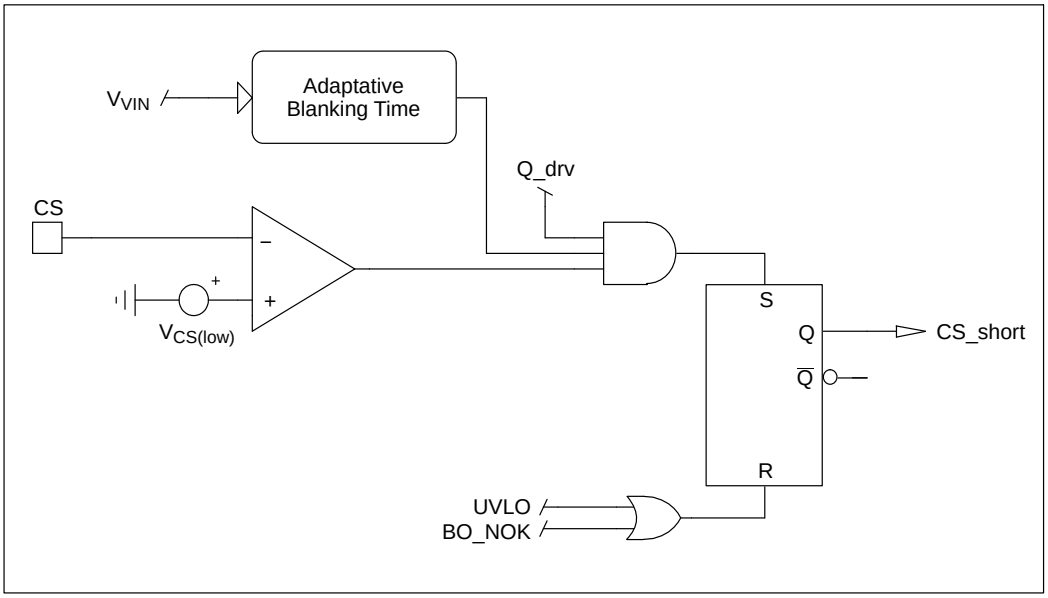


Figure 54. CS Pin Short Circuit Protection Schematic

Fault Management

OFF Mode

The circuit turns off whenever a major condition prevents it from operating:

- Incorrect feeding of the circuit: “UVLO high”. The UVLO signal becomes high when V_{CC} drops below $V_{CC(off)}$ and remains high until V_{CC} exceeds $V_{CC(on)}$.
- V_{CC} OVP
- Output diode short circuit protection: “WOD_SCP high”
- Output / Auxiliary winding Short circuit protection: “Aux_SCP high”
- Die over temperature (TSD)
- Brown−Out: “BO_NOK” high
- Pin CS short circuited to GND: “CS_short high”

In this mode, the DRV pulses are stopped and the controller turn−off some circuits to decrease the internal consumption. V_{CC} voltage decrease through the controller own consumption (I_{CC1}).

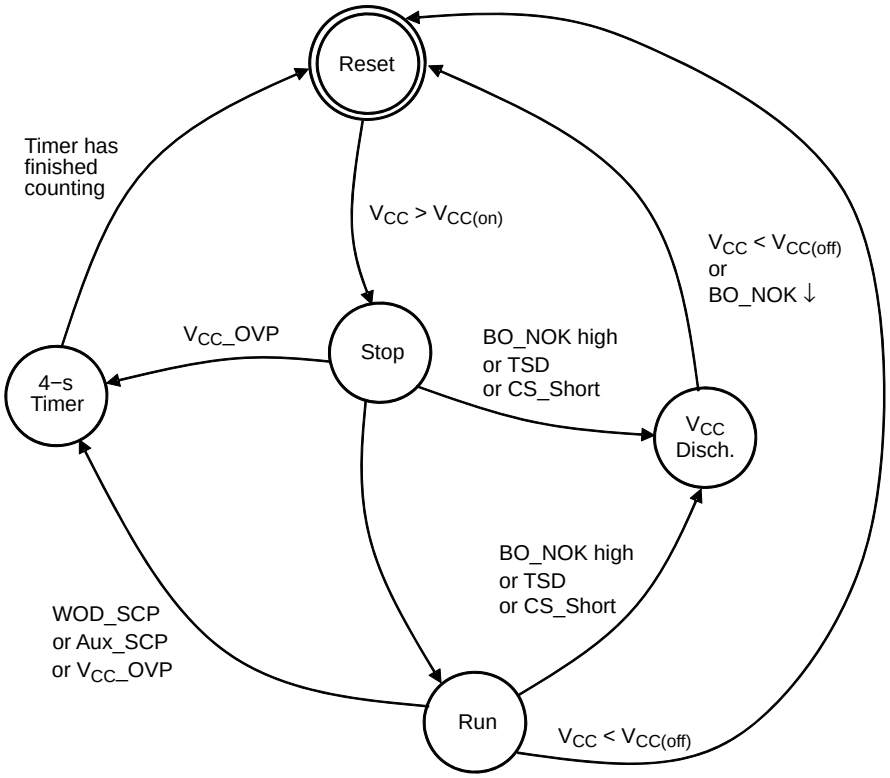
For the output diode short circuit protection, the output / aux. winding short circuit protection and the V_{CC} OVP, the controller waits 4 seconds (auto−recovery timer) and then initiates a startup sequence ($V_{CC} \geq V_{CC(on)}$) before re−starting switching.

Latch Mode

This mode is activated by the output diode short−circuit protection (WOD_SCP) and the Aux_SCP in **version A only.**

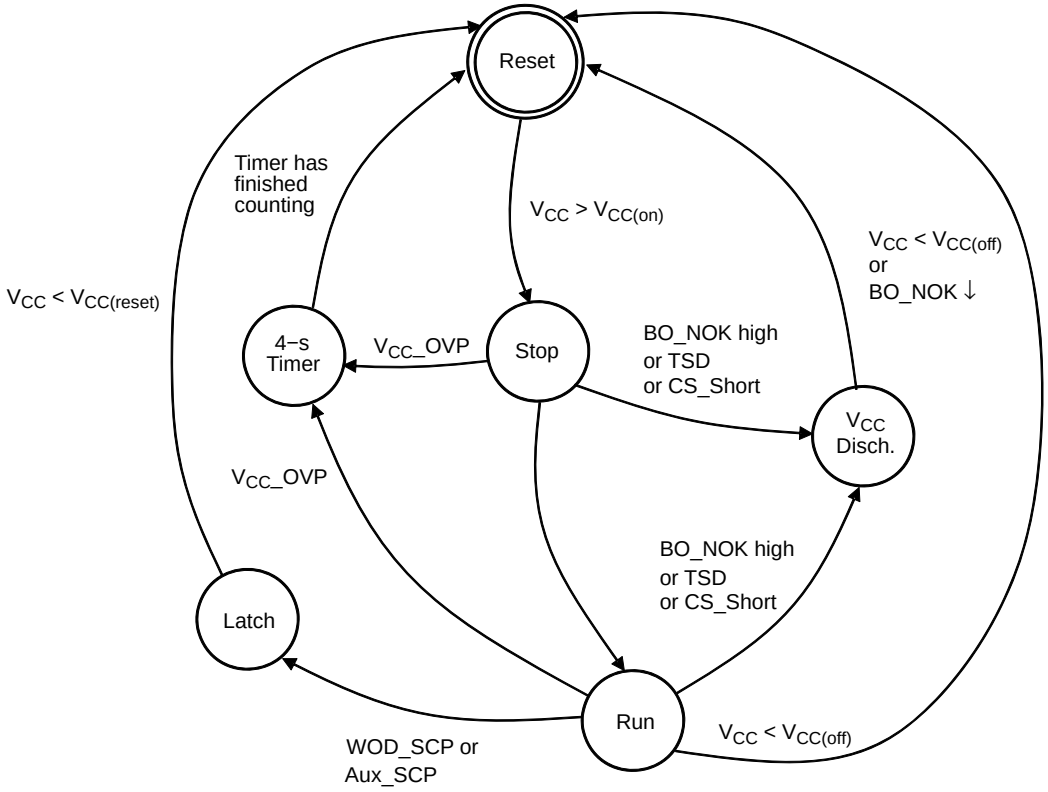
In this mode, the DRV pulses are stopped and the controller is latched. There are hiccups on V_{CC}.

The circuit un−latches when $V_{CC} < V_{CC(reset)}$.



With states: Reset → Controller is reset, $I_{CC} = I_{CC(start)}$
Stop → Controller is ON, DRV is not switching
Run → Normal switching
V_{CC} Disch. → No switching, $I_{CC} = I_{CC1}$, waiting for V_{CC} to decrease to $V_{CC(off)}$
4−s Timer → the auto−recovery timer is counting, V_{CC} is ramping up and down between $V_{CC(on)}$ and $V_{CC(off)}$

Figure 55. State Diagram for B Version Faults



With states:	Reset	→	Controller is reset, $I_{CC} = I_{CC(start)}$
	Stop	→	Controller is ON, DRV is not switching
	Run	→	Normal switching
	V_{CC} Disch.	→	No switching, $I_{CC} = I_{CC1}$, waiting for V_{CC} to decrease to $V_{CC(off)}$
	4−s Timer	→	the auto−recovery timer is counting, V_{CC} is ramping up and down between $V_{CC(on)}$ and $V_{CC(off)}$
	Latch	→	Controller is latched off, V_{CC} is ramping up and down between $V_{CC(on)}$ and $V_{CC(off)}$, only $V_{CC(reset)}$ can release the latch.

Figure 56. State Diagram for A Version Faults

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

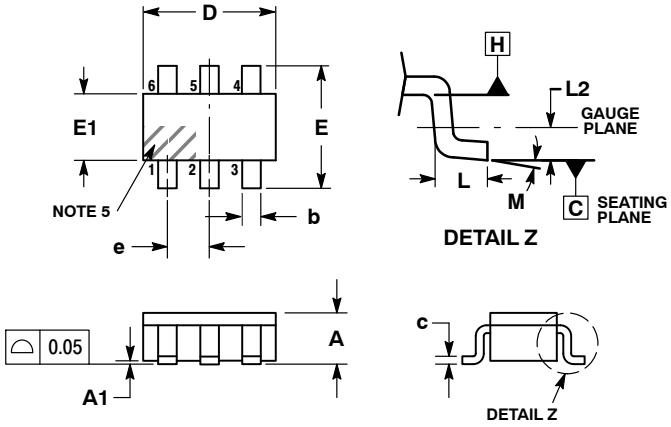
ON Semiconductor®



SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

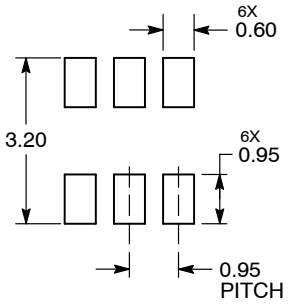
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

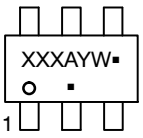
RECOMMENDED SOLDERING FOOTPRINT*



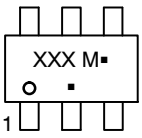
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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