NCL30095A

Power Factor Corrected LED Boost Switching Regulator

The NCL30095A high power factor boost PWM switching regulator is designed to regulate the average current through a string of LEDs. The circuit operates in Critical Conduction Mode (CrM) based on a proven constant on−time control scheme to achieve near unity power factor. In addition to regulating a constant current, the switching regulator is optimized to support leading and trailing edge phase dimming applications. When a dimmer is detected on the AC input, an internal voltage reference of the current regulation loop adjusts the current level based on the dimmer conduction angle so the current through the LED string has a desired value based on a programmed dimming curve. The shape of the dimming curve is intended to emulate the response of an incandescent bulb while achieving NEMA SSL6 and NEMA SSL7A recommendations.

An integrated HV MOSFET in a cascoded configuration supports biasing the controller during operation and eliminates the need for an auxiliary winding to provide bias power. A robust suite of protection features is included to ensure proper handling of expected fault conditions without the need for extra circuitry and a dedicated thermal fold−back input proves gradually reduction of the current above a user defined set−point.

General Features

- Near−Unity Power Factor
- Critical Conduction Mode (CrM)
- Constant On−time Control
- Accurate Current Regulation (+/− 2% typical)
- Compatible with Leading and Trailing Edge Phase Controlled Dimmers
- Fast Startup Time (< 100 ms typical)
- Integrated ZCD Detection
- User Programmable Thermal Current Fold−back
- Vcc Operation up to 18 V

Safety Features

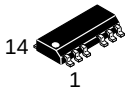
- Output Overvoltage Protection
- Cycle−by−Cycle Current Limiting
- Vcc UVLO

Typical Applications

- LED Bulbs
- LED Downlights
- LED Light Engines
- LED Modules

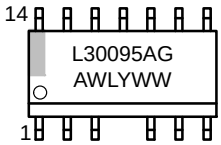
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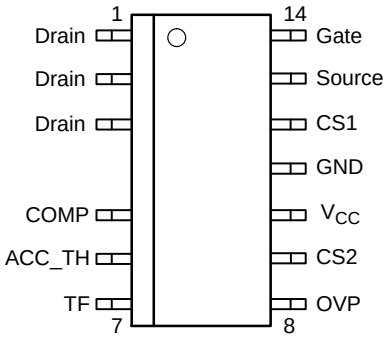
SOIC−14 NB (LESS PIN 4)
CASE 751DY

MARKING DIAGRAM



L30095A = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCL30095ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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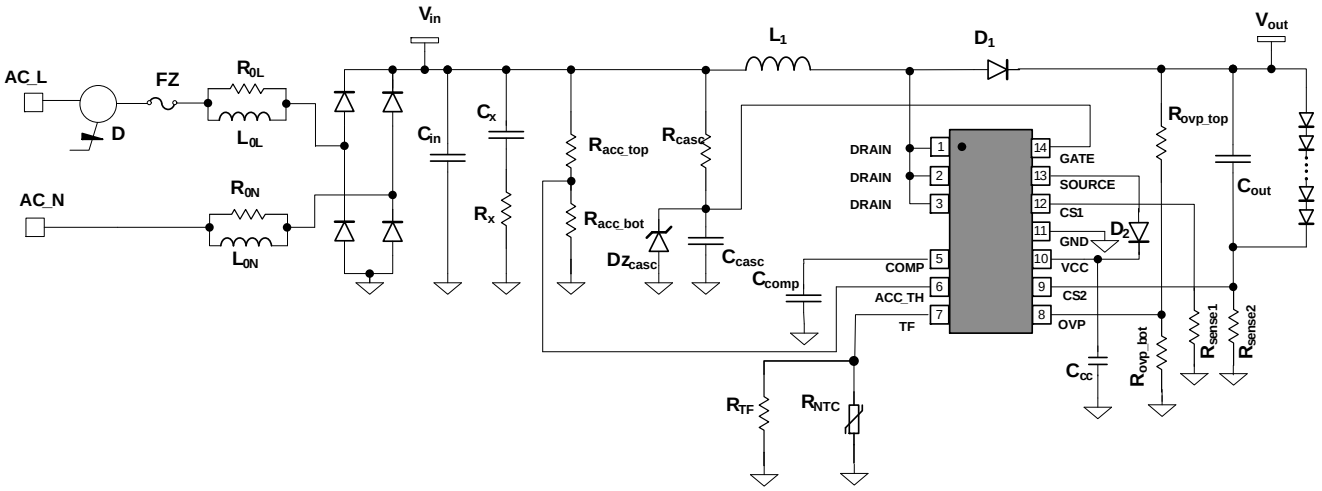


Figure 1. NCL30095A Application Schematic

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1, 2, 3	DRAIN	Drain of HV switch	The Drain of the High Voltage NMOS.
5	COMP	Compensation	Feedback loop compensation pin of the IC.
6	ACC_TH	Diming Detection Input	This pin receives a portion of the AC input voltage. It is compared to an internal reference voltage in order to determine the presence of a dimmer state and the phase angle.
7	TF	Thermal Fold−back	Connecting an NTC to this pin allows linear reduction of the output current above a user programmed temperature set−point.
8	OVP	Over−Voltage Protection Input	This pin receives a portion of the Boost output voltage V_{OUT} and serves to trigger an OVP fault in the event the LED string is open.
9	CS2	2nd Current Sense Input	This pin monitors the LED load current across the R_{sense2} resistor during the off time. This pin is used to monitor the instantaneous load current for regulation loop, and to determine when the Zero Current Detection (ZCD) point is reached.
10	VCC	V_{CC} Input	This positive supply pin accepts up to 18 Vdc. The supply for the device is ensured by the external diode from the source pin.
11	GND	−	The switching regulator ground
12	CS1	1st Current Sense Input	This pin monitors the inductor current across the R_{sense1} resistor during the on−time. This pin monitors the maximum current cycle by cycle.
13	SOURCE	Source of HV Switch	The Source of the High Voltage NMOS. Connect the external diode between the source and VCC pin to provide the IC supply.
14	GATE	Gate of HV Switch	The Gate of the High Voltage NMOS. External circuitry is used to bias this pin to 20V.

Simplified Internal Block Schematic

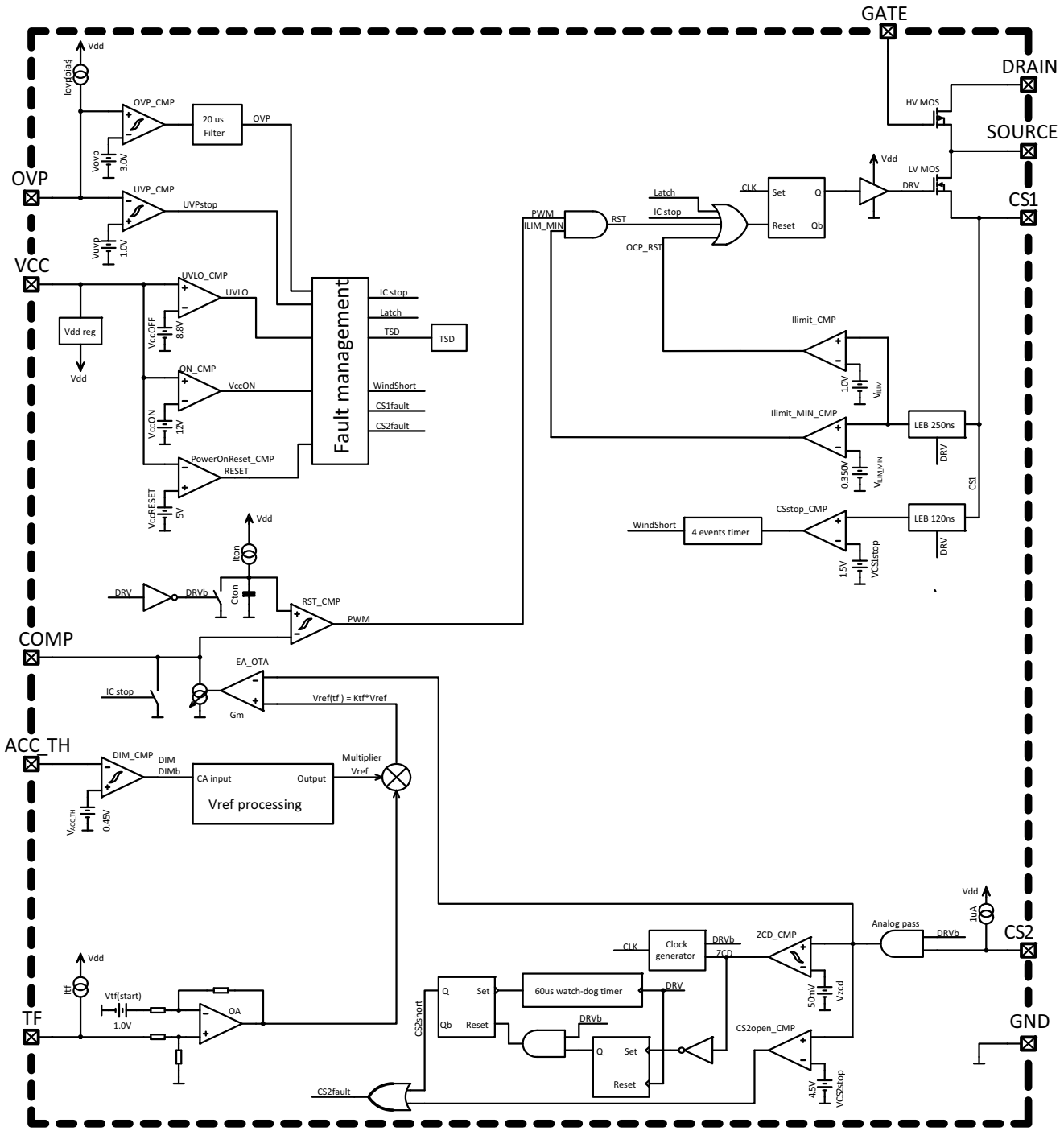


Figure 2. Simplified Internal Block Schematic

Table 2. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
$V_{DRAIN(MAX)}$	1, 2, 3	HV NMOS Drain to Source Voltage (V_{DSS}) Continuous Drain Current $R_{\theta J-C}$ steady state, T_C = 25°C (Note 1) Continuous Drain Current $R_{\theta J-C}$ Steady State, T_C = 100°C (Note 1) Peak Drain Current	+380 0.5 0.25 −0.01 / 1.7	V A A A
$V_{CC(MAX)}$	10	Maximum Power Supply voltage, VCC pin, continuous voltage Maximum Current for VCC pin	– 0.3 to 18 ±30 (peak)	V mA
$V_{CS1(MAX)}$	12	Maximum Voltage Continuous Current	– 0.3 to 5.5 −1.7/0.01	V A
$V_{SOURCE(MAX)}$	13	HV NMOS Source Voltage Maximum current is equal to DRAIN pin	−20 to 18 −1.7/1.7	V A
$V_{GATE(MAX)}$	14	HV NMOS Gate Voltage Maximum current to gate pin	−20 to 18 ±1000 (peak)	V mA
V_{MAX}		Maximum voltage on low power pins (except pins 1,2,3,10,12,13,14) Maximum current to low power pins	– 0.3 to 9 ±10 (peak)	V mA
P_D		Maximum Power Dissipation @ T_C = TBD°C	TBD	mW
$R_{\theta JA}$		Thermal Resistance SOIC−14 Junction−to−Air, low conductivity PCB Junction−to−Air, high conductivity PCB	 108 70	°C/W
T_{JMAX}		Operating Junction Temperature	−40 to +125	°C
$T_{STRGMAX}$		Storage Temperature Range	−60 to +150	°C
T_{LMAX}		Lead Temperature (Soldering, 10s)	300	°C
MSL		Moisture Sensitivity Level	1	–
		ESD Capability, HBM model (All pins except GATE) (Note 2)	3.5	kV
	14	ESD Capability, HBM model (pin GATE) (Note 2)	200	V
		ESD Capability, Machine Model (All pins except GATE) (Note 2)	250	V
	14	ESD Capability, Machine Model (pin GATE) (Note 2)	100	V
		ESD Capability, CDM model (Note 2)	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by the junction temperature.
2. This device contains ESD protection and exceeds the following tests:
   Human Body Model per JEDEC Standard JESD22−A114E
   Machine Model Method per JEDEC Standard JESD22−A115B
   Charged Device Model per JEDEC Standard JESD22−C101E.
3. This device contains latch−up protection and has been tested per JEDEC Standard JESD78D, Class I and exceeds ±100 mA

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 13 V, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
SUPPLY						
Turn−on Threshold Level	V_{CC} going up	$V_{CC(on)}$	11.0	12.0	13.0	V
Minimum Operating Voltage, Turn−off Threshold	V_{CC} going down	$V_{CC(off)}$	8.2	8.8	9.4	V
Hysteresis $V_{CC(on)} - V_{CC(off)}$		$V_{CC(hyst)}$	2.8	−	−	V
V_{CC} decreasing level at which the internal logic resets		$V_{CC(reset)}$	4.0	5.0	6.0	V
Blanking Duration on $V_{CC(off)}$		$t_{VCC(off)}$	−	10	−	μs
Blanking Duration on $V_{CC(reset)}$		$t_{VCC(reset)}$	−	10	−	μs
Internal Current Consumption of Device before Start−up	V_{CC} = 10V	I_{CC1}	−	10	100	μA
Internal Current Consumption, when DRAIN Pin is Switching	f_{sw} = 65 kHz, V_{COMP} = 2.5 V, V_{CS1} = 0.5 V	I_{CC2}	−	1.0	1.5	mA
Internal Current Consumption, when DRAIN Pin is Turned−on	V_{COMP} = 2.5 V, V_{CS1} = 0 V	I_{CC3}	−	0.9	1.1	mA
OUTPUT OVERVOLTAGE PROTECTION						
Over Voltage Protection Thresholds	V_{OVP} going up V_{OVP} going down	$V_{OVP(off)}$ $V_{OVP(on)}$	2.9 2.6	3.0 2.7	3.1 2.8	V
Over Voltage Protection Hysteresis		$V_{OVP(hyst)}$	−	300	−	mV
Timer Duration for Over Voltage Detection		t_{OVP}	23	33	43	μs
Internal OVP Pin Pull−up Current		$I_{OVP(bias)}$	50	250	450	nA
Under Voltage Detect Threshold		V_{UVP}	0.4	0.5	0.6	V
Under Voltage Detect Propagation Delay		t_{UVP}	23	33	43	μs
LED CURRENT REGULATION LOOP						
Error Amplifier Trans−Conductance		G_{EA}	85	100	115	μS
Error Amplifier Current Capability		I_{EA}	±13	±25	−	μA
Error Amplifier Input Offset	T_j = 25°C	V_{EAIO}	−20	−	20	mV
Maximum Control Voltage		$V_{COMP(max)}$	4.2	−	−	V
Minimum Control Voltage		$V_{COMP(min)}$	−	−	0.7	V
COMP Pin Discharge Resistance		$R_{COMP(dis)}$	−	200	−	Ω
CURRENT SENSE 1 − INDUCTOR OVERCURRENT LIMITATION						
Maximum Internal Current Set−Point	V_{COMP} > 4 V	V_{ILIM}	0.95	1.00	1.05	V
Propagation Delay from V_{ilimit} Detection To Switch Off	V_{CS1} > 1.2 V	t_{delay}	−	50	90	ns
Minimum Internal Current Set−Point (Dimming Is Detected)	V_{COMP} < 0.7 V	V_{ILIM_MIN}	300	350	400	mV
Propagation Delay from Reduced V_{ilimit} Detection to DRV Off	V_{CS1} > 1.2 V	t_{delay_DIM}	−	50	90	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	220	320	420	ns
Threshold for Winding Short Fault Protection Activation		$V_{CS1(stop)}$	1.42	1.50	1.58	V
Leading Edge Blanking Duration for $V_{CS(Stop)}$ (Note 4)		t_{BCS}	90	120	150	ns
CURRENT SENSE 2 − ZERO CURRENT DETECTION AND LED REGULATION INPUT						
Input Pull−Up Current	V_{CS2} = 0.7 V	$I_{CS2(bias)}$	−	1	−	μA

Table 3. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{CC} = 13 V, unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE 2 − ZERO CURRENT DETECTION AND LED REGULATION INPUT						
Internal Reference for Nominal LED Current		V_{REF}	233	250	267	mV
Lower ZCD Threshold	V_{CS2} falling	$V_{ZCD(falling)}$	15	50	80	mV
Upper ZCD Threshold	V_{CS2} rising	$V_{ZCD(rising)}$	30	65	95	mV
ZCD Comparator Hysteresis		$V_{ZCD(hyst)}$	−	15	−	mV
Propagation Delay from ZCD To Turn−On Internal Switch	V_{CS2} falling	t_{DEM}	400	500	600	ns
Current Sense Threshold for CS2 Pin Open Protection		$V_{CS2(stop)}$	4.0	4.5	5.0	V
Blanking Duration for ZCD Detection		$t_{ZCD(blank)}$	200	300	400	ns
ZCD Timeout		$t_{ZCD(timeout)}$	20	32	45	μs
DIMMING DETECTION						
Dimming Detection Comparator Thresholds	V_{ACCTH} going up V_{ACCTH} going down	V_{ACCTH_H} V_{ACCTH_L}	0.400 0.300	0.450 0.350	0.500 0.400	V
Dimming Detection Comparator Hysteresis		V_{ACCTH_Hyst}	−	100	−	mV
Dimming Detection Comparator Delay	V_{ACCTH} = V_{ACCTH_H} + 0.1 V	t_{DIM_D}	40	70	90	μs
ON−TIME GENERATOR						
Maximum On Time	V_{COMP} = 4.2 V	t_{ONmax}	15	18	22	μs
On Time	V_{COMP} = 2.5 V	t_{ON}	8.0	9.5	11.0	μs
Minimum On Time	V_{COMP} = 0.7 V	t_{ONmin}	−	0.6	1.2	μs
Thermal Foldback						
TF Pin Voltage at which Thermal Fold−Back Starts (V_{REF} is Decreased)		$V_{TF(start)}$	0.94	1.00	1.06	V
TF Pin Voltage at which Thermal Fold−Back Reduces V_{REF} to 10% V_{REF}		$V_{TF(10\%)}$	0.45	0.5	0.55	V
Current Source for Direct NTC Connection	V_{TF} = 0 V	I_{TF}	80	85	90	μA
Blanking Duration for TF Detection after Start−Up	V_{TF} = 0 V	$t_{TF(blank)}$	250	300	350	μs
INTERNAL TEMPERATURE SHUTDOWN						
Temperature Shutdown (Note 4)	T_J going up	T_{TSD}	135	150	165	°C
Temperature Shutdown Hysteresis (Note 4)	T_J going down	$T_{TSD(HYS)}$	−	30	−	°C
INTERNAL CASCODED SWITCH						
On State Resistance of the Low Voltage NMOS	I_{LDS} = 500 mA, Tj = 25°C	$R_{L,DS,on}$	−	3.5	4.5	Ω
On State Resistance of the High Voltage NMOS	I_{HDS} = 500 mA, V_{GATE} = 15 V V_{SOURCE} = 0 V, Tj = 25°C	$R_{H,DS,on}$	−	3.5	5.0	Ω
Maximum Drain to Source Voltage of the Low Voltage NMOS (Note 4)		$V_{L,DS,max}$	30	−	−	V
Maximum Drain to Source Voltage of the High Voltage NMOS		$V_{H,DS,max}$	380			V
Maximum Off State Leakage Current	V_{DRAIN} = 400 V	I_{DSS}	−	−	5.0	μA
Turn−On Time, 90 to 10 % of V_{DRAIN}	R_{LOAD} = 100 Ω, I_D = 500 mA	t_{on}	−	10	−	ns
Turn−Off Time, 10 to 90 % of V_{DRAIN}	R_{LOAD} = 100 Ω, I_D = 500 mA	t_{off}	−	30	−	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Guaranteed by Design

TYPICAL CHARACTERISTICS

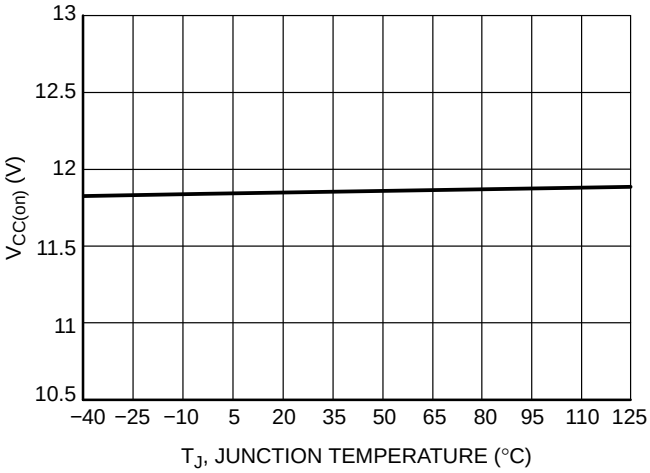


Figure 3. Turn−On Threshold Level, $V_{CC(on)}$

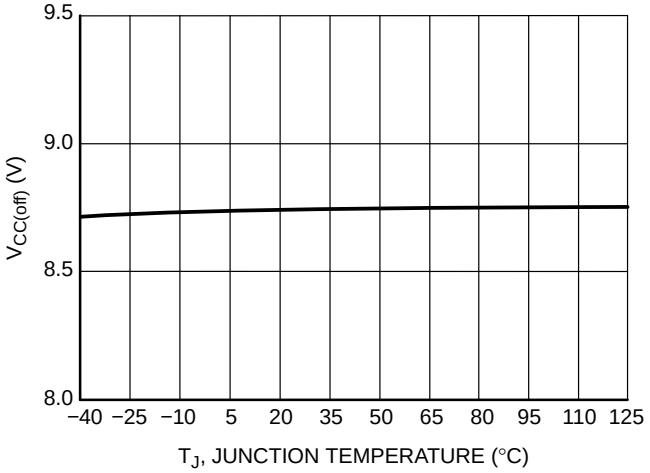


Figure 4. Minimum Operating Voltage, $V_{CC(off)}$

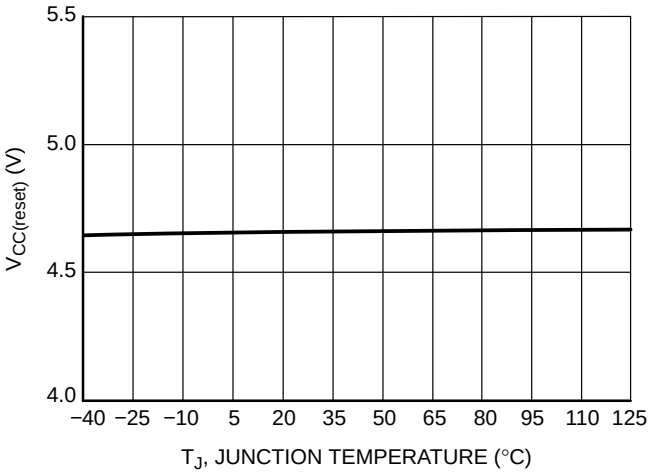


Figure 5. V_{CC} Decreasing Level at which the Internal Logic Resets, $V_{CC(reset)}$

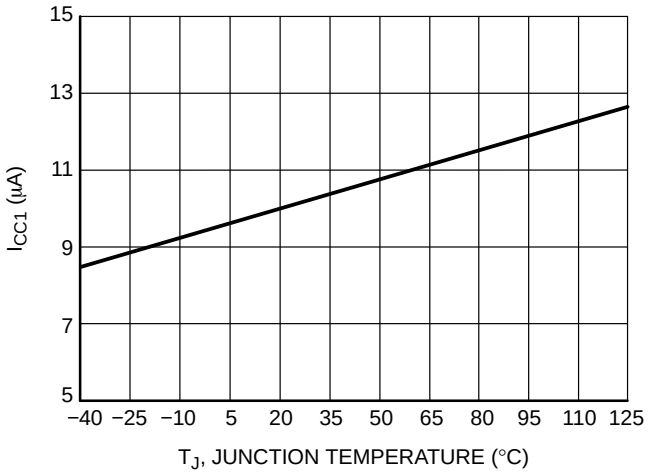


Figure 6. Internal Current Consumption before Start−Up, I_{CC1}

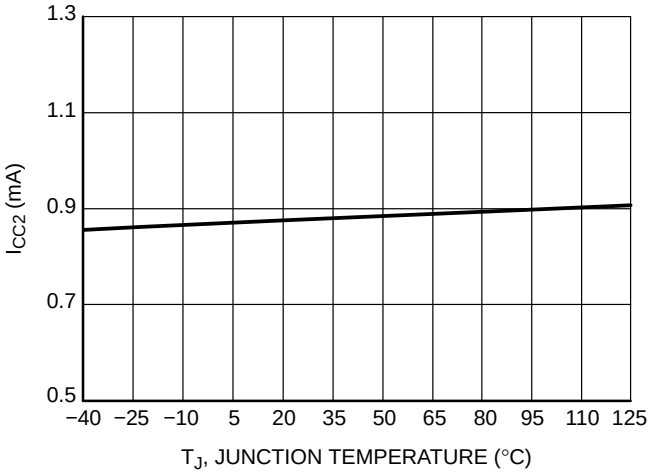


Figure 7. Internal Current Consumption when DRV Pin is Switching, I_{CC2}

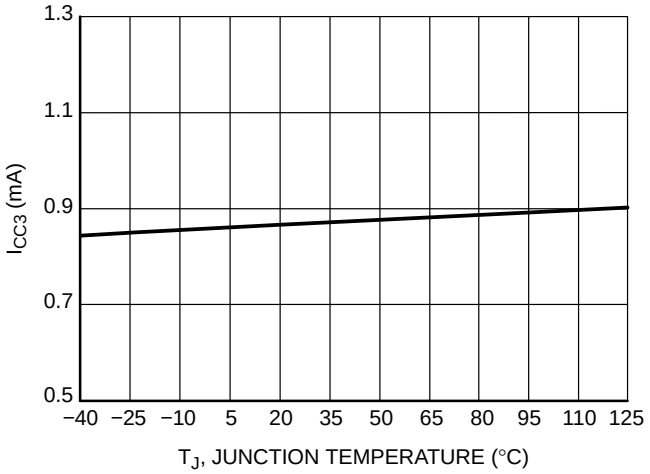


Figure 8. Internal Current Consumption when DRV Pin is Turned−On, I_{CC3}

TYPICAL CHARACTERISTICS

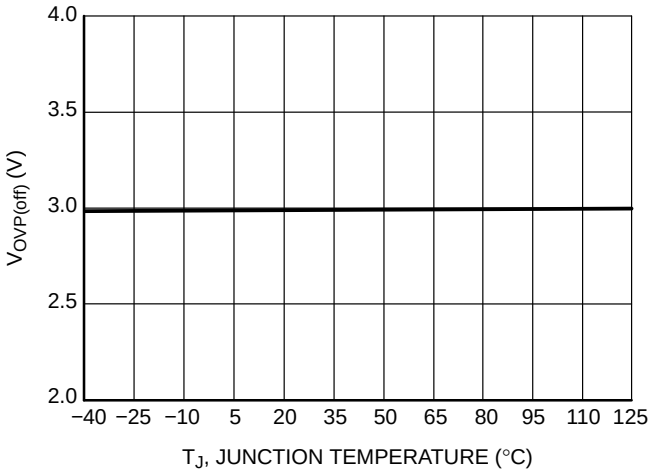


Figure 9. Overvoltage Protection Threshold (V_{OVP} going up), $V_{OVP(off)}$

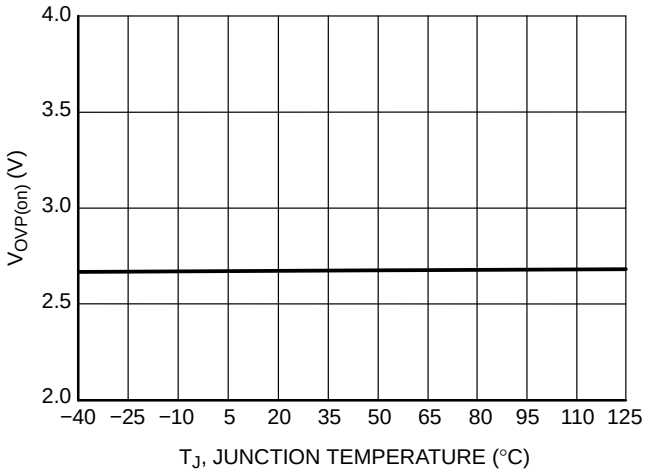


Figure 10. Overvoltage Protection Threshold (V_{OVP} going down), $V_{OVP(on)}$

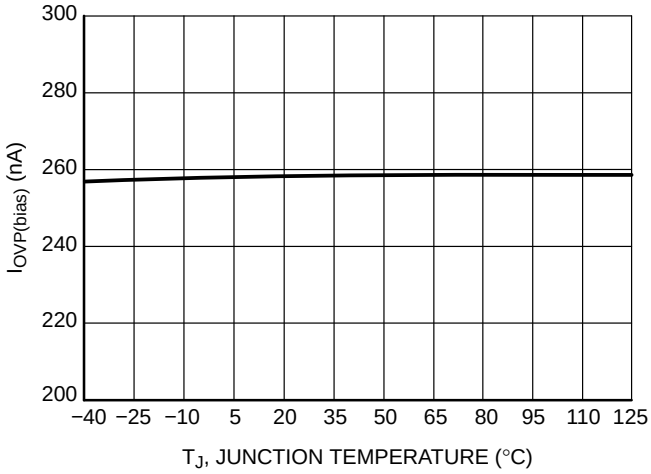


Figure 11. Internal OVP Pin Pull−Up Current, $I_{OVP(bias)}$

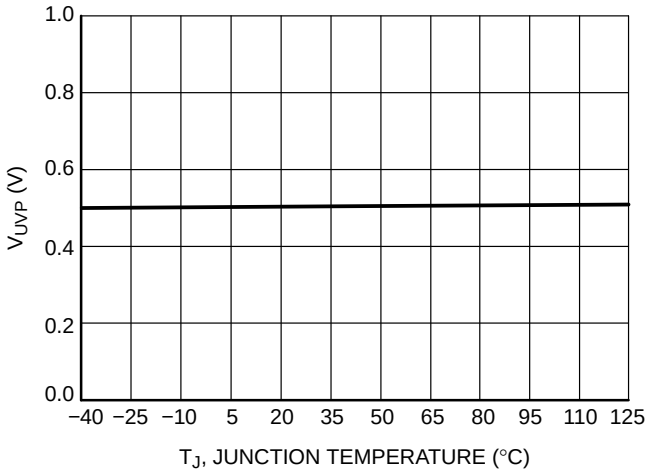


Figure 12. Undervoltage Detect Threshold, V_{UVP}

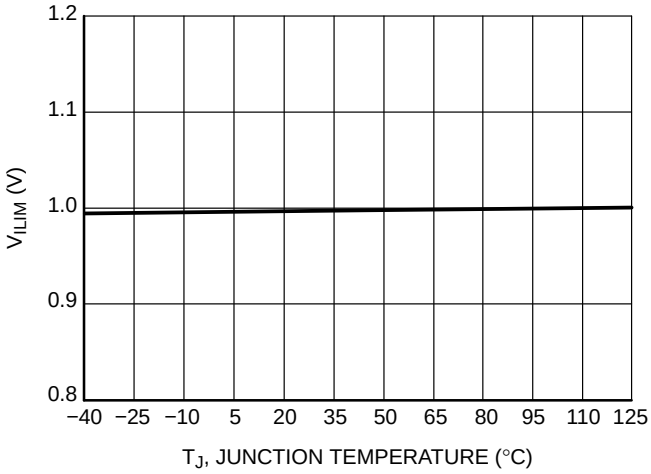


Figure 13. Maximum Internal Current Set−Point, V_{ILIM}

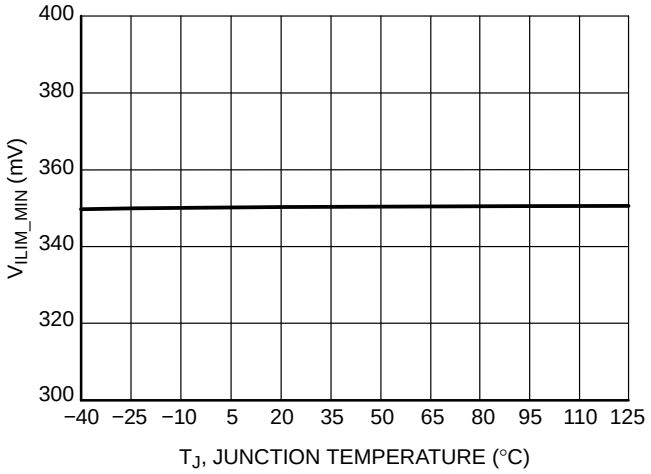


Figure 14. Minimum Internal Current Set−Point, V_{ILIM_MIN}

TYPICAL CHARACTERISTICS

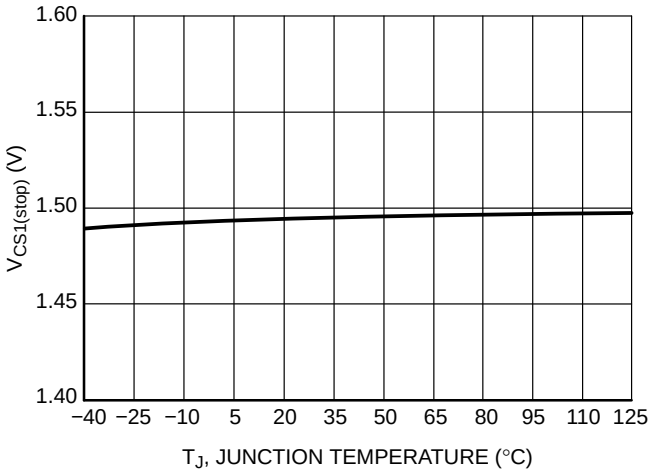


Figure 15. Threshold for Winding Short Fault Protection Activation, $V_{CS1(stop)}$

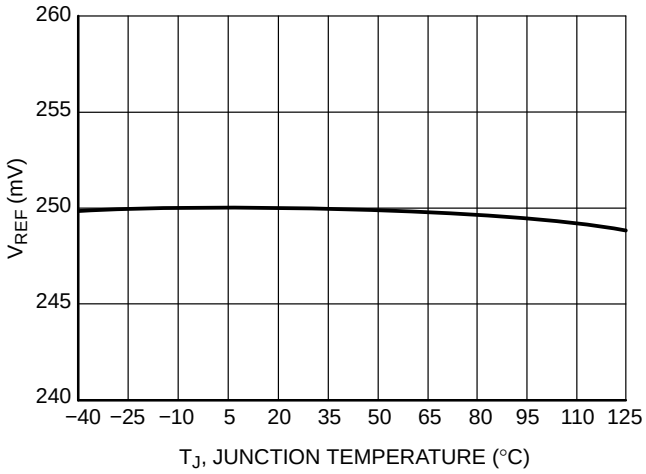


Figure 16. Internal Reference for Nominal LED Current, V_{REF}

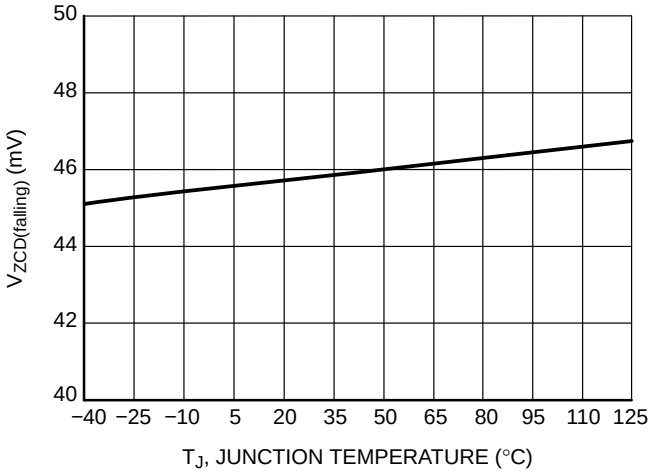


Figure 17. Lower ZCD Threshold, $V_{ZCD(falling)}$

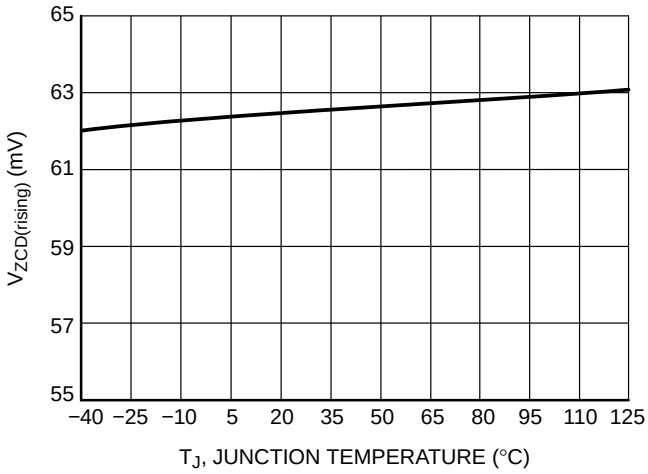


Figure 18. Upper ZCD Threshold, $V_{ZCD(rising)}$

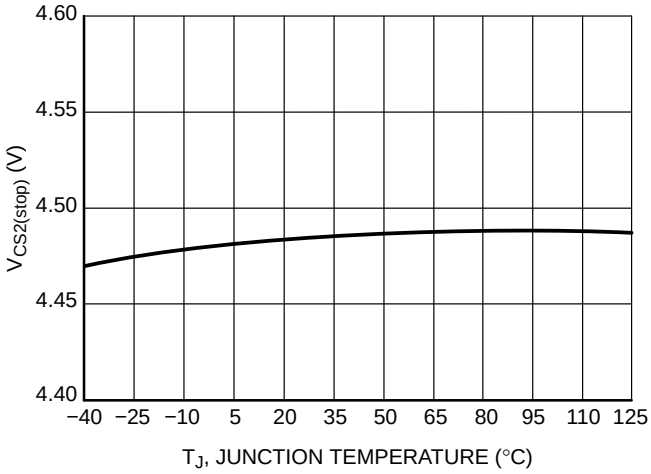


Figure 19. Current Sense Threshold for CS2 Pin Open Protection, $V_{CS2(stop)}$

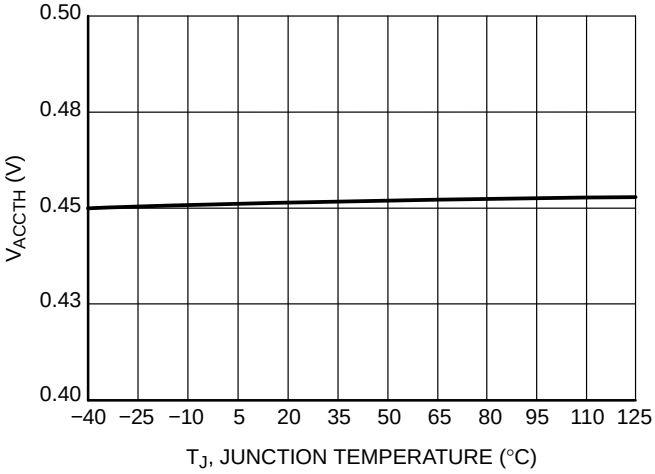


Figure 20. Dimming Detection Comparator Threshold, V_{ACCTH} Going Up, V_{ACCTH_H}

TYPICAL CHARACTERISTICS

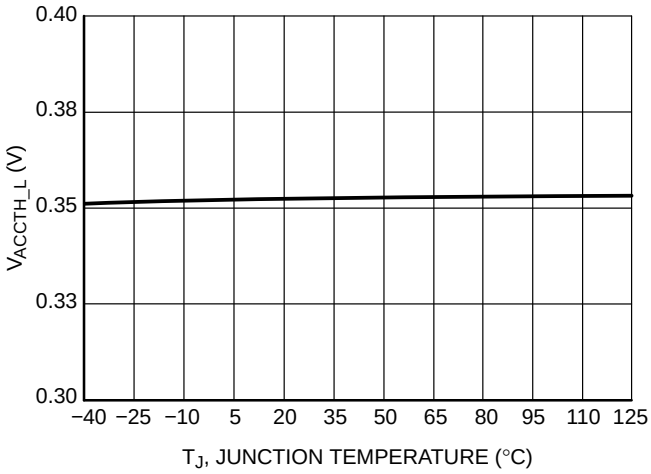


Figure 21. Dimming Detection Comparator Threshold, V_{ACCTH} Going Down, V_{ACCTH_L}

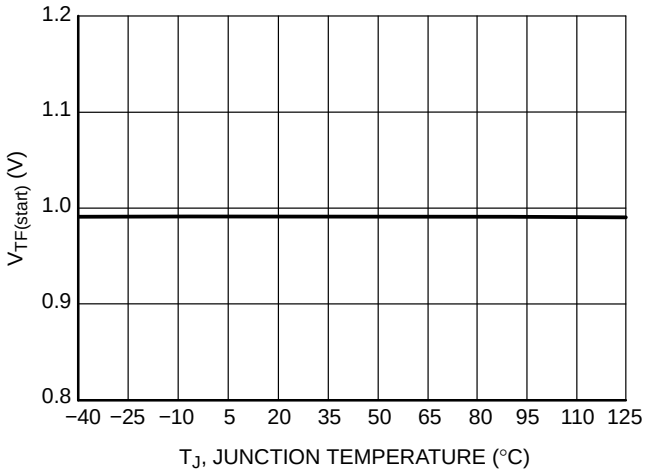


Figure 22. TF Pin Voltage at Which Thermal Fold−Back Starts, $V_{TF(start)}$

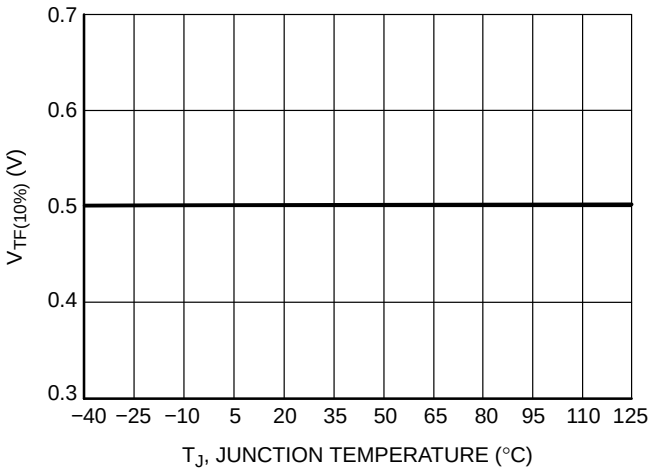


Figure 23. TF Pin Voltage at Which Thermal Fold−Back Reduces to 10%, $V_{TF(10\%)}$

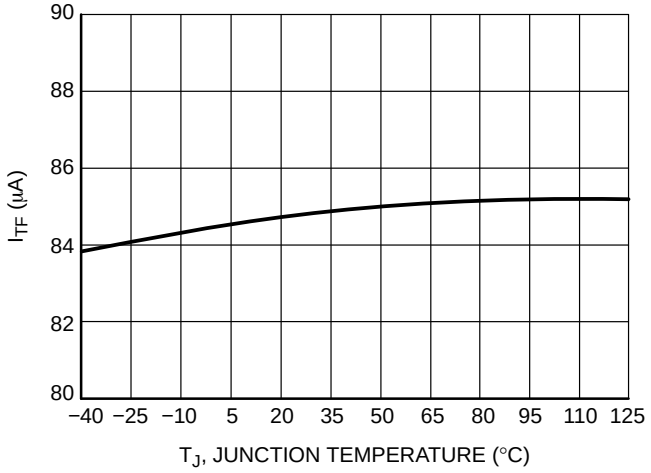


Figure 24. Current Source for Direct NTC Connection, I_{TF}

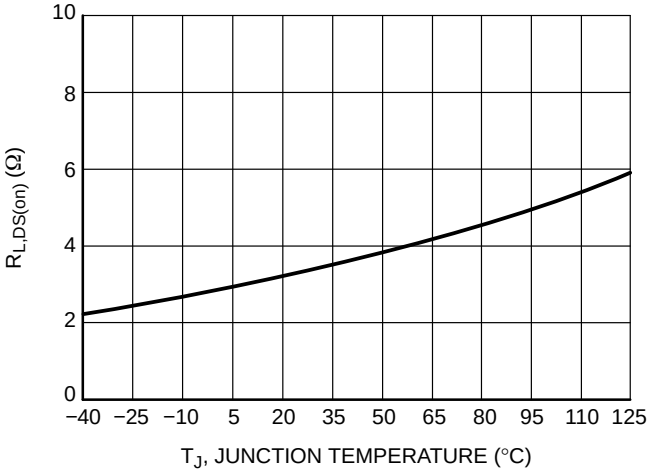


Figure 25. On−State Resistance of the Driving NMOS, $R_{L,DS(on)}$

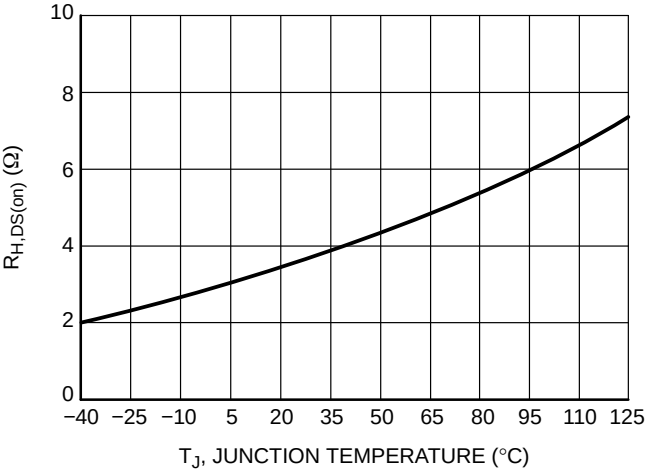


Figure 26. On−State Resistance of the Driving NMOS, $R_{H,DS(on)}$

TYPICAL CHARACTERISTICS

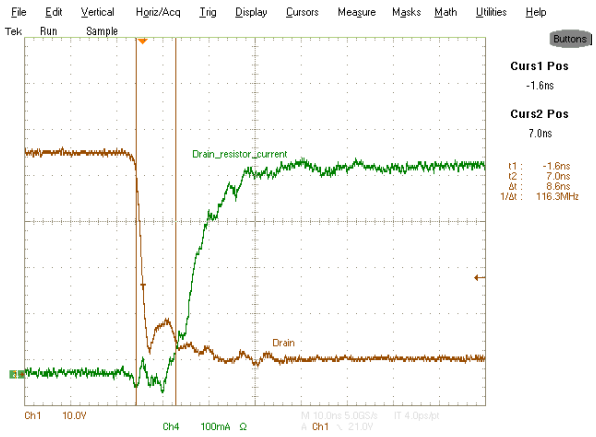


Figure 27. Typical On−Time Measured with 500 mA of Drain Current and Resistive Load

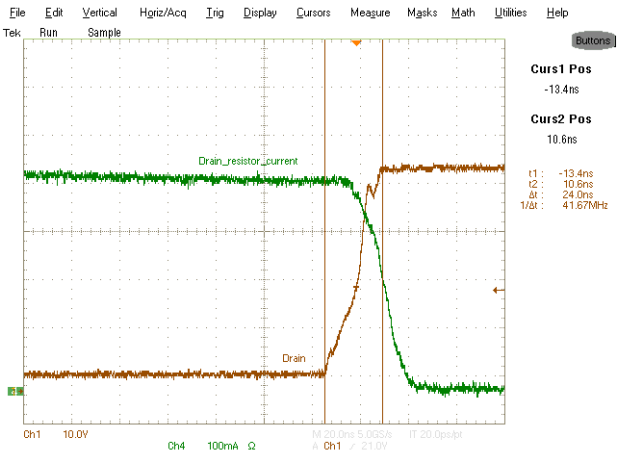


Figure 28. Typical Off−Time Measured with 500 mA of Drain Current and Resistive Load

APPLICATION IINFORMATION

Functional description

NCL30095A uses a Constant On−time Boost architecture in order to target a unity power factor, when no dimming is detected. The cascoded drain architecture shown in Figure 29, where Q1 is the High Voltage Cascode NMOS, allows a simple implementation of a V_{CC} supply by including a diode D_{VCC}, external to the switcher IC, between the SOURCE pin and capacitor C_{VCC}. Thanks to the cascoded DRAIN architecture, the startup time is very fast (typ < 100 ms). Unlike a traditional asynchronous boost architecture, where a power transistor is needed, the cascode architecture uses two MOSFETs, a low voltage MOSFET Q2 , internal to the IC Switching regulator, and a High−Voltage NMOS FET Q1, which is housed in a SOIC−14 package.

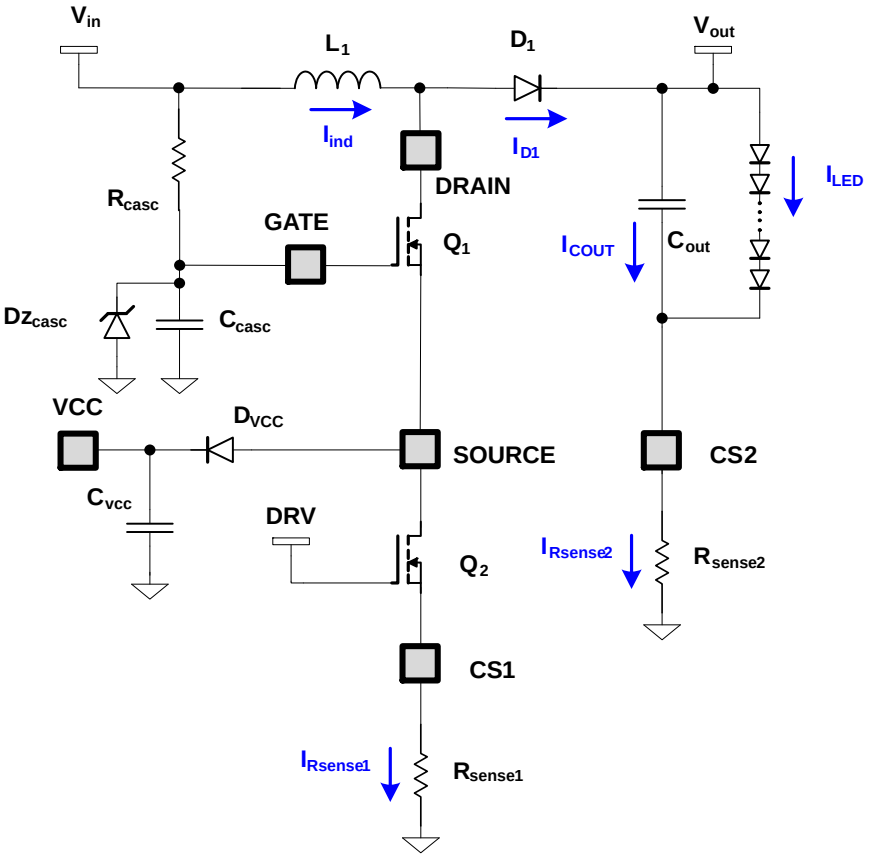


Figure 29. Cascode Architecture

The NCL30095A operates in Critical Conduction Mode (CrM) under all working conditions, regulating the average current flowing through the string of LEDs whether the dimmer is present or not.

The ACC_TH pin senses a scaled down input voltage (Vin) and by comparing it to an internal reference voltage named V_{ACC_TH} it provides a digital signal DIM/DIMb that contains the amount of dimming information. DIM/DIMb is processed then by a circuit block named “Vref processing”, which provides analog signal Vref. The reference voltage named Vref serves for the LED current regulation loop. The LED current regulation loop is working for all conduction angles, it is then possible by programming the Vref processing circuit block to get the desired dimming curve as depicted in Figure 31.

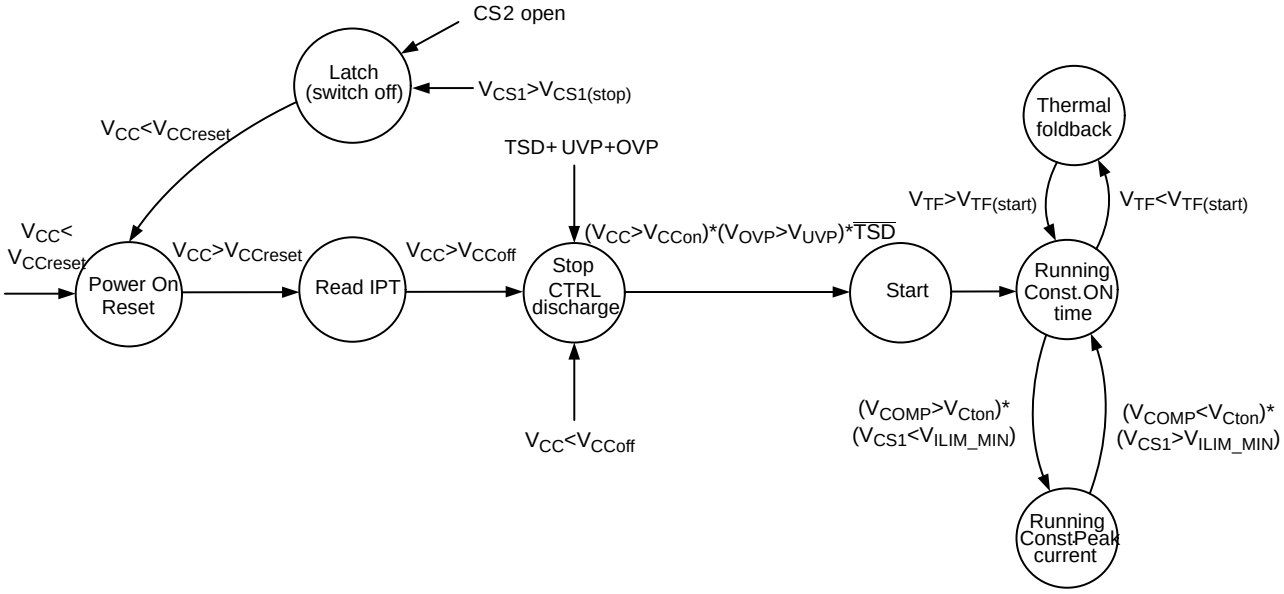


Figure 30. Operating status diagram of the device

Critical conduction mode

By looking at Figure 29 it can be seen that the current $I_{Rsense1}$ flowing through the external resistor R_{sense1}, connected between pin CS1 and GND, is the same as the inductor current I_{ind} plus current spikes associated with the turning on or turning off of Q2 NMOS FET. The inductor current information carried by the pin CS1 is used for the inductor peak current limitation. This voltage V_{CS1} is used to generate a reset signal (OCP_RST) resulting from having reached the inductor maximum peak current controlled by V_{ILIM} reference voltage. If the maximum peak inductor current is not reached it is the second branch that takes care of the reset signal (RST) indicating the end of the on−time. The second branch monitors the off−time current information at current sense input CS2. The second branch is inhibited during the MOSFET on−time.

As shown in Figure 2, the second branch voltage is an image of the off−time inductor current. It is sent to the input of an OTA and by comparing to a reference voltage (V_{REF}) a control voltage is generated at the COMP pin. The COMP pin voltage is proportional to the average LED current. It is compared to a constant on−time ramp voltage generated by charging the capacitor C_{TON} by a constant current I_{TON}. The output of the comparator generates constant on−time reset signal (RST). This process represents the “constant t_{on} average LED regulation loop” which, when steady state is reached, ensures that:

$$I_{LEDavg} = \frac{V_{REF}}{R_{sense2}} \quad \text{(eq. 1)}$$

There is one more condition to end the on−time cycle. The power MOSFET is turned−off only under a condition that the inductor peak current reaches a level set by the reference voltage named V_{ILIM_MIN}. Minimum input current is maintained by switching in Constant Peak Current mode. When a dimmer is present this feature helps to avoid the leakage current of the dimmer from charging the C_{in} capacitor. At the same time this feature sets a minimum input current to avoid the current loop cut off when the triac dimming is applied

The reset signal (RST or OCP_RST) indicates an end of the on−time and a start of the off−time. Once the off−time has started, the CS2 pin senses the inductor off−time current across R_{sense2}, which is compared to a reference voltage V_{ZCD} in order to generate a zero−crossing signal (ZCD) that in turn is processed by the clock generation block. The generated clock pulse triggers a start of the new on−time cycle.

LED Current Regulation and Dimming Curve

As long as the max peak current limitation is not exceeded or a thermal foldback condition is present, the average LED current regulation loop is controlled by the OTA via equation 1 and Triac Dimming Curve of Figure 31.

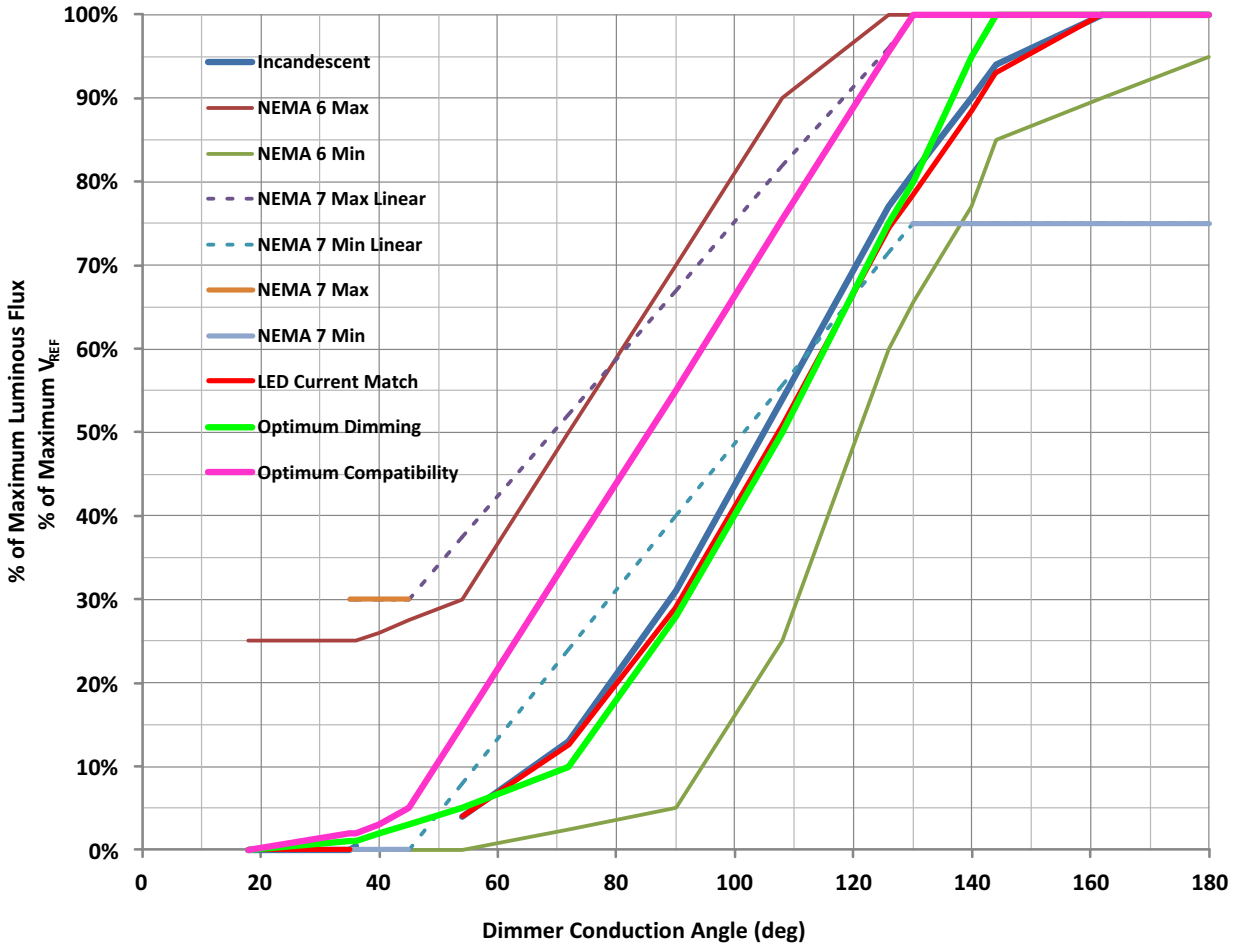


Figure 31. Triac Dimming Curve Digitally Generated

For example if R_{sense2} = 20 Ω and V_{REF} = 0.5 V this gives I_{LED} = 25 mA. The circuit block named V_{REF} processing which can be seen in Figure 2 will be programmed for the optimum compatibility acceleration curve by default (see Figure 31) with an option of the optimum diming acceleration curve.

Table 4. Coordinates of dimming curve programming points

Dimmer conduction angle (deg)	Optimum Dimming $V_{REF}/V_{REF,max}$	Optimum Compatibility $V_{REF}/V_{REF,max}$
18	0.0%	0.0%
35	1.0%	2.0%
36	1.0%	2.0%
40	2.0%	3.0%
45	3.0%	5.0%
54	5.0%	15.0%
72	10.0%	35.0%
90	28.0%	55.0%
108	50.0%	75.5%
126	75.0%	95.5%
130	80.0%	100.0%
140	95.0%	100.0%
144	100.0%	100.0%
162	100.0%	100.0%
180	100.0%	100.0%

To regulate an average LED current in a single stage architecture the instantaneous LED current can have as much as +/−50% ripple component (this ripple component depends on the value of C_{out} capacitor and LED string dynamic resistance). The OTA must work linearly while a voltage with ripple is applied. The transconductance (G_m) value is set as low as 100 μs and the minimal output current capability is at +/−25 μA to ensure the OTA linear operation, without entering the saturation level

Dimming presence sensing

The conduction angle of the dimmer is sensed through pin ACC_TH. The rectified and dimmed V_{in} voltage (see Figure 1) appears on pin ACC_TH divided by the resistor bridge composed of R_{acc_top} and R_{acc_bot}. The ACC_TH voltage is equal to:

$$V_{ACC_TH} = K_{acc} \cdot V_{in} \quad \text{(eq. 2)}$$

With:

$$K_{acc} = \frac{R_{acc_bot}}{R_{acc_bot} + R_{acc_top}} \quad \text{(eq. 3)}$$

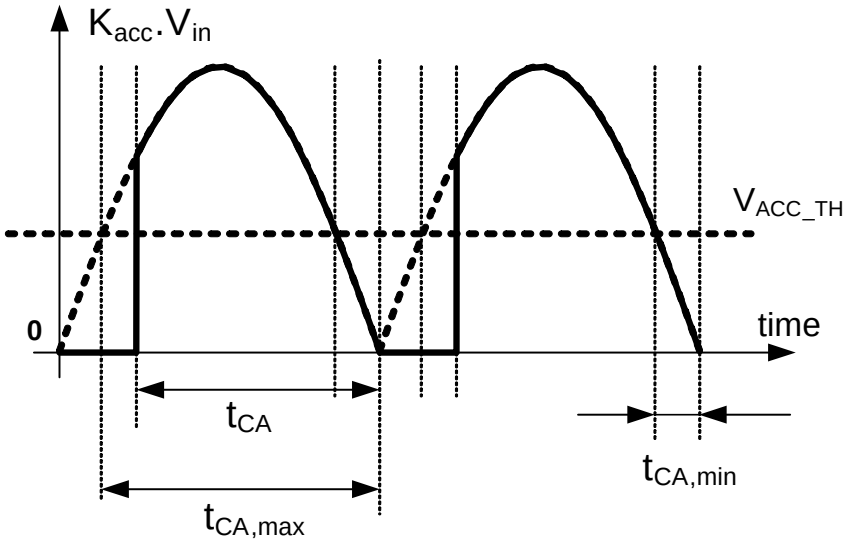


Figure 32. ACC_TH pin waveforms and max/min detectable dimmer conduction angles

Voltage sensed at the ACC_TH pin is compared to the V_{ACC_TH} reference voltage (see Figure 32) in order to generate a digital signal (DIM/DIMbar) (see Figure 2 and Figure 33). The DIM/DIMbar signal is used as the input of the block named “Vref processing block”. Every half period of the mains voltage, the “Vref processing block” computes and holds the dimmer duty cycle and sets the corresponding V_{REF} voltage.

Unless the minimum peak current at CS1 pin reaches the V_{ILIM_MIN} level the internal power MOSFET connected between DRAIN and CS pins is kept open to avoid the leakage current of the dimmer from charging the C_{in} capacitor (see Figure 1) and providing a low impedance path for “SMART” dimmer operation.

CA is the Dimmer Conduction Angle expressed in degrees and can be calculated based on the Dimmer Conduction Time t_{CA} (see Figure 33) and the AC mains frequency F_{mains} described in the following formula:

$$CA = 360 \cdot t_{CA} \cdot f_{mains} \quad \text{(eq. 4)}$$

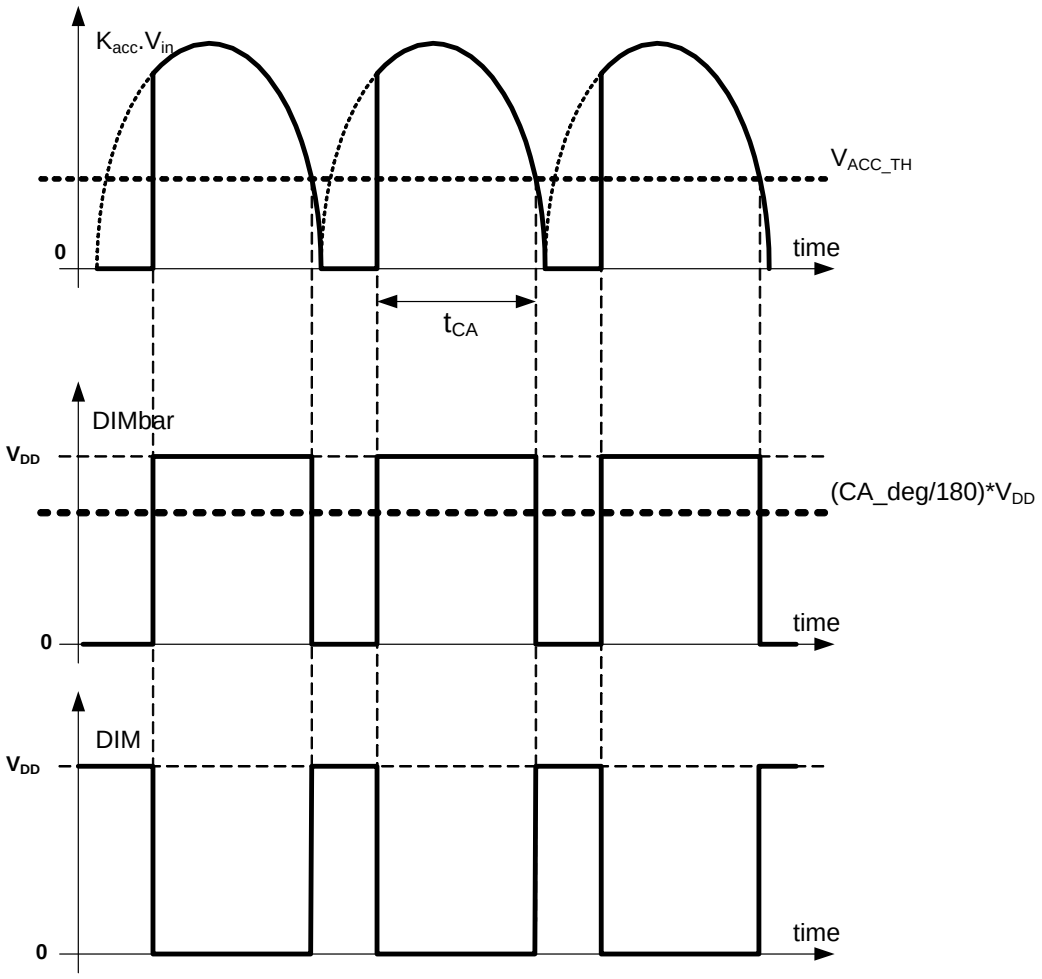


Figure 33. Dimming Waveforms

Detailed description of the V_{REF} processing

The conduction angle is obtained by the digital division of the sampled values of the conduction time and the period. The conduction time is counted by the timer A over the both periods of mains as the period of mains. This type of sensing decreases the diming system sensitivity to the asymmetry of the diming triac and reduces flickering. The conducting angle is obtained as the ratio of Timer A (conduction time) and Timer B (the mains period). Please refer to Figure 34 and Figure 35.

$$CA = \frac{2 \cdot T_{on}}{2 \cdot T} \quad \text{(eq. 5)}$$

The additional IIR filters and the conduction angle lockout for 32 cycles of the rectified mains signal helps to reduce flickering caused by the differing leading edges and quantization error of the A/D conversion at TF pin and CA measurement.

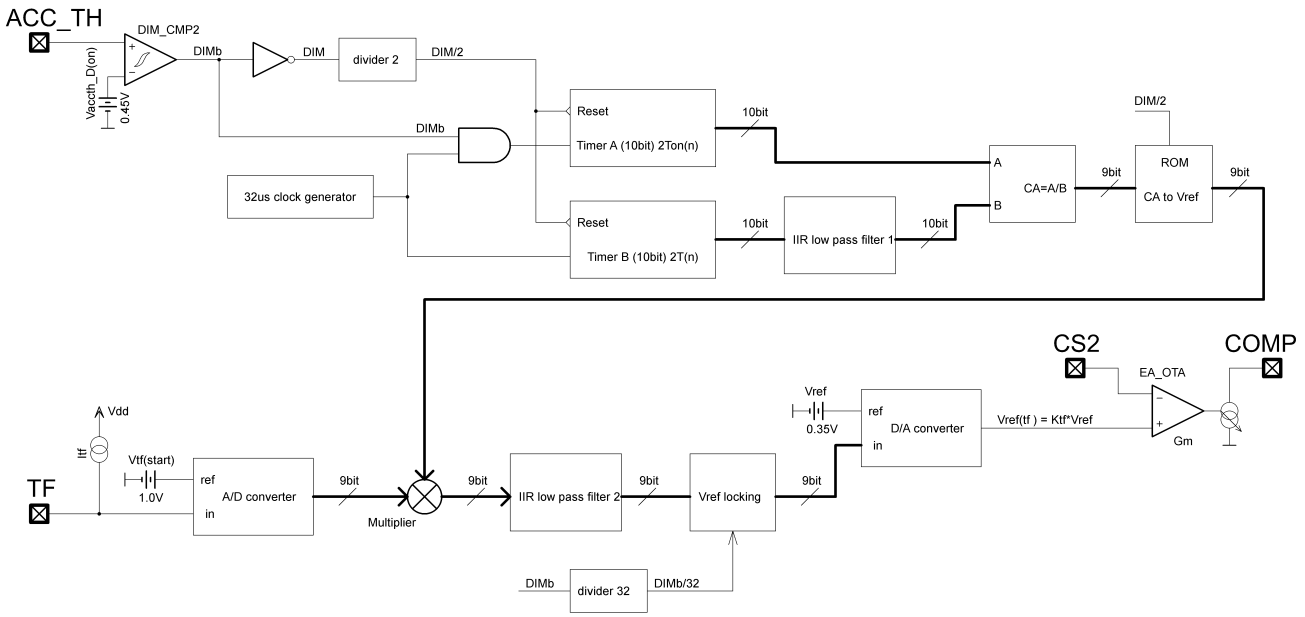


Figure 34. Detailed block schematic of the conduction angle measurement and the Vref processing

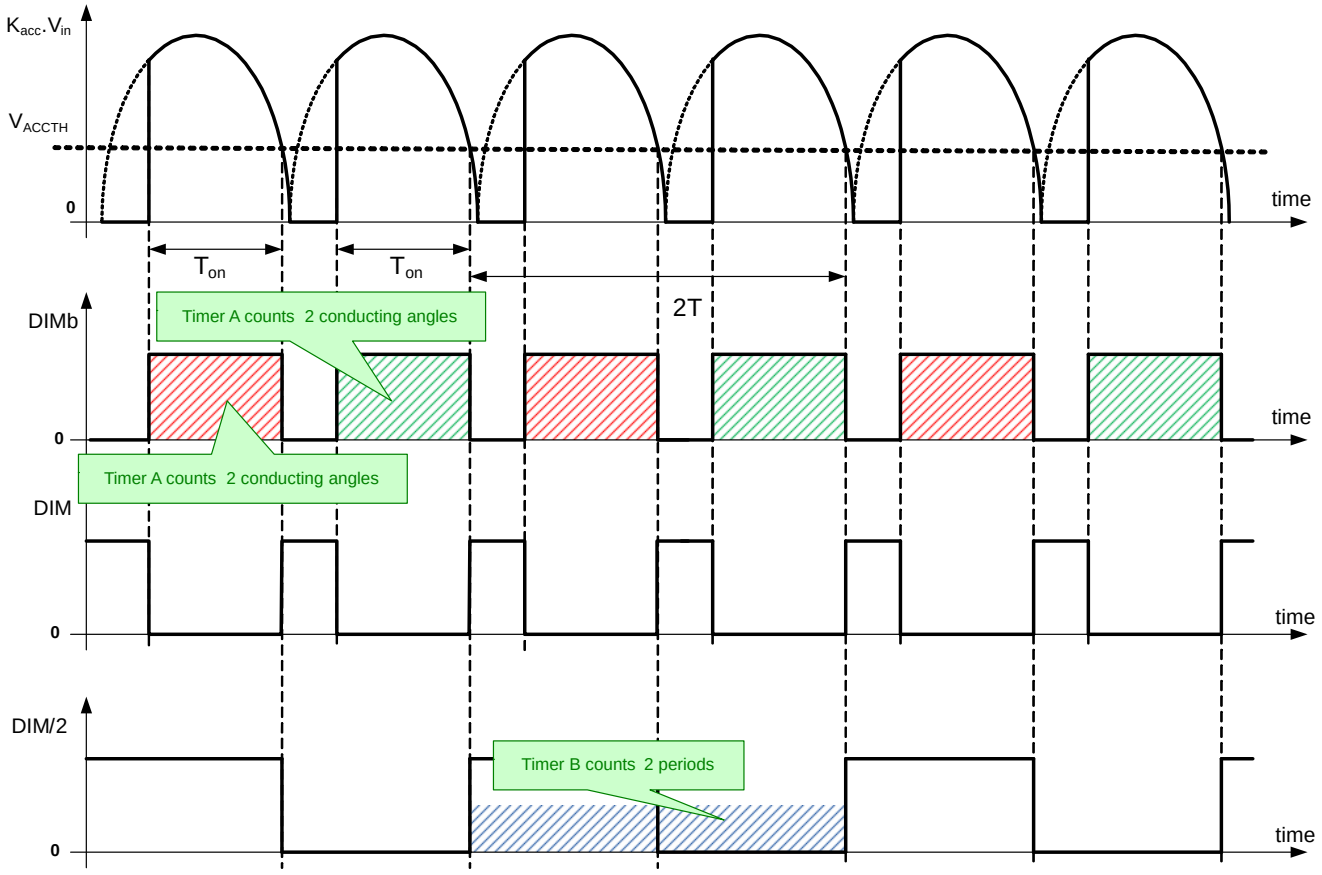


Figure 35. Time diagram of the implemented conduction angle measurement

The minimum current set−point feature is implemented. It starts play a role in case that the Vref is so small that the current set−point observed at CS1 pin is below the V_{ILIM_MIN} level. Then the regulation loop requirement is ignored and higher level of current set−point V_{ILIM_MIN} is applied. This feature sets the minimum current to avoid the current loop cut of when the triac dimming is applied. This feature increases the compatibility with the most of the triac dimmers.

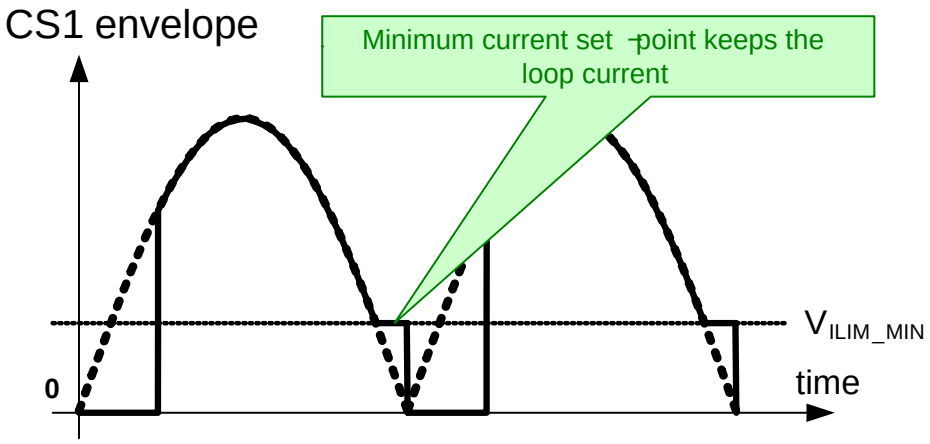


Figure 36. The minimum current set−point effect to keep the loop current

Operating modes and Protection modes

Table 5. Operating and protection modes

Event	Timer protection	Next device status	Release to normal operation mode
Overcurrent V_{ILIM} = 1.0 V	N/A	Normal operation	N/A
Reduced peak current V_{ILIM_MIN} = 0.35 V	N/A	Normal operation	N/A
Winding short $V_{sense1} > V_{CS1(stop)}$	4 consecutive pulses	Latch	$V_{CC} < V_{CC(reset)}$
Low supply $V_{CC} < V_{CC(off)}$	10 μs timer	Device stops	$V_{CC} > V_{CC(on)}$
Thermal foldback event $V_{OTP} < V_{TF(start)}$	Immediate reaction	Reduced output current, thermal fold−back	$V_{OTP} > V_{TF(start)}$
Output overvoltage $V_{OVP} > V_{OVP(off)}$	20 μs timer	Device stops	$V_{OVP} < V_{OVP(on)}$ $V_{CC} > V_{CC(on)}$
Overvoltage pin shorted to GND $V_{OVP} < V_{UVP}$	Immediate reaction	Device stops	$V_{CC} < V_{CC(reset)}$
Internal TSD	10 μs timer	Device stops	($V_{CC} > V_{CC(on)}$) & TSDb

CS2 ZCD timeout protection

The second CS2 pin has an additional feature. In case of very low average current is regulated the CS2 voltage can be too low. The CS2 sensed voltage can be too low that the CS2 ZCD is not detected. To avoid stopping the device under this condition the ZCD timeout feature is added. If no ZCD event is detected until the ZCD timer ($t_{ZCD(timeout)}$) elapses the internal cascode switch is turned on anyway.

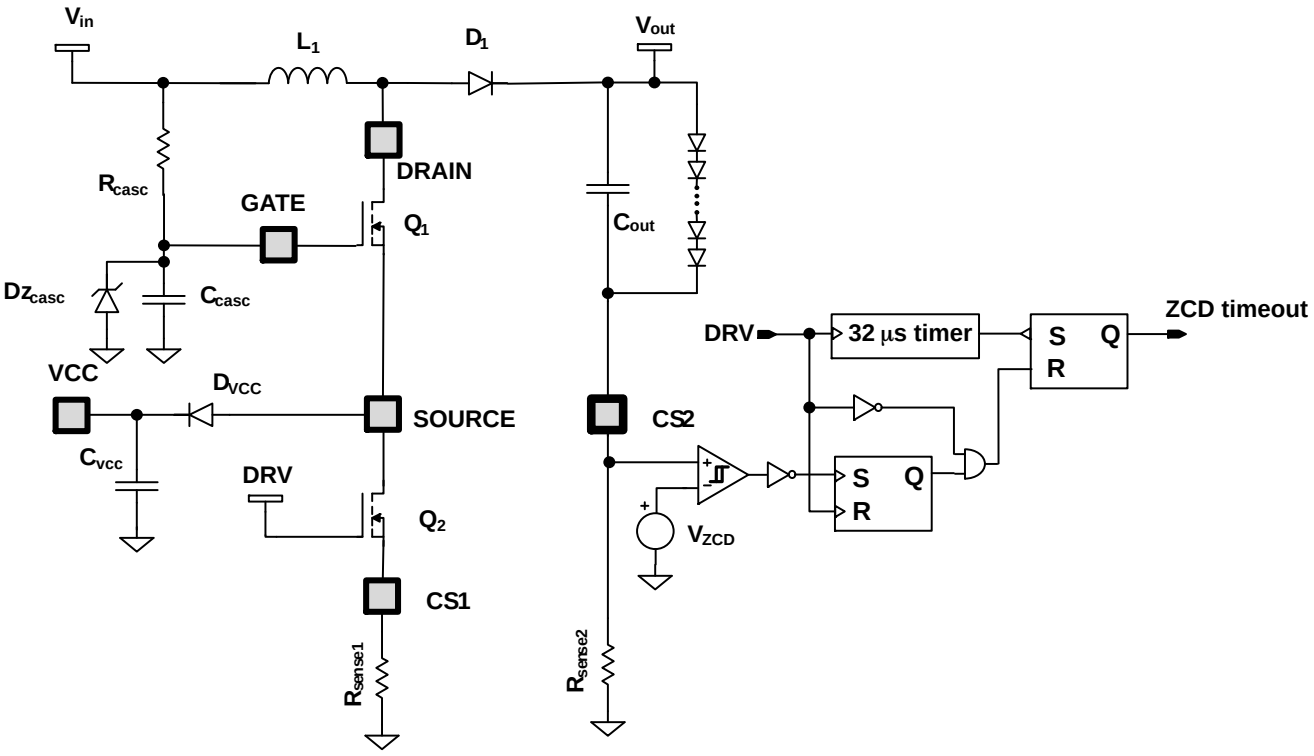


Figure 37. CS2 pin ZCD timeout protection – principal diagram

Protection against a winding short

Under some conditions, such as a winding short−circuit of the boost inductor, the on−time duration is at a minimum (based on the internal propagation delay of the detector and LEB duration). In this event, the current sense voltage increases above V_{ILIM}, because the controller is blanked due to the LEB time and fast current slope. Dangerously high current can occur in the system if nothing is done to stop the controller. To avoid this, an additional fast comparator senses when the current sense voltage on CS1 pin reaches $V_{CS1(stop)}$ = 1.5 x V_{ILIM}: if the fast comparator toggles 4 times, the controller immediately enters a protection mode. See the block diagram at Figure 2 for more details.

Overvoltage Protection

An overvoltage condition, for example if the LED string is open, can be sensed on V_{out} voltage by the external resistor divider comprised of R_{ovp_top} and R_{ovp_bot} resistors (see Figure 38) which is connected to the OVP pin. If the voltage of the OVP pin exceeds the $V_{OVP(off)}$ reference voltage, the OVP fault state goes high and the switching regulator stops switching. When the voltage at OVP pin drops below the $V_{OVP(on)}$ the device starts switching again. In addition the OVP input also has under−voltage protection (UVP) to ensure the resistor divider is properly connected. If the voltage at OVP pin is below the V_{UVP} threshold the device stops.

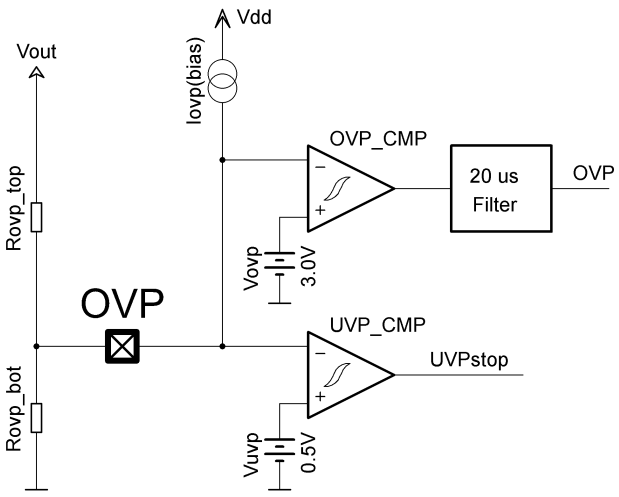


Figure 38. Overvoltage Protection Circuit

Thermal Fold−Back

The thermal fold−back circuit reduces the current supplying to the LED string if the temperature monitored by an external NTC resistor is too high.

The current is reduced down to 0% of its nominal value. The thermal fold−back starting temperature depends on the NTC resistor value selected by the power supply designer.

The TF pin allows the direct connection of an NTC. When the TF pin voltage V_{TF} drops below $V_{TF(start)}$, the internal reference for the constant current control V_{REF} is decreased proportionally to V_{TF}. When V_{TF} reaches $V_{TF(10\%)}$, V_{REF} is set to V_{REF10}, corresponding to 10% of the required output current. If V_{TF} drops below $V_{TF(10\%)}$ the switching regulator still reduces the V_{REF}. If V_{REF} drops below the 5% of its required value then the switching regulator enters the stop mode.

The thermal fold−back and OTP thresholds correspond roughly to the following resistances:

- Thermal fold−back starts when $R_{NTC} \leq 11.76$ kΩ.
- Thermal fold−back sets the 10% of VREF when $R_{NTC} \leq 5.88$ kΩ.

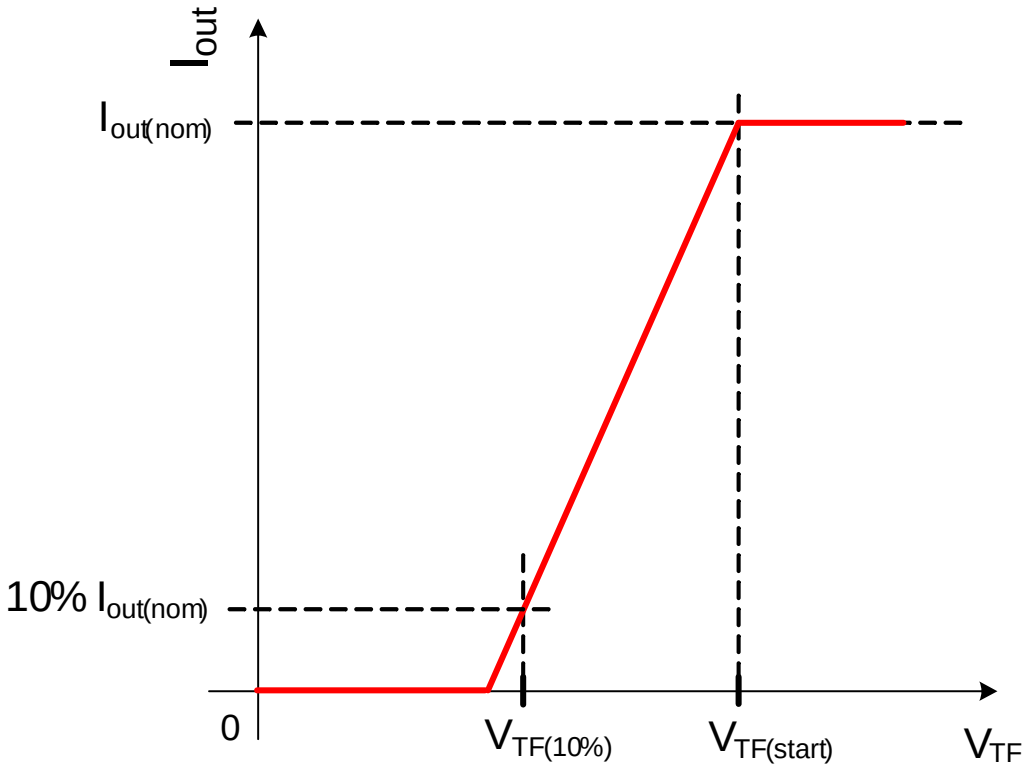


Figure 39. Output current reduction versus TF pin voltage

At startup, when V_{CC} reaches $V_{CC(on)}$, the TF pin sensing is blanked for at least 300 μs in order to allow the TF pin voltage to reach its nominal value if a filtering capacitor is connected to the TF pin. This is to avoid flickering of the LED light in case of over temperature or noise coupled to TF pin. The maximum value of OTP pin capacitor is given by the following formula (The standard start−up condition is considered and the NTC current is neglected):

$$C_{TFmax} = \frac{t_{TF(blank)min} \cdot I_{TFmin}}{V_{TF(start)max}} = \frac{250 \cdot 10^{-6} \cdot 80 \cdot 10^{-6}}{1.06} F = 19\ nF \quad \text{(eq. 6)}$$

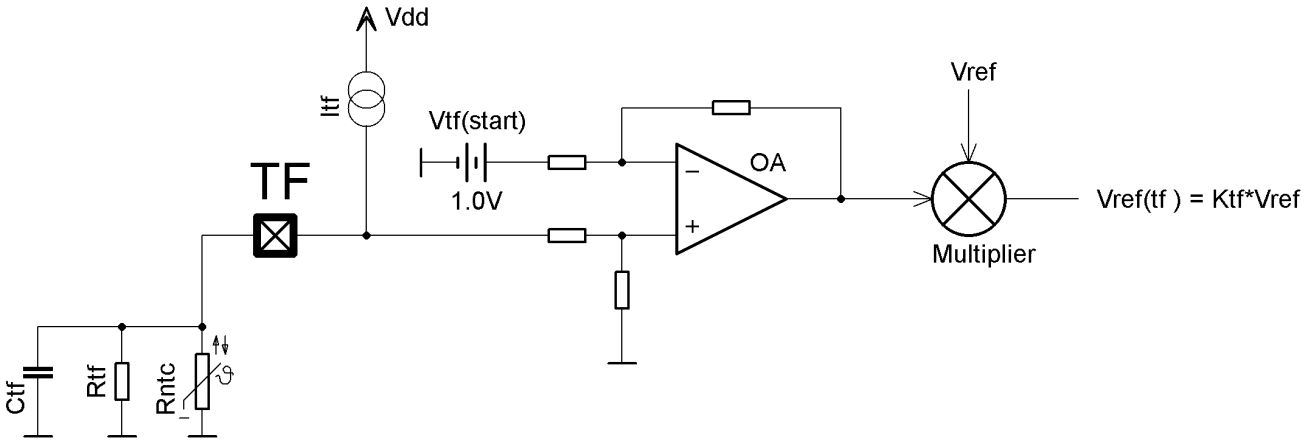


Figure 40. Thermal Fold−back circuitry

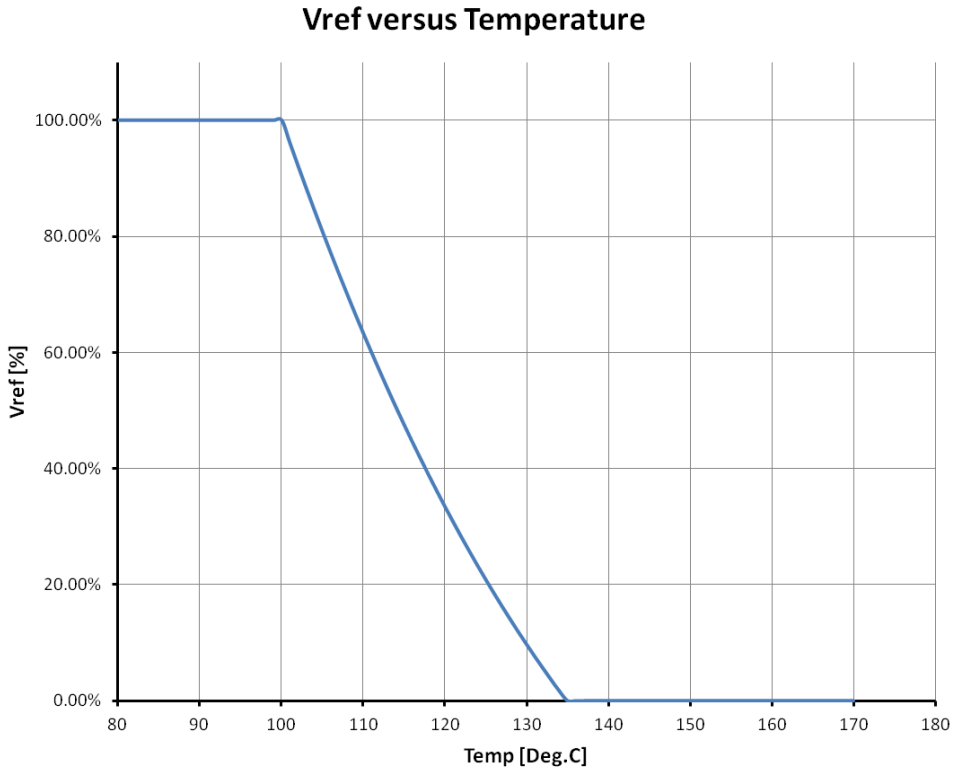


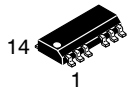
Figure 41. Typical thermal fold−back characteristic when the 330 kΩ NTC and 39 kΩ parallel resistor are connected to TF pin

Temperature shutdown

The NCL30095A includes a temperature shutdown protection with a trip point typically at 150°C and the typical hysteresis of 30°C. When the temperature rises above the high threshold, the switcher stops switching instantaneously, and goes to the stop mode with low power consumption. Specific blocks are still powered from the V_{CC} supply to keep the TSD information. When the temperature falls below the low threshold, the device restarts. See the status diagrams at the Figure 30.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

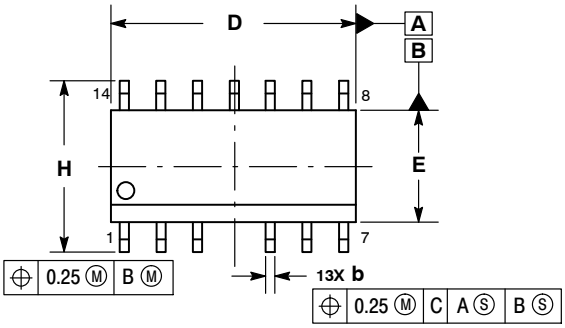
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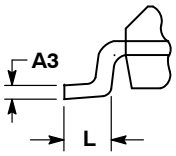


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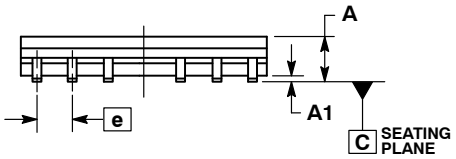
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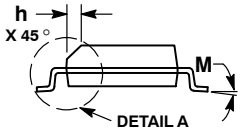
DATE 28 OCT 2015





DETAIL A

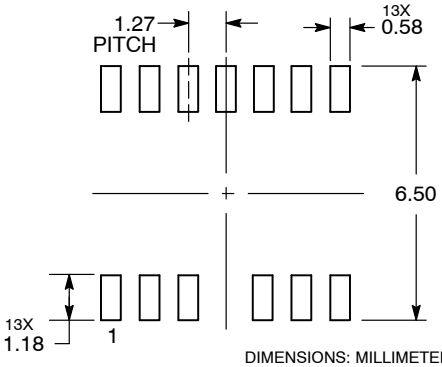




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

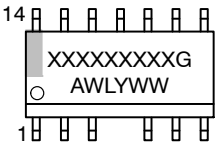
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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