NCL30105

Constant Off Time PWM Current-Mode Controller for LED Applications

The NCL30105 is a peak current controlled fixed off time controller designed for LED driver applications in which the LEDs are operated in deep Continuous Conduction Mode (CCM) without requiring slope compensation. Featuring an adjustable off time generator, the controller can drive a MOSFET up to a 500 kHz switching frequency.

A dedicated dimming pin enables the use of a pulse−width modulated logic signal to dim the LEDs directly. The soft−start pin creates a startup sequence that slowly ramps up the peak current and enables the adjustment of the peak current setpoint for analog dimming control. The device features robust protection features to detect switch overcurrent faults and to detect maximum on time events.

Features

- Constant Off Time Current−Mode Control Operation
- Adjustable Off Time (0.5 μs to 10 μs)
- Internal Leading Edge Blanking
- Source 250 mA / Sink 500 mA Peak Drive Capability
- ±3.2% Current Sense Accuracy at 25°C
- Internal Startup Delay
- 3.3 V Logic Level Dimming Input
- This is a Pb−Free Device

Safety Features

- Thermal Shutdown
- Maximum On Time Protection
- Overcurrent Protection

Typical Application

- LED Backlight Drivers for LCD Panels
- LED Light Bars
- LED Street Lighting
- LED Bulbs

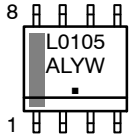
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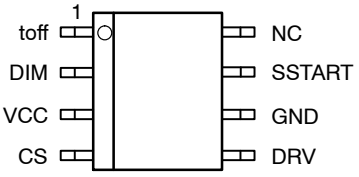
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



L0105 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCL30105DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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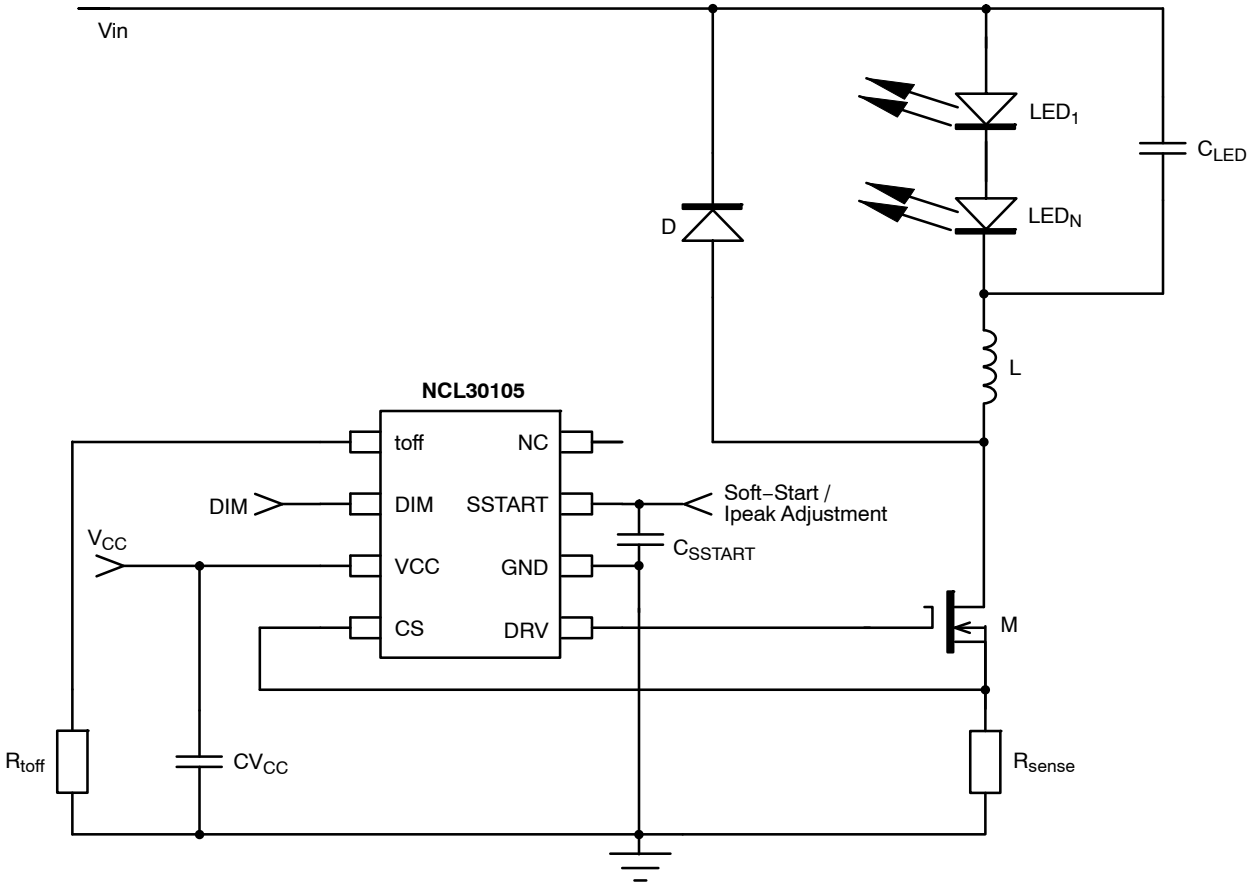


Figure 1. Typical Application Diagram

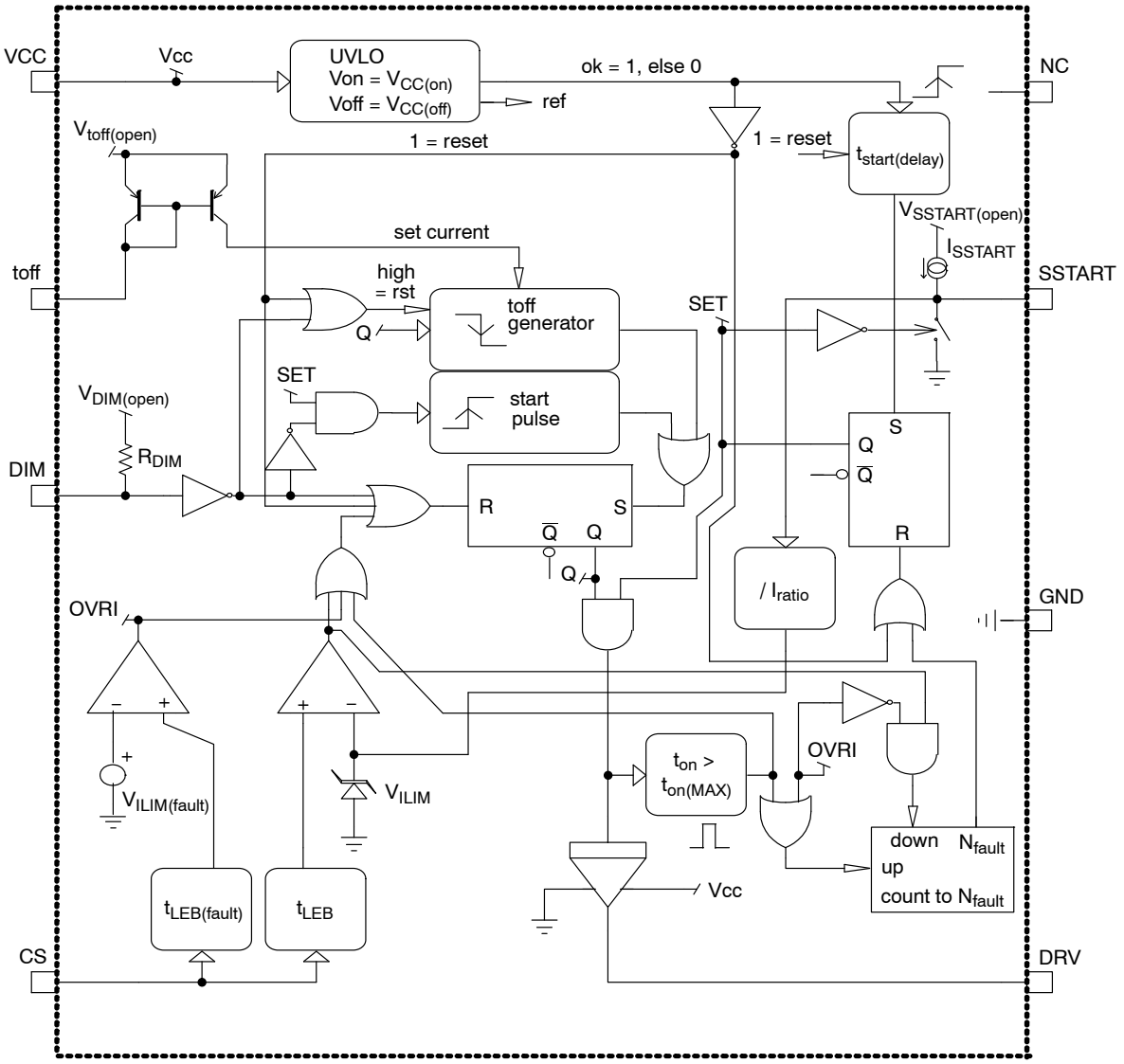


Figure 2. Internal Circuit Architecture

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Function	Pin Description
1	toff	Adjusts the Off Time Duration	A resistor to ground sets the off time duration.
2	DIM	Dimming Input	This pin is used for PWM dimming or to enable/disable the controller.
3	VCC	Supplies the Controller	An external auxiliary voltage connected to this pin supplies the controller.
4	CS	Current Sense Input	This pin monitors the peak current. When the peak current reaches the internal threshold, the DRV is turned off.
5	DRV	Driver Output	The output of the driver is connected to an external MOSFET gate.
6	GND	–	The controller ground.
7	SSTART	Soft−start / Peak Current Adjustment	A capacitor connected to this pin sets the soft−start duration. The voltage of this pin adjusts the peak current set point for analog dimming.
8	NC	Non−connected Pin	Non−connected pin

Table 2. MAXIMUM RATINGS TABLE (Notes 1 – 4)

Rating	Symbol	Value	Unit
toff Voltage	V_{toff}	−0.3 to 5.5	V
toff Current	I_{toff}	±10	mA
DIM Voltage	V_{DIM}	−0.3 to 7	V
DIM Current	I_{DIM}	±10	mA
SSTART Voltage	V_{SSTART}	−0.3 to 5.5	V
SSTART Current	I_{SSTART}	±10	mA
CS Voltage	V_{CS}	−0.3 to 7	V
CS Current	I_{CS}	±10	mA
DRV Voltage	V_{DRV}	−0.3 to V_{CC}	V
DRV Sink Current	$I_{DRV(sink)}$	500	mA
DRV Source Current	$I_{DRV(source)}$	250	mA
Supply Voltage	V_{CC}	−0.3 to 22	V
Supply Current	I_{CC}	±20	mA
Power Dissipation (SO−8) (T_A = 70°C, 2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)	P_D	450	mW
Thermal Resistance Junction−to−Ambient (SO−8) (2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad) Junction−to−Air, Low conductivity PCB (Note 3) Junction−to−Air, High conductivity PCB (Note 4)	$R_{\theta JA}$	 178 168 127	°C/W
Operating Junction Temperature Range	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Lead Temperature (Soldering, 10 s)	T_L	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1 − 8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A.
   Charged Device Model 2000 V per JEDEC Standard JESD22−C101C.
2. This device contains Latch−Up protection and exceeds ± 100 mA per JEDEC Standard JESD78.
3. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 80 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.

Table 3. ELECTRICAL CHARACTERISTICS (R_{toff} = 40.2 kΩ, V_{DIM} = 3 V, C_{SSTART} = 100 nF, V_{CS} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified (For typical values, T_J = 25°C. For min/max values, T_J = −40°C to 125°C, unless otherwise specified))

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Startup Voltage Threshold	V_{CC} Increasing	$V_{CC(on)}$	9	10	11	V
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8	8.8	10	V
Supply Voltage Hysteresis	$V_{CC(on)} - V_{CC(off)}$	$V_{CC(HYS)}$	1	1.2	1.5	V
Current Consumption in Latch Mode		$I_{CC(latch)}$	–	510	900	μA
Startup Current Consumption	$V_{CC} < V_{CC(on)} - 500$ mV	I_{CC1}	–	250	390	μA
Device Disabled Current Consumption	V_{DIM} = 0 V	I_{CC2}	–	0.71	1.7	mA
Device Switching Current Consumption	f_{SW} = 60 kHz	I_{CC3}	–	1.84	2.49	mA
GATE DRIVE						
Drive Sink Resistance	I_{SNK} = 25 mA	R_{SNK}	–	6.0	13.2	Ω
Drive Source Resistance	I_{SRC} = 25 mA	R_{SRC}	–	24	44	Ω
Rise Time	V_{DRV} = 10% to 90%	t_r	–	80	140	ns
Fall Time	V_{DRV} = 90% to 10%	t_f	–	25	60	ns
CURRENT SENSE						
Current Sense Voltage Threshold	T_J =−40°C to 125°C T_J =25°C	V_{ILIM}	0.95 0.977	1.01 1.01	1.05 1.042	V
Current Sense Propagation Delay	V_{CS} = 0 V to 1.2 V Step, dV/dt = 10 V/μs $V_{CS} = V_{ILIM}$ to V_{DRV} = 10%	t_{ILIM}	–	60	150	ns
Leading Edge Blanking Duration		t_{LEB}	470	545	670	ns
CONSTANT OFF TIME GENERATOR (Note 5)						
Off Time (Note 6)	R_{toff} = 5 kΩ	t_{off1}	0.87	1.02	1.13	μs
Recommended Off Time Resistor Range		$R_{toff(range)}$	2.5	–	60	kΩ
Minimum Off Time	R_{toff} = 0 Ω	$t_{off(MIN)}$	0.3	0.37	0.5	μs
Maximum Off Time	R_{toff} = open	$t_{off(MAX)}$	10	11.77	14.5	μs
t_{off} Pin Regulated Voltage		$V_{toff(REG)}$	0.95	1	1.05	V
Maximum Switching Frequency (Note 7)	R_{toff} = 0 Ω	$f_{(MAX)}$	500	–	–	kHz
SOFT−START						
Soft−Start Charge Current	V_{SSTART} = 3 V	I_{SSTART}	17	20	23	μA
Soft−Start Voltage to Peak Current Set Point Ratio	$V_{SSTART} = V_{ILIM} * I_{ratio}$	I_{ratio}	2.85	3	3.15	–
Soft−Start Pin Open Voltage		$V_{SSTART(open)}$	4.5	5	5.5	V
Soft−Start Internal Discharge Switch Resistance	I_{SSTART} = 5 mA	$R_{DS(on)SSTART}$	200	350	500	Ω
DIMMING INPUT						
Dimming Enable Voltage Threshold	V_{DIM} Increasing	$V_{DIM(H)}$	1.8	2	2.2	V
Dimming Disable Voltage Threshold	V_{DIM} Decreasing	$V_{DIM(L)}$	0.8	1	1.2	V
DIM Pin Open Voltage		$V_{DIM(open)}$	4	4.5	5.5	V
DIM Pin Internal Pull−Up Resistor	V_{DIM} = 0 V	R_{DIM}	50	90	150	kΩ
Dimming Wake−Up Time	V_{DIM} = 0 V to 3 V Step, dV/dt = 10 V/μs $V_{DIM} = V_{DIM(H)}$ to V_{DRV} = 90%	t_{wake}	–	0.28	1	μs

5. See Figure 17.
6. The tolerance of toff is guaranteed by design.
7. The thermal limitation of the device specified by the Maximum Ratings Table must not be exceeded.

Table 3. ELECTRICAL CHARACTERISTICS (R_{toff} = 40.2 kΩ, V_{DIM} = 3 V, C_{SSTART} = 100 nF, V_{CS} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified (For typical values, T_J = 25°C. For min/max values, T_J = −40°C to 125°C, unless otherwise specified))

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
PROTECTION						
Maximum On Time		$t_{on(MAX)}$	29.8	34	42.1	μs
Number of Consecutive Maximum On Time Events or Overcurrent Events		N_{fault}	–	8	–	–
Overcurrent Current Sense Voltage Threshold		$V_{ILIM(fault)}$	1.5	1.6	1.7	V
Overcurrent Propagation Delay	V_{CS} = 0 V to 2 V Step, dV/dt = 10 V/μs V_{CS} = $V_{ILIM(fault)}$ to V_{DRV} = 10%	$t_{ILIM(fault)}$	10	70	150	ns
Overcurrent Leading Edge Blanking Duration		$t_{LEB(fault)}$	170	220	280	ns
Leading Edge Blanking Duration Ratio	$t_{LEB(fault)}/t_{LEB}$	$t_{LEB(ratio)}$	0.3	0.4	0.8	–
Startup Delay	V_{CC} = $V_{CC(on)}$ to V_{DRV} = 90%	$t_{start(delay)}$	100	130	172	ms
Thermal Shutdown	T_J = Increasing	T_{SHDN}		155		°C
Thermal Shutdown Hysteresis	T_J = Decreasing	$T_{SHDN(HYS)}$		40		°C
Thermal Shutdown Delay		$T_{SHDN(delay)}$		75		μs

5. See Figure 17.
6. The tolerance of toff is guaranteed by design.
7. The thermal limitation of the device specified by the Maximum Ratings Table must not be exceeded.

TYPICAL CHARACTERISTICS

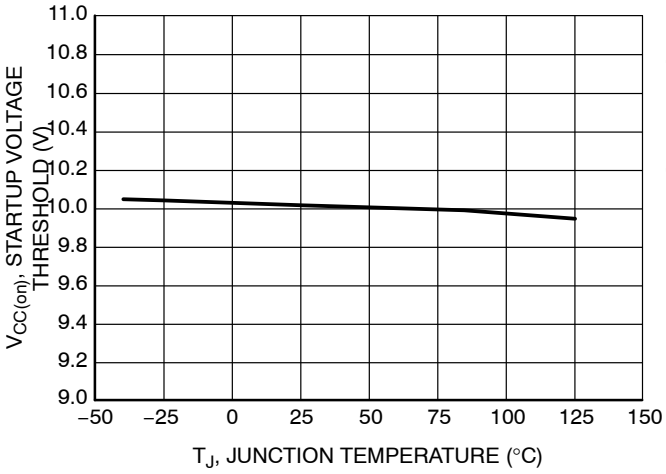


Figure 3. Startup Voltage Threshold vs. Junction Temperature

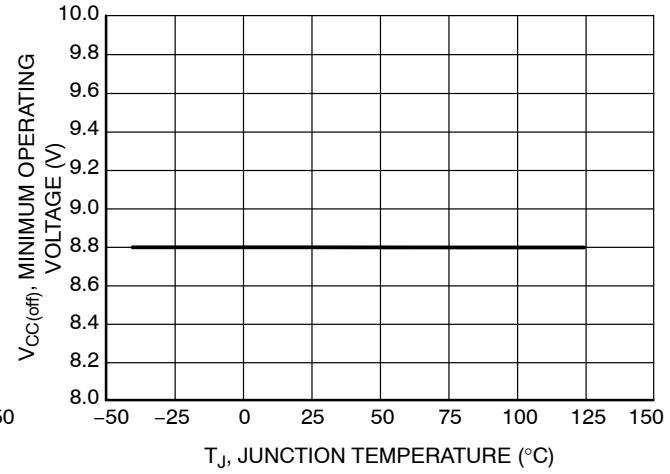


Figure 4. Minimum Operating Voltage vs. Junction Temperature

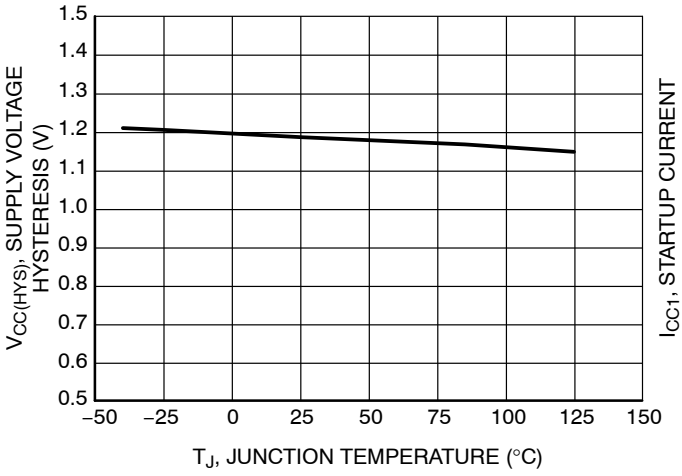


Figure 5. Supply Voltage Hysteresis vs. Junction Temperature

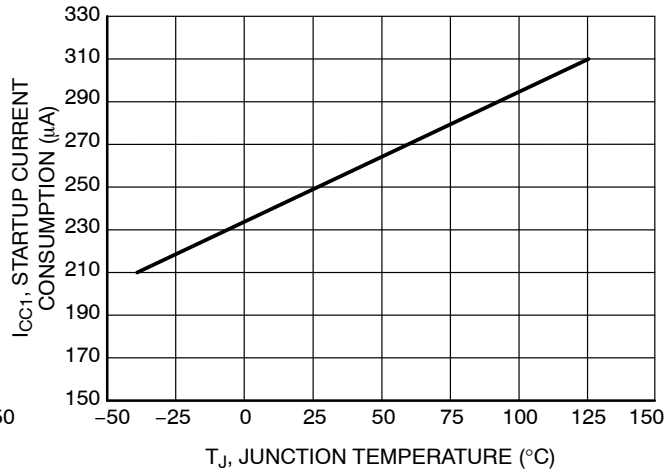


Figure 6. Startup Current Consumption vs. Junction Temperature

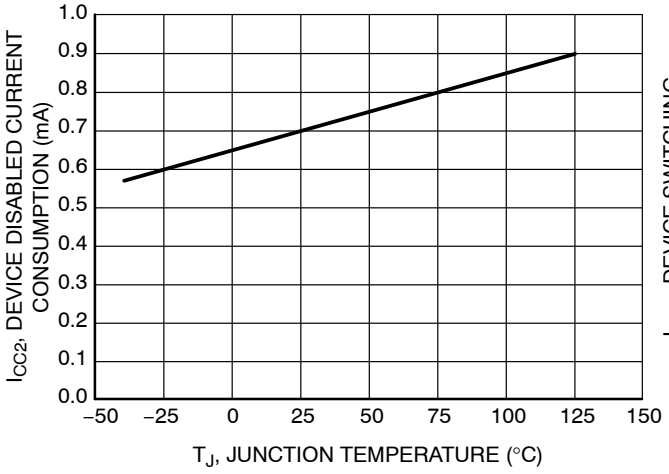


Figure 7. Device Disabled Current Consumption vs. Junction Temperature

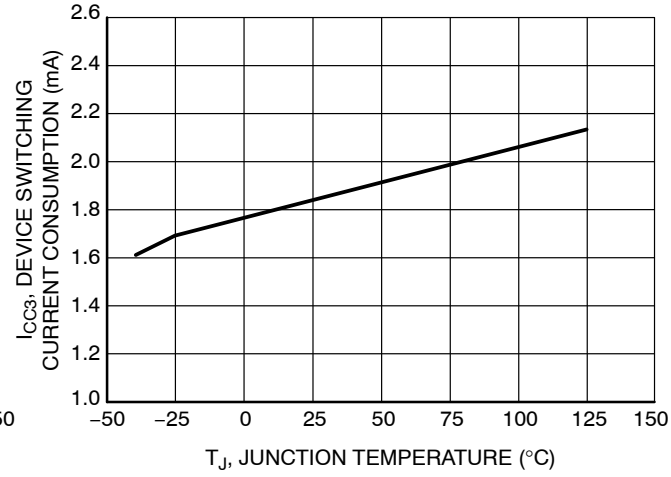


Figure 8. Device Switching Current Consumption vs. Junction Temperature

TYPICAL CHARACTERISTICS

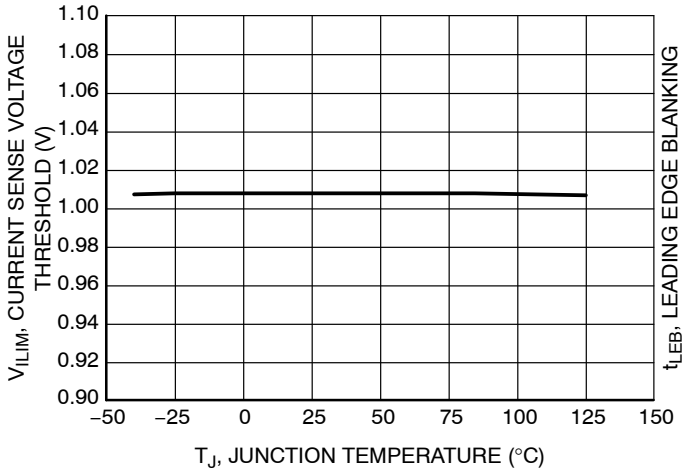


Figure 9. Current Sense Voltage Threshold vs. Junction Temperature

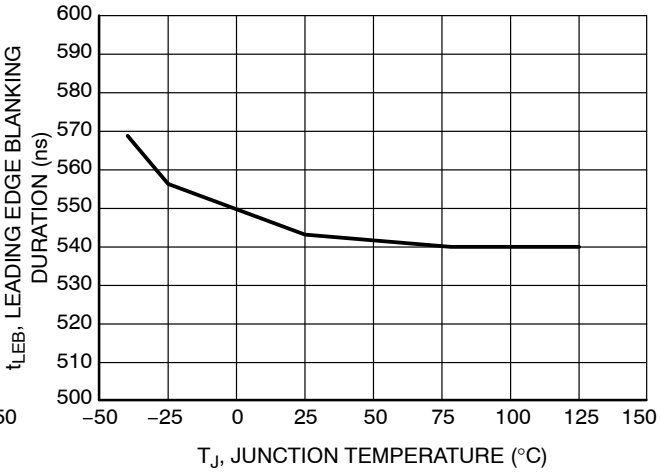


Figure 10. Leading Edge Blanking Duration vs. Junction Temperature

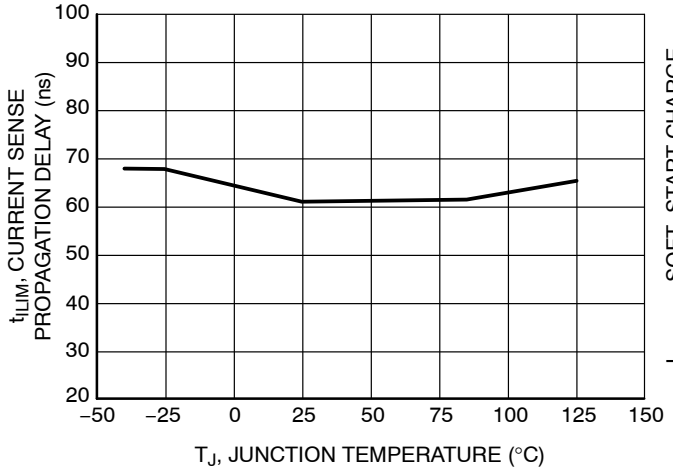


Figure 11. Current Sense Propagation Delay vs. Junction Temperature

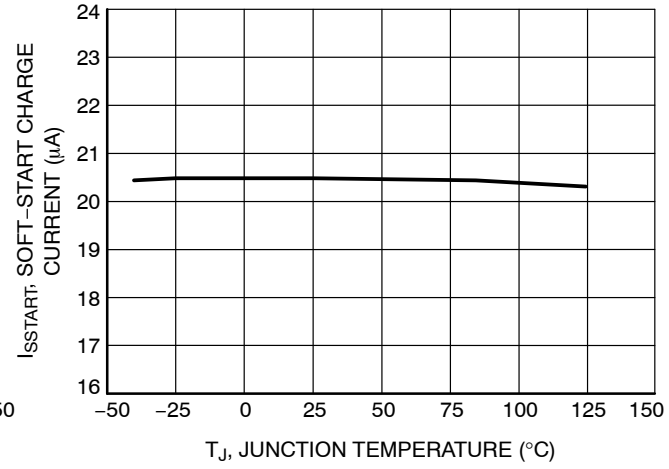


Figure 12. Soft−Start Charge Current vs. Junction Temperature

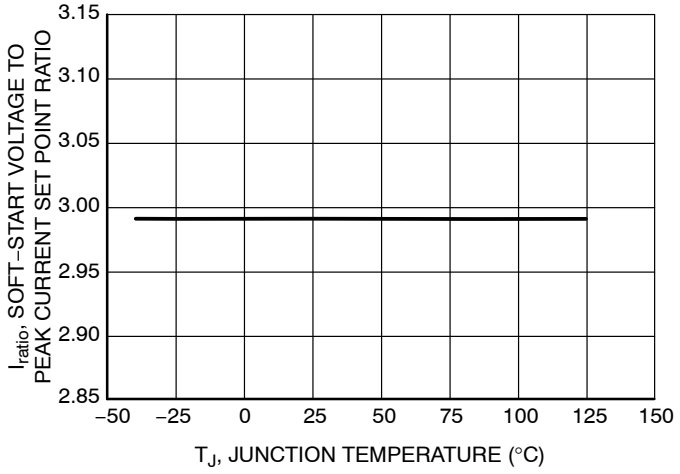


Figure 13. Soft−Start Voltage to Peak Current Set Point Ratio vs. Junction Temperature

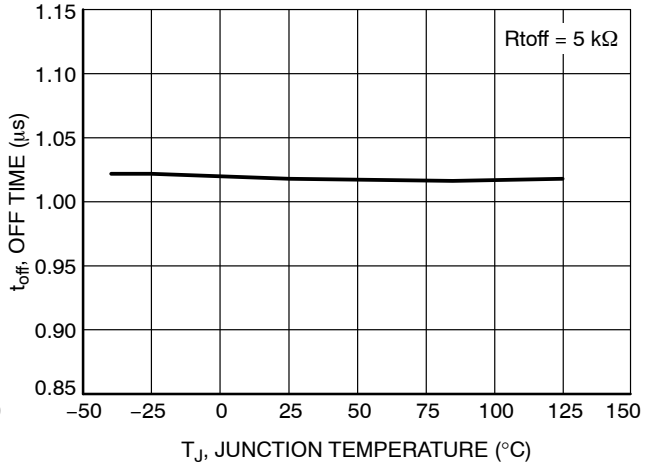


Figure 14. Off Time vs. Junction Temperature

TYPICAL CHARACTERISTICS

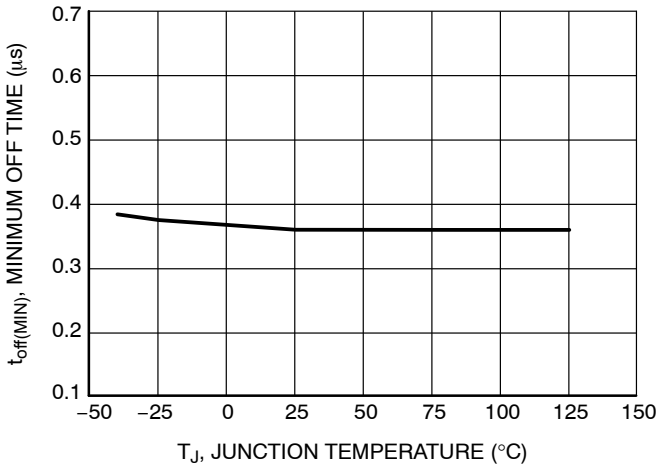


Figure 15. Minimum Off Time vs. Junction Temperature

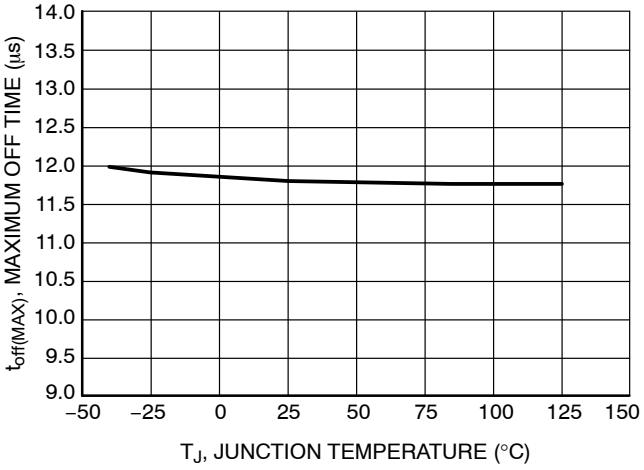


Figure 16. Maximum Off Time vs. Junction Temperature

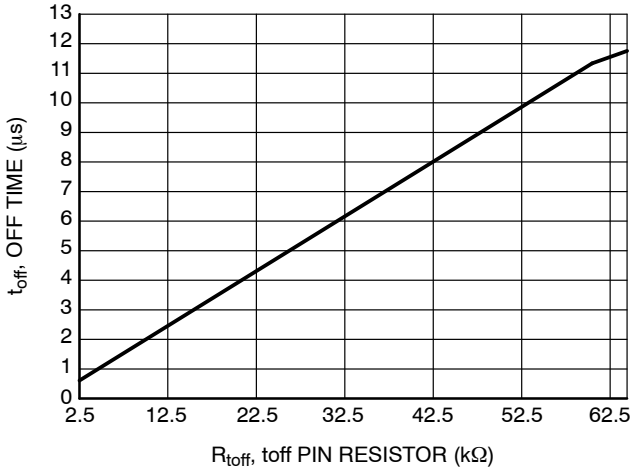


Figure 17. Off Time vs. toff Pin Resistor

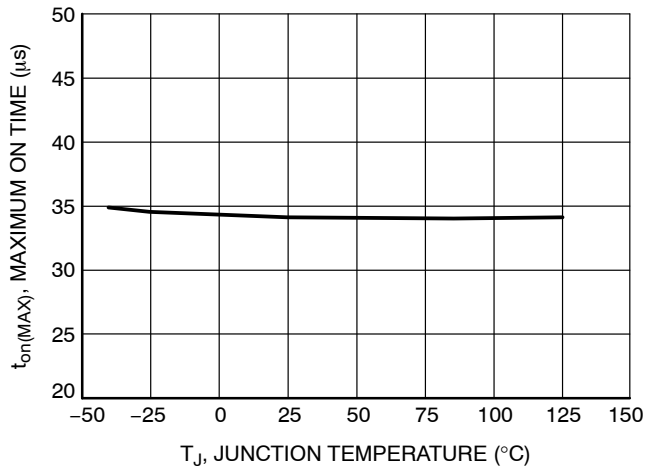


Figure 18. Maximum On Time vs. Junction Temperature

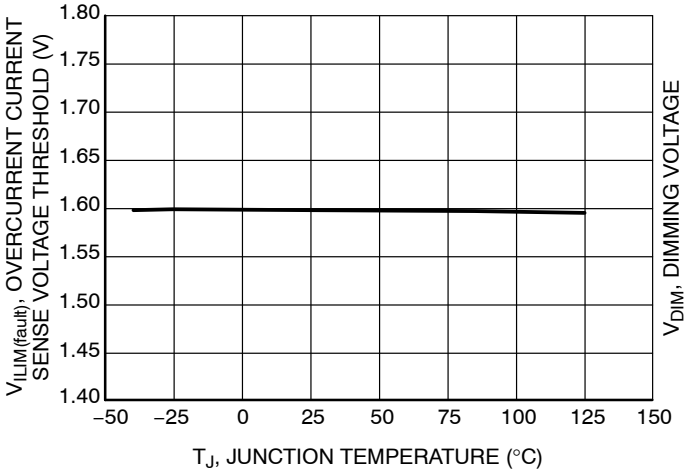


Figure 19. Overcurrent Current Sense Voltage Threshold vs. Junction Temperature

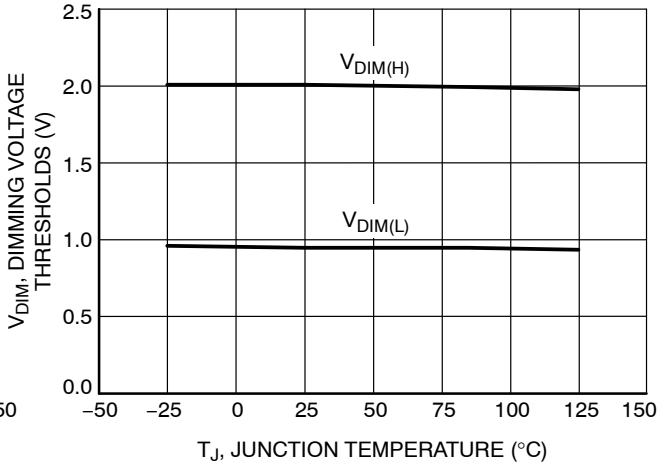


Figure 20. Dimming Thresholds vs. Junction Temperature

TYPICAL CHARACTERISTICS

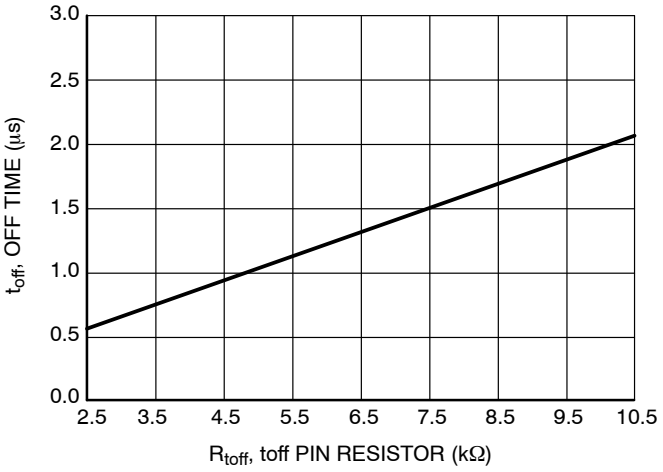


Figure 21. Zoomed In Off Time vs. toff Pin Resistor

Application Information

Introduction

NCL30105 implements a current−mode architecture operated with a constant off time. The internal current set point and the external sense resistor determine the on time duration. The off time duration is adjusted with a resistor connected from the toff pin to ground. The constant off time operation enables deep continuous conduction mode operation without requiring slope compensation. The DIM pin enables the use of a PWM signal to modulate the switching pattern and adjust the average luminosity. The SSTART pin creates a soft−start that reduces the stress on the power components during startup and enables the use of an analog dimming signal to set the peak current by adjusting the SSTART pin voltage.

- **Constant Off Time Peak Current−Mode Operation:** The constant off time technique enables the controller to operate a converter in deep continuous conduction mode without requiring slope compensation. The constant off time technique is inherently immune to sub−harmonic oscillations.
- **Off Time Adjustment:** A pull−down resistor connected to the toff pin sets the off time duration.
- **Maximum On Time Protection:** an internal circuit monitors the drive signal on time duration. If the drive on time duration reaches $t_{on(MAX)}$, the fault up/down counter is incremented by 1. If the drive on time duration reaches $t_{on(MAX)}$ during the next clock cycle, the counter is incremented again. If the drive on time duration does not reach $t_{on(MAX)}$ due to the current comparator being triggered during the next drive on time, the counter is decremented by 1. This sequence continues until the counter reaches 8. If the counter reaches 8, the NCL30105 is immediately latched off. When V_{CC} is forced below $V_{CC(off)}$ and then above $V_{CC(on)}$, the latch is reset.
- **LED Short−Circuit Protection:** If the CS pin voltage increases above $V_{ILIM(fault)}$, the overcurrent comparator is triggered, which turns off the drive and increments the fault up/down counter by 1. If the overcurrent comparator is triggered again during the next drive on time, the counter is incremented again. If the overcurrent comparator is not triggered due to the current comparator being triggered during the next drive on time, the counter is decremented by 1. This sequence continues until the counter reaches 8. If the counter reaches 8, the part is immediately latched off. When V_{CC} is forced below $V_{CC(off)}$ and then above $V_{CC(on)}$, the latch is reset.
- **Power On Delay:** When V_{CC} reaches $V_{CC(on)}$, the $t_{start(delay)}$ timer begins counting, during which the drive is disabled. When $t_{start(delay)}$ elapses, the SSTART pin current source is enabled and the soft−start sequence begins.
- **Soft−Start Operation:** A capacitor connected to the SSTART pin is charged by an internal current source after the $t_{start(delay)}$ timer period has elapsed. The soft−start period is completed when the SSTART pin voltage reaches $V_{ILIM}*I_{ratio}$. The soft−start capacitor is discharged during the $t_{start(delay)}$ to ensure the SSTART pin voltage begins charging from zero.
- **Peak Adjustment:** Analog dimming is achieved by forcing the SSTART pin below $V_{ILIM}*I_{ratio}$, which lowers the peak current set point. Note: even if the SSTART pin is forced to 0 V, there is still a minimum on time every switching cycle. Under this condition, the minimum on time is the current sense leading edge blanking time plus the propagation delay to turn off the MOSFET and the off time is determined by the toff resistor value.
- **Leading Edge Blanking:** an internal circuit blinds the current sense comparator for a few hundred nanoseconds when the output drive goes high. The LEB ensures that controller remains insensitive to the turn−on voltage spikes observed on the CS pin due to the free−wheel diode recovery time.
- **Dimming Input:** a dedicated pin is provided to PWM modulate the LED current to reduce the LED luminosity. The circuit is driven on and off via a 3.3−V logic level signal. The DIM pin can also be used as an enable/disable pin, since the switching is disabled when there is a logic low signal applied to this pin.
- **Thermal Shutdown:** if the junction temperature of the controller exceeds an internal threshold, the drive is disabled. The drive remains disabled until the junction temperature decreases below the internal hysteresis threshold. The disabling of the drive protects the controller from destruction due to overheating.

Startup Sequence

When V_{CC} reaches $V_{CC(on)}$, the NCL30105 maintains the drive low and the soft−start capacitor (C_{SSTART}, connected to the SSTART pin) remains pulled to ground by the internal pull−down switch until the startup delay ($t_{start(delay)}$) elapses. Once the $t_{start(delay)}$ period has elapsed, the drive is enabled and a soft−start sequence begins. The internal current source begins charging C_{SSTART} and the voltage on the SSTART pin (V_{SSTART}) begins increasing. The peak current set point is equal to V_{SSTART} divided by I_{ratio}. When V_{SSTART} reaches the voltage that sets the maximum peak current ($V_{SSTART} = V_{ILIM}*I_{ratio}$), the soft−start sequence is complete and the peak current set point is equal to V_{SSTART} divided by I_{ratio}. Figure 22 describes a typical start−up sequence.

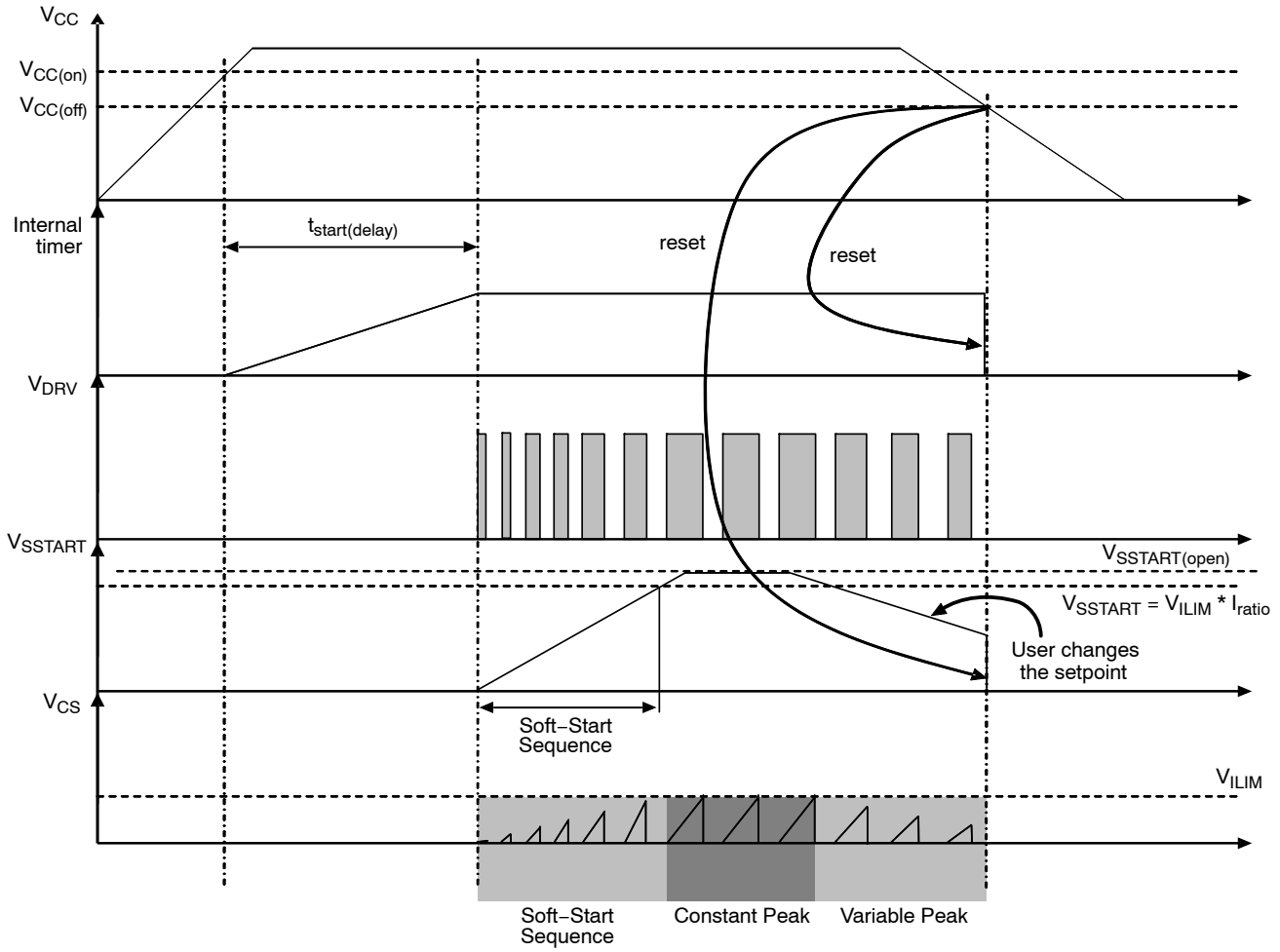


Figure 22. A Typical Startup Sequence

Soft−Start Pin

The soft−start internal section is shown in Figure 23. The soft−start sequence is implemented using a current source that charges an external capacitor. The relationship between the capacitor voltage and the peak current voltage set point is I_{ratio}. The maximum peak current set point is V_{SSTART}/I_{ratio}. For luminosity balancing purposes, it is possible to force the voltage on the SSTART pin from an external source. When forcing V_{SSTART} with an external source, the current into the SSTART pin must be limited to ensure that the maximum current rating is not exceeded. It is recommended to set V_{SSTART} by connecting a diode as shown in Figure 23. Using this configuration, the SSTART capacitor value to set a 15 ms soft−start duration (t_{SSTART}) is calculated using Equation 1:

(eq. 1)

$$C_{SSTART} = \frac{I_{SSTART} \cdot t_{SSTART}}{I_{ratio}} = \frac{20\ \mu \cdot 15\ m}{3} = 0.1\ \mu F$$

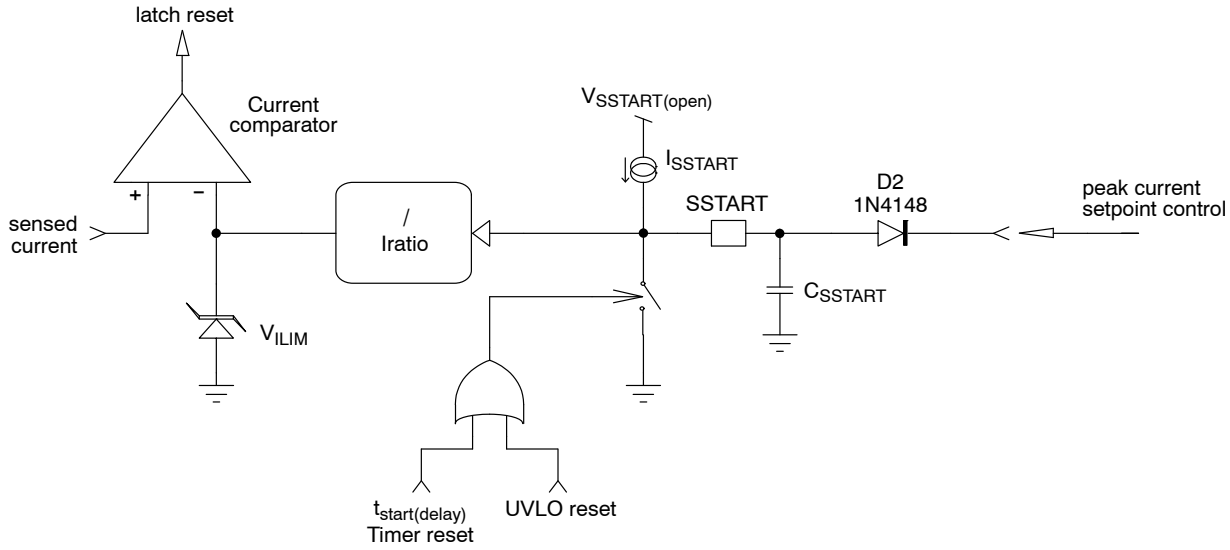


Figure 23. The Soft−start Block Configuration to Set the Peak Current Setpoint

Constant Off time Generator

The controller operates with a constant off time technique. The off time technique is implemented by forcing a constant off time with the on time being set by the combination of the peak current threshold, the inductor value, and the input voltage. Unlike traditional peak current mode control, the fixed off time technique is not susceptible to sub−harmonic instability as shown in Figure 24:

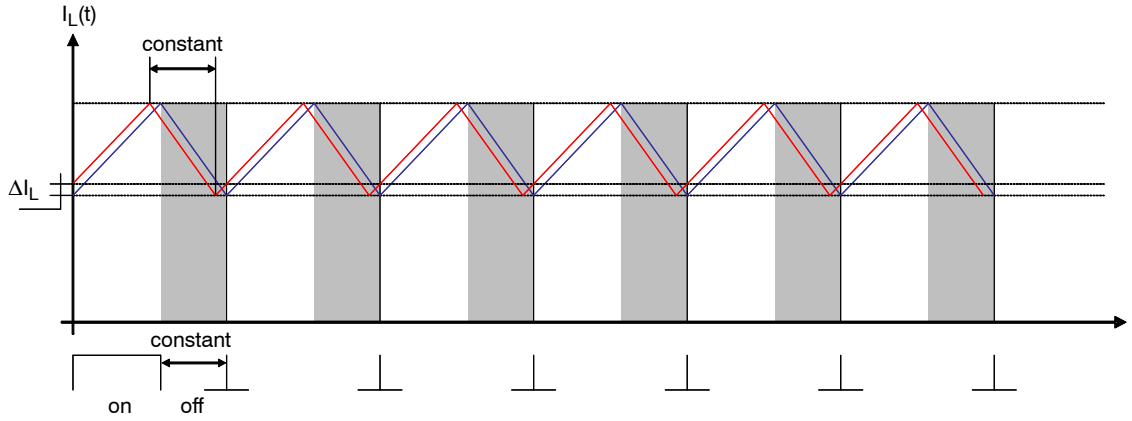


Figure 24. The Constant Off Time Technique is Immune to Sub−Harmonic Instabilities without Ramp Compensation

In Figure 24, the perturbation is corrected in one switching cycle, despite a duty ratio greater than 50%. This benefit enables the designer to exclude slope compensation when operating the inductor in a deep continuous conduction mode.

The constant off time generator follows the principle sketched in Figure 25 where an internal timer is started at the end of each on time. Once the off time generator has elapsed, it begins the next DRV pulse. The off time is programmed by connecting a resistor from the toff pin to ground. The off time range is from 0.5 μs to 10 μs.

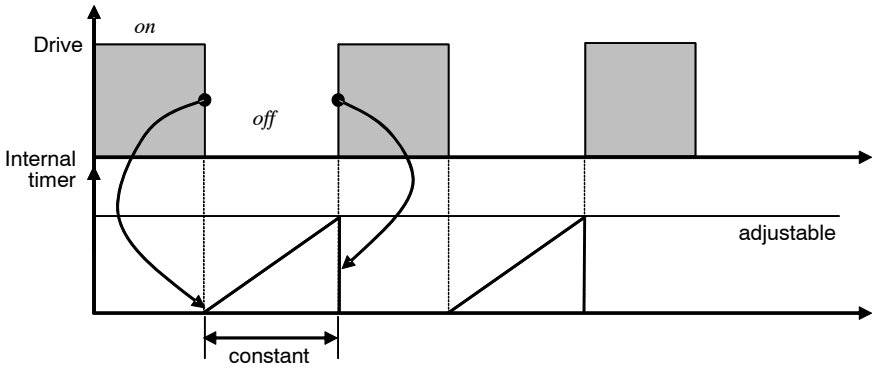


Figure 25. A Timer is Started at the End of the On Time Duration

Protection

The NCL30105 includes several methods of protection. One of the protection features is the maximum on time limitation, which protects the system if the CS pin does not receive a signal. The on time is internally limited to $t_{on(MAX)}$. The maximum on time limitation may occur if the input voltage is too low or if the CS pin is shorted to ground. After 8 consecutive maximum on times events, the controller is latched as shown in Figure 26.

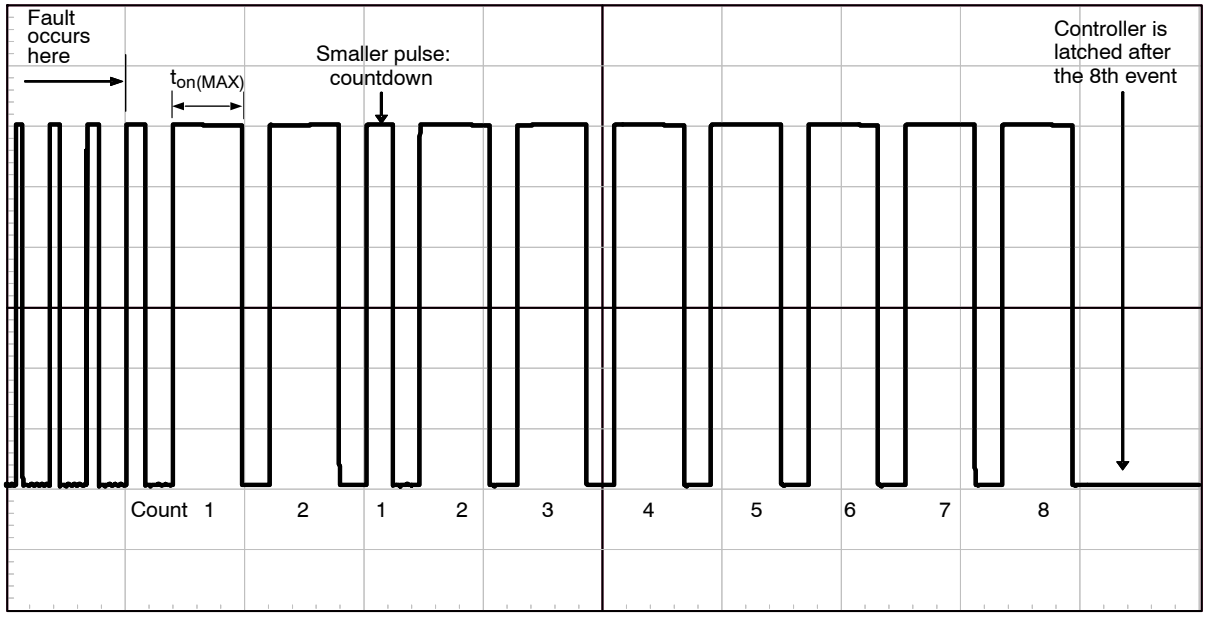


Figure 26. The Protection Feature Limits the Maximum On Time and Disables the Controller During a Fault

In latched mode, the controller consumes a low current and waits for a complete V_{CC} cycle (V_{CC} decreases to less than $V_{CC(off)}$ and then increased to greater than $V_{CC(on)}$) to resume operation. The tracking of the fault events is implemented with an up/down counter. The counter is incremented by 1 when the $t_{on(MAX)}$ duration ends the driving pulse. The counter is decremented by 1 when a normal reset occurs via the current comparator. When the counter reaches 0, it stores this value and waits for an up pulse to change state.

The NCL30105 includes Leading Edge Blanking (LEB) circuits to prevent inadvertent triggering of the current and overcurrent comparators. When the DRV pin goes high, noise is generated on the CS pin due to the parasitic elements in the circuit. The LEB circuit “blanks” the noise to ensure that the current and overcurrent comparators are not inadvertently triggered. If the LEB circuit is omitted, the noise causes the DRV to turn off before the required peak current is reached as shown in Figure 28. This causes the system to operate erratically. When the LEB circuit is included, the noise is “blanked” by blinding the current comparator for the LEB duration (t_{LEB}) and the required peak current is reached as shown in Figure 29. The inclusion of the LEB circuits prevents the erratic operation of the system.

Another protection feature is the overcurrent detection. The overcurrent detection activates when a short−circuit occurs in the inductor and LED string. To prevent false

detection during surge tests, the controller uses the same counter as the maximum on time limitation. Due to the two different LEB circuits (t_{LEB} and $t_{LEB(fault)}$) configuration, if there is a severe overload, the overcurrent comparator is triggered first and the counter is incremented. If the overcurrent comparator is not triggered during the next clock cycle, the counter is decremented by the current comparator. Figure 27 depicts the logical arrangement inside the controller. In the presence of a fast rising signal, the overcurrent comparator is triggered first since $t_{LEB(fault)} < t_{LEB}$. When the overcurrent comparator output goes high, it resets the PWM latch and increments the counter. The counter can no longer increment or decrement until the next switching cycle. If during the time the overcurrent comparator output is high, t_{LEB} elapses and causes the current comparator output to go high, the output of the current comparator is ignored due to the AND gate connection. Figure 30 illustrates the operation of the CS logic during an overcurrent fault. **Only one up count or one down count is made per switching cycle.**

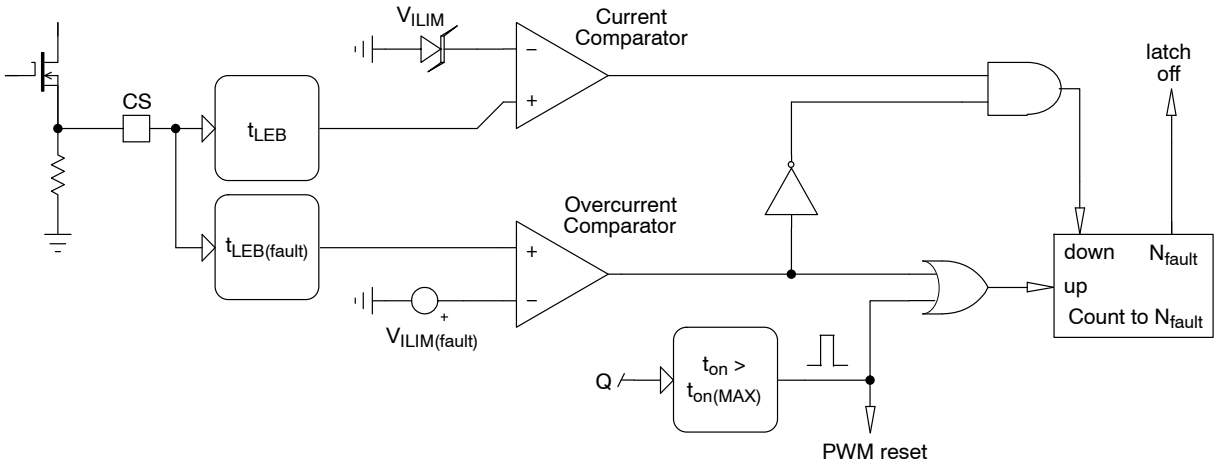


Figure 27. CS Internal Logic

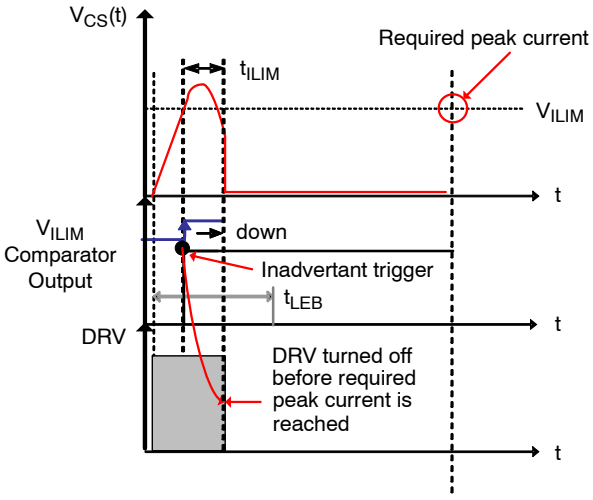


Figure 28. Circuit without Leading Edge Blanking

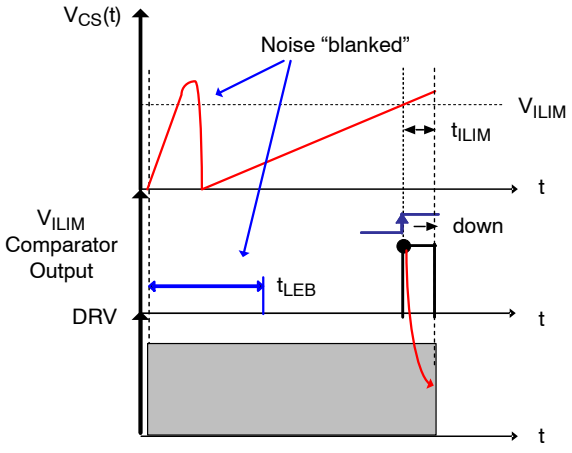


Figure 29. Circuit with Leading Edge Blanking

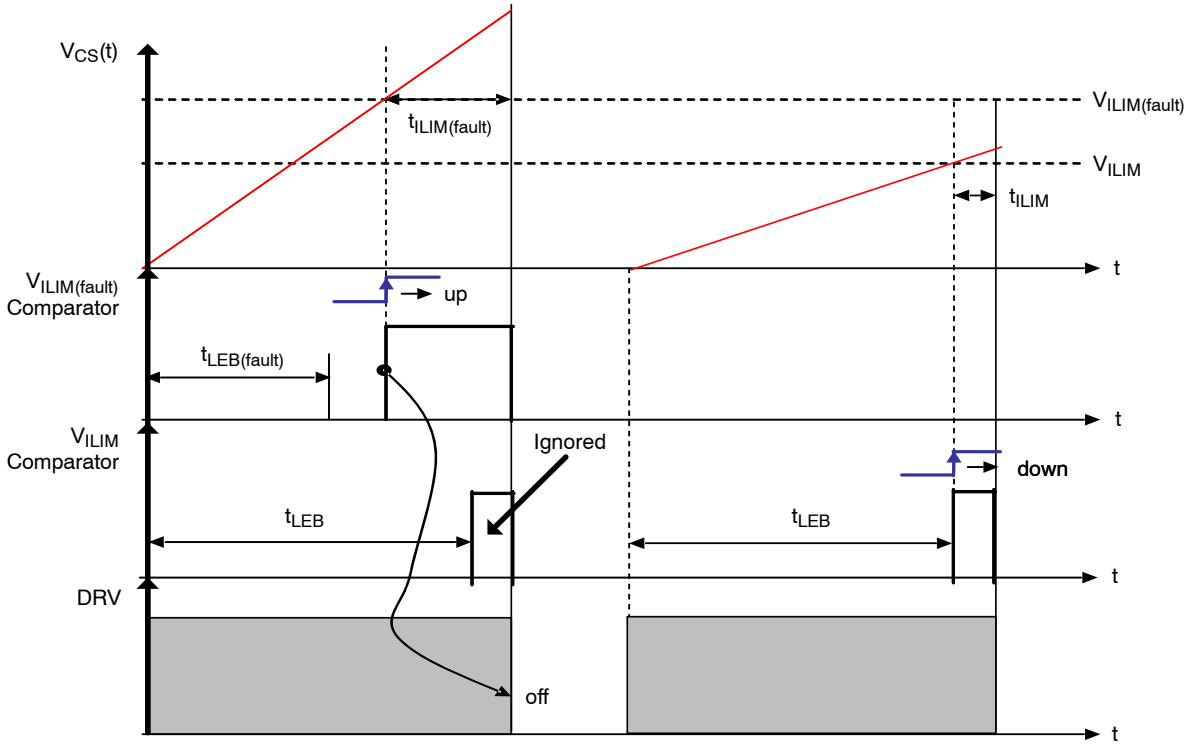


Figure 30. The Overcurrent Comparator Increments the Counter during a Fault

Minimum Dimming Duty Cycle

During each DIM cycle if the max on time limit is reached a certain number of times, the current comparator must be triggered the same number of times to reset the fault counter. For each DIM cycle, if the maximum on time limit is reached a greater number of times than the number of times the current comparator is triggered, the fault counter is not reset and is incremented each DIM cycle until the fault count is reached (Nfault = 8). This results in a minimum dimming duty cycle for a particular LED string voltage and inductor combination. The minimum dimming duty cycle is described in Figure 31 shown below. The first DRV pulse during the dimming duty cycle reaches the maximum on time, but the second DRV pulse does not and is turned off by the current comparator. If the dimming on time (duty cycle) is reduced, the second DRV pulse is turned off by the DIM pin voltage, the current comparator is not triggered, and the NCL30105 latches after 8 dimming cycles.

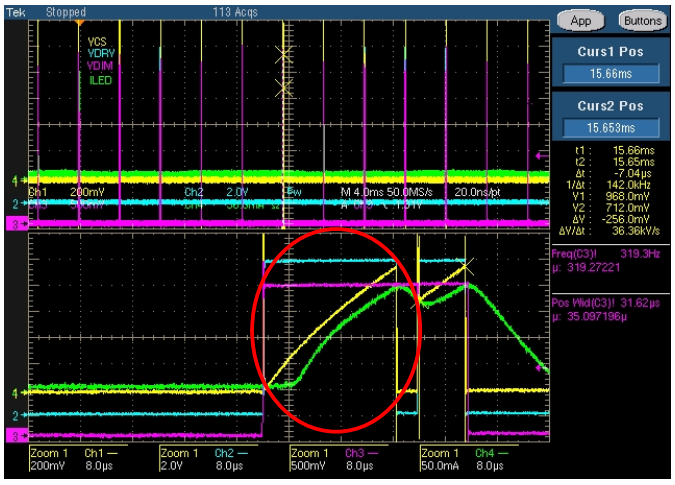


Figure 31. Minimum Dimming Duty Cycle

Example Calculation

The design begins with the system requirements. The following are the system requirements of an example system:

Input Voltage (Vin) = 80 V

Number of LEDs = 18

LED forward Voltage = 3.33 V

LED string Voltage (V_{LED}) = 60 V

LED average current (I_{LED}) = 350 mA

LED ripple current (ΔI_{LED}) = 150 mA (±75 mA)

Operating frequency = 100 kHz

The switching period is calculated using the target operating frequency:

$$T_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 1)}$$

$$T_{SW} = \frac{1}{100k} = 10\ \mu s$$

The off time (t_{off}) is calculated using the LED string voltage, input voltage, and switching period:

$$t_{off} = \left(1 - \frac{V_{LED}}{V_{in}}\right) \cdot T_{SW} \quad \text{(eq. 2)}$$

$$t_{off} = \left(1 - \frac{60}{80}\right) \cdot 10\ \mu s = 2.5\ \mu s$$

To set toff, the following calculation is used based on the on the approximation of the linear region of the t_{off} vs. R_{toff} transfer function as shown in Figure 17:

$$R_{toff}\ [k\Omega] = \frac{t_{off}\ [\mu s] - 0.1214}{0.1864}$$

Where t_{off} is entered in μs and R_{toff} is calculated in kΩ.

$$R_{toff} = \frac{2.5 - 0.1214}{0.1864} = 12.76\ k\Omega$$

R_{toff} is selected as 12.7 kΩ.

The inductor value is calculated using the off time:

$$L = \frac{V_{LED} \cdot t_{off}}{dILED} \quad \text{(eq. 3)}$$

$$L = \frac{60 \cdot 2.5\ \mu}{150m} = 1\ mH$$

The LED peak current ($I_{LED(peak)}$) is also the inductor peak current and is calculated using the average LED current and the LED ripple current:

$$I_{LED(peak)} = I_{LED} + \frac{dILED}{2} \quad \text{(eq. 4)}$$

$$I_{LED(peak)} = 350m + \frac{150m}{2} = 425\ mA$$

It is critical that the inductor saturation current is greater than the peak current. Sufficient margin is generally set to 20%. For 20% margin, the inductor should be selected to have a saturation current greater than 510 mA. The sense resistor (R_{sense}) value is calculated using the peak current:

$$R_{sense} = \frac{V_{ILIM}}{I_{LED(peak)}} \quad \text{(eq. 5)}$$

$$R_{sense} = \frac{1}{0.425} = 2.35\ \Omega$$

Typical Application Schematic:

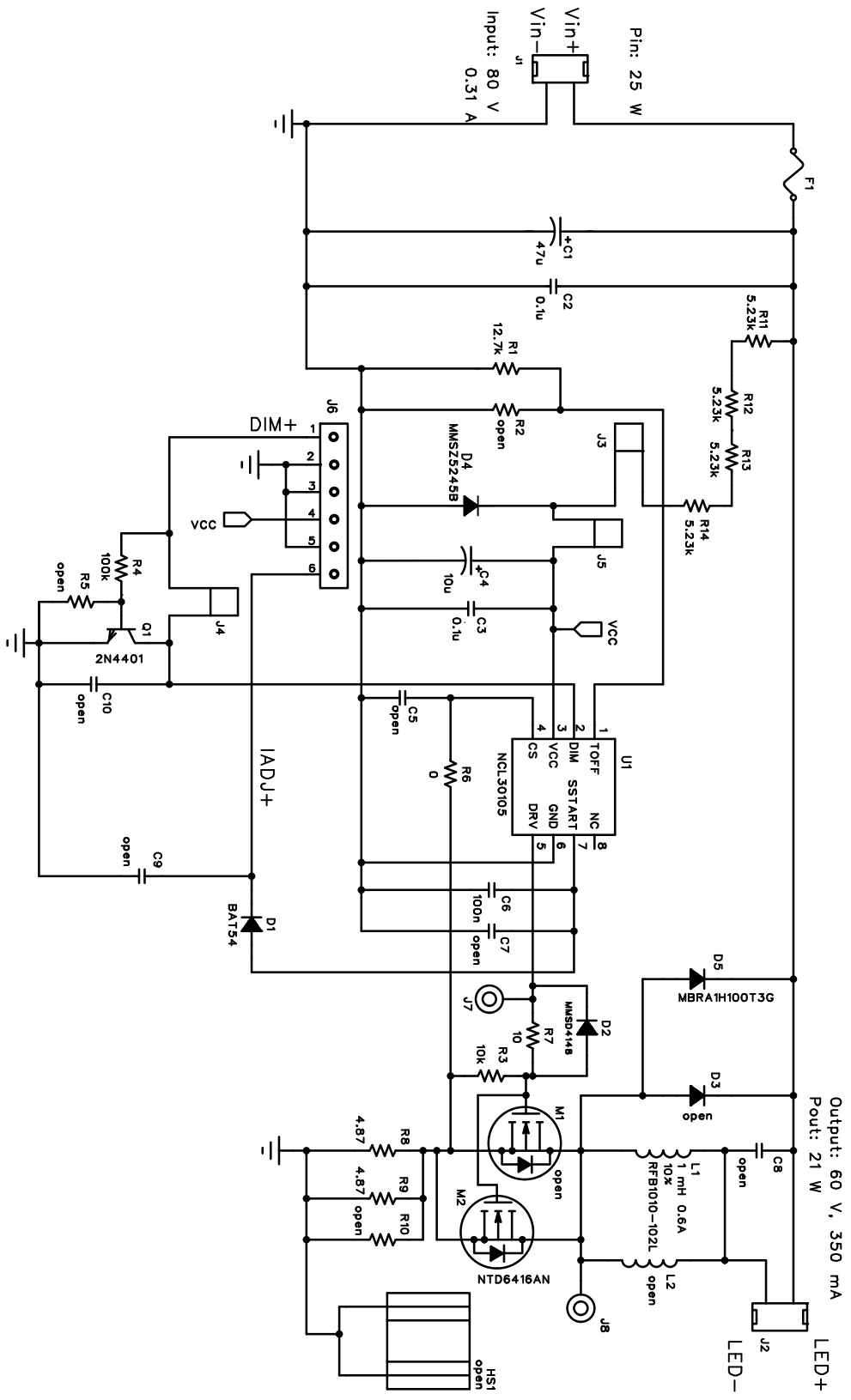


Figure 32. Typical Application Schematic

Thermal Considerations:

The designer must ensure that the junction temperature of the NCL30105 remains less than the value of the maximum operating junction temperature in the Maximum Ratings Table for the worst−case operating conditions. The maximum junction temperature is calculated using the estimated current consumption. The estimated current consumption is calculated using the following assumptions:

1. The switching frequency is at the maximum of 500 kHz ($f_{SW(MAX)}$).
2. The Vcc is at the maximum of 22 V ($V_{CC(MAX)}$)
3. The gate of the MOSFET is modeled using a 1 nF capacitor (C_g)
4. The non−switching bias current is at the maximum of 1.56 mA (I_{CC2})

Using these assumptions, the current consumption is calculated:

$$I_{CC(TJMAX)} = \left(C_g \cdot V_{CC} \cdot f_{SW(MAX)}\right) + I_{CC2}$$

$$I_{CC(TJMAX)} = (1\ n \cdot 22 \cdot 500\ k) + 1.56\ m = 12.56\ mA$$

The power dissipation of the NCL30105 is calculated:

$$P_{(TJMAX)} = I_{CC(TJMAX)} \cdot V_{CC(MAX)}$$

$$P_{(TJMAX)} = 12.56\ m \cdot 22 = 276\ mW$$

The junction temperature is calculated using the maximum thermal resistance ($R_{\theta JA(MAX)}$) with the minimum PCB copper area from the maximum ratings table:

$$T_{J(rise)} = P_{(TJMAX)} \cdot R_{\theta JA(MAX)}$$

$$T_{J(rise)} = 0.276 \cdot 178 = 40°C$$

Assuming a maximum ambient temperature of 70°C ($T_{ambient}$), the maximum junction temperature is calculated:

$$T_{J(MAX)} = T_{J(rise)} + T_{ambient}$$

$$T_{J(MAX)} = 49 + 70 = 119°C$$

Since this is less than the T_{SHDN} parameter with sufficient margin, the design is acceptable.

Layout Tips:

Careful layout is critical for all switch−mode power supply design. Successful layout includes special consideration for noise sensitive pins of the controller IC. For the NCL30105 the following pins should be carefully routed:

1. **Vcc:** This pin requires a ceramic decoupling capacitor (typically 100 nF) and a electrolytic capacitor (typically 10 μF) to ensure that IC supply is constant and decoupled from high frequency noise generated by switching currents.
2. **toff:** This pin requires a resistor connected to ground to set the off time. It is not recommended to leave this pin open or shorted to ground to set the off time. The connection from the toff pin to the resistor and from the resistor to ground must be made as short as possible and connected directly to the NCL30105 GND pin. High noise nodes and traces must be routed as far away from this pin as possible.
3. **SSTART:** A capacitor is connected to this pin to set the Soft−Start time. The connection from the SSTART pin to the capacitor and from the capacitor to ground must be made as short as possible.
4. **DIM:** A decoupling capacitor may need to be connected to this pin if it coupled to high noise traces. The connection from the DIM pin to the capacitor and from the capacitor to ground must be made as short as possible. The addition of the capacitor may affect the response of time of the DIM signal to the DRV output.
5. **CS:** If LEB period is not long enough to ensure predictable operation, a small RC filter may need to be connected to this pin. The addition of the RC filter affects the current set point accuracy.
6. **DRV:** The trace that connects the DRV pin to the MOSFET must be made as short as possible to reduce the parasitic inductance of the trace. The DRV pin switches high currents and the parasitic inductance can cause higher than expected voltages to be applied to the gate of the MOSFET. A small resistor is recommended to be connected in series with the DRV pin to the gate. The resistor reduces the effect of the parasitic inductance. The addition of the resistor may affect the switching losses of the MOSFET.

Recommended Layout:

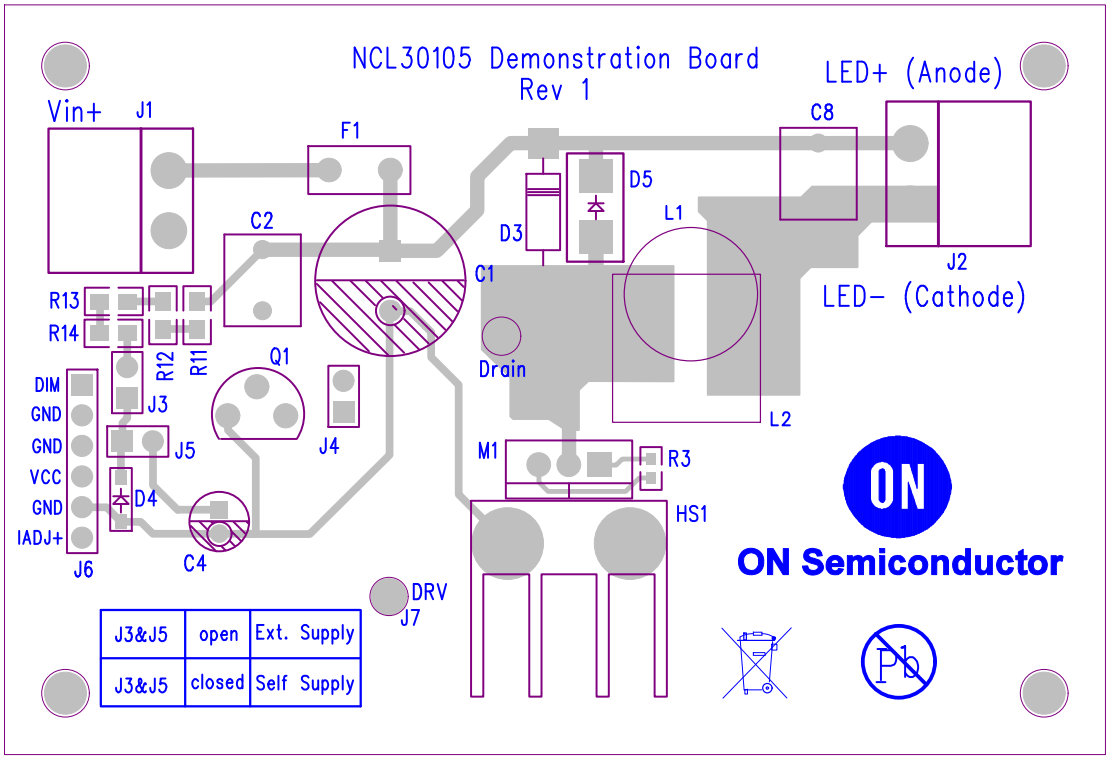


Figure 33. Top Layout

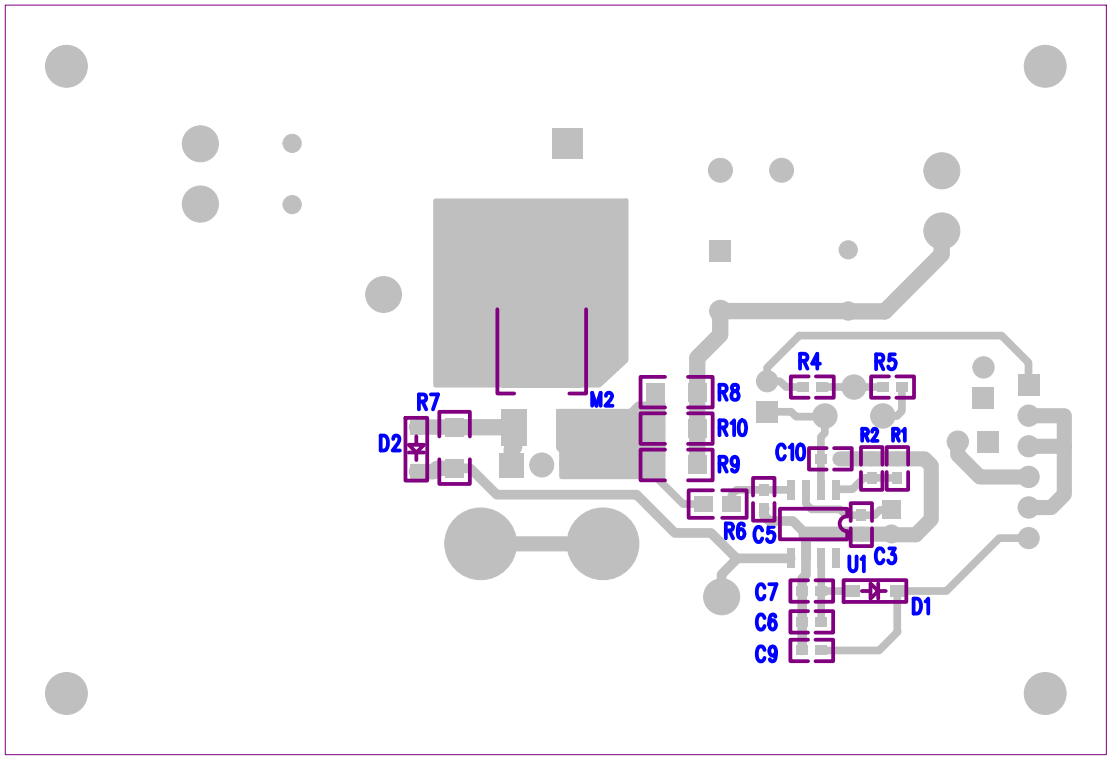


Figure 34. Bottom Layout

The critical components for layout are the following:

1. **R2 (R_{toff}):** This resistor sets the off time. The placement of this resistor is such that the distance to the pin and IC ground is minimized. The footprints R1 and R3 are optional to increase the precision of the resistance value.
2. **C5 (C_{VCC}):** This is the Vcc supply decoupling capacitor. The placement of this capacitor is such that the distance to the pin and IC ground is minimized. The recommended minimum value for this capacitor is 100 nF.
3. **C8 (C_{SSTART}):** This capacitor sets the soft−start time. The placement of this capacitor is such that the distance to the pin and IC ground is minimized.

The layout includes options to use a surface mount inductor (footprint L2) and MOSFET (footprint M2).

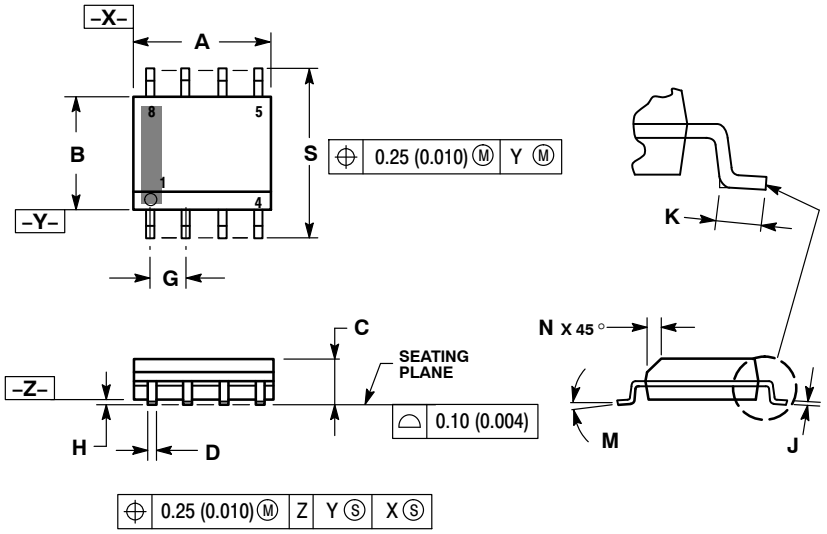
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

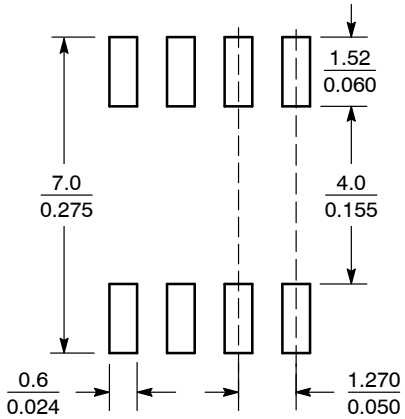
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

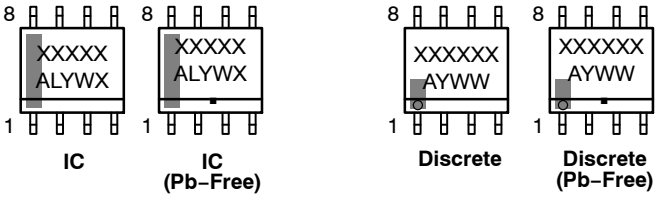
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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