Power Factor Corrected LED Driver Featuring Primary Side CC / CV Control

NCL30388

The NCL30388 is a power factor corrected controller targeting isolated and non−isolated constant current LED drivers. Designed to support flyback, buck−boost and SEPIC topologies, the controller operates in a quasi−resonant mode to provide high efficiency. Due to a novel control method, the device is able to tightly regulate a constant LED current from the primary side and provides near−unity power factor. This removes the need for secondary side feedback circuitry, its biasing and for an optocoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs and also provides a constant voltage regulation of the output if no load is connected to the LED driver.

Features

- High Voltage Startup
- Quasi−resonant Peak Current−mode Control Operation
- Primary Side Feedback
- CC / CV Control
- Tight LED Constant Current Regulation of ±2% Typical
- Digital Power Factor Correction
- Cycle by Cycle Peak Current Limit
- Wide Operating V_{CC} Range
- −40 to + 125°C
- Robust Protection Features
  - Brown−Out
  - OVP on V_{CC}
  - Constant Voltage / LED Open Circuit Protection
  - Winding Short Circuit Protection
  - Secondary Diode Short Protection
  - Output Short Circuit Protection
  - Thermal Shutdown

Typical Applications

- Integral LED Bulbs
- LED Power Driver Supplies
- LED Light Engines

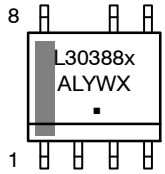
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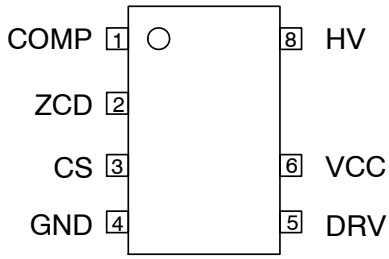
SOIC−7
CASE 751U

MARKING DIAGRAM



L30388	= Specific Device Code
x	= Version
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

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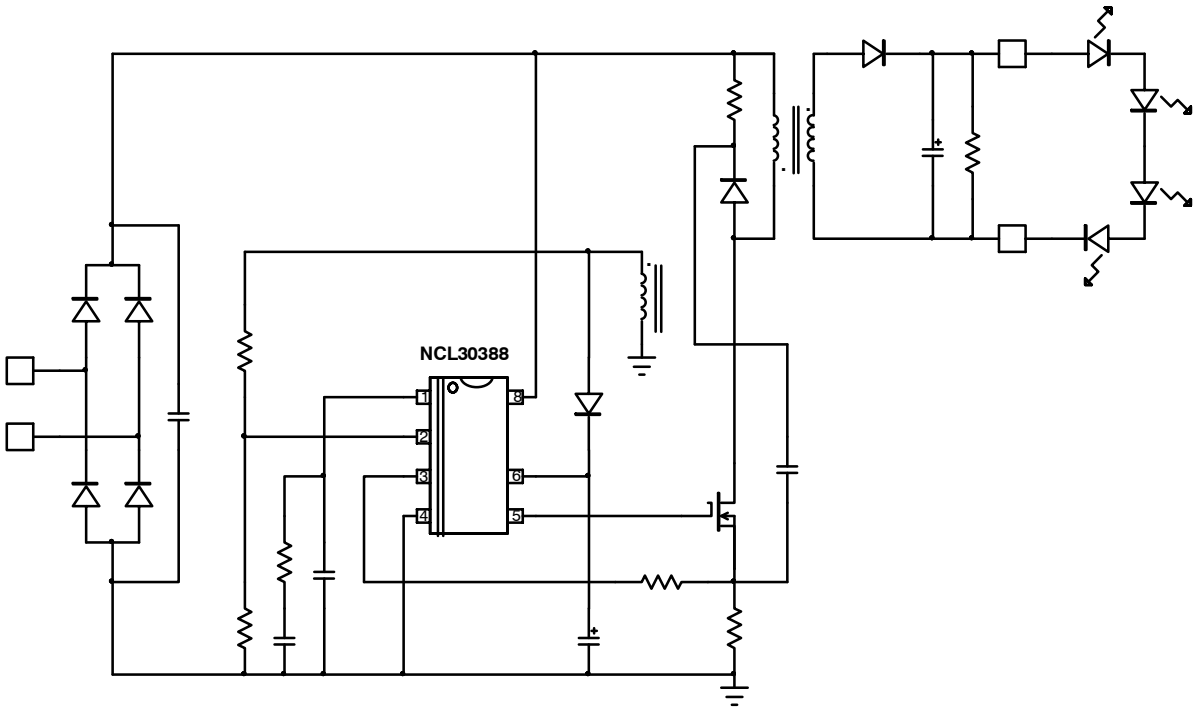


Figure 1. Typical Application Schematic in a Flyback Converter

PIN FUNCTION DESCRIPTION NCL30388

Pin No	Pin Name	Function	Pin Description
1	COMP	OTA output for CV loop	This pin receives a compensation network to stabilize the CV loop
2	ZCD	Zero crossing Detection V_{aux} sensing	This pin connects to the auxiliary winding and is used to detect the core reset event. This pin also senses the auxiliary winding voltage for accurate output voltage control
3	CS	Current sense	This pin monitors the primary peak current.
4	GND	–	The controller ground
5	DRV	Driver output	The driver's output to an external MOSFET
6	VCC	Supplies the controller	This pin is connected to an external auxiliary voltage.
8	HV	High Voltage sensing	This pin connects after the diode bridge to provide the startup current and internal high voltage sensing function.

INTERNAL CIRCUIT ARCHITECTURE

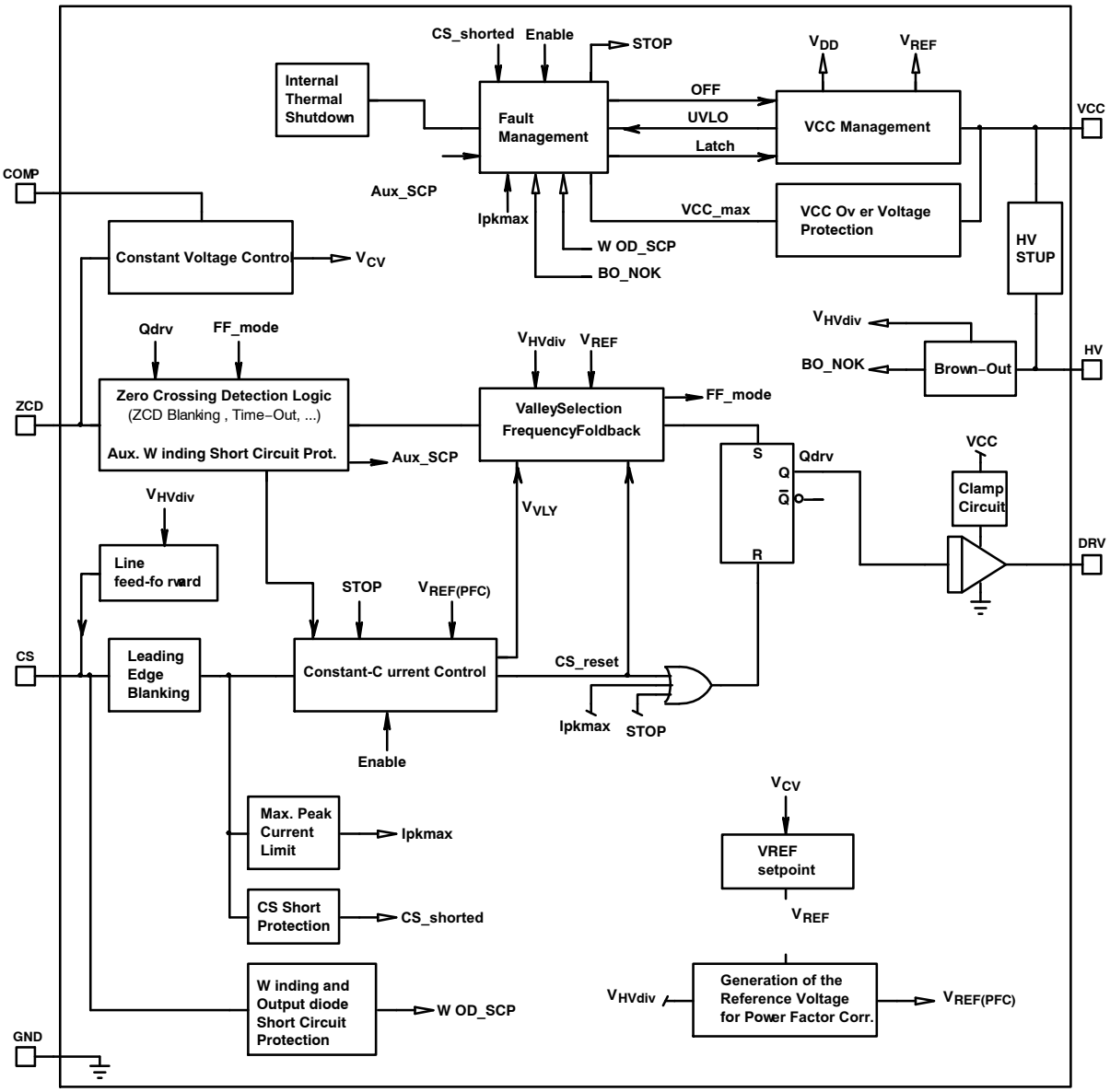


Figure 2. Internal Circuit Architecture NCL30388

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
$V_{CC(MAX)}$ $I_{CC(MAX)}$	Maximum Power Supply voltage, VCC pin, continuous voltage Maximum current for VCC pin	−0.3 to 30 Internally limited	V mA
$V_{DRV(MAX)}$ $I_{DRV(MAX)}$	Maximum driver pin voltage, DRV pin, continuous voltage Maximum current for DRV pin	−0.3, V_{DRV} (Note 1) −300, +500	V mA
$V_{HV(MAX)}$ $I_{HV(MAX)}$	Maximum voltage on HV pin Maximum current for HV pin (dc current self−limited if operated within the allowed range)	−0.3, +700 ±20	V mA
V_{MAX} I_{MAX}	Maximum voltage on low power pins (except pins HV, DRV and VCC) Current range for low power pins (except pins HV, DRV and VCC)	−0.3, 5.5 (Notes 2 and 6) −2, +5	V mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	180	°C/W
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
	Operating Temperature Range	−40 to +125	°C
	Storage Temperature Range	−65 to +150	°C
	ESD Capability, HBM model (Note 3)	2	kV
	ESD Capability, MM model (Note 3)	300	V
	ESD Capability, CDM model (Note 3)	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DRV} is the DRV clamp voltage $V_{DRV(high)}$ when V_{CC} is higher than $V_{DRV(high)}$. V_{DRV} is V_{CC} otherwise.
2. This level is low enough to guarantee not to exceed the internal ESD diode and 5.5 V ZENER diode. More positive and negative voltages can be applied if the pin current stays within the −2 mA / 5 mA range.
3. This device series contains ESD protection and exceeds the following tests: Human Body Model 2000 V per Mil−Std−883, Method 3015. Charged Device Model 2000 V per JEDEC Standard JESD22−C101D
4. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, , V_{CS} = 0 V) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE SECTION						
High voltage current source	V_{CC} = $V_{CC(on)}$ − 200 mV	$I_{HV(start2)}$	3.3	4.7	6.1	mA
High voltage current source	V_{CC} = 0 V	$I_{HV(start1)}$		300		μA
V_{CC} level for $I_{HV(start1)}$ to $I_{HV(start2)}$ transition		$V_{CC(TH)}$		2		V
Minimum startup voltage	V_{CC} = 0 V	$V_{HV(MIN)}$	–	17	–	V
HV source leakage current	V_{HV} = 450 V	$I_{HV(leak)}$		4.5	10	μA
Maximum rms input voltage for correct operation of the PFC loop (T_J = −20°C to 125°C)		$V_{HV(OL)}$	265			Vrms
SUPPLY SECTION						
Supply Voltage Startup Threshold Threshold for turning off DSS (Note 5) Minimum Operating Voltage Hysteresis $V_{CC(on)}$ − $V_{CC(off)}$ Internal logic reset	 V_{CC} increasing V_{CC} increasing V_{CC} decreasing V_{CC} decreasing	 $V_{CC(on)}$ $V_{CC(on2)}$ $V_{CC(off)}$ $V_{CC(HYS)}$ $V_{CC(reset)}$	 16 9.77 8.2 7.8 4	 18 10.50 8.8 – 5	 20 11.24 9.4 – 6	V
Over Voltage Protection V_{CC} OVP threshold		$V_{CC(OVP)}$	25.0	26.5	28	V
$V_{CC(off)}$ noise filter (Note 6) $V_{CC(reset)}$ noise filter− (Note 6)		$t_{VCC(off)}$ $t_{VCC(reset)}$	– –	5 20	– –	μs
Supply Current Device Disabled/Fault Device Enabled/No output load on pin 5 Device Switching (F_{sw} = 65 kHz) Device switching (F_{sw} = 15 kHz)	 V_{CC} > $V_{CC(off)}$ F_{sw} = 65 kHz C_{DRV} = 470 pF, F_{sw} = 65 kHz V_{REFX} = 10%of max value	 I_{CC1} I_{CC2} I_{CC3} I_{CC4}	 1.2 – – –	 1.5 3.0 3.3 2.9	 1.8 3.5 4.0 3.4	mA

5. Refer to ordering table option at the end of the document
6. Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, , V_{CS} = 0 V) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Maximum Internal current limit		V_{ILIM}	1.31	1.38	1.45	V
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	270	330	390	ns
Propagation delay from current detection to gate off−state		t_{ILIM}	–	100	150	ns
Maximum on−time (option B)		$t_{on(MAX)}$	29	39	49	μs
Maximum on−time (option A)		$t_{on(MAX2)}$	16	20	24	μs
Threshold for immediate fault protection activation (140% of V_{ILIM})		$V_{CS(stop)}$	1.91	1.99	2.07	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	–	170	–	ns
Current source for CS to GND short detection		$I_{CS(short)}$	400	500	600	μA
Current sense threshold for CS to GND short detection	V_{CS} rising	$V_{CS(low)}$	20	60	100	mV
GATE DRIVE						
Drive Resistance DRV Sink DRV Source		 R_{SNK} R_{SRC}	 – –	 13 30	 – –	Ω
Drive current capability DRV Sink (Note GBD) DRV Source (Note GBD)		 I_{SNK} I_{SRC}	 – –	 500 300	 – –	mA
Rise Time (10 % to 90 %)	C_{DRV} = 470 pF	t_r	–	30	–	ns
Fall Time (90 % to 10 %)	C_{DRV} = 470 pF	t_f	–	20	–	ns
DRV Low Voltage	V_{CC} = $V_{CC(off)}$+0.2 V C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(low)}$	8	–	–	V
DRV High Voltage	V_{CC} = $V_{CC(MAX)}$ C_{DRV} = 470 pF, R_{DRV}=33 kΩ	$V_{DRV(high)}$	10	12	14	V
ZERO VOLTAGE DETECTION CIRCUIT						
Upper ZCD threshold voltage	V_{ZCD} rising	$V_{ZCD(rising)}$	–	90	150	mV
Lower ZCD threshold voltage	V_{ZCD} falling	$V_{ZCD(falling)}$	35	55	–	mV
ZCD hysteresis		$V_{ZCD(HYS)}$	15	–	–	mV
Propagation Delay from valley detection to DRV high	V_{ZCD} decreasing	$t_{ZCD(DEM)}$	–	–	150	ns
Blanking delay after on−time (ZCD blank option B)	V_{REFX} > 0.35 V	$t_{ZCD(blank1)B}$	1.1	1.5	1.9	μs
Blanking Delay at light load (ZCD blank option B)	V_{REFX} < 0.25 V	$t_{ZCD(blank2)B}$	0.6	0.8	1.0	μs
Blanking delay after on−time (ZCD blank option A)	V_{REFX} > 0.35 V	$t_{ZCD(blank1)A}$	0.75	1.0	1.25	μs
Blanking Delay at light load (ZCD blank option A)	V_{REFX} < 0.25 V	$t_{ZCD(blank2)A}$	0.45	0.6	0.75	μs
Timeout after last DEMAG transition		t_{TIMO}	5	6.5	8	μs
Pulling−down resistor	V_{ZCD} = $V_{ZCD(falling)}$	$R_{ZCD(pd)}$		200		kΩ
CONSTANT CURRENT CONTROL						
Reference Voltage at T_J = 25°C to 85°C		V_{REF}	0.326	0.333	0.340	V
Reference Voltage T_J = −40°C to 125°C		V_{REF}	0.323	0.333	0.343	V
Current sense lower threshold for detection of the leakage inductance reset time	V_{CS} falling	$V_{CS(low)}$	20	50	100	mV
Blanking time for leakage inductance reset detection		$t_{CS(low)}$	–	120	–	ns
CONSTANT VOLTAGE SECTION						
Internal voltage reference for constant voltage regulation T_J = 25°C		$V_{REF(CV)}$	2.42	2.48	2.54	V
Internal voltage reference for constant voltage regulation T_J = −40°C to 125°C		$V_{REF(CV)}$	2.38	2.48	2.58	V

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, , V_{CS} = 0 V) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
CONSTANT VOLTAGE SECTION						
CV Error amplifier Gain		G_{EA}	40	50	60	μS
Error amplifier current capability	V_{REFX}=V_{REF}	I_{EA}		±60		μA
COMP pin lower clamp voltage		$V_{CV(clampL)}$		0.6		V
COMP pin higher clamp voltage		$V_{CV(clampH)}$		4.1		V
ZCD pin voltage below which the CV OTA is boosted	$V_{REF(CV)}$* 80%	$V_{boost(CV)}$	1.88	2	2.12	V
Error amplifier current capability during boost phase		$I_{EAboost}$		±140		μA
ZCD slow OVP threshold ($V_{ref(CV)}$*115%)		V_{OVP1}	2.69	2.87	3.04	V
Switching period during slow OVP		$T_{sw(OVP1)}$		1.5		ms
ZCD voltage at which slow OVP is exit ($V_{ref(CV)}$*105%)		$V_{OVP1rst}$		2.625		V
ZCD fast OVP threshold		V_{OVP2}	3.29	3.43	3.57	V
ZCD pin voltage below which the CV OTA is boosted	$V_{REF(CV)}$ * 80%	$V_{boost(CV)}$	1.88	2	2.12	V
LINE FEED FORWARD						
V_{HV} to $I_{CS(offset)}$ conversion ratio		K_{LFF}	0.153	0.185	0.217	μA/V
Offset current maximum value	V_{HV} > 400 V	$I_{offset(MAX)}$	76	95	114	μA
Line feed−forward current	DRV high, V_{HV} = 200 V	I_{FF}	32	37	42	μA
VALLEY LOCKOUT SECTION						
Threshold for line range detection V_{in} increasing	V_{HV} increases	V_{HL}	252	264	276	V
Threshold for line range detection V_{in} decreasing	V_{HV} decreases	V_{LL}	241	253	265	V
Blanking time for line range detection		$t_{HL(blank)}$	15	25	35	ms
Valley thresholds (expressed as a percentage of V_{REF}) 1st to 2nd valley transition at LL and 2nd to 3rd valley HL, V_{REF} decr. 2nd to 1st valley transition at LL and 3rd to 2nd valley HL, V_{REF} incr. 2nd to 3rd valley transition at LL and 3rd to 4th valley HL, V_{REF} decr. 3rd to 2nd valley transition at LL and 4th to 3rd valley HL, V_{REF} incr. 3rd to 4th valley transition at LL and 4th to 5th valley HL, V_{REF} decr. 4th to 3th valley transition at LL and 5th to 4th valley HL, V_{REF} incr. 4th to 5th valley transition at LL and 5th to 6th valley HL, V_{REF} decr. 5th to 4th valley transition at LL and 6th to 5th valley HL, V_{REF} incr.	 V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases V_{REF} decreases V_{REF} increases	 $V_{VLY1-2/2-3}$ $V_{VLY2-1/3-2}$ $V_{VLY2-3/3-4}$ $V_{VLY3-2/4-3}$ $V_{VLY3-4/4-5}$ $V_{VLY4-3/5-4}$ $V_{VLY4-5/5-6}$ $V_{VLY5-4/6-5}$		 80 90 65 75 50 60 35 45		%
V_{REF} value at which the FF mode is activated	V_{REF} decreases	$V_{FFstart}$		25		%
V_{REF} value at which the FF mode is removed	V_{REF} increases	V_{FFstop}		35		%
FREQUENCY FOLDBACK						
Added dead time	V_{REFX} = 25%V_{REF}	t_{FF1LL}	1.4	2.0	2.6	μs
Added dead time	V_{REFX} = 8% V_{REF}	t_{FFchg}	–	40	–	μs
Dead−time clamp (Maximum dead−time option C)	V_{REFX} < 1 mV	t_{FFend}		1.4	–	ms
Dead−time clamp (Maximum dead−time option B)	V_{REFX} < 3 mV	t_{FFend2}	–	687	–	μs
Dead−time clamp (Maximum dead−time option A)	V_{REFX} < 11.2 mV	t_{FFend3}	–	250	–	μs
FAULT PROTECTION						
Thermal Shutdown	Device switching (F_{SW} around 65 kHz)	T_{SHDN}	130	150	170	°C
Thermal Shutdown Hysteresis		$T_{SHDN(HYS)}$	–	50	–	°C
Threshold voltage for output short circuit or aux. winding short circuit detection		$V_{ZCD(short)}$	0.8	1.0	1.2	V
Short circuit detection Timer	V_{ZCD} < $V_{ZCD(short)}$	t_{OVLD}	70	90	110	ms
Auto−recovery Timer		$t_{recovery}$	3	4	5	s

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted: For typical values T_J = 25°C, V_{CC} = 12 V, V_{ZCD} = 0 V, , V_{CS} = 0 V) For min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V)

Description	Test Condition	Symbol	Min	Typ	Max	Unit
BROWN−OUT AND LINE SENSING						
Brown−Out ON level (IC start pulsing)	V_{HV} increasing	$V_{HVBO(on)}$	104	110	116	V
Brown−Out OFF level (IC stops pulsing)	V_{HV} decreasing	$V_{HVBO(off)}$	93	99	105	V
BO comparators delay		$t_{BO(delay)}$		30		μs
Brown−Out blanking time		$t_{BO(blank)}$	15	25	35	ms
HV pin voltage above which the sampling of ZCD is enabled	V_{HV} decreasing	V_{sampEN}		55		V
Sampling Enable comparator hysteresis	V_{HV} increasing	$V_{sampHYS}$		5		V

TYPICAL CHARACTERISTICS

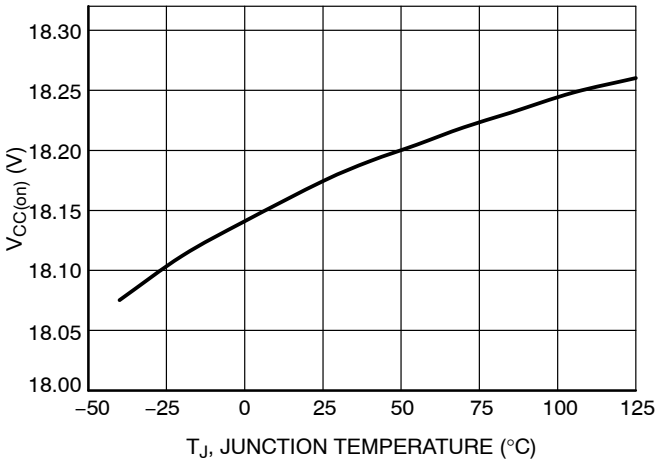


Figure 3. $V_{CC(on)}$ vs. Junction Temperature

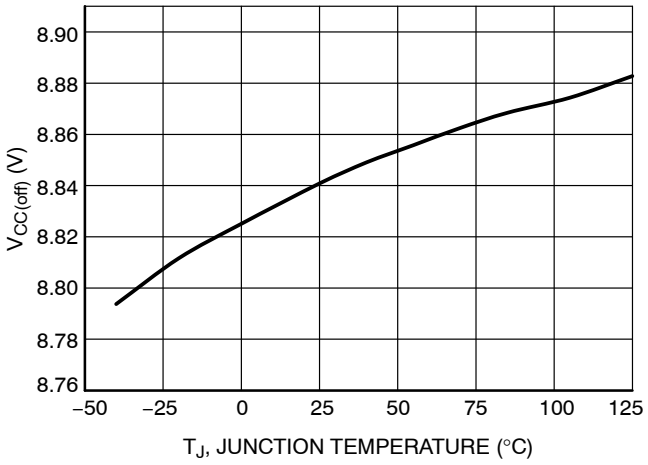


Figure 4. $V_{CC(off)}$ vs. Junction Temperature

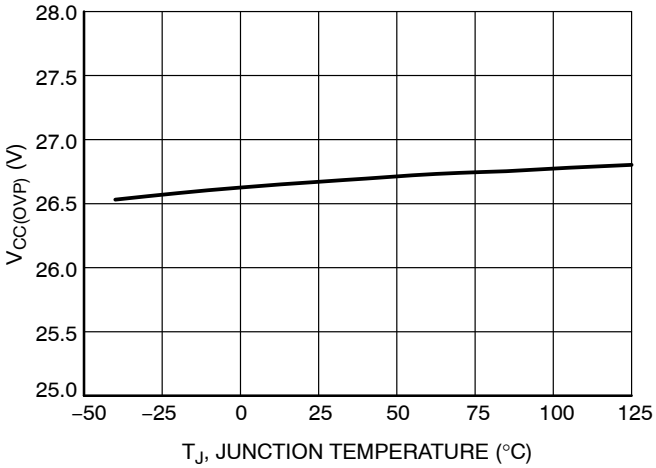


Figure 5. $V_{CC(OVP)}$ vs. Junction Temperature

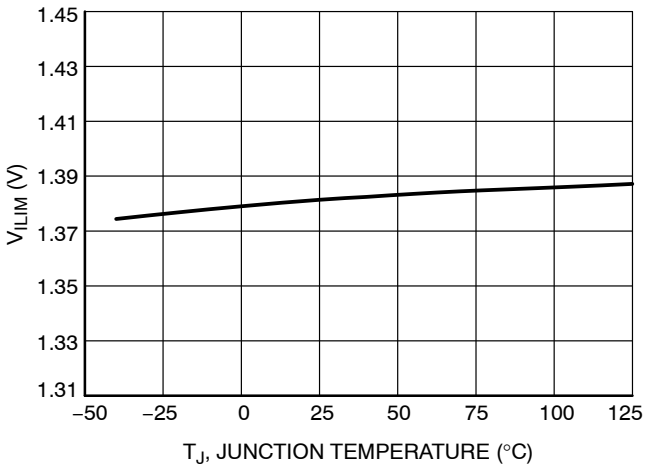


Figure 6. V_{ILIM} vs. Junction Temperature

TYPICAL CHARACTERISTICS

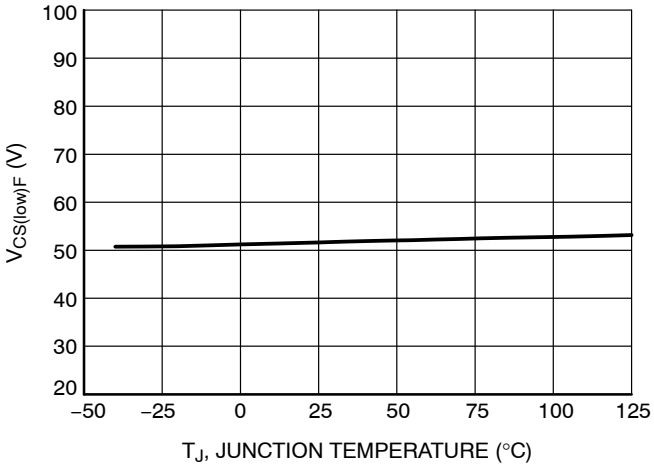


Figure 7. $V_{CS(low)F}$ vs. Junction Temperature

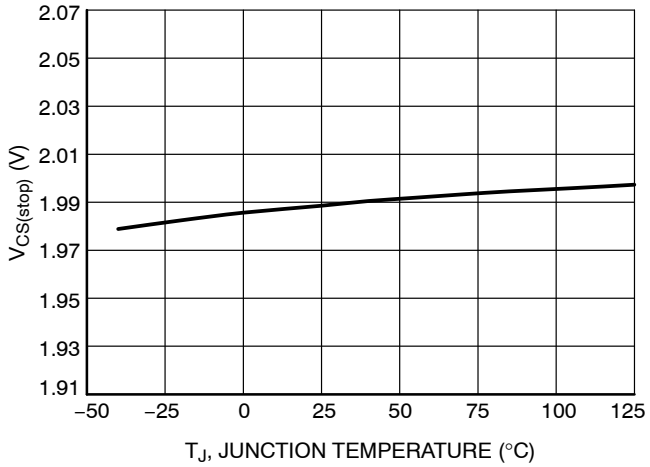


Figure 8. $V_{CS(stop)}$ vs. Junction Temperature

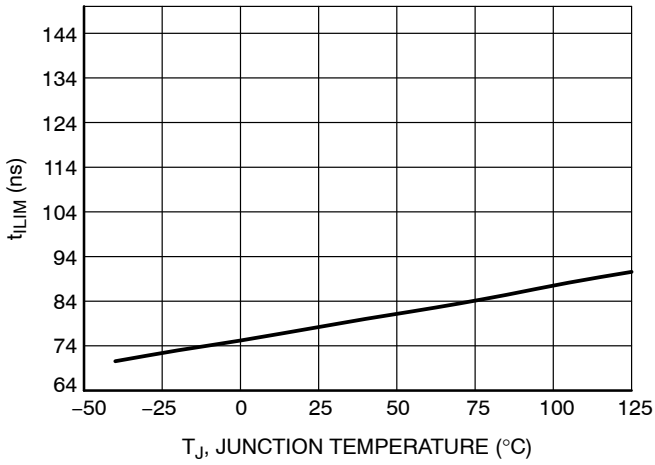


Figure 9. t_{ILIM} vs. Junction Temperature

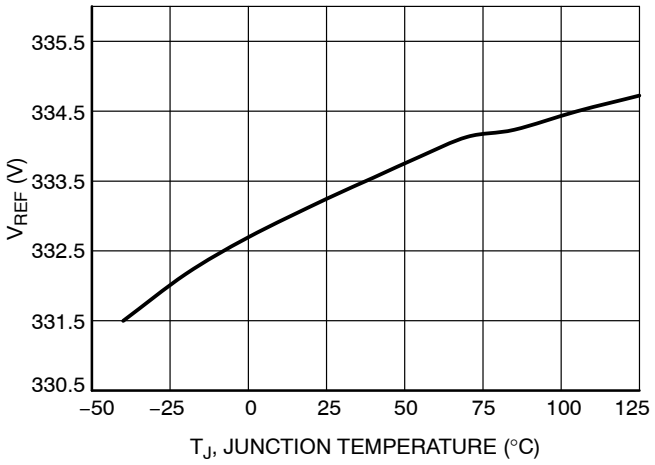


Figure 10. V_{REF} vs. Junction Temperature

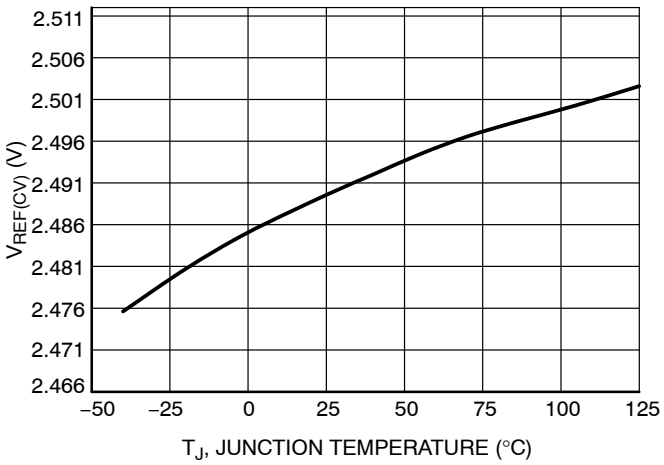


Figure 11. $V_{REF(CV)}$ vs. Junction Temperature

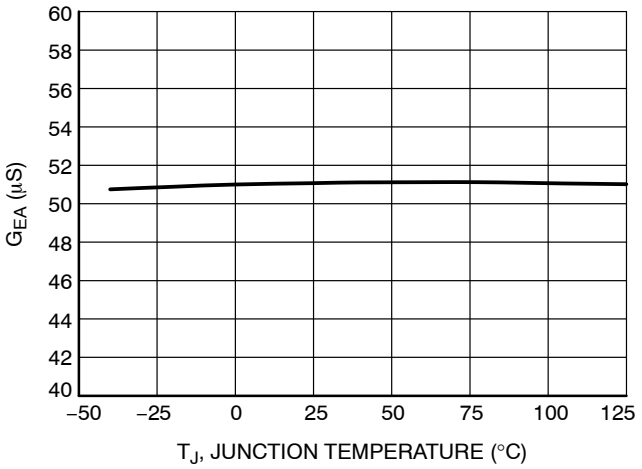


Figure 12. G_{EA} vs. Junction Temperature

TYPICAL CHARACTERISTICS

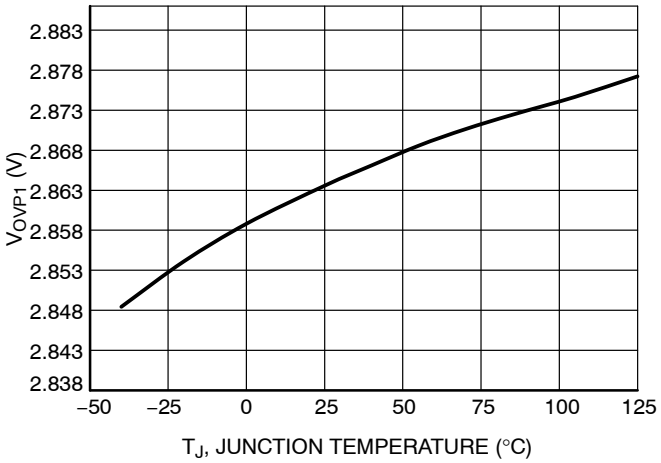


Figure 13. V_{OVP1} vs. Junction Temperature

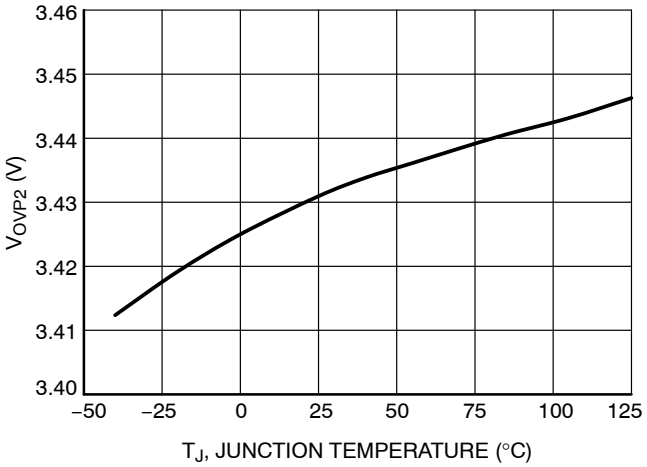


Figure 14. V_{OVP2} vs. Junction Temperature

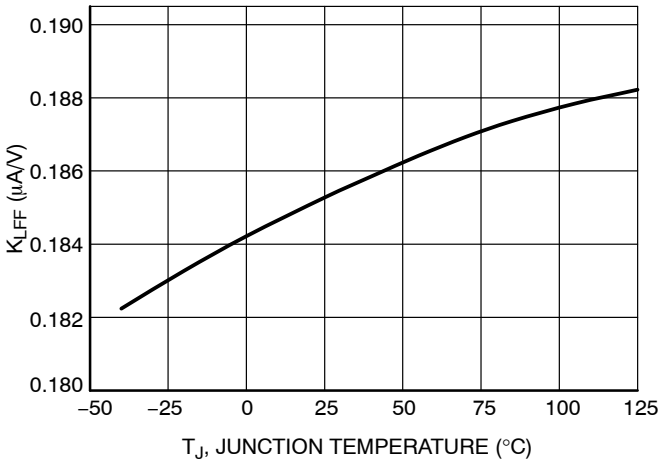


Figure 15. K_{LFF} vs. Junction Temperature

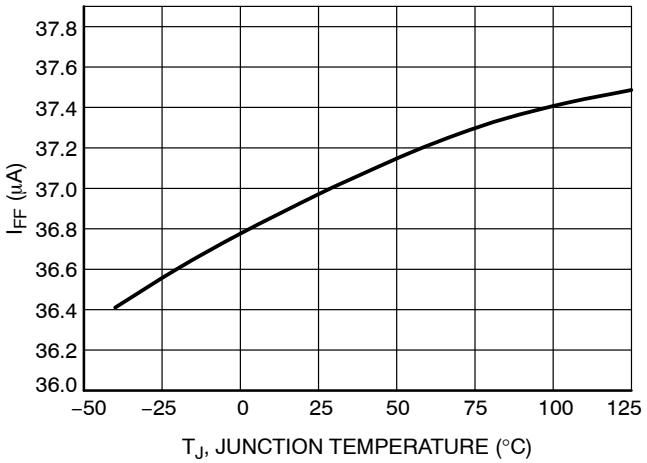


Figure 16. I_{FF} vs. Junction Temperature

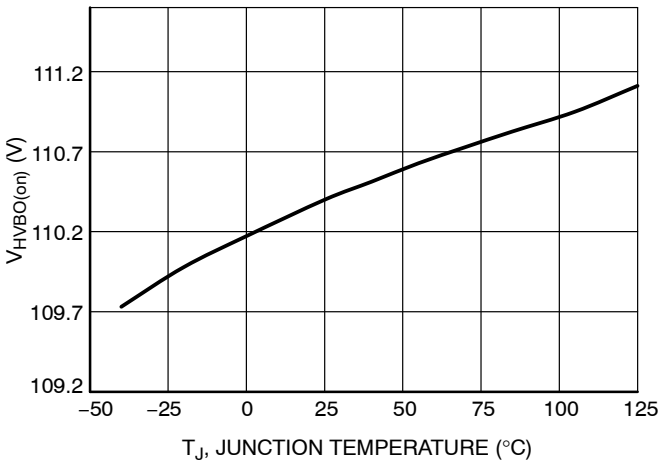


Figure 17. $V_{HVBO(on)}$ vs. Junction Temperature

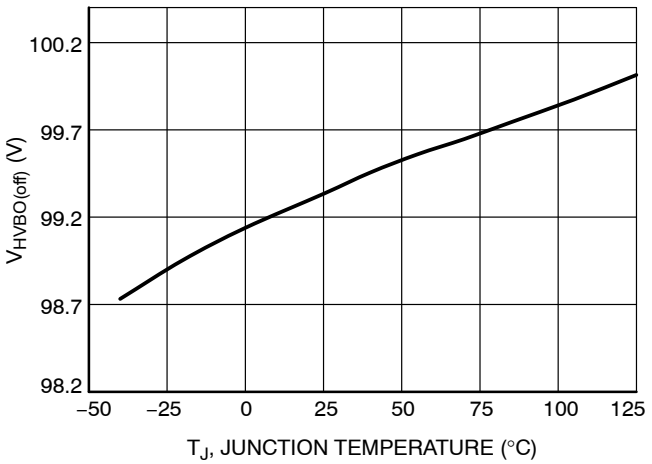


Figure 18. $V_{HVBO(off)}$ vs. Junction Temperature

APPLICATION INFORMATION

The NCL30388 implements a current−mode architecture operating in quasi−resonant mode. Due to proprietary circuitry, the controller is able to accurately regulate the secondary side current and voltage of the fly−back converter without using any opto−coupler or measuring directly the secondary side current or voltage.

The controller provides near unity power factor correction.

- Quasi−Resonance Current−Mode Operation: implementing quasi−resonance operation in peak current−mode control, the NCL30388 optimizes the efficiency by switching in the valley of the MOSFET drain−source voltage. Due to an internal algorithm control, the controller locks−out in a selected valley and remains locked until the input voltage or the output current set point significantly changes.
- Primary Side Constant Current Control: thanks to a proprietary circuit, the controller is able to take into account the effect of the leakage inductance of the transformer and allows an accurate control of the secondary side current regardless of the input voltage and output load variation
- Primary Side Constant Voltage Regulation: By monitoring the auxiliary winding voltage, it is possible to regulate accurately the output voltage. The output voltage regulation is typically within ±2%.
- Load Transient Compensation: Since PFC has low loop bandwidth, abrupt changes in the load may cause excessive over or under−shoot. The slow Over Voltage Protection contains the output voltage when it tends to become excessive. In addition, the NCL30388 speeds up the constant voltage regulation loop when the output voltage goes below 80% of its regulation level.
- Power Factor Correction: A proprietary concept allows achieving high power factor correction and low THD while keeping accurate constant current and constant voltage control.
- Line Feed−forward: allows compensating the variation of the output current caused by the propagation delay.
- V_{CC} Over Voltage Protection: if the V_{CC} pin voltage exceeds an internal limit, the controller shuts down and waits 4 seconds before restarting pulsing.
- Fast Over Voltage Protection: If the voltage of ZCD pin exceeds 130% of its regulation level, the controller shuts dwon and waits 4 s before trying to restart.
- Brown−Out: the controller includes a brown−out circuit which safely stops the controller in case the input voltage is too low. The device will automatically restart if the line recovers.
- Cycle−by−cycle peak current limit: when the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.
- Winding Short−Circuit Protection: an additional comparator senses the CS signal and stops the controller if V_{CS} reaches 1.4 x V_{ILIM} (after a reduced LEB of t_{BCS}). This additional comparator is enabled only during the main LEB duration t_{LEB}, for noise immunity reason.
- Output Under Voltage Protection: If a too low voltage is applied on ZCD pin for 90−ms time interval, the controllers assume that the output or the ZCD pin is shorted to ground and shutdown. After waiting 4 seconds, the IC restarts switching.
- Thermal Shutdown: an internal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C.

POWER FACTOR AND CONSTANT CURRENT CONTROL

The NCL30388 embeds an analog/digital block to control the power factor and regulate the output current by monitoring the ZCD, CS and HV pin voltages (signals V_{ZCD}, V_{HV_DIV}, V_{CS}). This circuit generates the current setpoint V_{CTRL_DIV} and compares it to the current sense signal to turn the MOSFET off. The HV pin provides the sinusoidal reference necessary for shaping the input current. The obtained current reference is further modulated so that when averaged over a half line period, it is equal to the output current reference (V_{REFX}). The modulation and averaging process is made internally by a digital circuit. If the HV pin properly conveys the sinusoidal shape, power factor will be close to 1. Also, the Total Harmonic Distortion (THD) will be low especially if the output voltage ripple is small.

The output current will be well regulated, following the equation below:

$$I_{OUT} = \frac{V_{REFX}}{2N_{sp}R_{sense}} \quad \text{(eq. 1)}$$

Where:

- N_{sp} is the secondary to primary transformer turns ratio: $N_{sp} = N_S / N_P$.
- R_{sense} is the current sense resistor
- V_{REFX} is the output current reference: $V_{REFX} = V_{REF}$ if $V_{COMP} \geq 4$ V

The output current reference (V_{REFX}) is V_{REF} unless the constant voltage mode is activated.

CONSTANT VOLTAGE CONTROL

The auxiliary winding voltage is sampled internally through the ZCD pin.

A precise internal voltage reference $V_{REF(CV)}$ sets the voltage target for the CV loop.

The sampled voltage is applied to the negative input of the CV OTA and compared to V_{REFCV}.

A type 2 compensator is needed at the CV OTA output to stabilize the loop. The COMP pin voltage modify the the output current internal reference in order to regulate the output voltage.

When $V_{COMP} \geq 4$ V, $V_{REFX} = V_{REF}$.

When $V_{COMP} < 0.6$ V, $V_{REFX} = 0$ V

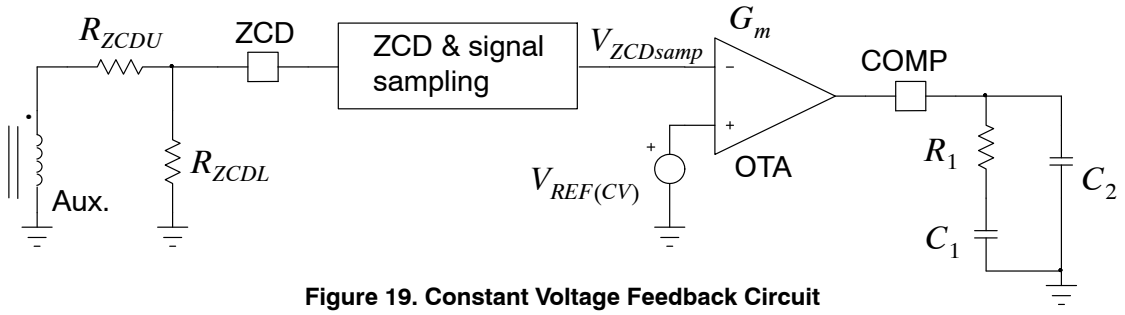


Figure 19. Constant Voltage Feedback Circuit

STARTUP PHASE (HV STARTUP)

It is generally requested that the LED driver starts to emit light in less than 1 s and possibly within 300 ms. It is challenging since the start−up consists of the time to charge the V_{CC} capacitor and that necessary to charge the output capacitor until sufficient current flows into the LED string. This second phase can be particularly long in dimming cases where the secondary current is a portion of the nominal one.

The NCL30388 features a high voltage startup circuit that allows charging VCC capacitor very fast.

When the power supply is first connected to the mains outlet, the internal current source is biased and charges up the V_{CC} capacitor. When the voltage on this V_{CC} capacitor reaches the $V_{CC(on)}$ level, the current source turns off. At this time, the controller is only supplied by the V_{CC} capacitor, and the auxiliary supply should take over before V_{CC} collapses below $V_{CC(off)}$.

The HV startup circuitry is made of two startup current levels, $I_{HV(start1)}$ and $I_{HV(start1)}$. This helps to protect the controller against short−circuit between V_{CC} and GND. At power−up, as long as V_{CC} is below $V_{CC(TH)}$, the source delivers $I_{HV(start1)}$ (around 300 μA typical). Then, when V_{CC} reaches $V_{CC(TH)}$, the source smoothly transitions to $I_{HV(start2)}$ and delivers its nominal value.

To speed−up the output voltage rise, the following is implemented:

- The digital OTA output is increased until $V_{REF(PFC)}$ signal reaches V_{REFX}. Again, this is to speed−up the control signal rise to their steady state value.
- At the beginning of each operating phase of a V_{CC} cycle, the digital OTA output is set to 0. Actually, the digital OTA output is set to 0 in the case of a cold start−up or in the case of a start−up sequence following an operation interruption due to a fault. On the other hand, if the V_{CC} hiccups just because the system fails to start−up in one V_{CC} cycle (DSS option not activated), the digital OTA output is not reset to ease the second (or more) attempt.
- If the load is shorted, the circuit will operate in hiccup mode with V_{CC} oscillating between $V_{CC(off)}$ and $V_{CC(on)}$ until the output under voltage protection (UVP) trips. UVP is triggered if the ZCD pin voltage does not exceed 1 V within a 90 ms operation of time. This indicates that the ZCD pin is shorted to ground or that an excessive load prevents the output voltage from rising.

CYCLE−BY−CYCLE CURRENT LIMIT

When the current sense voltage exceeds the internal threshold V_{ILIM}, the MOSFET is turned off for the rest of the switching cycle.

WINDING AND OUTPUT DIODE SHORT−CIRCUIT PROTECTION

In parallel to the cycle−by−cycle sensing of the CS pin, another comparator with a reduced LEB (t_{BCS}) and a threshold of ($V_{CS(stop)}$ = 140% *V_{ILIM}) monitors the CS pin to detect a winding or an output diode short circuit. The controller shuts down if it detects four consecutive pulses during which the CS pin voltage exceeds $V_{CS(stop)}$.

The controller goes into auto−recovery mode.

VALLEY LOCKOUT

Quasi−Square wave resonant systems have a wide switching frequency excursion. The switching frequency increases when the output load decreases or when the input voltage increases. The switching frequency of such systems must be limited.

The NCL30388 changes valley as V_{REFX} decreases and as the input voltage increases and as the output current setpoint is varied during dimming. This limits the frequency excursion.

By default, when the output current is not dimmed, the controller operates in the first valley at low line and in the second valley at high line.

REFX value at which the controller changes valley (I_{out} decreasing)	HV pin voltage for valley change		V_{REFX} value at which the controller changes valley (I_{out} increasing)
	0 −−LL −− 230 V	−−HL −− 400 V	
100%	1st	2nd	100%
80%	2nd	3rd	85%
65%	3rd	4th	70%
50%	4th	5th	55%
35%	5th	6th	40%
25%	FF mode	FF mode	30%
0%			0%
	0 −−LL −− 240 V	−−HL −− 400 V	
	HV pin voltage for valley change		

I_{out} decreases

I_{out} increase

Figure 20. TABLE II: Valley Selection

ZERO CROSSING DETECTION BLOCK

The ZCD pin allows detecting when the drain−source voltage of the power MOSFET reaches a valley.

A valley is detected when the ZCD pin voltage crosses below the 55 mV internal threshold.

At startup or in case of extremely damped free oscillations, the ZCD comparator may not be able to detect the valleys. To avoid such a situation, the NCL30388 a Time−Out circuit that generates pulses if the voltage on ZCD pin stays below the 55 mV threshold for 6.5 μs.

The Time−out also acts as a substitute clock for the valley detection and simulates a missing valley in case of too damped free oscillations.

At startup, the output voltage reflected on the auxiliary winding is low. Because of the ZCD resistor bridge setting the constant voltage regulation target, the voltage on the ZCD pin is very low and the ZCD comparator might be unable to detect the valleys. In this condition, setting the DRV Latch with the 6.5−μs time−out leads to a continuous conduction mode operation (CCM) at the beginning of the soft−start. This CCM operation only last a few cycles until the voltage on ZCD pin becomes high enough and trips the ZCD comparator.

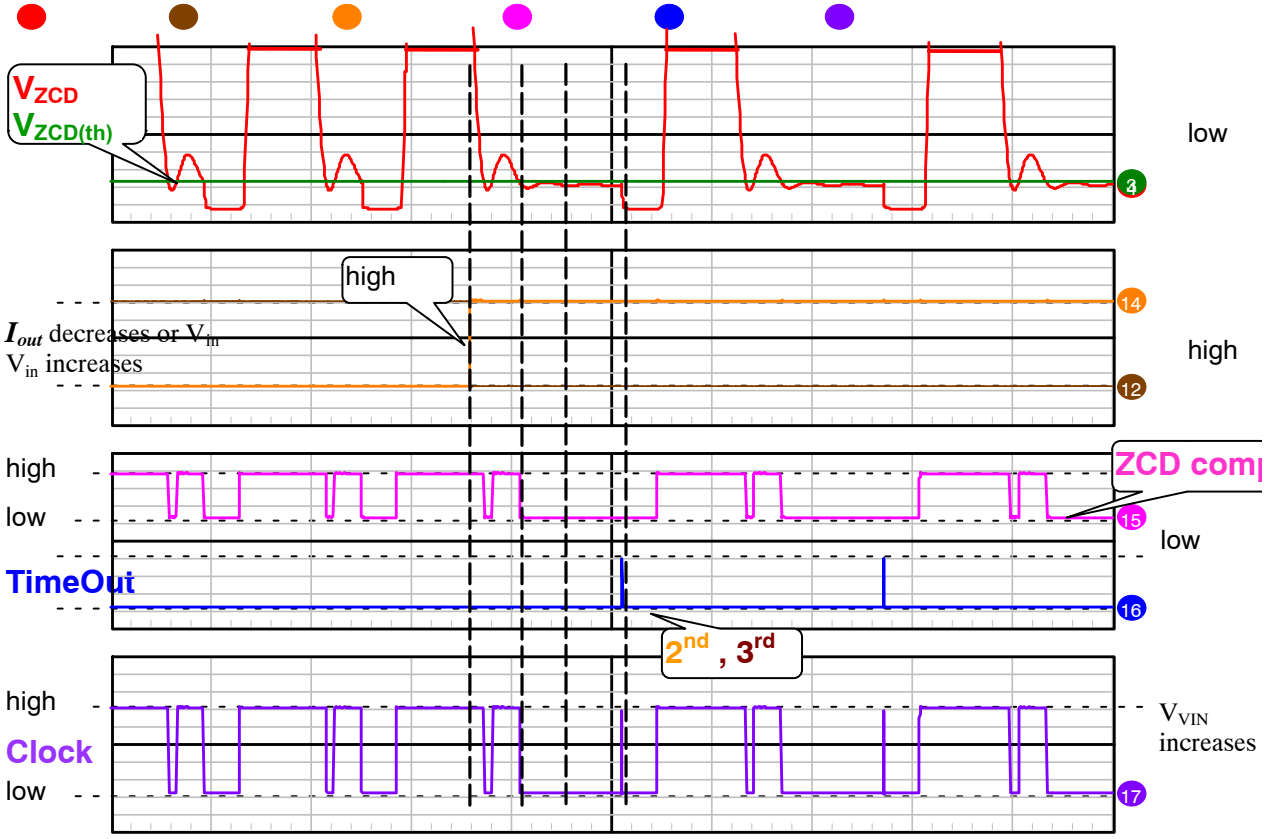


Figure 21.

If the ZCD pin or the auxiliary winding happen to be shorted the time−out function would normally make the controller keep switching and hence lead to improper regulation of the LED current.

The Under Voltage Protection (UVP) is implemented to avoid these scenarios: a secondary timer starts counting when the ZCD voltage is below the $V_{ZCD(short)}$ threshold. If this timer reaches 90 ms, the controller detects a fault and enters the auto−recovery fault mode.

ZCD PIN OVER VOLTAGE PROTECTION.

Because of the power factor correction, it is necessary to set the crossover frequency of the CV loop very low (target 10 Hz, depending on power stage phase shift). Because the loop is slow, the output voltage can reach high value during startup or during an output load step. It is necessary to limit the output voltage excursion. For this, the NCL30388 features a slow over voltage protection (slow OVP) and a fast over voltage protection (fast OVP) on ZCD pin.

Slow OVP

If ZCD voltage exceed $V_{ZCD(OVP1)}$ for four consecutive switching cycles, the controller stops switching during 1.4 ms. After 1.4 ms, the controller initiates a new DRV pulse to refresh ZCD sampling voltage. If V_{ZCD} is still too high (V_{ZCD} > 110%$V_{REF(CV)}$), the controller continues to switch with a 1.4 ms period. The controller resumes its normal operation when V_{ZCD} < 110%$V_{REF(CV)}$.

Fast OVP

If ZCD voltage exceeds $V_{ZCD(OVP2)}$ (130% of $V_{REF(CV)}$) for 4 consecutive switching cycles (slow OVP not triggered) or for 2 switching cycles if the slow OVP has already been triggered, the controller detects a fault and starts the auto−recovery fault mode (cf: Protections Section)

LINE FEEDFORWARD

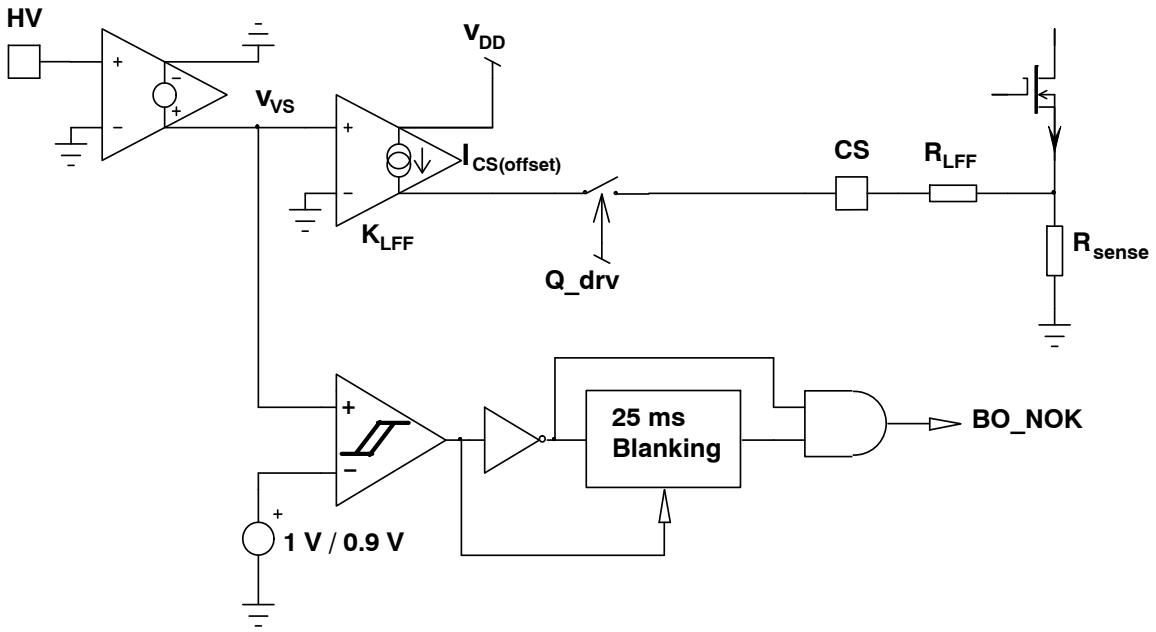


Figure 22. Line Feed−Forward and Brown−out Schematic

The line voltage is sensed by the HV pin and converted into a current. By adding an external resistor in series between the sense resistor and the CS pin, a voltage offset proportional to the line voltage is added to the CS signal. The offset is applied only during the MOSFET on−time in order to not influence the detection of the leakage inductance reset.

The offset is always applied even at light load in order to improve the current regulation at low output load.

BROWN−OUT

In order to protect the supply against a very low input voltage, the NCL30388 features a brown−out circuit with a fixed ON/OFF threshold. The controller is allowed to start if a voltage higher than 100 V is applied to the HV pin and shuts−down if the HV pin voltage decreases and stays below 90 V for 25 ms typical. Exiting a brown−out condition overrides the hiccup on V_{CC} (V_{CC} does not wait to reach $V_{CC(off)}$) and the IC immediately goes into startup mode.

PROTECTIONS

The circuit incorporates a large variety of protections to make the LED driver very rugged.

Among them, we can list:

- Fault of the GND connection
  If the GND pin is properly connected, the supply current drawn from the positive terminal of the V_{CC} capacitor, flows out of the GND pin to return to the negative terminal of the V_{CC} capacitor. If the GND pin is not connected, the circuit ESD diodes offer another return path. The accidental non connection of the GND pin can hence be detected by detecting that one of this ESD diode is conducting. Practically, the ESD diode of CS pin is monitored. If such a fault is detected for 200 μs, the circuit stops generating DRV pin.
- Output short circuit situation (Output Under Voltage Protection)
  Overload is detected by monitoring the ZCD pin voltage: if it remains below $V_{ZCD(short)}$ for 90 ms, an output short circuit is detected and the circuit stops generating pulses for 4 s. When this 4 s delay has elapsed, the circuit attempts to restart.
- ZCD pin incorrect connection:
  - If the ZCD pin grounded, the circuit will detect an output short circuit situation when 90 ms delay has elapsed.
  - A 200 kΩ resistor pulls down the ZCD pin so that the output short circuit detection trips if the ZCD pin is not connected (floating).
- Winding or Output Diode Short Circuit protection
  The circuit detects this failure when 4 consecutive DRV pulses occur within which the CS pin voltage exceeds ($V_{CS(stop)}$=140% *V_{ILIM}). In this case, the controller enters auto−recovery mode (4 s operation interruption between active bursts).
- V_{CC} Over Voltage Protection
  The circuit stops generating pulses if the V_{CC} exceeds $V_{CC(OVP)}$ and enters auto−recovery mode (4 s operation interruption between active bursts).
  This feature protects the circuit if output LEDs happen to be disconnected.

- ZCD fast OVP
  If ZCD voltage exceeds $V_{ZCD(OVP2)}$ for 4 consecutive switching cycles (slow OVP not triggered) or for 2 switching cycles if the slow OVP has already been triggered, the controller detects a fault and enters auto−recovery mode (4−s operation interruption between active bursts).
- Die Over Temperature (TSD)
  The circuit stops operating if the junction temperature (T_J) exceeds 150°C typically. The controller remains off until T_J goes below nearly 100°C.
- Brown−Out Protection (BO)
  The circuit prevents operation when the line voltage is too low to avoid an excessive stress of the LED driver. Operation resumes as soon as the line voltage is high enough and V_{CC} is higher than $V_{CC(on)}$.
- CS pin short to ground
  The CS pin is checked at start−up (cold start−up or after a brown−out event). A current source ($I_{cs(short)}$) is applied to the pin and no DRV pulse is generated until the CS pin exceeds $V_{cs(low)}$. $I_{cs(short)}$ and $V_{cs(low)}$ are 500 μA and 60 mV typically (V_{CS} rising). The typical minimum impedance to be placed on the CS pin for operation is then 120 Ω. In practice, it is recommended to place more than 250 Ω to take into account possible parametric deviations.
  Also, along the circuit operation, the CS pin could happen to be grounded. If it is grounded, the MOSFET conduction time is limited by the maximum on−time. If such an event occurs, a new pin impedance test is made.

ORDERING TABLE OPTION

	DSS		Maximum Dead−time			V_{REF}		Max. On−time		ZCD Blanking		Line Range Detector	
	Y	N	A	B	C	U	V	A	B	A	B	Y	N
OPN #	On	Off	250 μs	687 μs	1.4 ms	250 mV	333 mV	20 μs	33 μs	1 μs	1.5 μs	On	Off
NCL30388A1	x			x			x	x			x		x
NCL30388B1		x		x			x	x		x			x

ORDERING INFORMATION2

Device	Marking	Package type	Shipping†
NCL30388A1DR2G	L30388A1	SOIC8 – P7 COMP VHV PBFH	2500 / Tape & Reel
NCL30388B1DR2G	L30388B1	SOIC8 – P7 COMP VHV PBFH	2500 / Tape & Reel

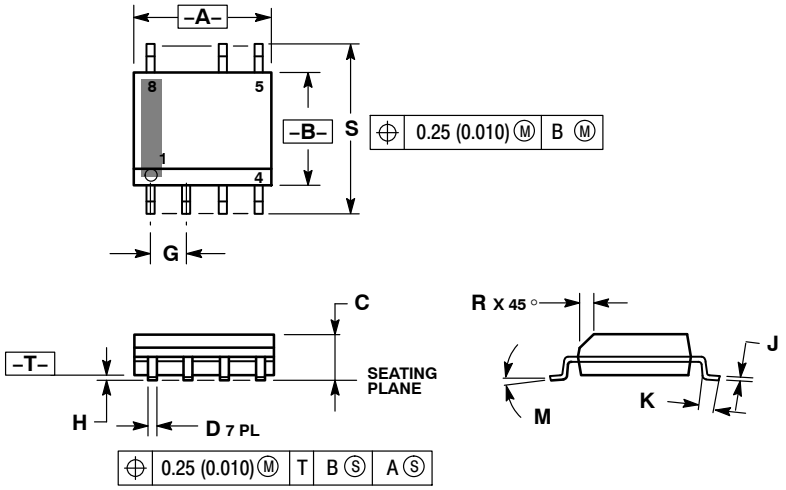
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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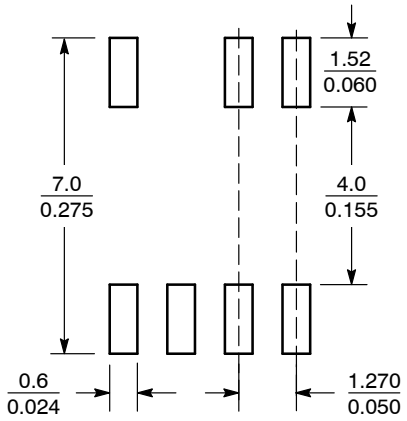
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

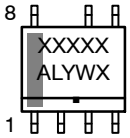
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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