NCN8026A

Compact Low Power Smart Card Interface IC

The NCN8026A is a compact and cost−effective single SIM & smart card interface IC. It can be used with 1.8 V, 3 V and 5 V IC cards. The card VCC supply is provided by a built−in very low drop out and low noise Regulator. The NCN8026A offers enhanced performances with low VCC output ripple under load−transient conditions, very low shutdown current and 1.8 V−to−5 V logic compatibility.

This device is fully compatible with the ISO 7816−3, EMV 4.2, UICC and related standards including NDS and other STB standards (Nagravision, Irdeto, Conax ..). It satisfies the requirements specifying conditional access into Set−Top−Boxes (STB) or Conditional Access Modules (CAM).

This smart card interface IC is available in a QFN−24 package providing all the industry−standard features usually required for STB smart card interface.



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QFN24
MN SUFFIX
CASE 485L

MARKING DIAGRAMS



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

Features

- Single IC Card Interface
- Fully Compatible with ISO 7816−3, EMV4.2, UICC and Related Standards Including NDS and Other STB Standards (Nagravision, Irdeto, Conax...)
- Three Bidirectional Buffered I/O Level Shifters (C4, C7 and C8)
- 1.8 V, 3.0 V or 5.0 V ± 5 % Regulated Card Power Supply Such as $I_{CC} \leq 70$ mA with Low VCC Ripple
- Regulator Power Supply: V_{DDP} = 2.7 V to 5.5 V (@ 1.8 V), 3.0 V to 5.5 V (@ 3.0 V) and 4.85 V to 5.5 V (@ 5.0 V)
- Independent Power Supply range on Controller Interface such as V_{DD} = 1.6 V to 5.5 V
- Handles Class A, B and C Smart Cards
- Short Circuit Protection on all Card Pins
- Support up to 27 MHz input Clock with Internal Division Ratio 1/1, 1/2, 1/4 and 1/8 through CLKDIV1 and CLKDIV2
- HBM ESD Protection on Card Pins up to +8 kV (Human Body Model)
- Activation / Deactivation Sequences (ISO7816 Sequencer)
- Fault Protection Mechanisms Enabling Automatic Device Deactivation in Case of Overload, Overheating, Card Take−off or Power Supply Drop−out (OCP, OTP, UVP)
- Interrupt Signal $\overline{INT}$ for Card Presence and Faults
- Chip Select Pin ($\overline{CS}$) for Dual Card Operating
- External Under−Voltage Lockout Threshold Adjustment on V_{DD} (PORADJ Pin)
- Available in One Package Formats: QFN−24
- These are Pb−Free Devices

Typical Application

- Pay TV, Set Top Box Decoder with Conditional Access and Pay−per−View
- Conditional Access Module (CAM / CAS)
- SIM card interface applications (UICC / USIM)
- Point Of Sales and Transaction Terminals
- Electronic Payment and Identification

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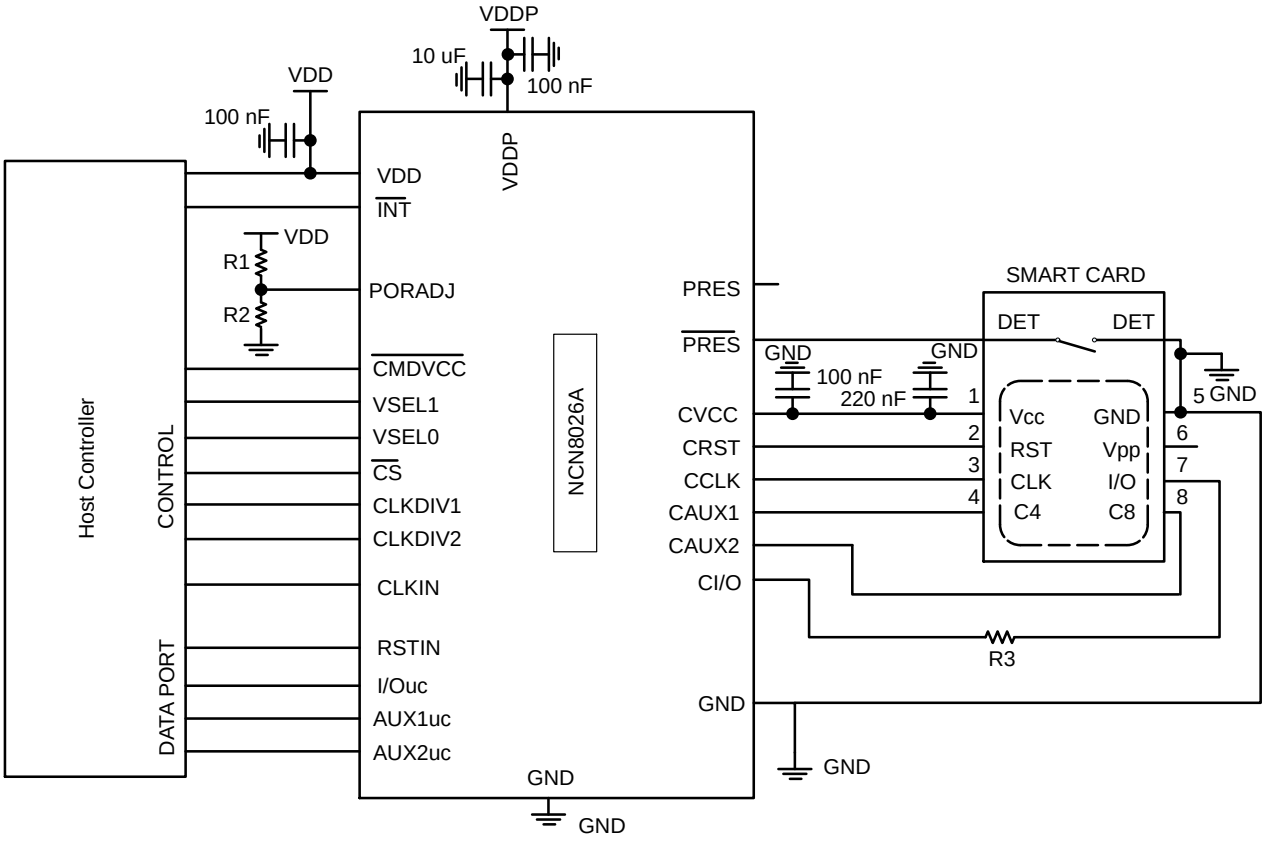


Figure 1. Typical Smart Card Interface Application

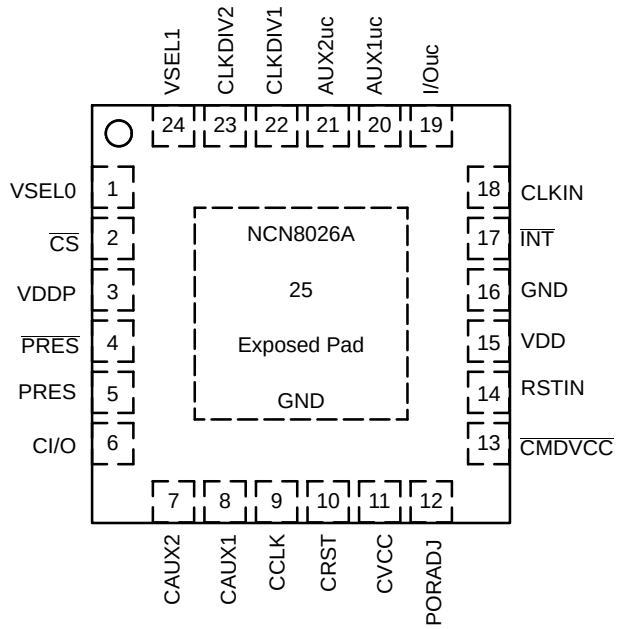


Figure 2. NCN8026A − QFN−24 Pinout
(Top View)

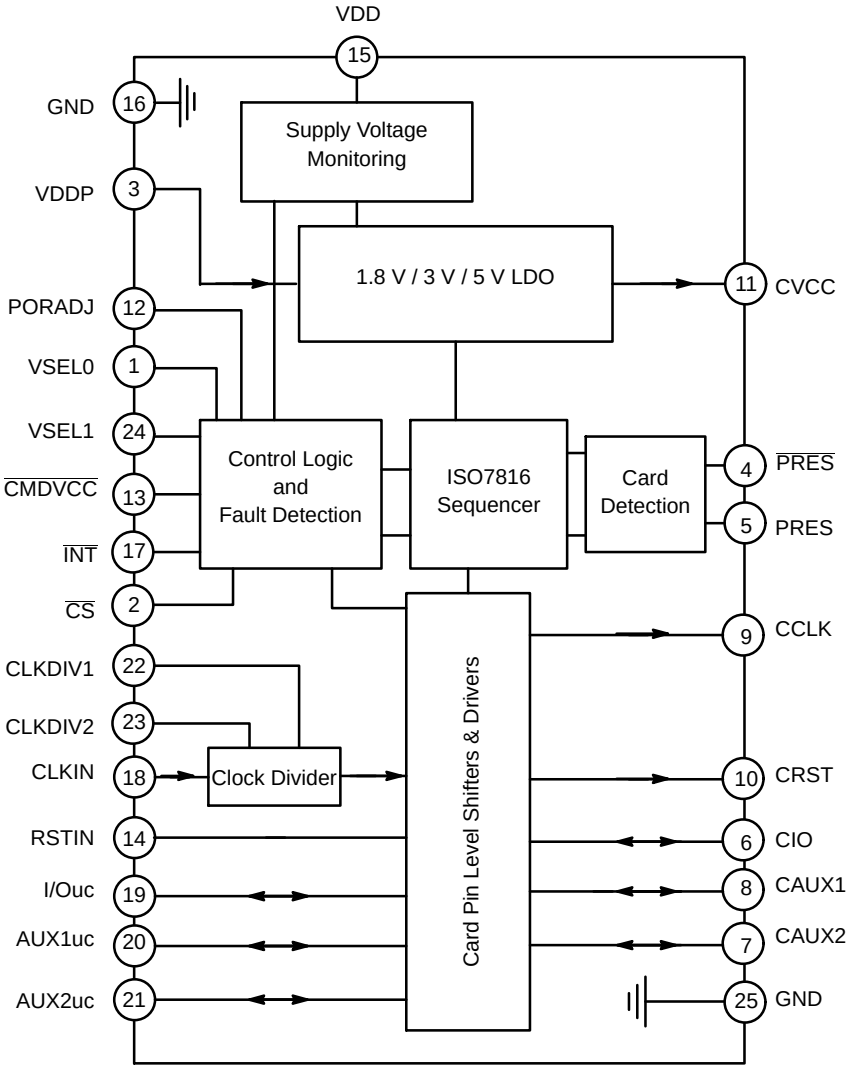


Figure 3. NCN8026A Block Diagram (QFN−24 Pin Numbering)

PIN FUNCTION AND DESCRIPTION

Pin (QFN24)	Name	Type	Description
1	VSEL0	Input	Allows selecting card V_{CC} power supply voltage mode (5V/$\overline{3V}$ or 1.8V/$\overline{3V}$) VSEL0 = Low; CVCC = 5 V when VSEL1 = High or 3 V when VSEL1 = Low VSEL0 = High; CVCC = 1.8 V when VSEL1 = High or 3 V when VSEL1 = Low
2	$\overline{CS}$	Input	When $\overline{CS}$ is Low, the corresponding chip is selected and the control and signal pins are configured normally. When $\overline{CS}$ is set High, $\overline{CMDVCC}$, VSEL0, VSEL1, CLKDIV1, CLKDIV2 and RSTIN are latched. IOuc, AUX1uc, and AUX2uc are set to high−impedance pull−up mode and data transmission to or from the smart card is no longer allowed. VCC card power supply and card clock are maintained active if the part is active.
3	VDDP	Power	Regulator power supply. When VDDP is below 2.5 V typical the card pins are disabled.
4	$\overline{PRES}$	Input	Card presence pin active (card present) when $\overline{PRES}$ = Low. A built−in debounce timer of about 8 ms is activated when a card is inserted. Convenient for Normally Open (NO) Smart card connector. This pin can be left open when not in use.
5	PRES	Input	Card presence pin active (card present) when PRES = High. A built−in debounce timer of about 8 ms is activated when a card is inserted. Convenient for Normally Closed (NC) smart card connector. This pin can be left open when not in use.

PIN FUNCTION AND DESCRIPTION

Pin (QFN24)	Name	Type	Description
6	CI/O	Input/ Output	This pin handles the connection to the serial I/O (C7) of the card connector. A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 kΩ (typical) pull up resistor to CVCC provides a High impedance state for the smart card I/O link.
7	CAUX2	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX2 I/O pin (C8). A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 kΩ (typical) pull up resistor to CVCC provides a High impedance state for the smart card C8 pin.
8	CAUX1	Input/ Output	This pin handles the connection to the chip card's serial auxiliary AUX1 I/O pin (C4). A bi−directional level translator adapts the serial I/O signal between the card and the micro controller. A 11 kΩ (typical) pull up resistor to CVCC provides a High impedance state for the smart card C4 pin.
9	CCLK	Output	This pin is connected to the CLOCK card connector's pin (Chip card's pin C3). The Clock signal comes from the CLKIN input through clock dividers and level shifter.
10	CRST	Output	This pin is connected to the chip card's RESET pin (C2) through the card connector. A level translator adapts the external Reset (RSTIN) signal to the smart card.
11	CVCC	Power Output	This pin is connected to the smart card power supply pin (C1). An internal low dropout regulator is programmable using the pins VSEL0 and VSEL1 to supply either 5 V or 3 V or 1.8 V output voltage. An external distributed ceramic capacitor ranging from 80 nF to 1.2 μF recommended must be connected across CVCC and CGND. This set of capacitor (if distributed) must be low ESR (< 100 mΩ).
12	PORADJ	Input	Power−on reset threshold adjustment input pin for changing the reset threshold (V_{DD} UVLO threshold) thanks to an external resistor power divider. Needs to be connected to ground when unused.
13	$\overline{\text{CMDVCC}}$	Input	Command V_{CC} pin. Activation sequence Enable/Disable pin (active Low). The activation sequence is enabled by toggling $\overline{\text{CMDVCC}}$ High to Low and when a card is present. When $\overline{\text{CMDVCC}}$ = High, the CVCC output is pulled low and the internal LDO is disabled unless the device has been latched by the $\overline{\text{CS}}$ pin.
14	RSTIN	Input	This Reset input connected to the host and referred to VDD (microcontroller side), is connected to the smart card Reset pin through the internal level shifter which translates the level according to the CVCC programmed value.
15	VDD	Power input	This pin is connected to the system controller power supply. It configures the level shifter input stage to accept the signals coming from the controller. A 0.1 μF decoupling capacitor shall be used. When V_{DD} is below 1.45 V typical the card pins are disabled.
16	GND	Ground	Ground
17	$\overline{\text{INT}}$	Output	The interrupt request is activated LOW on this pin. This is enabled when a card is present and the card presence is detected by $\overline{\text{PRES}}$ or PRES pins. Similarly an interrupt is generated when CVCC is overloaded. Inverter output (An open−drain output configuration with 50 kΩ pull−up resistor is available under request (metal change)).
18	CLKIN	Input	Clock Input for External Clock
19	I/Ouc	Input / Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial I/O signal between the smart card and the external controller. A built−in constant 11 kΩ (typical) resistor provides a high impedance state.
20	AUX1uc	Input / Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial C4 signal between the smart card and the external controller. A built−in constant 11 kΩ (typical) resistor provides a high impedance state.
21	AUX2uc	Input / Output	This pin is connected to an external micro−controller. A bi−directional level translator adapts the serial C8 signal between the smart card and the external controller. A built−in constant 11 kΩ (typical) resistor provides a high impedance state.
22	CLKDIV1	Input	This pin coupled with CLKDIV2 is used to program the clock frequency division ratio (Table 2).
23	CLKDIV2	Input	This pin coupled with CLKDIV1 is used to program the clock frequency division ratio (Table 2).
24	VSEL1	Input	Allows selecting card V_{CC} power supply voltage. VSEL0 = Low: CVCC = 5 V when VSEL1 = High or 3 V when VSEL1 = Low. VSEL0 = High: CVCC = 1.8 V when VSEL1 = High or 3 V when VSEL1 = Low.
25	GND	Ground	Regulator Power Supply Ground

ATTRIBUTES

Characteristics	Values
ESD protection Human Body Model (HBM) (Note 1) Card Pins (card interface pins 4−11) All Other Pins Machine Model (MM) Card Pins (card interface pins 4−11) All Other Pins	 8 kV 2 kV 400 V 150 V
Moisture sensitivity (Note 2) QFN−24	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch−up Test	

1. Human Body Model (HBM), R = 1500 Ω, C = 100 pF.
2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
Regulator Power Supply Voltage	V_{DDP}	$-0.3 \le V_{DDP} \le 5.5$	V
Power Supply from Microcontroller Side	V_{DD}	$-0.3 \le V_{DD} \le 5.5$	V
External Card Power Supply	CVCC	$-0.3 \le CVCC \le 5.5$	V
Digital Input Pins	V_{in}	$-0.3 \le V_{in} \le V_{DD}$	V
Digital Output Pins (I/Ouc, AUX1uc, AUX2uc, $\overline{INT}$)	V_{out}	$-0.3 \le V_{out} \le V_{DD}$	V
Smart card Output Pins	V_{out}	$-0.3 \le V_{out} \le CVCC$	V
Thermal Resistance Junction−to−Air QFN−24	$R_{\theta JA}$	90	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+125	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.

POWER SUPPLY SECTION (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 5 MHz)

Symbol	Rating	Min	Typ	Max	Unit
V_{DDP}	Regulator Power Supply, 5.0 V Mode, |ICC| ≤ 70 mA 3.0 V Mode, |ICC| ≤ 70 mA 1.8 V Mode, |ICC| ≤ 70 mA	 4.75 3.0 2.7	 5.0 3.3/5.0 3.3/5.0	 5.5 5.5 5.5	V
I_{DDP}	Inactive mode ($\overline{CMDVCC}$ = High, $\overline{CS}$ = Low)	−	2.0	3.0	μA
I_{DDP}	Active Mode, F_{CLKIN} = 0 MHz, $Cout_{CCLK}$ = 33 pF, $\|I_{CVCC}\|$ = 0 ($\overline{CMDVCC}$ = Low, $\overline{CS}$ = Low)	−	−	4.0	mA
I_{DDP}	DC Operating supply current, F_{CLKIN} = 5 MHz, $Cout_{CCLK}$ = 33 pF, $\|I_{CVCC}\|$ = 0 ($\overline{CMDVCC}$ = Low, $\overline{CS}$ = Low)	−	−	5.0	mA
I_{DDP}	DC Operating supply current with F_{CLKIN} = 5 MHz, I_{CVCC} = 70 mA	−	−	76	mA
V_{DD}	Operating Voltage	1.6	−	5.5	V
I_{VDD}	Inactive mode − standby current ($\overline{CMDVCC}$ = High)	−	−	1.0	μA
I_{VDD}	Operating Current − F_{CLKIN} = 0 MHz , $Cout_{CCLK}$ = 33 pF $\|I_{CVCC}\|$ = 0 ($\overline{CMDVCC}$ = Low)	−	−	1.0	μA
I_{VDD}	Operating Current − F_{CLKIN} = 5 MHz , $Cout_{CCLK}$ = 33 pF $\|I_{CVCC}\|$ = 0 ($\overline{CMDVCC}$ = Low)	−	−	100	μA
$UVLOV_{DD}$	Under Voltage Lock−Out (UVLO), no external resistor at pin PORADJ (connected to GND), falling V_{DD} level	1.35	1.45	1.55	V
UVLOHys	UVLO Hysteresis, no external resistor at pin PORADJ (Connected to GND) (Note 4)	50	100	150	mV
$UVLOV_{DDP}$	Under Voltage LockOut (UVLO) falling VDDP level	2.4	2.5	2.6	V
UVLOHys	VDDP UVLO Hysteresis (Note 4)	50	100	150	mV
PORADJ pin					
V_{PORth+}	External Rising threshold voltage on V_{DD} for Power On Reset − pin PORADJ	1.19	1.24	1.26	V
V_{PORth-}	External Falling threshold voltage on V_{DD} for Power On Reset − pin PORADJ	1.17	1.19	1.22	V
V_{PORHys}	Hysteresis on V_{PORth} (pin PORADJ) (Note 4)	30	80	100	mV
t_{POR}	Width of Power−On Reset pulse (Note 4) No external resistor on PORADJ External resistor on PORADJ	 4.0 4.0	 8.0 8.0	 12 12	 ms ms
I_{IL}	Low level input leakage current, V_{IL} < 0.5 V (Pull−down source current)		0.2		μA
Low Dropout Regulator					
C_{CVCC}	Output Capacitance on card power supply CVCC (Note 5)	0.08	0.32	1.2	μF
CVCC	Output Card Supply Voltage (including ripple) 1.8 V CVCC mode @ ICC ≤ 70 mA 3.0 V CVCC mode @ ICC ≤ 70 mA 5.0 V CVCC mode @ ICC ≤ 70 mA with 4.75 V ≤ VDDP ≤ 5.5 V	 1.68 2.85 4.65	 1.80 3.00 5.00	 1.90 3.15 5.25	 V V V
CVCC	Current pulses 7 nAs (t < 400 ns & $\|I_{CC}\|$ < 40 mA peak) (Note 4) 1.8 V mode / Ripple ≤ 150 mV (2.7 V ≤ V_{DDP} ≤ 5.5 V) Current pulses 40 nAs (t < 400 ns & $\|I_{CC}\|$ < 200 mA peak) (Note 4) 3.0 V mode / Ripple ≤ 150 mV (2.9 V ≤ V_{DDP} ≤ 5.5 V) Current pulses 40 nAs (t < 400 ns & $\|I_{CC}\|$ < 200 mA peak) (Note 4) 5.0 V mode / Ripple ≤ 150 mV (4.85 V ≤ V_{DDP} ≤ 5.5 V)	 1.66 2.70 4.60	 1.80 3.00 5.00	 1.90 3.30 5.30	 V V V
I_{CVCC}	Card Supply Current @ 1.8 V Mode @ 3.0 V Mode @ 5.0 V Mode			 70 70 70	mA
I_{CVCC_SC}	Short −Circuit Current − CVCC shorted to ground	−	120	150	mA
ΔV_{CVCC}	Output Card Supply Voltage Ripple peak−to−peak − f_{ripple} = 100 Hz to 200 MHz (load transient frequency with 65 mA peak current and 50% Duty Cycle) (Note 4)	−	−	150	mV
$CVCC_{SR}$	Slew Rate on CVCC turn−on / turn−off (Note 4)	−	−	0.22	V/μs

4. Guaranteed by design and characterization.
5. These values take into account the tolerance of the cms capacitor used. CMS capacitor very low ESR (< 100 mΩ, X5R / X7R).

HOST INTERFACE SECTION CLKIN, RSTIN, I/Ouc, AUX1uc, AUX2uc, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1, $\overline{CS}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 5 MHz)

Symbol	Rating	Min	Typ	Max	Unit
F_{CLKIN}	Clock frequency on pin CLKIN (Note 6)	−	−	27	MHz
V_{IL}	Input Voltage level Low: CLKIN, RSTIN, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1, $\overline{CS}$	−0.3	−	0.3 x V_{DD}	V
V_{IH}	Input Voltage level High: CLKIN, RSTIN, CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, VSEL0, VSEL1, $\overline{CS}$	0.7 x V_{DD}	−	V_{DD} + 0.3	V
$\|I_{IL}\|$	CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, CLKIN, VSEL0, VSEL1, $\overline{CS}$ Low Level Input Leakage Current, V_{IL} = 0 V	−	−	1.0	μA
$\|I_{IH}\|$	CLKDIV1, CLKDIV2, $\overline{CMDVCC}$, RSTIN, CLKIN, VSEL0, VSEL1, $\overline{CS}$ Low Level Input Leakage Current, V_{IH} = V_{DD}	−	−	1.0	μA
V_{IL}	Input Voltage level Low: I/Ouc, AUX1uc, AUX2uc	−0.3	−	0.5	V
V_{IH}	Input Voltage level High: I/Ouc, AUX1uc, AUX2uc	0.7 x V_{DD}	−	V_{DD} + 0.3	V
$\|I_{IL}\|$	I/Ouc, AUX1uc, AUX2uc Low level input leakage current, V_{IL} = 0 V	−	−	600	μA
$\|I_{IH}\|$	I/Ouc, AUX1uc, AUX2uc High level input leakage current, V_{IH} = V_{DD}	−	−	10	μA
V_{OH}	I/Ouc, AUX1uc, AUX2uc data channels, @ Cs ≤ 30 pF High Level Output Voltage (CRD_I/O = CAUX1 = CAUX2 = CVCC) IOH = 0 I_{OH} = −40 μA for V_{DD} > 2 V (I_{OH} = −20 μA for V_{DD} ≤ 2 V)	 0.9 x V_{DD} 0.75 x V_{DD}	 −	 V_{DD} + 0.1 V_{DD} + 0.1	 V V
V_{OL}	Low Level Output Voltage (CRD_I/O = CAUX1 = CAUX2 = 0 V) I_{OL}= + 1 mA	 0	−	 0.3	 V
$t_{Ri/Fi}$	Input Rising/Falling times (Note 6)	−	−	1.2	μs
$t_{Ro/Fo}$	Output Rising/Falling times (Note 6)	−	−	0.1	μs
R_{pu}	I/0uc, AUX1uc, AUX2uc Pull Up Resistor	8.0	11	16	kΩ
V_{OH}	Output High Voltage $\overline{INT}$ @ I_{OH} = −15 μA (source)	 0.75 x V_{DD}	 −	 −	V
V_{OL}	Output Low Voltage $\overline{INT}$ @ I_{OL} = 2 mA (sink)	 0	 −	 0.30	V
R_{INT}	$\overline{INT}$ Pull Up Resistor	−	20	−	kΩ

6. Guaranteed by design and characterization.

SMART CARD INTERFACE SECTION CI/O, CAUX1, CAUX2, CCLK, CRST, PRES, $\overline{PRES}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 5 MHz)

Symbol	Rating	Min	Typ	Max	Unit
	CRST @ CVCC = 1.8 V, 3.0 V, 5.0 V				
V_{OH}	Output RESET V_{OH} @ I_{rst} = −200 μA	0.9 x CV_{CC}	−	CVCC	V
V_{OL}	Output RESET V_{OL} @ I_{rst} = 200 μA	0	−	0.20	V
	Output RESET V_{OH} @ I_{rst} = −20 mA	0		0.4	V
t_R	Output RESET V_{OL} @ I_{rst} = 20 mA	CV_{CC} − 0.4		CV_{CC}	V
t_F					
$t_{R/F}$	Output RESET Rise time @ C_{out} = 100 pF (Note 7)	−	−	100	ns
td	Output RESET Fall time @ C_{out} = 100 pF (Note 7)	−	−	100	ns
	Output Rise/Fall times @ CVCC = 1.8 V & C_{out} = 100 pF (Note 7)	−	−	200	ns
	RSTIN to CRST delay − Reset enabled (Note 7)	−	−	2	μs
	CCLK @ CVCC = 1.8 V, 3.0 V or 5.0 V				
F_{CRDCLK}	Output Frequency (Note 7)	−	−	27	MHz
V_{OH}	Output CCLK V_{OH} @ I_{clk} = −200 μA	0.9 x CV_{CC}	−	CV_{CC}	V
V_{OL}	Output CCLK V_{OL} @ I_{clk} = 200 μA	0	−	+0.2	V
	Output CCLK V_{OH} @ I_{clk} = −70 mA	0		0.4	V
F_{DC}	Output CCLK V_{OL} @ I_{clk} = 70 mA	CV_{CC} − 0.4		CV_{CC}	V
	Output Duty Cycle (Note 7)	45	−	55	%
t_{rills}					
t_{ulsa}	Rise & Fall time				
	Output CCLK Rise time @ C_{out} = 33 pF (Note 7)	−	−	16	ns
SR	Output CCLK Fall time @ C_{out} = 33 pF (Note 7)	−	−	16	ns
	Slew Rate @ C_{out} = 33 pF (CVCC = 3.0 V or 5.0 V) (Note 7)	0.2	−	−	V/ns
	CAUX1, CAUX2, CI/O @ CVCC = 1.8 V, 3.0 V, 5.0 V				
V_{IH}	Input Voltage High Level				
	1.8 V Mode	0.7xV_{CC}	−	CV_{CC} + 0.3	V
	3.0 V Mode	1.6	−	CV_{CC}+ 0.3	V
	5.0 V Mode	1.8	−	CV_{CC} + 0.3	V
V_{IL}	Input Voltage Low Level				
	1.8 V mode	−0.30	−	0.50	V
	3.0 V and 5.0 V modes	−0.30	−	0.80	V
$\|I_{IL}\|$	Low Level Input current V_{IL} = 0 V	−		600	μA
$\|I_{IH}\|$	High Level Input current V_{IH} = CVCC	−		10	μA
V_{OH}	Output V_{OH}				
	@ I_{OH} = no DC load	0.9xCV_{CC}		CV_{CC} + 0.1	V
	@ I_{OH} = −40 μA for CVCC = 3.0 V and 5.0 V	0.75xCV_{CC}	−	CV_{CC} + 0.1	V
	@ I_{OH} = −20 μA for CVCC = 1.8 V	0.75xCV_{CC}	−	CV_{CC} + 0.1	
V_{OL}	@ I_{OH} ≥ −15 mA	0	−	0.4	V
	Output V_{OL}				
$t_{Ri / Fi}$	@ I_{OL} = 1 mA, V_{IL} = 0 V	0	−	0.30	μs
	@ I_{OL} ≥ +15 mA	V_{CC} − 0.4	−	V_{CC}	
$t_{Ro / Fo}$	Input Rising/Falling times (Note 7)	−	−	1.2	μs
	Output Rising/Falling times / C_{out} = 80 pF (Note 7)	−	−	0.1	
F_{bidi}	Maximum data rate through bidirectional I/O, AUX1 & AUX2 channels (Note 7)	−	−	1	MHz
R_{PU}	CAUX1, CAUX2, CI/O Pull− Up Resistor	8	11	16	kΩ
t_{IO}	Propagation delay IOuc −> CI/O and CI/O −> IOuc (falling edge) (Note 7)	−	−	200	ns
tpu	Active pull−up pulse width buffers I/O, AUX1 and AUX2 (Note 7)	−	−	200	ns
C_{in}	Input Capacitance on data channels (Note 7)	−	−	10	pF
	PRES, $\overline{PRES}$				V
V_{IH}	Card Presence Voltage High Level	0.7 x V_{DD}	−	V_{DD} + 0.3	
V_{IL}	Card Presence Voltage Low Level	−0.3	−	0.3 x V_{DD}	

SMART CARD INTERFACE SECTION CI/O, CAUX1, CAUX2, CCLK, CRST, PRES, $\overline{\text{PRES}}$ (V_{DD} = 3.3 V; V_{DDP} = 5 V; T_{amb} = 25°C; F_{CLKIN} = 5 MHz)

Symbol	Rating	Min	Typ	Max	Unit
	PRES, $\overline{\text{PRES}}$ Low level input leakage current, $V_{IH} = V_{DD}$				μA
$\lvert I_{IH} \rvert$	PRES $\overline{\text{PRES}}$		0.2	2.0 1.0	
	High level input leakage current, V_{IL} = 0 V				
$\lvert I_{IL} \rvert$	PRES $\overline{\text{PRES}}$		0.2	1.0 2.0	
$T_{debounce}$	Debounce time PRES and $\overline{\text{PRES}}$ (Note 7)	5	8	12	ms
$I_{CI/O}$	CI/O, CAUX1, CAUX2 current limitation, CVCC enabled	−	−	15	mA
I_{CCLK}	CCLK current limitation	−	−	70	mA
I_{CRST}	CRST current limitation	−	−	20	mA
T_{act}	Activation Time (Note 7)	30	−	100	μs
T5	RSTIN time control (Figure 5) (Note 7)	200	240	280	μs
T_{deact}	Deactivation Time (Note 7)	30	−	250	μs

7. Guaranteed by design and characterization.

POWER SUPPLY

The NCN8026A smart card interface has two power supplies: V_{DD} and V_{DDP}.

V_{DD} is common to the system controller and the interface. The applied V_{DD} range can go from 1.6 V up to 5.5 V. If V_{DD} goes below 1.45 V typical ($UVLO_{VDD}$) a power−down sequence is automatically performed. In that case the interrupt ($\overline{\text{INT}}$) pin is set Low.

A Low Drop−Out (LDO) and low noise regulator is used to provide the 1.8 V, 3 V or 5 V power supply voltage (CVCC) to the card. V_{DDP} is the LDO's input voltage. CVCC is the LDO output. The typical distributed reservoir output capacitor connected to CVCC is 100 nF + 220 nF. The capacitor of 100 nF is connected as close as possible to the CVCC's pin and the 220 nF one as close as possible to the card connector C1 pin. Both feature very low ESR values (lower than 50 mΩ). The decoupling capacitors on V_{DD} and V_{DDP} respectively 100 nF and 10 μF + 100 nF have also to be connected close to the respective IC pins.

The CVCC pin can source up to 70 mA at 1.8 V, 3 V and 5 V continuously over the V_{DDP} range (see corresponding specification table), the absolute maximum current being internally limited below 150 mA (Typical at 120 mA).

The card V_{CC} voltage (CVCC) can be programmed with the pins VSEL0 and VSEL1 and according to the below table:

Table 1. CVCC PROGRAMMING

VSEL0	VSEL1	CVCC
0	0	3.0 V
0	1	5.0 V
1	0	3.0 V
1	1	1.8 V

VSEL0 can be used to select the CVCC programming mode which can be 5V/$\overline{3V}$ (VSEL0 connected to Ground) or 1.8V/$\overline{3V}$ (VSEL0 connected to V_{DD}). VSEL0 and VSEL1 are usually programmed before activating the smart card interface that is when $\overline{\text{CMDVCC}}$ is High.

There's no specific sequence for applying V_{DD} or V_{DDP}. They can be applied to the interface in any sequence. After powering the device $\overline{\text{INT}}$ pin remains Low until a card is inserted.

SUPPLY VOLTAGE MONITORING

The supply voltage monitoring block includes the Power−On Reset (POR) circuitry and the under−voltage lockout (UVLO) detection (V_{DD} voltage dropout detection). PORADJ pin allows the user, according to the considered application, to adjust the V_{DD} UVLO threshold. If not used PORADJ pin is connected to Ground (recommended even if it may be left unconnected).

The input supply voltage is continuously monitored to prevent under voltage operation. At power up, the system initializes the internal logic during POR timing and no further signal can be provided or supported during this period.

The system is ready to operate when the input voltage has reached the minimum V_{DD}. Considering this, the NCN8026A will detect an Under−Voltage situation when the input supply voltage will drop below 1.45 V typical. When V_{DD} goes down below the UVLO falling threshold a deactivation sequence is performed.

The device is inactive during power−on and power−off of the V_{DD} supply (8 ms reset pulse).

PORADJ pin is used to modify the UVLO threshold according to the below relationship considering an external resistor divider R1 / R2 (see block diagram Figure 1):

$$UVLO = \frac{R1 + R2}{R2} V_{POR} \qquad \text{(eq. 1)}$$

If PORADJ is connected to Ground the V_{DD} UVLO threshold (V_{DD} falling) is typically 1.45 V. In some cases it can be interesting to adjust this threshold at a higher value and by the way increase the V_{DD} supply dropout detection

level which enables a deactivation sequence if the V_{DD} voltage is too low.

For example, there are microcontrollers for which the minimum supply voltage insuring a correct operating is higher than 1.45 V; increasing $UVLO_{VDD}$ (V_{DD} falling) is consequently necessary. Considering for instance a resistor bridge with R1 = 56 kΩ, R2 = 42 kΩ and V_{POR-} = 1.22 V typical the V_{DD} dropout detection level can be increased up to:

$$UVLO = \frac{56k + 42k}{42k} V_{POR-} = 2.85\ V \qquad \text{(eq. 2)}$$

CLOCK DIVIDER:

The input clock can be divided by 1/1, 1/2, 1/4, or 1/8, depending upon the specific application, prior to be applied to the smart card driver. These division ratios are programmed using pins CLKDIV1 and CLKDIV2 (see Table 2). The input clock is provided externally to pin CLKIN.

Table 2. CLOCK FREQUENCY PROGRAMMING

CLKDIV1	CLKDIV2	F_{CCLK}
0	0	CLKIN / 8
0	1	CKLKIN / 4
1	0	CLKIN
1	1	CLKIN / 2

The clock input stage (CLKIN) can handle a 27 MHz maximum frequency signal. Of course, the ratio must be defined by the user to cope with Smart Card considered in a given application

In order to avoid any duty cycle out of the 45% / 55% range specification, the divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, whatever be the divider ratio 1/2, 1/4 or 1/8. On the other hand, the output signal Duty Cycle cannot be guaranteed 50% if the division ratio is 1 and if the input Duty Cycle signal is not within the 46% − 56% range at the CLKIN input.

When the signal applied to CLKIN is coming from the external controller, the clock will be applied to the card under the control of the microcontroller or similar device after the activation sequence has been completed.

DATA I/O, AUX1 and AUX2 LEVEL SHIFTERS

The three bidirectional level shifters I/O, AUX1 and AUX2 adapt the voltage difference that might exist between the micro−controller and the smart card. These three channels are identical. The first side of the bidirectional level shifter dropping Low (falling edge) becomes the driver side until the level shifter enters again in the idle state pulling High CI/O and I/Ouc.

Passive 11 kΩ pull−up resistors have been internally integrated on each terminal of the bidirectional channel. In addition with these pull−up resistors, an active pull−up circuit provides a fast charge of the stray capacitance.

While CVCC is enabled, the current to and from the card I/O lines is limited internally to 15 mA and the maximum guaranteed frequency on these lines is 1 MHz. If required, an external series resistor up to 350 Ω can be added to limit the CI/O pin current when CVCC is off, as shown by resistor R3 in the application block diagram in Figure 1.

POWER−UP AND STANDBY MODE

After a Power−on reset, the circuit enters the standby mode. A minimum number of circuits are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- Pins I/Ouc, AUX1uc and AUX2uc are pulled−up to V_{DD} with an active pull−up circuit
- Card pins are inactive and pulled Low
- Supply Voltage monitoring is active

INITIALIZATION SEQUENCE

If the CVCC output is not enabled following the NCN8026A power up, a CVCC initialization is recommended. For this initialization process, the PRES or $\overline{\text{PRES}}$ pin can be activated by a card or the microcontroller. Toggle $\overline{\text{CMDVCC}}$ from high to low to then enable CVCC. After 10 ms, the $\overline{\text{CMDVCC}}$ pin can be set to high to return to the standby mode. If using a microcontroller to activate PRES or $\overline{\text{PRES}}$ pin, the microcontroller output can be set to high impedance. This initialization process is only needed upon NCN8026A power up.

SMART CARD POWER−UP

In the standby mode the microcontroller can check the presence of a card using the signals $\overline{\text{INT}}$ and $\overline{\text{CMDVCC}}$ as shown in Table 3:

Table 3. CARD PRESENCE STATE

$\overline{\text{INT}}$	$\overline{\text{CMDVCC}}$	State
HIGH	HIGH	Card present
LOW	HIGH	Card not present

If a card is detected present ($\overline{\text{PRES}}$ or PRES active) the controller can start a card session by pulling $\overline{\text{CMDVCC}}$ Low. Card activation is run (t0, Figure 5). This Power−Up Sequence makes sure all the card related signals are LOW during the CVCC positive going slope. These lines are validated when CVCC is stable and above the minimum voltage specified. When the CVCC voltage reaches the programmed value (1.8 V, 3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence (Figure 5):

- CVCC is powered−up at its nominal value (t1)
- I/O, AUX1 and AUX2 lines are activated (t2 ~ 10 μs)
- Then Clock is activated and the clock signal is applied to the card (typically 2 μs after I/Os lines) (t3)
- Finally the Reset level shifter is enabled (typically 2 μs after clock channel) (t4)

The clock can also be applied to the card using a **RSTIN mode** allowing controlling the clock starting by setting RSTIN Low (Figure 4). Before running the activation sequence, that is before setting Low $\overline{\text{CMDVCC}}$ RSTIN is set High. The following sequence is applied:

- The Smart Card Interface is enable by setting $\overline{\text{CMDVCC}}$ LOW (RSTIN is High).
- Between t2 (Figure 4) and t5 = 240 μs, RSTIN is reset to LOW and CCLK will start precisely at this moment allowing a precise count of clock cycles before toggling CRST Low to High for ATR (Answer To Reset) request.
- CRST remains LOW until 240 μs; after t5 = 240 μs CRST is enabled and is the copy of RSTIN which has no more control on the clock.

If controlling the clock with RSTIN is not necessary (**Normal Mode**), then $\overline{\text{CMDVCC}}$ can be set LOW with RSTIN LOW. In that case, CLK will start minimum 2 μs after the transition on I/O (Figure 5), and to obtain an ATR, CRST can be set High by RSTIN also about 2 μs after the clock channel activation (T_{act}).

The internal activation sequence activates the different channels according to a specific hardware built−in sequencing internally defined but at the end the actual activation sequencing is the responsibility of the application software and can be redefined by the micro−controller to comply with the different standards and the different ways the standards manage this activation (for example light differences exist between the EMV and the ISO7816 standards).

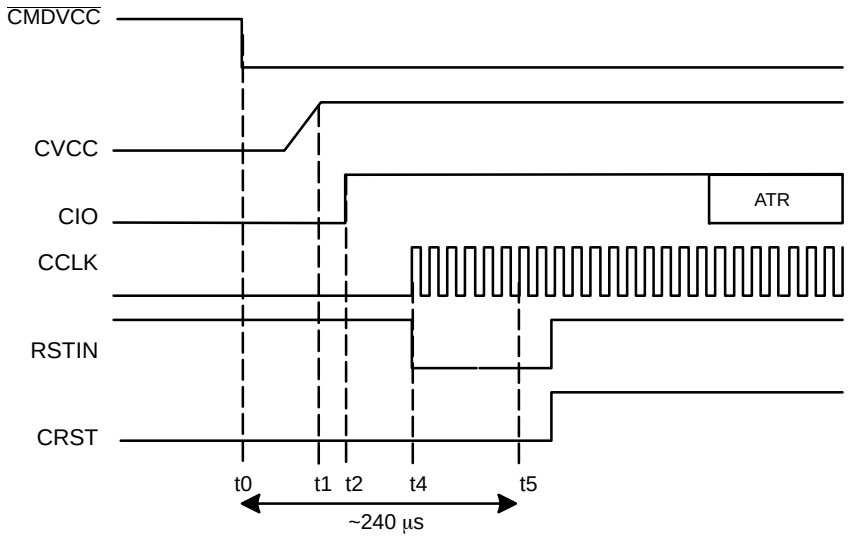


Figure 4. Activation Sequence − RSTIN Mode (RSTIN Starting High)

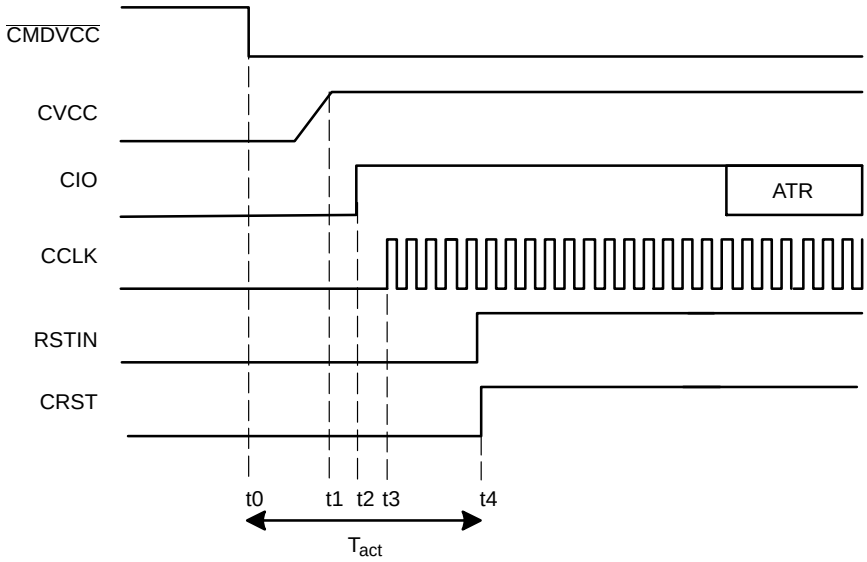


Figure 5. Activation Sequence − Normal Mode

SMART CARD POWER−DOWN

When the communication session is completed the NCN8026A runs a deactivation sequence by setting High $\overline{\text{CMDVCC}}$. The below power down sequence is executed:

- CRST is forced to Low
- CCLK is set Low 12 μs after CRST.
- CI/O, CAUX1 and CAUX2 are pulled Low
- Finally CVCC supply can be shut−off.

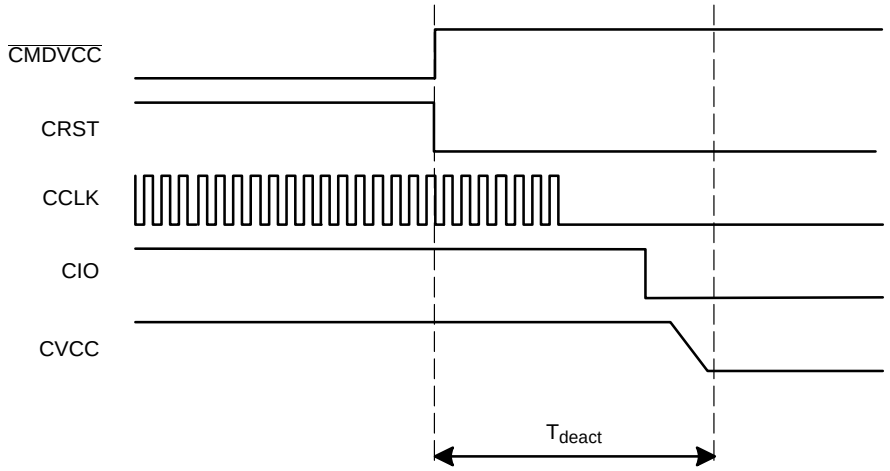


Figure 6. Deactivation Sequence

FAULT DETECTION

In order to protect both the interface and the external smart card, the NCN8026A provides security features to prevent failures or damages as depicted here after.

- Card extraction detection
- V_{DD} under voltage detection
- Short−circuit or overload on CVCC
- DC/DC operation: the internal circuit continuously senses the CVCC voltage (in the case of either over or under voltage situation).
- DC/DC operation: under−voltage detection on V_{DDP}
- Overheating
- Card pin current limitation: in the case of a short circuit to ground. No feedback is provided to the external MPU.

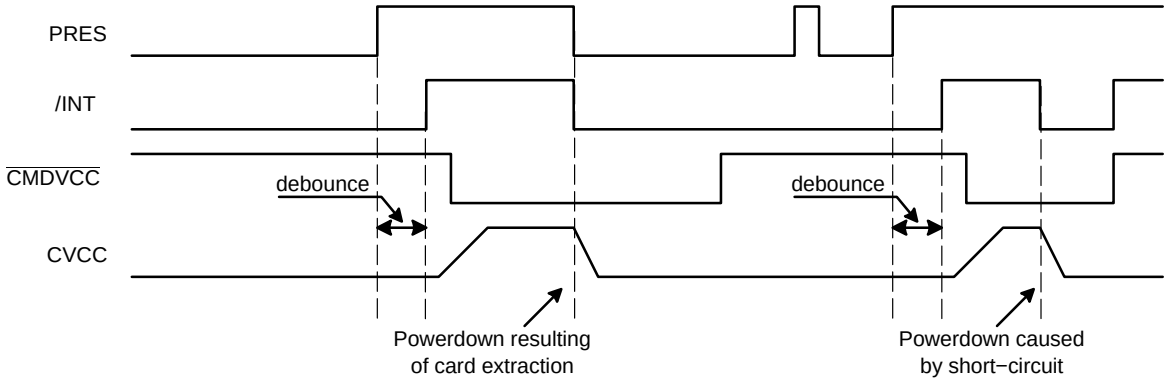


Figure 7. Fault Detection and Interrupt Management

Interrupt Pin Management:

A card session is opened by toggling $\overline{\text{CMDVCC}}$ High to Low.

Before a card session, $\overline{\text{CMDVCC}}$ is supposed to be in a High position. $\overline{\text{INT}}$ is Low if no card is present in the card connector (Normally open or normally closed type). $\overline{\text{INT}}$ is High if a card is present. If a card is inserted ($\overline{\text{INT}}$ = High) and if V_{DD} drops below the UVLO threshold then $\overline{\text{INT}}$ pin drops Low immediately. It switches High when V_{DD} increases again over the UVLO limit (including hysteresis), a card being still present.

During a card session, $\overline{\text{CMDVCC}}$ is Low and $\overline{\text{INT}}$ pin goes Low when a fault is detected. In that case a deactivation is immediately and automatically performed (see Figure 6). When the microcontroller resets $\overline{\text{CMDVCC}}$ to High it can sense the $\overline{\text{INT}}$ level again after having got completed the deactivation.

As illustrated by Figure 7 the device has a debounce timer of 8 ms typical duration. When a card is inserted, output $\overline{\text{INT}}$ goes High only at the end of the debounce time. When the card is removed a deactivation sequence is automatically and immediately performed and $\overline{\text{INT}}$ goes Low.

MULTIPLE CARD OPERATION

The chip select ($\overline{CS}$) feature of the NCN8026A allows the microcontroller to communicate with multiple smart cards, reducing the number of pins used on the microcontroller. For this feature to work, all cards in the system must be present and active at all times (CVCC enabled). When CVCC is deactivated, low impedance active pull−up circuits are enabled on I/Ouc, AUX1uc, and AUX2uc. If any of these pins are shared in a multiple card system, the active pull up circuit can prevent the pin from reaching low logic voltage levels.

Enable CVCC on all cards by toggling $\overline{CMDVCC}$ from high to low on all devices. The $\overline{CS}$ pin is used to enable and disable communication with the smart card without disabling CVCC. When the $\overline{CS}$ pin is logic high, $\overline{CMDVCC}$, VSEL0, VSEL1, CLKDIV1, CLKDIV2, and RSTIN become latched internally in the NCN8026A device. Use the $\overline{CS}$ pin to control communication between specific smart cards.

If I/Ouc and AUXuc pins of multiple NCN8026A devices are connected commonly to the microcontroller, each NCN8026A's $\overline{CMDVCC}$ should be set low to avoid bus collision on I/Ouc, AUX1uc, and AUX2uc. If disabling CVCC on any cards not in use, add a disconnecting function such as an analog switch on the I/Ouc, AUX1uc, and AUX2uc pins on that device.

WHEN CARD IS NOT IN USE

When the NCN8026A is powered on, CVCC is off. Upon power on, I/Ouc, AUX1uc, and AUX2uc pins are driven high with a low impedance active pull−up circuit sourcing about 25 mA. The microcontroller's I/O pins should be set to a high impedance or input state during this time.

When $\overline{CMDVCC}$ is switched from high to low, CVCC turns on. I/Ouc, AUX1uc, and AUX2uc are not driven by the active pull−up circuit when CVCC is enabled and the high−impedance pull−up resistor dominates.

When $\overline{CMDVCC}$ is switched from low to high, CVCC turns off. The I/Ouc, AUX1uc, and AUX2uc pins are driven high again with a low impedance active pull−up circuit sourcing about 25 mA. The microcontroller's I/O pins should be set to a high impedance or input state during this time.

ESD PROTECTION

The NCN8026A includes devices to protect the pins against the ESD spike voltages. To cope with the different ESD voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the micro controller side, or 8 kV when connected with the external contacts (HBM model). Practically, the CRST, CCLK, CI/O, CAUX1, CAUX2, PRES and $\overline{PRES}$ pins can sustain 8 kV. The CVCC pin has the same ESD protection and can source up to 70 mA continuously, the absolute maximum current being internally limited with a max at 150 mA. The CVCC current limit depends on V_{DDP} and CVCC.

APPLICATION SCHEMATIC

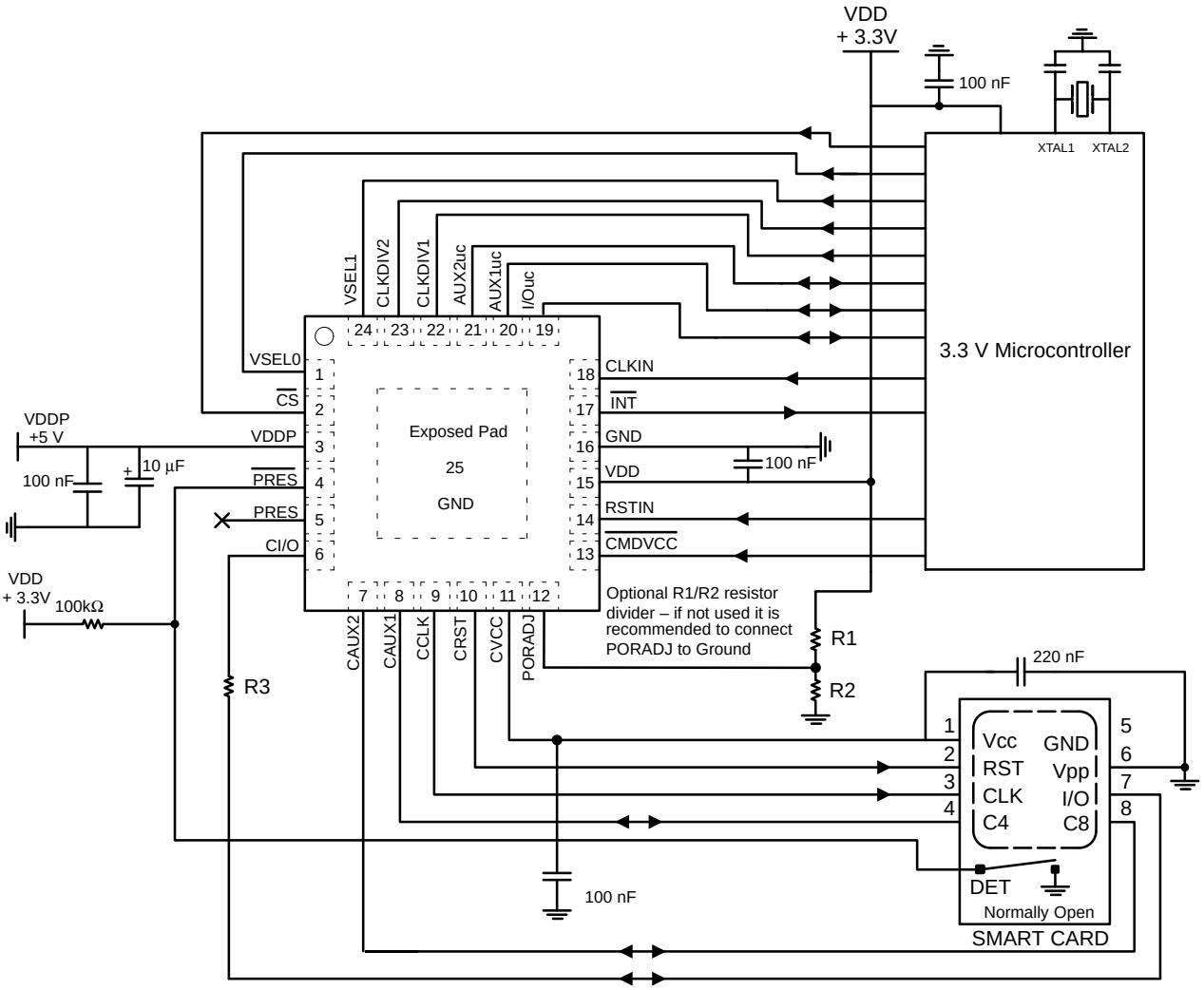


Figure 8. Application Schematic

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Device	Package	Shipping†
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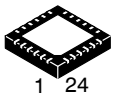
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

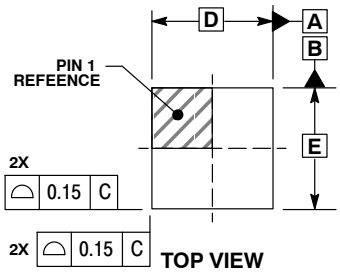
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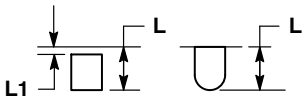
QFN24, 4x4, 0.5P
CASE 485L
ISSUE B

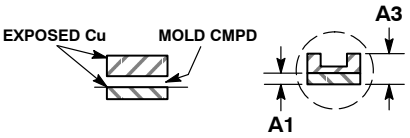
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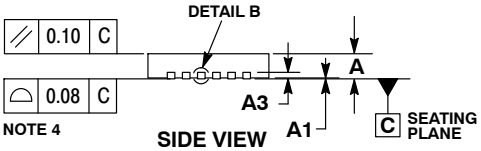


SCALE 2:1



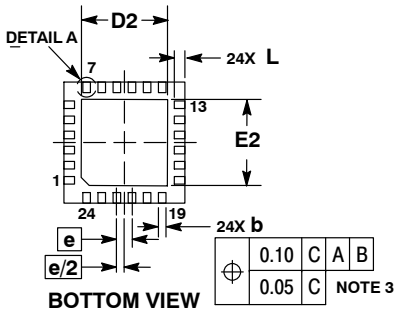






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
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A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.30	0.50
L1	0.05	0.15



GENERIC MARKING DIAGRAM*

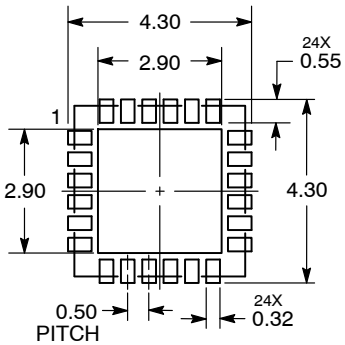


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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