NCP1398B/C

High Performance Resonant Mode Controller with Integrated High-Voltage Drivers

The NCP1398 is a high performance controller for half bridge LLC resonant converters. The integrated high voltage gate driver simplifies layout and reduces external component count. A unique architecture, which includes a 750 kHz Voltage Controlled Oscillator whose control mode permits flexibility when an ORing function is required allows the NCP1398 to deliver everything needed to build a reliable and rugged resonant mode power supply. The NCP1398 provides a suite of protection features with configurable settings allow optimization in any application. This includes: auto−recovery and latch−off over−current protection, brown−out detection, open optocoupler detection, adjustable soft−start and dead−time.

Features

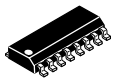
- High−Frequency Operation from 50 kHz up to 750 kHz
- Adjustable Minimum Switching Frequency with ± 3% Accuracy
- Adjustable Dead−Time
- Startup Sequence Via an Externally Adjustable Soft−Start
- Precise and High Impedance Brown−Out Protection
- Latched Input for Severe Fault Conditions, e.g. Over Temperature or OVP
- Timer−Based Auto−Recovery Overcurrent Protection
- Latched Output Short−Circuit Protection
- Open Feedback Loop Protection for NCP1398B Version
- Disable Input for ON/OFF Control
- Skip Mode with Adjustable Hysteresis
- V_{CC} Operation up to 20 V
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Common Collector Optocoupler Connection for Easier ORing
- Internal Temperature Shutdown
- Designed with Pin−to−Adjacent−Pin Short Testing Safety Considerations
- Designed with Open Pin Testing Safety Considerations
- These Devices are Pb−Free and Halogen Free/BFR Free

Typical Applications

- Flat panel Display Power Converters
- High Power AC/DC Adapters
- Computing Power Supplies
- Industrial and Medical Power Sources
- Offline Battery Chargers

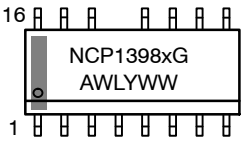
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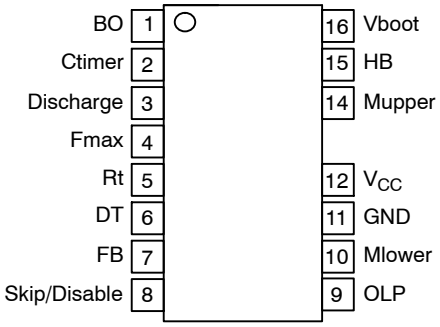
SOIC−16 NB, Less Pin 13
D SUFFIX
CASE 751AM

MARKING DIAGRAM



x	= B or C
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

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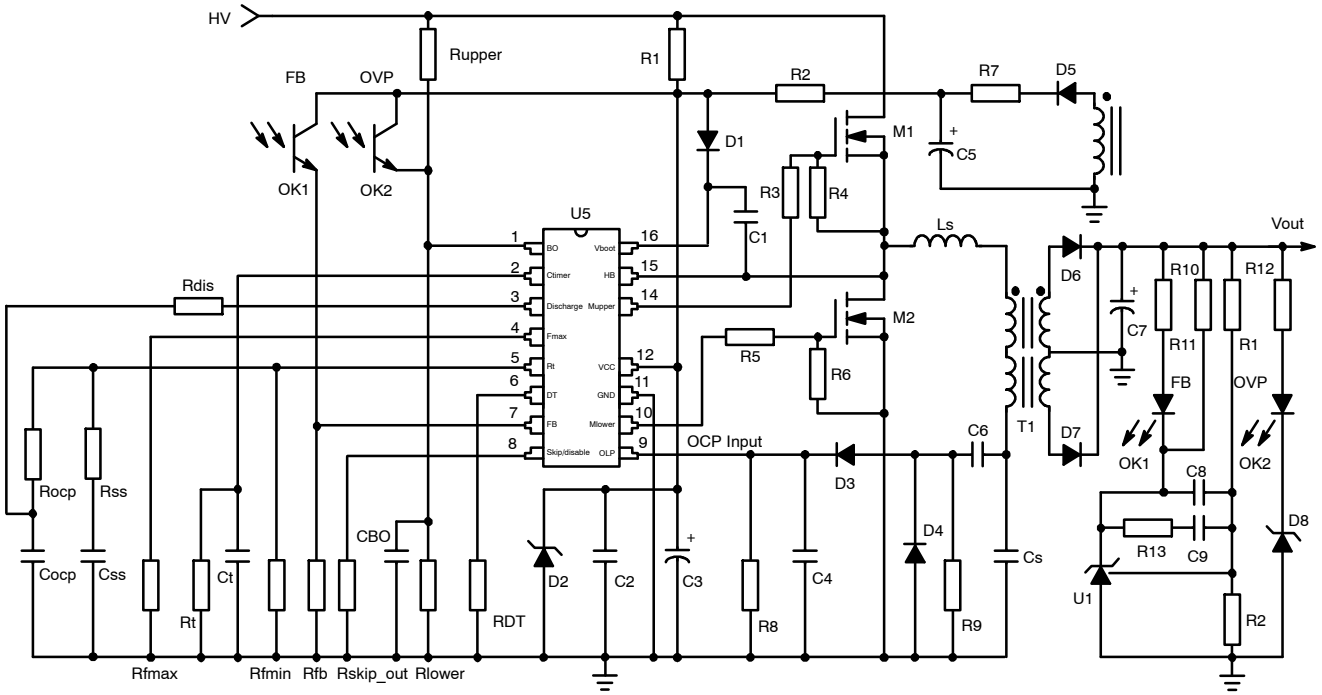


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin N°	Pin Name	Function	Pin Description
1	BO	Brown−Out	Detects low input voltage conditions. When brought above Vlatch (4V), fully latches off the controller.
2	Ctimer	Fault timer duration	Sets the fault timer and auto−recovery durations
3	Discharge	Overload protection	Implements frequency shift in case of overload.
4	Fmax	Maximum frequency clamp	A resistor connected between this pin and GND sets the maximum frequency excursion. Controller enters skip mode and disables drivers if the operating frequency exceeds this adjusted value.
5	Rt	Minimum frequency clamp	Connecting a resistor to this pin, sets the minimum oscillator frequency reached for VFB = 1.1 V. Discharge OCP and Soft Start networks before startup or reset.
6	DT	Dead−time adjust	A simple resistor adjusts the dead−time
7	FB	Feedback	Voltage on this pin modulates operating frequency between adjusted Fmin and Fmax clamps. Starts Fault timer when FB voltage stays below 0.28 V − function not active on NCP1398C version.
8	Skip/Disable	Skip or Disable input	Defines frequency and thus also FB voltage under which the controller returns from skip mode. Upon release, a clean startup sequence occurs if VFB < 0.28 V. During the skip mode, when FB doesn't drop below 0.28 V, the IC restarts without soft start sequence.
9	OLP	Overload protection detection input	Initiates fault timer when asserted. Increases operating frequency via discharge pin to protect application power stage. This input features also latch fault comparator that latches off the IC permanently.
10	Mlower	Low side output	Drives the lower side MOSFET
11	GND	IC ground	−
12	V_{CC}	Supplies the controller	The controller accepts up to 20 V
13	NC	Not connected	Increases the creepage distance
15	Mupper	High side output	Drives the higher side MOSFET
14	HB	Half−bridge connection	Connects to the half−bridge output
16	Vboot	Bootstrap pin	The floating V_{CC} supply for the upper stage

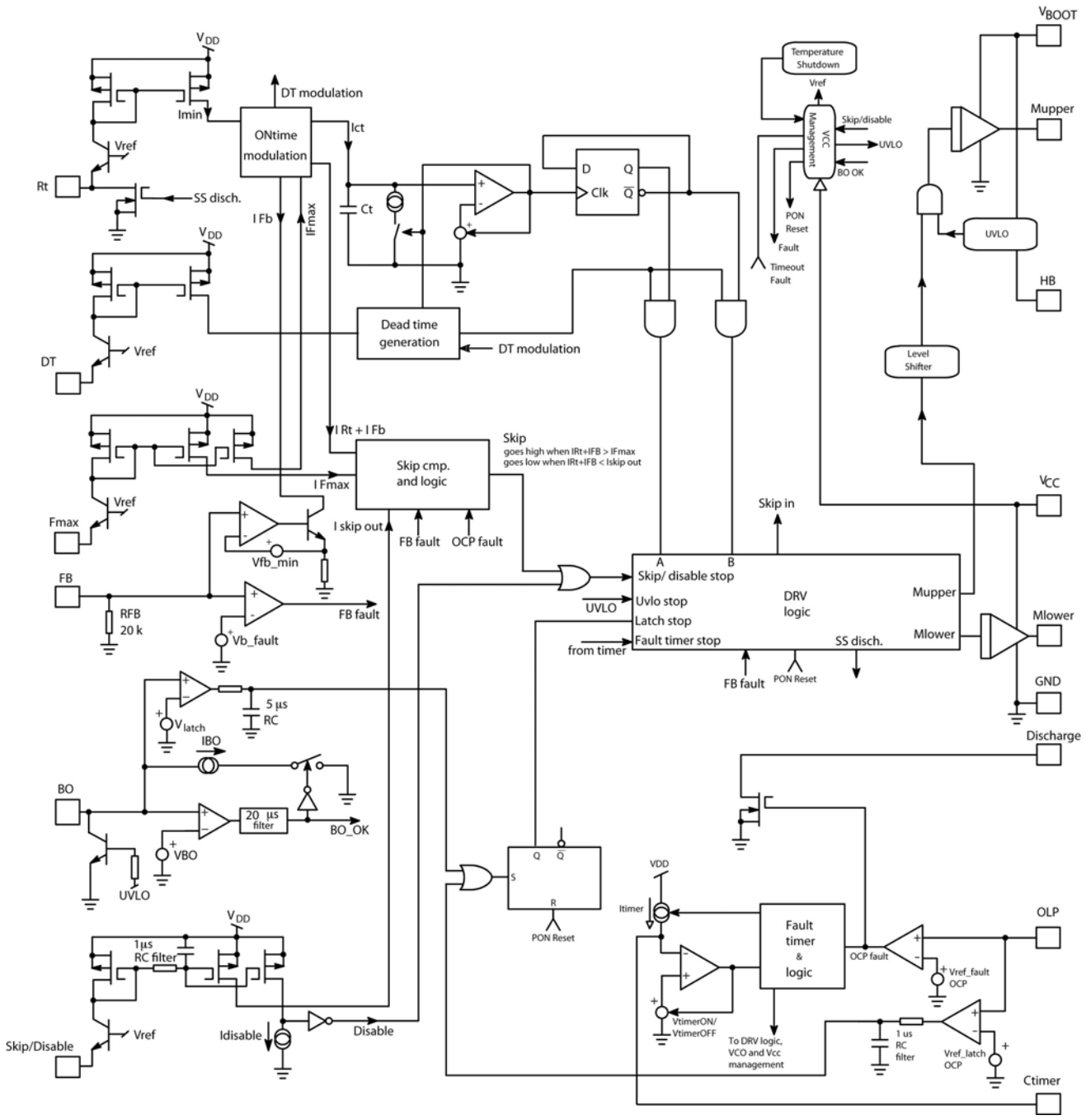


Figure 2. Internal Circuit Architecture – NCP1398C

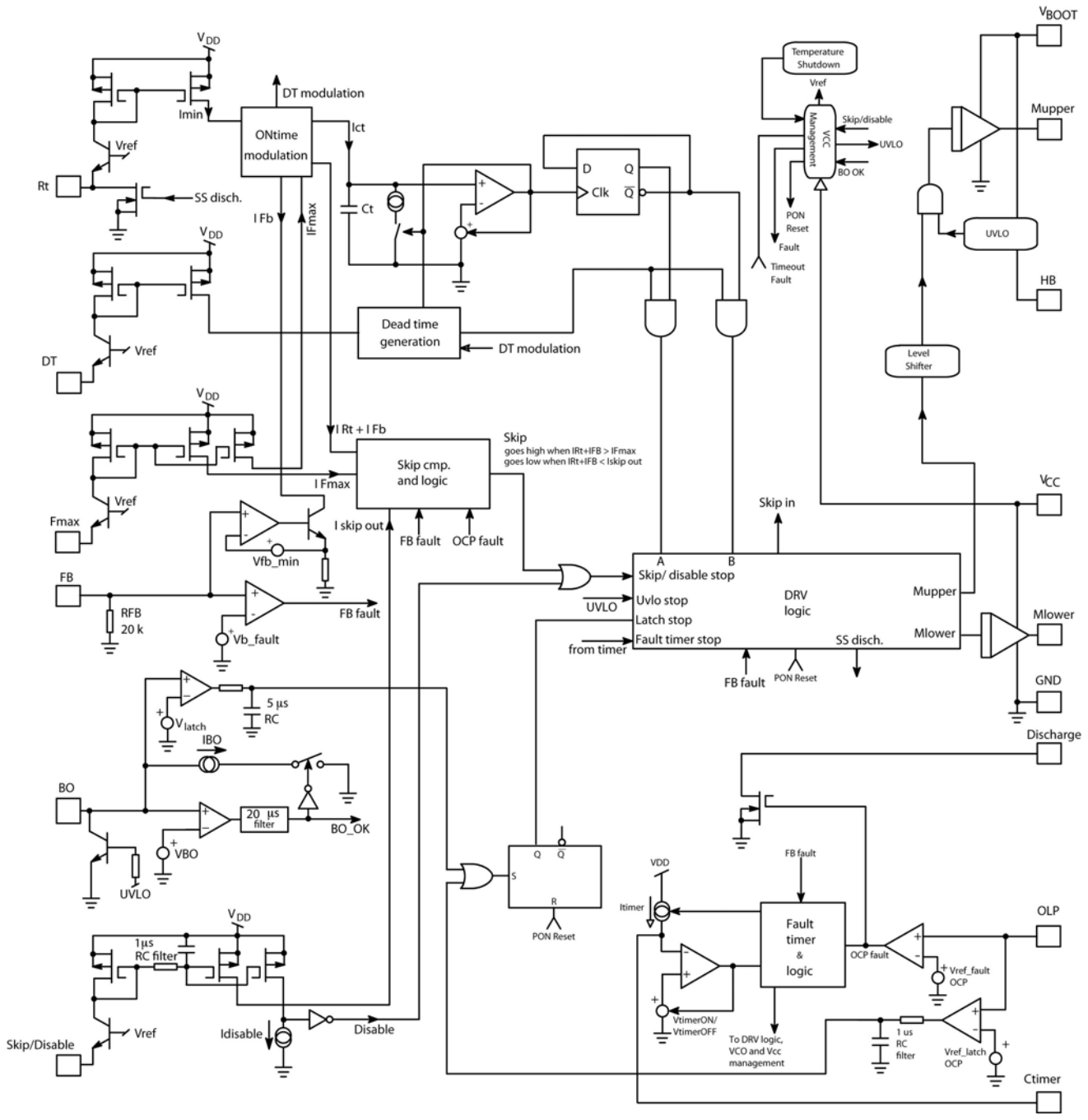


Figure 3. Internal Circuit Architecture – NCP1398B

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage bridge pin	VBRIDGE	−1 to 600	V
Floating supply voltage	VBOOT − VBRIDGE	0 to 20	V
High side output voltage	VDRV_HI	VBRIDGE−0.3 to VBOOT+0.3	V
Low side output voltage	VDRV_LO	−0.3 to V_{CC} + 0.3	V
Allowable output slew rate	dV_{BRIDGE}/dt	50	V/ns
FB and V_{CC} pin voltage (pins 7 and 12)	V_{CC}	−0.3 to 20	V
Maximum voltage, all pins (except pins 7, 12, 14, 15 and 16)	−	−0.3 to 10	V
Thermal Resistance Junction−to−Air, PDIP version	RθJ−A	100	°C/W
Thermal Resistance Junction−to−Air, SOIC version	RθJ−A	130	°C/W
Storage Temperature Range	−	−60 to +150	°C
ESD Capability, HBM model , Except pins 14, 15, 16	−	2	kV
ESD Capability, Machine Model	−	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model 200 V per JEDEC Standard JESD22−A115−A
2. This device meets latch−up tests defined by JEDEC Standard JESD78.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	Turn−on threshold level, Vcc going up	12	9.7	10.5	11.3	V
$VCC_{(min)}$	Minimum operating voltage after turn−on	12	8.7	9.5	10.3	V
$Vboot_{ON}$	Startup voltage on the floating section	16−15	8	9	10	V
$Vboot_{(min)}$	Cutoff voltage on the floating section	16−15	7.4	8.4	9.4	V
Istartup	Startup current, V_{CC} < VCC_{ON}	12	−	−	620	μA
VCC_{reset}	V_{CC} level at which the internal logic gets reset	12	−	6.6	−	V
ICC1+Iboot1	Internal IC consumption, no output load on pin 15/14 − 11/10, Fsw = 300 kHz, Rdt = 10 kΩ, RT = 31 kΩ, RFmax = 7.2 kΩ, RSkip/Disable = 7.9 kΩ, VFb = 3.6 V	12−11 16−15	−	5.1	−	mA
ICC2+Iboot2	Internal IC consumption, 1 nF output load on pin 15/14 − 11/10, Fsw = 300 kHz, Rdt = 10 kΩ, RT = 31 kΩ, RFmax = 7.2 kΩ, RSkip/Disable = 7.9 kΩ, VFb = 3.6 V	12−11 16−15	−	13.3	−	mA
ICC3+Iboot3	Consumption in fault or disable mode, All drivers disabled, Rdt =10 kΩ, RFmin = 31 kΩ, RFmax = 7.2 kΩ, RSkip/Disable = 7.9 kΩ, VFb = 1 V	12−11 16−15	−	1.05	−	mA
ICC4+Iboot4	Consumption in skip mode , All drivers disabled, Rdt =10 kΩ, RFmin = 31 kΩ, RFmax = 7.2 kΩ, RSkip/Disable = 7.9 kΩ, VFb = 5.7 V	12−11 16−15	−	2.2	−	mA
VOLTAGE CONTROL OSCILLATOR (VCO)						
Fsw_min	Minimum switching frequency, Rt = 31 kΩ on pin 5, Vpin 7 = 0.8 V, DT = 300 ns 0 to 125°C −40 to 125°C	5	 58.2 57.2	 60 60	 61.8 61.8	kHz

3. Guaranteed by design.
4. Not tested for NCP1398C.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
VOLTAGE CONTROL OSCILLATOR (VCO)						
Fsw_max	Maximum switching frequency clamp, Rfmax = 7.2 kΩ on pin 4, Vpin 7 ramps up above 5.3 V, DT = 300 ns	4	465	525	585	kHz
DC	Operating duty−cycle symmetry	10−14	48	50	52	%
Tdel	Delay before driver re−start from fault, skip or disable mode	−	−	10	−	μs
Vref_Rt	Reference voltage for Rt pin	5	2.18	2.3	2.42	V
FEEDBACK SECTION						
Rfb	Internal pull−down resistor	7	−	20	−	kΩ
Vfb_min	Voltage on pin 7 below which the VCO has no action and Fmin clamp is reached	7	−	1.1	−	V
Vfb_max	Voltage on pin 7 below which the VCO has no action and Fmax clamp is reached	7	−	5.5	−	V
Vfb_fault	Voltage on pin 7 below which the controller considers the FB fault (Note 4)	7	240	280	320	mV
Vfb_fault_hyste	Feedback fault comparator hysteresis (Note 4)	7	−	45	−	mV
DRIVE OUTPUT AND DEAD−TIME CLAMP						
T_r	Output voltage rise−time @ CL = 1 nF, 10−90% of output signal	14−15/ 12−11	−	40	−	ns
T_f	Output voltage fall−time @ CL = 1 nF, 10−90% of output signal	14−15/ 12−11	−	20	−	ns
R_{OH}	Source resistance	14−15/ 12−11	−	13	−	Ω
R_{OL}	Sink resistance	14−15/ 12−11	−	5.5	−	Ω
T_dead_nom	Dead time with R_{DT} = 10 kΩ from pin 6 to GND	6	250	290	340	ns
T_dead_max	Maximum dead−time with R_{DT} = 71.5 kΩ from pin 6 to GND	6	−	1.9	−	μs
T_dead_min	Minimum dead−time, R_{DT} = 2.8 kΩ from pin 6 to GND	6	−	100	−	ns
IHV_LEAK	Leakage current on high voltage pins to GND	14, 15, 16	−	−	5	μA
FAULT TIMER						
Itimer	Timer capacitor charge current during feedback fault or when Vref_fault < Vpin9 < Vref_OCP	3	165	195	215	μA
T−timer	Timer duration with a 1 μF capacitor and a 1 MΩ resistor, Itimer1 current applied (Note 3)	3	−	19.3	−	ms
T−timerR	Timer recurrence in permanent fault, same values as above (Note 3)	3	−	1.4	−	s
VtimerON	Voltage at which pin 3 stops output pulses	3	3.8	4	4.2	V
VtimerOFF	Voltage at which pin 3 re−starts output pulses	3	0.95	1	1.05	V
Rtimer_dis	Timer discharge switch resistance (Note 3)	1	−	100	−	Ω
BROW−OUT PROTECTION						
IBO_bias	Brown−Out input bias current (Note 3)	1	−	−	0.01	μA
VBO	Brown−Out level	1	0.98	1.008	1.08	V
VBO_hyst	Brown−Out comparator hysterisis	1	−	10	−	mV
Tfl_BO	BO filter duration (Note 3)	1	−	20	−	μs

3. Guaranteed by design.
4. Not tested for NCP1398C.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
BROW−OUT PROTECTION						
IBO	Hysteresis current, Vpin1 < VBO	1	7.5	8.5	9.1	μA
Vlatch	Latching voltage	1	3.7	4	4.3	V
Tfl_BO_latch	BO latch filter duration (Note 3)		–	5	–	μs
SKIP/DISABLE INPUT						
Fskip−out	Skip−out frequency, Rskip/disable = 7.9 kΩ	8	426	480	534	kHz
Idisable	Skip/Disable pin output current below which is the controller disabled	8	–	12	–	μA
Tfl_skip	Skip/Disable input filter time constant (Note 3)	8		1		μs
OVERLOAD PROTECTION						
Vref_Fault_OCP	Reference voltage for Fault comparator	9	0.95	1	1.05	V
Hyste_Fault_OCP	Hysteresis for fault comparator input	9	–	100	–	mV
Vref_latch_OCP	Reference voltage for OCP comparator	9	1.425	1.5	1.575	V
T_OCP_latch	Filtering time constant for OCP latch comparator (Note 3)	9	–	1	–	μs
TSD	Temperature shutdown (Note 3)	–	140	–	–	°C
TSD_hyste	Hysteresis (Note 3)	–	–	30	–	°C

3. Guaranteed by design.
4. Not tested for NCP1398C.

TYPICAL CHARACTERISTICS

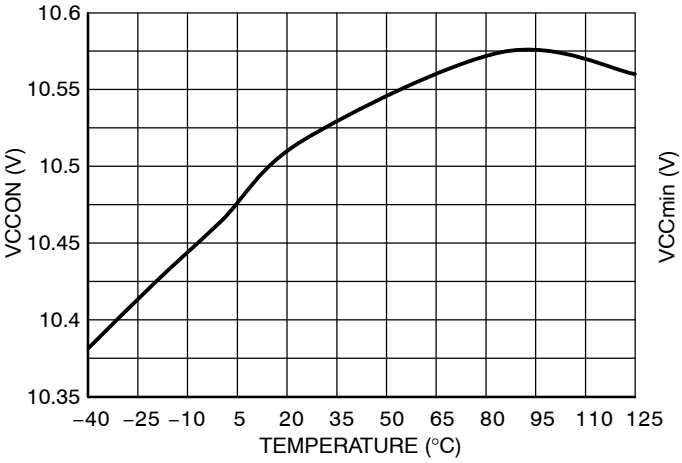


Figure 4. $V_{CC(on)}$ Threshold

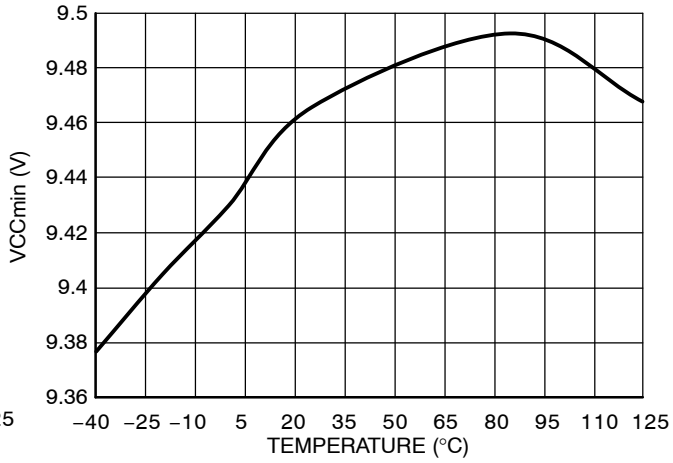


Figure 5. $V_{CC(min)}$ Threshold

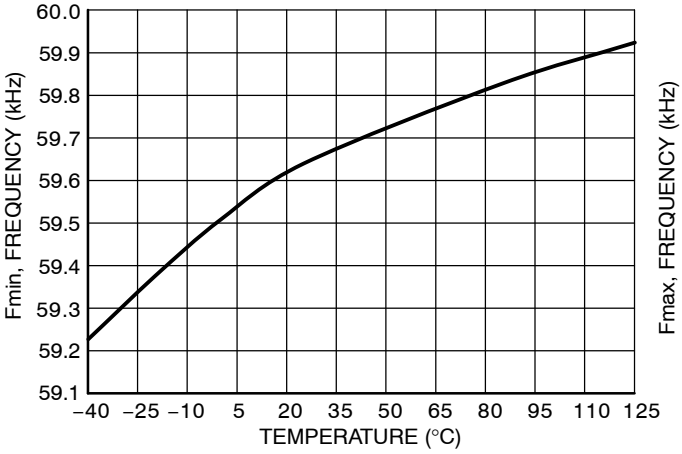


Figure 6. $F_{SW(min)}$ Frequency Clamp

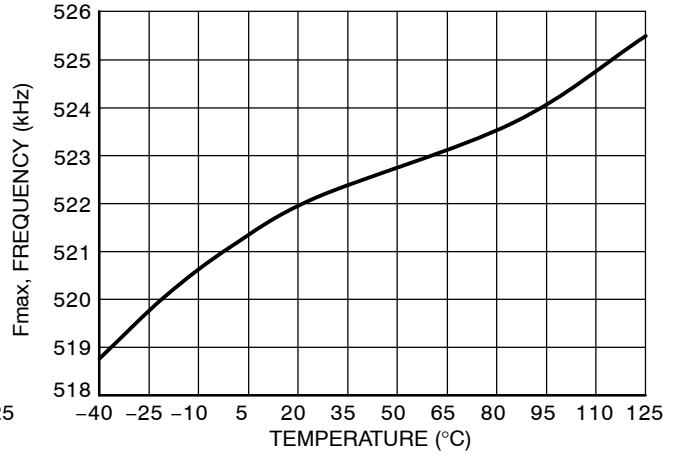


Figure 7. $F_{SW(max)}$ Frequency Clamp

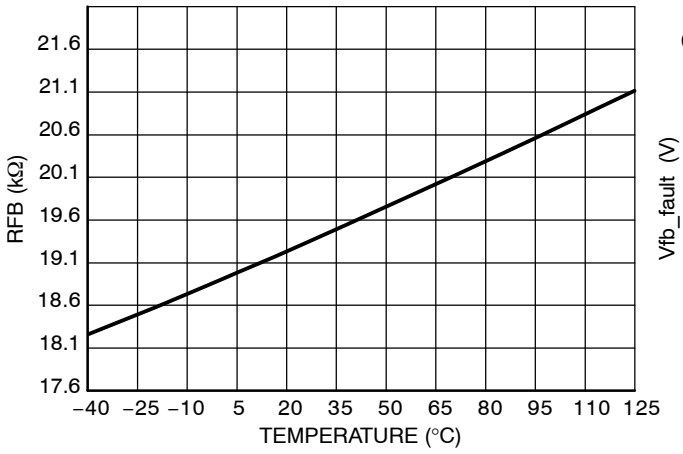


Figure 8. Pulldown Resistor (R_{FB})

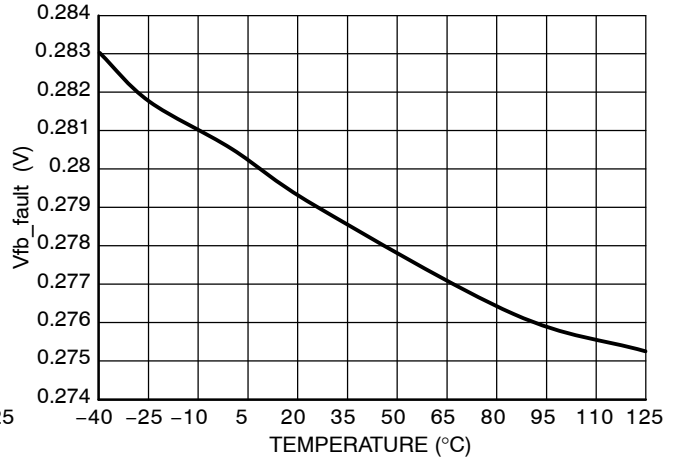


Figure 9. FB Fault Reference (V_{fb_Fault})

TYPICAL CHARACTERISTICS

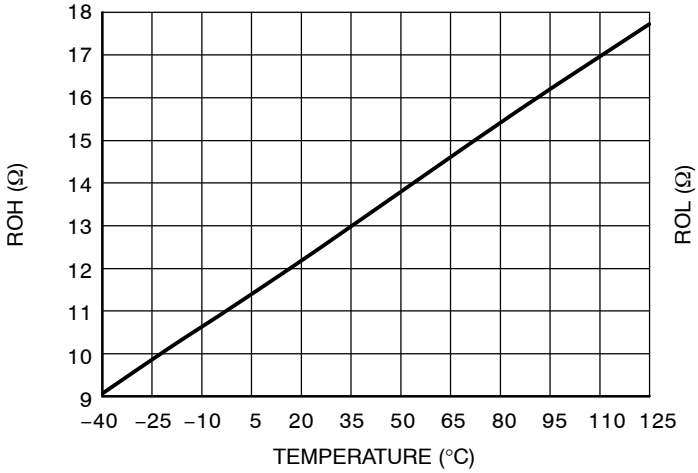


Figure 10. Source Resistance (ROH)

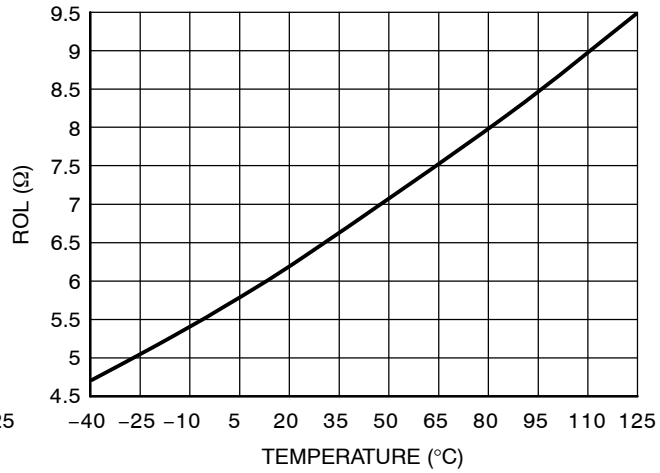


Figure 11. Sink Resistance (ROL)

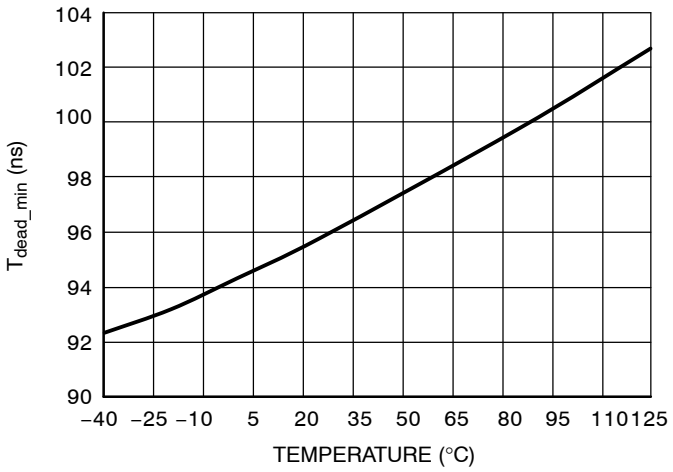


Figure 12. $T_{dead(min)}$

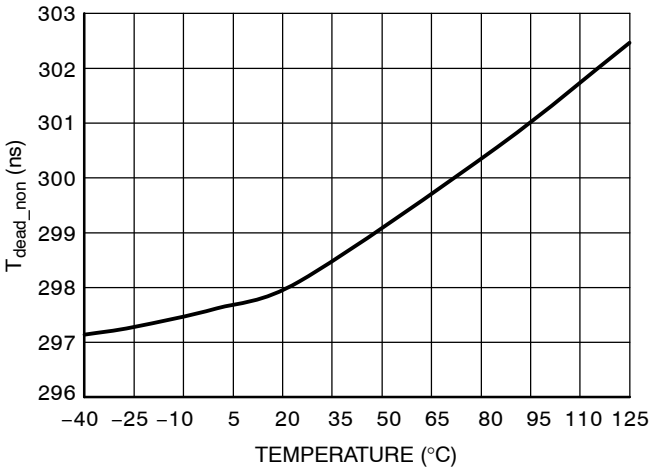


Figure 13. $T_{dead(nom)}$

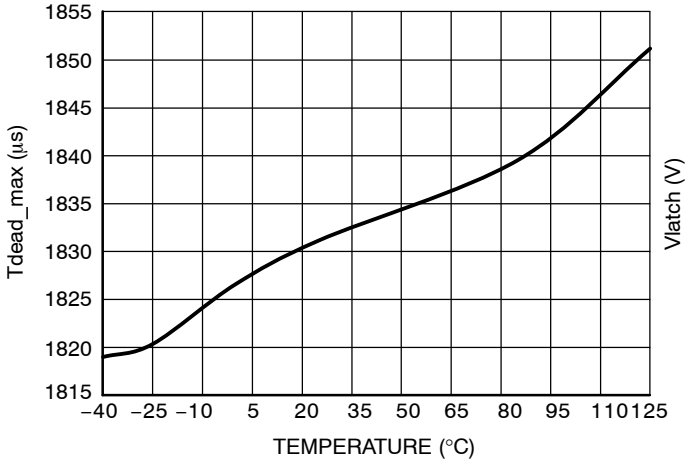


Figure 14. $T_{dead(max)}$

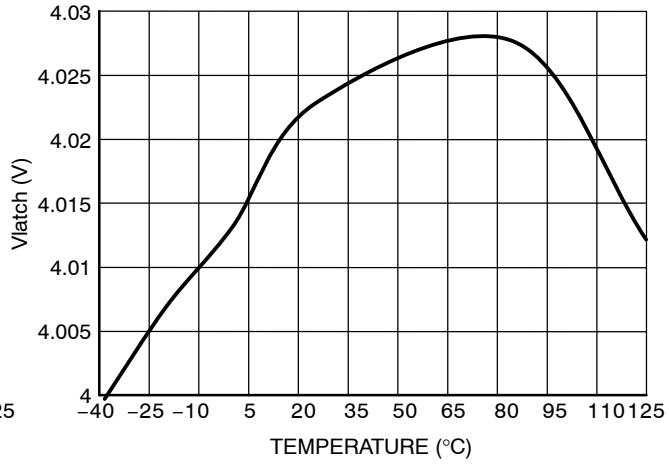


Figure 15. Latch Level (V_{latch})

TYPICAL CHARACTERISTICS

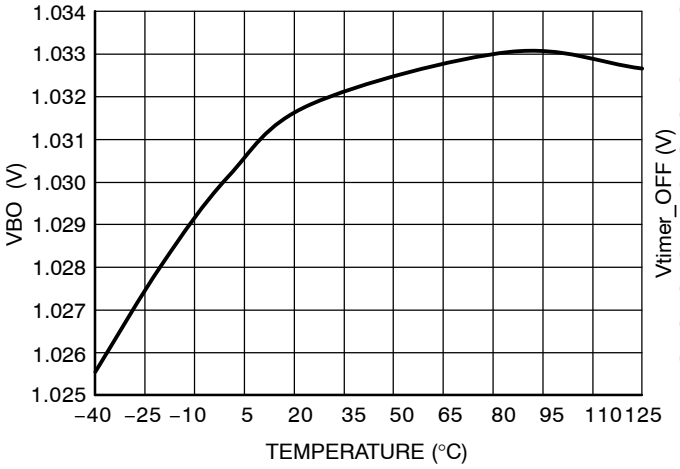


Figure 16. Brown−Out Reference (VBO)

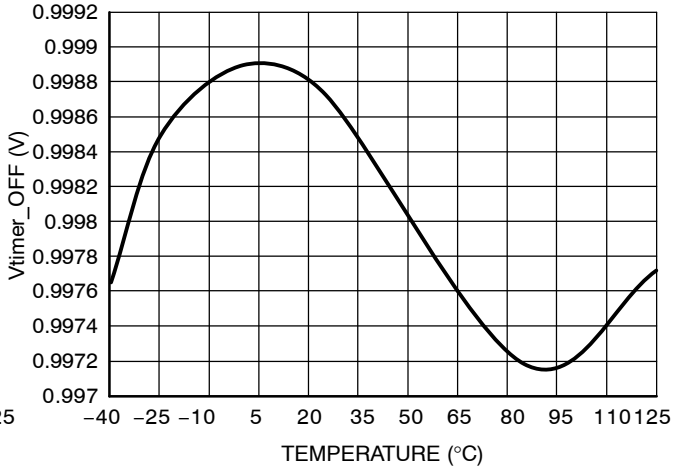


Figure 17. Fault tmr. Reset Voltage ($V_{timer(off)}$)

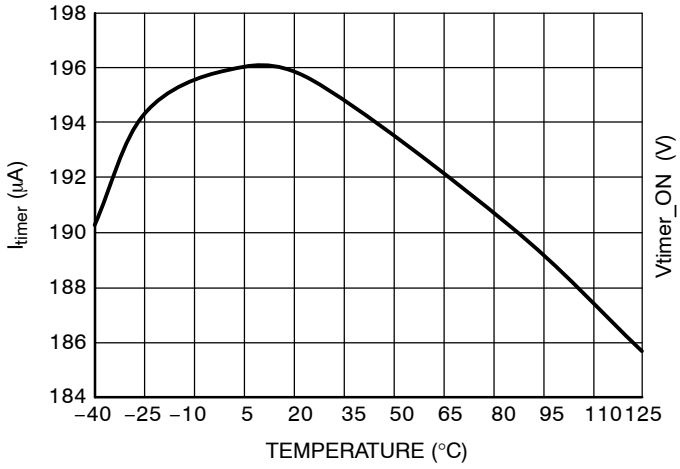


Figure 18. C_{timer} Charging Current (I_{timer})

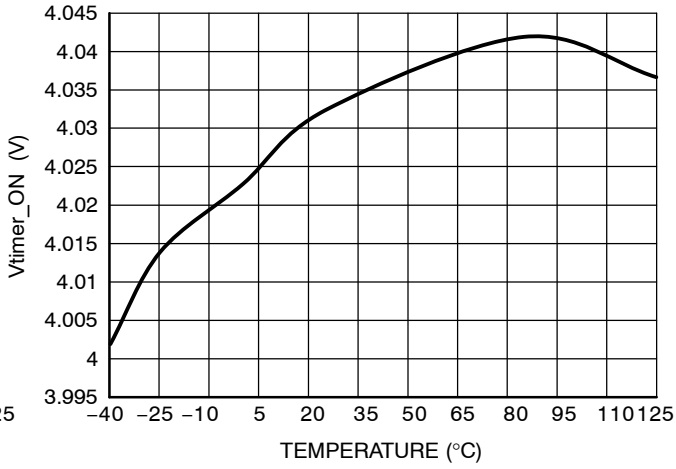


Figure 19. Fault Timer Ending Voltage ($V_{timer(on)}$)

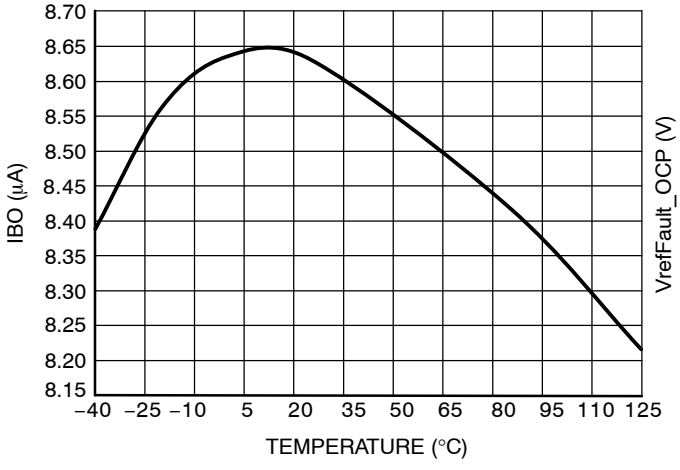


Figure 20. Brown−Out Hysteresis Current (IBO)

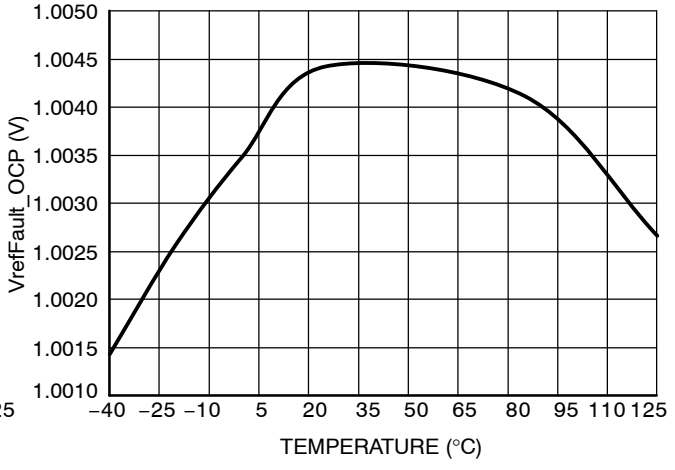


Figure 21. OCP Fault Reference (Vref_Fault_OCP)

TYPICAL CHARACTERISTICS

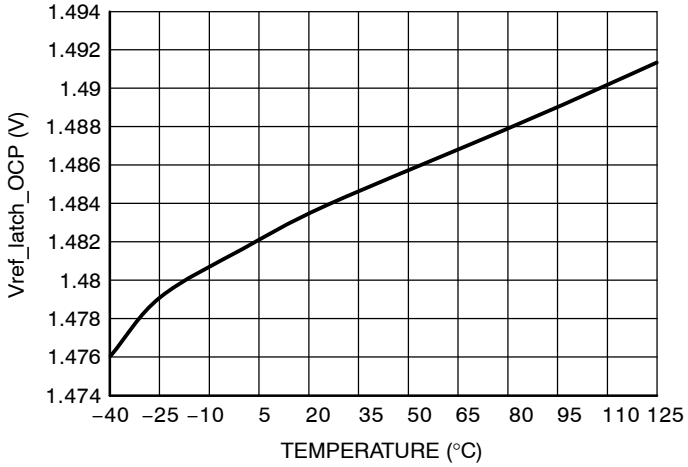


Figure 22. OCP Latch Reference ($V_{ref_latch_OCP}$)

APPLICATION INFORMATION

The NCP1398 includes all necessary features to help building a rugged and safe switch−mode power supply. The below bullets detail the benefits brought by implementing the NCP1398 controller:

- **Wide frequency range**: A high−speed Voltage Control Oscillator allows an output frequency excursion from 50 kHz up to 750 kHz on Mlower and Mupper outputs.
- **User adjustable dead−time**: Controller provides possibility to adjust optimum dead−time based on application parameters. The dead−time is modulated from this adjusted value with operating frequency i.e. dead−time period is reducing when frequency goes up.
- **Adjustable soft−start**: Every time the controller starts to operate (power on), the switching frequency is pushed to the programmed starting value that is defined by external components connected to Rt pin. Frequency then slowly moves down toward the minimum frequency, until the feedback loop closes. The Rt pin discharges the Soft Start capacitor before any IC restart except the restart from skip mode.
- **Adjustable minimum and maximum frequency excursion**: Due to a single external resistor, the designer can program lowest frequency point, obtained in lack of feedback voltage (at the end of the startup sequence or under overload conditions). Internally trimmed capacitors offer a ±3% precision on the selection of the minimum switching frequency. The adjustable upper frequency clam being less precise to ±6%.
- **Brown−Out detection**: To avoid operation from a low input voltage, it is interesting to prevent the controller from switching if the high−voltage rail is not within the right boundaries. Also, when teamed with a PFC front−end circuitry, the brown−out detection can ensure a clean start−up sequence with soft−start, ensuring that the PFC is stabilized before energizing the resonant tank. The BO input features an 8.5 μA hysteresis current to assure the lowest consumption from the sensed bulk voltage input.
- **Adjustable fault timer**: When a fault is detected on the OLP input or when the FB path is broken, Ctimer pin starts to charge an external capacitor. If the fault is removed, the timer opens charging path and supply continues in operation without any interruption. When the timer reaches its selected duration (via a capacitor on pin 2), all pulses are stopped. The controller now waits for the discharge via an external resistor on pin 2 to issue a new clean startup sequence via soft−start.
- **Cumulative fault events**: In the NCP1398, the timer capacitor is not reset when the fault disappears. It actually integrates the information and cumulates the occurrences. A resistor placed in parallel with the capacitor will offer a simple way to adjust the discharge rate and thus the auto−recovery retry rate.
- **Overload protection**: The overload input (OLP) is specifically designed to protect LLC application during overload or short circuit conditions. In case the voltage on this input grows above first OLP threshold, the Itimer current source is activated and Fault timer is initiated. The discharge pin is activated in the same time to increase operating frequency of the converter and thus to limit primary current. The second OLP threshold is implemented to stop the drivers fully in case of critical fail. The controller then latches off permanently until V_{CC} goes below VCC_reset.
- **Skip cycle possibility**: The NCP1398 features skip cycle mode operation with adjustable hysteresis to allow output regulation under light load or no−load conditions while keeping high efficiency.
- **Open feedback loop detection − NCP1398B only**: Upon start-up or anytime during operation, when the FB signal is missing, the fault timer starts to charge timer capacitor. If the loop is really broken, the FB level does not grow-up before the timer ends charging. The controller then stops all pulses and waits until the timer pin voltage collapses to 1 V typically before a new attempt to re-start, via the soft-start. If the optocoupler is permanently broken, a hiccup takes place.

Voltage−Controlled Oscillator

The VCO section features a high−speed circuitry allowing operation from 100 kHz up to 1.5 MHz. However, as a division by two internally creates the two Q and /Q outputs, the final effective signal on output Mlower and Mupper switches between 50 kHz and 750 kHz. The VCO is configured in such a way that if the feedback pin voltage goes up, the switching frequency also goes up. Figure 23 shows internal architecture of the VCO.

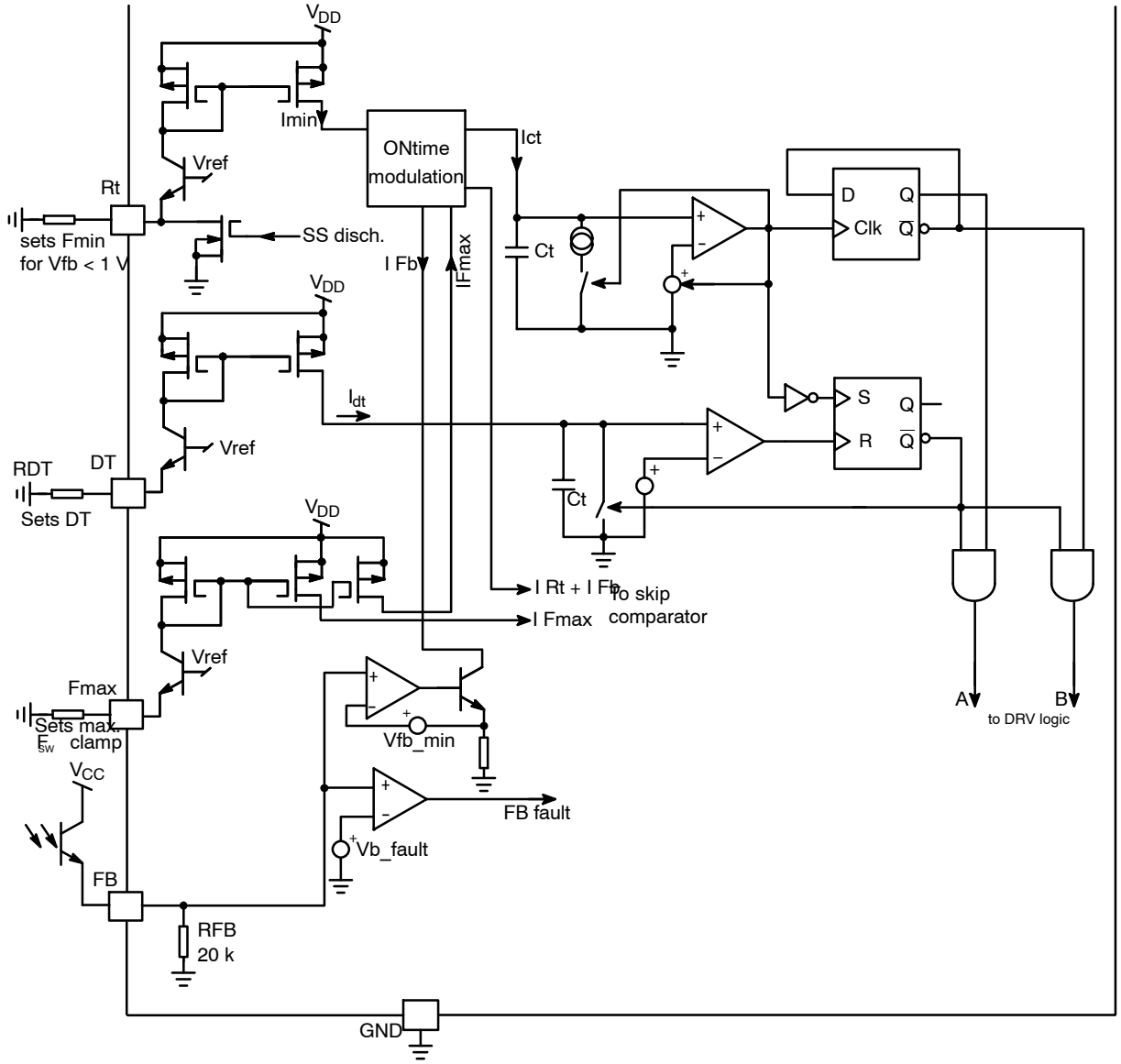


Figure 23. The Simplified VCO Architecture

When designing a resonant SMPS the designer needs to program the minimum and maximum switching frequencies to assure correct and reliable operation. The minimum switching frequency clamp adjustment accuracy is critical because this parameter defines maximum power the converter can deliver for given bulk voltage. The Fmin parameter is thus trimmed to ±3% tolerance in the NCP1398 controller to assure application reproducibility in manufacturing. The minimum frequency clamp, that is fully user adjustable via a resistor connected to the Rt pin, is reached when the feedback loop is not closed. It can happen during the startup sequence, a strong output transient loading or during short−circuit conditions.

The maximum operating frequency clamp, that is defined by the value of resistor connected between Fmax pin and GND, dictates the minimum output power that is needed to maintain output voltage regulation. This parameter, adjusts the threshold of when the part enters skip mode. Precision of the Fmax clamp is thus guaranteed to ±12 %.

The operating frequency is modulated by the secondary regulator via the FB pin in most applications. The frequency changes between minimum (Fmin) and maximum (Fmax)

adjusted clamps when the FB volatge swigs from 1.1 V to 5.5 V – refer to Figure 24. The internal resistor pulls the FB pin naturally down when the regulation loop is opened or if the application is in overload. The FB fault comparator initiates fault timer for NCP1398B version (refer to the Fault Timer section on Page 21) once the FB pin voltage drops below 0.28 V. By implementing this feature the NCP1398B controller increases application safety by keeping it turned off for a significant portion of time once an FB fault occurs.

If we take the default FB pin excursion numbers, 1.1 V – 50 kHz, 5.5 V – 750 kHz, then the VCO maximum slope will be:

$$\frac{750k - 50k}{4.4} = 159\ kHz/V \qquad \text{(eq. 1)}$$

Figures 24 and 25 portray the frequency evolution depending on the feedback pin voltage level for a different frequency clamp combinations.

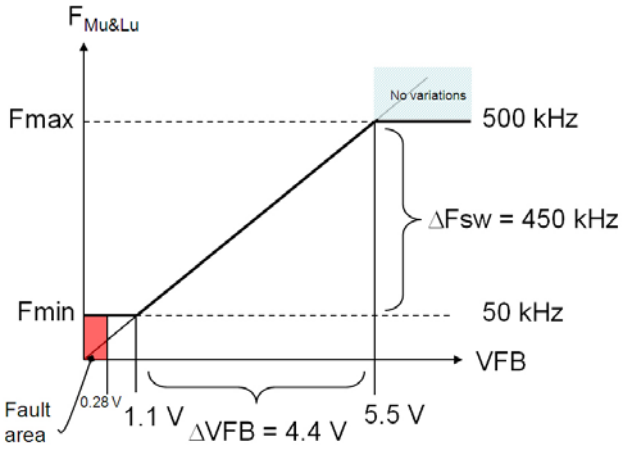


Figure 24. Maximal Default Excursion, Rt = 34.7 kΩ on Fmin Pin and Rfmax = 7.2 kΩ on Fmin Pin

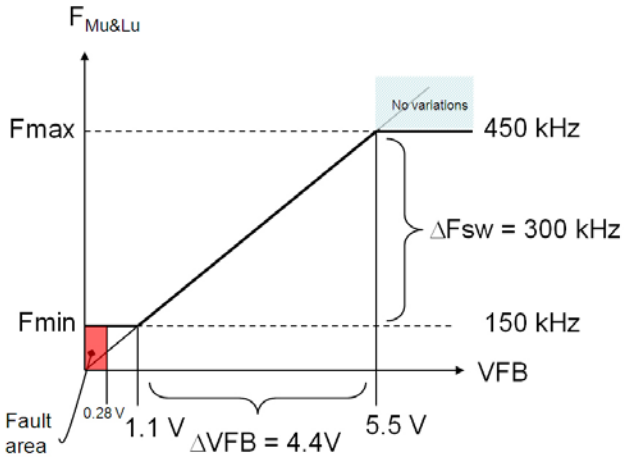


Figure 25. Here a Different Minimum Frequency Was Programmed as Well as the Maximum Frequency Clamp

Please note that the previous small−signal VCO slope from Figure 24 has now been reduced to 300k / 4.4 = 68 kHz/V on Mupper and Mlower outputs. This offers a mean to magnify the feedback excursion on systems where the load range does not generate a wide switching frequency excursion. Due to this option, it is possible to implement skip cycle at light loads.

The selection of the three setting resistors Fmin, dead−time and Fmax clamp) requires the usage of the selection charts displayed below:

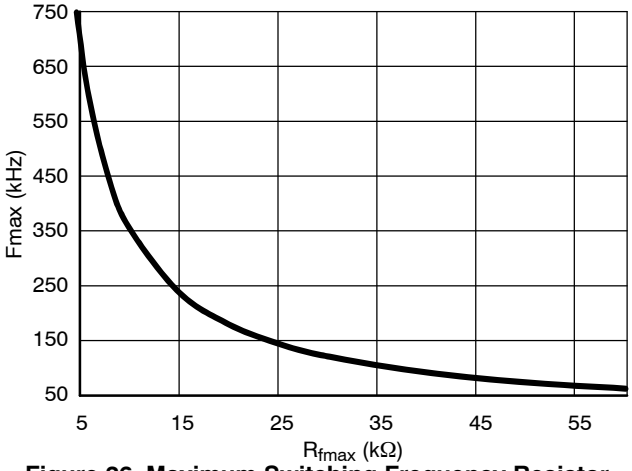


Figure 26. Maximum Switching Frequency Resistor Selection Depending on the Adopted Minimum Switching Frequency

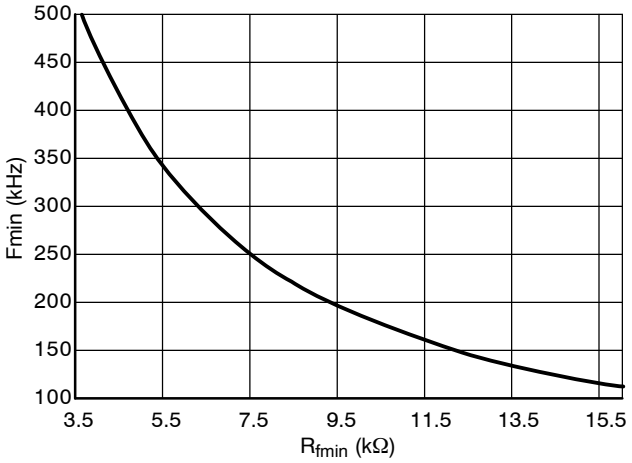


Figure 27. Minimum Switching Frequency Resistor Selection

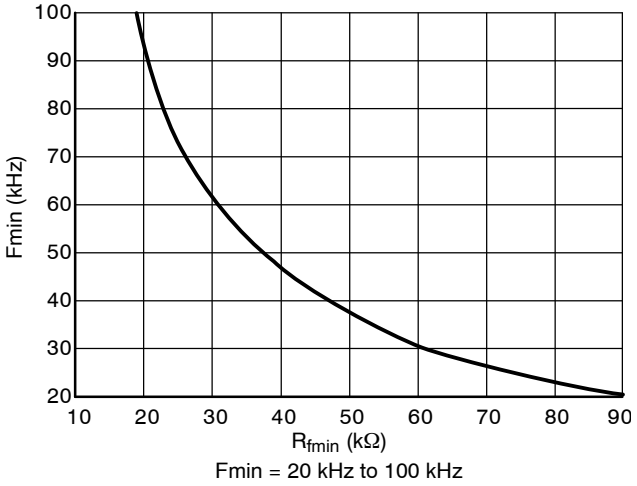


Figure 28. Minimum Switching Frequency Resistor Selection

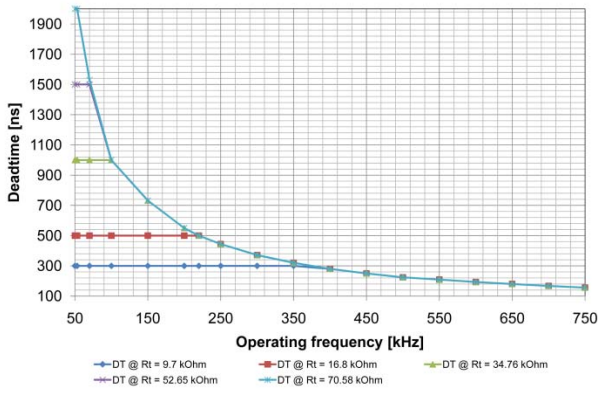


Figure 29. Dead−Time Clamp Resistor Selection

ORing Capability

If for any particular reason, there is a need for a frequency variation linked to an event appearance (instead of abruptly stopping pulses), then it is possible to pull up the FB pin using other sweeping loops than regular feedback. Several diodes can easily be used to perform the job in case of reaction to a fault event or to regulate on the output current (CC operation). Figure 30 shows how to do implement this technique.

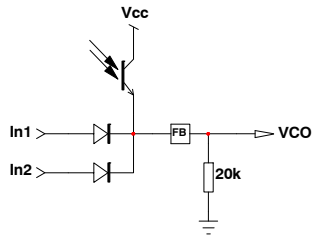


Figure 30. Due to the FB Configuration, Loop ORing is Easy to Implement

The oscillator configuration used in this IC also offers an easy way to connect additional pull down element (like optocoupler or bipolar transistor) directly to the Rt pin to modulate switching frequency if needed – refer to Figure 31.

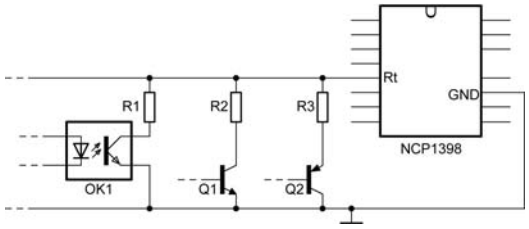


Figure 31. Other Possibilities How to Modulate Operating Frequency of the NCP1398 Using Direct Connection to Rt Pin

Dead−Time Control

Dead−time control is an absolute necessity when the half−bridge topology is used. The dead−time technique consists of inserting a period during which both high and low side switches are off. The needed dead−time amount depends on several application parameters like: magnetizing inductance, total parasitic capacitance of the bridge and maximum operating frequency.

The needed dead−time (or off time for ZVS preparation) is defined by RDT resistor connected between pin 6 and GND. The dead−time can be adjusted from 100 ns to 2 μs – refer to DT adjust characteristic in Figure 29. The dead−time period is placed by dead−time generator in the beginning of each on−time cycle – refer to Figure 2 and 32.

Note that external dead−time modulation is possible if needed. This can be achieved similarly to operating frequency modulation – refer to Figure 31 i.e. by injecting or pulling out current into DT pin.

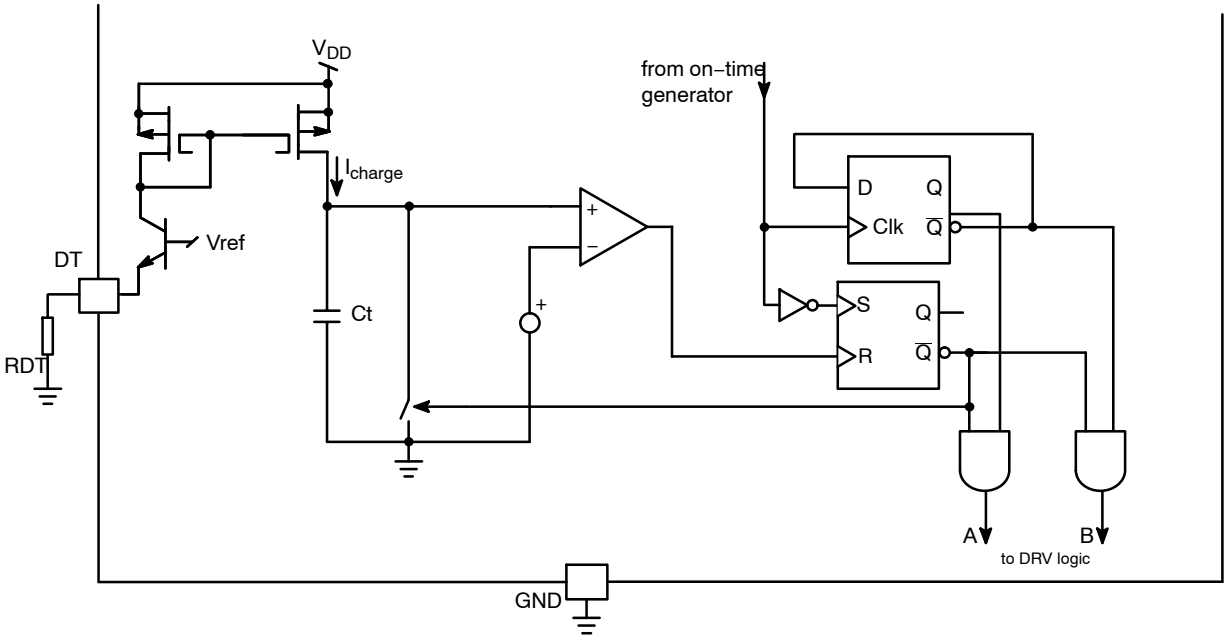


Figure 32. Dead−Time Generation

Soft−Start Sequence

In resonant controllers, a soft−start is needed to avoid applying the full current suddenly into the resonant circuit. The soft−start duration is fully adjustable using external components on this controller. There are normally two RC networks connected to the Rt pin when using NCP1398 – refer to Figure 33. The first network, formed by Rss and Css, is used to program main soft−start period duration. This soft−start period usually lasts from 5 ms to 10 ms, depends on application. The second RC network, formed by Rocp and Cocp components, is implemented to prepare overload protection via discharge pin when OLP input detects fault. The time constant of this RC network is usually selected to < 1 ms to assure fast enough transient response of the OLP system. It should be noted that both RC networks are discharged before application startup thus the "dual soft−start" sequence is present in the application. The startup frequency is given by parallel combination of Rocp, Rss and Rt resistors. The Cocp capacitor then charges in relatively short time so the regular soft−start continues until the Css capacitor charges to Vref_Rt level. As the soft−start capacitor charges up, the frequency smoothly decreases down, towards adjusted Fmin clamp. Of course, practically, the feedback loop is supposed to take over the VCO lead as soon as the output voltage has reached the target. If not, then the minimum switching frequency is reached and a fault is detected on the feedback and OLP pins.

The Rt pin is held low when controller is disabled, except in skip mode. The Css and Cocp capacitors are thus discharged before new restart. The Css capacitor is discharging via Rss resistor thus some minimum off time is needed before restart to assure correct soft−start. Optional discharge diode Ddis can be used between Css capacitor and Rt pin in applications where short restart period is required.

Please note that the soft−start and OCP capacitors are discharged before following sequences:

- startup sequence
- auto−recovery burst mode
- brown−out recovery
- temperature shutdown recovery
- recovery from disable mode if Vfb < Vfb_fault

The skip mode undergoes a special treatment. Since we want to implement skip cycle we cannot activate the soft−start every time when the controller stops the operations in low power mode. Therefore, no soft−start occurs when controller returns from skip mode to offer the best skip cycle behavior. However, it is very possible to combine skip cycle and true disable modes e.g. by driving Skip/disable pin by external current to disable controller operation. In that case, if a disable signal maintains the skip/disable input activated long enough to bring the feedback level down (below Vfb_fault level), then the soft−start discharge is activated.

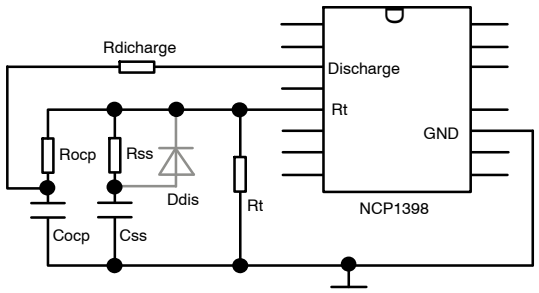


Figure 33. Soft−Start and OLP Components Arrangement

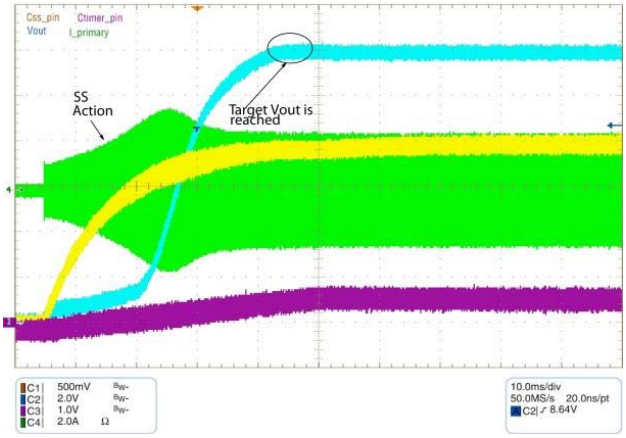


Figure 34. A Typical Start−up Sequence on a LLC Converter Using NCP1398

Brown−Out Protection

The resonant tank of an LLC converter is always designed for specific input voltage range. Operation below minimum designed bulk voltage level would result in current overstress of converter primary power stage. The NCP1398 offers Brown−Out input (BO) that allows for precise bulk voltage turn−on and turn−off levels adjustment. The internal circuitry, depicted by Figure 35, offers a way to observe the high−voltage (Vbulk) rail. A high−impedance resistive divider made of Rupper and Rlower, brings a portion of the Vbulk rail to BO pin. The Current sink (IBO) is active below the Vbulk turn−on level. Therefore, the turn−on level is higher than the one given by the division ratio of resistive divider. To the contrary, when the internal BO_OK signal is high, i.e. application is running, the IBO sink is disabled. The Vbulk turn−off level is thus given by BO comparator reference voltage and resistor divider ratio only. Advantage of this solution is that the Vbulk turn−off level reaches minimum error. This error is given only by VBO reference and resistor divider precisions and is not affected by IBO hysteresis current tolerance. The NCP1398 thus allows better resonant tank optimization.

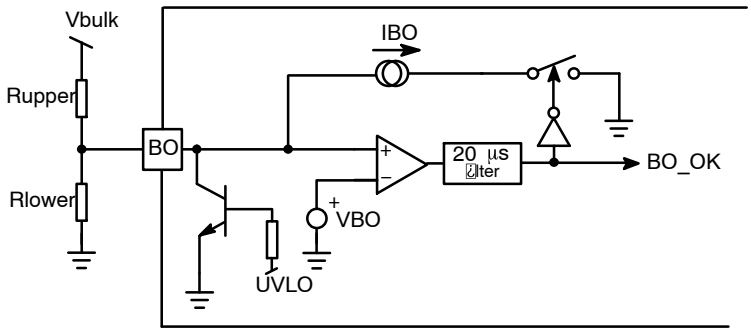


Figure 35. The Internal Brown−out Input Configuration

The turn−on and turn−off levels can be calculated using below equations:

IBO is on

$$V_{BO} + V_{BOhyst} = V_{bulk_ON} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad \text{(eq. 2)}$$

IBO is off

$$V_{BO} = V_{bulk_OFF} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad \text{(eq. 3)}$$

We can extract R_{lower} from Equation 3 and plug it into Equation 2, then solve for R_{upper}:

$$R_{lower} = \frac{\frac{V_{bulk_ON} \cdot V_{BO}}{V_{bulk_OFF}} - V_{BO} - V_{BOhyst}}{I_{BO} \cdot \left(1 - \frac{V_{BO}}{V_{bulk_OFF}} \right)} \quad \text{(eq. 4)}$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk_OFF} - V_{BO}}{V_{BO}} \quad \text{(eq. 5)}$$

If we decide to turn−on our converter for V_{bulk_ON} equal to 400 V and turn it off for V_{bulk_OFF} equal to 350 V, then for IBO = 8.5 μA, V_{BOhyst} = 10 mV and V_{BO} = 1.008 V we obtain:

R_{upper} = 5.47 MΩ

R_{lower} = 15.81 kΩ

Figure 36 simulation results confirms our calculations.

The power dissipation for V_{bulk} = 325 Vdc (i.e. for the case the PFC and LLC stages are off but bulk is still connected to rectified 230 Vac mains – like in standby mode) can be calculated as: 325^2 / 5.516 MΩ = 19 mW.

Note that the BO pin is pulled down by internal switch until the VCC−on level is available on pin 10. This feature assures that the BO pin won't charge up before IC starts operation. The IBO hysteresis current sink is activated and BO discharge switch disabled once the V_{CC} crosses VCC_on threshold. The BO pin voltage then ramps up naturally according to BO divider information. The BO comparator then authorizes operation or not – depends on the Vbulk level.

Small IBO hysteresis current of the NPC1398 allows increasing the BO divider resistance and thus reducing application power consumption during standby mode. On the other hand, the high impedance divider could be noise sensitive due to capacitive coupling to HV switching traces in the application. Thus the 20 μs filter is added after the BO comparator to increase noise immunity. Despite the internal filter, it is recommended to keep correct layout for BO divider resistors and use external filtering capacitor on BO pin if one wants to achieve precise BO detection.

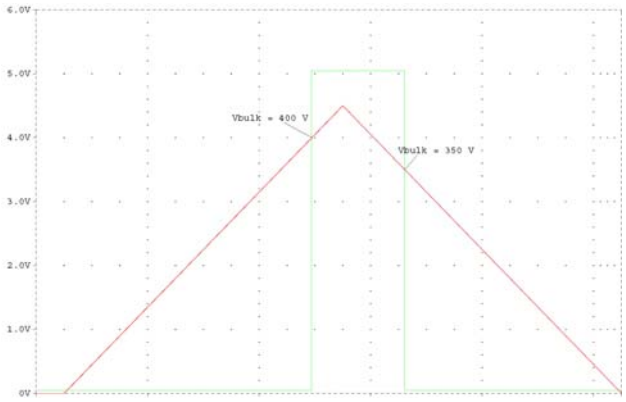


Figure 36. Simulation Results for Calculated BO Adjustment

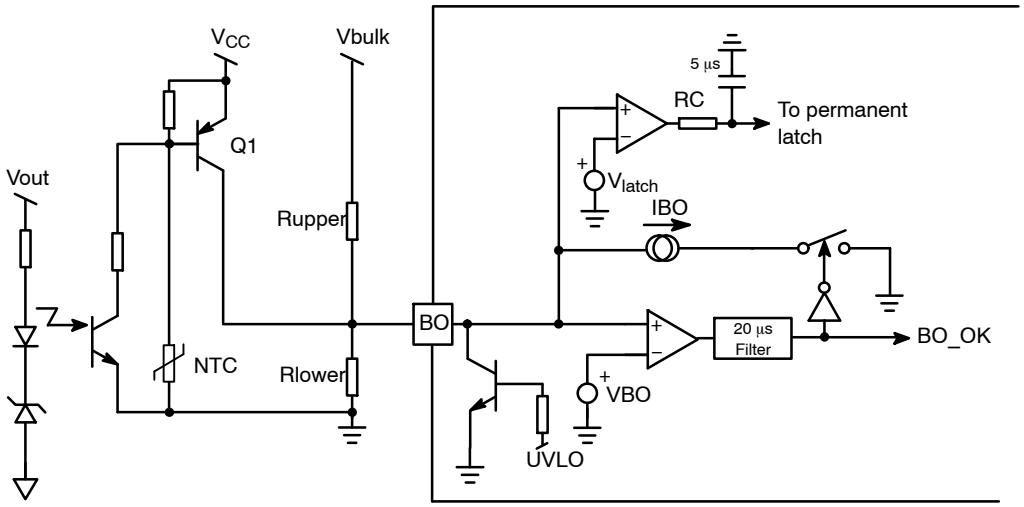


Figure 37. Adding a Comparator on the BO Pin Offers a Way to Latch−off the Controller

Latch−off Protection

There are some situations under which should be the converter fully turned−off and stay latched. This can happen in presence of an over−voltage (the feedback loop is drifting) or when an over temperature is detected. Due to the addition of a comparator on the BO pin, a simple external circuit can lift up this pin above VLATCH (4 V typical) and permanently disable pulses. The VCC pin voltage needs to be cycled down below 6.6 V typically to reset the controller.

On Figure 37, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is pulled down to ground and the BO pin goes up, permanently latching off the controller.

Overload Protection

This resonant controller features a proprietary overload protection system that assures application power stage safety under all possible fault conditions. This system consists of an OLP input for primary current sensing and a Discharge pin to enable a controlled frequency shift via the Rt pin once an overload condition occurs. Internal block diagram of the overload system with a typical application connection can be seen in Figures 39 and 40.

The primary current is sensed indirectly using charge pump (R1, R2, D1, D2, C1 and C2) connected between resonant capacitor and OLP input. When the primary current increases, the voltage on the OLP input grows up as well. It should be noted that other primary current sensing methods (like current sense transformer) can be used instead of charge pump if required by application.

The OCP network (Rshift, Rocp, Cocp), that is present on the Rt pin in addition to the Fmin adjust resistor and Soft Start network, plays important role in overload system implementation. This additional network is used to allow independent OCP and Soft Start parameters adjustment. The OCP network can be omitted in some applications where the Soft Start capacitor with low capacitance is used. The Rshift resistor is then connected directly to the Soft Start capacitor to implement frequency shift during overload.

Overload protection system implemented on OLP input composes of three particular subsystems with following functionality:

1. The fault timer charging current is activated when the OLP input voltage exceeds 1 V threshold. The controller stops operation and enters auto−recovery phase when the overload conditions last for longer time than the adjusted fault timer duration on Ctimer pin (Ct charged to 4 V). The controller then places full restart (including soft start) when auto−recovery period elapses i.e. when Ctimer capacitor discharges back below 1 V.
2. The second overload protection mode is activated additionally to the first one i.e. when the OLP pin voltage exceeds 1 V. The frequency shift is implemented via Rt and Discharge pins in this case by pulling the discharge switch down from Vref_Rt to ground – refer also to Figure 38 for Vdisable evaluation with OLP input voltage. The Discharge pin is connected to the Rocp and Cocp network, that is present on the Rt pin, via resistor Rshift. This configuration allows to adjust OCP frequency shift depth and reaction time and thus ease overload system implementation in any application.
   The Rt pin OCP components are normally designed in such a way that the OCP system shifts and regulates the operating frequency of the LLC converter during overload or secondary side short circuit conditions to maintain primary current at a save level and keep zero voltage switching operation.

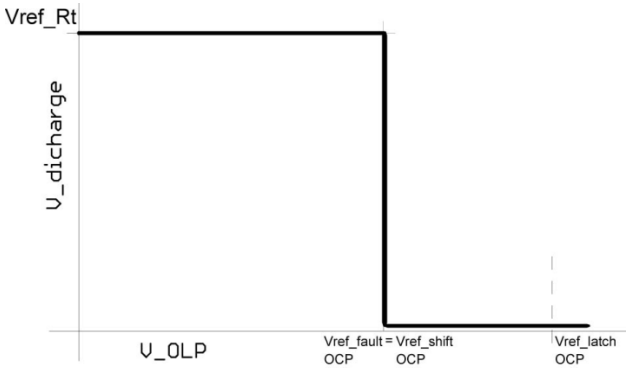


Figure 38. OLP to Discharge Pin Transfer Characteristic

3. The third overload protection is activated in case the OLP pin voltage exceeds 1.5 V threshold. This can happen during secondary side short circuit event or in case the adjusted frequency shift is not sufficient to limit primary current or the OCP network on RT pin fails (like open Soft Start pin event). The IC then stops operation after 1 μs delay to overcome excessive overloading of the power stage components. Both controller version i.e. NCP1398B and also NCP1398C latch fully off and keep the latched state until the V_{CC} drops down below V_{CC} reset level.

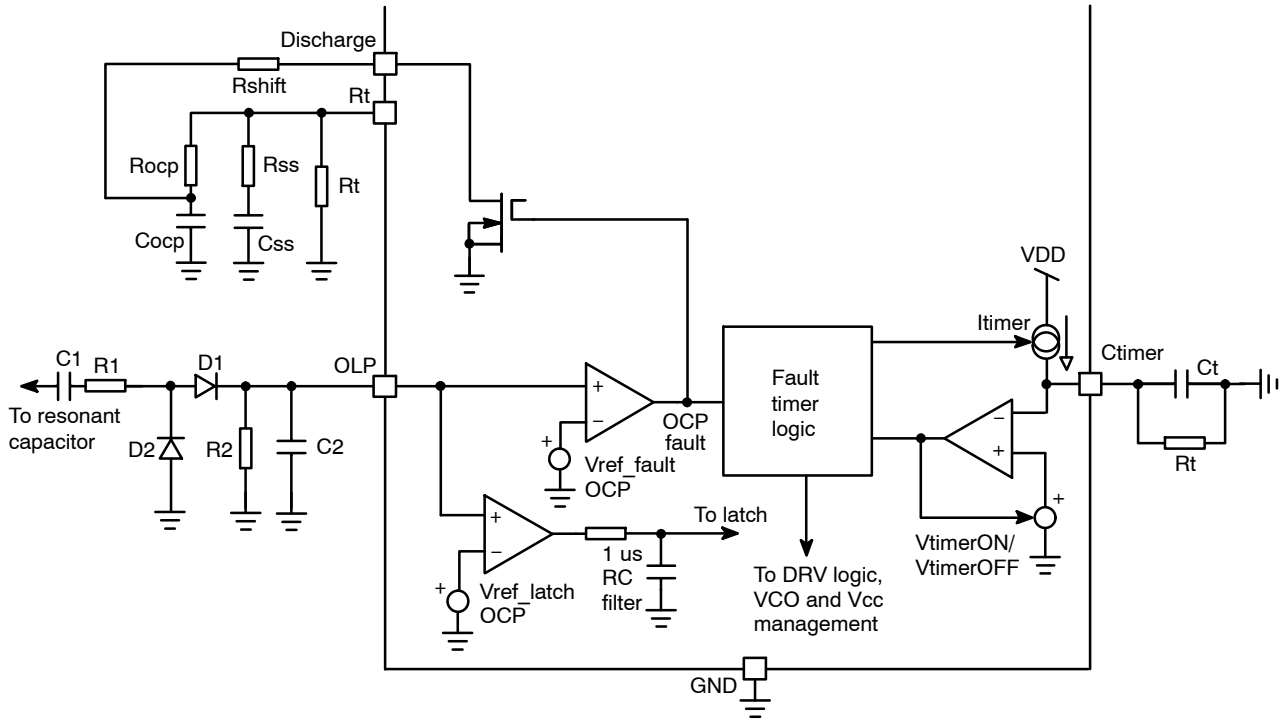


Figure 39. Overload Protection Input Connection NCP1398C − Fault Timer is Not Activated when FB Fault is Present

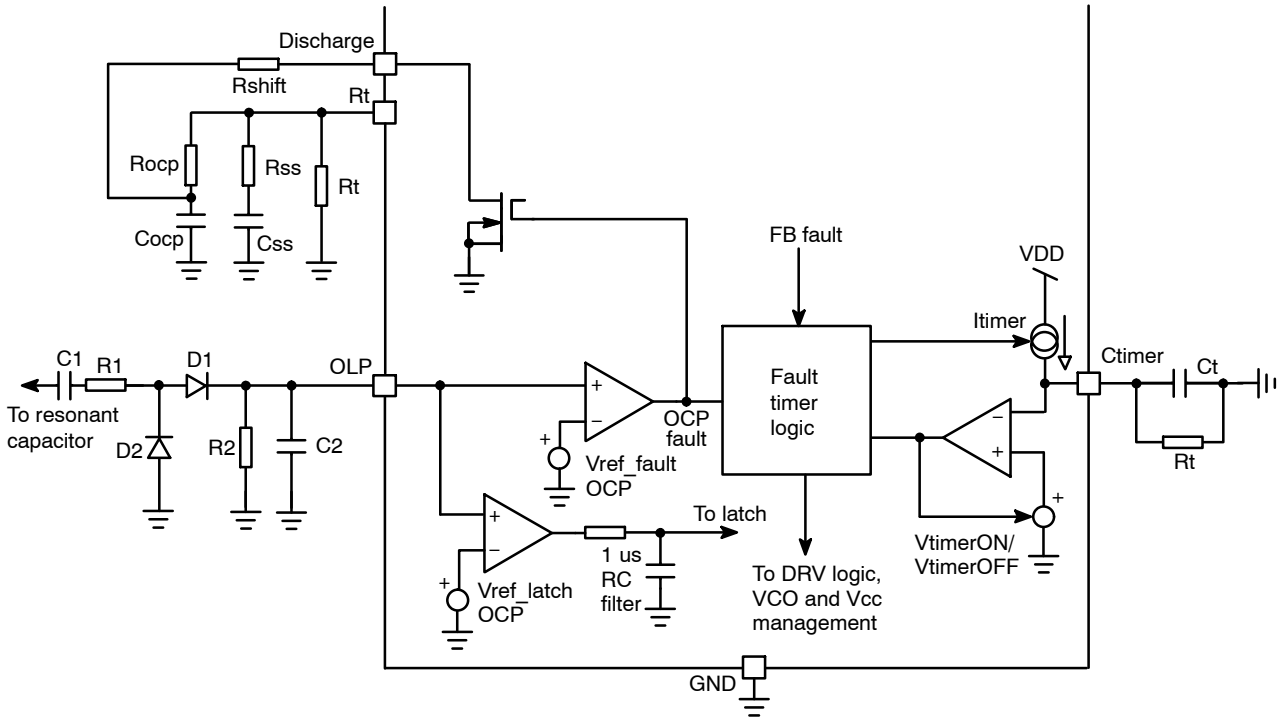


Figure 40. Overload Protection Input Connection NCP1398B

Fault Timer

The NCP1398 implements fault timer with fully adjustable fault and auto−recovery periods – refer to Figure 40 in OLP section. External capacitor Ct is used in combination with internal current source and voltage comparator to implement this function. Once the fault condition occurs the Ctimer pin sources current (Itimer) which charges Ct capacitor. The fault is confirmed and drivers are disabled once the Ctimer pin voltage exceeds Vtimer_off threshold. The Itimer current source is then disabled and Ct capacitor discharges via parallel resistor Rt. Controller places new try for restart (featuring Soft Start) once the Ctimer pin voltage drops below Vtimer_ON threshold. Controller will work in hiccup mode, repeating fault and auto−recovery sequences, if the fault condition remains present in the application (overload conditions or secondary side short circuit). The Fault timer is from the principle of operation a cumulative type of timer i.e. the Ctimer pin voltage integrates if there are multiple faults coming during short time period – refer to Figure 41.

The fault timer can be initiated by several fault sources:

1st – when feedback voltage drops below VFB_fault threshold. This could happen when the FB loop is opened i.e. during secondary regulator or optocoupler fail or open FB pin events. Note that the fault timer is not activated by FB fault detection circuitry for NCP1398C version.

2nd – when the OLP input voltage exceeds Vref_Fault_OCP threshold. This situation happens during overload. The fault timer is activated on both IC versions in this case.

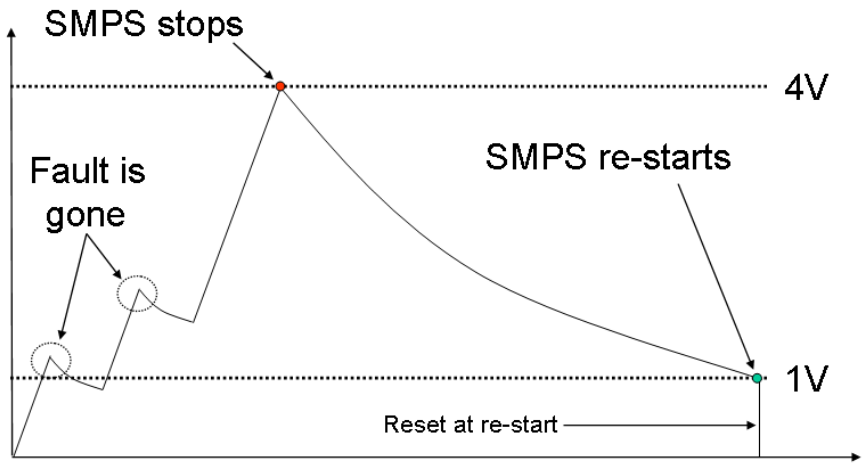


Figure 41. Ctimer Pin Voltage Evaluation When Multiple Faults Occur During Short Time Period

Skip/Disable

The Skip/Disable input (refer to Figure 42) together with Fmax adjust pin offer possibility to implement burst mode operation during light load conditions or just simply disable LLC stage operation using signal coming from other system – like standby. The NCP1398 controller allows for skip−in and also skip−out frequency adjustment. User has thus possibility to control output voltage ripple during skip mode and by this way also affect no−load consumption of the whole power stage.

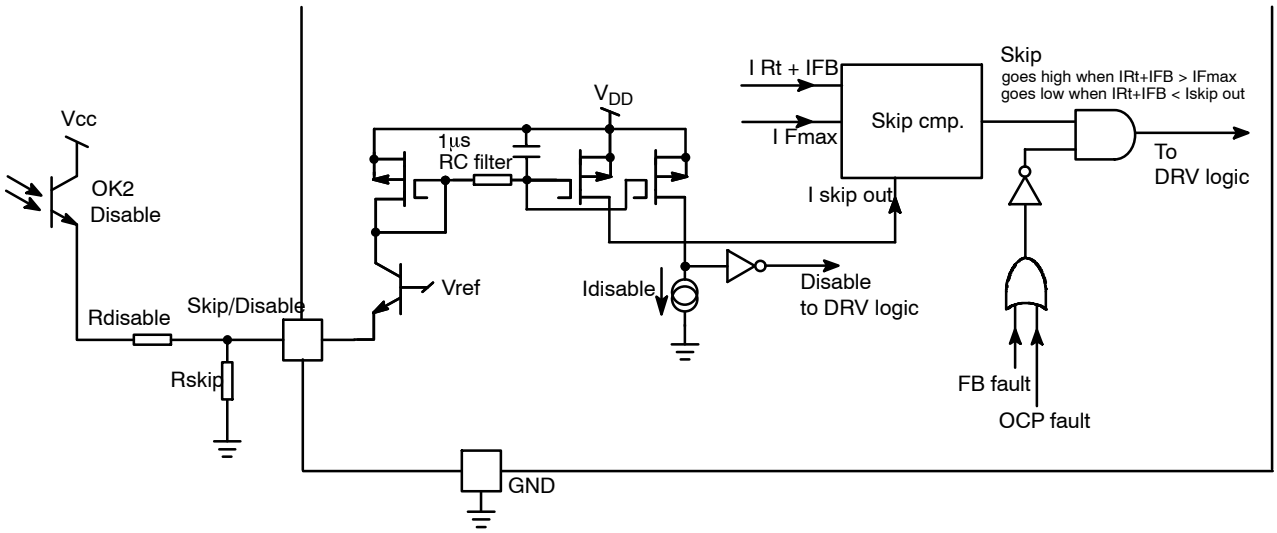


Figure 42. Skip/Disable Input Connection

The skip−in frequency threshold is given by the Fmax pin resistor. The skip−out frequency threshold is then given by the current flowing out from the Skip/Disable pin. The skip−out adjust characteristic is identical with the Fmax adjust characteristic – refer to Figure 26.

Controller turns−off the drivers once the internal current, that is given by sum of IRt and IFb currents, exceeds current adjusted by Fmax pin resistor. The FB pin voltage then naturally drops down thanks to the secondary regulator action. The NCP1398 enable drivers once the internal current IRt+IFb drops below level adjusted on the Skip/Disable pin. User has thus possibility of skip mode hysteresis adjustment and thus application no−load consumption optimization. Note that minimum restart delay of 10 μs is placed by the NCP1398 before restarting from skip mode. Note that skip function is disabled in case the FB or OCP faults are present in the application. Operating frequency of the controller can be thus increased above adjusted maximum on the Fmax pin during soft start period and overload conditions.

In addition to the skip−out threshold adjustment, the Skip/Disable pin will disable the drivers in case its current drops below Idisable threshold (12 μA typically). This feature is implemented to provide user with possibility to use this pin as a disable input. Application can thus be simply disabled by injecting current into the pin from external circuitry (like optocoupler in Figure 42 example).

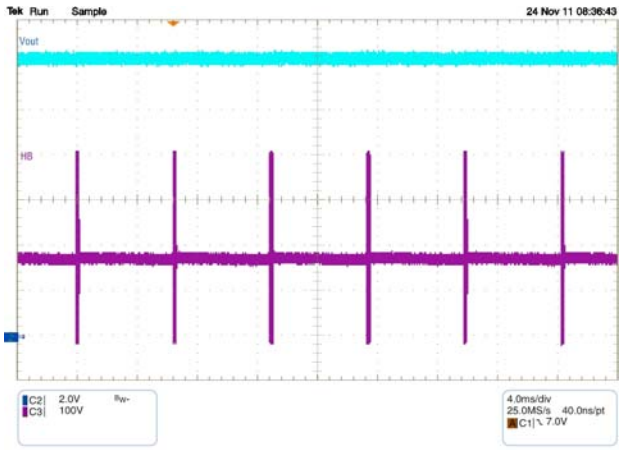


Figure 43. Typical Skip Mode Operation During Light Load Conditions When Using NCP1398 Resonant Controller

There is implemented internal 1 us RC network on the Skip input in order to filter out noise that can be created by power stage and driver currents on the GND bonding and layout parasitic inductances.

The High−Voltage Driver

The driver features a traditional bootstrap circuitry, requiring an external high−voltage diode for the capacitor refueling path. Figure 44 shows the internal architecture of the high−voltage section.

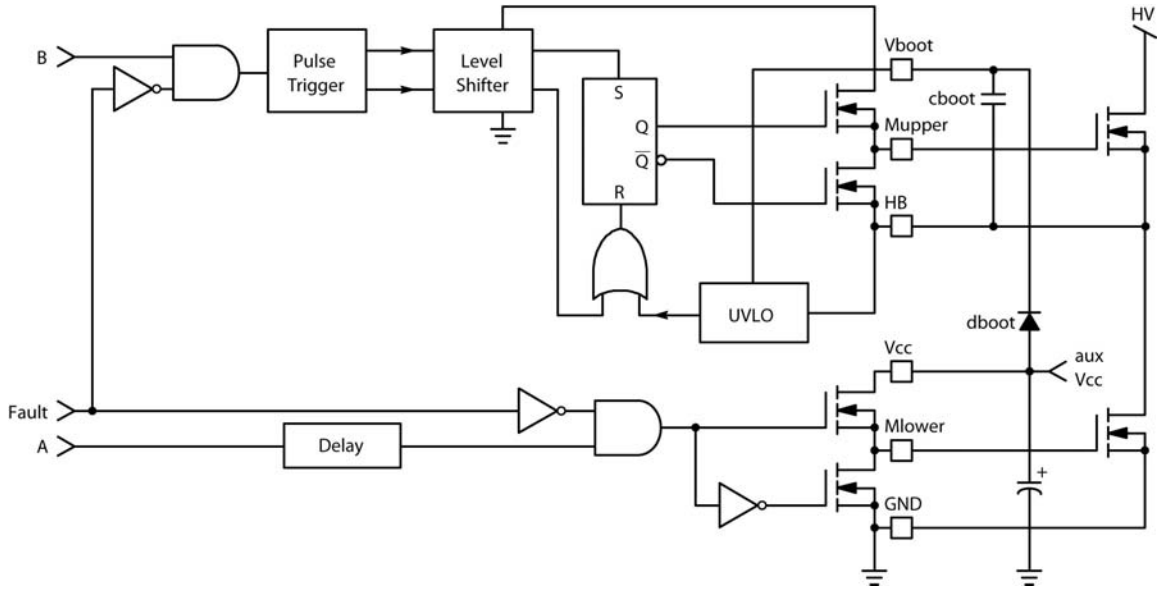


Figure 44. The Internal High−Voltage Section of the NCP1398B/C

The device incorporates an upper UVLO circuitry that makes sure enough Vgs is available for the upper side MOSFET. The A and B outputs are delivered by the internal DRV and fault logic refer to Figures 2 and 3. A delay is inserted in the lower rail to ensure good matching between these propagating signals.

As stated in the maximum ratings section, the floating portion can go up to 600 VDC and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front−end stage.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1398BDR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel
NCP1398CDR2G	SOIC−16, Less Pin 13 (Pb−Free)	2500 / Tape & Reel

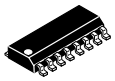
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

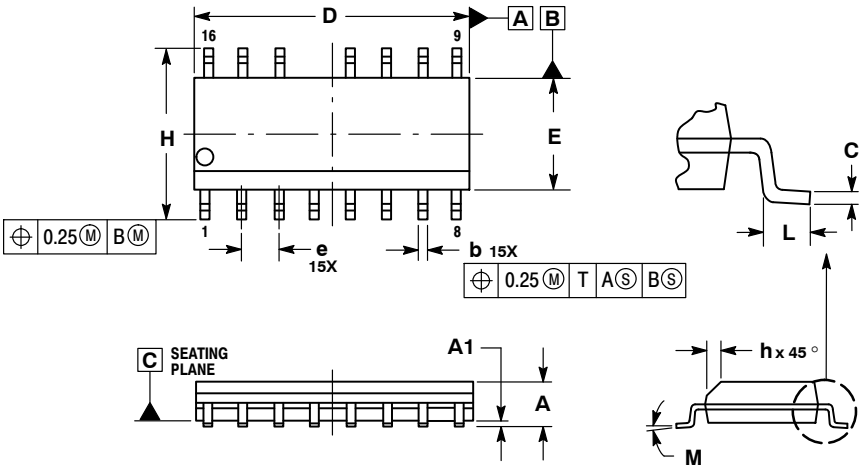
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SOIC−16 NB, LESS PIN 13
CASE 751AM−01
ISSUE O

DATE 20 AUG 2007



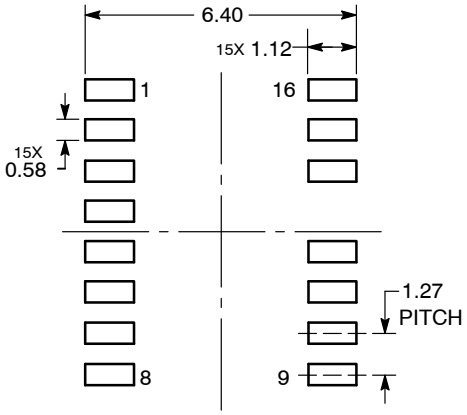
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

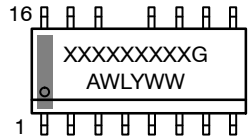
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
M	0 °	7 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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