NCP1840

8-Channel Programmable LED Driver

The NCP1840 is a general purpose LED driver that allows for full programmability of eight separate LED channels through a simple I^2C serial communication interface. The current through each of the channels can be up to 30 mA and is controlled via constant current regulation. Each channel has programmable Pulse−Width Modulation (PWM) control along with programmable current control, allowing for very flexible, optimized LED brightness and color control. Logarithmic output current levels are achieved to best accommodate natural eye viewing.

A QUAD−MODE® charge pump allows for higher forward voltage LEDs and/or multiple LEDs in series per channel to be driven with a low−voltage supply. This makes the NCP1840 capable of efficiently driving LEDs in applications that are running off of low−voltage processor supply levels along with battery−powered applications. Few external components are required making this a very cost−effective solution for multi−channel LED driving.

Features

- Individual Current Level Programmability (5−bit) per Channel
- Individual PWM Programmability (6−bit) per Channel
- I^2C Serial Communication Interface for Programming
- Constant Current Regulated Outputs − 30 mA Maximum per Channel
- Logarithmic Output Current Levels
- External Resistor for Setting Full−Scale Current for all Channels
- Low Noise QUAD−MODE Charge Pump Delivers > 90% Efficiency
- High LED Forward−Voltage Compliant − up to 4.1 V
- Soft−Start POR Reduces Noise
- Registers are Write/Read
- Fault and Thermal Protection
- Small QFN Package
- These are Pb−Free Devices

Typical Applications

- Status or Diagnostic Indicators
  - Portables (Notebook Battery Monitors, Handheld Equipment Testers, etc.)
  - Computing (Servers, Workstations, etc.)
  - Electronic Payment Systems
- Decorative Lighting
  - Toys and Gaming − “Fun Lighting”
  - Electronic Musical Instruments
  - Aftermarket Automotive Trim
  - Keypad Lighting
- Small−Format Display Drivers
  - Tablet PCs and PDAs
  - Smart Phones
- “True Green” LED Applications

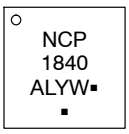
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM



QFN20
4 x 4 mm
CASE 485E



NCP1840 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1840Q8A6MNG	QFN20 (Pb−Free)	490 / Tray
NCP1840Q8A6MNTWG	QFN20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2013

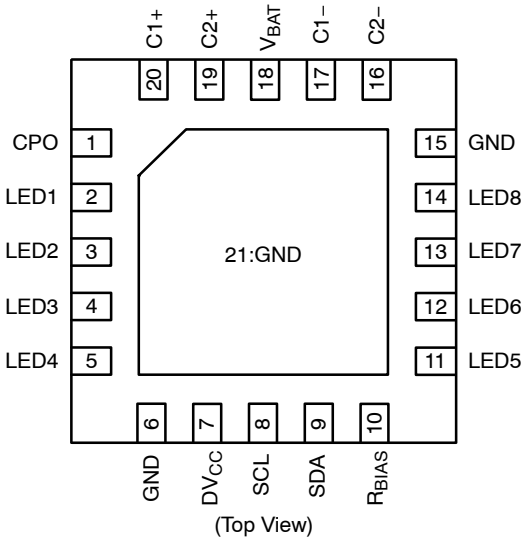


Figure 1. Pin Configuration

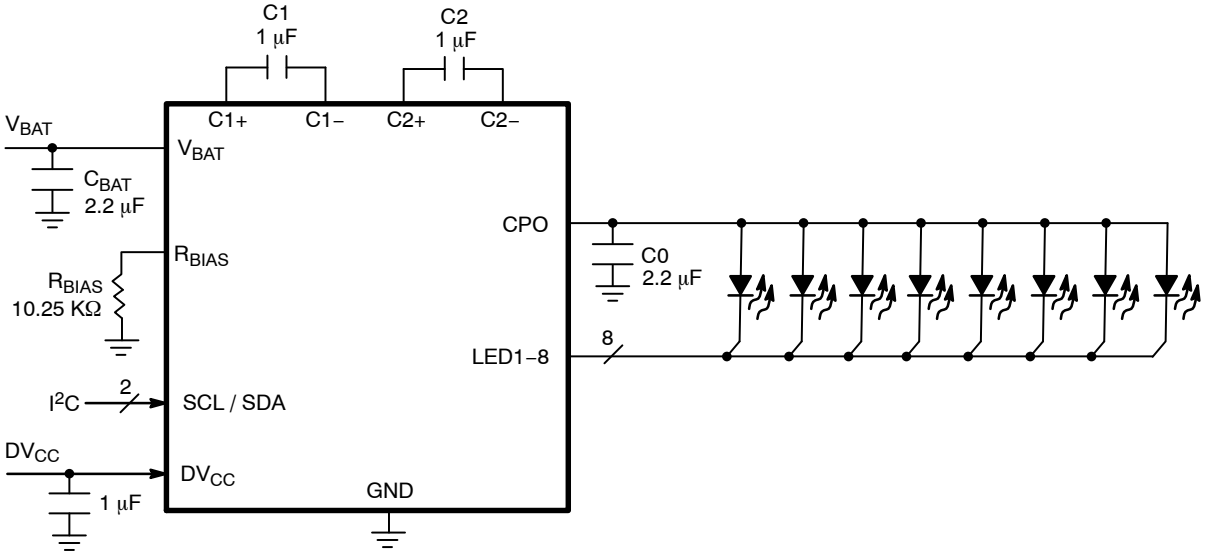


Figure 2. Typical NCP1840 Application

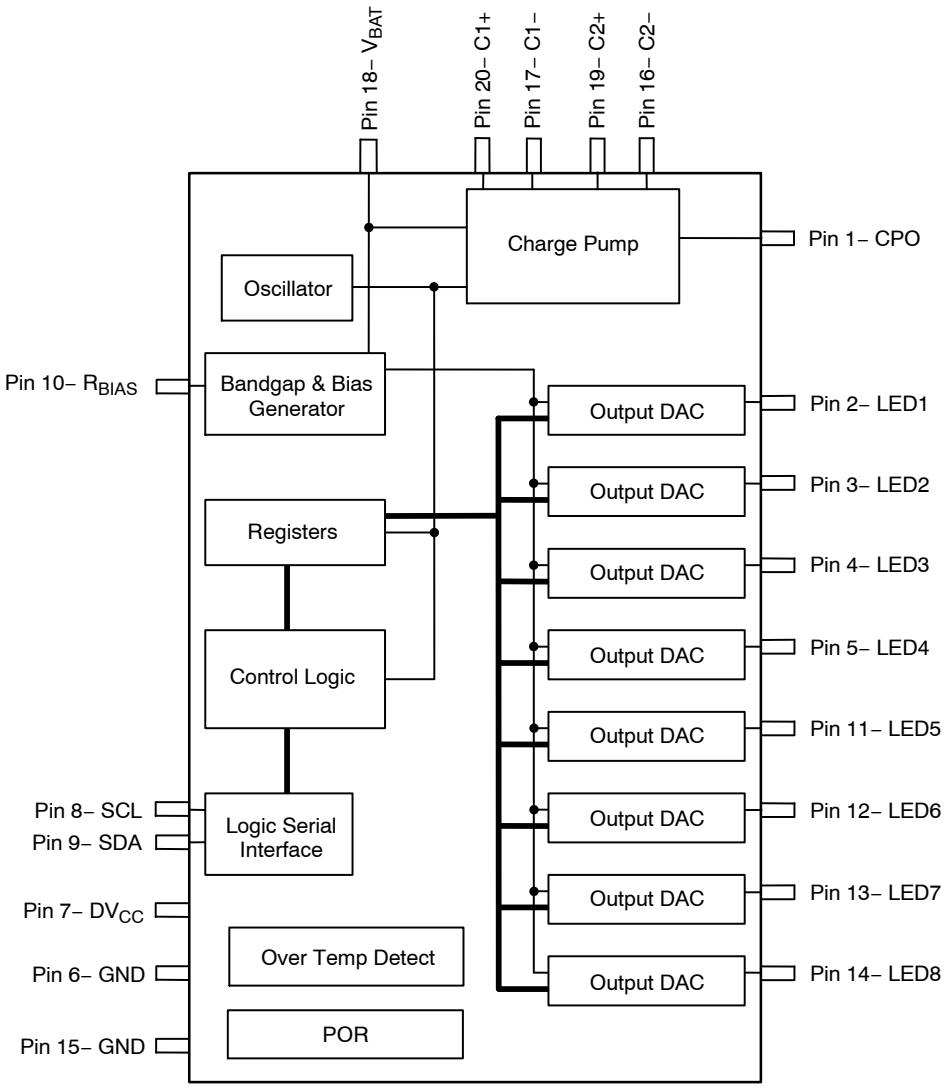


Figure 3. NCP1840 Block Diagram

PIN DESCRIPTION

Pin	Name	Function
1	CPO	Charge pump output used as power supply to the LEDs. Should have a 2.2 μF ceramic capacitor (X5R or X7R) connected to ground.
2–5, 11–14	LED1 – LED8	Current sink outputs for driving LEDs. Output current level and PWM duty cycle can be programmed through the I^2C interface.
6, 15, 21	GND	Ground connection (Pin 21 is the exposed paddle and should be connected to ground)
7	DV_{CC}	Supply input for digital circuitry. Should have a 1 μF ceramic capacitor (X5R or X7R) connected to ground.
8	SCL	I^2C clock input
9	SDA	I^2C serial data input/output
10	R_{BIAS}	An external resistor connected to ground defines the full–scale current for the LED outputs.
16, 17, 19, 20	C2–, C1–, C2+, C1+	Charge pump flying capacitor connections. A 1 μF ceramic capacitor (X5R or X7R) should be connected from C1+ to C1– and C2+ to C2–.
18	V_{BAT}	Supply input for the charge pump and analog circuitry. Should have a 2.2 μF low ESR ceramic capacitor connected to ground.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Battery Supply Voltage Range	V_{BAT}	−0.3 to 6	V
Digital Supply Voltage Range	DV_{CC}	−0.3 to 6	V
Charge Pump Output Voltage Range	V_{CPO}	−0.3 to 6	V
LED Outputs Voltage Range	V_{LED}	−0.3 to 6	V
SCL Voltage Range	V_{SCL}	−0.3 to (DV_{CC} + 0.3)	V
SDA Voltage Range	V_{SDA}	−0.3 to (DV_{CC} + 0.3)	V
Thermal Resistance, Junction−to−Air (Note 1)	$R_{\theta JA}$	66.7	°C/W
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (Note 2)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2.0	kV
ESD Capability, Machine Model (Note 3)	ESD_{MM}	175	V
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	500	V
ESD Capability, Charged Device Model − Corner Pins (Note 3)	ESD_{CDM-C}	750	V
Latch−up Current Immunity (Note 3)	LU	150	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum power dissipation level is the lower of 1) the maximum allowed power dissipation for this particular package, or 2) the power dissipation at which the junction temperature reaches its maximum operating value.
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per EIA/JESD22−A115
   ESD Charged Device Model per ESD−STM5.3.1−1999
   Latch−up Current Maximum Rating: ≤100 mA per JEDEC standard: EIA/JESD78

OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Battery Supply Voltage	V_{BAT}	3	5.5	V
Digital Supply Voltage	DV_{CC}	3	5.5	V
Ground	GND		0	V
LED Forward Voltage (Note 4)	V_f		4.1	V
R_{BIAS} External Resistor	R_{BIAS}	10.25	20.5	kΩ
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

4. At full PWM, max current level.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit
Digital Supply Current (Note 5)	I_{DVCC}		2.3	3.1	mA
Digital Supply Current − Low Power Mode (Note 6)	$I_{DVCC-LOQ}$		0.6	2	μA
Battery Supply Current (Note 5)	I_{VBATT}		520	750	μA
Battery Supply Current − Low Power Mode (Note 6)	$I_{VBATT-LOQ}$		120	500	nA
LED Output Current − Full−Scale (Note 7)	$I_{LED(31)}$	28	30	34.5	mA
LED Output Current − Zero−Scale (Note 7)	$I_{LED(0)}$	0.81	0.85	0.95	mA
LED−to−LED Matching (Note 8)	M_{LED}		4	6.9	%
High Level Input Voltage − SDA & SCL Pins	V_{IH}	0.8 * DV_{CC}			V
Low Level Input Voltage − SDA & SCL Pins	V_{IL}			0.2 * DV_{CC}	V
Low Level Input Current − SDA & SCL Pins	I_{IL}	−1.0		1.0	μA
High Level Input Current − SDA & SCL Pins	I_{IH}	−1.0		1.0	μA
High Level Output Voltage − SDA Pin	V_{OH}	2.4			V
Low Level Output Voltage − SDA Pin	V_{OL}			0.4	V
Low Level Output Current − SDA Pin	I_{OL}	4.0			mA
High Level Output Current − SDA Pin	I_{OH}			−4.0	mA

5. All LED outputs off, Charge Pump in 1X Mode, no I^2C Communication.
6. Part enters Low Power Mode around 5 ms after all LED outputs are OFF and there is no I^2C communication. Communication to the part resumes normal operation in less than 1 ms.
7. With external R_{BIAS} = 10.25 kΩ on R_{BIAS} pin.
8. For T = −40°C, maximum LED−to−LED matching 7.5%. LED−to−LED Matching is calculated by comparing the output with highest current against the output with lowest current, divided by the output with lowest current, all at the same programmed value. $(I_{max} - I_{min}) / I_{min}$.

I²C TIMING CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{SCL}		400	kHz
SCL Low Time	t_{LOW}	1.3		μs
SCL High Time	t_{HIGH}	0.6		μs
Start Hold Time	$t_{HD;STA}$	0.6		μs
Data Hold Time	$t_{HD;DAT}$		0.9	μs
Start Setup Time	$t_{SU;STA}$	0.6		μs
Data Setup Time	$t_{SU;DAT}$	100		μs
Stop Setup Time	$t_{SU;STO}$	0.6		μs
Bus Free Time (Stop and Start Conditions)	t_{BUF}	1.3		μs
Rise Time (SCL and SDA)	t_R	10	300	ns
Fall Time (SCL and SDA)	t_F	10	300	ns

TYPICAL PERFORMANCE CHARACTERISTICS (V_{BAT} = 4.0 V, DV_{CC} = 3.3 V, I_{OUT} = 160 mA (8 LEDs at 20 mA/ch), C_{IN} = C_{OUT} = 2.2 μF, C_1 = C_2 = 1 μF, T_{AMB} = 25°C unless otherwise specified.)

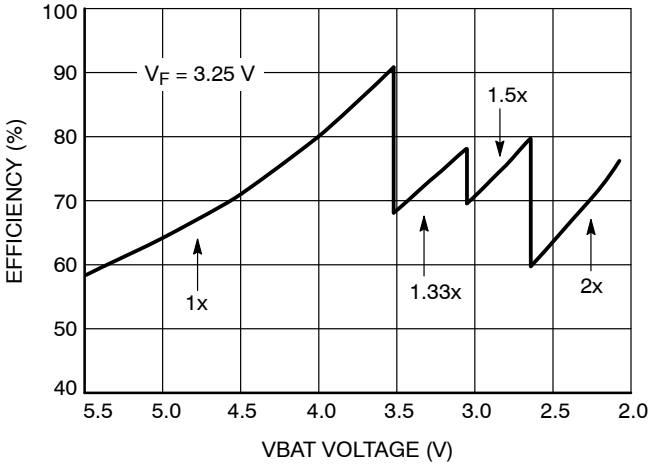


Figure 4. Efficiency vs. V_{BAT} Voltage

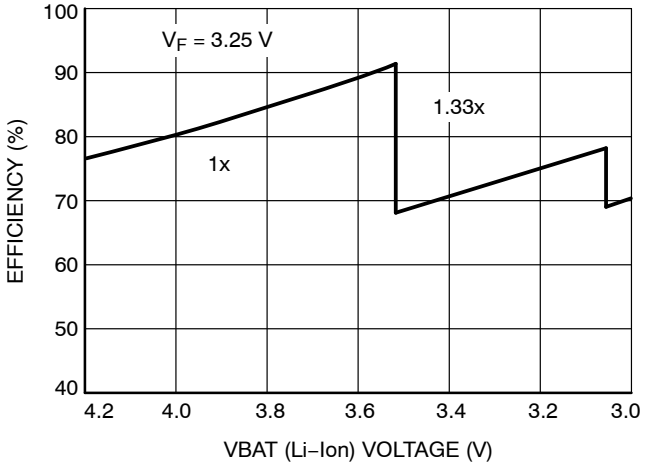


Figure 5. Efficiency vs. Li−Ion Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (V_{BAT} = 4.0 V, DV_{CC} = 3.3 V, I_{OUT} = 160 mA (8 LEDs at 20 mA/ch), C_{IN} = C_{OUT} = 2.2 μF, C_1 = C_2 = 1 μF, T_{AMB} = 25°C unless otherwise specified.)

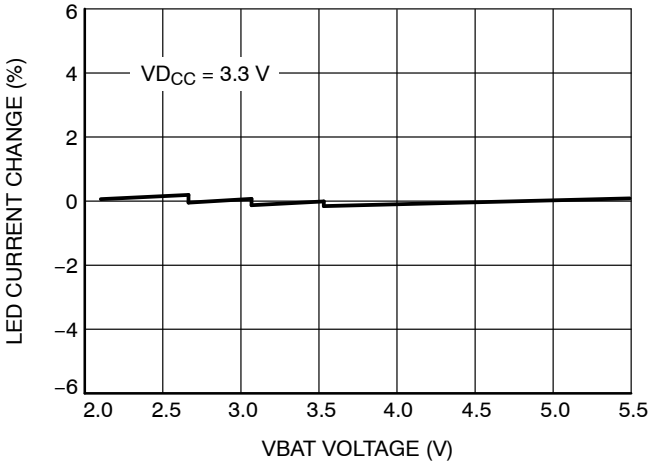


Figure 6. LED Current Change vs. V_{BAT} Voltage

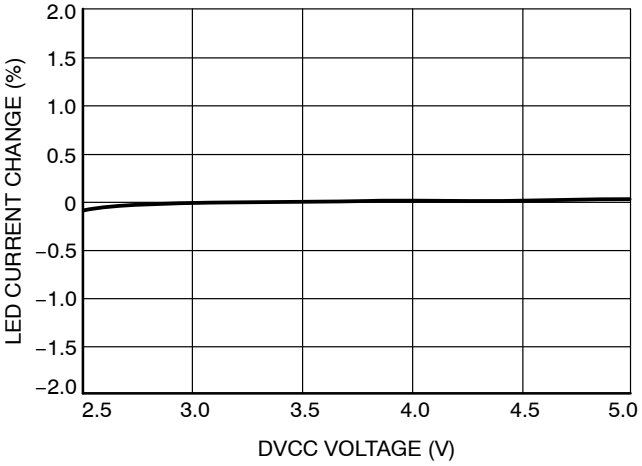


Figure 7. LED Current Change vs. DV_{CC} Voltage

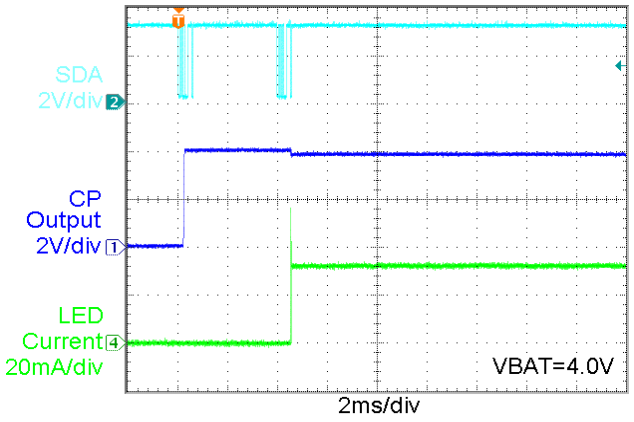


Figure 8. Power Up in 1x Mode, ILED = 30 mA/ch

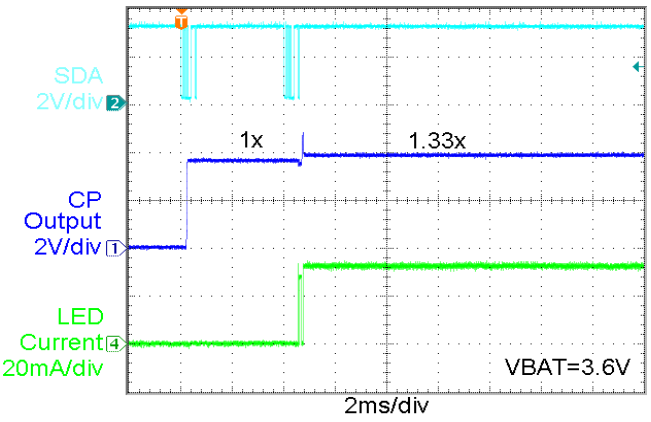


Figure 9. Power Up in 1.33x Mode, ILED = 30 mA/ch

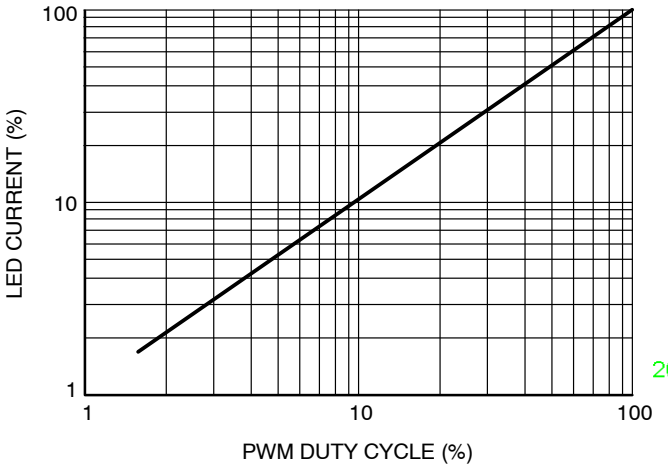


Figure 10. LED Current vs. PWM Duty Cycle

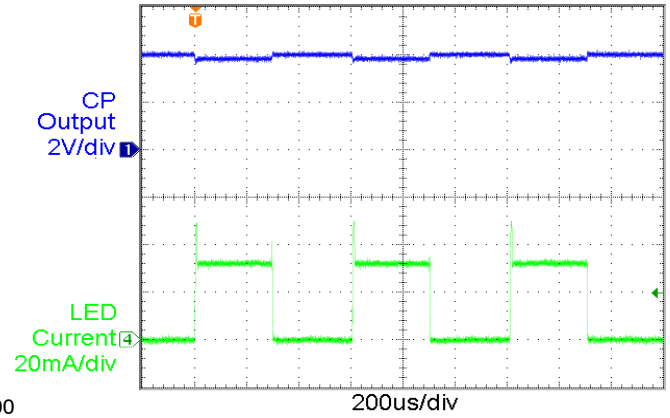


Figure 11. PWM Waveform, 50% Duty Cycle, ILED = 30 mA/ch

OPERATION DESCRIPTION

Constant Current Control

The NCP1840 has 8 LED channels that are individually regulated constant current sources. The maximum current per channel is 30 mA but can be reduced by adjusting the resistor R_{BIAS}, which is placed between the R_{BIAS} pin and ground. R_{BIAS} is required and can vary between 10.25 kΩ and 20.5 kΩ. The maximum current per channel can be calculated with the following equation:

$$I_{max} = 250 * \frac{1.23\ V}{R_{BIAS}}$$

Additionally, the NCP1840 allows for the current through each of the 8 channels to be fully programmable via a 5−bit DAC on each output, allowing for the desired luminance to be achieved for each channel. Programming the current level is achieved by loading data into channel−specific registers through the I²C serial interface. The output current levels are logarithmic, providing a perceived linear LED brightness to the human eye, as shown in Figure 12. This allows for a more gradual and natural viewing change in LED brightness between levels.

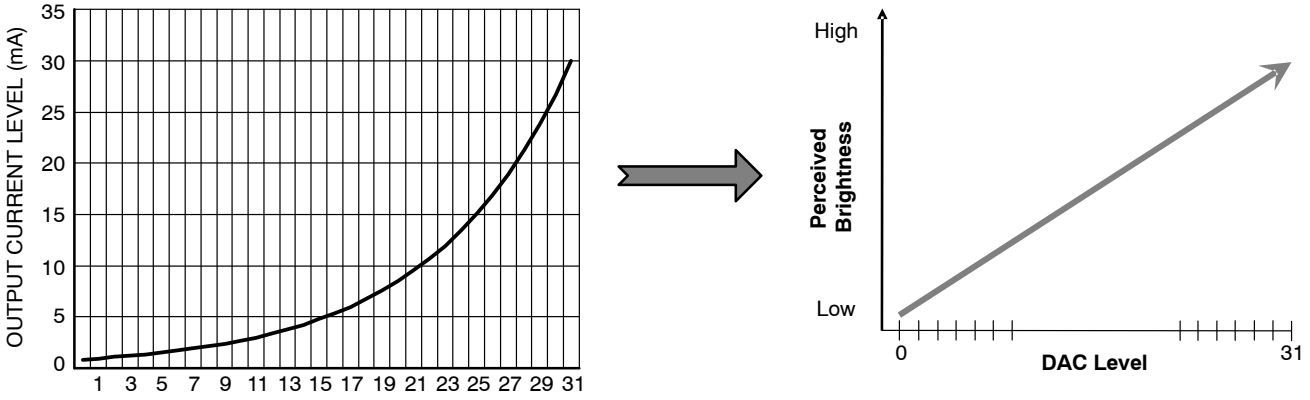


Figure 12. Logarithmic Output Current (R_{BIAS} = 10.25 KΩ)

PWM Control

The NCP1840 provides 6−bit PWM duty cycle control for each of its 8 channels, allowing each channel to be dimmed independent of the other channels and without sacrificing the LED color output. Programming PWM duty cycle is achieved by loading data into channel−specific registers through the I²C serial interface. The typical on time of the LED can be calculated by multiplying the duty cycle percentage by the typical PWM period of 575 μs.

Charge Pump

The NCP1840 incorporates a high efficiency, low noise, QUAD−MODE (1x, 1.33x, 1.5x, and 2x) charge pump. This allows for higher forward voltage LEDs and/or multiple LEDs in series per channel to be driven with a low−voltage supply. In order to optimize efficiency while maintaining constant current regulation, the NCP1840 automatically senses when it should change charge pump modes based on the voltage across the LED current sources. By utilizing the 1.33x mode, approximately 10% more efficiency than a typical 1.5x mode is achieved.

The NCP1840 powers up in 1x mode where the charge pump output voltage will be approximately equal to the input supply voltage. If the output voltage is sufficient to regulate all LED currents, the device remains in this mode. However, if the input voltage is insufficient to regulate the current in all active channels, the device automatically switches into 1.33x mode. In this mode, the output voltage is approximately equal to 1.33 times the input supply voltage. If the input voltage is insufficient again to maintain current regulation in all active channels, the device will automatically switch to the 1.5x mode. In this mode, the output voltage will be approximately equal to 1.5 times the input supply voltage. If the input voltage is still insufficient to maintain the constant current regulation in all active channels, the device will automatically switch to the 2x mode where the output voltage is approximately equal to two times the input supply voltage. In all modes, if the device detects a sufficient input voltage to drive all LED currents in 1x mode, it will automatically change back to 1x mode to optimize efficiency.

I²C Serial Interface

The registers of the NCP1840 are programmed and read through an I²C serial interface. Due to the NCP1840 only being configured as a Slave device, a Master device is required on the communication bus. The NCP1840 has a factory programmed 7−bit Slave address of 0011011 (1B hex). The last bit of the Slave address specifies whether a Read (1) or Write (0) operation is to be performed. The maximum clock frequency for the serial interface is 400 kHz and both the SCL and SDA lines require external pull−up resistors.

Register Writes & Reads

The ability of the NCP1840 to allow the internal registers to be both written and read provides the user with the benefit of being able to easily verify correct register writes and isolate system problem areas while troubleshooting. This ability also allows users to configure the register values according to desired LED performance, read these register values from the part, and then store these settings in external memory for future use. In addition, an over−temperature fault condition can also be read from a specific register, allowing for diagnostic feedback to the system controller.

Write Protocol

The Write protocol that is used by the NCP1840 is depicted in Figure 13. As can be seen, the Master initiates the communication by issuing a START condition and then by broadcasting the 7−bit part address of the NCP1840 followed by a Write operation request (0). The NCP1840 acknowledges the request and then the Master transmits the address byte which consists of 3−bits of control data followed by the 5−bit address of the register to be written to. Upon successful receipt of the address byte, the NCP1840 acknowledges to the Master which then transmits the data byte to be written. The NCP1840 then acknowledges the received register data and the Master issues a STOP condition to terminate the communication.

Read Protocol

The Read protocol that is used by the NCP1840 is depicted in Figure 14. As can be seen, the Master initiates the communication by issuing a START condition and then by broadcasting the 7−bit part address of the NCP1840 followed by a Write operation request (0). This is because the control bits need to first be set to 001 before a read operation takes place. The NCP1840 acknowledges the request and the Master then transmits the address byte which consists of 001, for the 3 control bits, followed by the 5−bit address of the register to be read from. Upon successful receipt of the address byte, the NCP1840 acknowledges to the Master which will then issue another START condition followed by the 7−bit part address of the NCP1840 and a Read operation request (1). The NCP1840 acknowledges the request and then transmits the data byte to be read by the Master. The NCP1840 then releases the SDA line and the Master terminates the Read session by not acknowledging the data byte and by issuing a STOP condition.

WRITE PROTOCOL USED BY NCP1840:

1	7	1	1	3	5	1	8	1	1
S	Part Address	W	A	Control Bits	Register Address	A	Register Data	A	P

S = Start Condition, W = Write, A = Acknowledge, P = Stop Condition

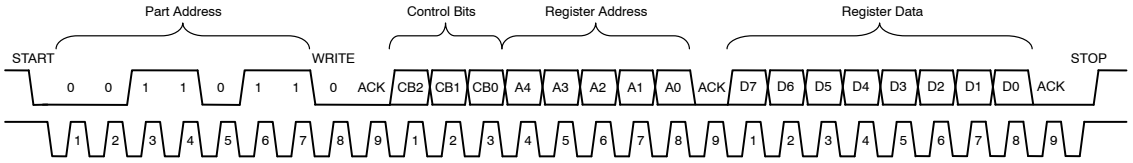


Figure 13. NCP1840 Write Protocol

READ PROTOCOL USED BY NCP1840:

1	7	1	1	3	5	1	8	7	1	1	8	1	1
S	Part Address	W	A	Control Bits	Register Address	A	S	Part Address	R	A	Register Data Out	$\overline{A}$	P

S = Start Condition, W = Write, R = Read, A = Acknowledge, $\overline{A}$ =No Acknowledge, P = Stop Condition

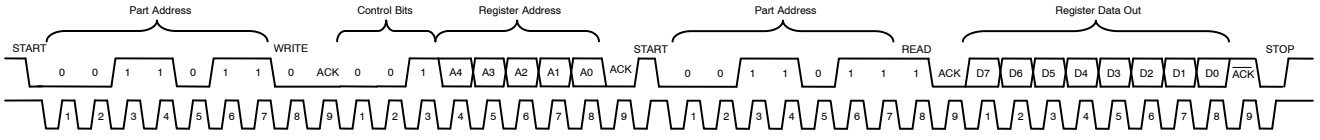


Figure 14. NCP1840 Read Protocol

Control Bits

The NCP1840 has 3 control bits that are used to dictate the function that will be performed by the part. The following table contains a description of each of these functions along with their dependencies on the register address, A[4:0], and the data byte, D[7:0].

CONTROL BITS DESCRIPTION

CB2	CB1	CB0	Function
0	0	0	Turn all LED Channels ON/OFF All channels are turned ON/OFF according to the data in the Output Control Register. The current and PWM duty cycle will depend on each channel's Current Level and PWM Register. The register address field, A[4:0], is ignored along with the data byte, D[7:0]. The Master can issue a STOP condition without sending a data byte.
0	0	1	Program a Single Register (also Read Operation Setting) The register address, A[4:0], defines the register to be written or read. For a write, the data byte, D[7:0], defines the data to be written. The data will be loaded in the register but will not take effect until either a 000 or 010 Control Bit setting is applied. This is also the Control Bit setting required for a Read operation (see Read Protocol).
0	1	0	Program a Single Register and Turn all LED Channels ON/OFF The register address, A[4:0], defines the register to be written to and the data byte, D[7:0], defines the data to be written. After the receipt of the data byte, all channels will be turned ON/OFF according to the data in the Output Control Register. The current and PWM duty cycle will depend on each channel's Current Level and PWM Register.
0	1	1	Program all 8 Current Level Registers All Current Level Registers will be loaded with the data defined by the data byte, D[7:0]. The register address, A[4:0], is ignored. The data will be loaded in the registers but will not take effect until either a 000 or 010 Control Bit setting is applied.
1	0	0	Program all 8 PWM Registers All PWM Registers will be loaded with the data defined by the data byte, D[7:0]. The register address, A[4:0], is ignored. The data will be loaded in the registers but will not take effect until either a 000 or 010 Control Bit setting is applied.
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Register Address Map

The NCP1840 has a total of 18 different register addresses, as shown in the table below, made up of the following: 8 addresses for the individual channel Current Level Registers, 8 addresses for the individual channel PWM Registers, 1 address for the Output Control Register, and 1 address for the Main Status Register. The 8 Current Level Registers are used to program the output current for each of the 8 channels. The 8 PWM Registers are used to program the PWM duty cycle for each of the 8 channels. The Output Control Register is used to set the status, either ON or OFF, of all 8 channels. The Main Status Register is used to indicate the operating condition of the part: normal operation, low power mode, or over temperature.

REGISTER ADDRESS MAP

Address – Binary						
A4	A3	A2	A1	A0	Address – Hex	Function
0	0	0	0	0	0	LED1 Current Level Register
0	0	0	0	1	1	LED2 Current Level Register
0	0	0	1	0	2	LED3 Current Level Register
0	0	0	1	1	3	LED4 Current Level Register
0	0	1	0	0	4	LED5 Current Level Register
0	0	1	0	1	5	LED6 Current Level Register
0	0	1	1	0	6	LED7 Current Level Register
0	0	1	1	1	7	LED8 Current Level Register
0	1	0	0	0	8	LED1 PWM Register
0	1	0	0	1	9	LED2 PWM Register

REGISTER ADDRESS MAP

Address – Binary						
A4	A3	A2	A1	A0	Address – Hex	Function
0	1	0	1	0	A	LED3 PWM Register
0	1	0	1	1	B	LED4 PWM Register
0	1	1	0	0	C	LED5 PWM Register
0	1	1	0	1	D	LED6 PWM Register
0	1	1	1	0	E	LED7 PWM Register
0	1	1	1	1	F	LED8 PWM Register
1	0	0	0	0	10	Output Control Register
1	0	0	0	1	11	Main Status Register

Current Level Registers

The current through each of the 8 channels on the NCP1840 can be individually programmed by loading the appropriate data into the Current Level Register for each channel. There are 32 different current levels per channel that are implemented as a logarithmically scaled percentage of the maximum current, dictated by an external resistor R_{BIAS}. A description of the 32 different current levels can be found in the following table.

CURRENT LEVEL REGISTER DESCRIPTION

Data – Binary									
D7	D6	D5	D4	D3	D2	D1	D0	Data – Hex	Percentage of Maximum Current
0	0	0	0	0	0	0	0	00	2.8333%
0	0	0	0	0	0	0	1	01	3.1667%
0	0	0	0	0	0	1	0	02	3.5333%
0	0	0	0	0	0	1	1	03	3.9667%
0	0	0	0	0	1	0	0	04	4.4667%
0	0	0	0	0	1	0	1	05	5.0000%
0	0	0	0	0	1	1	0	06	5.6333%
0	0	0	0	0	1	1	1	07	6.3000%
0	0	0	0	1	0	0	0	08	7.0667%
0	0	0	0	1	0	0	1	09	7.9333%
0	0	0	0	1	0	1	0	0A	8.9000%
0	0	0	0	1	0	1	1	0B	10.0000%
0	0	0	0	1	1	0	0	0C	11.2333%
0	0	0	0	1	1	0	1	0D	12.6000%
0	0	0	0	1	1	1	0	0E	14.1333%
0	0	0	0	1	1	1	1	0F	15.8667%
0	0	0	1	0	0	0	0	10	17.8000%
0	0	0	1	0	0	0	1	11	19.9667%
0	0	0	1	0	0	1	0	12	22.4000%
0	0	0	1	0	0	1	1	13	25.1333%
0	0	0	1	0	1	0	0	14	28.2000%
0	0	0	1	0	1	0	1	15	31.6333%
0	0	0	1	0	1	1	0	16	35.4667%
0	0	0	1	0	1	1	1	17	39.8000%

CURRENT LEVEL REGISTER DESCRIPTION

Data – Binary									
D7	D6	D5	D4	D3	D2	D1	D0	Data – Hex	Percentage of Maximum Current
0	0	0	1	1	0	0	0	18	44.6667%
0	0	0	1	1	0	0	1	19	50.2333%
0	0	0	1	1	0	1	0	1A	56.2333%
0	0	0	1	1	0	1	1	1B	63.1000%
0	0	0	1	1	1	0	0	1C	70.8000%
0	0	0	1	1	1	0	1	1D	79.4333%
0	0	0	1	1	1	1	0	1E	89.1333%
0	0	0	1	1	1	1	1	1F	100.0000%

PWM Registers

The PWM duty cycle of each of the 8 channels on the NCP1840 can be individually programmed by loading the appropriate data into the PWM Register for each channel. There are 64 different duty cycle settings per channel that are implemented in a linear fashion from 0%, fully OFF, to 100%, fully ON. A description of the 64 different PWM duty cycle settings can be found in the following table. Note that the typical on time of the LED can be calculated by multiplying the duty cycle percentage by the typical PWM period of 575 μs.

PWM REGISTER DESCRIPTION

Data – Binary									
D7	D6	D5	D4	D3	D2	D1	D0	Data – Hex	PWM Duty Cycle
0	0	0	0	0	0	0	0	00	0.000%
0	0	0	0	0	0	0	1	01	1.587%
0	0	0	0	0	0	1	0	02	3.175%
0	0	0	0	0	0	1	1	03	4.762%
0	0	0	0	0	1	0	0	04	6.349%
0	0	0	0	0	1	0	1	05	7.937%
0	0	0	0	0	1	1	0	06	9.524%
0	0	0	0	0	1	1	1	07	11.111%
0	0	0	0	1	0	0	0	08	12.698%
0	0	0	0	1	0	0	1	09	14.286%
0	0	0	0	1	0	1	0	0A	15.873%
0	0	0	0	1	0	1	1	0B	17.460%
0	0	0	0	1	1	0	0	0C	19.048%
0	0	0	0	1	1	0	1	0D	20.635%
0	0	0	0	1	1	1	0	0E	22.222%
0	0	0	0	1	1	1	1	0F	23.810%
0	0	0	1	0	0	0	0	10	25.397%
0	0	0	1	0	0	0	1	11	26.984%
0	0	0	1	0	0	1	0	12	28.571%
0	0	0	1	0	0	1	1	13	30.159%
0	0	0	1	0	1	0	0	14	31.746%
0	0	0	1	0	1	0	1	15	33.333%
0	0	0	1	0	1	1	0	16	34.921%

PWM REGISTER DESCRIPTION

Data – Binary									
D7	D6	D5	D4	D3	D2	D1	D0	Data – Hex	PWM Duty Cycle
0	0	0	1	0	1	1	1	17	36.508%
0	0	0	1	1	0	0	0	18	38.095%
0	0	0	1	1	0	0	1	19	39.683%
0	0	0	1	1	0	1	0	1A	41.270%
0	0	0	1	1	0	1	1	1B	42.857%
0	0	0	1	1	1	0	0	1C	44.444%
0	0	0	1	1	1	0	1	1D	46.032%
0	0	0	1	1	1	1	0	1E	47.619%
0	0	0	1	1	1	1	1	1F	49.206%
0	0	1	0	0	0	0	0	20	50.794%
0	0	1	0	0	0	0	1	21	52.381%
0	0	1	0	0	0	1	0	22	53.968%
0	0	1	0	0	0	1	1	23	55.556%
0	0	1	0	0	1	0	0	24	57.143%
0	0	1	0	0	1	0	1	25	58.730%
0	0	1	0	0	1	1	0	26	60.317%
0	0	1	0	0	1	1	1	27	61.905%
0	0	1	0	1	0	0	0	28	63.492%
0	0	1	0	1	0	0	1	29	65.079%
0	0	1	0	1	0	1	0	2A	66.667%
0	0	1	0	1	0	1	1	2B	68.254%
0	0	1	0	1	1	0	0	2C	69.841%
0	0	1	0	1	1	0	1	2D	71.729%
0	0	1	0	1	1	1	0	2E	73.016%
0	0	1	0	1	1	1	1	2F	74.603%
0	0	1	1	0	0	0	0	30	76.190%
0	0	1	1	0	0	0	1	31	77.778%
0	0	1	1	0	0	1	0	32	79.365%
0	0	1	1	0	0	1	1	33	80.952%
0	0	1	1	0	1	0	0	34	82.540%
0	0	1	1	0	1	0	1	35	84.127%
0	0	1	1	0	1	1	0	36	85.714%
0	0	1	1	0	1	1	1	37	87.302%
0	0	1	1	1	0	0	0	38	88.889%
0	0	1	1	1	0	0	1	39	90.476%
0	0	1	1	1	0	1	0	3A	92.063%
0	0	1	1	1	0	1	1	3B	93.651%
0	0	1	1	1	1	0	0	3C	95.238%
0	0	1	1	1	1	0	1	3D	96.825%
0	0	1	1	1	1	1	0	3E	98.413%
0	0	1	1	1	1	1	1	3F	100.000%

Output Control Register

The Output Control Register on the NCP1840 is used to set the status, either ON or OFF, of all 8 channels. As shown in the following table, each bit in the register corresponds to one of the 8 LED channels. Each channel will be turned ON with a 1 loaded into the corresponding bit and will be turned OFF with a 0 loaded into that bit. When an LED channel is turned ON, the current level and PWM duty cycle of that channel will be dictated by the data that is loaded into its Current Level Register and PWM Register. It is important to note that any unused LED channel should not be turned ON.

OUTPUT CONTROL REGISTER DESCRIPTION

Register Bit (1 = ON, 0 = OFF)	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding LED Channel	LED8	LED7	LED6	LED5	LED4	LED3	LED2	LED1

Main Status Register

The Main Status Register of the NCP1840 is used to indicate the operating condition of the part and is read−only. As shown in the following table, bit D0 indicates either normal operation (0) or an over temperature condition (1). When the on−chip temperature sensor detects an over−temperature condition, it will turn off all LED outputs, along with the charge pump, and set bit D0 to a logic one. If the over−temperature condition goes away, bit D0 will automatically reset to a logic zero and the part will resume normal operation. Therefore, bit D0 of this register can be read and used to help determine if an over−temperature condition currently exists on the part. Likewise, bit D2 indicates either normal operation (0) or low power mode operation (1). When all LED outputs are turned OFF and there is no I^2C communication for 5 ms, the part will put itself in a low power mode and set bit D2 to a logic one. When the Master wakes the device up with I^2C communication, bit D2 will be set to a logic zero once the entire chip is ready to run in normal operation. Therefore, when the Master wakes up the device, it can read bit D2 and wait for this bit to change to 0, indicating the return to normal operation.

MAIN STATUS REGISTER DESCRIPTION

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0 = Normal Operation	0	0 = Normal Operation
					1 = Low Power Mode		1 = Over Temperature

Fault Management

The NCP1840 has several fault management features intended to provide increased performance and reliability to both the system and the part itself:

- Each LED output will detect if it is shorted to the charge pump output and if so will turn that particular channel's circuitry OFF. This saves power consumption that would otherwise be lost and provides the user with the ability to ensure that unused channels are turned OFF by tying them to the charge pump output.
- The charge pump output will detect any over−current events and automatically limit the current to less than 800 mA. This helps to prevent any damage to the chip and the system due to elevated current on this output.
- The charge pump output will detect a short−circuit event (less than 0.7 V) and limit the current to the soft−start limit of less than 94 mA. This helps to prevent damage to the chip and the system that could potentially be seen with the output being short−circuited to ground.
- The charge pump will reset itself to 1x mode if it reaches an overvoltage level (5.5 V to 6 V). This helps to prevent damage to the chip and the system in the event that the supply voltage increases while the charge pump is operating in the 1.33x, 1.5x, or 2x mode.
- If the external resistor, R_{BIAS}, used to set the maximum output current and the internal reference current, is too small or otherwise short−circuits, the NCP1840 will detect this over−current condition and turn off the reference current and LED outputs. This helps to prevent damage to the chip and system due to elevated currents that would be present.
- The NCP1840 has an on−chip over temperature sensor that will detect any over−temperature condition (130°C − 163°C) and turn off all LED outputs along with the charge pump. In an over−temperature state, bit D0 of the Main Status Register will be set to a logic one. When the over−temperature condition goes away, the part will resume normal operation and bit D0 will be set to a logic zero. The D0 bit of the Main Status Register can be read through the I^2C interface and can be used to provide feedback to the Master controller. This helps to protect the chip and system in the event that the temperature increases beyond a safe operating condition.

Soft Start−Up

The NCP1840 has an on−chip power−on−reset (POR) circuitry that is used to provide soft start−up. As the supply voltage is applied, the POR will sense when the voltage reaches a level that will allow all circuitry to operate correctly. It then will gradually apply this supply voltage to the chip to minimize noise and reduce EMI. If during operation the supply voltage drops, the POR will ensure that the part is reset before the voltage reaches a level where the circuitry won't operate as intended. This helps to mitigate strange operation during a power glitch or brown−out situation.

All registers are reset to all zeros on start−up.

Low Power Mode

The NCP1840 minimizes power consumption by entering into low power mode about 5 ms after all LED outputs are turned OFF and there is no I^2C communication. During low power mode, the I^2C interface is still active and all register settings are retained, but the charge pump and other circuitry that is not needed is powered down. Bit D2 of the Main Status Register is set to a logic one during low power mode. The part is brought out of this mode when the Master initiates communication with it via the I^2C interface. When this happens, the part returns to normal operation and bit D2 is set to a logic zero. Therefore, when the Master wakes up the device, it can read bit D2 and wait for this bit to change to 0, indicating that all circuitry is back to full operation. The transition period from when the part receives the wake−up to full normal operation takes less than 1 ms.

Unused LED Channels

Any of the 8 LED channels that are not needed should be tied to the charge pump output to ensure that these channels remain OFF and to save power consumption that would otherwise be lost.

EXAMPLE

Objective: To set the currents for each LED, except LED8, to 1.5 mA. LED8 will be set to 3.0 mA. All LEDs will have a 50% PWM duty cycle. After these registers are loaded, then only LEDs 1, 2, 3, 4, and 8 will be activated. Later, LED8 will be turned off. Lastly the PWM register value for LED1 will be read. Note that R_{BIAS} = 10.25 kΩ for this example.

Step 1. Set the current level for ALL LEDs to 1.5 mA.
1.1 Set the Part Address to 1B (hex).
1.2 Set the Read/Write bit to 0.
1.3 Set the Control Bits to 011 to program all Current Level Registers at the same time.
1.4 Set the Data to 05 (hex), which will set the current to 1.5 mA.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	011	Don't Care	A	00000101	A	P

Step 2. Set the current level for LED8 to 3.0 mA.
2.1 Set the Part Address to 1B (hex).
2.2 Set the Read/Write bit to 0.
2.3 Set the Control Bits to 001 and set the Register address to 07 (hex) to write to LED8 Current Level Register.
2.4 Set the Data to 0B (hex), which will set the current to 3.0 mA.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	001	00111	A	00001011	A	P

Step 3. Set the PWM duty cycle for all LEDs to 50%.
3.1 Set the Part Address to 1B (hex).
3.2 Set the Read/Write bit to 0.
3.3 Set the Control Bits to 100 to program all PWM Registers at the same time.
3.4 Set the Data to 20 (hex), which will set the PWM duty cycle to 50%.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	100	Don't Care	A	00100000	A	P

Step 4a. Set LEDs 1, 2, 3, 4, 8 to be ON and immediately activate the change with settings loaded in Steps 1−3.
4a.1 Set the Part Address to 1B (hex).
4a.2 Set the Read/Write bit to 0.
4a.3 Set the Control Bits to 010 and set the Register address to 10 (hex) to write to the Output Control Register.
4a.4 Set the Data to 8F (hex), which will set LEDs 1, 2, 3, 4, 8 to be ON.
Note: After this step the LEDs will immediately be activated with the current level and PWM duty cycle settings previously loaded.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	010	10000	A	10001111	A	P

Step 4b. (Alternative to Step 4a.) Set LEDs 1, 2, 3, 4, 8 to be ON and later activate the change with settings loaded in Steps 1−3.
4b.1 Set the Part Address to 1B (hex).
4b.2 Set the Read/Write bit to 0.
4b.3 Set the Control Bits to 001 and set the Register address to 10 (hex) to write to the Output Control Register.
4b.4 Set the Data to 8F (hex), which will set LEDs 1, 2, 3, 4, 8 to be ON.
Note: After this step the LEDs will not be activated until either a 000 or 010 Control Bit setting is applied − see further 4b steps.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	001	10000	A	10001111	A	P

4b.5 Set the Part Address to 1B (hex).
4b.6 Set the Read/Write bit to 0.
4b.7 Set the Control Bits to 000.
Note: After this step the LEDs will immediately be activated with the current level and PWM duty cycle settings previously loaded.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Stop
S	0011011	0	A	000	Don't Care	A	P

Step 5. Turn OFF LED8, leaving LEDs 1, 2, 3, 4 ON.
5.1 Set the Part Address to 1B (hex).
5.2 Set the Read/Write bit to 0.
5.3 Set the Control Bits to 010 and set the Register address to 10 (hex) to write to the Output Control Register.
5.4 Set the Data to 0F (hex), which will set LED8 OFF and leave LEDs 1, 2, 3, 4 ON.

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Register Data	Ack	Stop
S	0011011	0	A	010	10000	A	00001111	A	P

Step 6. Read back the LED1 PWM Register value.
6.1 Set the part address to 1B (hex).
6.2 Set the Read/Write bit to 0.
6.3 Set the Controls Bits to 001 in order to perform a Read operation.
6.4 Set the Register Address to 08 (hex) in order to read LED1 PWM Register.
6.5 Issue another Start and set the part address to 1B (hex).
6.6 Set the Read/Write bit to 1.
Note: After this step, the NCP1840 will transmit the LED1 PWM Register data byte which should be 20 (hex).

Start	Part Address	R/W	Ack	Control Bits	Register Address	Ack	Start	Part Address	R/W	Ack	Register Data	Ack	Stop
S	0011011	0	A	001	01000	A	S	0011011	1	A	Data Out	notA	P

LAYOUT CONSIDERATIONS

Some key layout guidelines are as follows:
1. The NCP1840 requires a low−inductance ground.
2. Connect Pin 6 and Pin 15 to the “ground pad” of the NCP1840’s package − see Figure 15.
3. Place vias on the “ground pad,” connecting the GND of the NCP1840 directly to the PCB ground plane − see Figure 15.

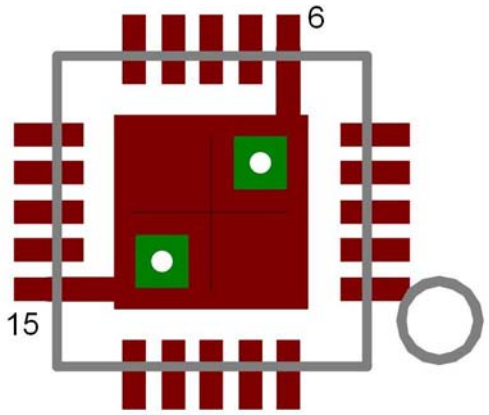


Figure 15. Ground Connection Recommendation

4. Use good−quality X5R or X7R ceramic capacitors for C_0, C_1, C_2, and C_{BAT} − see Figure 16.

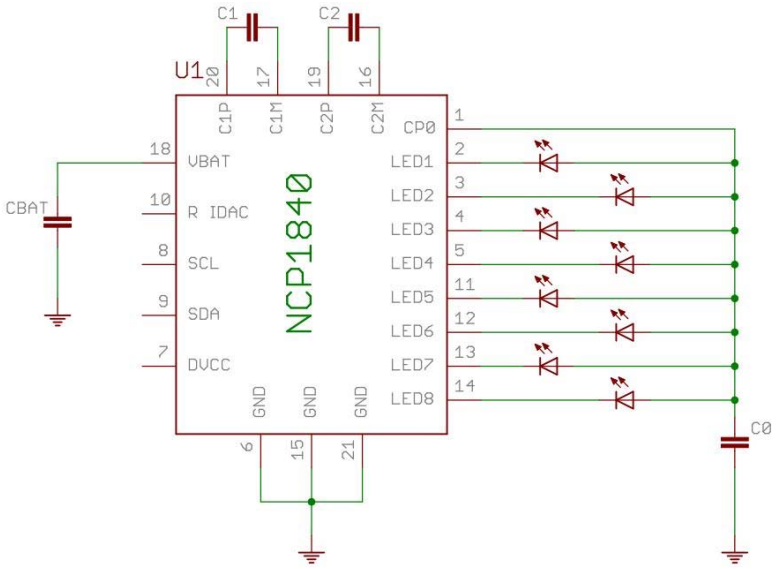


Figure 16. Schematic Showing Charge Pump and Decoupling Capacitors

5. Charge pump capacitors C_0, C_1, C_2, and decoupling capacitor C_{BAT} should be as physically close to the NCP1840 as possible − see Figure 17.

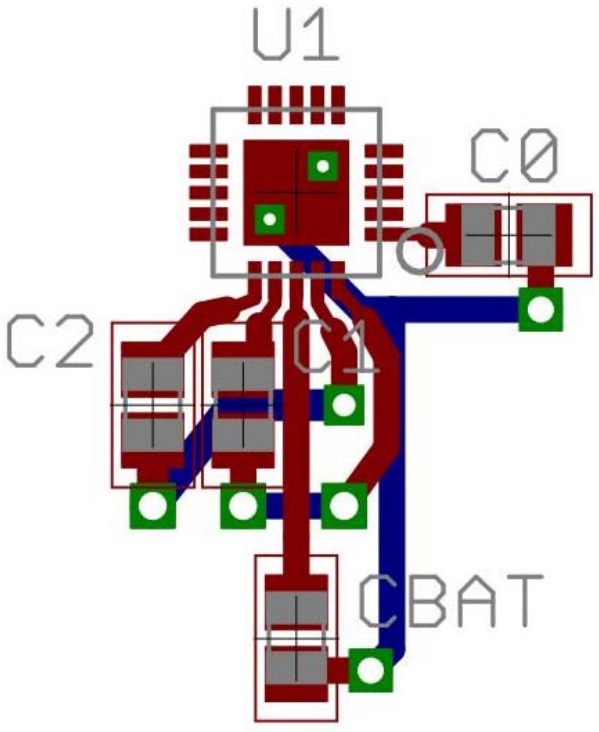


Figure 17. C_0, C_1, C_2, and C_{BAT} Layout Recommendation

QUAD−MODE is a registered trademark of Semiconductor Components Industries, LLC (SCILLC).

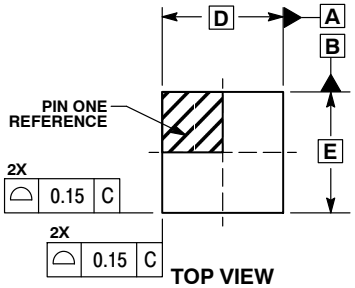
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

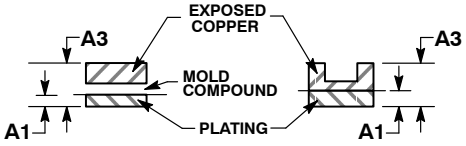
QFN20, 4x4, 0.5P
CASE 485E
ISSUE C

DATE 13 FEB 2018

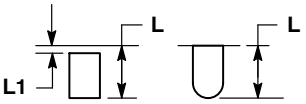


SCALE 2:1

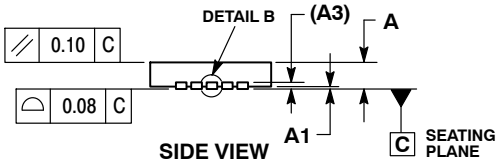




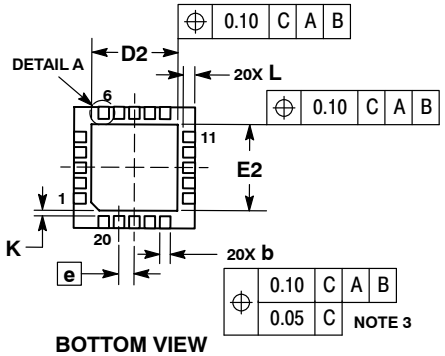
DETAIL B
ALTERNATE CONSTRUCTIONS



DETAIL A
OPTIONAL CONSTRUCTIONS

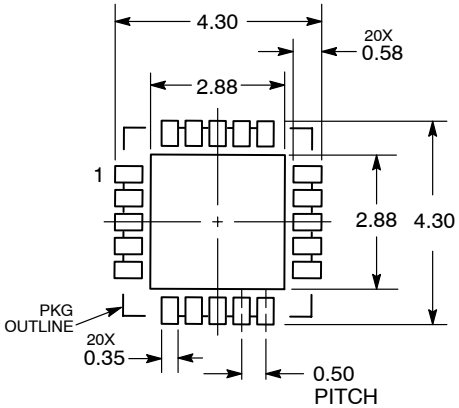


SIDE VIEW



BOTTOM VIEW

SOLDERING FOOTPRINT*



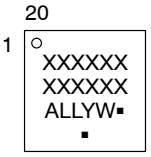
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

GENERIC MARKING DIAGRAM*



XXXXXX= Specific Device Code
A = Assembly Location
LL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03163D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN20, 4X4, 0.5P**	**PAGE 1 OF 1**

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊