NCP2824

Non−Clip and Power Limit Mono Class D Amplifier with AGC

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9 PIN FLIP−CHIP
FC SUFFIX
CASE 499AL

Description

The NCP2824 is a Filterless Class D amplifier capable of delivering up to 2.4 W to a 4 Ω load with a 5 V supply voltage. With the same battery voltage, it can deliver 1.2 W to an 8 Ω load with less than 1% THD+N. The non−clipping function automatically adjusts the output voltage in order to control the distortion when an excessive input is applied to the amplifier. This adjustment is done thanks to an Automatic Gain Control circuitry (AGC) built into the chip. A simple Single wire interface allows to the non Clipping function to be enabled and disabled. It also allows the maximum distortion level in the output to be configured. A programmable power limit function is also embedded in order to protect speakers from damage caused by an excessive sound level.

Features

- Non Clipping Function with Automatic Gain Control Circuitry
- Programmable Power Limit Function
- Single Wire Interface. No Need for Additional Components
- Max THD+N Configurable by Swire Interface
- Only One Capacitor Required
- Fully Differential Architecture: Better RF Immunity
- No Need for Input Capacitors in Fully Differential Configuration
- High Efficiency: up to 90%
- Low Quiescent Current: 2.2 mA Typ
- Large Output Power Capability
- High PSRR: up to −80 dB
- Fully Differential Capability: RF Immunity
- Thermal and Auto Recovery Short−Circuit Protection
- CMRR (−80 dB) Eliminates Two Input Coupling Capacitors
- Pb−Free and Halide−Free Device

Typical Applications

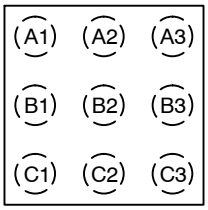
Audio Amplifier for:

- Cellular Phones
- Digital Cameras
- Personal Digital Assistant and Portable Media Player
- GPS

Demo Board Available:

- The NCP2824GEVB/D evaluation board configures the device in typical application.

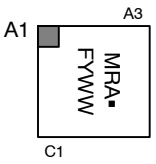
PIN CONFIGURATION



(Top View)

A1 = INP	B1 = AGND	C1 = INM
A2 = VDD	B2 = NC	C2 = CNTL
A3 = OUTP	B3 = PGND	C3 = OUTM

MARKING DIAGRAM



MRA	= Specific Device Code
F	= Assembly Location
Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP2824FCT2G	WCSP−9 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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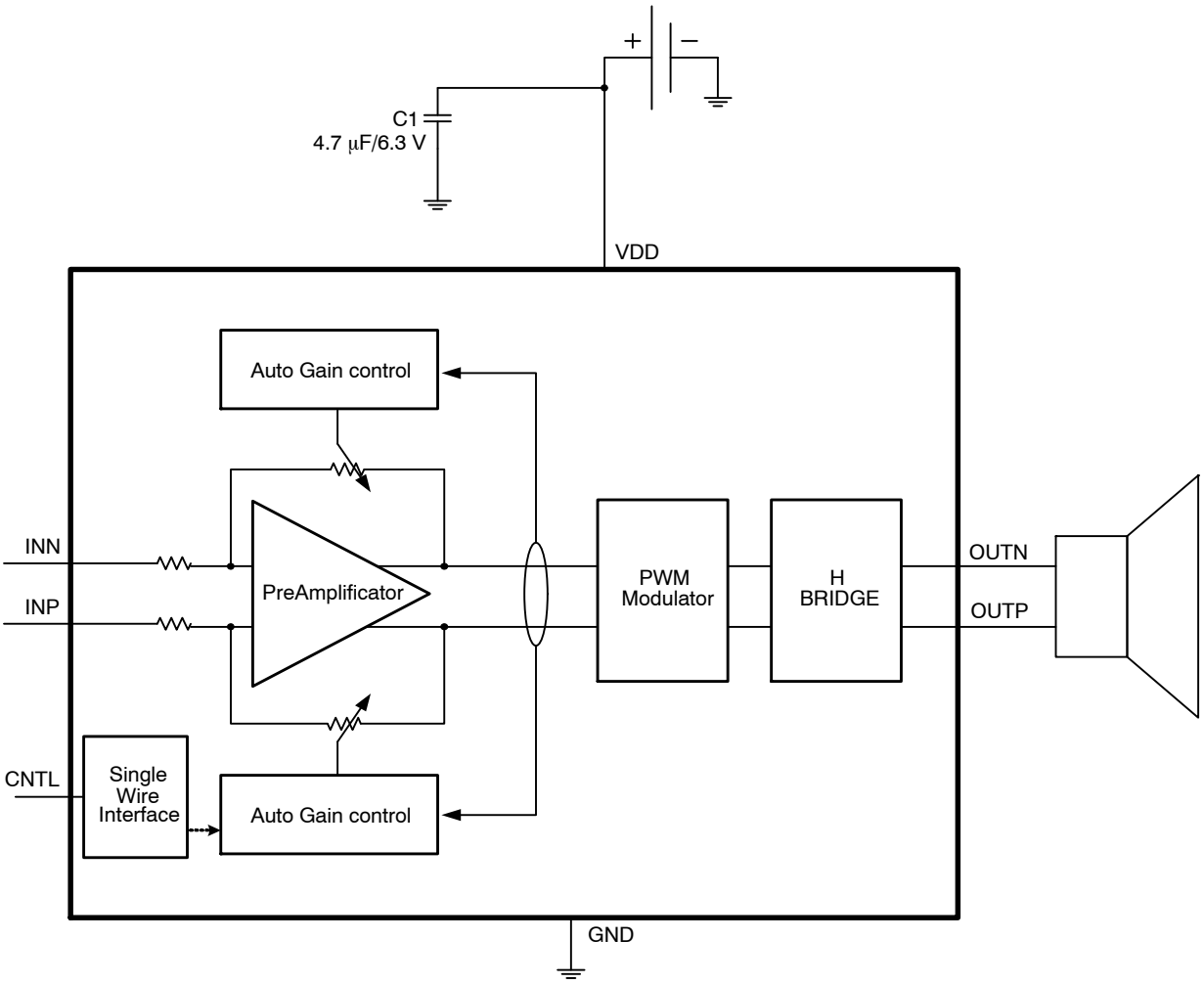


Figure 1. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	INP	Input	**Positive Input**
C1	INN	Input	**Negative Input**
A2	PVDD	POWER	**Power Supply:** This pin is the power supply of the device. A 4.7 μF ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
B2	NC	–	**Non−connected:** reserved for production. Must be kept floating in the final application
A3	OUTP	Output	**Positive output:** Special care must be observed at layout level. See the Layout consideration section
C3	OUTN	Output	**Negative output:** Special care must be observed at layout level. See the Layout consideration section
C2	CNTL	Input	**Control:** This pin is dedicated to the control of the chip via the Single wire protocol
B3	PGND	POWER	**Power Ground:** This pin is the power ground and carries the high switching current. A high quality ground must be provided to avoid any noise spikes/uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track.
B1	AGND	POWER	**Analog Ground:** This pin is the analog ground of the device and must be connected to GND plane.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
AVDD, PVDD Pins: Power Supply Voltage (Note 2)	V_{DD}	−0.3 to +6.0	V
INP/N Pins: Input (Note 2)	$V_{INP/N}$	−0.3 to +V_{DD}	V
Digital Input/Output: EN Pin: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_{DD} + 0.3 1	 V mA
Human Body Model (HBM) ESD Rating are (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)	ESD MM	200	V
WCSP 1.5 x 1.5 mm package (Notes 6 and 7) Thermal Resistance Junction to Case	 $R_{\theta JC}$	 90	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+150	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 150°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation (PD) is dependent on the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

Table 3. ELECTRICAL CHARACTERISTICS (Min & Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{DD} = 3.6 V. (see Note 8))

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GENERAL PERFORMANCES						
V_{DD}	Operational Power Supply		2.5		5.5	V
F_{OSC}	Oscillator Frequency		250	300	350	kHz
I_{dd}	Supply current	V_{DD} = 3.6 V, No Load V_{DD} = 5.5 V, No Load, T_A = 85°C		2.2	 4.2	mA
I_{sd}	Shutdown current	V_{DD} = 3.6 V, V_{CNTL} = 0 V V_{DD} = 5.5 V, V_{CNTL} = 0 V, T_A = 85°C		0.01	 1	μA
T_{ON}	Turn ON Time	Single Wire Activation		7.4		ms
T_{OFF}	Turn Off Time	Single Wire Deactivation		5		ms
Z_{sd}	Class D Output impedance in shutdown mode	V_{ENL} = 0 V		20		kΩ
$R_{DS(ON)}$	Static drain−source on−state resistance of power Mosfets			250		mΩ
η	Efficiency	V_{DD} = 3.6 V, Po = 800 mW, RL = 8 Ω, F = 1 kHz		86		%
		V_{DD} = 3.6 V, Po = 1.3 W, RL = 4 Ω, F = 1 kHz		79		
F_{LP}	−3 dB Cut off Frequency of the Built in Low Pass Filter			 30		kHz
T_{SD}	Thermal Shut Down Protection			150		°C
T_{SDH}	Thermal Shut Down Hysteresis			20		°C
AGC SECTION						
Av	Voltage gain	Single Wire 4		12		dB
Av	Voltage gain	Single Wire 5		18		dB
Aa	Max AGC attenuation			−15		dB
Avn	AGC Gain step resolution			0.5		dB
T_A	Attack time			0.033		ms/Step
T_R	Release Time			0.013		s/Step
T_H	Hold Time			0.013		s/Step
S−WIRE INTERFACE (see Note 9)						
V_{IH}	Rising Voltage Input Logic High		1.2	−	5.5	V
V_{IL}	Falling Voltage Input Logics Low		0	−	0.4	V
V_{IHYS}	Input Voltage Hysteresis			100		mV
R_{PLD}	Pull Down Resistor			20		kΩ
T_R	Swire Rising time				200	ns
T_F	Swire Falling time				200	ns
T_{SWH}	Swire High		5	10	45	μs
T_{SWL}	Swire Low		5	10	75	μs

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C.
9. Single Wire performances is guaranteed by design and characterized
10. Audio performances are given for Vdd = 3.6 V, T_A = 25°C and characterized

Table 3. ELECTRICAL CHARACTERISTICS (Min & Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = +25°C and V_{DD} = 3.6 V. (see Note 8))

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
S−WIRE INTERFACE (see Note 9)								
F_{SWF}	Input S−wire Frequency						100	kHz
T_{EHDT}	Enable High Delay Time				0		400	μs
T_{SDD}	Time to Shunt Down Delay				300		400	μs
$T_{WAKE-UP}$	Time to Wake up from shutdown						500	μs
T_{VALID}	Time to Valid Data				300		400	μs
AUDIO PERFORMANCES (see Note 10)								
v_{oo}	Output offset	Av = 12 dB				0.3		mV
$PSRR_{DC}$	Power supply rejection ratio	From V_{DD} = 2.5 V to 5.5 V				−80		dB
$PSRR_{AC}$	Power supply rejection ratio	F = 217 Hz, Input ac grounded, Av = 12 dB				−70		dB
		F = 1 kHz, Input ac grounded Av = 12 dB				−70		
SNR	Signal to noise ratio	Vp = 5 V, Pout = 600 mW (A. Weighted) Av = 12 dB				96		dB
CMRR	Common mode rejection ratio	Input shorted together V_{IC} = 1 V_{pp}, f = 217 Hz				−80		dB
Vn	Output Voltage noise	Input ac grounded, Av = 12 dB 20 Hz < f < 20 kHz A. Weighted				34		μV
Po	Output Power	RL = 8 Ω F = 1 kHz	THD+N<1%	V_{DD} = 5 V		1.2		W
				V_{DD} = 3.6 V		0.6		
				V_{DD} = 2.5 V		0.22		
			THD+N<10%	V_{DD} = 5 V		1.5		
				V_{DD} = 3.6 V		0.8		
				V_{DD} = 2.5 V		0.4		
		RL = 4 Ω F = 1 kHz	THD+N<1%	V_{DD} = 5 V		2		
				V_{DD} = 3.6 V		1		
				V_{DD} = 2.5 V		0.4		
			THD+N<10%	V_{DD} = 5 V		2.4		
				V_{DD} = 3.6 V		1.3		
				V_{DD} = 2.5 V		0.6		
THD+N	Total harmonic distortion plus noise	V_{DD} = 3.6 V, Po = 0.5 W				0.06		%
		V_{DD} = 5 V, Po = 1 W				0.09		

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at $T_J = T_A$ = 25°C.
9. Single Wire performances is guaranteed by design and characterized
10. Audio performances are given for Vdd = 3.6 V, T_A = 25°C and characterized

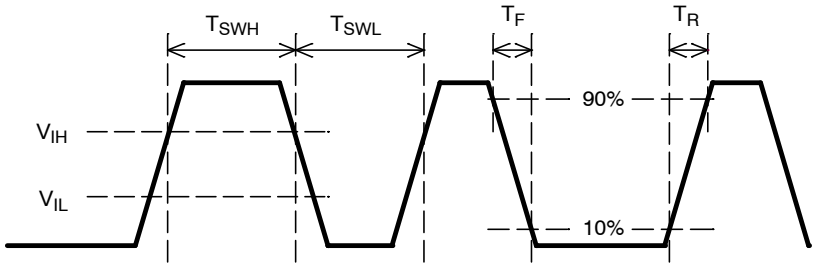


Figure 2. S−Wire Logic Diagram

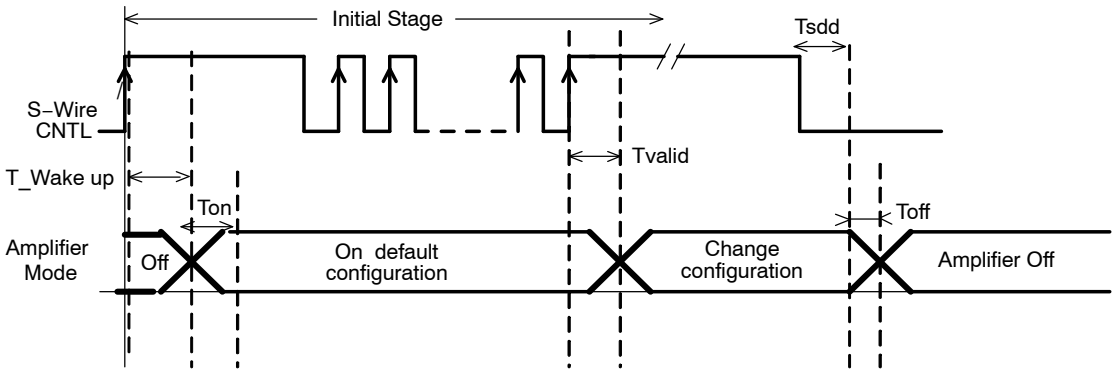


Figure 3. S−Wire / Enable Timing Diagram

TYPICAL OPERATING CHARACTERISTICS

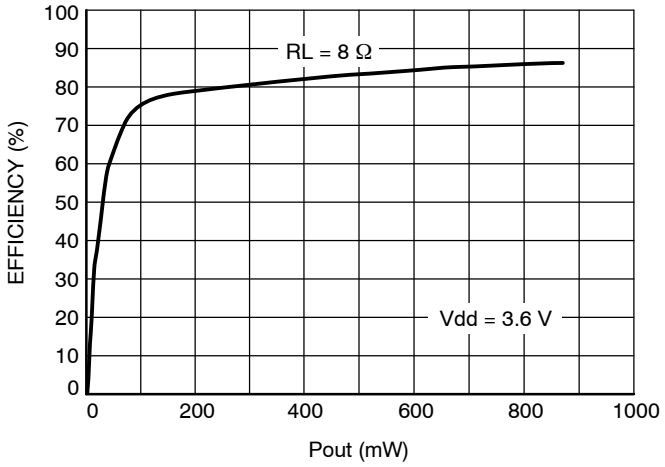


Figure 4. Efficiency vs. Pout

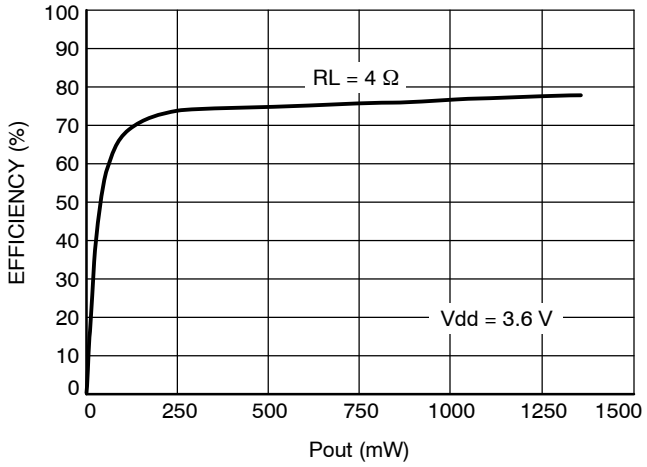


Figure 5. Efficiency vs. Pout

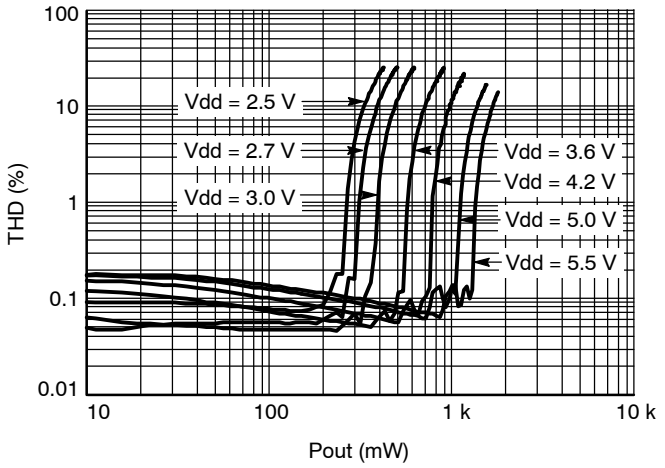


Figure 6. THD+N vs. Pout, RL = 8 Ω

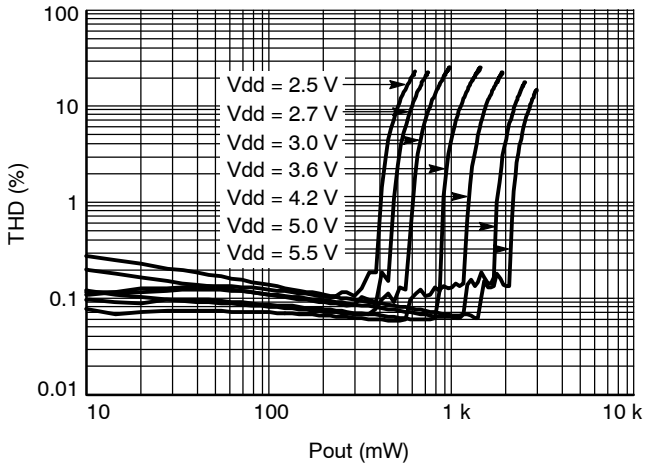


Figure 7. THD+N vs. Pout, RL = 4 Ω

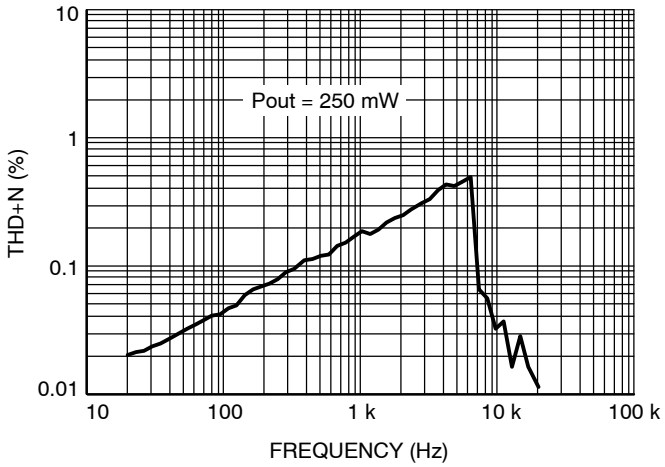


Figure 8. THD+N vs. Frequency, Vdd = 2.5 V

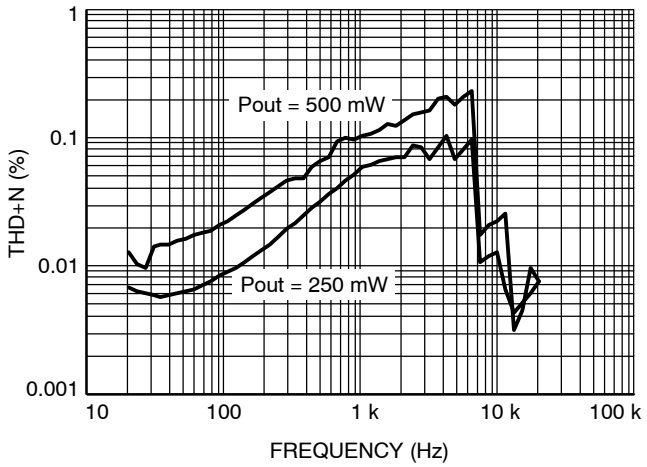


Figure 9. THD+N vs. Frequency, Vdd = 3.6 V

TYPICAL OPERATING CHARACTERISTICS

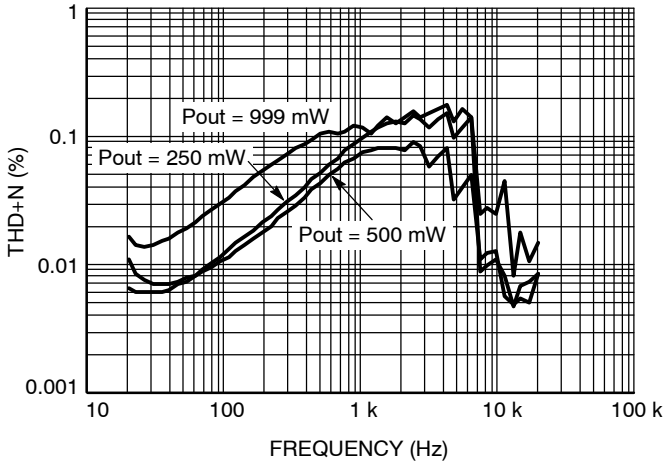


Figure 10. THD+N vs. Frequency, Vdd = 5 V

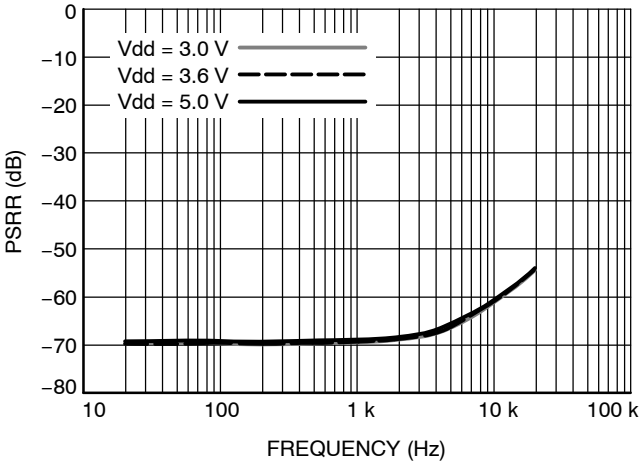


Figure 11. PSRR vs. Frequency (Inputs Grounded, Gain = 12 dB, Cin = 1 μF)

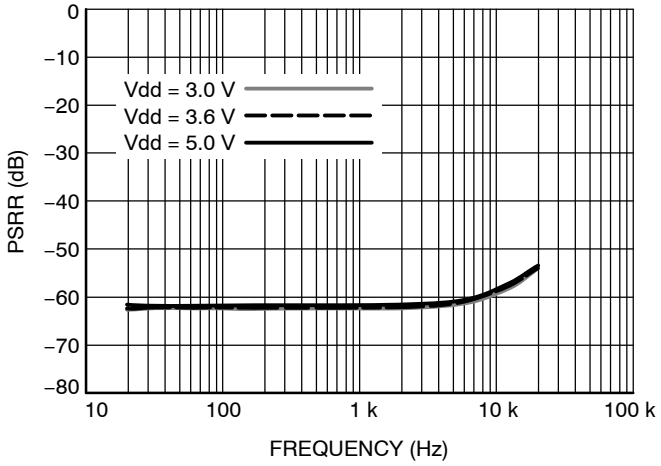


Figure 12. PSRR vs. Frequency (Inputs Grounded, Gain = 18 dB, Cin = 1 μF)

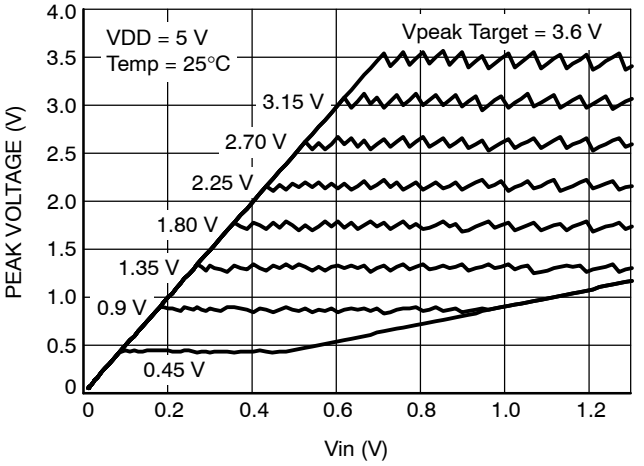


Figure 13. Peak Output Voltage in Power Limit vs. Input Voltage (rms) and Power Limit Settings, Av = 12 dB

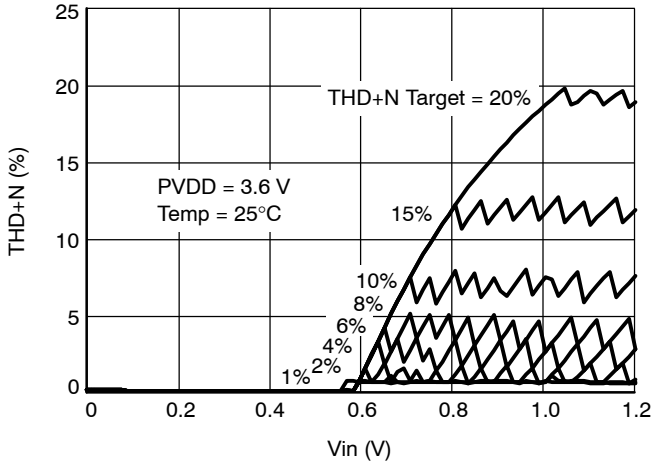


Figure 14. THD+N vs. Input Voltage (rms) and Non Clip Settings, RL = 8 Ω, Av = 12 dB

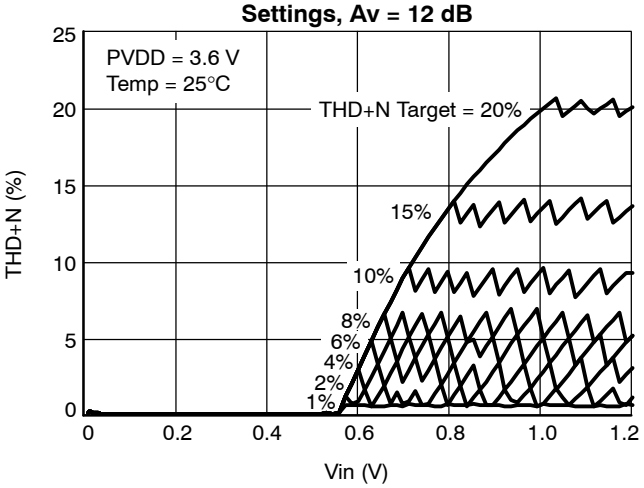


Figure 15. THD+N vs. Input Voltage (rms) and Non Clip Settings, RL = 4 Ω, Av = 12 dB

Detailed Operating Description

General Description

The NCP2824 is a Mono class D audio amplifier featuring a preamplifier stage, a PWM stage and an H−Bridge stage with an automatic Gain control circuitry which performs the non clipping function.

Non Clipping Function

In the presence of an exceeded input signal, when the audio signal is going to be clipped, the gain of the audio amplifier automatically decreases as defined by the AGC operation. The maximum level of THD is programmable and can be set by a final user through the single wire interface (see table n°1).

At the same time, the battery voltage is continuously monitored. The output signal is adapted to the dynamic battery voltage (Vdd) in order to avoid distortion due to supply voltage fluctuation like GSM burst.

This function solution allows the chip to maximize the sound pressure level while maintaining a controlled THD level.

The following picture depicts the non clipping operation.

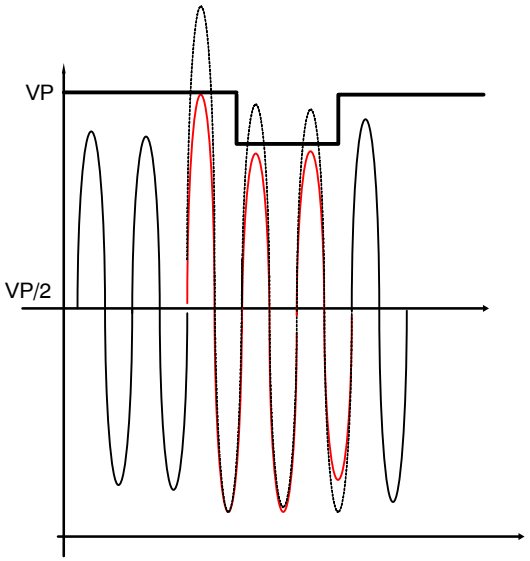


Figure 16. Output of the Amplifier during a Line Transient on the Battery Voltage

Power Limit Function: Speaker Protection

In addition to the non clipping function, a Power limit function is embedded in the NCP2824 in order to protect speakers from excessive output signal levels. When the output signal exceed this limit, the ???

Thus, the final user can use the Single Wire interface to program the maximum voltage rated by the speaker or to disable this power limit protection.

AGC Operation

The AGC operation defines the timings when the non clipping function is engaged.

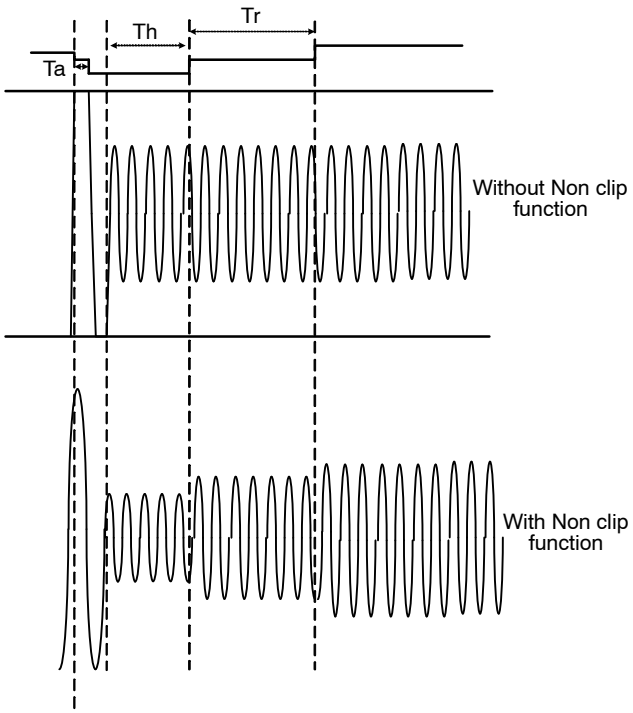
The typical values are described in the Electrical Table (“AGC Section”).

Attack time (Ta): is defined as the minimum time between two gain decrease.

Hold time (Th): is defined as the minimum time between a gain increase after a gain decrease.

Release time (Tr): is defined as the minimum time between two gain increase.

The following pictures depict the NCP2824 non clipping operation.



Single Wire Interface Operation

The single wire interface allows changing the default configuration of the NCP2824.

After Wake up, the NCP2824 is configured with:

- AGC enable
- Non Clip + Power limit
- Gain = 18 dB
- THD max = 1%

The following table described all the NCP2824 configurations.

Table 4. NCP2824 CONFIGURATION

Pulse Counting	Register	Description
01	AGC	AGC disable
02		AGC Enable
03	Reset	Reset configuration
04	Gain Control	Gain = 12 dB
05		Gain = 18 dB
06	THD Control	1%
07		2%
08		4%
09		6%
10		8%
11		10%
12		15%
13		20%
14	NC+L	Non Clip + Power limit
15	NC	Non Clip only
16	Power Limit Control	0.45 V_{Peak}
17		0.9 V_{Peak}
18		1.35 V_{Peak}
19		1.8 V_{Peak}
20		2.25 V_{Peak}
21		2.7 V_{Peak}
22		3.15 V_{Peak}
23		3.6 V_{Peak}

NOTE: The given values are typical for Vdd = 3.6 V and T_A = 25°C characterized

Built−in Low Pass Filter

This filter allows the user to connect a DAC or a CODEC directly to the NCP2824 input without increasing the output noise by mixing frequency with the DAC/CODEC output frequency. Consequently, optimized operation with DACs or CODECs is guaranteed without additional external components.

Decoupling Capacitors

The NCP2824 requires a correct decoupling of the power supply in order to guarantee the best operation in terms of audio performances. To achieve optimum performance, it is necessary to place a 4.7 μF low ESR ceramic capacitor as close as possible to the VDD pin in order to reduce high frequency transient spikes due to parasitic inductance (see Layout considerations).

Input Capacitors Cin

Thanks to its fully differential architecture, the NCP2824 does not require input capacitors. However, it is possible to use input capacitors when the differential source is not biased or in single ended configuration. In this case it is necessary to take into account the corner frequency which can influence the low frequency response of the NCP2824. The following equation will help choose the adequate input capacitor.

$$fc = \frac{1}{2 \cdot \pi \cdot 75 \cdot 10^3 \cdot Cin}$$

Over Current Protection

This protection allows an over current in the H−Bridge to be detected. When the current is higher than 2 A, the H−Bridge is positioned in high impedance. When the short circuit is removed or the current is lower, the NCP2824 goes back to normal operation. This protection avoids over current due to a bad assembly (Output shorted together, to Vdd or to ground).

Layout Recommendations

For Efficiency and EMI considerations, it is strongly recommended to use Power and ground plane in order to reduce parasitic resistance and inductance.

For the same reason, it is recommended to keep the output traces short and well shielded in order to avoid them to act as antenna.

The level of EMI is strongly dependent upon the application. However, ferrite beads placed close to the NCP2824 will reduce EMI radiation when it is needed.

Ferrite value is strongly dependent upon the application.

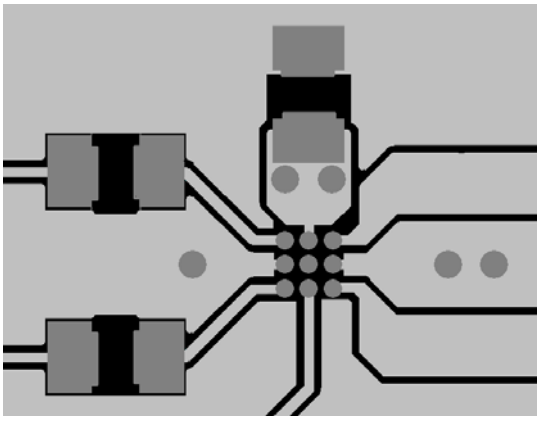


Figure 17. Example of PCB Layout

Components Selection

To achieve optimum performance, one 4.7 μF 6.3 V X5R should be used to bypass the power input supply (VDD).

Also particular care must be observed for DC−bias effects in the ceramic capacitor selection. Smaller case−size and higher DC bias voltage is preferred.

Some recommended capacitors include but are not limited to:

4.7 μF 6.3 V 0603

TDK: C1608X5R0J475MT 0.95 mm max.

Example of Application Schematic

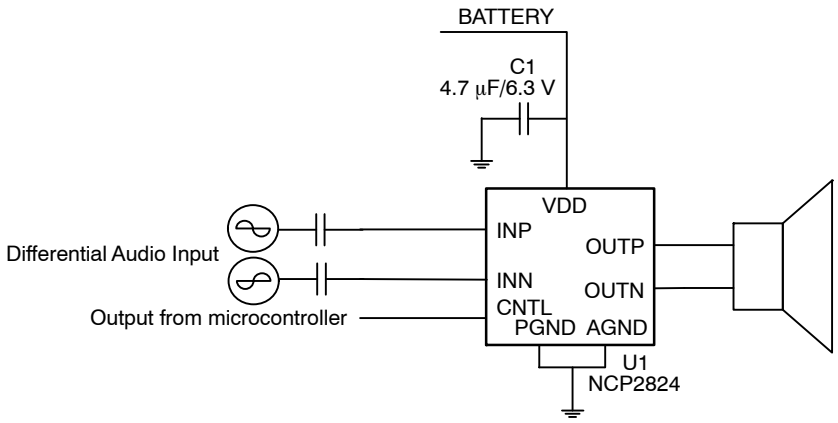


Figure 18. Differential Configuration

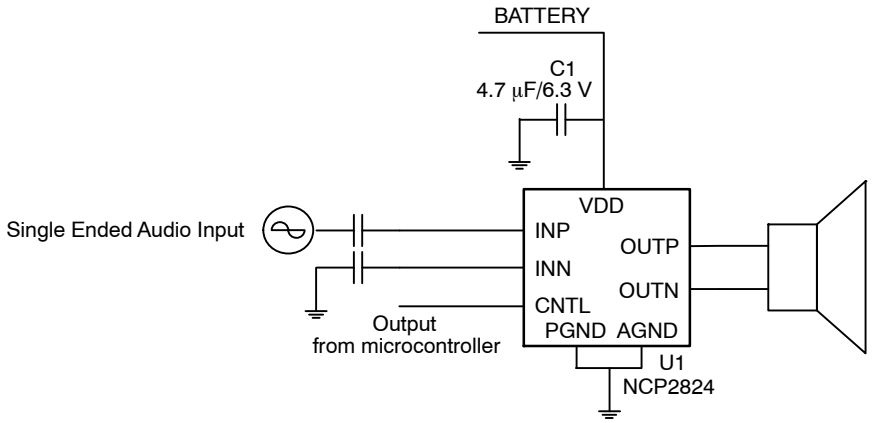
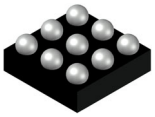
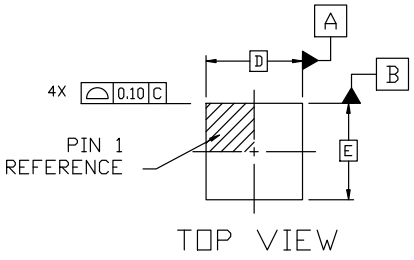


Figure 19. Single Ended Configuration

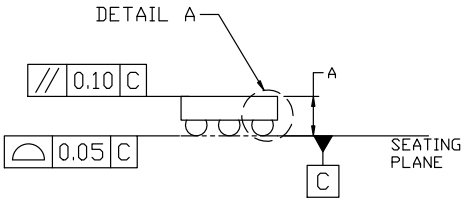


9 PIN FLIP−CHIP 1.45x1.45x0.596
CASE 499AL
ISSUE A

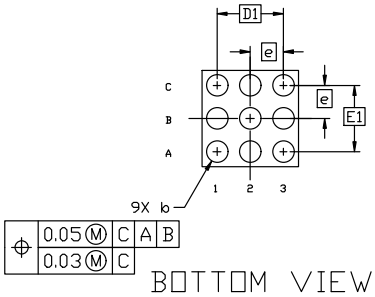
DATE 21 JUN 2022



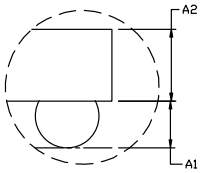
TOP VIEW



SIDE VIEW



BOTTOM VIEW

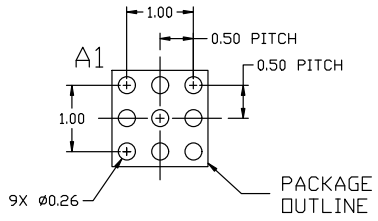


DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

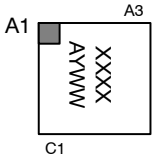
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.541	0.596	0.651
A1	0.206	0.236	0.266
A2	0.335	0.360	0.385
b	0.289	0.319	0.349
D	1.450 BSC		
D1	1.000 BSC		
E	1.450 BSC		
E1	1.000 BSC		
e	0.50 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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