NCP5007

Compact Backlight LED Boost Driver

The NCP5007 is a high efficiency boost converter operating in a current control loop, based on a PFM mode, to drive White LEDs. The current mode regulation allows a uniform brightness of the LEDs. The chip has been optimized for small ceramic capacitors and is capable of supplying up to 1.0 W output power.

Features

- Inductor Based Converter brings High Efficiency
- Constant Output Current Regulation
- 2.7 to 5.5 V Input Voltage Range
- V_{out} to 22 V Output Compliance Allows up to 5 LEDs to be Driven in Series which Provides Automatic LED Current Matching
- Built−in Output Overvoltage Protection
- 0.3 μA Standby Quiescent Current
- Includes Dimming Function (PWM)
- Enable Function Driven Directly from Low Battery Voltage Source
- Thermal Shutdown Protection
- All Pins are Fully ESD Protected
- Low EMI Radiation
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LED Display Back Light Control
- High Efficiency Step Up Converter

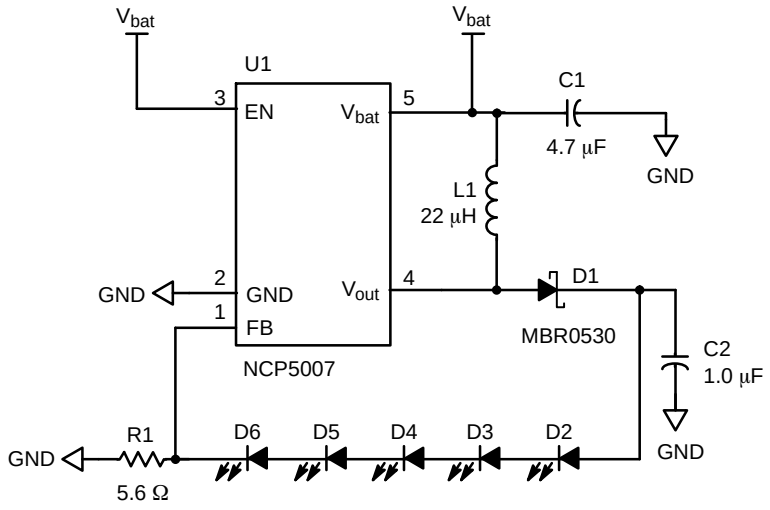
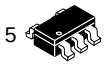


Figure 1. Typical Application

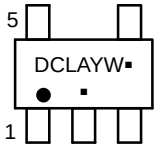
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TSOP−5
(SOT23−5, SCR59−5)
SN SUFFIX
CASE 483

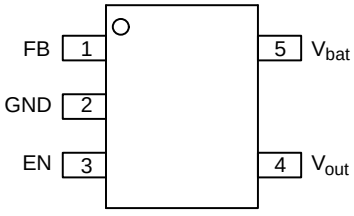
MARKING DIAGRAM



DCL = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5007SNT1G	TSOP−5 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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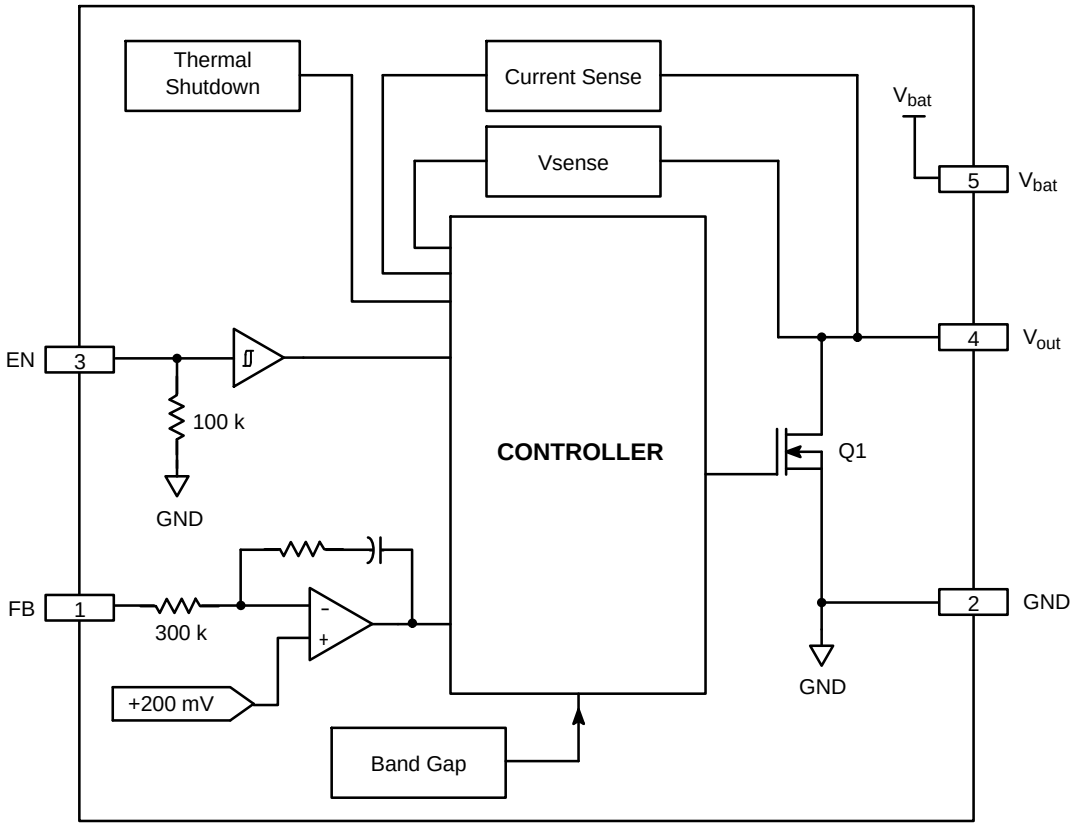


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1	FB	ANALOG INPUT	This pin provides the output current range adjustment by means of a sense resistor connected to the analog control or with a PWM control. The dimming function can be achieved by applying a PWM voltage technique to this pin (see Figure 29). The current output tolerance depends upon the accuracy of this resistor. Using a ±5% metal film resistor, or better, yields good output current accuracy. Note: A built−in comparator switches OFF the DC−DC converter if the voltage sensed across this pin and ground is higher than 700 mV typical.
2	GND	POWER	This pin is the system ground for the NCP5007 and carries both the power and the analog signals. High quality ground must be provided to avoid spikes and/or uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track so a robust ground plane connection is recommended.
3	EN	DIGITAL INPUT	This is an Active−High logic input which enables the boost converter. The built−in pulldown resistor disables the device when the EN pin is left open. Note the logic switching level of this input has been optimized to allow it to be driven from standard or 1.8 V CMOS logic levels. The LED brightness can be controlled by applying a pulse width modulated signal to the enable pin (see Figure 30).
4	V_{out}	POWER	This pin is the power side of the external inductor and must be connected to the external Schottky diode. It provides the output current to the load. Since the boost converter operates in a current loop mode, the output voltage can range up to +22 V but shall not exceed this limit. However, if the voltage on this pin is higher than the OVP threshold (Over Voltage Protection) the device enters a shutdown mode. To restart the chip, one must either apply a low to high logic signal to the EN pin, or switch off the V_{bat} supply. A capacitor must be used on V_{out} to avoid false triggering of the OVP (Overvoltage Protect) circuit. This capacitor filters the noise created by the fast switching transients. In order to limit the inrush current and still have acceptable startup time the capacitor value should range between 1.0 μF and 8.2 μF max. To achieve high efficiency this capacitor should be ceramic (ESR $<$ 100 mΩ). Care must be observed to avoid EMI through the PCB copper tracks connected to this pin.
5	V_{bat}	POWER	The external voltage supply is connected to this pin. A high quality reservoir capacitor must be connected across pin 5 and Ground to achieve the specified output voltage parameters. A 4.7 μF/6.3 V, low ESR capacitor must be connected as close as possible across pin 5 and ground pin 2. The X5R or X7R ceramic MURATA types are recommended. The return side of the external inductor shall be connected to this pin. Typical application will use a 22 μH, size 1210, to handle the 10 to 100 mA output current range. When the desired output current is above 20 mA, the inductor shall have an ESR ≤1.5 Ω to achieve good efficiency over the V_{bat} range. The output current tolerance can be improved by using a larger inductor value.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply	V_{bat}	6.0	V
Output Power Supply Voltage Compliance	V_{out}	28	V
Digital Input Voltage Digital Input Current	EN	$-0.3 \le V_{in} \le V_{bat}$ +0.3 1.0	V mA
ESD Capability (Note 1) Human Body Model (HBM) Machine Model (MM)	V_{ESD}	 2.0 200	 kV V
TSOP5 Package Power Dissipation @ T_A = +85°C (Note 2) Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$	 160 250	 mW °C/W
Operating Ambient Temperature Range	T_A	−25 to +85	°C
Operating Junction Temperature Range	T_J	−25 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
2. The maximum package power dissipation limit must not be exceeded.
3. Latchup current maximum rating: ±100 mA per JEDEC standard: JESD78.
4. Moisture Sensivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION (Typical values are referenced to T_a = +25°C, Min & Max values are referenced −25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
Power Supply	4	V_{bat}	2.7	−	5.5	V
Output Load Voltage Compliance	5	V_{out}	22	24.5	−	V
Continuous DC Current in the Load @ V_{out} = 3 × LED, L = 22 μH, ESR < 1.5 Ω, V_{bat} = 3.6 V	5	I_{out}	50	−	−	mA
Standby Current @ I_{out} = 0 mA, EN = L, V_{bat} = 3.6 V	4	I_{stdb}	−	0.45	−	μA
Standby Current @ I_{out} = 0 mA, EN = L, V_{bat} = 5.5 V	4	I_{stdb}	−	1.0	3.0	μA
Inductor Discharging Time @ V_{bat} = 3.6 V, L = 22 μH, 3 × LED, I_{out} = 10 mA	4	Toffmax	−	320	−	ns
Thermal Shutdown Protection	−	T_{SD}	−	160	−	°C
Thermal Shutdown Protection Hysteresis	−	T_{SDH}	−	30	−	°C

ANALOG SECTION (Typical values are referenced to T_a = +25°C, Min & Max values are referenced −25°C to +85°C ambient temperature, unless otherwise noted.)

Rating	Pin	Symbol	Min	Typ	Max	Unit
High Level Input Voltage Low Level Input Voltage	1	EN	1.3 −	− −	− 0.4	V
EN Pull Down Resistor	1	R_{EN}	−	100	−	kΩ
Feedback Voltage Threshold	4	FB	170	200	230	mV
Output Current Stabilizes @ 5% time delay following a DC−DC startup @ V_{bat} = 3.6 V, L = 22 μH, I_{out} = 20 mA	5	I_{outdly}	−	100	−	μs
Internal Switch ON Resistor @ T_{amb} = +25°C	5	QR_{DSON}	−	1.7	−	Ω

5. The overall tolerance depends upon the accuracy of the external resistor.

THEORY OF OPERATION

The DC−DC converter is designed to supply a constant current to the external load, the circuit being powered from a standard battery supply. Since the regulation is made by means of a current loop, the output voltage will vary depending upon the dynamic impedance presented by the load.

Considering a high intensity LED, the output voltage can range from a low of 6.4 V (two LED in series biased with a low current), up to 22 V, the maximum the chip can sustain continuously. The basic DC−DC structure is depicted in Figure 3.

With a 22 V operating voltage capability, the power device Q1 can accommodate a high voltage source without any leakage current degradation.

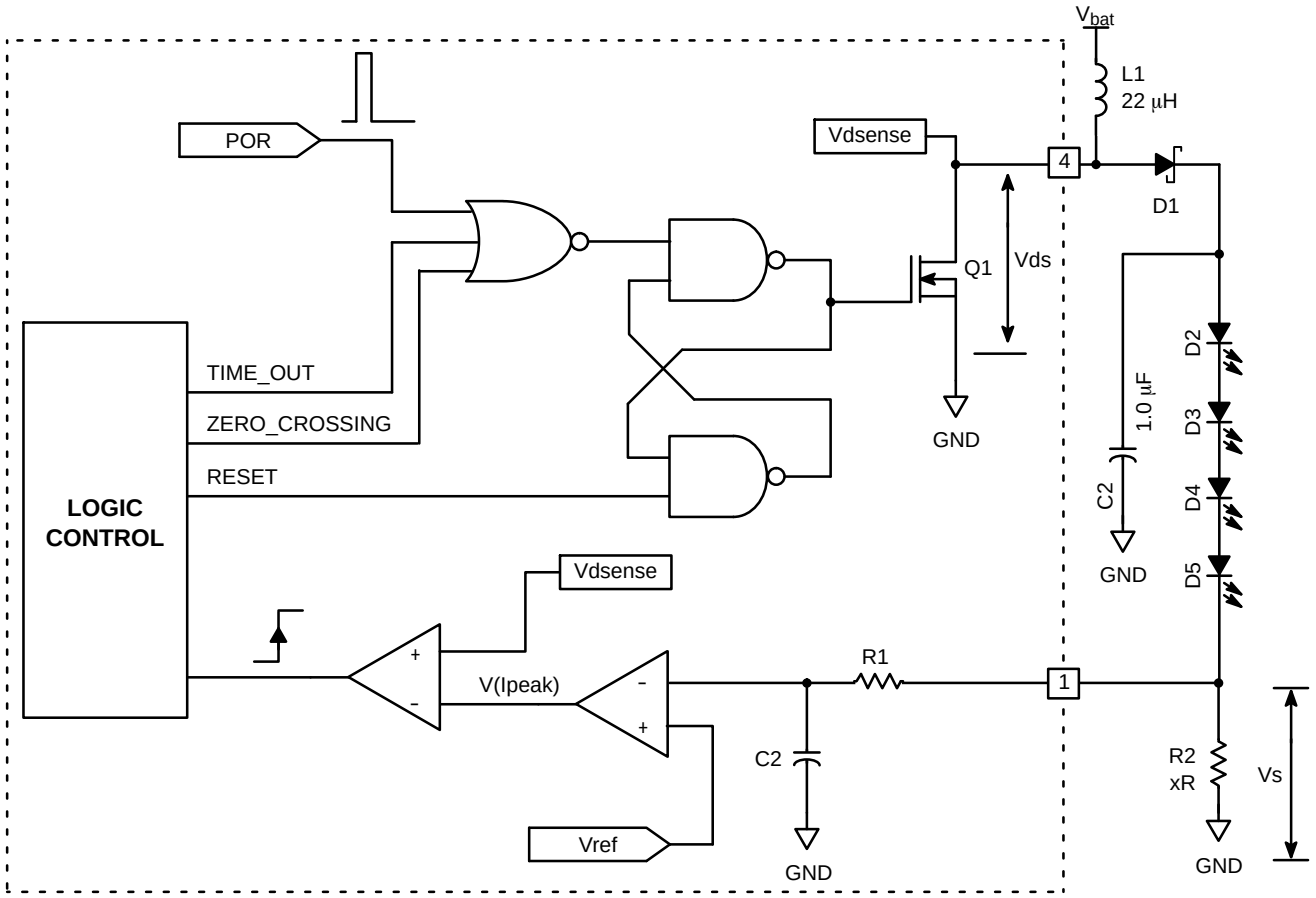


Figure 3. Basic DC−DC Converter Structure

Basically, the chip operates with two cycles:

Cycle #1 : time t1, the energy is stored into the inductor

Cycle #2 : time t2, the energy is dumped to the load

The POR signal sets the flip−flop and the first cycle takes place. When the current hits the peak value, defined by the error amplifier associated with the loop regulation, the flip−flop resets, the NMOS is deactivated and the current is dumped into the load. Since the timing is application dependent, the internal timer limits the Toff cycle to 320 ns (typical), making sure the system operates in a continuous mode to maximize the energy transfer.

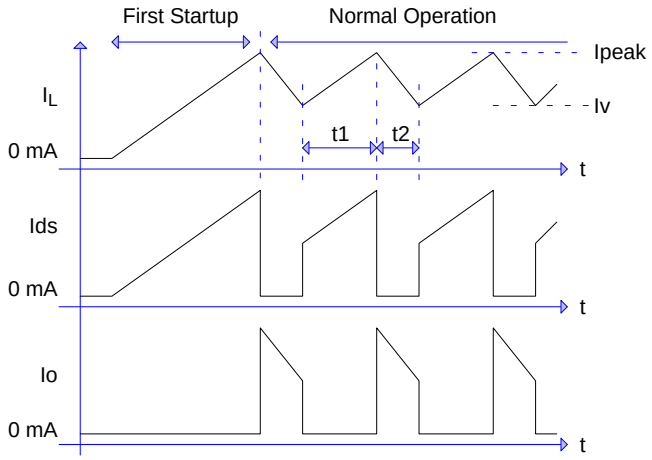


Figure 4. Basic DC−DC Operation

Based on the data sheet, the current flowing into the inductor is bounded by two limits:

- Ipeak Value: Internally fixed to 350 mA typical
- Iv Value: Limited by the fixed Toff time built in the chip (320 ns typical)

The system operates in a continuous mode as depicted in Figure 4 and t_1 & t_2 times can be derived from basic equations. (Note: The equations are for theoretical analysis only, they do not include the losses.)

$$E = L * \frac{di}{dt} \quad \text{(eq. 1)}$$

Let $E = V_{bat}$, then:

$$t1 = \frac{(Ip - Iv) * L}{Vbat} \quad \text{(eq. 2)}$$

$$t2 = \frac{(Ip - Iv) * L}{Vo - Vbat} \quad \text{(eq. 3)}$$

Since t_2 = 320 ns typical and Vo = 22 V maximum, then (assuming a typical V_{bat} = 3.0 V):

$$\Delta I = \frac{t2 * (Vo - Vbat)}{L} \quad \text{(eq. 4)}$$

$$\Delta Imax = \frac{320e-9 * (22 - 3.0)}{22e-6} = 276 \text{ mA}$$

Of course, from a practical stand point, the inductor must be sized to cope with the peak current present in the circuit to avoid saturation of the core. On top of that, the ferrite material shall be capable to operate at high frequency (1.0 MHz) to minimize the Foucault's losses developed during the cycles.

The operating frequency can be derived from the electrical parameters. Let $V = Vo - V_{bat}$, rearranging Equation 1:

$$ton = \frac{dI * L}{E} \quad \text{(eq. 5)}$$

Since toff is nearly constant (according to the 320 ns typical time), the dI is constant for a given load and inductance value. Rearranging Equation 5 yields:

$$ton = \frac{\frac{V*dt}{L} * L}{E} \quad \text{(eq. 6)}$$

Let $E = V_{bat}$, and Vopk = output peak voltage, then:

$$ton = \frac{(Vopk - Vbat) * dt}{Vbat} \quad \text{(eq. 7)}$$

Finally, the operating frequency is:

$$F = \frac{1}{ton + toff} \quad \text{(eq. 8)}$$

The output power supplied by the NCP5007 is limited to one watt: Figure 5 shows the maximum power that can be delivered by the chip as a function of the input voltage.

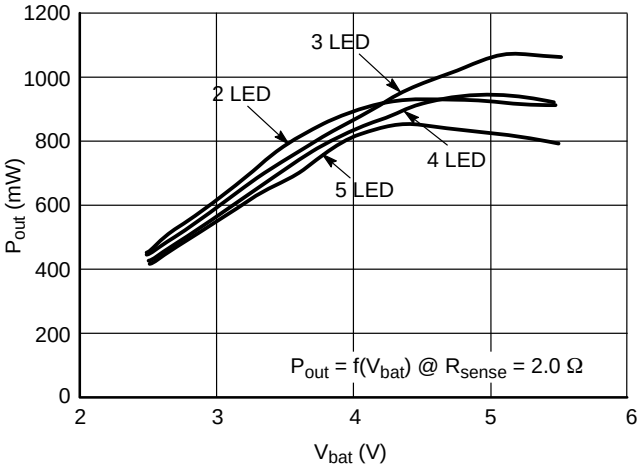
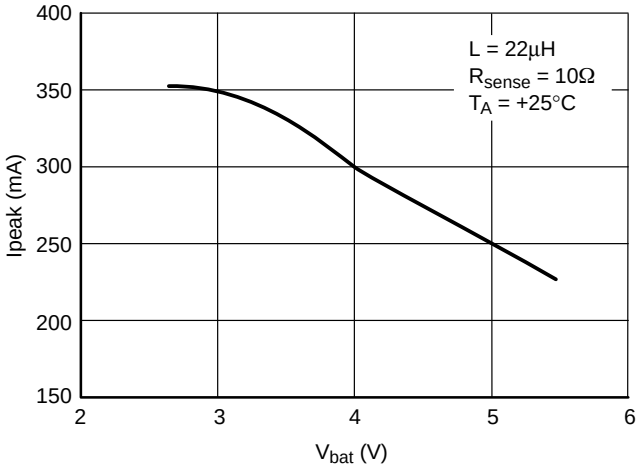
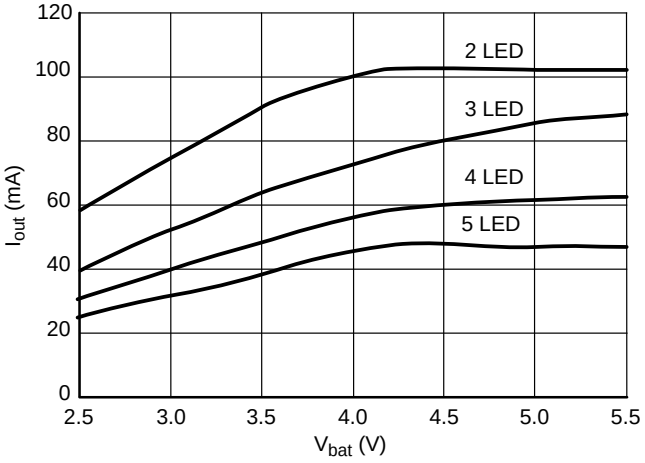


Figure 5. Maximum Output Power as a Function of the Battery Supply Voltage



Test conditions: 5 LEDs in series, steady state operation

Figure 6. Typical Inductor Peak Current as a Function of V_{bat} Voltage



Test conditions: L = 22 μH, Rsense = 2.0 Ω, Tamb = +25°C

Figure 7. Maximum Output Current as a Function of V_{bat}

Output Current Range Set−Up

The current regulation is achieved by means of an external sense resistor connected in series with the LED string.

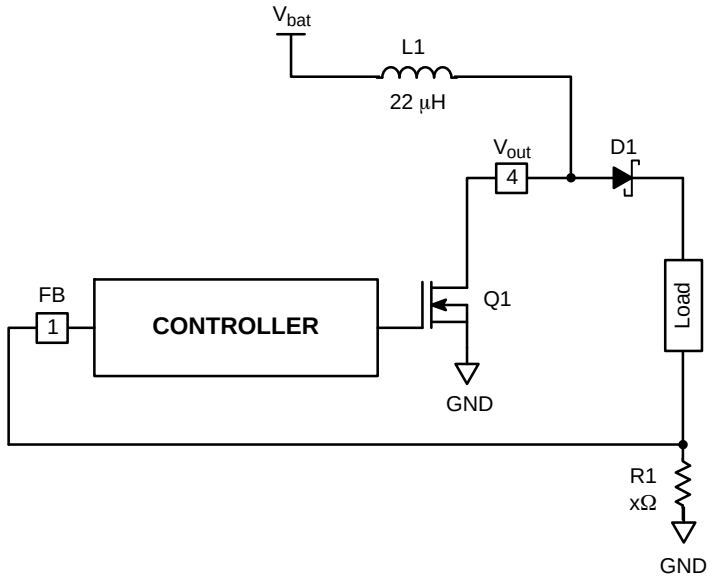


Figure 8. Output Current Feedback

The current flowing through the LED creates a voltage drop across the sense resistor R1. The voltage drop is constantly monitored internally, and maximum peak current allowed in the inductor is set accordingly in order to keep constant this voltage drop (and thus the current flowing through the LED). For example, should one need a 10 mA output current, the sense resistor should be sized according to the following equation:

$$R_1 = \frac{\text{Feedback Threshold}}{I_{out}} = \frac{200\ \text{mV}}{10\ \text{mA}} = 20\ \Omega \quad \text{(eq. 9)}$$

A standard 5% tolerance resistor, 22 Ω SMD device, yields 9.09 mA, good enough to fulfill the back light demand. The typical application schematic diagram is provided in Figure 9.

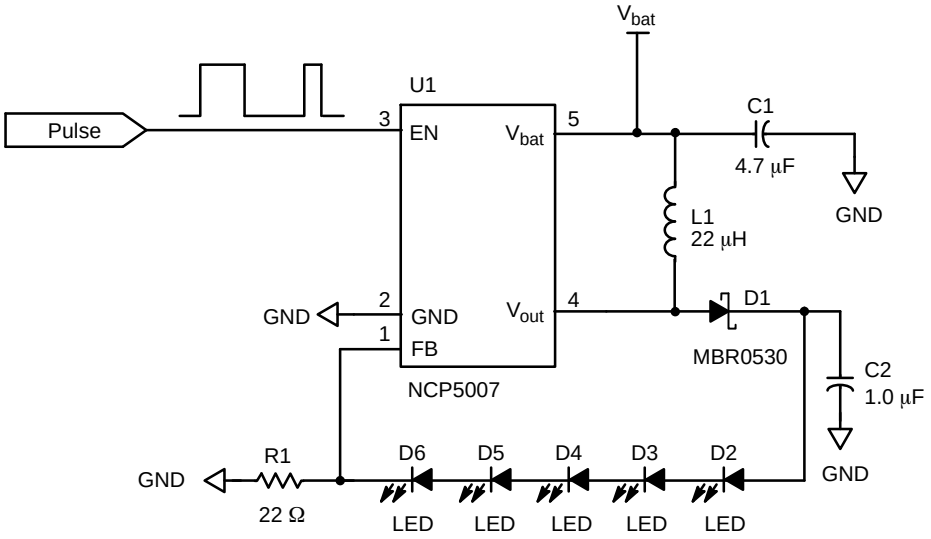


Figure 9. Basic Schematic Diagram

Output Load Drive

In order to take advantage of the built−in Boost capabilities, one shall operate the NCP5007 in the continuous output current mode. Such a mode is achieved by using and external reservoir capacitor (see Table 1) across the LED.

At this point, the peak current flowing into the LED diodes shall be within the maximum ratings specified for these devices. Of course, pulsed operation can be achieved, thanks to the EN signal pin 3, to force high current into the LED when necessary.

The Schottky diode D1, associated with capacitor C2 (see Figure 9), provides a rectification and filtering function.

When a pulse−operating mode is required:

- A PWM mode control can be used to adjust the output current range by means of a resistor and a capacitor connected across FB pin. On the other hand, the Schottky diode can be removed and replaced by at least one LED diode, keeping in mind such LED shall sustain the large pulsed peak current during the operation.

TYPICAL OPERATING CHARACTERISTICS

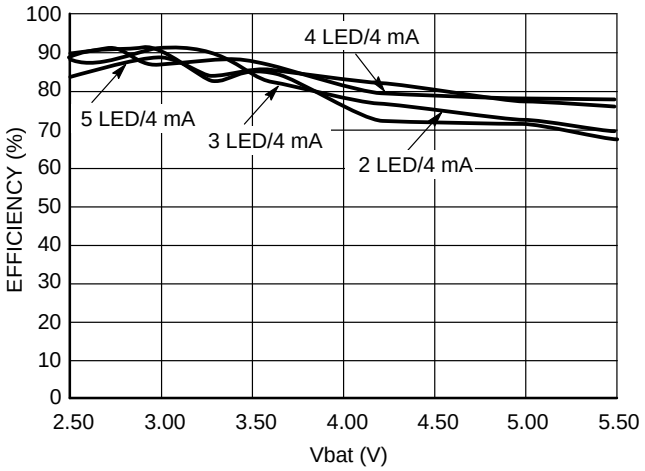


Figure 10. Overall Efficiency vs. Power Supply − I_{out} = 4.0 mA, L = 22 μH

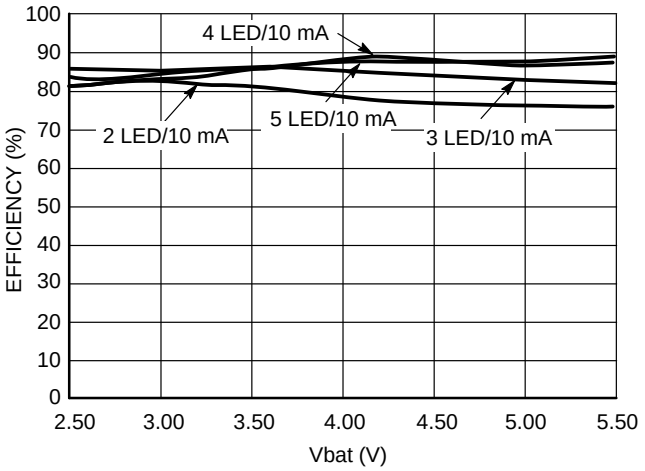


Figure 11. Overall Efficiency vs. Power Supply − I_{out} = 10 mA, L = 22 μH

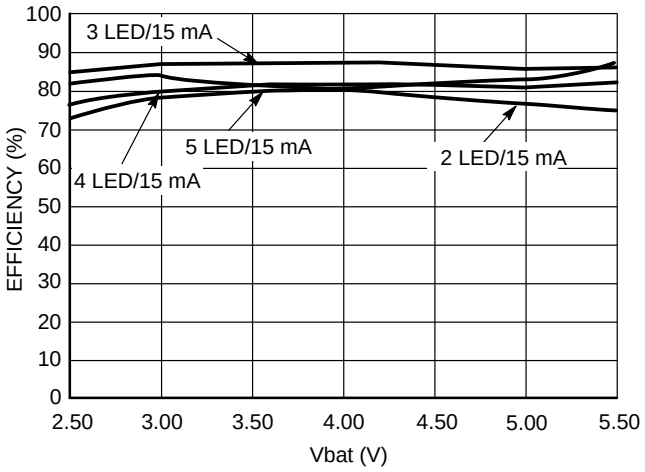


Figure 12. Overall Efficiency vs. Power Supply − I_{out} = 15 mA, L = 22 μH

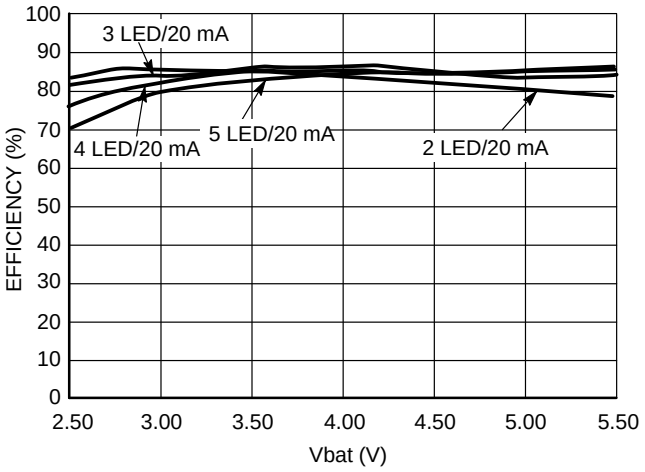


Figure 13. Overall Efficiency vs. Power Supply − I_{out} = 20 mA, L = 22 μH

TYPICAL OPERATING CHARACTERISTICS

(All curve conditions: L = 22 μH, Cin = 4.7 μF, C_{out} = 1.0 μF, Typical curve @ T_a = +25°C)

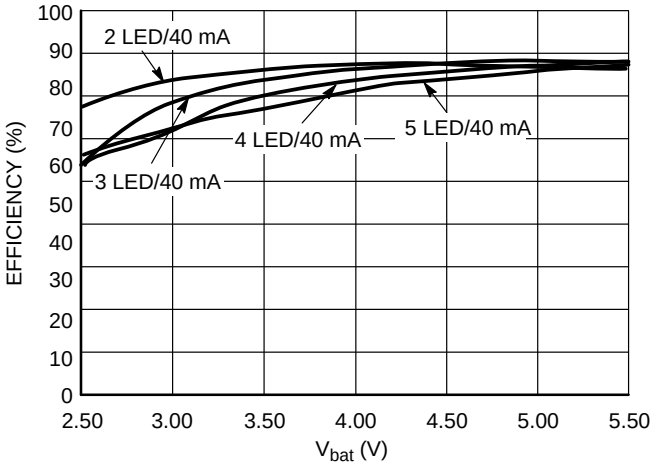


Figure 14. Overall Efficiency vs. Power Supply − I_{out} = 40 mA, L = 22 μH

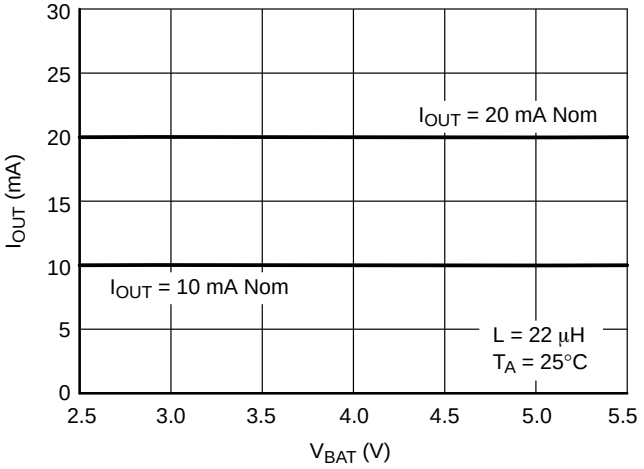


Figure 15. Current Variation vs. Power Supply with 3 Series LED's

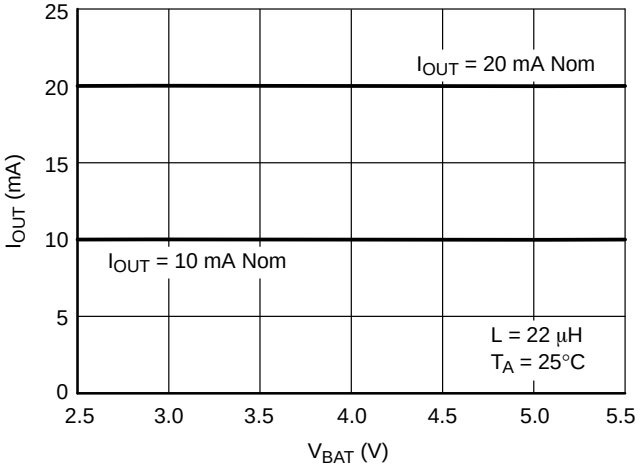


Figure 16. Current Variation vs. Power Supply with 4 Series LED's

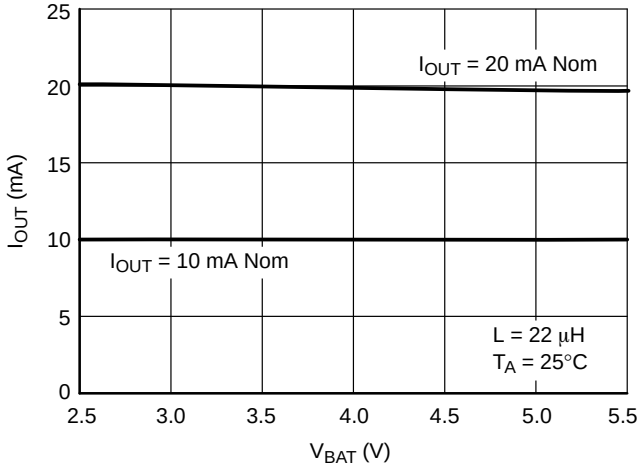


Figure 17. Current Variation vs. Power Supply with 5 Series LED's

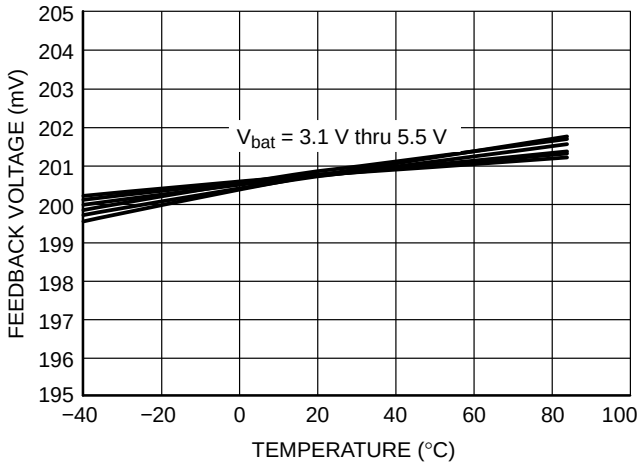


Figure 18. Feedback Voltage Stability

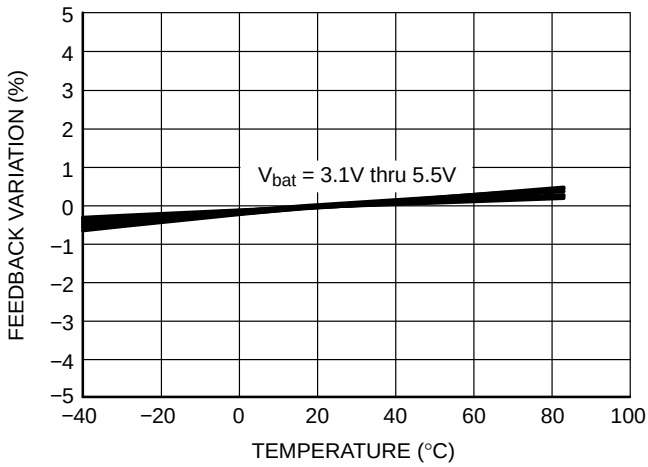


Figure 19. Feedback Voltage Variation

TYPICAL OPERATING CHARACTERISTICS

(All curve conditions: L = 22 μH, Cin = 4.7 μF, C_{out} = 1.0 μF, Typical curve @ T_a = +25°C)

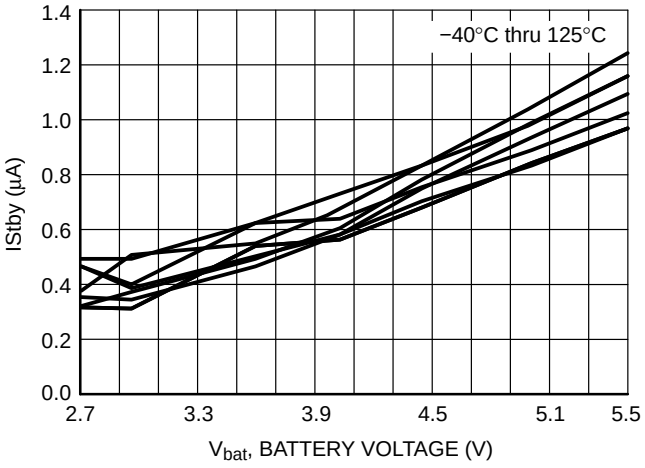


Figure 20. Standby Current

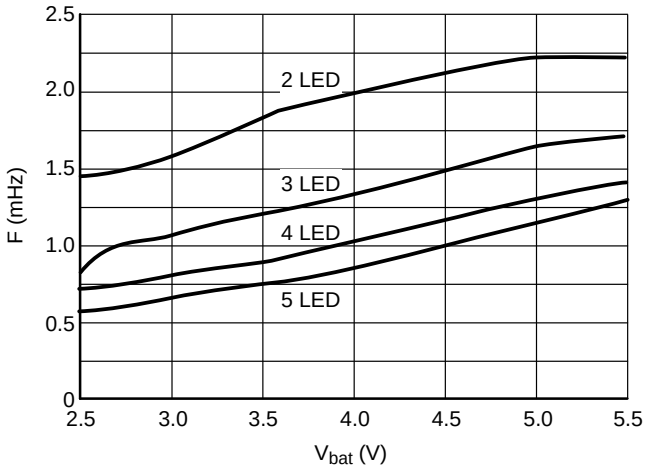


Figure 21. Typical Operating Frequency

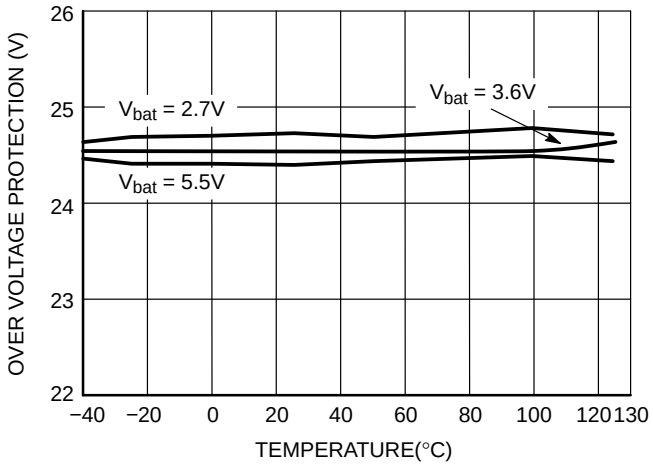
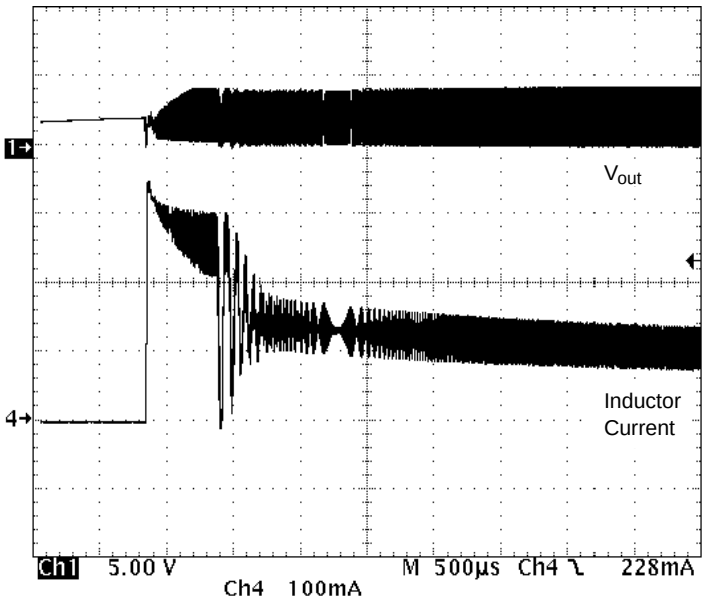


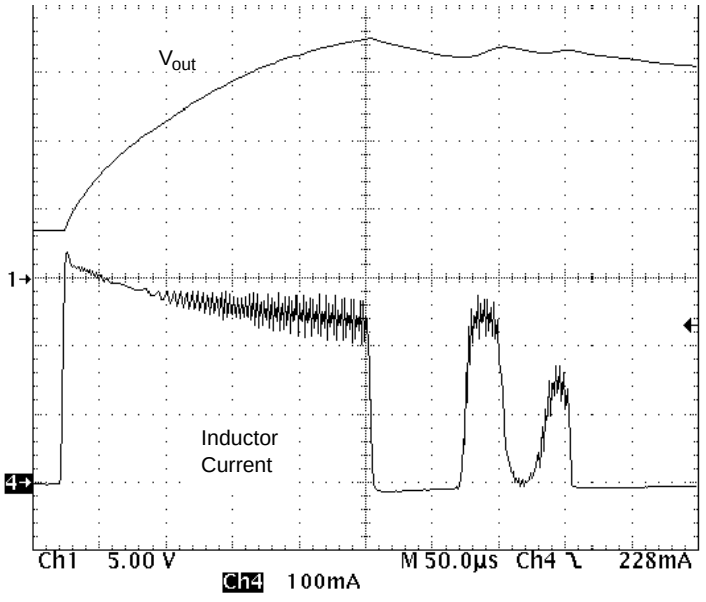
Figure 22. Overvoltage Protection

TYPICAL OPERATING WAVEFORMS



Conditions: V_{bat} = 3.6 V, L_{out} = 22 µH, 5 LED, I_{out} = 15 mA

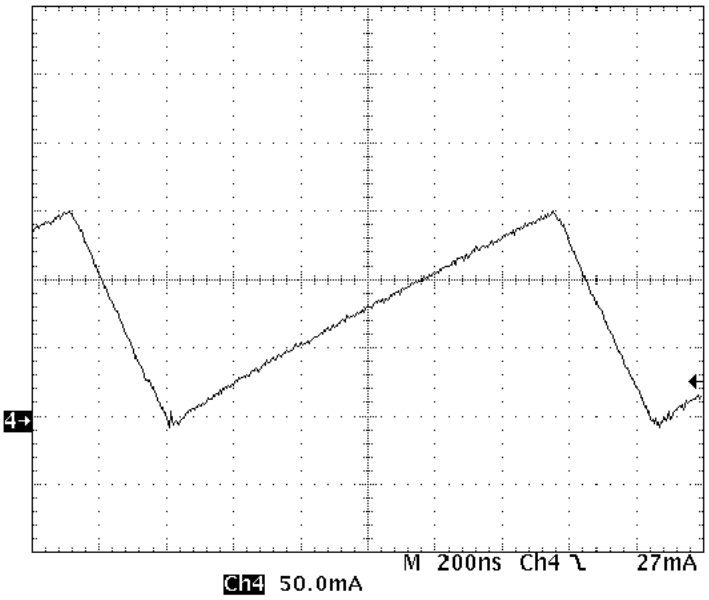
Figure 23. Typical Power Up Response



Conditions: V_{bat} = 3.6 V, L_{out} = 22 µH, 5 LED, I_{out} = 15 mA

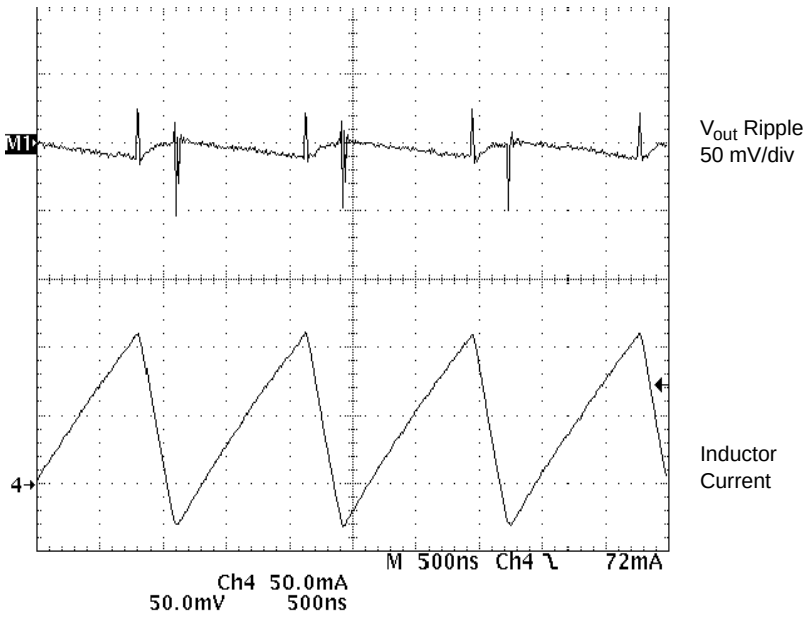
Figure 24. Typical Startup Inductor Current and Output Voltage

TYPICAL OPERATING WAVEFORMS



Conditions: V_{bat} = 3.6 V, L_{out} = 22 μH, 5 LED, I_{out} = 15 mA

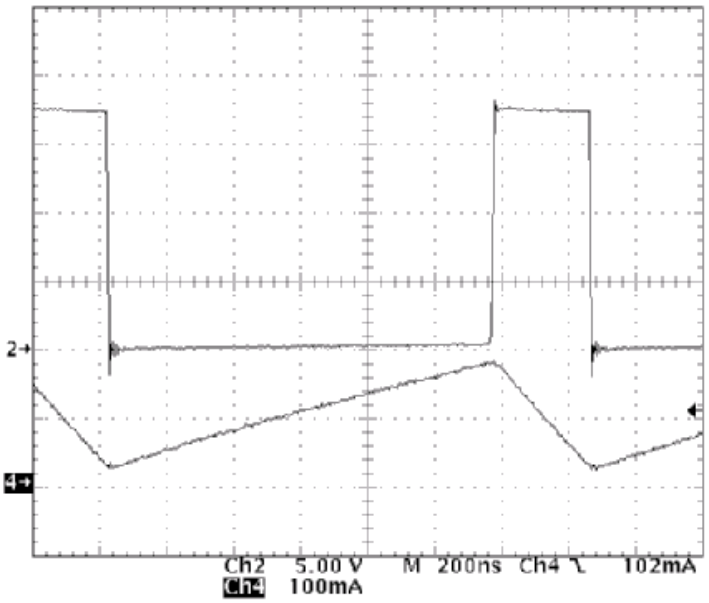
Figure 25. Typical Inductor Current



Conditions: V_{bat} = 3.6 V, L_{out} = 22 μH, 5 LED, I_{out} = 15 mA

Figure 26. Typical Output Voltage Ripple

TYPICAL OPERATING WAVEFORMS



Test Conditions: L = 22 μH, I_{out} = 15 mA, V_{bat} = 3.6 V, Ambient Temperature, LED = 5

Figure 27. Typical Output Peak Voltage

TYPICAL APPLICATIONS CIRCUITS

Standard Feedback

The standard feedback provides constant current to the LEDs, independently of the V_{bat} supply and number of LEDs in series. Figure 28 depicts a typical application to supply 13 mA to the load.

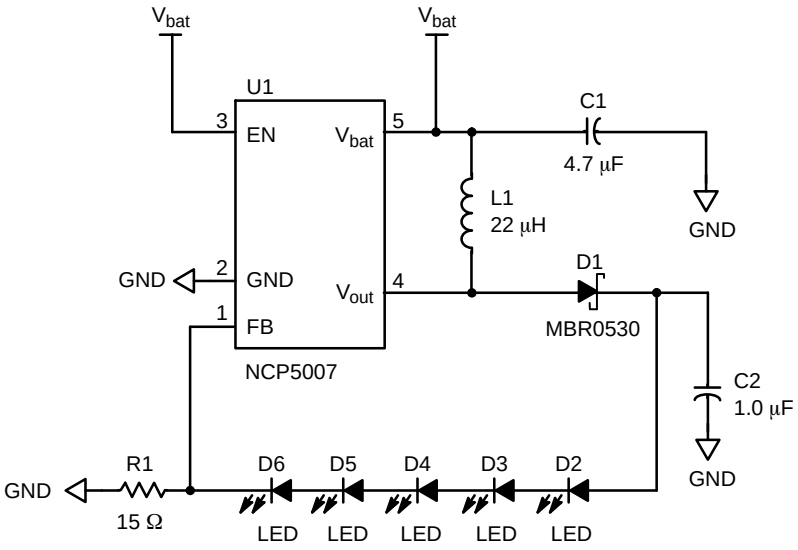


Figure 28. Basic DC Current Mode Operation with Analog Feedback

PWM Operation

The analog feedback pin 1 provides a way to dim the LED by means of an external PWM signal as depicted in Figure 29. Taking advantage of the high internal impedance presented by the FB pin, one can set up a simple R/C network to accommodate such a dimming function. Two modes of operation can be considered:

- Pulsed mode, with no filtering
- Averaged mode with filtering capacitor

Although the pulsed mode will provide a good dimming function, it will yield high switching transients which are difficult to filter out in the control loop. As such this first approach is not recommended. The output current depends upon the duty cycle of the signal presented to the node pin 1: this is very similar to the digital control shown in Figure 30.

The average mode yields a noise−free operation since the converter operates continuously, together with a very good dimming function. The cost is an extra resistor and one extra capacitor, both being low cost parts.

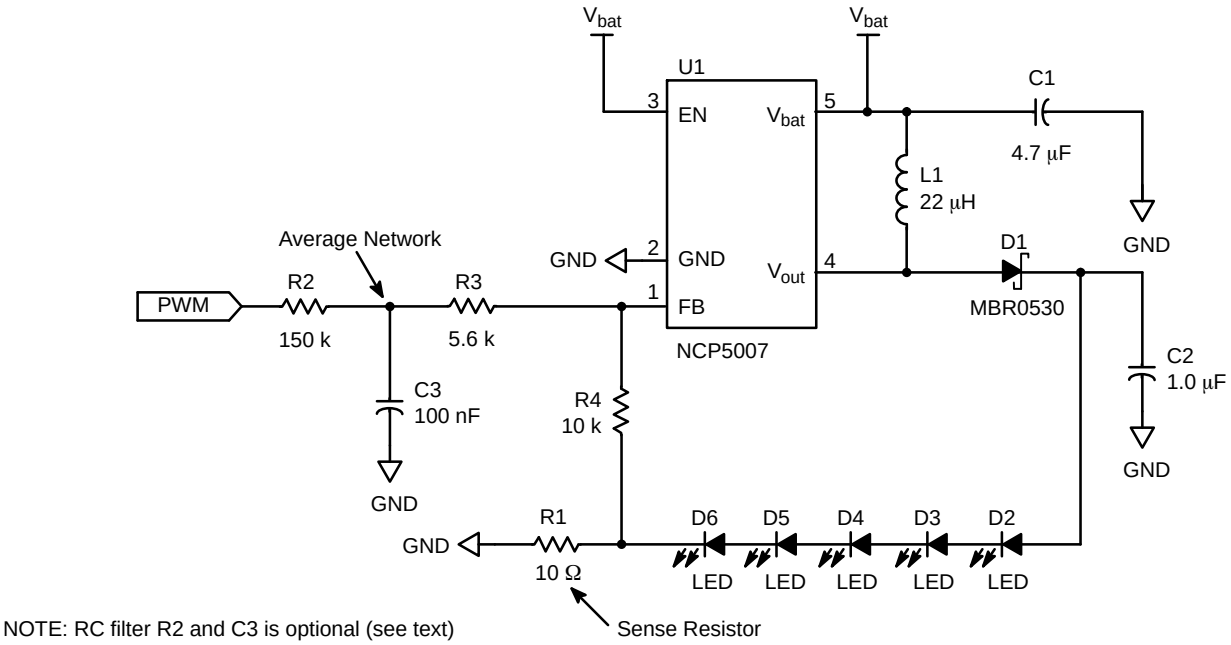


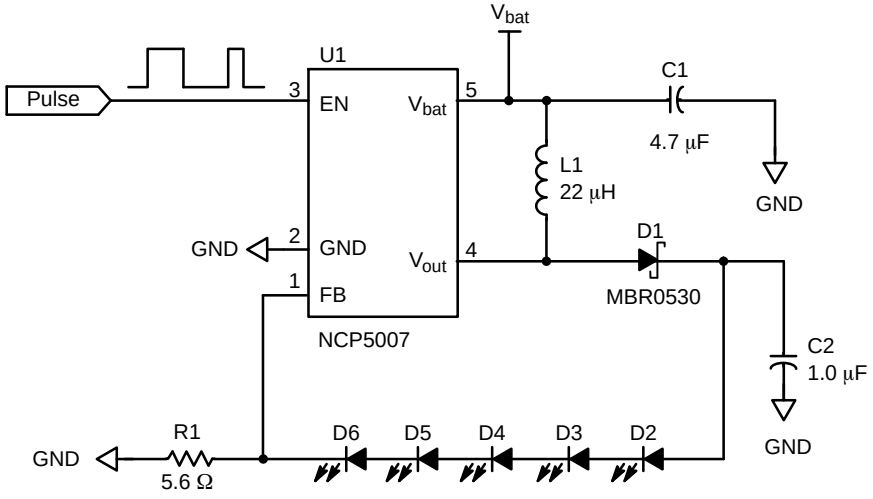
Figure 29. Basic DC Current Mode Operation with PWM Control

To implement such a function, lets consider the feedback input as an operational amplifier with a high impedance input (reference schematic Figure 29). The analog loop will keep going to balance the current flowing through the sense resistor R1 until the feedback voltage is 200 mV. An extra resistor (R4) isolates the FB node from low resistance to ground, making possible to add an external voltage to this pin.

The time constant R2/C3 generates the voltage across C3, added to the node pin 1, while R2/R3/R4/R1/C3 create the discharge time constant. In order to minimize the pick up noise at FB node, the resistors shall have relative medium value, preferably well below 1.0 MΩ. Consequently, let R2 = 150 k, R3 = 5.6 k and R4 = 10 k. In addition, the feedback delay to control the luminosity of the LED shall be acceptable by the user, 10 ms or less being a good compromise. The time constant can now be calculated based on a 400 mV offset voltage at the C3/R2/R3 node to force zero current to the LED. Assuming the PWM signal comes from a standard gate powered by a 3.0 V supply, running at 5.0 kHz, then full dimming of the LED can be achieved with a 95% span of the Duty Cycle signal.

Digital Control

An alternative method of controlling the luminosity of the LEDs is to apply a PWM signal to the EN pin (see Figure 30). The output current depends upon the Duty Cycle, but care must be observed as the DC−DC converter is continuously pulsed ON/OFF and noise is likely to be generated.



NOTE: Pulse width and frequency depends upon the application constraints.

Figure 30. Typical Semi−Pulsed Mode of Operation

Typical LEDs Load Mapping

Since the output power is battery limited (see Figure 5), one can arrange the LEDs in a variety of different configurations. Powering ten LEDs can be achieved by a series/parallel combination as depicted in Figure 31.

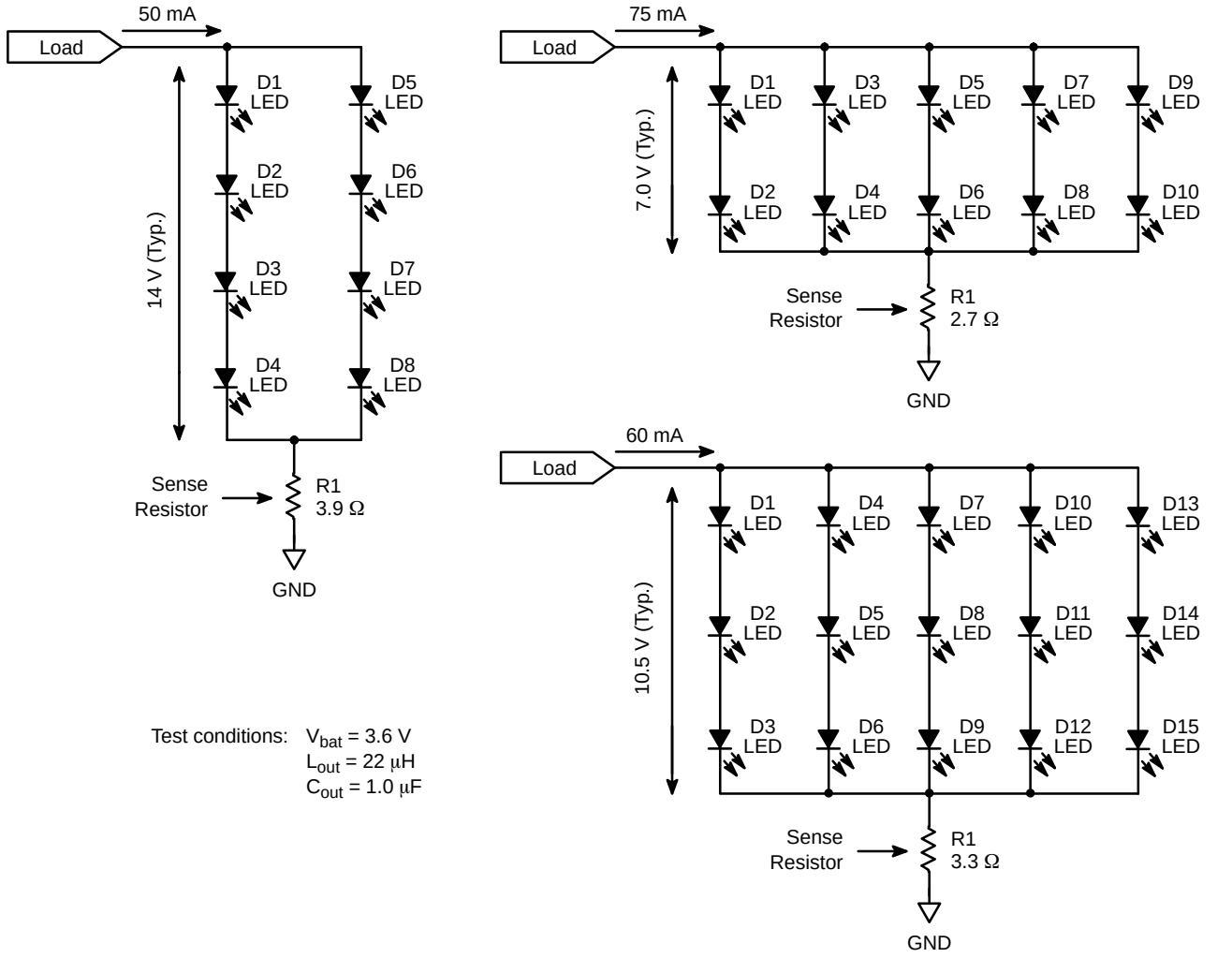


Figure 31. Examples of Possible LED Arrangements

ON Semiconductor provides a demo board to evaluate the performance of the NCP5007. The schematic for that demo board is illustrated in Figure 32.

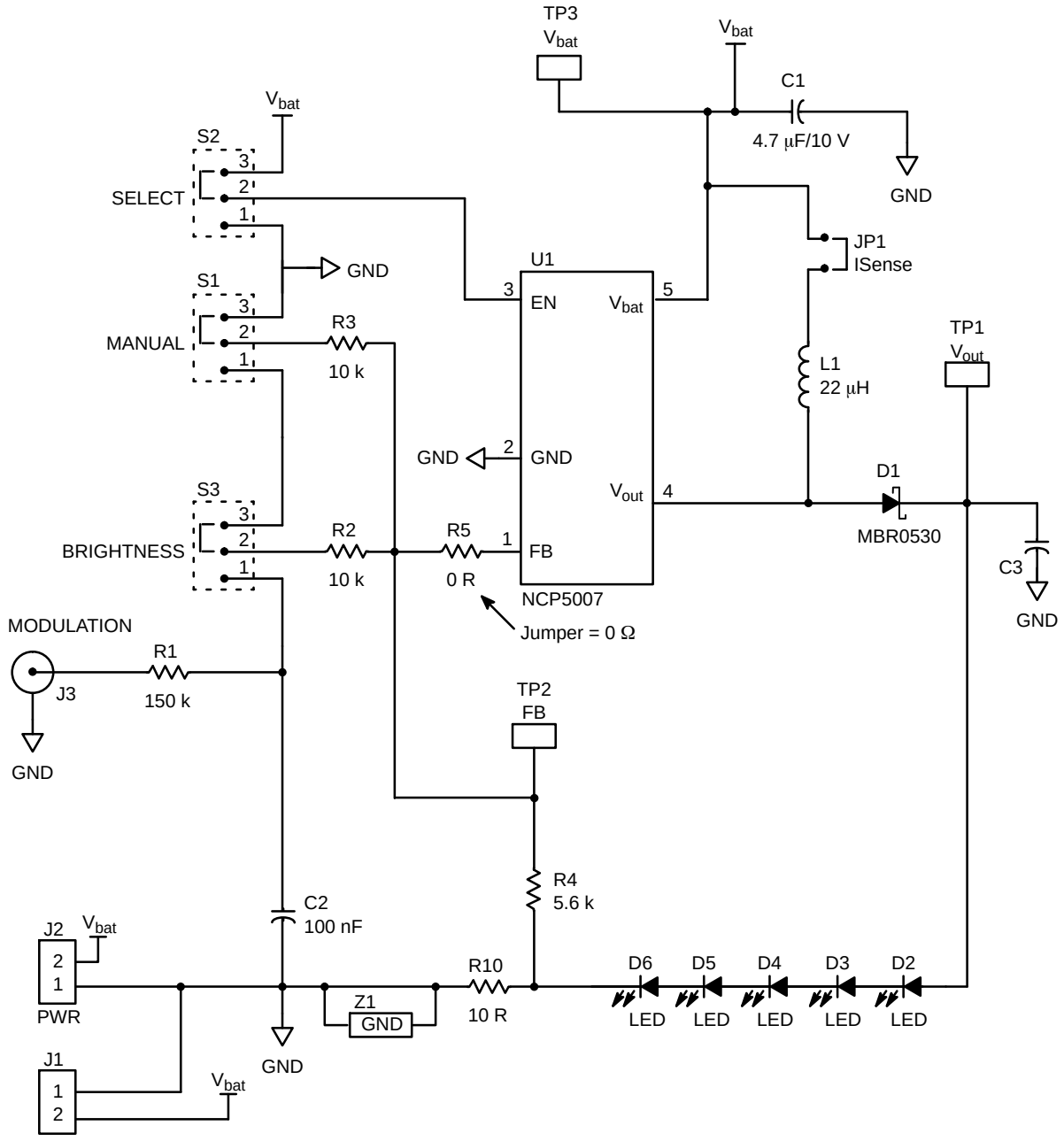


Figure 32. NCP5007 Demo Board Schematic Diagram

Table 1. Recommended External Parts

Part	Manufacturer	Description	Part Number
30 V Low Vf Schottky Diode	ON Semiconductor	SOD−123 (1.6 x 3.2 mm)	MBR0530T1
20 V Low Vf Schottky Diode	ON Semiconductor	SOD−323 (1.25 x 2.5 mm)	NSR0320MW2T1
20 V Low Vf Schottky Diode	ON Semiconductor	SOD−563 (1.6 x 1.6 mm)	NSR0320XV6T1
Ceramic Cap. 1.0 μF/16 V	MURATA	GRM42−X7R	GRM42−6X7R−105K16
Ceramic Cap. 4.7 μF/6.3 V	MURATA	GRM40−X5R	GRM40−X5R−475K6.3
Inductor 22 μH	CoilCraft	1008PS−Shielded	1008PS−223MC
Inductor 22 μH	CoilCraft	Power Wafer	LPQ4812−223KXC

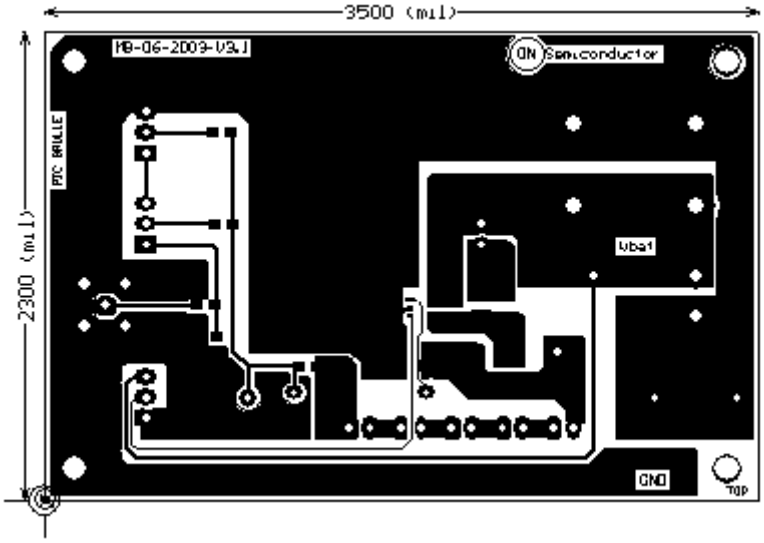


Figure 33. NCP5007 Demo Board PCB: Top Layer

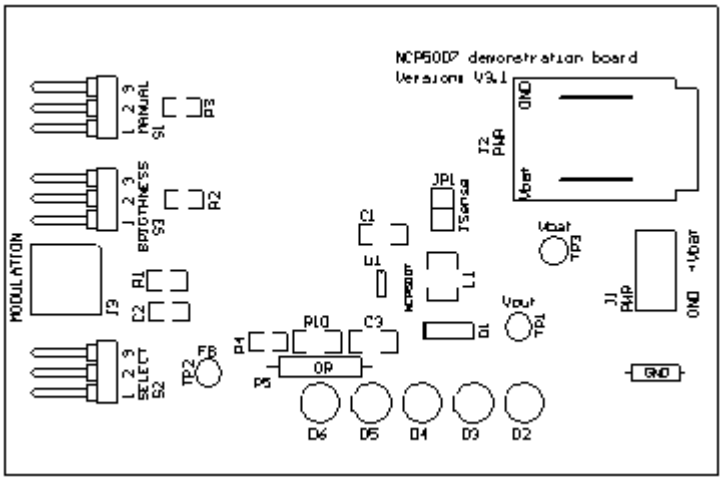


Figure 34. NCP5007 Demo Board Top Silkscreen

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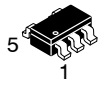
Note 1: This device series contains ESD protection and exceeds the following tests 4
Note 2: The maximum package power dissipation limit must not be exceeded 4
Note 3: Latchup current maximum rating: ±100 mA per JEDEC standard: JESD78 4
Note 4: Moisture Sensivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A 4
Note 5: The overall tolerance depends upon the accuracy of the external resistor 5

ABBREVIATIONS

EN Enable
FB Feed Back
POR Power On Reset: Internal pulse to reset the chip when the power supply is applied

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

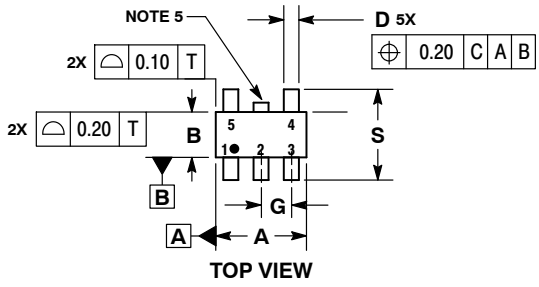
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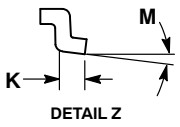
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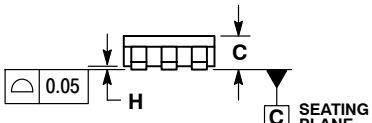
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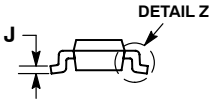
TOP VIEW



DETAIL Z



SIDE VIEW

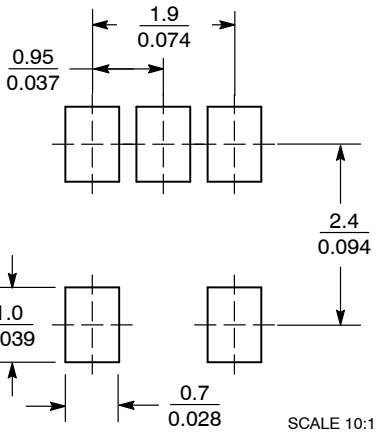


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

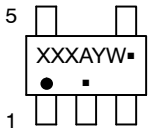
SOLDERING FOOTPRINT*



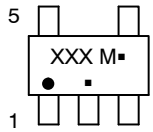
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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