High and Low Side Gate Driver, High Performance, 700 V, with 3.5 A Source and 3 A Sink Currents

NCP51530

NCP51530 is a 700 V high side and low side driver with 3.5 A source & 3 A sink current drive capability for AC−DC power supplies and inverters. NCP51530 offers best in class propagation delay, low quiescent current and low switching current at high frequencies of operation. This device is tailored for highly efficient power supplies operating at high frequencies. NCP51530 is offered in two versions, NCP51530A/B. NCP51530A has a typical 60 ns propagation delay, while NCP51530B has a typical propagation delay of 25 ns. NCP51530 comes in SOIC8 and DFN10 packages.

Features

- High voltage range: Up to 700 V
- NCP51530A: Typical 60 ns Propagation Delay
- NCP51530B: Typical 25 ns Propagation Delay
- Low Quiescent and Operating Currents
- 15 ns Max Rise and Fall Time
- 3.5 A Source / 3 A Sink Currents
- Under−voltage Lockout for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- High dv/dt Immunity up to 50 V/ns
- Pin to Pin Compatible with Industry Standard Half−bridge ICs.
- Matched Propagation Delay (7 ns Max)
- High Negative Transient Immunity on Bridge Pin
- DFN10 Package Offers Both Improved Creepage and Exposed Pad

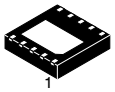
Applications

- High−density SMPS for Servers, Telecom and Industrial
- Half/Full−bridge & LLC Converters
- Active Clamp Flyback/Forward Converters
- Solar Inverters & Motor Controls
- Electric Power Steering



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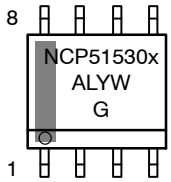
SOIC−8
D SUFFIX
CASE 751−07



1

DFN10
MN SUFFIX
CASE 506DJ

MARKING DIAGRAMS

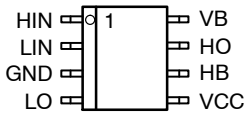




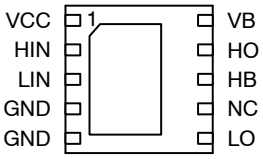
NCP51530 = Specific Device Code
x = A or B version
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT INFORMATION



8 Pin Package
(Top View)

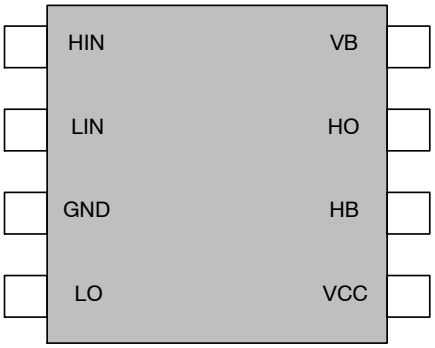


10 Pin DFN Package
(Top View)

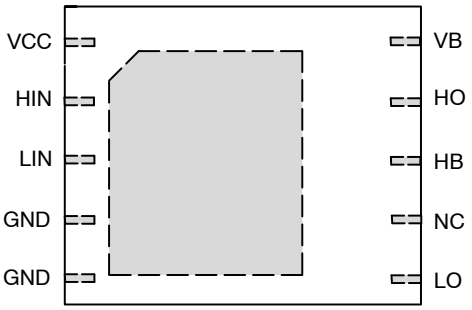
ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

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SOIC8
(Top View)



DFN10
(Top View)

Table 1. PIN DESCRIPTION SOIC 8 PACKAGE

Pin Out	Name	Function
1	HIN	High side input
2	LIN	Low side input
3	GND	Ground reference
4	LO	Low side output
5	VCC	Low side and logic supply
6	HB	High side supply return
7	HO	High side output
8	VB	High side voltage supply

Table 2. PIN DESCRIPTION DFN10 PACKAGE

Pin Out	Name	Function
1	VCC	Low side and logic supply
2	HIN	High side input
3	LIN	Low side input
4	GND	Ground reference
5	GND	Ground reference
6	LO	Low side output
7	NC	No Connect
8	HB	High side supply return
9	HO	High side output
10	VB	High side voltage supply

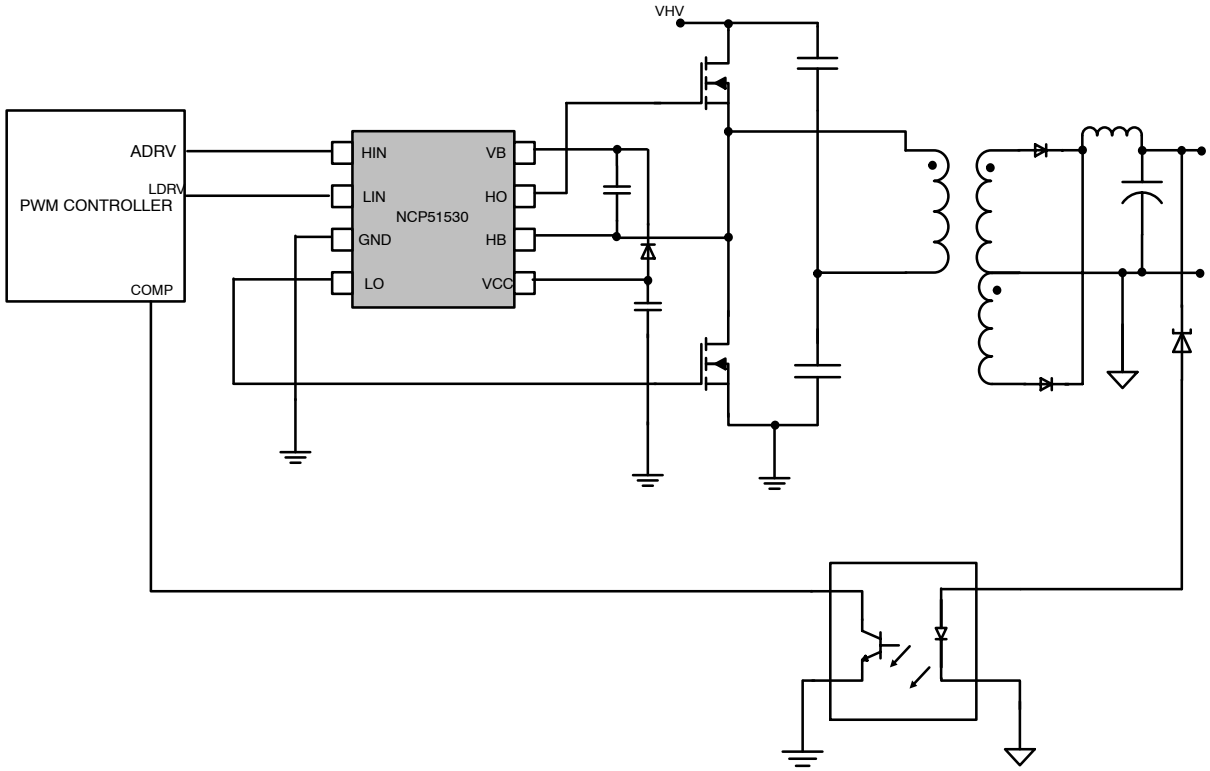


Figure 1. Simplified Applications Schematic for a Half−Bridge Converter (SOIC8)

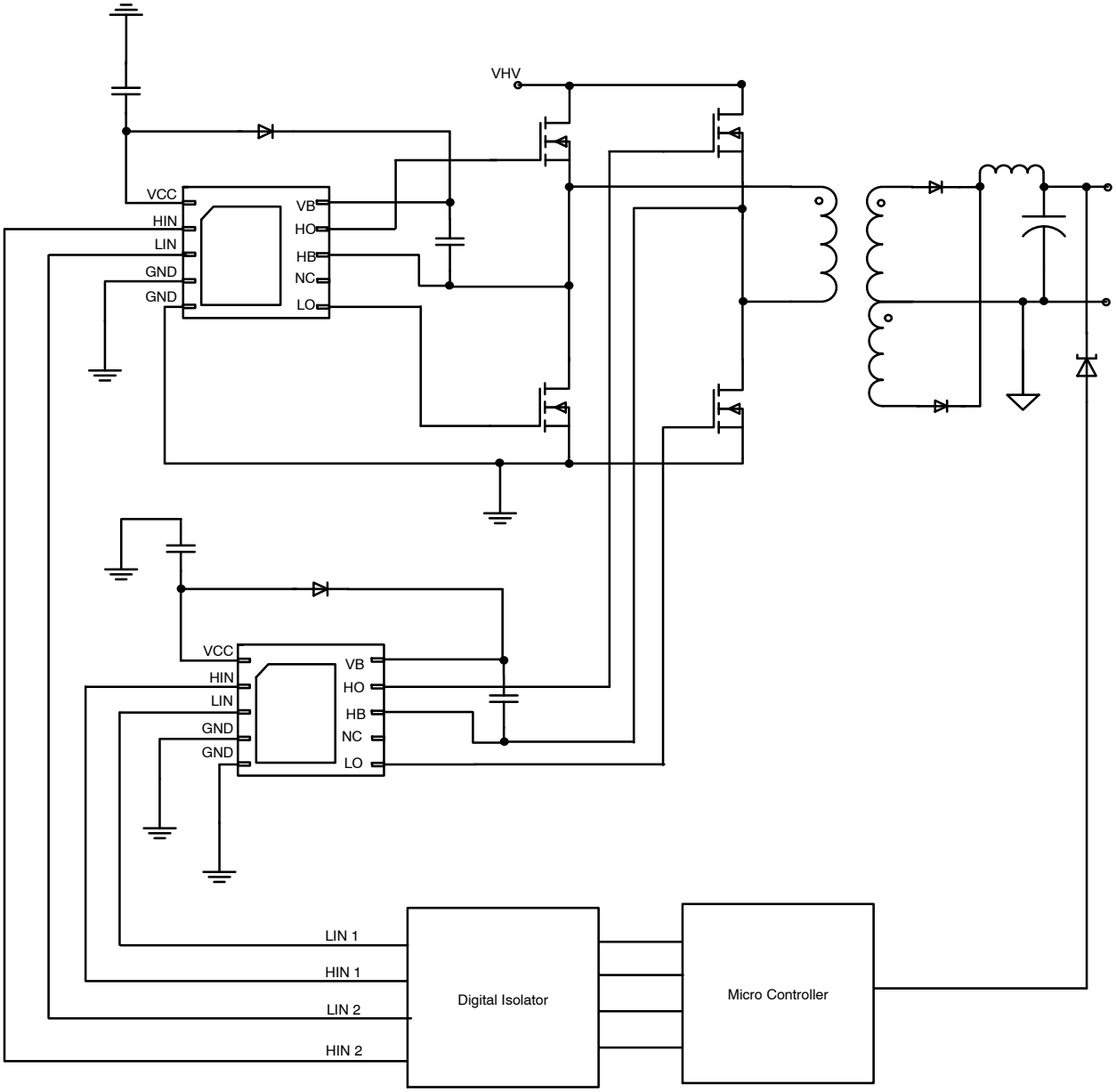


Figure 2. Simplified Applications Schematic for a Full Bridge Converter (DFN 10)

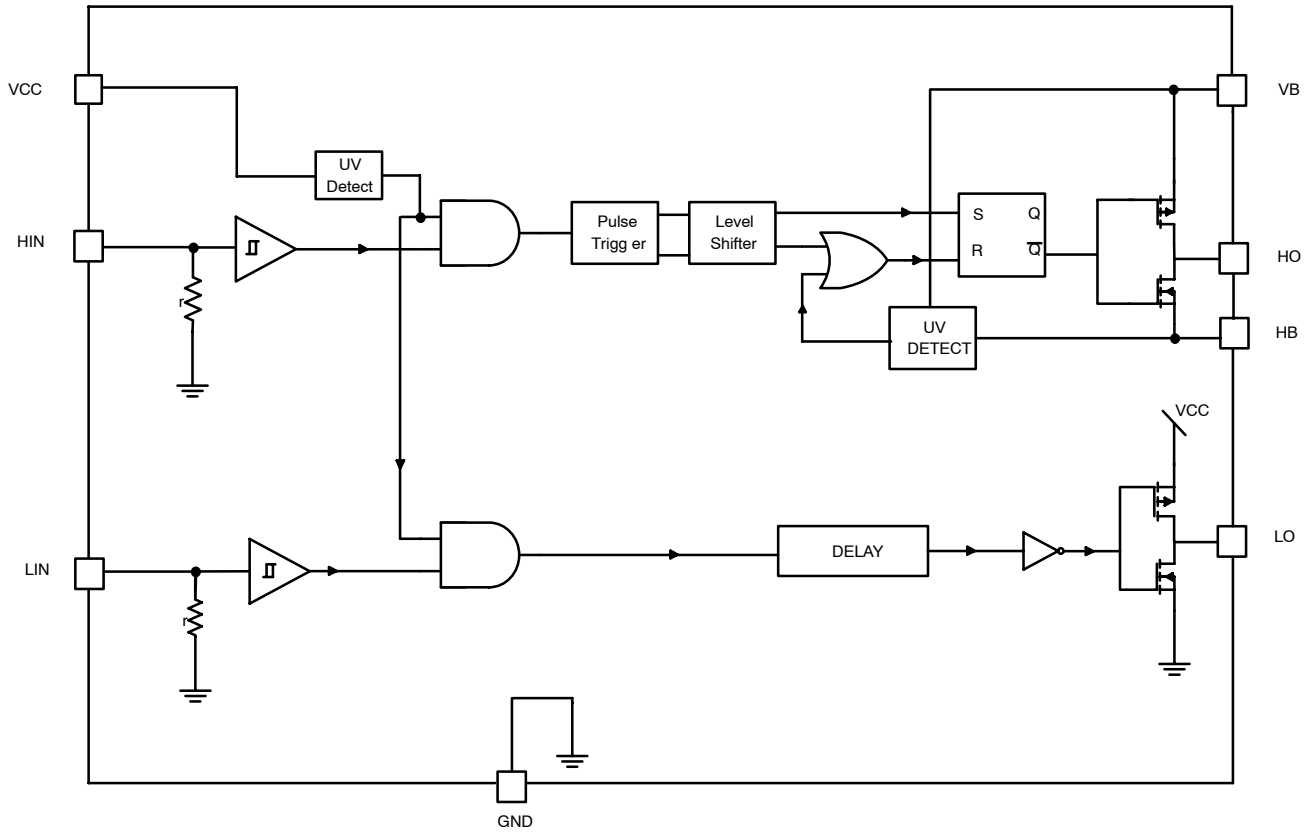


Figure 3. Internal Block Diagram for NCP51530

Table 3. ABSOLUTE MAXIMUM RATINGS All voltages are referenced to GND pin.

Rating	Symbol	Value	Unit
Input voltage range	V_{CC}	−0.3 to 20	V
High side boot pin voltage	V_B	−0.3 to 720	V
High side floating voltage	V_B−V_{HB}	−0.3 to 20	V
High side drive output voltage	V_{HO}	V_{HB} − 0.3 to V_B + 0.3	V
Low side drive output voltage	V_{LO}	−0.3 to V_{CC} + 0.3	V
Allowable hb slew rate	dV_{HB}/dt	50	V/ns
Drive input voltage	V_{LIN}, V_{HIN}	−5 to V_{CC} + 0.3	V
Junction temperature	$T_{J(MAX)}$	150°	C
Storage temperature range	T_{STG}	−55° to 150°	C
ESD Capability (Note 1) Human Body Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.		 4000 1000	V
Lead Temperature Soldering Reflow (SMD Styles ONLY), Pb−Free Versions (Note 2)		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series incorporates ESD protection and is tested by the following methods. ESD Human Body Model tested per AEC−Q100−002(EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−11(EIA/JESD22−C101E)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 4. THERMAL CHARACTERSTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC8 (Note 3) Thermal Resistance, Junction to Air	$R_{\theta JA}$	183	°C/W
Thermal Characteristics, DFN10 Thermal Resistance, Junction to Air (Note 4)	$R_{\theta JA}$	162	°C/W

3. Refer to ELECTRICAL CHARACTERSTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Values based on copper area of 50 mm^2 of 1 oz thickness and FR4 PCB substrate.

Table 5. RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage Range	V_{CC}	10	17	V
High Side Floating Voltage	V_B–V_{HB}	10	17	V
High Side Bridge pin Voltage	V_{HB}	–1	700	V
High Side Output Voltage	V_{HO}	V_{HB}	V_B	V
High Side Output Voltage	V_{LO}	GND	V_{CC}	V
Input Voltage on LIN and HIN pins	V_{LIN}, V_{HIN}	GND	V_{CC}–2	V
Operating Junction Temperature Range	T_J	–40	125	°C

Table 6. ELECTRICAL CHARACTERISTICS

(–40°C <T_J < 125°C, V_{CC} =V_B =12V, V_{HB} = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted, Typical values are at T_J = 25°C.)

Parameters	Test Conditions	Symbol	Min	Typ	Max	Unit
SUPPLY SECTION						
V_{CC} quiescent current	V_{LIN}=V_{HIN}=0	I_{CCQ}		0.15	0.25	mA
V_{CC} operating current	f = 500 kHz, C_{LOAD} = 0	I_{CCO}		0.7	1.0	mA
Boot voltage quiescent current	V_{LIN} = V_{HIN} = 0 V	I_{BQ}		0.1	0.15	mA
Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0	I_{BO}		0.7	1.0	mA
HB to GND quiescent current	V_{HS} = V_{HB} = 700 V	I_{HBQ}		6	11	μA
INPUT SECTION						
Input rising threshold		V_{HIT}	2.3	2.7	3.1	V
Input falling threshold		V_{LIT}	1	1.4	1.8	V
Input voltage Hysteresis		V_{IHYS}		1.3		V
Input pulldown resistance	V_{XIN}= 5 V	R_{IN}	100	175	250	kΩ
UNDER VOLTAGE LOCKOUT (UVLO)						
V_{CC} ON	V_{CC} Rising	V_{CCon}	8.6	9.1	9.6	V
V_{CC} hysteresis		V_{CChys}		0.5		V
V_B ON	V_B Rising	V_{Bon}	8	8.5	9	V
V_B hysteresis		V_{Bhyst}		0.5		V
High Side Startup Time	Time between V_B > UVLO & 1st HO Pulse	$T_{startup}$			10	μs
LO GATE DRIVER						
Low level output voltage	I_{LO} = 100 mA	V_{LOL}		0.125		V
High level output voltage	I_{LO} = –100 mA, V_{LOH} = V_{CC} –V_{LO}	V_{LOH}		0.150		V
Peak source current	V_{LO} = 0 V	$I_{LOpullup}$		3.5		A

Table 6. ELECTRICAL CHARACTERISTICS

(−40°C <T_J < 125°C, V_{CC} =V_B =12V, V_{HB} = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted, Typical values are at T_J = 25°C.)

Parameters	Test Conditions	Symbol	Min	Typ	Max	Unit
LO GATE DRIVER						
Peak sink current	V_{LO} = 12 V	$I_{LOpulldown}$		3.0		A
HO GATE DRIVER						
Low level output voltage	I_{HO} = 100 mA	V_{HOL}		0.125		V
High level output voltage	I_{HO} = −100 mA, V_{HOH} = V_{HB} −V_{HO}	V_{HOH}		0.150		V
Peak source current	V_{HO} = 0 V	$I_{HOpullup}$		3.5		A
Peak sink current	V_{HO} = 12 V	$I_{HOpulldown}$		3.0		A
OUTPUT RISE AND FALL TIME						
Rise Time LO, HO	C_{load} = 1000 pF	T_R		8	15	ns
Fall Time LO, HO	C_{load} = 1000 pF	T_F		8	15	ns
DELAY MATCHING						
LI ON, HI OFF	Pulse width = 1 μs	T_{MON}			7	ns
LI OFF, HI ON	Pulse width = 1 μs	T_{MOFF}			7	ns
TIMING						
Minimum Input Filter (NCP51530A)	V_{XIN} = 5 V , Input pulse width above which output change occurs.	T_{FT}	30	40		ns
PROPAGATION DELAY NCP51530A						
V_{LI} falling to V_{LO} falling	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DLFF}		60	100	ns
V_{HI} falling to V_{HO} falling	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DHFF}		60	100	ns
V_{LI} rising to V_{LO} rising	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DLRR}		60	100	ns
V_{HI} rising to V_{HO} rising	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DHRR}		60	100	ns
PROPAGATION DELAY NCP51530B						
V_{LI} falling to V_{LO} falling	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DLFF}		25	40	ns
V_{HI} falling to V_{HO} falling	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DHFF}		25	40	ns
V_{LI} rising to V_{LO} rising	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DLRR}		25	40	ns
V_{HI} rising to V_{HO} rising	C_{load} = 0, Minimum On/Off−time to register as a valid change = 50 ns	T_{DHRR}		25	40	ns

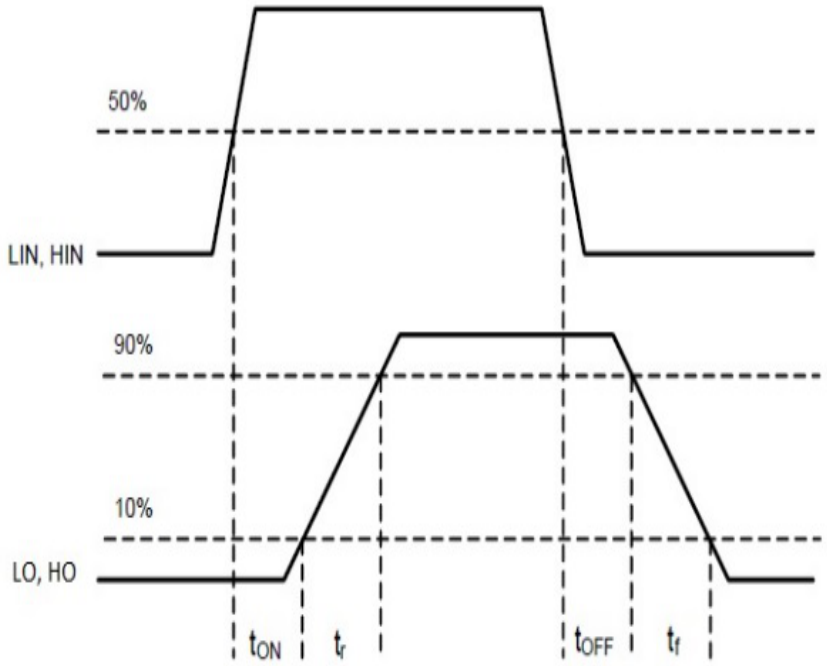


Figure 4. Propagation Delay, Rise and Fall Times

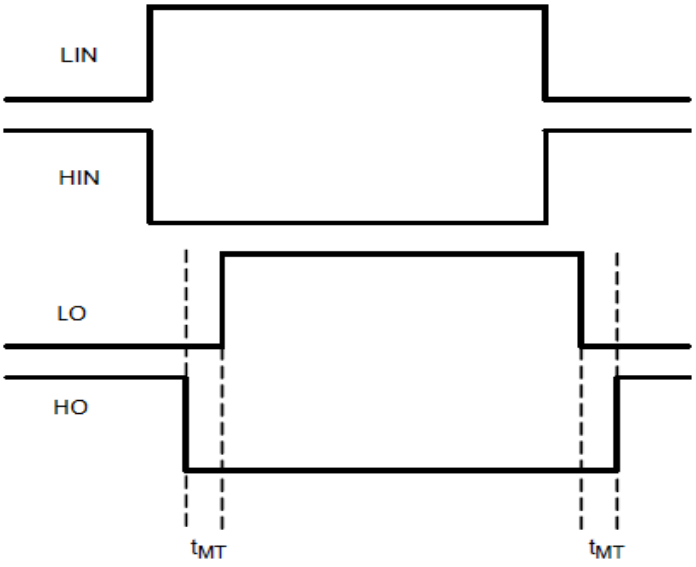


Figure 5. Delay Matching

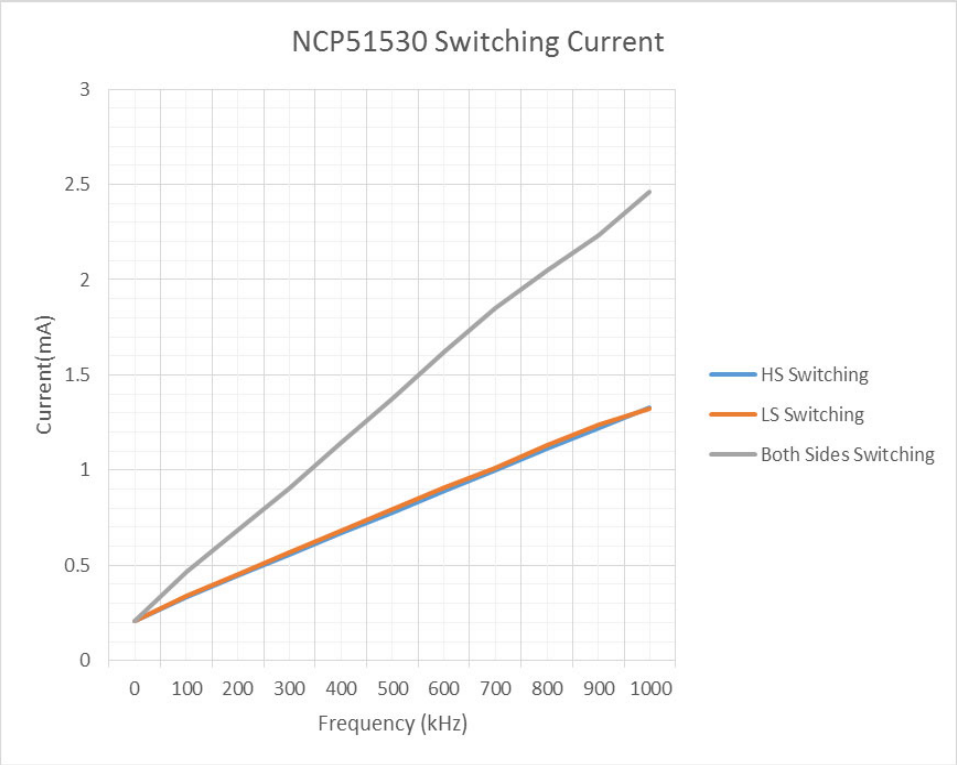


Figure 6. NCP51530 Operating Currents (No Load, V_{CC} = 12V)

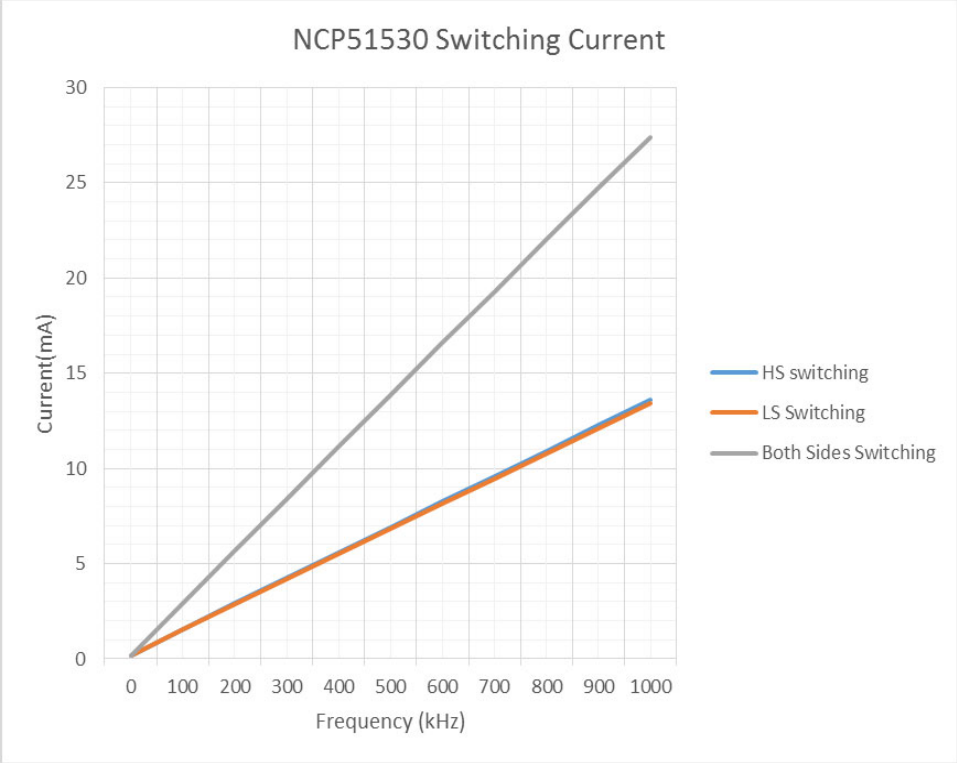


Figure 7. NCP51530 Operating Currents (1nF load, V_{CC} = 12V)

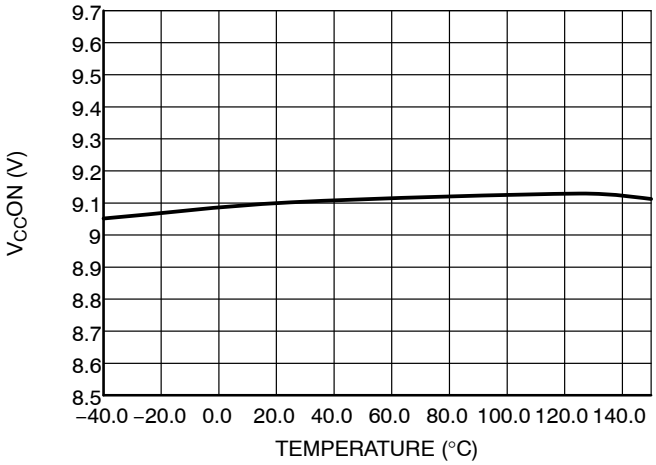


Figure 8. V_{CC}ON vs Temperature

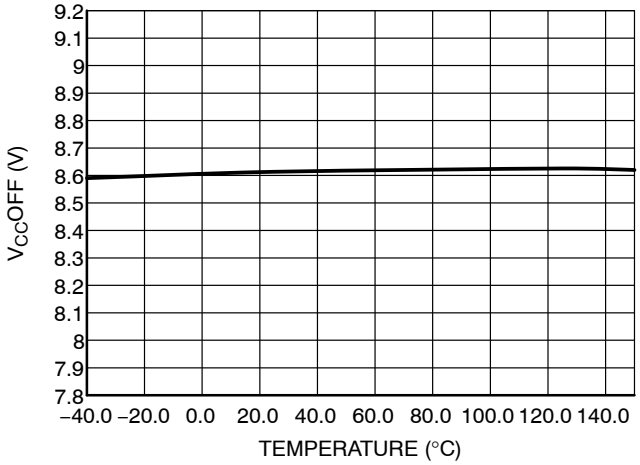


Figure 9. V_{CC}OFF vs Temperature

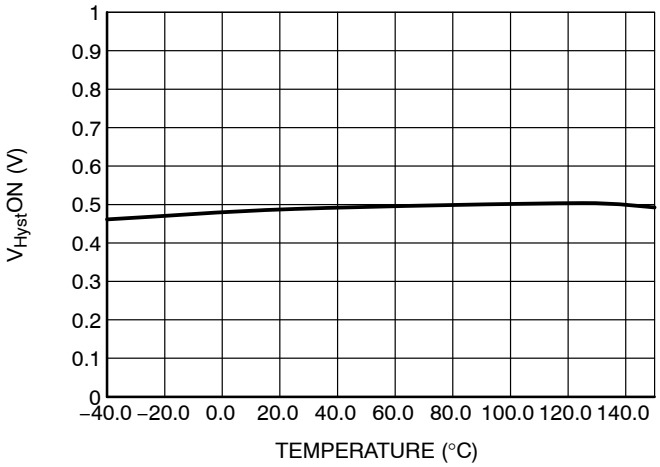


Figure 10. V_{CC}Hyst vs Temperature

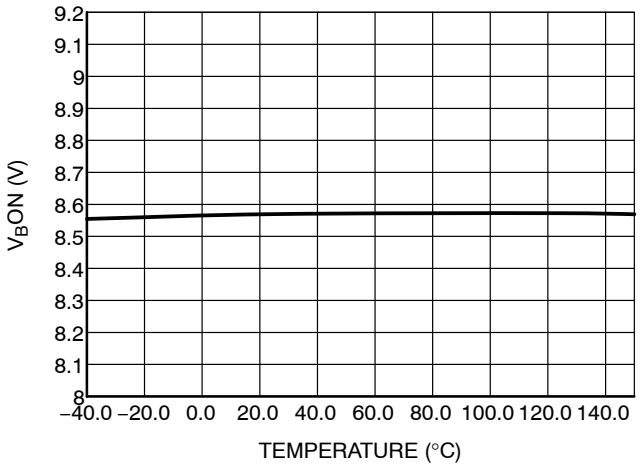


Figure 11. V_BON vs Temperature

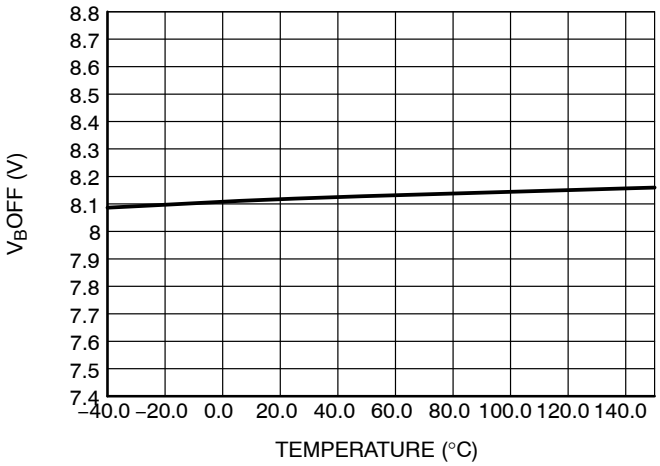


Figure 12. V_BOff vs Temperature

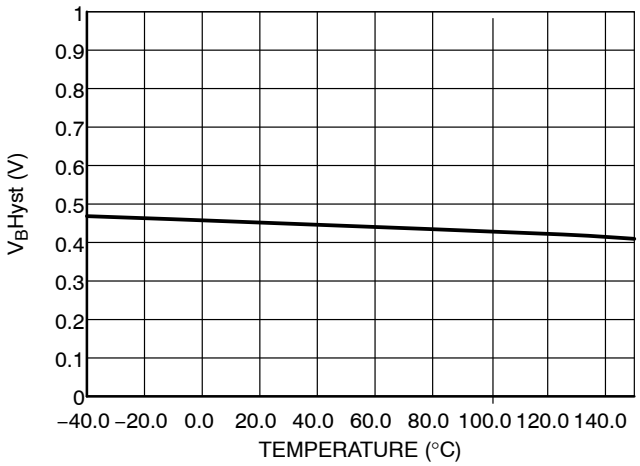


Figure 13. VbHyst vs Temperature

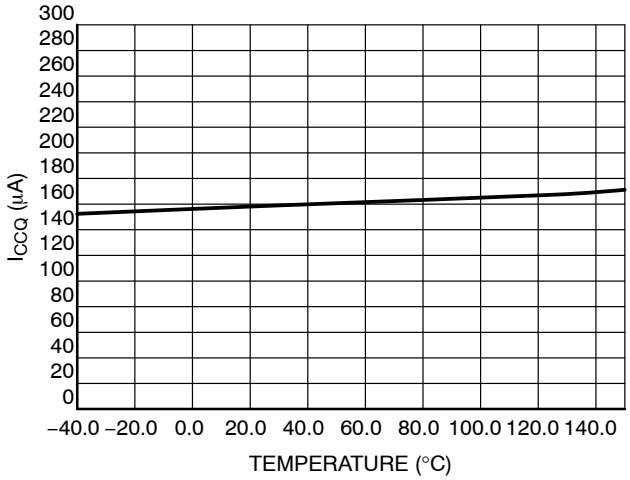


Figure 14. I_{CCQ} vs Temperature

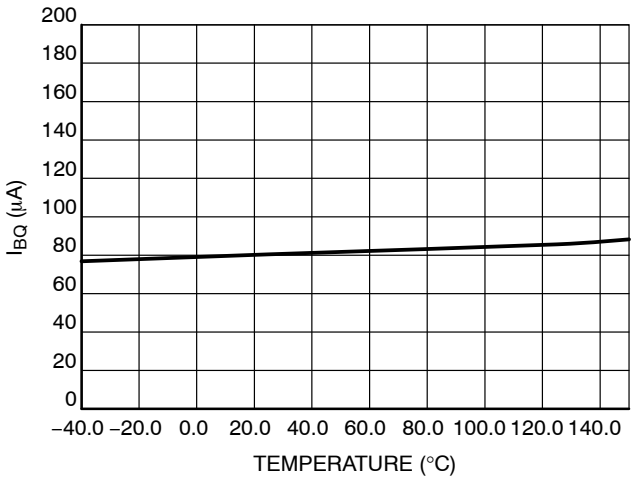


Figure 15. I_{BQ} vs Temperature

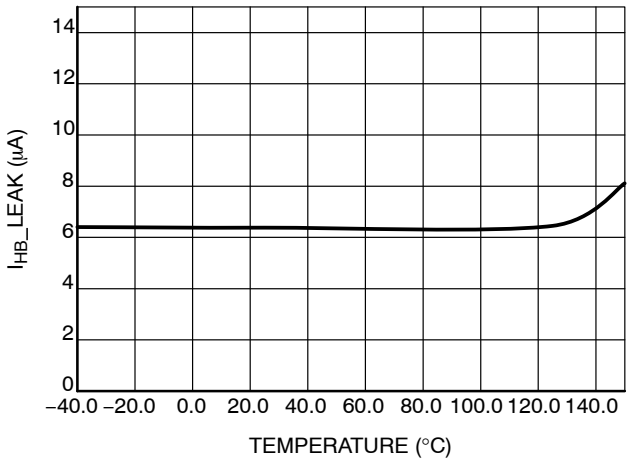


Figure 16. I_{HB}_Leakage vs Temperature

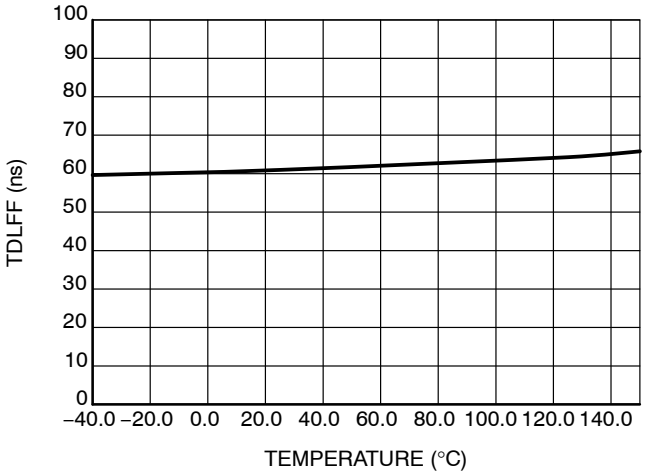


Figure 17. Low Side Turn on Propagation Delay vs Temperature

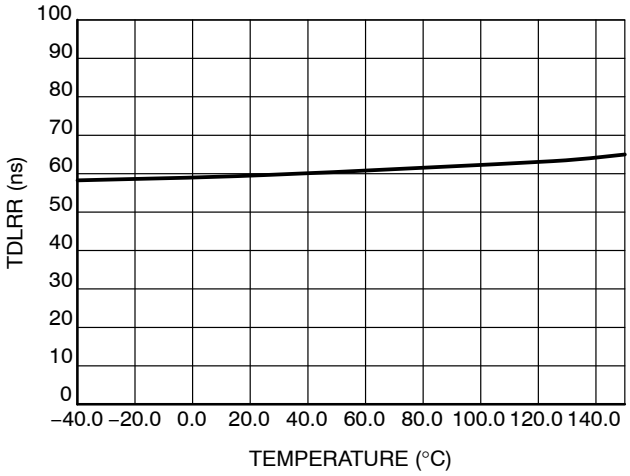


Figure 18. Low Side Turn on Propagation Delay vs Temperature

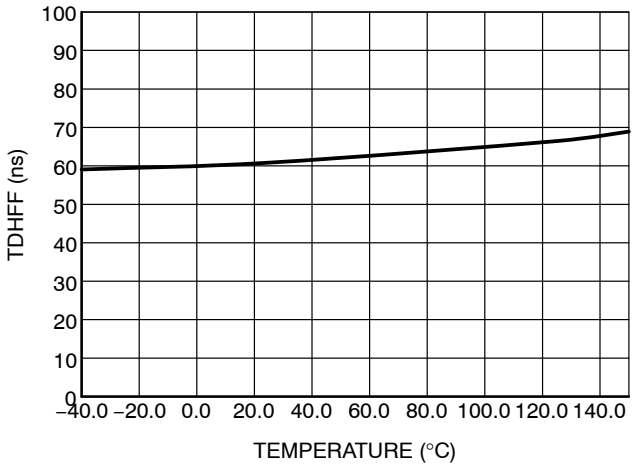


Figure 19. High Side Turn off Propagation Delay vs Temperature

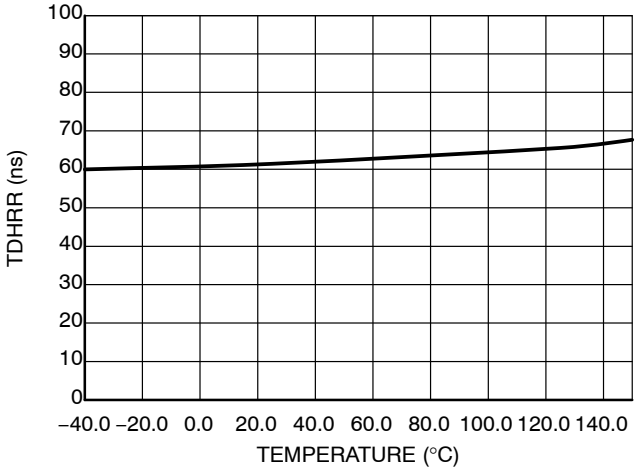


Figure 20. High Side Turn off Propagation Delay vs Temperature

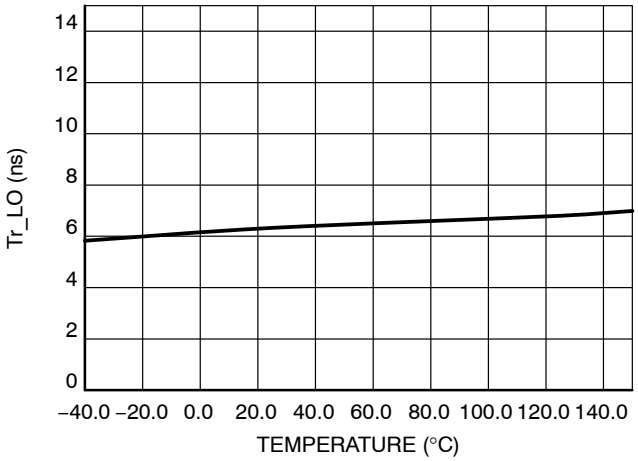


Figure 21. Low Side Rise Time vs Temperature

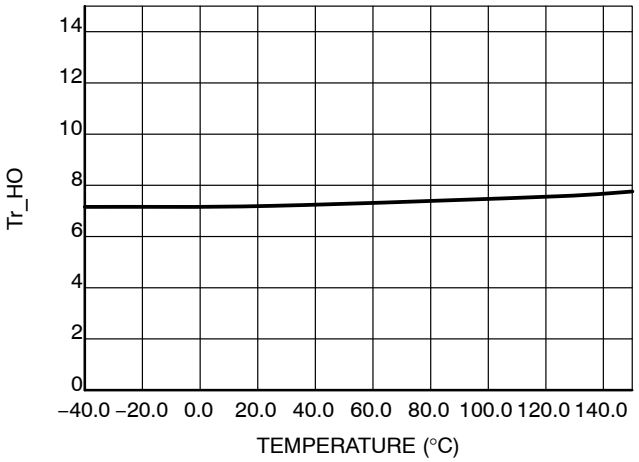


Figure 22. High Side Rise Time vs Temperature

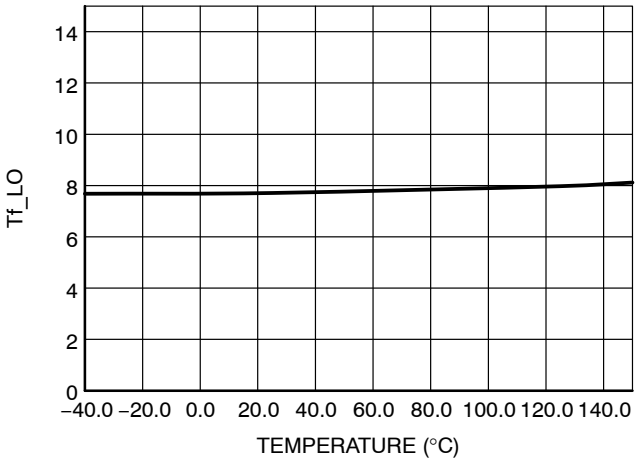


Figure 23. Low Side Fall Time vs Temperature

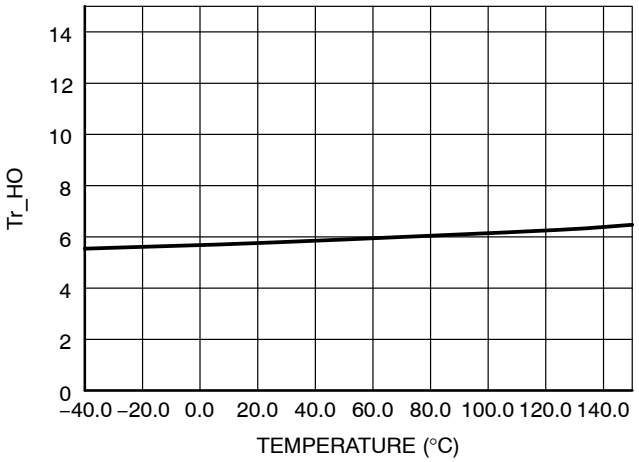


Figure 24. High Side Fall Time vs Temperature

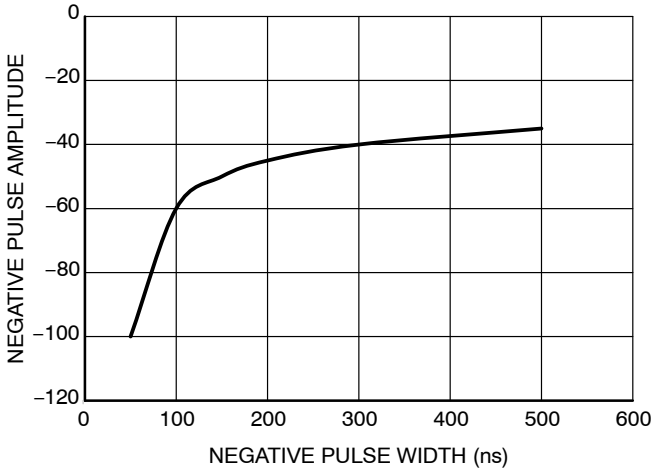


Figure 25. Typical Safe Operating Area with Negative Transient Voltage on HB Pin

GENERAL DESCRIPTION

For popular topologies like LLC, half bridge converters, full bridge converters, two switch forward converter etc. low−side high−side drivers are needed which perform the function of both buffer and level shifter. These devices can drive the gate of the topside MOSFETs whose source node is a dynamically changing node. The bias for the high side driver in these devices is usually provided through a bootstrap circuit.

In a bid to make modern power supplies more compact and efficient, power supply designers are increasingly opting for high frequency operations. High frequency operation causes higher losses in the drivers, hence reducing the efficiency of the power supply.

NCP51530 is a 700 V high side−low side driver for AC−DC power supplies and inverters. NCP51530 offers best in class propagation delay, low quiescent current and low switching current at high frequencies of operation. This device thus enables highly efficient power supplies operating at high frequencies.

NCP51530 is offered in two versions, NCP51530A/B. NCP51530A has a typical 60 ns propagation delay, while NCP51530B has propagation delay of 25 ns.

NCP51530 comes in SOIC8 and DFN10 packages. SOIC8 package of the device is pin to pin compatible with industry standard solutions.

NCP51530 has two independent input pins HIN and LIN allowing it to be used in a variety of applications. This device also includes features wherein, in case of floating input, the logic is still defined. Driver inputs are compatible with both CMOS and TTL logic hence it provides easy interface with analog and digital controllers. NCP51530 has under voltage lock out feature for both high and low side drivers which ensures operation at correct V_{CC} and V_B voltage levels. The output stage of NCP51530 has 3.5 A/3 A current source/sink capability which can effectively charge and discharge a 1 nF load in 15 ns.

FEATURES

INPUT STAGES

NCP51530 has two independent input pins HIN and LIN allowing it to be used in a variety of applications. The input stages of NCP51530 are TTL and CMOS compatible. This ensures that the inputs of NCP51530 can be driven with 3.3 V or 5 V logic signals from analog or digital PWM controllers or logic gates.

The input pins have Schmitt triggers to avoid noise induced logic errors. The hysteresis on the input pins is typically 1.3 V. This high value ensures good noise immunity.

NCP51530 comes with an important feature wherein outputs (HO, LO) stays low in case any of the input pin is floating. At both the input pins there is an internal pull down resistor to define its logic value in case the pin is left open or NCP51530 is driven by open drain signal. The input logic is explained in the Table 7 below.

NCP51530 input pins are also tolerant to negative voltage below the GND pin level as long as it is within the ratings defined in the datasheet. This tolerance allows the use of transformer as an isolation barrier for input pulses.

NCP51530A features a noise rejection function to ensure that any pulse glitch shorter than 30 ns will not produce any output. These features are well illustrated in the Figure 26 below.

NCP51530B has no such filters in the input stages. The timing diagram NCP51530B is Figure 27 below.

Table 7. INPUT TABLE

S.No	LIN	HIN	LO	HO
1	0	0	0	0
2	0	1	0	1
3	1	0	1	0
4	1	1	1	1
5	X	0	0	0
6	X	1	0	1
7	X	X	0	0
8	0	X	0	0
9	1	X	1	0

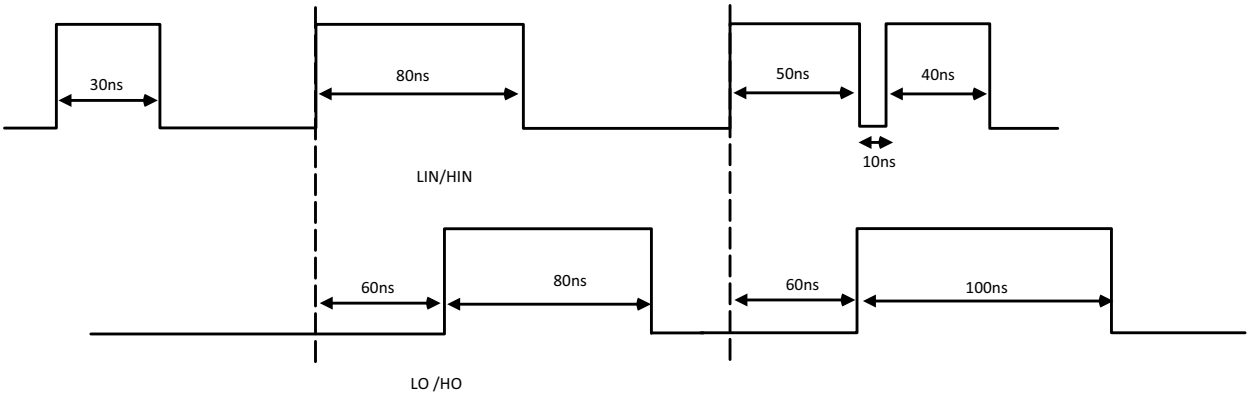


Figure 26. Input Filter (NCP51530A)

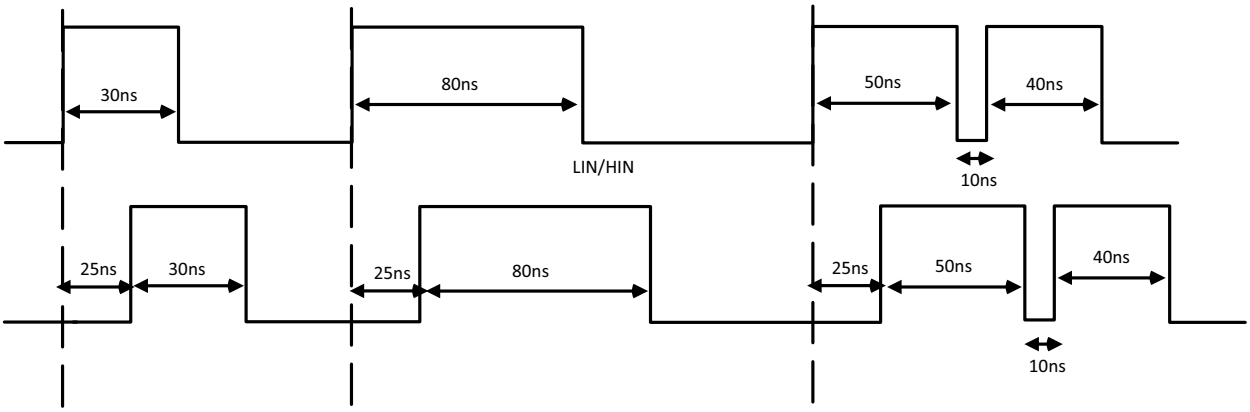


Figure 27. No Input Filter (NCP51530B)

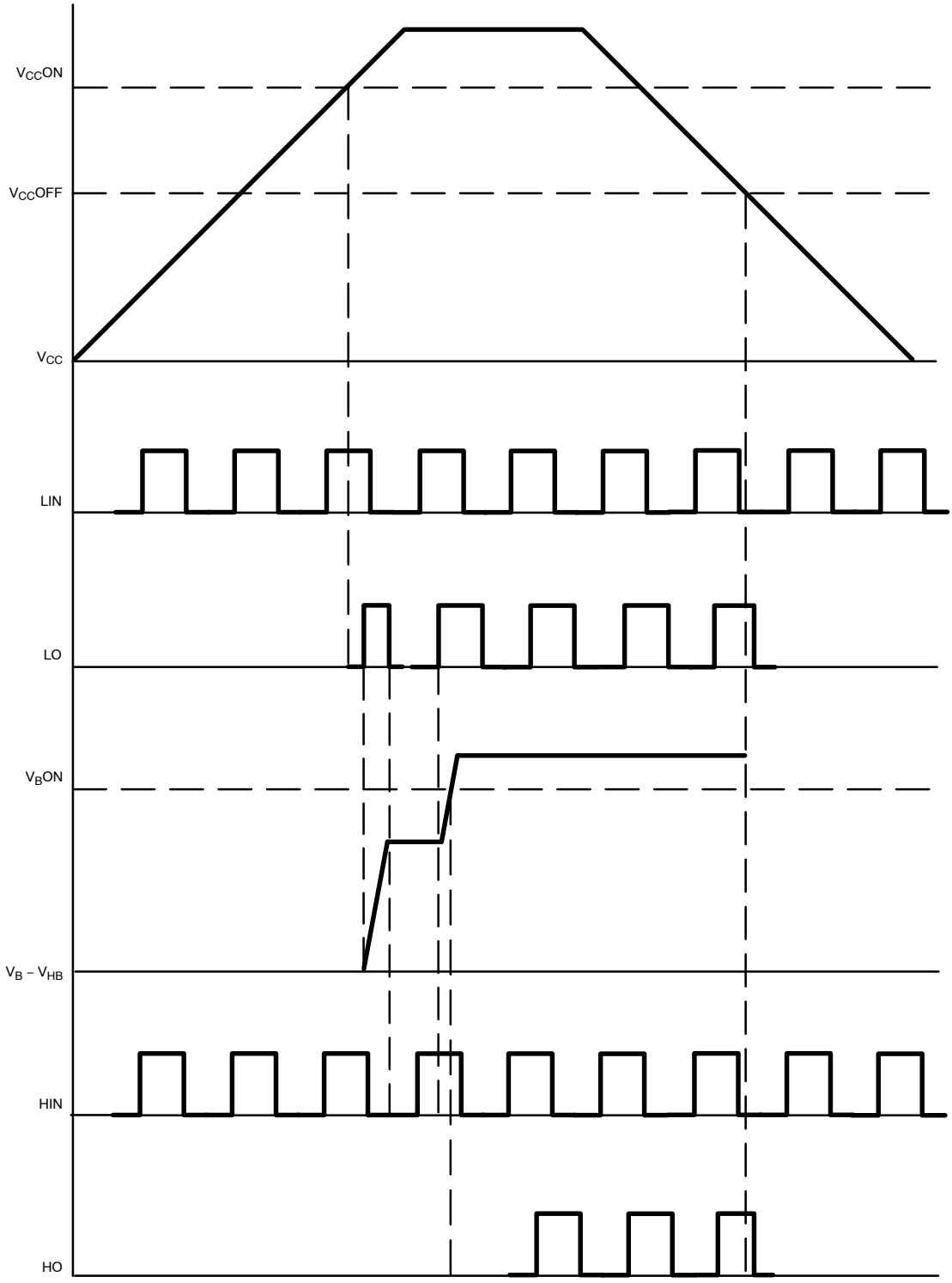


Figure 28. UVLO Timing Diagram

UNDER VOLTAGE LOCK–OUT

NCP51530 has under voltage lockout protection on both the high side and the low side driver. The function of the UVLO circuits is to ensure that there is enough supply voltages (V_{CC} and V_B) to correctly bias high side and low side circuits. This also ensures that the gate of external MOSFETs are driven at an optimum voltage.

If the V_{CC} is below the V_{CC} UVLO voltage, the low side driver output (LO) and high side driver output (HO) both remain low.

If V_B is below V_B UVLO voltage the high side driver output (HO) remains low. However if the V_{CC} is above V_{CC} UVLO voltage level, the low side driver output (LO) can still turn on and off based on the low side driver input (LI)

and is not affected by the V_B status. This ensures proper charging of the bootstrap capacitor to bring the high side bias supply V_B above UVLO voltage.

Both the V_{CC} and V_B UVLO circuits are provided with hysteresis feature. This hysteresis feature avoids errors due to ground noise in the power supply. The hysteresis also ensures continuous operation in case of a small drop in the bias voltage. This drop in the bias can happen when device starts switching MOSFET and the operating current of the device increases. The UVLO feature of the device is explained in the Figure 28.

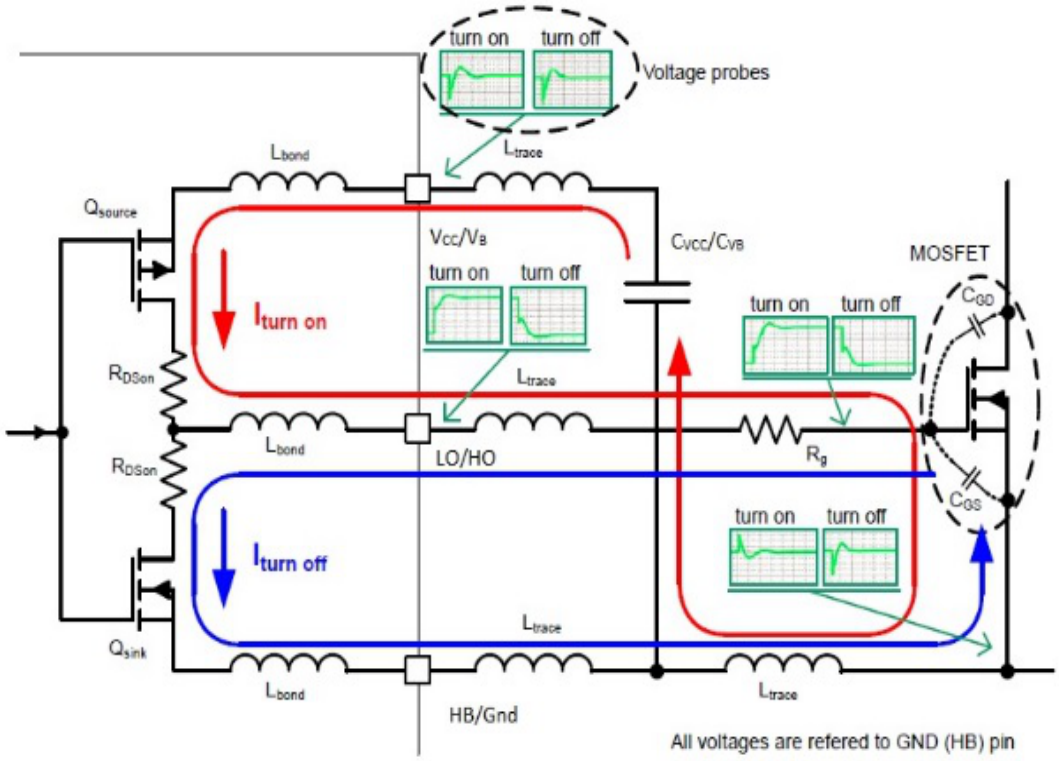


Figure 29. NCP51530 Turn ON−OFF Paths

OUTPUT STAGES

The NCP51530 is equipped with two independent drivers. The output stage of NCP51530 has 3.5 A/3 A current source/sink capability which can effectively charge and discharge a 1 nF load in 15 ns.

The outputs of NCP51530 can be turned on at the same time and there is no internal dead−time built between them. This allows NCP51530 to be used in topologies like two switch forward converter.

The figure below show the output stage structure and the charging and discharging path of the external power MOSFET. The bias supply V_{CC} or V_B supply the energy to charge the gate capacitance Cgs of the low side or the top side external MOSFETs respectively. When a logic high is received from input stage, Qsource turns on and V_{CC}/V_B starts charging Cgs through Rg. Once the Cgs is charged to the drive voltage level the external power MOSFET turns on the external MOSFET to discharge to GND/HB level.

When a logic low signal is received from the input stage, Qsource turns off and Qsink turns on providing a path for gate terminal of

As seen in the figure, there are parasitic inductances in charging and discharging path of the Cgs. This can result in a little dip in the bias voltages V_{CC}/V_B. If the V_{CC}/V_B drops below UVLO the power supply can shut down the device.



Figure 30. Low Side Turn−ON Propagation Delay (NCP51530A)

FAST PROPAGATION DELAY

NCP51530 boasts of industry best propagation delay between input and output. NCP51530A has a typical of 60 ns propagation delay. The best in class propagation delay in NCP51530 makes it suitable for high frequency operation.

Since NCP51530B doesn't have the input filter included, the propagation delay are even faster. NCP51530B offers 25 ns propagation delay between input and output.



Figure 31. Low Side Turn−Off Propagation Delay (NCP51530A)

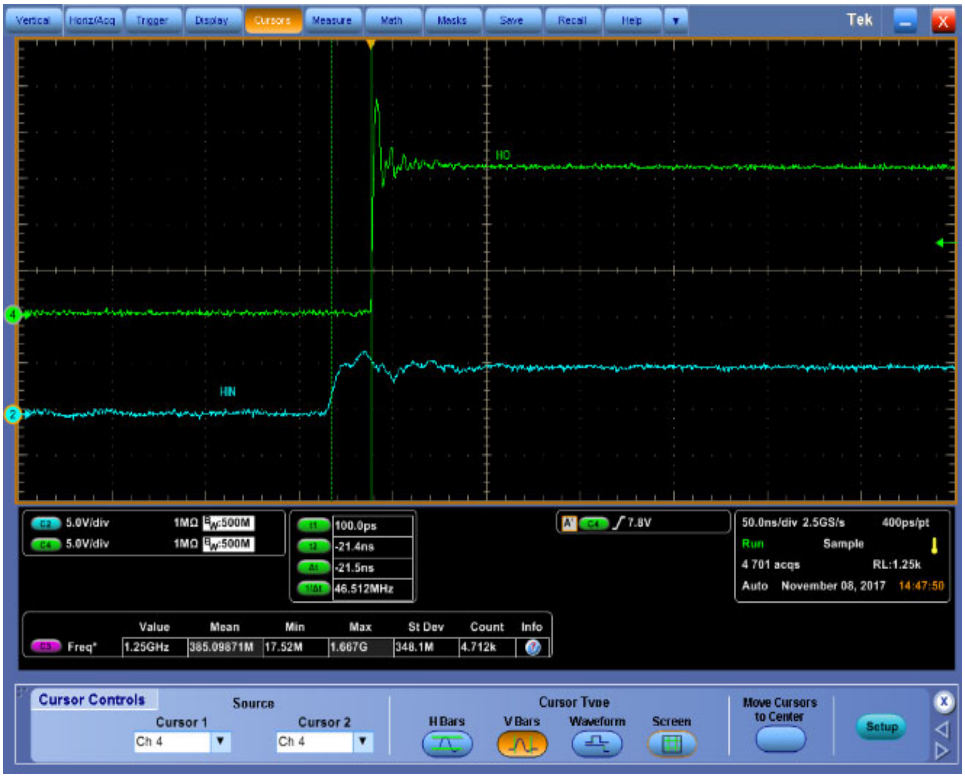


Figure 32. High Side Turn−Off Propagation Delay (NCP51530B)

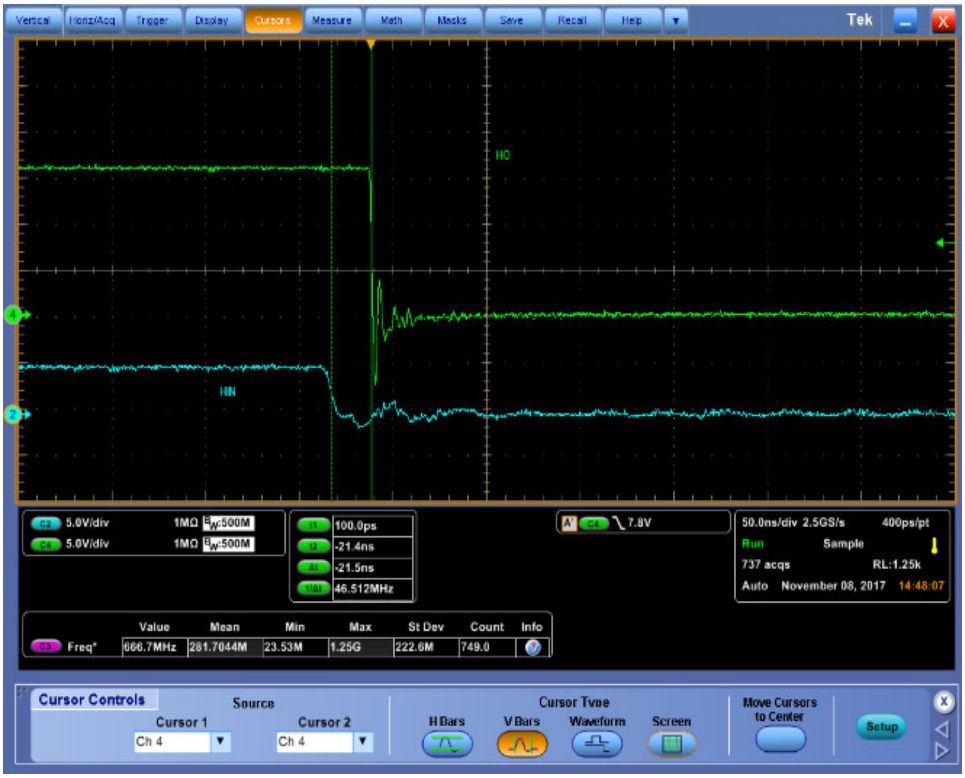


Figure 33. High Side Turn−Off Propagation Delay (NCP51530B)

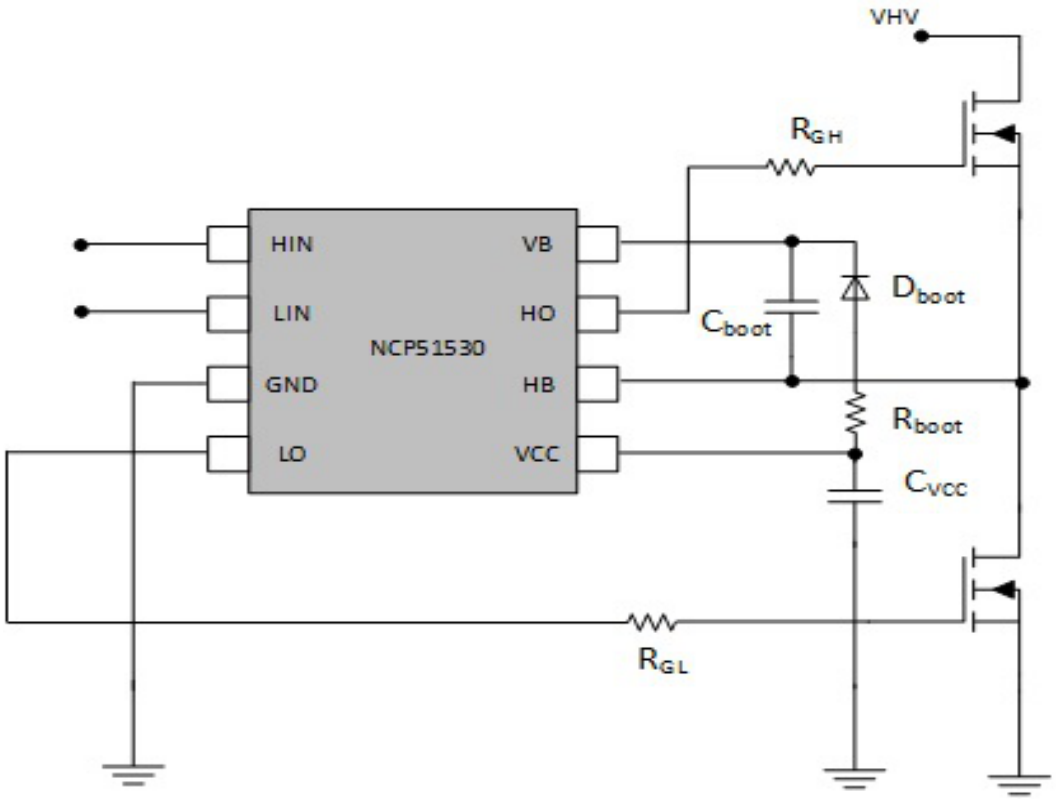


Figure 34. Bootstrap Circuit

COMPONENT SELECTION

C_{BOOT} CAPACITOR VALUE CALCULATION

NCP51530 has two independent drivers for driving high side and low side external MOSFETs. The bias for the high side driver is usually provided through a bootstrap circuit. A typical bootstrap circuit is shown in the figure 8 below.

The high side driver is biased by the C_{boot} (bootstrap capacitor). As can be seen in the circuit, C_{boot} will charge only when HB goes to GND level. Low value of C_{boot} can result in a little dip in the bias voltages V_B. If the V_B drops below UVLO the power supply can shut down the high side driver. Therefore choosing the right value of C_{boot} is very important for a robust design.

An example design for C_{boot} is given below.

$$Q_g = 30\ nC,\ V_{CC} = 15\ V \quad \text{(eq. 1)}$$

$$Q_b = I_{BQ} * t_{discharge} = 81\ \mu C * 5\ \mu S = 405\ pC \quad \text{(eq. 2)}$$

$$Q_{tot} = Q_g + Q_b = 30\ nC + 405p = 30.4\ pC \quad \text{(eq. 3)}$$

$$C_{boot} = \frac{Q_{tot}}{V_{ripple}} = \frac{30.4\ nC}{150\ mV} = 203\ nF \quad \text{(eq. 4)}$$

Qg is equivalent gate charge of the FET
I_{BQ} is the boot quiescent current
$t_{dishcharge}$ is the discharge time for bootstrap capacitor
V_{ripple} is the allowed ripple voltage in the bootstrap capacitor

It is recommended to use a larger value so as to cover any variations in the gate charge and voltage with temperature.

R_{boot} RESISTOR VALUE CALCULATION

R_{boot} resistor value is very important to ensure proper function of the device. A high value of R_{boot} would slow down the charging of the C_{boot} while too low a value would push very high charging currents for C_{boot}. For NCP51530 a value between 2 Ω and 10 Ω is recommended for R_{boot}.

For example R_{boot} = 5 Ω

$$I_{boot(pk)} = \frac{V_{CC} - V_D}{R_{boot}} = \frac{15\ V - 1\ V}{5\ \Omega} = 2.8\ A \quad \text{(eq. 5)}$$

Where V_D is the bootstrap diode forward drop.
Thus, R_{boot} value of 5 Ω keeps the peak current below 2.8 A.

HIN AND LIN INPUT FILTER

For PWM connection on the LIN and HIN pin of the NCP51530, a RC is recommended to filter high frequency input noise.

This filter is particularly important in case of NCP51530B where no internal filter is included.

The recommended value for R_{LIN}/R_{HIN} and C_{HIN}/C_{LIN} are as below.

R_{LIN}/R_{HIN} = 100 Ω
C_{HIN}/C_{LIN} = 120 pF

V_{CC} CAPACITOR SELECTION

V_{CC} capacitor value should be selected at least ten times the value of C_{boot}. In this case thus $C_{VCC} > 2\ \mu F$.

R_{gate} SELECTION

R_{gate} are selected to limit the peak gate current during charging and discharging of the gate capacitance. This resistance also helps to damp the ringing due to the parasitic inductances.

For example for a R_{gate} value of 5 Ω, the peak source and sink currents would be limited to the following values.

$$R_{gate} = 5\Omega \quad \text{(eq. 6)}$$

$$I_{LO_Source} = \frac{V_{CC}}{R_{Lgate} + R_{LOH}} = \frac{15\ V}{6.7\ \Omega} = 2.23\ A \quad \text{(eq. 7)}$$

$$I_{LO_Sink} = \frac{V_{CC}}{R_{Lgate} + R_{LOL}} = \frac{15\ V}{6.8\ \Omega} = 2.20\ A \quad \text{(eq. 8)}$$

$$I_{HO_Source} = \frac{V_{CC} - V_{Dboot}}{R_{Lgate} + R_{HOH}} = \frac{14\ V}{6.7\ \Omega} = 2.09\ A \quad \text{(eq. 9)}$$

$$I_{HO_Sink} = \frac{V_{CC} - V_{Dboot}}{R_{Lgate} + R_{HOL}} = \frac{15\ V - 1\ V}{6.8\ \Omega} = 2.06\ A \quad \text{(eq. 10)}$$

TOTAL POWER DISSIPATION

Total power dissipation of NCP51530 can be calculated as follows.

1. Static power loss of device (excluding drivers) while switching at an appropriate frequency.

$$P_{operating} = V_{boot} * I_{BO} + V_{CC} * I_{CCO} \quad \text{(eq. 11)}$$
$$= 14\ V * 0.4\ mA + 15\ V * 0.4\ mA = 11.6\ mW$$

I_{BO} is the operating current for the high side driver
I_{CCO} is the operating current for the low side driver

2. Power loss of driving external FET (Hard Switching)

$$P_{drivers} = \left(\left(Q_g * V_{boost}\right) + \left(Q_g * V_{CC}\right)\right)f \quad \text{(eq. 12)}$$
$$= ((30\ nC * 14\ V) + (30\ nC * 15\ V)) * 100\ kHz = 87\ mW$$

Q_g is total gate charge of the MOSFET

3. Power loss of driving external FET (Soft Switching)

$$P_{drivers} = \left(\left(Q_{gs} * V_{boot}\right) + \left(Q_{gs} * V_{CC}\right)\right) * f \quad \text{(eq. 13)}$$
$$= ((4\ nC * 14\ V) + (4\ nC * 15\ V)) * 100\ kHz = 11\ mW$$

4. Level shifting losses

$$P_{levelshifting} = \left(V_r + V_b\right) * Q * f \quad \text{(eq. 14)}$$
$$= 415\ V * 0.5\ nC * 100\ kHz = 20.75\ mW$$

Vr is the rail voltage
Q is the substrate charge on the level shifter

5. Total Power Loss (Hard Switching)

$$P_{total} = P_{driver} + P_{operating} + P_{levelshifting} \quad \text{(eq. 15)}$$
$$= 11.6\ mW + 87\ mW + 20.75\ mW = 119.35\ mW$$

6. Junction temperature increase

$$t_J = R_{\theta JA} * P_{total} = 183 * 0.14 = 25^\circ C \quad \text{(eq. 16)}$$

LAYOUT RECOMMENDATIONS

NCP51530 is a high speed and high current high side and low side driver. To avoid any device malfunction during device operation, it is very important that there is very low parasitic inductance in the current switching path. It is very important that the best layout practices are followed for the PCB layout of the NCP51530. An example layout is shown in the figure below. Some of the layout rules to be followed are listed below.

- Keep the low side drive path LO−Q1−GND as small as possible. This reduces the parasitic inductance in the path and hence eliminates ringing on the gate terminal of the low side MOSFET Q1.
- Keep the high side drive loop HO−Q2−HB as small as possible. This reduces the parasitic inductance in the path and hence eliminates ringing on the gate terminal of the low side MOSFET Q1.
- Keep C_{VCC} as near to the V_{CC} pin as possible and the V_{CC}−CV_{CC}−GND loop as small as possible.
- Keep C_{VB} as near to VB pin as possible and VB−CVB−HB loop as small as possible.
- Keep the HB−GND−Q1 loop as small as possible. This loop has the potential to produce a negative voltage spike on the HB pin. This negative voltage spike can cause damage to the driver. This negative spike can increase the boot capacitor voltage above the maximum rating and hence cause damage to the driver.

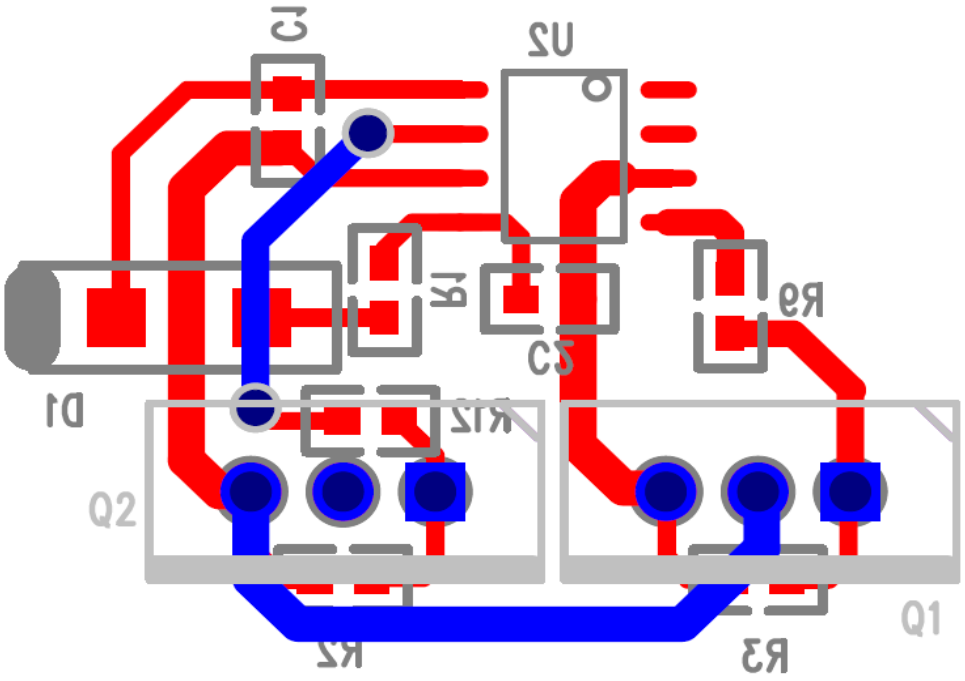


Figure 35. Example Layout

IMPACT IONIZATION CURRENT

NCP51530 tends to exhibit an Impact Ionization current that flows from the boot pin (VB) to ground (GND) under certain conditions. This happens when voltage on the bridge pin (HB) is less than 40 V for a time greater than 100 μs and that is immediately followed by switching event that pulls−up the HB pin above 150 V. This current can potentially last multiple switching cycle before it diminishes. Furthermore, Impact Ionization current is not seen in systems where the bulk voltage is always below 150 V i.e., HB node is never pulled above 150 V, for instance, a 48 V to 12 V full−bridge power converter.

Figure 36 below shows an example of Impact Ionization current. This example shows a half−bridge converter running at 100 kHz frequency with 3 μs on−time. It shows Impact Ionization current flowing in first three pulses during startup and subsiding thereafter.

Depending on the duration and magnitude of the Impact Ionization current it can lead to thermal stress on the device which can potentially, in corner cases, cause a thermal failure of NCP51530.

Following are the safe conditions under which the Impact Ionization current doesn't occur:

1. Systems where VHB < 150 V and VBOOT < 170 V.
   OR
2. Systems where VHB > 40 V before the start of switching
   OR

3. Further, if the dv/dt of the VHB is kept under 0.1 V/ns, then the Impact Ionization current substantially reduces.

Mitigating Impact Ionization Current in Various Topologies

- Flyback Converters and derivatives: Any topologies based on flyback or derivatives (DCM/CCM Flyback, Active Clamp Flyback, and AHB Flyback) do not show any Impact Ionization current. This is because that transformer in the flyback topology is connected to input directly hence the VHB at t = 0 is at input voltage (> 40 V) satisfying the second conditioned mentioned above.

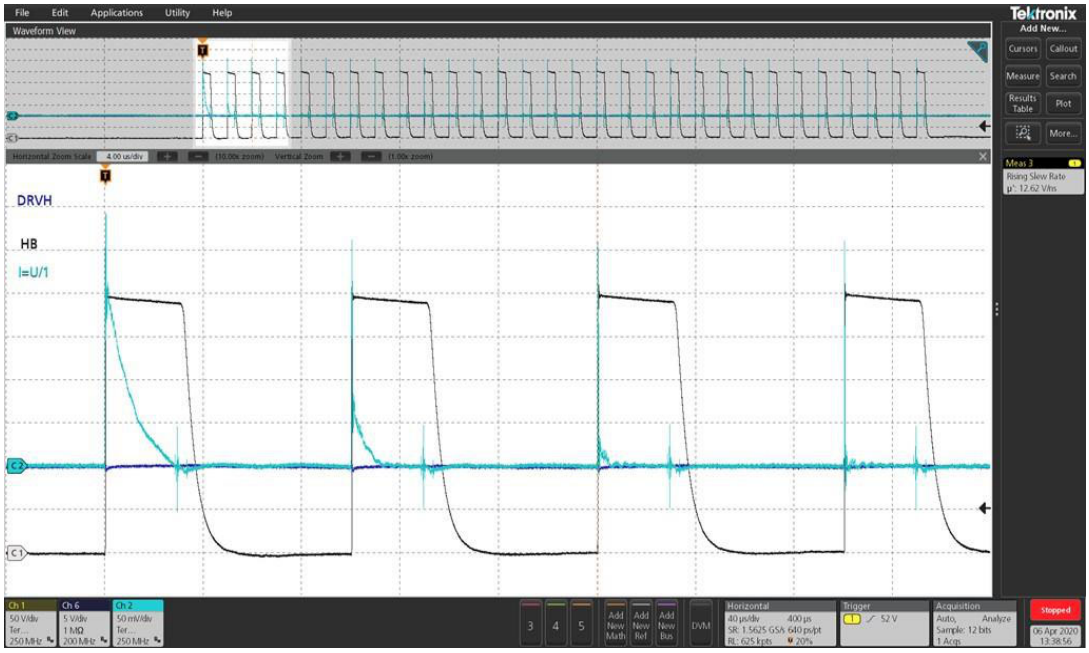


Figure 36. Impact Ionization Current in NCP51530. C1 is HB node at 50 V/div and C2 is Impact Ionization Current at 50 mA/div

- Synchronous Boost Converter: Similar to flyback the VHB at t = 0 is at input voltage (> 40 V) so no Impact Ionization current flows.
- Phase Shifted Full−bridge: The HB pin can be potentially at less than 40 V when switching starts. This can cause Impact Ionization current to flow during startup and in burst mode. This can be mitigated by adding parallel resistors (>1 Meg) across the FETs. This ensures that the voltage on HB pin at t = 0 is greater than 40 V. This is shown in figure 2 below. R1, R2, R3 and R4 ensure that the switch node voltage is at a voltage greater than 40 V before the switching starts.
- High Voltage Synchronous Buck Converter: Synchronous buck presents the worst case for the Impact Ionization current. The HB is at a voltage equal to output voltage always at t= 0. Hence at the startup or in the cases of burst mode we see Impact Ionization current when the Vout < 40 V. One potential solution can be pre−charging the output with VCC through a diode and running the system in soft−switching from first pulse itself. However if the regulated Vout is less than 40 V then there is a chance of Impact Ionization current every burst cycle. But as explained earlier this occurs only in case of HV systems. When the bulk voltage is less than 150 V no Impact Ionization current is seen.

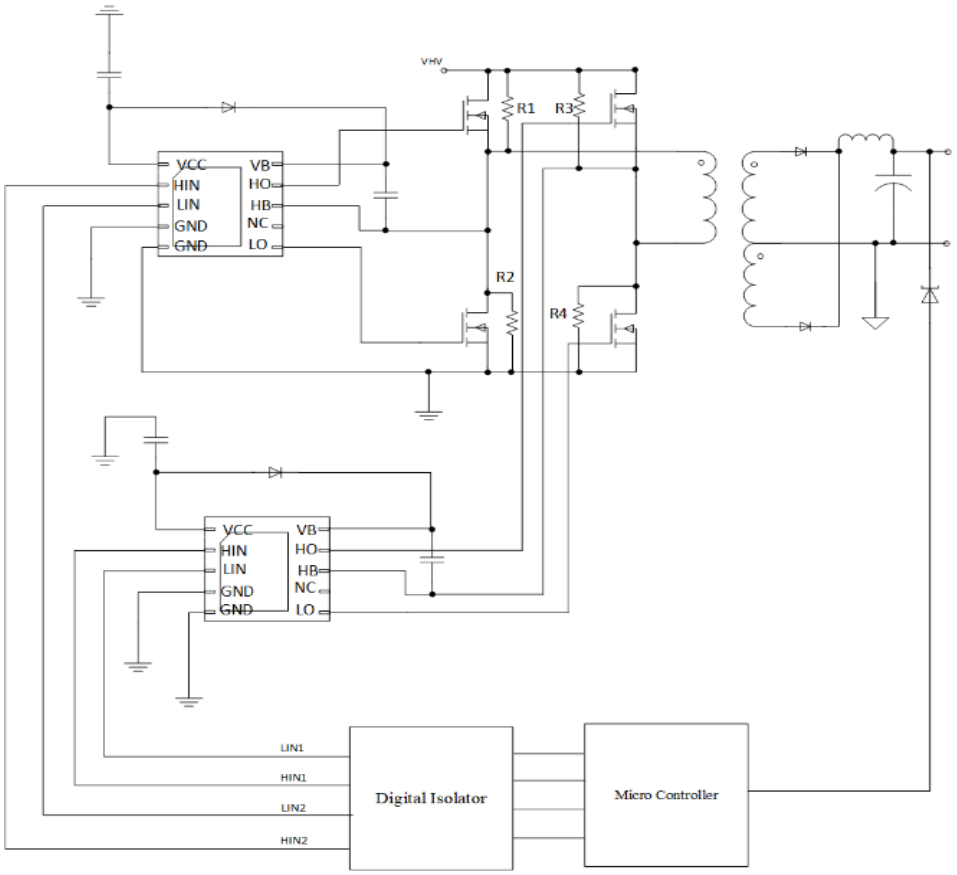


Figure 37. Phase Shifted Full Bridge Using NCP51530

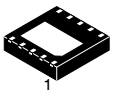
ORDERING INFORMATION

Device	Propagation Delay (ns)	Input filter	Package	Shipping†
NCP51530ADR2G	60	Yes	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP51530BDR2G	25	No	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP51530AMNTWG	60	Yes	DFN10 4x4 (Pb−Free)	4000 / Tape & Reel
NCP51530BMNTWG	25	No	DFN10 4x4 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

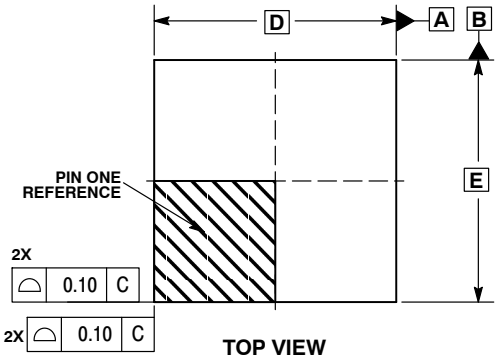
ON Semiconductor®

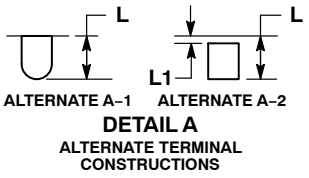


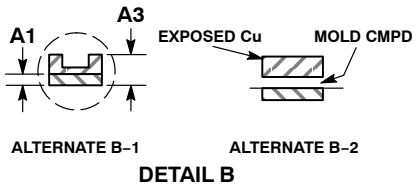
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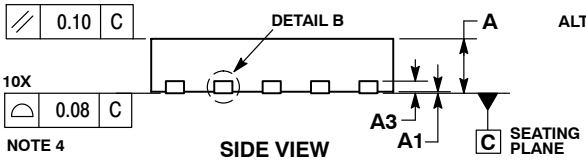
DFN10 4x4, 0.8P
CASE 506DJ
ISSUE O

DATE 20 MAY 2016



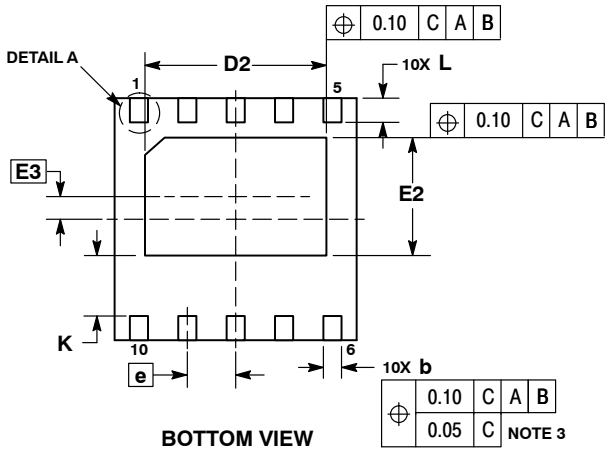






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A ALTERNATE CONSTRUCTION A–2 AND DETAIL B ALTERNATE CONSTRUCTION B–2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	2.90	3.10
E	4.00 BSC	
E2	1.85	2.05
E3	0.375 BSC	
e	0.80 BSC	
K	0.90	---
L	0.35	0.45
L1	0.00	0.15



GENERIC MARKING DIAGRAM*

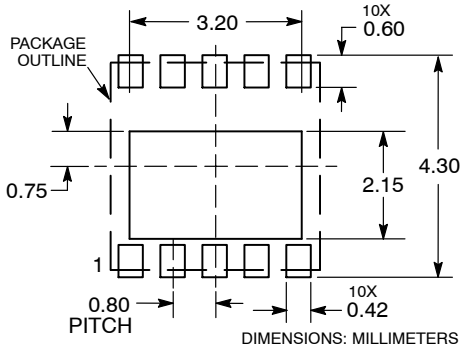


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	DFN10 4X4, 0.8P	PAGE 1 OF 1

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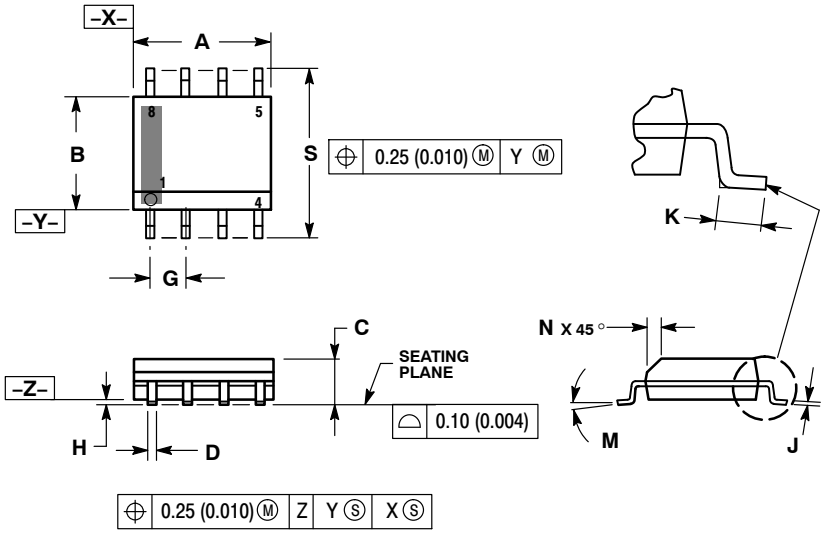
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

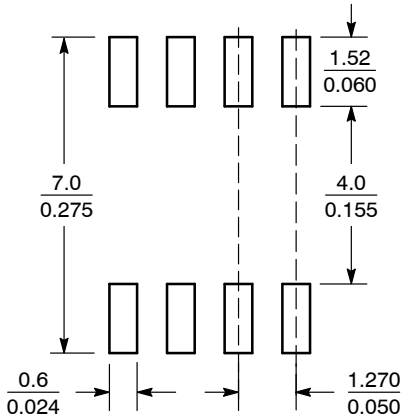
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

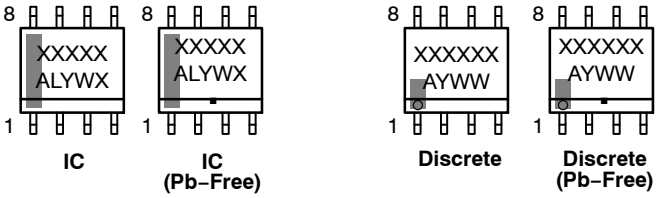
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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