NCP5183, NCV5183

High Voltage High Current High and Low Side Driver

The NCP5183 is a High Voltage High Current Power MOSFET Driver providing two outputs for direct drive of 2 N−channel power MOSFETs arranged in a half−bridge (or any other high−side + low−side) configuration.

It uses the bootstrap technique to insure a proper drive of the High−side power switch. The driver works with 2 independent inputs to accommodate any topology (including half−bridge, asymmetrical half−bridge, active clamp and full−bridge…).

Features

- Automotive Qualified to AEC Q100
- Voltage Range: up to 600 V
- dV/dt Immunity ±50 V/ns
- Gate Drive Supply Range from 9 V to 18 V
- Output Source / Sink Current Capability 4.3 A / 4.3 A
- 3.3 V and 5 V Input Logic Compatible
- Extended Allowable Negative Bridge Pin Voltage Swing to –10 V
  - Matched Propagation Delays between Both Channels
  - Propagation Delay 120 ns typically
  - Under V_{CC} LockOut (UVLO) for Both Channels
- Pin to Pin Compatible with Industry Standards
- These are Pb−free Devices

Typical Application

- Power Supplies for Telecom and Datacom
- Half−Bridge and Full−Bridge Converters
- Push−Pull Converters
- High Voltage Synchronous−Buck Converters
- Motor Controls
- Electric Power Steering
- Class−D Audio Amplifiers

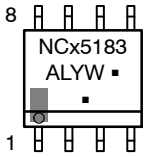
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SOIC−8 NB
CASE 751−07

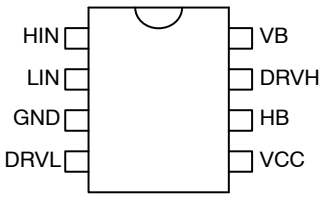
MARKING DIAGRAM



x	= P or V
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP5183DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCV5183DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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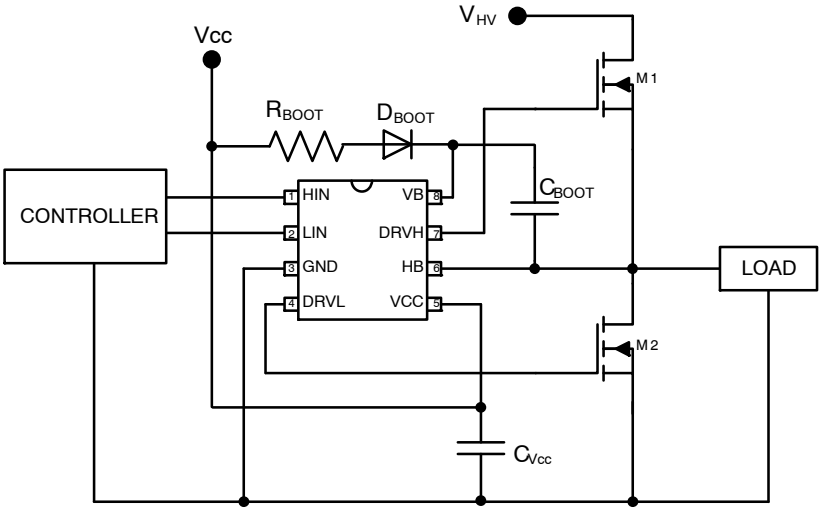


Figure 1. Application Schematic

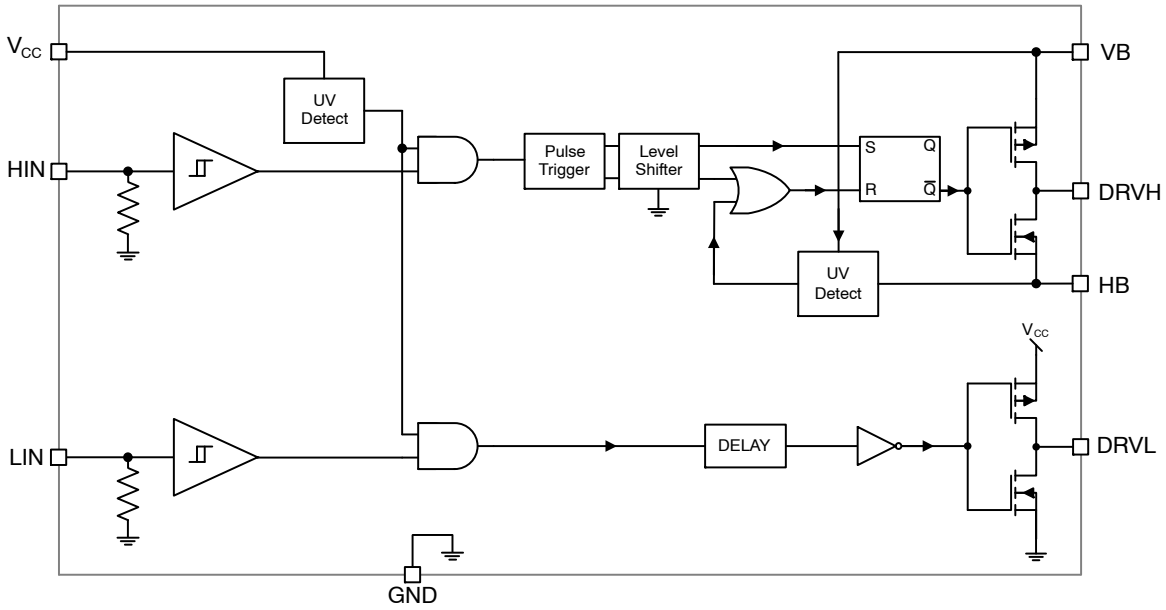


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. (SOIC8)	Pin Name	Description
1	HIN	High Side Logic Input
2	LIN	Low Side Logic Input
3	GND	Ground
4	DRVL	Low Side Gate Drive Output
5	V_{CC}	Main Power Supply
6	HB	Bootstrap Return or High Side Floating Supply Return
7	DRVH	High Side Gate Drive Output
8	VB	Bootstrap Power Supply

Table 2. ABSOLUTE MAXIMUM RATINGS
All voltages are referenced to GND pin

Rating	Symbol	Value	Units
Input Voltage Range	V_{CC}	−0.3 to 18	V
Input Voltage on LIN and HIN pins	V_{LIN}, V_{HIN}	−0.3 to 18	V
High Side Boot pin Voltage	V_B	(higher of {−0.3 ; V_{CC} − 1.5}) to 618	V
High Side Bridge pin Voltage	V_{HB}	V_B − 18 to V_B + 0.3	V
High Side Floating Voltage	$V_B - V_{HB}$	−0.3 to 18	V
High Side Output Voltage	V_{DRVH}	V_{HB} − 0.3 to V_B + 0.3	V
Low Side Output Voltage	V_{DRVL}	−0.3 to V_{CC} + 0.3	V
Allowable output slew rate	dV_{HB}/dt	50	V/ns
Maximum Operating Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	−55 to 150	°C
ESD Capability, Human Body Model (Note 1)	ESDHBM	3	kV
ESD Capability, Charged Device Model (Note 1)	ESDCDM	1	kV
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per AEC−Q100−11 (EIA/JESD22−C101E)
   Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Units
Thermal Characteristics SO8 (Note 3) Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	183	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 5)
All voltages are referenced to GND pin

Rating	Symbol	Min	Max	Units
Input Voltage Range	V_{CC}	10	17	V
High Side Floating Voltage	$V_B - V_{HB}$	10	17	V
High Side Bridge pin Voltage	V_{HB}	−1	580	V
High Side Output Voltage	V_{DRVH}	V_{HB}	V_B	V
Low Side Output Voltage	V_{DRVL}	GND	V_{CC}	V
Input Voltage on LIN and HIN pins	V_{LIN}, V_{HIN}	GND	V_{CC} − 2	V
Operating Junction Temperature Range	T_J	−40	125	°C

5. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$, $V_{CC} = V_B = 15$ V, V_{HB} = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted. Typical values are at $T_J = +25°C$. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Supply Section						
V_{CC} UVLO	V_{CC} rising	V_{CCon}	7.8	8.8	9.8	V
	V_{CC} falling	V_{CCoff}	7.2	8.3	9.1	V
	V_{CC} hysteresis	V_{CChyst}		0.5		V
V_B UVLO	V_B rising	V_{Bon}	7.8	8.8	9.8	V
	V_B falling	V_{Boff}	7.2	8.3	9.1	V
	V_B hysteresis	V_{Bhyst}		0.5		V
V_{CC} pin operating current	f = 20 kHz, C_L = 1 nF	I_{CC1}		520	700	μA
V_B pin operating current	f = 20 kHz, C_L = 1 nF	I_{B1}		700	800	μA
V_{CC} pin quiescent current	$V_{LIN} = V_{HIN} = 0$ V	I_{CC2}		95	160	μA
V_B pin quiescent current	$V_{LIN} = V_{HIN} = 0$ V	I_{B2}		65	100	μA
V_B to GND quiescent current	$V_B = V_{HB} = 600$ V	I_{HSleak}			50	μA
Input Section						
Logic High Input Voltage		V_{INH}	2.5			V
Logic Low Input Voltage		V_{INL}			1.2	V
Logic High Input Current	$V_{xIN} = 5$ V	I_{xIN+}		25	50	μA
Logic Low Input Current	$V_{xIN} = 0$ V	I_{xIN-}			1	μA
Input Pull Down Resistance	$V_{xIN} = 5$ V	R_{xIN}	100	250		kΩ
Output Section						
Low Level Output Voltage	$I_{DRVL} = 0$ A	V_{DRVLL}			35	mV
Low Level Output Voltage (HS Driver)	$I_{DRVH} = 0$ A	V_{DRVHL}			35	mV
High Level Output Voltage	$I_{DRVL} = 0$ A, $V_{DRVLH} = V_{CC} - V_{DRVL}$	V_{DRVLH}			35	mV
High Level Output Voltage (HS Driver)	$I_{DRVH} = 0$ A, $V_{DRVHH} = V_B - V_{DRVH}$	V_{DRVHH}			35	mV
Output Positive Peak current	$V_{DRVL} = 0$ V, PW = 10 μs	I_{DRVLH}		4.3		A
Output Negative Peak current	$V_{DRVL} = 15$ V, PW = 10 μs	I_{DRVLL}		4.3		A
Output Positive Peak current (HS Driver)	$V_{DRVH} = 0$ V, PW = 10 μs	I_{DRVHH}		4.3		A
Output Negative Peak current (HS Driver)	$V_{DRVH} = 15$ V, PW = 10 μs	I_{DRVHL}		4.3		A
Output Resistance		R_{OH}		1.7		Ω
Output Resistance		R_{OL}		1.1		Ω
Dynamic Section						
Turn On Propagation Delay		t_{ON}		120	200	ns
Turn Off Propagation Delay		t_{OFF}		120	200	ns
Delay Matching	Pulse width = 1 μs	t_{MT}		0	50	ns
Minimum Positive Pulse Width	$V_{xIN} = 0$ V to 5 V	t_{minH}			150	ns
Minimum Negative Pulse Width	$V_{xIN} = 5$ V to 0 V	t_{minL}			100	ns

6. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible

Table 5. ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$, $V_{CC} = V_B = 15$ V, V_{HB} = GND, outputs are not loaded, all voltages are referenced to GND; unless otherwise noted. Typical values are at $T_J = +25°C$. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
Switching Parameters						
Output Voltage Rise Time	10% to 90%, C_L = 1 nF	t_r		12	40	ns
Output Voltage Fall Time	90% to 10%, C_L = 1 nF	t_f		12	40	ns
Negative HB pin Voltage	$PW \le t_{ON}$, $V_{CC} = V_B = 10$ V	V_{HBneg}		–8	–7	V

6. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible

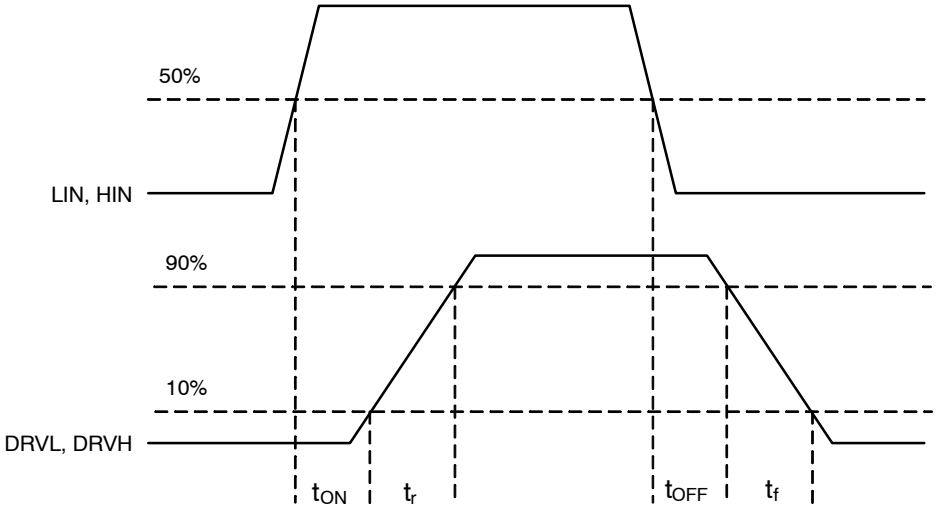


Figure 3. Propagation Delay, Rise Time and Fall Time Timing

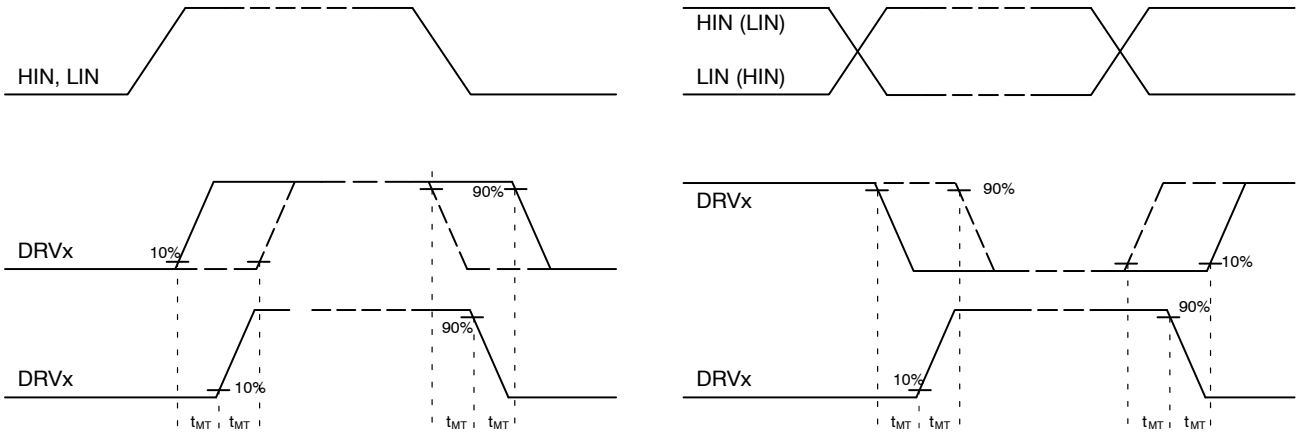


Figure 4. Delay Matching

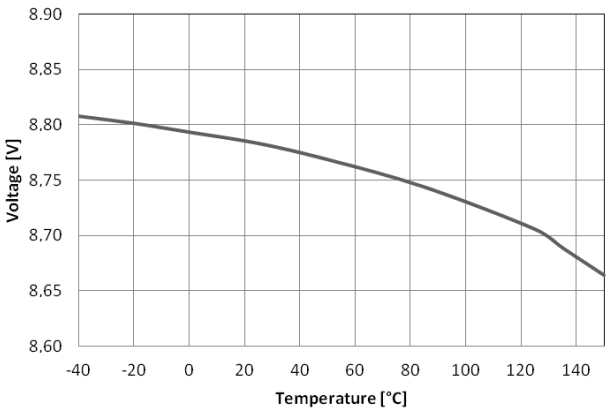


Figure 5. V_{CCon} vs. Temperature

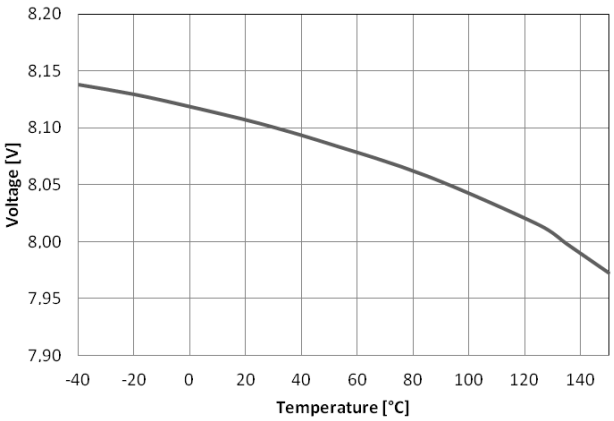


Figure 6. V_{CCoff} vs. Temperature

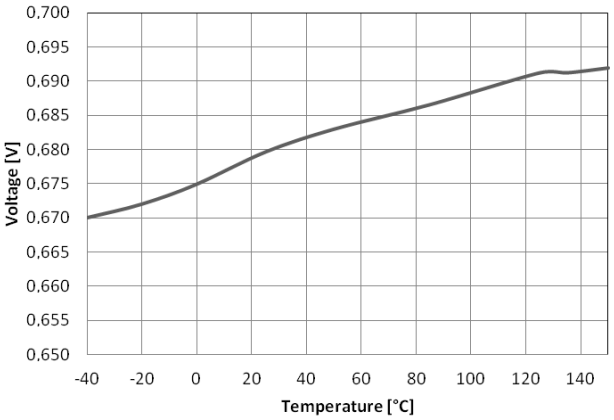


Figure 7. $V_{CCUVLOHYS}$ vs. Temperature

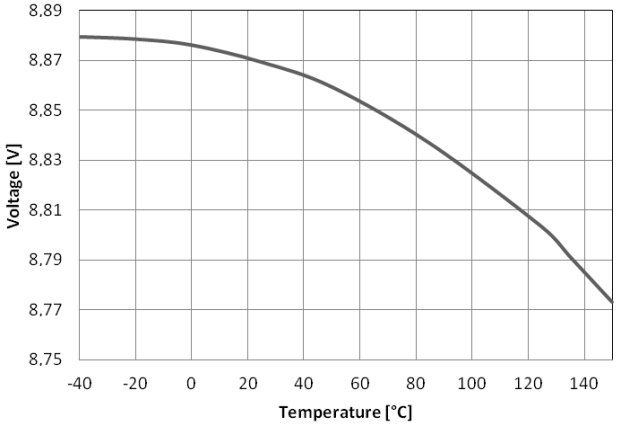


Figure 8. V_{Bon} vs. Temperature

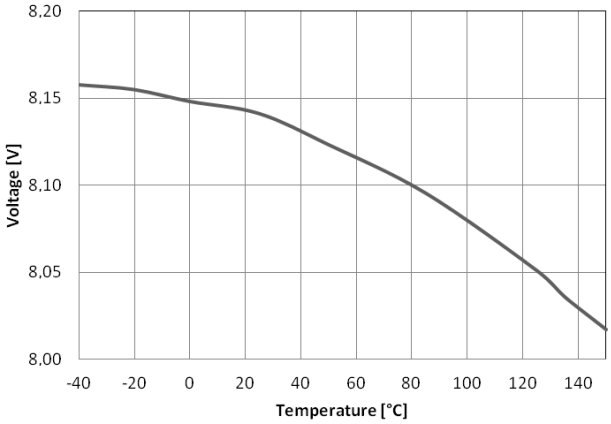


Figure 9. V_{Boff} vs. Temperature

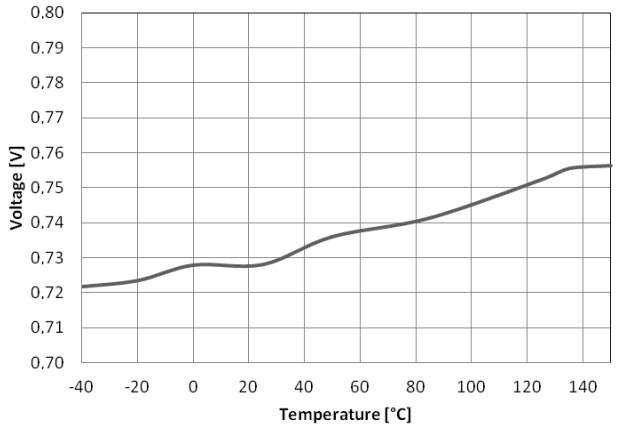


Figure 10. V_{Bhyst} vs. Temperature

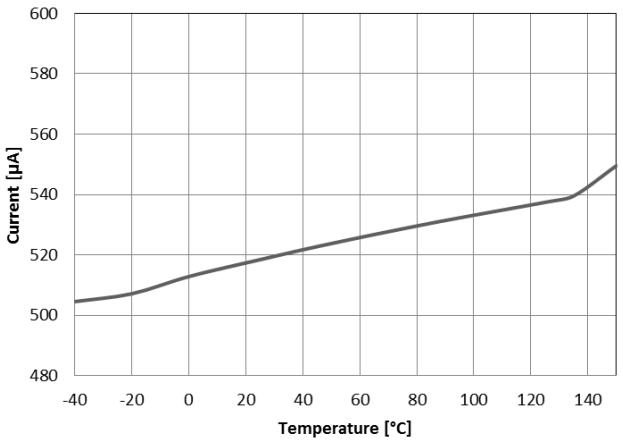


Figure 11. I_{CC1} vs. Temperature

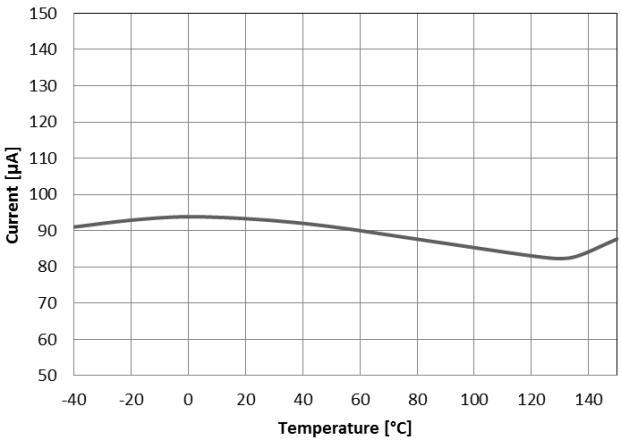


Figure 12. I_{CC2} vs. Temperature

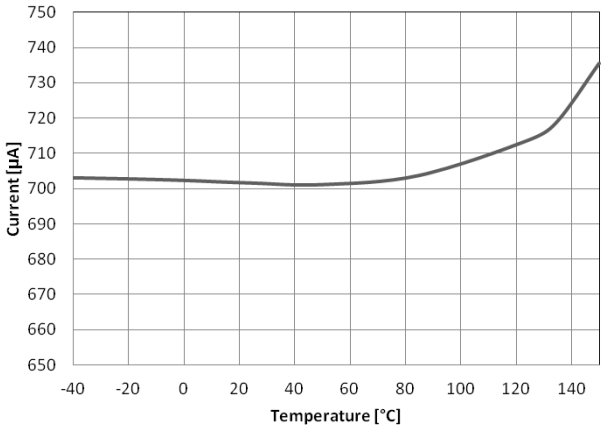


Figure 13. I_{B1} vs. Temperature

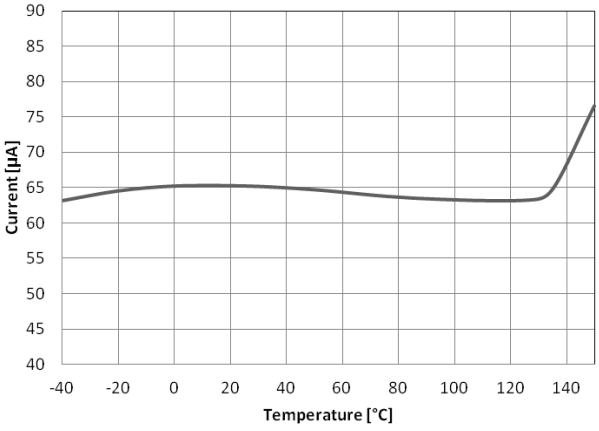


Figure 14. I_{B2} vs. Temperature

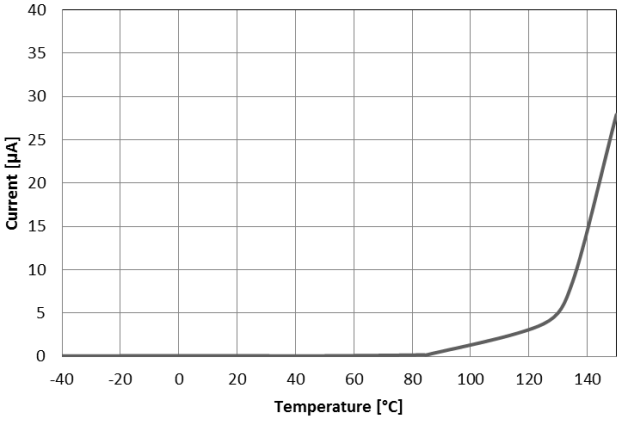


Figure 15. I_{HSleak} vs. Temperature

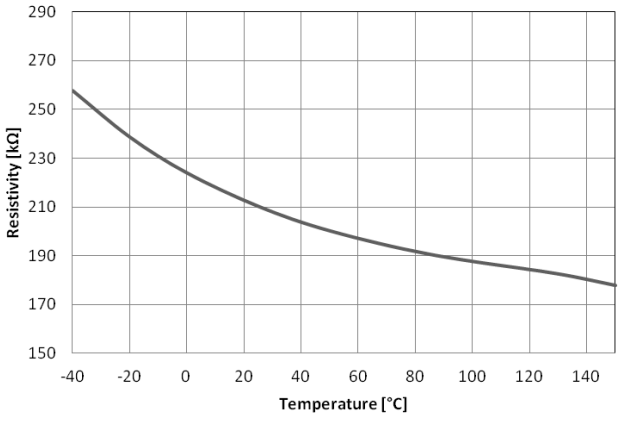


Figure 16. R_{IN} vs. Temperature

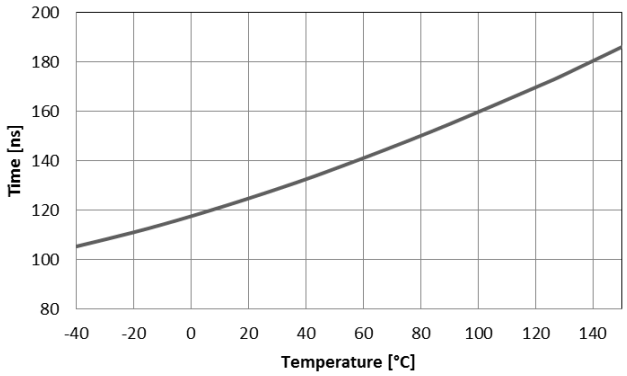


Figure 17. t_{ON} vs. Temperature

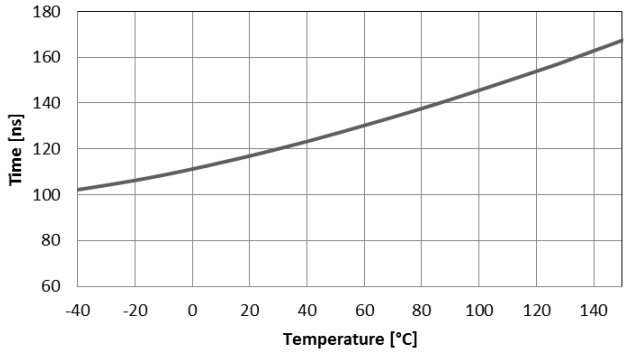


Figure 18. t_{OFF} vs. Temperature

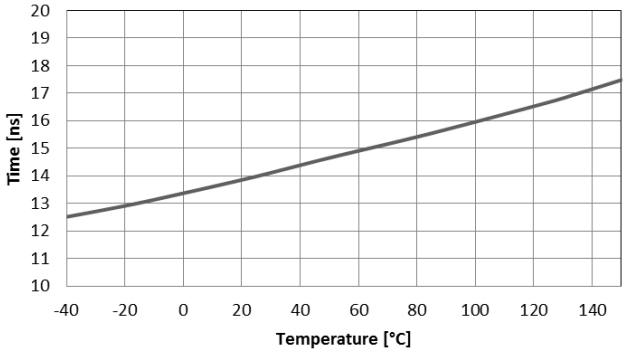


Figure 19. t_r vs. Temperature

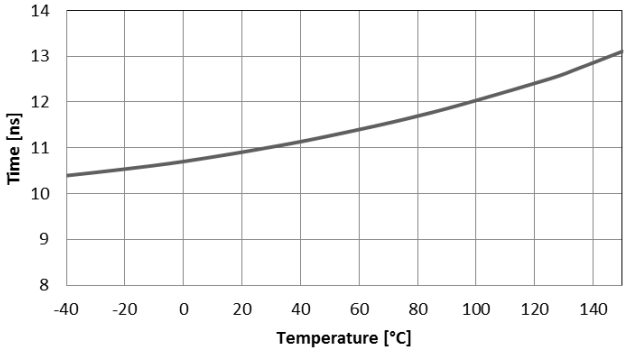


Figure 20. t_f vs. Temperature

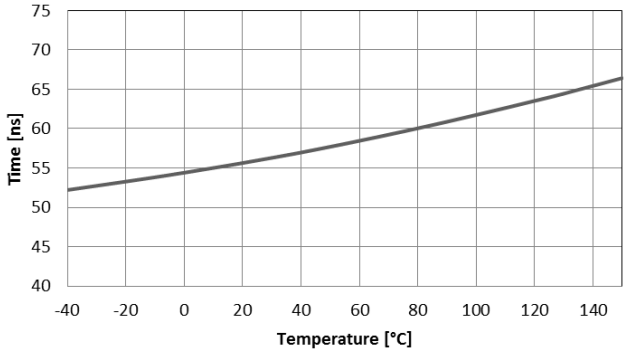


Figure 21. t_r for 10 nF Load vs. Temperature

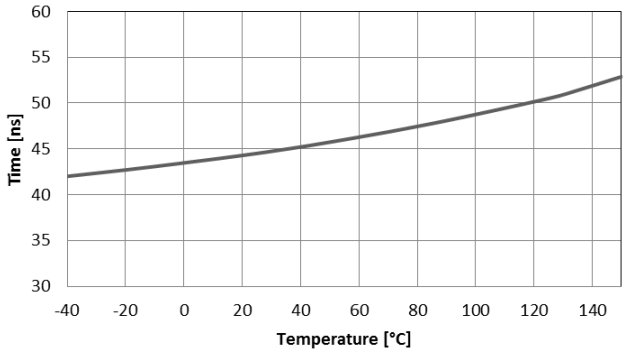


Figure 22. t_f for 10 nF Load vs. Temperature

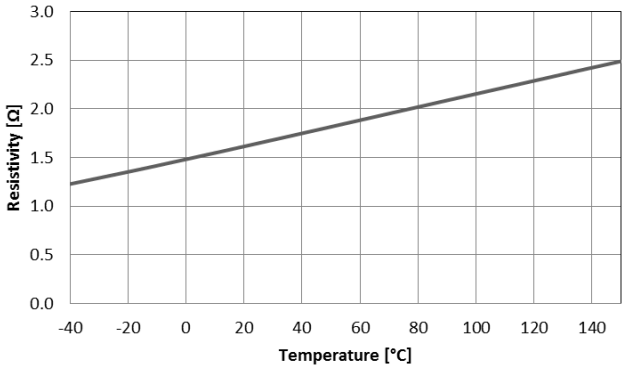


Figure 23. R_{OH} vs. Temperature

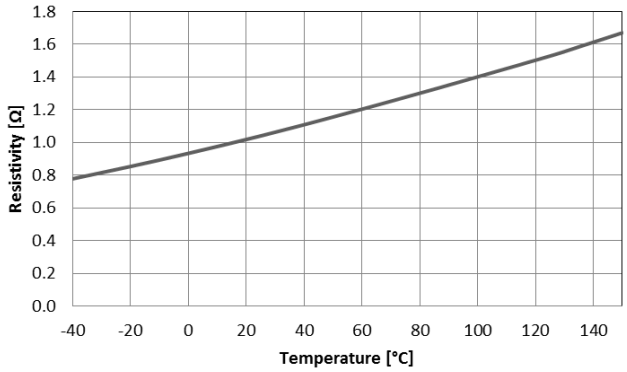


Figure 24. R_{OL} vs. Temperature

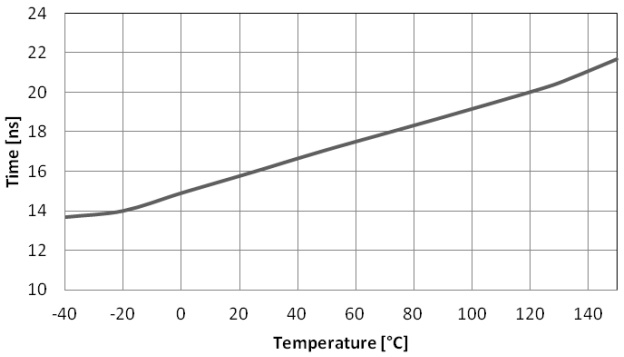


Figure 25. t_{MT} vs. Temperature

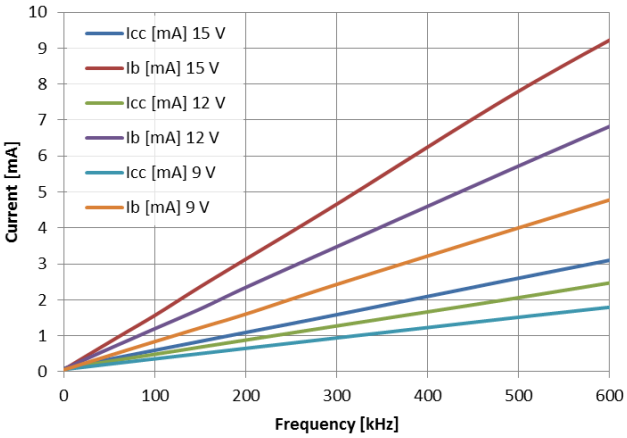
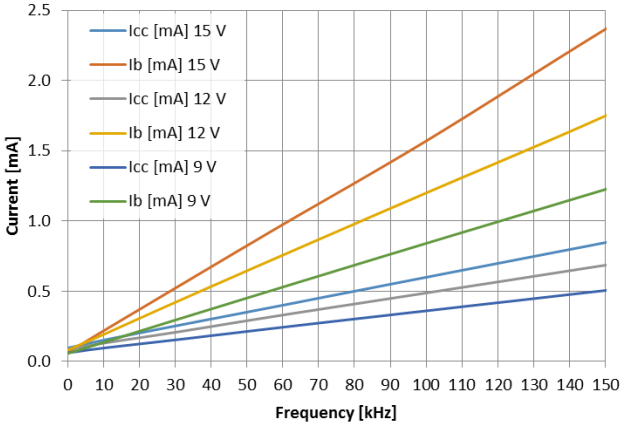


Figure 26. I_{CC} and I_B Current Consumption vs. Frequency



Detail of I_{CC} and I_B Consumption to 150 kHz

MOSFET Turn On and Turn Off Current Path

A capacitor connected from VCC (VB) to GND (HB) terminal is source of energy for charging the gate terminal of an external MOSFET(s). For better understanding of this process see Figure 27 (all voltages are related to GND (HB) pin). When there is a request from internal logic to turn on the external MOSFET, then the Q_{source} is turned on. The current starts to flow from C_{VCC} (C_{boot}), through Q_{source}, gate resistor R_g to the gate terminal of the external MOSFET (depictured by red line). The current loop is closed from external MOSFET source terminal back to the C_{VCC} (C_{boot}) capacitor. After a while the C_{GS} capacitance is fully charged so no current flows this path. When the external MOSFET going to be turned off, the internal Q_{source} is turned off first and after a short dead time Q_{sink} is turned on. Then C_{VCC} (C_{boot}) is not a source any more, the source of energy became the C_{GS} (and all capacitance connected to this terminal, like Muller capacitance). Now the current flows from gate terminal, through R_g resistor and Q_{sink} back to the MOSFET (depictured by blue line). In both cases (charging and discharging external MOSFET) there are several parasitic inductances in the path. All of them play a role during switching. In Figure 27 an influence of the inductances in some places is showed. On VCC (VB) pin a drop during turn on and turn off is observed. If too long an UVLO protection can be triggered and the driver can be turned off subsequently, which result in improper operation of the application.

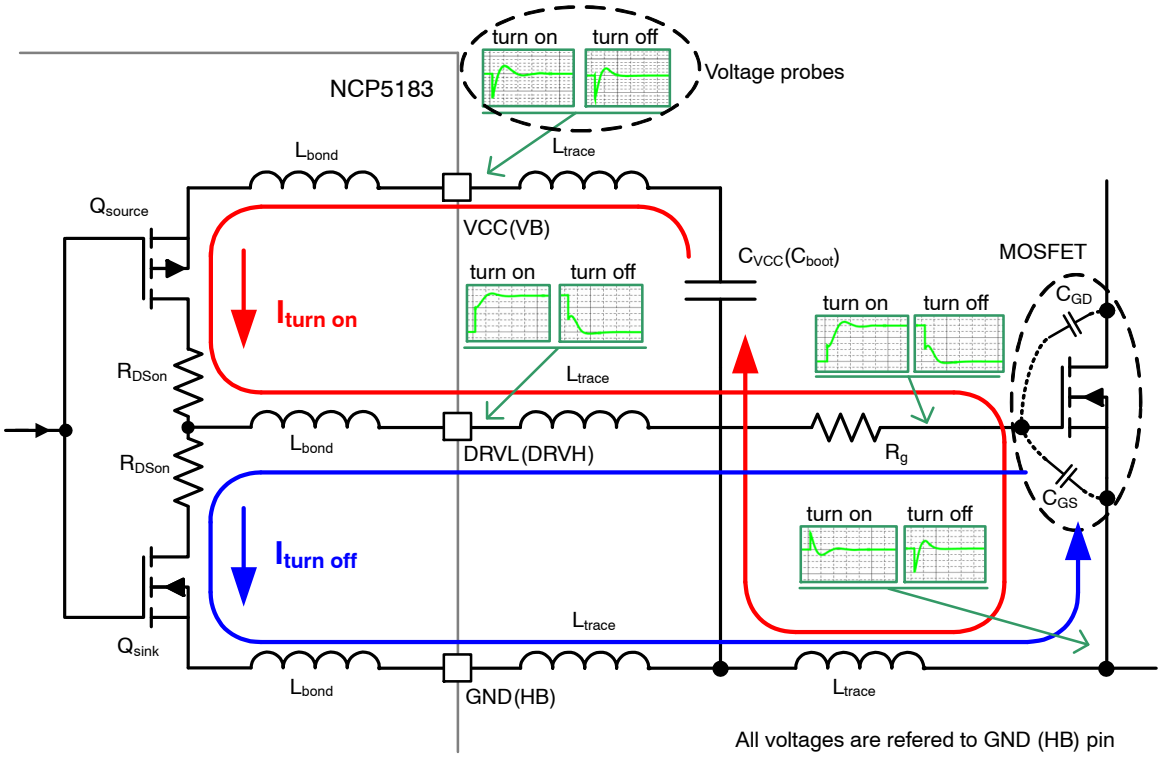


Figure 27. Equivalent Circuit of Power Switch Driver

Layout Recommendation

The NCP5183 is high speed, high current (sink/source 4.3 A/4.3 A) driver suitable for high power application. To avoid any damage and/or malfunction during switching (and/or during transients, overloads, shorts etc.) it is very important to avoid a high parasitic inductances in high current paths (see “MOSFET turn on and turn off current path” section). It is recommended to fulfill some rules in layout. One of a possible layout for the IC is depictured in Figure 28.

- Keep loop HB_pin – GND_pin – Q_LO as small as possible. This loop (parasitic inductance) has potential to increase negative spike on HB pin which can cause of malfunction or damage of HB driver. The negative voltage presented on HB pin is added to V_{CC}−V_f voltage so V_{Cboot} is increased. In extreme case the C_{boot} voltage can be so high it will reach maximum rating value which can lead to device damage.
- Keep loop VDD_pin – GND_pin – C_{VCC} as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q_LO turn on and voltage drop on VCC pin which can result in UVLO activation.
- Keep loop VB_pin – HB_pin – C_{boot} as small as possible. The IC featured high current capability driver. Any parasitic inductance in this path will result in slow Q_HI turn on and voltage drop on VB pin which can result in UVLO activation.
- Do not let high current flow through trace between GND_pin and C_{VCC} even a small parasitic inductance here will create high voltage drop if high current flows through this path. This voltage is added or subtracted from HIN and LIN signal, which results in incorrect thresholds or device damaging.
- Keep loops DRVL_pin – Q_LO – GND_pin and DRVH_pin – Q_HI – HB_pin as small as possible. A high parasitic inductance in these paths will result in slow MOSFET switching and undesired resonance on gate terminal.

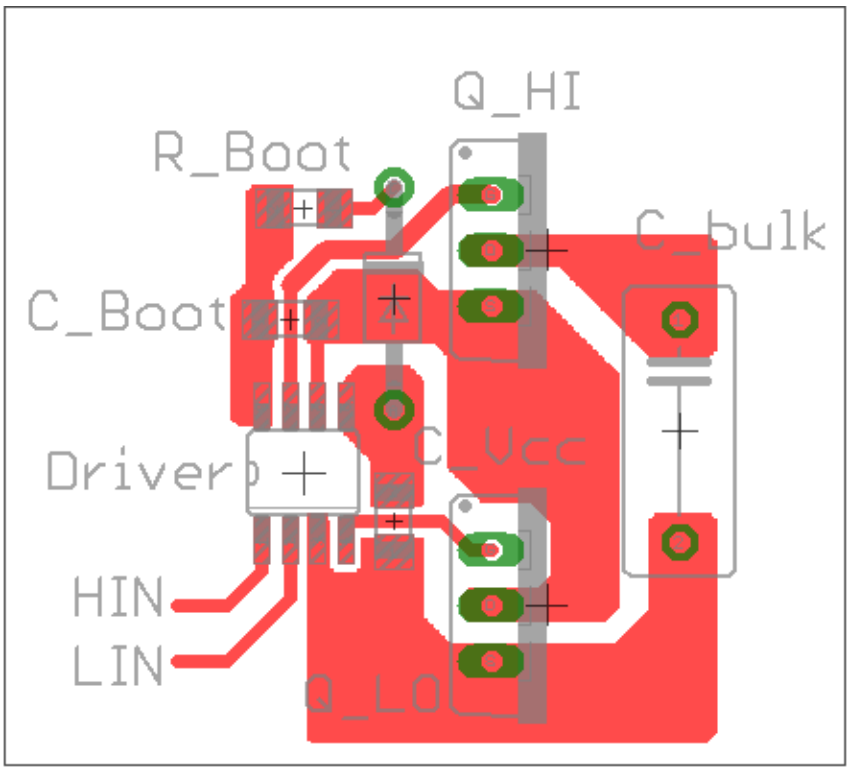


Figure 28. Recommended Layout

C_{boot} Capacitor Value Calculation

The device featured two independent 4.3 A sink and source drivers. The low side driver (DRVL) supplies a MOSFET whose source is connected to ground. The driver is powered from V_{CC} line. The high side driver (DRVH) supplies a MOSFET whose source is floating from GND to bulk voltage. The floating driver is powered from C_{boot} capacitor. The capacitor is charged only when HB pin is pulled to GND (by inductance or the low side MOSFET when turned on). If too small C_{boot} capacitor is used the high side UVLO protection can disable the high side driver which leads to improper switching.

Expected voltage on C_{boot} is depictured in Figure 29. The curves are valid for ZVS (Zero Voltage Switching) observed in LLC applications. For hard switch the curves are slightly different, but from charge on C_{boot} point of view more favorable. Under the hard switch conditions the energy to charge Q_g (from zero voltage to V_{th} of the MOSFET) is taken from V_{CC} capacitor (through an external boot strap diode) so the voltage drop on C_{boot} is smaller. For the calculation of C_{boot} value the ZVS conditions are taken account.

The switching cycle is divided into two parts, the charging (t_{charge}) and the discharging ($t_{discharge}$) of the C_{boot} capacitor. The discharging can be divided even more to discharging by floating driver current consumption I_{B2} (t_{dsIb}) and to discharging by transfering energy from C_{boot} to gate terminal of the MOSFET (t_{dsQm}). Discharging by I_{B2} becoming more dominant when driver runs at lower frequencies and/or during skip mode operation. To calculate C_{boot} value, follow these steps:

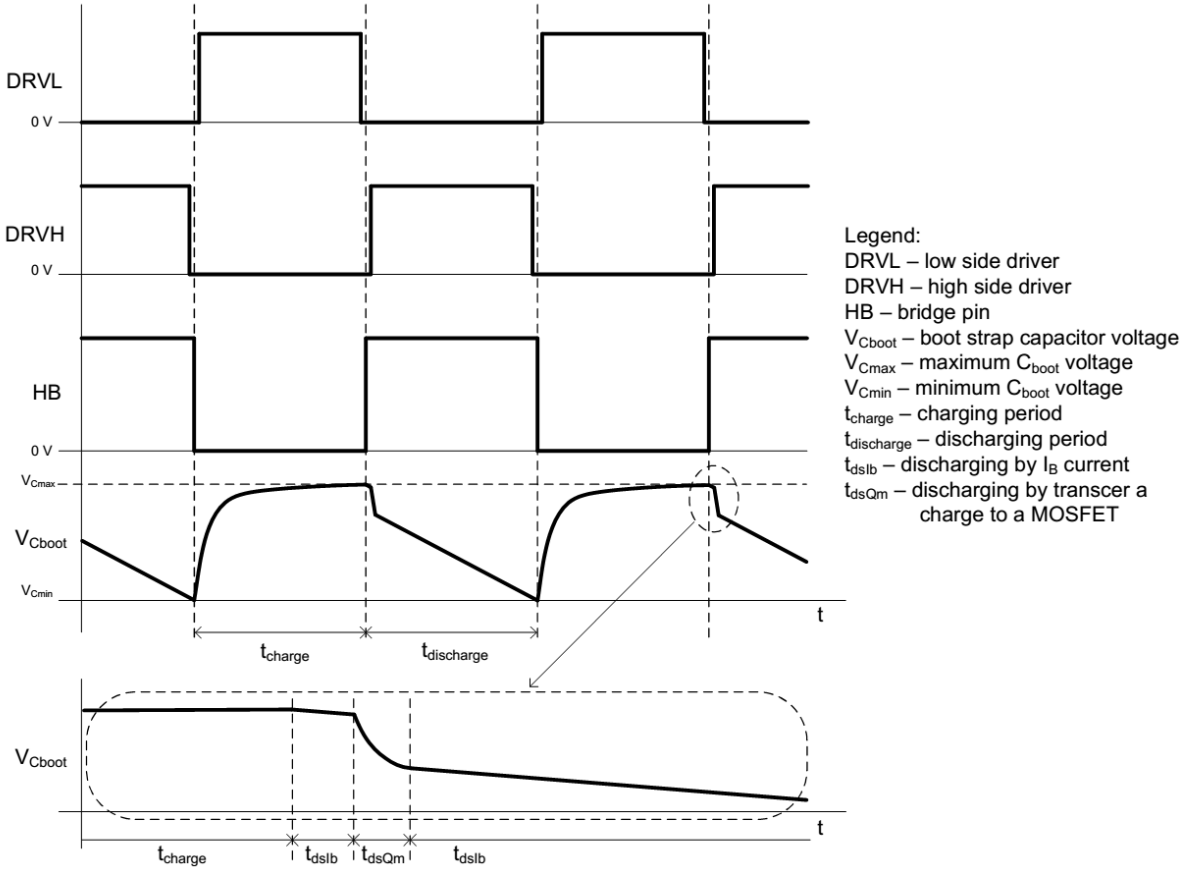


Figure 29. Boot Strap Capacitor Charging Principle

1. For example, let's have a MOSFET with Q_g = 30 nC, V_{DD} = 15 V.
2. Charge stored in C_{boot} necessary to cover the period the C_{boot} is not supplied from V_{CC} line (which is basically the period the high side MOSFET is turned on). Let's say the application is switching at 100 kHz, 50% duty cycle, which means the upper MOSFET is conductive for 5 μs. It means the C_{boot} is discharged by I_{B2} current (65 μA typ) for 5 μs, so the charge consumed by floating driver is:

$$Q_b = I_{B2} \cdot t_{discharge} = 65\mu \cdot 5\mu = 325\ pC \quad \text{(eq. 1)}$$

3. Total charge loss during one switching cycle is sum of charge to supply the high side driver and MOSFET's gate charge:

$$Q_{tot} = Q_g + Q_b = 30n + 325p = 30.3\ nC \quad \text{(eq. 2)}$$

4. Let's determine acceptable voltage ripple on C_{boot} to 1% of nominal value, which is 150 mV. To cover charge losses from eq. 2

$$C_{boot} = \frac{Q_{tot}}{V_{ripple}} = \frac{30.3n}{0.15} = 202\ nF \quad \text{(eq. 3)}$$

It is recommended to increase the value as consumption and gate charge are temperature and voltage dependent, so let's choose a capacitor 330 nF in this case.

R_{boot} Resistor Value Calculation

To keep the application running properly, it is necessary to charge the C_{boot} again. This is done by external diode from V_{CC} line to VB pin. In serial with the diode a resistor is placed to reduce the current peaks from V_{CC} line. The resistor value selection is critical for proper function of the high side driver. If too small high current peaks are drown from V_{CC} line, if too high the capacitor will not be charged to appropriate level and the high side driver can be disabled by internal UVLO protection.

First of all keep in mind the capacitor is charged through the external boot strap diode, so it can be charged to a maximum voltage level of $V_{CC} - V_f$. The resistor value is calculated using this equation:

$$R_{boot} = \frac{t_{charge}}{C_{boot} \cdot \ln\left(\frac{V_{max} - V_{Cmin}}{V_{max} - V_{Cmax}}\right)} = \frac{5\mu}{330n \cdot \ln\left(\frac{14.4 - 14.2}{14.4 - 14.35}\right)} \cong$$

$$\cong 11\ \Omega \quad \text{(eq. 4)}$$

Where:

t_{charge} – time period the C_{boot} is being charged, usually the period the low side MOSFET is turned on

C_{boot} – boot strap capacitor value

V_{max} – maximum voltage the C_{boot} capacitor can be theoretically charged to. Usually the $V_{CC} - V_f$. The V_f is forward voltage of used diode.

V_{Cmin} –the voltage level the capacitor is charged from

V_{Cmax} –the voltage level the capacitor is charged to. It is necessary to determine the target voltage for charging, because in theory, when a capacitor is charged from a voltage source through a resistor, the capacitor can never reach the voltage of the source. In this particular case a 50 mV difference (between the voltage behind the diode and V_{Cmax}) is used.

The resistor value obtained from eq. 4 does not count with the quiescent current I_{B2} of the high side driver. This current will create another voltage drop of:

$$V_{IB2_drop} = R_{boot} \cdot I_{B2} = 11 \cdot 65\mu \cong 0.7\ mV \quad \text{(eq. 5)}$$

The current consumed by high side driver will be higher, because the I_{B2} is valid when the device is not switching. While switching, losses by charging and discharging internal transistors as well as the level shifters will be added. This current will increase with frequency.

The additional 0.7 mV drop will be added to V_{Cmax} value. The additional 0.7 mV drop can be either accepted or the R_{boot} value can be recalculated to eliminate this additional drop.

The resistor R_{boot} calculated in eq. 4 is valid under steady state conditions. During start and/or skip operation the starting point voltage value is different (lower) and it takes more time to charge the boot strap capacitor. More over it is not counted with temperature and voltage variability during normal operation or the dynamic resistance of the boot strap diode (approximately 0.34 Ω for MURA160). From these reasons the resistor value should be decreased especially with respect to skip operation.

Boot strap resistor losses calculation.

$$P_{Rboot} \cong Q_{tot} \cdot V_{Cmax} \cdot f = 30.3n \cdot 14.4 \cdot 100k \cong 43.6\ mW \quad \text{(eq. 6)}$$

Boot strap diode losses calculation.

$$P_{Dboot} \cong Q_{tot} \cdot V_f \cdot f = 30.3n \cdot 0.6 \cdot 100k \cong 1.8\ mW \quad \text{(eq. 7)}$$

Please keep in mind the value is temperature and voltage dependent. Especially C_{boot} voltage can be higher than calculated value. See "Layout recommendation" section for more details.

Total Power Dissipation

The NCP5183 is suitable to drive high input capacitance MOSFET, from this reason it is equipped with high current capability drivers. Power dissipation on the die, especially at high frequencies can be limiting factor for using this driver. It is important to not exceed maximum junction temperature (listed in absolute maximum ratings table) in any cases. To calculate approximate power losses follow these steps:

1. Power loss of device (except drivers) while switching at appropriate frequency (see Figure 26) is equal to

$$P_{logic} = P_{HS} + P_{LS} = (V_{boot} \cdot I_{B2SW}) + (V_{CC} \cdot I_{CC2SW}) =$$

$$= (14.4 \cdot 1.6m) + (15 \cdot 0.6m) \cong 32.1\ mW \quad \text{(eq. 8)}$$

2. Power loss of drivers

$$P_{drivers} = \left((Q_g \cdot V_{boot}) + (Q_g \cdot V_{CC})\right) \cdot f =$$

$$= ((30n \cdot 14.4) + (30n \cdot 15)) \cdot 100k \cong 88\ mW \quad \text{(eq. 9)}$$

3. Total power losses

$$P_{total} = P_{logic} + P_{drivers} = 32.1m + 88m \cong 120\ mW \quad \text{(eq. 10)}$$

4. Junction temperature increase for calculated power loss

$$t_J = R_{tJa} \cdot P_{total} = 183 \cdot 0.12 \cong 22\ K \quad \text{(eq. 11)}$$

The temperature calculated in eq. 11 is the value which has to be added to ambient temperature. In case the ambient temperature is 30°C, the junction temperature will be 52°C.

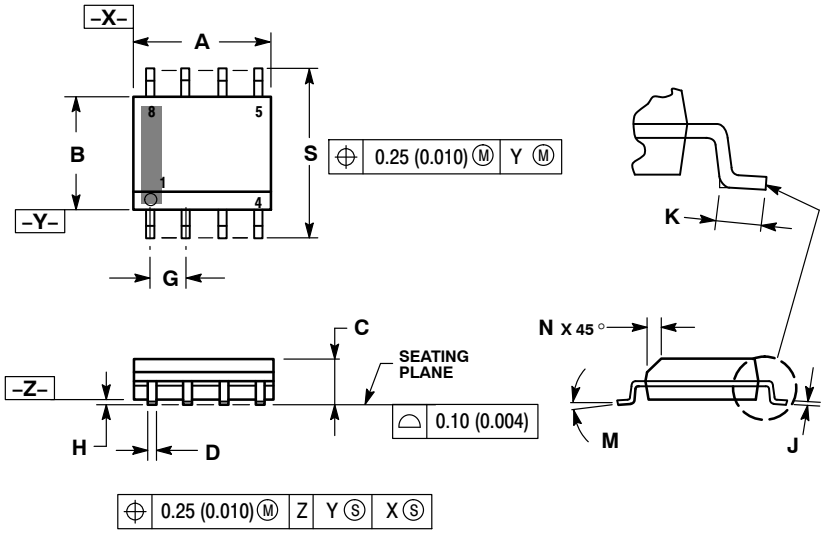
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

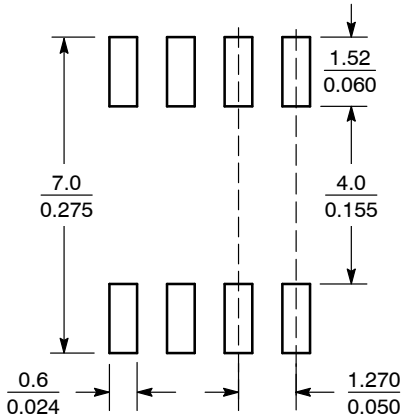
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

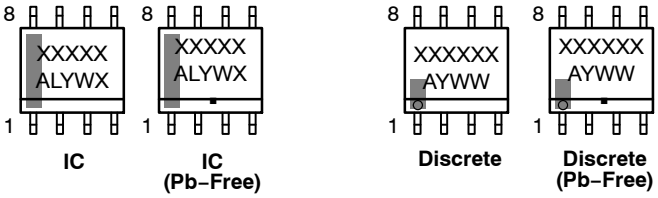
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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